National Interface Databook

1996

National Semiconductor

400045

National Interface Databook

LVDS Circuits
Bus Circuits
Data Transmission Circuits
System Design Guide

INTERFACE
DATABOOK

1996 Edition

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Introduction

Since its creation in 1973, National Semiconductor's Interface design and production teams have continuously produced technically advanced products unparalleled in the semiconductor industry.

Growing from a line of early drivers and receivers, which pioneered the introduction of the TRI-STATE® function, National Semiconductor's Interface product line today is the most comprehensive available—with over 175 devices in a variety of product categories. These Interface devices support both cable and backplane applications.

Based on its advance design and process capabilities, National's Interface product line includes:

- The industry's first CMOS TIA/EIA-232 (RS-232) Drivers and Receivers
- The industry's first CMOS TIA/EIA-422 (RS-422) Drivers and Receivers
- The industry's first TIA/EIA-485 (RS-485) type Military Qualified (883) Transceivers, Drivers and Receivers
- The industry's first TIA/EIA-485 (RS-485) Quad Transceiver
- The industry's first 3.3V powered RS-232 3 Driver X 5 Receiver Device for Laptop and Notebook Applications
- The industry's first Trapezoidal™ Bus Transceiver
- The industry's first BTL (Backplane Transceiver Logic) Transceivers
- The industry's first IEEE 1194 compliant BTL devices
- The industry's first LVDS—Low Voltage Differential Signaling Quad Drivers and Receivers for applications requiring ultra low power dissipation and switching rates exceeding 155 Mbps
- The industry's first FPD (Flat Panel Display) Link Chipsets using LVDS

In addition to the detailed product datasheets, this databook includes the following documents to speed component selection and for technical reference: Selection Guides, Cross References, Package Drawings, Modeling Information, System Considerations, and over 50 application notes devoted solely to the topic of Data Transmission over cables and backplanes.

For applications support or product information on National Semiconductor's Interface Products, please contact the National Support Center in your area (listed on the back cover of this book). Product line applications may be reached directly at:

1-408-721-8500 (USA)

Interface Applications Hotline

National Semiconductor

Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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***Boldface denotes new product Introduction and Application Notes.**

Cross Reference for Related Interface/Bus Products

(Device Type/Family to National Databook Title)

Device Type/ Family	Databook Title
Octal Buffer/Line Driver Octal Bidirectional Transceivers 244/245 Function	Advanced BiCMOS Logic (ABT, BiCMOS, LV, . . .) Databook Advanced Bipolar Logic (FAST®, FASTr™, ALS, ...) Databook Crossvolt Low Voltage Series Databook FACT™ Advanced CMOS Logic Databook
ECL Line Drivers and Receivers	F100K ECL Logic Databook
Display Drivers (LED/LCD/Dot-Bar) Power/Peripheral Drivers	Application Specific Analog Products Databook
Ethernet® Drivers	Ethernet Databook
IBM® 3270 Devices	IBM Data Communications Handbook
FDDI	FDDI Databook
Package Drawings	Packaging Databook

For a complete listing of all of National's Databooks and Handbooks, please refer to the "Bookshelf" in Section 17 of this databook.

Section 1

Line Drivers and Receivers Introduction

Section 1 Contents

National Semiconductor

Line Drivers and Receivers Selection Guide

The common purpose of transmission line drivers and receivers is to transmit data quickly and reliably through a variety of environments over electrically long distances. This task is complicated by the fact that externally introduced noise and ground shifts can severely degrade the data.

The connection between two elements in a system should be considered a transmission line if the transmitted signal takes longer than half its rise or fall time to travel from the driver to the receiver.

The Electronics Industry Association (EIA) and the Telecommunications Industry Association (TIA) have developed several standards to simplify the interface in data communications systems. Previously, EIA labeled the standards with the prefix "RS", which stood for recommended standard. This has been deleted and replaced with TIA/EIA, to help identify the standardizing organizations. The letter suffix represents the revision level of the standard. For example TIA/EIA-232-E denotes the fifth revision of RS-232.

All new and revised standards (EIA, EIA/TIA, and TIA/EIA) will adopt the new prefix nomenclature of TIA/EIA. Existing standards utilize the prefix that was current at the time the standard was balloted (approved). This includes the familiar RS, EIA, and EIA/TIA prefix. Looking forward, this selection guide adopts the TIA/EIA prefix for all TIA-EIA data transmission standards.

Single-Ended Data Transmission

In data processing systems today there are two basic means of communicating between components. One method is single-ended, which uses only one signal line for data transmission, and the other is differential, which uses two signal lines.

TIA/EIA-232-E (RS-232)

The first of these, "RS-232", was introduced in 1962 and has been widely used throughout the industry. TIA/EIA-232-E was developed for single-ended data transmission at relatively slow data rates (20 kbps) over short distances (typically up to ~50 ft.).

TIA/EIA-423-B (RS-423)

With the need to transmit data faster and over longer distances, TIA/EIA-423-B, a newer standard for single-ended applications, was established. TIA/EIA-423-B extends the maximum data rate to 100 kbps (up to 30 ft.) and the maximum distance to 4000 feet (up to 1 kbps). TIA/EIA-423-B also requires high impedance driver outputs with power off to not load the transmission line.

Differential Data Transmission

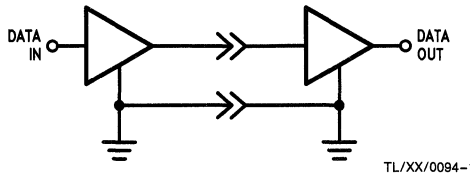
When transmitting at very high data rates, over long distances and through noisy environments, single-ended transmission is often inadequate. In these applications, differential data transmission offers superior performance. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common mode voltages on the transmission line.

TIA/EIA-422-B (RS-422)

TIA/EIA-422-B was defined by the EIA for this purpose and allows data rates up to 10 Mbps (up to 40 ft.) and line lengths up to 4000 feet (up to 100 kbps).

Drivers designed to meet this standard are well suited for party-line type applications where only one driver is connected to, and transmits on, a bus and up to 10 receivers can receive the data. While a party-line type of application has many uses, TIA/EIA-422-B devices cannot be used to construct a truly multipoint bus. A multipoint bus consists of multiple drivers and receivers connected to a single bus, and any one of them can transmit or receive data.

TIA/EIA-232-E Application



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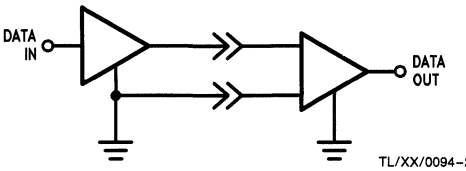
TIA/EIA-423-B Application



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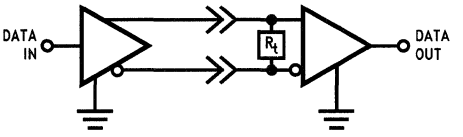
TIA/EIA-422-B Application



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Differential Data Transmission (Continued)

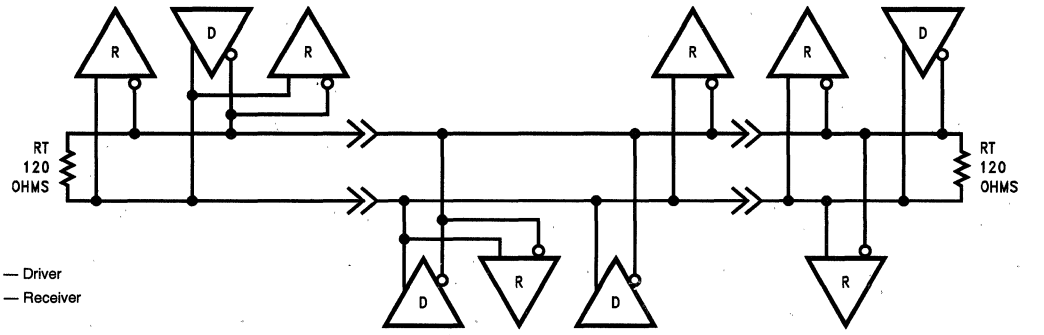
TIA/EIA-485 (RS-485)

To meet the need for truly multipoint communications, the EIA established TIA/EIA-485 in 1983. TIA/EIA-485 meets all the requirements of TIA/EIA-422-B, but in addition, this new standard allows up to 32 drivers and 32 receivers to be connected to a single bus—thus allowing a truly multipoint bus to be constructed.

The key features of TIA/EIA-485:

- Implements a truly multipoint bus consisting of up to 32 drivers and 32 receivers (32 unit loads).
- An extended common-mode range for both drivers and receivers in TRI-STATE and with power off (−7V to +12V).
- Drivers can withstand bus contention and bus faults.

TIA/EIA-485 Application



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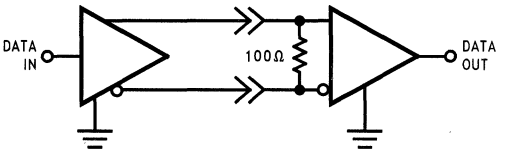
TIA/EIA-644 (LVDS)

To meet the need for a very high speed interface, the TIA/EIA committee TR30.2 established TIA/EIA-644 in 1995. This electrical standard generically known as LVDS (Low Voltage Differential Signaling) provides all the benefits of differential data transmission and is capable of operating at data rates up to 655 Mb/s.

TIA/EIA-644 Application



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National Semiconductor produces a variety of drivers, receivers, and transceivers for these popular transmission standards and numerous other data transmission requirements.

Shown below are tables that highlight key aspects of the TIA/EIA Standards. More detailed comparisons can be found in the various application notes located in Section 14 of this databook.

Single-Ended Data Transmission Standards

Specification		TIA/EIA-232-E	TIA/EIA-423-B	TIA/EIA-562
Number of Drivers and Receivers Allowed on One Line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 1 Receiver
Maximum Cable Length		~ 50 feet	4000 feet	—— ——
Maximum Data Rate		20 kb/s	100 kb/s	64 kb/s
Driver Output Maximum Voltage		±25V	±6V	±13.2V
Driver Output Signal Level	Loaded	± 5V to ± 15V	±3.6V	±3.7V
	Unloaded	±25V	±6V	±13.2V
Driver Load Impedance		3 kΩ to 7 kΩ	≥450Ω	3 kΩ to 7 kΩ
Maximum Driver Output Current (High Impedance State)	Power On	—— ——	—— ——	—— ——
	Power Off	±6.6 mA (± 2V)	±100 μA	±6.6 mA (± 2V)
Slew Rate		30 V/μs max	Controls Provided	—— ——
Receiver Input Voltage Range		±15V	±12V	±15V
Receiver Input Sensitivity		±3V	±200 mV	± 3V
Receiver Input Resistance		3 kΩ to 7 kΩ	4 kΩ min	3 kΩ to 7 kΩ

Differential Data Transmission Standards

Specification		TIA/EIA-422-B	TIA/EIA-485	TIA/EIA-644
Number of Drivers and Receivers Allowed on One Line		1 Driver, 10 Receivers	32 Drivers, 32 Receivers	1 Driver, 1 Receiver
Maximum Cable Length		4000 feet	4000 feet	—— ——
Maximum Data Rate		10 Mb/s	10 Mb/s	655 Mb/s
Driver Output Maximum Voltage		−0.25V to +6V	−7V to +12V	±450 mV
Driver Output Signal Level	Loaded	±2V	±1.5V	±250 mV
	Unloaded	±10V	±6V	±450 mV
Driver Load Impedance		100Ω	54Ω	100Ω
Maximum Driver Output Current (High Impedance State)	Power On	—— ——	± 100 μA	—— ——
	Power Off	±100 μA	±100 μA	—— ——
Slew Rate		—— ——	—— ——	—— ——
Receiver Input Voltage Range		−10V to +10V	−7V to +12V	GND to +2.4V
Receiver Input Sensitivity		±200 mV	± 200 mV	±100 mV
Receiver Input Resistance		4 kΩ min	~ ≥ 12 kΩ	High Z

See TIA/EIA Standards for exact conditons. For reference, the "as published" nomenclature of the TIA/EIA Standards are listed below:

EIA/TIA-232-E-1991
TIA/EIA-422-B-1995
TIA/EIA-423-B-1995
EIA RS-485-1983
EIA/TIA-562-1989
TIA/EIA-644-1996
TIA/EIA-644-1995

TIA/EIA-232 UNBALANCED LINE DRIVERS

Device Number			Number of Drivers	Power Supplies V_{CC}/V_{EE} (V)	Max I_{CC} (mA)	Max I_{EE} (mA)	Typical I_O (mA)	Min V_O (V)	Typical Prop. Delay (ns)	Slew Rate Control	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military											
0°C to +70°C	−40°C to +85°C	−55°C to +125°C											
DS1488			4	±9 to ±15	25	−23	±6	±6/±9	230	External Cap.	N, J, M		2-71
DS14C88	DS14C88T		4	±5 to ±12	0.5	−0.06	±10	±3/±9	1500	Internal	N, J, M	Low Power CMOS	2-67
DS75150			2	±12	22	−20	±10	±5	60	External Cap.	N, M		2-82
		DS9616HM	3	±12	25	−25	—	±5	—	External Cap.	J, E		2-91

TIA/EIA-232 UNBALANCED RECEIVERS

Device Number			Number of Receivers	Power Supply V_{CC} (V)	Max I_{CC} (mA)	Typical Prop. Delay (ns)	Response Control	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military								
0°C to +70°C	−40°C to +85°C	−55°C to +125°C								
DS1489			4	5	26	28	External Cap.	N, J, M	Noise Filter, Adjustable Thresholds	2-78
DS1489A			4	5	26	28	External Cap.	N, M	Noise Filter, Adjustable Thresholds	2-78
DS14C89A	DS14C89AT		4	5	0.9/2.0	3500	Internal	N, J, M	Low Power CMOS Device	2-75
DS75154			4	5 or 12	35/40	22	—	N, M		2-86
		DS9627M	2	±12	18/−16		—	J		2-95

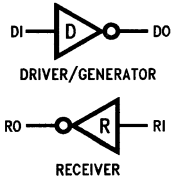
TIA/EIA-232 UNBALANCED LINE DRIVERS AND RECEIVERS

Device Number			Number of Drivers	Number of Receivers	Number of External Caps	Nom. Cap. (μF)	Shutdown Mode	Rec. Output TRI-STATE	Power Supply (V)	Max I_{CC} (mA)	Packages	Page #
Commercial	Industrial	Military										
0°C to +70°C	−40°C to +85°C	−55°C to +125°C										
DS14185			3	5	—	—	No	No	+5, ±9–13.2	30/22/−28	WM	2-3
DS14196			5	3	—	—	No	No	+5, ±9–13.2		WM	2-10
DS14C202	DS14C202T		2	2	4	0.1	No	No	+5		M, N, WM	2-15
DS14C232C	DS14C232T	DS14C232	2	2	4	1.0	No	No	+5	3.0	M, N, WM	2-16
DS14C237	DS14C237T		5	3	4	1.0	No	No	+5	10	N, WM	2-25
DS14C238	DS14C238T		4	4	4	1.0	No	No	+5	10	N, WM	2-29
DS14C239	DS14C239T		3	5	2	1.0	No	Yes	+5, +7.5–+13.2	TBD	N, WM	2-34
DS14C241	DS14C241T		4	5	4	1.0	Yes	Yes	+5	10	WM	2-39
DS14C335	DS14C335T		3	5	5	0.47	Yes	No	+3.3	20	MSA	2-46
DS14C535	DS14C535T		3	5	4	0.1	Yes	No	+5	12	MSA	2-55
DS14C561*			4	5	4	1.0	Yes	Yes	+3.3	6	WM	2-62

Characteristics of an TIA/EIA-232-E Device:

DRIVER/GENERATOR:
Minimum driver high output voltage with 3 kΩ load — +5V
Minimum driver low output voltage with 3 kΩ load — −5V
Power off driver output resistance (V_O = ±2V) — ≥300Ω
Maximum data rate — 20 kb/s (Standard limit, many devices operate at higher rates)
Maximum driver slew rate — ≤30 V/μs
See TIA/EIA Standard TIA/EIA-232-E for exact conditions.

RECEIVERS:
Receiver input voltage range — ±15V
Receiver input sensitivity — ±3V
Receiver input resistance — >3 kΩ and <7 kΩ



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***Note:** DS14C561 is 232 compatible only, and conforms to TIA/EIA-562.
See Datasheets for Complete Specifications.

TIA/EIA-422 BALANCED LINE DRIVERS

Device Number			Number of Drivers	Power Supply V_{CC} (V)	Min V_{OH} (V)	Rated I_{OH} (mA)	Max V_{OL} (V)	Rated I_{OL} (mA)	Max I_{CC} (mA)	Typ Prop. Delay (ns)	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military											
0°C to +70°C	−40°C to +85°C	−55°C to +125°C											
	DS26C31T	DS26C31M	4	5	2.5	−20	0.5	20	0.5	6	N, J, M, E, W	Low Power	3-10
DS26F31C		DS26F31M	4	5	2.5	−20	0.5	20	50	10	J, E, W		3-19
DS26LS31C		DS26LS31M	4	5	2.5	−20	0.5	20	60	10	N, J, M, W		3-22
	DS26LV31T		4	3.3							N, M		3-18
DS3487			4	5	2.5	−20	0.5	48	80	10	N, M		3-65
	DS34C87T		4	5	2.5	−20	0.5	48	0.5	6	N, J, M	Low Power	3-55
DS34F87		DS35F87	4	5	2.5	−20	0.5	48	50	—	N, J		3-61
	DS34LV87T		4	3.3							N, M		3-60
DS3691		DS1691A	2	5 or ±5	—	—	—	—	30	120	N, J, M, V	422 or 423	3-3
DS9638C		DS9638M	2	5	2	−40	0.5	40	65	10	N, J, M		3-181
	DS89C387T		12	5	2	−20	0.5	48	1.5	6	MEA	SSOP Package	3-163

Characteristics of an TIA/EIA-422-B Line Driver:

Minimum driver output voltage with 100Ω test termination load — Greater than |2V|

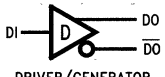
Driver output resistance — <100Ω

Driver output short circuit current (V_O = 0V) — ≤150 mA

Driver power off current (V_O = −250 mV to +6V) — ≤|100 μA|

Typical maximum data rate — 10 Mb/s

See TIA/EIA Standard TIA/EIA-422-B for exact conditions.



DRIVER/GENERATOR

TL/XX/0094–6

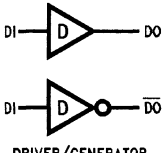
See Datasheets for Complete Specifications

TIA/EIA-423 UNBALANCED LINE DRIVERS

Device Number		Number of Drivers per Package	Power Supplies V_{CC}/V_{EE} (V)	Max Supply Current I_{CC}/I_{EE} (mA)	Min V_O (V)	Typical I_{OS} (mA)	Typical Prop. Delay (ns)	Slew Rate Control	Packages	Comments and Special Features	Page #
Commercial	Military										
0°C to +70°C	−55°C to +125°C										
DS3691	DS1691A	4	±5	30/−22	±4	±80	180	External Cap.	N, J, M, V	422 or 423	3-3
DS9636AC	DS9636A/M	2	±12	18/−18	±4	±60	—	External Res.	N, J	One Resistor Sets Slew Rate	3-172

Characteristics of an TIA/EIA-423-B line driver:

Minimum driver output voltage with 450Ω load — ≥|3.6V|
Driver output resistance — <50Ω
Driver output short circuit current (V_O = 0V) — ≤|150 mA|
Maximum driver output voltage — ±10V
Driver power off current (V_O = ±6V) — ≤|100 μA|
Typical maximum data rate — 100 kbps
See TIA/EIA Standard TIA/EIA-423-B for exact conditions.



DRIVER/GENERATOR

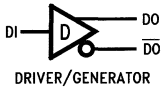
TL/XX/0094–7

See Datasheets for Complete Specifications

TIA/EIA-422/3 LINE DRIVER RECEIVER DEVICES

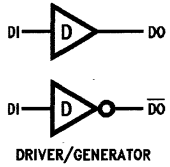
Device Number			Number of Drivers	Number of Receivers	Power Supply (V)	Max Power Supply Current (mA)	Typical Driver Prop. Delay (ns)	Typical Receiver Prop. Delay (ns)	Packages	Standard	Comments and Special Features	Page #
Commercial	Industrial	Military										
0°C to +70°C	−40°C to +85°C	−55°C to +125°C										
DS8921			1	1	5	35	10	14	N, M	422		3-87
DS8921A	DS8921AT		1	1	5	35	10	14	N, J, M	422	Low Skew	3-87
	DS89C21T		1	1	5	6	10		N, M	422	Low Power	3-92
	DS89LV21T		1	1	3.3					~422		3-97
DS8922			2	2	5	78	12	12	N, M	422		3-102
DS8922A			2	2	5	78	12	12	N, M	422		3-102
DS8923			2	2	5	78	12	12	N, M	422		3-102
DS8923A			2	2	5	78	12	12	N, M	422		3-102
DS8925*			2	3	±5	65/−15	150	33	M	422/3	Local Talk™ XCVR	3-112
DS8926*			2	3	±5				M	422/3	High Speed Rec. (8925)	3-126
DS8933			2	1	±5	30/−10	160	29	M	~423	V.FAST XCVR	3-127
DS8934			5	3	±5	65/−20	175	29	WM	~423	V.FAST XCVR	3-134
DS8935*			2	3	±5	65/−15	150	33	WM	422/3	Local Talk XCVR	3-141
DS8936*			2	3	±5				WM	422/3	High Speed Rec. (8935)	3-153

***Note:** 1 Differential Driver, 1 Single-ended Driver, 1 Differential Receiver, and 2 Single-ended Receivers.



DRIVER/GENERATOR

TL/XX/0094–6



DRIVER/GENERATOR

TL/XX/0094–7

RECEIVER

TL/XX/0094–8

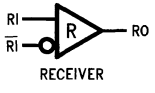
TIA/EIA-422 and TIA/EIA-423 BALANCED RECEIVERS

Device Number			Number of Receivers	Power Supply V_{CC} (V)	Max I_{CC} (mA)	Typ Prop. Delay (ns)	Max VCM (V)	Output Stage	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military									
0°C to +70°C	−40°C to +85°C	−55°C to +125°C									
	DS26C32AT	DS26C32AM	4	5	23/25	19	±14	TRI-STATE	N, J, M, W, E	Low Power CMOS Device	3-26
DS26F32C		DS26F32M	4	5	50	15	±25	TRI-STATE	W, J, E		3-34
DS26LS32C		DS26LS32M	4	5	70	17	±25	TRI-STATE	N, J, M, W		3-38
DS26LS32AC			4	5	70	23	±25	TRI-STATE	N, M	Failsafe Feature	3-38
	DS26LV32AT		4	3.3			±10	TRI-STATE	N, M		3-33
	DS34C86T		4	5	23	19	±14	TRI-STATE	N, J, M	Low Power CMOS Device	3-41
DS34F86		DS35F86	4	5	50	15	±15	TRI-STATE	J		3-47
	DS34LV86T		4	3.3			±10	TRI-STATE	N, M		3-46
DS3486			4	5	85	19	±25	TRI-STATE	N, J, M		3-51
DS88C20		DS78C20	2	5 to 15	15/30	100	±25	Strobe	N, J	Response Control	3-68
DS88C120		DS78C120	2	5 to 15	15/30	100	±25	Strobe	N, J	Response Control, Failsafe	3-72
DS88LS120		DS78LS120	2	5	16	38	±25	Strobe	N, J, W		3-80
DS9637AC		DS9637AM	2	5	50	15	±15	—	N, J, M		3-176
DS9639AC			2	5	50	55	±15	—	N		3-185
	DS89C386T		12	5	69	19	±14	TRI-STATE	MEA	SSOP Package	3-154

Characteristics of an TIA/EIA-422-B / 423-B Receiver:

Receiver common mode voltage range — ±7V
Receiver sensitivity over ±10V common mode — ±200 mV
Maximum differential input voltage — ±12V
Minimum receiver input impedance — 4 kΩ

See TIA/EIA Standard TIA/EIA-422-B or TIA/EIA-423-B for exact conditions.



TL/XX/0094–8

See Datasheets for Complete Specifications

TIA/EIA-485 BALANCED LINE DRIVERS, RECEIVERS AND TRANSCEIVERS

Device Number			Number of Drivers	Number of Receivers	Max I_{CC} (mA)	Typ. Driver Prop. Delay (ns)	Typ. Receiver Prop. Delay (ns)	Packages	Comments and Special Features	Page #
Commercial	Industrial	Military								
0°C to +70°C	−40°C to +85°C	−55°C to +125°C								
DS36F95		DS16F95	1	1	28	12	19	W, J, E	Low Power	4-18
DS3695	DS3695T		1	1	60	15	25	N, J		4-3
DS3696	DS3696T		1	1	60	15	25	N, J	Thermal Shutdown Reporting	4-3
DS3697			1	1	60	15	25	N	Repeater	4-3
DS3698			1	1	60	15	25	N	Repeater, Thermal Shutdown Reporting	4-3
DS3695A	DS3695AT		1	1	60	15	25	M	SOIC Package	4-12
DS3696A			1	1	60	15	25	M	SOIC Package, Thermal Shutdown Reporting	4-12
DS75176B	DS75176BT		1	1	55	17	32	N, M		4-92
DS96F172C		DS96F172M	4	0	50	12	—	N, W, J, E	Low Power, Common Enable	4-102
DS96F174C		DS96F174M	4	0	50	12	—	W, J, E	Low Power, Enable Pair	4-102
DS96172C			4	0	70	12	—	N, J	Common Enable	4-102
DS96174C			4	0	70	12	—	N, J	Enable Pair	4-102
DS96F173C		DS96F173M	0	4	50	—	15	W, J, E	Low Power, Common Enable	4-115
DS96F175C		DS96F175M	0	4	50	—	15	W, J, E	Low Power, Enable Pair	4-115
DS96173C			0	4	75	—	15	N, J		4-110
DS96175C			0	4	75	—	15	N, J		4-110
DS96176C			1	1	35	12	16	N, J		4-123
DS96177C			1	1	35	12	16	N	Repeater	4-133
DS36276			1	1	60	60	60	M, N	Failsafe RS-485 Compatible	4-28
	DS36277T		1	1	60	60	90	M, N	Dominant Mode RS-485 Compatible	4-40
DS36C278	DS36C278T		1	1	0.5	40	210	N, M	Low Power	4-52
DS36C279	DS36C279T		1	1	0.5	40	210	N, M	Auto Sleep Mode	4-59
DS36C280	DS36C280T		1	1	0.5	400	210	N, M	Slew Rate Control	4-68
DS36950			4	4	90	15	14	V	QUAD Transceiver, IPI Applications	4-76
DS36954			4	4	90	15	14	V	QUAD Transceiver, SCSI Applications	4-85

Characteristics of an TIA/EIA-485 Device:

RECEIVERS:

Receiver common mode voltage range — −7V to +12V

Receiver sensitivity over common mode range — ±200 mV

Typical receiver input impedance — 12 kΩ

See TIA/EIA Standard TIA/EIA-485 for exact conditions.

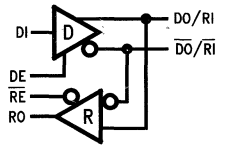
DRIVERS:

Minimum driver output voltage with 54Ω load — $\geq |1.5V|$

Driver output short circuit current (V_O = −7V to +12V) — $\leq |250\ mA|$

Maximum driver output offset voltage — 3V

Typical maximum data rate — 10 Mb/s.



TYPICAL TRANSCEIVER

TL/XX/0094–9

See Datasheets for Complete Specifications

LVDS TIA/EIA-644 LINE DRIVERS AND RECEIVERS

Device Number Industrial −40°C to +85°C	Number of Drivers	Number of Receivers	Power Supply (V)	Max I_{CC} (mA)	Typ. Driver Prop. Delay (ns)	Typ. Receiver Prop. Delay (ns)	Max Pulse Width Slew (ns)	Packages	Page #
DS90C031T	4	0	5	4	2	—	0.4	M	5-4
DS90LV031T	4	0	3.3					M	5-15
DS90C032T	0	4	5	10	—	3.5	0.6	M	5-16
DS90LV032T	0	4	3.3					M	5-24

CHANNEL LINK TRANSMITTERS AND RECEIVERS

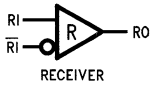
Device Number Commercial 0°C to +70°C	Transmitter or Receiver	# TTL Inputs	# Differential Pair Outputs	Max Clock Frequency	Power Supply	Strobe Edge	Package	Page #
DS90CR211MTD	Transmitter	21	4	40 MHz	5V	Rising	MTD	5-25
DS90CR212MTD	Receiver	21	4	40 MHz	5V	Rising	MTD	5-25
DS90CR281MTD	Transmitter	28	5	40 MHz	5V	Rising	MTD	5-34
DS90CR282MTD	Receiver	28	5	40 MHz	5V	Rising	MTD	5-34

Characteristics of an LVDS Device:

RECEIVERS:
Receiver common mode voltage range — GND to +2.4 V
Receiver sensitivity over common mode range — ±100 mV
See TIA/EIA Standard TIA/EIA-644 for exact conditions.

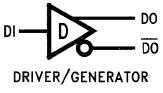
DRIVERS:
Minimum driver output voltage with 100Ω load — ≥|250 mV|
Driver output short circuit current (V_O = GND) — ≤| 24 mA|
Driver output offset voltage — +1.2V

See Datasheets for Complete Specifications



RECEIVER

TL/XX/0094-8



DRIVER/GENERATOR

TL/XX/0094-6

FPD LINK TRANSMITTERS AND RECEIVERS

Device Number Commercial 0°C to +70°C	Transmitter or Receiver	# RGB Inputs	# Differential Pair Outputs	Control Bits	Max Clock Frequency	Power Supply	Strobe Edge	Package	Page #
DS90CR561MTD	Transmitter	18	4	3	40 MHz	5V	Rising	MTD	5-43
DS90CR562MTD	Receiver	18	4	3	40 MHz	5V	Rising	MTD	5-43
DS90CR581MTD	Transmitter	24	5	4	40 MHz	5V	Rising	MTD	5-65
DS90CR582MTD	Receiver	24	5	4	40 MHz	5V	Rising	MTD	5-65
DS90CF561MTD	Transmitter	18	4	3	40 MHz	5V	Falling	MTD	5-54
DS90CF562MTD	Receiver	18	4	3	40 MHz	5V	Falling	MTD	5-54
DS90CF581MTD	Transmitter	24	5	4	40 MHz	5V	Falling	MTD	5-76
DS90CF582MTD	Receiver	24	5	4	40 MHz	5V	Falling	MTD	5-76
DS90CR563MTD	Transmitter	18	4	3	65 MHz	5V	Rising	MTD	5-87
DS90CR564MTD	Receiver	18	4	3	65 MHz	5V	Rising	MTD	5-87
DS90CR583MTD	Transmitter	24	5	4	65 MHz	5V	Rising	MTD	5-109
DS90CR584MTD	Receiver	24	5	4	65 MHz	5V	Rising	MTD	5-109
DS90CF563MTD	Transmitter	18	4	3	65 MHz	5V	Falling	MTD	5-98
DS90CF564MTD	Receiver	18	4	3	65 MHz	5V	Falling	MTD	5-98
DS90CF583MTD	Transmitter	24	5	4	65 MHz	5V	Falling	MTD	5-120
DS90CF584MTD	Receiver	24	5	4	65 MHz	5V	Falling	MTD	5-120

See Datasheets for Complete Specifications

SPECIAL INTERFACE

DS36C200	Dual High Speed Bi-Directional Differential Transceiver	Similar to IEEE P1394 Levels	Page # 6-3
DS36C250	Controller Area Network (CAN) Transceiver	Meets CAN Standard	Page # 6-12

GENERAL PURPOSE BALANCED AND UNBALANCED LINE DRIVERS

Standard	Device Number		Type of Driver	Number of Drivers	Power Supply V_{CC} (V)	Max I_{CC} (mA)	Output Stage	Output Voltage Min V_O (V)	Output Current I_O (mA)	Typical Prop. Delay (ns)	Packages	Page #
	Commercial	Military										
	0°C to +70°C	−55°C to +125°C										
188-114	DS3692	DS1692	Differential	2	5 or ±5	30/−22	TRI-STATE	±6	±20	190	N, J	7-3
—	DS75110A		Differential	2	±5	35/−50	TRI-STATE		±12	9	N, J, M	7-7
—	DS75113	DS55113	Differential	2	5	65	Note 2	3/0.2	±40	13	N, J, M	7-12
—	DS75114		Differential	2	5	50	Note 2	3/0.2	±40	15	N, J, W, E	7-19
—	DS75121		Single Ended	2	5	60	—	2.4	−100	11	N	7-24
IBM 360	DS75123		Single Ended	2	5	60	—	3.11	−100	12	N	7-26
—	DS8830	DS7830	Differential	2	5	18	—	1.8/0.5	±40	11	N, J, W	7-28
—	DS8831	DS7831	Note 1	2/4	5	90	TRI-STATE	1.8/0.5	±40	13	N, J, W	7-38
—	DS8832	DS7832	Note 1	2/4	5	90	TRI-STATE	1.8/0.5	±40	13	N, J, W	7-38
—	MM88C29	MM78C29	Single Ended	4	3 to 15						N, M, J, W	7-32
—	MM88C30	MM78C30	Differential	2	3 to 15						N, M, J, W	7-32

Note 1: Driver can be used in differential or single ended mode.

Note 2: Output features TRI-STATE, Choice of open collector or active pull-up.

See Datasheets for Complete Specifications

GENERAL PURPOSE BALANCED AND UNBALANCED RECEIVERS

Standard	Device Number		Number of Receivers	Input Sensitivity (mV)	Power Supply V_{CC} (V)	Max I_{CC}/I_{EE} (mA)	Rated V_{CM} (V)	Typ. Prop. Delay (ns)	Packages	Output Stage	Comments and Special Features	Page #
	Commercial	Military										
	0°C to +70°C	−55°C to +125°C										
—	DS26LS33C	DS26LS33M	4	±500	5	80	±25	17	N, J, W	TRI-STATE	422/3 Type	3-38
—	DS26LS33AC		4	±500	5	80	±25	23	N	TRI-STATE	422/3 Type	3-38
—	DS3603	DS1603	2	±25	±5	40/−15	±3	17	N, J, W	TRI-STATE		8-3
—	DS3650		4	±25	±5	60/−30	±3	21	N, M	TRI-STATE		8-7
—	DS3652	DS1652	4	±25	±5	60/−30	±3	22	J, M	TRI-STATE	Note 1	8-7
—	DS75107/A	DS55107A	2	±25	±5	30/−15	±3	17	N, J, M	Strobe		8-15
—	DS75108/A		2	±25	±5	30/−15	±3	19	N, M	Strobe	Note 1	8-15
—	DS75208		2	±10	±5	30/−15	±3		N, J	Strobe		8-15
—	DS75115	DS9615M	2	±500	5	50	±15	20	N, J, W, E	Strobe	Response Control	8-22
—		DS55122	3	—	5	72	6	20	J, W	Strobe		8-27
IBM 360	DS75124		3	—	5	72	7	20	N	Strobe		8-30
IBM 360/370	DS75129		8	—	5	53	7	18	N	Strobe		8-33
—	DS8820	DS7820	2	1000	5	10.2	±15	150	N, J, W	Strobe	Response Control	8-37
—	DS8820A	DS7820A	2	1000	5	10.2	±15	30	N, J, W	Strobe	Response Control	8-41
		DS9622M	2	—	5	22.9/−11.1	±15	50	J, W, E		Open Collector	8-46

Note 1: Open collector output stage.

See Datasheets for Complete Specifications

National Semiconductor

Line Driver and Receiver Cross Reference Guide

The Line Driver and Receiver Cross Reference Guide is provided as an aid in identifying replacement part numbers. Direct replacements feature identical pin-outs and very similar electrical specifications. Similar replacements also feature the same pin-out, and similar electrical specifications. Consult the data sheets for recommended operating conditions and package availability. Before replacing a specific product, it is recommended to compare electrical, functional, and mechanical specifications. Interchangeability between devices is not guaranteed. Manufacturers' most current data sheets take precedence over this guide.

AMD to National		
Device	**Direct**	**Similar**
AM26LS30	DS3691	
AM26LS31	DS26LS31	
AM26LS32	DS26LS32A	
AM26LS33	DS26LS33A	
AM26LS32B		DS26F32
AM26LS34		DS96173

Motorola to National		
Device	**Direct**	**Similar**
AM26LS30	DS3691	
AM26LS31	DS26LS31	
AM26LS32		DS26LS32A
MC1488	DS1488	
MC14C88	DS14C88	
MC1489	DS1489	
MC1489A	DS1489A	
MC14C89	DS14C89A	
MC26C31	DS26C31	
MC26C32	DS26C32A	
MC34C86	DS34C86	
MC34C87	DS34C87	
MC3450	DS3650	
MC3452	DS3652	
MC3486	DS3486	
MC3487	DS3487	
MC3488	DS9636A	
MC55107		DS55107
MC55S110		DS55110A
MC75107	DS75107	
MC75108	DS75108	
MC75S110	DS75110A	
MC75129	DS75129	
MC8T13		DS55121
MC8T14		DS55122
MC8T24		DS75124
SN75172B	DS96172C	
SN75173	DS96173C	
SN75174B	DS96174C	
SN75175	DS96175C	
SN75176	DS75176B	
SN75177	DS96177C	

National Semiconductor

Line Driver and Receiver Cross Reference Guide

Signetics to National		
Device	**Direct**	**Similar**
AM26LS30	DS3691	
AM26LS31	DS26LS31	
AM26LS32	DS26LS32A	
AM26LS33	DS26LS33A	
DS7820	DS7820	
DS7830	DS7830	
DS8820	DS8820	
DS8830	DS8830	
MC1488	DS1488	
MC1489	DS1489	
MC1489A	DS1489A	
8T13	DS75121	
8T14	DS55122	
8T23	DS75123	
8T24	DS75124	
8T129	DS75129	

TI to National		
Device	**Direct**	**Similar**
AM26LS31	DS26LS31	
AM26LS32A	DS26LS32A	
AM26LS33A	DS26LS33A	
MAX232	DS14C232	
MC3486	DS3486	
MC3487	DS3487	
SN55107B	DS55107	
SN55108B	DS55108	
SN55110A	DS55110A	
SN55113	DS55113	
SN55114	DS9614	
SN55115	DS9615	
SN55121	DS55121	
SN55122	DS55122	
SN55173		DS96F173M
SN55182	DS7820A	
SN55183	DS7830	
SN55ALS192		DS26C31M
SN55ALS194		DS35F87
SN55ALS195		DS35F86
SN65176B	DS75176BT	
SN65ALS176		DS75176BT
SN65C188	DS14C88T	
SN65C189A	DS14C89AT	
SN75107B	DS75107	
SN75108B	DS75108	
SN75110A	DS75110A	
SN75113	DS75113	
SN75114	DS75114	
SN75115	DS75115	
SN75121	DS75121	
SN75123	DS75123	
SN75124	DS75124	
SN75129	DS75129	
SN75146		DS9639A
SN75150	DS75150	
SN75154	DS75154	

Line Driver and Receiver Cross Reference Guide

Texas Instruments to NSC		
Device	**Direct**	**Similar**
SN75172	DS96172C	
SN75173	DS96173C	
SN75174	DS96174C	
SN75175	DS96175C	
SN75176	DS96176C	
SN75176A	DS75176B	
SN75176B	DS75176B	
SN75LBC176		DS36C278
SN75177	DS96177C	
SN75177B	DS3697	
SN75182	DS8820A	
SN75183	DS8830	
SN75188	DS1488	
SN75189	DS1489	
SN75189A	DS1489A	
SN75ALS176	DS36F95	
SN75ALS191		DS9638
SN75ALS192		DS26C31C
SN75ALS193		DS26C32AC
SN75ALS194		DS34C87
SN75ALS195		DS34C86
SN75C188	DS14C88	
SN75C189A	DS14C89A	
SN75276	DS36276	
SN75LBC241	DS14C241T	
SN75LV4737A		DS14C335
SN95176B	DS16F95	
TL3695	DS3695	
μA9636A	DS9636A	
μA9637A	DS9637A	
μA9638	DS9638	
μA9639	DS9639A	

National Semiconductor

Line Driver and Receiver Cross Reference Guide

Maxim to National		
Device	**Direct**	**Similar**
MAX232	DS14C232	
MAX237	DS14C237	
MAX238	DS14C238	
MAX239	DS14C239	
MAX241	DS14C241	
MAX481	DS36C279	
MAX485	DS36C278	
MAX561	DS14C561	

SIPEX to National		
Device	**Direct**	**Similar**
SP481	DS36C279	
SP485	DS36C278	

LTC to National		
Device	**Direct**	**Similar**
LTC485	DS36C278	

Analog Devices to National		
Device	**Direct**	**Similar**
ADM485	DS36C278	

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Extended Temperature Range Devices

Line Drivers and Receivers

Commercial		Military	
−40°C to +85°C	−55°C to +125°C	883	MLS
DS14C88T	DS1691A	DS14C232	DS16F95
DS14C89AT	DS1692	DS1603	DS26C31M
DS14C232T	DS16F95	DS1652	DS26C32AM
DS14C237T	DS26F31M	DS1691A	DS26F31M
DS14C238T	DS26LS31M	DS16F95	DS26F32M
DS14C239T	DS26F32M	DS26C31M	DS26F33M
DS14C241T	DS26LS32M	DS26F31M	DS26LS31M
DS14C335T	DS26LS33M	DS26LS31M	DS26LS32AM
DS14C535T	DS35F86	DS26C32AM	DS26LS33M
DS26C31T	DS35F87	DS26F32M	DS78C120
DS26C32AT	DS55113	DS26LS32M	DS78LS120
DS34C86T	DS7820	DS26LS33M	DS7820A
DS34C87T	DS7820A	DS55107A	DS7820
DS3695T	DS78C20	DS55113	DS7830
DS3695AT	DS9636AM	DS55122	DS9615M
DS3696T	DS9637AM	DS7820	DS9638M
DS36277T	DS9638M	DS7820A	DS96F174M
DS36C278T	DS96F172M	DS78C20	DS96F175M
DS36C279T	DS96F173M	DS7830	
DS36C280T	DS96F174M	DS7831	
DS75176BT	DS96F175M	DS7832	
DS8921AT		DS78C120	
DS89C21T		DS78LS120	
DS89C386T		DS9615M	
DS89C387T		DS9616HM	
DS90C031T		DS9622M	
DS90C032T		DS9627M	
MM88C29		DS9636A	
MM88C30		DS9637AM	
		DS9638M	
		DS96F172M	
		DS96F173M	
		DS96F174M	
		DS96F175M	
		MM78C29	
		MM78C30	

Note 1: Package suffix is not shown, see Datasheet.

National Semiconductor

New Additions to this Databook
Data Transmission Circuits

Datasheets:	Description:	Standards:
DS14196	5 Driver × 3 Receiver	RS-232
DS14C202	2 Driver × 2 Receiver (+5V, 0.1 μF)	RS-232
DS26LV31	Quad Differential Driver (3V)	~RS-422
DS26LV32A	Quad Differential Receiver (3V)	~RS-422/3
DS34LV86	Quad Differential Receiver (3V)	~RS-422/3
DS34LV87	Quad Differential Driver (3V)	~RS-422
DS89LV21	Driver/Receiver Pair (3V)	~RS-422
DS8926	Local Talk Transceiver	RS-422/3
DS8933	V.34 2 Driver × 1 Receiver	~RS-423
DS8934	V.34 5 Driver × 3 Receiver	~RS-423
DS8935	Local Talk Transceiver	RS-422/3
DS8936	Local Talk Transceiver	RS-422/3
DS89C386	12 Channel Differential Receiver	RS-422/3
DS89C387	12 Channel Differential Driver	RS-422
DS36C200	Dual Differential Transceiver	LSD
DS36C250	CAN Transceiver	CAN
DS36C278	Low Power Transceiver	RS-485
DS36C279	Low Power Transceiver w/Sleep Mode	RS-485
DS36C280	Low Power Transceiver w/Slew Control	RS-485
DS90LV031	LVDS Quad Differential Driver (3V)	RS-644
DS90LV032	LVDS Quad Differential Receiver (3V)	RS-644
DS90CR211/2	21-Bit (TTL) Channel Link	RS-644
DS90CR281/2	28-Bit (TTL) Channel Link	RS-644
DS90CR561/2	FPD-Link	RS-644
DS90CF561/2	FPD-Link	RS-644
DS90CR581/2	FPD-Link	RS-644
DS90CF581/2	FPD-Link	RS-644
DS90CR563/4	FPD-Link (65 MHz)	RS-644
DS90CF563/4	FPD-Link (65 MHz)	RS-644
DS90CR583/4	FPD-Link (65 MHz)	RS-644
DS90CF583/4	FPD-Link (65 MHz)	RS-644

Application Notes:	TOPIC:
AN-967	Local Talk Application
AN-971	LVDS Overview
AN-972	Inter-Operation of Interfaces
AN-977	LVDS Signal Quality
AN-979	RS-485 Overview
AN-1031	RS-422 Overview
AN-1032	FPD Link Overview
AN-1034	V.34 Interface
AN-1035	LVDS PCB Guidelines

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Application Note—Selection Guide
Line Drivers and Receivers

Application Note Number AN-XXXX	Title	Devices Referenced	TIA/EIA Standards Referenced	ITU-T (CCITT) Related Recommendations
AN-22	Integrated Circuits for Digital Data Transmission	DS7830/DS8830, DS7820/DS8820		
AN-108	Transmission Line Characteristics	DS7820/DS8820		
AN-214	Transmission Line Drivers and Receivers for EIA Standards, RS-422 and RS-423	DS3691, DS88LS120	422 423	V.11 V.10
AN-216	Summary of Well Known Interface Standards		ALL	
AN-336	Understanding Integrated Circuit Package Power Capabilities			
AN-409	Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard	DS3695/DS3696, DS3697/DS3698	485	
AN-438	Low Power RS-232C Driver and Receiver in CMOS	DS14C88, DS14C89A	232	V.28
AN-450	Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability			
AN-454	Automotive Multiplex Wiring	DS75176B DS3695	485	
AN-457	High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Programs	DS8921/A, DS8922/A, DS8923/A	422	V.11
AN-643	EMI/RFI Board Design			
AN-702	Build a Directional-Sensing Bidirectional Repeater	DS75176B, DS96175C	485	
AN-759	Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications		422 485	V.11
AN-805	Calculating Power Dissipation for Differential Line Drivers	DS26LS31, DS96F172	422 485	V.11
AN-806	Data Transmission Lines and Their Characteristics			
AN-807	Reflections: Computations and Waveforms			
AN-808	Long Transmission Lines and Data Signal Quality			
AN-847	FAILSAFE Biasing of Differential Buses	DS3695, DS96172, DS96F172	422 485	V.11
AN-876	Inter-Operation of the DS14C335 with +5V UARTs	DS14C335	232	V.28
AN-878	Increasing System ESD Tolerance for Line Drivers and Receivers used in RS-232 Interfaces	DS1488, DS1489A	232	V.28

Application Note—Selection Guide—Line Drivers and Receivers (Continued)

Application Note Number AN-XXXX	Title	Devices Referenced	TIA/EIA Standards Referenced	ITU-T (CCITT) Related Recommendations
AN-903	A Comparison of Differential Termination Techniques		422 485	V.11
AN-904	An Introduction to the Differential SCSI Interface	DS36954	485	
AN-905	Transmission Line Rapidesigner Operation and Applications Guide		All	
AN-912	Common Data Transmission Parameters and their Definitions		All	
AN-914	Understanding Power Requirements in RS-232 Applications	DS14C335	232 562	
AN-915	Automotive Physical Layer SAE J1708 and the DS36277	DS36277 DS75176B	485	
AN-916	A Practical Guide to Cable Selection		All	
AN-917	Popular Connector Pin Assignments for Data Communication		All	
AN-967	Local Talk™ Physical Layer Alternatives	DS8925/26 DS8935/36	422 423	V.11 V.10
AN-971	An Overview of LVDS Technology	DS90C031 DS90C032	644	
AN-972	Inter-operation of Interface Standards		All	
AN-977	LVDS Signal Quality: Jitter Measurements using Eye Patterns Test Report #1	DS90C031 DS90C032	644	
AN-979	The Practical Limits of RS-485	DS75176B DS3695	485	
AN-1031	TIA/EIA-422-B Overview		422	V.11
AN-1032	An Introduction to FPD-Link	DS90CR561/2 DS90CF561/2 DS90CR581/2 DS90CF581/2	644	
AN-1034	An Optimized DCE Interface for V.34 Modems using the DS8933 and DS8934 Line Driver and Receivers	DS8933 DS8934	423	V.10
AN-1035	PCB Design Guidelines for LVDS Technology		644	

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Data Transmission Standards Cross Reference

TIA/EIA Electrical Interface Standards	ITU-T* (CCITT) Recommendations	ISO* Standards	Other*
EIA/TIA-232-E	V.24 - Functional V.28 - Electrical	ISO 2110	
TIA/EIA-422-B	V.11		
TIA/EIA-423-B	V.10		
EIA RS-485		ISO 8482	
EIA/TIA-562			
TIA/EIA-612	V.12		
TIA/EIA-644			IEEE 1596.3

*Cross reference is to similar standards. Differences in parameters, test conditions, and or limits may exist.

Section 2

RS-232 Serial Port Devices

Section 2 Contents

National Semiconductor

DS14185
EIA/TIA-232 3 Driver x 5 Receiver

General Description

The DS14185 is a three driver, five receiver device which conforms to the EIA/TIA-232-E standard.

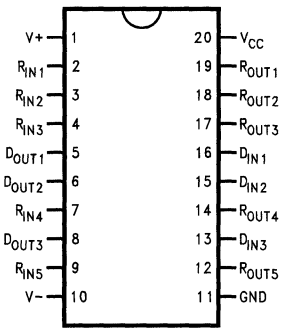
The flow-through pinout facilitates simple non-crossover board layout. The DS14185 provides a one-chip solution for the common 9-pin serial RS-232 interface between data terminal and data communications equipment.

Features

- Replaces one 1488 and two 1489s
- Conforms to EIA/TIA-232-E
- 3 drivers and 5 receivers
- Flow through pinout
- Failsafe receiver outputs
- 20-pin SOIC package
- LapLink® compatible −200 kbps data rate

Connection Diagram

SOIC



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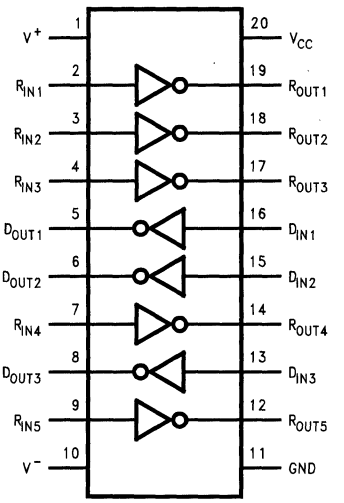
Order Number DS14185WM
See NS Package M20B

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V^+)	+15V
Supply Voltage (V^-)	−15V
Driver Input Voltage	0V to V_{CC}
Driver Output Voltage (Power Off)	±15V
Receiver Input Voltage	±25V
Receiver Output Voltage (R_{OUT})	0V to V_{CC}
Maximum Package Power Dissipation @ +25°C	
M Package	1488 mW
Derate M Package	11.9 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 seconds)	+260°C
ESD Ratings (HBM, 1.5 kΩ, 100 pF)	≥1.5 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V^+)	+9.0	+12.0	+13.2	V
Supply Voltage (V^-)	−13.2	−12.0	−9.0	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
I_{CC}	V_{CC} Supply Current	No Load, All Inputs at +5V			24	30	mA
I^+	V^+ Supply Current (Note 2)	No Load, All Driver Inputs at 0.8V or +2V All Receiver Inputs at 0.8V or 2.4V.	$V^+ = 9V, V^- = -9V$		11.8	15	mA
			$V^+ = 13.2V, V^- = -13.2V$		17.7	22	mA
I^-	V^- Supply Current (Note 2)		$V^+ = 9V, V^- = -9V$		−18.5	−22	mA
			$V^+ = 13.2V, V^- = -13.2V$		−24	−28	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current (Note 2)	$V_{IN} = 5V$				10	μA
I_{IL}	Low Level Input Current (Note 2)	$V_{IN} = 0V$			−1.24	−1.5	mA
V_{OH}	High Level Output Voltage (Note 2)	$R_L = 3\,k\Omega, V_{IN} = 0.8V, V^+ = 9V, V^- = -9V$		6	7		V
		$R_L = 3\,k\Omega, V_{IN} = 0.8V, V^+ = +12V, V^- = -12V$		8.5	10		V
		$R_L = 7\,k\Omega, V_{IN} = 0.8V, V^+ = +13.2V, V^- = -13.2V$		10	11.5		V
V_{OL}	Low Level Output Voltage (Note 2)	$R_L = 3\,k\Omega, V_{IN} = 2V, V^+ = 9V, V^- = -9V$			−7	−6	V
		$R_L = 3\,k\Omega, V_{IN} = 2V, V^+ = +12V, V^- = -12V$			−8	−7.5	V
		$R_L = 7\,k\Omega, V_{IN} = 0.8V, V^+ = +13.2V, V^- = -13.2V$			−11	−10	V
I_{OS}^+	Output High Short Circuit Current (Note 2)	$V_O = 0V, V_{IN} = 0.8V$		−6	−13	−18	mA
I_{OS}^-	Output Low Short Circuit Current (Note 2)	$V_O = 0V, V_{IN} = 2.0V$		6	13	18	mA
R_O	Output Resistance	$-2V \le V_O \le +2V, V^+ = V^- = V_{CC} = 0V$		300			Ω
		$-2V \le V_O \le +2V, V^+ = V^- = V_{CC}$ = Open Ckt		300			Ω

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 2). (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold (Recognized as a High Signal)	$V_O \leq 0.4V$, $I_O = 3.2$ mA		2.0	2.4	V
V_{TL}	Input Low Threshold (Recognized as a Low Signal)	$V_O \geq 2.5V$, $I_O = -0.5$ mA	0.8	1.0		V
R_{IN}	Input Resistance	$V_{IN} = \pm 3V$ to $\pm 15V$	3.0	4.1	7.0	kΩ
I_{IN}	Input Current (Note 2)	$V_{IN} = +15V$	2.1	4.1	5.0	mA
		$V_{IN} = +3V$	0.43	0.7	1	mA
		$V_{IN} = -15V$	−5.0	−4.1	−2.1	mA
		$V_{IN} = -3V$	−1	−0.65	−0.43	mA
V_{OH}	High Level Output Voltage (Note 7)	$I_{OH} = -0.5$ mA, $V_{IN} = -3V$	2.6	4		V
		$I_{OH} = -10\ \mu A$, $V_{IN} = -3V$	4.0	4.9		V
		$I_{OH} = -0.5$ mA, V_{IN} = Open Circuit	2.6	4		V
		$I_{OH} = -10\ \mu A$, V_{IN} = Open Circuit	4.0	4.9		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 3.2$ mA, $V_{IN} = +3V$		0.2	0.4	V
I_{OSR}	Short Circuit Current (Note 2)	$V_O = 0V$, $V_{IN} = 0V$	−4	−2.7	−1.7	mA

Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 3$ kΩ, $C_L = 50$ pF (*Figures 1* and *2*)		90	350	ns
t_{PLH}	Propagation Delay Low to High			220	350	ns
t_r, t_f	Output Slew Rate (Note 8)			50		ns
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 1.5$ kΩ, $C_L = 15$ pF (includes fixture plus probe), (*Figures* 3 and *4*)		60	100	ns
t_{PLH}	Propagation Delay Low to High			100	160	ns
t_r	Rise Time			87	175	ns
t_f	Fall Time			15	50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if −6V is a maximum, the typical value (−6.8V) is more negative.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $V^+ = +12.0V$, $V^- = -12V$, $T_A = +25°C$.

Note 4: Only one driver output shorted at a time.

Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, duty cycle = 50%.

Note 7: If receiver inputs are unconnected, receiver output is a logic high.

Note 8: Refer to typical curves. Driver output slew rate is measured from the +3.0V to the −3.0V level on the output waveform. Inputs not under test are connected to V_{CC} or GND. Slew rate is determined by load capacitance. To comply with a 30 V/μs maximum slew rate, a minimum load capacitance of 390 pF is recommended.

Parameter Measurement Information

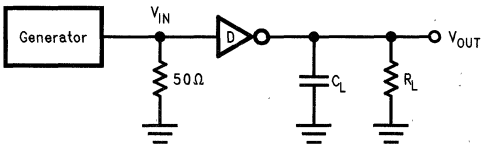

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FIGURE 1. Driver Propagation Delay and Transition Time Test Circuit (Note 5)

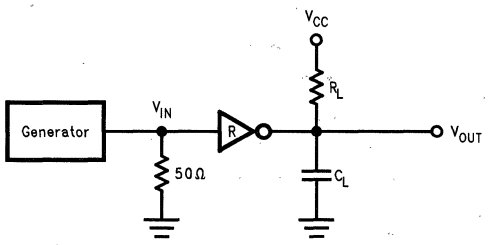

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FIGURE 3. Receiver Propagation Delay and Transition Time Test Circuit (Note 6)

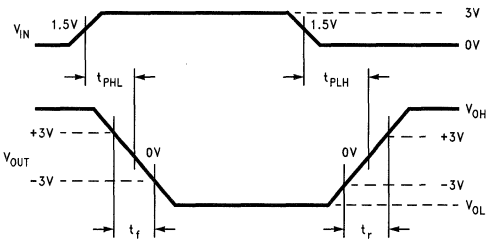

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FIGURE 2. Driver Propagation Delay and Transition Time Waveforms Slew Rate (SR) = 6V/(t_r or t_f)

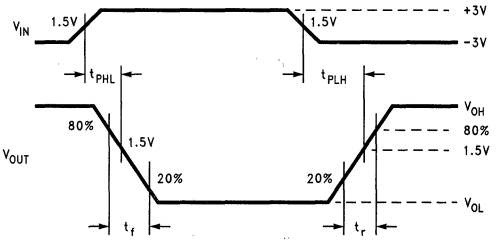

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FIGURE 4. Receiver Propagation Delay and Transition Time Waveform

Pin Descriptions

Pin #	Name	Description
13, 15, 16	D_{IN}	TTL Level Driver Inputs
5, 6, 8	D_{OUT}	Driver Output Pins, RS-232 Levels
2, 3, 4, 7, 9	R_{IN}	Receiver Input Pins, RS-232 Levels
12, 14, 17, 18, 19	R_{OUT}	Receiver Output Pins, TTL Levels
11	GND	Ground
1	V^+	Positive Power Supply Pin ($+9.0 \leq V^+ \leq +13.2$)
10	V^-	Negative Power Supply Pin ($-9.0 \leq V^- \leq -13.2$)
20	V_{CC}	Positive Power Supply Pin ($+5V \pm 5\%$)

Applications Information

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD. The control lines are RTS, DTR, DSR, DCD, CTS, and RI.

The DS14185 is a 3 x 5 Driver/Receiver and offers a single chip solutuion for this DTE interface. As shown in *Figure 5*, this interface allows for direct flow-thru interconnect. For a more conservative design, the user may wish to insert ground traces between the signal lines to minimize cross talk.

LapLink COMPATIBILITY

The DS14185 can easily provide 128 kbps data rate under maximum driver load conditions of C_L = 2500 pF and R_L = 3 kΩ, while power supplies are:

$$V_{CC} = 4.75V, V^+ = 10.8V, V^- = -10.8V$$

MOUSE DRIVING

A typical mouse can be powered from the drivers. Two driver outputs connected in parallel and set to V_{OH} can be used to supply power to the V^+ pin of the mouse. The third driver output is set to V_{OL} to sink the current from the V^- terminal. Refer to typical curves of V_{OUT}/I_{OUT}. Typical mouse specifications are:

10 mA at +6V
5 mA at −6V

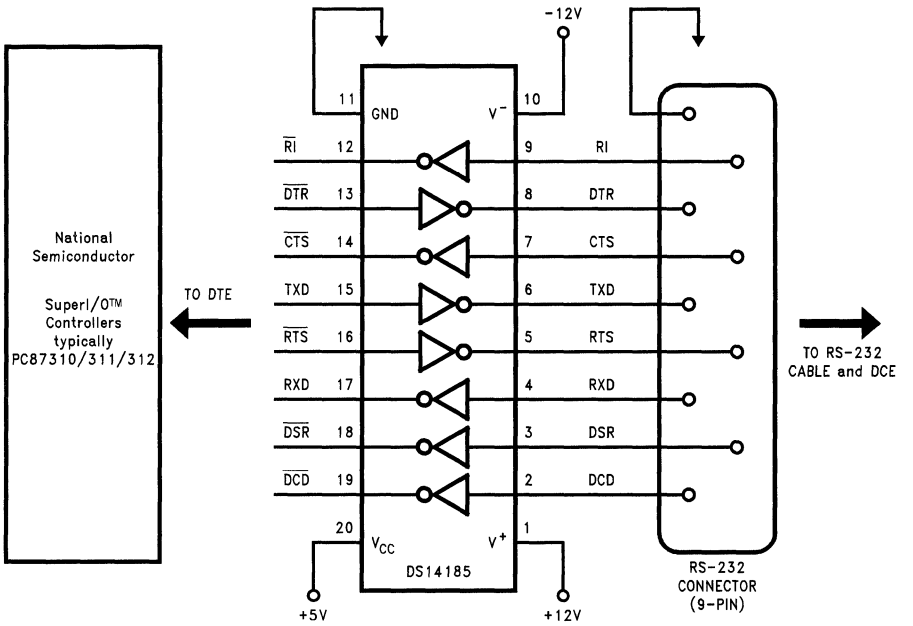

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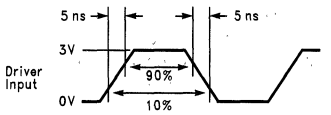
FIGURE 5. Typical DTE Application

Typical Performance Characteristics



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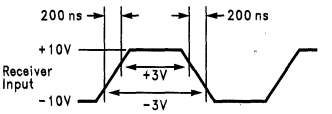
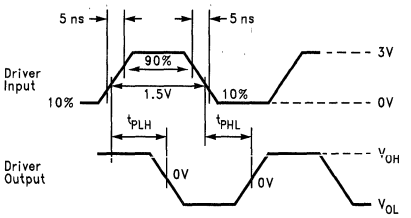


TL/F/11938-9

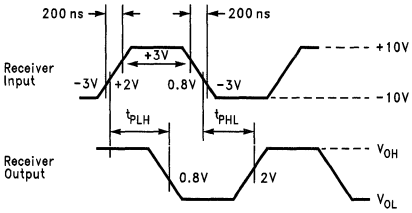
The above input waveforms were used to generate all Typical AC Characteristics.

Driver Propagation Delay vs C_L

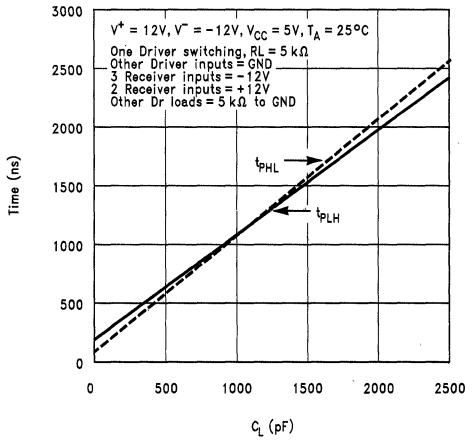


TL/F/11938-10

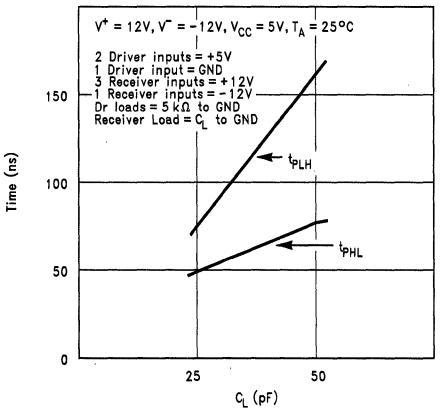
Receiver Propagation Delay vs C_L



TL/F/11938-11



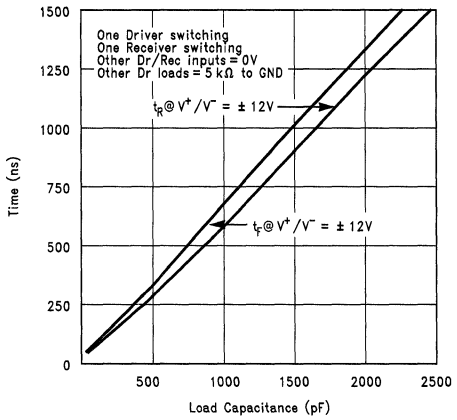
TL/F/11938-12



TL/F/11938-14

Driver Output Slew Rate between +3V and −3V vs Load Capacitance

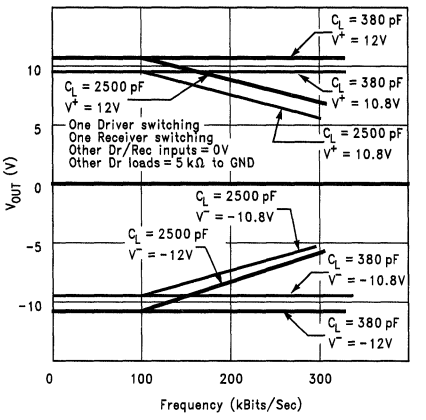
Conditions: V_{CC} = 5V, R_L = 5 kΩ, T_A = 25°C, f_{IN} = 64 kHz Square Wave



TL/F/11938-15

Driver Output Voltage vs Frequency and C_L

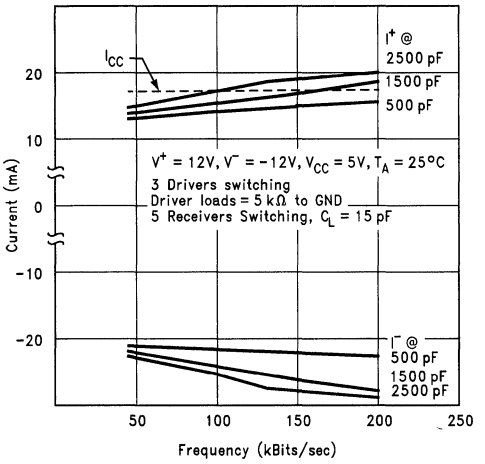
Conditions: V_{CC} = 5V, R_L = 5 kΩ, T_A = 25°C



TL/F/11938-16

Typical Performance Characteristics (Continued)

Supply Current vs Frequency and Driver C_L



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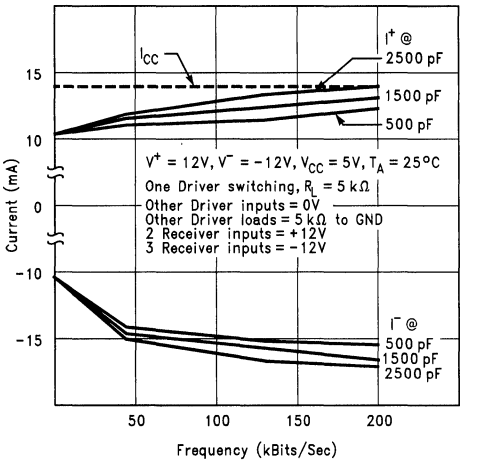
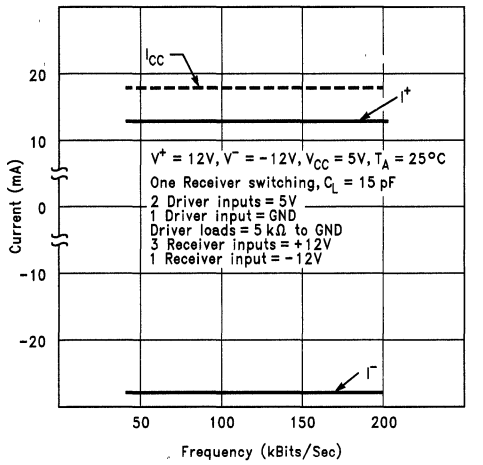
Supply Current vs Frequency and Driver C_L



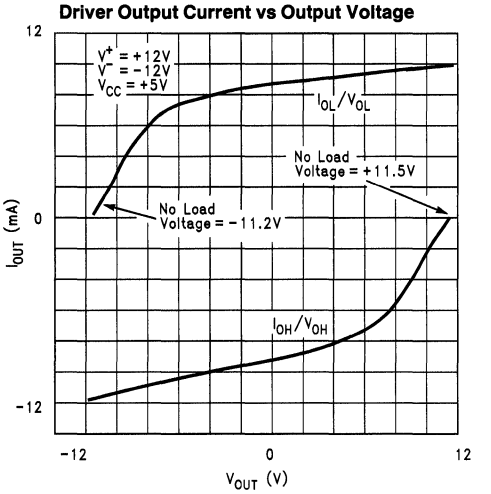
TL/F/11938–17

Supply Current vs Frequency



TL/F/11938–18

Driver Output Current vs Output Voltage



TL/F/11938–19

National Semiconductor

ADVANCE INFORMATION

DS14196
EIA/TIA-232 5 Driver x 3 Receiver

General Description

The DS14196 is a five driver, three receiver device which conforms to the EIA/TIA-232-E standard.

The flow-through pinout facilitates simple non-crossover board layout. The DS14196 provides a peripheral side one-chip solution for the common 9-pin serial RS-232 interface between data terminals and data communications equipment.

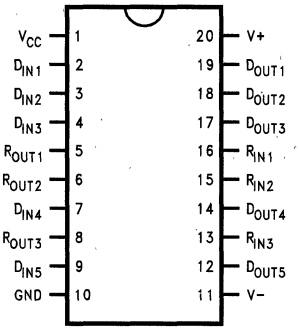
The DS14196 offers optimum performance when used with the DS14185 3 x 5 Driver/Receiver, a host side one-chip solution for the common 9-pin serial RS-232 interface between data terminals and data communications equipment.

Features

- Replaces two 1488s and one 1489
- Conforms to EIA/TIA-232-E
- 5 drivers and 3 receivers
- Flow-through pinout
- Failsafe receiver outputs
- 20-pin wide SOIC package
- LapLink® compatible—300 kbps data rate
- Pin compatible with: SN75196
  GD7532

Connection Diagram

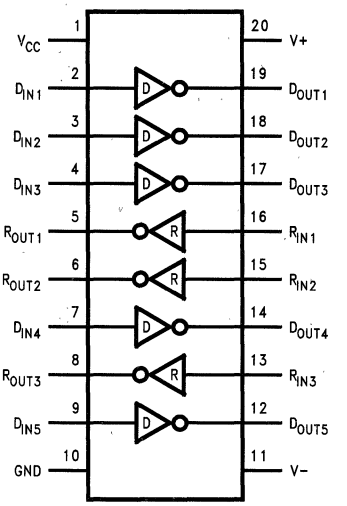
SOP



TL/F/12613–1

Order Number DS14196WM
See NS Package Number M20B

Functional Diagram



TL/F/12613–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V^+)	+15V
Supply Voltage (V^-)	−15V
Driver Input Voltage	0V to V_{CC}
Driver Output Voltage (Power Off)	±15V
Receiver Input Voltage	±25V
Receiver Output Voltage (R_{OUT})	0V to V_{CC}
Maximum Power Package Dissipation @ +25°C	
M Package	TBD
Derate M Package	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 sec.)	+260°C
ESD Ratings (HBM. 1.5 kΩ, 100 pF)	≥1.5 kV

Recommended Operating Conditons

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V^+)	+9.0	+12.0	+13.2	V
Supply Voltage (V^-)	−13.2	−12.0	−9.0	V
Operating Free Air Temperature (T_A)	0	+25	+70	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
I_{CC}	V_{CC} Supply Current	No Load, All Inputs at +5V				TBD	mA
I^+	V^+ Supply Current (Note 2)	No Load, All Driver Inputs at 0.8V or +2V. All Receiver Inputs at 0.8V or 2.4V.	$V^+ = +9V, V^- = -9V$			TBD	mA
			$V^+ = +13.2V, V^- = -13.2V$			TBD	mA
I^-	V^- Supply Current (Note 2)		$V^+ = +9V, V^- = -9V$			TBD	mA
			$V^+ = +13.2V, V^- = -13.2V$			TBD	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current (Note 2)	$V_{IN} = 5V$				10	μA
I_{IL}	Low Level Input Current (Note 2)	$V_{IN} = 0V$				TBD	mA
V_{OH}	High Level Output Voltage (Note 2)	$R_L = 3\ k\Omega, V_{IN} = 0.8V, V^+ = +9V, V^- = -9V$		6	7		V
		$R_L = 3\ k\Omega, V_{IN} = 0.8V, V^+ = +12V, V^- = -12V$		8.5	10		V
		$R_L = 7\ k\Omega, V_{IN} = 0.8V, V^+ = +13.2V, V^- = -13.2V$		10	11.5		V
V_{OL}	Low Level Output Voltage (Note 2)	$R_L = 3\ k\Omega, V_{IN} = 2V, V^+ = +9V, V^- = -9V$			−7	−6	V
		$R_L = 3\ k\Omega, V_{IN} = 2V, V^+ = +12V, V^- = -12V$			−8	−7.5	V
		$R_L = 7\ k\Omega, V_{IN} = 2V, V^+ = +13.2V, V^- = -13.2V$			−11	−10	V
I_{OS}^+	Output High Short Circuit Current (Note 2)	$V_{OUT} = 0V, V_{IN} = 0.8V$		−6	−9	−14	mA
I_{OS}^-	Output Low Short Circuit Current (Note 2)	$V_{OUT} = 0V, V_{IN} = 2.0V$		6	9	14	mA
R_O	Output Resistance	$-2V \le V_{OUT} \le +2V, V^+ = V^- = V_{CC} = 0V$		300			Ω
		$-2V \le V_{OUT} \le +2V, V^+ = V^- = V_{CC}$ = Open Circuit		300			Ω

Electrical Characteristics

Over recommended operating supply voltage and temperature ranges, unless otherwise specified (Note 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold (Recognized as a High Signal)	$V_{OUT} \leq 0.4V$, $I_O = 3.2$ mA		2.0	2.4	V
V_{TL}	Input Low Threshold (Recognized as a Low Signal)	$V_{OUT} \geq 2.5V$, $I_O = -0.5$ mA	0.8	1.0		V
R_{IN}	Input Resistance	$V_{IN} = \pm 3V$ to $\pm 15V$	3.0	4.1	7.0	kΩ
I_{IN}	Input Current (Note 2)	$V_{IN} = +15V$	2.1	4.1	5.0	mA
		$V_{IN} = +3V$	0.43	0.7	1.0	mA
		$V_{IN} = -15V$	−2.1	−4.1	−5.0	mA
		$V_{IN} = -3V$	−0.43	−0.65	−1.0	mA
V_{OH}	High Level Output Voltage (Note 7)	$I_{OH} = -0.5$ mA, $V_{IN} = -3V$	2.6	4.0		V
		$I_{OH} = -10\ \mu A$, $V_{IN} = -3V$	4.0	4.9		V
		$I_{OH} = -0.5$ mA, V_{IN} = Open Circuit	2.6	4.0		V
		$I_{OH} = -10\ \mu A$, V_{IN} = Open Circuit	4.0	4.9		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 3.2$ mA, $V_{IN} = +3V$		0.2	0.4	V
I_{OSR}	Short Circuit Current (Note 2)	$V_{OUT} = 0V$, $V_{IN} = 0V$ (Note 4)	−1.7	−2.7	−4	mA

Switching Characteristics

Over recommended operating supply and temperature ranges, unless otherwise specified (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 3$ kΩ, $C_L = 50$ pF (*Figures 1* and *2*)		90	350	ns
t_{PLH}	Propagation Delay Low to High			220	350	ns
t_r, t_f	Output Slew Rate (Note 8)			50		ns
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 1.5$ kΩ, $C_L = 15$ pF (includes fixture plus probe), (*Figures* 3 and *4*)		60	100	ns
t_{PLH}	Propagation Delay Low to High			100	160	ns
t_r	Rise Time			87	175	ns
t_f	Fall Time			15	50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of the device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. For current, minimum and maximum values are specified as an absolute value and the sign is used to indicate direction. For voltage logic levels, the more positive value is designated as maximum. For example, if −6V is a maximum, the typical value −6.8V is more negative.

Note 3: All typicals are given for: $V_{CC} = +5V$, $V^+ = +12V$, $V^- = -12V$, $T_A = +25°C$.

Note 4: Only one driver output shorted at a time.

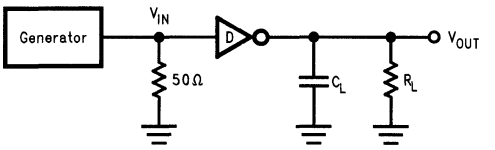
Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbps), $t_r = t_f < 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbps), $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, duty cycle = 50%.

Note 7: If receiver inputs are unconnected, receiver output is a logic high.

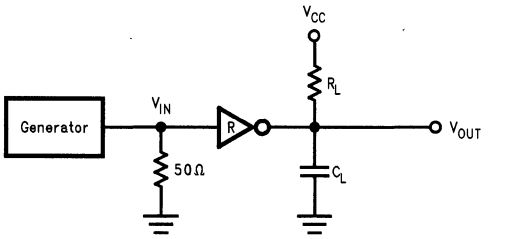
Note 8: Refer to typical curves. Driver output slew rate is measured from the +3V to the −3V level on the output waveform. Inputs not under test are connected to V_{CC} or GND. Slew rate is determined by load capacitance. To comply with a 30 V/μs maximum slew rate, a minimum load capacitance of 390 pF is recommended.

Parameter Measurement Information



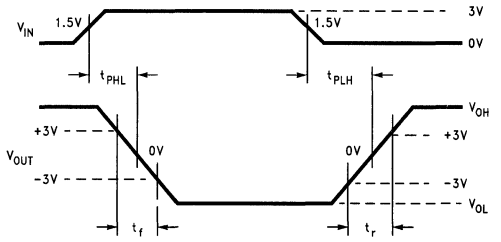
TL/F/12613–3

FIGURE 1. Driver Propagation Delay and Transition Time Test Circuit (Note 5)



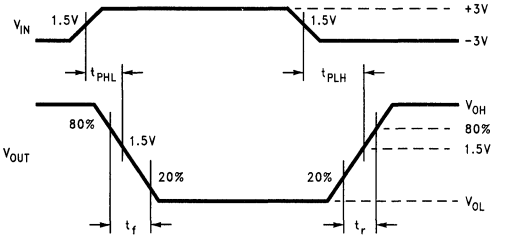
TL/F/12613–5

FIGURE 3. Receiver Propagation Delay and Transition Time Test Circuit (Note 6)



TL/F/12613–4

FIGURE 2. Driver Propagation Delay and Transition Time Waveforms Slew Rate (SR) = 6V/(t_r or t_f)



TL/F/12613–6

FIGURE 4. Receiver Propagation Delay and Transition Time Waveform

Pin Descriptions

Pin #	No.	Description
2, 3, 4, 7, 9	D_{IN}	Driver Input Pins, RS-232 Levels
12, 14, 17, 18, 19	D_{OUT}	TTL Level Driver Outputs
13, 15, 16	R_{IN}	TTL Level Receiver Inputs
5, 6, 8	R_{OUT}	Receiver Output Pins, RS-232 Levels
GND	GND	Ground
20	V^+	Positive Power Supply Pin ($+9.0 \leq V^+ \leq +13.2$)
11	V^-	Negative Power Supply Pin ($-9.0 \leq V^- \leq -13.2$)
1	V_{CC}	Positive Power Supply Pin ($+5V \pm 5\%$)

Applications Information

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD. The control lines are RTS, DTR, DSR, DCD, CTS and RI.

The DS14196 is a 5 x 3 Driver/Receiver and offers a single chip solutuion for this DTE interface. As shown in *Figure 5*, this interface allows for direct flow-thru interconnect. For a more conservative design, the user may wish to insert ground traces between the signal lines to minimize cross talk.

LapLink COMPATIBILITY

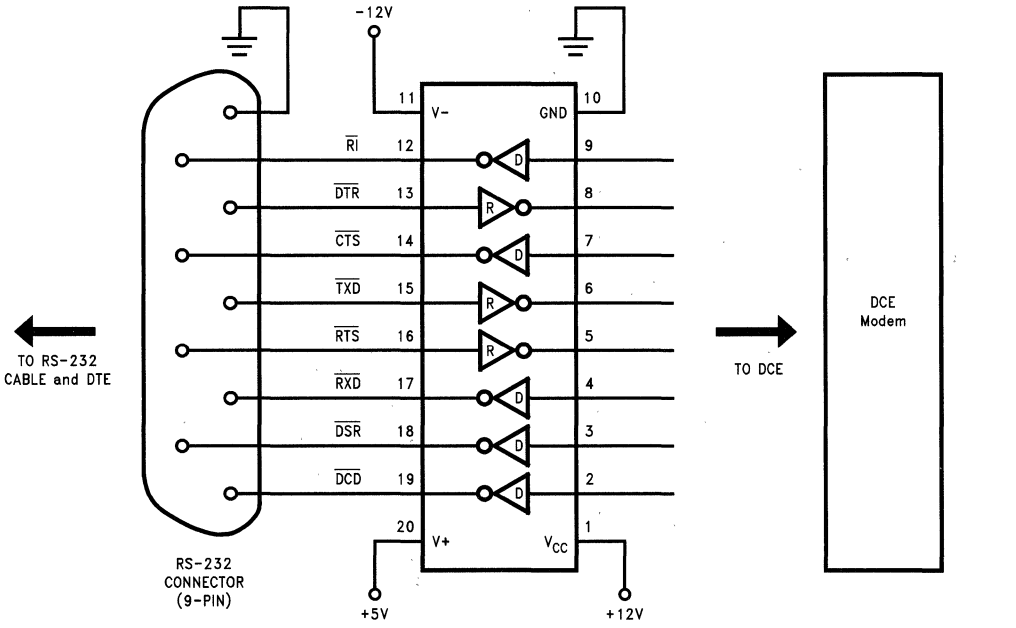
The DS14196 can easily provide 128 kbps data rate under maximum driver load conditions of C_L = 2500 pF and R_L = 3 kΩ, while power supplies are:

$$V_{CC} = +4.75V, V^+ = 10.8V, V^- = -10.8V$$

MOUSE DRIVING

A typical mouse can be powered from the drivers. Two driver outputs connected in parallel and set to V_{OH} can be used to supply power to the V^+ pin of the mouse. The third driver output is set to V_{OL} to sink the current from the V^- terminal. Refer to typical curves of V_{OUT}/I_{OUT}.Typical mouse specifications are:

10 mA at +6V 5 mA at −6V



TL/F/12613–7

FIGURE 5. Typical DCE Application

National Semiconductor

ADVANCE INFORMATION

DS14C202
Low Power +5V Powered EIA/TIA-232 Dual Driver/Receiver

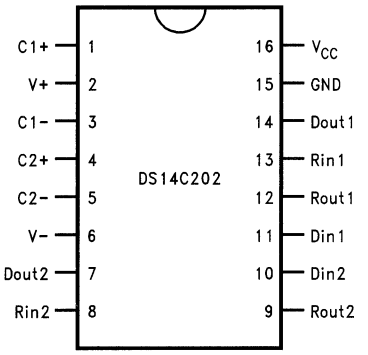
General Description

The DS14C202 is a low power dual driver/receiver featuring an onboard DC to DC convertor. This eliminates the need for ±12V power supplies and requires only a +5V power supply. Only four 0.1 μF capacitors are needed for the DC to DC convertor. The drivers maintain greater than ±5V output signal levels at data rates in excess of 120 kbits/sec when loaded in accordance with the EIA/TIA-232-E specification. I_{CC} is specified at TBD mA maximum, making the device ideal for battery and power conscious applications. The drivers' slew rate is set internally, eliminating the need for external slew rate capacitors. The device is designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The driver inputs and receiver outputs are TTL and CMOS compatible. DS14C202 driver outputs and receiver inputs meet EIA/TIA-232-E and ITU-T V.28 standards. This device is an enhanced version of the DS14C232 that requires smaller external capacitors (0.1 μF) and has a higher data rate of 120 kbit/sec.

Features

- Used only four small 0.1 μF capacitors for DC to DC convertor
- Operates over 120 kbit/sec
- Pin compatible with MAX202, MAX232A and others
- Single +5V power supply
- Low power
- DS14C202 meets EIA/TIA-232-E and ITU-T V.28 standards
- CMOS technology
- Package efficiency—2 drivers and 2 receivers
- Available in Plastic DIP and Narrow and Wide SOIC packages
- Extended temperature range: −40°C to +85°C

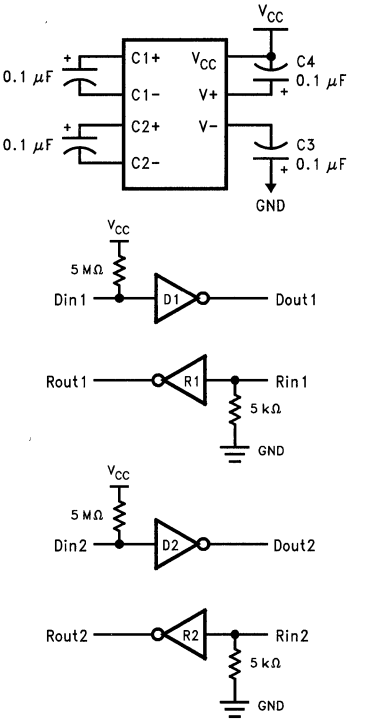
Connection Diagram



TL/F/12622–1

Order Number DS14C202CN, DS14C202CM, DS14C202TN, DS14C202TM, DS14C202CWM or DS14C202TWM
See NS Package Number M16A, M16B or N16A

Functional Diagram



TL/F/12622–2

National Semiconductor

DS14C232
Low Power +5V Powered TIA/EIA-232 Dual Driver/Receiver

General Description

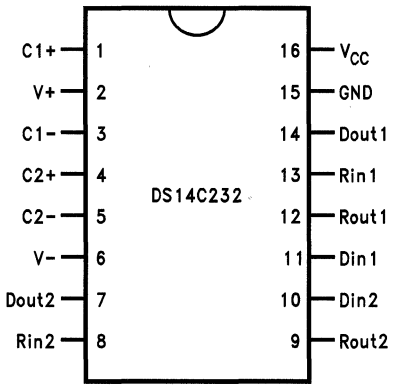
The DS14C232 is a low power dual driver/receiver featuring an onboard DC to DC converter, eliminating the need for ±12V power supplies. The device only requires a +5V power supply. I_{CC} is specified at 3.0 mA maximum, making the device ideal for battery and power conscious applications. The drivers' slew rate is set internally and the receivers feature internal noise filtering, eliminating the need for external slew rate and filter capacitors. The device is designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The driver inputs and receiver outputs are TTL and CMOS compatible. DS14C232C driver outputs and receiver inputs meet TIA/EIA-232-E (RS-232) and CCITT V.28 standards.

Features

- Pin compatible with industry standard MAX232, LT1081, ICL232 and TSC232
- Single +5V power supply
- Low power—I_{CC} 3.0 mA maximum
- DS14C232C meets TIA/EIA-232-E (RS-232) and CCITT V.28 standards
- CMOS technology
- Receiver Noise Filter
- Package efficiency—2 drivers and 2 receivers
- Available in Plastic DIP, Narrow and Wide SOIC packages
- TIA/EIA-232 compatible extended temperature range options:

DS14C232T	−40°C to +85°C
DS14C232	−55°C to +125°C

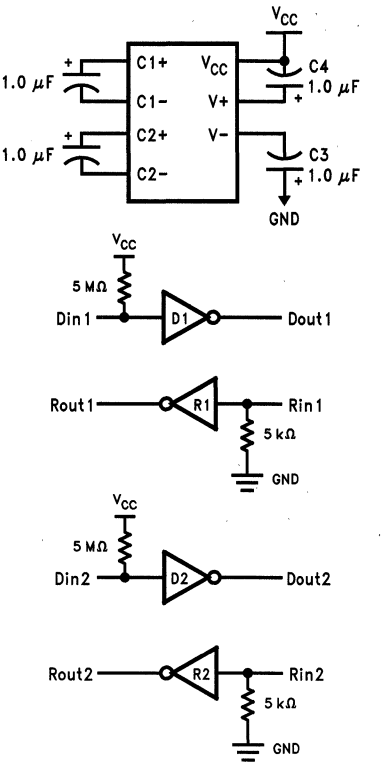
Connection Diagrams



TL/F/10744–1

Order Number DS14C232CN, DS14C232TN, DS14C232CM, DS14C232TM, DS14C232CWM or DS14C232TWM
See NS Package Number N16A, M16A or M16B

Functional Diagram



TL/F/10744–2

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Supply Voltage, V_{CC}	−0.3V to 6V
V^+ Pin	$(V_{CC} - 0.3)$V to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to $(V_{CC} + 0.3)$V
Driver Output Voltage	$(V^+ + 0.3)$V to $(V^- - 0.3)$V
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to $(V_{CC} + 0.3)$V
Junction Temperature	+150°C
Maximum Package Power Dissipation @ 25°C (Note 6)	
N Package	1698 mW
M Package	1156 mW
WM Package	1376 mW
Short Circuit Duration, D_{OUT}	Continuous
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 sec.)	+260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.5 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C232C	0	+70	°C
DS14C232T	−40	+85	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DC TO DC CONVERTER CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.5		V
I_{CC}	Supply (V_{CC}) Current	No Load			1.0	3.0	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq$ 2.0V		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq$ 0.8V		−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	8.0		V
V_{OL}	Low Level Output Voltage	R_L = 3 kΩ			−7.0	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	(Note 3)	−30	−15	−5.0	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2V		5.0	11	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = 0V = GND		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage	V_{CC} = 5.0V			1.9	2.4	V
		V_{CC} = 5.0V ±10%			1.9	2.6	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis	T_A = 0°C to +85°C		0.2	0.4	1.0	V
		T_A = −40°C to 0°C		0.1	0.4	1.0	V
R_{IN}	Input Resistance	T_A = 0°C to +85°C	−15V ≤ V_{IN} ≤ +15V	3.0	4.7	7.0	kΩ
		T_A = −40°C to 0°C (Note 8)		3.0	4.7	10	kΩ
I_{IN}	Input Current	V_{IN} = +15V	0°C to +85°C	+2.14	+3.75	+5.0	mA
		V_{IN} = +3V		+0.43	+0.64	+1.0	mA
		V_{IN} = −3V		−1.0	−0.64	−0.43	mA
		V_{IN} = −15V		−5.0	−3.75	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA		3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA			0.15	0.4	V

COMMERCIAL

Switching Characteristics Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay Low to High	R_L = 3 kΩ, C_L = 50 pF	*Figure 1* and *Figure 2*		1.0	4.0	μs
t_{PHL}	Propagation Delay High to Low				1.0	4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.1	1.0	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF	(Note 7)	4.0		30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF			4.5		V/μs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay Low to High	Input Pulse Width > 10 μs, C_L = 50 pF *(Figures 3* and *4)*			2.9	6.5	μs
t_{PHL}	Propagation Delay High to Low				2.5	6.5	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.4	2.0	μs
t_{nw}	Noise Pulse Width Rejected	*(Figures 3* and *4)*	T_A = 0°C to +85°C		0.7	0.5	μs
			T_A = −40°C to 0°C		0.7	0.3	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{OS+} and I_{OS-} values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 30 kHz.

Note 5: All typicals are given for V_{CC} = 5.0V.

Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N Package 15.6 mW/°C, M Package 10.6 mW/°C and WM Package 12.7 mW/°C.

Note 7: Slew rate is defined as $\Delta V/\Delta t$, measured between ±3V level.

Note 8: TIA/EIA-232-E receiver input impedance maximum limit is 7 kΩ.

MIL-STD 883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage, V_{CC}	−0.3V to 6V
V^+ Pin	$(V_{CC} - 0.3)$V to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to $(V_{CC} + 0.3V)$
Driver Output Voltage	$(V^+ + 0.3V)$ to $(V^- - 0.3V)$
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to $(V_{CC} + 0.3V)$
Maximum Package Power Dissipation @ 25°C (Note 8)	
J Package	1520 mW
E Package	2000 mW
Short Circuit Duration, D_{OUT}	Continuous
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 sec.)	+260°C
ESD Rating (HMB, 1.5 kΩ, 100 pF)	≥ 2.5 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C232	−55	+125	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Max	Units
DEVICE CHARACTERISTICS (C1–C4 = 1.0 μF)						
I_{CC}	Supply (V_{CC}) Current	No Load			8.0	mA
DRIVER CHARACTERISTICS						
V_{IH}	High Level Input Voltage			2		V
V_{IL}	Low Level Input Voltage				0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$			100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0V$			100	μA
V_{OH}	High Level Output Voltage	$R_L = 3$ kΩ		5.0		V
V_{OL}	Low Level Output Voltage	$R_L = 3$ kΩ			−5.0	V
I_{OS+}	Output High Short Circuit Current	$V_O = 0V$	(Note 3)	−25		mA
I_{OS-}	Output Low Short Circuit Current	$V_O = 0V$			25	mA
R_O	Output Resistance	$-2V \leq V_O \leq +2V$, $T_A = 25°C$, $V_{CC} = 0V = GND$		300		Ω
RECEIVER CHARACTERISTICS (C1–C4 = 1.0 μF)						
V_{TH}	Input High Threshold Voltage				3.0	V
V_{TL}	Input Low Threshold Voltage			0.2		V
V_{HY}	Hysteresis	$T_A = 25°C, +125°C$		0.1	1.0	V
		$T_A = -55°C$		0.05	1.0	V
R_{IN}	Input Resistance	$V_{IN} = \pm 3V$ and $\pm 15V$, $T_A = 25°C$		3.0	7.0	kΩ
V_{OH}	High Level Output Voltage	$I_O = -3.2$ mA		3.5		V
		$I_O = -20$ μA		4.0		V
V_{OL}	Low Level Output Voltage	$I_O = +3.2$ mA			0.4	V

MIL-STD-883C

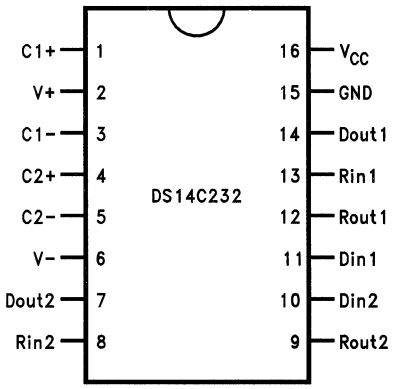
Switching Characteristics Over recommended operating conditions, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Units
DRIVER CHARACTERISTICS (C1–C4 = 1.0 μF)						
t_{PLH}	Propagation Delay Low to High	R_L = 3 kΩ, C_L = 50 pF	*Figures 1* and *2*		4.0	μs
t_{PHL}	Propagation Delay High to Low				4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				1.0	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF	(Note 7)	1.5	30	V/μs
RECEIVER CHARACTERISTICS (C1–C4 = 1.0 μF)						
t_{PLH}	Propagation Delay Low to High	Input Pulse Width > 10 μs			8.0	μs
t_{PHL}	Propagation Delay High to Low	C_L = 50 pF			8.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$	*(Figures 3* and *4)*			2.0	μs

Note 8: Ratings apply to ambient temperature at +25°C. Above this temperature derate: J Package 12.2 mW/°C and E Package 13.3 mW/°C.

Connection Diagrams (Continued)

J Package
16-Lead Dual-In-line Package



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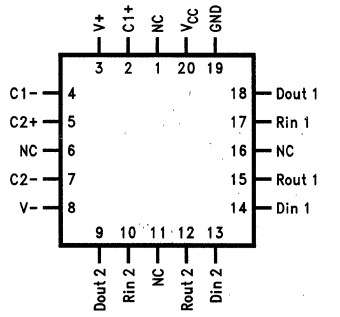
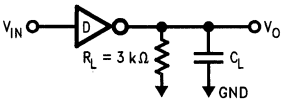
E Package
20-Lead Ceramic Leadless Chip Carrier



TL/F/10744–10

For Complete Military 883 Specifications
See RETS Data Sheet.
Order Number DS14C232J/883 or DS14C232E/883
See NS Package Number E20A or J16A

Parameter Measurement Information



TL/F/10744–3

FIGURE 1. Driver Load Circuit

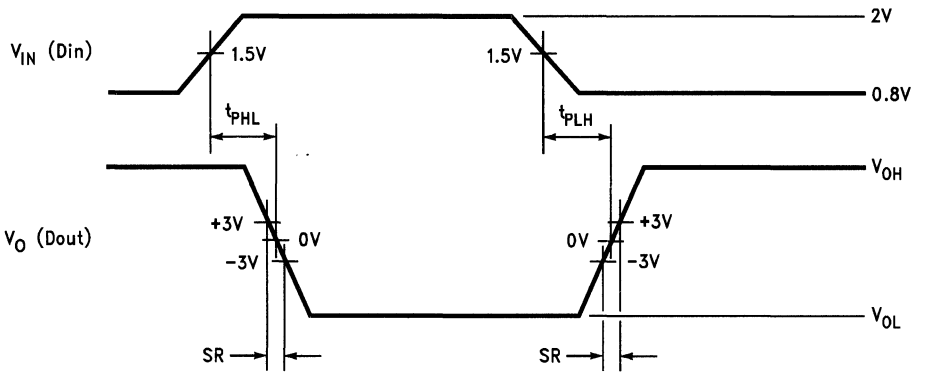


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FIGURE 2. Driver Switching Waveform

Parameter Measurement Information (Continued)

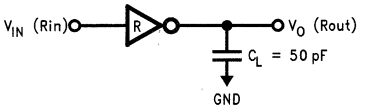

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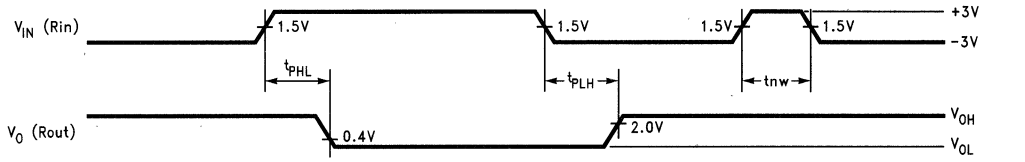
FIGURE 3. Receiver Load Circuit



TL/F/10744–6

FIGURE 4. Receiver Propagation Delays and Noise Rejection (Note 4)

Pin Descriptions

V_{CC} (Pin 16)

Power supply pin for the device, +5V (±10%).

V+ (Pin 2)

Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4-1.0 μF (6.3V). Capacitor value should be larger than 1 μF. This supply is not intended to be loaded externally.

V− (Pin 6)

Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3-1.0 μF (16V). Capacitor value should be larger than 1 μF. This supply is not intended to be loaded externally.

C1+, C1− (Pins 1, 3)

External capacitor connection pins. Recommended capacitor: 1.0 μF (6.3V). Capacitor value should be larger than 1 μF.

C2+, C2− (Pins 4, 5)

External capacitor connection pins. Recommended capacitor: 1.0 μF (16V). Capacitor value should be greater than 1 μF.

D_{IN}1, D_{IN}2 (Pins 11, 10)

Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal active pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input HIGH. Output will be LOW for open inputs.

D_{OUT}1, D_{OUT}2 (Pins 14, 7)

Driver output pins conform to TIA/EIA-232-E levels.

R_{IN}1, R_{IN}2 (Pins 13, 8)

Receiver input pins accept TIA/EIA-232-E input voltages (±25V). Receivers feature a noise filter and guaranteed hysteresis of 100 mV. Unused receiver input pins may be left open. Internal input resistor 4.7 kΩ pulls input low, providing a failsafe high output.

R_{OUT}1, R_{OUT}2 (Pins 12, 9)

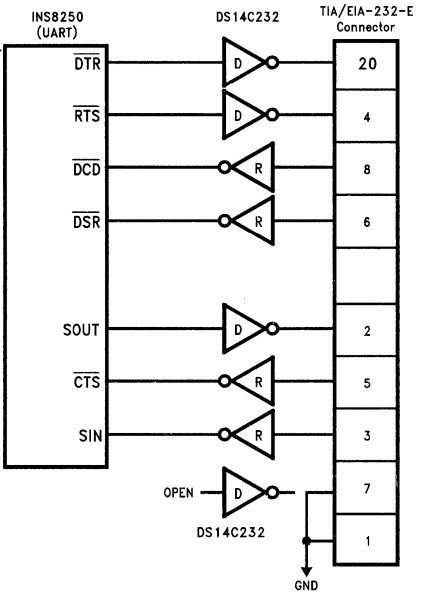
Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (Pin 15)

Ground Pin.

Typical Application Information

Application of DS14C232 and INS8250



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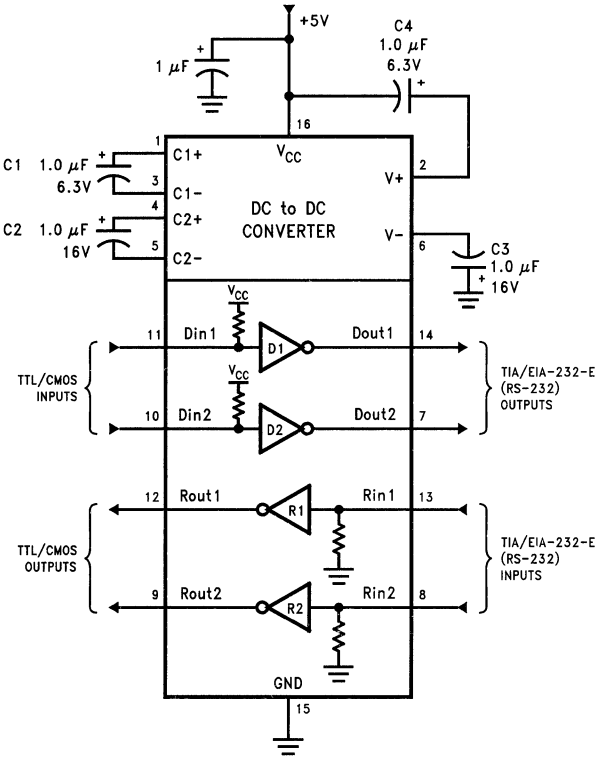
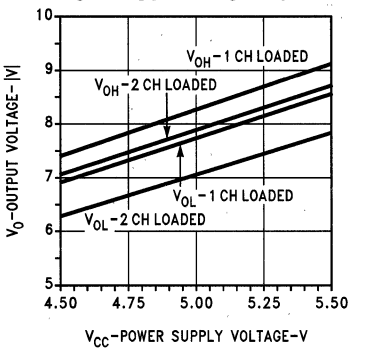
Typical Connection Diagram



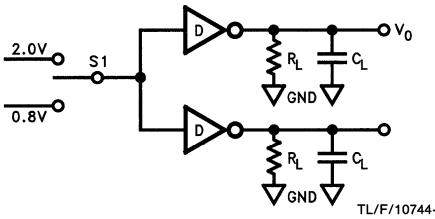
TL/F/10744–9

Typical Performance Characteristics

DRIVER V_{OH} & V_{OL} vs POWER SUPPLY VOLTAGE

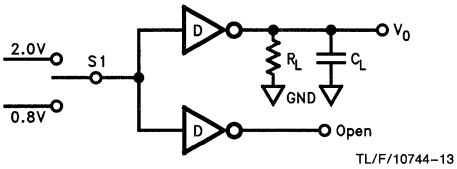


TL/F/10744–11



TL/F/10744–12

V_{CC} = 5.0V, R_L = 3 kΩ, C_L = 15 pF (includes jig and probe capacitance), C_P = 1 μF



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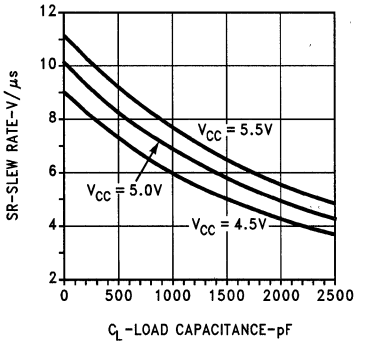
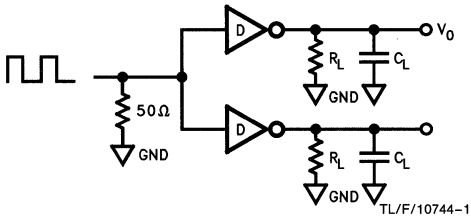
S1	V_O
2.0V	V_{OL}
0.8V	V_{OH}

DRIVER SLEW RATE vs POWER SUPPLY VOLTAGE & LOAD CAPACITANCE

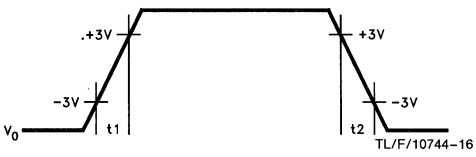


TL/F/10744–14



TL/F/10744–15

T_a = 25°C, R_L = 5 kΩ, C_P = 1 μF, f = 30 KHz



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SR = 6V/t1 or 6V/t2, whichever is greater.

National Semiconductor

DS14C237
Single Supply TIA/EIA-232 5 x 3 Driver/Receiver

General Description

The DS14C237 is a five driver, three receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors.

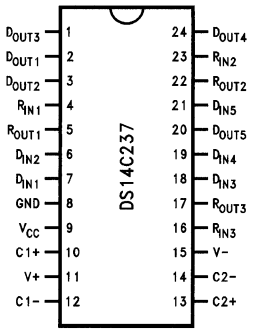
One device is capable of implementing a complete nine pin interface. The combination of its extended operating temperature range and low power requirement makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Internal driver slew rate control
- Receiver Noise Filtering
- Operates above 120 kbits/sec
- Direct replacement for MAX237
- Industrial temperature range option-DS14C237T (−40°C to +85°C)

2

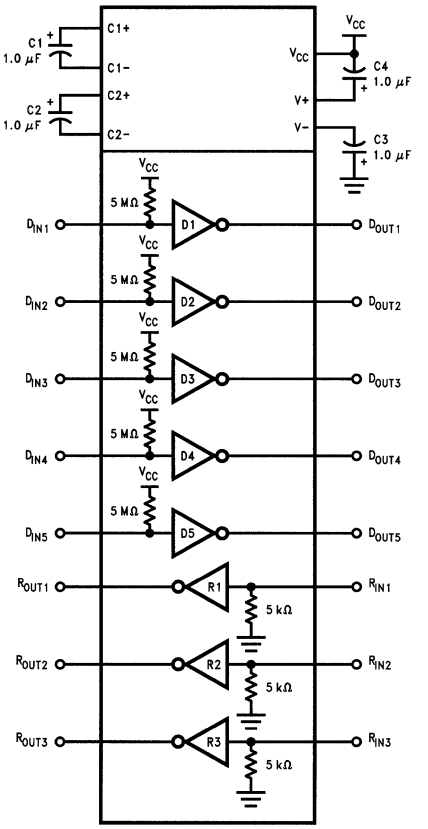
Connection Diagram



TL/F/11284–1

Order Number
DS14C237N, DS14C237WM,
DS14C237TN or DS14C237TWM
See NS Package Number M24B or NA24G

Functional Diagram



TL/F/11284–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +15V
V^- Pin	+0.3V to −15V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
N Package	2400 mW
WM Package	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temperature (T_A)			
DS14C237	0	+70	°C
DS14C237T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.5		V
I_{CC}	Supply Current (V_{CC})	No Load			6.5	10	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	7.4		V
V_{OL}	Low Level Output Voltage				−6.3	−5.0	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	(Note 3)	−30	−15	−5.0	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		5.0	12	30	mA
R_O	Output Resistance	$-2V \leq V_O \leq +2V$, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.9	2.4	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis			0.2	0.4	1.0	V
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V		2.14	3.8	5.0	mA
		V_{IN} = +3V		0.43	0.6	1.0	mA
		V_{IN} = −3V		−1.0	−0.6	−0.43	mA
		V_{IN} = −15V		−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA		3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA			0.25	0.4	V

Switching Characteristics

Over recommended operating conditions, unless otherwise specified (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ C_L = 50 pF *Figures 1* and *2*		0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW			0.6	4.0	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.1	1.0	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF	4.0	15	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF	3.0	5.0		V/μs
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs C_L = 50 pF *Figures 3* and *4*		2.0	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW			2.8	6.5	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.8	2.0	μs
t_{nw}	Noise Pulse Width Rejected			2.5	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

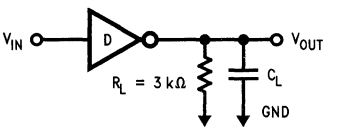
Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 64 kHz (128 kbits/sec). Drive AC Input Waveform for test purposes: $t_r = t_f \leq$ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

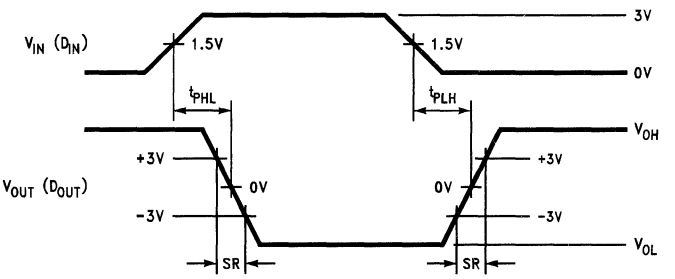
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N package 20 mW/°C and WM package 13.5 mW/°C.

Parameter Measurement Information



TL/F/11284–4

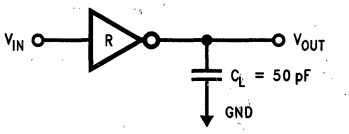
FIGURE 1. Driver Load Circuit



TL/F/11284–5

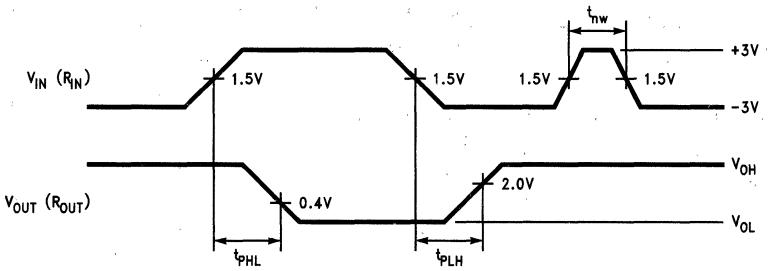
FIGURE 2. Driver Switching Waveform

Parameter Measurement Information (Continued)



TL/F/11284–6

FIGURE 3. Receiver Load Circuit



TL/F/11284–7

FIGURE 4. Receiver Propagation Delays and Noise Rejection

Pin Description

V_{CC} (Pin 9)—Power supply pin for the device, +5V (±10%).

V^+ (Pin 11)—Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μF (6.3V). This supply is not intended to be loaded externally.

V^- (Pin 15)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μF (16V). This supply is not intended to be loaded externally.

$C1^+$, $C1^-$ (Pins 10, 12)—External capacitor connection pins. Recommended capacitor—1.0 μF (6.3V).

$C2^+$, $C2^-$ (Pins 13, 14)—External capacitor connection pins. Recommended capacitor—1.0 μF (16V).

D_{IN} 1–5 (Pins 7, 6, 18, 19, 21)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–5 (Pins 2, 3, 1, 24, 20)—Driver output pins conform to TIA/EIA-232-E levels.

R_{IN1} 1–3 (Pins 4, 23, 16)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–3 (Pins 5, 22, 17)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (Pin 8)—Ground Pin.

National Semiconductor

DS14C238
Single Supply TIA/EIA-232 4 x 4 Driver/Receiver

General Description

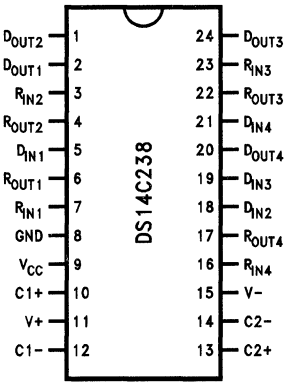
The DS14C238 is a four driver, four receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors.

The combination of its extended operating temperature range and low power requirement makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Internal driver slew rate control
- Receiver noise filtering
- Operates above 120 kbits/sec
- Direct replacement for MAX238
- Industrial temperature range option—DS14C238T (−40°C to +85°C)

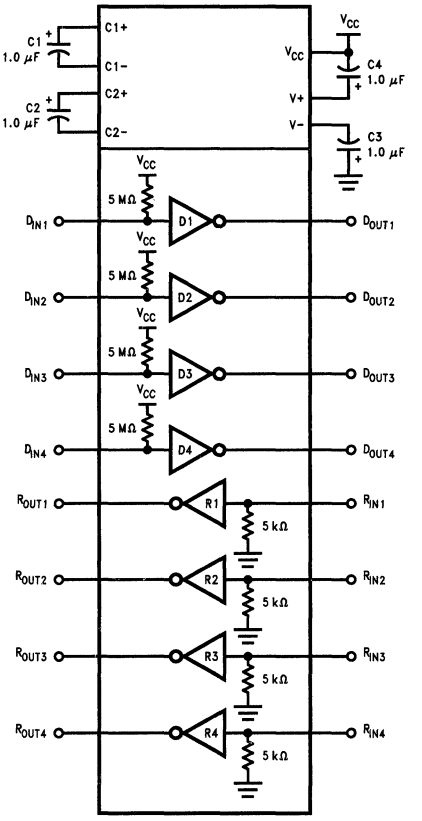
Connection Diagram



TL/F/11282–1

Order Number DS14C238N, DS14C238WM, DS14C238TN or DS14C238TWM
See NS Package Numbers M24B or NA24G

Functional Diagram



TL/F/11282–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V+ Pin	(V_{CC} −0.3V) to +15V
V− Pin	+0.3V to −15V
Driver Input Voltage	−0.3V to (V_{CC} +0.3V)
Driver Output Voltage	(V+ +0.3V) to (V− −0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} +0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
N Package	2400 mW
WM Package	1400 mW
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering, 4 Seconds)	+260°C
Short Circuit Duration (D_{OUT})	Continuous
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C238	0	+70	°C
DS14C238T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V−	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.0		V
I_{CC}	Supply Current (V_{CC})	No Load			7.0	10	mA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} ≥ 2.0V		−10		+10	μA
I_{IL}	Low Level Input Current	V_{IN} ≤ 0.8V		−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	7.4		V
V_{OL}	Low Level Output Voltage				−6.3	−5.0	V
I_{OS}+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	(Note 3)	−30	−15	−5.0	mA
I_{OS}−	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		5.0	12	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω

Electrical Characteristics (Continued)

Over recommended operating conditions, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold Voltage			1.9	2.4	V
V_{TL}	Input Low Threshold Voltage		0.8	1.5		V
V_{HY}	Hysteresis		0.2	0.4	1.0	V
R_{IN}	Input Resistance		3.0	4.5	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V	2.14	3.8	5.0	mA
		V_{IN} = +3V	0.43	0.6	+1.0	mA
		V_{IN} = −3V	−1.0	−0.6	−0.43	mA
		V_{IN} = −15V	−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA	3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA	4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA		0.25	0.4	V

Switching Characteristics

Over recommended operating conditions, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ, C_L = 50 pF (*Figures 1* and *2*)		0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW			0.6	4.0	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.1	1.0	μs
SR1	Output Slew Rate	R_L = 3kΩ to 7 kΩ, C_L = 50 pF	4.0	15	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF	3.0	5.0		V/μs
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs, C_L = 50 pF (*Figures 3* and *4*)		2.0	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW			2.8	6.5	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.8	2.0	μs
t_{NW}	Noise Pulse Width Rejected			2.5	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

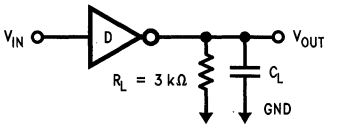
Note 3: I_{OS}+ and I_{OS}− values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \leq$ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

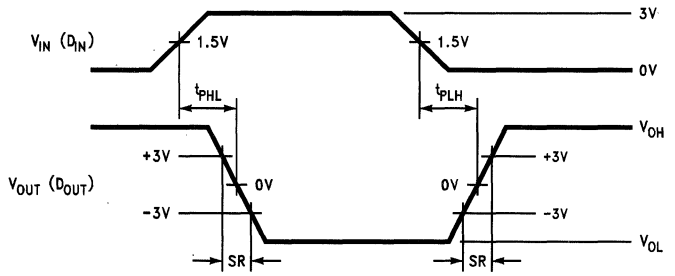
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N package 20 mW/°C and WM package 13.5 mW/°C.

Parameter Measurement Information



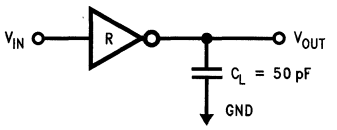
TL/F/11282–4

FIGURE 1. Driver Load Circuit



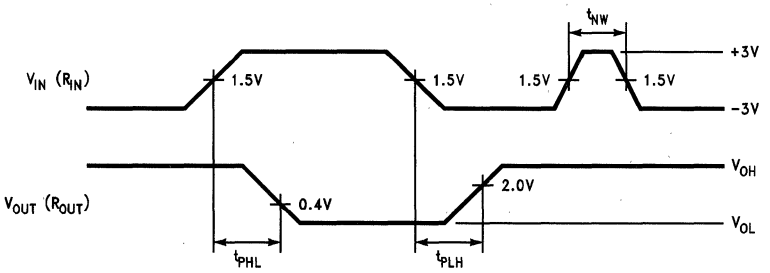
TL/F/11282–5

FIGURE 2. Driver Switching Waveform



TL/F/11282–6

FIGURE 3. Receiver Load Circuit



TL/F/11282–7

FIGURE 4. Receiver Propagation Delays and Noise Rejection

Pin Descriptions

V_{CC} (pin 9)—Power supply pin for the device, +5V (±10%).

V+ (pin 11)—Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μF (6.3V). This supply is not intended to be loaded externally.

V− (pin 15)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (pins 10 and 12)—External capacitor connection pins. Recommended capacitor – 1.0 μF (6.3V).

C2+, C2− (pins 13 and 14)—External Capacitor connection pins. Recommended capacitor – 1.0 μF (16V).

D_{IN} 1–5 (pins 7, 6, 8, 18, 19, and 21)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–5 (pins 2, 3, 1, 24, and 20)—Driver output pins conform to TIA/EIA-232-E levels.

R_{IN1} 1–3 (pins 4, 23, and 16)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–3 (pins 5, 22, and 17)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (pin 8)—Ground Pin.

National Semiconductor

DS14C239
Dual Supply TIA/EIA-232 3 x 5 Driver/Receiver

General Description

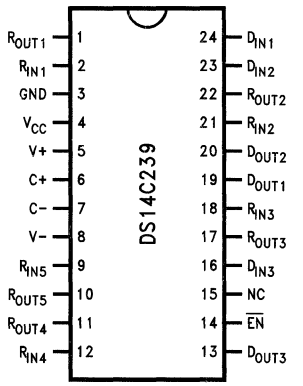
The DS14C239 is a three driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates −12V supply by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply and a positive voltage power supply (+7.5V to +13.2V). Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors. With the addition of TRI-STATE® receiver outputs, device power consumption is kept to a minimum.

The combination of its low power requirement and extended operating temperature range makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Low power requirement: I^+ = 10 mA max
  I_{CC} = 1 mA max
- Internal driver slew rate control
- Receiver Noise Filtering
- Operates above 120 kbits/sec
- TRI-STATE Receiver Outputs
- Direct replacement for MAX239
- Industrial temperature range option—DS14C239T (−40°C to +85°C)

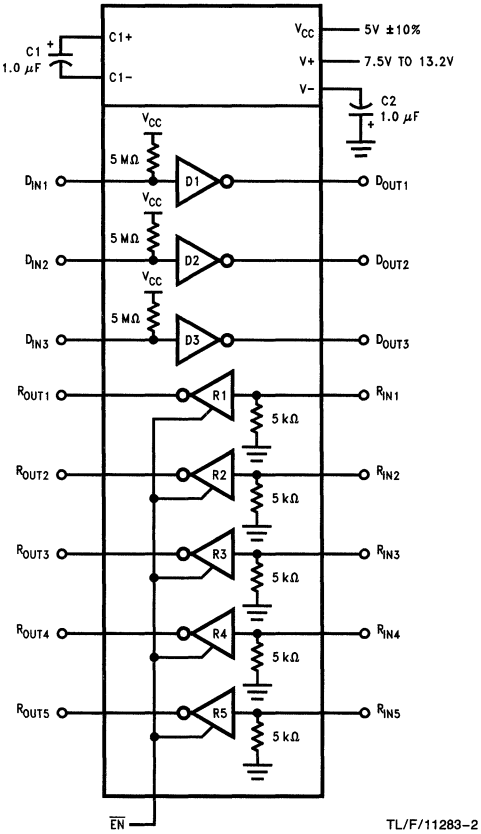
Connection Diagram



TL/F/11283–1

Order Number DS14C239N, DS14C239WM, DS14C239TN or DS14C239TWM
See NS Package Number M24B or NA24G

Functional Diagram



TL/F/11283–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +15V
V^- Pin	+0.3V to −15V
Driver Input Voltage	− 0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
N Package	2400 mW
WM Package	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Supply Pin (V^+)	7.5	13.2	V
Operating Free Air Temp. (T_A)			
DS14C239	0	+70	°C
DS14C239T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DEVICE CHARACTERISTICS						
V^-	Negative Power Supply	R_L = 3 kΩ, C1, C2 = 1.0 μF, D_{IN} = 2.0V		−9.5		V
I^+	Supply Current (V^+)	No Load		4	10	mA
I_{CC}	Supply Current (V_{CC})	No Load		0.1	1.0	mA
DRIVER CHARACTERISTICS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$	−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$	−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ	5.0	8.7		V
V_{OL}	Low Level Output Voltage			−8.0	−5.0	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V	−40	−20	−5.0	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V	5.0	16	40	mA
R_O	Output Resistance	$-2V \leq V_O \leq +2V$, $V_{CC} = V^+ = GND = 0V$	300			Ω
RECEIVER CHARACTERISTICS						
V_{TH}	Input High Threshold Voltage	T_A = 25°C		2	2.4	V
		T_A = −40°C to +85°C		2	2.6	V
V_{TL}	Input Low Threshold Voltage		0.8	1.5		V
V_{HY}	Hysteresis	T_A = 25°C	0.2	0.5	1.0	V
		T_A = −40°C to +85°C	0.1	0.5	1.0	V

Electrical Characteristics (Continued)

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V		2.14	3.8	5.0	mA
		V_{IN} = +3V		0.43	0.6	1.0	mA
		V_{IN} = −3V		−1.0	−0.6	−0.43	mA
		V_{IN} = −15V		−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −3.2 mA		3.5	4.5		V
		V_{IN} = −3V, I_O = −20 μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +3.2 mA			0.25	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.4		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq$ 2.4V		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq$ 0.8V		−10		+10	μA
I_{OZ}	Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}		−10	0.1	+10	μA

Switching Characteristics

Over recommended operating conditions, unless otherwise specified (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ, C_L = 50 pF (*Figures 1* and *2*)			0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW				0.7	4.0	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0	1.0	μs
SR1	Output Slew Rate	R_L = 3kΩ to 7 kΩ, C_L = 50 pF, $V^+ \leq$ 10.35V		4.0	17	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF, $V^+ \leq$ 10.35V		3.0	6.4		V/μs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs, C_L = 50 pF (*Figures 3* and *4*)			2.1	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW				2.9	6.5	μs
t_{sk}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.8	2.0	μs
t_{PLZ}		(*Figures 5* and *7*)			0.25	2.0	μs
t_{PZL}					0.70	2.0	μs
t_{PHZ}		(*Figures 5* and *6*)			0.25	2.0	μs
t_{PZH}					0.70	2.0	μs
t_{nw}	Noise Pulse Width Rejected	(*Figures 3* and *4*)			2.0	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

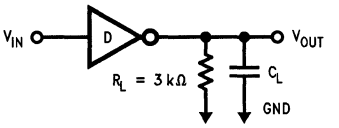
Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \leq$ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for V_{CC} = 5.0V and T_A = +25°C, V^+ = 10.35V.

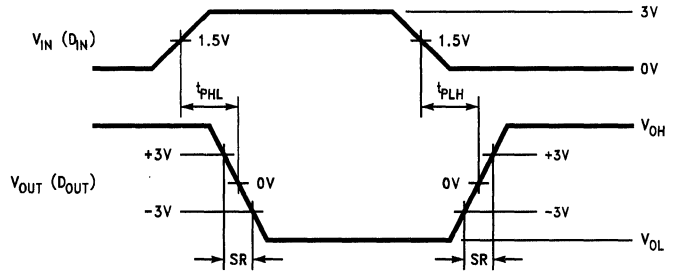
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: N package 20 mW/°C and WM package 13.5 mW/°C.

Parameter Measurement Information



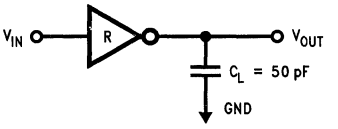
TL/F/11283–4

FIGURE 1. Driver Load Circuit



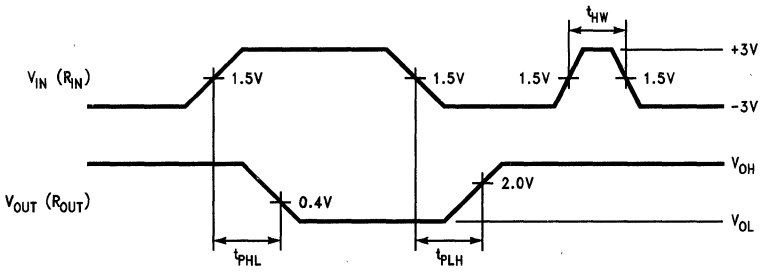
TL/F/11283–5

FIGURE 2. Driver Switching Waveform



TL/F/11283–6

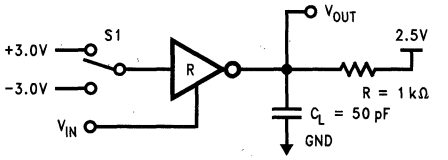
FIGURE 3. Receiver Load Circuit



TL/F/11283–7

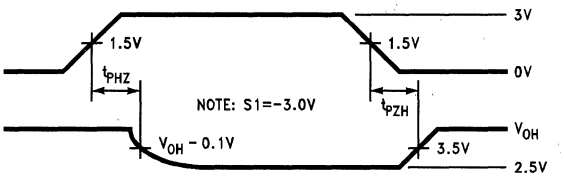
FIGURE 4. Receiver Propagation Delays and Noise Rejection

Parameter Measurement Information (Continued)



TL/F/11283–8

FIGURE 5. Receiver Disable Load Circuit



TL/F/11283–9

FIGURE 6. Receiver TRI-STATE Timing (t_{PHZ}, t_{PZH})

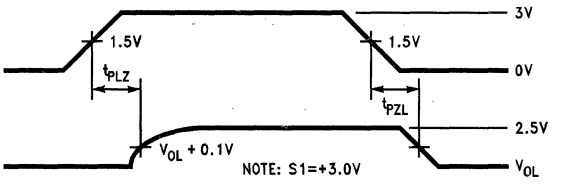


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FIGURE 7. Receiver TRI-STATE Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 4)—Power supply pin for the device, +5V (±10%).

V^+ (pin 5)—Positive supply for TIA/EIA-232-E drivers. Specified at 7.5V minimum and 13.2V maximum.

V^- (pin 8)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C2 = 1.0 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (pins 6, 7)—External capacitor connection pins. Recommended capacitor—1.0 μF (16V).

$\overline{EN}$ (pin 14)—Controls the Receiver output TRI-STATE Circuit. A High level on this pin will disable the Receiver Output.

D_{IN} 1–3 (pins 24, 23, 16)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–3 (pins 19, 20, 13)—Driver output pins conform to TIA/EIA-232-E levels.

R_{IN} 1–5 (pins 2, 21, 18, 12, 9)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 100 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (pins 1, 22, 17, 11, 10)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (pin 3)—Ground pin.

National Semiconductor

DS14C241
Single Supply TIA/EIA-232 4 x 5 Driver/Receiver

General Description

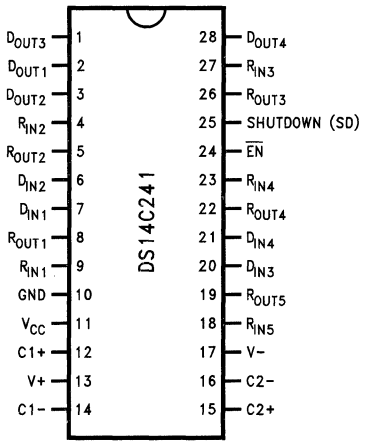
The DS14C241 is four driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC–DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors. With the addition of TRI-STATE® receiver outputs and a shutdown mode, device power consumption is kept to a minimum.

The combination of its low power requirement and extended operating temperature range makes this device an ideal choice for a wide variety of commercial, industrial, and battery powered applications

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC–DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Shutdown mode—I_{CX} 10 μA max
- Internal driver slew rate control
- Receiver noise filtering
- Operates above 120 kbits/sec
- TRI-STATE receiver outputs
- Direct replacement for MAX241
- Industrial temperature range option—DS14C241T (−40°C to +85°C)

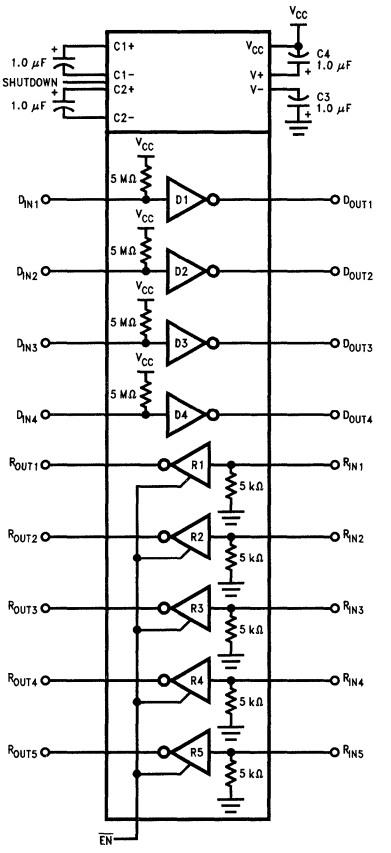
Connection Diagram



TL/F/11281–1

Order Number DS14C241WM or DS14C241TWM
See NS Package Number M28B

Functional Diagram



TL/F/11281–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +15V
V^- Pin	+0.3V to −15V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6)	
WM Package	1520 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Free Air Temp. (T_A)			
DS14C241	0	+70	°C
DS14C241T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 0.8V			9.0		V
V^-	Negative Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 μF, D_{IN} = 2.0V			−8.0		V
I_{CC}	Supply Current (V_{CC})	No Load			8.5	10	mA
I_{CX}	Supply Current Shutdown	R_L = 3 kΩ, SD = V_{CC}			1.0	10	μA
V_{IH}	High Level Enable Voltage		SD	2.4		V_{CC}	V
V_{IL}	Low Level Enable Voltage			GND		0.8	V
I_{IH}	High Level Enable Current			−10		+10	μA
I_{IL}	Low Level Enable Current			−10		+10	μA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} ≥ 2.0V		−10		+10	μA
I_{IL}	Low Level Input Current	V_{IN} ≤ 0.8V		−10		+10	μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		5.0	7.5		V
V_{OL}	Low Level Output Voltage				−6.5	−5.0	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V		−30	−15	−5.0	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		5.0	12	30	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.9	2.4	V
V_{TL}	Input Low Threshold Voltage			0.8	1.5		V
V_{HY}	Hysteresis			0.2	0.4	1.0	V
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ

Electrical Characteristics (Continued)

Over recommended operating conditions, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
I_{IN}	Input Current	$V_{IN} = +15V$		2.14	3.8	5.0	mA
		$V_{IN} = +3V$		0.43	0.6	1.0	mA
		$V_{IN} = -3V$		−1.0	−0.6	−0.43	mA
		$V_{IN} = -15V$		−5.0	−3.8	−2.14	mA
V_{OH}	High Level Output Voltage	$V_{IN} = -3V$, $I_O = -3.2$ mA		3.5	4.6		V
		$V_{IN} = -3V$, $I_O = -20$ μA		4.0	4.9		V
V_{OL}	Low Level Output Voltage	$V_{IN} = +3V$, $I_O = +3.2$ mA			0.25	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.8V$		−10		+10	μA
I_{OZ}	Output Leakage Current	$\overline{EN} = V_{CC}$, $0V \leq R_{OUT} \leq V_{CC}$		−10		+10	μA

Switching Characteristics

Over recommended operating conditions, unless otherwise specified (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	$R_L = 3$ kΩ, $C_L = 50$ pF (*Figures 1* and *2*)			0.7	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW				0.6	4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.1	1.0	μs
SR1	Output Slew Rate	$R_L = 3$ kΩ to 7 kΩ, $C_L = 50$ pF		4.0	15	30	V/μs
SR2	Output Slew Rate	$R_L = 3$ kΩ, $C_L = 2500$ pF		3.0	5.0		V/μs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	Input Pulse Width > 10 μs, $C_L = 50$ pF (*Figures 3* and *4*)			2.0	6.5	μs
t_{PHL}	Propagation Delay HIGH to LOW				2.8	6.5	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.8	2.0	μs
t_{PLZ}		(*Figures 5* and *7*)			0.1	2.0	μs
t_{PZL}					0.6	2.0	μs
t_{PHZ}		(*Figures 5* and *6*)			0.2	2.0	μs
t_{PZH}					0.6	2.0	μs
t_{NW}	Noise Pulse Width Rejected	(*Figures 3* and *4*)			2.5	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

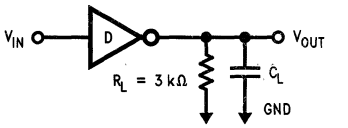
Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

Note 4: Receiver AC input waveform for test purposes: $t_r = t_f = 200$ ns, $V_{IH} = 3V$, $V_{IL} = -3V$, f = 64 kHz (128 kbits/sec). Driver AC input waveform for test purposes: $t_r = t_f \leq 10$ ns, $V_{IH} = 3V$, $V_{IL} = 0V$, f = 64 kHz (128 kbits/sec).

Note 5: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$.

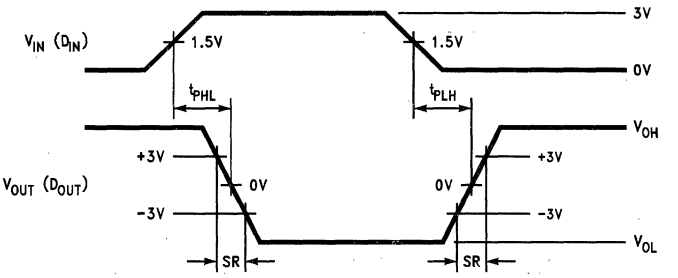
Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: WM package 14.3 mW/°C.

Parameter Measurement Information



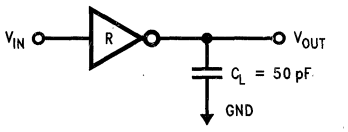
TL/F/11281–4

FIGURE 1. Driver Load Circuit



TL/F/11281–5

FIGURE 2. Driver Switching Waveform



TL/F/11281–6

FIGURE 3. Receiver Load Circuit

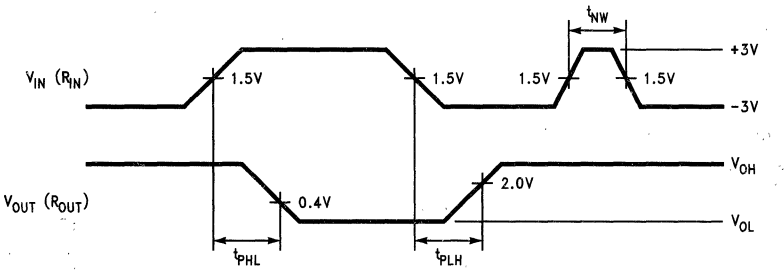


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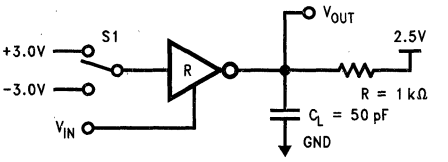
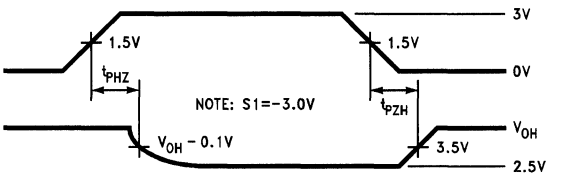
FIGURE 4. Receiver Propagation Delays and Noise Rejection



TL/F/11281–8

FIGURE 5. Receiver Disable Load Circuit

Parameter Measurement Information (Continued)



TL/F/11281–9

FIGURE 6. Receiver TRI-STATE Timing (t_{PHZ}, t_{PZH})

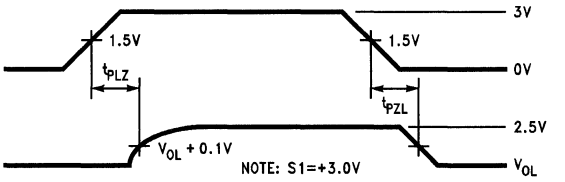


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FIGURE 7. Receiver TRI-STATE Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 11)—Power supply pin for the device, +5V (±10%).

V^+ (pin 13)—Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor: C4 = 1.0 μF (6.3V). This supply is not intended to be loaded externally.

V^- (pin 17)—Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor: C3 = 1.0 μF (16V). This supply is not intended to be loaded externally.

$C1^+$, $C1^-$ (pins 12 and 14)—External capacitor connection pins. Recommended capacitor—1.0 μF (6.3V).

$C2^+$, $C2^-$ (pins 15 and 16)—External capacitor connection pins. Recommended capacitor—1.0 μF (16V).

$\overline{EN}$ (pin 24)—Controls the Receiver output TRI-STATE Circuit. A HIGH level on this pin will disable the Receiver Output.

SHUTDOWN (SD) (pin 25)—A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA. Providing a low power state.

D_{IN} 1–4 (pins 7, 6, 20 and 21)—Driver input pins are TTL/CMOS compatible. Inputs of unused drivers may be left open, an internal pull-up resistor (500 kΩ minimum, typically 5 MΩ) pulls input to V_{CC}. Output will be LOW for open inputs.

D_{OUT} 1–4 (pins 2, 3, 1 and 28)—Driver output pins conform to TIA/EIA-232-E levels.

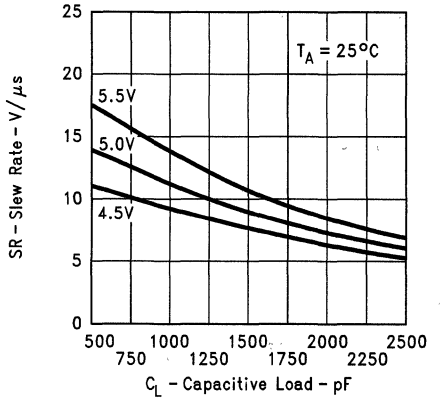
R_{IN} 1–5 (pins 9, 4, 27, 23 and 18)—Receiver input pins accept TIA/EIA-232-E input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 200 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (pins 8, 5, 26, 22 and 19)—Receiver output pins are TTL/CMOS compatible. Receiver output HIGH voltage is specified for both CMOS and TTL load conditions.

GND (pin 10)—Ground pin.

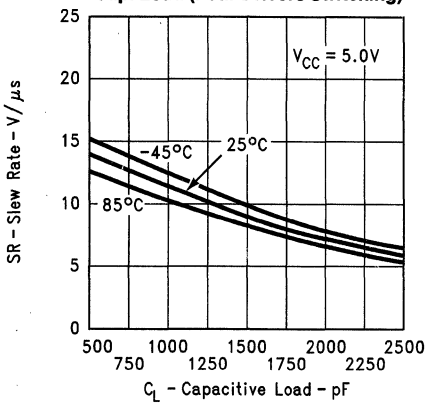
Typical Performance Characteristics

Slew Rate vs Cap. Load vs V_{CC} (Four Drivers)



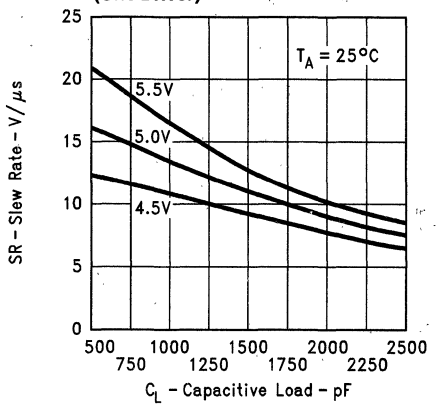
TL/F/11281–11

Slew Rate vs Temperature vs Cap. Load (Four Drivers Switching)



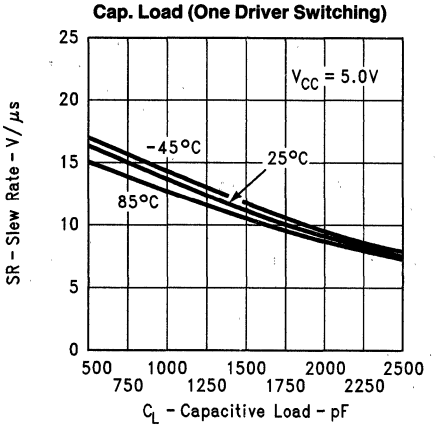
TL/F/11281–12

Slew Rate vs Cap. Load vs V_{CC} (One Driver)



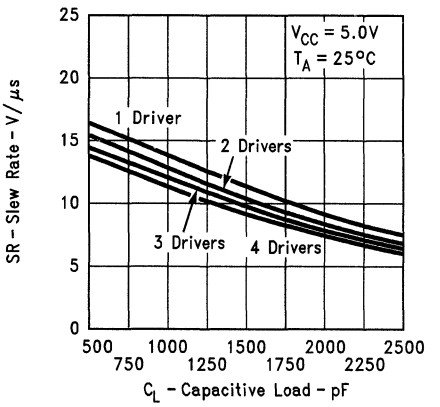
TL/F/11281–13

Slew Rate vs Temperature vs Cap. Load (One Driver Switching)



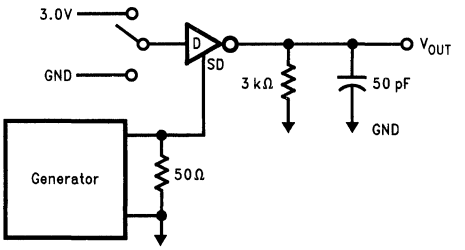
TL/F/11281–14

Driver Slew Rate vs Cap. Load vs Number of Drivers



TL/F/11281–15

Typical Performance Characteristics (Continued)



TL/F/11281–16

FIGURE 8. Driver Shutdown (SD) Delay Test Circuit

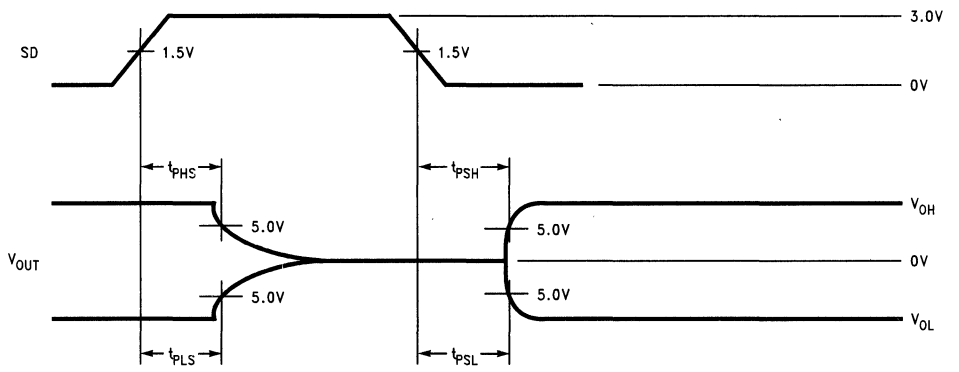


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FIGURE 9. Driver Shutdown (SD) Delay Timing Waveforms

Typical data only.

Symbol	Parameter	Conditions	Typ	Units
t_{PHS}	Propagation Delay High to SD	V_{CC} = 5V(Notes 7 and 8)	124	μs
t_{PLS}	Propagation Delay Low to SD	T_A = 25°C	110	μs
t_{PSH}	Propagation Delay SD to High		114	μs
t_{PSL}	Propagation Delay SD to Low		97	μs

Note 7: Sample size = 10 parts; 3 different datecodes.

Note 8: All drivers are loaded as shown in *Figure 8.*

National Semiconductor

DS14C335
+3.3V Supply TIA/EIA-232 3 x 5 Driver/Receiver

General Description

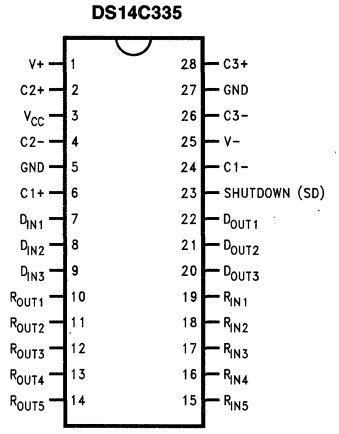
The DS14C335 is three driver, five receiver device which conforms to TIA/EIA-232-E and CCITT V.28 standard specifications. This device employs an internal DC-DC converter to generate the necessary output levels from a +3.3V power supply. A SHUTDOWN (SD) mode reduces the supply current to 10 μA maximum. In the SD mode, one receiver is active, allowing ring indicator (RI) to be monitored. PC Board space consumption is minimized by the availability of Shrink Small Outline Packaging (SSOP).

This device's low power requirement and small footprint makes it an ideal choice for Laptop and Notebook applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28 specifications
- Operates with single +3.3V power supply
- Low power requirement—I_{CC} 20 mA maximum
- SHUTDOWN mode—I_{CX} 10 μA maximum
- One Receiver (R5) active during SHUTDOWN
- Operates up to 128 kbps—Lap-Link® Compatible
- Flow through pinout
- 4V/μs minimum Slew Rate guaranteed
- Inter-operates with +5V UARTs
- Available in 28-lead SSOP EIAJ Type II package

Connection Diagram



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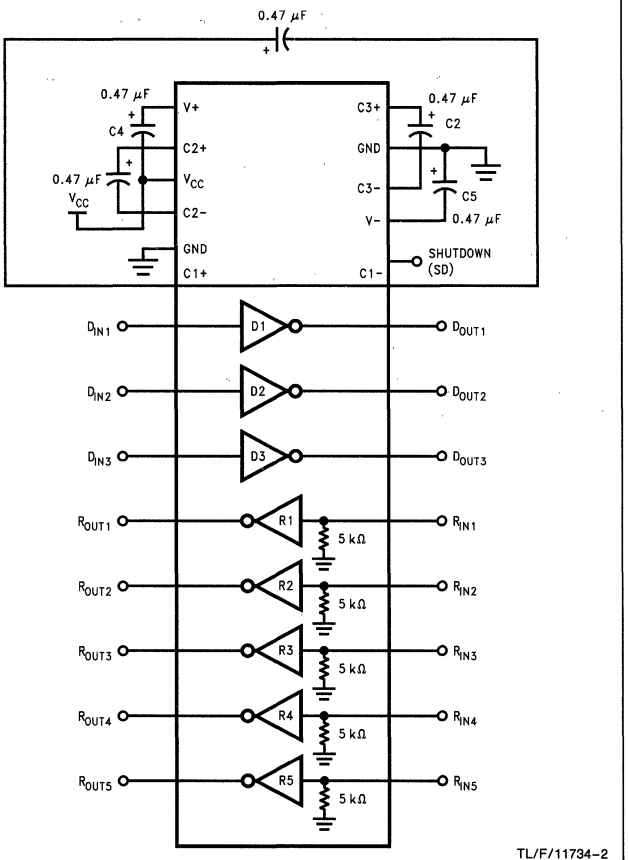
Order Number DS14C335MSA or DS14C335TMSA
See NS Package Number MSA28

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Input Voltage (DIN, SD)	−0.3V to +5.5V
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous
Maximum Package Power Dissipation @ +25°C	
SSOP MSA Package	1286 mW
Derate MSA Package 10.3 mW/°C above +25C	
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 2.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
DC-DC Converter Capacitors (C1–C5)	0.47		µF
Operating Free Air Temperature (T_A)			
DS14C335	0	+70	°C
DS14C335T	−40	+85	°C

Electrical Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DEVICE CHARACTERISTICS								
V^+	Positive Power Supply	No Load C1–C5 = 0.47 µF	D_{IN} = 0.8V			+9.3		V
V^-	Negative Power Supply		D_{IN} = 2.0V			−9.0		V
I_{CC}	Supply Current	No Load				11.5	20	mA
I_{CX}	SHUTDOWN Supply Current	R_L = 3 kΩ, SD = V_{CC}, 5.5V				1.0	10	µA
V_{IH}	High Level Enable Voltage			SD	2.0			V
V_{IL}	Low Level Enable Voltage				GND		0.8	V
I_{IH}	High Level Enable Current	2.0V ≤ V_{IN} ≤ 5.5V	0°C to +85°C				+2.0	µA
			−40°C to 0°C				+4.0	µA
I_{IL}	Low Level Enable Current	GND ≤ V_{IN} ≤ 0.8V			−2.0			µA
DRIVER CHARACTERISTICS								
V_{IH}	High Level Input Voltage		D_{IN}		2.0			V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	2.0V ≤ V_{IN} ≤ 5.5V					+1.0	µA
I_{IL}	Low Level Input Current	GND ≤ V_{IN} ≤ 0.8V			−1.0			µA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ			+5.0	+7.1		V
V_{OL}	Low Level Output Voltage					−6.3	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V (Note 7)			−40	−16.5	−8	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V (Note 7)			6	12.3	40	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V			300			Ω

Electrical Characteristics (Continued)

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Note 4)						
V_{TH}	Input High Threshold Voltage	R1–R5, SD = 0.8V		1.4	2.4	V
		R5, 2.0V ≤ SD ≤ 5.5V		2.0	2.8	V
V_{TL}	Input Low Threshold Voltage	R1–R5, SD = 0.8V	0.4	1.1		V
		R5, 2.0V ≤ SD ≤ 5.5V	0.1	0.5		V
V_{HY}	Hysteresis		50	300		mV
R_{IN}	Input Resistance	V_{IN} = ±3V to ±15V	3.0	3.8	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V	2.14		5.0	mA
		V_{IN} = +3V	0.43		1.0	mA
		V_{IN} = −3V	−1.0		−0.43	mA
		V_{IN} = −15V	−5.0		−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_{OH} = −1 mA	2.4	3.1		V
		V_{IN} = −3V, I_{OH} = −100 μA	2.8	3.28		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_{OL} = +2 mA		0.23	0.4	V

Switching Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ C_L = 50 pF (*Figures 1* and *2*)	0.1	0.6	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0	0.2	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF *(Figure 2)*	4	13	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF *(Figure 2)*	4	10	30	V/μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 5* and *6*) R_L = 3 kΩ C_L = 50 pF		0.48		ms
t_{PSL}	Propagation Delay SD to LOW			1.88		ms
t_{PHS}	Propagation Delay HIGH to SD			0.62		ms
t_{PSH}	Propagation Delay SD to HIGH			1.03		ms
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF (*Figures 3* and *4*)	0.1	0.4	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0.2	0.8	μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 7* and *8*) R_L = 1 kΩ C_L = 50 pF R1–R4 Only		0.13		μs
t_{PSL}	Propagation Delay SD to LOW			1.0		μs
t_{PHS}	Propagation Delay HIGH to SD			0.19		μs
t_{PSH}	Propagation Delay SD to HIGH			0.58		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 3.3V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Receiver characteristics are guaranteed for SD = 0.8V. When SD = 2.0V, receiver five (R5) is active and meets receiver parameters in SHUTDOWN (SD) mode, unless otherwise specified.

Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, V_{IH} = 3V, V_{IL} = 0V, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), $t_r = t_f$ = 200 ns, V_{IH} = 3V, V_{IL} = −3V, duty cycle = 50%.

Note 7: Only one driver output shorted at a time.

Parameter Measurement Information

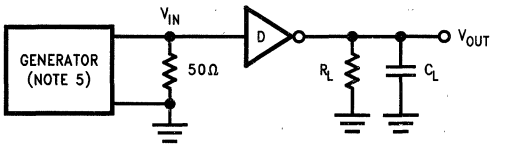

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FIGURE 1. Driver Propagation Delay and Slew Rate Test Circuit

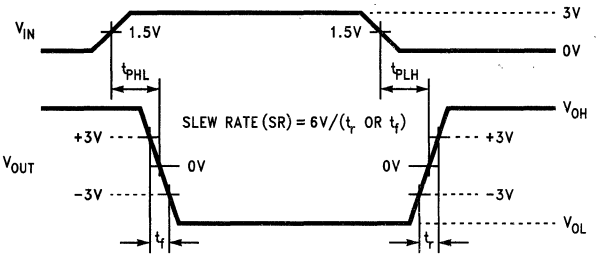

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FIGURE 2. Driver Propagation Delay and Slew Rate Timing

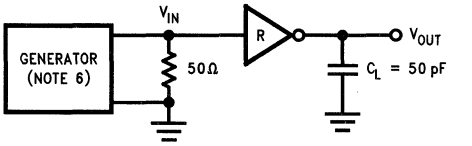

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FIGURE 3. Receiver Propagation Delay Test Circuit

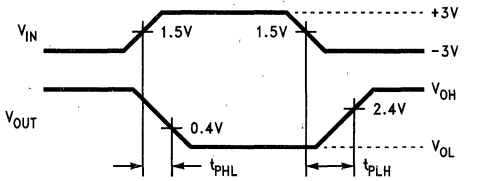

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FIGURE 4. Receiver Propagation Delay Timing

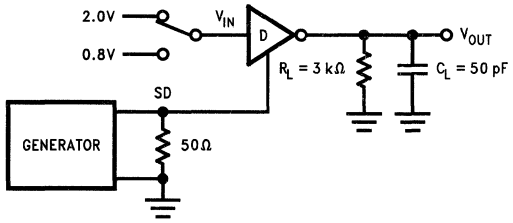

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FIGURE 5. Driver SHUTDOWN (SD) Delay Test Circuit

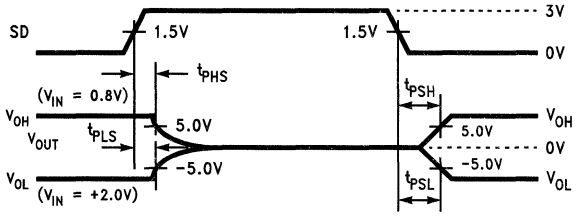

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FIGURE 6. Driver SHUTDOWN (SD) Delay Timing

Parameter Measurement Information (Continued)

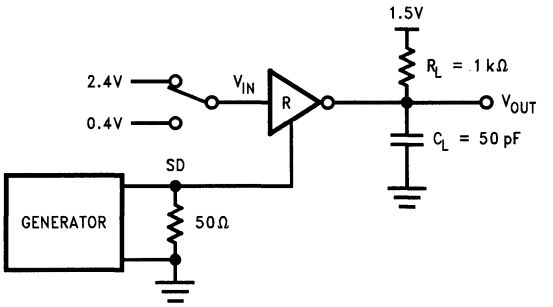

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FIGURE 7. Receiver SHUTDOWN (SD) Delay Test Circuit

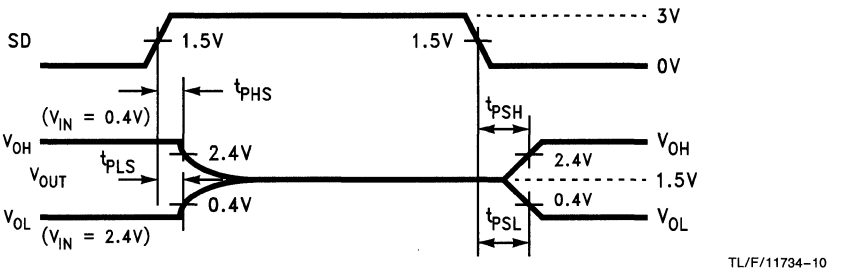

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FIGURE 8. Receiver SHUTDOWN (SD) Delay Timing

Pin Descriptions

V_{CC} (Pin 3). Power supply pin for the device, +3.3V (±0.3V).

V^+ (Pin 1). Positive supply for TIA/EIA-232-E drivers. Recommended external capacitor—0.47 μF (16V). This supply is not intended to be loaded externally.

V^- (Pin 25). Negative supply for TIA/EIA-232-E drivers. Recommended external capacitor—0.47 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (Pins 6, 24). External capacitor connection pins. Recommended capacitor—0.47 μF (6.3V).

C2+, C2− (Pins 2, 4). External capacitor connection pins. Recommended capacitor—0.47 μF (16V).

C3+, C3− (Pins 28, 26). External capacitor connection pins. Recommended capacitor—0.47 μF (6.3V).

SHUTDOWN (SD) (Pin 23). A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA, providing a low power state. In this mode receiver R5 remains active. The SD pin should be driven or tied low (GND) to disable the shutdown mode.

D_{IN} 1–3 (Pins 7, 8, 9). Driver input pins are JEDEC 3.3V standard compatible.

D_{OUT} 1–3 (Pins 22, 21, 20). Driver output pins conform to TIA/EIA-232 -E levels.

R_{IN} 1–5 (Pins 19, 18, 17, 16, 15). Receiver input pins accept TIA/EIA-232-E input voltages (±25V). Receivers guarantees hysteresis of TBD mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (Pins 10, 11, 12, 13, 14). Receiver output pins are JEDEC 3.3V standard compatible.

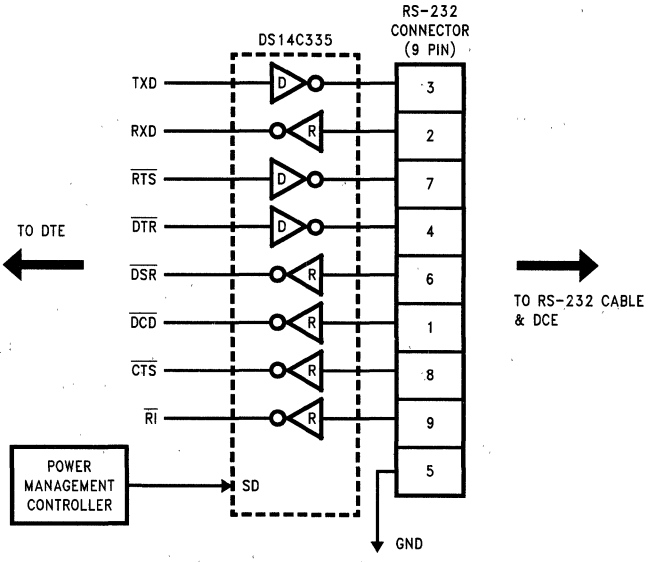
GND (Pin 27). Ground Pin.

Application Information

9-Pin SERIAL PORT APPLICATION

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD and the control lines are RTS, DTR, DSR, DCD, CTS and RI. The DS14C335 is a 3 x 5 Driver/Receiver and offers a single chip solution for the DTE interface as shown in *Figure 9*.

Ring Indicator (RI) is used to inform the DTE that an incoming call is coming from a remote DCE. When the DS14C335 is in SHUTDOWN (SD) mode, receiver five (R5) remains active and monitors RI circuit. This active receiver (R5) alerts the DTE to switch the DS14C335 from SHUTDOWN to active mode.



TL/F/11734-11

FIGURE 9. Typical DTE Application

Application Information (Continued)

MOUSE DRIVING

The DS14C335 was tested for drive current under the following mouse driving conditions:

- Two driver outputs set at V_{OH} and their outputs were tied together (paralleled), sourcing current to supply the V+ terminal of the mouse electronics
- One driver output set at V_{OL} to sink the current from the V− terminal of the mouse electronics
- One receiver was used to accept data from the mouse
- Power Supply Voltage (V_{CC}): 3.0V to 3.6V

Completion of the testing (performed by National's Data Transmission Applications Group and a major PC manufacturer) concluded that the DS14C335 and it's DC-DC Convertor supplied adequate drive capability to power a typical PC mouse. The mouse tested was specified with the following conditions:

10 mA at +6V
5.0 mA at −6V

Since driver current is limited, it is recommended that newer lower power mice be specified for battery powered applications. Using older high power mice is wasteful of precious battery charge.

EXTERNAL DC-DC CONVERTOR COMPONENTS

The DS14C335 with it's unique DC-DC Convertor triples the power supply voltage (3.0V) to +9.3V and then inverts it to a −9V potential. This unique convertor **ONLY** requires 5 external surface mount 0.47 μF capacitors. The five identical components were chosen to simplify PCB layout and the procurement of components. The DS14C335's DC-DC Convertor also provides a larger signal swing (higher at RS-232 standard data rates) which translates to more noise margin for the rejection of ground potential differences, induced noise, and crosstalk compared to other DC-DC convertor schemes which only provide limited signal swing and limited noise margin.

DC-DC CONVERTOR CAPACITORS

The use of polarized capacitors is not required. However, if they are used, the polarity indicated in the DS14C335 Functional Diagram must be honored for proper operation. Surface mount capacitors or ceramic capacitors may be used, however, for optimal efficiency, capacitors with a low effective series resistance (ESR) should be used. Values in the low Ohms(Ω) is normally acceptable.

INTEROPERATION WITH +5V UARTs

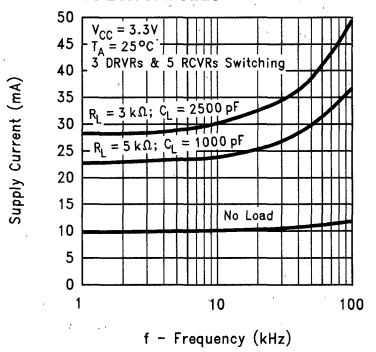
The DS14C335 provides full RS-232 driver output levels and a single chip solution for the popular 9-pin defacto serial port. This device may be used in either pure +3V applications or mixed power supplied +3V/+5V applications. The Driver Input (DIN) and ShutDown (SD) input pins can directly accept full +5V levels without the need for any external components. The Receiver Output (ROUT) is specified at 2.4V minimum while sourcing 1 mA. This level is compatible with standard TTL thresholds. For a complete discussion on "Interoperation of the DS14C335 with +5V UARTs" please see National Application Note AN-876.

POWER DISSIPATION IN REAL RS-232 APPLICATIONS

The DS14C335 DC-DC Convertor uses special circuitry that helps limit the increase in power supply current as frequency increases. A complete description of power dissipation and calculations for RS-232 applications can be found in National Application Note AN-914 titled "Understanding Power Requirements in RS-232 Applications". Typical performance curves are also located in this datasheet for quick reference.

Typical Performance Characteristics

Supply Current vs Frequency vs Driver Loads



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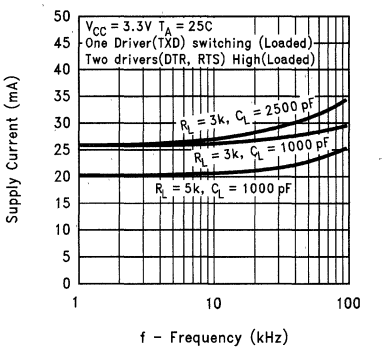
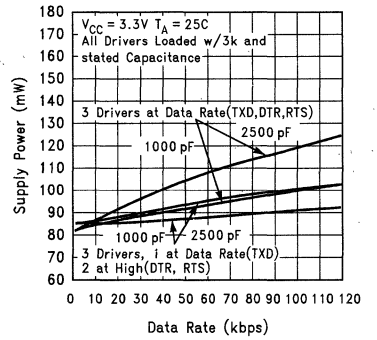
Supply Current vs Frequency vs Driver Loads



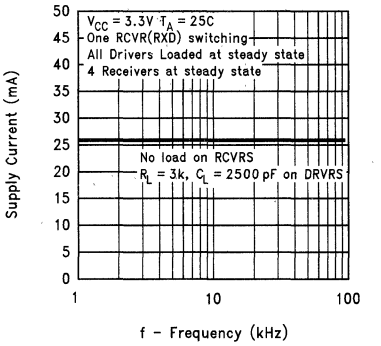
TL/F/11734–13

Supply Power vs Data Rate



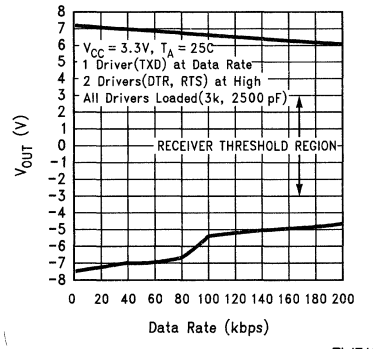
TL/F/11734–14

Supply Current vs Frequency (Receiver)



TL/F/11734–15

Driver Output vs Data Rate



TL/F/11734–16

National Semiconductor

DS14C535
+5V Supply EIA/TIA-232 3 x 5 Driver/Receiver

General Description

The DS14C535 is three driver, five receiver device which conforms to EIA/TIA-232-E and CCITT (ITU-T) V.28 standard specifications. This device employs an internal DC-DC converter to generate the necessary output levels from a +5V power supply. A SHUTDOWN (SD) mode reduces the supply current to 10 μA maximum. In the SD mode, one receiver is active, allowing ring indicator (RI) to be monitored. PC Board space consumption is minimized by the availability of Shrink Small Outline Packaging (SSOP).

The DS14C535 provides a one-chip solution for the common 9-pin serial RS-232 interface between data terminal and data circuit-terminating equipment.

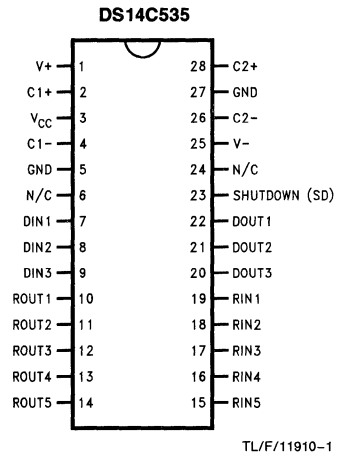
This device allows an easy migration path to the 3.3V DS14C335. The packages are the same. The N/C pins on the DS14C535 are not physically connected to the chip. Board layout for the DS14C335 will accommodate both devices.

This device's low power requirement and small footprint makes it an ideal choice for Laptop and Notebook applications.

Features

- Pin compatible with DS14C335
- Conforms to EIA/TIA-232-E and CCITT (ITU-T) V.28 specifications
- Failsafe receiver outputs high when inputs open
- Operates with single +5V power supply
- Low power requirement—I_{CC} 12 mA maximum
- SHUTDOWN mode—I_{CX} 10 μA maximum
- One Receiver (R5) active during SHUTDOWN
- Operates up to 128 kbps—Lap-Link® Compatible
- 4V/μs minimum Slew Rate guaranteed
- ESD rating of 3 kV on all pins (H, B, M)
- Available in 28-lead SSOP EIAJ Type II package
- Only four 0.1 μF capacitors required for the DC-DC converter

Connection Diagram



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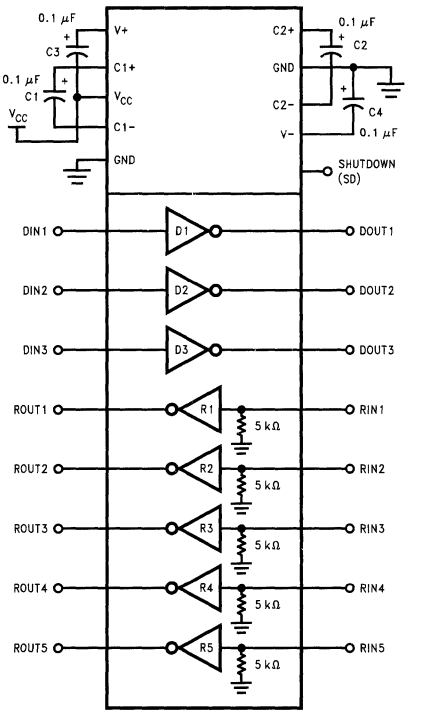
Order Number DS14C535MSA or DS14C535TMSA
See NS Package Number MSA28

Functional Diagram



TL/F/11910–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Input Voltage (D_{IN}, SD)	−0.3V to +5.5V
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±25V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	Continuous
Maximum Package Power Dissipation @ +25°C	
SSOP MSA Package	1286 mW
Derate MSA Package 10.3 mW/°C above +25°C	
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 3.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Free Air Temperature (T_A)			
DS14C535	0	+70	°C

DC-DC Converter Capacitors (C1−C4)

Recommended range of values is 0.1 μF to 0.68 μF, ±20%. For more detail refer to application information section of this data sheet.

Electrical Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DEVICE CHARACTERISTICS								
V^+	Positive Power Supply	No Load C1−C4 = 0.1 μF	D_{IN} = 0.8V			+8.5		V
V^-	Negative Power Supply		D_{IN} = 2.0V			−7.0		V
I_{CC}	Supply Current	No Load					12	mA
I_{CX}	SHUTDOWN Supply Current	R_L = 3 kΩ, SD = V_{CC}				1.0	10	μA
V_{IH}	High Level Enable Voltage			SD	2.0			V
V_{IL}	Low Level Enable Voltage				GND		0.8	V
I_{IH}	High Level Enable Current	2.0V ≤ V_{IN} ≤ 5.5V					+2.0	μA
I_{IL}	Low Level Enable Current	GND ≤ V_{IN} ≤ 0.8V			−2.0			μA
DRIVER CHARACTERISTICS								
V_{IH}	High Level Input Voltage		D_{IN}		2.0			V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	2.0V ≤ V_{IN} ≤ 5.5V					+1.0	μA
I_{IL}	Low Level Input Current	GND ≤ V_{IN} ≤ 0.8V			−1.0			μA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ			+5.0	8		V
V_{OL}	Low Level Output Voltage					−6.7	−5.0	V
I_{OS+}	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.8V (Note 7)			−40	−20	−8	mA
I_{OS-}	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V (Note 7)			6	15	40	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V			300	1200		Ω

Electrical Characteristics (Continued)

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Note 4)						
V_{TH}	Input High Threshold Voltage	R1–R5, SD = 0.8V (Active Mode)		1.4	2.4	V
		R5, 2.0V ≤ SD ≤ 5.5V (Shutdown Mode)		2.0	2.8	V
V_{TL}	Input Low Threshold Voltage	R1–R5, SD = 0.8V (Active Mode)	0.8	1.1		V
		R5, 2.0V ≤ SD ≤ 5.5V (Shutdown Mode)	0.8	1.1		V
V_{HY}	Hysteresis (Note 4)		0.15		1.0	V
R_{IN}	Input Resistance	V_{IN} = ±3V to ±15V	3.0	5.4	7.0	kΩ
I_{IN}	Input Current	V_{IN} = +15V	2.14		5.0	mA
		V_{IN} = +3V	0.43		1.0	mA
		V_{IN} = −3V	−1.0		−0.43	mA
		V_{IN} = −15V	−5.0		−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_{OH} = −2.0 mA	3.8			V
		V_{IN} = −3V, I_{OH} = −20 μA	4.0			V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_{OL} = +2.0 mA		0.23	0.4	V

Switching Characteristics

Over recommended operating conditions, SD = 0.8V, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	R_L = 3 kΩ C_L = 50 pF (*Figures 1* and *2*)	0.1	0.6	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0	0.2	μs
SR1	Output Slew Rate	R_L = 3 kΩ to 7 kΩ, C_L = 50 pF *(Figure 2)*	4	13	30	V/μs
SR2	Output Slew Rate	R_L = 3 kΩ, C_L = 2500 pF *(Figure 2)*	4	10	30	V/μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 5* and *6*) R_L = 3 kΩ C_L = 50 pF		0.48		ms
t_{PSL}	Propagation Delay SD to LOW			1.88		ms
t_{PHS}	Propagation Delay HIGH to SD			0.62		ms
t_{PSH}	Propagation Delay SD to HIGH			1.03		ms
RECEIVER CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF (*Figures 3* and *4*)	0.1	0.4	1.0	μs
t_{PHL}	Propagation Delay HIGH to LOW		0.1	0.6	1.0	μs
t_{SK}	Skew $\lvert t_{PLH}-t_{PHL}\rvert$			0.1	0.5	μs
t_{PLS}	Propagation Delay LOW to SD	(*Figures 7* and *8*) R_L = 1 kΩ C_L = 50 pF R1–R4 Only		0.13		μs
t_{PSL}	Propagation Delay SD to LOW			1.0		μs
t_{PHS}	Propagation Delay HIGH to SD			0.19		μs
t_{PSH}	Propagation Delay SD to HIGH			0.58		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified. For voltage logic levels, the more positive value is designated as maximum. For example, if −5V is a maximum, the typical value (−6.7V) is more negative.

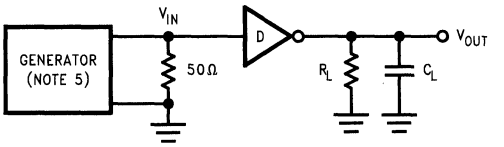
Note 4: Receiver characteristics are guaranteed for SD = 0.8V. When SD = 2.0V, receiver five (R5) is active and meets receiver parameters in SHUTDOWN (SD) mode, unless otherwise specified.

Note 5: Generator characteristics for driver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, V_{IH} = 3V, V_{IL} = 0V, duty cycle = 50%.

Note 6: Generator characteristics for receiver input: f = 64 kHz (128 kbits/sec), $t_r = t_f < 10$ ns, V_{IH} = 3V, V_{IL} = −3V, duty cycle = 50%.

Note 7: Only one driver output shorted at a time.

Parameter Measurement Information



TL/F/11910–3

FIGURE 1. Driver Propagation Delay and Slew Rate Test Circuit

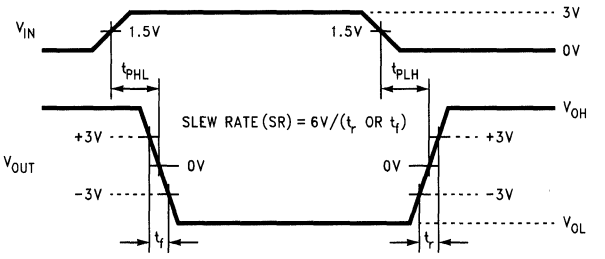


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FIGURE 2. Driver Propagation Delay and Slew Rate Timing

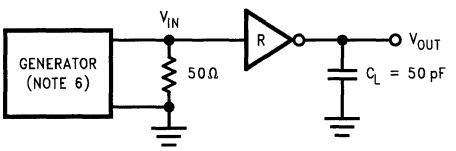

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FIGURE 3. Receiver Propagation Delay Test Circuit

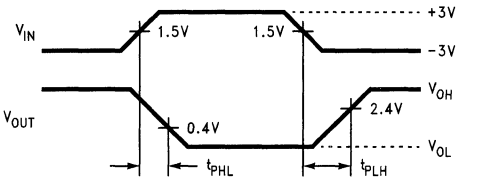

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FIGURE 4. Receiver Propagation Delay Timing

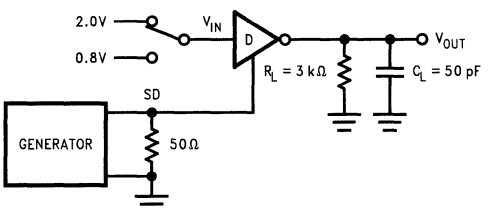

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FIGURE 5. Driver SHUTDOWN (SD) Delay Test Circuit

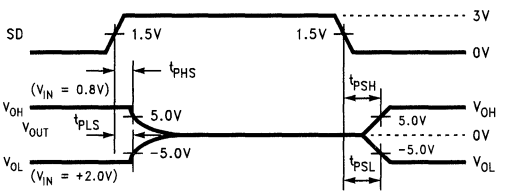

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FIGURE 6. Driver SHUTDOWN (SD) Delay Timing

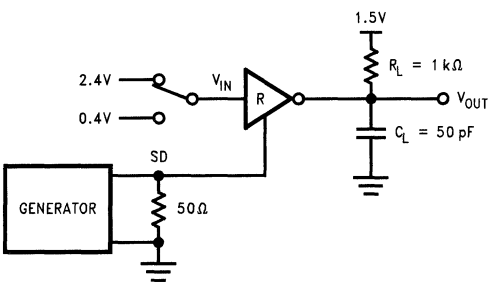

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FIGURE 7. Receiver SHUTDOWN (SD) Delay Test Circuit

Parameter Measurement Information (Continued)

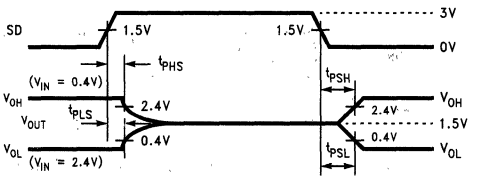

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FIGURE 8. Receiver SHUTDOWN (SD) Delay Timing

Pin Descriptions

V_{CC} (Pin 3). Power supply pin for the device, +5V (±0.5V).

V^+ (Pin 1). Positive supply for EIA/TIA-232-E drivers. Recommended external capacitor—0.1 μF (16V). This supply is not intended to be loaded externally.

V^- (Pin 25). Negative supply for EIA/TIA-232-E drivers. Recommended external capacitor—0.1 μF (16V). This supply is not intended to be loaded externally.

C1+, C1− (Pins 2, 4). External capacitor connection pins.

C2+, C2− (Pins 28, 26). External capacitor connection pins.

SHUTDOWN (SD) (Pin 23). A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 10 μA, providing a low power state. In this mode receiver R5 remains active. The SD pin should be driven or tied low (GND) to disable the shutdown mode.

D_{IN} 1–3 (Pins 7, 8, 9). Driver input pins.

D_{OUT} 1–3 (Pins 22, 21, 20). Driver output pins conform to EIA/TIA-232 -E levels.

R_{IN} 1–5 (Pins 19, 18, 17, 16, 15). Receiver input pins accept EIA/TIA-232-E input voltages (±25V). Receivers guarantees hysteresis of TBD mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT} 1–5 (Pins 10, 11, 12, 13, 14). Receiver output pins.

GND (Pins 5, 27). Ground Pins. Both pins must be connected to external ground. These pins are not connected together on the chip.

Application Information

In a typical Data Terminal Equipment (DTE) to Data Circuit-Terminating Equipment (DCE) 9-pin de-facto interface implementation, 2 data lines and 6 control lines are required. The data lines are TXD and RXD and the control lines are RTS, DTR, DSR, DCD, CTS and RI. The DS14C535 is a 3 x 5 Driver/Receiver and offers a single chip solution for the DTE interface as shown in *Figure 9.*

Ring Indicator (RI) is used to inform the DTE that an incoming call is coming from a remote DCE. When the DS14C535 is in SHUTDOWN (SD) mode, receiver five (R5) remains active and monitors RI circuit. This active receiver (R5) alerts the DTE to switch the DS14C535 from SHUTDOWN to active mode.

To achieve minimum power consumption, the DS14C535 can be in SHUTDOWN mode and only activated when communications are needed.

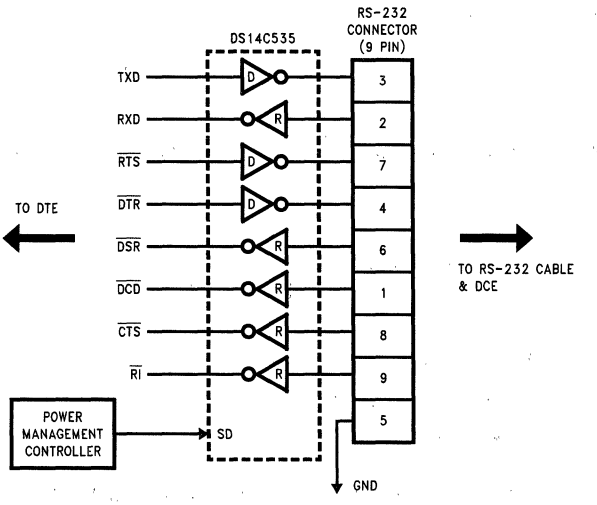

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FIGURE 9. Typical DTE Application

Application Information (Continued)

Capacitors:

Capacitors can be ceramic or tantalum. Standard surface mount in the range of 0.1 μF to 0.68 μF are readily available from several manufacturers. A minimum 20V rating is recommended. Contact manufacturers for specific detail on surface mounting and dielectrics. A partial list of manufacturers include:

Manufacturer	Phone Number
KEMET	803-963-6300
AVX	803-448-9411
MURATA-ERIE	800-831-9172

National Semiconductor

DS14C561
+3.3V-Powered 4 x 5 Driver/Receiver

General Description

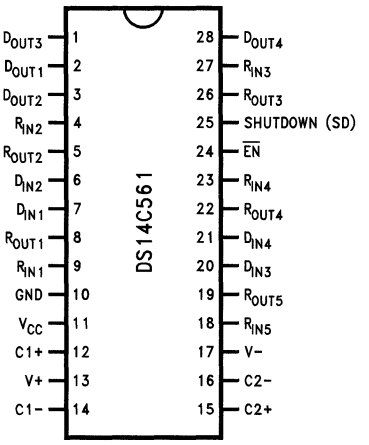
The DS14C561 is a +3.3V-powered device that conforms to the new TIA/EIA-562 standard. This standard provides a faster, lower-power alternative to TIA/EIA-232-E (RS-232) Interfaces, while guaranteeing interoperation with TIA/EIA-232-E Interfaces. The DS14C561 is guaranteed to operate with a minimum supply voltage of +3V, while maintaining the TIA/EIA-562 output signal levels ±3.7V.

The DS14C561 features an internal DC-DC converter, with four external 1.0 μF capacitors to double and invert +3.3V to ±6.6V. The device also offers a shutdown mode that reduces supply current to 100 μA, making the part ideal for use in battery-powered or power-conscious applications.

Features

- Conforms to TIA/EIA-562
- Full AC Specifications
- Internal DC-DC converter
- Operates with a single +3.3V supply
- Low power requirement I_{CC} 6 mA max
- Shutdown mode I_{CX} 100 μA max
- Operates over 64 kbits/sec
- Receiver noise filtering
- TRI-STATE® receiver outputs
- Pin compatible with MAX561

Connection Diagram



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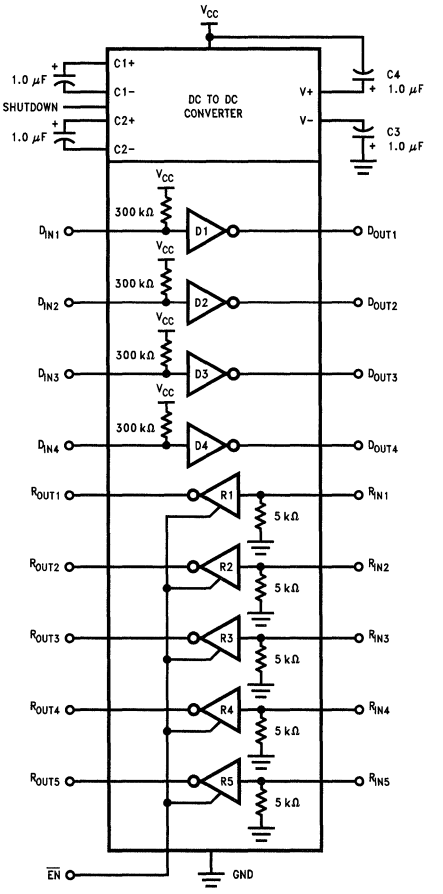
Order Number DS14C561WM
See NS Package Number M28B

Functional Diagram



TL/F/11363–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
V^+ Pin	(V_{CC} − 0.3V) to +14V
V^- Pin	+0.3V to −14V
Driver Input Voltage	−0.3V to (V_{CC} + 0.3V)
Driver Output Voltage	(V^+ + 0.3V) to (V^- − 0.3V)
Receiver Input Voltage	±30V
Receiver Output Voltage	−0.3V to (V_{CC} + 0.3V)
Junction Temperature	+150°C
Maximum Package Power Dissipation @ +25°C (Note 6) Wide SOIC (WM) Package	1520 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Short Circuit Duration (D_{OUT})	continuous

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Operating Free Air Temp. (T_A) DS14C561	0	+70	°C

Electrical Characteristics

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 µF, T_A = 0°C to +70°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V^+	Positive Power Supply	R_L = 3 kΩ, C1–C4 = 1.0 µF	D_{IN} = 0.4V		6.0		V
V^-	Negative Power Supply		D_{IN} = 2.4V		−5.0		V
I_{CC}	Supply Current (V_{CC})	No Load			3.5	6.0	mA
I_{CX}	Supply Current Shutdown	R_L = 3 kΩ, SD = V_{CC}			20	100	µA
V_{IH}	High Level Enable Voltage		SD	2.0		V_{CC}	V
V_{IL}	Low Level Enable Voltage			GND		0.4	V
I_{IH}	High Level Enable Current			−10		+10	µA
I_{IL}	Low Level Enable Current			−10		+10	µA
DRIVER CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.4	V
I_{IH}	High Level Input Current	$V_{IN} \geq 2.0V$		−10		+10	µA
I_{IL}	Low Level Input Current	$V_{IN} \leq 0.4V$		−10		+10	µA
		V_{IN} = 0V		−10		+10	µA
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		3.7	5.0	13.2	V
V_{OL}	Low Level Output Voltage	3 Drivers Loaded		−13.2	−4.0	−3.7	V
V_{OH}	High Level Output Voltage	R_L = 3 kΩ		3.7	4.8	13.2	V
V_{OL}	Low Level Output Voltage	4 Drivers Loaded, V_{CC} = +3.3V		−13.2	−4.2	−3.7	V
I_{OS}^+	Output High Short Circuit Current	V_O = 0V, V_{IN} = 0.4V		−20	−10	−2	mA
I_{OS}^-	Output Low Short Circuit Current	V_O = 0V, V_{IN} = 2.0V		2.0	8.0	20	mA
R_O	Output Resistance	−2V ≤ V_O ≤ +2V, V_{CC} = GND = 0V		300			Ω
RECEIVER CHARACTERISTICS							
V_{TH}	Input High Threshold Voltage				1.3	2.0	V
V_{TL}	Input Low Threshold Voltage			0.4	1.0		V
V_{HY}	Hysteresis			0.05	0.3		V
R_{IN}	Input Resistance			3.0	4.5	7.0	kΩ

Electrical Characteristics (Continued)

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 μF, T_A = 0°C to +70°C, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS (Continued)							
I_{IN}	Input Current	V_{IN} = +15V		2.14		5.0	mA
		V_{IN} = +3V		0.43		1.0	mA
		V_{IN} = −3V		−1.0		−0.43	mA
		V_{IN} = −15V		−5.0		−2.14	mA
V_{OH}	High Level Output Voltage	V_{IN} = −3V, I_O = −200 μA		2.6	3.0		V
V_{OL}	Low Level Output Voltage	V_{IN} = +3V, I_O = +1.6 mA			0.2	0.4	V
V_{IH}	High Level Input Voltage		$\overline{EN}$	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.4	V
I_{IH}	High Level Input Current	$V_{IN} \geq$ 2.0V		−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} \leq$ 0.4V		−10		+10	μA
I_{OZ}	Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}		−10		+10	μA

Switching Characteristics

V_{CC} = +3.3V ±0.3V, C1–C4 = 1 μF, T_A = 0°C to +70°C, unless otherwise specified (Note 4)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH		R_L = 3 kΩ, C_L = 50 pF (*Figures 1* and *2*)		1.0	4.0	μs
t_{PHL}	Propagation Delay HIGH to LOW				0.8	4.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				0.2	1.0	μs
SR1	Output Slew Rate		R_L = 3 kΩ to 7 kΩ, C_L = 50 pF			30	V/μs
SR2	Output Slew Rate		R_L = 3 kΩ, C_L = 2500 pF, f = 10 kHz			30	V/μs
t_r, t_f	Output Rise, Fall Time (Note 7)	V_{CC} = 3.3V	R_L = 3 kΩ, C_L = 2500 pF, f = 10 kHz	0.2	2.7	3.1	μs
			R_L = 3 kΩ, C_L = 1000 pF, f = 32 kHz	0.2	1.7	2.1	μs
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH		Input Pulse Width > 10 μs, C_L = 150 pF (*Figures 3* and *4*)		3.7	9.0	μs
t_{PHL}	Propagation Delay HIGH to LOW				4.7	9.0	μs
t_{SK}	Skew $\lvert t_{PLH} - t_{PHL} \rvert$				1.0	3.0	μs
t_{PLZ}			(*Figures 5* and *7*)		0.2		μs
t_{PZL}					1.2		μs
t_{PHZ}			(*Figures 5* and *6*)		0.4		μs
t_{PZH}					1.2		μs
t_{NW}	Noise Pulse Width Rejected		(*Figures 3* and *4*)		4.0	1.0	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{OS}^+ and I_{OS}^- values are for one output at a time. If more than one output is shorted simultaneously, the device power dissipation may be exceeded.

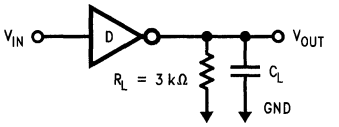
Note 4: Receiver AC input waveform for test purposes: t_r = t_f = 200 ns, V_{IH} = 3V, V_{IL} = −3V, f = 32 kHz (64 kbits/sec). Driver AC input waveform for test purposes: t_r = t_f = ≤ 10 ns, V_{IH} = 3V, V_{IL} = 0V, f = 32 kHz (64 kbits/sec).

Note 5: All typicals are given for V_{CC} = 3.3V and T_A = +25°C.

Note 6: Ratings apply to ambient temperature at +25°C. Above this temperature derate: WM package 14.3 mW/°C..

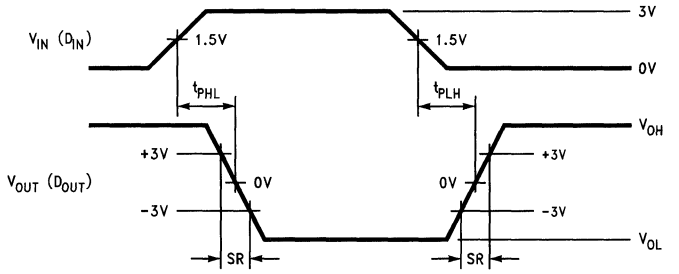
Note 7: Rise and Fall Times (t_r, t_f) are measured between the ±3.3V levels on the driver output. One output switching.

Parameter Measurement Information



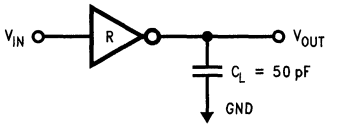
TL/F/11363–3

FIGURE 1. Driver Load Circuit



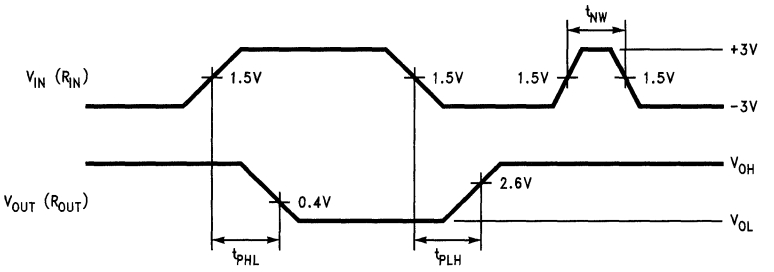
TL/F/11363–4

FIGURE 2. Driver Switching Waveform



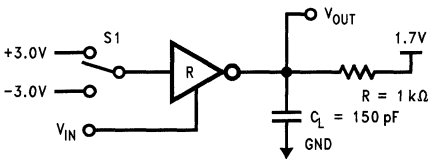
TL/F/11363–5

FIGURE 3. Receiver Load Circuit



TL/F/11363–6

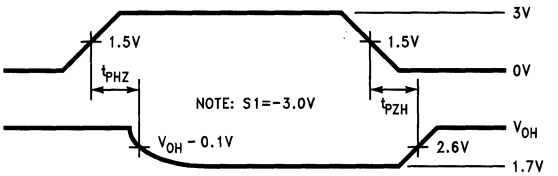
FIGURE 4. Receiver Propagation Delays and Noise Rejection



TL/F/11363–7

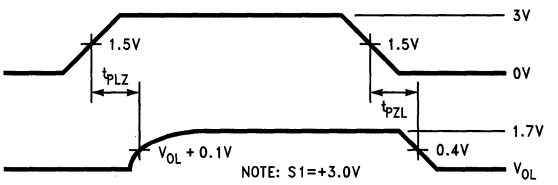
FIGURE 5. Receiver Disable Load Circuit

Parameter Measurement Information (Continued)



TL/F/11363–8

FIGURE 6. Receiver TRI-STATE® Delay Timing (t_{PHZ}, t_{PZH})



TL/F/11363–9

FIGURE 7. Receiver TRI-STATE® Delay Timing (t_{PLZ}, t_{PZL})

Pin Descriptions

V_{CC} (pin 11)—Power supply pin for the device, +3.3V ±0.3V.

V^+ (pin 13)—Positive supply for drivers. Recommended external capacitor: C4 = 1 μF. This supply is not intended to be loaded externally.

V^- (pin 17)—Negative supply for drivers. Recommended external capacitor: C3 = 1 μF. This supply is not intended to be loaded externally.

$C1^+$, $C1^-$ (pins 12 and 14)—External capacitor connection pins. Recommended capacitor: 1μF.

$C2^+$, $C2^-$ (pins 15 and 16)—External capacitor connection pins. Recommended capacitor: 1 μF.

$\overline{EN}$ (pin 24)—Controls the Receiver output TRI-STATE® Circuit. A HIGH level on this pin will disable the Receiver Output.

SHUTDOWN (SD) (pin 25)—A High on the SHUTDOWN pin will lower the total I_{CC} current to less than 100 μA. Providing a low power state.

D_{IN} 1–4 (pins 7, 6, 20 and 21)—Inputs of unused drivers may be left open, an internal pull-up resistor pulls input to V_{CC}. Output will be LOW for open inputs. (300 kΩ minimum, typically 3.3 MΩ)

D_{OUT} 1–4 (pins 2, 3, 1 and 28)—Driver output pins conform to TIA/EIA-562 levels.

R_{IN} 1–5 (pins 9, 4, 27, 23 and 18)—Receiver input pins accept TIA/EIA-562 input voltages (±15V). Receivers feature a noise filter and guaranteed hysteresis of 50 mV. Unused receiver input pins may be left open. Internal input resistor (5 kΩ) pulls input LOW, providing a failsafe HIGH output.

R_{OUT}1–5 (pins 8, 5, 26, 22 and 19)—Receiver output pins generate a maximum V_{OL} of 0.4V given an I_O of 1.6 mA and a minimum V_{OH} of 2.6V given an I_O of −200 μA.

GND (pin 10)—Ground pin.

National Semiconductor

DS14C88/DS14C88T
QUAD CMOS Line Driver

General Description

The DS14C88 and DS14C88T, pin-for-pin compatible to the DS1488/MC1488, are line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate standard TTL/CMOS logic levels to levels conforming to EIA-232-D and CCITT V.28 standards.

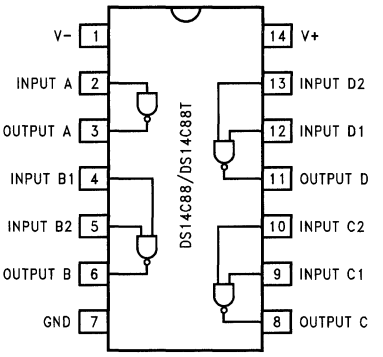
The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to its bipolar equivalents: 500 μA (DS14C88) versus 25 mA (DS1488).

The DS14C88/DS14C88T simplifies designs by eliminating the need for external slew rate control capacitors. Slew rate control in accordance with EIA-232D is provided on-chip, eliminating the output capacitors.

Features

- Meets EIA-232D and CCITT V.28 standards
- Industrial temperature range
  −40°C to +85°C—DS14C88T
- LOW power consumption
- Wide power supply range
  ±5V to ±12V
- Available in SOIC package

Connection Diagram



TL/F/11105–1

Order Number DS14C88N, DS14C88M, DS14C88TJ, DS14C88TN or DS14C88TM
See NS Package Number J14A, N14A or M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
- V^+ Pin: +13V
- V^- Pin: −13V

Driver Input Voltage: (V^+) +0.3V to GND −0.3V

Driver Output Voltage: $|(V^+) - V_O| \leq 30V$, $|(V^-) - V_O| \leq 30V$

Continuous Power Dissipation @ +25°C (Note 2)
- N Package: 1513 mW
- J Package: 1935 mW
- M Package: 1063 mW

Junction Temperature: +150°C

Lead Temperature (Soldering 4 seconds): +260°C

Storage Temperature Range: −65°C to +150°C

This Product does not meet 2000V ESD rating. (Note 9)

Recommended Operating Conditions

	Min	Max	Units
V^+ Supply (GND = 0V)	+4.5	+12.6	V
V^- Supply (GND = 0V)	−4.5	−12.6	V
Operating Free Air Temp. (T_A)			
DS14C88	0	+75	°C
DS14C88T	−40	+85	°C

Electrical Characteristics Over Recommended Operating Conditions, unless otherwise specified

Symbol	Parameter	Conditions			Min	Typ	Max	Units
I_{IL}	Maximum Low Input Current	V_{IN} = GND					+10	μA
I_{IH}	Maximum High Input Current	$V_{IN} = V^+$			−10			μA
V_{IL}	Low Level Input Voltage	$V^+ \geq +7V, V^- \leq -7V$			GND		0.8	V
		$V^+ < +7V, V^- > -7V$			GND		0.6	V
V_{IH}	High Level Input Voltage				2.0		V^+	V
V_{OL}	Low Level Output Level	$V_{IN} = V_{IH}$, R_L = 3 kΩ or 7 kΩ	$V^+ = 4.5V, V^- = -4.5V$			−4.0	−3.0	V
			$V^+ = 9V, V^- = 9V$			−8.0	−6.5	V
			$V^+ = 12V, V^- = -12V$			−10.5	−9.0	V
V_{OH}	High Level Output Level	$V_{IN} = V_{IL}$, R_L = 3 kΩ or 7 kΩ	$V^+ = 4.5V, V^- = -4.5V$		3.0	4.0		V
			$V^+ = 9V, V^- = -9V$		6.5	8.0		V
			$V^+ = 12V, V^- = -12V$		9.0	10.5		V
I_{OS+}	High Level Output Short Circuit Current (Note 3)	V_{IN} = 0.8V, V_O = GND		$V^+ = +12V$, $V^- = -12V$	−45			mA
I_{OS-}	Low Level Output Short Circuit Current (Note 3)	V_{IN} = 2.0V, V_O = GND					+45	mA
R_{OUT}	Output Resistance	$V^+ = V^- = GND = 0V$, $-2V \leq V_O \leq +2V$ (Note 4) *(Figure 1)*			300			Ω
I_{CC+}	Positive Supply Current	$V_{IN} = V_{ILmax}$, R_L = OPEN	$V^+ = 4.5V, V^- = -4.5V$				10	μA
			$V^+ = 9V, V^- = -9V$				30	μA
			$V^+ = 12V, V^- = -12V$				60	μA
		$V_{IN} = V_{IHmin}$, R_L = OPEN	$V^+ = 4.5V, V^- = -4.5V$				50	μA
			$V^+ = 9V$, $V^- = -9V$	DS14C88			300	μA
				DS14C88T			400	μA
			$V^+ = 12V$, $V^- = -12V$	DS14C88			500	μA
				DS14C88T			700	μA
I_{CC-}	Negative Supply Current	$V_{IN} = V_{ILmax}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$	DS14C88			−10	μA
				DS14C88T			−15	μA
			$V^+ = 9V$, $V^- = -9V$	DS14C88			−10	μA
				DS14C88T			−15	μA
			$V^+ = 12V$, $V^- = -12V$	DS14C88			−10	μA
				DS14C88T			−15	μA
		$V_{IN} = V_{IHmin}$, R_L = OPEN	$V^+ = 4.5V$, $V^- = -4.5V$	DS14C88			−30	μA
				DS14C88T			−45	μA
			$V^+ = 9V$, $V^- = -9V$	DS14C88			−30	μA
				DS14C88T			−45	μA
			$V^+ = 12V$, $V^- = -12V$	DS14C88			−60	μA
				DS14C88T			−80	μA

Switching Characteristics

Over Recommended Operating Conditions, unless otheriwse specified (*Figures 2* and *3*) (Notes 5 and 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	$V^+ = +4.5V, V^- = -4.5V$		1.5	6.0	μs
		$V^+ = +9.0V, V^- = -9.0V$		1.2	5.0	μs
		$V^+ = +12V, V^- = -12V$		1.2	4.0	μs
t_{PHL}	Propagation Delay High to Low	$V^+ = +4.5V, V^- = -4.5V$		1.5	6.0	μs
		$V^+ = +9.0V, V^- = -9.0V$		1.35	5.0	μs
		$V^+ = +12V, V^- = -12V$		1.3	4.0	μs
t_r	Rise Time (Note 7)		0.2	1.0		μs
t_f	Fall Time (Note 7)		0.2	1.0		μs
tsk	Typical Propagation Delay Skew	$V^+ = +4.5V, V^- = -4.5V$		250		ns
		$V^+ = +9.0V, V^- = -9.0V$		200		ns
		$V^+ = +12V, V^- = -12V$		150		ns
S_R	Output Slew Rate (Note 7)	$R_L = 3\ k\Omega$ to $7\ k\Omega$ $C_L = 15\ pF$ to $2500\ pF$			30	V/μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Derate N Package 12.1 mW/°C, J Package 12.9 mW/°C, and M Package 8.5 mW/°C above +25°C.

Note 3: I_{OS+} and I_{OS-} values are for one output at a time. If more than one output is shorted simultaneously, the device dissipation may be exceeded.

Note 4: Power supply (V^+, V^-) and GND pins are connected to ground for the Output Resistance Test (R_O).

Note 5: AC input test waveforms for test purposes: $t_r = t_f \leq 20$ ns, $V_{IH} = 2V$, $V_{IL} = 0.8V$ (0.6V at $V^+ = 4.5V$, $V^- = -4.5V$)

Note 6: Input rise and rall times must not exceed 5 μs.

Note 7: The output slew rate, rise time, and fall time are measured from the +3.0V to the −3.0V level on the output waveform.

Note 8: C_L include jig and probe capacitances.

Note 9: ESD Rating (HBM, 1.5 kΩ, 100 pF) ≥ 1.0 kV.

Parameter Measure Information

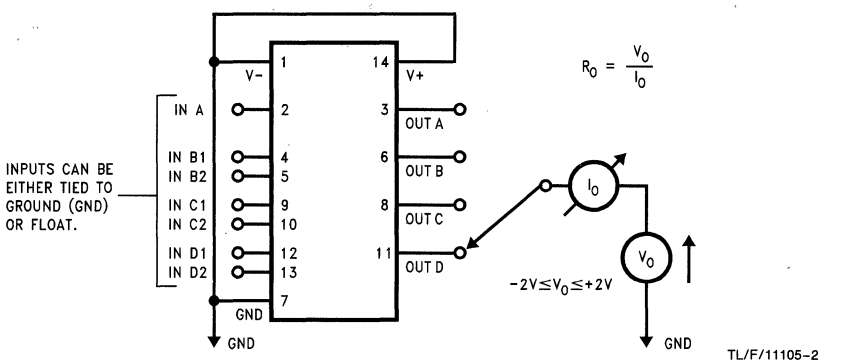


FIGURE 1. Output Resistance Test Circuit (Power-Off)

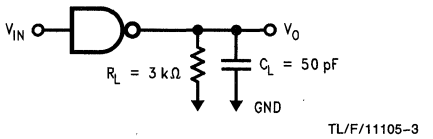


FIGURE 2. Driver Load Circuit (Note 8)

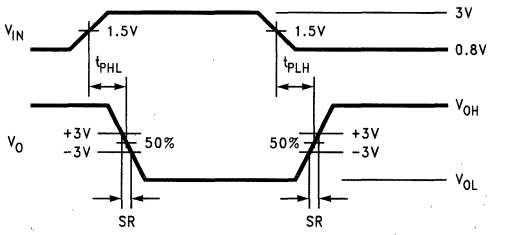


FIGURE 3. Driver Switching Waveform

Typical Application Information

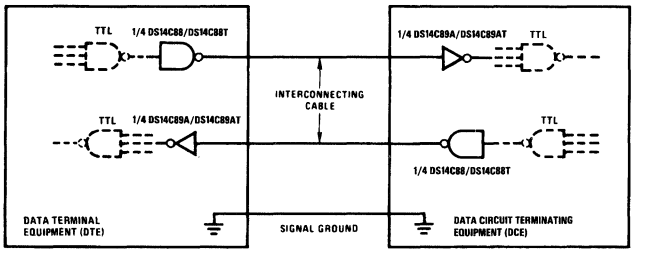


FIGURE 4. EIA-232D Data Transmission

National Semiconductor

DS1488 Quad Line Driver

General Description

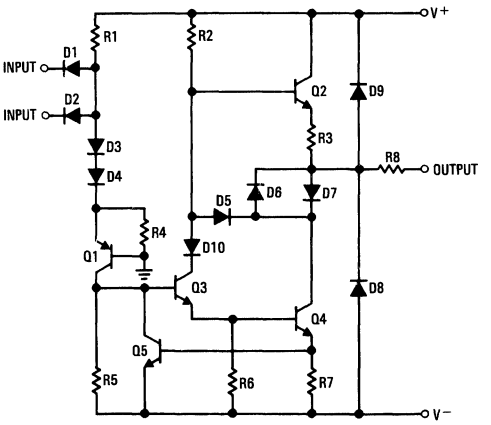
The DS1488 is a quad line driver which converts standard TTL input logic levels through one stage of inversion to output levels which meet EIA Standard RS-232D and CCITT Recommendation V.24.

Features

- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are TTL/LS compatible

Schematic and Connection Diagrams

1/4 Circuit



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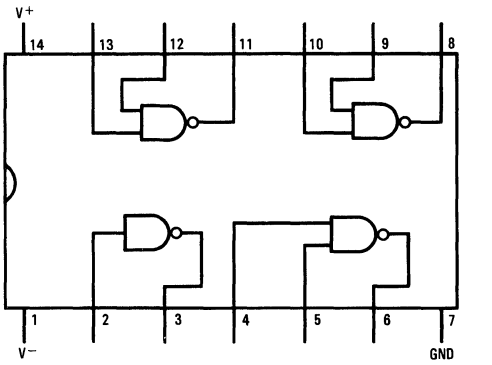
Dual-In-Line Package



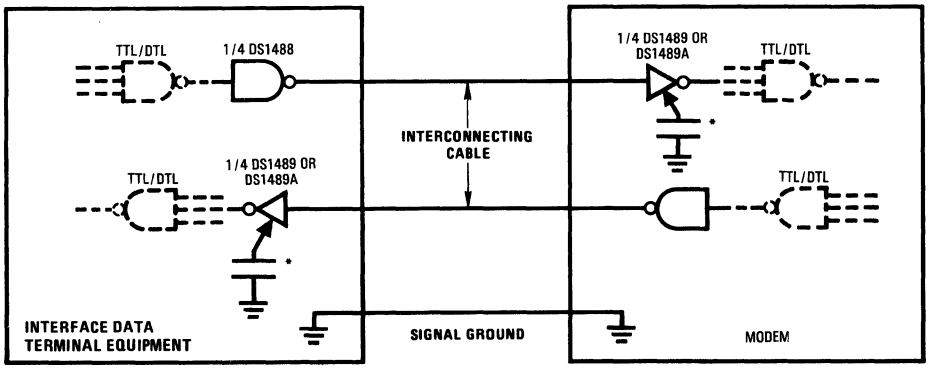
TL/F/5776–2

Top View

Order Number DS1488J, DS1488M or DS1488N
See NS Package Number J14A, M14A or N14A

Typical Applications

RS-232C Data Transmission



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*Optional for noise filtering

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \le V_{IN} \le 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded DIP Package	1280 mW
SO Package	974 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded DIP package 10.2 mW/°C above 25°C; derate SO package 7.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) $V_{CC}+ = 9V$, $V_{CC}- = -9V$ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	μA
V_{OH}	High Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$	6.0	7.0		V
			$V^+ = 13.2V, V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0\ k\Omega$, $V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$	−6.0	−6.8		V
			$V^+ = 13.2V, V^- = -13.2V$	−9.0	−10.5		V
I_{OS}^+	High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{OS}^-	Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
I_{CC}^+	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V, V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V, V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V, V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V, V^- = -15V$		8.0	12.0	mA
I_{CC}^-	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V, V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V, V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V, V^- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V, V^- = -9.0V$		−0.001	−0.015	mA
			$V^+ = 12V, V^- = -12V$		−0.001	−0.015	mA
			$V^+ = 15V, V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V, V^- = -9.0V$			252	333	mW
		$V^+ = 12V, V^- = -12V$			444	576	mW

Switching Characteristics ($V_{CC} = 9V$, $V_{EE} = -9V$, $T_A = 25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}(\Delta T/\Delta V)$$

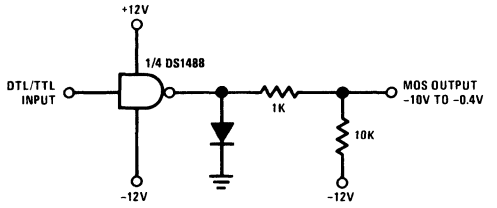
where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS-232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

See Typical Performance Characteristics.

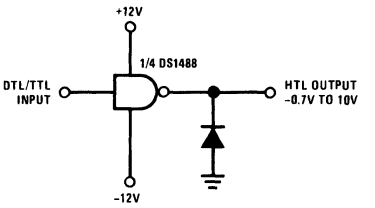
Typical Applications (Continued)

DTL/TTL-to-MOS Translator



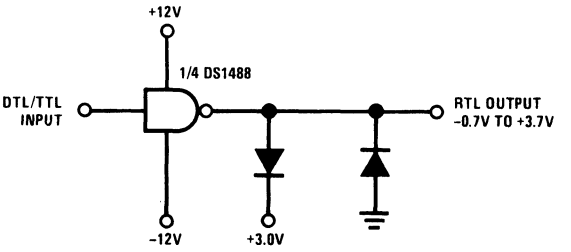
TL/F/5776–4

DTL/TTL-to-HTL Translator



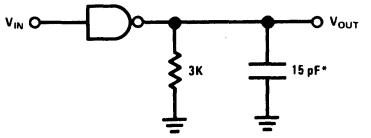
TL/F/5776–5

DTL/TTL-to-RTL Translator



TL/F/5776–6

AC Load Circuit and Switching Time Waveforms



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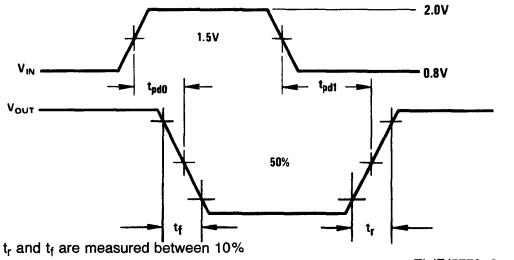
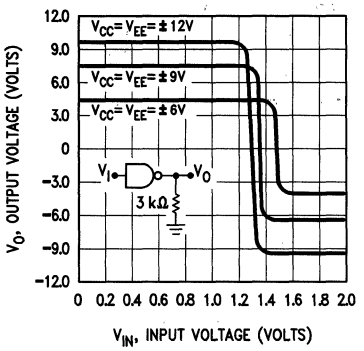
*C_L includes probe and jig capacitance.



t_r and t_f are measured between 10% and 90% of the output waveform.

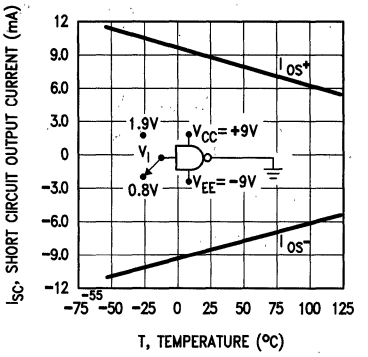
TL/F/5776–8

Typical Performance Characteristics T_A = +25°C unless otherwise noted



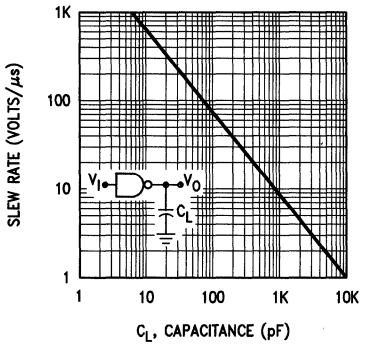
TL/F/5776–9

FIGURE 1. Transfer Characteristics vs Power Supply Voltage



TL/F/5776–10

FIGURE 2. Short-Circuit Output Current vs Temperature



TL/F/5776–11

FIGURE 3. Output Slew Rate vs Load Capacitance

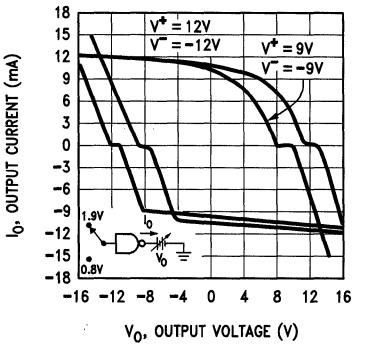


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FIGURE 4. Output Voltage and Current-Limiting Characteristics

National Semiconductor

DS14C89A/DS14C89AT
Quad CMOS Receiver

General Description

The DS14C89A/DS14C89AT, pin-for-pin compatible to the DS1489A/MC1489A, are receivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate levels conforming to EIA-232E and CCITT V.28 standards to TTL/CMOS logic levels.

The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to their bipolar equivalents: 900 μA (DS14C89A) versus 26 mA (DS1489A).

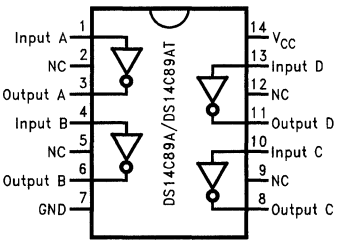
The DS14C89A/DS14C89AT provide on chip noise filtering which eliminates the need for external response control filter capacitors. When replacing the DS1489A with the DS14C89A/DS14C89AT, the response control filter pins can be tied high, low, or not connected.

Features

- Meets EIA/TIA-232-E and CCITT V.28 Standards
- Industrial Temperature Range
  −40°C to +85°C–DS14C89AT
- LOW Power consumption
- On chip noise filter
- Available in SOIC Package

2

Connection Diagram



TL/F/11106–1

Order Number DS14C89AN, DS14C89AM, DS14C89ATJ, DS14C89ATN, DS14C89ATM
See NS Package Number J14A, M14A, N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	+6V
Input Voltage	−30V to +30V
Receiver Output Voltage	(V_{CC}) +0.3V to GND−0.3V
Junction Temperature	+150°C
Continuous Power Dissipation @ +25°C (Note 2)	
N Package	1513 mW
J Package	1935 mW
M Package	1063 mW
Lead Temp. (Soldering 4 seconds)	+260°C
Storage Temp. Range	−65°C to +150°C
ESD Rating ≥ 1.8 kV, Typically ≥ 2 kV (HMB, 1.5 kΩ, 100 pF)	

Recommended Operating Conditions

	Min	Max	Units
V_{CC} (GND = 0V)	+4.5	+5.5	V
Operating Free Air Temp. (T_A)			
DS14C89A	0	+75	°C
DS14C89AT	−40	+85	°C

Electrical Characteristics Over recommended operating conditions, unless otherwise specified

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold				1.3		2.7	V
V_{TL}	Input Low Threshold				0.5		1.9	V
V_{HY}	Typical Input Hysteresis					1.0		V
I_{IN}	Input Current	V_{IN} = +25V	V_{CC} = +4.5V to +5.5V		3.6		8.3	mA
		V_{IN} = −25V			−3.6		−8.3	mA
		V_{IN} = +3V			0.43		1.0	mA
		V_{IN} = −3V			−0.43		−1.0	mA
		V_{IN} = +15V	V_{CC} = 0V (Power-Off) (Note 4)		2.14		5.0	mA
		V_{IN} = −15V			−2.14		−5.0	mA
		V_{IN} = +3V			0.43		1.0	mA
		V_{IN} = −3V			−0.43		−1.0	mA
V_{OH}	Output High Voltage	V_{IN} = V_{TL} (min)	I_{OUT} = −3.2 mA		2.8	4.0		V
			I_{OUT} = −20μA		3.5	4.7		V
V_{OL}	Output Low Voltage	V_{IN} = V_{TH} (max) I_{OUT} = +3.2 mA				0.15	0.4	V
I_{CC}	Supply Current	No Load V_{IN} = 2.7V or 0.5V		DS14C89A		0.5	900	μA
				DS14C89AT		0.5	2.0	mA

AC Electrical Characteristics

Over recommended operating conditions, unless otherwise specified, C_l = 50 pF (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Low to High	Input Pulse Width ≥ 10 μs		3.5	6.5	μs
t_{PHL}	Propagation Delay High to Low	Input Pulse Width ≥ 10 μs		3.2	6.5	μs
t_{SK}	Typical Propagation Delay Skew			400		ns
t_r	Output Rise TIme			40	300	ns
t_f	Output Fall Time			40	300	ns
t_{nw}	Pulse Width assumed to be Noise				1.0	μs

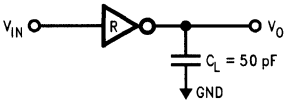
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Derate N Package 12.1 mW/°C, J Package 12.9 mW/°C, and M Package 8.5 mW/°C above +25°C.

Note 3: AC input waveforms for test purposes: t_r = t_f = 200 ns, V_{IH} = +3V, V_L = −3V, f = 20 KHz.

Note 4: Under the power-off supply conditions it is assumed that the power supply potential drops to zero (0V) and is replaced by a low impedance or short circuit to ground.

Parameter Measurement Information



TL/F/11106–2

FIGURE 1. Receiver Load Circuit

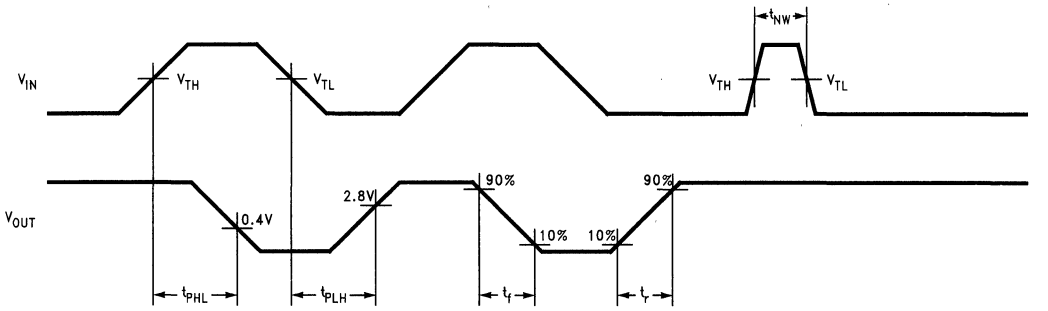


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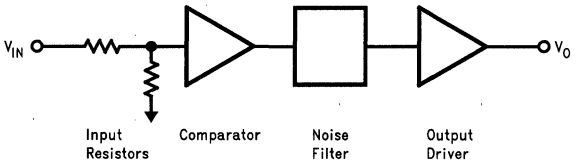
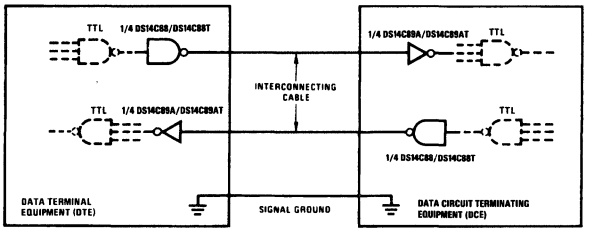
FIGURE 2. Receiver Switching Waveform (Note 3)

Typical Application Information



TL/F/11106–4

FIGURE 3. Receiver Block Diagram



TL/F/11106–5

FIGURE 4. EIA-232D Data Transmission

National Semiconductor

DS1489/DS1489A Quad Line Receiver

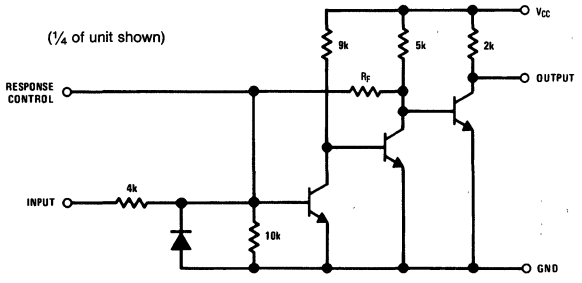
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA Standard RS-232D. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements.

Features

- Four separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode: high output for open inputs
- Inputs withstand ±30V

Schematic and Connection Diagrams



DS1489: R_F = 10k
DS1489A: R_F = 2k

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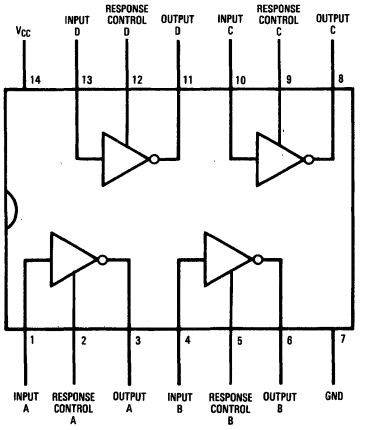
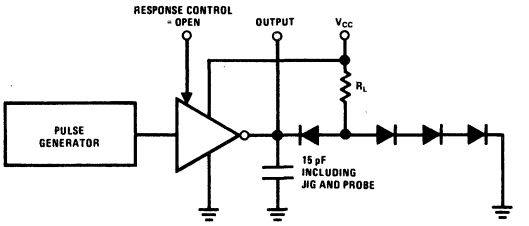
Dual-In-Line Package



TL/F/5777–2

Top View
Order Number DS1489J, DS1489M, DS1489AM, DS1489N or DS1489AN
See NS Package Number J14A, M14A or N14A

AC Test Circuit and Voltage Waveforms



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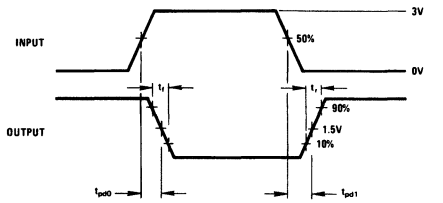

TL/F/5777–4

FIGURE 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

Maximum Power Dissipation* at 25°C

Cavity Package	1308 mW
Molded DIP Package	1207 mW
SO Package	1042 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 9.7 mW/°C above 25°C; derate SO package 8.33 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for V_{CC} = 5.0V ±1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Input High Threshold Voltage	V_{OUT} ≤ 0.45V, I_{OUT} = 10 mA	DS1489	T_A = 25°C	1.0	1.25	1.5	V
					0.9		1.6	V
			DS1489A	T_A = 25°C	1.75	2.00	2.25	V
					1.55		2.40	V
V_{TL}	Input Low Threshold Voltage	V_{OUT} ≥ 2.5V, I_{OUT} = −0.5 mA		T_A = 25°C	0.75	1.00	1.25	V
					0.65		1.35	V
I_{IN}	Input Current	V_{IN} = +25V			+3.6	+5.6	+8.3	mA
		V_{IN} = −25V			−3.6	−5.6	−8.3	mA
		V_{IN} = +3V			+0.43	+0.53		mA
		V_{IN} = −3V			−0.43	−0.53		mA
V_{OH}	Output High Voltage	I_{OUT} = −0.5 mA	V_{IN} = 0.75V		2.6	3.8	5.0	V
			Input = Open		2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	V_{IN} = 3.0V, I_{OUT} = 10 mA				0.33	0.45	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.75V				−3.0		mA
I_{CC}	Supply Current	V_{IN} = 5.0V				14	26	mA
P_d	Power Dissipation	V_{IN} = 5.0V				70	130	mW

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Input to Output "High" Propagation Delay	R_L = 3.9k, *(Figure 1)* (AC Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	R_L = 390Ω, *(Figure 1)* (AC Test Circuit)		20	50	ns
t_r	Output Rise Time	R_L = 3.9k, *(Figure 1)* (AC Test Circuit)		110	175	ns
t_f	Output Fall Time	R_L = 390Ω, *(Figure 1)* (AC Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These specifications apply for response control pin = open.

Typical Characteristics V_{CC} = 5.0V, T_A = +25°C unless otherwise noted

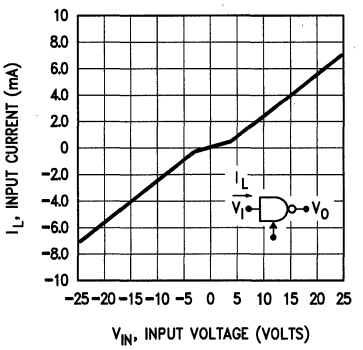

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FIGURE 2. Input Current

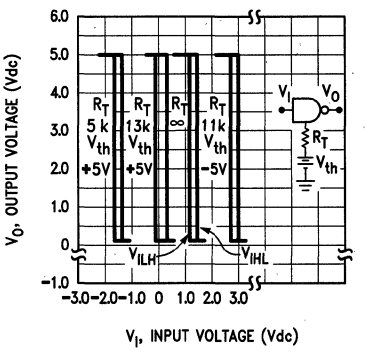

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FIGURE 3. DS1489 Input Threshold Voltage Adjustment

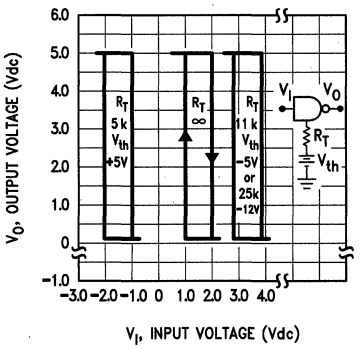

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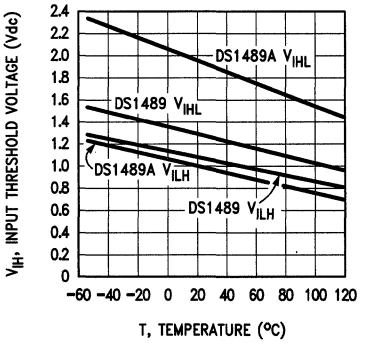
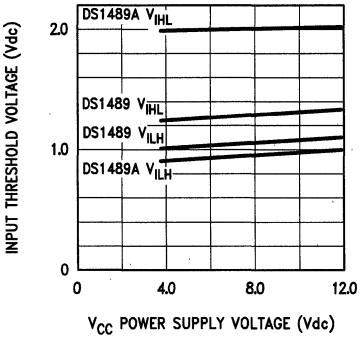
FIGURE 4. DS1489A Input Threshold Voltage Adjustment



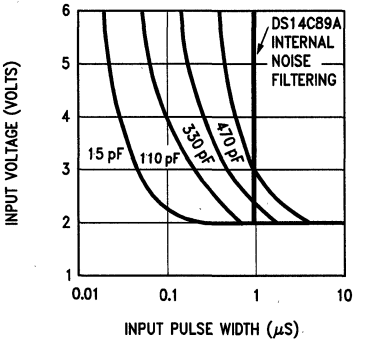
TL/F/5777–10

FIGURE 5. Input Threshold Voltage vs Temperature



TL/F/5777–11

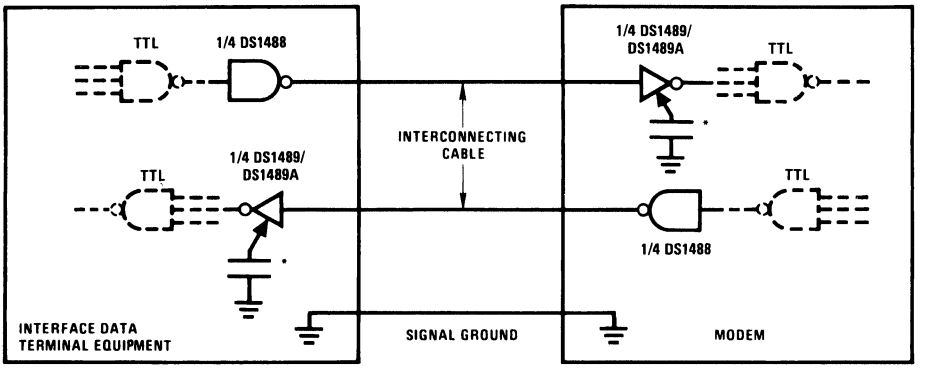
FIGURE 6. Input Threshold vs Power Supply Voltage



TL/F/5777–12

FIGURE 7. Noise Rejection vs Capacitance for DS1489A

Typical Application Information

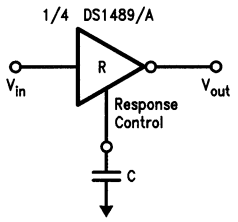


*Optional for noise filtering.

TL/F/5777–5

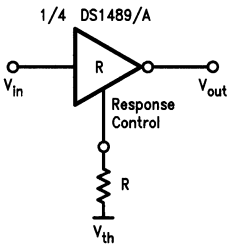
Applications Using the Response Control Pin

Noise Filter
(See *Figure 7*)



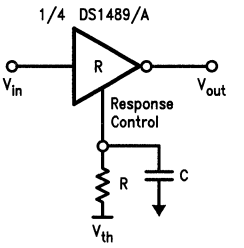
TL/F/5777–13

Threshold Shift
(See *Figures 3* and *4*)



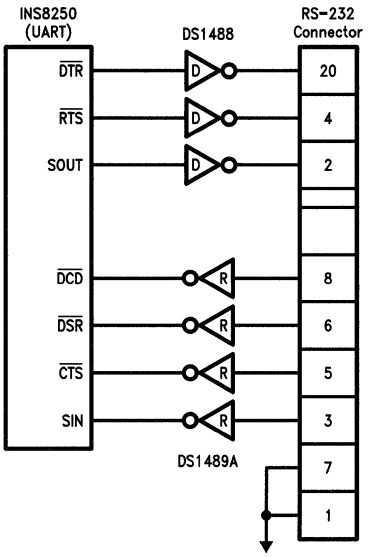
TL/F/5777–14

Noise Filter and Threshold Shift
(See *Figures 3, 4* and *7*)



TL/F/5777–15

Application of DS148, DS1489A and INS8250



TL/F/5777–16

National Semiconductor

DS75150 Dual Line Driver

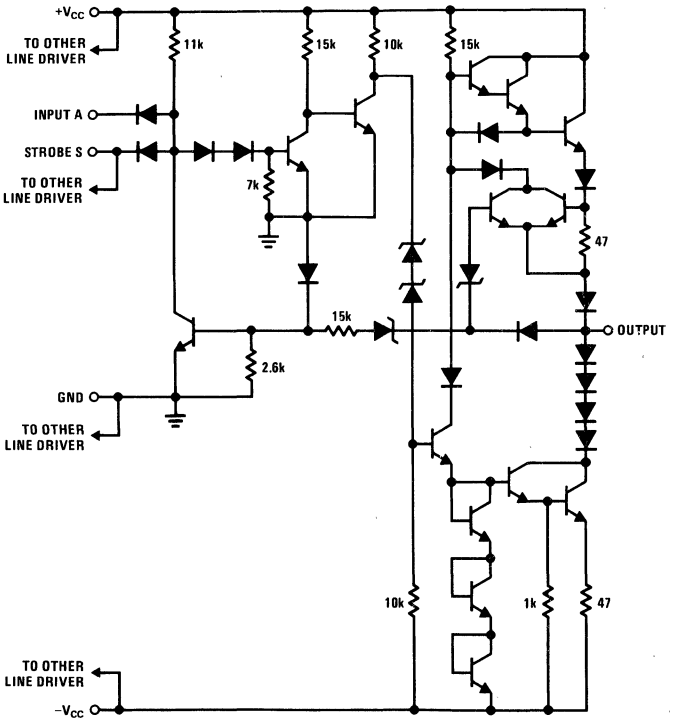
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from −12V and +12V power supplies.

Features

- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2 μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

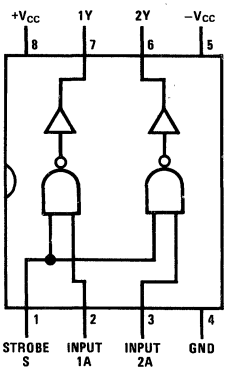
Schematic and Connection Diagrams



TL/F/5794–1

Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package



TL/F/5794–2

Top View

Positive Logic C = $\overline{AS}$

Order Number
DS75150M or DS75150N
See NS Package Number
M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	15V
Input Voltage	15V
Applied Output Voltage	+25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1022 mW
SO Package	655 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate molded DIP package 8.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −13.2V, V_{IL} = 0.8V, R_L = 3 kΩ to 7 kΩ *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −10.8V, V_{IH} = 2V, R_L = 3 kΩ to 7 kΩ *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Data Input		1	10	μA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Strobe Input		2	20	μA
I_{IL}	Low-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Data Input		−1	−1.6	mA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Strobe Input		−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, *(Figure 4)*, (Note 4)	V_O = 25V		2	5	mA
			V_O = −25V		−3	−6	mA
			V_O = 0V, V_I = 3V		15	30	mA
			V_O = 0V, V_I = 0V		−15	−30	mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are T_A = 25°C and $+V_{CC}$ = 12V, $-V_{CC}$ = −12V.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

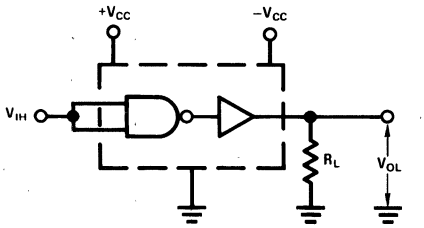
Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is more-negative voltage.

AC Electrical Characteristics ($+V_{CC} = 12V$, $-V_{CC} = -12V$, $T_A = 25°C$)

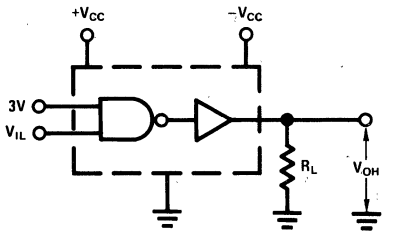
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 2500$ pF, $R_L = 3$ kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 2500$ pF, $R_L = 3$ kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L = 15$ pF, $R_L = 7$ kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L = 15$ pF, $R_L = 7$ kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	$C_L = 15$ pF, $R_L = 7$ kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	$C_L = 15$ pF, $R_L = 7$ kΩ, *(Figure 6)*		45		ns

DC Test Circuits



TL/F/5794–3

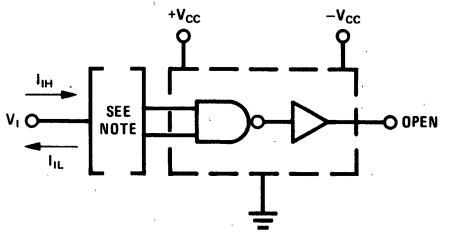
FIGURE 1. V_{IH}, V_{OL}



TL/F/5794–4

Each input is tested separately.

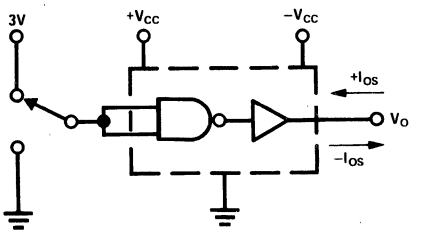
FIGURE 2. V_{IL}, V_{OH}



TL/F/5794–5

Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

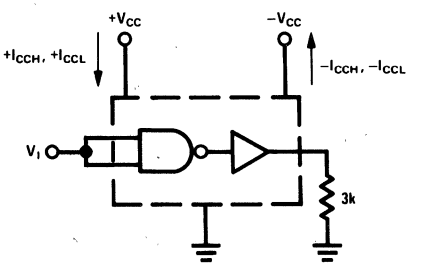
FIGURE 3. I_{IH}, I_{IL}



TL/F/5794–6

I_{OS} is tested for both input conditions at each of the specified output conditions.

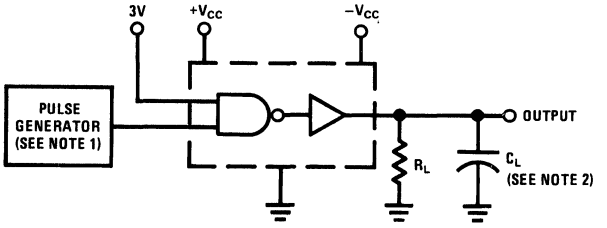
FIGURE 4. I_{OS}



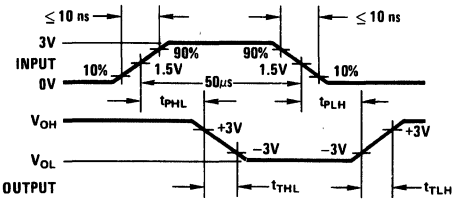
TL/F/5794–7

FIGURE 5. $I_{CCH}+$, $I_{CCH}-$, $I_{CCL}+$, $I_{CCL}-$

AC Test Circuit and Switching Waveforms



TL/F/5794–8



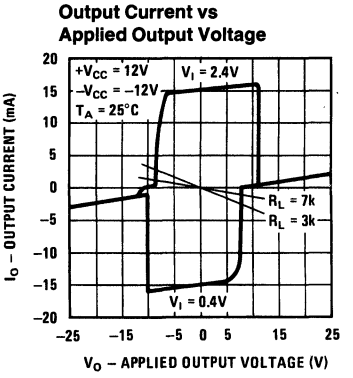
TL/F/5794–9

Note 1: The pulse generator has the following characterstics: duty cycle ≤ 50%, $Z_{OUT} \cong 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

Typical Performance Characteristics



TL/F/5794–10

FIGURE 7

National Semiconductor

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

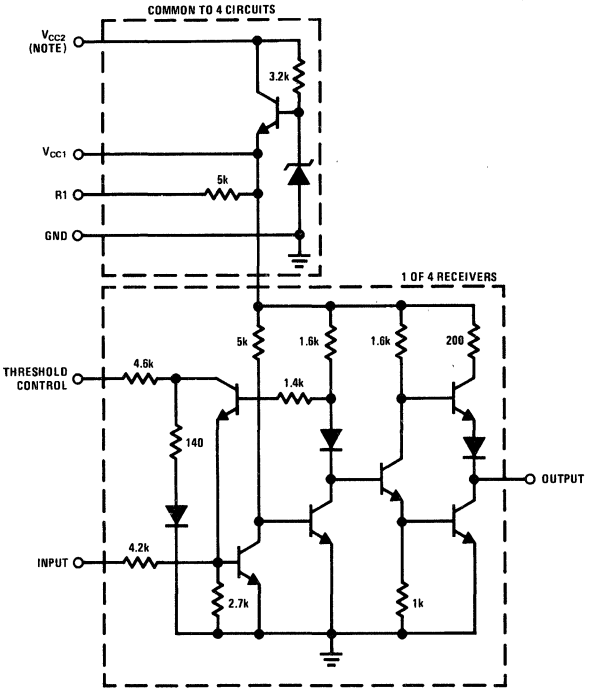
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic Diagram



TL/F/5795–1

Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16), (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	$I_{OH}=-400\ \mu A$, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	$I_{OL}=16$ mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	$\Delta V_I=-25V$ to $-14V$	3	5	7	kΩ
			$\Delta V_I=-14V$ to $-3V$	3	5	7	kΩ
			$\Delta V_I=-3V$ to $+3V$	3	6		kΩ
			$\Delta V_I=3V$ to 14V	3	5	7	kΩ
			$\Delta V_I=14V$ to 25V	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	$I_I=0$, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	$V_{CC1}=5.5V$, $V_I=-5V$, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	$V_{CC1}=5.5V$, $T_A=25°C$, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	$V_{CC2}=13.2V$, $T_A=25°C$, *(Figure 5)*			23	40	mA

Switching Characteristics ($V_{CC1}=5V$, $T_A=25°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	$C_L=50$ pF, $R_L=390\Omega$, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for $T_A=25°C$ and $V_{CC1}=5V$.

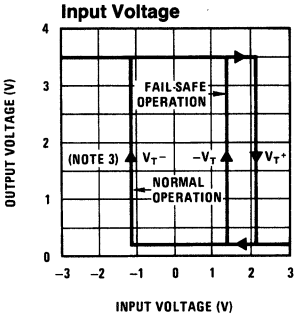
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

Typical Performance Characteristics

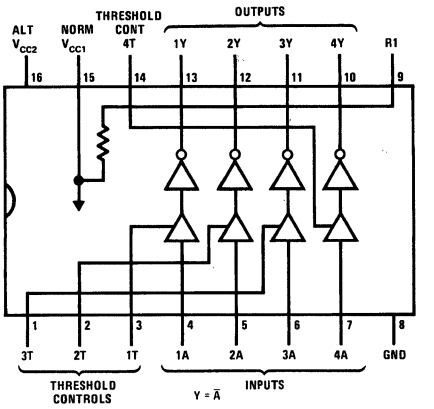
Output Voltage vs Input Voltage



TL/F/5795–10

Connection Diagram

Dual-In-Line Package

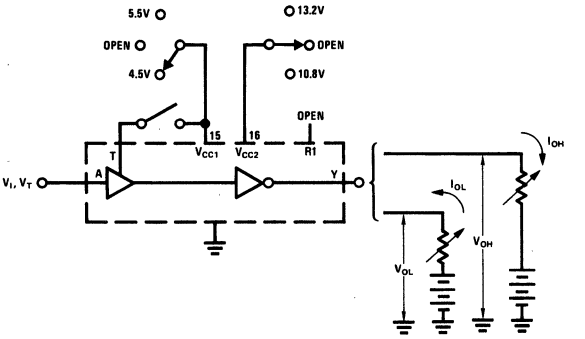


TL/F/5795–2

Top View

Order Number DS75154M or DS75154N
See NS Package Number M16A or N16A

DC Test Circuits and Truth Tables



TL/F/5795–3

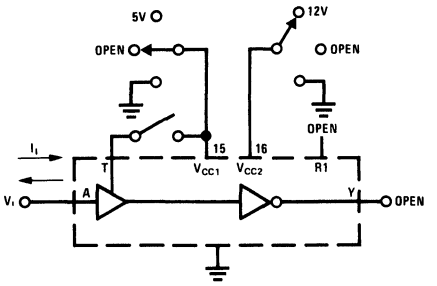
Test	Measure	A	T	Y	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open-Circuit Input (Fail-Safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (Fail-Safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	(Note 1) (Note 1)	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	−3V −3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (Fail-Safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max, (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	(Note 2) (Note 2)	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

Note 1: Momentarily apply −5V, then 0.8V.

Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}

DC Test Circuits and Truth Tables (Continued)

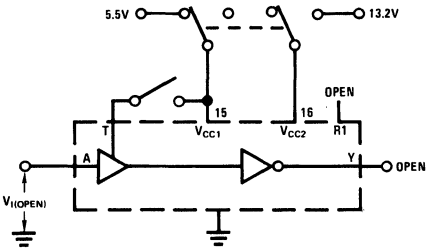


$r_I = \frac{\Delta V_I}{\Delta I_I}$

TL/F/5795–4

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

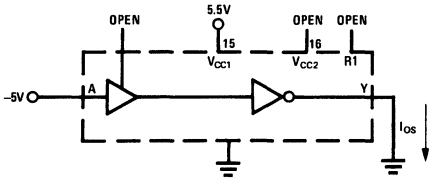
FIGURE 2. r_I



TL/F/5795–5

T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

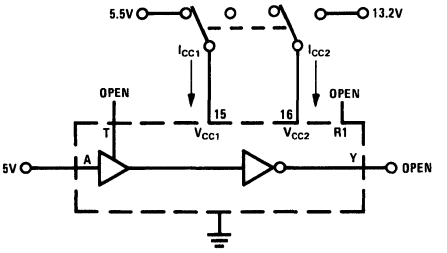
FIGURE 3. $V_{I(OPEN)}$



TL/F/5795–6

Each output is tested separately.

FIGURE 4. I_{OS}

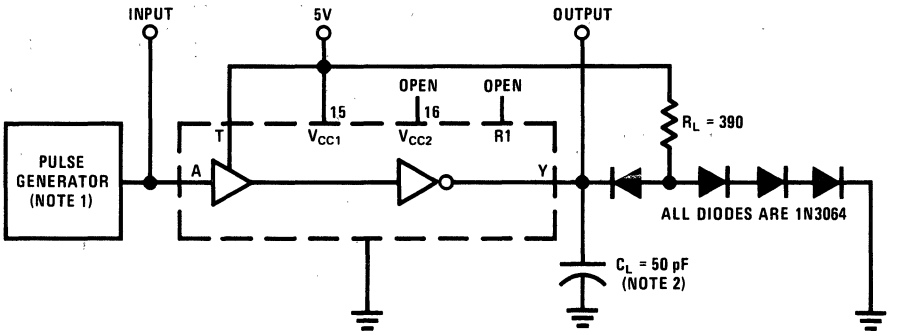


TL/F/5795–7

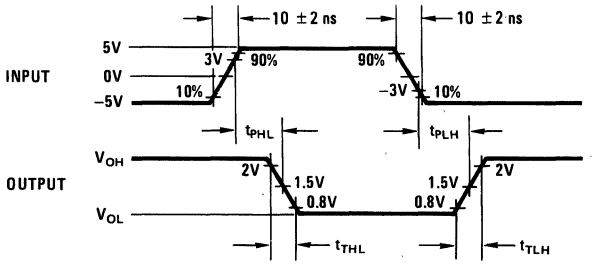
All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms



TL/F/5795–8



TL/F/5795–9

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, $t_W = 200$ ns, duty cycle ≤ 20%.

Note 2: C_L includes probe and jig capacitance.

FIGURE 6

National Semiconductor

DS9616H
Triple Line Driver

General Description

The DS9616H is a triple line driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C. Each driver converts TTL/DTL logic levels to EIA/CCIT and/or MIL-STD-188C logic levels for transmission between data terminal equipment and data communications equipment. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH on the inhibit terminal interrupts signal transfer and forces the output to a V_{OL} (EIA/CCITT MARK) state.

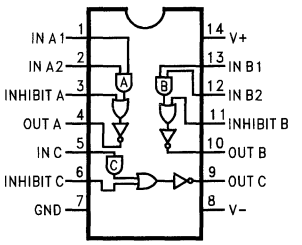
For the complementary function, see the DS9627MJ Dual EIA RS-232-C and MIL-STD-188C Line Receiver.

Features

- Internal slew rate limiting
- Meets EIA RS-232-C and CCITT V.24 and/or MIL-STD-188C
- Logic true inhibit function
- Output short circuit current-limiting
- Output voltage levels independent of supply voltages

Connection Diagrams

14-Lead DIP

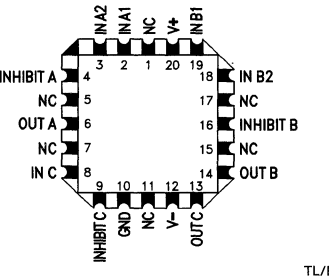


TL/F/10815–1

Top View

Order Number DS9616HMJ/883
See NS Package Number J14A

20-Terminal LCC



TL/F/10815–2

Top View

Order Number DS9616HME/883
See NS Package Number E20A

For Complete Military 883 Specifications, see RETS Data Sheet.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 4) DIP and CCP	400 mW
Supply Voltage	±15V
Input or Inhibit Voltage	−1.5V to +6.0V
Output Signal Voltage	±15V

Note 1: V_{IH} and V_{IL} are guaranteed by the V_{OH} and V_{OL} tests.

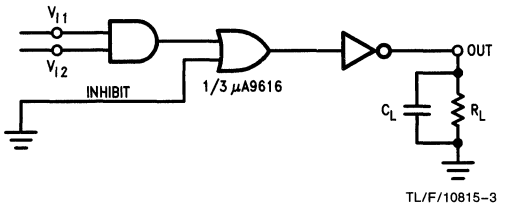
Note 2: All input and supply leads are grounded.

Note 3: An external capacitor may be needed to meet signal wave shaping requirements of MIL-STD-188C at the applicable modulation rate. No external capacitor is needed to meet RS-232-C.

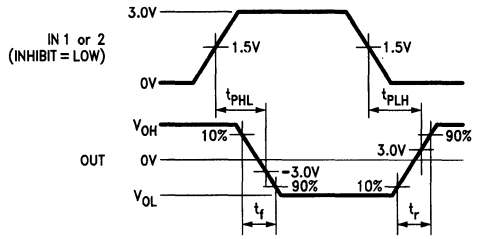
Note 4: Rating applies to ambient temperatures up to 125°C. Above 125°C ambient, derate linearly at 120°C/W.

DS9616HM
Electrical Characteristics $\pm 10.8V \le V_{CC} \le \pm 13.2V$, $R_L = 3.0\ k\Omega$, unless otherwise specified

Symbol	Characteristic	Condition	Min	Max	Unit
V_{OH}	Output Voltage HIGH	V_{I1} and/or $V_{I2} = V_{INHIBIT} = 0.8V$	5.0	7.0	V
V_{OL}	Output Voltage LOW	$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$	−7.0	−5.0	V
V_{OH} to V_{OL}	Output Voltage HIGH to Output Voltage LOW Magnitude Matching Error			±10	%
$I_{OS}+$	Positive Output Short Circuit Current	$R_L = 0\Omega$, V_{I1} and/or $V_{I2} = V_{INHIBIT} = 0.8V$	−45	−12	mA
$I_{OS}-$	Negative Output Short Circuit Current	$R_L = 0\Omega$, $V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$	12	60	mA
V_{IH}	Input Voltage HIGH (Note 1)		2.0		V
V_{IL}	Input Voltage LOW (Note 1)			0.8	V
I_{IH}	Input Current HIGH	$V_{I1} = V_{I2} = 2.4V$		40	μA
		$V_{I1} = V_{12} = 5.5V$		1.0	mA
I_{IL}	Input Current LOW	$V_{I1} = V_{12} = 0.4V$	−1.6		mA
I+	Positive Supply Current	$V_{I1} = V_{I2} = V_{INHIBIT} = 0.8V$		25	mA
		$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$		15	mA
I−	Negative Supply Current	$V_{I1} = V_{I2} = V_{INHIBIT} = 0.8V$	−1.0		mA
		$V_{I1} = V_{I2} = V_{INHIBIT} = 2.0V$	−25		mA
R_O	Output Resistance, Power Off (Note 2)	$-2.0V \le V_O \le 0.5V$	300		Ω
SR+	Positive Slew Rate (Note 3)	$C_L = 2500\ pF$, $R_L = 3.0\ k\Omega$ (See *Figure 1*)	4.0	30	V/μs
			4.0	30	V/μs
SR−	Negative Slew Rate (Note 3)	$C_L = 2500\ pF$, $R_L = 3.0\ k\Omega$ (See *Figure 1*)	−30	−4.0	V/μs
			−30	−4.0	V/μs



TL/F/10815–3

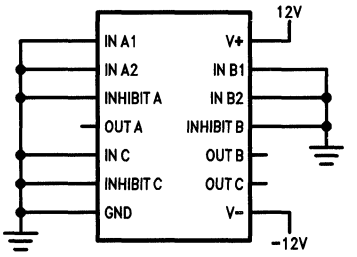


TL/F/10815–4

Omit V_{I2} for channel "C".
Input: FR = 50 kHz
Pulse Width = 10 μs
$t_r = t_f = 10 \pm 5.0$ ns

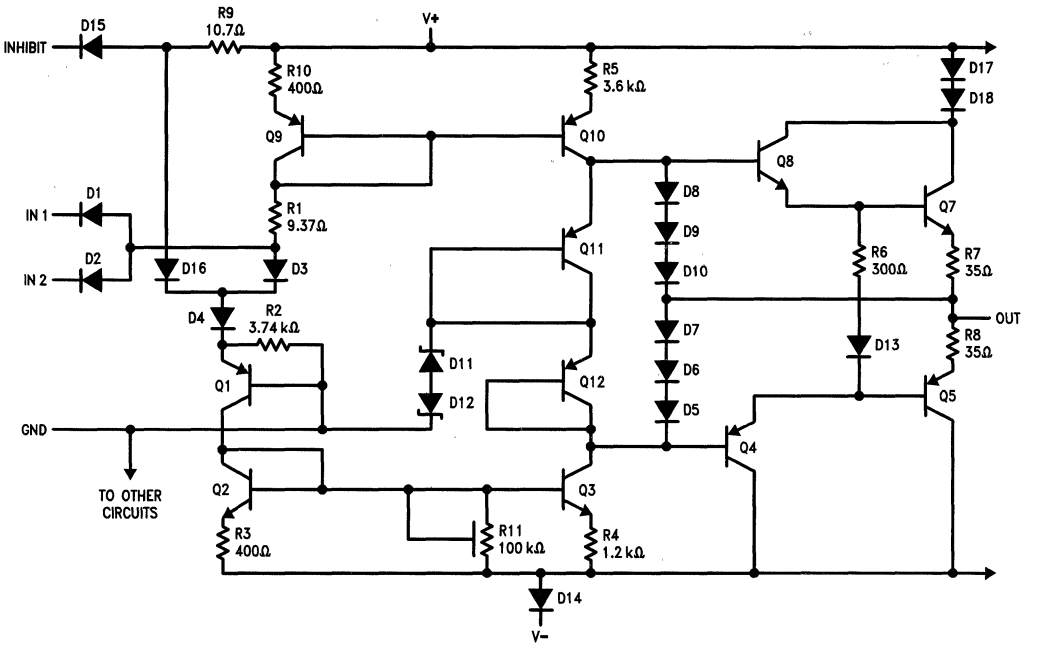
FIGURE 1. Switching Time Test Circuit and Waveforms

Primary Burn-In Circuit



TL/F/10815–5

Equivalent Circuit (⅓ of circuit)



TL/F/10815–6

National Semiconductor

DS9627 Dual Line Receiver

General Description

The DS9627 is a dual-line receiver which meets the electrical interface specifications of EIA RS-232C and MIL-STD-188C. The input circuitry accommodates ±25V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The DS9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V−, the typical switching points are at 2.6V and −2.6V, thus meeting RS-232-C requirements. When pin 1 is open, the typical switching points are at 50 μA and −50 μA, thus satisfying the requirements of MIL-STD-188C LOW level interface. Connecting the RA and/or RB pins to the (−) input yields an input impedance in the range of 3 kΩ to 7 kΩ and satisfies RS-232-C requirements; leaving RA and/or RB pins unconnected, the input resistance will be greater than 6 kΩ to satisfy MIL-STD-188C.

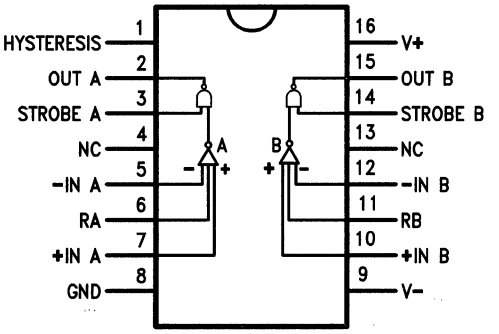
The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wired-OR function. A TTL/DTL strobe is also provided for each receiver.

Features

- EIA RS-232-C input standards
- MIL-STD-188C input standards
- Variable hysteresis control
- High common mode rejection
- R control (5 kΩ or 10 kΩ)
- Wired-OR capability
- Choice of inverting and non-inverting inputs
- Outputs and strobe TTL compatible

Connection Diagram

16-Lead DIP



TL/F/9761–1

Top View

Order Number DS9627MJ/883
See NS Package Number J16A

For Complete Military 883 Specifications, see RETS Data Sheet.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Internal Power Dissipation (Note 5)	400 mW
V^+ to GND	0V to +15V
V^- to GND	0V to −15V
Input Voltage Referred to GND	±25V
Strobe to GND	−0.5V to +5.5V
Applied Output Voltage	−0.5V to +15V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)	−55	+125	°C

Electrical Characteristics

Hysteresis, −IN A, −IN B, RA and RB Open for MIL-STD-188C, unless otherwise specified (Notes 2 and 3)

Symbol	Characteristics	Conditions		Min	Max	Units
V_{OL}	Output Voltage LOW	$V^+ = 10.8V, V^- = -13.2V,$ $V_I^+ = 0.6V, I_{OL} = 6.4$ mA			0.4	V
V_{OH}	Output Voltage HIGH	$V^+ = 10.8V, V^- = -13.2V,$ $V_I^+ = 0.6V, I_{OH} = -0.5$ mA		2.4		V
I_{OS}	Output Short Circuit Current (Note 4)	$V^+ = 13.2V, V^- = -10.8V,$ $V_I^+ = 0.6V, V_O = 0V$		−3.0		mA
$I_{IH}(ST)$	Input Current HIGH (Strobe)	$V^+ = 10.8V,$ $V^- = -13.2V, V_I^+ = 0.6V$	$V_{ST} = 2.4V$		40	μA
			$V_{ST} = 5.5V$		1.0	mA
R_I	Input Resistance	$V^+ = 13.2V, V^- = -13.2V,$ $-3.0V \le V_I^+ \le 3.0V$		6.0		kΩ
I_{TH}^+	Positive Threshold Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V,$ $V_O = 2.4V$			100	μA
I_{TH}^-	Negative Threshold Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V,$ $V_O = 0.4V$		−100		μA
$V_{IL}(ST)$	Input Voltage LOW (Strobe)	$V_I^+ = -0.6V$			0.8	V
$V_{IH}(ST)$	Input Voltage HIGH (Strobe)	$V^+ = 13.2V, V^- = -10.8V,$ $V_I^+ = -0.6V$		2.0		V
I^+	Positive Supply Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$ $V_I^+ = -0.6V$			18	mA
I^-	Negative Supply Current	$\pm 10.8V \le V_{CC} \le \pm 13.2V$ $V_I^+ = 0.6V$		−16		mA

Electrical Characteristics

+IN A and −IN B connected to ground, RA and RB connected to −IN A and −IN B and Hysteresis connected to V^- for RS-232C, unless otherwise specified

Symbol	Characteristics	Conditions	Min	Max	Units
R_I	Input Resistance	$3.0V \le V_I \le 25V$	3.0	7.0	kΩ
		$-3.0V \le V_I \le -25V$	3.0	7.0	kΩ
V_I	Input Voltage		−2.0	2.0	V
V_{TH+}	Positive Threshold Voltage			3.0	V
V_{TH-}	Negative Threshold Voltage		−3.0		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range.

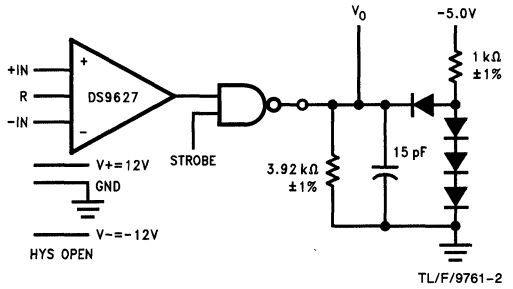
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

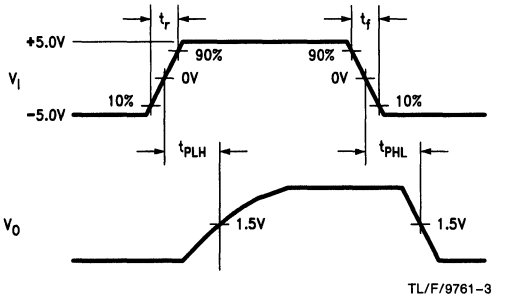
Note 5: Rating applies to ambient temperatures up to +125°C. Above 125°C ambient, derate linearity at 120°C/W.

Electrical Characteristics $V_{CC} = \pm 12V$ for MIL-STD-188C and RS-232C, $T_A = 25°C$

Symbol	Characteristics	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay to High Level	(See *Figure 1*)		250	ns
t_{PHL}	Propagation Delay to Low Level	(See *Figure 1*)		250	ns



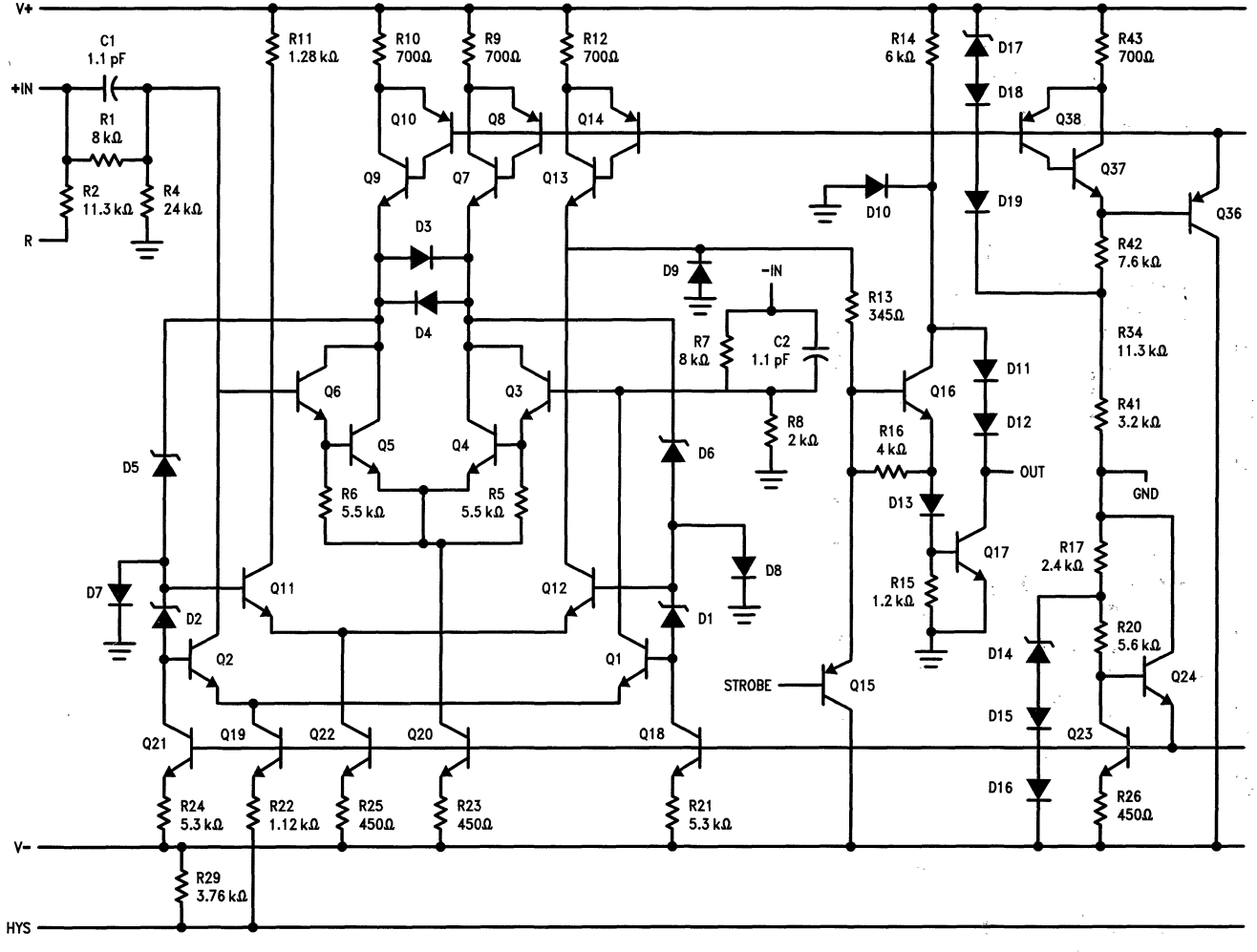
15 pF includes jig capacitance. All diodes are FD777 or equivalent.



PRR = 10 kHz
PW = 50 μs
$t_r = t_f = 5$ ns

FIGURE 1. Switching Time Test Circuit and Waveforms

Equivalent Circuit (½ of Circuit)



TL/F/9761–4

Section 3

RS-422/423 Line Drivers and Receivers

Section 3 Contents

National Semiconductor

DS1691A/DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE® Outputs

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 single-ended line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to slow the rise time for suppression of near end crosstalk to other receivers in the cable. Rise time capacitors are primarily intended for waveshaping output signals in the single-ended driver mode. Multipoint applications in differential mode with waveshaping capacitors is not allowed.

With the mode select pin low, the DS1691A/DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

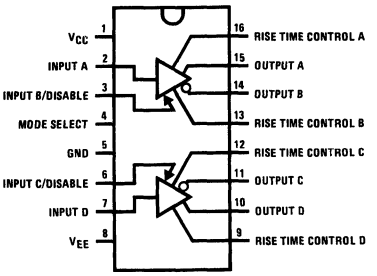
Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- TRI-STATE outputs in RS-422 mode
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - RS-422: I_{CC} = 9 mA/driver typ
  - RS-423: I_{CC} = 4.5 mA/driver typ; I_{EE} = 2.5 mA/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Pin compatible with AM26LS30

3

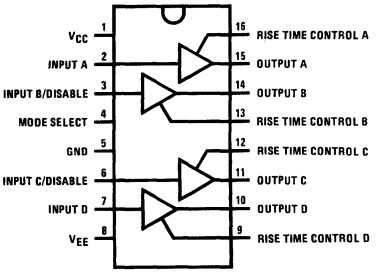
Connection Diagrams

With Mode Select LOW (RS-422 Connection)



Top View TL/F/5783–1

With Mode Select HIGH (RS-423 Connection)

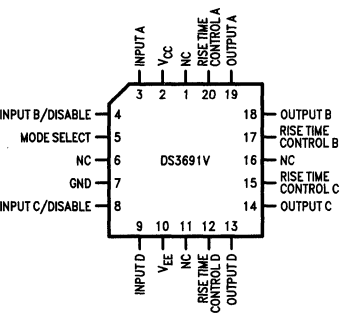


Top View TL/F/5783–2

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

Order Number DS1691AJ, DS3691J, DS3691M, DS3691N or DS3691V
See NS Package Number J16A, M16A, N16A or V20A
For Complete Military 883 Specifications, see RETS Data Sheet
Order Number DS1691AJ/883
See NS Package Number J16A



TL/F/5783–18

Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to + 150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1691A			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1691A	−55	+125	°C
DS3691	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		V_{IN} ≤ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Differential Output Voltage	R_L = ∞	V_{IN} = 2V		3.6	6.0	V
$\overline{V_O}$	$V_{A,B}$		V_{IN} = 0.8V		−3.6	−6.0	V
V_T	Differential Output Voltage	R_L = 100Ω	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$	$V_{A,B}$	V_{CC} ≥ 4.75V	V_{IN} = 0.8V	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE}$ = 2.4V		±10			V
I_{XA}	Output Leakage Current Power OFF	V_{CC} = 0V	V_{CMR} = 10V			100	μA
I_{XB}			V_{CMR} = −10V			−100	μA
I_{OX}	TRI-STATE Output Current	V_{CC} = Max	V_{CMR} ≤ 10V			100	μA
		V_{EE} = 0V and −5V	V_{CMR} ≥ −10V			−100	μA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Output Rise Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_f	Output Fall Time	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns
t_{PZH}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PLZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		180	300	ns
t_{PHZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF *(Figure 4)*		250	350	ns

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\|V_{CC}\| = \|V_{EE}\|$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	μA
		$V_{IN} \leq$ 15V			10	100	μA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Output Voltage	R_L = ∞, (Note 6) $V_{CC} \geq$ 4.75V	V_{IN} = 2V	4.0	4.4	6.0	V
$\overline{V_O}$			V_{IN} = 0.4V	−4.0	−4.4	−6.0	V
V_T	Output Voltage	R_L = 450Ω $V_{CC} \geq$ 4.75V	V_{IN} = 2.4V	3.6	4.1		V
$\overline{V_T}$			V_{IN} = 0.4V	−3.6	−4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\|$ = 4.75V, R_L = 450Ω			0.02	0.4	V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = 6V		2	100	μA
I_X^-	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = −6V		−2	−100	μA
I_S^+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

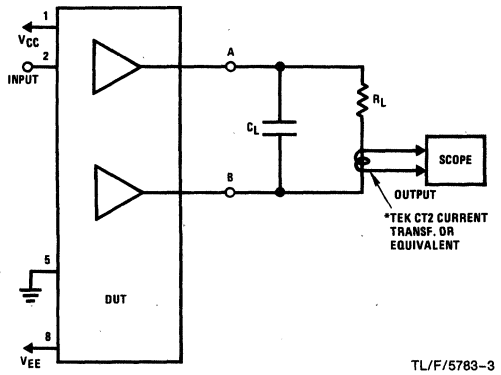
Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Note 6: At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

AC Electrical Characteristics T_A = 25°C (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, V_{CC} = 5V, V_{EE} −5V, MODE SELECT = 2.4V						
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		120	300	ns
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		μs
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF *(Figure 3)*		3.0		μs
t_{rc}	Rise Time Coefficient	R_L = 450Ω, C_L = 500 pF, C_C = 50 pF *(Figure 3)*		0.06		μs/pF
t_{PDH}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns
t_{PDL}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 *(Figure 2)*		180	300	ns

AC Test Circuits and Switching Time Waveforms



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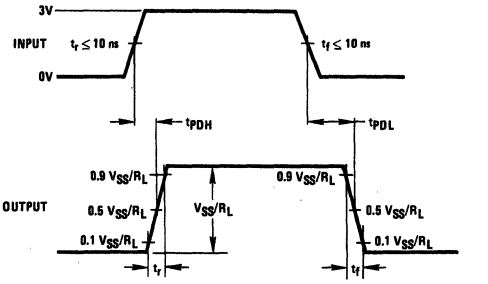

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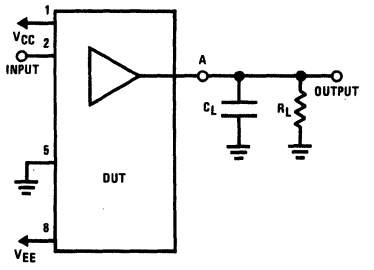
FIGURE 1. Differential Connection



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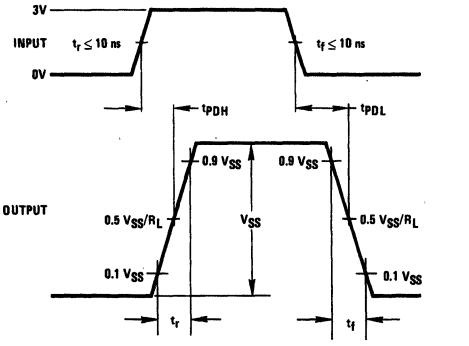

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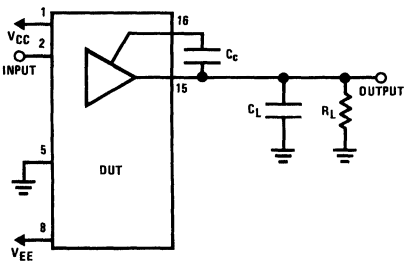
FIGURE 2. RS-423 Connection

AC Test Circuits and Switching Time Waveforms (Continued)



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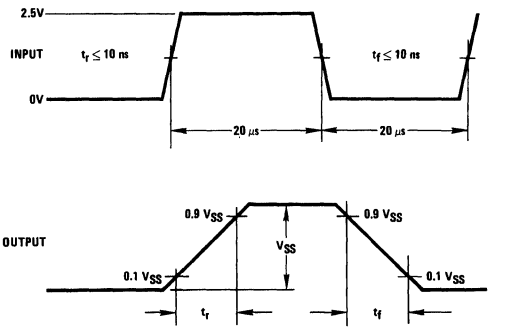

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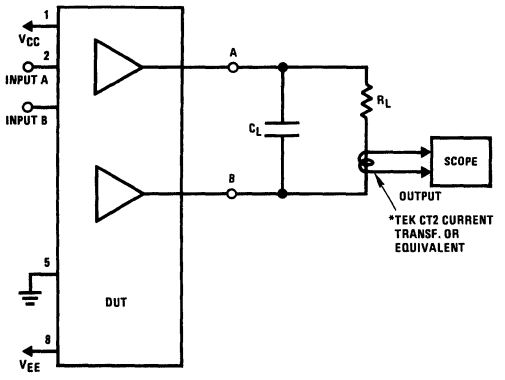
FIGURE 3. Rise Time Control for RS-423



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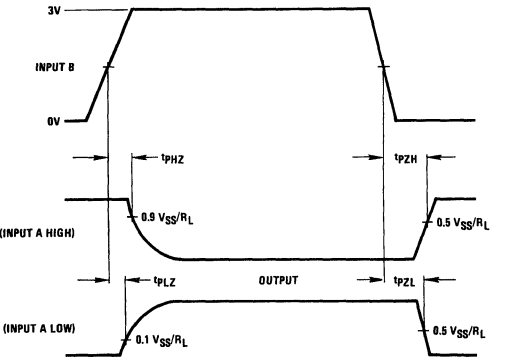

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FIGURE 4. TRI-STATE Delays

Switching Waveforms

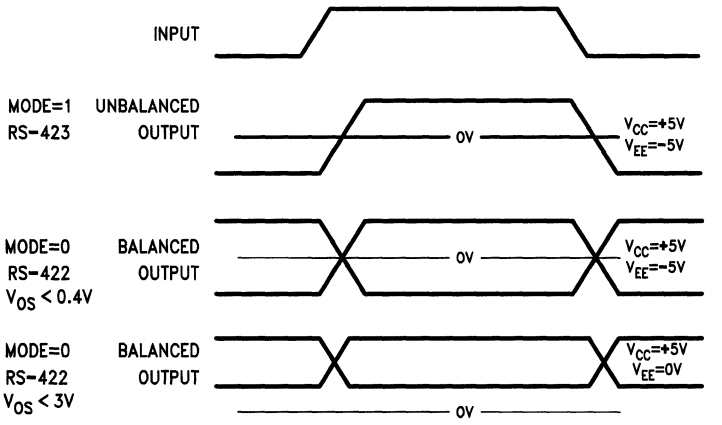

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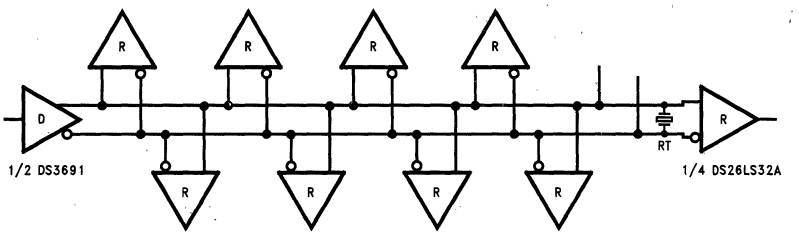
FIGURE 5. Typical Output Voltage

Typical Application Information

Fully Loaded RS-422 Interface



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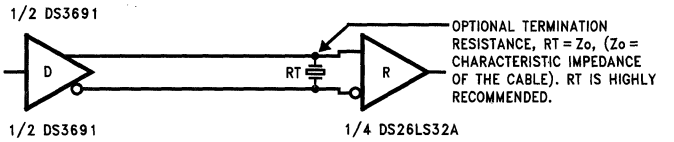
RS-422 Point to Point Application



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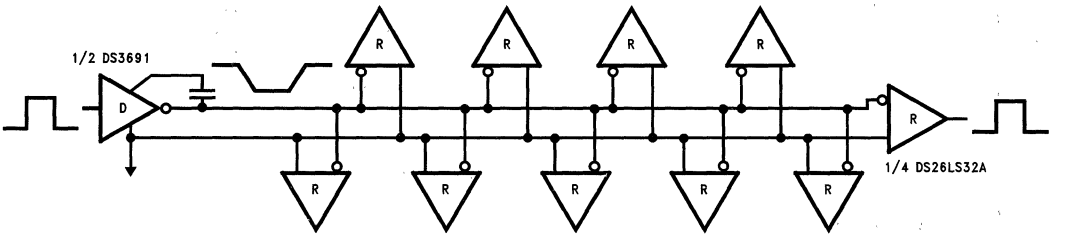
Fully Loaded RS-423 Interface



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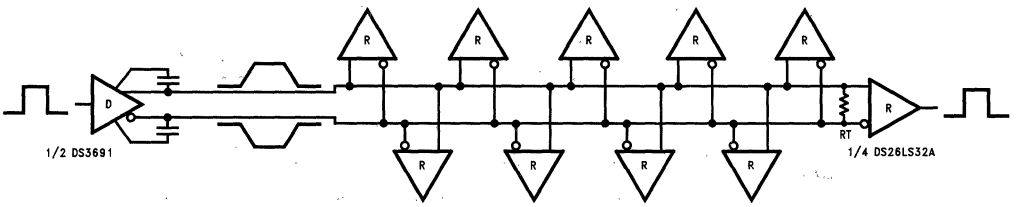
Differential Application with Rise Time Control



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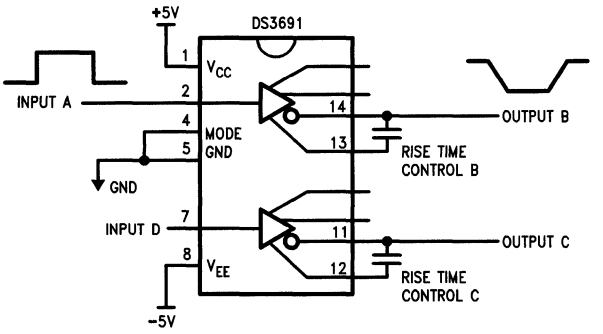
***Note:** Controlled edge allows longer stub lengths. Multiple Drivers are NOT allowed.

Typical Application Information (Continued)

Dual RS-423 Inverting Driver



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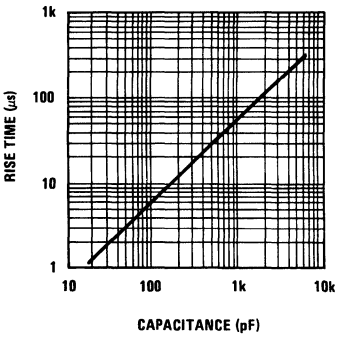
Typical Rise Time Control Characteristics (RS-423 Mode)

Rise Time vs External Capacitor



TL/F/5783–12

National Semiconductor

DS26C31T/DS26C31M
CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (see Note 8). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

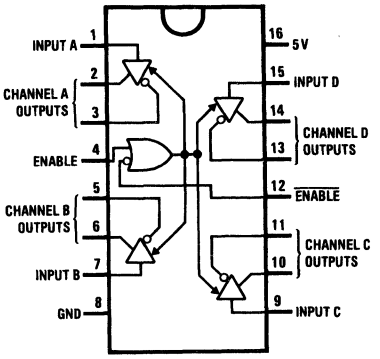
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs will not load line when V_{CC} = 0V
- DS26C31T meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount
- Mil-Std-883C compliant

Connection Diagrams

Dual-In-Line Package



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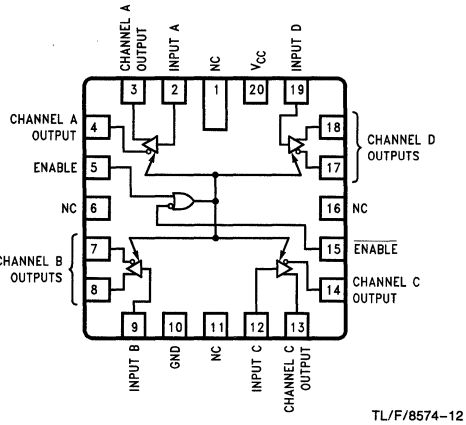
Top View

Order Number DS26C31TJ, DS26C31TM or DS26C31TN
See NS Package Number J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet

Order Number DS26C31ME/883, DS26C31MJ/883 or DS26C31MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier (E)



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Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Max. Power Dissipation (P_D) @25°C (Note 3)	
Ceramic "J" Pkg.	2419 mW
Plastic "N" Pkg.	1736 mW
SOIC "M" Pkg.	1226 mW
Ceramic "W" Pkg.	1182 mW
Ceramic "E" Pkg.	2134 mW
Lead Temperature (T_L) (Soldering, 4 sec.)	260°C

This device does not meet 2000V ESD Rating. (Note 13)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS26C31T	−40	+85	°C
DS26C31M	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 20 mA			0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100Ω (Note 5)		2.0	3.1		V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference In Differential Output	R_L = 100Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100Ω (Note 5)			1.8	3.0	V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$	Difference In Common Mode Output	R_L = 100Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current (Note 6)	DS26C31T I_{OUT} = 0 μA	V_{IN} = V_{CC} or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.0	mA
		DS26C31M I_{OUT} = 0 μA	V_{IN} = V_{CC} or GND		200	500	μA
			V_{IN} = 2.4V or 0.5V (Note 6)		0.8	2.1	mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, ENABLE = V_{IL}, $\overline{\text{ENABLE}}$ = V_{IH}			±0.5	±5.0	μA

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Notes 5, 7)		−30		−150	mA
I_{OFF}	Output Leakage Current Power Off (Note 5)	DS26C31T V_{CC} = 0V	V_{OUT} = 6V			100	μA
			V_{OUT} = −0.25V			−100	μA
		DS26C31M V_{CC} = 0V	V_{OUT} = 6V			100	μA
			V_{OUT} = 0V (Note 8)			−100	μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N package at 13.89 mW/°C, J package 16.13 mW/°C, M package 9.80 mW/°C, E package 12.20 mW/°C, and W package 6.75 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Note 8: The DS26C31M (−55°C to +125°C) is tested with V_{OUT} between +6V and 0V while RS-422A condition is +6V and −0.25V.

Switching Characteristics V_{CC} = 5V ±10%, $t_r \leq 6$ ns, $t_f \leq 6$ ns (*Figures 1, 2, 3* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C31T	CS26C31M	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	S1 Open	2	6	11	14	ns
Skew	(Note 9)	S1 Open		0.5	2.0	3.0	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	14	ns
t_{PZH}	Output Enable Time	S1 Closed		11	19	22	ns
t_{PZL}	Output Enable Time	S1 Closed		13	21	28	ns
t_{PHZ}	Output Disable Time (Note 10)	S1 Closed		5	9	12	ns
t_{PLZ}	Output Disable Time (Note 10)	S1 Closed		7	11	14	ns
C_{PD}	Power Dissipation Capacitance (Note 11)			50			pF
C_{IN}	Input Capacitance			6			pF

Note 9: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 10: Output disable time is the delay from ENABLE or $\overline{\text{ENABLE}}$ being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 11: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

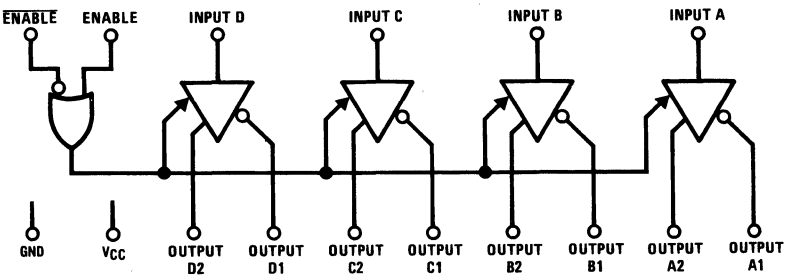
V_{CC} = 5V, T_A = 25°C, $t_r \leq 6$ ns, $t_f \leq 6$ ns (*Figures 2, 4, 5* and *6*) (Note 12)

Symbol	Parameter	Conditions	DS26C31T		DS26LS31C		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delays Input to Output	C_L = 30 pF S1 Closed S2 Closed	6	8	10	15	ns
Skew	(Note 9)	C_L = 30 pF S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times	C_L = 30 pF S1 Closed S2 Closed	4	6			ns
t_{PLZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Closed S2 Open	6	9	15	35	ns
t_{PHZ}	Output Disable Time (Note 10)	C_L = 10 pF S1 Open S2 Closed	4	7	15	25	ns
t_{PZL}	Output Enable Time	C_L = 30 pF S1 Closed S2 Open	14	20	20	30	ns
t_{PZH}	Output Enable Time	C_L = 30 pF S1 Open S2 Closed	11	17	20	30	ns

Note 12: This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or guaranteed.

Note 13: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥ 1500V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Logic Diagram



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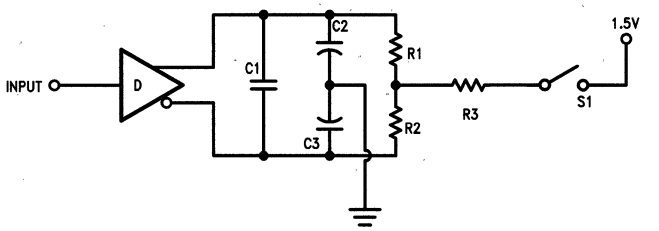
AC Test Circuit and Switching Time Waveforms



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Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

FIGURE 1. AC Test Circuit

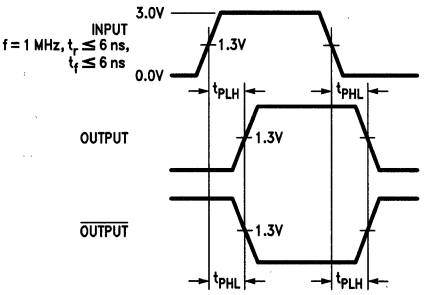

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FIGURE 2. Propagation Delays

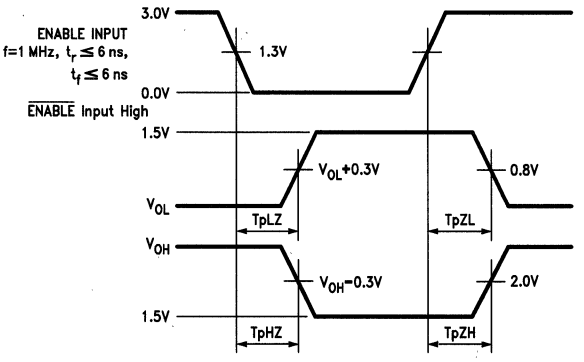

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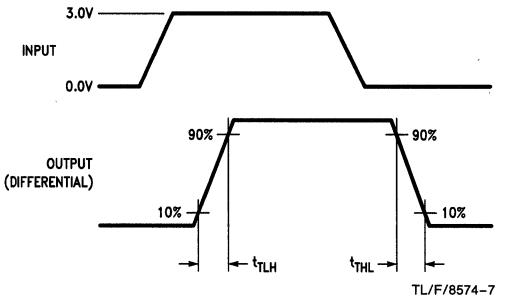
FIGURE 3. Enable and Disable Times



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Input pulse; f = 1 MHz, 50%; $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

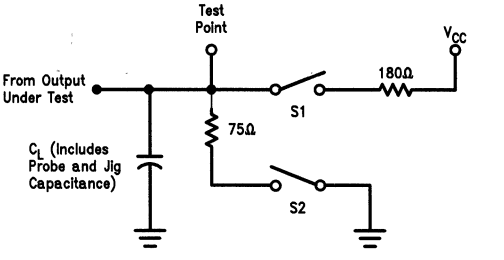

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FIGURE 5. Load AC Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)

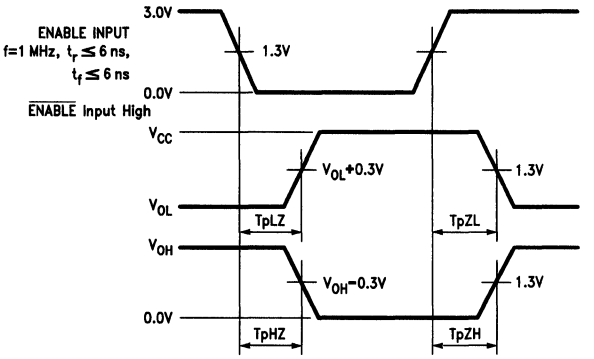

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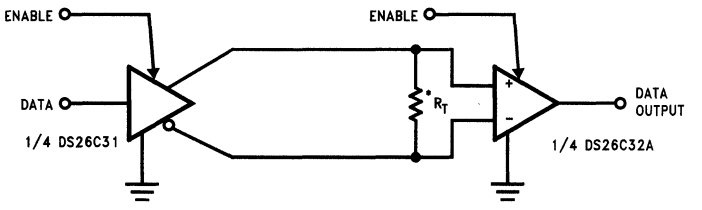
FIGURE 6. Enable and Disable Times for "LS-Type" Load

Typical Applications

Two-Wire Balanced System, RS-422



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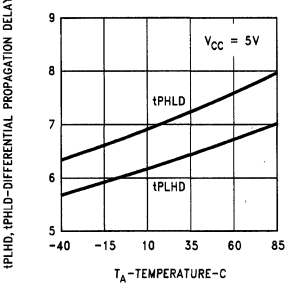
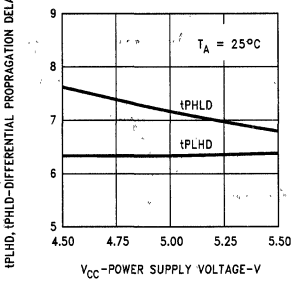
*R_T is optional although highly recommended to reduce reflection.

Typical Performance Characteristics

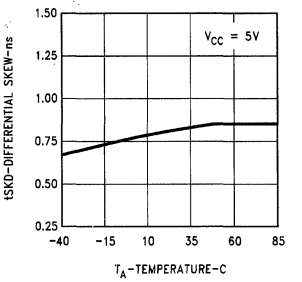
Differential Propagation Delay vs Temperature



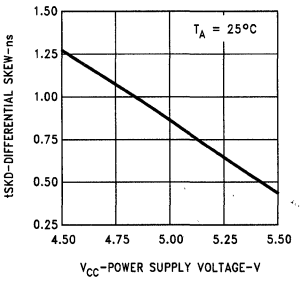
Differential Propagation Delay vs Power Supply Voltage



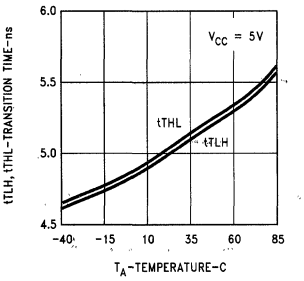
Differential Skew vs Temperature



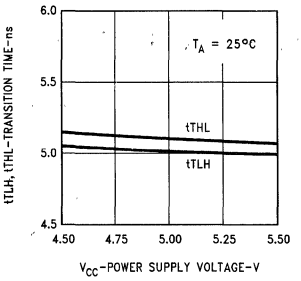
Differential Skew vs Power Supply Voltage



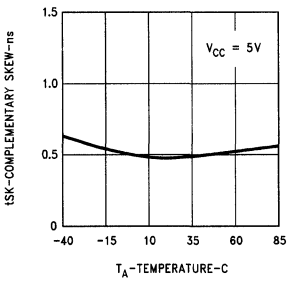
Differential Transition Time vs Temperature



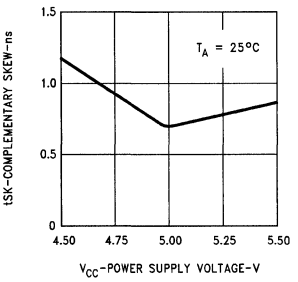
Differential Transition Time vs Power Supply Voltage



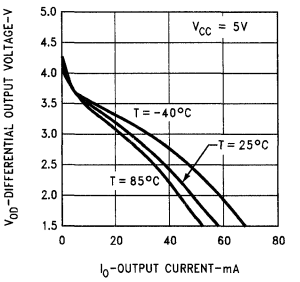
Complementary Skew vs Temperature



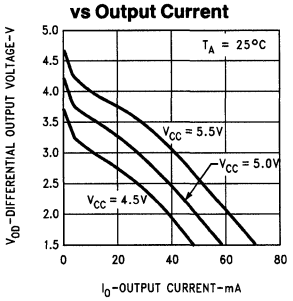
Complementary Skew vs Power Supply Voltage



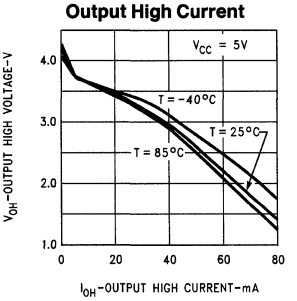
Differential Output Voltage vs Output Current



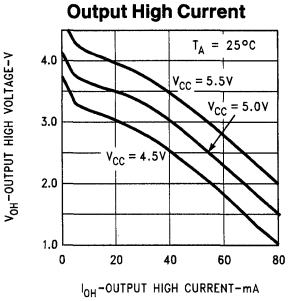
Differential Output Voltage vs Output Current



Output High Voltage vs Output High Current



Output High Voltage vs Output High Current



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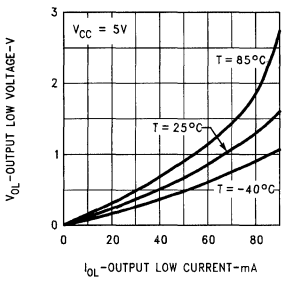
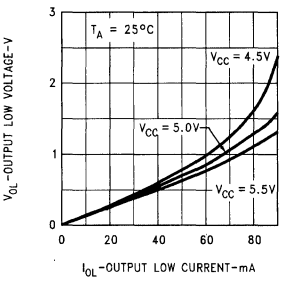
Typical Performance Characteristics (Continued)

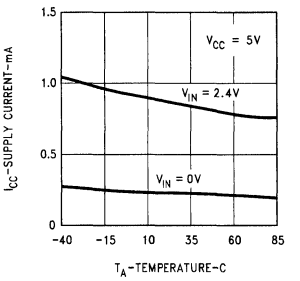
Output Low Voltage vs Output Low Current



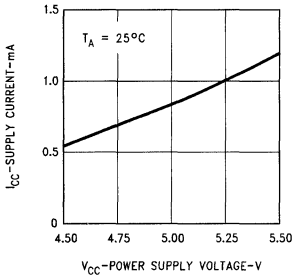
Output Low Voltage vs Output Low Current



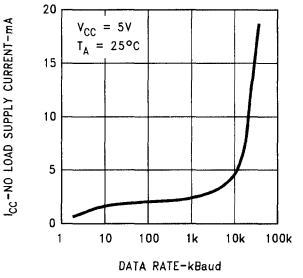
Supply Current vs Temperature



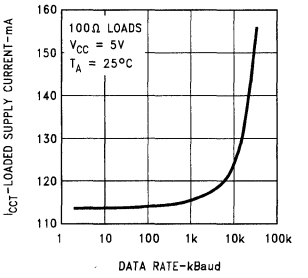
Supply Current vs Power Supply Voltage



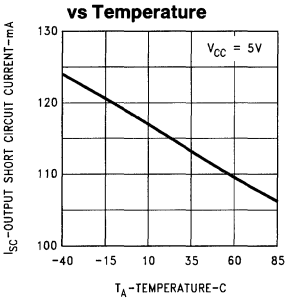
No Load Supply Current vs Data Rate



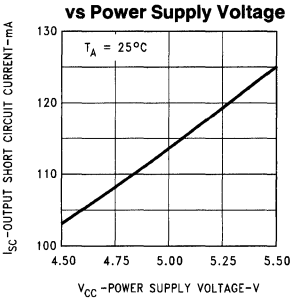
Loaded Supply Current vs Data Rate



Output Short Circuit Current vs Temperature



Output Short Circuit Current vs Power Supply Voltage



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National Semiconductor

ADVANCE INFORMATION

DS26LV31
3V Enhanced CMOS Quad Differential Line Driver

General Description

The DS26LV31 is a high-speed quad differential CMOS driver that is compatible with both TIA/EIA-422-B and CCITT V.11. The CMOS DS26LV31 features low I_{CC} of XX mA MAX which makes it ideal for battery powered and power conscious applications.

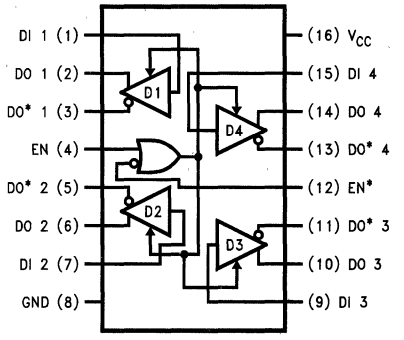
The TRI-STATE® enables, EN and $\overline{EN}$, allow the device to be active High or active Low. The enables are common to all four drivers. Protection diodes protect all the driver inputs against electrostatic discharge. The driver inputs (DI) are compatible with TTL and CMOS levels.

Features

- Low power design
  — $I_{CC} \leq 500\ \mu A$ max
- Compatible with TIA/EIA-422-B (RS-422) and CCITT V.11 recommendation
- Guaranteed AC parameter:
  — Maximum driver skew TBD
  — Transition time TBD
- Pin compatible with DS26C31
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package
DS26LV31



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Order Number DS26LV31M or DS26LV31N
See NS Package Number M16A or N16A

Truth Table

Enables		Input	Outputs	
EN	**$\overline{EN}$**	**DI**	**DO**	**$\overline{DO}$**
L	H	X	Z	Z
H	L	H	H	L
H	H	L	L	H
L	L			

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

National Semiconductor

DS26F31C/DS26F31M
Quad High Speed Differential Line Driver

General Description

The DS26F31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26F31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The DS26F31 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F31 features lower power, extended temperature range, and improved specifications.

The circuit provides an enable and disable function common to all four drivers. The DS26F31C/DS26F31M features TRI-STATE® outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

The DS26F31C/DS26F31M offers optimum performance when used with the DS26F32 Quad Differential Line Receiver.

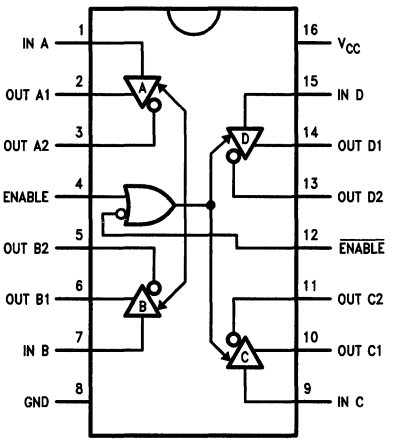
Features

- Military temperature range
- Output skew—2.0 ns typical
- Input to output delay—10 ns
- Operation from single +5.0V supply
- 16-lead ceramic DIP Package
- Outputs won't load line when V_{CC} = 0V
- Output short circuit protection
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines

3

Connection and Logic Diagrams

16-Lead Dual-In-Line Package



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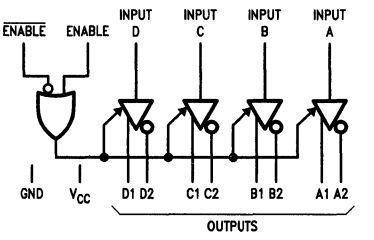
Top View

Order Number DS26F31CJ or DS26F31MJ
See NS Package Number J16A

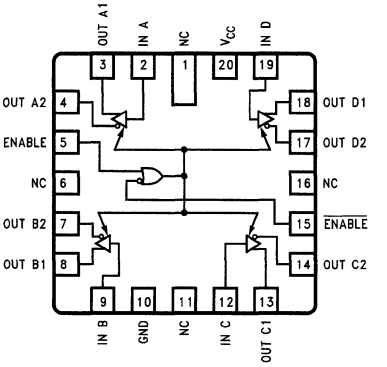
For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS26F31ME/883, DS26F31MJ/883, or DS26F31MW/883
See NS Package Numbers E20A, J16A, or W16A



TL/F/9614-2

FIGURE 1. Logic Symbol

20-Lead Ceramic Leadless Chip Carrier (E)



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Lead Temperature	
Ceramic DIP (Soldering, 60 sec.)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Supply Voltage	7.0V
Input Voltage	7.0V
Output Voltage	5.5V

*Derate cavity package 10 mW/°C above 25°C.

Operating Range

DS26F31C	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS26F31M	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output Voltage HIGH	V_{CC} = Min, I_{OH} = −20 mA	2.5	3.2		V
V_{OL}	Output Voltage LOW	V_{CC} = Min, I_{OL} = 20 mA		0.32	0.5	V
V_{IH}	Input Voltage HIGH	V_{CC} = Min	2.0			V
V_{IL}	Input Voltage LOW	V_{CC} = Max			0.8	V
I_{IL}	Input Current LOW	V_{CC} = Max, V_I = 0.4V		−0.10	−0.20	mA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_I = 2.7V		0.5	20	μA
I_{IR}	Input Reverse Current	V_{CC} = Max, V_I = 7.0V		0.001	0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max, V_O = 2.5V		0.5	20	μA
		V_{CC} = Max, V_O = 0.5V		0.5	−20	μA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA		−0.8	−1.5	V
I_{OS}	Output Short Circuit	V_{CC} = Max (Note 4)	−30	−60	−150	mA
I_{CCX}	Supply Current	V_{CC} = Max, All Outputs Disabled			50	mA
I_{CC}		V_{CC} = Max, All Outputs Enabled			40	mA
t_{PLH}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5, Note 6		10	15	ns
t_{PHL}	Input to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5		10	15	ns
SKEW	Output to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5, Note 6		2.0	4.5	ns
t_{LZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF		23	32	ns
t_{HZ}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, C_L = 10 pF		15	25	ns
t_{ZL}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5		20	30	ns
t_{ZH}	Enable to Output	V_{CC} = 5.0V, T_A = 25°C, Load = Note 5		23	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F31M and across the 0°C to +70°C range for the DS26F31C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

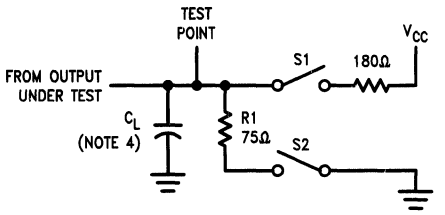
Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: C_L = 30 pF, V_I = 1.3V to V_O = 1.3V, V_{PULSE} = 0V to +3V (See AC Load Test Circuit for TRI-STATE Outputs).

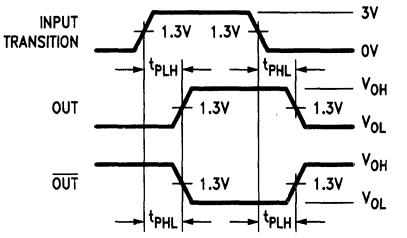
Note 6: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Test Circuit and Timing Waveforms



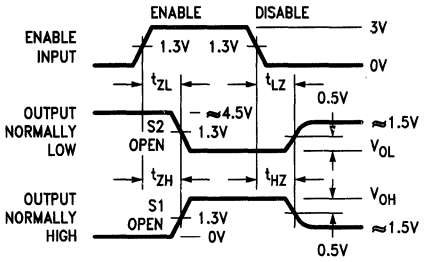
TL/F/9614–3

FIGURE 2. AC Load Test Circuit for TRI-STATE Outputs



TL/F/9614–4

FIGURE 3. Propagation Delay (Notes 1 and 3)



TL/F/9614–5

FIGURE 4. Enable and Disable Times (Notes 2 and 3)

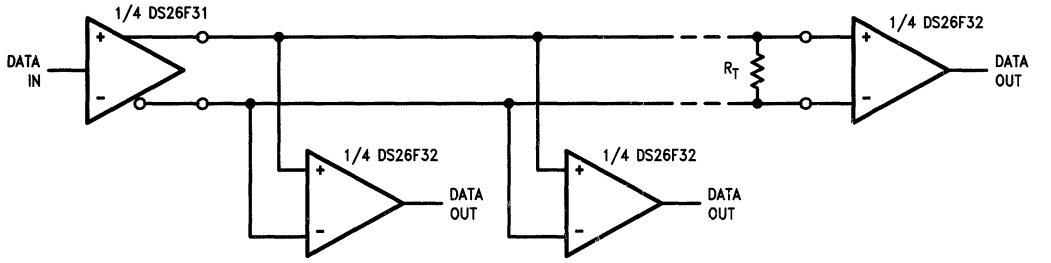
Note 1: Diagram shown for Enable Low. Switches S1 and S2 open.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator for all Pulses: Rate ≤ 1.0 MHz, $Z_O = 50\Omega$, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns.

Note 4: C_L includes probe and jig capacitance.

Typical Application



TL/F/9614–6

FIGURE 5. Typical Application

National Semiconductor

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

General Description

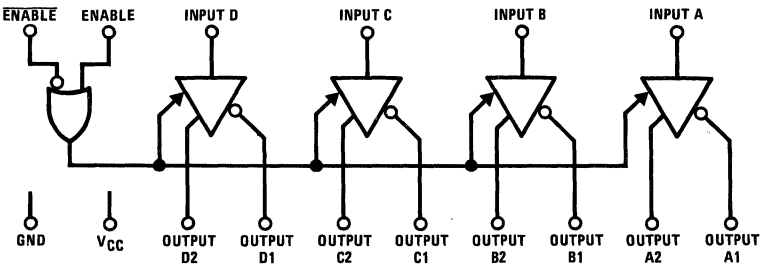
The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

Features

- Output skew—2.0 ns typical
- Input to output delay—10 ns typical
- Operation from single 5V supply
- Outputs won't load line when V_{CC} = 0V
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range

Logic and Connection Diagrams



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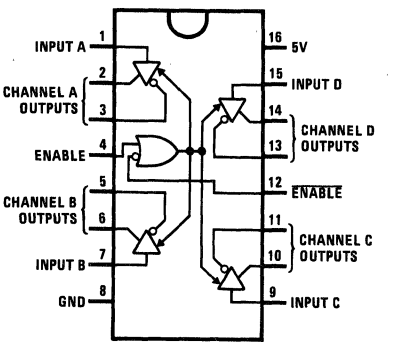
Dual-In-Line Package



TL/F/5778–2

Top View
Order Number DS26LS31CJ, DS26LS31CM, DS26LS31CN or DS26LS31MJ
See NS Package Number J16A, M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS26LS31MJ/883 or DS26LS31MW/883
See NS Package J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5.5V
Output Voltage (Power OFF)	−0.25 to 6V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.9 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage	I_{OH} = −20 mA	2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA			0.5	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V		−40	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.7V			20	μA
I_I	Input Reverse Current	V_{IN} = 7V			0.1	mA
I_O	TRI-STATE Output Current	V_O = 2.5V			20	μA
		V_O = 0.5V			−20	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA			−1.5	V
I_{SC}	Output Short-Circuit Current		−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Input to Output	C_L = 30 pF		10	15	ns
t_{PHL}	Input to Output	C_L = 30 pF		10	15	ns
Skew	Output to Output	C_L = 30 pF		2.0	6.0	ns
t_{LZ}	Enable to Output	C_L = 10 pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	C_L = 10 pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	C_L = 30 pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	C_L = 30 pF, S1 Open		20	30	ns

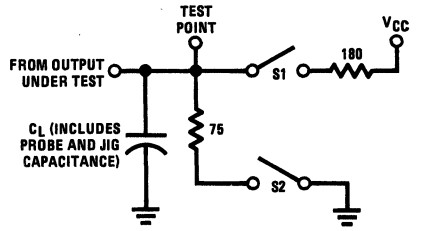
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS726LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



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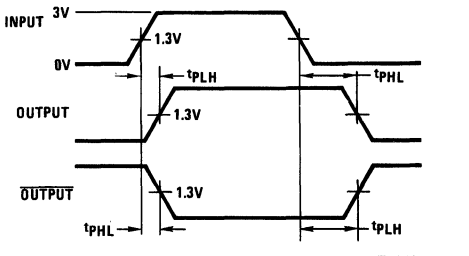
Note: S1 and S2 of load circuit are closed except where shown.

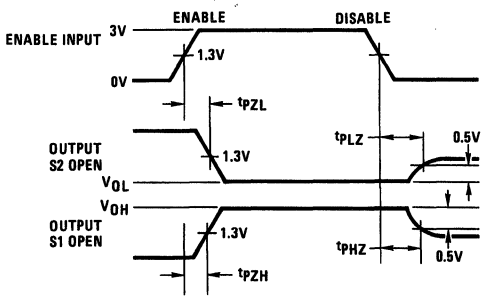
FIGURE 1. AC Test Circuit



TL/F/5778–4

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 2. Propagation Delays



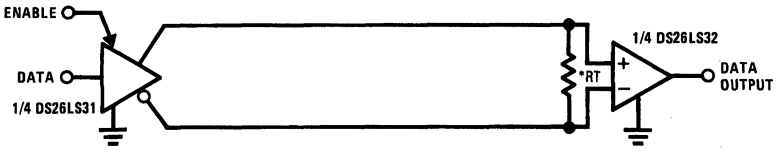
TL/F/5778–5

f = 1 MHz, $t_r \leq 15$ ns, $t_f \leq 6$ ns

FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422



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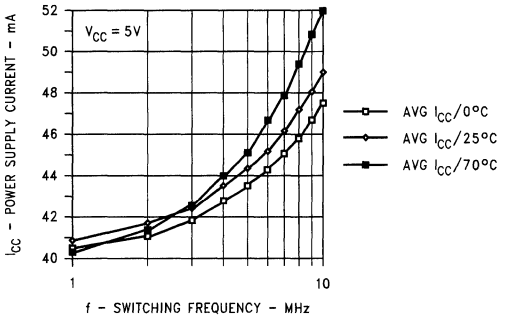
*R_T is optional although highly recommended to reduce reflection.

Typical Performance Characteristics

DS26LS31CN Unloaded I_C vs Frequency vs T_A



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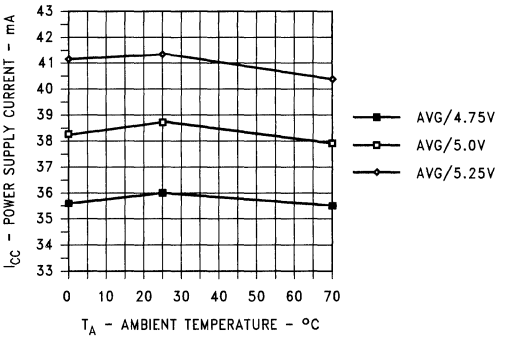
DS26LS31 I_{CC} vs V_{CC} vs T_A



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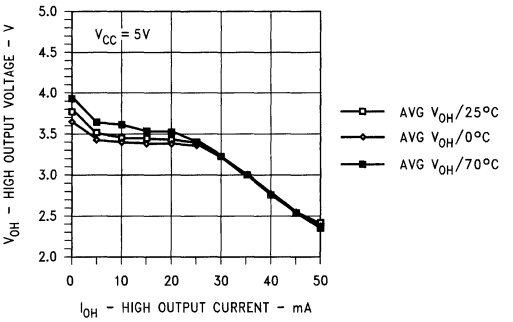
DS26LS31CN V_{OH} vs I_{OH} vs T_A



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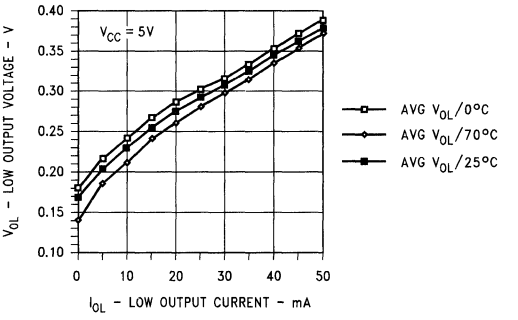
DS26LS31CN V_{OL} vs I_{OL} vs T_A



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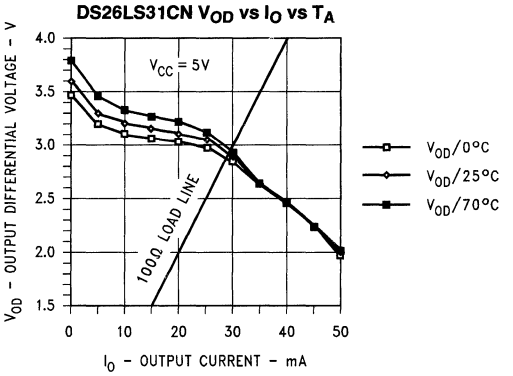
DS26LS31CN V_{OD} vs I_O vs T_A



TL/F/5778–11

National Semiconductor

DS26C32AT/DS26C32AM
Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

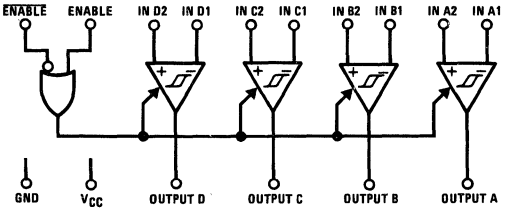
The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- CMOS design for low power
- ±0.2V sensitivity over input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses
- Available in Surface Mount
- Mil-Std-883C compliant

Logic Diagram



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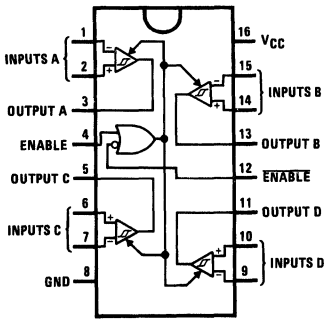
Connection Diagrams

Dual-In-Line Package



TL/F/8764–2

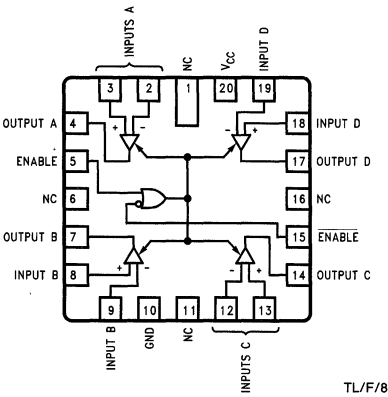
Top View

Order Number DS26C32ATJ, DS26C32ATM or DS26C32ATN
See NS Package J16A, M16A or N16E

For Complete Military 883 Specifications, See RETS Data Sheet.

Order Number DS26C32AME/883, DS26C32AMJ/883 or DS26C32AMW/883
See NS Package E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



TL/F/8764–12

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq V_{TH}$ (Max)	H
		$V_{ID} \leq V_{TH}$ (Min)	L
		Open	H

Z = TRI-STATE

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Pkg.	2308 mW
Plastic "N" Pkg.	1645 mW
SOIC "M" Pkg.	1190 mW
Ceramic "E" Pkg.	2108 mW
Ceramic "W" Pkg.	1215 mW
Maximum Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS26C32AT	−40	+85	°C
DS26C32AM	−55	+125	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$		−200	35	+200	mV
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	DS26C32AT	5.0	6.8	10	kΩ
			DS26C32AM	4.5	6.8	11	kΩ
I_{IN}	Input Current	$V_{IN} = +10V$, Other Input = GND	DS26C32AT		+1.1	+1.5	mA
			DS26C32AM		+1.1	+1.8	mA
		$V_{IN} = -10V$, Other Input = GND	DS26C32AT		−2.0	−2.5	mA
			DS26C32AM		−2.0	−2.7	mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min, $V_{DIFF} = +1V$ $I_{OUT} = -6.0$ mA		3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max, $V_{DIFF} = -1V$ I_{OUT} = 6.0 mA			0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage			2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage					0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{ENABLE} = V_{IL}$, $ENABLE = V_{IH}$			±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND				±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max, $V_{DIF} = +1V$	DS26C32AT		16	23	mA
			DS26C32AM		16	25	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V			60		mV

AC Electrical Characteristics V_{CC} = 5V ±10% (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max		Units
					DS26C32AT	DS26C32AM	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V	10	19	30	35	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	22	29	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	23	29	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply over recommended operating conditions. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥2000V
All other pins ≥1000V
EIAJ (0Ω, 200 pF) ≥350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C, M Package 9.52 mW/°C, E Package 12.04 mW/°C, and W package 6.94 mW/°C.

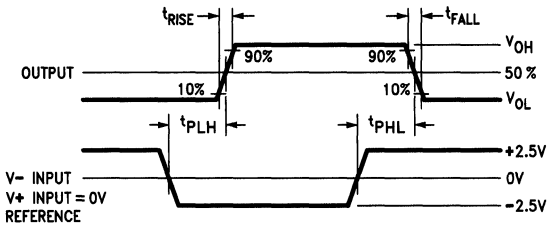
Comparison Table of Switching Characteristics into "LS-Type" Load

(*Figures 4, 5,* and *6*) (Note 6)

Symbol	Parameter	Conditions	DS26C32A	DS26LS32A	Units
			Typ	Typ	
t_{PLH}	Input to Output	C_L = 15 pF	17	23	ns
t_{PHL}			19	23	ns
t_{LZ}	ENABLE to Output	C_L = 5 pF	13	15	ns
t_{HZ}			12	20	ns
t_{ZL}	ENABLE to Output	C_L = 15 pF	13	14	ns
t_{ZH}			13	15	ns

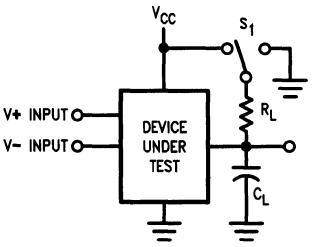
Note 6: This table is provided for comparison purposes only. The values in this table for the DS26C32A reflect the performance of the device, but are not tested or guaranteed.

Test and Switching Waveforms



TL/F/8764-3

FIGURE 1. Propagation Delay



TL/F/8764-4

C_L includes load and test jig capacitance.

S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.

S_1 = Gnd for t_{PZH} and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

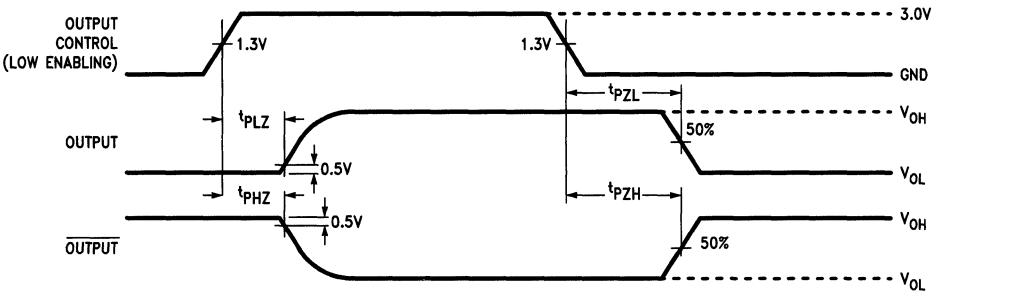


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FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

AC Test Circuit and Switching Time Waveforms

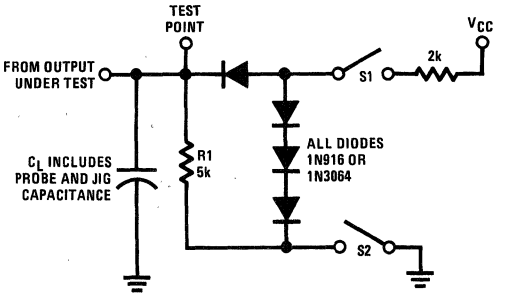

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FIGURE 4. Load Test Circuit for TRI-STATE Outputs for "LS-Type" Load

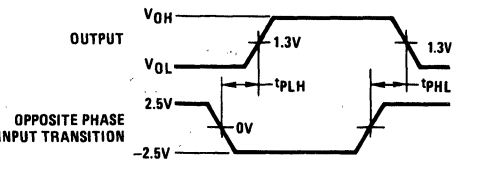

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FIGURE 5. Propagation Delay for "LS-Type" Load (Notes 7, 9)

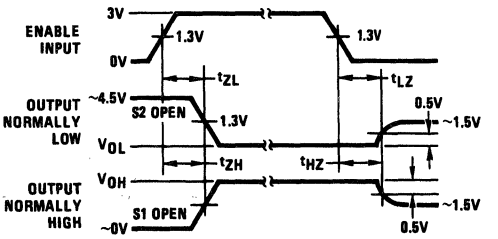

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FIGURE 6. Enable and Disable Times for "LS-Type" Load (Notes 8, 9)

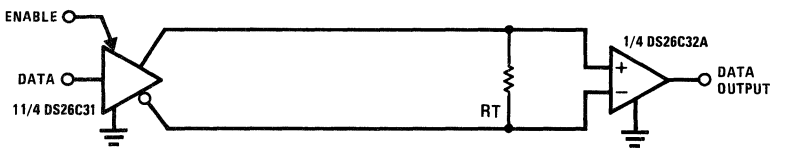
Note 7: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 8: S1 and S2 of load circuit are closed except where shown.

Note 9: Pulse generator for all pulses: Rate ≤ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced Systems, RS-422



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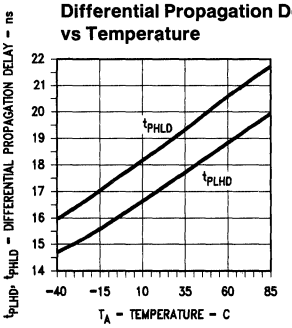
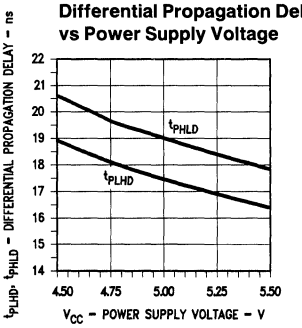
Typical Performance Characteristics

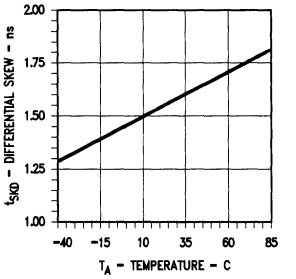
Differential Propagation Delay vs Temperature



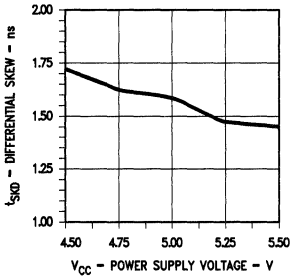
Differential Propagation Delay vs Power Supply Voltage



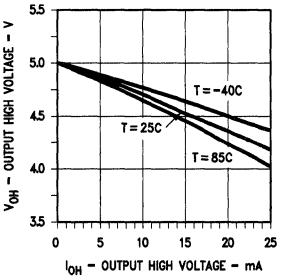
Differential Skew vs Temperature



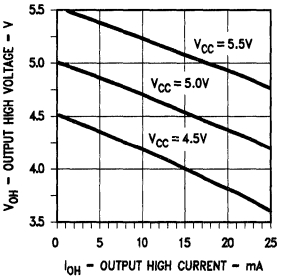
Differential Skew vs Power Supply Voltage



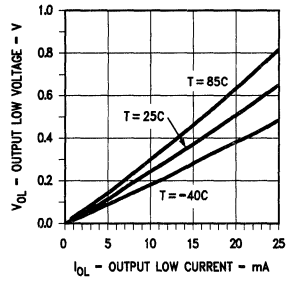
Output High Voltage vs Output High Current



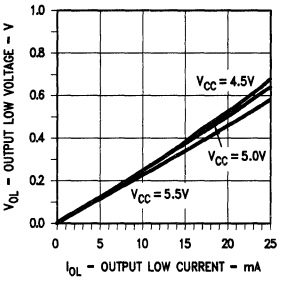
Output High Voltage vs Output High Current



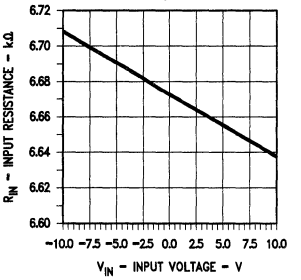
Output Low Voltage vs Output Low Current



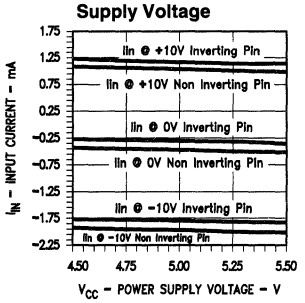
Output Low Voltage vs Output Low Current



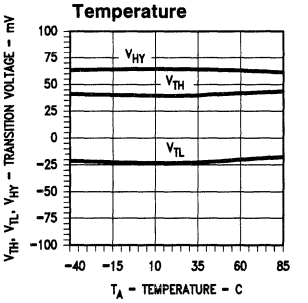
Input Resistance vs Input Voltage



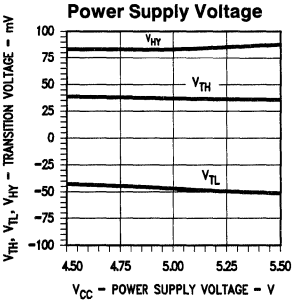
Input Current vs Power Supply Voltage



Hysteresis & Differential Transition Voltage vs Temperature



Hysteresis & Differential Transition Voltage vs Power Supply Voltage



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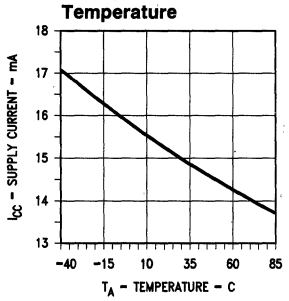
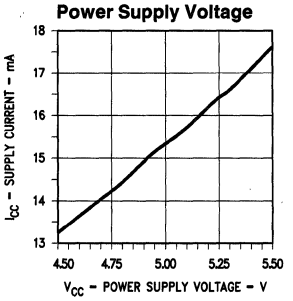
Typical Performance Characteristics (Continued)

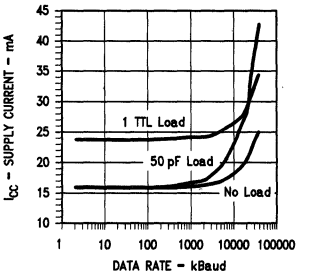
Supply Current vs Temperature



Disabled Supply Current vs Power Supply Voltage



Supply Current vs Data Rate



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National Semiconductor

ADVANCE INFORMATION

DS26LV32A
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS26LV32A is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and CCITT V.11. The CMOS DS26LV32A features low I_{CC} of X mA which makes it ideal for battery powered and power conscious applications.

The TRI-STATE® enables, EN and $\overline{EN}$, allow the device to be active High or active Low. The enables are common to all four receivers.

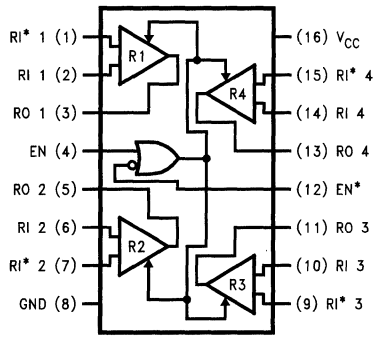
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±7V. The receiver outputs (RO) are compatible with TTL and CMOS levels.

Features

- Low power CMOS design
- Meets TIA/EIA-422-B (RS-422) and CCITT V.11 recommendation
- Receiver OPEN input failsafe feature
- Guaranteed AC parameter:
  - — Maximum receiver skew TBD
  - — Transition time TBD
- Pin compatible with DS26C32A
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package
DS26LV32A



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Order Number DS26LV32AM or DS26LV32AN
See NS Package Number M16A or N16E

Truth Table

Enables		Inputs	Outputs
EN	**$\overline{EN}$**	**RI–RI***	**RO**
L	H	X	Z
H	L	$V_{ID} \geq V_{TH\ (Max)}$	H
H	H	$V_{ID} \leq V_{TH\ (Min)}$	L
L	L	Open	H

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

National Semiconductor

DS26F32C/DS26F32M
Quad Differential Line Receiver

General Description

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE® outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

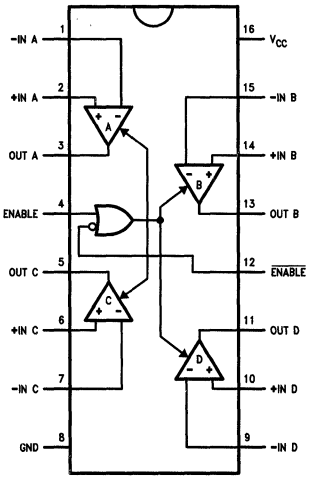
The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

Features

- Military temperature range
- Input voltage range of ±7.0V (differential or common mode) ±0.2V sensitivity over the input voltage range
- Meets all the requirements of EIA standards RS-422 and RS-423
- High input impedance (18k typical)
- 30 mV input hysteresis
- Operation from single +5.0V supply
- Input pull-down resistor prevents output oscillation on unused channels
- TRI-STATE outputs, with choice of complementary enables, for receiving directly onto a data bus
- Propagation delay 15 ns typical

Connection Diagrams

16-Lead DIP



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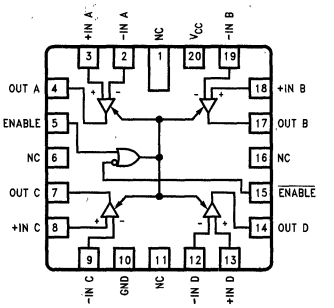
Top View

Order Number DS26F32CJ or DS26F32MJ
See NS Package Number J16A

For Complete Military 883 Specifications, see RETS Datasheet.

Order Number DS26F32ME/883, DS26F32MJ/883 or DS26F32MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



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Function Table (Each Receiver)

Differential Inputs	Enables		Outputs
$V_{ID} = (V_{IN}+) - (V_{IN}-)$	E	$\overline{E}$	OUT
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
X = Immaterial

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
Ceramic DIP −65°C to + 175°C

Operating Temperature Range
DS26F32M −55°C to +125°C
DS26F32C 0°C to +70°C

Lead Temperature
Ceramic DIP (soldering, 60 sec) 300°C

Maximum Power Dissipation* at 25°C
Cavity Package 1500 mW

Supply Voltage 7.0V

*Derate cavity package 10 mW/°C above 25°C.

Common Mode Voltage Range ±25V
Differential Input Voltage ±25V
Enable Voltage 7.0V
Output Sink Current 50 mA

Operating Range

DS26F32C
Temperature 0°C to +70°C
Supply Voltage 4.75V to 5.25V

DS26F32M
Temperature −55°C to +125°C
Supply Voltage 4.5V to 5.5V

Electrical Characteristics Over operating range, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$-7.0V \le V_{CM} \le +7.0V$, $V_O = V_{OL}$ or V_{OH}		−0.2	±0.06	+0.2	V
R_I	Input Resistance	$-15V \le V_{CM} \le +15V$, One Input AC Ground		14	18		kΩ
I_I	Input Current (under Test)	$V_I = +15V$, Other Input $-15V \le V_I \le +15V$				2.3	mA
		$V_I = -15V$, Other Input $-15V \le V_I \le +15V$				−2.8	
V_{OH}	Output Voltage HIGH	V_{CC} = Min, $\Delta V_I = +1.0V$, $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\ \mu A$	0°C to +70°C	2.8	3.4		V
			−55°C to +125°C	2.5	3.4		
V_{OL}	Output Voltage LOW	V_{CC} = Min, $\Delta V_I = -1.0V$, $V_{\overline{ENABLE}} = 0.8V$	I_{OL} = 4.0 mA			0.4	V
			I_{OL} = 8.0 mA			0.45	
V_{IL}	Enable Voltage LOW					0.8	V
V_{IH}	Enable Voltage HIGH			2.0			V
V_{IC}	Enable Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	
I_{IL}	Enable Current LOW	V_I = 0.4V			−0.2	−0.36	mA
I_{IH}	Enable Current HIGH	V_I = 2.7V			0.5	10	μA
I_I	Enable Input High Current	V_I = 5.5V			1.0	50	μA
I_{OS}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 4) $\Delta V_I = +1.0V$		−15	−50	−85	mA
I_{CC}	Supply Current	V_{CC} = Max, All V_I = GND, Outputs Disabled			30	50	mA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5.0V, V_{CM} = 0V			30		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

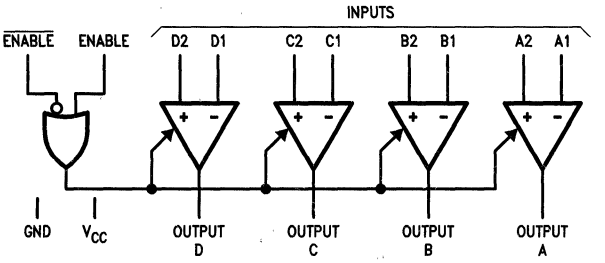
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS26F32M and across the 0°C to +70°C range for the DS26F32C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

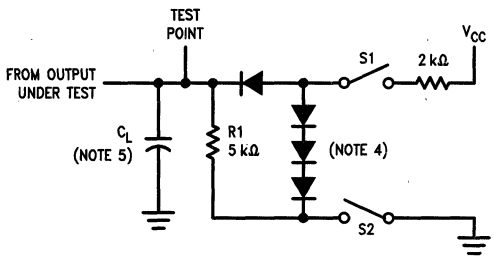
Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Input to Output	*Figures 2, 3*	C_L = 15 pF		15	22	ns
t_{PHL}	Input to Output				15	22	ns
t_{LZ}	Enable to Output	*Figures 2, 4*	C_L = 5 pF		14	18	ns
t_{HZ}	Enable to Output				15	20	ns
t_{ZL}	Enable to Output		C_L = 15 pF		13	18	ns
t_{ZH}	Enable to Output				12	16	ns



TL/F/9615–2

FIGURE 1. Logic Symbol



TL/F/9615–3

FIGURE 2. Load Test Circuit for Three-State Outputs

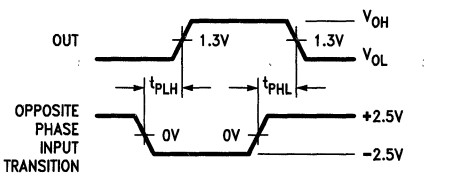


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FIGURE 3. Propagation Delay (Notes 1, 2 and 3)

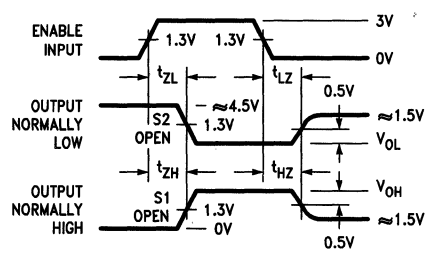

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FIGURE 4. Enable and Disable Times (Notes 1, 2 and 3)

Note 1: Diagram shown for $\overline{\text{ENABLE}}$ Low.

Note 2: S1 and S2 of Load Circuit are closed except where shown.

Note 3: Pulse Generator of all Pulses: Rate ≤ 1.0 MHz, Z_O = 50Ω, t_r ≤ 6.0 ns, t_f ≤ 6.0 ns.

Note 4: All diodes are IN916 or IN3064.

Note 5: C_L includes probe and jig capacitance.

Typical Application

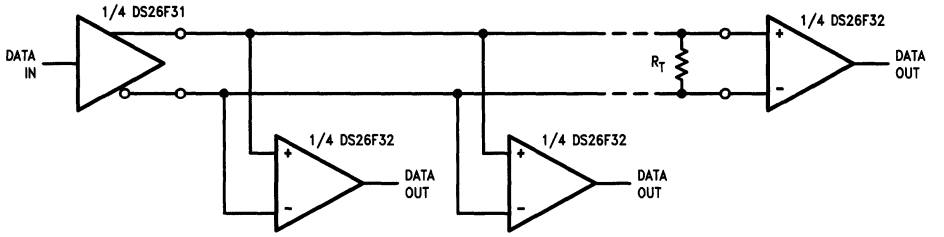

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FIGURE 5

National Semiconductor

DS26LS32C/DS26LS32M/DS26LS32AC/DS26LS33C/ DS26LS33M/DS26LS33AC Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 and DS26LS33A have an input sensitivity of 500 mV over the input voltage range of ±15V.

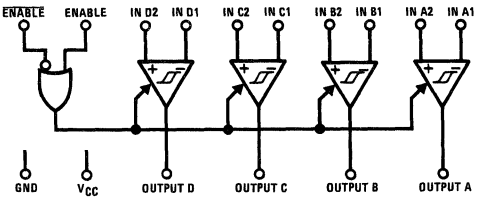
Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commerical operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33 and DS26LS33A
- ±0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ±0.5V sensitivity on the DS26LS33 and DS26LS33A
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33 and DS26LS33A
- Operation from a single 5V supply
- TRI-STATE outputs, with choice of complementary output enables for receiving directly onto a data bus

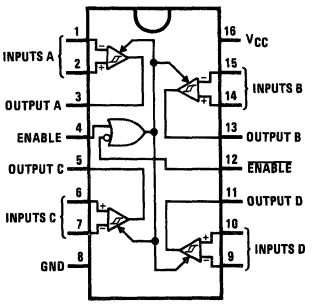
Logic Diagram



TL/F/5255–1

Connection Diagram

Dual-In-Line Package



TL/F/5255–2

Top View

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0

HI-Z = TRI-STATE

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Order Number DS26LS32CM, DS26LS32CN, DS26LS32MJ, DS26LS32ACM, DS26LS32ACN, DS26LS33CN, DS26LS33MJ or DS26LS33ACN
See NS Package Number J16A, M16A or N16A

For Complete Military 883 Specifications, See RETS Data Sheet.

Order Number DS26LS32MJ/883, DS26LS32MW/883, DS26LS33MJ/883, DS26LS33MW/883
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Dip Package	1362 mW
SO Package DS26LS32	1002 mW
DS26LS32A	1051 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C.

Derate SO Package 8.01 mW/°C for DS26LS32
8.41 mW/°C for DS26LS32A

Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	4.75	5.25	V
Temperature, (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	0	+70	°C

Electrical Characteristics over the operating temperature range unless otherwise specified (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	DS26LS32, DS26LS32A, $-7V \le V_{CM} \le +7V$	−0.2	±0.07	0.2	V
			DS26LS33, DS26LS33A, $-15V \le V_{CM} + 15V$	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One Input AC GND)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = 15V$, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
		$V_{IN} = -15V$, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = MIN, ΔV_{IN} = 1V, $V_{\overline{ENABLE}}$ = 0.8V, $I_{OH} = -440\ \mu A$	Commercial	2.7	4.2		V
			Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, $\Delta V_{IN} = -1V$, $V_{\overline{ENABLE}}$ = 0.8V	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18$ mA				−1.5	V
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	V_O = 2.4V			20	μA
			V_O = 0.4V			−20	μA
I_{IL}	Enable Low Current	V_{IN} = 0.4V				−0.36	mA
I_{IH}	Enable High Current	V_{IN} = 2.7V				20	μA
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max, ΔV_{IN} = 1V		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled	DS26LS32, DS26LS32A		52	70	mA
			DS26LS33, DS26LS33A		57	80	mA
I_I	Input High Current	V_{IN} = 5.5V				100	μA
V_{HYST}	Input Hysteresis	T_A = 25°C, V_{CC} = 5V, V_{CM} = 0V	DS26LS32, DS26S32A		100		mV
			DS26LS33, DS26LS33A		200		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, all currents out of device pins are shown as negative, all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

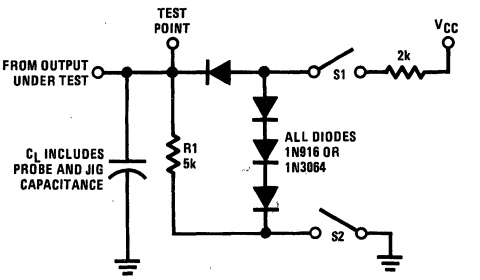
Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Input to Output	C_L = 15 pF		17	25		23	35	ns
t_{PHL}				17	25		23	35	ns
t_{LZ}	ENABLE to Output	C_L = 5 pF		20	30		15	30	ns
t_{HZ}				15	22		20	25	ns
t_{ZL}	ENABLE to Output	C_L = 15 pF		15	22		14	22	ns
t_{ZH}				15	22		15	22	ns

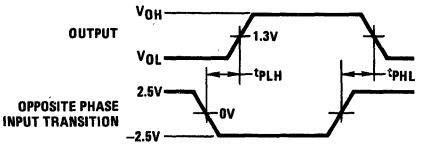
AC Test Circuit and Switching Time Waveforms

Load Test Circuit for TRI-STATE Outputs



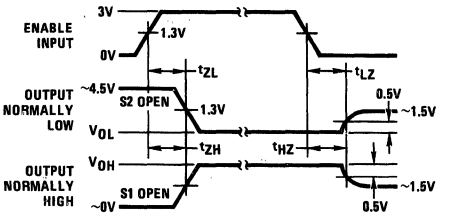
TL/F/5255–3

Propagation Delay (Notes 1 and 3)



TL/F/5255–4

Enable and Disable Times (Notes 2 and 3)



TL/F/5255–5

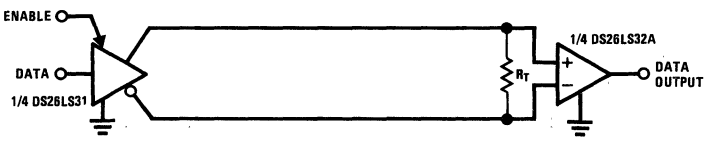
Note 1: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 2: S1 and S2 of load circuit are closed except where shown.

Note 3: Pulse generator for all pulses: Rate = 1.0 MHz; Z_O = 50Ω; $t_r \leq 6$ ns; $t_f \leq 6.0$ ns.

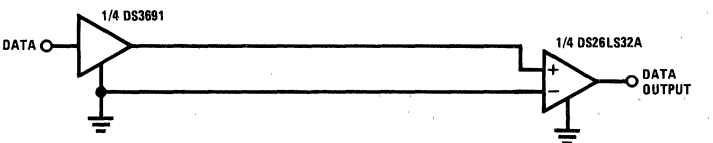
Typical Applications

Two-Wire Balanced Interface—RS-422



TL/F/5255–6

Single Wire with Driver Ground Reference—RS-423



TL/F/5255–7

National Semiconductor

DS34C86T
Quad CMOS Differential Line Receiver

General Description

The DS34C86T is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS34C86T has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

The DS34C86T features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

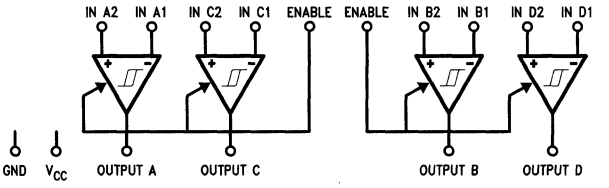
Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86T is pin compatible with the DS3486.

Features

- CMOS design for low power
- ±0.2V sensitivity over the input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for system bus compatibility
- Available in surface mount
- Open input Failsafe feature, output high for open input

3

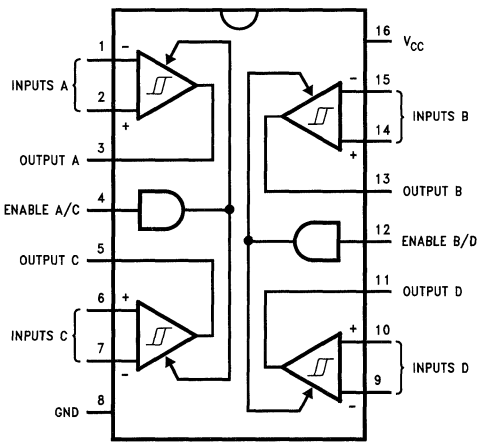
Logic Diagram



TL/F/8699–1

Connection Diagram

Dual-In-Line Package



TL/F/8699–2

Top View

Order Number DS34C86TJ, DS34C86TM, and DS34C86TN
See NS Package Number J16A, M16A and N16E

Truth Table

Enable	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	H
H	$V_{ID} \leq V_{TH}$ (Min)	L
H	Open*	H

*Open, not terminated
Z = TRI-STATE

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	260°C
Maximum Power Dissipation at 25°C (Note 5)	
Ceramic "J" Package	2308 mW
Plastic "N" Package	1645 mW
SOIC Package	1190 mW
Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 4)

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Minimum Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−200	35	+200	mV
R_{IN}	Input Resistance	$V_{IN} = -7V, +7V$ (Other Input = GND)	5.0	6.8	10	kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = +10V$, Other Input = GND $V_{IN} = -10V$, Other Input = GND		+1.1 −2.0	+1.5 −2.5	mA mA
V_{OH}	Minimum High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)} = +1V$ $I_{OUT} = -6.0$ mA	3.8	4.2		V
V_{OL}	Maximum Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)} = -1V$ I_{OUT} = 6.0 mA		0.2	0.3	V
V_{IH}	Minimum Enable High Input Level Voltage		2.0			V
V_{IL}	Maximum Enable Low Input Level Voltage				0.8	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, TRI-STATE Control = V_{IL}		±0.5	±5.0	μA
I_I	Maximum Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)} = +1V$		16	23	mA
V_{HYST}	Input Hysteresis	V_{CM} = 0V		60		mV

AC Electrical Characteristics V_{CC} = 5V ±10% (Note 3) (*Figures 1, 2, and 3*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		19	30	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	18	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	21	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Unless otherwise specified, Min/Max limits apply across the operating temperature range.

All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: ESD Rating; HBM (1.5kΩ, 100 pF)
Inputs ≥ 2000V
All other pins ≥ 1000V
EIAJ (0Ω, 200 pF) ≥ 350V

Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.16 mW/°C, J Package 15.38 mW/°C and M Package 9.52 mW/°C.

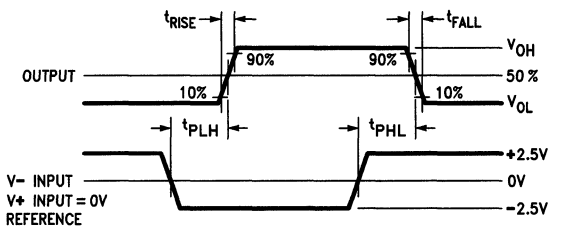
Comparison Table of Switching Characteristics into "LS-Type" Load

V_{CC} = 5V, T_A = 25°C (*Figures 4* and *5*) (Note 6)

Symbol	Parameter	DS34C86		DS3486		Units
		Typ	Max	Typ	Max	
$t_{PHL(D)}$	Propagation Delay Time Output High to Low	17		19		ns
$t_{PLH(D)}$	Propagation Delay Time Output Low to High	19		19		ns
t_{PLZ}	Output Low to TRI-STATE	13		23		ns
t_{PHZ}	Output High to TRI-STATE	12		25		ns
t_{PZH}	Output TRI-STATE to High	13		18		ns
t_{PZL}	Output TRI-STATE to Low	13		20		ns

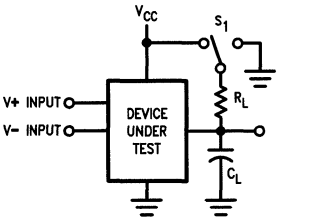
Note 6: This Table is provided for comparison purposes only. The values in this table for the DS34C86 reflect the performance of the device but are not tested or guaranteed.

Test and Switching Waveforms



TL/F/8699–3

FIGURE 1. Propagation Delays



TL/F/8699–4

C_L Includes load and test jig capacitance.
S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

FIGURE 2. Test Circuit for TRI-STATE Output Tests

Test and Switching Waveforms (Continued)

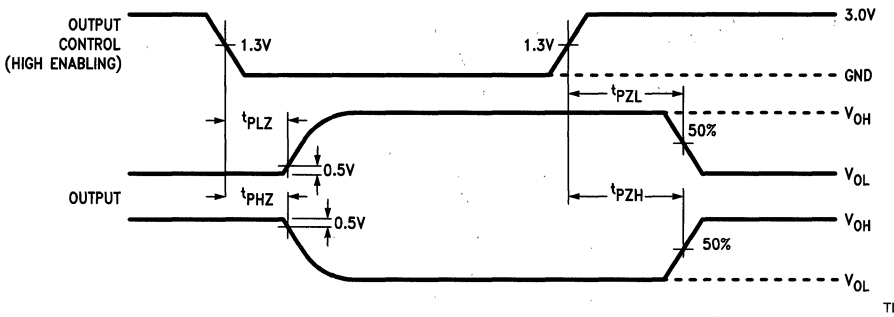
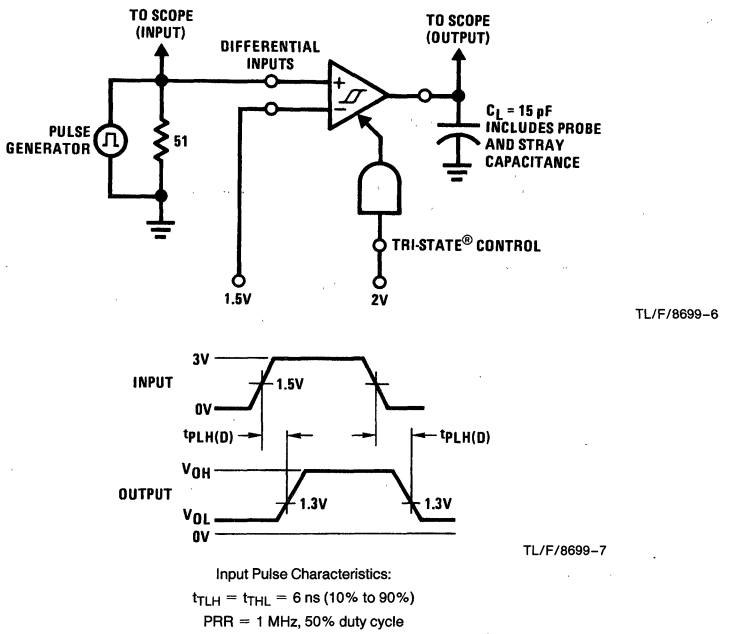


FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

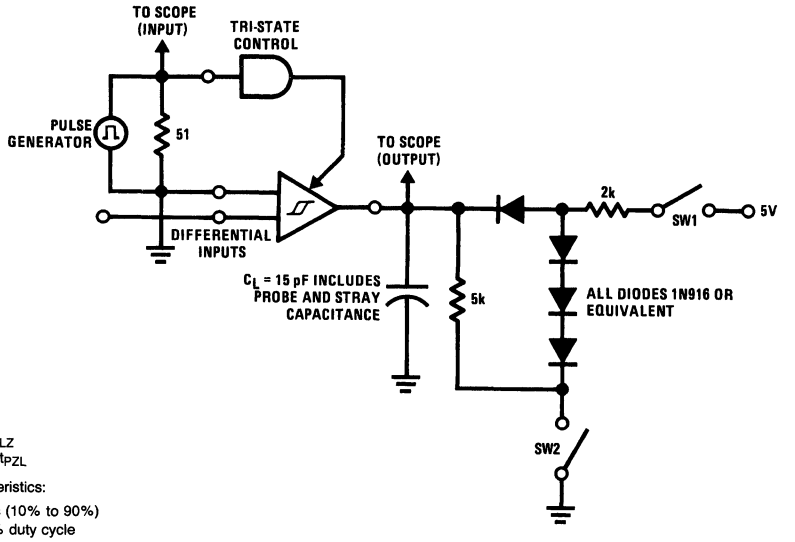
AC Test Circuits and Switching Time Waveforms



Input Pulse Characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 4. Propagation Delay Differential Input to Output for "LS-Type" Load

AC Test Circuits and Switching Time Waveforms (Continued)

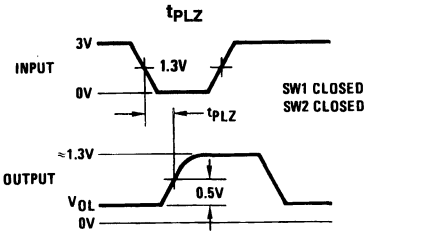


1.5V for t_{PHZ} and t_{PLZ}
−1.5V for t_{PLZ} and t_{PZL}

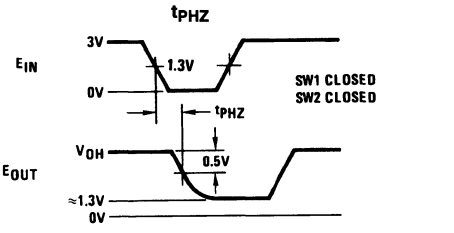
Input Pulse Characteristics:

$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

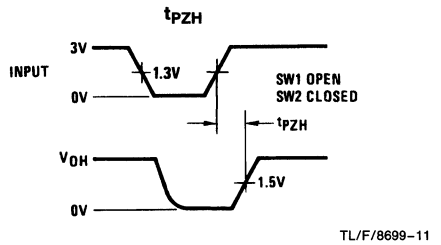
TL/F/8699–8



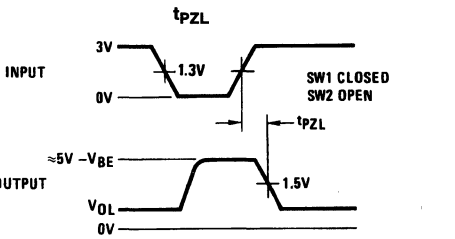
TL/F/8699–9



TL/F/8699–10



TL/F/8699–11



TL/F/8699–12

FIGURE 5. Propagation Delay TRI-STATE Control Unit to Output for "LS-Type" Load

National Semiconductor

ADVANCE INFORMATION

DS34LV86T
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS34LV86T is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and CCITT V.11. The CMOS DS34LV86T features low I_{CC} of X mA which makes it ideal for battery powered and power conscious applications.

The TRI-STATE® enables, EN, allow the device to be disabled when not in use to minimize power consumption. The dual enable scheme allows for flexibility in turning receivers on and off.

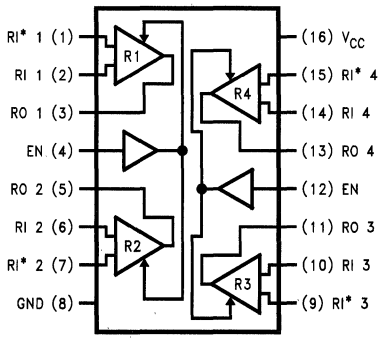
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±7V. The receiver outputs (RO) are compatible with TTL and CMOS levels.

Features

- Low power CMOS design
- Meets TIA/EIA-422-B (RS-422) and CCITT V.11 recommendation
- Receiver OPEN input failsafe feature
- Guaranteed AC parameter:
  - — Maximum receiver skew TBD
  - — Transition time TBD
- Pin compatible with DS34C86T
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package
DS34LV86T



TL/F/12644–1

Order Number DS34LV86TM or DS34LV86TN
See NS Package Number M16A or N16E

Truth Table

Enables		Inputs	Outputs
EN	**$\overline{EN}$**	**RI–RI***	**RO**
L	H	X	Z
H	L	$V_{ID} \geq V_{TH\ (Max)}$	H
H	H	$V_{ID} \leq V_{TH\ (Min)}$	L
L	L	Open	H

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

National Semiconductor

DS34F86/DS35F86
RS-422/RS-423 Quad Line Receiver with TRI-STATE® Outputs

General Description

The DS34F86/DS35F86 RS-422/3 Quad Receiver features four independent receivers, which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. A PNP device buffers each output control lead to assure minimum loading for either logic one or logic zero inputs. In addition each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

The DS34F86/DS35F86 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F86/DS35F86 features lower power, extended temperature range, and improved specifications.

The DS34F86/DS35F86 offers optimum performance when used with the DS34F87/DS35F87 Quad Line Driver.

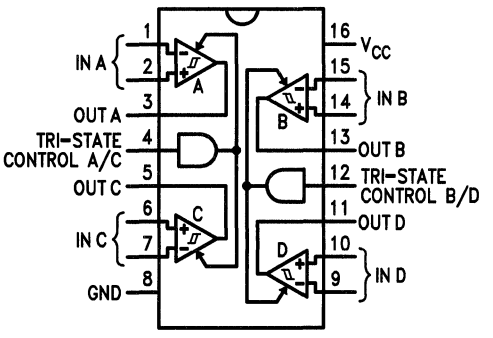
Features

- Military temperature range
- TRI-STATE outputs
- Fast propagation times (15 ns typical)
- TTL compatible
- 5.0V supply
- Lead compatible and interchangeable with MC3486 and DS3486

3

Connection Diagram

16-Lead DIP



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Top View

Order Number DS34F86J or DS35F86J
See NS Package Number J16A

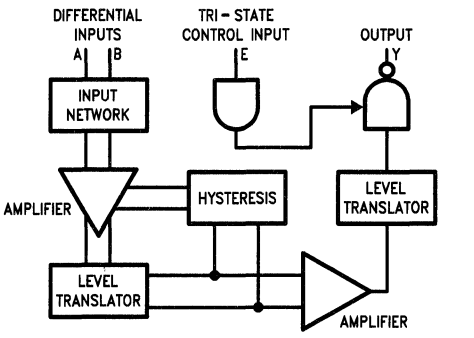

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FIGURE 1. Block Diagram

Function Table (Each Receiver)

Differential Inputs $V_{ID} = (V_{IN}+) - (V_{IN}-)$	Enable E	Output OUT
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

H = High Level
L = Low Level
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Operating Temperature Range	
DS35F86	−55°C to +125°C
DS34F86	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW
Supply Voltage	8.0V
Input Voltage	8.0V
Input Common Mode Voltage	±15V
Input Differential Voltage	±25V

*Derate cavity package 10 mW/°C above 25°C.

Operating Conditions

DS34F86	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS35F86	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V
Input Common Mode Voltage Range	−7.0V to +7.0V
Input Differential Voltage Range	6V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2			V
V_{IL}	Input Voltage LOW					0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage (Note 6)	$-7V \le V_{CM} \le 7V$, $V_{IH} = 2V$	$V_O = V_{OH}$			0.2	V
			$V_O = V_{OL}$	−0.2			
I_{IB}	Input Bias Current	V_{CC} = 0V or 5.25V, Other inputs at 0V	$V_I = -10V$			−3.25	mA
			$V_I = -3V$			−1.50	
			$V_I = +3V$			+1.50	
			$V_I = +10V$			+3.25	
V_{OH}	Output Voltage HIGH (Note 5)	$-7V \le V_{CM} \le 7V$, $V_{IH} = 2V$, $I_O = -0.4$ mA, $V_{ID} = 0.4V$	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$-7V \le V_{CM} \le 7V$, $V_{IH} = 2V$	$I_O = 8$ mA, $V_{ID} = 0.4V$			0.5	V
I_{OZ}	Off State (High Impedance) Output Current	$V_{I(D)} = +3V$, $V_{IL} = 0.8V$, $V_O = 0.5V$				−10	μA
		$V_{I(D)} = -3V$, $V_{IL} = 0.8V$, $V_O = 2.7V$				10	
I_{OS}	Output Short Circuit Current (Note 4)	$V_{I(D)} = +3V$, $V_{IH} = 2V$, $V_O = 0V$		−15		−100	mA
I_{IL}	Input Current LOW (TRI-STATE Control)	$V_{IL} = 0.5V$				−100	μA
I_{IH}	Input Current HIGH (TRI-STATE Control)		$V_{IH} = 2.7V$			20	μA
			$V_{IH} = 5.25V$			40	
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IC} = -10$ mA				−1.5	V
I_{CC}	Supply Current	$V_{IL} = 0V$				50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS35F86 and across the 0°C to +70°C range for the DS34F86. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA RS-422/3 for exact conditions. Input balance and V_{OH}/V_{OL} levels are tested simultaneously for worse case.

Note 6: Differential input threshold voltage and guaranteed output levels are tested simultaneously for worst case.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (Figures 2 & 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
$t_{PHL(D)}$	Propagation Delay Time Differential Inputs to Outputs	*Figure 2*		15	22	ns
$t_{PLH(D)}$				15	22	ns
t_{LZ}	Propagation Delay Time Controls to Outputs	C_L = 5 pF *Figure 3*		14	18	ns
t_{HZ}				15	20	ns
t_{ZH}		*Figure 3*		12	16	ns
t_{ZL}				13	18	ns

Parameter Measurement Information

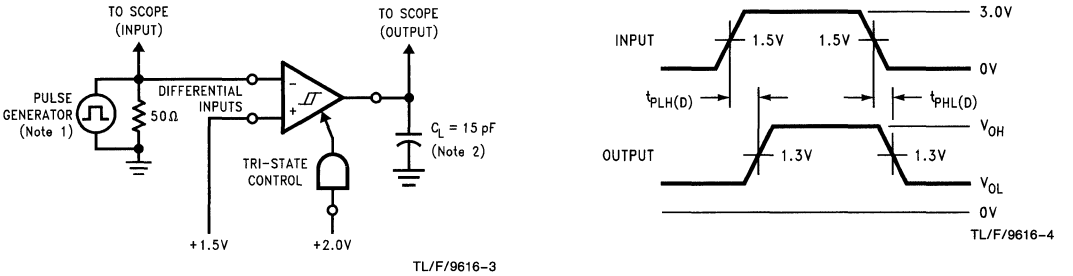

FIGURE 2. Propagation Delay Differential Input to Output

Parameter Measurement Information (Continued)

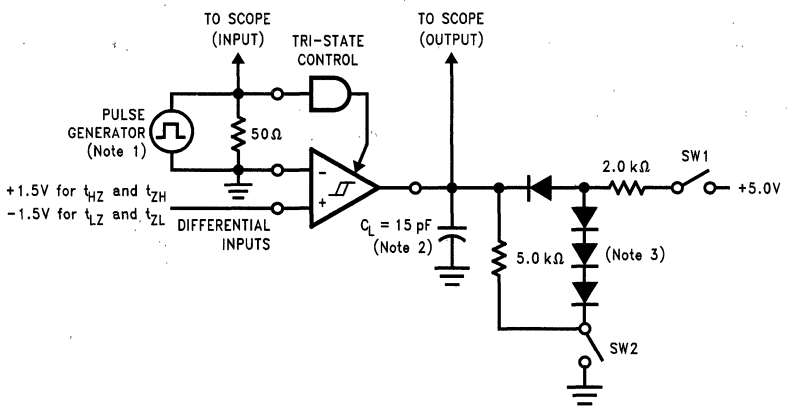

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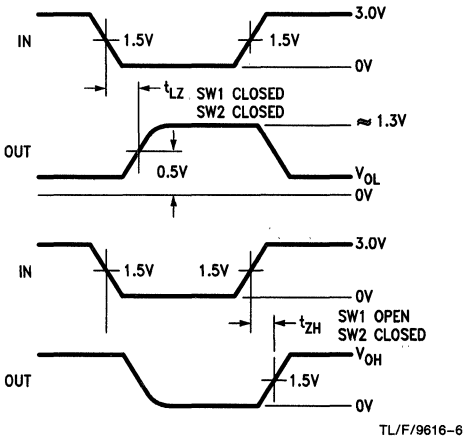
FIGURE 3. Propagation Delay TRI-STATE Control Input to Output



TL/F/9616–6

FIGURE 3a. t_{LZ}, t_{ZH}

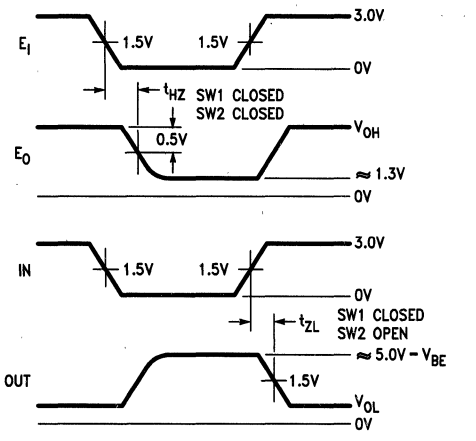


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FIGURE 3b. t_{HZ}, t_{ZL}

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%), Z_O = 50Ω.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are IN916 or equivalent.

National Semiconductor

DS3486 Quad RS-422, RS-423 Line Receiver

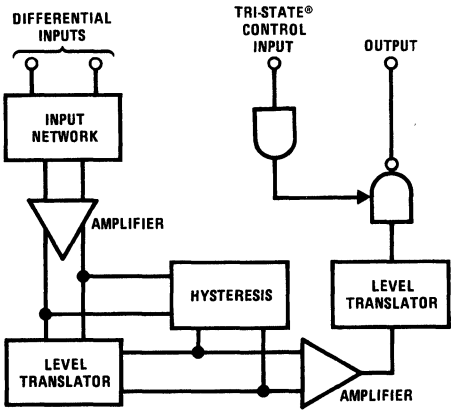
General Description

National's quad RS-422, RS-423 receiver features four independent receivers which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

Features

- Four independent receivers
- TRI-STATE outputs
- Internal hysteresis −140 mV (typ)
- Fast propagation times −19 ns (typ)
- TTL compatible outputs
- 5V supply
- Pin compatible and interchangeable with MC3486

Block and Connection Diagrams



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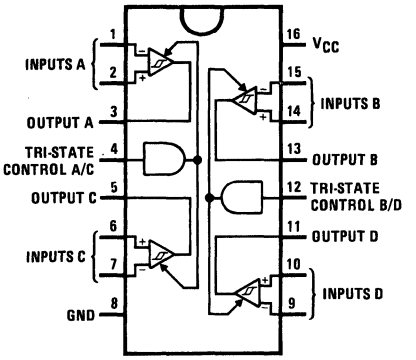
Dual-In-Line Package



TL/F/5779–2

Top View

Order Number DS3486J, DS3486M or DS3486N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage, V_{CC}	8V
Input Common-Mode Voltage, V_{ICM}	±25V
Input Differential Voltage, V_{ID}	±25V
TRI-STATE Control Input Voltage, V_I	8V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433mW
Molded Dip Package	1362 mW
SO Package	1002 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate Dip molded package 10.2 mW/°C above 25°C. Derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage Range, V_{ICR}	−7.0	7.0	V

Electrical Characteristics

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5V and V_{IC} = 0V. See Note 2.)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage—High Logic State (TRI-STATE Control)			2.0			V
V_{IL}	Input Voltage—Low Logic State (TRI-STATE Control)					0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage		$-7V \le V_{IC} \le 7V$, V_{IH} TRI-STATE = 2V $I_O = -0.4$ mA, $V_{OH} \ge 2.7V$		0.070	0.2	V
			I_O = 8 mA, $V_{OL} \ge 0.5V$		0.070	−0.2	V
$I_{IB\ (D)}$	Input Bias Current		V_{CC} = 0V or 5.25V, Other Inputs at 0V				
			$V_I = -10V$			−3.25	mA
			$V_I = -3V$			−1.50	mA
			V_I = 3V			1.50	mA
			V_I = 10V			3.25	mA
	Input Balance		$-7V \le V_{IC} \le 7V$, $V_{IH(3C)}$ = 2V, (Note 4)				
		V_{OH}	$I_O = -0.4$ mA, V_{ID} = 0.4V	2.7			V
		V_{OL}	I_O = 8 mA, $V_{ID} = -0.4V$			0.5	V
I_{OZ}	Output TRI-STATE Leakage Current		$V_{I(D)}$ = 3V, V_{IL} = 0.8V, V_{OL} = 0.5V			−40	μA
			$V_{I(D)} = -3V$, V_{IL} = 0.8V, V_{OH} = 2.7V			40	μA
I_{OS}	Output Short-Circuit Current		$V_{I(D)}$ = 3V, V_{IH} TRI-STATE = 2V, V_O = 0V, (Note 3)	−15		−100	mA
I_{IL}	Input Current—Low Logic State (TRI-STATE Control)		V_{IL} = 0.5V			−100	μA
I_{IH}	Input Current—High Logic State (TRI-STATE Control)		V_{IH} = 2.7V			20	μA
			V_{IH} = 5.25V			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)		$I_{IN} = -10$ mA			−1.5	V
I_{CC}	Power Supply Current		All Inputs V_{IL} = 0V			85	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

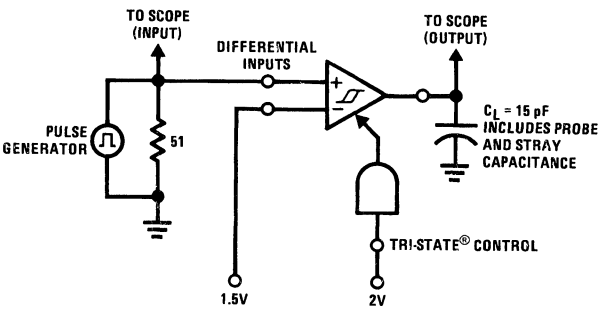
Note 3: Only one output at a time should be shorted.

Note 4: Refer to EIA RS-422/3 for exact conditions.

Switching Characteristics (Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

Symbol	Parameter	Min	Typ	Max	Units
$t_{PHL(D)}$	Propagation Delay Time—Differential Inputs to Output Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
t_{PLZ}	TRI-STATE Control to Output Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

AC Test Circuits and Switching Time Waveforms



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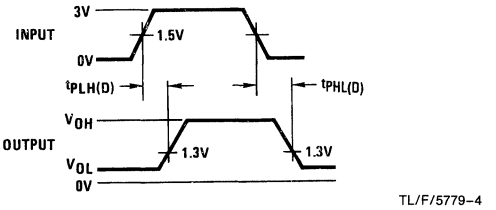
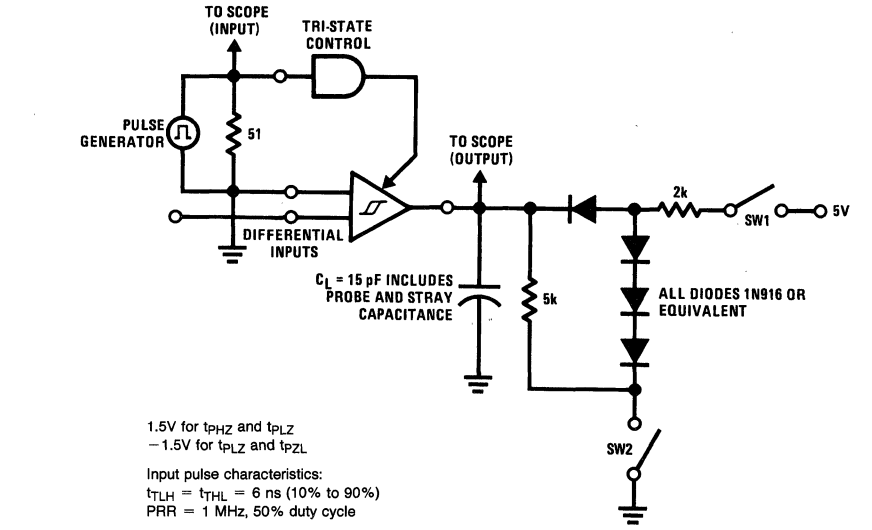


TL/F/5779–4

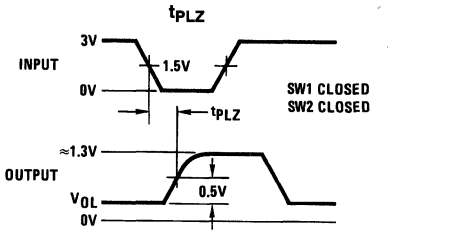
Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 1. Propagation Delay Differential Input to Output

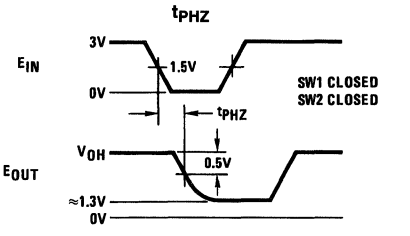
AC Test and Switching Time Waveforms (Continued)



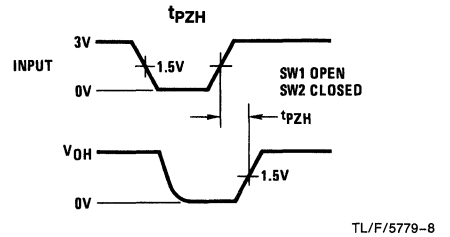
TL/F/5779–5



TL/F/5779–6



TL/F/5779–7



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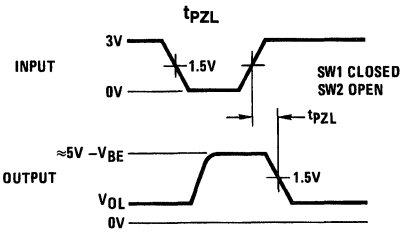

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FIGURE 2. Propagation Delay TRI-STATE Control Input to Output

National Semiconductor

DS34C87T CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS34C87T is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87T accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has separate enable circuitry for each pair of the four drivers. The DS34C87T is pin compatible to the DS3487T.

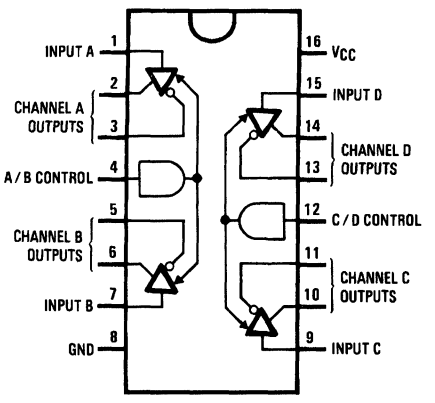
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount

Connection and Logic Diagrams

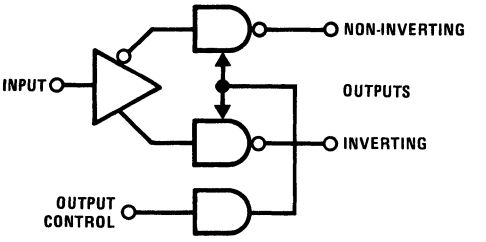
Dual-In-Line Package



TL/F/8576–1

Top View

Order Number DS34C87TJ, DS34C87TM or DS34C87TN
See NS Package Number J16A, M16A or N16E



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Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±150 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Power Dissipation (P_D) @ 25°C (Note 3)	
Ceramic "J" Package	2419 mW
Plastic "N" Package	1736 mW
SOIC Package	1226 mW
Lead Temperature (T_L) (Soldering 4 sec)	260°C

This device does not meet 2000V ESD rating. (Note 12)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A) DS34C87T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA	2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 48 mA		0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100 Ω (Note 5)	2.0	3.1		V
$\lvert V_T\rvert - \lvert \overline{V}_T\rvert$	Difference In Differential Output	R_L = 100 Ω (Note 5)			0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100 Ω (Note 5)		2.0	3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	R_L = 100 Ω (Note 5)			0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}			±1.0	μA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 μA, V_{IN} = V_{CC} or GND V_{IN} = 2.4V or 0.5V (Note 6)		200 0.8	500 2.0	μA mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, Control = V_{IL}		±0.5	±5.0	μA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Notes 5, 7)	−30		−150	mA
I_{OFF}	Power Off Output Leakage Current	V_{CC} = 0V (Note 5); V_{OUT} = 6V V_{CC} = 0V (Note 5); V_{OUT} = −0.25V			100 −100	μA μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate N Package 13.89 mW/°C, J Package 16.13 mW/°C, and M Package 9.80 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See EIA Specification RS-422 for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (*Figures 1, 2, 3,* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open		6	11	ns
Skew	(Note 8)	S1 Open		0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time (Note 9)	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time (Note 9)	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			6		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Note 9: Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Comparison Table of Switching Characteristics into "LS-Type" Load

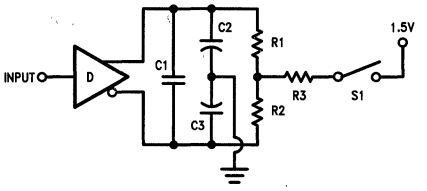
V_{CC} = 5V, T_A = +25°C, t_r ≤ 6 ns, t_f ≤ 6 ns (*Figures 4, 5, 6, 7, 8* and *9*) (Note 11)

Symbol	Parameter	Conditions	DS34C87		DS3487		Units
			Typ	Max	Typ	Max	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output		6	10	10	15	ns
Skew	(Note 8)		1.5	2.0			ns
t_{THL}, t_{TLH}	Differential Output Rise and Fall Times		4	7	10	15	ns
t_{PHZ}	Output Disable Time (Note 9)	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	8	11	17	25	ns
t_{PLZ}	Output Disable Time (Note 9)	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Closed	7	10	15	25	ns
t_{PZH}	Output Enable Time	C_L = 50 pF, R_L = ∞, S1 Open, S2 Closed	11	19	11	25	ns
t_{PZL}	Output Enable Time	C_L = 50 pF, R_L = 200Ω, S1 Closed, S2 Open	14	21	15	25	ns

Note 11: This table is provided for comparison purposes only. The values in this table for the DS34C87 reflect the performance of the device but are not tested or guaranteed.

Note 12: ESD Rating: HBM (1.5 kΩ, 100 pF)
Inputs ≥ 1500V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF)
All Pins ≥ 350V

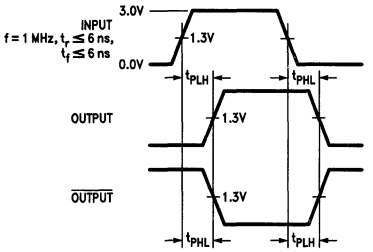
AC Test Circuit and Switching Time Waveforms



TL/F/8576–3

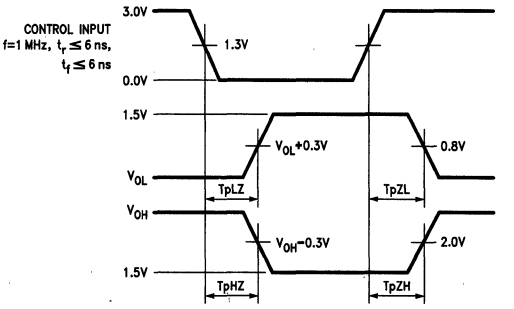
Note: C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

FIGURE 1. AC Test Circuit



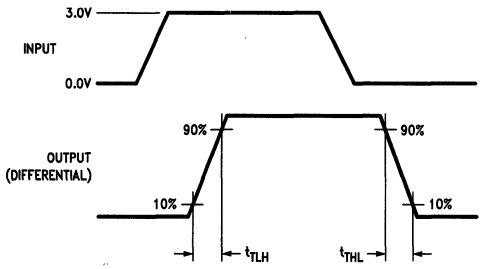
TL/F/8576–4

FIGURE 2. Propagation Delays



TL/F/8576–5

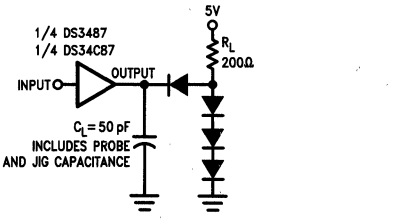
FIGURE 3. Enable and Disable Times



TL/F/8576–7

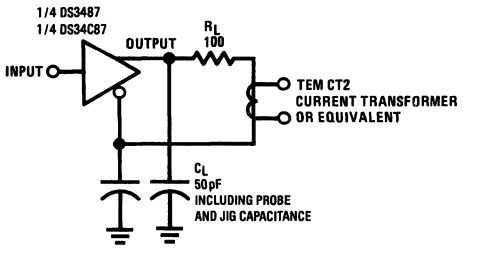
Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times



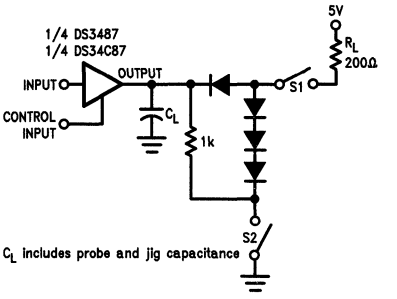
TL/F/8576–8

FIGURE 5. Propagation Delays Test Circuit for "LS-Type" Load



TL/F/8576–6

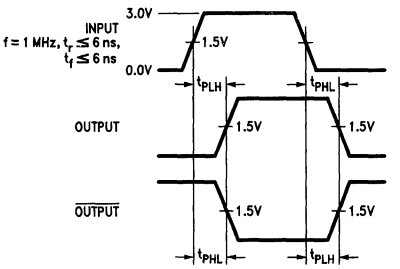
FIGURE 6. Differential Rise and Fall Times Test Circuit for "LS-Type" Load



TL/F/8576–9

FIGURE 7. Load Enable and Disable Times Test Circuit for "LS-Type" Load

AC Test Circuit and Switching Time Waveforms (Continued)



TL/F/8576–10

FIGURE 8. Load Propagation Delays for "LS-Type" Load

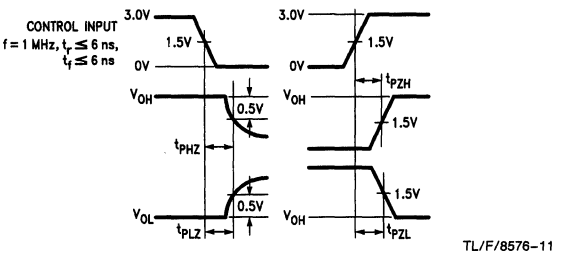


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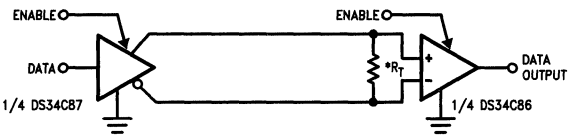
FIGURE 9. Load Enable and Disable Times for "LS-Type" Load

Typical Applications

Two-Wire Balanced System, RS-422



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*R_T is optional although highly recommended to reduce reflection.

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ADVANCE INFORMATION

DS34LV87T
Enhanced CMOS Quad Differential Line Driver

General Description

The DS34LV87T is a high speed quad differential CMOS driver that is compatible with both TIA/EIA-422-B and CCITT V.11 devices. The CMOS DS34LV87T features low I_{CC} of X mA which makes it ideal for battery powered and power conscious applications.

The TRI-STATE® enable, EN, allow the device to be disabled when the device is not in use to minimize power. The dual enable scheme allows for flexibility in turning the devices on or off.

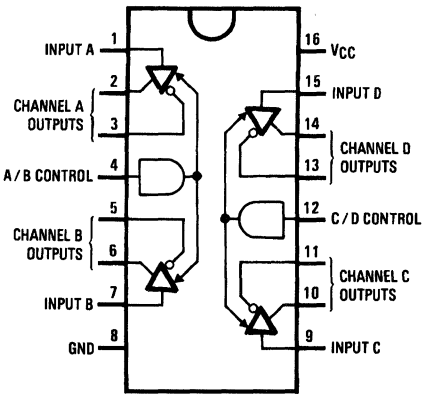
Protection diodes protect all the driver inputs against electrostatic discharge. The driver inputs (DI) are compatible with TTL and CMOS levels.

Features

- Low power design
  — $I_{CC} \leq 500\ \mu A$ max
- Compatible with TIA/EIA-422-B (RS-422) and CCITT V.11 recommendation
- Guaranteed AC parameter:
  — Maximum driver skew TBD
  — Transition time TBD
- Pin compatible with DS34C87T
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package
DS34LV87T



TL/F/12645–2

Order Number DS34LV87TM or DS34LV87TN
See NS Package Number M16A or N16A

Truth Table

Enables		Input	Outputs	
EN	**$\overline{EN}$**	**DI**	**DO**	**$\overline{DO}$**
L	H	X	Z	Z
H	L	H	H	L
H	H	L	L	H
L	L			

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

National Semiconductor

DS34F87/DS35F87
RS-422 Quad Line Driver with TRI-STATE® Outputs

General Description

The DS34F87/DS35F87 RS-422 Quad Line Driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltages digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control lead reaches a logic zero condition. All input leads are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power-up and power-down.

The DS34F87/DS35F87 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS34F87/DS35F87 features lower power, extended temperature range, and improved specifications.

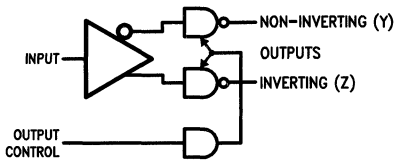
The DS34F87/DS35F87 offers optimum performance when used with the DS34F86/DS35F86 Quad Line Receiver.

Features

- Military temperature range
- Four independent drivers
- TRI-STATE outputs
- PNP high impedance inputs
- Fast propagation time
- TTL compatible
- 5.0V supply
- Output rise and falls times less than 15 ns
- Lead compatible and interchangeable with MC3487 and DS3487

3

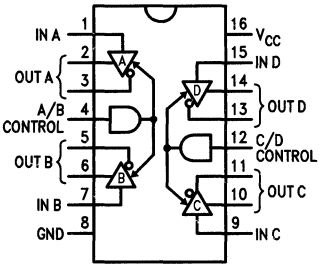
Block and Connection Diagrams



TL/F/9618–2

FIGURE 1

16-Lead DIP



TL/F/9618–1

Top View

Order Number DS34F87J, DS34F87N or DS35F87J
See NS Package Number J16A or N16A

Function Table (Each Driver)

Input	Enable	Output	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Supply Voltage	8.0V
Input Voltage	5.5V

Maximum Power Dissipation* at 25°C	
Cavity Package	1500 mW

*Derate cavity package 10 mW/°C above 25°C.

Operating Range

DS34F87	
Temperature	0°C to +70°C
Supply Voltage	4.75V to 5.25V
DS35F87	
Temperature	−55°C to +125°C
Supply Voltage	4.5V to 5.5V

Electrical Characteristics over operating range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Voltage LOW				0.8	V
V_{IH}	Input Voltage HIGH		2.0			V
I_{IL}	Input Current LOW	V_{IL} = 0.5V			−200	μA
I_{IH}	Input Current HIGH	V_{IH} = 2.7V			+50	μA
		V_{IH} = 5.5V			+100	
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
V_{OL}	Output Voltage LOW	I_{OL} = 48 mA			0.5	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA	2.5			V
I_{OS}	Output Short Circuit Current (Note 4)	V_{IH} = 2.0V	−40		−140	mA
I_{OZ}	Output Leakage Current Hi-Z State	V_{IL} = 0.5V, V_{IL} (z) = 0.8V			±100	μA
		V_{IH} = 2.7V, V_{IL} (z) = 0.8V			±100	
$I_{OL(off)}$	Output Leakage Current Power Off	V_{OH} = 6.0V, V_{CC} = 0V			+100	μA
		V_{OL} = −0.25V, V_{CC} = 0V			−100	
V_{OS}-$\overline{V}_{OS}$	Output Offset Voltage Difference (Note 5)				±0.4	V
V_{OD}	Output Differential Voltage (Note 5)		2.0			V
ΔV_{OD}	Output Differential Voltage Change				±0.4	V
I_{CCX}	Supply Current	Control Leads Gnd			50	mA
I_{CC}		Control Leads 2.0V			40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS35F87 and across the 0°C to +70°C range for the DS34F87. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA RS-422/3 for exact conditions.

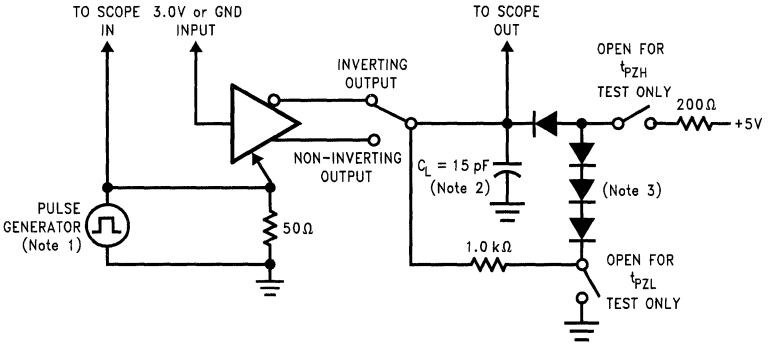
Switching Characteristics V_{CC} = 5.0 V, T_A = 25°C (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Times	High to Low Input			20	ns
t_{PLH}		Low to High Input			15	ns
t_{THL}	Output Transition Times—Differential	High to Low Input			15	ns
t_{TLH}		Low to High Input			15	ns
$t_{PHZ(E)}$	Propagation Delay Control to Output	R_L = 200, C_L = 50 pF			35	ns
$t_{PLZ(E)}$		R_L = 200, C_L = 50 pF			35	ns
$t_{PZH(E)}$		R_L = ∞, C_L = 50 pF			35	ns
$t_{PZL(E)}$		R_L = 200, C_L = 50 pF			35	ns
SKEW	Output to Output	Note 2			4.5	ns

Note 1: C_L = 50 pF, V_I = 1.5V to V_O = 1.5V, V_{PULSE} = 0V to +3.0V.

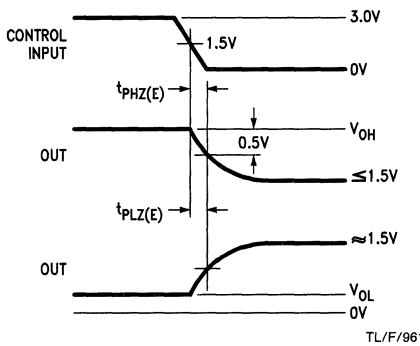
Note 2: Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

Parameter Measurement Information



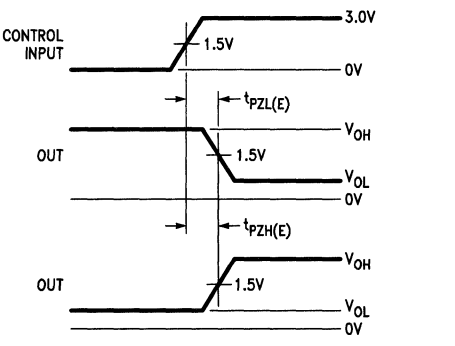
TL/F/9618-3

FIGURE 2. TRI-STATE Enable Test Circuit and Waveforms



TL/F/9618-4

FIGURE 2a



TL/F/9618-5

FIGURE 2b

Parameter Measurement Information (Continued)

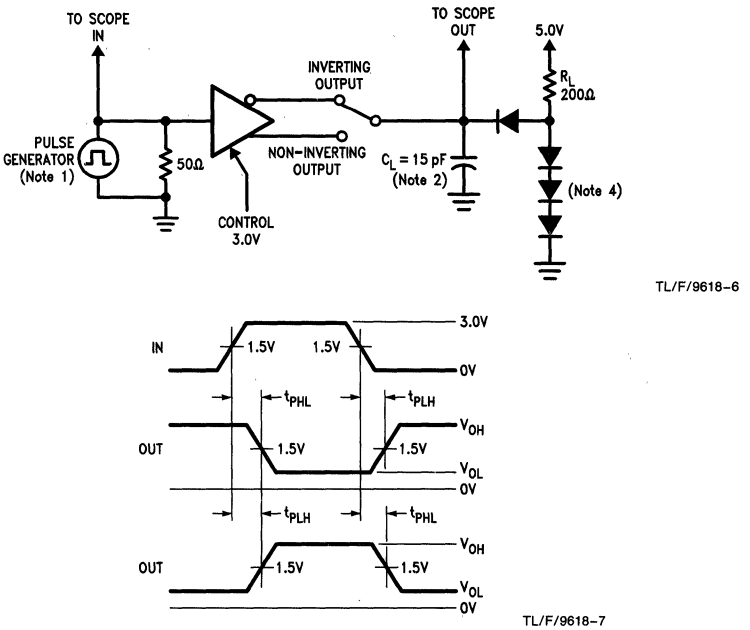


FIGURE 3. Propagation Delay Times Input to Output Waveforms and Test Circuit

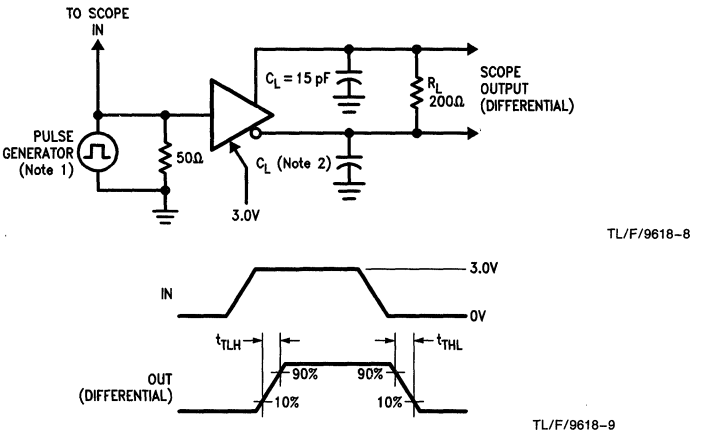


FIGURE 4. Output Transition Times Circuit and Waveforms

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_{TLH} = t_{THL} \leq 5.0$ ns (10% to 90%), $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: All diodes are IN3064 or equivalent.

Note 4: All diodes are IN914 or equivalent.

National Semiconductor

DS3487 Quad TRI-STATE® Line Driver

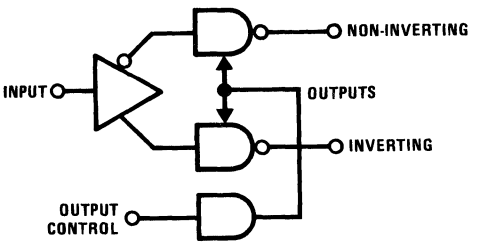
General Description

National's quad RS-422 driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs.

Features

- Four independent drivers
- TRI-STATE outputs
- Fast propagation times (typ 10 ns)
- TTL compatible
- 5V supply
- Output rise and fall times less than 15 ns
- Pin compatible with DS8924 and MC3487

Block and Connection Diagrams



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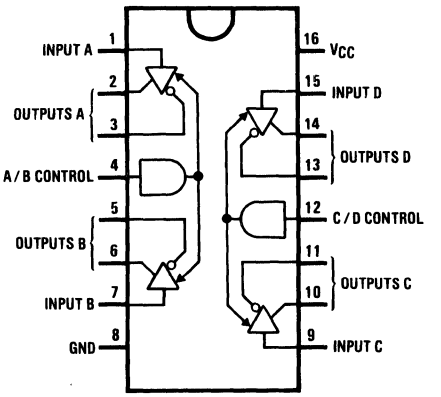
Dual-In-Line Package



TL/F/5780–2

Top View

Order Number DS3487M or DS3487N
See NS Package Number M16A or N16A

Truth Table

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded DIP Package	1476 mW
SO Package	1051 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate DIP molded package 11.9 mW/°C above 25°C. Derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3487	0	+70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0V	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\lvert V_{OS}-\overline{V}_{OS}\rvert$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\lvert V_T\rvert-\lvert\overline{V}_T\rvert$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

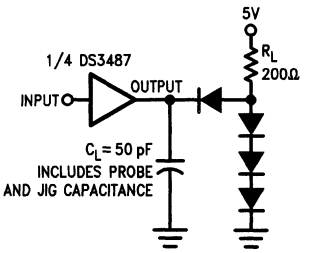
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive, all currents out of device pins as negative. All voltages are referenced to ground unless otherwise specified.

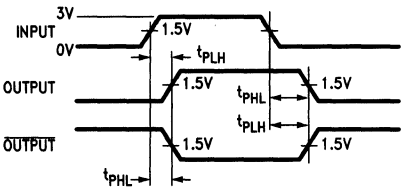
Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

AC Test Circuits and Switching Time Waveforms



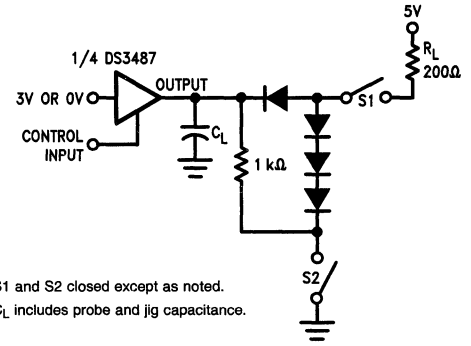
TL/F/5780-3



TL/F/5780-4

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

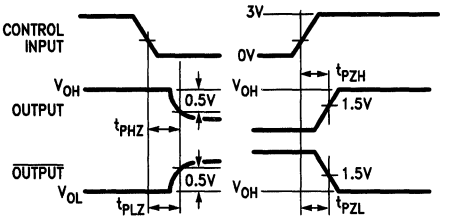
FIGURE 1. Propagation Delays



S1 and S2 closed except as noted.

C_L includes probe and jig capacitance.

TL/F/5780-5



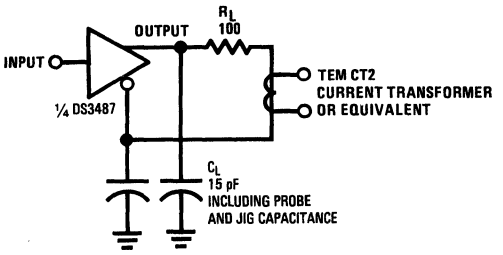
TL/F/5780-6

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

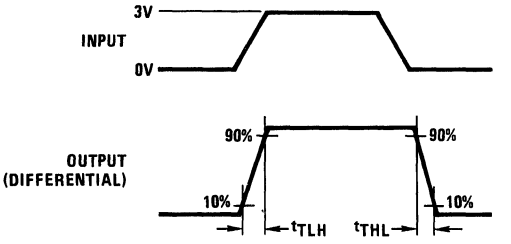
S1 = open for t_{PZH}

S2 = open for t_{PZL}

FIGURE 2. TRI-STATE Enable and Disable Delays



TL/F/5780-7



TL/F/5780-8

Input pulse: f = MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 3. Differential Rise and Fall Times

National Semiconductor

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

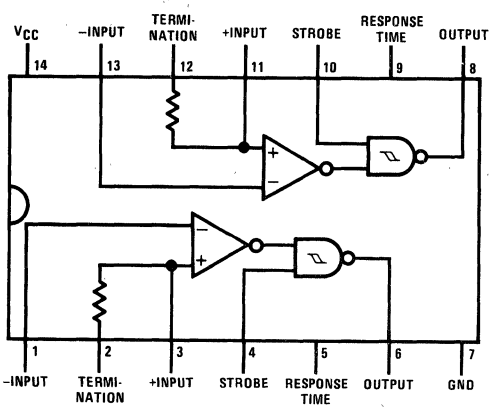
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- ½ V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 or MM78C30/MM88C30 recommended driver

Connection Diagram

Dual-In-Line Package



TL/F/5798–1

Top View

Order Number DS78C20J or DS88C20N
See NS Package Numbers J14A or N14A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS78C20J/883
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	18V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded Package	1280 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.1 mW/°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −200 μA, $V_{OUT} \geq V_{CC}$ −1.2V	−10V ≤ V_{CM} ≤ 10V		0.06	0.2	V
			−15V ≤ V_{CM} ≤ 15V		0.06	0.3	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq$ 0.5V	−10V ≤ V_{CM} ≤ 10V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V			5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V			2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance	I_{OUT} = 200 μA, $V_{OUT} \geq$ V_{CC} −1.2V, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		0.1	0.4	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq$ 0.5V, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −200 μA, V_{DIFF} = 1V		V_{CC} − 1.2	V_{CC} − 0.75		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DIFF} = −1V			0.25	0.5	V
I_{CC}	Power Supply Current	15V ≤ V_{CM} ≤ −15V, V_{DIFF} = −0.5V (Both Receivers)	V_{CC} = 5.5V		8	15	mA
			V_{CC} = 15V		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 15V, V_{DIFF} = 3V	V_{CC} = 15V		15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V	V_{CC} = 15V		−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	I_{OUT} = 1.6 mA, $V_{OL} \leq$ 0.5V	V_{CC} = 5V	3.5	2.5		V
			V_{CC} = 10V	8.0	5.0		V
			V_{CC} = 15V	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	I_{OUT} = −200 μA, V_{OH} = V_{CC} −1.2V	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

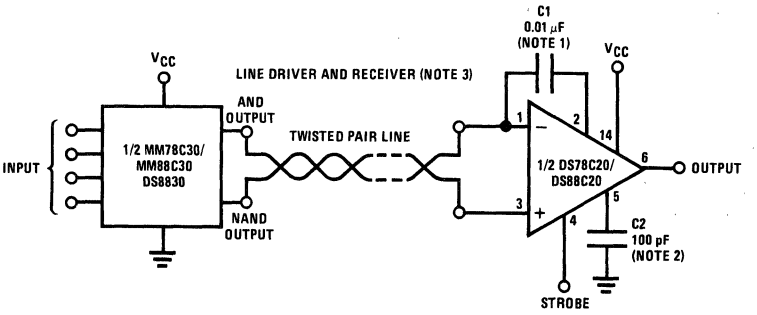
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

Typical Applications

RS-422/RS-423 Application



TL/F/5798–2

Note 1: (Optional internal termination resistor.)

a) Capacitor in series with internal line termination resistor, terminates the line and saves termination power. Exact value depends on line length.

b) Pin 1 connected to pin 2; terminates the line.

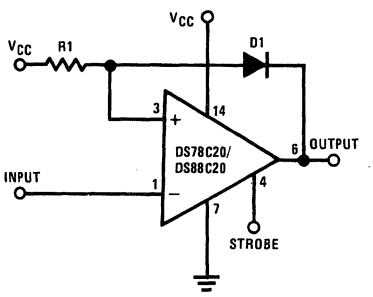
c) Pin 2 open; no internal line termination.

d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

Note 3: V_{CC} 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to applicaton notes AN-22, AN-83 and AN-108.

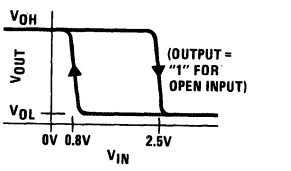
RS-232-C Application with Hysteresis



TL/F/5798–3

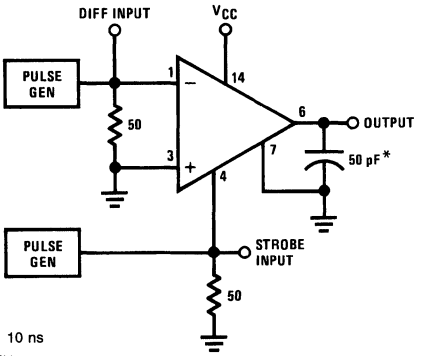
For signals which require fail-safe or have slow rise and fall times, use R1 and D1 as shown above. Otherwise, the positive input (pin 3 or 11) may be connected to ground.

V_{CC}	R1 ±5%
5V	4,3 kΩ
10V	15 kΩ
15V	24 kΩ



TL/F/5798–4

AC Test Circuit

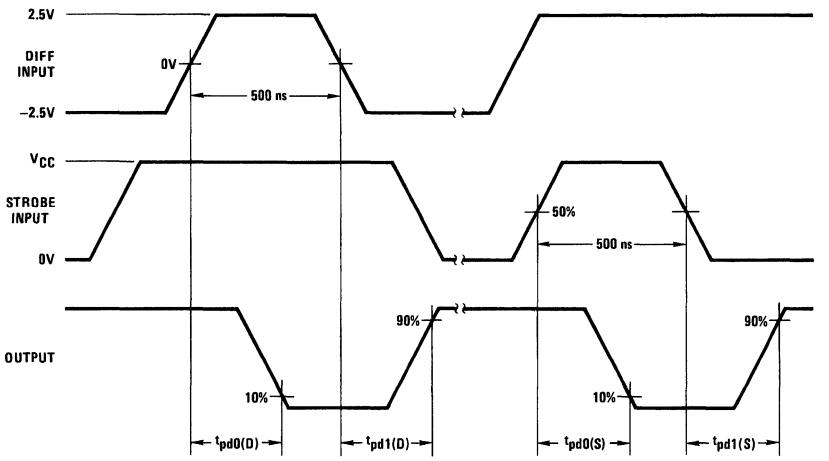


$t_r = t_f = \leq 10$ ns
PRR = 1 MHz

TL/F/5798–5

*Includes probe and jig capacitance

Switching Time Waveforms



TL/F/5798–6

National Semiconductor

DS78C120/DS88C120 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 and DS88C120 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

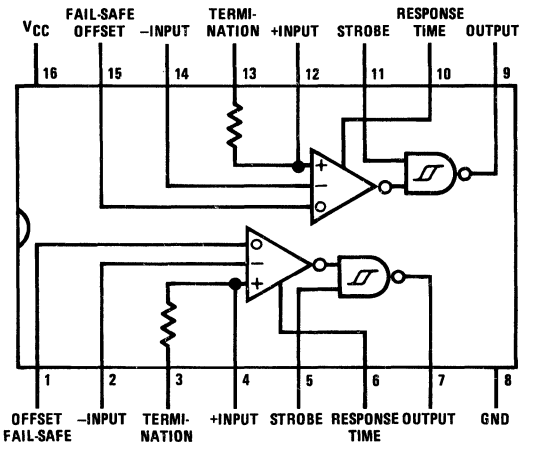
Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range and the DS88C120 from 0°C to +70°C.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



TL/F/5801–1

Top View

Order Number DS88C120N
See NS Package Number N16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS78C120J/883
See NS Package Number J16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C120	−55	+125	°C
DS88C120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage Fail-Safe	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	Offset = 5V	$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	0.2	0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V, 0V \leq V_{CC} \leq 15V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$			56		kΩ
I_{IND}	Data Input Current (Unterminated)	$0V \leq V_{CC} \leq 15V$	$V_{CM} = 10V$		2	3.1	mA
			$V_{CM} = 0V$		0	−0.5	mA
			$V_{CM} = -10V$		−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	$I_{OUT} = 200\ \mu A, V_{OUT} \geq V_{CC} - 1.2V, R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6\ mA, V_{OUT} \leq 0.5V, R_S = 500\Omega$	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A, V_{DIFF} = 1V$		$V_{CC} - 1.2$	$V_{CC} - 0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6\ mA, V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V, V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V, V_{DIFF} = -3V$			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5V, I_{OUT} = 1.6\ mA$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Logical "0" Strobe Input Voltage	V_{OH} V_{CC} − 1.2V, I_{OUT} = −200 μA	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C120 and across the 0°C to +70°C range for the DS88C120. All typical values for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

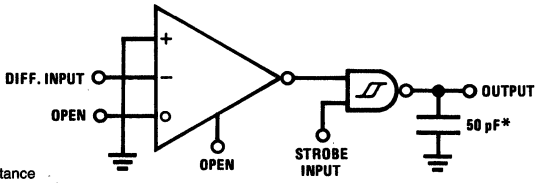
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

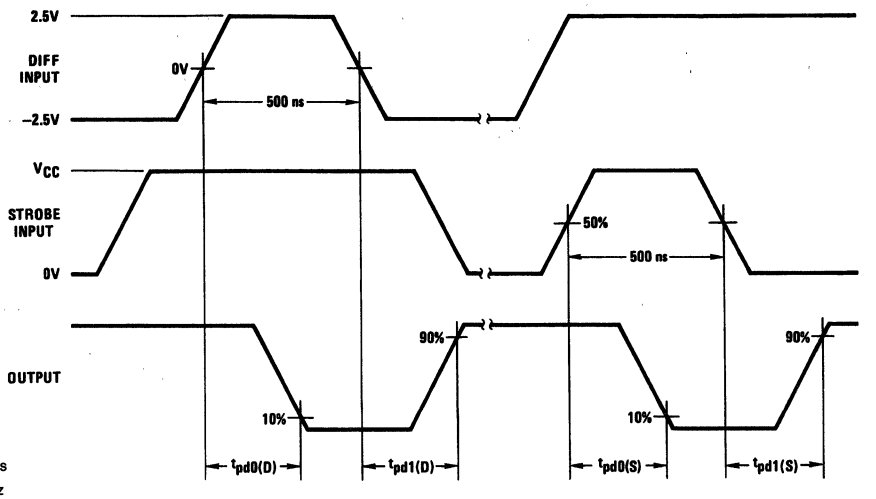
AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

TL/F/5801–3



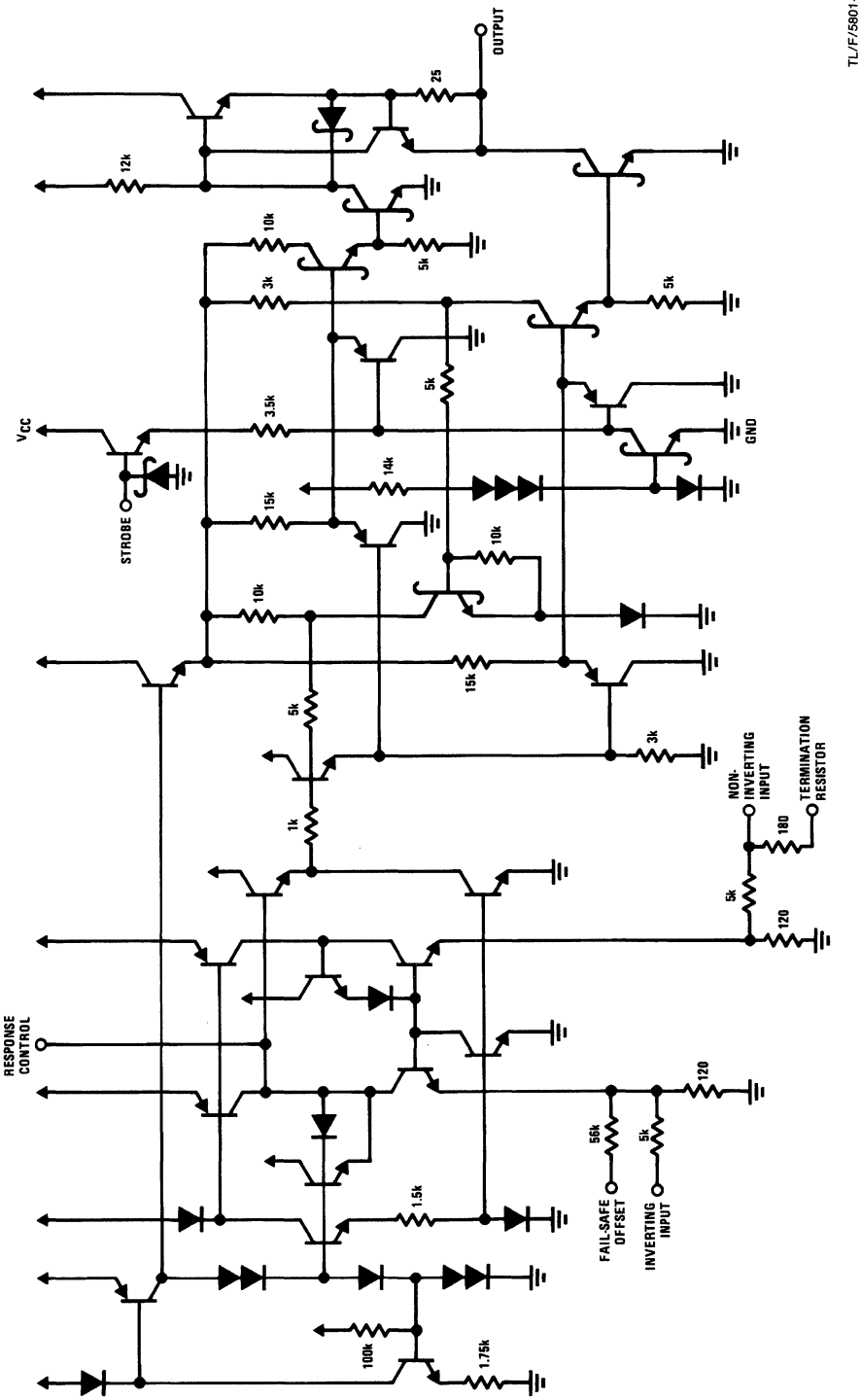
$t_r = t_f \leq 10$ ns

PRR = 1 MHz

TL/F/5801–4

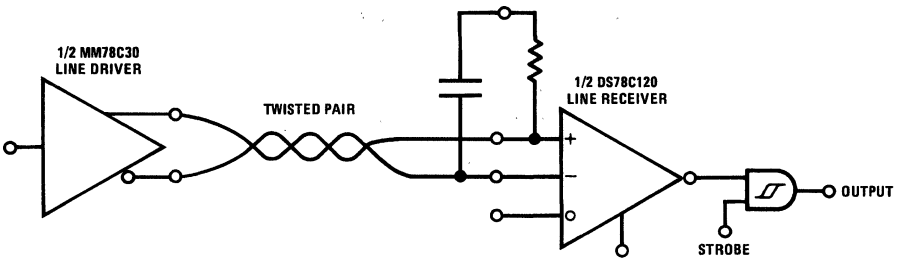
Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

Schematic Diagram (1/2 Circuit Shown)



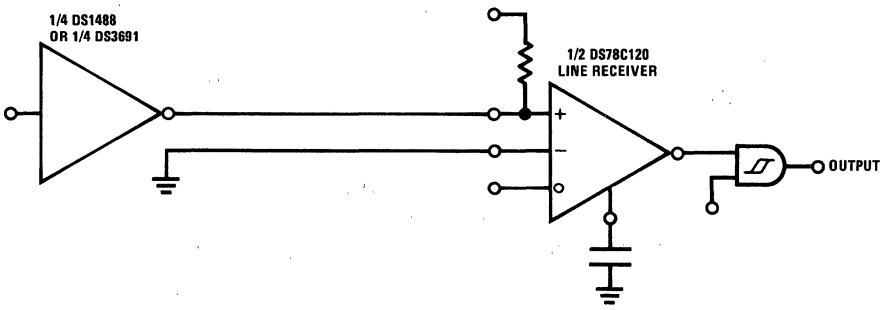
Application Hints

Balanced Data Transmission



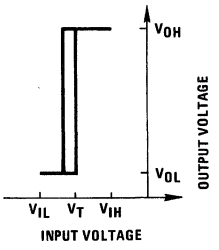
TL/F/5801–5

Unbalanced Data Transmission

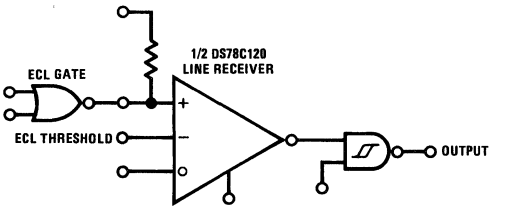


TL/F/5801–6

Logic Level Translator



TL/F/5801–7



TL/F/5801–8

The DS78C120/DS88C120 may be used as a level transistor to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

Application Hints (Continued)

LINE DRIVERS

Line drivers which will interface with the DS78C120/DS88C120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3587, DS3487	Quad TRI-STATE RS-422

Unbalanced Drivers

DS1488	Quad RS-232
DS14C88	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

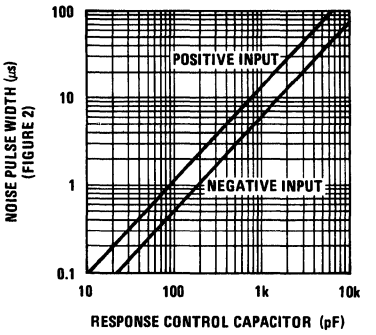
In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78C120/DS88C120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78C120/DS88C120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

TRANSMISSION LINE TERMINATION

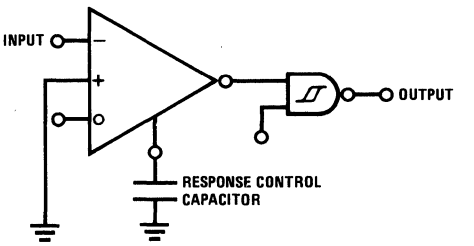
On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78C120/DS88C120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns) the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

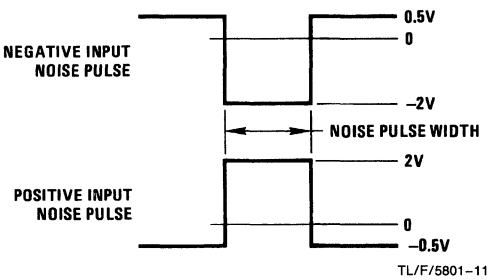


TL/F/5801–9

FIGURE 1. Noise Pulse Width vs Response Control Capacitor



TL/F/5801–10



TL/F/5801–11

FIGURE 2

Application Hints (Continued)

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78C120/DS88C120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

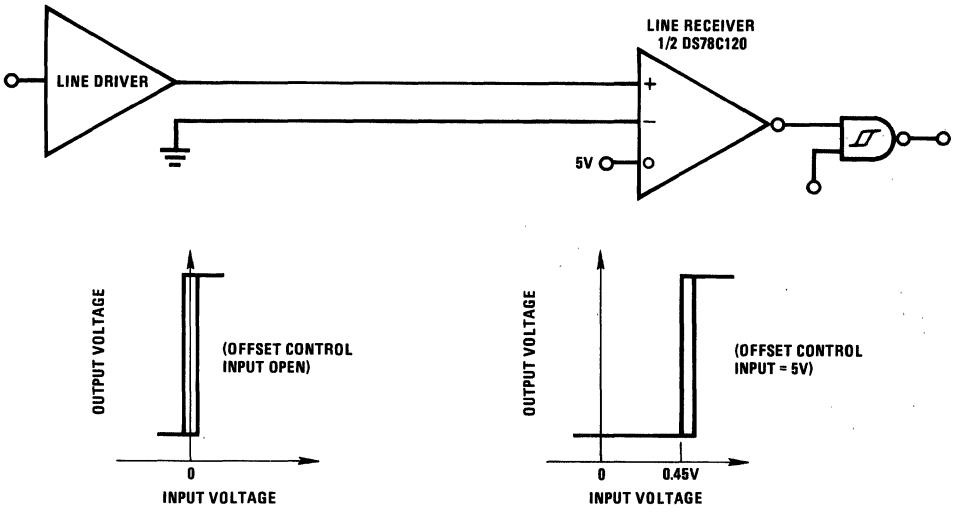
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or shorted.

For balanced operation with inputs shorted or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault condition. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

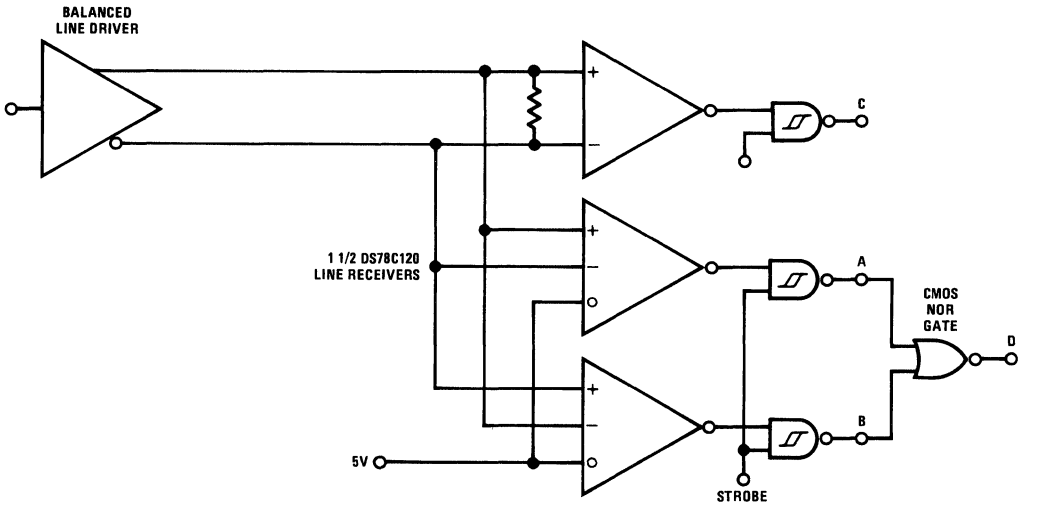
Unbalanced RS-423 and RS-232 Fail-Safe



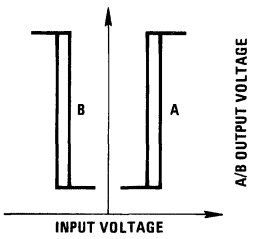
TL/F/5801–12

Application Hints (Continued)

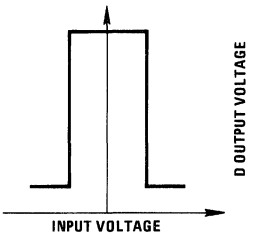
Balanced RS-422 Fail-Safe



TL/F/5801–13



TL/F/5801–14



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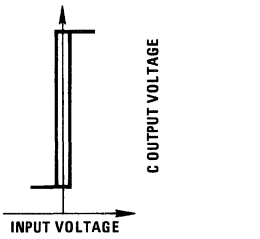


TL/F/5801–16

Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

National Semiconductor

DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

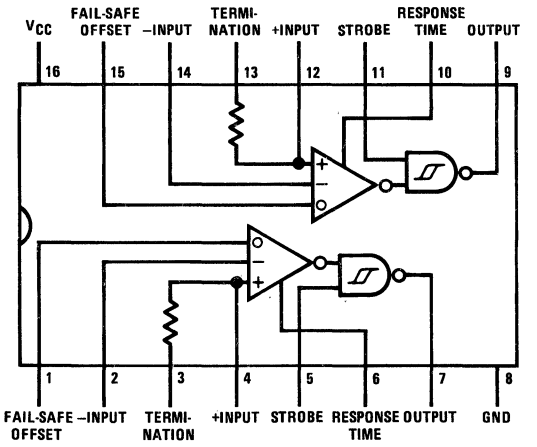
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Meets EIA standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



TL/F/7499–1

Top View

Order Number DS88LS120N or DS88LS120M
See NS Package Number M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS78LS120J/883 or DS78LS120W/883
See NS Package Number J16A or W16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	±25V
Strobe Voltage	7V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mV
Molded Package	1362 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS120	−55	+125	°C
DS88LS120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V	−7V ≤ V_{CM} ≤ 7V		0.06	0.2	V
			−15 ≤ V_{CM} ≤15V		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	I_{OUT} = 4 mA, V_{OUT} ≤ 0.5V	−7V ≤ V_{CM} ≤7V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
V_{TH} V_{TL}	Differential Threshold Voltage with Fail-Safe Offset = 5V	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V	−7V ≤ V_{CM} ≤ 7V		0.47	0.7	V
		I_{OUT} = 4 mA, V_{OUT} ≤ 0.5V	−7V ≤ V_{CM} ≤ 7V	−0.2	−0.42		V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V, 0V ≤ V_{CC} ≤ 7V		4	5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
R_O	Offset Control Resistance	T_A = 25°C		42	56	70	kΩ
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V	0V ≤ V_{CC} ≤ 7V		2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance (Note 5)	I_{OUT} = −400 μA, V_{OUT} ≥ 2.5V, R_S = 500Ω	−7V ≤ V_{CM} 7V		0.1	0.4	V
		I_{OUT} = 4 mA, V_{OUT} ≤ 0.5V, R_S = 500Ω	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400 μA, V_{DIFF} = 1V, V_{CC} = 4.5V		2.5	3		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 4 mA, V_{DIFF} = −1V, V_{CC} = 4.5V			0.35	0.5	V
I_{CC}	Power Supply Current	V_{CC} = 5.5V, V_{DIFF} = −0.5V, (Both Receivers)	V_{CM} = 15V		10	16	mA
			V_{CM} = −15V		10	16	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V			1	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V			−290	−400	μA
V_{IH}	Logical "1" Strobe Input Voltage	V_{OL} ≤ 0.5, I_{OUT} = 4mA		2.0	1.12		V
V_{IL}	Logical "0" Strobe Input Voltage	V_{OH} ≥ 2.5V, I_{OUT}, = −400 μA			1.12	0.8	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V, (Note 4)		−30	−100	−170	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for the DS88LS120. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

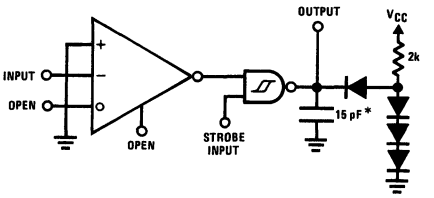
Note 5: Refer to EIA-RS422 for exact conditions.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd0(D)}$	Differential Input to "0" Output	Response Pin Open, C_L = 15 pF, R_L = 2 kΩ		38	60	ns
$t_{pd1(D)}$	Differential Input to "1" Output			38	60	ns
$t_{pd0(S)}$	Strobe Input to "0" Output			16	25	ns
$t_{pd1(S)}$	Strobe Input to "1" Output			12	25	ns

AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



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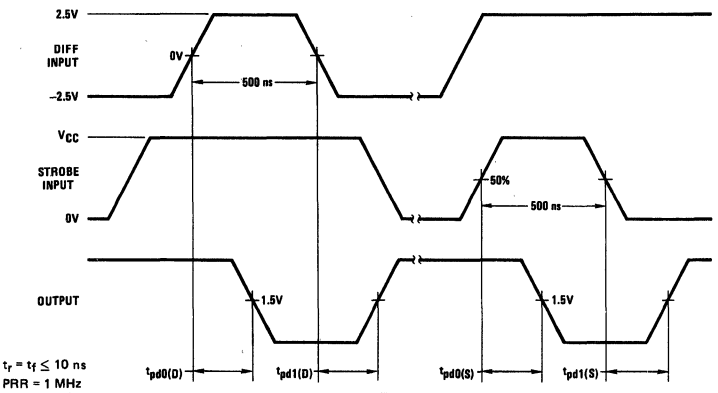
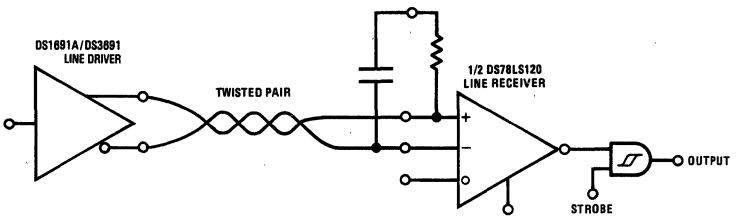
*Includes probe and test fixture capacitance



Note: Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection). TL/F/7499–4

Application Hints

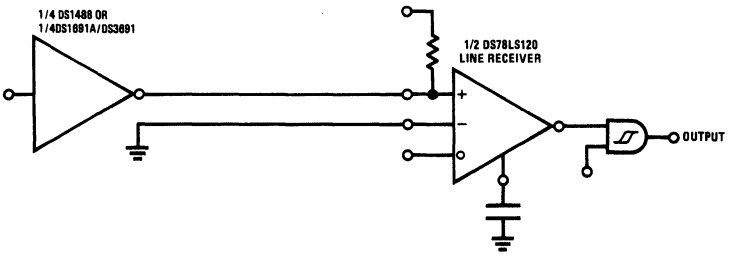
Balanced Data Transmission



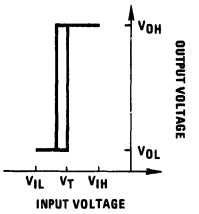
TL/F/7499–5

Application Hints (Continued)

Unbalanced Data Transmission

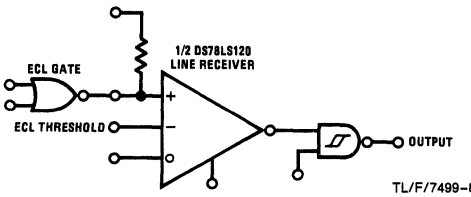


TL/F/7499-6



TL/F/7499-7

Logic Level Translator



TL/F/7499-8

The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78LS120/DS88LS120 are listed below.

Balanced Drivers

DS26LS31	Quad RS-422 Line Driver Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691A, DS3691	Quad RS-423/Dual RS-422 TTL
DS1692, DS3692	Quad RS-423/Dual TRI-STATE RS-422 TTL
DS3487	Quad TRI-STATE RS-422

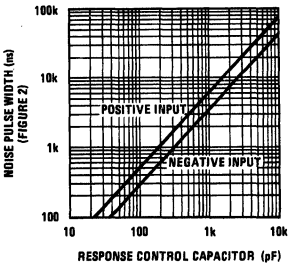
Unbalanced Drivers

DS1488	Quad RS-232
DS75150	Dual RS-232

RESPONSE CONTROL AND HYSTERESIS

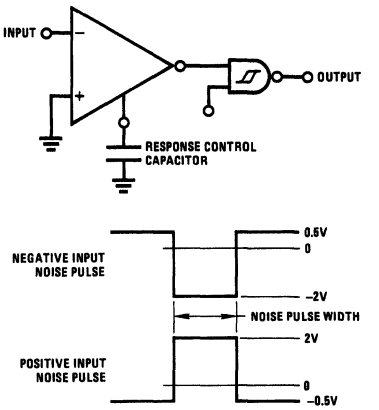
In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1* and *2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.



TL/F/7499-9

FIGURE 1. Noise Pulse Width vs Response Control Capacitor



TL/F/7499-10

FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/crosstalk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

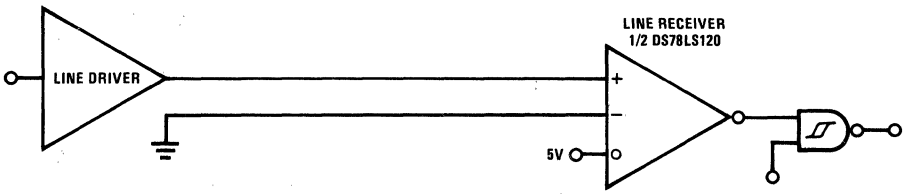
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ +0.45V or $V_{IN(INVERTING)}$ +0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

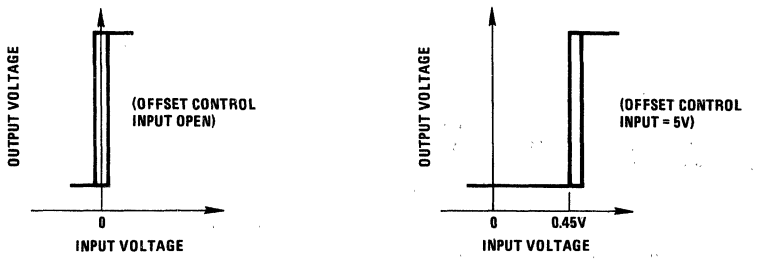
The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the fail-safe offset pin to 5V, offsets the receiver threshold to 0.45V. The output is forced to a logic zero state if the input is open or shorted.

Unbalanced RS-423 and RS-232 Fail-Safe



TL/F/7499–11



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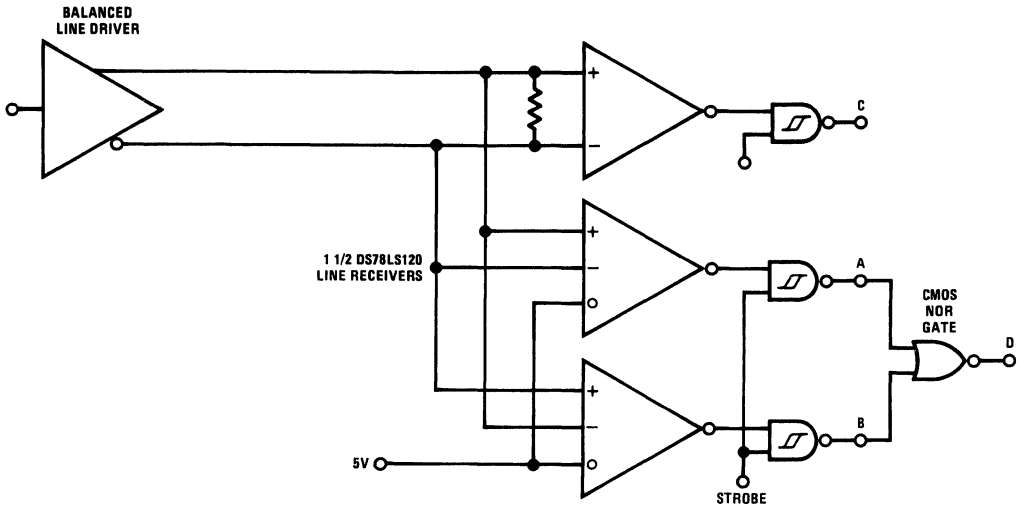
Application Hints (Continued)

Balanced RS-422 Fail-Safe



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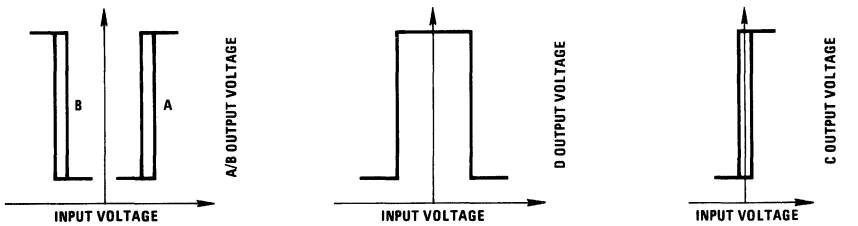


TL/F/7499–14

For balanced operation with inputs open or shorted, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the open or short condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

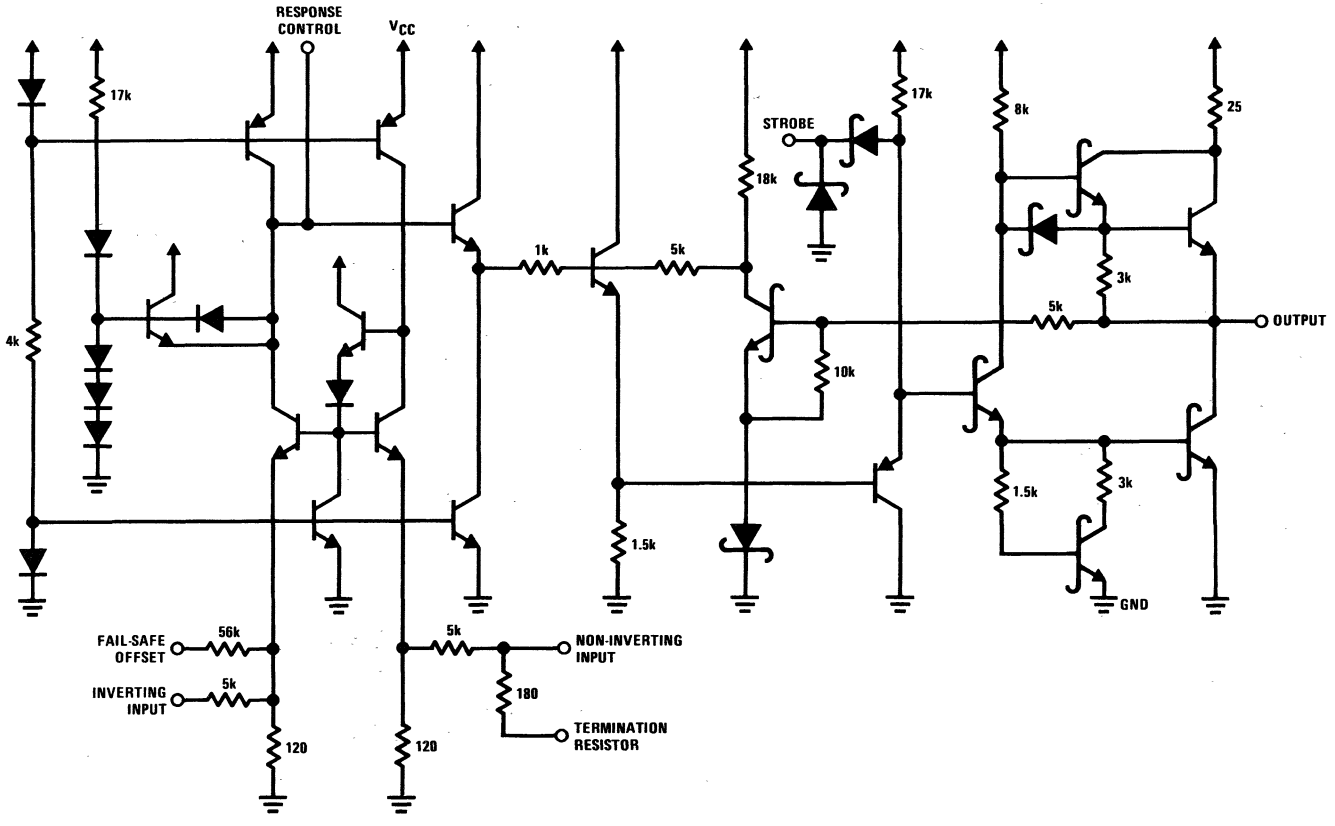
In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

Truth Table (For Balanced Fail-Safe)

Input	Strobe	A-Out	B-Out	C-Out	D-Out
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

Schematic Diagram



TL/F/7499–2

National Semiconductor

DS8921/DS8921A/DS8921AT
Differential Line Driver and Receiver Pair

General Description

The DS8921, DS8921A are Differential Line Driver and Receiver pairs designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, these devices meet the requirements of the EIA Standard RS-422.

The DS8921, DS8921A receivers offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms.

The DS8921, DS8921A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

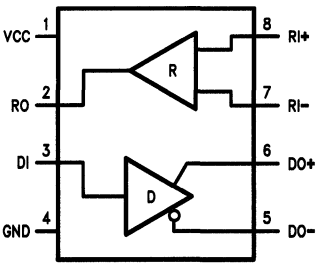
The DS8921, DS8921A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew - 0.5 ns typical
- Meet the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input hysteresis-70 mV typical
- DS8921AT industrial temperature operation (−40°C to +85°C)

3

Connection Diagram



TL/F/8512–1

Order Number DS8921M, DS8921N, DS8921AM, DS8921AN, DS8921ATM, DS8921ATN or DS8921ATJ
See NS Package Number J08A, M08A or N08E

Truth Table

Receiver		Driver		
Input	V_{OUT}	Input	V_{OUT}	$\overline{V_{OUT}}$
$V_{ID} \geq V_{TH}$ (MAX)	1	1	1	0
$V_{ID} \leq V_{TH}$ (MIN)	0	0	0	1
Open	1			

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Driver Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V
Maximum Package Power Dissipation @ +25°C	
J Package	1220 mW
M Package	730 mW
N Package	1160 mW
Derate J Package	9.8 mW/°C above +25°C
Derate M Package	9.3 mW/°C above +25°C
Derate N Package	5.8 mW/°C above +25°C
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	+260°C
Maximum Junction Temperature	+150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)			
DS8921/DS8921A	0	70	°C
DS8921AT	−40	+85	°C

DS8921/DS8921A Electrical Characteristics (Notes 2, 3 and 4)

Symbol	Conditions	Min	Typ	Max	Units
RECEIVER					
V_{TH}	$-7V \le V_{CM} \le +7V$	−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$	15	70		mV
R_{IN}	$V_{IN} = -7V, +7V$ (Other Input = GND)	4.0	6.0		kΩ
I_{IN}	$V_{IN} = 10V$			3.25	mA
	$V_{IN} = -10V$			−3.25	mA
V_{OH}	$I_{OH} = -400\ \mu A$	2.5			V
V_{OL}	$I_{OL} = 8$ mA			0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V	−15		−100	mA
DRIVER					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V		−40	−200	μA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V			20	μA
I_I	V_{CC} = MAX, V_{IN} = 7.0V			100	μA
V_{CL}	V_{CC} = MIN, $I_{IN} = -18$ mA			−1.5	V
V_{OH}	V_{CC} = MIN, $I_{OH} = -20$ mA	2.5			V
V_{OL}	V_{CC} = MIN, $I_{OL} = +20$ mA			0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V			100	μA
$\lvert V_T \rvert - \lvert \overline{VT} \rvert$				0.4	V
V_T		2.0			V
$\lvert V_{OS} - \overline{V_{OS}} \rvert$				0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V	−30		−150	mA
DRIVER and RECEIVER					
I_{CC}	V_{CC} = MAX, V_{OUT} = Logic 0			35	mA

Receiver Switching Characteristics (*Figures 1* and *2*)

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF *(Figures 1, 2)*		14	22.5	20	20	ns
T_{pHL}	C_L = 30 pF *(Figures 1, 2)*		14	22.5	20	20	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	C_L = 30 pF *(Figures 1, 2)*		0.5	5	3.5	5	ns

Driver Switching Characteristics (*Figures 3* and *4*)

SINGLE ENDED CHARACTERISTICS

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF *(Figures 3, 4)*		10	15	15	15	ns
T_{pHL}	C_L = 30 pF *(Figures 3, 4)*		10	15	15	15	ns
T_{TLH}	C_L = 30 pF *(Figures 7, 8)*		5	8	8	9.5	ns
T_{THL}	C_L = 30 pF *(Figures 7, 8)*		5	8	8	9.5	ns
Skew	CL = 30 pF *(Figures 3, 4)*		1	5	3.5	3.5	ns

Driver Switching Characteristics (*Figures 3* and *5*)

DIFFERENTIAL CHARACTERISTICS (Note 6)

Symbol	Conditions	Min	Typ	Max			Units
				8921	8921A	8921AT	
T_{pLH}	C_L = 30 pF *(Figures 3, 5, 6)*		10	15	15	15	ns
T_{pHL}	C_L = 30 pF *(Figures 3, 5, 6)*		10	15	15	15	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	C_L = 30 pF *(Figures 3, 5, 6)*		0.5	6	2.75	2.75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

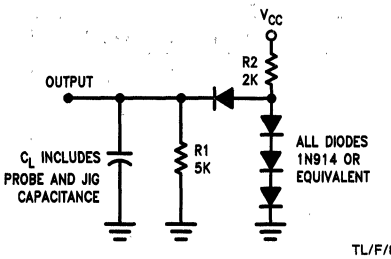
The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$T_{cr} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

Where: T_{cr} = Crossing Point

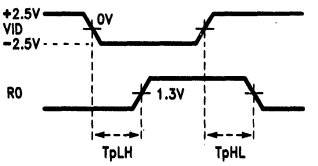
T_{ra}, T_{rb}, T_{fa} and T_{fb} are time measurements with respect to the input. See *Figure 6.*

AC Test Circuits and Switching Diagrams



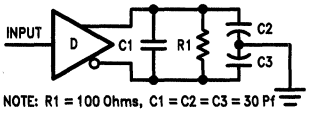
TL/F/8512-3

FIGURE 1



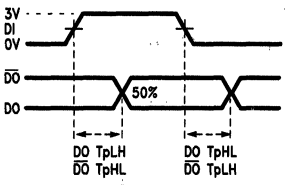
TL/F/8512-4

FIGURE 2



TL/F/8512-5

FIGURE 3



TL/F/8512-6

FIGURE 4

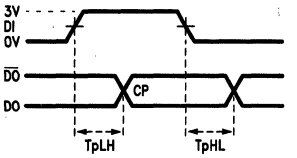


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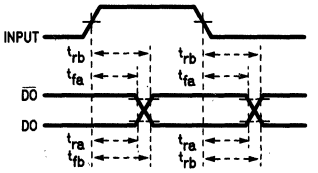
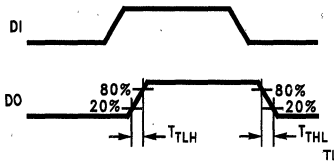
FIGURE 5



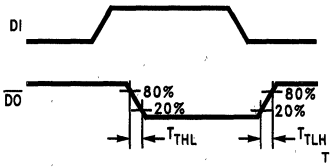
TL/F/8512-2

FIGURE 6



TL/F/8512-10

FIGURE 7

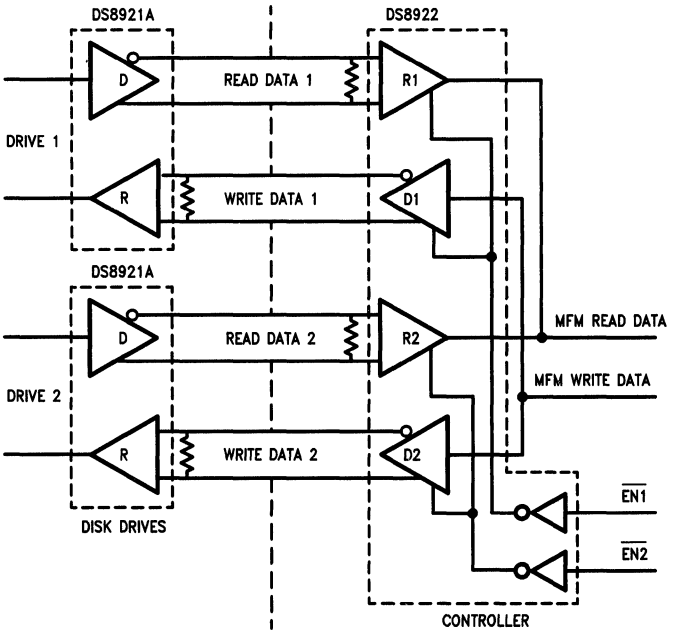


TL/F/8512-11

FIGURE 8

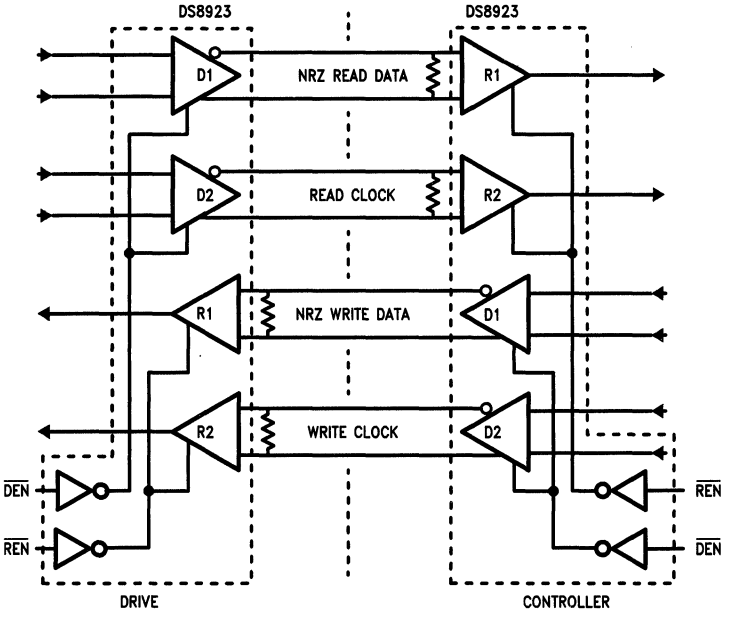
Typical Applications

ST506 and ST412 Application



TL/F/8512–8

ESDI Application



TL/F/8512–9

National Semiconductor

DS89C21
Differential CMOS Line Driver and Receiver Pair

General Description

The DS89C21 is a differential CMOS line driver and receiver pair, designed to meet the requirements of TIA/EIA-422-A (RS-422) electrical characteristics interface standard. The DS89C21 provides one driver and one receiver in a minimum footprint. The device is offered in an 8-pin SOIC package.

The CMOS design minimizes the supply current to 6 mA, making the device ideal for use in battery powered or power conscious applications.

The driver features a fast transition time specified at 2.2 ns, and a maximum differential skew of 2 ns making the driver ideal for use in high speed applications operating above 10 MHz.

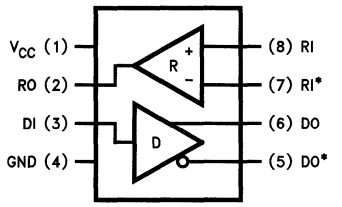
The receiver can detect signals as low as 200 mV, and also incorporates hysteresis for noise rejection. Skew is specified at 4 ns maximum.

The DS89C21 is compatible with TTL and CMOS levels (DI and RO).

Features

- Meets TIA/EIA-422-A (RS-422) and CCITT V.11 recommendation
- LOW POWER design—15 mW typical
- Guaranteed AC parameters:
  — Maximum driver skew 2.0 ns
  — Maximum receiver skew 4.0 ns
- Extended temperature range
  −40°C to +85°C
- Available in SOIC packaging
- Operates over 20 Mbps
- Receiver OPEN input failsafe feature

Connnection Diagram



TL/F/11753–1

Order Number DS89C21TM or DS89C21TN
See NS Package Number M08A or N08E

Truth Tables

Driver

Input	Outputs	
DI	**DO**	**DO***
H	H	L
L	L	H

Receiver

Inputs	Output
RI–RI*	**RO**
$V_{DIFF} \geq +200$ mV	H
$V_{DIFF} \leq -200$ mV	L
OPEN†	H

†Non-terminated

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Driver Input Voltage (DI)	−1.5V to V_{CC} + 1.5V
Driver Output Voltage (DO, DO*)	−0.5V to +7V
Receiver Input Voltage—V_{CM} (RI, RI*)	±14V
Differential Receiver Input Voltage—V_{DIFF} (RI, RI*)	±14V
Receiver Output Voltage (RO)	−0.5V to V_{CC} +0.5V
Receiver Output Current (RO)	±25 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering 4 sec.)	+260°C
Maximum Junction Temperature	150°C
Maximum Package Power Dissipation @ +25°C	
M Package	714 mW
N Package	1275 mW
Derate M Package	5.7 mW/°C above +25°C
Derate N Package	10.2 mW/°C above +25°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature (T_A)	−40	+85	°C
Input Rise or Fall Time (DI)		500	ns

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
V_{IH}	Input Voltage HIGH			DI	2.0		V_{CC}	V
V_{IL}	Input Voltage LOW				GND		0.8	V
I_{IH}, I_{IL}	Input Current	V_{IN} = V_{CC}, GND, 2.0V, 0.8V				0.05	±10	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA					−1.5	V
V_{OD1}	Unloaded Output Voltage	No Load		DO, DO*		4.2	6.0	V
V_{OD2}	Differential Output Voltage	R_L = 100Ω			2.0	3.0		V
ΔV_{OD2}	Change in Magnitude of V_{OD2} for Complementary Output States					5.0	400	mV
V_{OD3}	Differential Output Voltage	R_L = 150Ω			2.1	3.1		V
V_{OD4}	Differential Output Voltage	R_L = 3.9 kΩ				4.0	6.0	V
V_{OC}	Common Mode Voltage	R_L = 100Ω				2.0	3.0	V
ΔV_{OC}	Change in Magnitude of V_{OC} for Complementary Output States					2.0	400	mV
I_{OSD}	Output Short Circuit Current	V_{OUT} = 0V			−30	−115	−150	mA
I_{OFF}	Output Leakage Current	V_{CC} = 0V	V_{OUT} = +6V			0.03	+100	μA
			V_{OUT} = −0.25V			−0.08	−100	μA

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TL}, V_{TH}	Differential Thresholds	V_{IN} = +7V, 0V, −7V		RI, RI*	−200	±25	+200	mV
V_{HYS}	Hysteresis	V_{CM} = 0V			20	50		mV
R_{IN}	Input Impedance	V_{IN} = −7V, +7V, Other = 0V			5.0	9.5		kΩ
I_{IN}	Input Current	Other Input = 0V, V_{CC} = 5.5V and V_{CC} = 0V	V_{IN} = +10V			+1.0	+1.5	mA
			V_{IN} = +3.0V		0	+0.22		mA
			V_{IN} = +0.5V			−0.04		mA
			V_{IN} = −3V		0	−0.41		mA
			V_{IN} = −10V			−1.25	−2.5	mA
V_{OH}	Output HIGH Voltage	I_{OH} = −6 mA	V_{DIFF} = +1V	RO	3.8	4.9		V
			V_{DIFF} = OPEN		3.8	4.9		V
V_{OL}	Output LOW Voltage	I_{OL} = +6 mA, V_{DIFF} = −1V				0.08	0.3	V
I_{OSR}	Output Short Circuit Current	V_{OUT} = 0V			−25	−85	−150	mA
DRIVER AND RECEIVER CHARACTERISTICS								
I_{CC}	Supply Current	No Load	DI = V_{CC} or GND	V_{CC}		3.0	6	mA
			DI = 2.4V or 0.5V			3.8	12	mA

Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified. (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
t_{PLHD}	Propagation Delay LOW to HIGH	R_L = 100Ω, C_L = 50 pF	*(Figures 2, 3)*	2	4.9	10	ns
t_{PHLD}	Propagation Delay HIGH to LOW			2	4.5	10	ns
t_{SKD}	Skew, $\lvert t_{PLHD} - t_{PHLD} \rvert$				0.4	2.0	ns
t_{TLH}	Transition Time LOW to HIGH		*(Figures 2, 4)*		2.2	9	ns
t_{THL}	Transition Time HIGH to LOW				2.1	9	ns
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF, V_{DIFF} = 2.5V, V_{CM} = 0V	*(Figures 5, 6)*	6	18	30	ns
t_{PHL}	Propagation Delay HIGH to LOW			6	17.5	30	ns
t_{SK}	Skew, $\lvert t_{PLH} - t_{PHL} \rvert$				0.5	4.0	ns
t_r	Rise Time		*(Figure 7)*		2.5	9	ns
t_f	Fall Time				2.1	9	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

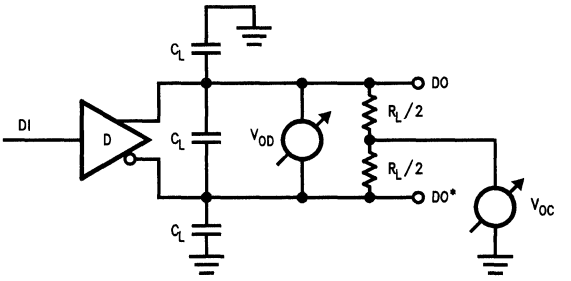
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 4: f = 1 MHz, t_r and t_f ≤ 6 ns.

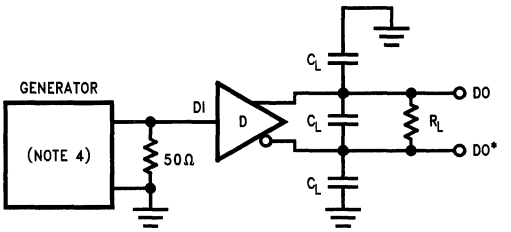
Note 5: ESD Rating: HBM (1.5 kΩ, 100 pF) all pins ≥ 2000V.
EIAJ (0Ω, 200 pF) ≥ 250V

Parameter Measurement Information



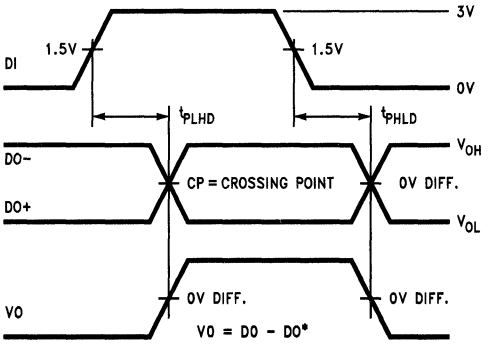
TL/F/11753-2

FIGURE 1. V_{OD} and V_{OC} Test Circuit



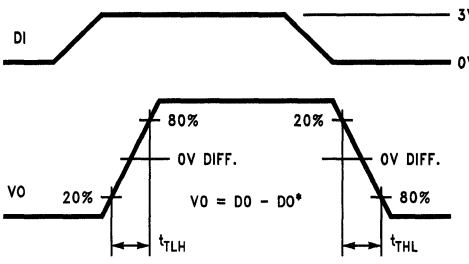
TL/F/11753-3

FIGURE 2. Driver Propagation Delay Test Circuit



TL/F/11753-4

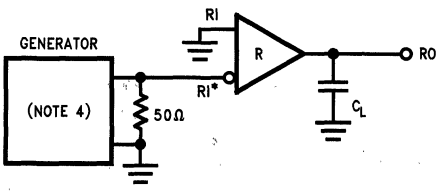
FIGURE 3. Driver Differential Propagation Delay Timing



TL/F/11753-5

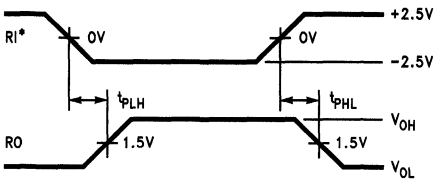
FIGURE 4. Driver Differential Transition Timing

Parameter Measurement Information (Continued)



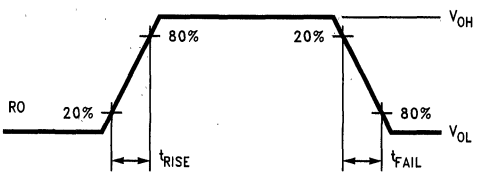
TL/F/11753–6

FIGURE 5. Receiver Propagation Delay Test Circuit



TL/F/11753–7

FIGURE 6. Receiver Propagation Delay Timing



TL/F/11753–8

FIGURE 7. Receiver Rise and Fall Times

National Semiconductor

PRELIMINARY

DS89LV21
3V Differential CMOS Line Driver and Receiver Pair

General Description

The DS89LV21 is a differential CMOS line driver and receiver pair, designed to operate with TIA/EIA-422-B (RS-422) and V.11 electrical characteristics interface standards. The DS89LV21 provides one driver and one receiver in a minimum footprint. The device is featured in 8-pin SOIC and DIP packages.

The 3V CMOS design minimizes the supply current to 1.8 mA, making the device ideal for use in battery powered or power conscious applications.

The driver features a fast transition time specified at 3 ns, and a maximum differential skew of 2 ns making the driver ideal for use in high speed applications operating above 5 MHz.

The receiver can detect signals as low as 200 mV, and also incorporates hysteresis for noise rejection. Skew is specified at 4 ns maximum.

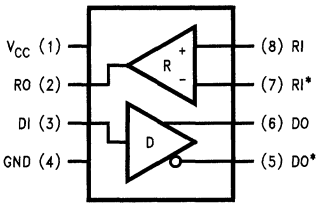
The DS89LV21 is compatible with TTL and CMOS levels (DI and RO).

Features

- Single 3.3V power supply operation
- Operates with TIA/EIA-422-B (RS-422) and ITU V.11
- LOW POWER design—6 mW typical
- Guaranteed AC parameters:
  - — Maximum driver skew 2.0 ns
  - — Maximum receiver skew 4.0 ns
- Extended temperature range
  −40°C to +85°C
- Available in SOIC packaging
- Operates over 10 Mbps
- Receiver OPEN† input failsafe feature

3

Connection Diagram



TL/F/12620–1

Order Number DS89LV21TM or DS89LV21TN
See NS Package Number M08A or N08E

Truth Tables

Driver

Input	Outputs	
DI	**DO**	**DO***
H	H	L
L	L	H

Receiver

Inputs	Output
RI–RI*	**RO**
$V_{DIFF} \geq +200$ mV	H
$V_{DIFF} \leq -200$ mV	L
OPEN†	H

†Non-terminated

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Driver Input Voltage (DI)	−1.5V to V_{CC} + 1.5V
Driver Output Voltage (DO, DO*)	−0.5V to +7V
Receiver Input Voltage—V_{CM} (RI, RI*)	±14V
Differential Receiver Input Voltage—V_{DIF} (RI, RI*)	±14V
Receiver Output Voltage (RO)	−0.5V to V_{CC} + 0.5V
Receiver Output Current (RO)	±25 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering 4 sec.)	+260°C
Maximum Junction Temperature	150°C
Maximum Package Power Dissipation @ +25°C	
M Package	714 mW
N Package	1275 mV
Derate M Package	5.7 mW/°C above +25°C
Derate N Package	10.2 mW/°C above +25°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	3.0	3.6	V
Operating Temperature (T_A)	−40	+85	°C
Input Rise or Fall Time (DI)		500	ns

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
V_{IH}	Input Voltage HIGH			DI	2.0		V_{CC}	V
V_{IL}	Input Voltage LOW				GND		0.8	V
I_{IH}, I_{IL}	Input Current	V_{IN} = V_{CC}, GND, 2.0V, 0.8V				0.05	±10	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA					−1.5	V
V_{OD1}	Unloaded Output Voltage	No Load		DO, DO*		2.6	4.0	V
V_{OD2}	Differential Output Voltage	R_L = 100Ω			1.2	1.6		V
ΔV_{OD2}	Change in Magnitude of V_{OD2} for Complementary Output States					5.0	400	mV
V_{OD3}	Differential Output Voltage	R_L = 150Ω			1.3	1.8		V
V_{OD4}	Differential Output Voltage	R_L = 3.9 kΩ				2.3	4.0	V
V_{OC}	Common Mode Voltage	R_L = 100Ω				2.0	3.0	V
ΔV_{OC}	Change in Magnitude of V_{OC} for Complementary Output States					2.0	400	mV
I_{OSD}	Output Short Circuit Current	V_{OUT} = 0V			−30	−65	−100	mA
I_{OFF}	Output Leakage Current	V_{CC} = 0V	V_{OUT} = +4V			0.03	+100	μA
			V_{OUT} = −0.25V			−0.08	−100	μA

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3) (Continued)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TL}, V_{TH}	Differential Thresholds	V_{IN} = +7V, 0V, −7V		RI, RI*	−200	±35	+200	mV
V_{HYS}	Hysteresis	V_{CM} = 0V				70		mV
R_{IN}	Input Impedance	V_{IN} = −7V, +7V, Other = 0V			6.5	8.5		kΩ
I_{IN}	Input Current	Other Input = 0V, V_{CC} = 3.6V and V_{CC} = 0V	V_{IN} = +10V			+1.1	+1.5	mA
			V_{IN} = +3.0V		0	+0.27		mA
			V_{IN} = +0.5V			−0.02		mA
			V_{IN} = −3V		0	−0.43		mA
			V_{IN} = −10V			−1.25	−2.0	mA
V_{OH}	Output HIGH Voltage	I_{OH} = −6 mA	V_{DIFF} = +1V	RO	2.4	3.0		V
			V_{DIFF} = OPEN		2.4	3.0		V
V_{OL}	Output LOW Voltage	I_{OL} = +6 mA, V_{DIFF} = −1V				0.08	0.3	V
I_{OSR}	Output Short Circuit Current	V_{OUT} = 0V			−15	−40	−100	mA
DRIVER AND RECEIVER CHARACTERISTICS								
I_{CC}	Supply Current	No Load	DI = V_{CC} or GND	V_{CC}		1.8	3	mA
			DI = 2.4V or 0.5V			2.0	6	mA

Switching Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Note 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
t_{PLHD}	Propagation Delay LOW to HIGH	R_L = 100Ω, C_L = 50 pF	*(Figures 2, 3)*	2	5.5	11	ns
t_{PHLD}	Propagation Delay HIGH to LOW			2	6.5	11	ns
t_{SKD}	Skew, $\lvert t_{PLHD} - t_{PHLD} \rvert$				1	2.0	ns
t_{TLH}	Transition Time LOW to HIGH		*(Figures 2, 4)*		3	6	ns
t_{THL}	Transition Time HIGH to LOW				3	6	ns
RECEIVER CHARACTERISTICS							
t_{PLH}	Propagation Delay LOW to HIGH	C_L = 50 pF, V_{DIFF} = 2.5V, V_{CM} = 0V	*(Figures 5, 6)*	10	27	45	ns
t_{PHL}	Propagation Delay HIGH to LOW			10	26	45	ns
t_{SK}	Skew, $\lvert t_{PLH} - t_{PHL} \rvert$				1	4.0	ns
t_r	Rise Time		*(Figure 7)*		3	6	ns
t_f	Fall Time				3	6	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

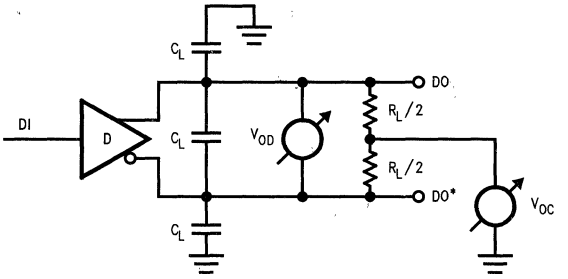
Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 3.3V and T_A = 25°C.

Note 4: f = 1 MHz, t_r and $t_f \leq$ 6 ns.

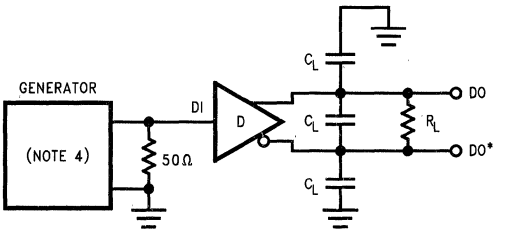
Note 5: ESD Rating: HBM (1.5 kΩ, 100 pF) all pins ≥ 2000V.
EIAJ (0Ω, 200 pF) ≥ 250V

Parameter Measurement Information



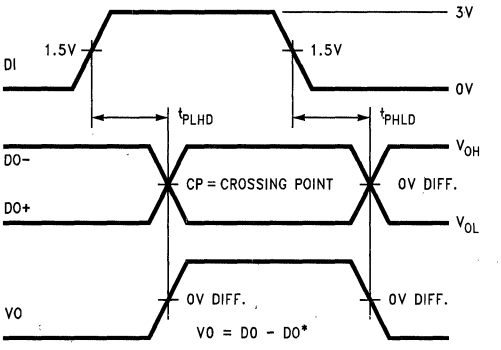
TL/F/12620–2

FIGURE 1. V_{OD} and V_{OC} Test Circuit



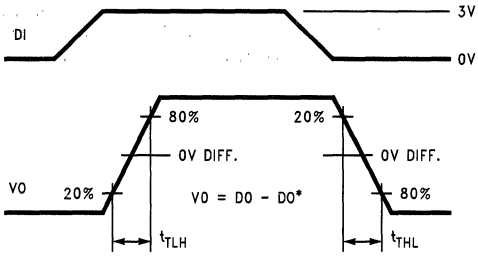
TL/F/12620–3

FIGURE 2. Driver Propagation Delay Test Circuit



TL/F/12620–4

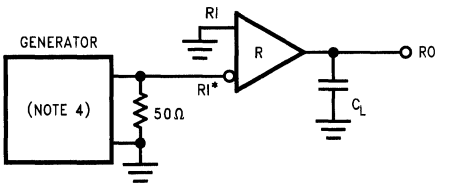
FIGURE 3. Driver Differential Propagation Delay Timing



TL/F/12620–5

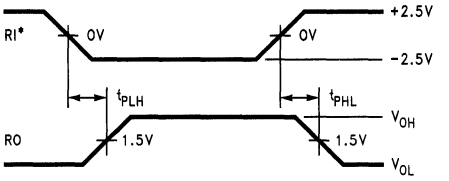
FIGURE 4. Driver Differential Transition Timing

Parameter Measurement Information (Continued)



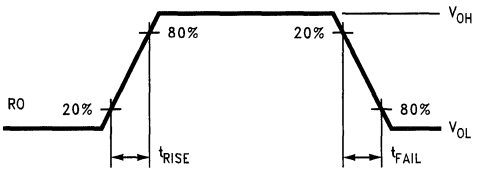
TL/F/12620–6

FIGURE 5. Receiver Propagation Delay Test Circuit



TL/F/12620–7

FIGURE 6. Receiver Propagation Delay Timing



TL/F/12620–8

FIGURE 7. Receiver Rise and Fall Times

National Semiconductor

DS8922/DS8922A/DS8923/DS8923A TRI-STATE® RS-422 Dual Differential Line Driver and Receiver Pairs

General Description

The DS8922/22A and DS8923/23A are Dual Differential Line Driver and Receiver pairs. These devices are designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, the devices meet the requirements of the EIA Standard RS-422.

These devices offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8922A and DS8923A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

Both devices feature TRI-STATE outputs. The DS8922/22A have independent control functions common to a driver and receiver pair. The DS8923/23A have separate driver and receiver control functions.

Power up/down circuitry is featured which will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or power down operation.

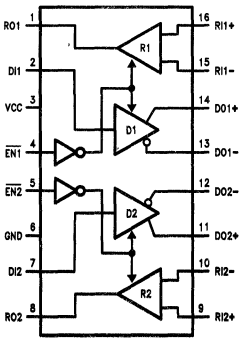
The DS8922/22A and DS8923/23A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew—±0.5 ns typical
- Meets the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis—70 mV typical
- Glitch free power up/down
- TRI-STATE outputs

Connection Diagrams

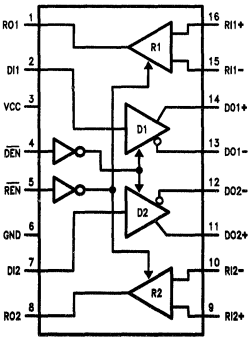
DS8922A Dual-In-Line



TL/F/8511–1

Order Number DS8922M, DS8922N, DS8922AM or DS8922AN
See NS Package Number M16A or N16A

DS8923A Dual-In-Line



TL/F/8511–2

Order Number DS8923M, DS8923N, DS8923AM or DS8923AN
See NS Package Number M16A or N16A

Truth Tables

DS8922/22A

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

DS8923/23A

$\overline{DEN}$	$\overline{REN}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Drive Input Voltage	−0.5V to +7V
Output Voltage	5.5V
Receiver Output Sink Current	50 mA
Receiver Input Voltage	±10V
Differential Input Voltage	±12V

Maximum Package Power Dissapation @ +25°C	
M Package	1300 mW
N Package	1450 mW
Derate M Package 10.4 mW/°C above +25°C	
Derate N Package 11.6 mW/°C above +25°C	
Storage Temperature Range	−65°C to +165°C
Lead Temp. (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.5	5.5	V
Temperature (T_A)	0	70	°C

DS8922/22A and DS8923/23A Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER						
V_{TH}	$-7V \le V_{CM} \le +7V$		−200	±35	+200	mV
V_{HYST}	$-7V \le V_{CM} \le +7V$		15	70		mV
R_{IN}	V_{IN} = −7V, +7V (Other Input = GND)		4.0	6.0		kΩ
I_{IN}	V_{IN} = 10V				3.25	mA
	V_{IN} = −10V				−3.25	mA
V_{OH}	V_{CC} = MIN, I_{OH} = − 400 μA		2.5			V
V_{OL}	V_{CC} = MAX, I_{OL} = 8 mA				0.5	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−15		−100	mA
DRIVER						
V_{OH}	V_{CC} = MIN, I_{OH} = −20 mA		2.5			V
V_{OL}	V_{CC} = MIN, I_{OL} = +20 mA				0.5	V
I_{OFF}	V_{CC} = 0V, V_{OUT} = 5.5V				100	μA
$\lvert VT\rvert - \lvert\overline{VT}\rvert$					0.4	V
VT			2.0			V
$\lvert V_{OS} - \overline{V_{OS}}\rvert$					0.4	V
I_{SC}	V_{CC} = MAX, V_{OUT} = 0V		−30		−150	mA
DRIVER and RECEIVER						
I_{OZ} TRI-STATE Leakage	V_{CC} = MAX	V_{OUT} = 2.5V			50	μA
		V_{OUT} = 0.4V			−50	μA
I_{CC}	V_{CC} = MAX	ACTIVE			76	mA
		TRI-STATE			78	mA
DRIVER and ENABLE INPUTS						
V_{IH}			2.0			V
V_{IL}					0.8	V
I_{IL}	V_{CC} = MAX, V_{IN} = 0.4V			−40	−200	μA
I_{IH}	V_{CC} = MAX, V_{IN} = 2.7V				20	μA
I_I	V_{CC} = MAX, V_{IN} = 7.0V				100	μA
V_{CL}	V_{CC} = MIN, I_{IN} = −18 mA				−1.5	V

Receiver Switching Characteristics (*Figures 1, 2* and *3*)

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
T_{pLH}	CL = 30 pF		12	22.5	20	ns
T_{pHL}	CL = 30 pF		12	22.5	20	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	5	3.5	ns
Skew (Channel to Channel)	CL = 30 pF		0.5	3.0	2.0	ns
T_{pLZ}	CL = 15 pF S2 Open		15			ns
T_{pHZ}	CL = 15 pF S1 Open		15			ns
T_{pZL}	CL = 30 pF S2 Open		20			ns
T_{pZH}	CL = 30 pF S1 Open		20			ns

Driver Switching Characteristics

Parameter	Conditions	Min	Typ	Max		Units
				8922/23	8922A/23A	
SINGLE ENDED CHARACTERISTICS (*Figures 4, 5, 6* and *8*)						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
T_{TLH}	CL = 30 pF		5	10	10	ns
T_{THL}	CL = 30 pF		5	10	10	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5			ns
Skew	CL = 30 pF (Note 5)		0.5	5	3.5	ns
Skew (Channel to Channel)			0.5	3.0	2.0	ns
T_{pLZ}	CL = 30 pF		15			ns
T_{pHZ}	CL = 30 pF		15			ns
T_{pZL}	CL = 30 pF		20			ns
T_{pZH}	CL = 30 pF		20			ns
DIFFERENTIAL SWITCHING CHARACTERISTICS (Note 6, *Figures 4* and *7*)						
T_{pLH}	CL = 30 pF		12	15	15	ns
T_{pHL}	CL = 30 pF		12	15	15	ns
$\lvert T_{pLH}-T_{pHL}\rvert$	CL = 30 pF		0.5	6.0	2.75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis.

Note 3: All typical values are V_{CC} = 5V, T_A = 25°C.

Note 4: Only one output at a time should be shorted.

Note 5: Difference between complementary outputs at the 50% point.

Note 6: Differential Delays are defined as calculated results from single ended rise and fall time measurements. This approach in establishing AC performance specifications has been taken due to limitations of available Automatic Test Equipment (ATE).

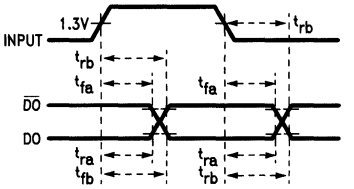
The calculated ATE results assume a linear transition between measurement points and are a result of the following equations:

$$Tcp = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

Where: Tcp = Crossing Point

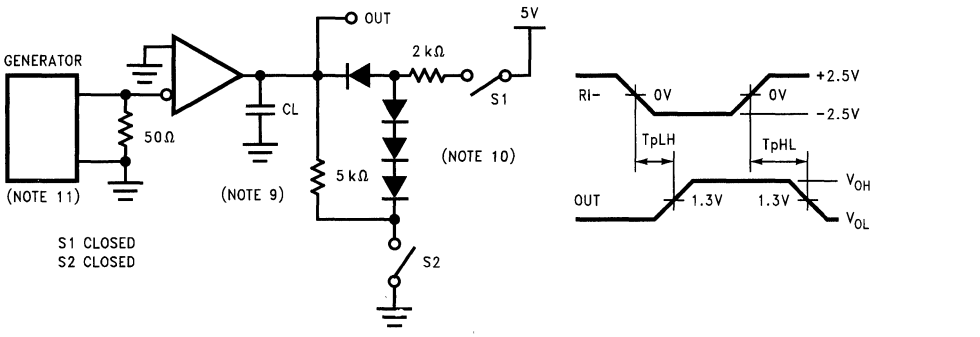
Tra, Trb, Tfa and Tfb are time measurements with respect to the input.

Switching Time Waveforms



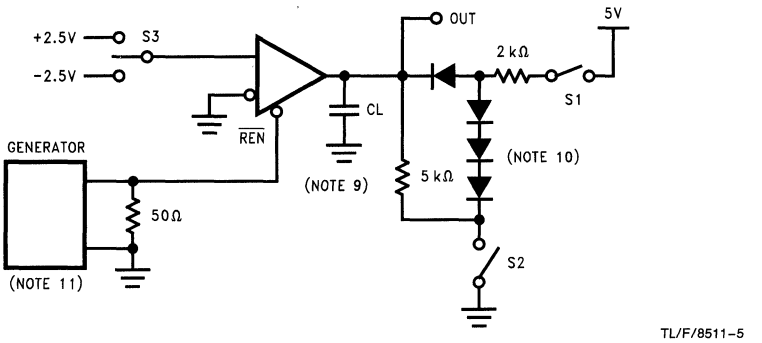
TL/F/8511–3

AC Test Circuits and Switching Waveforms



TL/F/8511–4

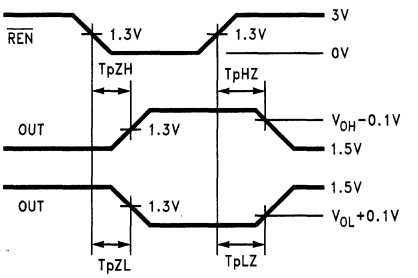
FIGURE 1



TL/F/8511–5

FIGURE 2

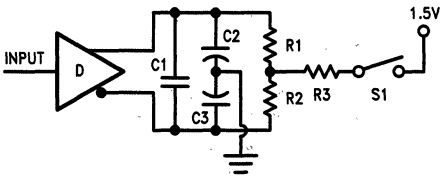
	S1	S2	S3
T_{PLZ}	Closed	Open	+2.5V
T_{PHZ}	Open	Closed	−2.5V
T_{PZL}	Closed	Open	+2.5V
T_{PZH}	Open	Closed	−2.5V



TL/F/8511–6

FIGURE 3

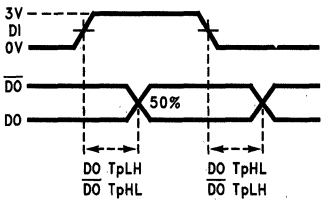
AC Test Circuit and Switching Waveforms (Continued)



NOTE: C1=C2=C3=30 pF, R1=R2=50 Ω, R3=500 Ω

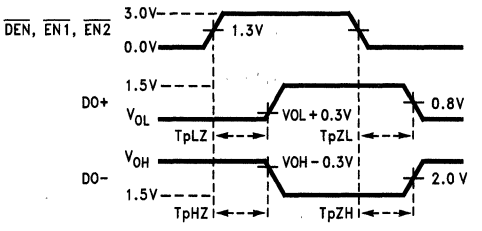
TL/F/8511-7

FIGURE 4



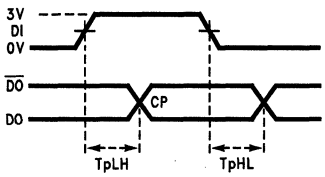
TL/F/8511-8

FIGURE 5



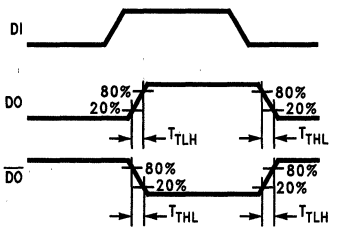
TL/F/8511-9

FIGURE 6



TL/F/8511-10

FIGURE 7

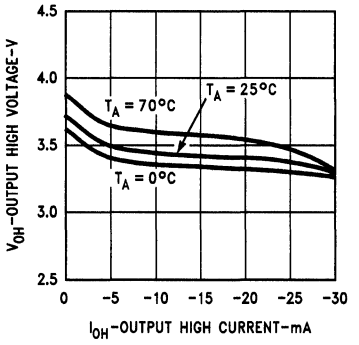


TL/F/8511-13

FIGURE 8

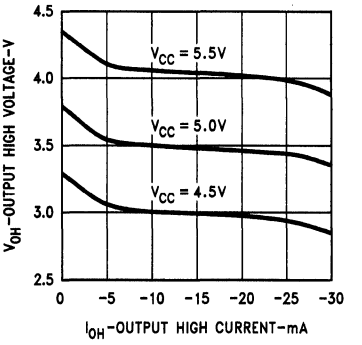
Typical Performance Characteristics (DS8923A)

Driver V_{OH} vs I_{OH} vs Temperature



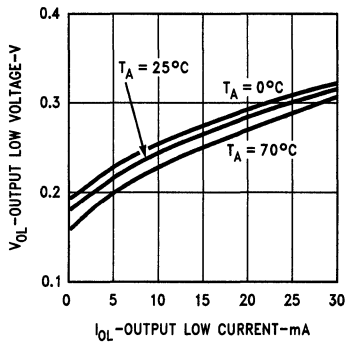
TL/F/8511–14

Driver V_{OH} vs I_{OH} vs V_{CC}



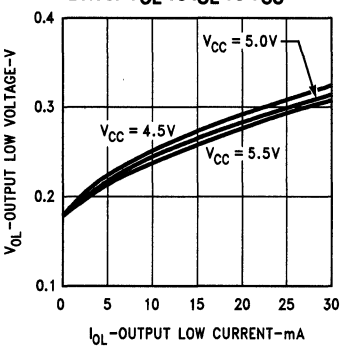
TL/F/8511–15

Driver V_{OL} vs I_{OL} vs Temperature



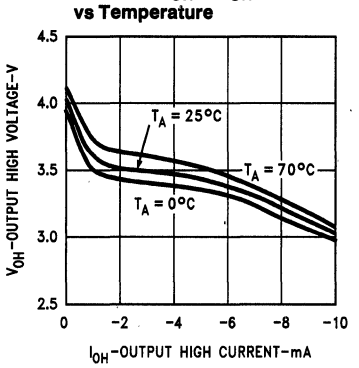
TL/F/8511–16

Driver V_{OL} vs I_{OL} vs V_{CC}



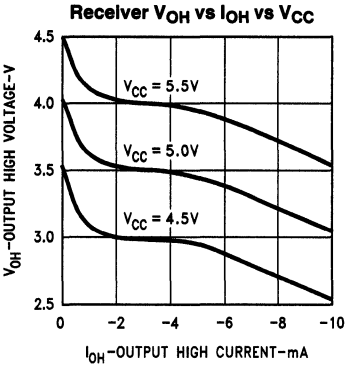
TL/F/8511–17

Receiver V_{OH} vs I_{OH} vs Temperature



TL/F/8511–18

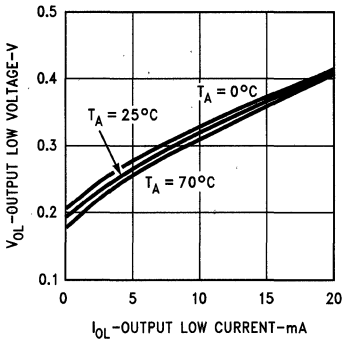
Receiver V_{OH} vs I_{OH} vs V_{CC}



TL/F/8511–19

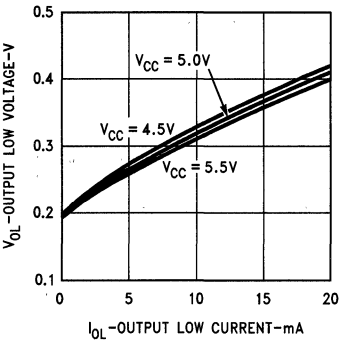
Typical Performance Characteristics (DS8923A) (Continued)

Receiver V_{OL} vs I_{OL} vs Temperature



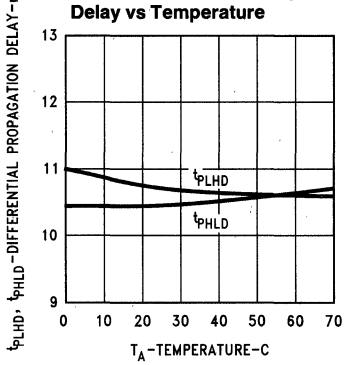
TL/F/8511–20

Receiver V_{OL} vs I_{OL} vs V_{CC}



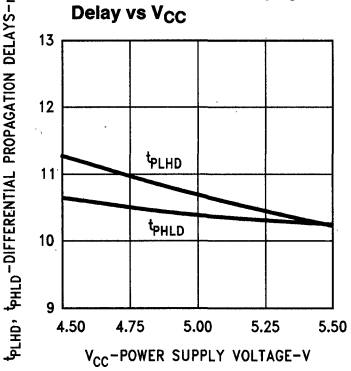
TL/F/8511–21

Driver Differential Propagation Delay vs Temperature



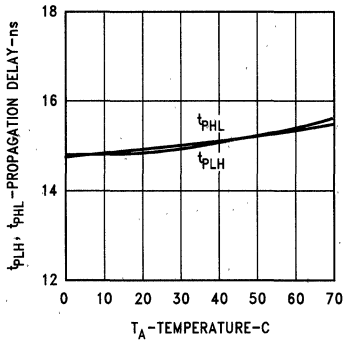
TL/F/8511–22

Driver Differential Propagation Delay vs V_{CC}



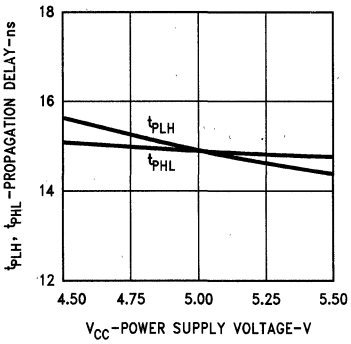
TL/F/8511–23

Receiver Propagation Delay vs Temperature



TL/F/8511–24

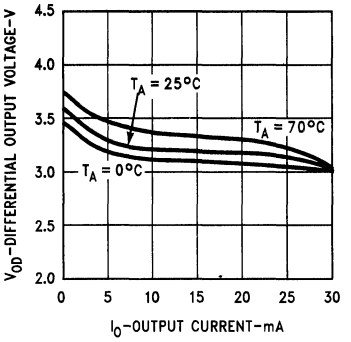
Receiver Propagation Delay vs V_{CC}



TL/F/8511–25

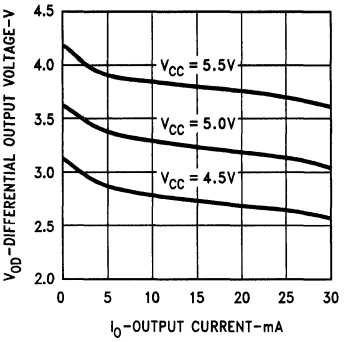
Typical Performance Characteristics (DS8923A) (Continued)

Driver V_{OD} vs Temperature



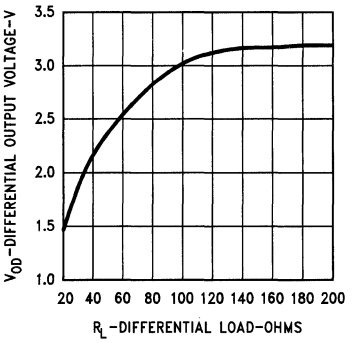
TL/F/8511–26

Driver V_{OD} vs V_{CC}



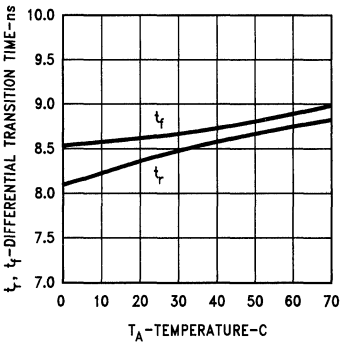
TL/F/8511–27

Driver V_{OD} vs R_L



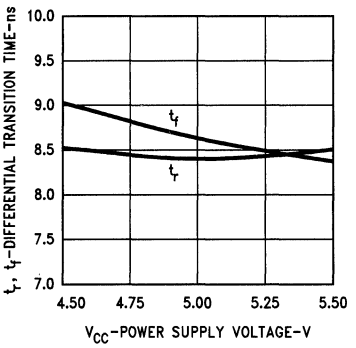
TL/F/8511–28

Driver Differential Transition Time vs Temperature



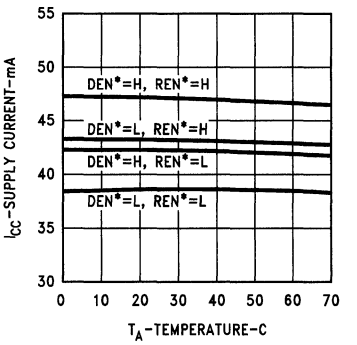
TL/F/8511–29

Driver Differential Transition Time vs V_{CC}



TL/F/8511–30

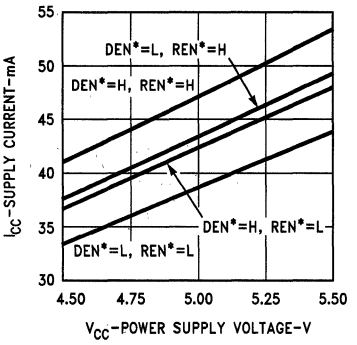
Supply Current vs Temperature



TL/F/8511–31

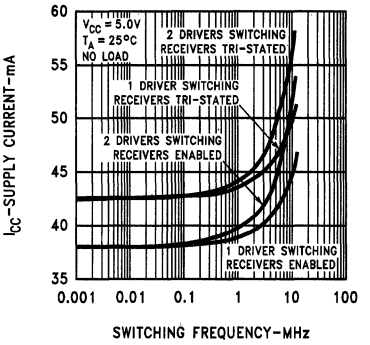
Typical Performance Characteristics (DS8923A) (Continued)

Supply Current vs V_{CC}



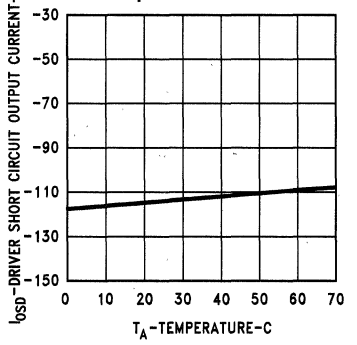
TL/F/8511–32

I_{CC} vs Driver Switching Frequency



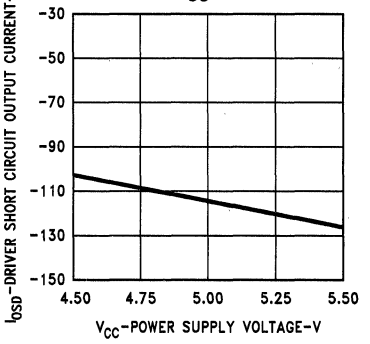
TL/F/8511–33

Driver Short Circuit Current vs Temperature



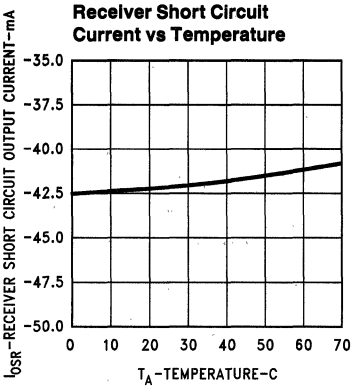
TL/F/8511–34

Driver Short Circuit Current vs V_{CC}



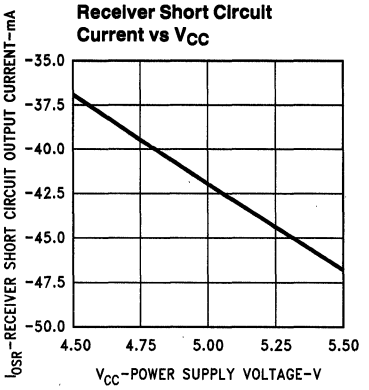
TL/F/8511–35

Receiver Short Circuit Current vs Temperature



TL/F/8511–36

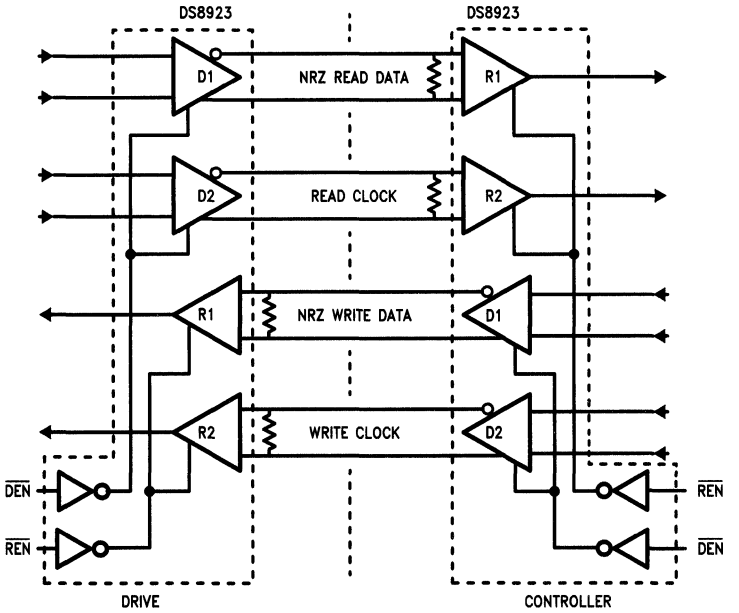
Receiver Short Circuit Current vs V_{CC}



TL/F/8511–37

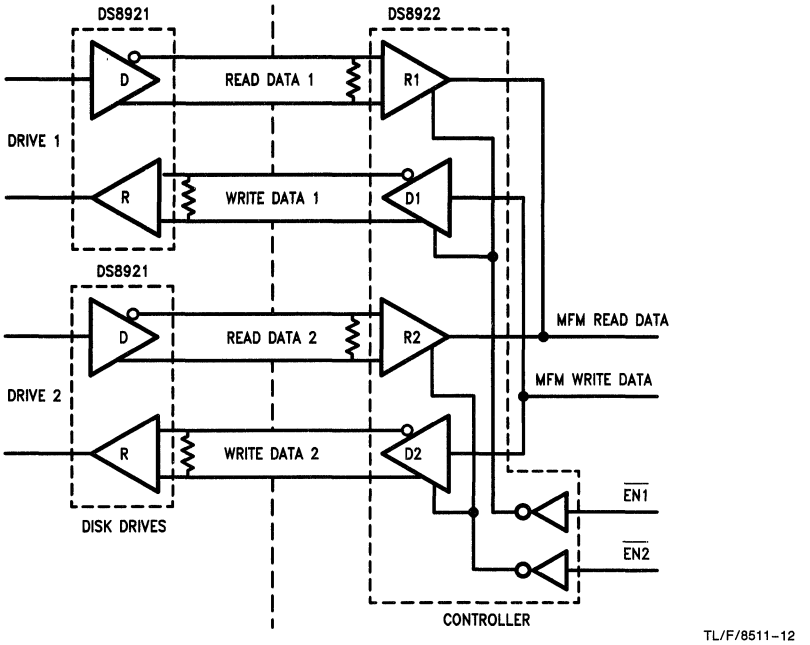
Typical Applications

ESDI Application



TL/F/8511–11

ST504 and ST412 Applications



TL/F/8511–12

National Semiconductor

DS8925
LocalTalk™ Dual Driver/Triple Receiver

General Description

The DS8925 is a dual driver/triple receiver device optimized to provide a single chip solution for a LocalTalk Interface. The device provides one differential TIA/EIA-422 driver, one TIA/EIA-423 single ended driver, one TIA/EIA-422 receiver and two TIA/EIA-423 receivers, all in a surface mount 16 pin package. This device is electrically similar to the 26LS30 and 26LS32 devices.

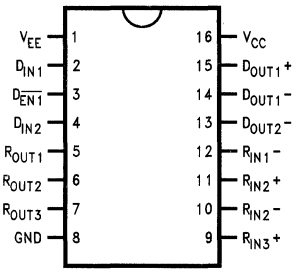
The drivers feature ±10V common mode range, and the differential driver provides TRI-STATEable outputs. The receivers offer ±200 mV thresholds over the ±10V common mode range.

Features

- Single chip solution for LocalTalk port
- Two driver/three receivers per package
- Wide common mode range: ±10V
- ±200 mV receiver sensitivity
- 70 mV typical receiver input hysteresis
- Available in SOIC packaging

Connection Diagram

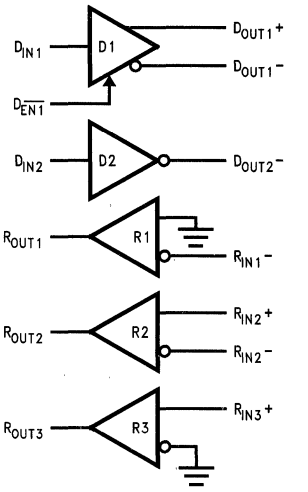
Dual-In-Line Package



TL/F/11895–1

Order Number DS8925M
See NS Package Number M16A

Functional Diagram



TL/F/11895–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V_{EE})	−7V
Enable Input Voltage ($D_{\overline{EN1}}$)	+7V
Driver Input Voltage (D_{IN})	+7V
Driver Output Voltage (Power Off: D_{OUT})	±15V
Receiver Input Voltage (V_{ID}: $R_{IN}+ - R_{IN}-$)	±25V
Receiver Input Voltage (V_{CM}: ($R_{IN}+ + R_{IN}-$)/2)	±25V
Receiver Input Voltage (Input to GND: R_{IN})	±25V
Receiver Output Voltage (R_{OUT})	+5.5V

Maximum Package Power Dissipation @ +25°C	
M Package	1.33W
Derate M Package 10.6 mW/°C above +25°C	
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 Sec.)	+260°C
This Device Does Not Meet 2000V ESD Rating	(Note 7)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V_{EE})	−4.75	−5.0	−5.25	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD}	Output Differential Voltage	$R_L = \infty$ or $R_L = 3.9\ k\Omega$		$D_{OUT}+$, $D_{OUT}-$	±7	±9.0	±10	V
V_O	Output Voltage	$R_L = \infty$ or $R_L = 3.9\ k\Omega$				±4.5	±5.25	V
V_{OD1}	Output Differential Voltage	$R_L = 100\Omega$, *Figure 1*			4.0	6.4		|V|
V_{SS}	$\|V_{OD1} - V_{OD1*}\|$				8.0	12.8		|V|
ΔV_{OD1}	Output Unbalance					0.02	0.4	V
V_{OS}	Offset Voltage					0	3	V
ΔV_{OS}	Offset Unbalance					0.05	0.4	V
V_{OD2}	Output Differential Voltage	RL = 140Ω, *Figure 1*			6.0	7.0		|V|
I_{OZD}	TRI-STATE® Leakage Current	V_{CC} = 5.25V, V_{EE} = −5.25V	V_O = +10V			2	150	μA
			V_O = +6V			1	100	μA
			V_O = −6V			−1	−100	μA
			V_O = −10V			−2	−150	μA
SINGLE ENDED DRIVER CHARACTERISTICS								
V_O	Output Voltage (No Load)	$R_L = \infty$ or $R_L = 3.9\ k\Omega$, *Figure 2*		$D_{OUT}-$	4	4.4	6	|V|
V_T	Output Voltage	$R_L = 3\ k\Omega$, *Figure 2*			3.7	4.3		|V|
		$R_L = 450\Omega$, *Figure 2*			3.6	4.1		|V|
ΔV_T	Output Unbalance					0.02	0.4	V
DRIVER CHARACTERISTICS								
V_{CM}	Common Mode Range	Power Off, or D1 Disabled		$D_{OUT}+$, $D_{OUT}-$	±10			V
I_{OSD}	Short Circuit Current	V_O = 0V, Sourcing Current				−80	−150	mA
		V_O = 0V, Sinking Current				80	150	mA
I_{OXD}	Power-Off Leakage Current ($V_{CC} = V_{EE} = 0V$)	V_O = +10V				2	150	μA
		V_O = +6V				1	100	μA
		V_O = −6V				−1	−100	μA
		V_O = −10V				−2	−150	μA

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS							
V_{TH}	Input Threshold	$-7V \le V_{CM} \le +7V$	$R_{IN}+$, $R_{IN}-$	−200	±35	+200	mV
V_{HY}	Hysteresis	$V_{CM} = 0V$			70		mV
R_{IN}	Input Resistance	$-10V \le V_{CM} \le +10V$		6.0	8.5		kΩ
I_{IN}	Input Current (Other Input = 0V, Power On, or $V_{CC} = V_{EE} = 0V$)	$V_{IN} = +10V$				3.25	mA
		$V_{IN} = +3V$		0		1.50	mA
		$V_{IN} = -3V$		0		−1.50	mA
		$V_{IN} = -10V$				−3.25	mA
V_{IB}	Input Balance Test	$R_S = 500\Omega$ (R2 only)				±400	mV
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$, $V_{IN} = +200$ mV	R_{OUT}	2.7	4.2		V
		$I_{OH} = -400\ \mu A$, V_{IN} = OPEN		2.7	4.2		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 8.0$ mA, $V_{IN} = -200$ mV			0.3	0.5	V
I_{OSR}	Short Circuit Current	$V_O = 0V$		−15	−34	−85	mA
DEVICE CHARACTERISTICS							
V_{IH}	High Level Input Voltage		D_{IN}, $\overline{D_{EN}}$	2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−10	−200	μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
I_{CC}	Power Supply Current	No Load, D1 Enabled or Disabled	V_{CC}		40	65	mA
I_{EE}			V_{EE}		−5	−15	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 500$ pF, (*Figures 3* and *4*) $C_1 = C_2 = 50$ pF	70	134	350	ns
t_{PLHD}	Differential Propagation Delay Low to High		70	141	350	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			7	50	ns
t_r	Rise Time		50	140	300	ns
t_f	Fall Time		50	140	300	ns
t_{PHZ}	Disable Time High to Z	$R_L = 100\Omega$, $C_L = 500$ pF (*Figures 7* and *8*)		300	600	ns
t_{PLZ}	Disable Time Low to Z			300	600	ns
t_{PZH}	Enable Time Z to High			160	350	ns
t_{PZL}	Enable Time Z to Low			160	350	ns
SINGLE ENDED DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 450\Omega$, $C_L = 500$ pF (*Figures 5* and *6*)	70	120	350	ns
t_{PLH}	Propagation Delay Low to High		70	150	350	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			30	70	ns
t_r	Rise Time		50	100	300	ns
t_f	Fall Time		20	50	300	ns
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$C_L = 15$ pF (*Figures 9* and *10*)	10	33	75	ns
t_{PLH}	Propagation Delay Low to High		10	30	75	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			3	20	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}, V_{OD1}, V_{OD2}, and V_{SS}.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $V_{EE} = -5.0V$, $T_A = +25°C$ unless otherwise specified.

Truth Tables

Driver (D1)

Inputs		Outputs	
$D_{\overline{EN1}}$	D_{IN1}	$D_{OUT1}+$	$D_{OUT1}-$
H	X	Z	Z
L	L	L	H
L	H	H	L

Driver (D2)

Input	Output
D_{IN2}	$D_{OUT2}-$
L	H
H	L

H = Logic High Level (Steady State)
L = Logic Low Level (Steady State)
X = Irrelevant (Any Input)
Z = Off State (TRI-STATE, High Impedance)
†OPEN = Non-Terminated

Receiver (1)

Input	Output
$R_{IN1}-$	R_{OUT1}
≤ −200 mV	H
≥ +200 mV	L
OPEN†	H

Receiver (2)

Inputs	Output
$R_{IN2}+ - R_{IN2}-$	R_{OUT2}
≤ −200 mV	L
≥ +200 mV	H
OPEN†	H

Receiver (3)

Input	Output
$R_{IN3}+$	R_{OUT3}
≤ −200 mV	L
≥ +200 mV	H
OPEN†	H

Parameter Measurement Information

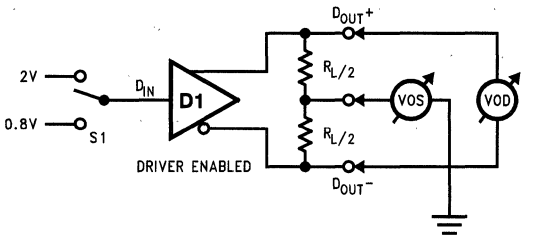


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FIGURE 1. Differential Driver DC Test Circuit

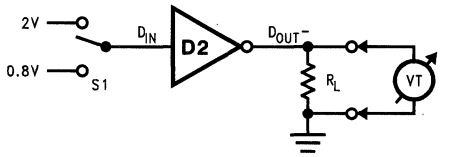

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FIGURE 2. Single Ended Driver DC Test Circuit

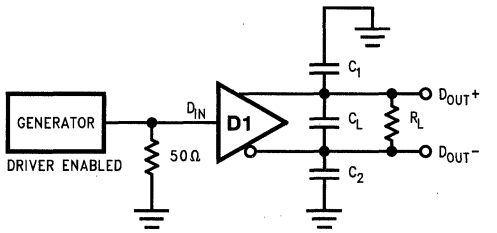

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FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit

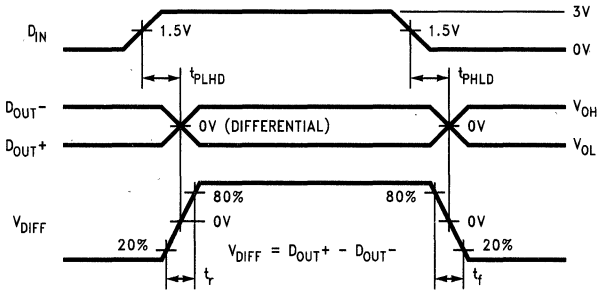

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FIGURE 4. Differential Driver Propagation Delay and Transition Time Waveforms

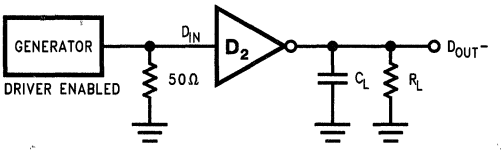

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FIGURE 5. Single Ended Driver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)

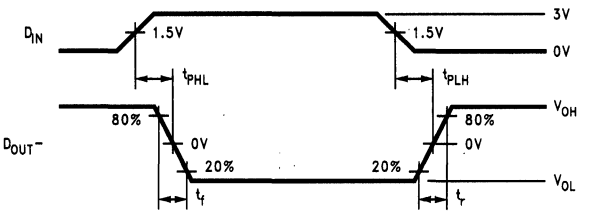

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FIGURE 6. Single Ended Driver Propagation Delay and Transition Time Waveform

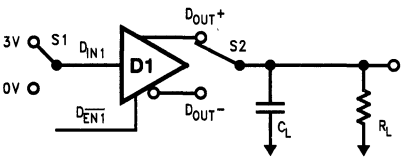

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FIGURE 7. Differential Driver TRI-STATE Test Circuit

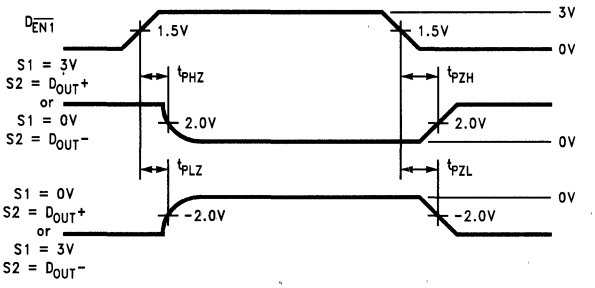

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FIGURE 8. Differential Driver TRI-STATE Waveforms

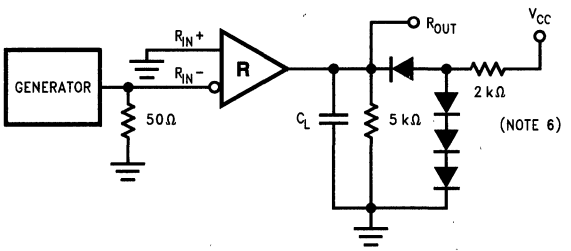

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FIGURE 9. Receiver Propagation Delay Test Circuit

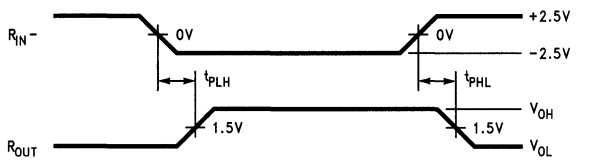

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FIGURE 10. Receiver Propagation Delay Waveform

Note 4: Generator waveform for all tests unless otherwise specified: f = 500 kHz, Z_O = 50Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: All diodes are 1N916 or equivalent.

Note 7: ESD Rating HBM (1.5 kΩ, 100 pF) pins 10, 12 ≥ 1500V, all other pins ≥ 2000V.

Typical Application Information

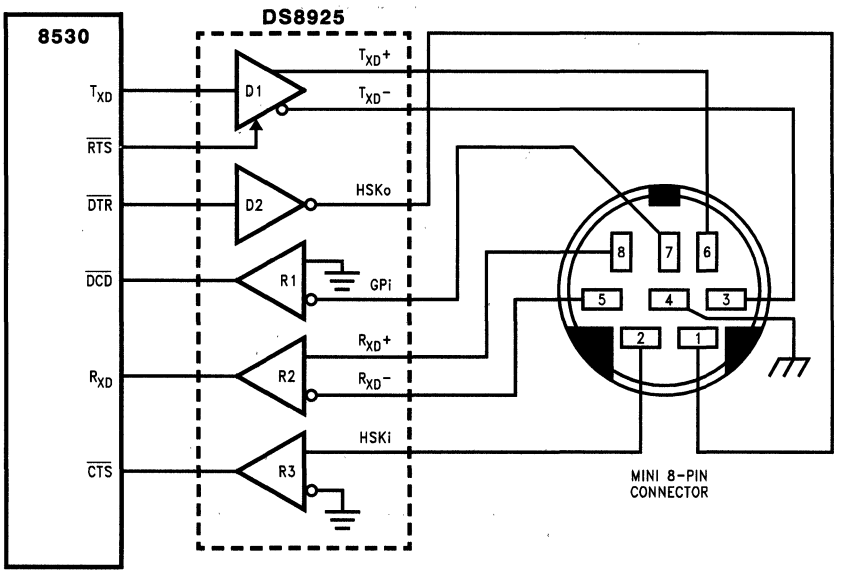

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FIGURE 11. Typical LocalTalk Application

TABLE I. Device Pin Descriptions

Pin #	Name	Description
2, 4	D_{IN}	TTL Driver Input Pins
3	$D_{\overline{ENT}}$	Active Low Driver Enable Pin. A High on this Pin TRI-STATES the Driver Outputs (D1 Only)
15	$D_{OUT}+$	Non-Inverting Driver Output Pin
13, 14	$D_{OUT}-$	Inverting Driver Output Pin
9, 11	$R_{IN}+$	Non-Inverting Receiver Input Pin
10, 12	$R_{IN}-$	Inverting Receiver Input Pin
5, 6, 7	R_{OUT}	Receiver Output Pin
8	GND	Ground Pin
1	V_{EE}	Negative Power Supply Pin, −5V ±5%
16	V_{CC}	Positive Power Supply Pin, +5V ±5%

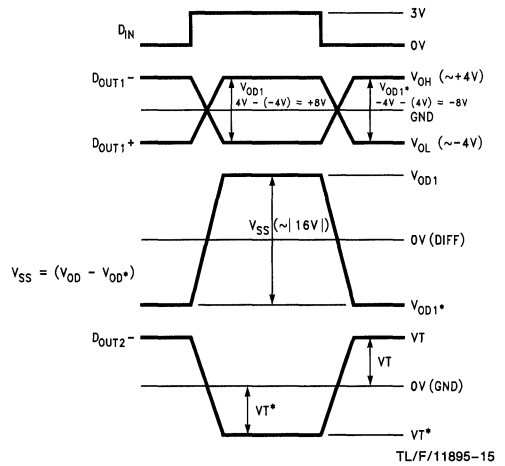
Typical Application Information (Continued)

DRIVER OUTPUT WAVEFORMS

The driver configuration on the DS8925 is unique among TIA/EIA-422 devices in that it utilizes −5V V_{EE} supply. A typical TIA/EIA-422 driver uses +5V only and generates signal swings of approximately 0V–5V.

By utilizing V_{EE}, the differential driver is able to generate a much larger differential signal. The typical output voltage is about |4| V, which gives |8| V differentially, thus providing a much greater noise margin than +5V drivers. See *Figure 12*. The receiver therefore has a range of +8V to −8V or V_{SS} of 16V ($V_{SS} = V_{OD}-V_{OD*}$).

Each side of the differential driver operates similar to a TIA/EIA-423 driver. The output voltages are slightly different due to the loading: the differential driver has differential termination, the single-ended driver is terminated with a resistor to ground.



Note: Star (*) represents the opposite input condition for a parameter.

FIGURE 12. Typical Driver Output Waveforms

UNUSED PINS

Unused driver outputs should be left open. If tied to either ground or supply, the driver may enter an I_{OS} state and consume excessive power. Unused driver inputs should not be left floating as this may lead to unwanted switching which may affect I_{CC}, particularly the frequency component. Unused driver inputs should be tied to ground.

Receiver outputs will be in a HIGH state when inputs are open; therefore, outputs should not be tied to ground. It is best to leave unused receiver outputs floating.

RECEIVER FAILSAFE

All three receivers on this device incorporate open input failsafe protection. The differential receiver output will be in a HIGH state when inputs are open, but will be indetermined if inputs are shorted together. Unused differential inputs should be left floating.

Both single-ended receivers (inverting and non-inverting) are biased internally so that an open input will result in a HIGH output. Therefore, these inputs should not be shorted to ground when unused.

BYPASS CAPACITORS

Bypass capacitors are recommended for both V_{CC} and V_{EE}. Noise induced on the supply lines can affect the signal quality of the output; V_{CC} affects the V_{OH} and V_{EE} affects the V_{OL}. Capacitors help reduce the effect on signal quality. A value of 0.1 μF is typically used.

Since this is a power device, it is recommended to use a bypass capacitor for each supply and for each device. Sharing a bypass capacitor between other devices may not be sufficient.

TERMINATION

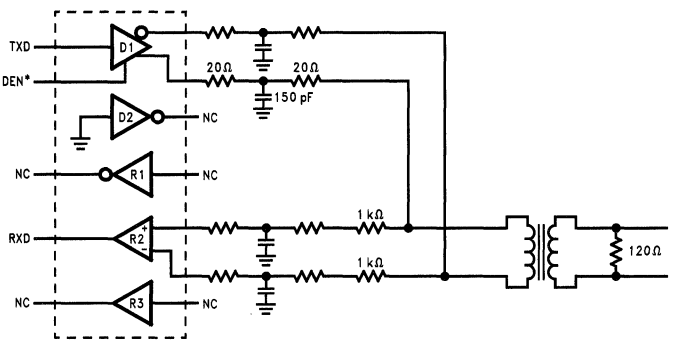
On a multi-point transmission line which is electrically long, it is advisable to terminate the line at both ends with its characteristic impedance to prevent signal reflection and its associated noise/crosstalk.

A 100Ω termination resistor is commonly specified by TIA/EIA-422 for differential signals. The DS8925 is also specified using 140Ω termination which will result in less power associated with the driver output. The additional resistance is typical of applications requiring EMI filtering on the driver outputs.

TWO-WIRE LocalTalk

The DS8925 is a single chip solution for a LocalTalk interface. A typical application is shown in *Figure 11*.

An alternative implementation of LocalTalk is to only use two wires to communicate. The differential data lines can be transformer-coupled on to a twisted pair medium. See *Figure 13*. The handshake function must then be accomplished in software.



Note: Star (*) represents the opposite input condition for a parameter.

FIGURE 13. Differential Communication, Transformer-Coupled to a Twisted-Pair Line

Typical Application Information (Continued)

SINGLE +5V SUPPLY

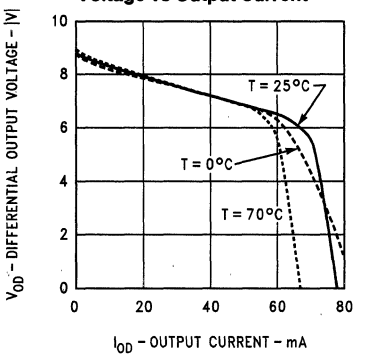
The DS8925 is derived from the DS3691/92 which could be configured using a single +5V supply (V_{EE} = 0V). This device is not specified for this type of operation. However, the device will not be damaged if operated using a single +5V supply.

Both drivers require the −5V supply in order to meet the output voltage levels specified. When the device switches from a positive voltage to the complimentary state, it is pulled toward the V_{EE} level. If that level is 0V, then the complimentary state will be near 0V instead of V_{EE}. Thus, the output would switch from about 4V to 0V, instead of 4V to −4V. The differential driver will meet TIA/EIA-422, but with a reduced noise margin. The single-ended driver will not meet TIA/EIA-423 without the −5V supply.

The receivers will be functional but may suffer parametrically. The inverting receiver is referenced to V_{EE} therefore, the threshold may shift slightly. The inputs can still vary over the ±10V common mode range.

Typical Performance Characteristics*

Differential Driver Output Voltage vs Output Current



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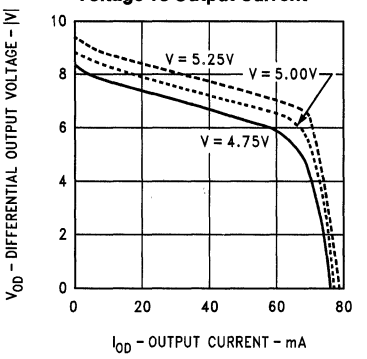
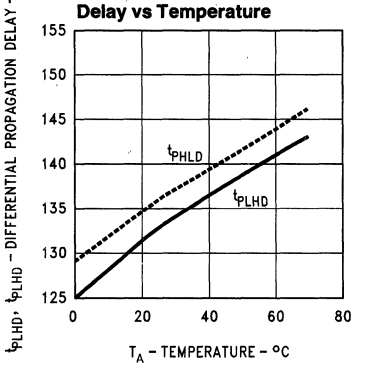
Differential Driver Output Voltage vs Output Current



TL/F/11895–18

Differential Driver Propagation Delay vs Temperature



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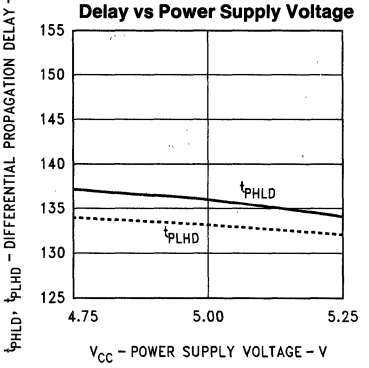
Differential Driver Propagation Delay vs Power Supply Voltage



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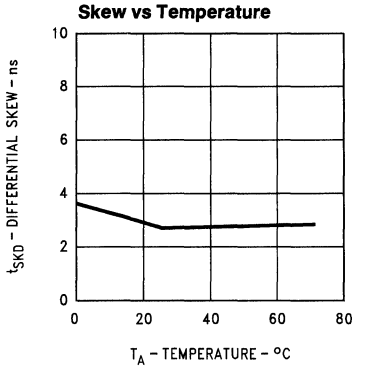
*V defined as $V_{CC} = |V_{EE}|$

Typical Performance Characteristics* (Continued)

Differential Driver Skew vs Temperature



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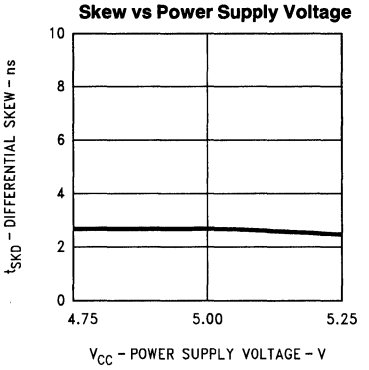
Differential Driver Skew vs Power Supply Voltage



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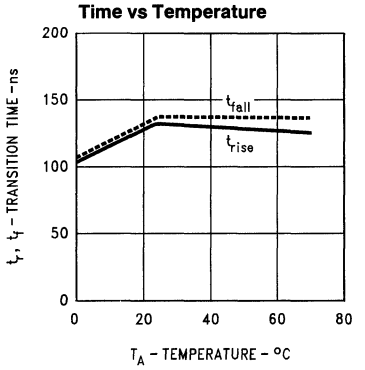
Differential Transition Time vs Temperature



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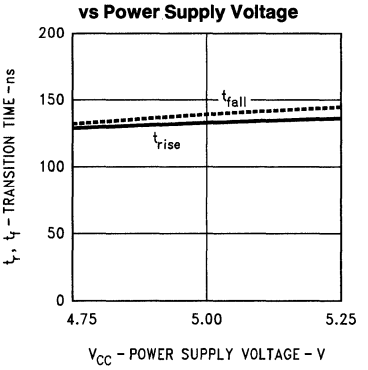
Differential Transition Time vs Power Supply Voltage



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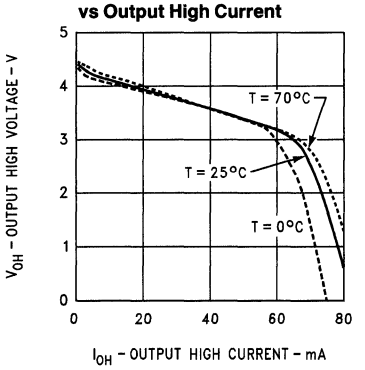
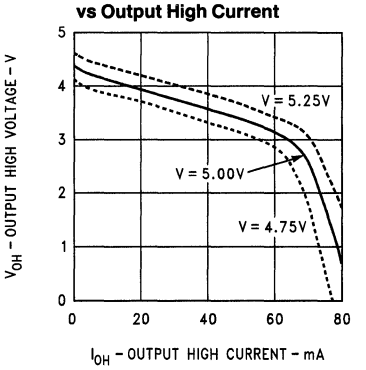
Driver Output High Voltage vs Output High Current



TL/F/11895–25

Driver Output High Voltage vs Output High Current

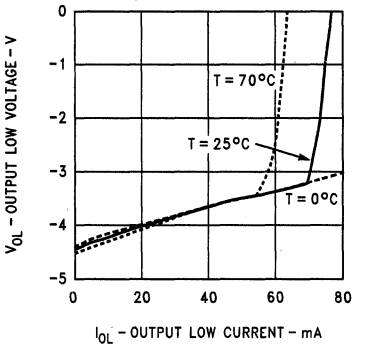


TL/F/11895–26

*V defined as $V_{CC} = |V_{EE}|$

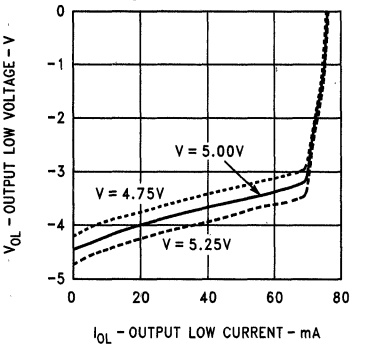
Typical Performance Characteristics* (Continued)

Driver Output Low Voltage vs Output Low Current



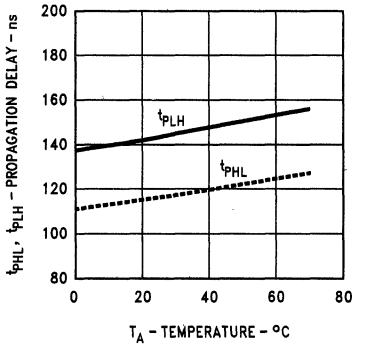
TL/F/11895–27

Driver Output Low Voltage vs Output Low Current



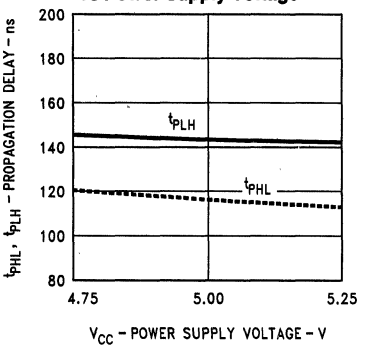
TL/F/11895–28

Driver Propagation Delay vs Temperature



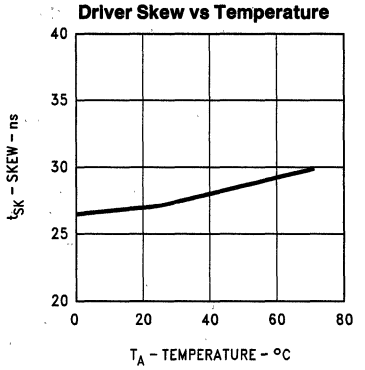
TL/F/11895–29

Driver Propagation Delay vs Power Supply Voltage



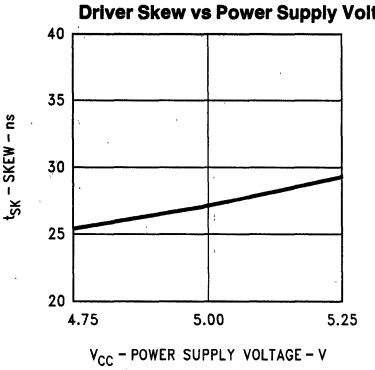
TL/F/11895–30

Driver Skew vs Temperature



TL/F/11895–31

Driver Skew vs Power Supply Voltage

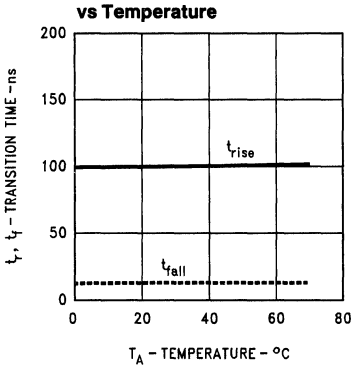


TL/F/11895–32

*V defined as $V_{CC} = |V_{EE}|$

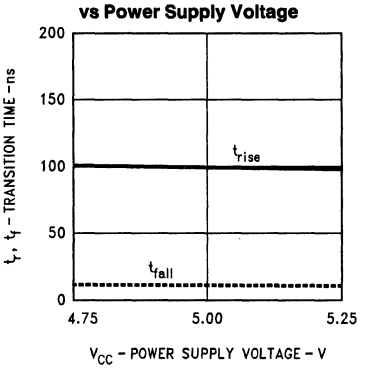
Typical Performance Characteristics* (Continued)

Driver Transition Time vs Temperature



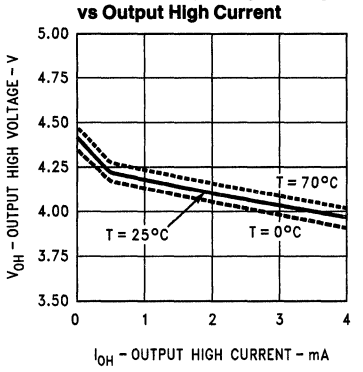
TL/F/11895–33

Driver Transition Time vs Power Supply Voltage



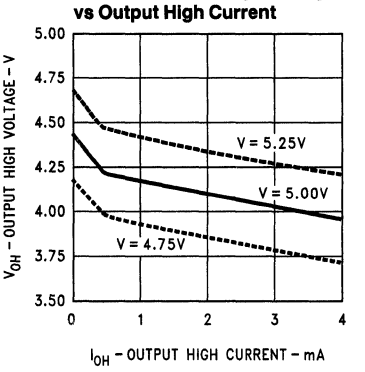
TL/F/11895–34

Receiver Output High Voltage vs Output High Current



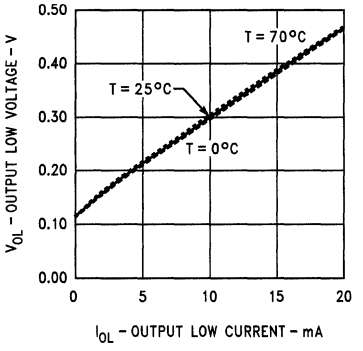
TL/F/11895–35

Receiver Output High Voltage vs Output High Current



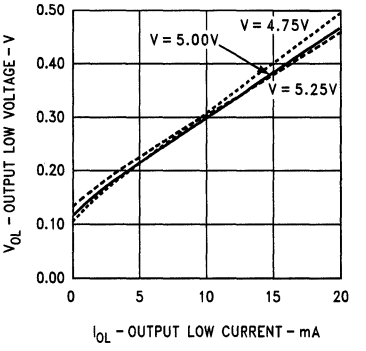
TL/F/11895–36

Receiver Output Low Voltage vs Output Low Current



TL/F/11895–37

Receiver Output Low Voltage vs Output Low Current

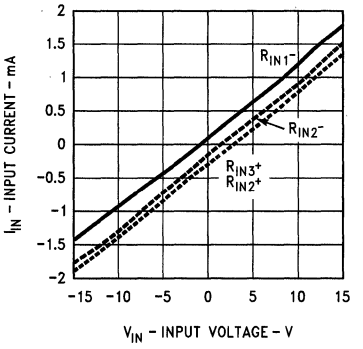


TL/F/11895–38

*V defined as $V_{CC} = |V_{EE}|$

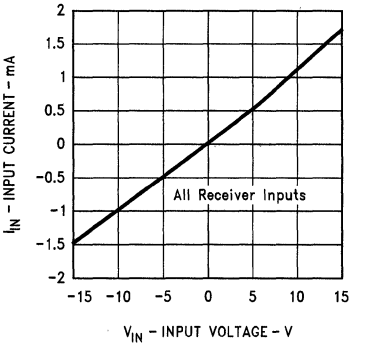
Typical Performance Characteristics* (Continued)

Receiver Input Current vs Input Voltage (Power On)



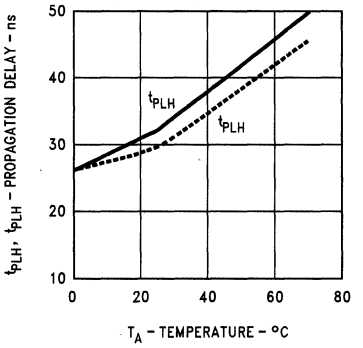
TL/F/11895–39

Receiver Input Current vs Input Voltage (Power Off)



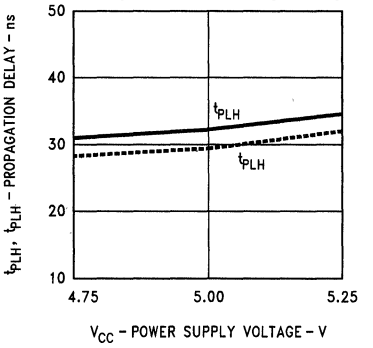
TL/F/11895–40

Receiver Output Propagation Delay vs Temperature



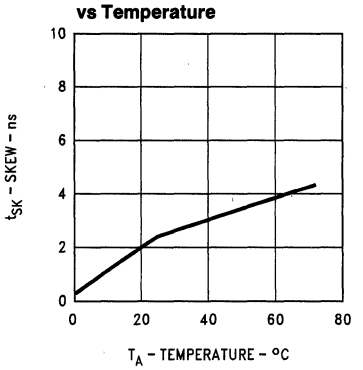
TL/F/11895–41

Receiver Output Propagation Delay vs Power Supply Voltage



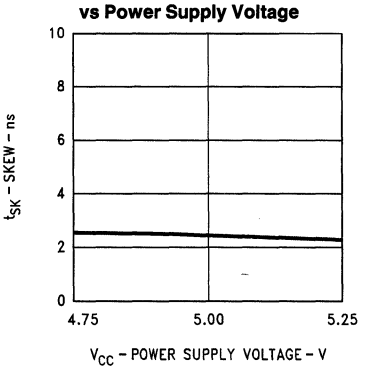
TL/F/11895–42

Receiver Output Skew vs Temperature



TL/F/11895–43

Receiver Output Skew vs Power Supply Voltage

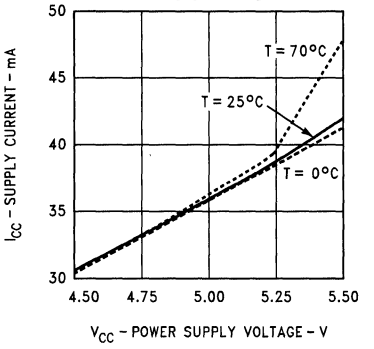


TL/F/11895–44

*V defined as $V_{CC} = |V_{EE}|$

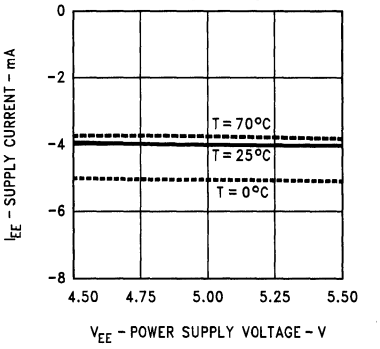
Typical Performance Characteristics* (Continued)

Supply Current vs Power Supply Voltage



TL/F/11895–45

Supply Current vs Power Supply Voltage



TL/F/11895–46

*V defined as $V_{CC} = |V_{EE}|$

National Semiconductor

ADVANCE INFORMATION

DS8926
LocalTalk™ Dual Driver/Triple Receiver

General Description

The DS8926 is a dual driver/triple receiver device optimized to provide a single chip solution for a LocalTalk Interface. The device provides one differential TIA/EIA-422 driver, one TIA/EIA-423 single ended driver, one TIA/EIA-422 receiver and two TIA/EIA-423 receivers, all in a surface mount 16 pin package. This device is electrically similar to the 26LS30 and 26LS32 devices and is a direct replacement for the DS8925.

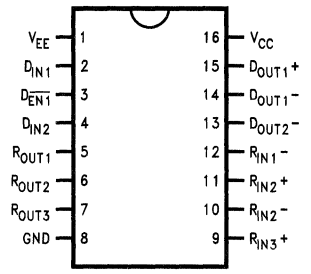
The drivers feature ±10V common mode range, and the differential driver provides TRI-STATEable® outputs. The receivers offer ±200 mV thresholds over the ±10V common mode range.

Features

- Single chip solution for LocalTalk port
- Two driver/three receivers per package
- Fast rise/fall times and propagation delay on receivers
- Wide common mode range: ±10V
- ±200 mV receiver sensitivity
- 70 mV typical receiver input hysteresis
- Available in SOIC packaging

Connection Diagram

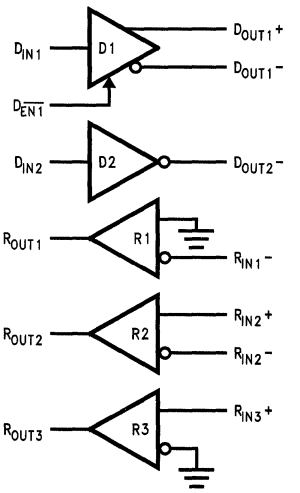
Dual-In-Line Package



TL/F/12646–1

Order Number DS8926M
See NS Package Number M16A

Functional Diagram



TL/F/12646–2

National Semiconductor

DS8933
V.34 Serial Port 2 X 1 Driver/Receiver

General Description

The DS8933 is a 2 driver X 1 receiver device optimized to provide a two chip solution for a synchronous V.FAST (V.34) modem serial port when used with the DS8934 5 driver X 3 receiver device. The TIA/EIA-423-B (V.10) single-ended drivers are compatible with EIA/TIA-232-E (V.28) receivers, and the receivers are compatible with TIA/EIA-423-B (V.10) and EIA/TIA-232-E (V.28) drivers.

The drivers provide a minimum output voltage of ±3.6V, while the receivers offer a +1.4V threshold, a failsafe output state, and an input range of ±10V minimum.

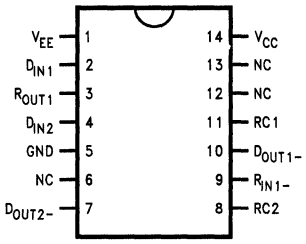
Both the drivers and the receivers provide an inverting logic function and the drivers are electrically similar to the industry standard 26LS30 (3691) devices. The device is available in a surface mount 14-pin package.

Features

- Dual chip solution for V.34 sync. modem serial port when used with complementary DS8934
- Conforms to industry standards:
  TIA/EIA-423-B.1994 (RS-423)
  ITU-T V.10 (formerly CCITT)
- Compatible with EIA/TIA-232-E (RS-232) and ITU-T V.28 (formerly CCITT) drivers and receivers
- Adjustable driver slew rate reduces noise generation
- Operates above 1 Mbps
- Wide receiver input voltage range - ±10V
- +1.4V receiver threshold with hysteresis
- Failsafe receivers: output high for open input
- Available in SOIC packaging

Connection Diagram

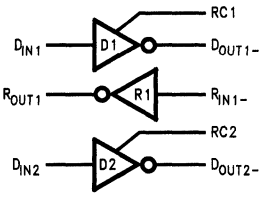
Dual-In-Line



TL/F/12374–1

Order Number DS8933M
See NS Package Number M14A

Functional Diagram



TL/F/12374–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V_{EE})	−7V
Driver Input Voltage (D_{IN})	+7V
Driver Output Voltage (Power Off: D_{OUT})	±15V
Receiver Input Voltage (Input to GND: R_{IN})	±25V
Receiver Output Voltage (R_{OUT})	+5.5V
Maximum Package Power Dissipation @ +25°C M Package	1.5W
Derate M Package 12.2 mW/°C above +25°C	
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 Sec.)	+260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	>2 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V_{EE})	−4.75	−5.0	−5.25	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_O	Output Voltage	$R_L = \infty$ or R_L = 3.9 kΩ, *Figure 1*	D_{OUT}-		4.4	6	|V|
V_T	Output Voltage	R_L = 3 kΩ, *Figure 1*		3.7	4.3		|V|
		R_L = 450Ω, *Figure 1*		3.6	4.1		|V|
ΔV_T	Output Unbalance				0.1	0.4	V
I_{OSD}	Short Circuit Current	V_O = 0V, Sourcing Current			−100	−150	mA
		V_O = 0V, Sinking Current			80	150	mA
I_{OXD}	Power-Off Leakage Current ($V_{CC} = V_{EE}$ = 0V)	V_O = +10V			1	150	µA
		V_O = +6V			1	100	µA
		V_O = −6V			−1	−100	µA
		V_O = −10V			−1	−150	µA
V_{CM}	Common Mode Range	Power-Off		±10			V
V_{IH}	High Level Input Voltage		D_{IN}	2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−3	−200	µA
V_{CL}	Input Clamp Voltage	I_{IN} = −12 mA			−0.7	−1.5	V
RECEIVER CHARACTERISTICS							
V_{T-}	Negative-Going Threshold Voltage	(See *Figure 7*)	R_{IN}-	0.9	1.36		V
V_{T+}	Positive-Going Threshold Voltage				1.4	1.7	V
V_{HY}	Hysteresis				40		mV
R_{IN}	Input Resistance	−10V ≤ V_{IN} ≤ +10V		4.0	6.0	8.0	kΩ
I_{IN}	Input Current (Power On, or Power Off— $V_{CC} = V_{EE}$ = 0V)	V_{IN} = +10V			1.6	3.25	mA
		V_{IN} = +3V		0	0.38	1.50	mA
		V_{IN} = −3V		0	−0.67	−1.50	mA
		V_{IN} = −10V			−1.9	−3.25	mA
V_{OH}	High Level Output Voltage	I_{OH} = −400 µA, V_{IN} −3V	R_{OUT}	3.5	4.2		V
		I_{OH} = −400 µA, V_{IN} OPEN		3.5	4.2		V
V_{OL}	Low Level Output Voltage	I_{OL} = 8.0 mA, V_{IN} = +3V			0.3	0.5	V
I_{OSR}	Short Circuit Current	V_O = 0V		−15	−35	−85	mA

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
I_{CC}	Power Supply Current	No Load	V_{CC}		20	30	mA
I_{EE}	Power Supply Current		V_{EE}		−5	−10	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 450\Omega$, $C_L = 50$ pF, C_C = Open (*Figures 2* and *3*)	40	160	300	ns
t_{PLH}	Propagation Delay Low to High		40	120	300	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$		0	40	150	ns
t_{tcc}	Transition Time Coefficient	$t_{tcc}(C_C) = t_t$, where $t_t = t_r$ or t_f		54		ns/pF
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 50$ pF, C_C = Open (*Figures 2 and 3*)		100	250	ns
t_f	Fall Time			50	250	ns
t_r	Rise Time	$R_L = 3$ kΩ, $C_L = 2{,}500$ pF, $C_C = 5$ pF (*Figures 2* and *3*) Maximum Load (V.28/232)		275	475	ns
t_f	Fall Time			275	475	ns
SR	Slew Rate (±3V)		12.6	21		V/μs
t_r	Rise Time	$R_L = 3$ kΩ, $C_L = 2{,}500$ pF, $C_C = 15$ pF (*Figures 2* and *3*) Maximum Load (V.28/232)		800		ns
t_f	Fall Time			800		ns
SR	Slew Rate (±3V)			7		V/μs
t_r	Rise Time	$R_L = 7$ kΩ, $C_L = 50$ pF, $C_C = 15$ pF (*Figures 2* and *3*) Maximum Load (V.28/232)		800		ns
t_f	Fall Time			800		ns
SR	Slew Rate (±3V)			7		V/μs
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$C_L = 15$ pF (*Figures 4* and *5*)	10	29	75	ns
t_{PLH}	Propagation Delay Low to High		10	26	75	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$		0	3	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.

Note 3: All typicals are given for: $V_{CC} = +5.0$V, $V_{EE} = -5.0$V, $T_A = +25°C$ unless otherwise specified. Typical AC numbers are rounded off. Measurements of the driver with a response control capacitor connected may vary due to tolerance of the capacitor, the use of surface mount components is recommended.

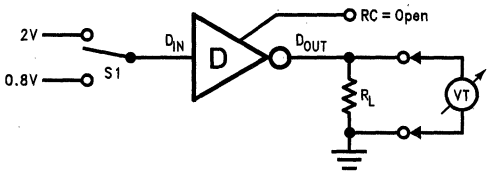
Note 4: Generator waveform for all tests unless otherwise specified: f = 500 kHz, $Z_O = 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: All diodes are 1N916 or equivalent.

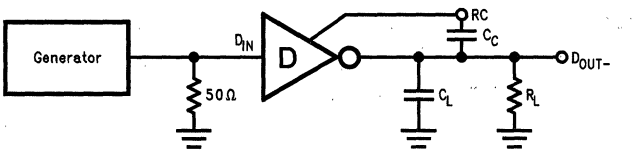
Note 7: ESD rating HBM (1.5 kΩ, 100 pF) ≥ 2 kV.

Parameter Measurement Information



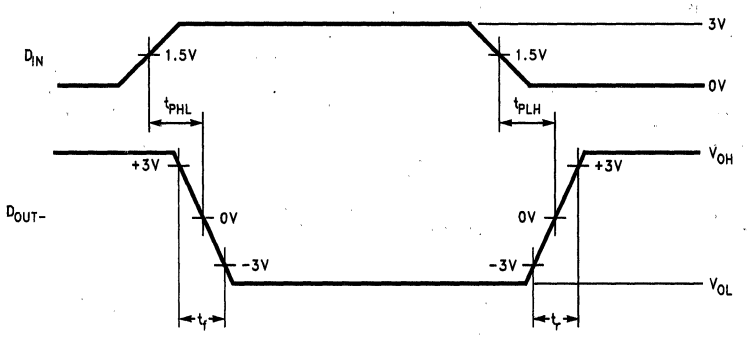
TL/F/12374–3

FIGURE 1. Driver DC Test Circuit



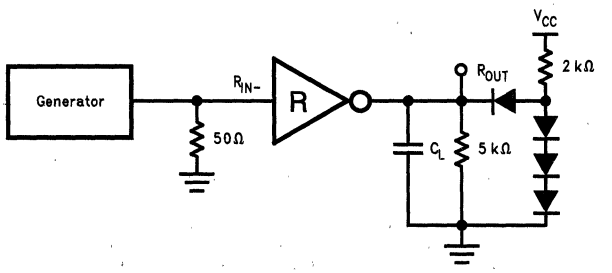
TL/F/12374–4

FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit



TL/F/12374–5

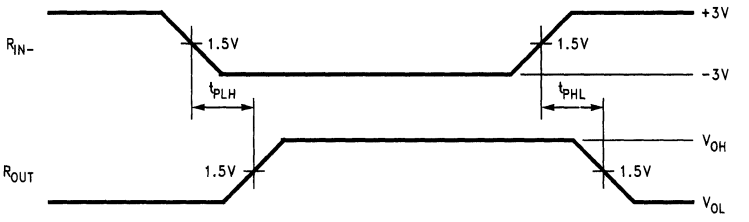
FIGURE 3. Driver Propagation Delay and Transition Time Waveform



TL/F/12374–6

FIGURE 4. Receiver Propagation Delay Test Circuit (Note 6)

Parameter Measurement Information (Continued)



TL/F/12374–7

FIGURE 5. Receiver Propagation Delay Waveform

Pin Descriptions

Pin #	Name	Description
2, 4	D_{IN}	TTL Driver Input Pins
7, 10	D_{OUT-}	Inverting Driver Output Pin
8, 11	RC	Driver Response Control Pin
9	R_{IN-}	Inverting Receiver Input Pin
3	R_{OUT}	Receiver Output Pin
5	GND	Ground Pin
1	V_{EE}	Negative Power Supply Pin, −5V ±5%
14	V_{CC}	Positive Power Supply Pin, +5V ±5%

Truth Tables

Driver (D1, D2)

Input D_{IN}	Output D_{OUT-}
L	H
H	L

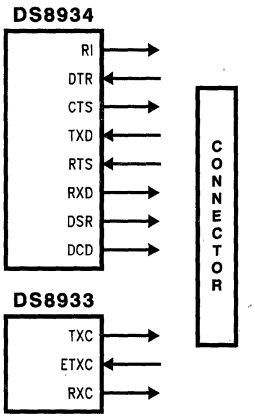
H = Logic high level (steady state)
L = Logic low level (steady state)

Receiver (R1)

Input R_{IN-}	Output R_{OUT}
≤ +0.9V	H
≥ +1.7V	L
OPEN†	H

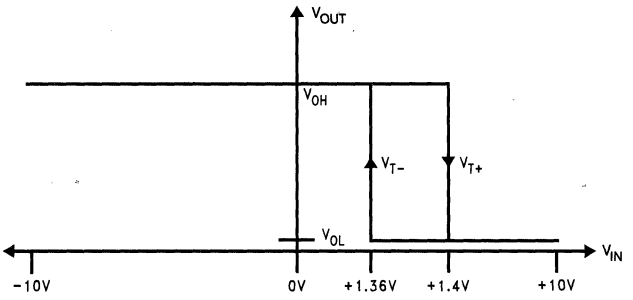
†OPEN = Non-terminated

Typical Application Information



TL/F/12374–11

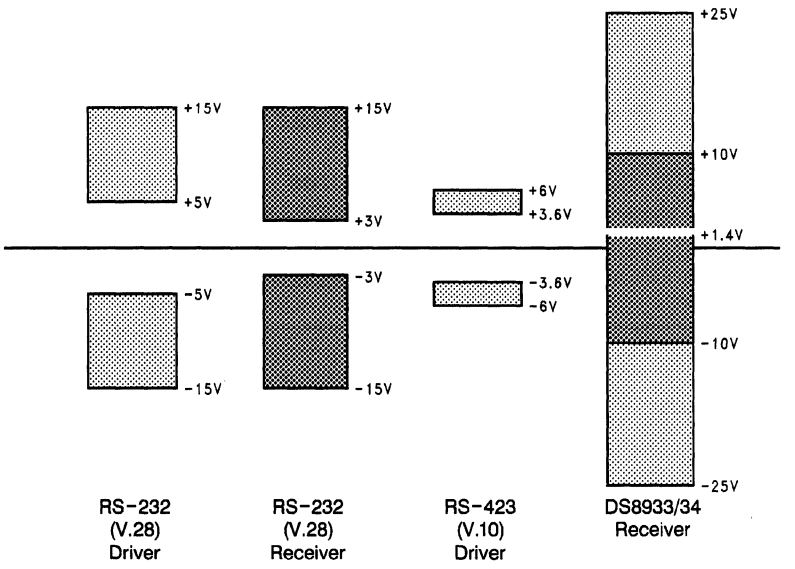
FIGURE 6. Typical V.34 Sync. Application



TL/F/12374–8

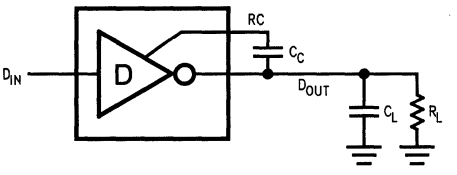
FIGURE 7. Receiver Threshold Voltage Transfer Curve (VTC)

Typical Application Information (Continued)



TL/F/12374–9

FIGURE 8. RS-423 and RS-232 Levels



TL/F/12374–10

FIGURE 9. External Slew Rate Control Capacitor Connection

National Semiconductor

DS8934
V.34 Serial Port 5 X 3 Driver/Receiver

General Description

The DS8934 is a 5 driver X 3 receiver device optimized to provide a single chip solution for an asynchronous V.34 (V.FAST) modem serial port. The TIA/EIA-423-B (V.10) single-ended drivers are compatible with EIA/TIA-232-E (V.28) receivers, and the receivers are compatible with TIA/EIA-423-B (V.10) and EIA/TIA-232-E (V.28) drivers.

The drivers provide a minimum output voltage of ±3.6V, while the receivers offer a +1.4V threshold, a failsafe output state, and an input range of ±10V minimum.

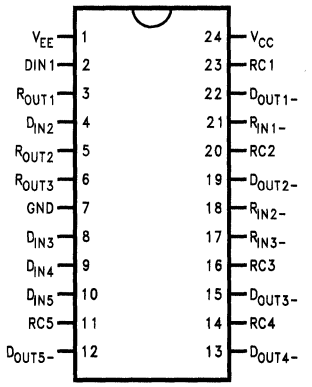
Both the drivers and the receivers provide an inverting logic function and the drivers are electrically similar to the industry standard 26LS30 (3691) devices. The pinout of the device maps the common DB-9 connector, and provides a straight through connection. The device is available in a surface mount 24-pin package.

Features

- Single chip solution for V.34 async. modem serial port
- Companion 2 X 1 DS8933 for dual chip sync. serial port
- Conforms to industry standards:
  TIA/EIA-423-B.1994 (RS-423)
  ITU-T V.10 (formerly CCITT)
- Compatible with EIA/TIA-232-E (RS-232) and ITU-T V.28 (formerly CCITT) drivers and receivers
- Adjustable driver slew rate reduces noise generation
- Operates above 1 Mbps
- Wide receiver input voltage range ±10V
- +1.4V receiver threshold with hysteresis
- Failsafe receivers: output high for open input
- Available in SOIC packaging

Connection Diagram

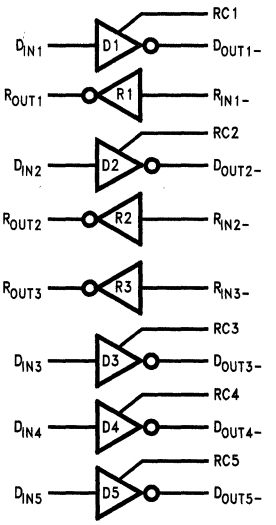
Dual-In-Line



TL/F/12373-1

Order Number DS8934WM
See NS Package Number M24B

Functional Diagram



TL/F/12373-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V_{EE})	−7V
Driver Input Voltage (D_{IN})	+7V
Driver Output Voltage (Power Off: D_{OUT})	±15V
Receiver Input Voltage (Input to GND: R_{IN})	±25V
Receiver Output Voltage (R_{OUT})	+5.5V
Maximum Package Power Dissipation @ +25°C WM Package	1.3W
Derate WM Package 10.7 mW/°C above +25°C	
Maximum Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. Range Soldering (4 sec.)	+260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	>2 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V_{EE})	−4.75	−5.0	−5.25	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_O	Output Voltage	$R_L = \infty$ or $R_L = 3.9\ k\Omega$, *Figure 1*	D_{OUT}-		4.4	6	|V|
V_T	Output Voltage	$R_L = 3\ k\Omega$, *Figure 1*		3.7	4.3		|V|
		$R_L = 450\Omega$, *Figure 1*		3.6	4.1		|V|
ΔV_T	Output Unbalance				0.1	0.4	V
I_{OSD}	Short Circuit Current	$V_O = 0V$, Sourcing Current			−100	−150	mA
		$V_O = 0V$, Sinking Current			80	150	mA
I_{OXD}	Power-off Leakage Current ($V_{CC} = V_{EE} = 0V$)	$V_O = +10V$			1	150	μA
		$V_O = +6V$			1	100	μA
		$V_O = -6V$			−1	−100	μA
		$V_O = -10V$			−1	−150	μA
V_{CM}	Common Mode Range	Power Off		±10			V
V_{IH}	High Level Input Voltage		D_{IN}	2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
I_{IH}	Low Level Input Current	$V_{IN} = 0.4V$			−3	−200	μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -12$ mA			−0.7	−1.5	V
RECEIVER CHARACTERISTICS							
V_{T-}	Negative-Going Threshold Voltage	(See *Figure 7*)	R_{IN}-	0.9	1.36		V
V_{T+}	Positive-Going Threshold Voltage				1.4	1.7	V
V_{HY}	Hysteresis				40		mV
R_{IN}	Input Resistance	$-10V \le V_{IN} \le +10V$		4.0	6.0	8.0	kΩ
I_{IN}	Input Current (Power on, or Power off − $V_{CC} = V_{EE} = 0V$)	$V_{IN} = +10V$			1.6	3.25	mA
		$V_{IN} = +3V$		0	0.38	1.50	mA
		$V_{IN} = -3V$		0	−0.67	−1.50	mA
		$V_{IN} = -10V$			−1.9	−3.25	mA
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$, V_{IN} −3V	R_{OUT}	3.5	4.2		V
		$I_{OH} = -400\ \mu A$, V_{IN} OPEN		3.5	4.2		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 8.0$ mA, $V_{IN} = +3V$			0.3	0.5	V
I_{OSR}	Short Circuit Current	$V_O = 0V$		−15	−35	−85	mA

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
I_{CC}	Power Supply Current	No Load	V_{CC}		46	65	mA
I_{EE}	Power Supply Current		V_{EE}		−10	−20	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 450\Omega$, $C_L = 50$ pF, C_C = Open (*Figures 2* and *3*)	40	175	300	ns
t_{PLH}	Propagation Delay Low to High		40	125	300	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$		0	50	150	ns
t_{tcc}	Transition Time Coefficient	($t_{tcc}(C_C) = t_t$, where $t_t = t_r$ or t_f)		54		ns/pF
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 50$ pF, C_C = Open (*Figures 2* and *3*)		100	250	ns
t_f	Fall Time			50	250	ns
t_r	Rise Time	$R_L = 3$ kΩ, $C_L = 2{,}500$ pF, $C_C = 5$ pF (*Figures 2* and *3*) Maximum Load (V.28/232)		275	475	ns
t_f	Fall Time			275	475	ns
SR	Slew Rate (±3V)		12.6	21		V/μs
t_r	Rise Time	$R_L = 3$ kΩ, $C_L = 2{,}500$ pF, $C_C = 15$ pF (*Figures 2* and *3*) Maximum Load (V.28/232)		800		ns
t_f	Fall Time			800		ns
SR	Slew Rate (±3V)			7		V/μs
t_r	Rise Time	$R_L = 7$ kΩ, $C_L = 50$ pF, $C_C = 15$ pF (*Figures 2* and *3*) Minimum Load (V.28/232)		800		ns
t_f	Fall Time			800		ns
SR	Slew Rate (±3V)			7		V/μs
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$C_L = 15$ pF (*Figures 4* and *5*)	10	29	75	ns
t_{PLH}	Propagation Delay Low to High		10	26	75	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$		0	3	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground.

Note 3: All typicals are given for: $V_{CC} = +5.0$V, $V_{EE} = -5.0$V, $T_A = +25°C$ unless otherwise specified. Typical AC numbers are rounded off. Measurements of the driver with a response control capacitor connected may vary due to tolerance of the capacitor, the use of surface mount components is recommended.

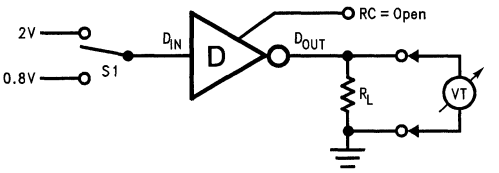
Note 4: Generator waveform for all tests unless otherwise specified: f = 500 kHz, $Z_O = 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: All diodes are 1N916 or equivalent.

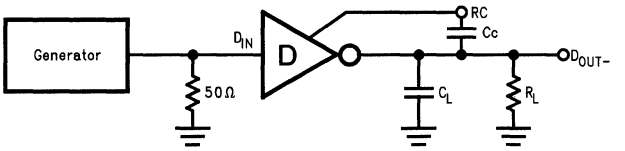
Note 7: ESD rating HBM (1.5 kΩ, 100 pF) ≥ 2 kV.

Parameter Measurement Information



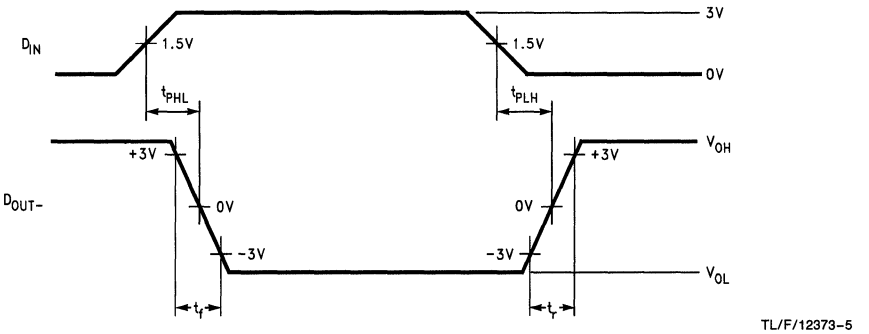
TL/F/12373–3

FIGURE 1. Driver DC Test Circuit



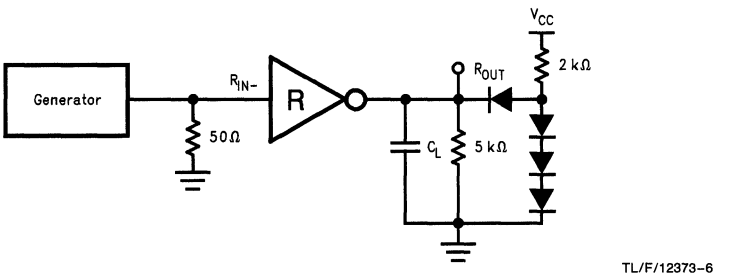
TL/F/12373–4

FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit



TL/F/12373–5

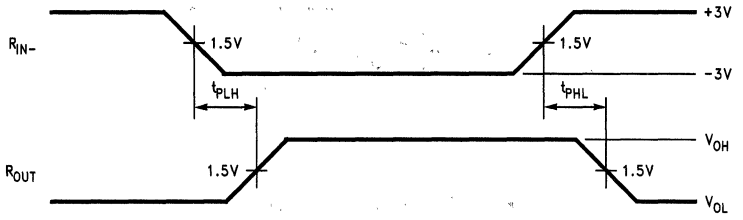
FIGURE 3. Driver Propagation Delay and Transition Time Waveform



TL/F/12373–6

FIGURE 4. Receiver Propagation Delay Test Circuit (Note 6)

Parameter Measurement Information (Continued)



TL/F/12373–7

FIGURE 5. Receiver Propagation Delay Waveform

Pin Descriptions

Pin #	Name	Description
2, 4, 8, 9, 10	D_{IN}	TTL Driver Input Pins
12, 13, 15, 19, 22	$D_{OUT}-$	Inverting Driver Output Pin
11, 14, 16, 20, 23	RC	Driver Response Control Pin
17, 18, 21	$R_{IN}-$	Inverting Receiver Input Pin
3, 5, 6	R_{OUT}	Receiver Output Pin
7	GND	Ground Pin
1	V_{EE}	Negative Power Supply Pin, −5V ±5%
24	V_{CC}	Positive Power Supply Pin, +5V ±5%

Truth Tables

Driver (D1–5)

Input D_{IN}	Output $D_{OUT}-$
L	H
H	L

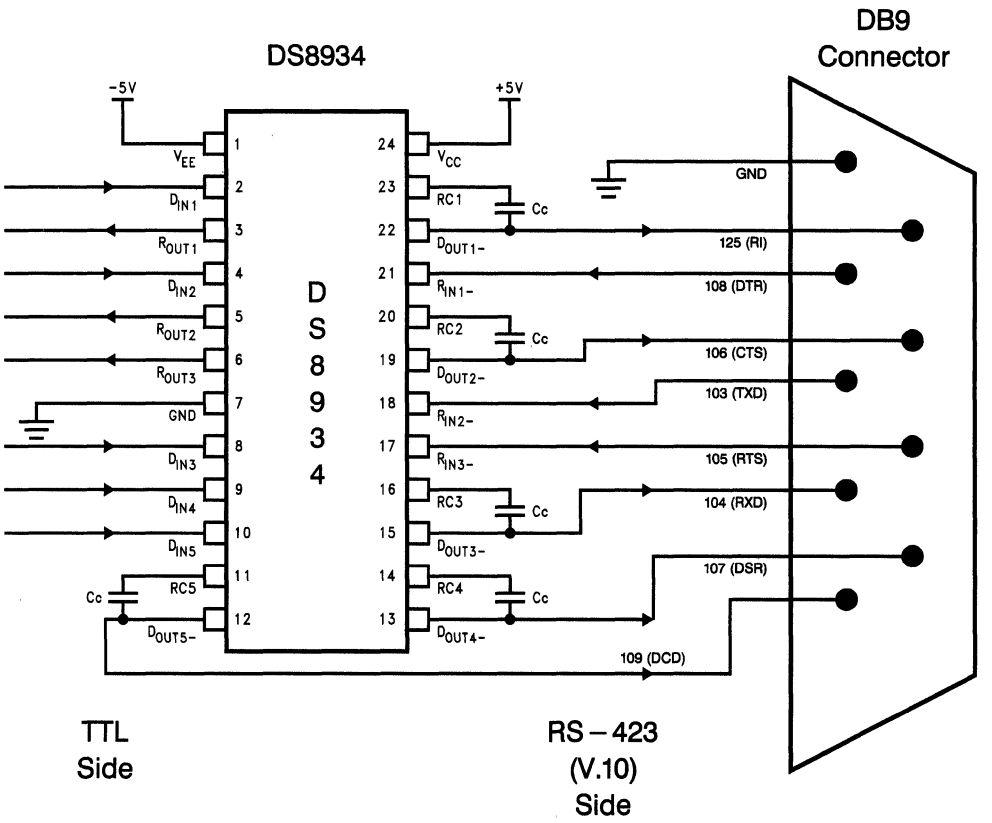
H = Logic high level (steady state)
L = Logic low level (steady state)

Receiver (R1–3)

Input $R_{IN}-$	Output R_{OUT}
≤ +0.9V	H
≥ +1.7V	L
OPEN†	H

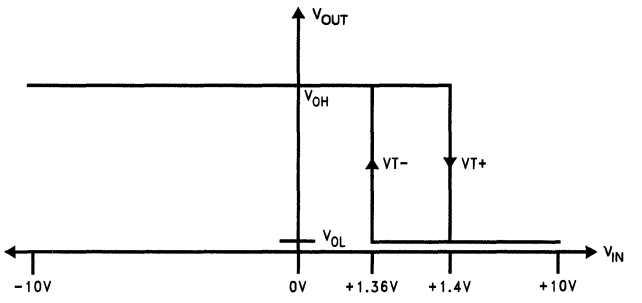
†OPEN = non-terminated

Typical Application Information



TL/F/12373–8

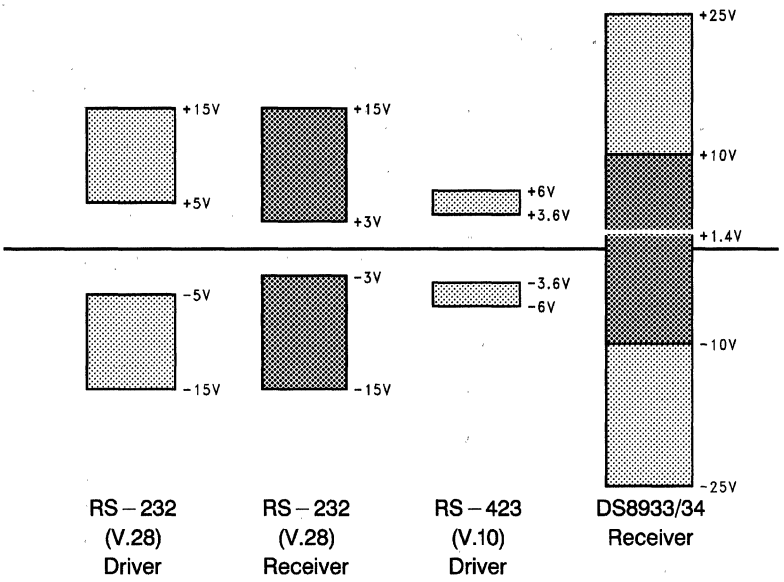
FIGURE 6. Typical V.34 9-Pin DCE Application



TL/F/12373–9

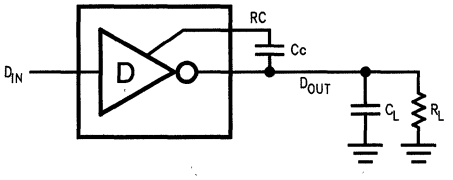
FIGURE 7. Receiver Threshold Voltage Transfer Curve (VTC)

Typical Application Information (Continued)



TL/F/12373–10

FIGURE 8. RS-423 and RS-232 Levels



TL/F/12373–11

FIGURE 9. External Slew Rate Control Capacitor Connection

National Semiconductor

DS8935
LocalTalk™ Dual Driver/Triple Receiver

General Description

The DS8935 is a dual driver/triple receiver device optimized to provide a single chip solution for a LocalTalk Interface. The device provides one differential TIA/EIA-422 driver, one TIA/EIA-423 single ended driver, one TIA/EIA-422 receiver and two TIA/EIA-423 receivers, all in a surface mount 16-pin package. This device is electrically similar to the 26LS30 and 26LS32 devices.

The drivers feature ±10V common mode range, and the differential driver provides TRI-STATEable outputs. The receivers offer ±200 mV thresholds over the ±10V common mode range.

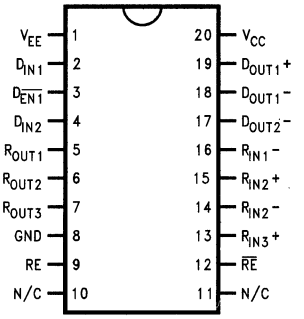
The device offers enable circuitry for the differential driver and selectable enabling for the three receivers.

Features

- Single chip solution for LocalTalk port
- Two driver/three receivers per package
- Wide common mode range: ±10V
- ±200 mV receiver sensitivity
- 70 mV typical receiver input hysteresis
- Available in SOIC packaging
- Failsafe receiver for open inputs

Connection Diagram

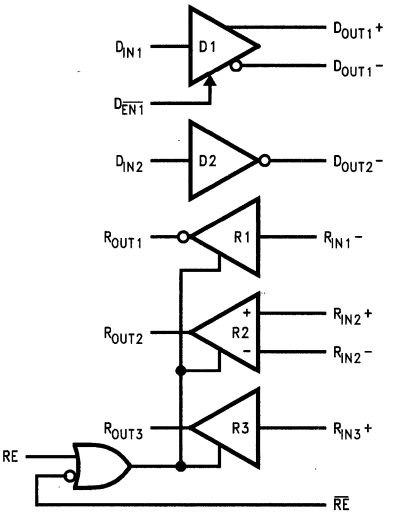
Dual-In-Line Package



TL/F/12066–1

Order Number DS8935WM
See NS Package Number M20B

Functional Diagram



TL/F/12066–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+7V
Supply Voltage (V_{EE})	−7V
Enable Input Voltage ($D_{\overline{EN1}}$, RE, $\overline{RE}$)	+7V
Driver Input Voltage (D_{IN})	+7V
Driver Output Voltage (Power Off: D_{OUT})	±15V
Receiver Input Voltage (V_{ID}: $R_{IN}+ - R_{IN}-$)	±25V
Receiver Input Voltage (V_{CM}: ($R_{IN}+ + R_{IN}-$)/2)	±25V
Receiver Input Voltage (Input to GND: R_{IN})	±25V
Receiver Output Voltage (R_{OUT})	+5.5V

Maximum Package Power Dissipation @ +25°C
M Package 1.34W
Derate M Package 10.7 mW/°C above +25°C
Storage Temperature Range −65°C to +150°C
Lead Temperature Range (Soldering, 4 Sec.) +260°C
This device does not meet 2000V ESD Rating (Note 8)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Supply Voltage (V_{EE})	−4.75	−5.0	−5.25	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD}	Output Differential Voltage	$R_L = \infty$ or $R_L = 3.9\ k\Omega$		$D_{OUT}+$, $D_{OUT}-$	±7	±9.0	±10	V
V_O	Output Voltage	$R_L = \infty$ or $R_L = 3.9\ k\Omega$				±4.5	±5.25	V
V_{OD1}	Output Differential Voltage	$R_L = 100\Omega$, *Figure 1*			4.0	6.4		|V|
V_{SS}	$\lvert V_{OD1} - V_{\overline{OD1}} \rvert$				8.0	12.8		|V|
ΔV_{OD1}	Output Unbalance					0.02	0.4	V
V_{OS}	Offset Voltage					0	3	V
ΔV_{OS}	Offset Unbalance					0.05	0.4	V
V_{OD2}	Output Differential Voltage	RL = 140Ω, *Figure 1*			6.0	7.0		|V|
I_{OZD}	TRI-STATE® Leakage Current	V_{CC} = 5.25V, V_{EE} = −5.25V	V_O = +10V			2	150	μA
			V_O = +6V			1	100	μA
			V_O = −6V			−1	−100	μA
			V_O = −10V			−2	−150	μA
SINGLE ENDED DRIVER CHARACTERISTICS								
V_O	Output Voltage (No Load)	$R_L = \infty$ or $R_L = 3.9\ k\Omega$, *Figure 2*		$D_{OUT}-$	4	4.4	6	|V|
V_T	Output Voltage	$R_L = 3\ k\Omega$, *Figure 2*			3.7	4.3		|V|
		$R_L = 450\Omega$, *Figure 2*			3.6	4.1		|V|
ΔV_T	Output Unbalance					0.02	0.4	V
DRIVER CHARACTERISTICS								
V_{CM}	Common Mode Range	Power Off, or D1 Disabled		$D_{OUT}+$, $D_{OUT}-$	±10			V
I_{OSD}	Short Circuit Current	V_O = 0V, Sourcing Current				−80	−150	mA
		V_O = 0V, Sinking Current				80	150	mA
I_{OXD}	Power-Off Leakage Current (V_{CC} = V_{EE} = 0V)	V_O = +10V				2	150	μA
		V_O = +6V				1	100	μA
		V_O = −6V				−1	−100	μA
		V_O = −10V				−2	−150	μA

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Input Threshold	$-7V \le V_{CM} \le +7V$		$R_{IN}+$, $R_{IN}-$	−200	±35	+200	mV
V_{HY}	Hysteresis	$V_{CM} = 0V$				70		mV
R_{IN}	Input Resistance	$-10V \le V_{CM} \le +10V$			6.0	8.5		kΩ
I_{IN}	Input Current (Other Input = 0V, Power On, or $V_{CC} = V_{EE} = 0V$)	$V_{IN} = +10V$					3.25	mA
		$V_{IN} = +3V$			0		1.50	mA
		$V_{IN} = -3V$			0		−1.50	mA
		$V_{IN} = -10V$					−3.25	mA
V_{IB}	Input Balance Test	$R_S = 500\Omega$ (R2 only)					±400	mV
V_{OH}	High Level Output Voltage	$I_{OH} = -400\ \mu A$, $V_{IN} = +200$ mV		R_{OUT}	2.7	4.2		V
		$I_{OH} = -400\ \mu A$, V_{IN} = OPEN			2.7	4.2		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 8.0$ mA, $V_{IN} = -200$ mV				0.3	0.5	V
I_{OSR}	Short Circuit Current	$V_O = 0V$			−15	−34	−85	mA
I_{OZR}	TRI-STATE Output Current	V_{CC} = Max	$V_O = 2.4V$			0	+20	μA
			$V_O = 0.4V$			0	−20	μA
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			D_{IN}, $D_{\overline{ENT}}$, RE, $\overline{RE}$	2.0			V
V_{IL}	Low Level Input Voltage						0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$				1	40	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$				−10	−200	μA
V_{CL}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
I_{CC}	Power Supply Current	No Load D1 Enabled or Disabled		V_{CC}		40	65	mA
I_{EE}				V_{EE}		−5	−15	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 4 and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	$R_L = 100\Omega$, $C_L = 500$ pF, (*Figures 3* and *4*) $C_1 = C_2 = 50$ pF	70	134	350	ns
t_{PLHD}	Differential Propagation Delay Low to High		70	141	350	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			7	50	ns
t_r	Rise Time		50	140	300	ns
t_f	Fall Time		50	140	300	ns
t_{PHZ}	Disable Time High to Z	$R_L = 100\Omega$, $C_L = 500$ pF (*Figures 7* and *8*)		300	600	ns
t_{PLZ}	Disable Time Low to Z			300	600	ns
t_{PZH}	Enable Time Z to High			160	350	ns
t_{PZL}	Enable Time Z to Low			160	350	ns
SINGLE ENDED DRIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$R_L = 450\Omega$, $C_L = 500$ pF (*Figures 5* and *6*)	70	120	350	ns
t_{PLH}	Propagation Delay Low to High		70	150	350	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			30	70	ns
t_r	Rise Time		50	100	300	ns
t_f	Fall Time		20	50	300	ns
RECEIVER CHARACTERISTICS						
t_{PHL}	Propagation Delay High to Low	$C_L = 15$ pF (*Figures 9* and *10*)	10	33	75	ns
t_{PLH}	Propagation Delay Low to High		10	30	75	ns
t_{SK}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$			3	20	ns
t_{HZ}	Disable Time High to Z	$C_L = 15$ pF (*Figures 9* and *11*)		20	75	ns
t_{LZ}	Disable Time Low to Z			20	75	ns
t_{ZH}	Enable Time Z to High			20	75	ns
t_{ZL}	Enable Time Z to Low			20	75	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}, V_{OD1}, V_{OD2}, and V_{SS}.

Note 3: All typicals are given for: $V_{CC} = +5.0V$, $V_{EE} = -5.0V$, $T_A = +25°C$ unless otherwise specified.

Truth Tables

Driver (D1)

Inputs		Outputs	
$D_{\overline{EN1}}$	D_{IN1}	$D_{OUT1}+$	$D_{OUT1}-$
H	X	Z	Z
L	L	L	H
L	H	H	L

Receiver (1)

RE	$\overline{RE}$	Input	Output
		$R_{IN1}-$	R_{OUT1}
0	1	X	Z
Any Other Combination		≤ -200 mV	H
		$\geq +200$ mV	L
		Open†	H

Driver (D2)

Input	Output
D_{IN2}	$D_{OUT2}-$
L	H
H	L

Receiver (2)

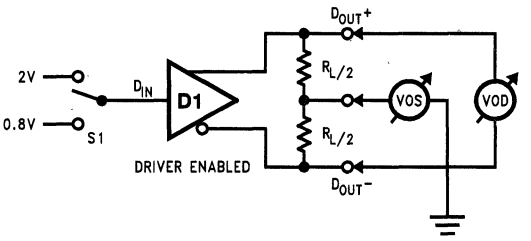
RE	$\overline{RE}$	Inputs	Output
		$R_{IN2}+ - R_{IN2}-$	R_{OUT2}
0	1	X	Z
Any Other Combination		≤ -200 mV	L
		$\geq +200$ mV	H
		Open†	H

Receiver (3)

RE	$\overline{RE}$	Input	Output
		$R_{IN3}+$	R_{OUT3}
0	1	X	Z
Any Other Combination		≤ -200 mV	L
		$\geq +200$ mV	H
		Open†	H

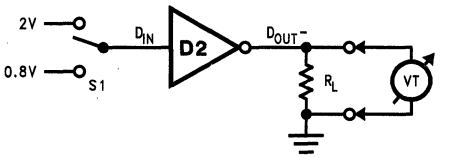
H = Logic High Level (Steady State)
L = Logic Low Level (Steady State)
X = Irrelevant (Any Input)
Z = Off State (TRI-STATE, High Impedance)
†OPEN = Non-Terminated

Parameter Measurement Information



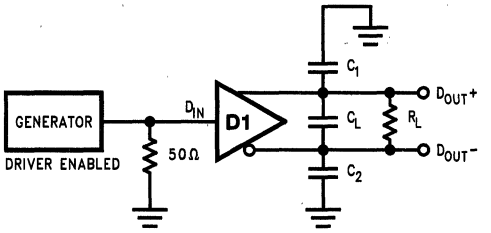
TL/F/12066–3

FIGURE 1. Differential Driver DC Test Circuit



TL/F/12066–4

FIGURE 2. Single Ended Driver DC Test Circuit



TL/F/12066–5

FIGURE 3. Differential Driver Propagation Delay and Transition Time Test Circuit

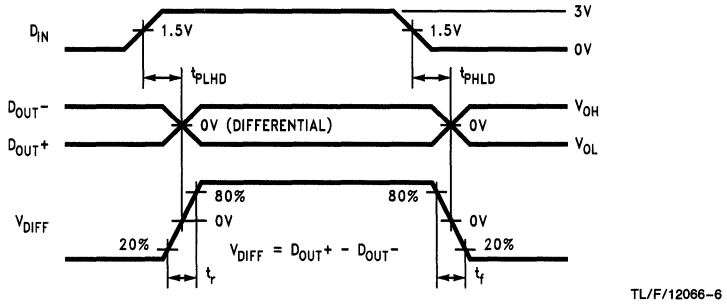


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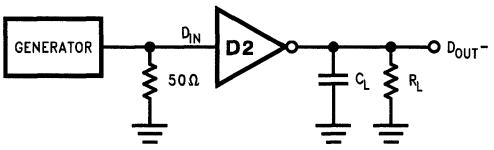
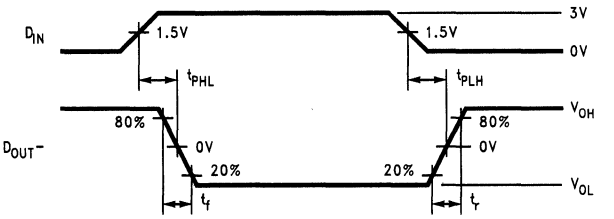
FIGURE 4. Differential Driver Propagation Delay and Transition Time Waveforms



TL/F/12066–7

FIGURE 5. Single Ended Driver Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)



TL/F/12066–8

FIGURE 6. Single Ended Driver Propagation Delay and Transition Time Waveform

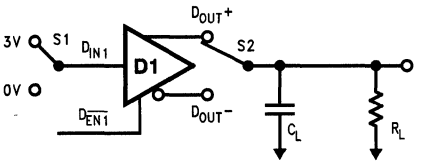


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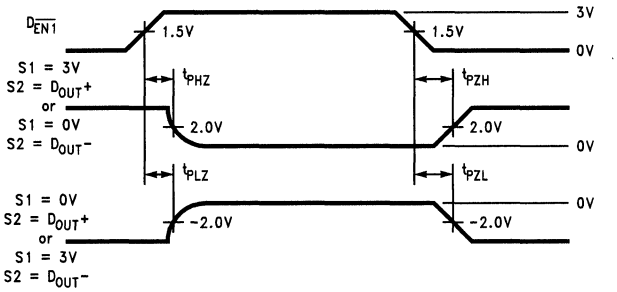
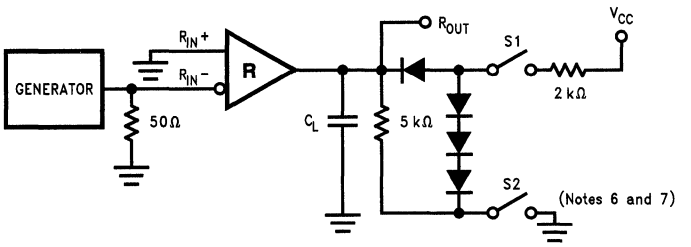
FIGURE 7. Differential Driver TRI-STATE Test Circuit



TL/F/12066–10

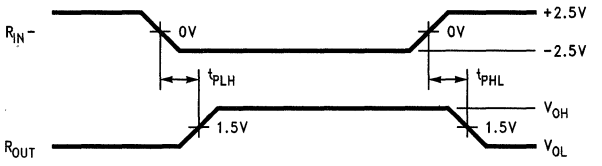
FIGURE 8. Differential Driver TRI-STATE Waveforms



TL/F/12066–11

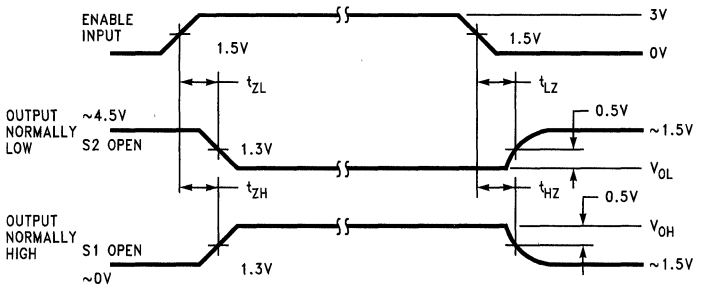
FIGURE 9. Receiver Propagation Delay Test Circuit

Parameter Measurement Information (Continued)



TL/F/12066–12

FIGURE 10. Receiver Propagation Delay Waveform



TL/F/12066–13

FIGURE 11. Receiver TRI-STATE Delay Waveform

Note 4: Generator waveform for all tests unless otherwise specified: f = 500 kHz, Z_O = 50Ω, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

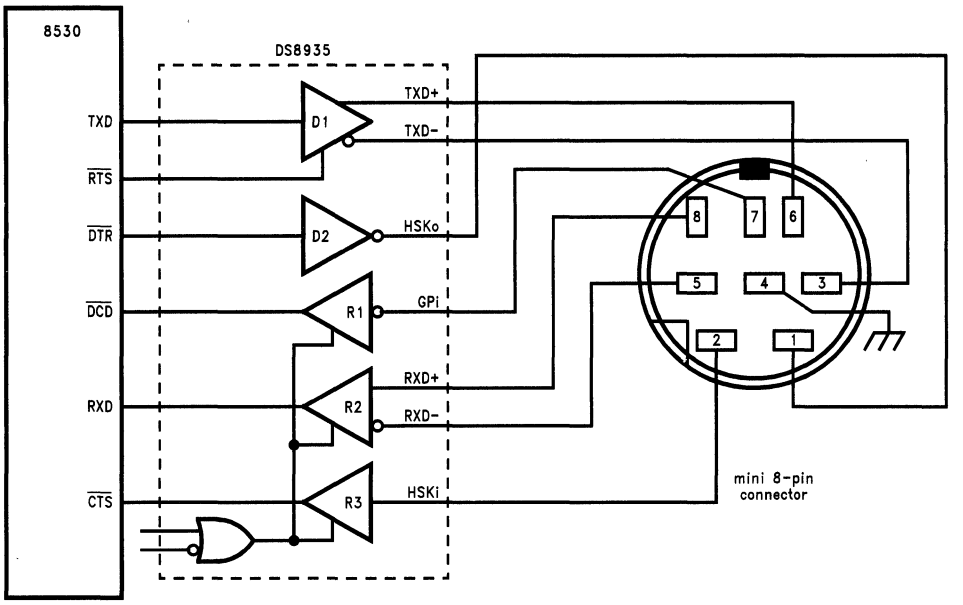
Note 5: C_L includes probe and jig capacitance.

Note 6: All diodes are 1N916 or equivalent.

Note 7: S1 and S2 closed except where shown.

Note 8: ESD Rating HBM (1.5 kΩ, 100 pF) pins 14, 16 ≥1500V, all other pins ≥2000V.

Typical Application Information



TL/F/12066–14

FIGURE 12. Typical LocalTalk™ Application

TABLE I. Device Pin Descriptions

Pin #	Name	Description
2, 4	D_{IN}	TTL Driver Input Pins
3	$D_{\overline{EN1}}$	Active Low Driver Enable Pin. A High on this Pin TRI-STATEs the Driver Outputs (D1 Only)
19	$D_{OUT}+$	Non-Inverting Driver Output Pin
17, 18	$D_{OUT}-$	Inverting Driver Output Pin
13, 15	$R_{IN}+$	Non-Inverting Receiver Input Pin
16, 14	$R_{IN}-$	Inverting Receiver Input Pin
5, 6, 7	R_{OUT}	Receiver Output Pin
9	R_{EN}	Active Low Receiver Enable
12	$R_{\overline{EN}}$	Active High Receiver Enable
10, 11	N/C	Not Connected
8	GND	Ground Pin
1	V_{EE}	Negative Power Supply Pin, −5V ±5%
20	V_{CC}	Positive Power Supply Pin, +5V ±5%

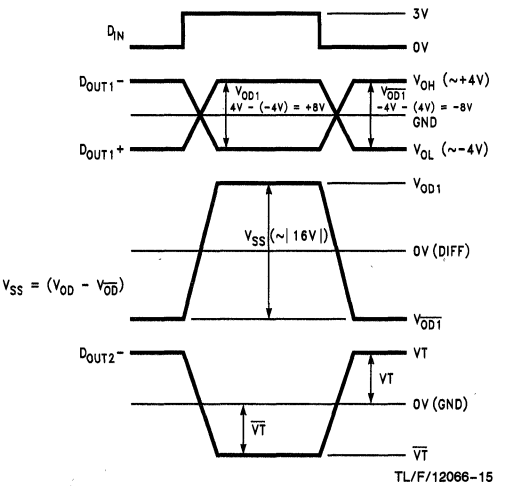
Typical Application Information (Continued)

DRIVER OUTPUT WAVEFORMS

The driver configuration on the DS8935 is unique among TIA/EIA-422 devices in that it utilizes −5V V_{EE} supply. A typical TIA/EIA-422 driver uses +5V only and generates signal swings of approximately 0V–5V.

By utilizing V_{EE}, the differential driver is able to generate a much larger differential signal. The typical output voltage is about |4| V, which gives |8| V differentially, thus providing a much greater noise margin than +5V drivers. See *Figure 13*. The receiver therefore has a range of +8V to −8V or V_{SS} of 16V ($V_{SS} = V_{OD}-V_{OD*}$).

Each side of the differential driver operates similar to a TIA/EIA-423 driver. The output voltages are slightly different due to the loading: the differential driver has differential termination, the single-ended driver is terminated with a resistor to ground.



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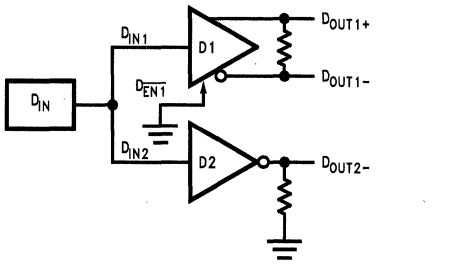


TL/F/12066–16

Note:
- V_{CC} = +5V, V_{EE} = −5V
- D1 Enabled (Active)

FIGURE 13. Typical Driver Output Waveforms

UNUSED PINS

Unused driver outputs should be left open. If tied to either ground or supply, the driver may enter an I_{OS} state and consume excessive power. Unused driver inputs should not be left floating as this may lead to unwanted switching which may affect I_{CC}, particularly the frequency component. Unused driver inputs should be tied to ground.

Receiver outputs will be in a HIGH state when inputs are open; therefore, outputs should not be tied to ground. It is best to leave unused receiver outputs floating.

RECEIVER FAILSAFE

All three receivers on this device incorporate open input failsafe protection. The differential receiver output will be in a HIGH state when inputs are open, but will be indetermined if inputs are shorted together. Unused differential inputs should be left floating.

Both single-ended receivers (inverting and non-inverting) are biased internally so that an open input will result in a HIGH output. Therefore, these inputs should not be shorted to ground when unused.

BYPASS CAPACITORS

Bypass capacitors are recommended for both V_{CC} and V_{EE}. Noise induced on the supply lines can affect the signal quality of the output; V_{CC} affects the V_{OH} and V_{EE} affects the V_{OL}. Capacitors help reduce the effect on signal quality. A value of 0.1 μF is typically used.

Since this is a power device, it is recommended to use a bypass capacitor for each supply and for each device. Sharing a bypass capacitor between other devices may not be sufficient.

TERMINATION

On a multi-point transmission line which is electrically long, it is advisable to terminate the line at both ends with its characteristic impedance to prevent signal reflection and its associated noise/crosstalk.

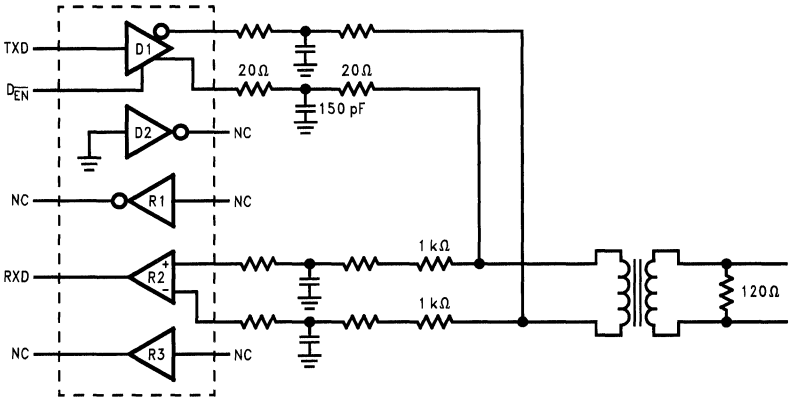
A 100Ω termination resistor is commonly specified by TIA/EIA-422 for differential signals. The DS8935 is also specified using 140Ω termination which will result in less power associated with the driver output. The additional resistance is typical of applications requiring EMI filtering on the driver outputs.

TWO-WIRE LocalTalk

The DS8935 is a single chip solution for a LocalTalk interface. A typical application is shown in *Figure 12*.

An alternative implementation of LocalTalk is to only use two wires to communicate. The differential data lines can be transformer-coupled on to a twisted pair medium. See *Figure 14*. The handshake function must then be accomplished in software.

Typical Application Information (Continued)



TL/F/12066–17

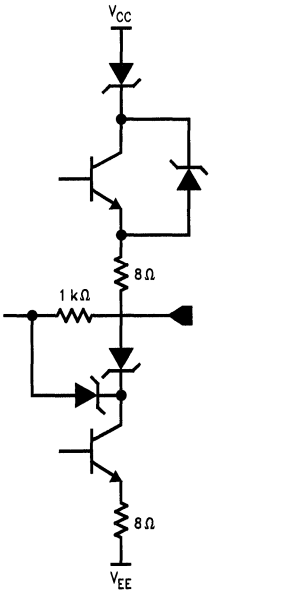
FIGURE 14. Differential Communication, Transformer-Coupled to a Twisted-Pair Line

SINGLE +5V SUPPLY

The DS8935 is derived from the DS3691/92 which could be configured using a single +5V supply (V_{EE} = 0V). This device is not specified for this type of operation. However, the device will not be damaged if operated using a single +5V supply.

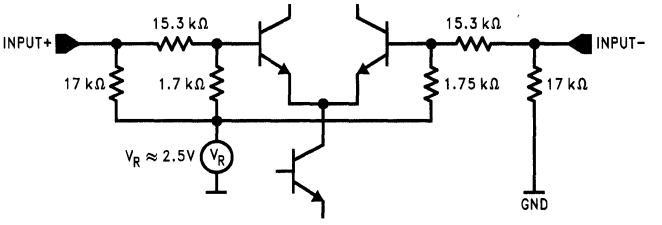
Both drivers require the −5V supply in order to meet the output voltage levels specified. When the device switches from a positive voltage to the complimentary state, it is pulled toward the V_{EE} level. If that level is 0V, then the complimentary state will be near 0V instead of V_{EE}. Thus, the output would switch from about 4V to 0V, instead of 4V to −4V. The differential driver will meet TIA/EIA-422, but with a reduced noise margin. The single-ended driver will not meet TIA/EIA-423 without the −5V supply.

The receivers will be functional but may suffer parametrically. The inverting receiver is referenced to V_{EE} therefore, the threshold may shift slightly. The inputs can still vary over the ±10V common mode range.



TL/F/12066–48

FIGURE 15. Driver Output Structure



TL/F/12066–49

FIGURE 16. Receiver Input Structure

Typical Performance Characteristics

The DS8935 is very closely related to the DS8925. Please refer to the DS8925 datasheet for the typical performance characteristics.

National Semiconductor

ADVANCE INFORMATION

DS8936
LocalTalk™ Dual Driver/Triple Receiver

General Description

The DS8936 is a dual driver/triple receiver device optimized to provide a single chip solution for a LocalTalk Interface. The device provides one differential TIA/EIA-422 driver, one TIA/EIA-423 single ended driver, one TIA/EIA-422 receiver and two TIA/EIA-423 receivers, all in a surface mount 16-pin package. This device is electrically similar to the 26LS30 and 26LS32 devices and is a direct replacement for the DS8935.

The drivers feature ±10V common mode range, and the differential driver provides TRI-STATEable® outputs. The receivers offer ±200 mV thresholds over the ±10V common mode range.

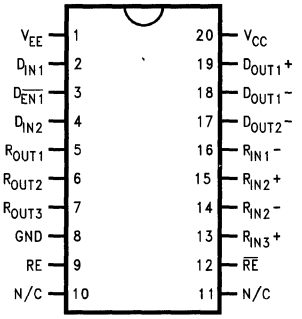
The device offers enable circuitry for the differential driver and selectable enabling for the three receivers.

Features

- Single chip solution for LocalTalk port
- Two driver/three receivers per package
- Fast rise/fall times and prop delay on receivers
- Wide common mode range: ±10V
- ±200 mV receiver sensitivity
- 70 mV typical receiver input hysteresis
- Available in SOIC packaging
- Failsafe receiver for open inputs

Connection Diagram

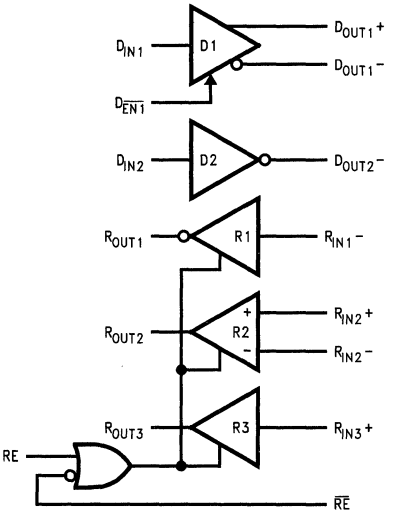
Dual-In-Line Package



TL/F/12647–1

Order Number DS8936WM
See NS Package Number M20B

Functional Diagram



TL/F/12647–2

National Semiconductor

DS89C386
Twelve Channel CMOS Differential Line Receiver

General Description

The DS89C386 is a high speed twelve channel CMOS differential receiver that meets the requirements of TIA/EIA-422-B. The DS89C386 features low power dissipation of 240 mW typical.

Each TRI-STATE® enable, EN, allows the receiver output to be active or in a Hi-impedance off state. Each enable is common to only two receivers for flexibility and multiplexing of receiver outputs.

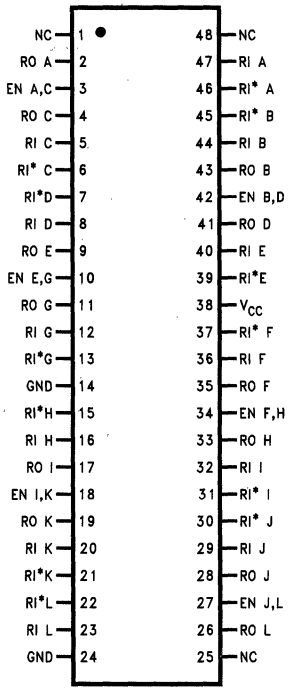
The receiver output (RO) is guaranteed to be High when the inputs are left open and unterminated. The receiver can detect signals as low and including ±200 mV over the common mode range of ±7V. The receiver outputs (RO) are compatible with both TTL and CMOS levels.

Features

- Low power design—240 mW typical
- Meets TIA/EIA-422-B (RS-422)
- Receiver OPEN input failsafe feature
- Guaranteed AC parameters:
  - — Maximum receiver skew −4 ns
  - — Maximum transition time −9 ns
- High Output Drive Capability: ±6 mA
- Available in SSOP packaging:
  Requires 30% less PCB space than 3 DS34C86TMs

Connection Diagram

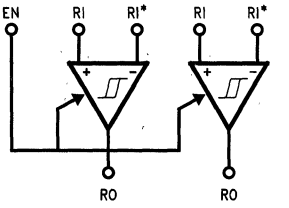
48L SSOP
DS89C386



TL/F/12085–1

Order Number DS89C386TMEA
See NS Package Number MS48A

Function Diagram



TL/F/12085–2

1/6 of package

Truth Table

Enable	Inputs	Output
EN	RI–RI*	RO
L	X	Z
H	≥200 mV or OPEN†	H
H	≤ −200 mV	L
H	+200 mV > and > −200 mV	X

†Not terminated.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to 7V
Input Common Mode Range (V_{CM})	±14V
Differential Input Voltage (V_{DIFF})	±14V
Enable Input Voltage (V_{IN})	7V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	260°C
Maximum Power Dissipation at 25°C (Note 4)	
SSOP Package	1359 mW
Current Per Output	±25 mA

This device does not meet 2000V ESD rating. (Note 5)

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	4.50	5.50	V
Operating Temperature Range (T_A)			
DS89C386T	−40	+85	°C
Enable Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Note 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL} $-7V < V_{CM} < +7V$	−200	±35	+200	mV
V_{HYST}	Input Hysteresis	V_{CM} = 0V		70		mV
R_{IN}	Input Resistance	V_{IN} = −7V, +7V (Other Input = GND)	5.0	6.8	10	kΩ
I_{IN}	Input Current (Under Test)	V_{IN} = +10V, Other Input = GND		+1.1	+1.5	mA
		V_{IN} = −10V, Other Input = GND		−2.0	−2.5	mA
V_{OH}	High Level Output Voltage	V_{CC} = Min., $V_{(DIFF)}$ = +1V I_{OUT} = −6.0 mA	3.8	4.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Max., $V_{(DIFF)}$ = −1V I_{OUT} = 6.0 mA		0.2	0.3	V
V_{IH}	Enable High Input Level Voltage		2.0		V_{CC}	V
V_{IL}	Enable Low Input Level Voltage		GND		0.8	V
I_{OZ}	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, EN = V_{IL}		±0.5	±5.0	μA
I_I	Enable Input Current	$V_{IN} = V_{CC}$ or GND			±1.0	μA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., $V_{(DIFF)}$ = +1V		48	69	mA

AC Electrical Characteristics V_{CC} = 5V ±10% (Note 3) (*Figures 1, 2,* and *3*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V	10	19	30	ns
t_{SK}	Skew	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V	0	2	4	ns
t_{RISE}, t_{FALL}	Output Rise and Fall Times	C_L = 50 pF V_{DIFF} = 2.5V V_{CM} = 0V		4	9	ns
t_{PLZ}, t_{PHZ}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	18	ns
t_{PZL}, t_{PZH}	Propagation Delay ENABLE to Output	C_L = 50 pF R_L = 1000Ω V_{DIFF} = 2.5V		13	21	ns

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

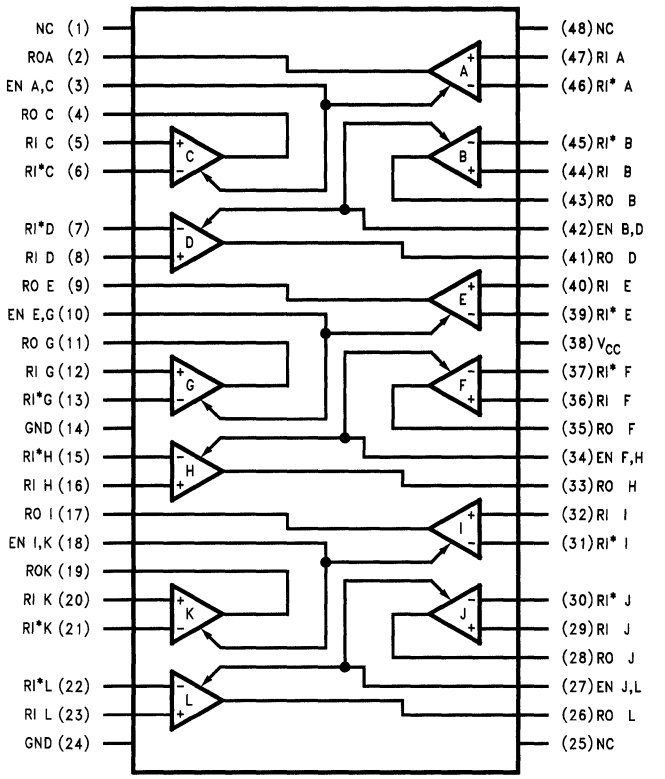
Note 3: Unless otherwise specified, Min/Max limits apply across the operating temperature range.

All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 4: Ratings apply to ambient temperature at 25°C. Above this temperature derate SSOP (MEA) Package 10.9 mW/°C.

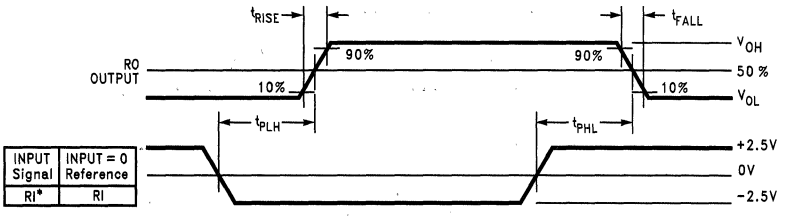
Note 5: ESD Rating: HEM (1.5 kΩ, 100 pF)
Inputs ≥ 2000V
Outputs ≥ 1000V
EIAJ (0Ω, 200 pF)
All Pins ≥ 350V

Logic Diagram



TL/F/12085–3

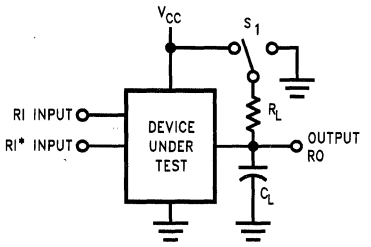
Parameter Measurement Information



TL/F/12085–4

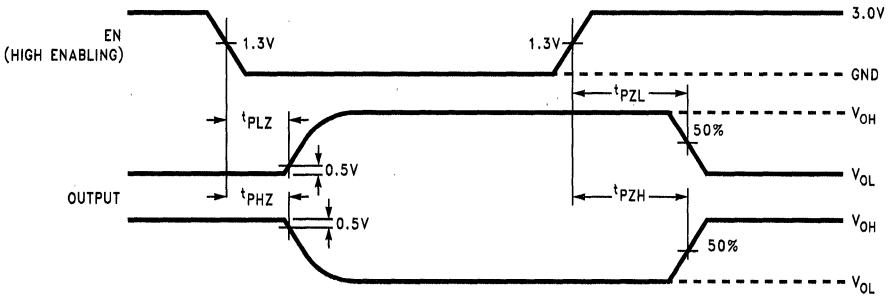
FIGURE 1. Propagation Delays

C_L includes load and test jig capacitance.
S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.
S1 = Open for t_{PLH}, t_{PHL}, and t_{SK}.



TL/F/12085–5

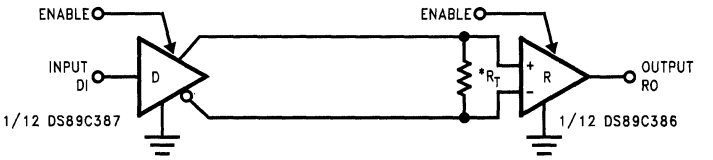
FIGURE 2. Test Circuit for Switching Characteristics



TL/F/12085–6

FIGURE 3. TRI-STATE Output Enable and Disable Waveforms

Application Information



TL/F/12085–7

*R_T is optional although highly recommended to reduce reflections.

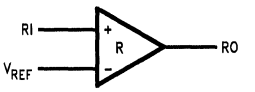
FIGURE 4. Two-Wire Balanced System, RS-422

SKEW

Skew may be thought of in a lot of different ways, the next few paragraphs should clarify what is represented by t_{SK} in this datasheet and how it is determined. Skew, as used in this databook, is the absolute value of a mathematical difference between two propagation delays. This is commonly accepted throughout the semiconductor industry. However, there is no standardized method of measuring propagation delay, from which skew is calculated, of differential line receivers. Elucidating, the voltage level, at which propagation delays are measured, on both input and output waveforms are not always consistant. Therefore, skew calculated in this datasheet, may not be calculated the same as skew defined in another. This is important to remember whenever making a skew comparison.

Skew may be calculated for the DS89C386, from many different propagation delay measurements. They may be classified into two categories, single-ended and differential. Single-ended skew is calculated from t_{PHL} and t_{PLH} propagation delay measurements (see *Figures 5* and *6*). Differential skew is calculated from t_{PHLD} and t_{PLHD} differential propagation delay measurements (see *Figures 7* and *8*).

(Circuit 1)



TL/F/12085–8

(Circuit 2)

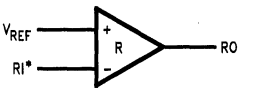


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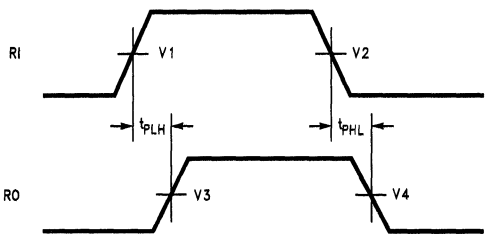
FIGURE 5. Circuits for Measuring Single-Ended Propagation Delays (See *Figure 6*)

Waveforms for Circuit 1



TL/F/12085–10

Waveforms for Circuit 2

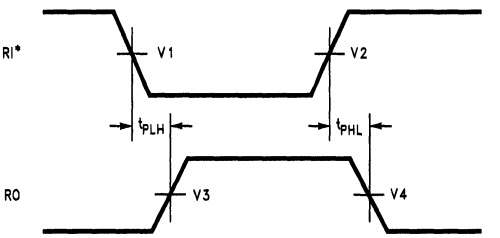


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FIGURE 6. Propagation Delay Waveforms for Circuit 1 and Circuit 2 (See *Figure 5*)

Application Information (Continued)

In *Figure 6*, VX, where X is a number, is the waveform voltage level at which the propagation delay measurement either starts or stops. Furthermore, V1 and V2 are normally identical. The same is true for V3 and V4. However, as mentioned before, these levels are not standardized and may vary, even with similar devices from other companies. Also note, V_{REF} in *Figure 1* should equal V1 and V2 in *Figure 6*.

The single-ended skew provides information about the pulse width distortion of the output waveform. The lower the skew, the less the output waveform will be distorted. For best case, skew would be zero, and the output duty cycle would be 50%, assuming the input has a 50% duty cycle.

(Circuit 3)

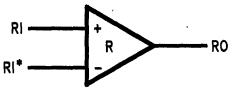

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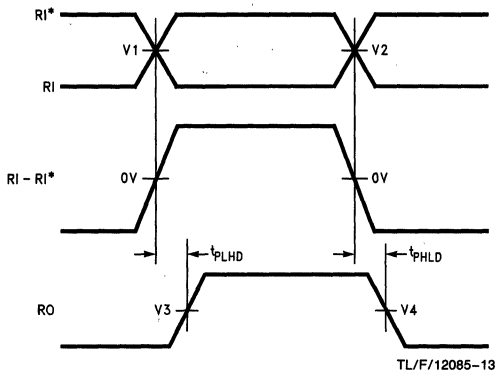
FIGURE 7. Circuit for Measuring Differential Propagation Delays (See *Figure 8*)

Waveforms for Circuit 3



TL/F/12085–13

FIGURE 8. Propagation Delay Waveforms for Circuit 3 (see *Figure 7*)

For differential propagation delays, V1 may not equal V2. Furthermore, the crossing point of RI and RI* corresponds to zero volts on the differential waveform. (See middle waveform in *Figure 8*.) This is true whether V1 equals V2 or not. However, if V1 and V2 are specified voltages, then V1 and V2 are less likely to be equal to the crossing point voltage. Thus, the differential propagation delays will not be measured from zero volts on the differential waveform.

The differential skew also provides information about the pulse width distortion of the output waveform relative to the differential input waveform. The higher the skew, the greater the distortion of the output waveform. Assuming the differential input has a 50% duty cycle, the output will have a 50% duty cycle if skew equals zero and less than a 50% duty cycle if skew is greater than zero.

Only t_{SK} is specified in this datasheet for the DS89C386. t_{SK} is measured single-endedly but corresponds to differential skew. Because, for single-ended skew, when V_{REF} equals V1 and V2, t_{PHL} equals t_{PHLD} when t_{PHLD} is measured from the crossing point.

More information can be calculated from the propagation delays. The channel to channel and device to device skew may be calculated in addition to the types of skew mentioned previously. These parameters provide timing performance information beneficial when designing. The channel to channel skew is calculated from the variation in propagation delay from receiver to receiver within one package. The device to device skew is calculated from the variation in propagation delay from one DS89C386 to another DS89C386.

For the DS89C386, the maximum channel to channel skew is 20 ns (t_p max—t_p min) where t_p is the low to high or high to low propagation delay. The minimum channel to channel skew is 0 ns since it is possible for all 12 receivers to have identical propagation delays. Note, this is best and worst case calculations used whenever t_{SK} (channel) is not independently characterized and specified in the datasheet. The device to device skew may be calculated in the same way and the results are identical. Therefore, the device to device skew is 20 ns and 0 ns maximum and minimum respectively.

TABLE I. DS89C386 Skew Table

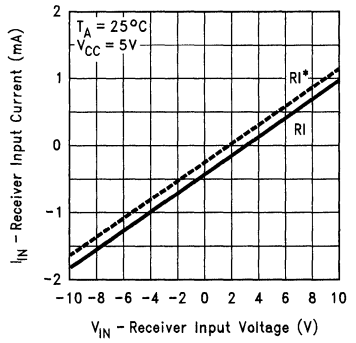
Parameter	Min	Typ	Max	Units
t_{SK} (diff.)	0	2	4	ns
t_{SK} (channel)	0		20	ns
t_{SK} (device)	0		20	ns

Note t_{SK} (diff.) in Table I is the same as t_{SK} in the datasheet. Also, t_{SK} (channel) and t_{SK} (device) are calculations, but are guaranteed by the propagation delay tests. Both t_{SK} (channel) and t_{SK} (device) would normally be tighter whenever specified from characterization data.

The information in this section of the datasheet is to help clarify how skew is defined in this datasheet. This should help when designing the DS89C386 into most applications.

Typical Performance Characteristics

Receiver Input Voltage vs Receiver Input Current (Notes 6 and 7)



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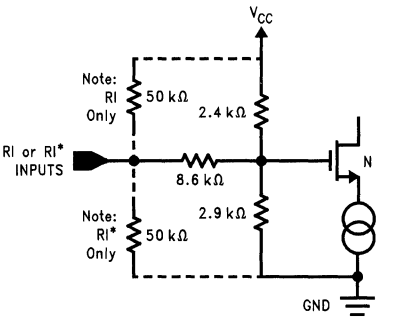
Note 6: The DS89C386 is V.11 compatible. I_{IN} (RI input) is not ≥ 0 when V_{IN} = 3V due to internal failsafe bias resistors (see *Figure 6*). See ITU V.11 for complete conditions.

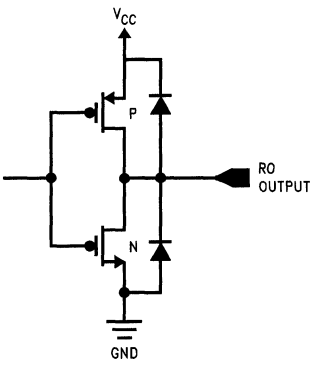
Note 7: Failsafe (open inputs) is maintained over entire common mode range and operating range ±10V.

DS89C386 Equivalent Input/Output Circuits



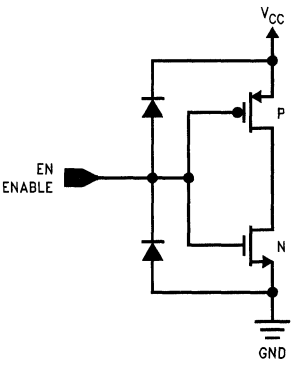
TL/F/12085–15

FIGURE 10. Receiver Input Equivalent Circuit



TL/F/12085–16

FIGURE 11. Receiver Output Equivalent Circuit



TL/F/12085–17

FIGURE 12. Receiver Enable Equivalent Circuit

Pin Descriptions

TABLE II. Device Pin Names and Descriptions

Pin #	Pin Name	Pin Description
2, 4, 9, 11, 17, 19, 26, 28, 33, 35, 41, 43	RO	TTL/CMOS Compatible Receiver Output Pin
5, 8, 12, 16, 20, 23, 29, 32, 36, 40, 44, 47	RI	Non-Inverting Signal Receiver Input Pin
6, 7, 13, 15, 21, 22, 30, 31, 37, 39, 45, 46	RI*	Inverting Signal Receiver Input Pin
3, 10, 18, 27, 34, 42	EN	Active High Dual Receiver Enabling Pin
38	V_{CC}	Positive Power Supply Pin $+5 \pm 10\%$
14, 24	GND	Device Ground Pin
1, 25, 48	NC	Unused Pin (NOT CONNECTED)

National Semiconductor

DS89C387
Twelve Channel CMOS Differential Line Driver

General Description

The DS89C387 is a high speed twelve channel CMOS differential driver that meets the requirements of TIA/EIA-422-B. The DS89C387 features a low I_{CC} specification of 1.5 mA maximum, which makes it ideal for battery powered and power conscious applications. The device replaces three DS34C87s and offers a PC board space savings up to 30%. The twelve channel driver is available in a SSOP package. The device is ideal for wide parallel bus applications.

Each TRI-STATE® enable (EN) allows the driver outputs to be active or in a HI-impedance off state. Each enable is common to only two drivers for flexibility and control. The drivers may be disabled to turn off load current and to save power when data is not being transmitted.

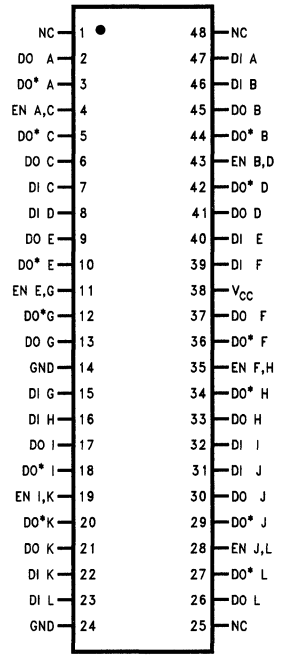
The driver's input (DI) is compatible with both TTL and CMOS signal levels.

Features

- Low power I_{CC}: 1.5 mA maximum
- Meets TIA/EIA-422-B (RS-422)
- Guaranteed AC parameters:
  - — Maximum driver skew −3 ns
  - — Maximum transition time −10 ns
- Available in SSOP packaging:
  Requires 30% less PCB space than 3 DS34C87TMs

Connection Diagram

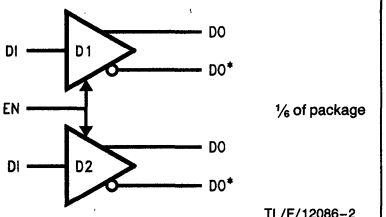
48L SSOP
DS89C387



TL/F/12086–1

Order Number DS89C387TMEA
See NS Package Number MS48A

Functional Diagram



TL/F/12086–2

Truth Table

Enable	Input	Outputs	
EN	DI	DO	DO*
L	X	Z	Z
H	H	H	L
H	L	L	H

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to 7.0V
DC Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±150 mA
DC V_{CC} or GND Current (I_{CC})	±500 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Power Dissipation (P_D) @ 25°C (Note 3)	
SSOP Package	1359 mW
Lead Temperature (T_L) (Soldering 4 sec.)	260°C

This device does not meet 2000V ESD rating. (Note 11)

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
DS89C387T	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified) (Notes 2 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = −20 mA		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 48 mA			0.3	0.5	V
V_T	Differential Output Voltage	R_L = 100Ω (Note 5)		2.0	3.1		V
$\lvert V_T\rvert - \lvert \overline{V}_T\rvert$	Difference In Differential Output	R_L = 100Ω (Note 5)				0.4	V
V_{OS}	Common Mode Output Voltage	R_L = 100Ω (Note 5)			2.0	3.0	V
$\lvert V_{OS} - \overline{V}_{OS}\rvert$	Difference In Common Mode Output	R_L = 100Ω (Note 5)				0.4	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, V_{IH}, or V_{IL}				±1.0	μA
I_{CC}	Quiescent Supply Current	I_{OUT} = 0 μA, V_{IN} = V_{CC} or GND			600	1500	μA
		V_{IN} = 2.4V or 0.5V (Note 6)			0.8	2.0	mA
I_{OZ}	TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Control = V_{IL}			±0.5	±5.0	μA
I_{SC}	Output Short Circuit Current	V_{IN} = V_{CC} or GND (Notes 5, 7)		−30	−115	−150	mA
I_{OFF}	Power Off Output Leakage Current	V_{CC} = 0V (Note 5)	V_{OUT} = 6V			100	μA
			V_{OUT} = −0.25V			−100	μA

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive; all currents out of device pins are negative.

Note 3: Ratings apply to ambient temperature at 25°C. Above this temperature derate SSOP (MEA) Package 10.9 mW/°C.

Note 4: Unless otherwise specified, min/max limits apply across the −40°C to 85°C temperature range. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 5: See TIA/EIA-422-B for exact test conditions.

Note 6: Measured per input. All other inputs at V_{CC} or GND.

Note 7: This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V ±10%, t_r, t_f ≤ 6 ns (*Figures 1, 2, 3,* and *4*) (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	S1 Open	2	6	11	ns
Skew	(Note 8)	S1 Open	0	0.5	3	ns
t_{TLH}, t_{THL}	Differential Output Rise And Fall Times	S1 Open		6	10	ns
t_{PZH}	Output Enable Time	S1 Closed		12	25	ns
t_{PZL}	Output Enable Time	S1 Closed		13	26	ns
t_{PHZ}	Output Disable Time (Note 9)	S1 Closed		4	8	ns
t_{PLZ}	Output Disable Time (Note 9)	S1 Closed		6	12	ns
C_{PD}	Power Dissipation Capacitance (Note 10)			100		pF
C_{IN}	Input Capacitance			6		pF

Note 8: Skew is defined as the difference in propagation delays between complementary outputs at the crossing point.

Note 9: Output disable time is the delay from the control input being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

Note 10: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 11: ESD Rating: HBM (1.5 kΩ, 100 pF)

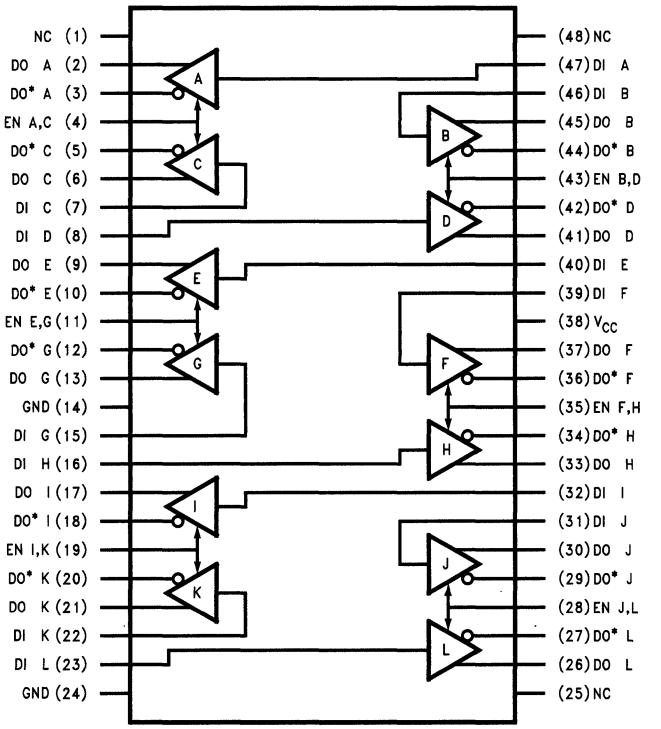
Inputs ≥ 1500V

Outputs ≥ 1000V

EIAJ (0Ω, 200 pF)

All Pins ≥ 350V

Logic Diagram



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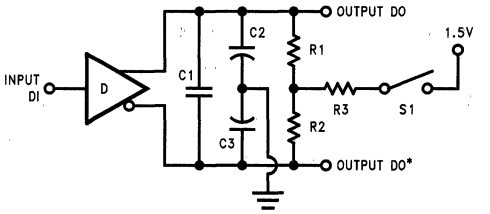
Parameter Measurement Information



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Note: C1 = C2 = C3 = 40 pF (including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω

FIGURE 1. AC Test Circuit

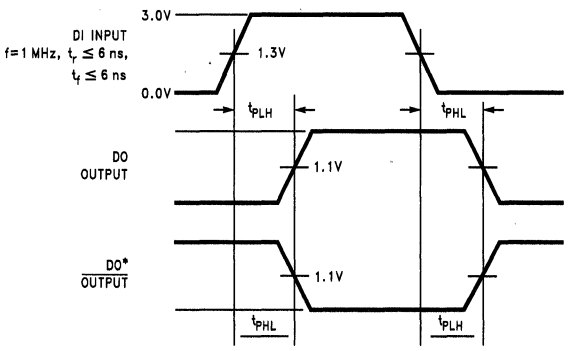

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FIGURE 2. Propagation Delays

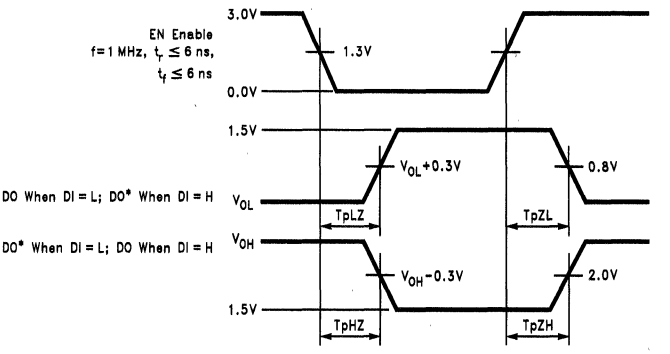

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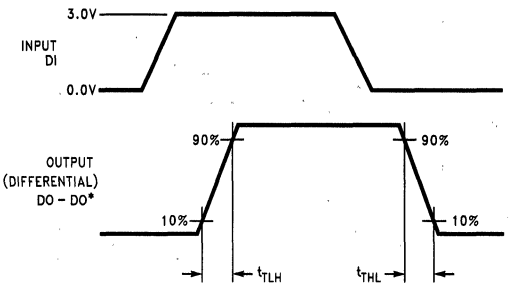
FIGURE 3. Enable and Disable Times



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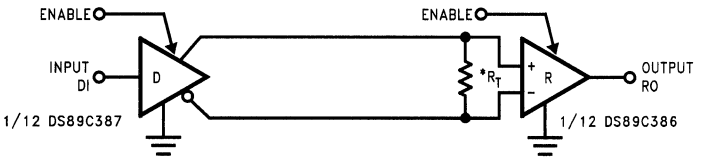
Input pulse; f = 1 MHz, 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

FIGURE 4. Differential Rise and Fall Times

Typical Application



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*R_T is optional although highly recommended to reduce reflection.

FIGURE 5. Two-Wire Balanced System, RS-422

Application Information

SKEW

Skew may be thought of in a lot of different ways, the next few paragraphs should clarify what is represented by "Skew" in the datasheet and how it is determined. Skew, as used in this databook, is the absolute value of a mathematical difference between two propagation delays. This is commonly accepted throughout the semiconductor industry. However, there is no standardized method of measuring propagation delay, from which skew is calculated, of differential line drivers. Elucidating, the voltage level, at which propagation delays are measured, on both input and output waveforms are not always consistant. Therefore, skew calculated in this datasheet, may not be calculated the same as skew defined in another. This is important to remember whenever making a skew comparison.

Skew may be calculated for the DS89C387, from many different propagation delay measurements. They may be classified into three categories, single-ended, differential, and complementry. Single-ended skew is calculated from t_{PHL} and t_{PLH} measurements (see *Figures 6* and *7*). Differential skew is calculated from t_{PHLD} and t_{PLHD} measurements (see *Figures 8* and *9*). Complementry skew is calculated from t_{PHL} and t_{PLH} measurements (see *Figures 10* and *11*).

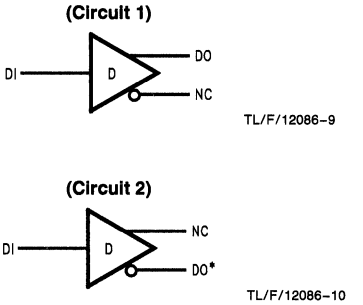

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FIGURE 6. Circuits for Measuring Single-Ended Propagation Delays (See *Figure 7*)

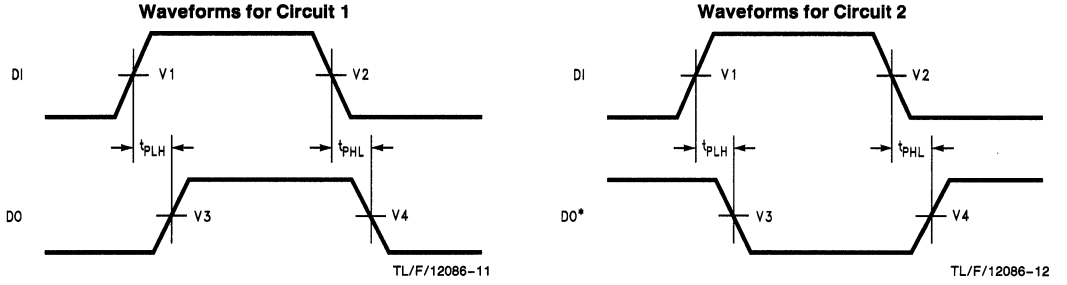

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FIGURE 7. Propagation Delay Waveforms for Circuit 1 and Circuit 2 (See *Figure 6*)

Application Information (Continued)

In *Figure 2*, VX, where X is a number, is the waveform voltage level at which the propagation delay measurement either starts or stops. Furthermore, V1 and V2 are normally identical. The same is true for V3 and V4. However, as mentioned before, these levels are not standardized and may vary, even with similar devices from other companies. Also note, NC (no connection) in *Figure 1* means the pin is not used in propagation delay measurement for the corresponding circuit.

The single-ended skew provides information about the pulse width distortion of the output waveform. The lower the skew, the less the output waveform will be distorted. For best case, skew would be zero, and the output duty cycle would be 50%, assuming the input has a 50% duty cycle.

(Circuit 3)

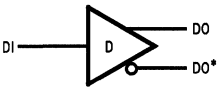

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FIGURE 8. Circuit for Measuring Differential Propagation Delays (See *Figure 9*)

Waveforms for Circuit 3

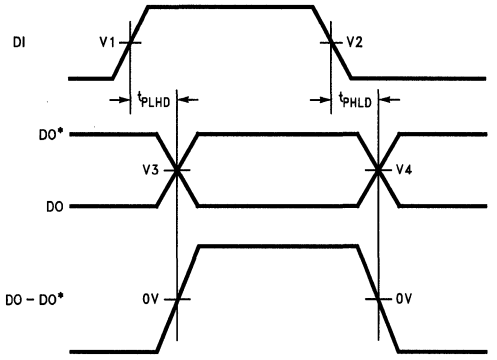

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FIGURE 9. Propagation Delay Waveforms for Circuit 3 (See *Figure 8*)

For differential propagation delays, V1 should equal V2. Furthermore, the crossing point of DO and DO* corresponds to zero volts on the differential waveform (see bottom waveform in *Figure 9*). This is true whether V3 equals V4 or not. However, if V3 and V4 are specified voltages, then V3 and V4 are less likely to be equal to the crossing point voltage. Thus, the differential propagation delays will not be measured to zero volts on the differential waveform.

The differential skew also provides information about the pulse width distortion of the differential output waveform relative to the input waveform. The higher the skew, the greater the distortion of the differential output waveform. Assuming the input has a 50% duty cycle, the differential output will have a 50% duty cycle if skew equals zero and less than a 50% duty cycle if skew is greater than zero.

(Circuit 4)

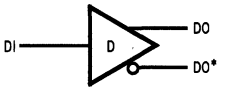

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FIGURE 10. Circuit for Measuring Complementary Skew (See *Figure 11*)

Waveforms for Circuit 4

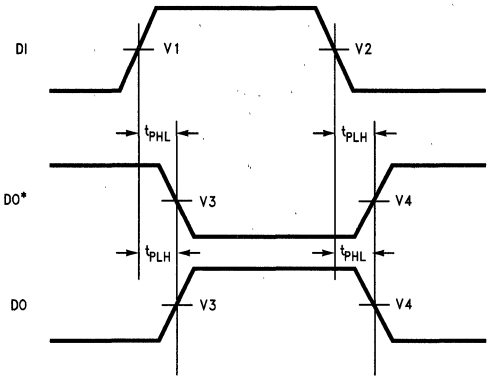

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FIGURE 11. Waveforms for Circuit 4 (See *Figure 10*)

Complementary skew is calculated from single-ended propagation delay measurements on complementary output signals, DO and DO*. Note, when V3 and V4 are absolute values, they are identical on DO and DO*; but vary whenever they are relative values.

Application Information (Continued)

The complementary skew reveals information about the contour of the rising and falling edge of the differential output signal of the driver. This is important information because the receiver will interpret the differential output signal. If the differential transitions do not continuously ascend or decend through the receivers threshold region, errors may occur. Errors may also occur if the transitions are too slow.

In addition, complementary skew provides information about the common mode modulation of the driver. The common mode voltage is represented by (DO−DO*)/2. This information may be used as a means for determining EMI affects.

Only "Skew" is specified in this datasheet for the DS89C387. It refers to the complementary skew of the driver. Complementary skew is measured at both V3 and V4 (see *Figure 11*).

More information can be calculated from the propagation delays. The channel to channel and device to device skew may be calculated in addition to the types of skew mentioned previously. These parameters provide timing performance information beneficial when designing. The channel to channel skew is calculated from the variation in propagation delay from receiver to receiver within one package. The device to device skew is calculated from the variation in propagation delay from one DS89C387 to another DS89C387.

For the DS89C387, the maximum channel to channel skew is 9 ns (t_p max−t_p min) where t_p is the low to high or high to low propagation delay. The minimum channel to channel skew is 0 ns since it is possible for all 12 drivers to have identical propagation delays. Note, this is best and worst case calculations used whenever Skew (channel) is not independently characterized and specified in the datasheet. The device to device skew may be calculated in the same way and the results are the same. Therefore, the device to device skew is 9 ns and 0 ns maximum and minimum respectively.

TABLE I. DS89C387 Skew Table

Parameter	Min	Typ	Max	Units
Skew (comp.)	0	0.5	3	ns
Skew (channel)	0		9	ns
Skew (device)	0		9	ns

Note Skew (comp.) in Table I is the same as "Skew" in the datasheet. Also Skew (channel) and Skew (device) are calculations, but are guaranteed by the propagation delay tests. Both Skew (channel) and Skew (device) would normally be tighter whenever specified from characterization data.

The information in this section of the datasheet is to help clarity how skew is defined in this datasheet. This should help when designing the DS89C387 into most applications.

DS89C387 Equivalent Input/Output Circuits

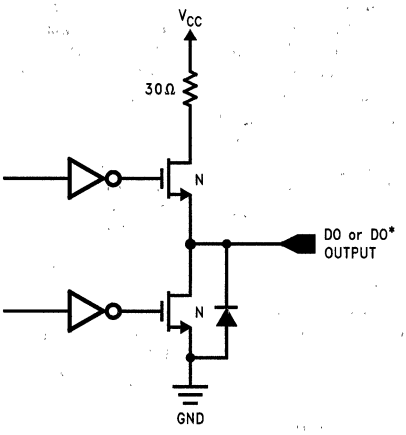

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FIGURE 12. Driver Output Equivalent Circuit

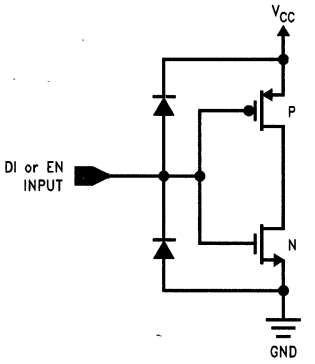

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FIGURE 13. Driver Input or Driver Enable Equivalent Circuit

Pin Descriptions

TABLE II. Device Pin Names and Descriptions

Pin #	Pin Name	Pin Description
7, 8, 15, 16, 22, 23, 31, 32, 39, 40, 46, 47	DI	TTL/CMOS Compatible Driver Input
2, 6, 9, 13, 17, 21, 26, 30, 33, 37, 41, 45	DO	Non-Inverting Driver Output Pin
3, 5, 10, 12, 18, 20, 27, 29, 34, 36, 44, 44	DO*	Inverting Driver Output Pin
4, 11, 19, 28, 35, 43	EN	Active High Dual Driver Enabling Pin
38	V_{CC}	Positive Power Supply Pin $+5 \pm 10\%$
14, 24	GND	Device Ground Pin
1, 25, 48	NC	Unused Pin (NOT CONNECTED)

National Semiconductor

DS9636A
RS-423 Dual Programmable Slew Rate Line Driver

General Description

The DS9636A is a TTL/CMOS compatible, dual, single ended line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The DS9636A is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control lead (WS) and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current-limiting is provided in both output states. The DS9636A is designed for nominal power supplies of ±12V.

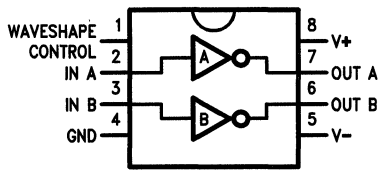
Inputs are TTL compatible with input current loading low enough (1/10 UL) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

Features

- Programmable slew rate limiting
- Meets EIA Standard RS-423
- Commercial or extended temperature range
- Output short circuit protection
- TTL and CMOS compatible inputs

Connection Diagram

8-Lead DIP



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Top View

Order Number DS9636ACJ, DS9636ACN or DS9636AMJ
See NS Package Number J08A or N08E

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS9636AJ/883
See NS Package Number J08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 seconds): 300°C
- Molded DIP (Soldering, 10 seconds): 265°C

Maximum Power Dissipation* at 25°C (Note 5)
- Cavity Package: 1560 mW
- Molded Package: 1300 mW

V+ Lead Potential to Ground Lead: V− to +15V

V− Lead Potential to Ground Lead: +0.5V to −15V

V+ Lead Potential to V− Lead: 0V to +30V

Output Potential to Ground Lead: ±15V

Output Source Current: −150 mA

Output Sink Current: 150 mA

Recommended Operating Conditions

Characteristics	DS9636AM			DS9636AC			Units
	Min	Typ	Max	Min	Typ	Max	
Positive Supply Voltage (V+)	10.8	12	13.2	10.8	12	13.2	V
Negative Supply Voltage (V−)	−13.2	−12	−10.8	−13.2	−12	−10.8	V
Operating Temperature (T_A)	−55	25	125	0	25	70	°C
Wave Shaping Resistance (R_{WS})	10		500	10		1000	kΩ

Electrical Characteristics Over recommended operating temperature, supply voltage and wave shaping resistance ranges unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH1}	Output Voltage HIGH	R_L to GND ($R_L = \infty$)	5.0	5.6	6.0	V
V_{OH2}		R_L to GND (R_L = 3.0 kΩ)	5.0	5.6	6.0	V
V_{OH3}		R_L to GND (R_L = 450Ω)	4.0	5.5	6.0	V
V_{OL1}	Output Voltage LOW	R_L to GND ($R_L = \infty$)	−6.0	−5.7	−5.0	V
V_{OL2}		R_L to GND (R_L = 3.0 kΩ)	−6.0	−5.6	−5.0	V
V_{OL3}		R_L to GND (R_L = 450Ω)	−6.0	−5.4	−4.0	V
R_O	Output Resistance	450Ω ≤ R_L		25	50	Ω
I_{OS+}	Output Short Circuit Current (Note 4)	V_O = 0V, V_I = 0V	−150	−60	−15	mA
I_{OS-}		V_O = 0V, V_I = 2.0V	15	60	150	mA
I_{CEX}	Output Leakage Current	V_O = ±6.0V, Power-Off	−100		+100	μA
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{IC}	Input Clamp Diode Voltage	I_I = 15 mA	−1.5	−1.1		V
I_{IL}	Input Current LOW	V_I = 0.4V	−80	−16		V
I_{IH}	Input Current HIGH	V_I = 2.4V		1.0	10	μA
		V_I = 5.5V		10	100	
I+	Positive Supply Current	V_{CC} = ±12V, $R_L = \infty$, R_{WS} = 100 kΩ, V_I = 0V		13	18	mA
I−	Negative Supply Current	V_{CC} = ±12V, $R_L = \infty$, R_{WS} = 100 kΩ, V_I = 0V	−18	−13		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for the DS9636AM and across the 0°C to +70°C range for the DS9636AC. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

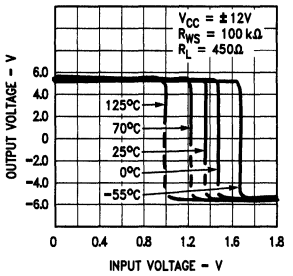
Note 5: Ratings apply to ambient temperature at 25°C. Above this temperature, derate J and N packages 10.4 mW/°C.

Switching Characteristics $V_{CC} = \pm 12V \pm 10\%$, $T_A = 25°C$, see AC Test Circuit

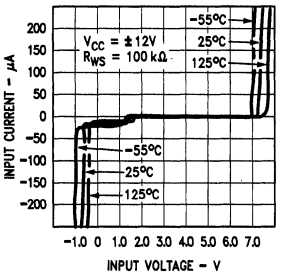
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r	Rise Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	
t_f	Fall Time	$R_{WS} = 10\ k\Omega$	0.8	1.1	1.4	μs
		$R_{WS} = 100\ k\Omega$	8.0	11	14	
		$R_{WS} = 500\ k\Omega$	40	55	70	
		$R_{WS} = 1000\ k\Omega$	80	110	140	

Typical Performance Characteristics

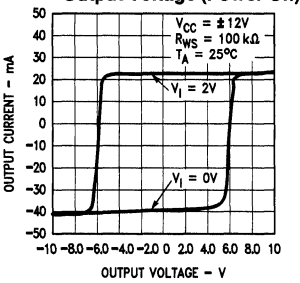
Input/Output Transfer Characteristic vs Temperature



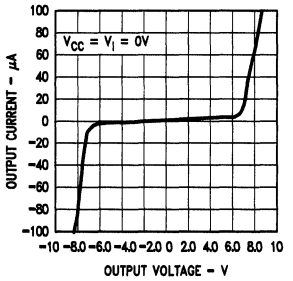
Input Current vs Input Voltage



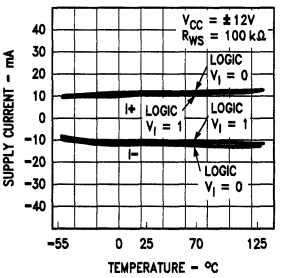
Output Current vs Output Voltage (Power On)



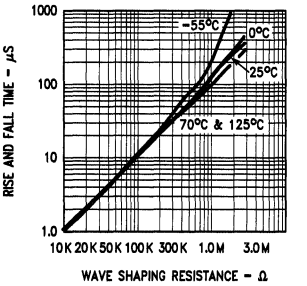
Output Current vs Output Voltage (Power Off)



Supply Current vs Temperature



Transition Time vs R_{WS}



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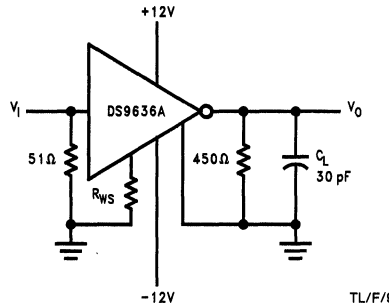

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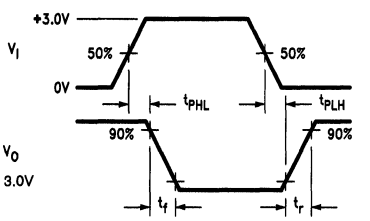
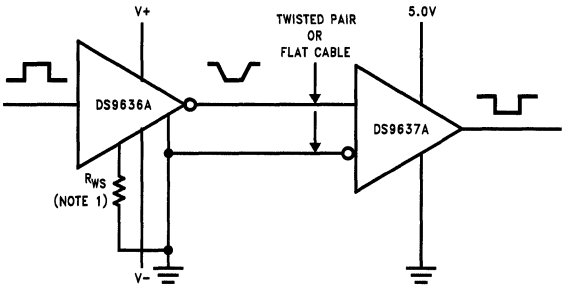


V_I V_O
Amplitude: 3.0V
Offset: 0V
Pulse Width: 500 µs
PRR: 1.0 kHz
$t_r = t_f \leq 10$ ns

TL/F/9620-5

Note: C_L includes jig and probe capacitance

FIGURE 1. AC Test Circuit and Waveforms



TL/F/9620-6

FIGURE 2. RS-423 System Application

National Semiconductor

DS9637A
Dual Differential Line Receiver

General Description

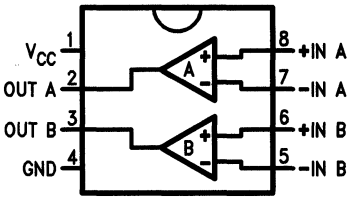
The DS9637A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the DS9637A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9637A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5V power supply and has Schottky TTL compatible outputs. The DS9637A has an operational input common mode range of ±7V either differentially or to ground.

Features

- Dual channel
- Single 5V supply
- Satisfies EIA standards RS-422 and RS423
- Built-in ±35 mV hysteresis
- High input common mode voltage range
- High input impedance
- TTL compatible outputs
- Schottky technology
- Extended temperature range

Connection Diagram

8-Lead DIP and SO-8 Package



TL/F/9621–1

Top View

Order Number DS9637ACJ, DSA9637AMJ, DS9637ACM or DS9637ACN
See NS Package Number J08A, M08A or N08E

For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number DS9637AMJ/883
See NS Package Number J08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to + 175°C
- Molded DIP: −65°C to + 150°C

Lead Temperature
- Ceramic DIP (Soldering, 30 seconds): 300°C
- Molded DIP and SO Package (Soldering, 10 seconds): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1300 mW
- Molded Package: 930 mW
- SO Package: 810 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW/°C above 25°C.

V_{CC} Lead Potential to Ground	−0.5V to 7.0V
Input Potential to Ground	±15V
Differential Input Voltage	±15V
Output Potential to Ground	−0.5V to +5.5V
Output Sink Current	50 mA

Recommended Operating Conditions

DS9637AM	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temperature (T_A)	−55	+125	°C
DS9637AC			
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics

Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold Voltage (Note 5)	$-7.0V \le V_{CM} \le +7.0V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage (Note 6)	$-7.0V \le V_{CM} \le +7.0V$	−0.4		+0.4	V
I_I	Input Current (Note 7)	$V_I = 10V, 0V \le V_{CC} \le +5.5V$		1.1	3.25	mA
		$V_I = -10V, 0V \le V_{CC} \le +5.5V$		−1.6	−3.25	
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA, V_{CC} = Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	I_{OH} = −1.0 mA, V_{CC} = Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current (Note 4)	V_O = 0V, V_{CC} = Max	−40	−75	−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I+ = 0.5V, V_I- = GND		35	50	mA
V_{HYST}	Input Hysteresis	V_{CM} = ±7.0V (See Curves)		70		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range for DS9637AM and across the 0°C to +70°C range for the DS9637ASC. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

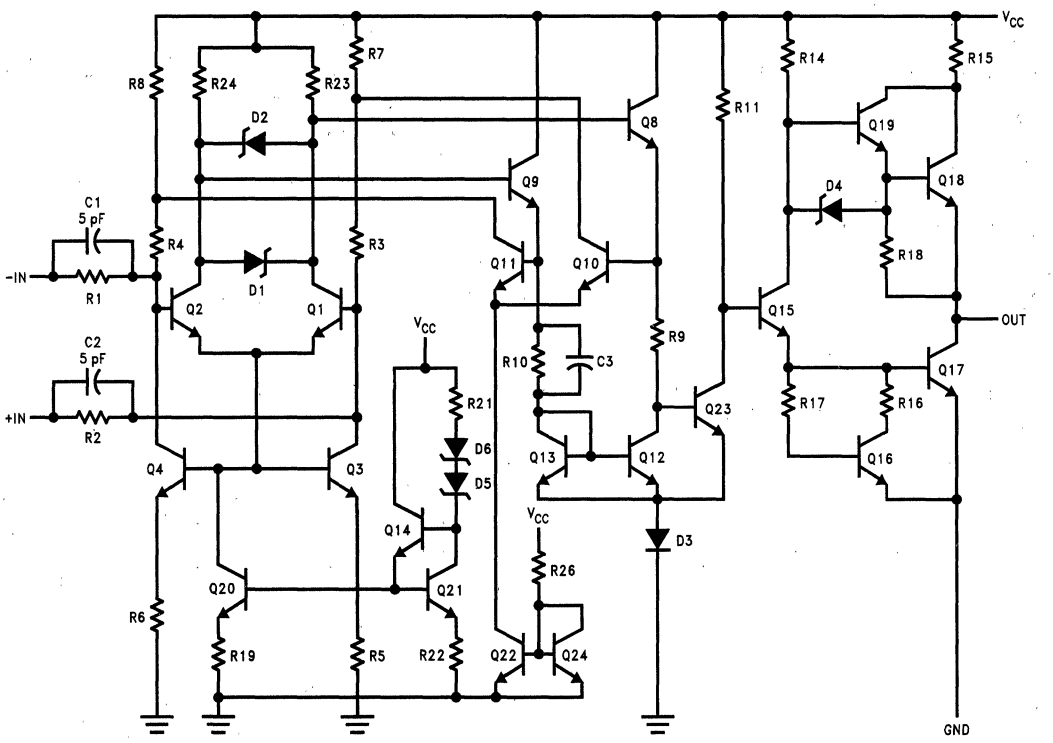
Note 5: V_{DIFF} (Differential Input Voltage) = $(V_I+) - (V_I-)$. V_{CM} (Common Mode Input Voltage) = V_I+ or V_I-.

Note 6: 500Ω ±1% in series with inputs.

Note 7: The input not under test is tied to ground.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

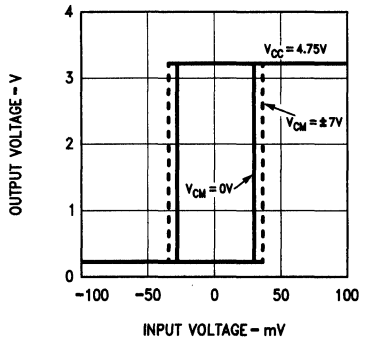
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		15	25	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		13	25	ns



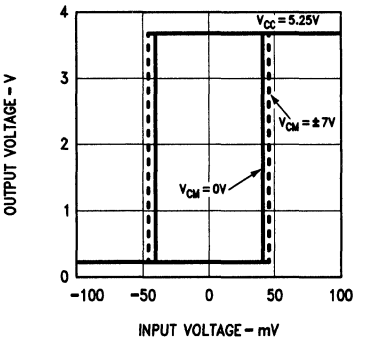
TL/F/9621–2

FIGURE 1. Equivalent Circuit

Typical Input/Output Transfer Characteristics

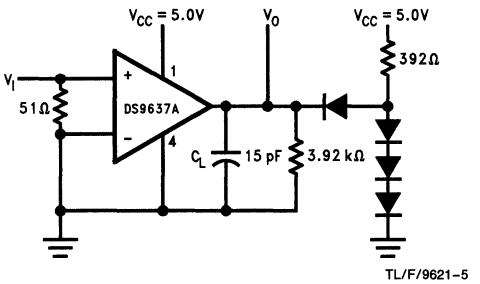


TL/F/9621–3



TL/F/9621–4

AC Test Circuit and Waveforms



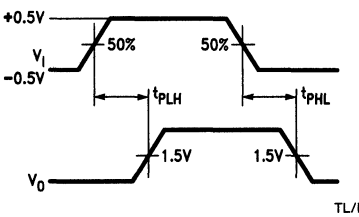
TL/F/9621–5

Notes:

C_L includes jig and probe capacitance.

All diodes are FD700 or equivalent.

FIGURE 2



TL/F/9621–6

V_I

Amplitude: 1.0V

Offset: 0.5V

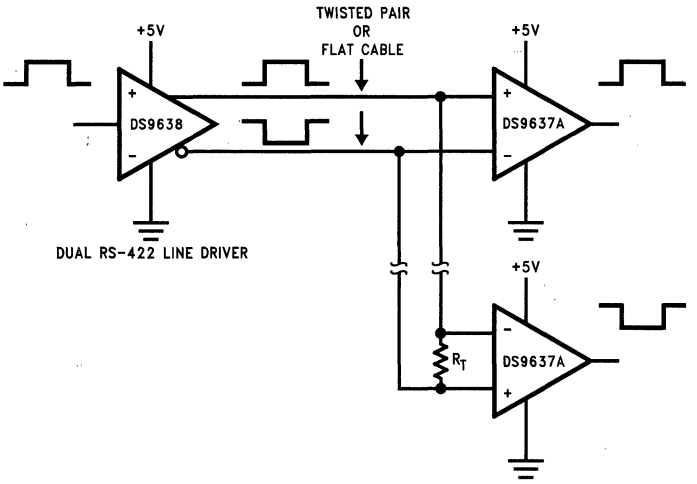
Pulse Width: 100 ns

PRR: 5.0 MHz

$t_r = t_f \leq 5.0$ ns

FIGURE 2a

Typical Applications



TL/F/9621–7

FIGURE 3. RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission

Notes:

$R_T \geq 50\Omega$ for RS-422 operation.

R_T combined with input impedance of receivers must be greater than 90Ω.

National Semiconductor

DS9638
RS-422 Dual High Speed Differential Line Driver

General Description

The DS9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50Ω transmission lines at high speed. The mini-DIP provides high package density.

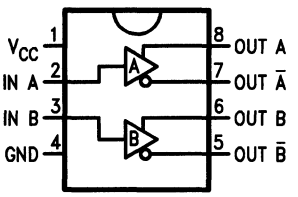
Features

- Single 5V supply
- Schottky technology
- TTL and CMOS compatible inputs
- Output short circuit protection
- Input clamp diodes
- Complementary outputs
- Minimum output skew (<1.0 ns typical)
- 50 mA output drive capability for 50Ω transmission lines
- Meets EIA RS-422 specifications
- Propagation delay of less than 10 ns
- "Glitchless" differential output
- Delay time stable with V_{CC} and temperature variations (<2.0 ns typical) *(Figure 3)*
- Extended temperature range

3

Connection Diagram

8-Lead DIP



TL/F/9622–1

Top View

Order Number DS9638CJ, DS9638MJ, DS9638CM or DS9638CN
See NS Package Number J08A, M08A or N08E

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS9638MJ/883
See NS Package Number J08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-8: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Cavity Package: 1300 mW
- Molded Package: 930 mW
- SO Package: 810 mW

V_{CC} Lead Potential to Ground: −5V to 7V

Input Voltage: −0.5V to +7V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C; derate SO package 6.5 mW°C above 25°C.

Recommended Operating Conditions

	DS9638M			DS9638C			
	Min	Typ	Max	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	4.75	5.0	5.25	V
Output Current HIGH (I_{OH})			−50			−50	mA
Output Current LOW (I_{OL})			50	40		50	mA
Operating Temperature (T_A)	−55	25	125	0	25	70	°C

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW	0°C to +70°C				0.8	V
		−55°C to +125°C				0.5	
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.0	−1.2	V
V_{OH}	Output Voltage HIGH	V_{CC} = Min, V_{IH} = $V_{IH\ Min}$, V_{IL} = $V_{IL\ Max}$	I_{OH} = −10 mA	2.5	3.5		V
			I_{OH} = −40 mA	2.0			
V_{OL}	Output Voltage LOW	V_{CC} = Min, V_{IH} = $V_{IH\ Min}$, V_{IL} = $V_{IL\ Max}$, I_{OL} = 40 mA				0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, $V_{I\ Max}$ = 5.5V				50	μA
I_{IH}	Input Current HIGH	V_{CC} = Max, V_{IH} = 2.7V				25	μA
I_{IL}	Input Current LOW	V_{CC} = Max, V_{IL} = 0.5V				−200	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V (Note 4)		−50		−150	mA
V_T, $\overline{V}_T$	Terminated Output Voltage	See *Figure 1*		2.0			V
V_T−$\overline{V}_T$	Output Balance					0.4	V
V_{OS}, $\overline{V}_{OS}$	Output Offset Voltage					3.0	V
V_{OS}−$\overline{V}_{OS}$	Output Offset Balance					0.4	V
I_X	Output Leakage Current	T_A = 25°C, −0.25V < V_X < 5.5V				100	μA
I_{CC}	Supply Current (Both Drivers)	V_{CC} = 5.5V, All input at 0V, No Load			45	65	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics provide conditions for actual device operation.

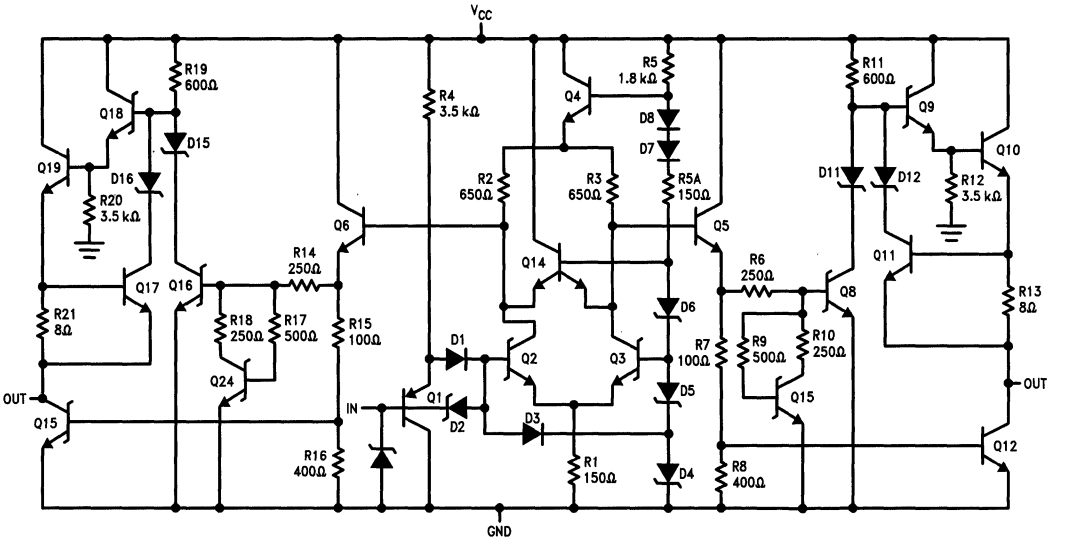
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS9638M and across the 0°C to +70°C range for the DS9638C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C.

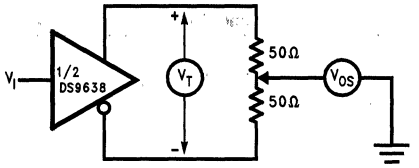
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay	C_L = 15 pF R_L = 100Ω, See *Figure 2*		10	20	ns
t_{PLH}				10	20	ns
t_f	Fall Time, 90%–10%			10	20	ns
t_r	Rise Time, 10%–90%			10	20	ns
$t_{PO}-t_{\overline{PO}}$	Skew Between Outputs A/$\overline{A}$ and B/$\overline{B}$			1.0		ns



TL/F/9622–2

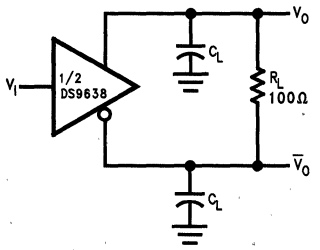
FIGURE 1. Equivalent Circuit

DC Test Circuit

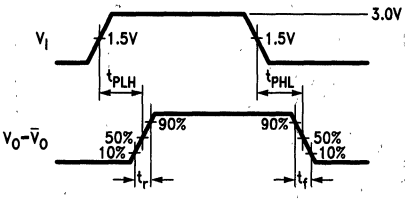


TL/F/9622–3

FIGURE 2. Terminated Output Voltage and Output Balance



TL/F/9622–4



TL/F/9622–5

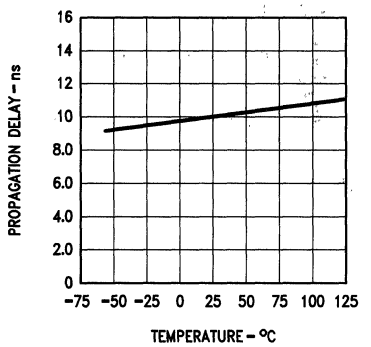
Note:

The pulse generator has the following characteristics:
PRR = 500 kHz, t_W = 100 ns,
$t_r \leq 5.0$ ns, Z_O = 50Ω.

C_L includes probe and jig capacitance.

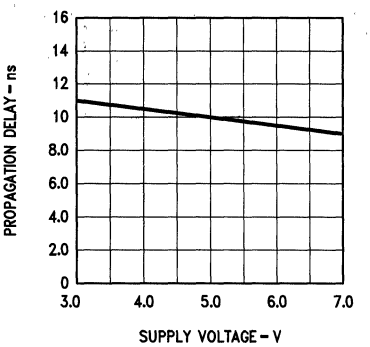
FIGURE 3. AC Test Circuit and Voltage Waveform

FIGURE 3a



TL/F/9622–6

FIGURE 4. Typical Delay Characteristics



TL/F/9622–7

FIGURE 4a

National Semiconductor

DS9639A
Dual Differential Line Receiver

General Description

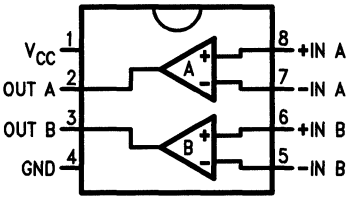
The DS9639A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422, RS-423 and RS-232C. In addition, the DS9639A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9639A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5.0V power supply and has Schottky TTL compatible outputs. The DS9639A has an operational input common mode range of ±7.0V either differentially or to ground.

Features

- Dual channel
- Single 5.0V supply
- Satisfies EIA Standards RS-422, RS-423 and RS-232C
- Built-in ±35 mV hysteresis
- High input common mode voltage range
- High input impedance
- TTL compatible outputs
- Schottky technology

Connection Diagram

8-Lead DIP



TL/F/9623–1

Top View

Order Number DS9639ACN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Molded DIP (soldering, 10 sec.)	265°C
V_{CC} Lead Potential to Ground	−0.5V to +7.0V
Input Potential to Ground Lead	±25V
Differential Input Voltage	±25V
Output Differential to Ground Lead	−0.5V to 5.5V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	930 mW

*Derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics Over recommended operating temperature and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions (Note 1)	Min	Typ	Max	Units
V_{TH}	Differential Input Threshold Voltage (Note 5)	$-7.0V \le V_{CM} \le +7.0V$	−0.2		+0.2	V
$V_{TH(R)}$	Differential Input Threshold Voltage (Note 6)	$-7.0V \le V_{CM} \le +7.0V$	−0.4		+0.4	V
I_I	Input Current (Note 7)	$V_I = 10V, 0V \le V_{CC} \le 5.5V$		1.1	3.25	mA
		$V_I = -10V, 0V \le V_{CC} \le 5.5V$		−1.6	−3.25	
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA, V_{CC} = Min		0.35	0.5	V
V_{OH}	Output Voltage HIGH	$I_{OH} = -1.0$ mA, V_{CC} = Min	2.5	3.5		V
I_{OS}	Output Short Circuit Current (Note 4)	V_O = 0V, V_{CC} = Max	−40	−75	−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_I+ = 0.5V, V_I- = GND		35	50	mA
V_{HYST}	Input Hysteresis	V_{CM} = ±7.0V (See Curves)		70		mV

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High	See AC Test Circuit		55	85	ns
t_{PHL}	Propagation Delay Time High to Low	See AC Test Circuit		50	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS9639A. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

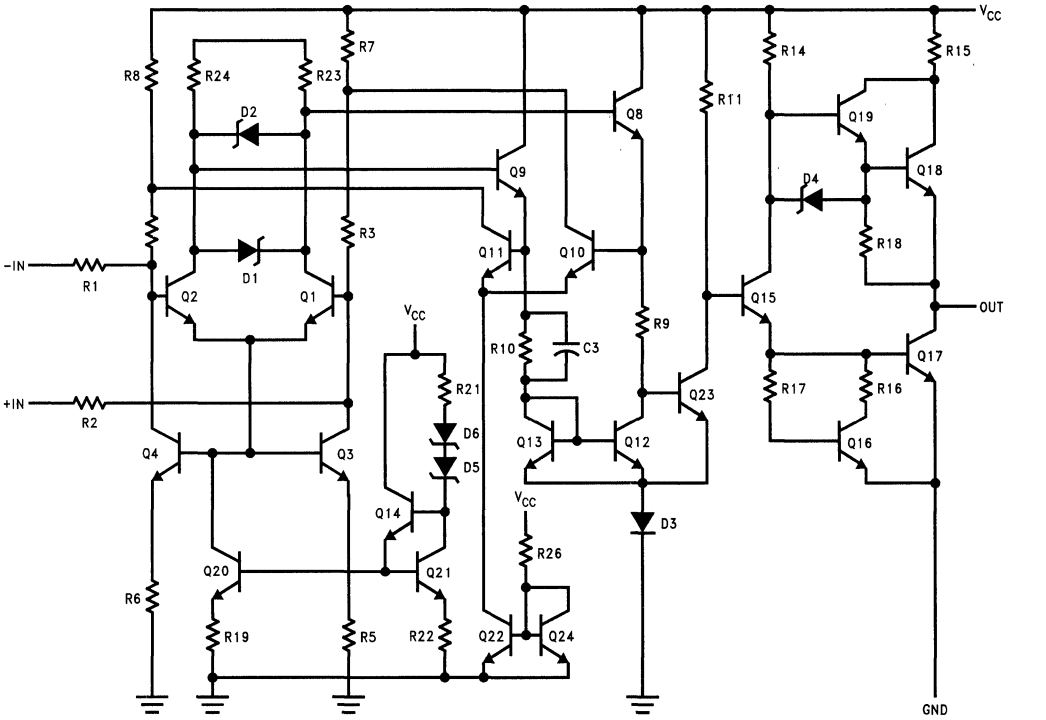
Note 4. Only one output at a time should be shorted.

Note 5: V_{DIFF} (Differential Input Voltage) = $(V_{I+}) - (V_{I-})$. V_{CM} (Common Mode Input Voltage) = V_{I+} or V_{I-}.

Note 6: 500Ω ±1% in series with inputs.

Note 7: The input not under test is tied to ground.

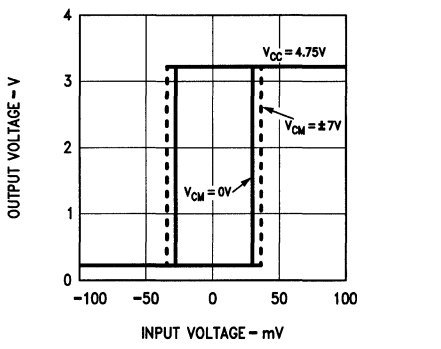
Equivalent Circuit



TL/F/9623-2

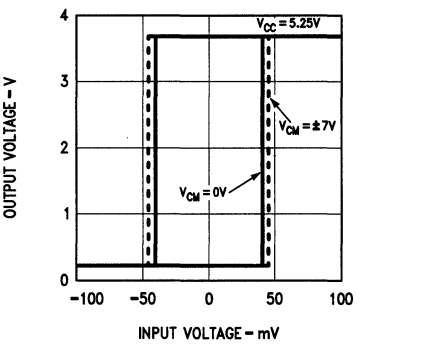
FIGURE 1. Equivalent Circuit

Typical Input/Output Transfer Characteristics



TL/F/9623-3

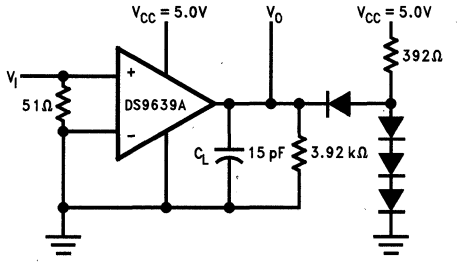
FIGURE 2



TL/F/9623-4

FIGURE 2a

AC Test Circuit and Switching Time Waveform



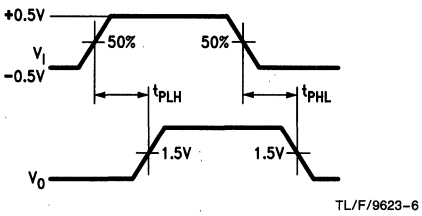
TL/F/9623–5

Notes:

C_L includes jig and probe capacitance.

All diodes are FD700 or equivalent.

FIGURE 3. AC Test Circuit and Waveforms



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V_I

Amplitude: 1.0V

Offset: 0.5V

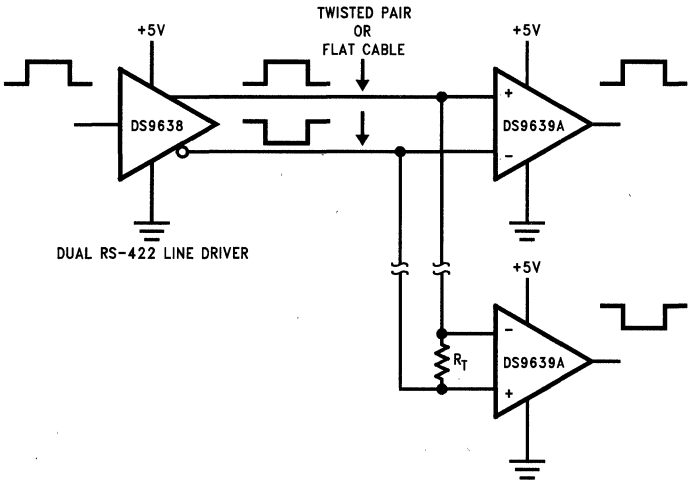
Pulse Width: 500 ns

PRR: 1 MHz

$t_r = t_f \leq 5.0$ ns

FIGURE 3a

Typical Applications



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Notes:

$R_t \geq 50\Omega$ for RS-422 operation.

R_t combined with input impedance of receivers must be greater than 90Ω.

FIGURE 4. RS-422 System Application (FIPS 1020) Differential Simplex Bus Transmission

Section 4

RS-485 Multipoint Line Drivers, Receivers and Transceivers

Section 4 Contents

National Semiconductor

DS3695/DS3695T/DS3696/DS3696T/DS3697/DS3698 Multipoint RS485/RS422 Transceivers/Repeaters

General Description

The DS3695, DS3696, DS3697 and DS3698 are high speed differential TRI-STATE® bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission.

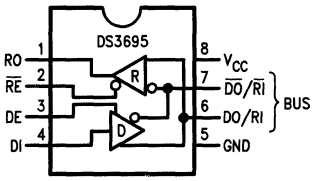
The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 and DS3698 provide an output pin TS (thermal shutdown) which reports the occurrence of the thermal shutdown of the device. This is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422
- 15 ns driver propagation delays with 2 ns skew (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis

Connection and Logic Diagrams



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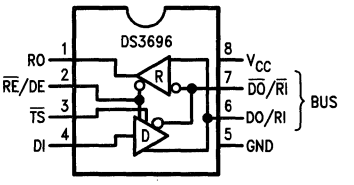
Top View



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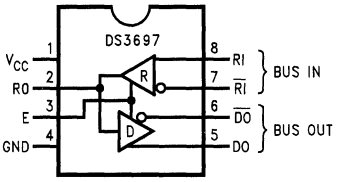
Top View



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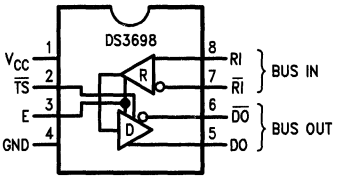
Top View



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Top View

Order Number DS3695N, DS3696N, DS3697N, DS3698N, DS3695TN, DS3696TN, DS3695TJ or DS3696TJ
See NS Package Number J08A or N08E

Note: $\overline{TS}$ pin was $\overline{LF}$ (Line Fault) in previous datasheets and reports the occurrence of a thermal shutdown of the device.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/−10V
Receiver Input Voltages (DS3695, DS3696)	+15V/−10V
Receiver Common Mode Voltage (DS3697, DS3698)	±25V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C N Package	1.07W (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temp. (T_A)			
Commercial	0	+70	°C
Industrial	−40	+85	°C

Electrical Characteristics $0°C \le T_A \le +70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 5)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage for Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E, $\overline{RE}$/DE			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}$/$\overline{RI}$ RI, $\overline{RI}$	$V_{CC} = 0V$ or 5.25V $\overline{RE}$/DE or DE = 0V	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
I_{OZD}	TRI-STATE Current DS3697 & DS3698	DO, $\overline{DO}$	$V_{CC} = 0V$ or 5.25V, E = 0V $-7V < V_O < +12V$				±100	μA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ μA		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 5)				0.5	V
		$\overline{TS}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 5)	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA

Electrical Characteristics (Continued)

$0°C \leq T_A \leq +70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 5)			−250	mA
		$V_O = +12V$ (Note 5)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 11.1 mW/°C to 570 mW at 70°C.

Note 5: All limits for which Note 5 is applied must be derated by 10% for DS3695T and DS3696T. Other parameters remain the same for this extended temperature range device ($-40°C \leq T_A \leq +85°C$).

Switching Characteristics

$0°C \leq T_A \leq +70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 3, 6)

Receiver Switching Characteristics *(Figures 2, 3 and 4)*

Symbol	Conditions	Min	Typ	Max	Units
t_{PLH}	$C_L = 15$ pF S1 and S2 Closed	15	25	37	ns
t_{PHL}		15	25	37	ns
$\lvert t_{PLH} - t_{PHL} \rvert$		0			ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	5	12	16	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	5	12	16	ns
t_{PZL}	$C_L = 15$ pF, S2 Open	7	15	20	ns
t_{PZH}	$C_L = 15$ pF, S1 Open	7	15	20	ns

Driver Switching Characteristics

Symbol	Conditions	Min	Typ	Max	Units
SINGLE ENDED CHARACTERISTICS *(Figures 5, 6 and 7)*					
t_{PLH}	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	9	15	22	ns
t_{PHL}		9	15	22	ns
$t_{SKEW} \lvert t_{PLH} - t_{PHL} \rvert$			2	8	ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	7	15	30	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	7	15	30	ns
t_{PZL}	$C_L = 100$ pF, S2 Open	30	35	50	ns
t_{PZH}	$C_L = 100$ pF, S1 Open	30	35	50	ns
DIFFERENTIAL CHARACTERISTICS *(Figures 5 and 8)*					
t_r, t_f	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	6	10	18	ns

Note 6: Switching Characteristics apply for DS3695, DS3695T, DS3696, DS3696T, DS3697 only.

AC Test Circuits and Switching Waveforms

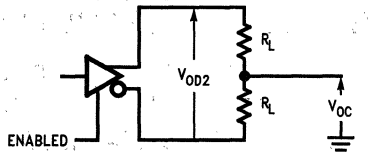

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FIGURE 1. Driver V_{OD} and V_{OC}

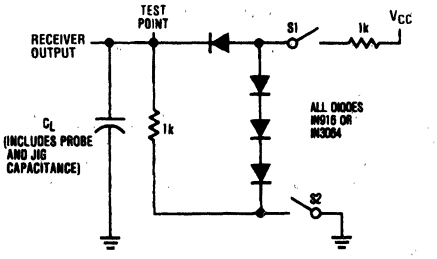

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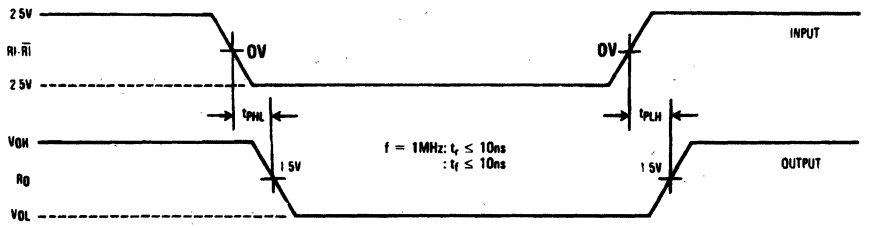
FIGURE 2. Receiver Propagation Delay Test Circuit



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Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V.

FIGURE 3. Receiver Input-to-Output Propagation Delay Timing

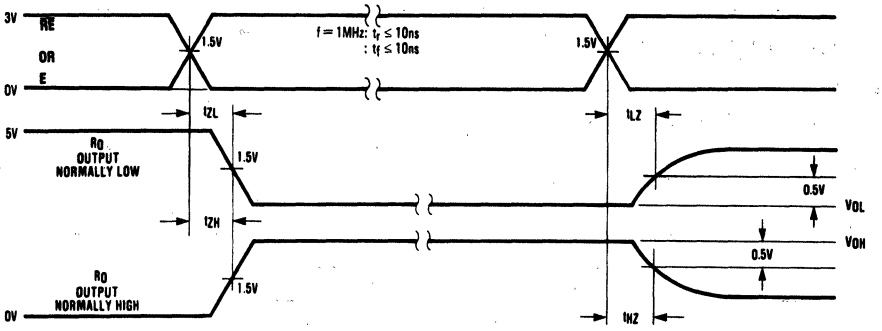

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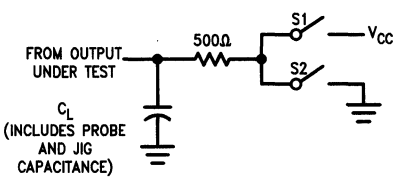
FIGURE 4. Receiver Enable/Disable Propagation Delay Timing

AC Test Circuits and Switching Waveforms (Continued)



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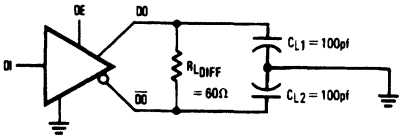

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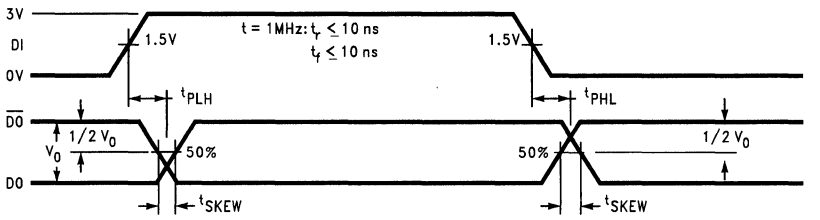
Note: Unless otherwise specified the switches are closed.

FIGURE 5. Driver Propagation Delay and Transition Time Test Circuits



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Note: t_{PLH} and t_{PHL} are measured to the respective 50% points. t_{SKEW} is the difference between propagation delays of the complementary outputs.

FIGURE 6. Driver Input-to-Output Propagation Delay Timing (Single-Ended)

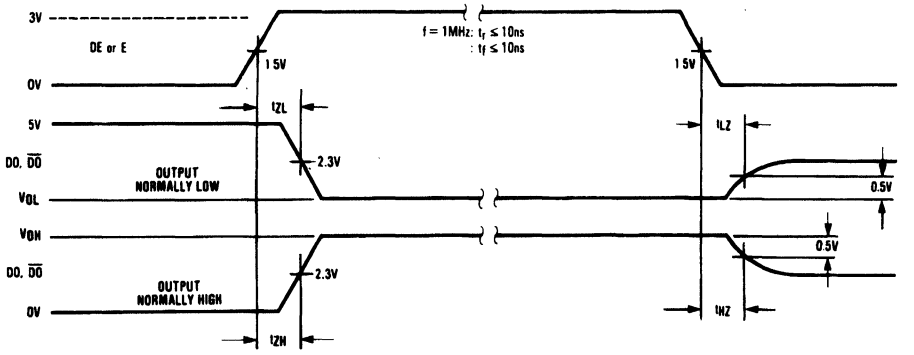

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FIGURE 7. Driver Enable/Disable Propagation Delay Timing

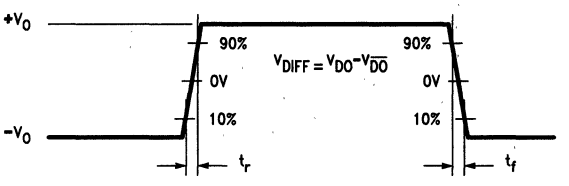

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FIGURE 8. Driver Differential Transition Timing

Function Tables

DS3695/DS3696 Transmitting

Inputs			Thermal Shutdown	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{TS}$* (DS3696 Only)
X	1	1	OFF	0	1	H
X	1	0	OFF	1	0	H
X	0	X	OFF	Z	Z	H
X	1	X	ON	Z	Z	L

DS3695/DS3696 Receiving

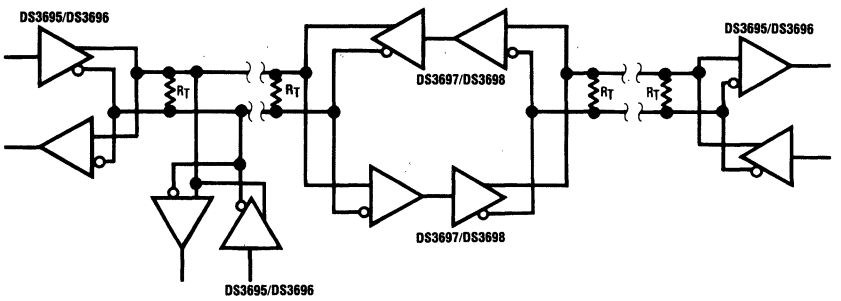
Inputs			Outputs	
$\overline{RE}$	DE	RI-$\overline{RI}$	RO	$\overline{TS}$* (DS3696 Only)
0	0	$\geq +0.2V$	1	H
0	0	$\leq -0.2V$	0	H
1	0	X	Z	H

DS3697/DS3698

Inputs		Thermal Shutdown	Outputs			
E	RI-$\overline{RI}$		$\overline{DO}$	DO	RO (DS3697 Only)	$\overline{TS}$* (DS3698 Only)
1	$\geq +0.2V$	OFF	0	1	1	H
1	$\leq -0.2V$	OFF	1	0	0	H
0	X	OFF	Z	Z	Z	H
1	$\geq +0.2V$	ON	Z	Z	1	L
1	$\leq -0.2V$	ON	Z	Z	0	L

X—Don't care condition
Z—High impedance state
*$\overline{TS}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor that reports the occurrence of a thermal shutdown of the device.

Typical Application



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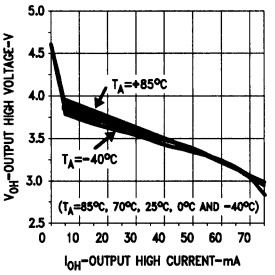
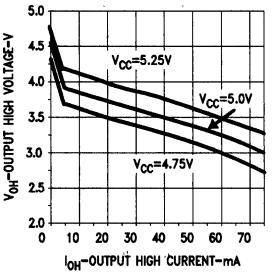
Note: Repeater control logic not shown, see AN-702.

Typical Performance Characteristics

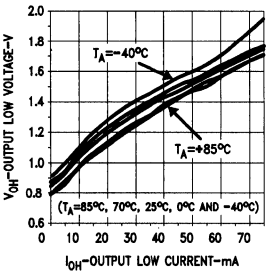
Driver V_{OH} vs I_{OH} vs Temperature



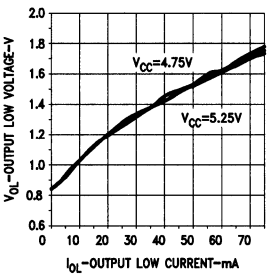
Driver V_{OH} vs I_{OH} vs V_{CC}



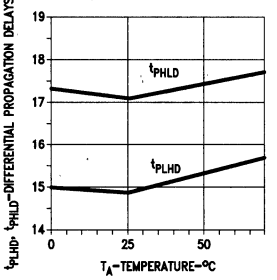
Driver V_{OL} vs I_{OL} vs Temperature



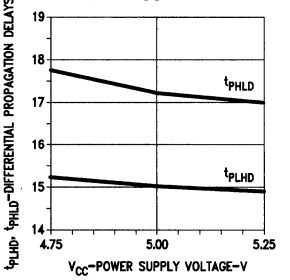
Driver V_{OL} vs I_{OL} vs V_{CC}



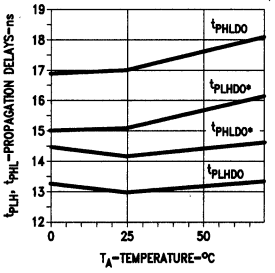
Driver Differential Propagation Delay vs Temperature



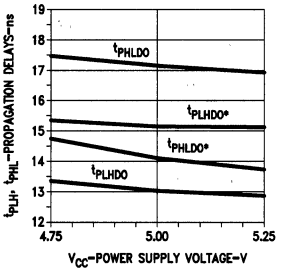
Driver Differential Propagation Delay vs V_{CC}



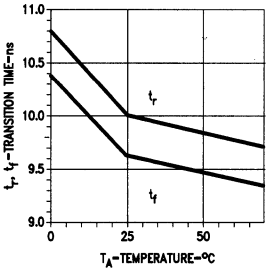
Driver Single-Ended Propagation Delay vs Temperature



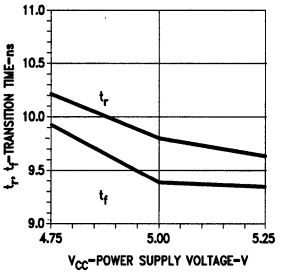
Driver Single-Ended Propagation Delay vs V_{CC}



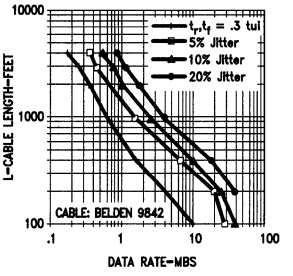
Driver Transition Time vs Temperature



Driver Transition Time vs V_{CC}



Cable Length vs Data Rate



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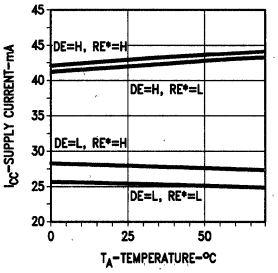
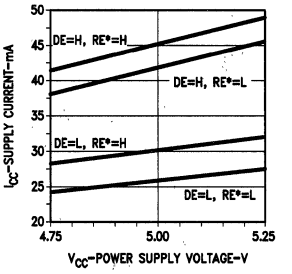
Typical Performance Characteristics (Continued)

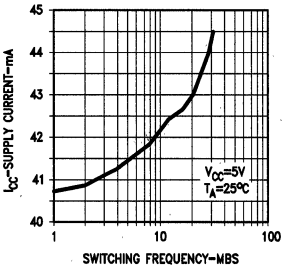
Supply Current vs Temperature



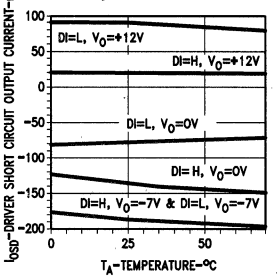
Supply Current vs Power Supply Voltage



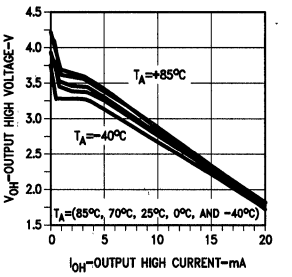
Driver I_{CC} vs Switching Frequency



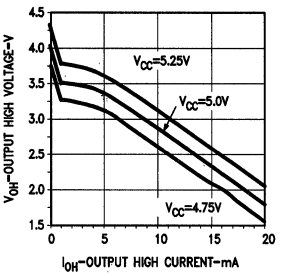
Driver Short Circuit Current vs Temperature



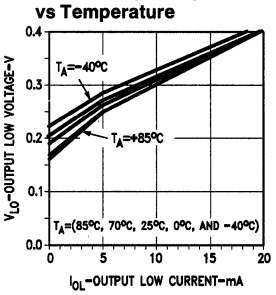
Receiver V_{OH} vs I_{OH} vs Temperature



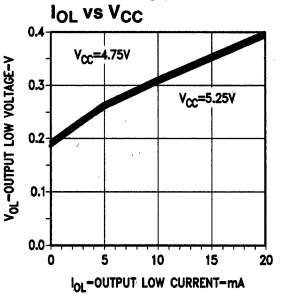
Receiver V_{OH} vs I_{OH} vs V_{CC}



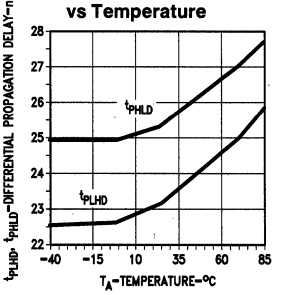
Receiver V_{OL} vs I_{OL} vs Temperature



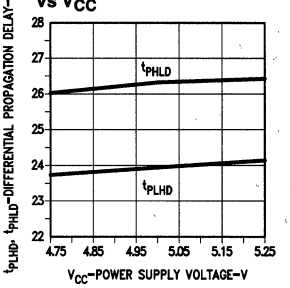
Receiver V_{OL} vs I_{OL} vs V_{CC}



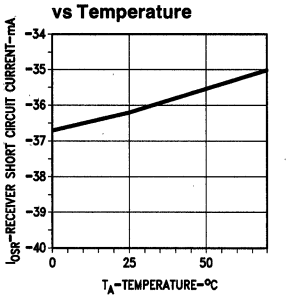
Receiver Differential Propagation Delay vs Temperature



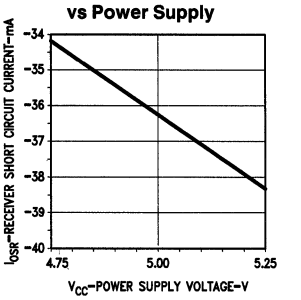
Receiver Differential Propagation Delay vs V_{CC}



Receiver Short Circuit Current vs Temperature



Receiver Short Circuit Current vs Power Supply



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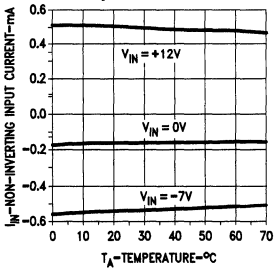
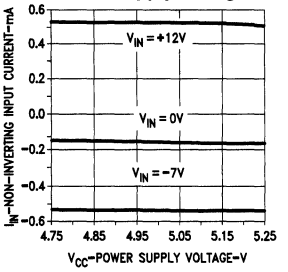
Typical Performance Characteristics (Continued)

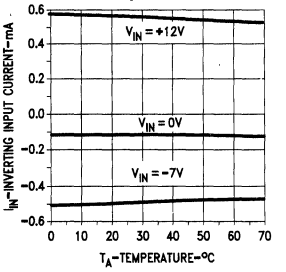
Receiver Non-Inverting Input Current vs Temperature



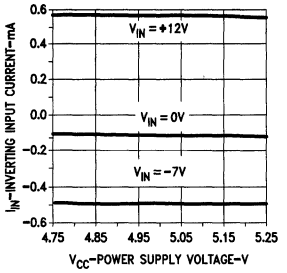
Receiver Non-Inverting Input Current vs Power Supply Voltage



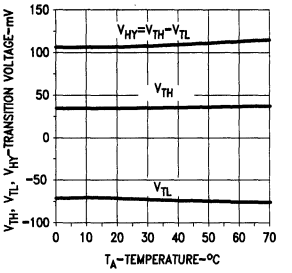
Receiver Inverting Input Current vs Temperature



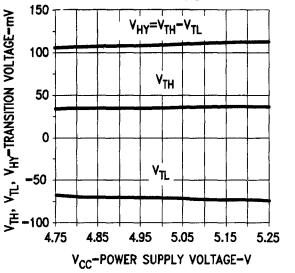
Receiver Inverting Input Current vs Power Supply Voltage



Hysteresis and Differential Transition Voltage vs Temperature



Hysteresis and Differential Transition Voltage vs V_{CC}



TL/H/10408–18

National Semiconductor

DS3695A/DS3695AT/DS3696A Multipoint RS485/RS422 Transceivers

General Description

The DS3695A and DS3696A are high speed differential TRI-STATE® bus/line transceivers designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition they are compatible with requirements of RS-422.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696A provides an output pin (TS) which reports the thermal shutdown of the device. TS is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the TS outputs of several devices to be wire OR-ed.

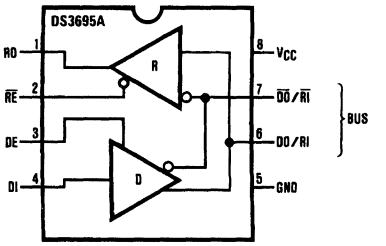
Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422
- 10 ns driver propagation delays (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis
- Available in SOIC packaging

Connection and Logic Diagram

Molded Package, Small Outline (M)



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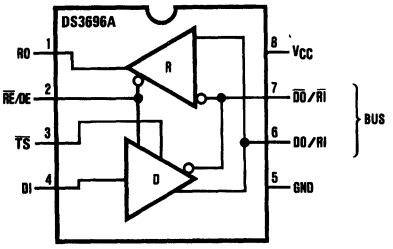
Top View



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Top View

Note: $\overline{TS}$ was $\overline{LF}$ (Line Fault) on previous datasheets, $\overline{TS}$ goes low upon thermal shutdown.

Order Number DS3695AM, DS3695ATM or DS3696AM
See NS Package Number M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/−10V
Receiver Input Voltages	+15V/−10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C M Package	630 mW (Note 4)
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temp. (T_A)			
Commercial (DS3695AM)	0	+70	°C
Industrial (DS3695ATM)	−40	+85	°C
Commercial (DS3696AM)	0	+70	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)			R = 50Ω; (RS-422) (Note 5)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States						0.2	V
V_{OC}	Driver Common Mode Output Voltage			R = 27Ω			3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, $R\overline{E}$/DE			2			V
V_{IL}	Input Low Voltage						0.8	V
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	V
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$	$V_{CC} = 0V$ or 5.25V	$V_{IN} = 12V$			+1.0	mA
		RI, $\overline{RI}$	DE or $R\overline{E}$/DE = 0V	$V_{IN} = -7V$			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ μA		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 5)				0.5	V
		$\overline{TS}$	$I_{OL} = 8$ mA				0.45	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		$V_{CC} = Max$, $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 5)	Driver Outputs Enabled		42	60	mA
				Driver Outputs Disabled		27	40	mA

Electrical Characteristics

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Notes 2 & 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 5)			−250	mA
		$V_O = +12V$ (Note 5)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 6.5 mW/°C to 337 mW at 70°C.

Note 5: All limits for which Note 5 is applied must be derated by 10% for DS3695AT. Other parameters remain the same for this extended temperature range device ($-40°C \le T_A \le +85°C$).

Switching Characteristics

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Note 3)

Receiver Switching Characteristics (*Figures 1, 2* and *3*)

Symbol	Conditions	Min	Typ	Max	Units
t_{PLH}	$C_L = 15$ pF S1 and S2 Closed	15	28	42	ns
t_{PHL}		15	28	42	ns
$\lvert t_{PLH} - t_{PHL} \rvert$		0	3		ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	5	29	35	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	5	12	16	ns
t_{PZL}	$C_L = 15$ pF, S2 Open	7	15	28	ns
t_{PZH}	$C_L = 15$ pF, S1 Open	7	15	20	ns

Driver Switching Characteristics

Symbol	Conditions	Min	Typ	Max	Units
SINGLE ENDED CHARACTERISTICS (*Figures 4, 5* and *6*)					
t_{PLH}	$R_{LDIFF} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	9	15	22	ns
t_{PHL}		9	15	22	ns
$t_{SKEW} \lvert t_{PLH} - t_{PHL} \rvert$		0	2	8	ns
t_{PLZ}	$C_L = 15$ pF, S2 Open	7	15	30	ns
t_{PHZ}	$C_L = 15$ pF, S1 Open	7	15	30	ns
t_{PZL}	$C_L = 100$ pF, S2 Open	30	35	50	ns
t_{PZH}	$C_L = 100$ pF, S1 Open	30	35	50	ns
DIFFERENTIAL SWITCHING CHARACTERISTICS (*Figure 7*)					
t_r, t_f	$R_{LDIFF} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF	6	10	18	ns

AC Test Circuits and Switching Waveforms

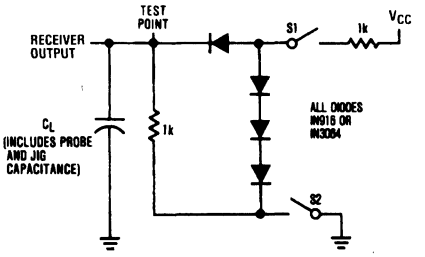

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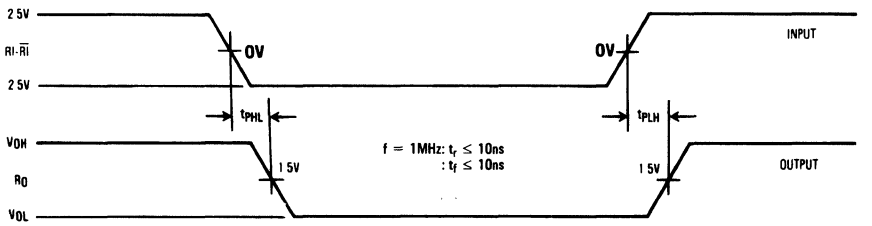
FIGURE 1. Receiver Propagation Delay Test Circuit



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Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 2. Receiver Input-to-Output Propagation Delay Timing

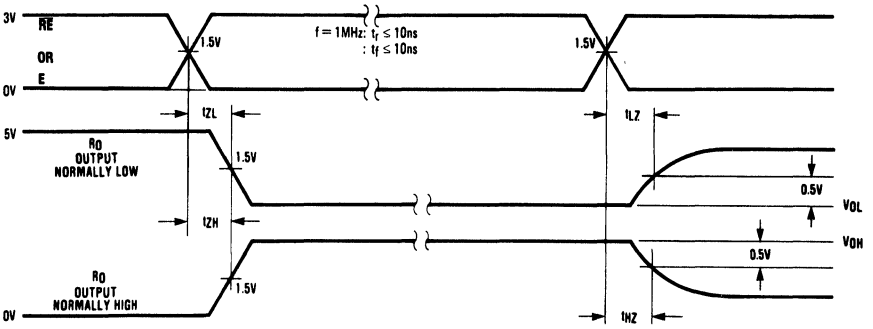

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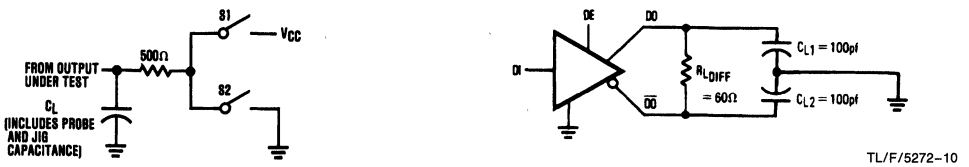
FIGURE 3. Receiver Enable/Disable Propagation Delay Timing

AC Test Circuits and Switching Waveforms (Continued)



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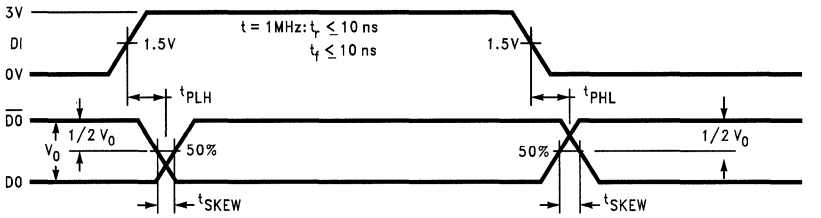
Note: Unless otherwise specified the switches are closed.

FIGURE 4. Driver Propagation Delay Test Circuits



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Note: t_{PLH} and t_{PHL} are measured to the respective 50% points. t_{SKEW} is the difference between propagation delays of the complementary outputs.

FIGURE 5. Driver Input-to-Output Propagation Delay Timing (Single-Ended)

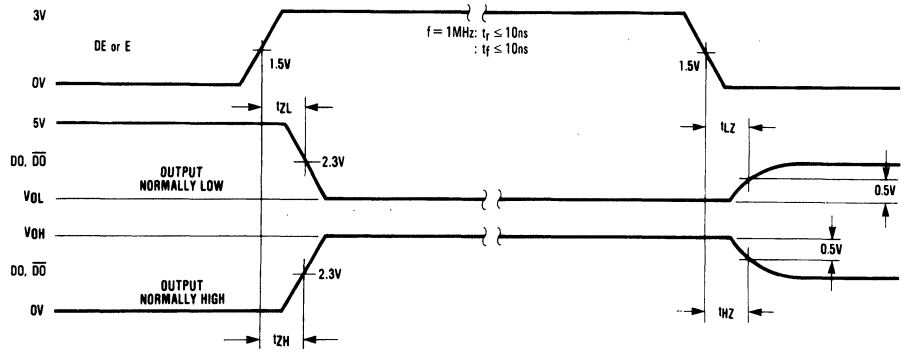

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FIGURE 6. Driver Enable/Disable Propagation Delay Timing

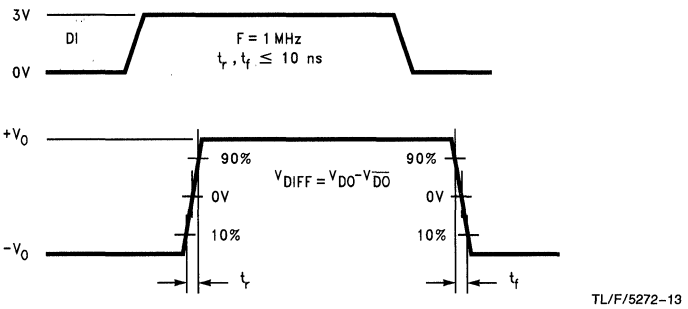

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FIGURE 7. Driver Differential Transition Timing

Function Tables

DS3695A/DS3696A Transmitting

Inputs			Line Condition	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{TS}$* (DS3696A Only)
X	1	1	No Fault	0	1	H
X	1	0	No Fault	1	0	H
X	0	X	X	Z	Z	H
X	1	X	Fault	Z	Z	L

DS3695A/DS3696A Receiving

Inputs			Output	
$\overline{RE}$	DE	RI–$\overline{RI}$	RO	$\overline{TS}$* (DS3696A Only)
0	0	$\geq +0.2V$	1	H
0	0	$\leq -0.2V$	0	H
0	0	Inputs Open**	1	H
1	0	X	Z	H

X — Don't care condition

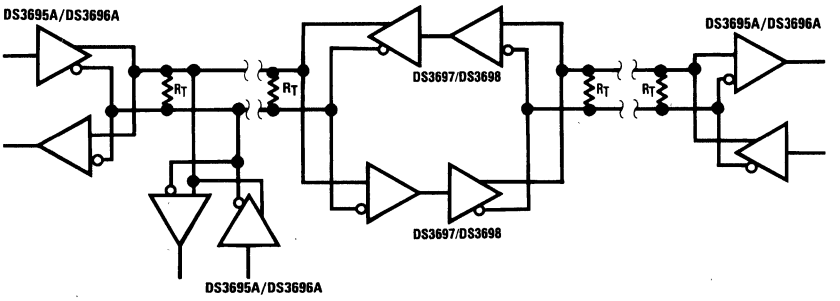
Z — High impedance state

Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

* $\overline{TS}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor.

** **This is a fail safe condition**

Typical Application



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Note: Repeater control logic not shown. See AN-702.

National Semiconductor

DS16F95, DS36F95
EIA-485/EIA-422A Differential Bus Transceiver

General Description

The DS16F95/DS36F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets both EIA-485 and EIA-422A standards.

The DS16F95/DS36F95 offers improved performance due to the use of L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by minimizing gate delay times. Thus, the DS16F95 and DS36F95 consume less power, and feature an extended temperature range as well as improved specifications.

The DS16F95/DS36F95 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

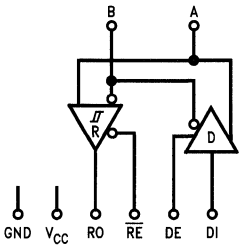
The driver is designed to accommodate loads of up to 60 mA of sink or source current and features positive and negative current limiting in addition to thermal shutdown for protection from line fault conditions.

The DS16F95/DS36F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Meets EIA-485 and EIA-422A
- Meets SCSI-1 (5 MHZ) specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Reduced power consumption
- Pin compatible with DS3695 and SN75176A
- Military temperature range available
- Qualified for MIL-STD 883C
- Standard Military Drawings (SMD) available
- Available in DIP (J), LCC (E), and Flatpak (W) packages

Logic Diagram



TL/F/9629–20

Function Tables

Driver

Driver Input	Enable	Outputs	
DI	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A-B	**$\overline{RE}$**	**RO**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C 'J' Package	1300 mW
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

*Derate 'J' package 8.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS36F95	4.75	5.0	5.25	V
DS16F95	4.50	5.0	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		+12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)				
DS36F95	0	+25	+70	°C
DS16F95	−55	+25	+125	°C

Driver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −55 mA	0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	I_{OL} = 55 mA	0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.3	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1*		1.5	2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*	−40°C to +125°C			±0.2	V
			−55°C to +125°C			±0.4	
V_{OC}	Common Mode Output Voltage (Note 5)					3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled	V_O = +12V			1.0	mA
			V_O = −7.0V			−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = +12V				250	
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE}$ = 0.8V Outputs Enabled			28	mA
I_{CCX}			DE = 0.8V, $\overline{RE}$ = 2V Outputs Disabled			25	

COMMERCIAL

Driver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 3*	8.0	15	20	ns
t_{TD}	Differential Output Transition Time		8.0	15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 4*	6.0	12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	16	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 5*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 6*		25	32	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 5*		20	25	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per *Figure 5* Timing per *Figure 6*		300		ns
t_{SKEW}	Skew (Pulse Width Distortion)	R_L = 60Ω, *Figure 3*		1.0	4.0	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V		35	50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.3	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 2*	0°C to +70°C	2.8			V
			−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 2*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = +12V			1.0	mA
			V_I = −7.0V			0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−50	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load, All Inputs Open	DE = 2V, $\overline{RE}$ = 0.8V Outputs Enabled			28	mA
I_{CCX}			DE = 0.8V, $\overline{RE}$ = 2V Outputs Disabled			25	

COMMERCIAL

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to +3.0V, C_L = 15 pF, *Figure 7*	14	19	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		14	19	24	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 8*		10	16	ns
t_{ZL}	Output Enable Time to Low Level			12	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 8*		12	20	ns
t_{LZ}	Output Disable Time from Low Level			12	18	ns
$\|t_{PLH} - t_{PHL}\|$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16F95 and across the 0°C to +70°C range for the DS36F95. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In TIA/EIA-422A and TIA/EIA-485 Standards, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_T+, and the negative-going input threshold voltage, V_T-.

Note 8: Refer to TIA/EIA-485 Standard for exact conditions.

Note 9: Only one output at a time should be shorted.

Order Number: DS16F95J, NS Package Number J08A
DS36F95J, NS Package Number J08A

MIL-STD 883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Power Dissipation* at 25°C	
Ceramic 'E' Package	1800 mW
Ceramic 'J' Package	1300 mW
Ceramic 'W' Package	TBD
Supply Voltage	7.0V
Input Voltage (Bus Terminal)	+15V/−10V
Enable Input Voltage	5.5V

*Above T_A = 25°C, derate E package, J package 8.7 mW/°C, W package 12.5 mW/°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS16F95	4.50	5.50	V
Voltage at Any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0	+12	V
Differential Input Voltage (V_{ID})		±12	V
Output Current HIGH (I_{OH})			
Driver		−60	mA
Receiver		−400	μA
Output Current LOW (I_{OL})			
Driver		60	mA
Receiver		16	mA
Operating Temperature (T_A)			
DS16F95	−55	+125	°C

Driver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Input Voltage HIGH	V_{CC} = 5.5V		2.0		V
V_{IL}	Input Voltage LOW	V_{CC} = 5.5V			0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA, V_{CC} = 4.5V		3.0		V
V_{OL}	Output Voltage LOW	I_{OL} = +20 mA, V_{CC} = 4.5V			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.3	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA, V_{IN} = 0.8V or 2V, V_{CC} = 5.5V			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, V_{CC} = 4.5V, *Figure 1*		2.0		V
		R_L = 54Ω, V_{CC} = 4.5V, *Figure 1*		1.5		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*, V_{CC} = 4.5V			±0.2	V
V_{OD3}	Differential Output Voltage	V_{CM} = −7V to +12V		1.0		V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)	V_{CC} = 4.5V, R_L = 54Ω or 100Ω			±0.2	V
I_O	Output Current (Note 8) (Includes Receiver I_I)	Output Disabled V_{CC} = 0V or 5.5V	V_O = +12V		1.0	mA
			V_O = −7.0V		−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V			20	μA
I_{IL}	Input Current LOW	V_I = 0.4V			−50	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V, V_{IN} = 0V or 3V			−250	mA
		V_O = 0V, V_{IN} = 0V or 3V			−150	
		V_O = V_{CC}, V_{IN} = 0V or 3V			150	
		V_O = +12V, V_{IN} = 0V or 3V			250	
I_{CC}	Supply Current (Total Package)	No Load, DE = 2V, $\overline{RE}$ = 0.8V, Inputs Open			28	mA
I_{CCX}		No Load, DE = 0.8V, $\overline{RE}$ = 2V, Inputs Open			25	

MIL-STD 883C

Driver Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	Min	Typ	T_A = 25°C Max	T_A = 125°C Max	T_A = −55°C Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 3*	8.0	15	25	30	30	ns
t_{TD}	Differential Output Transition Time		8.0	15	25	30	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 4*	6.0	12	18	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		6.0	12	18	25	25	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 5*		25	35	45	45	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 6*		25	40	50	50	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 5*		20	30	40	40	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 6*		20	30	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND	Load per *Figure 5* Timing per *Figure 6*		300				ns
t_{SKEW}	Skew (Pulse Width Distortion)	R_L = 60Ω, *Figure 3*		1.0	6	12	12	ns

Receiver Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.5V, I_O = −0.4 mA, V_{CM} = −7V, 0V, +12V V_{CC} = 4.5V, 5.5V			0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA, V_{CM} = −7V, 0V, +12V, V_{CC} = 4.5V, 5.5V		−0.2		V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V, V_{CC} = 4.5V, 5.5V		35		mV
V_{IH}	Enable Input Voltage HIGH			2.0		V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA, V_{CC} = 5.5V			−1.3	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 2*, V_{CC} = 4.5V	−55°C to +125°C	2.5		V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 2*, V_{CC} = 4.5V	I_{OL} = 8.0 mA		0.45	V
			I_{OL} = 16 mA		0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V, 2.4V			±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V V_{CC} = 5.5V or V_{CC} = 0V	V_I = +12V		1.0	mA
			V_I = −7.0V	−0.8		
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V			20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V			−50	μA
R_I	Input Resistance			10		kΩ
I_{OS}	Short Circuit Output Current	V_{IN} = 1V, V_{OUT} = 0.0V (Note 9)		−15	−85	mA
I_{CC}	Supply Current (Total Package)	No Load, DE = 2V, $\overline{RE}$ = 0.8V, Inputs Open			28	mA
I_{CCX}		No Load, DE = 0.8V, $\overline{RE}$ = 2.0V, Inputs Open			25	

MIL-STD 883C

Receiver Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	Min	Typ	T_A = 25°C Max	T_A = 125°C Max	T_A = −55°C Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to +3.0V C_L = 15 pF, *Figure 7*	10	19	27	38	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	19	27	38	38	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 8*		10	20	30	30	ns
t_{ZL}	Output Enable Time to Low Level			12	20	30	30	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 8*		12	20	30	30	ns
		C_L = 20.0 pF, *Figure 8* (Note 14)		12	30	40	40	ns
t_{LZ}	Output Disable Time from Low Level	C_{IL} = 50 pF, *Figure 8*		12	20	30	30	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 7*		1.0	8	16	16	ns

Ordering Number: **DS16F95J/883, NS Package Number J08A**
DS16F95E/883, NS Package Number E20A
DS16F95W/883, NS Package Number W10A

SMD Number: **DS16F95J/883 ⟷ 5962-896150PX**
DS16F95E/883 ⟷ 5962-8961502X
DS16F95W/883 ⟷ 5962-896150HX

Parameter Measurement Information

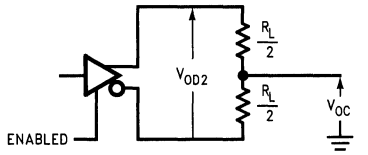


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FIGURE 1. Driver V_{OD} and V_{OC} (Note 13)

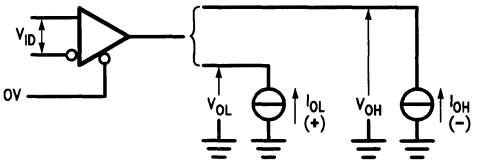

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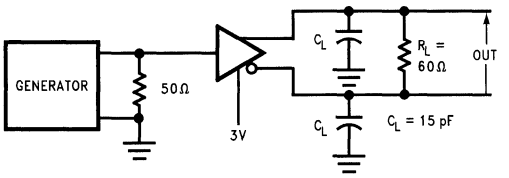
FIGURE 2. Receiver V_{OH} and V_{OL}



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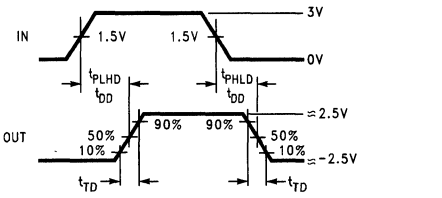

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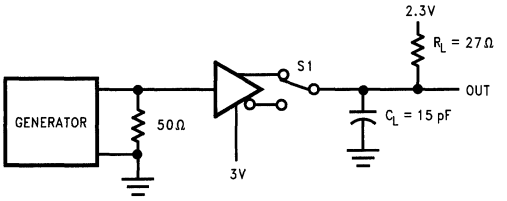
$t_{SKEW} = |t_{PLHD} - t_{PHLD}|$

FIGURE 3. Driver Differential Output Delay and Transition Times (Notes 10, 12)



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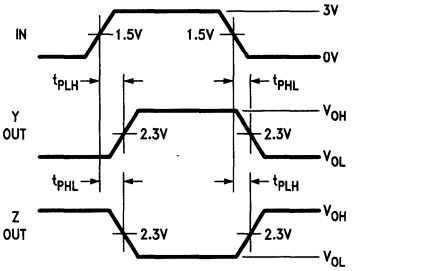

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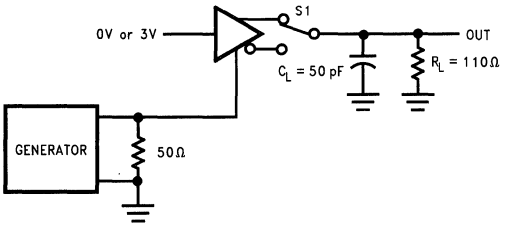
FIGURE 4. Driver Propagation Times (Notes 10, 11)



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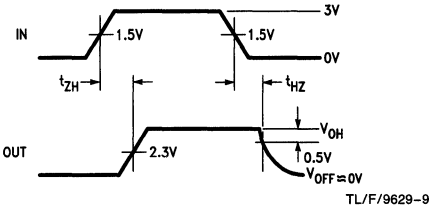

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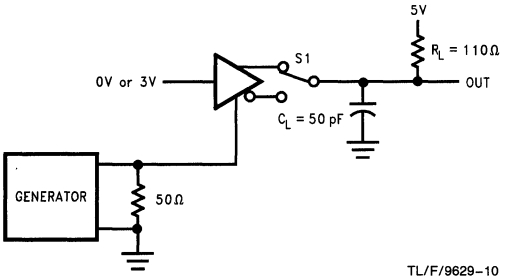
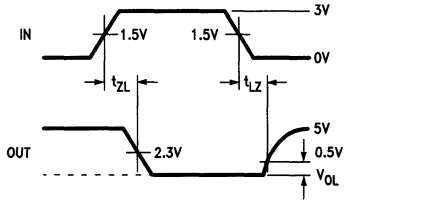
FIGURE 5. Driver Enable and Disable Times (t_{ZH}, t_{HZ}) (Notes 10, 11, 12)



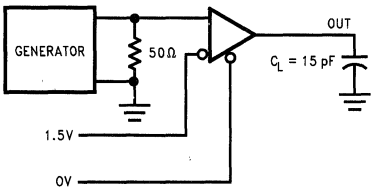
TL/F/9629–10



TL/F/9629–11

FIGURE 6. Driver Enable and Disable Times (t_{ZL}, t_{LZ}, t_{LZL}) (Notes 10, 11, 12)

Parameter Measurement Information (Continued)



TL/F/9629–12

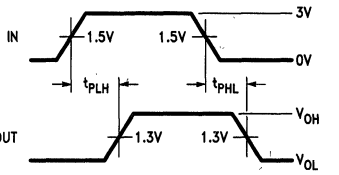


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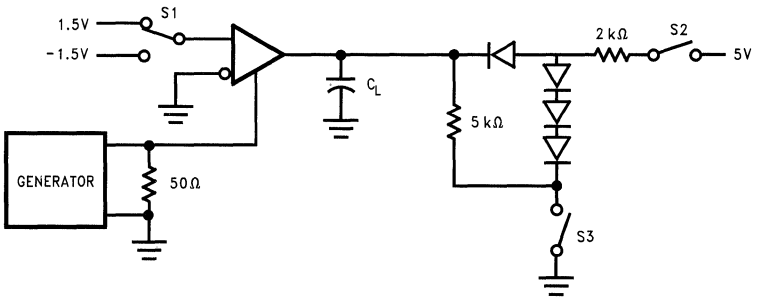
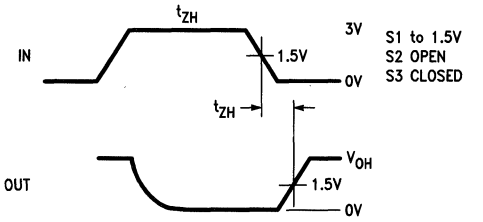
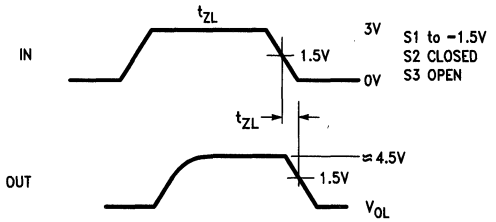
FIGURE 7. Receiver Propagation Delay Times (Notes 10, 11)



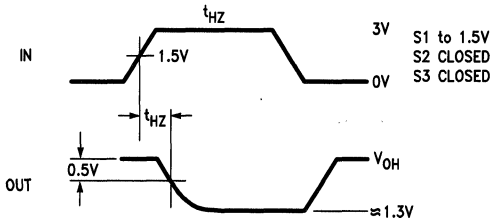
TL/F/9629–14



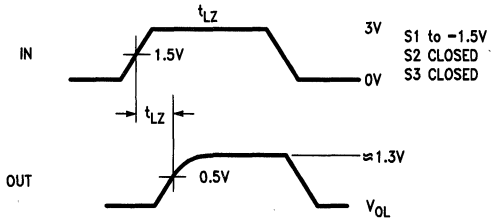
TL/F/9629–15



TL/F/9629–16



TL/F/9629–17



TL/F/9629–18

FIGURE 8. Receiver Enable and Disable Times (Notes 10, 11, 13)

Note 10: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

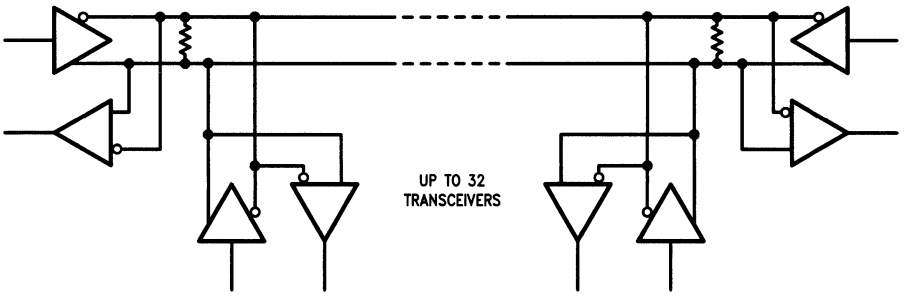
Note 11: C_L includes probe and stray capacitance.

Note 12: DS16F95/DS36F95 Driver enable is Active-High.

Note 13: All diodes are 1N916 or equivalent.

Note 14: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application



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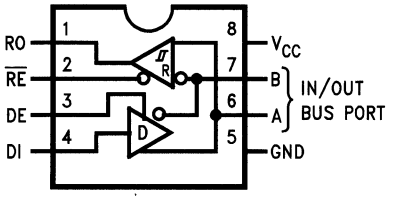
Note:

The line should be terminated at both ends in its characteristic impedance, typically 120Ω.
Stub lengths off the main line should be kept as short as possible.

Connection Diagrams

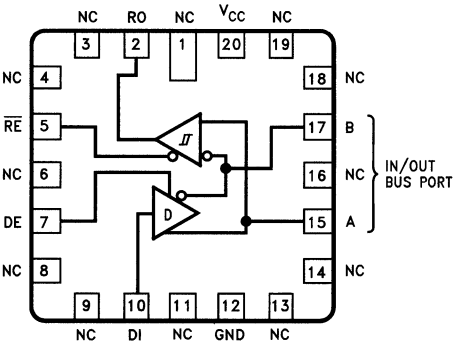
8-Lead Dual-In-Line Package



TL/F/9629–1

Order Number DS16F95, DS16F95J/883, DS36F95J
See NS Package Number J08A

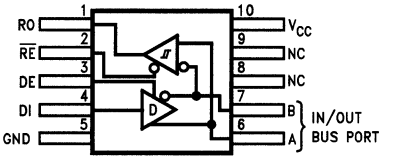
20-Lead Ceramic Leadless Chip Carrier



TL/F/9629–21

Order Number DS16F95E/883
See NS Package Number E20A

10-Lead Ceramic Flatpak



TL/F/9629–22

Order Number DS16F95W/883
See NS Package Number W10A

For Complete Military 883 Specifications, See RETS Data Sheet

National Semiconductor

DS36276
FAILSAFE Multipoint Transceiver

General Description

The DS36276 FAILSAFE Multipoint Transceiver is designed for use on bi-directional differential busses. It is compatible with existing TIA/EIA-485 transceivers, however, it offers an additional feature not supported by standard transceivers.

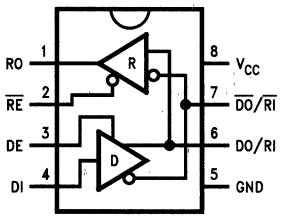
The FAILSAFE feature guarantees the receiver output to a known state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault conditions (open or short). The receiver output is in a HIGH state for the following conditions: OPEN Inputs, Terminated Inputs (50Ω), and SHORTED Inputs.

FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Compatible with popular interface standards:
  - — TIA/EIA-485 (RS-485)
  - — TIA/EIA-422-A (RS-422-A)
  - — CCITT Recommendation V.11
- Bi-Directional Transceiver
  - — Designed for multipoint transmission
- Separate driver input, driver enable, receiver enable, and receiver output for maximum flexibility
- Wide bus common mode range
  - — (−7V to +12V)
- Pin compatible with: DS75176B, DS96176, DS3695 and SN75176A and B
- Available in plastic DIP and SOIC packages

Connection and Logic Diagram



TL/F/11383–1

Order Number DS36276N or DS36276M
See NS Package Number N08E or M08A

Truth Tables

Driver

Inputs			Outputs	
$\overline{RE}$	DE	DI	DO/RI	$\overline{DO/RI}$
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

Receiver

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	≥0V	H
L	L	≤ −500 mV	L
H	X	X	Z

Receiver FAILSAFE

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	SHORTED	H
L	L	OPEN	H
H	X	X	Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage (DE, $\overline{RE}$, and DI)	5.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage (RO)	5.5V
Maximum Package Power Dissipation @ +25°C	
N Package (derate 9.3 mW/°C above +25°C)	1168 mW
M Package (derate 5.8 mW/°C above +25°C)	726 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Max Junction Temperature	150°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 6.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Temperature (T_A) DS36276	0	+70	°C

Electrical Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_{OD}	Differential Output Voltage	I_O = 0 mA (No Load)		1.5	4.8	6.0	V
V_{oDO}	Output Voltage	I_O = 0 mA (Output to GND)		0		6.0	V
$V_{o\overline{DO}}$	Output Voltage			0		6.0	V
V_{T1}	Differential Output Voltage (Termination Load)	R_L = 54Ω (485)	*(Figure 1)*	1.5	2.0	5.0	V
		R_L = 100Ω (422)		2.0	2.3	5.0	V
ΔV_{T1}	Balance of V_{T1} $\lvert V_{T1}\rvert - \lvert\overline{V_{T1}}\rvert$	R_L = 54Ω	(Note 3)	−0.2	0.07	+0.2	V
		R_L = 100Ω		−0.2	0.07	+0.2	V
V_{OS}	Driver Common Mode Output Voltage	R_L = 54Ω	*(Figure 1)*	0	2.5	3.0	V
		R_L = 100Ω		0	2.3	3.0	V
ΔV_{OS}	Balance of V_{OS} $\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	R_L = 54Ω	(Note 3)	−0.2	0.08	+0.2	V
		R_L = 100Ω		−0.2	0.08	+0.2	V
I_{OSD}	Driver Short-Circuit Output Current	V_O = +12V	*(Figure 3)*		134	290	mA
		V_O = V_{CC}			140		mA
		V_O = 0V			−140		mA
		V_O = −7V			−180	−290	mA

Electrical Characteristics (Continued)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage (Note 5)	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \le V_{CM} \le +12V$				-0.18	0	V
V_{TL}	Differential Input Low Threshold Voltage (Note 5)	$V_O = V_{OL}$, $I_O = 8.0$ mA $-7V \le V_{CM} \le +12V$			-0.5	-0.23		V
V_{HST}	Hysteresis (Note 6)	$V_{CM} = 0V$				50		mV
I_{IN}	Line Input Current (V_{CC} = 4.75V, 5.25V, 0V)	Other Input = 0V DE = V_{IH} (Note 7)	$V_I = +12V$			0.7	1.0	mA
			$V_I = -7V$			-0.5	-0.8	mA
I_{OSR}	Short Circuit Current	$V_O = 0V$		RO	-5.0	-30	-85	mA
I_{OZ}	TRI-STATE® Leakage Current	V_O = 0.4 to 2.4V			-20		$+20$	μA
V_{OH}	Output High Voltage *(Figure 12)*	$V_{ID} = 0V$, $I_{OH} = -0.4$ mA			2.5	3.5		V
		V_{ID} = OPEN, $I_{OH} = -0.4$ mA			2.5	3.5		V
V_{OL}	Output Low Voltage *(Figure 12)*	$V_{ID} = -0.5V$, $I_{OL} = +8$ mA				0.25	0.6	V
		$V_{ID} = -0.5V$, $I_{OL} = +16$ mA				0.35	0.7	V
R_{IN}	Input Resistance				12	19		kΩ
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE, $\overline{RE}$, or DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = 2.4V$					20	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0.4V$					-100	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				-0.75	-1.5	V
I_{CC}	Output Low Voltage Supply Current (No Load)	DE = 3V, $\overline{RE}$ = 0V, DI = 0V				42	60	mA
I_{CCR}		DE = 0V, $\overline{RE}$ = 0V, DI = 0V				28	45	mA
I_{CCD}		DE = 3V, $\overline{RE}$ = 3V, DI = 0V				43	60	mA
I_{CCX}		DE = 0V, $\overline{RE}$ = 3V, DI = 0V				31	50	mA

Switching Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	$R_L = 54\Omega$, $C_L = 50$ pF, $C_D = 50$ pF *(Figures 4, 5)*	7	21	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low		7	19	60	ns
t_{SKD}	Diff. Skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)			2	10	ns
t_r	Diff. Rise Time			12	50	ns
t_f	Diff. Fall Time			12	50	ns
t_{PLH}	Prop. Delay Low to High	$R_L = 27\Omega$, $C_L = 15$ pF *(Figures 6, 7)*		22	45	ns
t_{PHL}	Prop. Delay High to Low			22	45	ns
t_{PZH}	Enable Time Z to High	$R_L = 110\Omega$, $C_L = 50$ pF *(Figures 8–11)*		32	55	ns
t_{PZL}	Enable Time Z to Low			32	65	ns
t_{PHZ}	Disable Time High to Z			22	55	ns
t_{PLZ}	Disable Time Low to Z			16	55	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	$V_{ID} = -1.5V$ to $+1.5V$, $C_L = 15$ pF *(Figures 13, 14)*	15	40	70	ns
t_{PHL}	Prop. Delay High to Low		15	42	70	ns
t_{SK}	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			2	15	ns
t_{PZH}	Enable Time Z to High	$C_L = 15$ pF *(Figures 15, 16)*		15	50	ns
t_{PZL}	Enable Time Z to Low			17	50	ns
t_{PHZ}	Disable Time High to Z			24	50	ns
t_{PLZ}	Disable Time Low to Z			19	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: $\Delta \lvert V_{T1} \rvert$ and $\Delta \lvert V_{OS} \rvert$ are changes in magnitude of V_{T1} and V_{OS}, respectively, that occur when the input changes state.

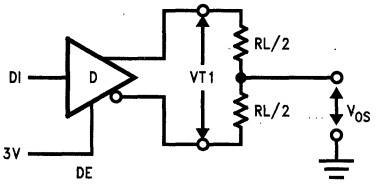
Note 4: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Parameter Measurement Information



TL/F/11383–2

FIGURE 1. Driver V_{T1} and V_{OS} Test Circuit

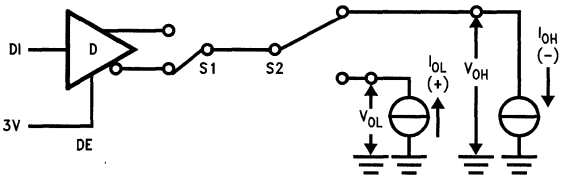


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FIGURE 2. Driver V_{OH} and V_{OL} Test Circuit

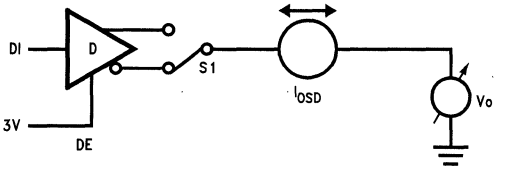

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FIGURE 3. Driver Short Circuit Test Circuit

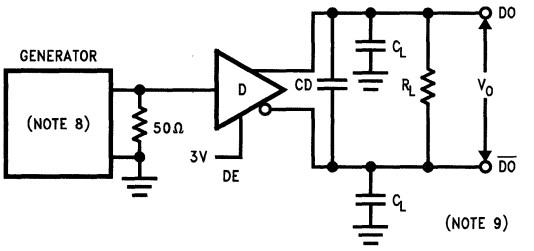

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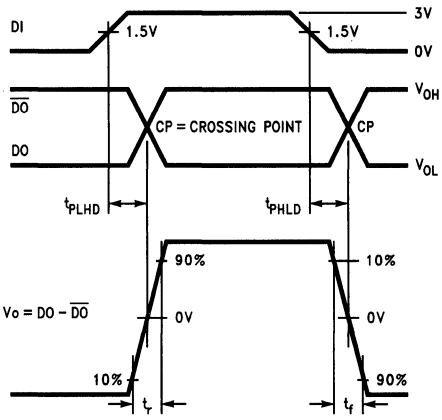
FIGURE 4. Driver Differential Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)



TL/F/11383–6

FIGURE 5. Driver Differential Propagation Delays and Transition Times

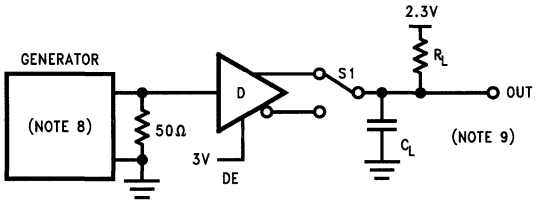


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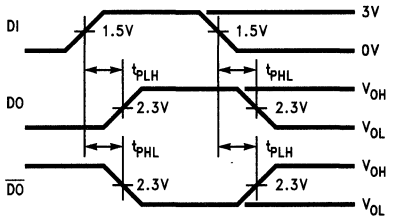
FIGURE 6. Driver Propagation Delay Test Circuit



TL/F/11383–8

FIGURE 7. Driver Propagation Delays

Parameter Measurement Information (Continued)

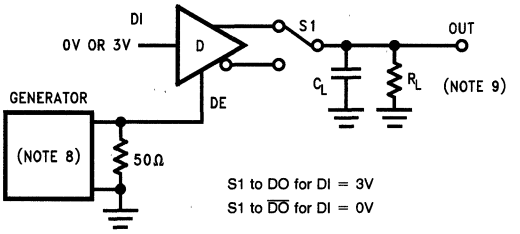


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FIGURE 8. Driver TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})

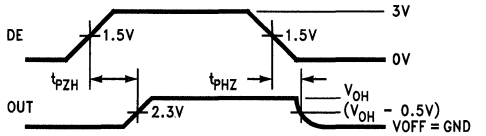

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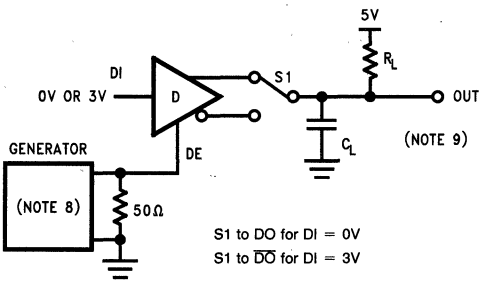
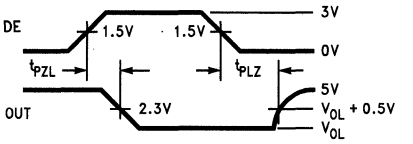
FIGURE 9. Driver TRI-STATE Delays (t_{PZH}, t_{PHZ})



TL/F/11383–11

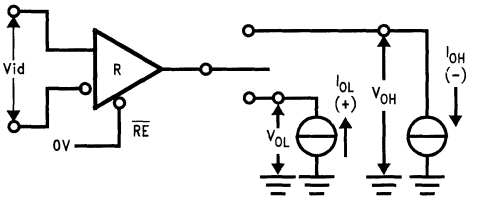
FIGURE 10. Driver TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})



TL/F/11383–12

FIGURE 11. Driver TRI-STATE Delays (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)



TL/F/11383–13

FIGURE 12. Receiver V_{OH} and V_{OL}

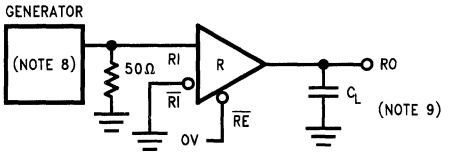


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FIGURE 13. Receiver Propagation Delay Test Circuit

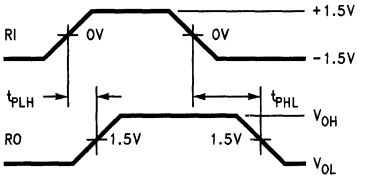

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FIGURE 14. Receiver Propagation Delays

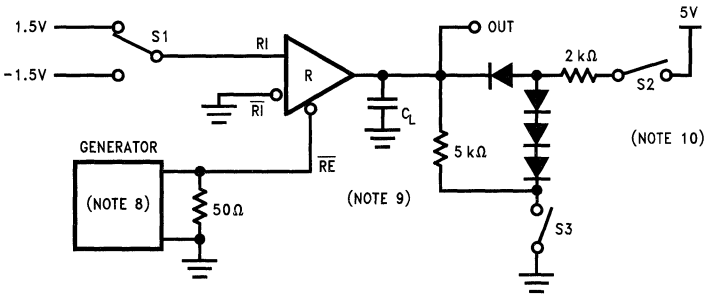

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FIGURE 15. Receiver TRI-STATE Delay Test Circuit

Parameter Measurement Information (Continued)

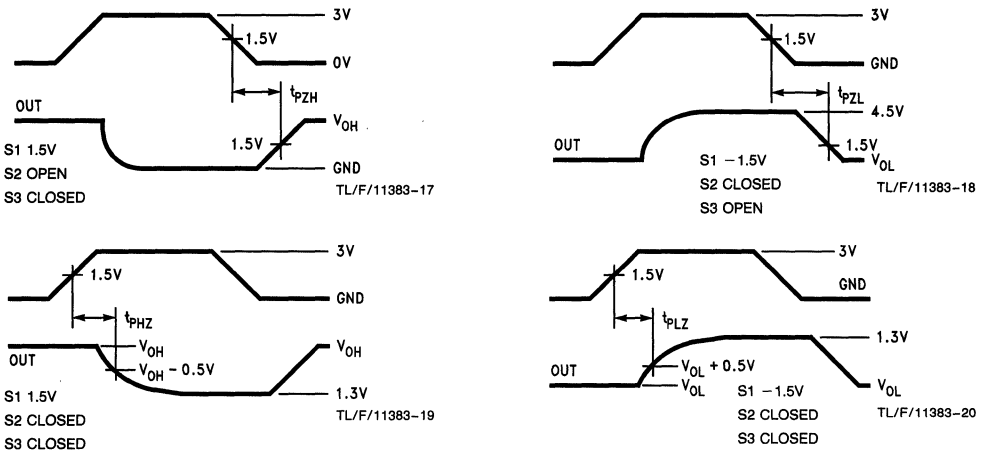


FIGURE 16. Receiver Enable and Disable Timing

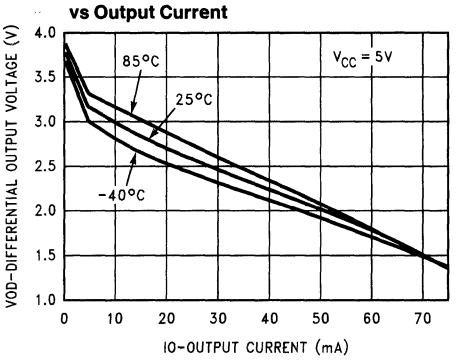
Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and stray capacitance.

Note 10: Diodes are 1N916 or equivalent.

Typical Performance Characteristics

Differential Output Voltage vs Output Current



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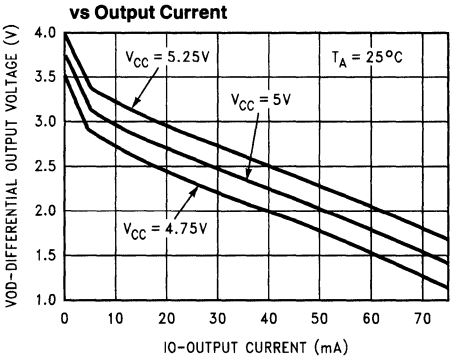
Differential Output Voltage vs Output Current



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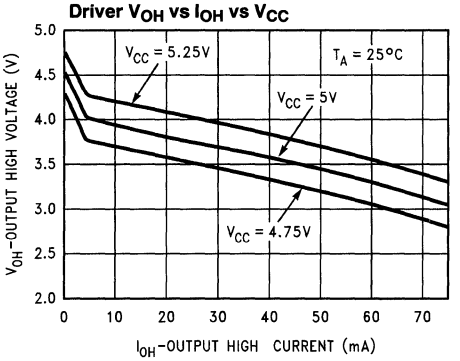
Driver V_{OH} vs I_{OH} vs V_{CC}



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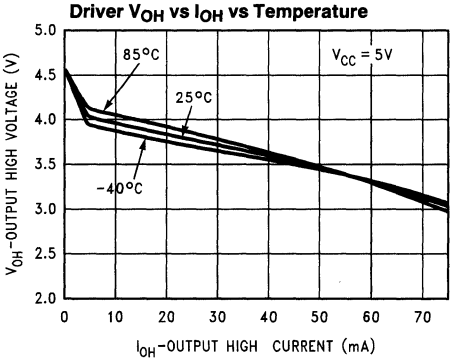
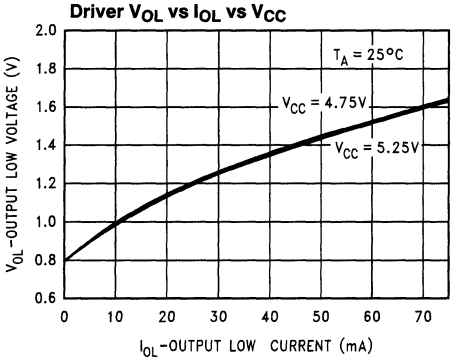
Driver V_{OH} vs I_{OH} vs Temperature



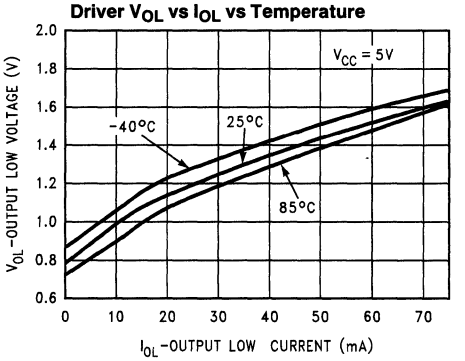
TL/F/11383–24

Driver V_{OL} vs I_{OL} vs V_{CC}



TL/F/11383–25

Driver V_{OL} vs I_{OL} vs Temperature



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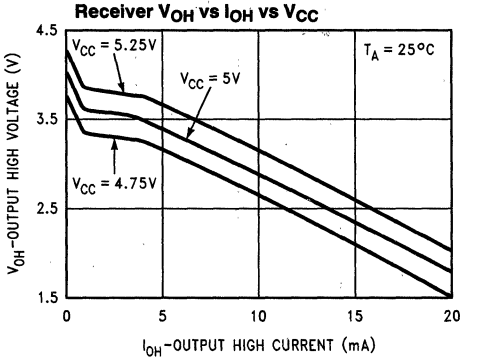
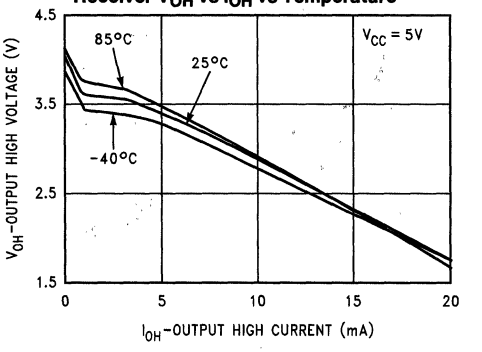
Typical Performance Characteristics (Continued)

Receiver V_{OH} vs I_{OH} vs V_{CC}



TL/F/11383–27

Receiver V_{OH} vs I_{OH} vs Temperature



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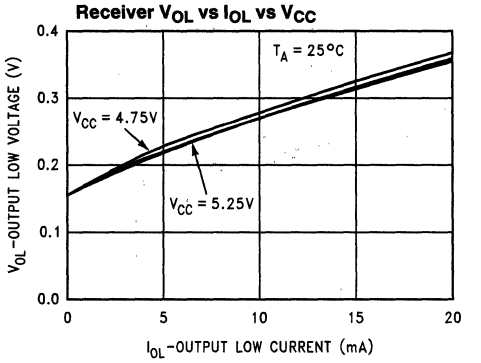
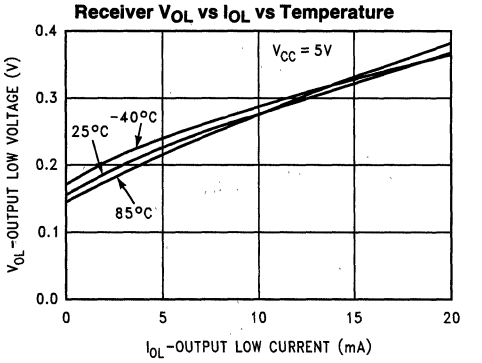
Receiver V_{OL} vs I_{OL} vs V_{CC}



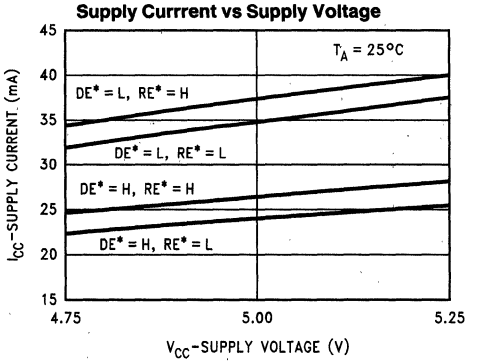
TL/F/11383–29

Receiver V_{OL} vs I_{OL} vs Temperature



TL/F/11383–30

Supply Currrent vs Supply Voltage



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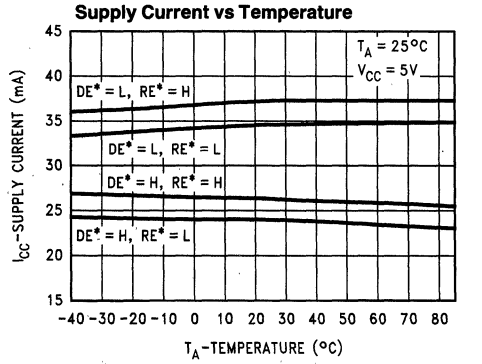
Supply Current vs Temperature



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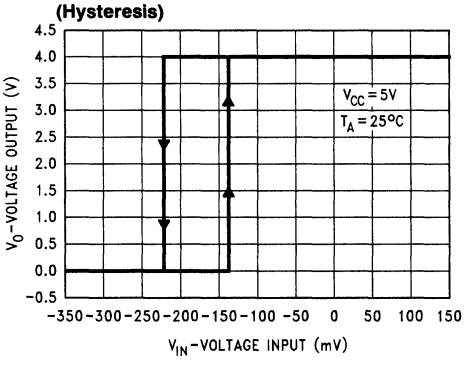
Typical Performance Characteristics (Continued)

Voltage Output vs Voltage Input (Hysteresis)



TL/F/11383–33

National Semiconductor

DS36277
Dominant Mode Multipoint Transceiver

General Description

The DS36277 Dominant Mode Multipoint Transceiver is designed for use on bi-directional differential busses. It is optimal for use on Interfaces that utilize Society of Automotive Engineers (SAE) J1708 Electrical Standard.

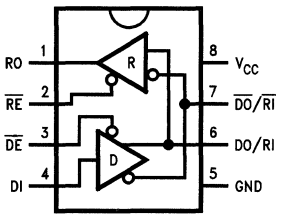
The device is similar to standard TIA/EIA-485 transceivers, but differs in enabling scheme. The Driver's Input is normally externally tied LOW, thus providing only two states: Active (LOW), or Disabled (OFF). When the driver is active, the dominant mode is LOW, conversely, when the driver is disabled, the bus is pulled HIGH by external bias resistors.

The receiver provides a FAILSAFE feature that guarantees a known output state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault Conditions (open or short). The receiver output is HIGH for the following conditions: Open Inputs, Terminated Inputs (50Ω), or Shorted Inputs. FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Optimal for use in SAE J1708 Interfaces
- Compatible with popular interface standards:
  - — TIA/EIA-485 and TIA/EIA-422-A
  - — CCITT recommendation V.11
- Bi-directional transceiver
  - — Designed for multipoint transmission
- Wide bus common mode range
  - — (−7V to +12V)
- Available in plastic DIP and SOIC packages

Connection and Logic Diagram



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Order Number DS36277TM or DS36277TN
See NS Package Number M08A or N08E

Truth Tables

Driver

Inputs		Outputs	
$\overline{DE}$	DI	DO/RI	$\overline{DO/RI}$
L	L	L	H
L	H	H	L
H	X	Z	Z

Receiver

Inputs		Output
$\overline{RE}$	DO/RI–$\overline{DO/RI}$	RO
L	≥ 0 mV	H
L	≤ −500 mV	L
L	SHORTED	H
L	OPEN	H
H	X	Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage ($\overline{DE}$, $\overline{RE}$, and DI)	5.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage (RO)	5.5V
Maximum Package Power Dissipation @ +25°C	
N Package (derate 9.3 mW/°C above +25°C)	1168 mW
M Package (derate 5.8 mW/°C above +25°C)	726 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 6.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Temperature (T_A) DS36277T	−40	+85	°C

Electrical Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_{OD}	Differential Output Voltage	I_O = 0 mA (No Load)		1.5	3.6	6	V
V_{oDO}	Output Voltage	I_O = 0 mA (Output to GND)		0		6	V
$V_{o\overline{DO}}$	Output Voltage			0		6	V
V_{T1}	Differential Output Voltage (Termination Load)	R_L = 54Ω (485)	*(Figure 1)*	1.3	2.2	5.0	V
		R_L = 100Ω (422)		1.7	2.6	5.0	V
ΔV_{T1}	Balance of V_{T1} $\lvert V_{T1} - \overline{V_{T1}} \rvert$	R_L = 54Ω	(Note 3)	−0.2		0.2	V
		R_L = 100Ω		−0.2		0.2	V
V_{OS}	Driver Common Mode Output Voltage	R_L = 54Ω	*(Figure 1)*	0	2.5	3.0	V
		R_L = 100Ω		0	2.5	3.0	V
ΔV_{OS}	Balance of V_{OS} $\lvert V_{OS} - \overline{V_{OS}} \rvert$	R_L = 54Ω	(Note 3)	−0.2		0.2	V
		R_L = 100Ω		−0.2		0.2	V
V_{OH}	Output Voltage High	I_{OH} = −22 mA	*(Figure 2)*	2.7	3.7		V
V_{OL}	Output Voltage Low	I_{OL} = +22 mA			1.3	2	V
I_{OSD}	Driver Short-Circuit Output Current	V_O = +12V	*(Figure 3)*		92	290	mA
		V_O = −7V			−187	−290	mA

Electrical Characteristics (Continued)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage (Note 5)	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \le V_{CM} \le +12V$				−0.150	0	V
V_{TL}	Differential Input Low Threshold Voltage (Note 5)	$V_O = V_{OL}$, $I_O = 8.0$ mA $-7V \le V_{CM} \le +12V$			−0.5	−0.230		V
V_{HST}	Hysteresis (Note 6)	$V_{CM} = 0V$				80		mV
I_{IN}	Line Input Current (V_{CC} = 4.75V, 5.25V, 0V)	Other Input = 0V, $\overline{DE} = V_{IH}$ (Note 7)	$V_I = +12V$			0.5	1.5	mA
			$V_I = -7V$			−0.5	−1.5	mA
I_{OSR}	Short Circuit Current	$V_O = 0V$		RO	−15	−32	−85	mA
I_{OZ}	TRI-STATE® Leakage Current	V_O = 0.4 to 2.4V			−20	1.4	+20	μA
V_{OH}	Output High Voltage *(Figure 12)*	$V_{ID} = 0V$, $I_{OH} = -0.4$ mA			2.3	3.7		V
		V_{ID} = OPEN, $I_{OH} = -0.4$ mA			2.3	3.7		V
V_{OL}	Output Low Voltage *(Figure 12)*	$V_{ID} = -0.5V$, $I_{OL} = +8$ mA				0.3	0.7	V
		$V_{ID} = -0.5V$, $I_{OL} = +16$ mA				0.3	0.8	V
R_{IN}	Input Resistance				10	20		kΩ
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			$\overline{DE}$, $\overline{RE}$, or DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = 2.4V$					20	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0.4V$					−100	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				−0.7	−1.5	V
I_{CC}	Output Low Voltage Supply Current (No Load)	$\overline{DE} = 0V$, $\overline{RE} = 0V$, DI = 0V				39	60	mA
I_{CCR}		$\overline{DE} = 3V$, $\overline{RE} = 0V$, DI = 0V				24	50	mA
I_{CCD}		$\overline{DE} = 0V$, $\overline{RE} = 3V$, DI = 0V				40	75	mA
I_{CCX}		$\overline{DE} = 3V$, $\overline{RE} = 3V$, DI = 0V				27	45	mA

Switching Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	$R_L = 54\Omega$, $C_L = 50$ pF, $C_D = 50$ pF *(Figures 4, 5)*	8	17	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low		8	19	60	ns
t_{SKD}	Diff. Skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)			2	10	ns
t_r	Diff. Rise Time			11	60	ns
t_f	Diff. Fall Time			11	60	ns
t_{PLH}	Prop. Delay Low to High	$R_L = 27\Omega$, $C_L = 15$ pF *(Figures 6, 7)*		22	85	ns
t_{PHL}	Prop. Delay High to Low			25	85	ns
t_{PZH}	Enable Time Z to High	$R_L = 110\Omega$, $C_L = 50$ pF *(Figures 8–11)*		25	60	ns
t_{PZL}	Enable Time Z to Low			30	60	ns
t_{PHZ}	Disable Time High to Z			16	60	ns
t_{PLZ}	Disable Time Low to Z			11	60	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	$V_{ID} = -1.5V$ to $+1.5V$, $C_L = 15$ pF *(Figures 13, 14)*	15	37	90	ns
t_{PHL}	Prop. Delay High to Low		15	43	90	ns
t_{SK}	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			6	15	ns
t_{PZH}	Enable Time Z to High	$C_L = 15$ pF *(Figures 15, 16)*		12	60	ns
t_{PZL}	Enable Time Z to Low			28	60	ns
t_{PHZ}	Disable Time High to Z			20	60	ns
t_{PLZ}	Disable Time Low to Z			10	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: $\Delta \lvert V_{T1} \rvert$ and $\Delta \lvert V_{OS} \rvert$ are changes in magnitude of V_{T1} and V_{OS}, respectively, that occur when the input changes state.

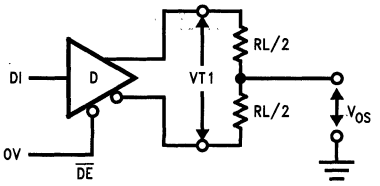
Note 4: All typicals are given for $V_{CC} = 5.0V$ and $T_A = +25°C$.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

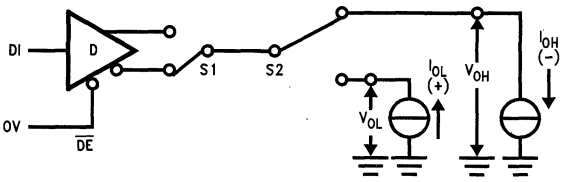
Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Parameter Measurement Information



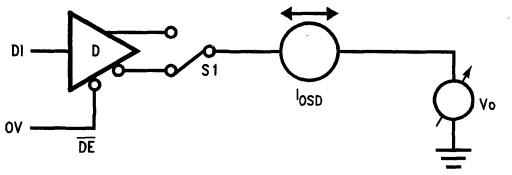
TL/F/11384–2

FIGURE 1. Driver V_{T1} and V_{OS} Test Circuit



TL/F/11384–3

FIGURE 2. Driver V_{OH} and V_{OL} Test Circuit



TL/F/11384–4

FIGURE 3. Driver Short Circuit Test Circuit

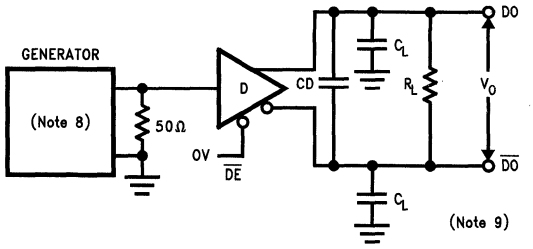


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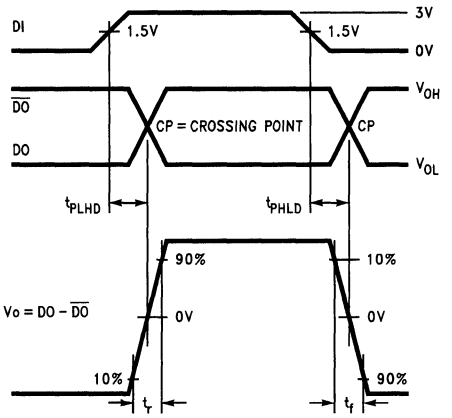
FIGURE 4. Driver Differential Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)



TL/F/11384–6

FIGURE 5. Driver Differential Propagation Delays and Transition Times

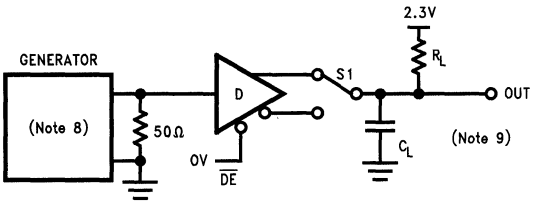


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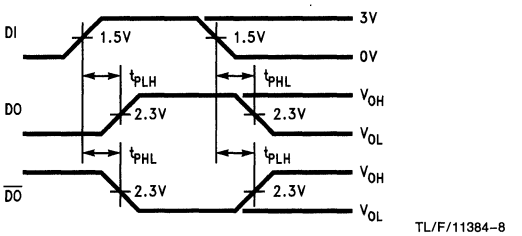
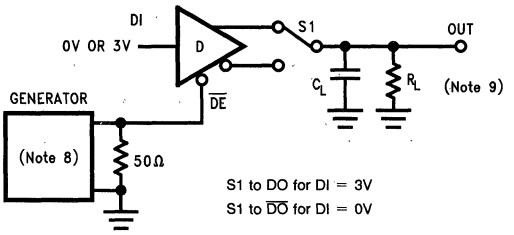
FIGURE 6. Driver Propagation Delay Test Circuit



TL/F/11384–8

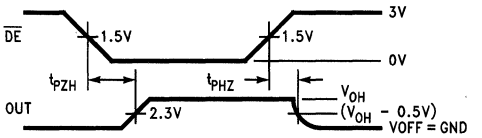
FIGURE 7. Driver Propagation Delays

Parameter Measurement Information (Continued)



TL/F/11384–9

FIGURE 8. Driver TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})



TL/F/11384–10

FIGURE 9. Driver TRI-STATE Delays (t_{PZH}, t_{PHZ})

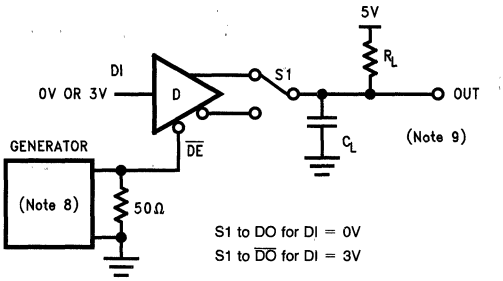


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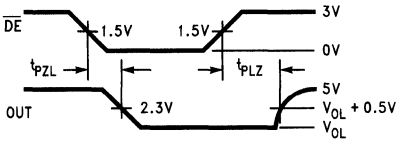
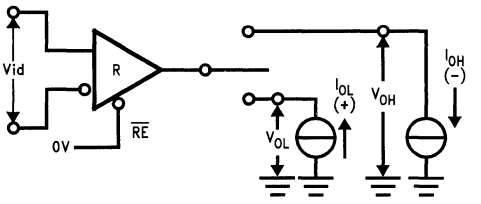
FIGURE 10. Driver TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)



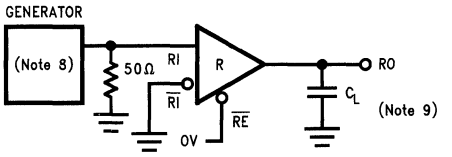
TL/F/11384–12

FIGURE 11. Driver TRI-STATE Delays (t_{PZL}, t_{PLZ})



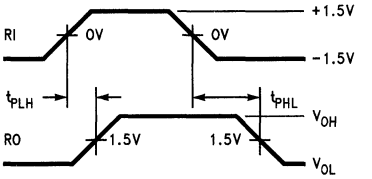
TL/F/11384–13

FIGURE 12. Receiver V_{OH} and V_{OL}



TL/F/11384–14

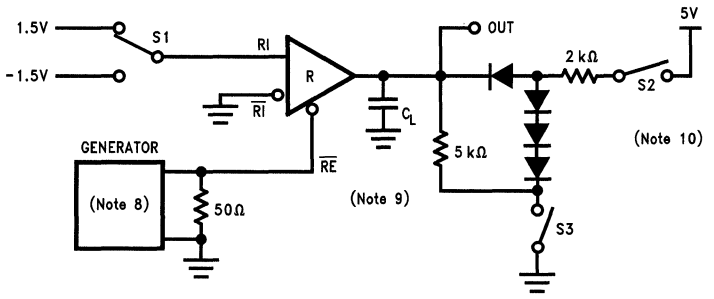
FIGURE 13. Receiver Propagation Delay Test Circuit



TL/F/11384–15

FIGURE 14. Receiver Propagation Delays

Parameter Measurement Information (Continued)



TL/F/11384–16

FIGURE 15. Receiver TRI-STATE Delay Test Circuit

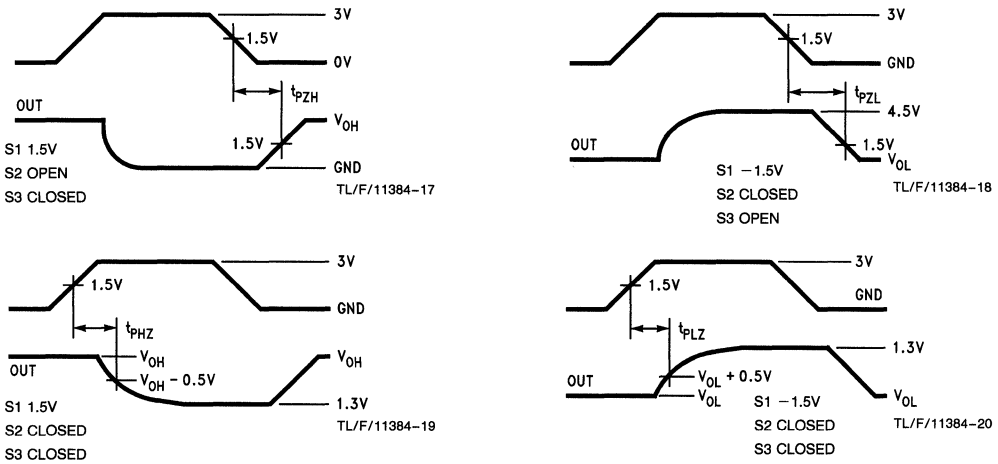


FIGURE 16. Receiver Enable and Disable Timing

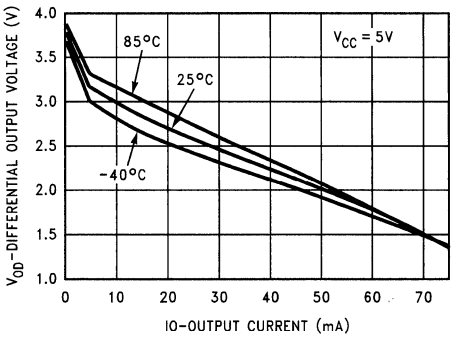
Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and stray capacitance.

Note 10: Diodes are 1N916 or equivalent.

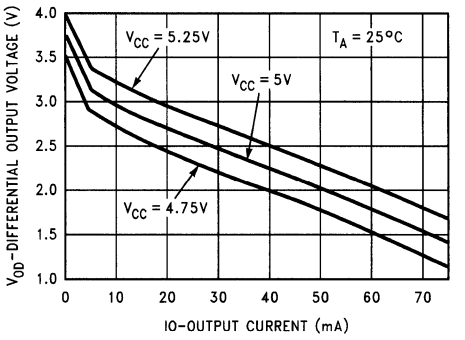
Typical Performance Characteristics

Differential Output Voltage vs Output Current



TL/F/11384–22

Differential Output Voltage vs Output Current



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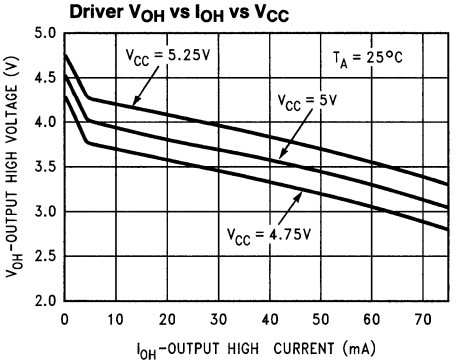
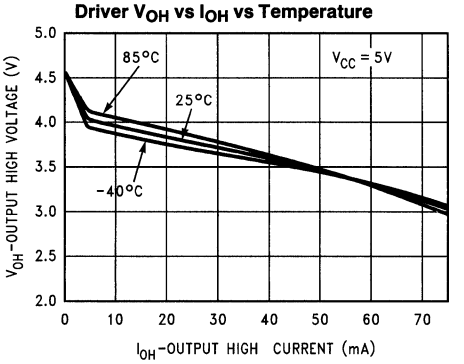
Driver V_{OH} vs I_{OH} vs V_{CC}



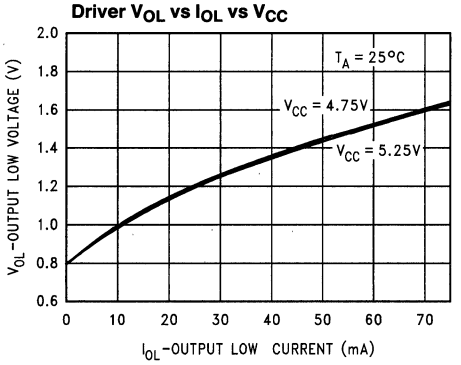
TL/F/11384–24

Driver V_{OH} vs I_{OH} vs Temperature



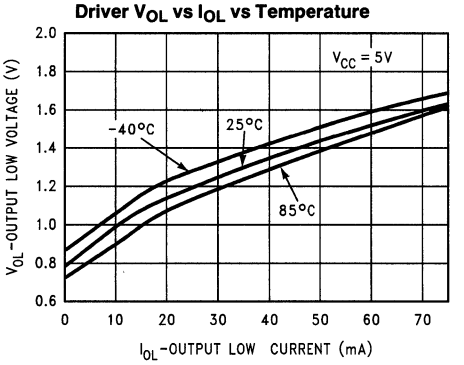
TL/F/11384–25

Driver V_{OL} vs I_{OL} vs V_{CC}



TL/F/11384–26

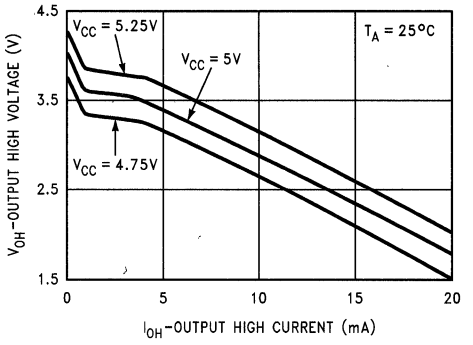
Driver V_{OL} vs I_{OL} vs Temperature



TL/F/11384–27

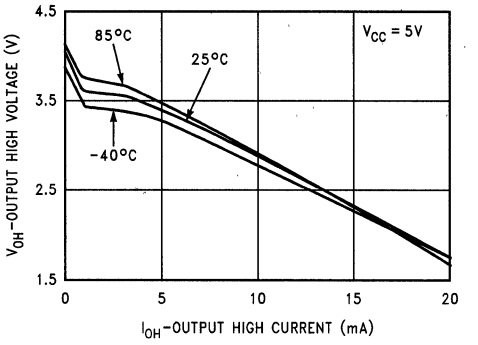
Typical Performance Characteristics (Continued)

Receiver V_{OH} vs I_{OH} vs V_{CC}



TL/F/11384–28

Receiver V_{OH} vs I_{OH} vs Temperature



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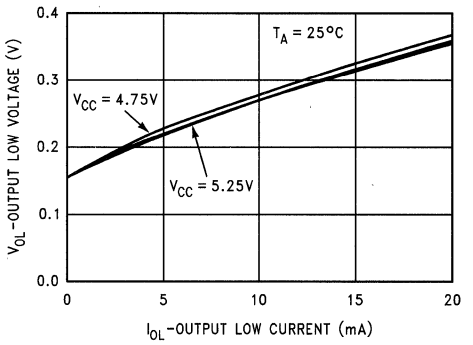
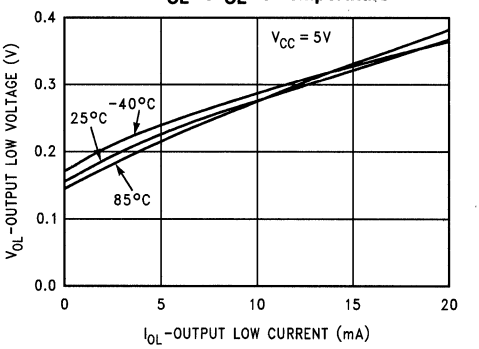
Receiver V_{OL} vs I_{OL} vs V_{CC}



TL/F/11384–30

Receiver V_{OL} vs I_{OL} vs Temperature



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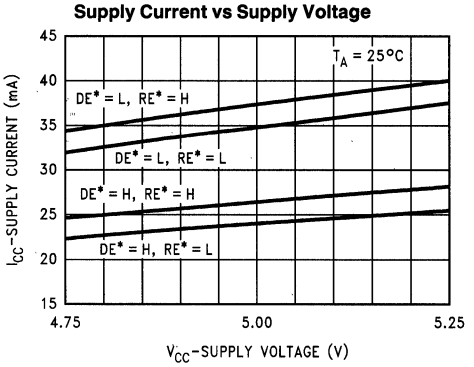
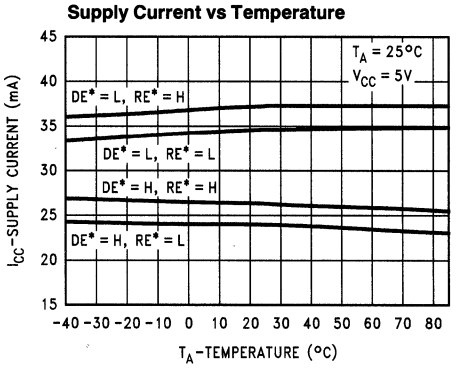
Supply Current vs Supply Voltage



TL/F/11384–32

Supply Current vs Temperature



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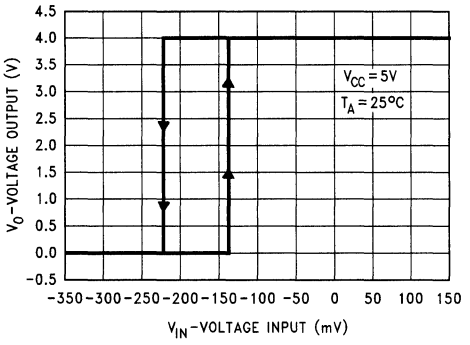
Typical Performance Characteristics (Continued)

Voltage Output vs Voltage Input (Hysteresis)



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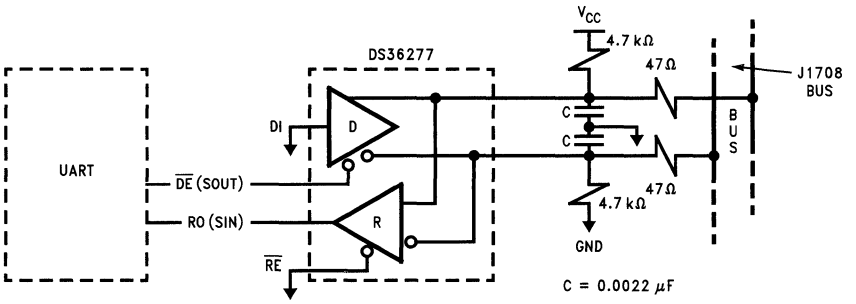
Typical Applications Information

SAE J1708 Node with External Bias Resistors and Filters



TL/F/11384–21

National Semiconductor

DS36C278
Low Power Multipoint EIA-RS-485 Transceiver

General Description

The DS36C278 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 standard for multipoint data transmission. In addition it is compatible with TIA/EIA-422-B.

The CMOS design offers significant power savings over its bipolar and ALS counterparts without sacrificing ruggedness against ESD damage. The device is ideal for use in battery powered or power conscious applications. I_{CC} is specified at 500 μA maximum.

The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

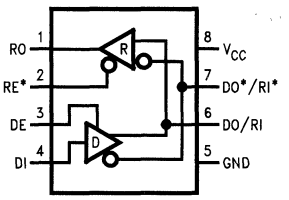
The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open.†

The DS36C278T is fully specified over the industrial temperature range (−40°C to +85°C).

Features

- 100% RS-485 compliant
  - — Guaranteed RS-485 device interoperation
- Low power CMOS design I_{CC} 500 μA max
- Built-in power up/down glitch-free circuitry
  - — Permits live transceiver insertion/displacement
- DIP and SOIC packages available
- Industrial temperature range −40°C to +85°C
- On-board thermal shutdown circuitry
  - — Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range −7V to +12V
- Receiver open input fail-safe†
- ¼ unit load (DS36C278) ≥128 nodes
- ½ unit load (DS36C278T) ≥64 nodes
- ESD (human body model) ≥2 kV
- Drop in replacement for:
  - — LTC485, MAX485, DS75176, DS3695

Connection and Logic Diagram



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Order Number DS36C278TM, DS36C278TN, DS36C278M, DS36C278N
See NS Package Number M08A or N08E

Truth Table

DRIVER SECTION				
RE*	**DE**	**DI**	**DO/RI**	**DO*/RI***
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

RECEIVER SECTION			
RE*	**DE**	**RI-RI***	**RO**
L	L	≥ +0.2V	H
L	L	≤ −0.2V	L
H	L	X	Z
L	L	OPEN†	H

†**Note:** Non-terminated, open input only

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+12V
Input Voltage (DE, RE*, & DI)	−0.5V to (V_{CC} +0.5V)
Common Mode (V_{CM})	
Driver Output/Receiver Input	±15V
Input Voltage (DO/RI, DO*/RI*)	±14V
Receiver Output Voltage	−0.5V to (V_{CC} +0.5V)
Maximum Package Power Dissipation @ +25°C	
M Package 1190 mW, derate	9.5 mW/°C above +25°C
N Package 744 mW, derate	6.0 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	+260°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Bus Voltage	−7		+12	V
Operating Free Air Temperature (Ta)				
DS36C278T	−40	25	+85	°C
DS36C278	0	25	+70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Reference		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD1}	Differential Output Voltage	I_O = 0 mA (No Load)	(422) (485)		1.5		5.0	V
V_{OD0}	Output Voltage	I_O = 0 mA			0		5.0	V
V_{OD0*}	Output Voltage	(Output to GND)			0		5.0	V
V_{OD2}	Differential Output Voltage (Termination Load)	R_L = 50Ω	(422)	*Figure 1*	2.0	2.8		V
		R_L = 27Ω	(485)		1.5	2.3	5.0	V
ΔV_{OD2}	Balance of V_{OD2} $\lvert V_{OD2} - V_{OD2*}\rvert$	R_L = 27Ω or 50Ω	(Note 4) (422, 485)		−0.2	0.1	+0.2	V
V_{OD3}	Differential Output Voltage (Full Load)	R1 = 54Ω, R2 = 375Ω V_{TEST} = −7V to +12V	*Figure 2*		1.5	2.0	5.0	V
V_{OC}	Driver Common Mode Output Voltage	R_L = 27Ω	(485)	*Figure 1*	0		3.0	V
		R_L = 50Ω	(422)		0		3.0	V
ΔV_{OC}	Balance of V_{OC} $\lvert V_{OC} - V_{OC*}\rvert$	R_L = 27Ω or R_L = 50Ω	(Note 4) (422, 485)		−0.2		+0.2	V
I_{OSD}	Driver Output Short-Circuit Current	V_O = +12V	(485) *Figure 4*			200	+250	mA
		V_O = −7V	(485)			−190	−250	mA
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage	V_O = V_{OH}, I_O = −0.4V −7V ≤ V_{CM} ≤ +12V	(Note 5) (422, 485)			+0.035	+0.2	V
V_{TL}	Differential Input Low Threshold Voltage	V_O = V_{OL}, I_O = 0.4 mA −7V ≤ V_{CM} ≤ +12V			−0.2	−0.035		V
V_{HST}	Hysteresis	V_{CM} = 0V	(Note 6)			70		mV
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V	DS36C278T		24	68		kΩ
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V	DS36C278		48	68		kΩ

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Reference	Min	Typ	Max	Units
I_{IN}	Line Input Current (Note 7)	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}, V_{CC} = 4.75 to 5.25 or 0V	DS36C278	V_{IN} = +12V	0	0.19	0.25	mA
				V_{IN} = −7V	0	−0.1	−0.2	mA
			DS36C278T	V_{IN} = +12V	0	0.19	0.5	mA
				V_{IN} = −7V	0	−0.1	−0.4	mA
I_{ING}	Line Input Current Glitch (Note 7)	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}, V_{CC} = +3.0V or 0V, T_A = 25°C	DS36C278	V_{IN} = +12V	0	0.19	0.25	mA
				V_{IN} = −7V	0	−0.1	−0.2	mA
			DS36C278T	V_{IN} = +12V	0	0.19	0.5	mA
				V_{IN} = −7V	0	−0.1	−0.4	mA
I_B	Input Balance Test	RS = 500Ω		(422) (Note 9)			±400	mV
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA, V_{ID} = +0.2V		RO *Figure 11*	3.5	4.6		V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA, V_{ID} = −0.2V				0.3	0.5	V
I_{OSR}	Short Circuit Current	V_O = GND		RO	7	35	85	mA
I_{OZR}	TRI-STATE Leakage Current	V_O = 0.4V to 2.4V					±1	μA
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE, RE*, DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}					2	μA
I_{IL}	Low Level Input Current	V_{CC} = 5V	V_{IL} = 0V				−2	μA
		V_{CC} = +3.0V					−2	μA
I_{CC}	Power Supply Current (No Load)	Driver and Receiver ON		V_{CC}		200	500	μA
I_{CCR}		Driver OFF, Receiver ON				200	500	μA
I_{CCD}		Driver ON, Receiver OFF				200	500	μA
I_{CCZ}		Driver and Receiver OFF				200	500	μA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 3 and 8)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 54Ω, C_L = 100 pF	*Figures 5, 6*	10	39	80	ns
t_{PLHD}	Differential Propagation Delay Low to High			10	40	80	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0	1	10	ns
t_r	Rise Time			3	25	50	ns
t_f	Fall Time			3	25	50	ns
t_{PHZ}	Disable Time High to Z	C_L = 15 pF	*Figures 7, 8*	—	80	200	ns
t_{PLZ}	Disable Time Low to Z	RE * = L	*Figures 9, 10*	—	80	200	ns
t_{PZH}	Enable Time Z to High	C_L = 100 pF	*Figures 7, 8*	—	50	200	ns
t_{PZL}	Enable Time Z to Low	RE * = L	*Figures 9, 10*	—	65	200	ns

Switching Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 3 and 8)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS							
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF	*Figures 12, 13*	30	210	400	ns
t_{PLH}	Propagation Delay Low to High			30	190	400	ns
t_{SK}	Skew, $\|t_{PHL} - t_{PLH}\|$			0	20	50	ns
t_{PLZ}	Output Disable Time	C_L = 15 pF	*Figures 14, 15, 16*	—	50	150	ns
t_{PHZ}				—	55	150	ns
t_{PZL}	Output Enable Time			—	40	150	ns
t_{PZH}				—	45	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD1} and V_{OD2}.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.

Note 4: Delta $|V_{OD2}|$ and Delta $|V_{OC}|$ are changes in magnitude of V_{OD2} and V_{OC}, respectively, that occur when input changes state.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

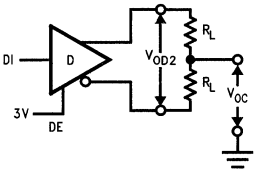
Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 8: C_L includes probe and jig capacitance.

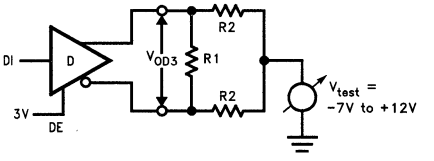
Note 9: For complete details of test, see RS-485.

Parameter Measurement Information



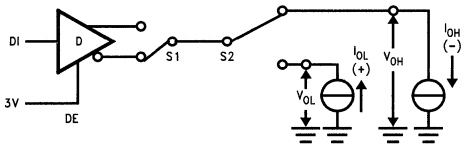
TL/F/12040–2

FIGURE 1. Driver V_{OD2} and V_{OC}



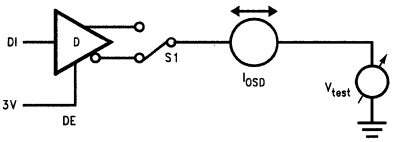
TL/F/12040–18

FIGURE 2. Driver V_{OD3}



TL/F/12040–3

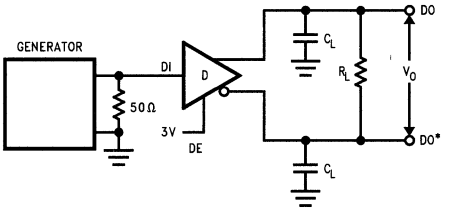
FIGURE 3. Driver V_{OH} and V_{OL}



TL/F/12040–4

Vtest = −7V to +12V

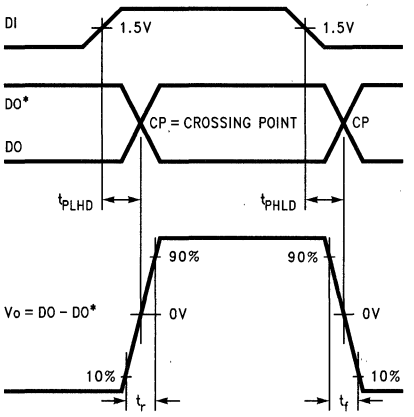
FIGURE 4. Driver I_{OSD}



TL/F/12040–5

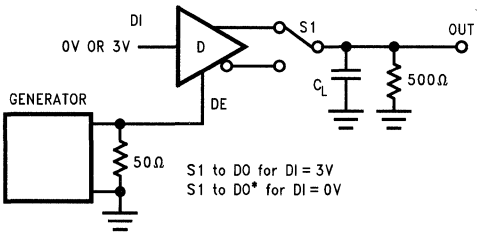
FIGURE 5. Driver Differential Propagation Delay Test Circuit

Parameter Measurement Information (Continued)



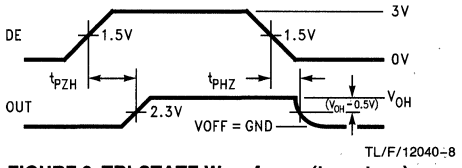
TL/F/12040–6

FIGURE 6. Driver Differential Propagation Delays and Differential Rise and Fall Times



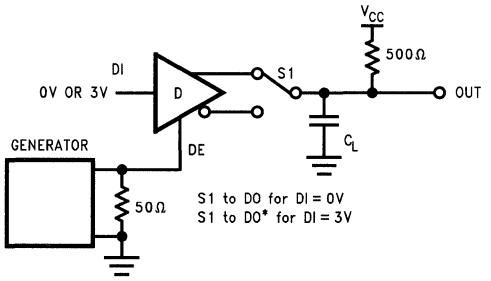
TL/F/12040–7

FIGURE 7. TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})



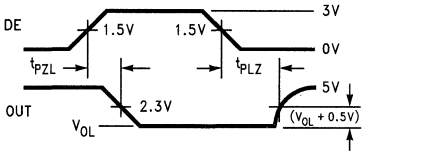
TL/F/12040–8

FIGURE 8. TRI-STATE Waveforms (t_{PZH}, t_{PHZ})



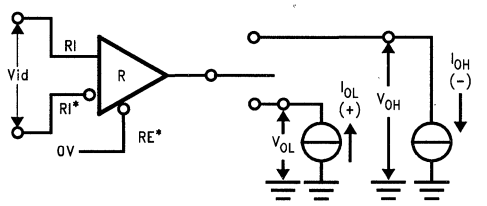
TL/F/12040–9

FIGURE 9. TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})



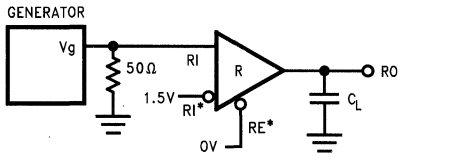
TL/F/12040–10

FIGURE 10. TRI-STATE Waveforms (t_{PZL}, t_{PLZ})



TL/F/12040–11

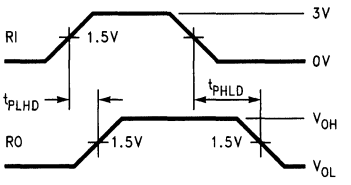
FIGURE 11. Receiver V_{OH} and V_{OL}



TL/F/12040–12

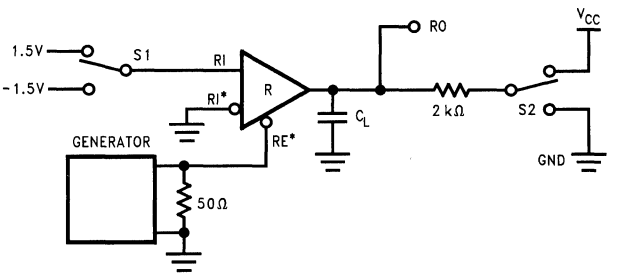
FIGURE 12. Receiver Differential Propagation Delay Test Circuit

Parameter Measurement Information (Continued)



TL/F/12040–13

FIGURE 13. Receiver Differential Propagation Delay Waveforms



TL/F/12040–14

FIGURE 14. Receiver TRI-STATE Test Circuit

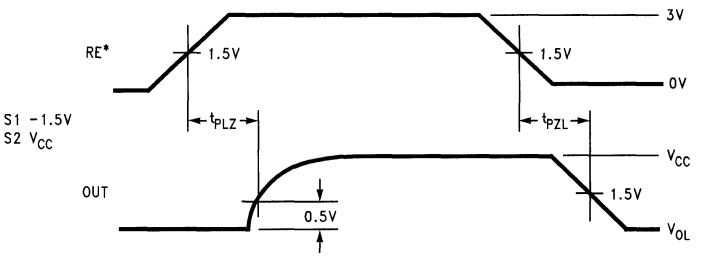


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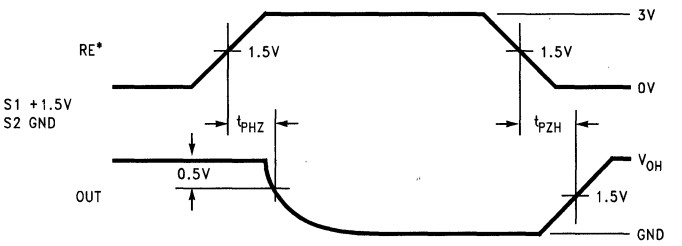
FIGURE 15. Receiver Enable and Disable Waveforms (t_{PLZ}, t_{PZL})



TL/F/12040–16

FIGURE 16. Receiver Enable and Disable Waveforms (t_{PHZ}, t_{PZH})

Typical Application Information

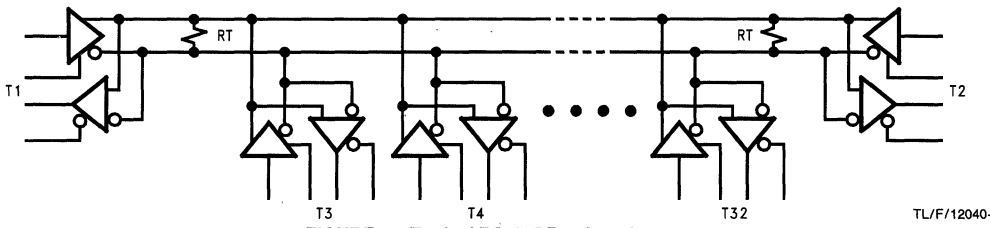


FIGURE 17. Typical RS-485 Bus Interface

TABLE I. Device Pin Descriptions

Pin No.	Name	Description
1	RO	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI ≥ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI ≤ DO*/RI* by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
2	RE*	Receiver Output Enable: When RE* is LOW the receiver output is enabled. When RE* is HIGH, the receiver output is in TRI-STATE (OFF).
3	DE	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF).
4	DI	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection.
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO*/RI*	Driver Output/Receiver Input, 485 Bus Pin.
8	V_{CC}	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.75V to +5.25V.

Unit Load

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see *Figure 18*). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes. For example, an aircraft that has 32 rows with 4 seats per row would benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS36C278, the DS36C279, and the DS36C280 all have ½ unit load and ¼ unit load (UL) options available. These devices will allow up to 64 nodes or 128 nodes guaranteed over temperature depending upon which option is selected. The ½ UL option is available in industrial temperature and the ¼ UL is available in commercial temperature.

First, for a ½ UL device the top and bottom borders shown in *Figure 18* are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see *Figure 18*). Second, for a ¼ UL device the top and bottom borders shown in *Figure 18* are scaled also. Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see *Figure 18*).

The advantage of the ½ UL and ¼ UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS36C278/279/280 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

The DS36C279 and DS36C280 have an additional feature which offers more advantages. The DS36C279 has an automatic sleep mode function for power conscious applications. The DS36C280 has a slew rate control for EMI conscious applications. Refer to the sleep mode and slew rate control portion of the application information section in the corresponding datasheet for more information on these features.

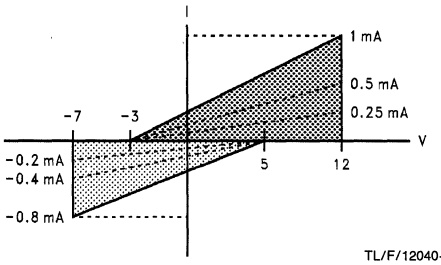


FIGURE 18. Input Current vs Input Voltage Operating Range

National Semiconductor

DS36C279
Low Power EIA-RS-485 Transceiver with Sleep Mode

General Description

The DS36C279 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition it is compatible with TIA/EIA-422-B.

The sleep mode feature automatically puts the device in a power saving mode when both the driver and receiver are disabled.†† The device is ideal for use in power conscious applications where the device may be disabled for extended periods of time.

The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into a high impedance state.

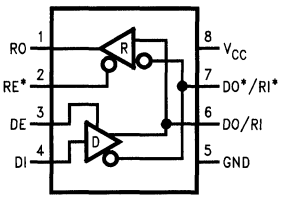
The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open.†

The DS36C279T is fully specified over the industrial temperature range (−40°C to +85°C).

Features

- 100% RS-485 compliant
  — Guaranteed RS-485 device interoperation
- Low power CMOS design — I_{CC} 500 μA max
- Automatic sensing sleep mode
  — Reduces I_{CC} to 10 μA maximum
- Built-in power up/down glitch-free circuitry
  — Permits live transceiver intersection/displacement
- DIP and SOIC packages available
- Industrial temperature range — −40°C to +85°C
- On-board thermal shutdown circuitry
  — Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range — −7V to +12V
- Receive open input fail-safe†
- ¼ unit load (DS36C279) — ≥ 128 nodes
- ½ unit load (DS36C279T) — ≥ 64 nodes
- ESD (Human Body Model) — ≥ 2 kV
- Drop-in replacement for:
  — LTC485 MAX485 DS75176 DS3695

Connection and Logic Diagram



TL/F/12053–1

Order Number DS36C279M, DS36C279N, DS36C279TM or DS36C279TN
See NS Package Number M08A or N08E

Truth Table

DRIVER SECTION				
RE*	**DE**	**DI**	**DO/RI**	**DO*/RI***
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

RECEIVER SECTION			
RE*	**DE**	**RI-RI***	**RO**
L	L	≥ +0.2V	H
L	L	≤ −0.2V	L
H	L	X	Z††
L	L	OPEN†	H

Note†: Non-terminated, open input only

††: Device enters sleep mode if enable conditions are held > 600 ns

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	+12V
Input Voltage (DE, RE*, & DI)	−0.5V to (V_{CC} +0.5V)
Common Mode (V_{CM})	
Driver Output/Receiver Input	±15V
Input Voltage (DO/RI, DO*/RI*)	±14V
Receiver Output Voltage	−0.5V to (V_{CC} +0.5V)
Maximum Package Power Dissipation @ +25°C	
M Package 1190 mW, derate	9.5 mW/°C above +25°C
N Package 744 mW, derate	6.0 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec)	+260°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Bus Voltage	−7		+12	V
Operating Free Air Temperature (T_A)				
DS36C279T	−40	+25	+85	°C
DS36C279	0	+25	+70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Reference		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD1}	Differential Output Voltage	I_O = 0 mA (No Load)	(422) (485)		1.5		5.0	V
V_{OD0}	Output Voltage	I_O = 0 mA (Output to GND)			0		5.0	V
V_{OD0*}	Output Voltage				0		5.0	V
V_{OD2}	Differential Output Voltage (Termination Load)	R_L = 50Ω	(422)	*Figure 1*	2.0	2.8		V
		R_L = 27Ω	(485)		1.5	2.3	5.0	V
ΔV_{OD2}	Balance of V_{OD2} $\lvert V_{OD2} - V_{OD2*}\rvert$	R_L = 27Ω or 50Ω	(Note 4) (422, 485)		−0.2	0.1	+0.2	V
V_{OD3}	Differential Output Voltage (Full Load)	R1 = 54Ω, R2 = 375Ω V_{TEST} = −7V to +12V	*Figure 2*		1.5	2.0	5.0	V
V_{OC}	Driver Common Mode Output Voltage	R_L = 27Ω	(485)	*Figure 1*	0		3.0	V
		R_L = 50Ω	(422)		0		3.0	V
ΔV_{OC}	Balance of V_{OC} $\lvert V_{OC} - V_{OC*}\rvert$	R_L = 27Ω or R_L = 50Ω	(Note 4) (422, 485)		−0.2		+0.2	V
I_{OSD}	Driver Output Short-Circuit Current	V_O = +12V	(485) *Figure 4*			200	+250	mA
		V_O = −7V	(485)			−190	−250	mA

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Reference	Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \le V_{CM} \le +12V$		(Note 5) (422, 485)		+0.035	+0.2	V
V_{TL}	Differential Input Low Threshold Voltage	$V_O = V_{OL}$, $I_O = 0.4$ mA $-7V \le V_{CM} \le +12V$			−0.2	−0.035		V
V_{HST}	Hysteresis	$V_{CM} = 0V$		(Note 6)		70		mV
R_{IN}	Input Resistance	$-7V \le V_{CM} \le +12V$	DS36C279T		24	68		kΩ
			DS36C279		48	68		kΩ
I_{IN}	Line Input Current (Note 7)	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}, V_{CC} = 4.75 to 5.25 or 0V	DS36C279	$V_{IN} = +12V$	0	0.19	0.25	mA
				$V_{IN} = -7V$	0	−0.1	−0.2	mA
			DS36C279T	$V_{IN} = +12V$	0	0.19	0.5	mA
				$V_{IN} = -7V$	0	−0.1	−0.4	mA
I_{ING}	Line Input Current Glitch (Note 7)	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}, V_{CC} = +3.0V or 0V, T_A = 25°C	DS36C279	$V_{IN} = +12V$	0	0.19	0.25	mA
				$V_{IN} = -7V$	0	−0.1	−0.2	mA
			DS36C279T	$V_{IN} = +12V$	0	0.19	0.5	mA
				$V_{IN} = -7V$	0	−0.1	−0.4	mA
I_B	Input Balance Test	RS = 500Ω		(422) (Note 10)			±400	mV
V_{OH}	High Level Output Voltage	$I_{OH} = -4$ mA, $V_{ID} = +0.2V$		RO *Figure 11*	3.5	4.6		V
V_{OL}	Low Level Output Voltage	$I_{OL} = +4$ mA, $V_{ID} = -0.2V$				0.3	0.5	V
I_{OSR}	Short Circuit Current	V_O = GND		RO	7	35	85	mA
I_{OZR}	TRI-STATE Leakage Current	V_O = 0.4V to 2.4V					±1	μA
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE, RE*, DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{CC}$					2	μA
I_{IL}	Low Level Input Current	V_{CC} = 5V	V_{IL} = 0V				−2	μA
		$V_{CC} = +3.0V$					−2	μA
I_{CC}	Power Supply Current (No Load)	Driver and Receiver ON		V_{CC}		200	500	μA
I_{CCR}		Driver OFF, Receiver ON				200	500	μA
I_{CCD}		Driver ON, Receiver OFF				200	500	μA
I_{CCX}		Sleep Mode				0.2	10	μA

4

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 3 and 8)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 54Ω, C_L = 100 pF	*Figures 5, 6*	10	39	80	ns
t_{PLHD}	Differential Propagation Delay Low to High			10	40	80	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$			0	1	10	ns
t_r	Rise Time			3	25	50	ns
t_f	Fall Time			3	25	50	ns
t_{PHZ}	Disable Time High to Z	C_L = 15 pF, RE* = L	*Figures 7, 8*		80	200	ns
t_{PLZ}	Disable Time Low to Z		*Figures 9, 10*		80	200	ns
t_{PZH}	Enable Time Z to High	C_L = 100 pF, RE* = L	*Figures 7, 8*		50	200	ns
t_{PZL}	Enable Time Z to Low		*Figures 9, 10*		65	200	ns
t_{PSH}	Driver Enable from Sleep Mode to Output High	C_L = 100 pF (Note 9)	*Figures 7, 8*	70	98	250	ns
t_{PSL}	Driver Enble from Sleep Mode to Output Low	C_L = 100 pF (Note 9)	*Figures 9, 10*	70	98	250	ns
RECEIVER CHARACTERISTICS							
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF	*Figures 12, 13*	30	210	400	ns
t_{PLH}	Propagation Delay Low to High			30	190	400	ns
t_{SK}	Skew, $\|t_{PHL} - t_{PLH}\|$			0	20	50	ns
t_{PLZ}	Output Disable Time	C_L = 15 pF, DE = H	*Figures 14, 15, 16*		50	150	ns
t_{PHZ}					55	150	ns
t_{PZL}	Output Enable Time				40	150	ns
t_{PZH}					45	150	ns
t_{PSH}	Receiver Enable from Sleep Mode to Output High	C_L = 15 pF (Note 9)	*Figures 14, 16*	70	97	250	ns
t_{PSL}	Receiver Enable from Sleep Mode to Output Low	C_L = 15 pF (Note 9)	*Figures 14, 15*	70	95	250	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD1} and V_{OD2}.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.

Note 4: Delta $|V_{OD2}|$ and Delta $|V_{OC}|$ are changes in magnitude of V_{OD2} and V_{OC}, respectively, that occur when input changes state.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

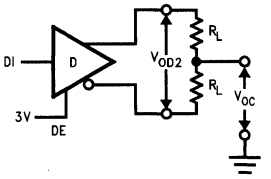
Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 8: C_L includes probe and jig capacitance.

Note 9: For enable from sleep mode delays DE = L and RE* = H for greater than 600 ns prior to test (device is in sleep mode).

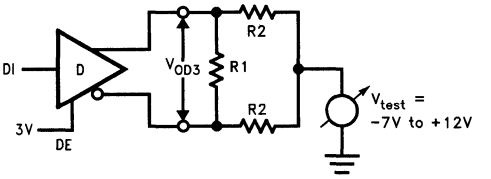
Note 10: For complete details of test, see RS-485.

Parameter Measurement Information



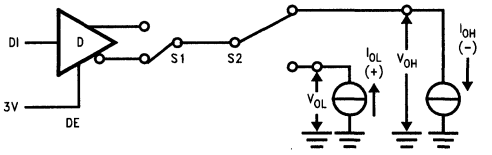
TL/F/12053-2

FIGURE 1. Driver V_{OD2} and V_{OC}



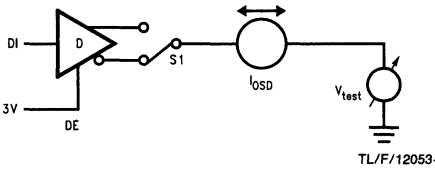
TL/F/12053-17

FIGURE 2. Driver V_{OD3}



TL/F/12053-3

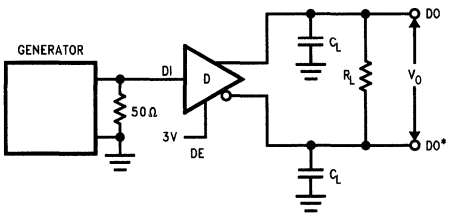
FIGURE 3. Driver V_{OH} and V_{OL}



TL/F/12053-4

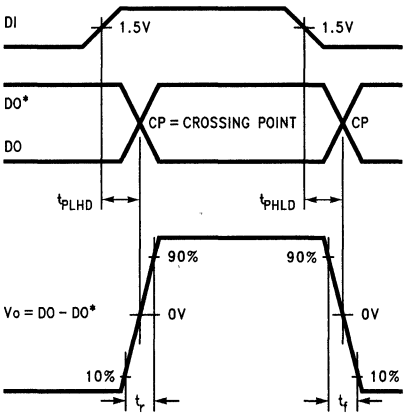
Vtest = −7V to +12V

FIGURE 4. Driver I_{OSD}



TL/F/12053-5

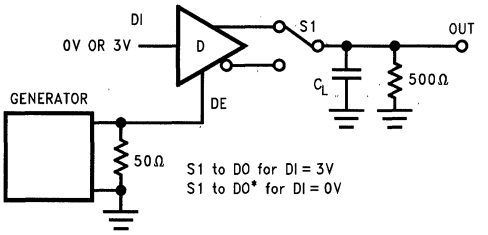
FIGURE 5. Driver Differential Propagation Delay Test Circuit



TL/F/12053-6

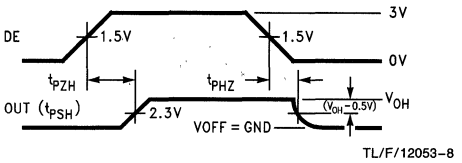
FIGURE 6. Driver Differential Propagation Delays and Differential Rise and Fall Times

Parameter Measurement Information (Continued)



TL/F/12053–7

FIGURE 7. TRI-STATE and Sleep Mode Test Circuit (t_{PZH}, (t_{PSH}), t_{PHZ})



TL/F/12053–8

FIGURE 8. TRI-STATE and Sleep Mode Waveforms (t_{PZH}, (t_{PSH}), t_{PHZ})

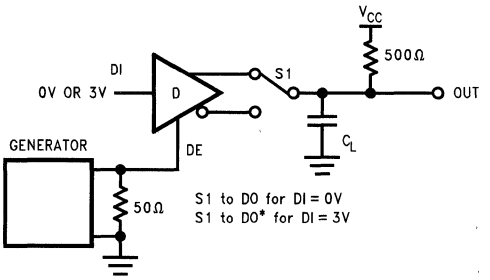


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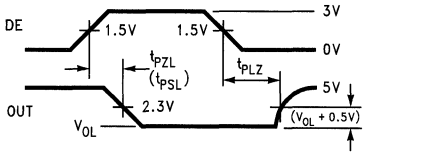
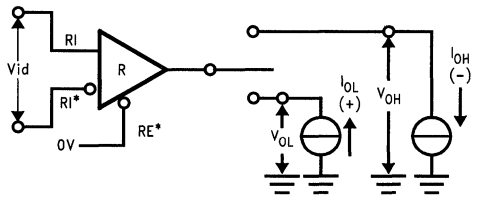
FIGURE 9. TRI-STATE and Sleep Mode Test Circuit (t_{PZL}, (t_{PSL}), t_{PLZ})



TL/F/12053–10

FIGURE 10. TRI-STATE and Sleep Mode Waveforms (t_{PZL}, (t_{PSL}), t_{PLZ})



TL/F/12053–11

FIGURE 11. Receiver V_{OH} and V_{OL}

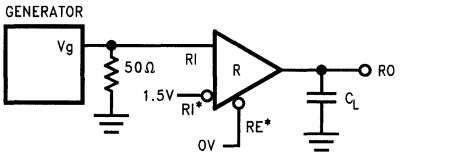


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FIGURE 12. Receiver Differential Propagation Delay Test Circuit

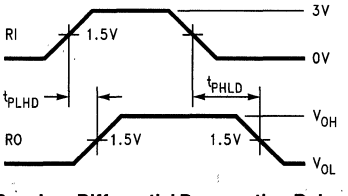

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FIGURE 13. Receiver Differential Propagation Delay Waveforms

Parameter Measurement Information (Continued)

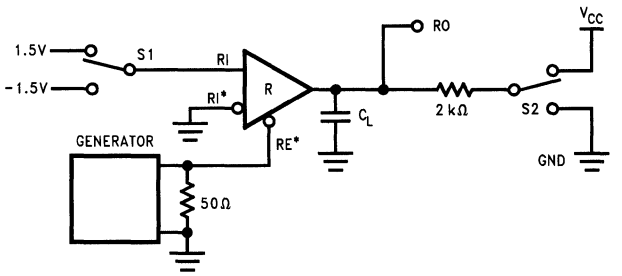

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FIGURE 14. Receiver TRI-STATE and Sleep Mode Test Circuit

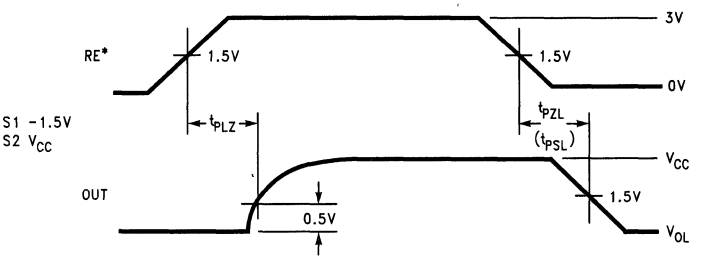

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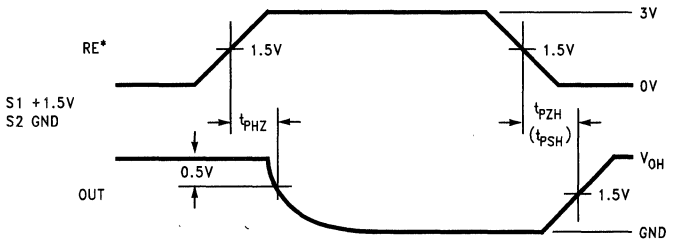
FIGURE 15. Receiver Enable and Disable Waveforms (t_{PLZ}, t_{PZL}, (t_{PSL}))



TL/F/12053–16

FIGURE 16. Receiver Enable and Disable Waveforms (t_{PHZ}, t_{PZH}, (t_{PSH}))

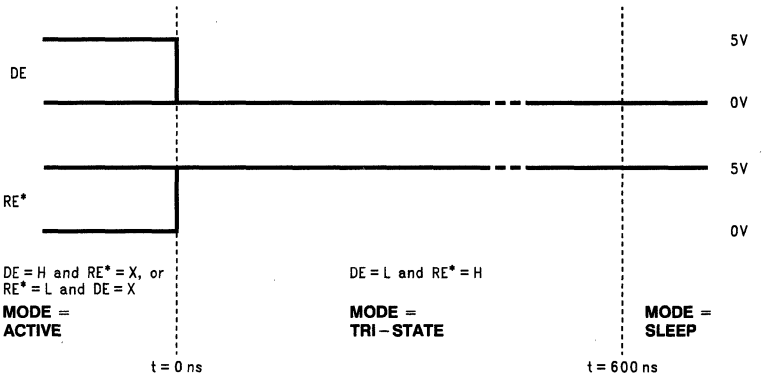


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FIGURE 17. Entering Sleep Mode Conditions

Typical Application Information

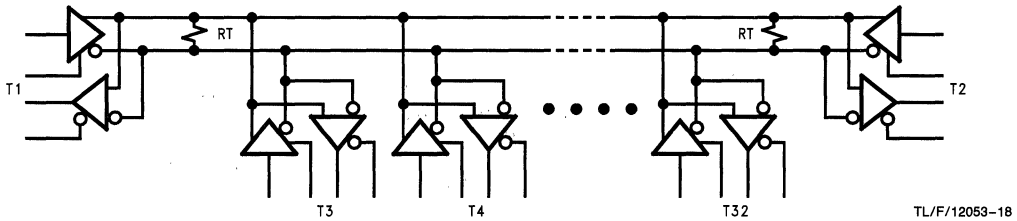


FIGURE 18. Typical RS-485 Bus Interface

TABLE I. Device Pin Descriptions

Pin No.	Name	Description
1	RO	Receiver Output: When RE (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI ≥ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI ≤ DO*/RI* by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) Inputs.
2	RE*	Receiver Output Enable: When RE* is LOW the receiver output is enabled. When RE* is HIGH, the receiver output is in TRI-STATE (OFF). When RE* is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
3	DE	Driver Output Enable: When DE is HIGH, the driver outputs are enabled. When DE is LOW, the driver outputs are in TRI-STATE (OFF). When RE* is HIGH and DE is LOW, the device will enter a low-current sleep mode after 600 ns.
4	DI	Driver Input: When DE (Driver Enable) is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection.
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO*/RI*	Driver Output/Receiver Input, 485 Bus Pin.
8	V_{CC}	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.75V to +5.25V.

Unit Load

A unit load for an RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see *Figure 19*). An RS-485 driver is capable of driving up to 32 unit loads. This allows up to 32 nodes on a single bus. Although sufficient for many applications, it is sometimes desirable to have even more nodes. For example, an aircraft that has 32 rows with 4 seats per row would benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS36C278, the DS36C279, and the DS36C280 all have ½ unit load and ¼ unit load (UL) options available. These devices will allow up to 64 nodes or 128 nodes guaranteed over temperature depending upon which option is selected. The ½ UL option is available in industrial temperature and the ¼ UL is available in commercial temperature.

First, for a ½ UL device the top and bottom borders shown in *Figure 19* are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see *Figure 19*). Second, for a ¼ UL device the top and bottom borders shown in *Figure 19* are scaled also. Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see *Figure 19*).

The advantage of the ½ UL and ¼ UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application where the number of slaves exceeds 32, the DS36C278/279/280 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

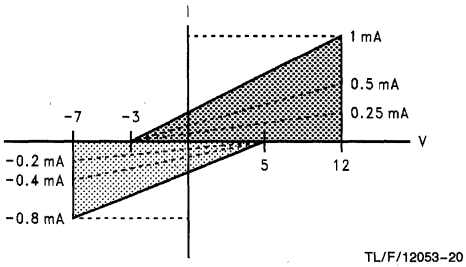


FIGURE 19. Input Current vs Input Voltage Operating Range

Unit Load (Continued)

The DS36C279 and DS36C280 have an additional feature which offers more advantages. The DS36C279 has an automatic sleep mode function for power conscious applications. The DS36C280 has a slew rate control for EMI conscious applications. Refer to the sleep mode and slew rate control portion of the application information section in the corresponding datasheet for more information on these features.

Sleep Mode

The DS36C279 features an automatic shutdown mode that allows the device to save power when not transmitting data. Since the shutdown mode is automatic, no external components are required. It may be used as little or as much as the application requires. The more the feature is utilized, the more power it saves.

The sleep mode is automatically entered when both the driver and receiver are disabled. This occurs when both the DE pin is asserted to a logic low and the RE* pin is asserted to a logic high. Once both pins are asserted the device will enter sleep mode typically in 50 ns. The DS36C279 is guaranteed to go into sleep mode within 600 ns after both pins are asserted. The device wakes up (comes out of sleep mode) when either the DE pin is asserted to a logic high and/or the RE* pin is asserted to a logic low. After the device enters sleep mode it will take longer for the device to wake up than it does for the device to enable from TRI-STATE. Refer to datasheet specifications t_{PSL} and t_{PSH} and compare with t_{PZL} and t_{PZH} for timing differences.

The benefit of the DS36C279 is definitely its power savings. When active the device has a maximum I_{CC} of 500 μA. When in sleep mode the device has a maximum I_{CC} of only 10 μA, which is 50 times less power than when active. The I_{CC} when the device is active is already very low but when in sleep mode the I_{CC} is ultra low.

National Semiconductor

DS36C280
Slew Rate Controlled CMOS EIA-RS-485 Transceiver

General Description

The DS36C280 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition, it is compatible with TIA/EIA-422-B.

The slew rate control feature allows the user to set the driver rise and fall times by using an external resistor. Controlled edge rates can reduce switching EMI.

The CMOS design offers significant power savings over its bipolar and ALS counterparts without sacrificing ruggedness against ESD damage. The device is ideal for use in battery powered or power conscious applications. I_{CC} is specified at 500 μA maximum.

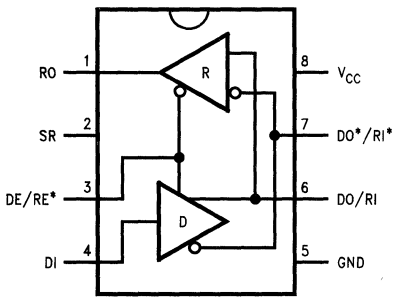
The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open†.

Features

- 100% RS-485 compliant
  — Guaranteed RS-485 device interoperation
- Low power CMOS design I_{CC} 500 μA max
- Adjustable slew rate control
  — Minimizes EMI affects
- Built-in power up/down glitch-free circuitry
  — Permits live transceiver insertion/displacement
- DIP and SOIC packages available
- Industrial temperature range −40°C to +85°C
- On-board thermal shutdown circuitry
  — Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range −7V to +12V
- Receiver open input fail-safe†
- ¼ unit load (DS36C280) ≥128 nodes
- ½ unit load (DS36C280T) ≥64 nodes
- ESD (human body model) ≥2 kV

Connection and Logic Diagram



TL/F/12052–1

Order Number DS36C280TM, DS36C280TN
DS36C280M and DS36C280N
See NS Package Number M08A or N08E

Truth Table

DRIVER SECTION			
DE/RE*	**DI**	**DO/RI**	**DO*/RI***
H	H	H	L
H	L	L	H
L	X	Z	Z

RECEIVER SECTION		
DE/RE*	**RI-RI***	**RO**
L	≥ +0.2V	H
L	≤ −0.2V	L
H	X	Z
L	OPEN†	H

†**Note:** Non-terminated, Open Inputs only

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) +12V

Input Voltage (DE/RE*, & DI) −0.5V to (V_{CC} +0.5V)

Common Mode (V_{CM})
Driver Output/Receiver Input ±15V

Input Voltage (DO/RI, DO*/RI*) ±14V

Receiver Output Voltage −0.5V to (V_{CC} +0.5V)

Maximum Package Power Dissipation @ +25°C
M Package 1190 mW, derate 9.5 mW/°C above +25°C
N Package 794 mW, derate 6.0 mW/°C above +25°C

Storage Temperature Range −65°C to +150°C

Lead Temperature (Soldering 4 sec) +260°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.75	+5.0	+5.25	V
Bus Voltage	−7		+12	V
Operating Free Air Temperature (T_A)				
DS36C280T	−40	+25	+85	°C
DS36C280	0	+25	+70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Reference		Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS								
V_{OD1}	Differential Output Voltage	I_O = 0 mA (No Load)	(422) (485)		1.5		5.0	V
V_{OD0}	Output Voltage	I_O = 0 mA			0		5.0	V
V_{OD0*}	Output Voltage	(Output to GND)			0		5.0	V
V_{OD2}	Differential Output Voltage (Termination Load)	R_L = 50Ω	(422)	*Figure 1*	2.0	2.8		V
		R_L = 27Ω	(485)		1.5	2.3	5.0	V
ΔV_{OD2}	Balance of V_{OD2} $\lvert V_{OD2} - V_{OD2*}\rvert$	R_L = 27Ω or 50Ω	(Note 4) (422, 485)		−0.2	0.1	+0.2	V
V_{OD3}	Differential Output Voltage (Full Load)	R1 = 54Ω, R2 = 375Ω	*Figure 2*		1.5	2.0	5.0	V
		V_{TEST} = −7V to +12V						
V_{OC}	Driver Common Mode Output Voltage	R_L = 27Ω	(485)	*Figure 1*	0		3.0	V
		R_L = 50Ω	(422)		0		3.0	V
ΔV_{OC}	Balance of V_{OC} $\lvert V_{OC} - V_{OC*}\rvert$	R_L = 27Ω or R_L = 50Ω	(Note 4) (422, 485)		−0.2		+0.2	V
I_{OSD}	Driver Output Short-Circuit Current	V_O = +12V	(485) *Figure 4*			200	+250	mA
		V_O = −7V	(485)			−190	−250	mA
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage	$V_O = V_{OH}$, I_O = −0.4 mA −7V ≤ V_{CM} ≤ +12V	(Note 5) (422, 485)			+0.035	+0.2	V
V_{TL}	Differential Input Low Threshold Voltage	$V_O = V_{OL}$, I_O = 0.4 mA −7V ≤ V_{CM} ≤ +12V			−0.2	−0.035		V
V_{HST}	Hysteresis	V_{CM} = 0V				70		mV
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V	DS36C280T		24	68		kΩ
R_{IN}	Input Resistance	−7V ≤ V_{CM} ≤ +12V	DS36C280		48	68		kΩ

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Reference	Min	Typ	Max	Units
I_{IN}	Line Input Current (Note 7)	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}	DS36C280	V_{IN} = +12V	0	0.19	0.25	mA
				V_{IN} = −7V	0	−0.1	−0.2	mA
		V_{CC} = 4.75 to 5.25 or 0V	DS36C280T	V_{IN} = +12V	0	0.19	0.5	mA
				V_{IN} = −7V	0	−0.1	−0.4	mA
I_{ING}	Line Input Current Glitch (Note 7)	Other Input = 0V, DE = V_{IL}, RE* = V_{IL}	DS36C280	V_{IN} = +12V	0	0.19	0.25	mA
				V_{IN} = −7V	0	−0.1	−0.2	mA
		V_{CC} = +3.0V or 0V T_A = 25°C	DS36C280T	V_{IN} = +12V	0	0.19	0.5	mA
				V_{IN} = −7V	0	−0.1	−0.4	mA
I_B	Input Balance Test	RS = 500Ω		(422) (Note 9)			±400	mV
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA, V_{ID} = +0.2V		RO *Figure 11*	3.5	4.6		V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA, V_{ID} = −0.2V				0.3	0.5	V
I_{OSR}	Short Circuit Current	V_O = GND		RO	7	35	85	mA
I_{OZR}	TRI-STATE Leakage Current	V_O = 0.4V to 2.4V					±1	μA
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE/RE*, DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}					2	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.0V	V_{IL} = 0V				−2	μA
		V_{CC} = +3.0V					−2	μA
		SR = 0V		SR			−1	mA
I_{CCR}	Power Supply Current (No Load)	Driver OFF, Receiver ON		V_{CC}		200	500	μA
I_{CCD}		Driver ON, Receiver OFF				200	500	μA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 3, 8, and 10)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 54Ω, C_L = 100 pF	*Figures 5, 6*	10	399	1000	ns
t_{PLHD}	Differential Propagation Delay Low to High			10	400	1000	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$			0	1	10	ns
t_r	Rise Time	SR = Open			2870		ns
t_f	Fall Time				3070		ns
t_r	Rise Time	SR = 100 kΩ			1590		ns
t_f	Fall Time				1640		ns
t_r	Rise Time	SR = Short		100	337	1000	ns
t_f	Fall Time			100	348	1000	ns

Switching Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 3, 8, and 10)

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DRIVER CHARACTERISTICS (Continued)							
t_{PHZ}	Disable Time High to Z	C_L = 15 pF	*Figures 7, 8*		1100	2000	ns
t_{PLZ}	Disable Time Low to Z		*Figures 9, 10*		500	800	ns
t_{PZH}	Enable Time Z to High	C_L = 100 pF	*Figures 7, 8*		300	500	ns
t_{PZL}	Enable Time Z to Low		*Figures 9, 10*		300	500	ns
RECEIVER CHARACTERISTICS							
t_{PHL}	Propagation Delay High to Low	C_L = 15 pF	*Figures 12, 13*	30	210	400	ns
t_{PLH}	Propagation Delay Low to High			30	190	400	ns
t_{SK}	Skew, $\|t_{PHL} - t_{PLH}\|$			0	20	50	ns
t_{PLZ}	Output Disable Time	C_L = 15 pF	*Figures 14, 15, 16*		50	150	ns
t_{PHZ}					55	150	ns
t_{PZL}	Output Enable Time				40	150	ns
t_{PZH}					45	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD1} and V_{OD2}.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = + 25°C.

Note 4: Delta $|V_{OD2}|$ and Delta $|V_{OC}|$ are changes in magnitude of V_{OD2} and V_{OC}, respectively, that occur when input changes state.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

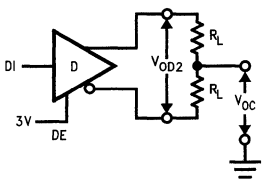
Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 8: C_L includes probe and jig capacitance.

Note 9: For complete details of test, see RS-485.

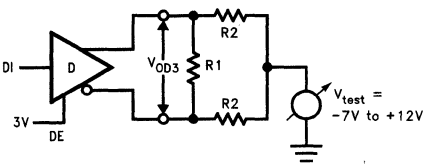
Note 10: SR = GND for all Switching Characteristics unless otherwise specified.

Parameter Measurement Information



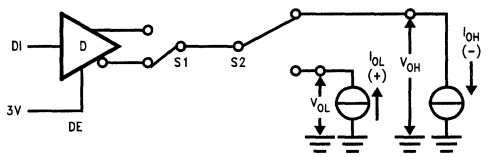
TL/F/12052–2

FIGURE 1. Driver V_{OD2} and V_{OC}



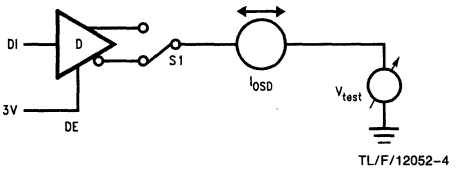
TL/F/12052–18

FIGURE 2. Driver V_{OD3}



TL/F/12052–3

FIGURE 3. Driver V_{OH} and V_{OL}

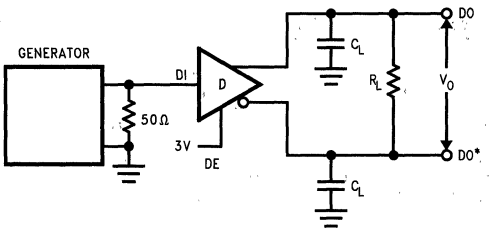


TL/F/12052–4

Vtest = −7V to +12V

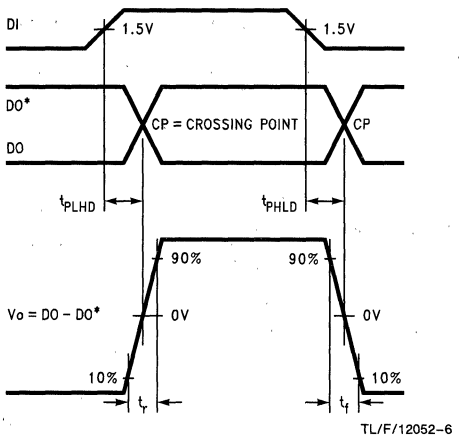
FIGURE 4. Driver I_{OSD}

Parameter Measurement Information (Continued)



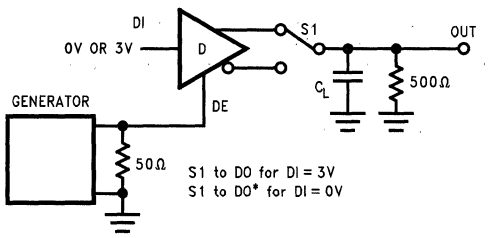
TL/F/12052-5

FIGURE 5. Driver Differential Propagation Delay Test Circuit



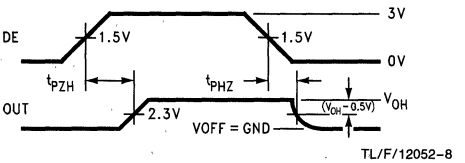
TL/F/12052-6

FIGURE 6. Driver Differential Propagation Delays and Differential Rise and Fall Times



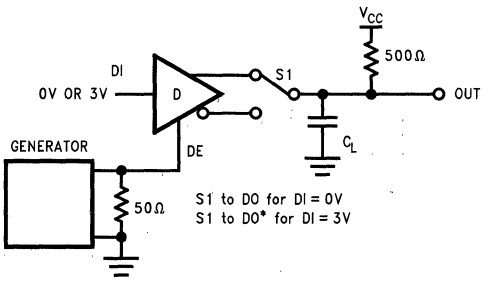
TL/F/12052-7

FIGURE 7. TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})



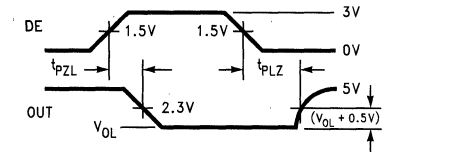
TL/F/12052-8

FIGURE 8. TRI-STATE Waveforms (t_{PZH}, t_{PHZ})



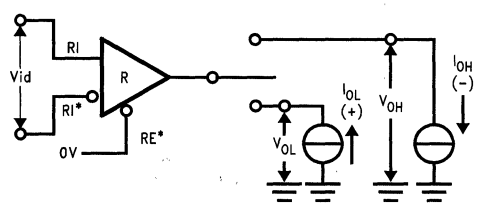
TL/F/12052-9

FIGURE 9. TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})



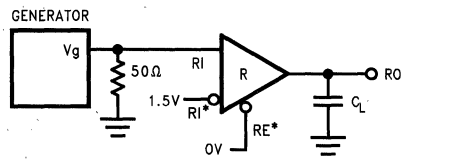
TL/F/12052-10

FIGURE 10. TRI-STATE Waveforms (t_{PZL}, t_{PLZ})



TL/F/12052-11

FIGURE 11. Receiver V_{OH} and V_{OL}



TL/F/12052-12

FIGURE 12. Receiver Differential Propagation Delay Test Circuit

Parameter Measurement Information (Continued)

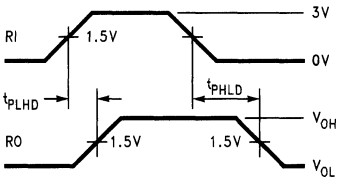


FIGURE 13. Receiver Differential Propagation Delay Waveforms

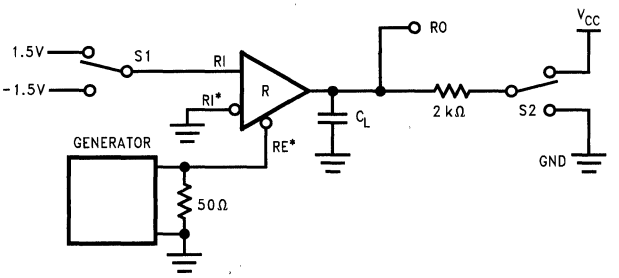


FIGURE 14. Receiver TRI-STATE Test Circuit

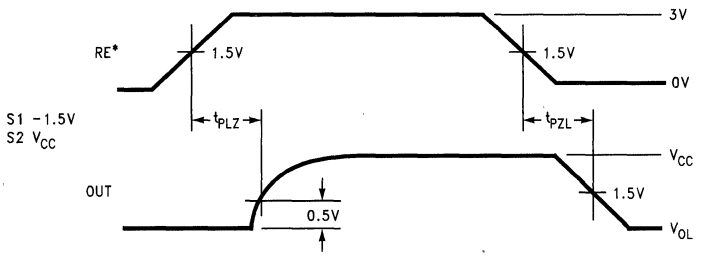


FIGURE 15. Receiver Enable and Disable Waveforms (t_{PLZ}, t_{PZL})

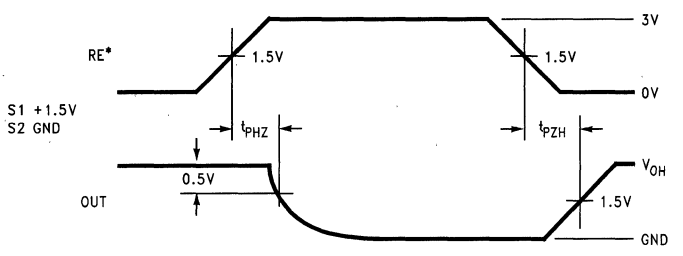


FIGURE 16. Receiver Enable and Disable Waveforms (t_{PHZ}, t_{PZH})

Typical Application Information

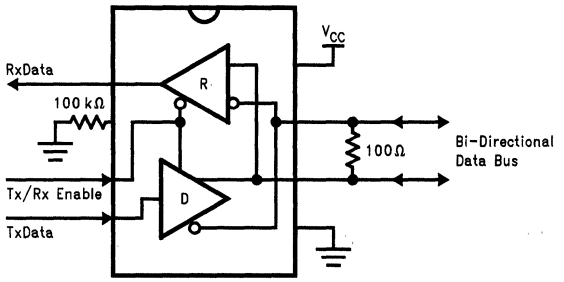


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FIGURE 17. Typical Pin Connection

TABLE I. Device Pin Descriptions

Pin #	Name	Description
1	RO	Receiver Output: When DE/RE* (Receiver Enable) is LOW, the receiver is enabled (ON), if DO/RI ≥ DO*/RI* by 200 mV, RO will be HIGH. If DO/RI ≤ DO*/RI* by 200 mV, RO will be LOW. Additionally RO will be HIGH for OPEN (Non-terminated) inputs.
2	SR	Slew Rate Control: A resistor connected to Ground controls the Driver Output rising and falling edge rates.
3	DE/RE*	Combined Driver and Receiver Output Enable: When signal is LOW the receiver output is enabled and the driver outputs are in TRI-STATE (OFF). When signal is HIGH, the receiver output is in TRI-STATE (OFF) and the driver outputs are enabled.
4	DI	Driver Input: When DE/RE* is HIGH, the driver is enabled, if DI is LOW, then DO/RI will be LOW and DO*/RI* will be HIGH. If DI is HIGH, then DO/RI is HIGH and DO*/RI* is LOW.
5	GND	Ground Connection
6	DO/RI	Driver Output/Receiver Input, 485 Bus Pin.
7	DO*/RI*	Driver Output/Receiver Input, 485 Bus Pin.
8	V_{CC}	Positive Power Supply Connection: Recommended operating range for V_{CC} is +4.75V to +5.25V.

Unit Load

A unit load for a RS-485 receiver is defined by the input current versus the input voltage curve. The gray shaded region is the defined operating range from −7V to +12V. The top border extending from −3V at 0 mA to +12V at +1 mA is defined as one unit load. Likewise, the bottom border extending from +5V at 0 mA to −7V at −0.8 mA is also defined as one unit load (see *Figure 18*). A RS-485 driver is capable of driving up to 32 unit loads. This allows upto 32 nodes on a single bus. Although sufficient for many applications, it is sometime desirable to have even more nodes. For example an aircraft that has 32 rows with 4 seats per row could benefit from having 128 nodes on one bus. This would allow signals to be transferred to and from each individual seat to 1 main station. Usually there is one or two less seats in the last row of the aircraft near the restrooms and food storage area. This frees the node for the main station.

The DS36C278, the DS36C279, and the DS36C280 all have ½ unit load and ¼ unit load (UL) options available. These devices will allow upto 64 nodes or 128 nodes guaranteed over temperature depending upon which option is selected. The ½ UL option is available in industrial temperature and the ¼ UL is available in commercial temperature.

First, for a ½ UL device the top and bottom borders shown in *Figure 18* are scaled. Both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.5 mA for the top border and −7V at −0.4 mA for the bottom border (see *Figure 18*). Second, for a ¼ UL device the top and bottom borders shown in *Figure 18* are scaled also. Again, both 0 mA reference points at +5V and −3V stay the same. The other reference points are +12V at +0.25 mA for the top border and −7V at −0.2 mA for the bottom border (see *Figure 18*).

Unit Load (Continued)

The advantage of the ½ UL and ¼ UL devices is the increased number of nodes on one bus. In a single master multi-slave type of application were the number of slaves exceeds 32, the DS36C278/279/280 may save in the cost of extra devices like repeaters, extra media like cable, and/or extra components like resistors.

The DS36C279 and DS36C280 have addition feature which offer more advantages. The DS36C279 has an automatic sleep mode function for power conscious applications. The DS36C280 has a slew rate control for EMI conscious applications. Refer to the sleep mode and slew rate control portion of the application information section in the corresponding datasheet for more information on these features.

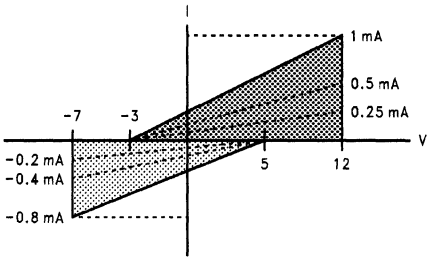

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FIGURE 18. Input Current vs Input Voltage Operating Range

Slew Rate Control

The DS36C280 features an adjustable slew rate control. This feature allows more control over EMI levels than tradition fixed edge rate devices. The slew rate control may be adjusted with or without any external components. The DS36C280 offers both low power (I_{CC} 500 μA max) and low EMI for an RS-485 interface.

The slew rate control is located at pin two of the device and only controls the driver output edges. The slew rate control pin (SR) may be left open or shorted to ground, with or without a resistor. When the SR pin is shorted to ground without a resistor, the driver output edges will transition typically 350 ns. When the SR pin is left open, the driver output edges will transition typically 3 μs. When the SR pin is shorted to ground with a resistor, the driver output edges will transition between 350 ns and 3 μs depending on the resistor value. Refer to the slew rate versus resistor value curve in this datasheet for determining resistor values and expected typical slew rate value. Please note, when slowing the edge rates of the device (see *Figure 19*) will decrease the maximum data rate also.

Differential Rise/Fall Time vs Slew Rate Resistor

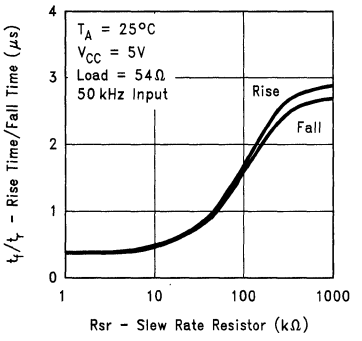

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FIGURE 19. Slew Rate Resistor vs Rise/Fall Time

National Semiconductor

DS36950
Quad Differential Bus Transceiver

General Description

The DS36950 is a low power, space-saving quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, computer I/O bus applications. A compact 20-pin surface mount PLCC package provides high transceiver integration and a very small PC board footprint.

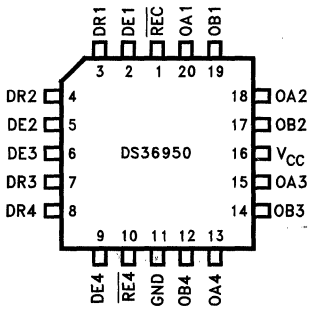
Timing uncertainty across an interface using multiple devices, a typical problem in a parallel interface, is specified—minimum and maximum propagation delay times are guaranteed.

Six devices can implement a complete IPI master or slave interface. Three transceivers in a package are pinned out for connection to a parallel databus. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

Features

- Pinout for IPI interface
- Compact 20-pin PLCC package
- Meets EIA-485 standard for multipoint bus transmission
- Greater than 60 mA source/sink
- Thermal Shutdown Protection

Pinout and Logic Diagram



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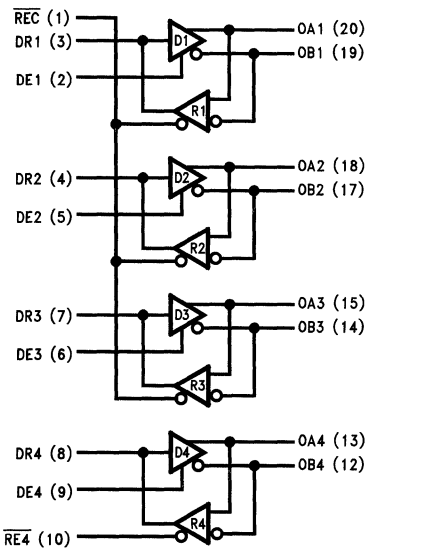
Order Number DS36950
See NS Package Number V20A



TL/F/10602–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Control Input Voltage	V_{CC} + 0.5V
Driver Input Voltage	V_{CC} + 0.5V
Driver Output Voltage/Receiver Input Voltage	−10V to +15V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ 25°C	
V Package	1.73W
Derate V Package 13.9 mW/°C above 25°C	
Storage Temp. Range	−65°C to +150°C
Lead Temp. (Soldering 4 Sec.)	260°C

Recommended Operating Conditions

Supply Voltage, V_{CC}	4.75V to 5.25V
Bus Voltage	−7V to +12V
Operating Free Air Temp. (T_A)	0°C to +70°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
V_{ODL}	Differential Driver Output Voltage (Full Load)	I_L = 60 mA, V_{CM} = 0V	1.5	1.9		V
V_{OD}	Differential Driver Output Voltage (Termination Load)	R_L = 100Ω (EIA-422)	2.0	3.5		V
		R_L = 54Ω (EIA-485)	1.5	3.2		V
$\Delta\lvert V_{OD}\rvert$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R_L = 54Ω or 100Ω (Note 4) *(Figure 1)* (EIA-485)			0.2	V
V_{OC}	Driver Common Mode Output Voltage (Note 5)	R_L = 54Ω *(Figure 1)* (EIA-485)			3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Common Mode Output Voltage	(Note 4) *(Figure 1)* (EIA-485)			0.2	V
V_{OH}	Output Voltage HIGH	I_{OH} = −55 mA	2.7	3.2		V
V_{OL}	Output Voltage LOW	I_{OL} = 55 mA		1.4	1.7	V
V_{IH}	Input Voltage HIGH		2.0			V
V_{IL}	Input Voltage LOW				0.8	V
V_{CL}	Input Clamp Voltage	I = −18 mA			−1.5	V
I_{IH}	Input High Current	V_I = 2.4V (Note 3)			20	μA
I_{IL}	Input Low Current	V_I = 0.4V (Note 3)			−20	μA
I_{OSC}	Driver Short-Circuit Output Current (Note 9)	V_O = −7V (EIA-485)		−130	−250	mA
		V_O = 0V (EIA-422)		−90	−150	mA
		V_O = +12V (EIA-485)		130	250	mA
RECEIVER CHARACTERISTICS						
I_{OSR}	Short Circuit Output Current	V_O = 0V (Note 9)	−15	−28	−75	mA
I_{OZ}	TRI-STATE® Output Current	V_O = 0.4V to 2.4V			20	μA
V_{OH}	Output Voltage High	V_{ID} = 0.20V, I_{OH} = −0.4 mA	2.4	3.0		V
V_{OL}	Output Voltage Low	V_{ID} = −0.20V, I_{OL} = 4 mA		0.35	0.5	V
V_{TH}	Differential Input High Threshold Voltage	V_O = V_{OH}, I_O = −0.4 mA (EIA-422/485)		0.03	0.20	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = V_{OL}, I_O = 4.0 mA (EIA-422/485)	−0.20	−0.03		V
V_{HST}	Hysteresis (Note 7)	V_{CM} = 0V	35	60		mV

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND RECEIVER CHARACTERISTICS							
V_{IH}	Enable Input Voltage High			2.0			V
V_{IL}	Enable Input Voltage Low					0.8	V
V_{CL}	Enable Input Clamp Voltage	$I = -18$ mA				−1.5	V
I_{IN}	Line Input Current (Note 8)	Other Input = 0V	$V_I = +12V$		0.5	1	mA
			$V_I = -7V$		−0.45	−0.8	mA
I_{IH}	Enable Input Current High	$V_{OH} = 2.4V$	$\overline{RE4}$ or DE			20	μA
			$\overline{REC}$			60	μA
I_{IL}	Enable Input Current Low	$V_{OL} = 0.4V$	$\overline{RE4}$ or DE			−20	μA
			$\overline{REC}$			−60	μA
I_{CC}	Supply Current (Note 10)	No Load, Outputs Enabled			75	90	mA
I_{CCZ}	Supply Current (Note 10)	No Load, Outputs Disabled			50	70	mA

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Conditions		Min	Typ	Max	Units
DRIVER SINGLE-ENDED CHARACTERISTICS						
t_{PZH}	$R_L = 110\Omega$ *(Figure 4)*			35	40	ns
t_{PZL}	$R_L = 110\Omega$ *(Figure 5)*			25	40	ns
t_{PHZ}	$R_L = 110\Omega$ *(Figure 4)*			15	25	ns
t_{PLZ}	$R_L = 110\Omega$ *(Figure 5)*			35	40	ns
DRIVER DIFFERENTIAL CHARACTERISTICS						
t_R, t_F	Rise & Fall Time	$R_L = 54\Omega$, $C_L = 50$ pF, $C_D = 15$ pF *(Figures 3, 8)*		13	16	ns
t_{PLHD}	Differential Propagation Delays (Note 15)		9	15	19	ns
t_{PHLD}			9	15	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Differential Skew			3	6	ns

Switching Characteristics (Continued)

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS						
t_{PLHD}	Differential Propagation Delays		9	14	19	ns
t_{PHLD}	C_L = 15 pF, V_{CM} = 1.5V *(Figure 6)*		9	14	19	ns
t_{SKD}	$\|t_{PLHD} - t_{PHLD}\|$ Differential Receiver Skew			1	3	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF *(Figure 7)*		15	22	ns
t_{ZL}	Output Enable Time to Low Level			20	30	ns
t_{HZ}	Output Disable Time from High Level			10	17	ns
t_{LZ}	Output Disable Time from Low Level			17	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is define as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{IH} and I_{IL} includes driver input current and receiver TRI-STATE leakage current.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.

Note 5: In EIA Standards EIA-422 and EIA-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 7: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

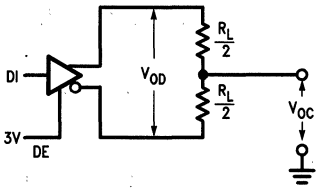
Note 8: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 9: Short one output at a time.

Note 10: Total package supply current.

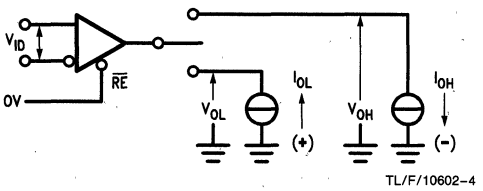
Note 11: All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Parameter Measurement Information



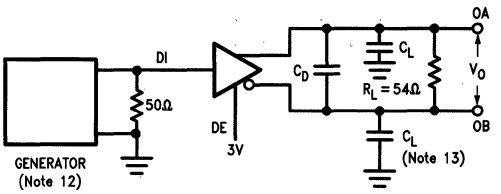
TL/F/10602-3

FIGURE 1. Driver V_{OD} and V_{OC}

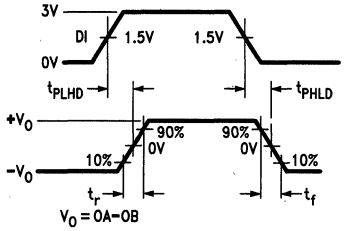


TL/F/10602-4

FIGURE 2. Receiver V_{OH} and V_{OL}

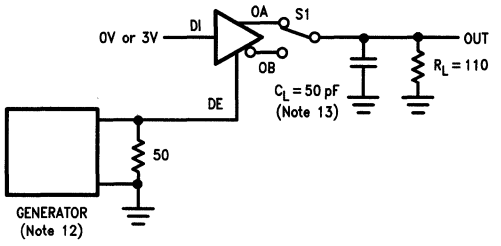


TL/F/10602-5



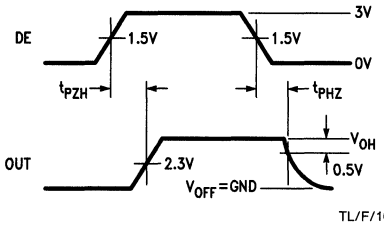
TL/F/10602-6

FIGURE 3. Driver Differential Propagation Delay and Transition Timing



TL/F/10602-9

S1 to OA for DI = 3V
S1 to OB for DI = 0V



TL/F/10602-10

FIGURE 4. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})

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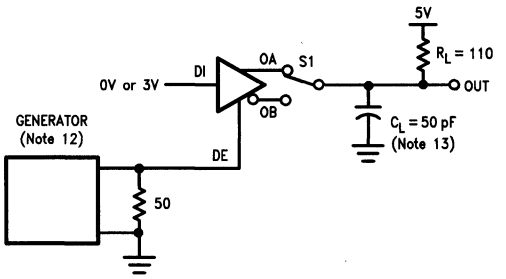

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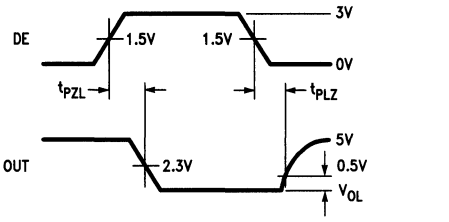

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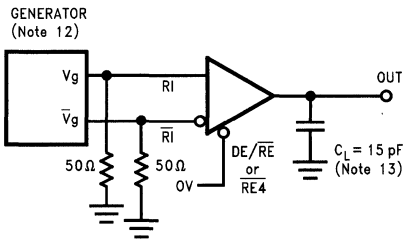
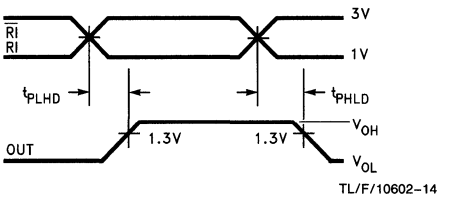
S1 to OA for DI = 0V
S1 to OB for DI = 3V

FIGURE 5. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})



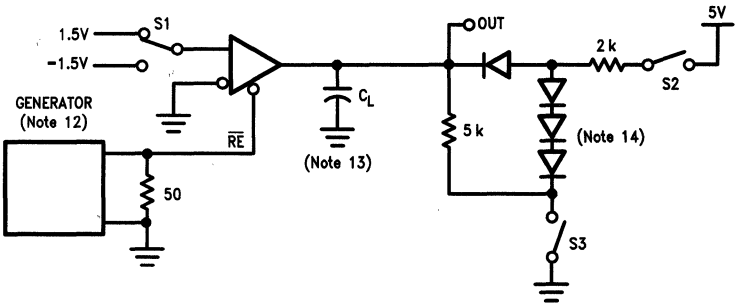


TL/F/10602–14

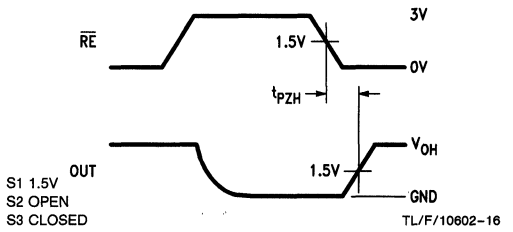
TL/F/10602–13

FIGURE 6. Receiver Differential Propagation Delay Timing

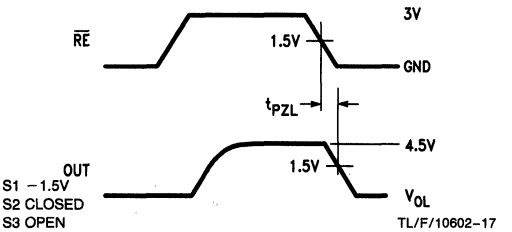
Parameter Measurement Information (Continued)



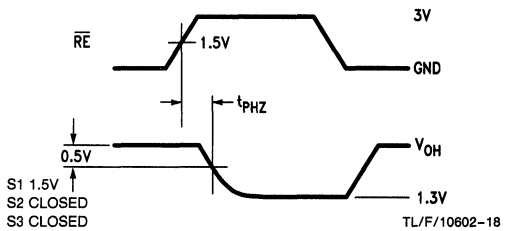
TL/F/10602–15



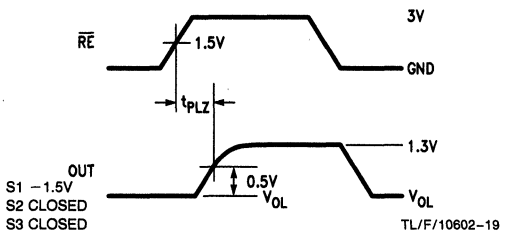
TL/F/10602–16



TL/F/10602–17

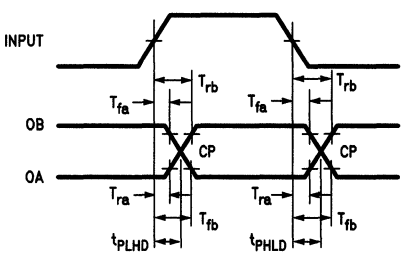


TL/F/10602–18



TL/F/10602–19

FIGURE 7. Receiver Enable and Disable Timing



TL/F/10602–20

$$TCP = \frac{(Tfb \times Trb) - (Tra \times Tfa)}{Trb - Tra - Tfa + Tfb}$$

TCP = Crossing Point

Tra, Trb, Tfa, and Tfb are propagation delay measurements to the 20% and 80% levels.

FIGURE 8. Propagation Delay Timing for Calculation of Driver Differential Propagation Delays

Note 12: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% Duty Cycle, t_f and t_r < 6.0 ns, Z_O = 50Ω

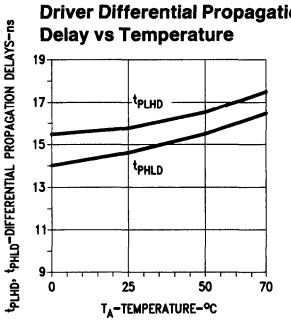
Note 13: C_L includes probe and stray capacitance.

Note 14: Diodes are 1N916 or equivalent.

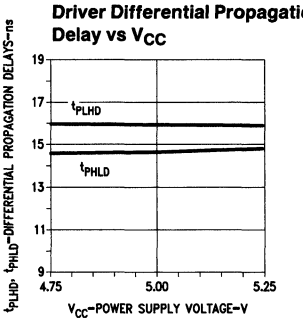
Note 15: Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs (See *Figure 8*).

Typical Performance Characteristics

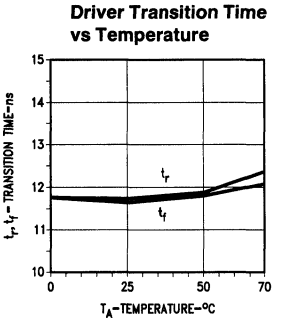
Driver Differential Propagation Delay vs Temperature



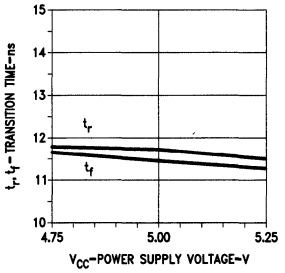
Driver Differential Propagation Delay vs V_{CC}



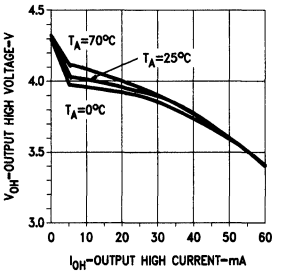
Driver Transition Time vs Temperature



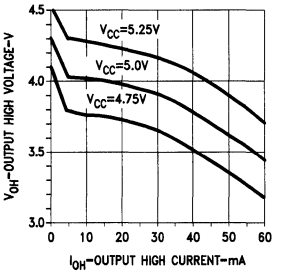
Driver Transition Time vs V_{CC}



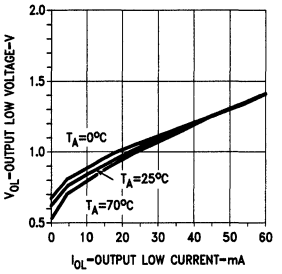
Driver V_{OH} vs I_{OH} vs Temperature



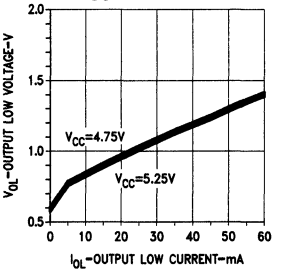
Driver V_{OH} vs I_{OH} vs V_{CC}



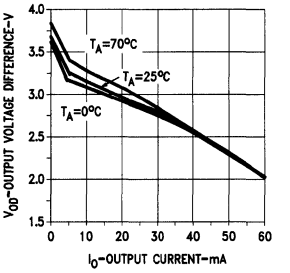
Driver V_{OL} vs I_{OL} vs Temperature



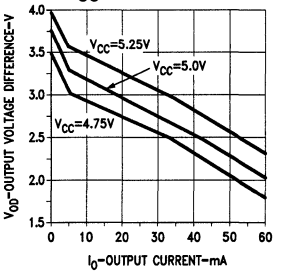
Driver V_{OL} vs I_{OL} vs V_{CC}



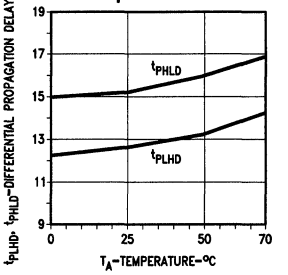
Driver V_{OD} vs I_O vs Temperature



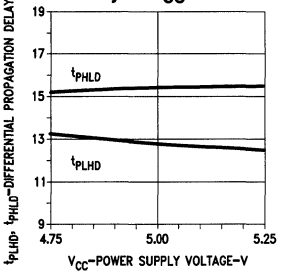
Driver V_{OD} vs I_O vs V_{CC}



Receiver Differential Propagation Delay vs Temperature



Receiver Differential Propagation Delay vs V_{CC}



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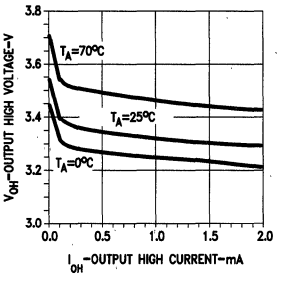
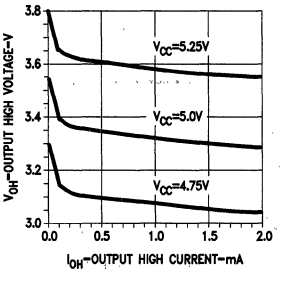
Typical Performance Characteristics (Continued)

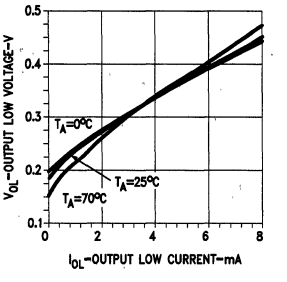
Receiver V_{OH} vs I_{OH} vs Temperature



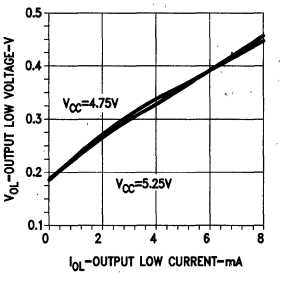
Receiver V_{OH} vs I_{OH} vs V_{CC}



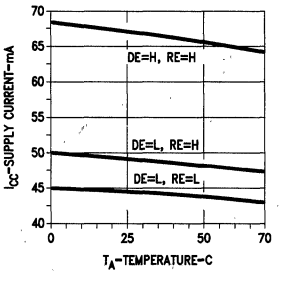
Receiver V_{OL} vs I_{OL} vs Temperature



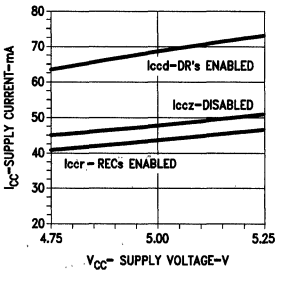
Receiver V_{OL} vs I_{OL} vs V_{CC}



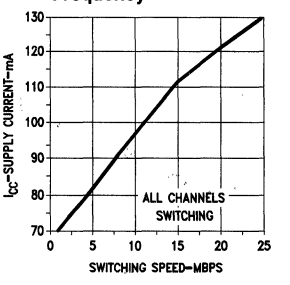
Supply Current vs Temperature



Power Supply Current vs Power Supply Voltage



Driver I_{CC} vs Switching Frequency



TL/F/10602–22

National Semiconductor

DS36954
Quad Differential Bus Transceiver

General Description

The DS36954 is a low power, quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, I/O bus applications. A compact 20-pin surface mount PLCC or SOIC package provides high transceiver integration and a very small PC board footprint.

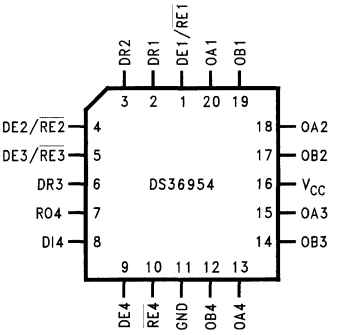
Propagation delay skew between devices is specified to aid in parallel interface designs—limits on maximum and minimum delay times are guaranteed.

Five devices can implement a complete SCSI initiator or target interface. Three transceivers in a package are pinned out for data bus connections. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

Features

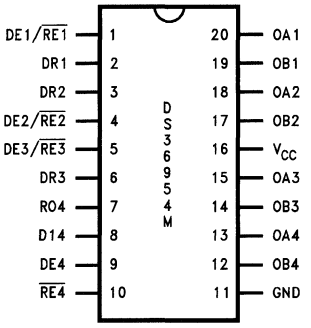
- Pinout for SCSI interface
- Compact 20-pin PLCC or SOIC package
- Meets EIA-485 standard for multipoint bus transmission
- Greater than 60 mA source/sink currents
- Thermal shutdown protection
- Glitch-free driver outputs on power up and down

Connection Diagrams



TL/F/11014–1

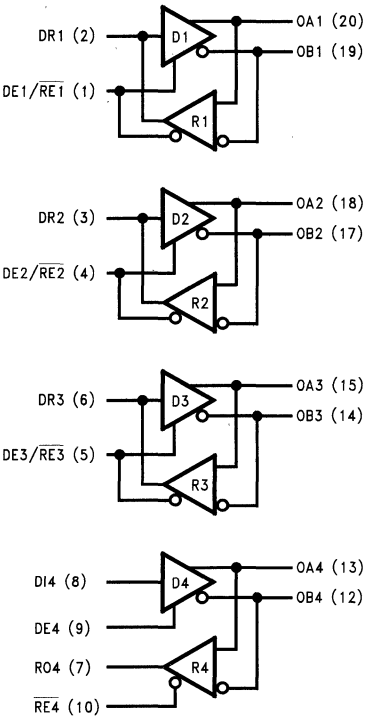
Order Number DS36954V
See NS Package Number V20A



TL/F/11014–19

Order Number DS36954M
See NS Package Number M20B

Logic Diagrams



TL/F/11014–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Control Input Voltage	V_{CC} + 0.5V
Driver Input Voltage	V_{CC} + 0.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ +25°C	
V Package	1.73W
M Package	1.73W
Derate V Package	13.9 mW/°C above +25°C
Derate M Package	13.7 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 Sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Free Air Temperature (T_A)	0	+70	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
V_{ODL}	Differential Driver Output Voltage (Full Load)	I_L = 60 mA, V_{CM} = 0V	1.5	1.9		V
V_{OD}	Differential Driver Output Voltage (Termination Load)	R_L = 100Ω (EIA-422)	2.0	2.25		V
		R_L = 54Ω (EIA-485)	1.5	2.0		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R_L = 54 or 100Ω (Note 4) *(Figure 1)* (EIA-422/485)			0.2	V
V_{OC}	Driver Common Mode Output Voltage (Note 5)	R_L = 54Ω *(Figure 1)* (EIA-485)			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage	(Note 4) *(Figure 1)* (EIA-422/485)			0.2	V
V_{OH}	Output Voltage High	I_{OH} = −55 mA	2.7	3.2		V
V_{OL}	Output Voltage Low	I_{OL} = 55 mA		1.4	1.7	V
V_{IH}	Input Voltage High		2.0			V
V_{IL}	Input Voltage Low				0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	V
I_{IH}	Input High Current	V_{IN} = 2.4V (Note 3)			20	μA
I_{IL}	Input Low Current	V_{IN} = 0.4V (Note 3)			−20	μA
I_{OSC}	Driver Short-Circuit Output Current (Note 9)	V_O = −7V (EIA-485)		−130	−250	mA
		V_O = 0V (EIA-422)		−90	−150	mA
		V_O = +12V (EIA-485)		130	250	mA

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER CHARACTERISTICS							
I_{OSR}	Short Circuit Output Current	V_O = 0V (Note 9)		−15	−28	−75	mA
I_{OZ}	TRI-STATE® Output Current	V_O = 0.4V to 2.4V				20	μA
V_{OH}	Output Voltage High	V_{ID} = 0.2V, I_{OH} = 0.4 mA		2.4	3.0		V
V_{OL}	Output Voltage Low	V_{ID} = −0.2V, I_{OL} = 4 mA			0.35	0.5	V
V_{TH}	Differential Input High Threshold Voltage	V_O = V_{OH}, I_O = −0.4 mA (EIA-422/485)			0.03	0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = V_{OL}, I_O = 4.0 mA (EIA-422/485)		−0.20	−0.03		V
V_{HST}	Hysteresis (Note 7)	V_{CM} = 0V		35	60		mV
DRIVER AND RECEIVER CHARACTERISTICS							
V_{IH}	Enable Input Voltage High			2.0			V
V_{IL}	Enable Input Voltage Low					0.8	V
V_{CL}	Enable Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
I_{IN}	Line Input Current (Note 8)	Other Input = 0V, DE/$\overline{RE}$ = 0.8V, DE4 = 0.8V	V_I = +12V		0.5	1.0	mA
			V_I = −7V		−0.45	−0.8	mA
I_{ING}	Line Input Current (Note 8)	Other Input = 0V, DE/$\overline{RE}$ and DE4 = 2V, V_{CC} = 3.0V, T_A = +25°C	V_I = +12V			1.0	mA
			V_I = −7V			−0.8	mA
I_{IH}	Enable Input Current High	V_{IN} = 2.4V, DE/$\overline{RE}$	V_{CC} = 3.0V		1	40	μA
			V_{CC} = 4.75V		1		μA
			V_{CC} = 5.25V		1	40	μA
		V_{IN} = 2.4V, DE4 or $\overline{RE4}$	V_{CC} = 3.0V		1	20	μA
			V_{CC} = 5.25V		1	20	μA
I_{IL}	Enable Input Current Low	V_{IN} = 0.8V, DE/$\overline{RE}$	V_{CC} = 3.0V		−6	−40	μA
			V_{CC} = 4.75V		−12		μA
			V_{CC} = 5.25V		−14	−40	μA
		V_{IN} = 0.8V, DE4 or $\overline{RE4}$	V_{CC} = 3.0V		−3	−20	μA
			V_{CC} = 5.25V		−7	−20	μA
I_{CCD}	Supply Current (Note 10)	No Load, DE/$\overline{RE}$ and DE4 = 2.0V			75	90	mA
I_{CCR}	Supply Current (Note 10)	No Load, DE/$\overline{RE}$ and $\overline{RE4}$ = 0.8V			50	70	mA

4

Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER SINGLE-ENDED CHARACTERISTICS							
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω	*(Figure 5)*		35	40	ns
t_{PZL}	Output Enable Time to Low Level		*(Figure 6)*		25	40	ns
t_{PHZ}	Output Disable Time to High Level		*(Figure 5)*		15	25	ns
t_{PLZ}	Output Disable Time to Low Level		*(Figure 6)*		35	40	ns
DRIVER DIFFERENTIAL CHARACTERISTICS							
t_r, t_f	Rise and Fall Time	R_L = 54Ω C_L = 50 pF C_D = 15 pF *(Figures 3, 4,* and *9)*			13	16	ns
t_{PLHD}	Differential Propagation Delays (Note 15)			9	15	19	ns
t_{PHLD}				9	12	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Diff. Skew				3	6	ns
RECEIVER CHARACTERISTICS							
t_{PLHD}	Differential Propagation Delays	C_L = 15 pF V_{CM} = 2.0V *(Figure 7)*		9	14	19	ns
t_{PHLD}				9	13	19	ns
t_{SKD}	$\lvert t_{PLHD} - t_{PHLD} \rvert$ Diff. Receiver Skew				1	3	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF *(Figure 8)*			15	22	ns
t_{PZL}	Output Enable Time to Low Level				20	30	ns
t_{PHZ}	Output Disable Time from High Level				20	30	ns
t_{PLZ}	Output Disable Time from Low Level				17	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: I_{IH} and I_{IL} include driver input current and receiver TRI-STATE leakage current on DR(1–3).

Note 4: Δ IVODI and Δ IVOCI are changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes state.

Note 5: In EIA Standards EIA-422 and EIA-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 7: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

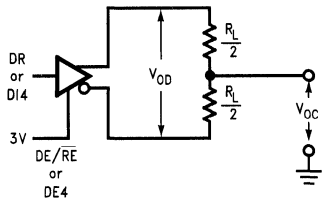
Note 8: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Note 9: Short one output at a time.

Note 10: Total package supply current.

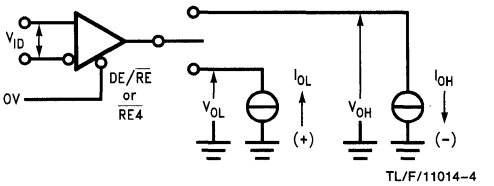
Note 11: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Parameter Measurement Information



TL/F/11014-3

FIGURE 1. Driver V_{OD} and V_{OC} (Note 13)



TL/F/11014-4

FIGURE 2. Receiver V_{OH} and V_{OL}

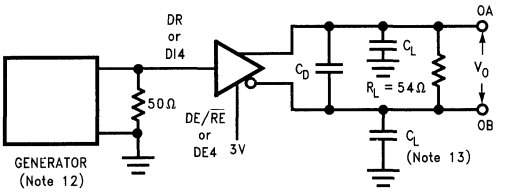


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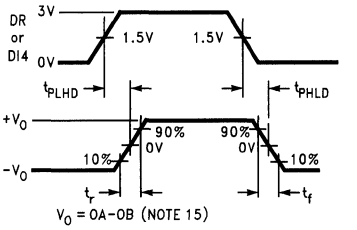
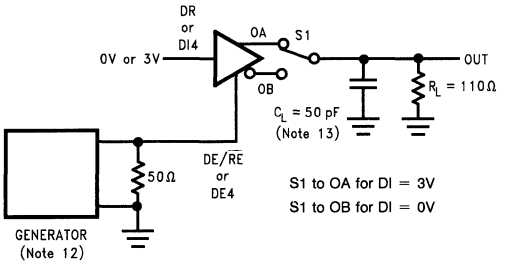
FIGURE 3. Driver Differential Propagation Delay Load Circuit

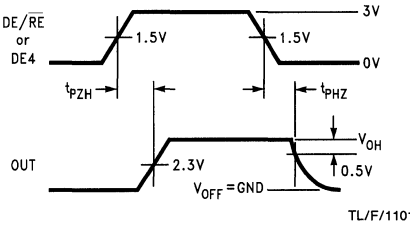


TL/F/11014-6

FIGURE 4. Driver Differential Propagation Delays and Transition Times

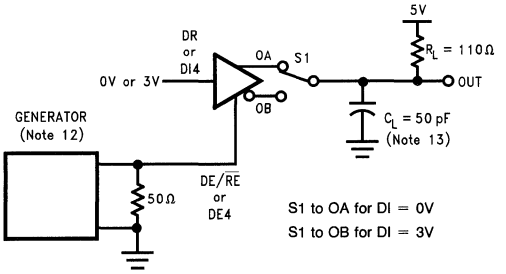


TL/F/11014-7



TL/F/11014-8

FIGURE 5. Driver Enable and Disable Timing (t_{PZH}, t_{PHZ})



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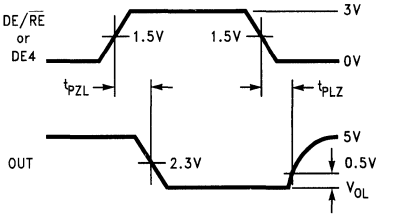

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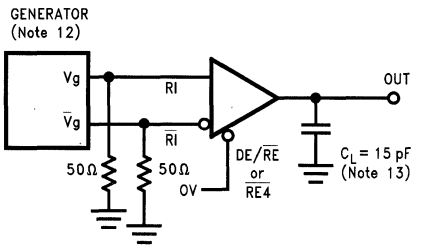
FIGURE 6. Driver Enable and Disable Timing (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)



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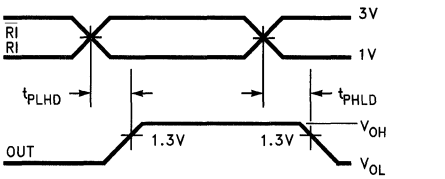

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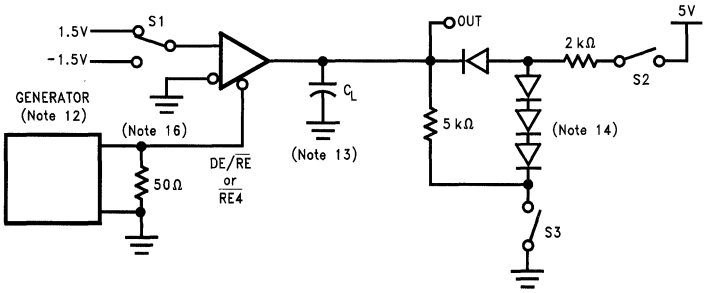
FIGURE 7. Receiver Differential Propagation Delay Timing



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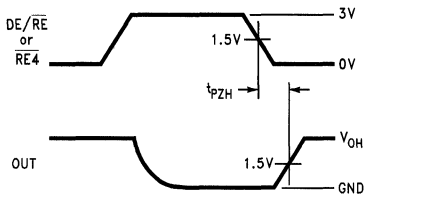

S1 1.5V
S2 Open
S3 Closed

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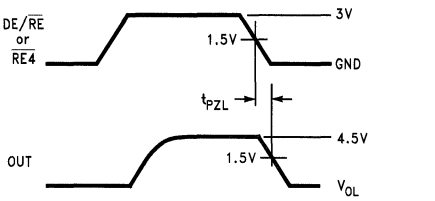
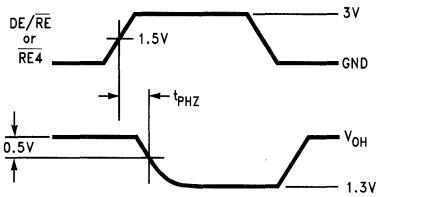


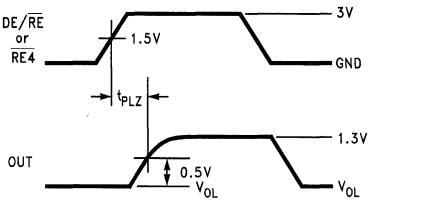
S1 −1.5V
S2 Closed
C3 Open

TL/F/11014–15



S1 1.5V
S2 Closed
C3 Closed

TL/F/11014–16



S1 −1.5V
S2 Closed
C3 Closed

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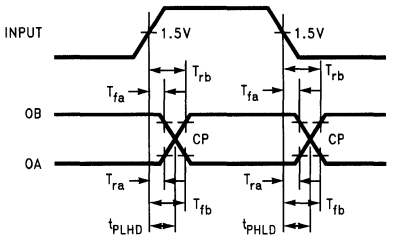
FIGURE 8. Receiver Enable and Disable Timing

Parameter Measurement Information (Continued)



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$$T_{CP} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

T_{ra}, T_{rb}, T_{fa} and T_{fb} are propagation delay measurements to the 20% and 80% levels.

T_{CP} = Crossing Point

FIGURE 9. Propagation Delay Timing for Calculations of Driver Differential Propagation Delays

Note 12: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 13: C_L includes probe and stray capacitance.

Note 14: Diodes are 1N916 or equivalent.

Note 15: Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs *(Figure 9)*.

Note 16: On transceivers 1–3 the driver is loaded with receiver input conditions when DE/$\overline{RE}$ is high. Do not exceed the package power dissipation limit when testing.

National Semiconductor

DS75176B/DS75176BT
Multipoint RS-485/RS-422 Transceivers

General Description

The DS75176B is a high speed differential TRI-STATE® bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition, it is compatible with RS-422.

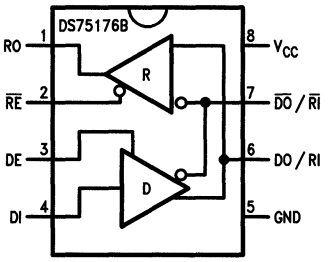
The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays.
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out compatible with DS3695/A and SN75176A/B.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagram



TL/F/8759–1

Top View

Order Number DS75176BN, DS75176BTN, DS75176BM or DS75176BTM
See NS Package Number N08E or M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Control Input Voltages	7V
Driver Input Voltage	7V
Driver Output Voltages	+15V/ −10V
Receiver Input Voltages (DS75176B)	+15V/ −10V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @25°C	
for M Package	675 mW (Note 5)
for N Package	900 mW (Note 4)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Voltage at Any Bus Terminal (Separate or Common Mode)	−7	+12	V
Operating Free Air Temperature T_A			
DS75176B	0	+70	°C
DS75176BT	−40	+85	°C
Differential Input Voltage, VID (Note 6)	−12	+12	V

Electrical Characteristics (Notes 2 and 3)

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		*(Figure 1)*	R = 50Ω; (RS-422) (Note 7)	2			V
				R = 27Ω; (RS-485)	1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States		*(Figure 1)*	R = 27Ω			0.2	V
V_{OC}	Driver Common Mode Output Voltage						3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States						0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage						0.8	
V_{CL}	Input Clamp Voltage			$I_{IN} = -18$ mA			−1.5	
I_{IL}	Input Low Current			$V_{IL} = 0.4V$			−200	μA
I_{IH}	Input High Current			$V_{IH} = 2.4V$			20	μA
I_{IN}	Input Current	DO/RI, $\overline{DO}/\overline{RI}$	$V_{CC} = 0V$ or 5.25V, DE = 0V	$V_{IN} = 12V$			+1.0	mA
				$V_{IN} = -7V$			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		$-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ μA		2.7			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA (Note 7)				0.5	V
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max, $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply Current		No Load (Note 7)	Driver Outputs Enabled			55	mA
				Driver Outputs Disabled			35	mA

Electrical Characteristics (Notes 2 and 3)

$0°C \le T_A \le 70°C$, $4.75V < V_{CC} < 5.25V$ unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OSD}	Driver Short-Circuit Output Current	$V_O = -7V$ (Note 7)			−250	mA
		$V_O = +12V$ (Note 7)			+250	mA
I_{OSR}	Receiver Short-Circuit Output Current	$V_O = 0V$	−15		−85	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 4: Derate linearly at 5.56 mW/°C to 650 mW at 70°C.

Note 5: Derate linearly @ 6.11 mW/°C to 400 mW at 70°C.

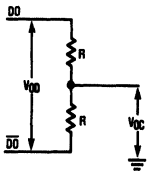
Note 6: Differential - Input/Output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

Note 7: All worst case parameters for which note 7 is applied, must be increased by 10% for DS75176BT. The other parameters remain valid for $-40°C < T_A < +85°C$.

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$

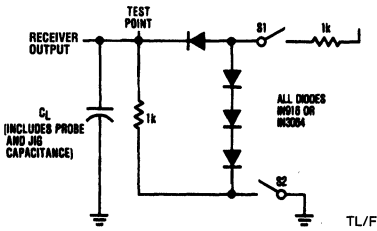
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF		12	22	ns
t_{PHL}	Driver Input to Output			17	22	ns
t_r	Driver Rise Time	$R_{L_{DIFF}} = 60\Omega$, $C_{L1} = C_{L2} = 100$ pF (*Figures 3* and *5*)			18	ns
t_f	Driver Fall Time				18	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100$ pF (*Figures 4* and *6*) S1 Open		29	100	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100$ pF (*Figures 4* and *6*) S2 Open		31	60	ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15$ pF (*Figures 4* and *6*) S2 Open		13	30	ns
t_{HZ}	Driver Disable Time from High	$C_L = 15$ pF (*Figures 4* and *6*) S1 Open		19	200	ns
t_{PLH}	Receiver Input to Output	$C_L = 15$ pF (*Figures 2* and *7*) S1 and S2 Closed		30	37	ns
t_{PHL}	Receiver Input to Output			32	37	ns
t_{ZL}	Receiver Enable to Output Low	$C_L = 15$ pF (*Figures 2* and *8*) S2 Open		15	20	ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15$ pF (*Figures 2* and *8*) S1 Open		11	20	ns
t_{LZ}	Receiver Disable from Low	$C_L = 15$ pF (*Figures 2* and *8*) S2 Open		28	32	ns
t_{HZ}	Receiver Disable from High	$C_L = 15$ pF (*Figures 2* and *8*) S1 Open		13	35	ns

AC Test Circuits



TL/F/8759–2

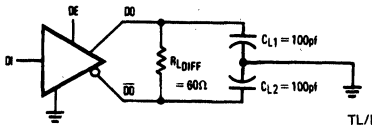
FIGURE 1



TL/F/8759–3

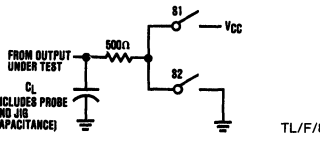
Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

FIGURE 2



TL/F/8759–4

FIGURE 3

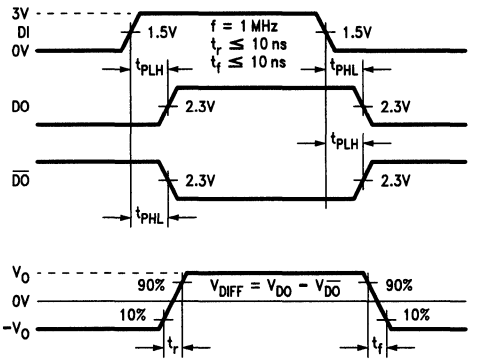


TL/F/8759–5

Note: Unless otherwise specified the switches are closed.

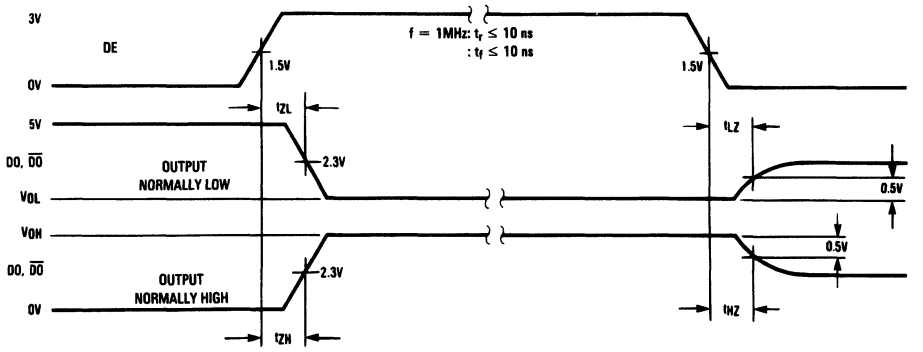
FIGURE 4

Switching Time Waveforms



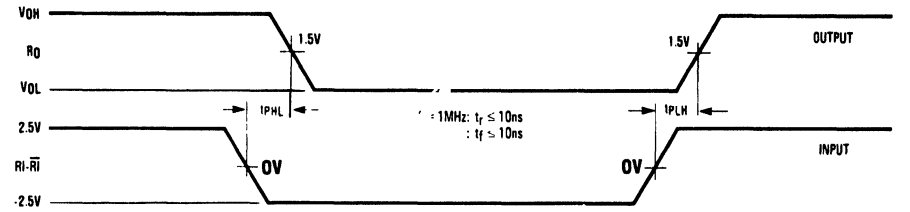
TL/F/8759–6

FIGURE 5. Driver Propagation Delays and Transition Times



TL/F/8759–7

FIGURE 6. Driver Enable and Disable Times



TL/F/8759–8

Note: Differential input voltage may may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays

Switching Time Waveforms (Continued)

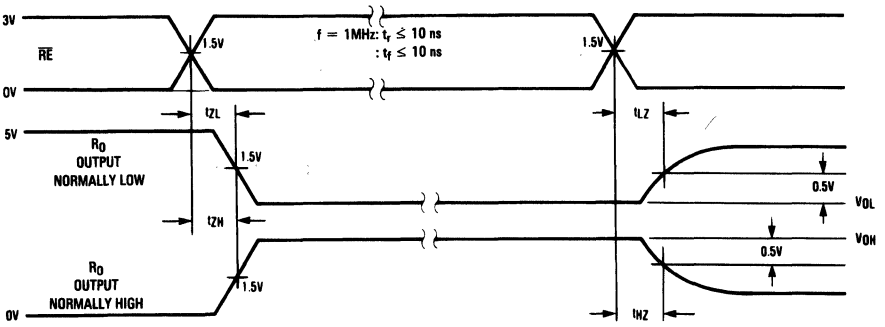


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FIGURE 8. Receiver Enable and Disable Times

Function Tables

DS75176B Transmitting

Inputs			Line Condition	Outputs	
$\overline{RE}$	DE	DI		$\overline{DO}$	DO
X	1	1	No Fault	0	1
X	1	0	No Fault	1	0
X	0	X	X	Z	Z
X	1	X	Fault	Z	Z

DS75176B Receiving

Inputs			Outputs
$\overline{RE}$	DE	RI-$\overline{RI}$	RO
0	0	$\geq +0.2V$	1
0	0	$\leq -0.2V$	0
0	0	Inputs Open**	1
1	0	X	Z

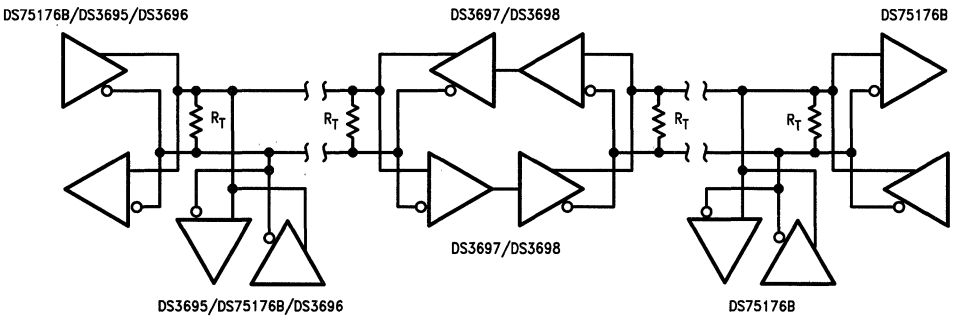
X — Don't care condition

Z — High impedance state

Fault — Improper line conditons causing excessive power dissipation in the driver, such as shorts or bus contention situations

**This is a fail safe condition

Typical Application



TL/F/8759–11

National Semiconductor

DS96172/DS96174
RS-485/RS-422 Quad Differential Line Drivers

General Description

The DS96172 and DS96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The DS96172 features an active high and active low Enable, common to all four drivers. The DS96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96173, DS96175, DS96176 AND DS96177.

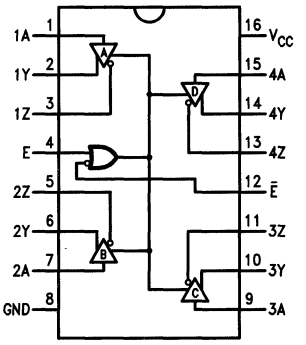
Features

- Meets EIA Standard RS-485 and RS-422A
- Monotonic differential output switching
- Transmission rate to 10 Mbs
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7V to +12V
- Operates from single +5V supply
- Thermal shutdown protection
- DS96172/DS96174 are lead and function compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively

4

Connection Diagrams

16-Lead DIP
DS96172



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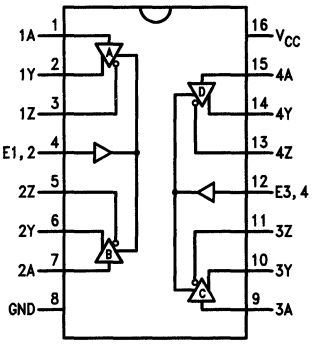
Top View

16-Lead DIP
DS96174



TL/F/9626–2

Top View

Order Number DS96172CJ or DS96174CJ
See NS Package Number J16A
Order Number DS96172CN or DS96174CN
See NS Package Number N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Supply Voltage	7V
Enable Input Voltage	5.5V
Maximum Power Dissipation*	25°C
J-Cavity Package	1.74W
N-Molded Package	1.98W

*Derate cavity package 14 mW/°C above 25°C; derate molded DIP package l6 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Output Voltage (V_{OC})	−7		+12	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

over recommended temperature and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA			3.1		V
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA			0.8		V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, *Figure 1*		1.5	2		V
		R_L = 100Ω, *Figure 1*		2	2.3		V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*				±0.2	V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω, *Figure 1*				3	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to 12V				±100	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to 12V			±50	±200	μA
I_{IH}	Input Current HIGH	V_I = 2.7V				20	μA
I_{IL}	Input Current LOW	V_I = 0.5V				−100	μA
I_{OS}	Short Circuit Output Current (Note 6)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled		50	70	mA
			Output Disabled		50	60	

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 2*		15	25	ns
t_{TD}	Differential Output Transition Time			15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 3*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 4*		30	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 5*		30	45	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 4*		25	35	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 5*		30	45	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96172/DS96174. All typicals are given for V_{CC} = 5V and T_A = 25°C.

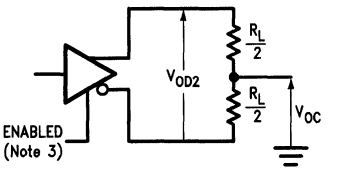
Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Δ $|V_{OD}|$ and Δ$|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

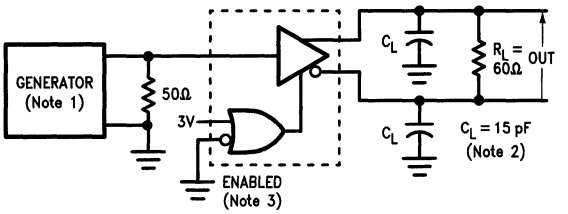
Note 6: Only one output at a time should be shorted.

Parameter Measurement Information

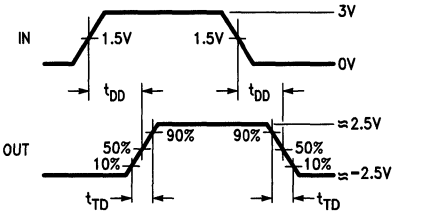


TL/F/9626–4

FIGURE 1. Differential and Common Mode Output Voltage



TL/F/9626–5



TL/F/9626–6

FIGURE 2. Differential Output Delay and Transition Times

Parameter Measurement Information (Continued)

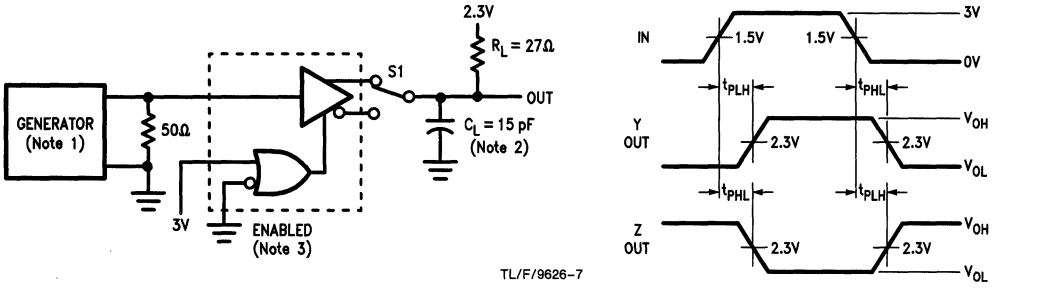


FIGURE 3. Propagation Delay Times

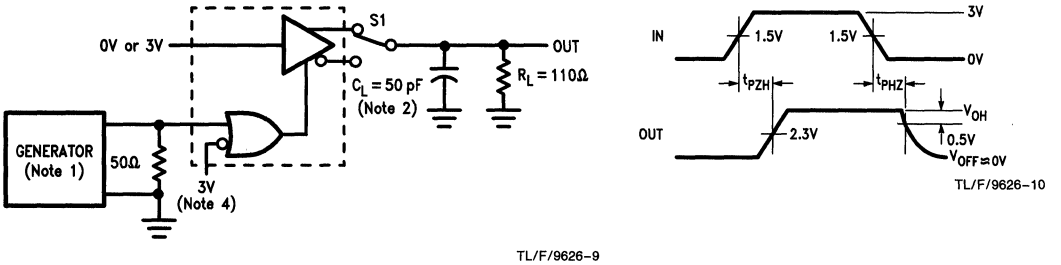


FIGURE 4. t_{PZH} and t_{PHZ}

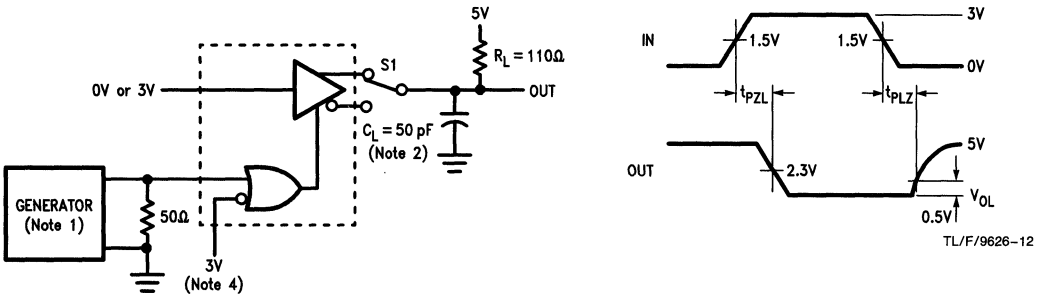


FIGURE 5. t_{PZL} and t_{PLZ}

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

Note 3: DS96172 with active high and active low Enables is shown here. DS96174 has active high Enable only.

Note 4: To test the active low Enable $\overline{E}$ of DS96172, ground E and apply an inverted waveform to $\overline{E}$. DS96174 has active high Enable only.

Function Tables

DS96172

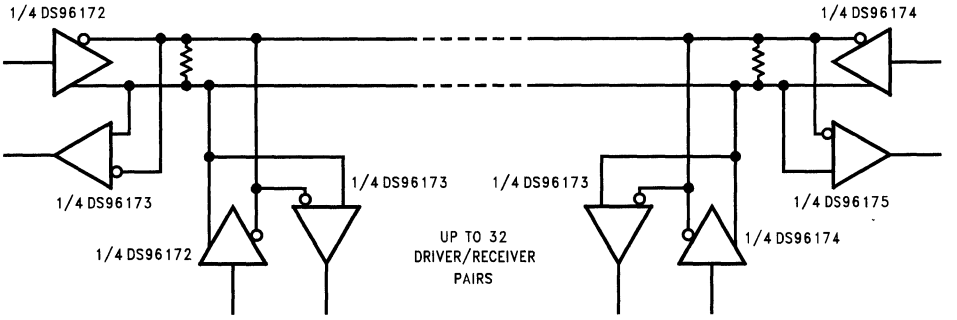
Input A	Enables		Outputs	
	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96174

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Typical Application



TL/F/9626–13

FIGURE 6

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96F172C/DS96F172M/DS96F174C/DS96F174M EIA-485/EIA-422 Quad Differential Drivers

General Description

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

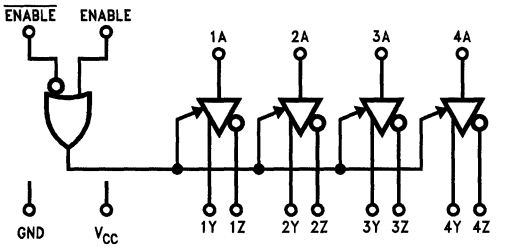
The DS96F172 and the DS96F174 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Features

- Meets EIA-485 and EIA-422A standards
- Monotonic differential output switching
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7.0V to +12V
- Operates from single +5.0V supply
- Reduced power consumption
- Thermal shutdown protection
- DS96F172 and DS96F174 are lead and function compatible with the SN75172/174 or the AM26LS31/MC3487
- Military temperature range available
- Qualified for MIL-STD-883C
- Standard military drawings available (SMD)
- Available in DIP (J), LCC (E), and Flatpak (W) packages

Logic Diagrams

DS96F172



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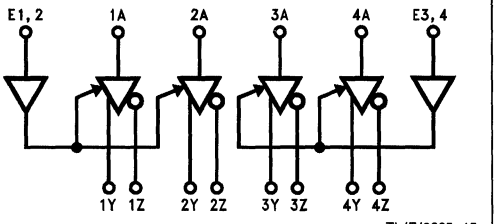
DS96F174



TL/F/9625–15

Function Tables (Each Driver)

DS96F172

Input	Enable		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96F174

Input	Enable	Outputs	
A	E	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately on the following pages.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C Ceramic DIP (J)	1500 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

*Derate "J" package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F172C/DS96F174C	4.75	5.0	5.25	V
DS96F172M/DS96F174M	4.50	5.0	5.50	
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A)				
DS96F172C/DS96F174C	0		+70	°C
DS96F172M/DS96F174M	−55		+125	

Electrical Characteristics

Over recommended supply voltage and operating temperature range, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW		T_A = 0°C to +70°C			0.8	V
			T_A = −55°C to +125°C			0.7	
V_{OH}	Output Voltage HIGH	I_{OH} = −33 mA	T_A = 0°C to +70°C	3.0			V
V_{OL}	Output Voltage LOW	I_{OL} = 33 mA	T_A = 0°C to +70°C			2.0	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, *Figure 1*	T_A = −55°C	1.2	2.0		V
				1.5			
		R_L = 100Ω, *Figure 1*		2.0	2.3		
V_{OD}	Differential Output Voltage	*Figure 1a*	T_A = 0°C to +70°C	1.0			V
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*	−40°C to +125°C			±0.2	V
			−55°C to +125°C			±0.4	V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)	R_L = 54Ω or 100Ω, *Figure 1*				±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V				±50	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±20	±50	μA
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−50	μA
I_{OS}	Short Circuit Output Current (Note 6)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = +12V				250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			30	

COMMERCIAL

Switching Characteristics $V_{CC} = 5.0V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	$R_L = 60\Omega$, *Figure 2*		15	20	ns
t_{TD}	Differential Output Transition Time			15	22	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	$R_L = 27\Omega$, *Figure 3*		12	16	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			12	16	ns
t_{ZH}	Output Enable Time to High Level	$R_L = 110\Omega$, *Figure 4*		25	32	ns
t_{ZL}	Output Enable Time to Low Level	$R_L = 110\Omega$, *Figure 5*		25	32	ns
t_{HZ}	Output Disable Time from High Level	$R_L = 110\Omega$, *Figure 4*		25	30	ns
t_{LZ}	Output Disable Time from Low Level	$R_L = 110\Omega$, *Figure 5*		20	25	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND (Note 7)	*Figure 5*		300		ns
t_{SKEW}	Driver Output to Output	$R_L = 60\Omega$		1.0	4.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS96F172M/DS96F174M and across the 0°C to +70°C range for the DS96F172C/DS96F174C. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA-422A and EIA-485 standards, VOC, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: Only one output at a time should be shorted.

Note 7: For more information see Application Bulletin, contact Product Marketing.

Order Number:

DS96F172CJ
DS96F172CN
DS96F172MJ
DS96F174CJ
DS96F174MJ
NS Package Number J16A or N16A

MIL-STD-883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Maximum Package Power Dissipation* at 25°C	
Ceramic LCC (E)	2000 mW
Ceramic DIP (J)	1800 mW
Ceramic Flatpak (W)	1000 mW
Supply Voltage	7.0V
Enable Input Voltage	5.5V

*Above T_A = 25°C, derate "E" package 13.4, "J" package 12.5, "W" package 7.1 mW/°C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F172M/DS96F174M	4.50	5.0	5.50	V
Common Mode Output Voltage (V_{OC})	−7.0		+12.0	V
Output Current HIGH (I_{OH})			−60	mA
Output Current LOW (I_{OL})			60	mA
Operating Temperature (T_A) DS96F172M/DS96F174M	−55		+125	

Electrical Characteristics

Over recommended supply voltage and operating temperature range unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{IH}	Input Voltage HIGH			2.0		V
V_{IL}	Input Voltage LOW		T_A = 25°C		0.8	V
			T_A = −55°C, or +125°C		0.7	
V_{IC}	Input Clamp Voltage	I_I = −18 mA			−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA			6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 54Ω, V_{CC} = 4.5V *Figure 1*	T_A = −55°C	1.2		V
			T_A = 25°C, or +125°C	1.5		
		R_L = 100Ω, V_{CC} = 4.5V, *Figure 1*		2.0		
$\Delta\|V_{OD}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω or 100Ω, V_{CC} = 4.5V, *Figure 1*	T_A = 25°C, or +125°C		±0.2	V
			−55°C		±0.4	V
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*			3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)	R_L = 54Ω or 100Ω, V_{CC} = 4.5V, *Figure 1*			±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V			±50	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±50	μA
I_{IH}	Input Current HIGH	V_I = 2.4V			20	μA
I_{IL}	Input Current LOW	V_I = 0.4V			−50	μA
I_{OS}	Short Circuit Output Current (Note 6)	V_O = −7.0V			−250	mA
		V_O = 0V			−150	
		V_O = V_{CC}			150	
		V_O = +12V			250	
I_{CC}	Supply Current (All Drivers)	No Load	Outputs Enabled		50	mA
I_{CCX}			Outputs Disabled		30	

MIL-STD-883C

Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25°C		T_A = 55°C	T_A = 125°C	Units
			Typ	Max	Max	Max	
t_{DD}	Differential Output Delay Time	R_L = 60Ω, C_L = 15 pF, *Figure 2*	15	22	30	30	ns
t_{TD}	Differential Output Transition Time		15	22	40	40	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, C_L = 15 pF, *Figure 3*	12	16	25	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		12	16	25	25	ns
t_{ZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 4*	25	32	40	40	ns
t_{ZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 5*	25	35	100	100	ns
t_{HZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 4*, Note 13	25	30	80	80	ns
t_{LZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 5*	20	25	40	40	ns
t_{LZL}	Output Disable Time from Low Level with Load Resistor to GND (Note 12)	*Figure 5*	300				ns
t_{SKEW}	Driver Output to Output	R_L = 60Ω	1.0	4.0	10	10	ns

SMD Numbers:

DS96F172MJ/883 5962-9076501MEA
DS96F172ME/883 5962-9076501M2A

DS96F174MJ/883 5962-9076502MEA
DS96F174MW/883 5962-9076502MFA
DS96F174ME/883 5962-9076502M2A

Order Number:

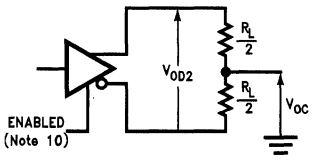
DS96F172MJ/883, DS96F174MJ/883
NS Package Number J16A

DS96F172ME/883, DS96F174ME/883
NS Package Number E20A

DS96F172MW-MIL, DS96F174MW/883
NS Package Number W16A

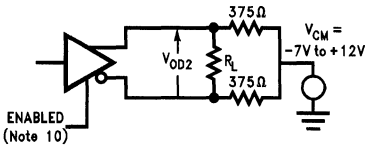
For Complete Military 883 Specifications, see RETS Data Sheet.

Parameter Measurement Information



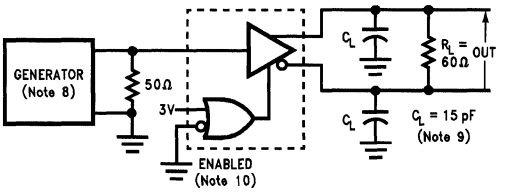
TL/F/9625-3

FIGURE 1. Differential and Common Mode Output Voltage

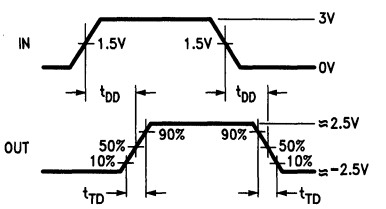


TL/F/9625-13

FIGURE 1a. Differential Output Voltage with Varying Common Mode Voltage

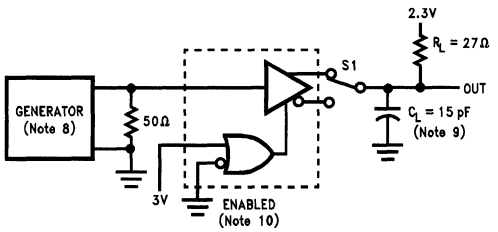


TL/F/9625-4

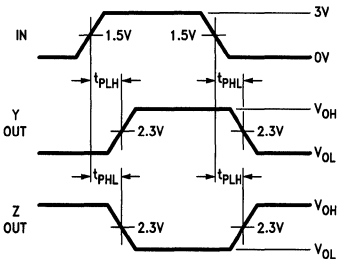


TL/F/9625-5

FIGURE 2. Differential Output Delay and Transition Times

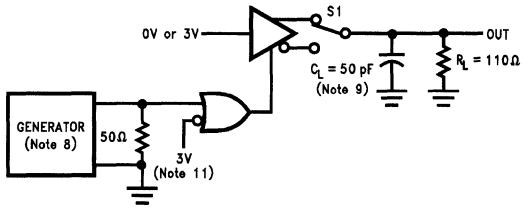


TL/F/9625-6



TL/F/9625-7

FIGURE 3. Propagation Delay Times



TL/F/9625-8

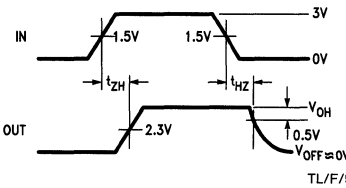


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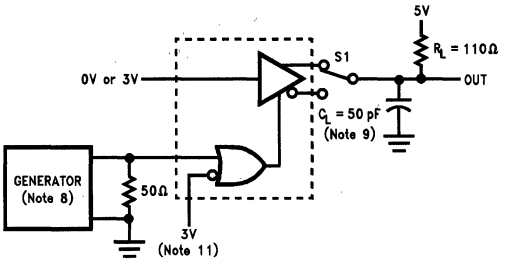
FIGURE 4. t_{ZH} and t_{HZ}

Parameter Measurement Information (Continued)



TL/F/9625–10

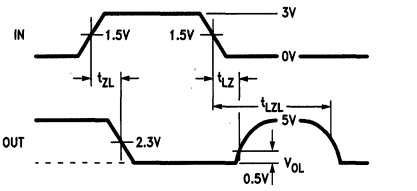


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FIGURE 5. t_{ZL}, t_{LZ}, t_{LZL}

Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, duty cycle = 50%, $t_r \leq 5.0$ ns, $t_f \leq 5.0$ ns, $Z_O = 50\Omega$.

Note 9: C_L includes probe and jig capacitance.

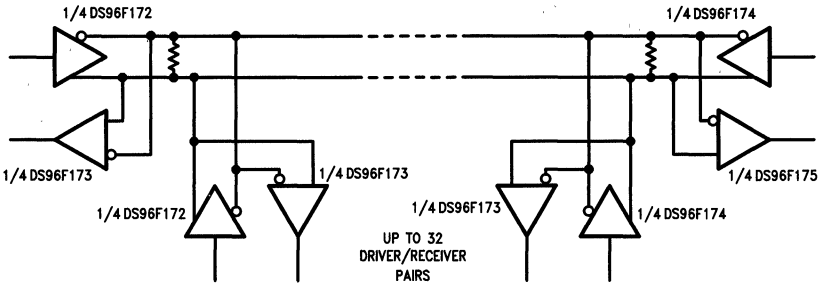
Note 10: DS96F172 with active high and active low Enables is shown. DS96F174 has active high Enable only.

Note 11: To test the active low Enable $\overline{E}$ of DS96F172 ground E and apply an inverted waveform to $\overline{E}$. DS96F174 has active high Enable only.

Note 12: For more information see Application Bulletin, Contact Product Marketing.

Note 13: Not tested for DS96F172MW-MIL device.

Typical Application



TL/F/9625–12

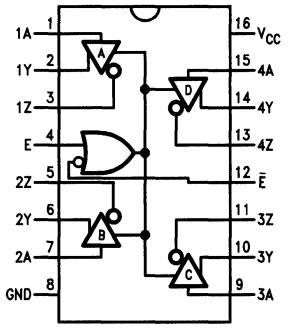
Note:

The line length should be terminated at both ends in its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

Connection Diagrams

16-Lead Ceramic Dual-In-Line Package
NS Package Number J16A

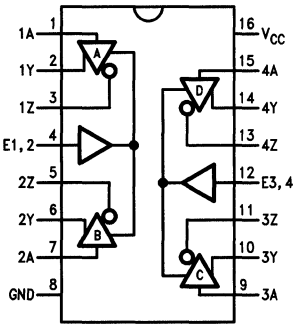
DS96F172



TL/F/9625–1

Top View

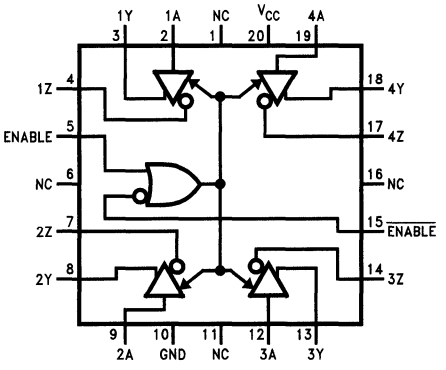
DS96F174



TL/F/9625–2

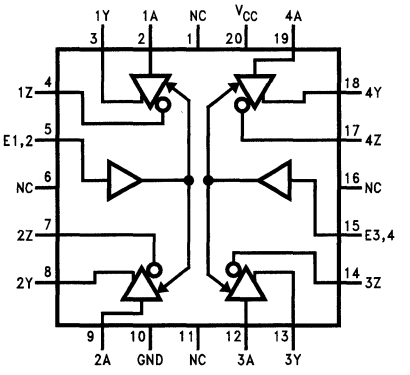
Top View

20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



TL/F/9625–18

Top View

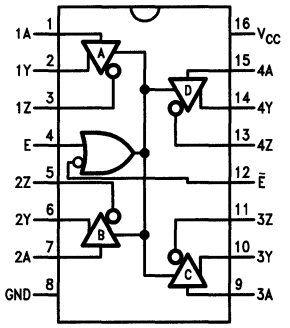


TL/F/9625–19

Top View

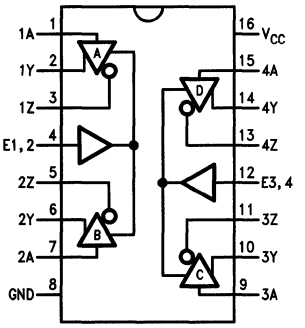
NC = No connection

16-Lead Ceramic Flatpak
NS Package Number W16A



TL/F/9625–1

Top View



TL/F/9625–2

Top View

Order Numbers are located at the end of the respective Electrical Tables.

National Semiconductor

DS96173/DS96175
RS-485/RS-422 Quad Differential Line Receivers

General Description

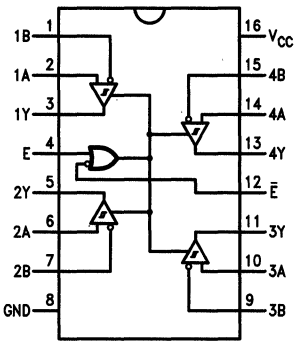
The DS96173 and DS96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96173 features an active high and active low Enable, common to all four receivers. The DS96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96172, DS96174, DS96176 and DS96177.

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE Outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5V supply
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- DS96173/DS96175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively

Connection Diagrams

16-Lead DIP
DS96173



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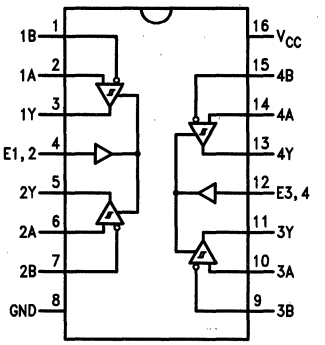
16-Lead DIP
DS96175



TL/F/9628–2

Order Number DS96173CJ, DS96173CN, DS96175CJ or DS96175CN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
J-Cavity Package	1.63W
N-Molded Package	1.84W
Supply Voltage	7V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7V
Low Level Output Current	50 mA

*Derate cavity package 13 mW/°C above 25°C; derate molded DIP package 15 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5	5.25	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})	−7		+12	V
Output Current High (I_{OH})			−400	μA
Output Current LOW (I_{OL})			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 & 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = − 0.4 mA				0.2	V
V_{TL}	Differential Input (Note 4) Low Threshold Voltage	V_O = 0.5V, I_O = 16 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 5)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA		2.7			V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.4V to 2.4V				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	Outputs Disabled				75	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96173/DS96175. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 6: Refer to EIA Standards RS-485 for exact conditions.

Note 7: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to 2.5V, C_L = 15 pF, *Figure 1*		15	25	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output			15	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*		15	22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*		15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, *Figure 2*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, *Figure 3*		24	40	ns

Function Tables

(Each Receiver) DS96173

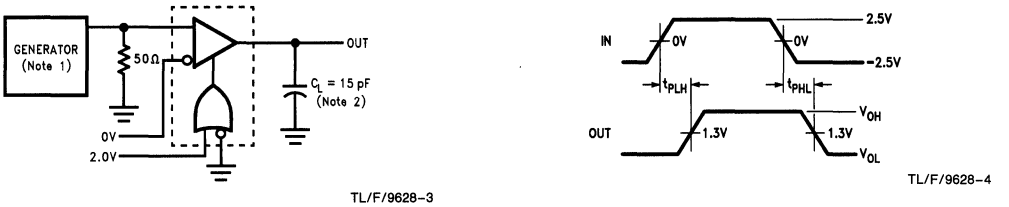
Differential Inputs	Enables		Outputs
A–B	E	$\overline{E}$	V
V_{ID} > 0.2V	H	X	H
	X	L	H
V_{ID} < −0.2V	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

(Each Receiver) DS96175

Differential Inputs A–B	Enable	Output Y
$V_{ID} \geq$ 0.2V	H	H
$V_{ID} \leq$ −0.2V	H	L
X	L	Z

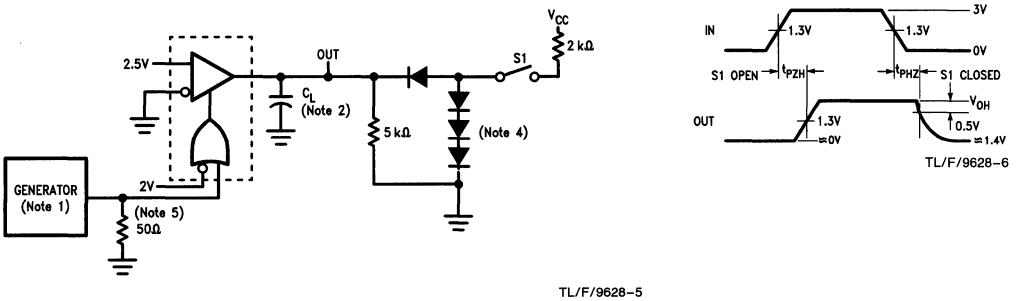
Parameter Measurement Information



TL/F/9628–3

TL/F/9628–4

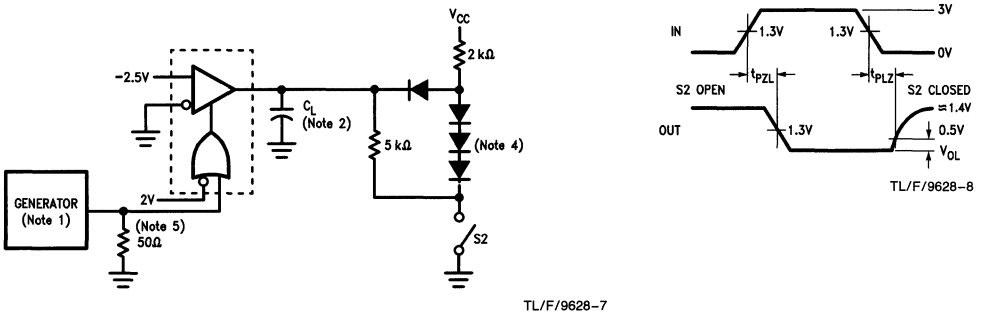
FIGURE 1. t_{PLH}, t_{PHL} (Note 3)



TL/F/9628–5

TL/F/9628–6

FIGURE 2. t_{PHZ}, t_{PZH} (Note 3)



TL/F/9628–7

TL/F/9628–8

FIGURE 3. t_{PZL}, t_{PLZ} (Note 3)

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

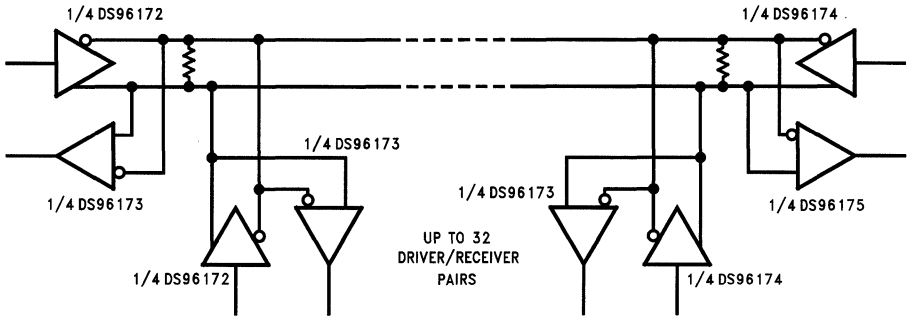
Note 2: C_L includes probe and stray capacitance.

Note 3: DS96173 with active high and active low Enables is shown here. DS96175 has active high Enable only.

Note 4: All diodes are 1N916 or equivalent.

Note 5: To test the active low Enable $\overline{E}$ of DS96173, ground E and apply an inverted input waveform to $\overline{E}$. DS96175 has active high Enable only.

Typical Application



TL/F/9628–9

FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96F173C/DS96F173M/DS96F175C/DS96F175M EIA-485/EIA-422 Quad Differential Receivers

General Description

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

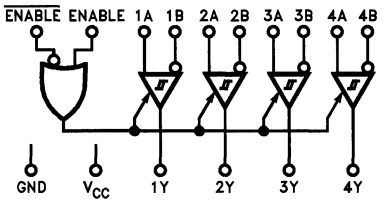
The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Features

- Meets EIA-485, EIA-422A, EIA-423A standards
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Reduced power consumption (I_{CC} = 50 mA max)
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Military temperature range available
- Qualified for MIL STD 883C
- Available to standard military drawings (SMD)
- Available in DIP(J), LCC(E), and FlatPak (W) packages
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

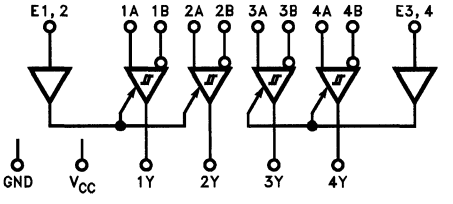
Logic Diagrams

DS96F173



TL/F/9627–10

DS96F175



TL/F/9627–11

Function Tables

(Each Receiver) DS96F173

Differential Inputs A–B	Enable E	Enable $\overline{E}$	Output Y
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

(Each Receiver) DS96F175

Differential Inputs A–B	Enable E	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

COMMERCIAL

Absolute Maximum Ratings (Note 1)

Specifications for the 883 version of this product are listed separately.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Max. Package Power Dissipation* at 25°C Ceramic DIP (J)	1500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

*Derate package 10 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})				
DS96F173C/DS96F175C	4.75	5.0	5.25	V
DS96F173M/DS96F175M	4.50	5.0	5.50	
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	μA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A)				
DS96F173C/DS96F175C	0	25	70	°C
DS96F173M/DS96F175M	−55	25	125	

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	$V_O = V_{OH}$				0.2	V
V_{TL}	Differential-Input (Note 4) Low Threshold Voltage	$V_O = V_{OL}$		−0.2			V
$V_{TH} - V_{TL}$	Hysteresis (Note 5)	$V_{CM} = 0V$			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	Output Voltage HIGH	$V_{ID} = 200$ mV	0°C to +70°C	2.8			V
		$I_{OH} = -400$ μA	−55°C to +125°C	2.5			
V_{OL}	Output Voltage LOW	$V_{ID} = -200$ mV	$I_{OL} = 8.0$ mA			0.45	V
			$I_{OL} = 11$ mA			0.50	
I_{OZ}	High-Impedance State Output	$V_O = 0.4V$ to 2.4V				±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	$V_I = 12V$			1.0	mA
			$V_I = -7.0V$			−0.8	
I_{IH}	Enable Input Current HIGH	$V_{IH} = 2.7V$				20	μA
I_{IL}	Enable Input Current LOW	$V_{IL} = 0.4V$				−100	μA
R_I	Input Resistance			14	18	22	kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15		−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled			50	mA
I_{CCX}			Outputs Disabled			50	

COMMERCIAL

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, *Figure 1* V_{CM} = 0V	5.0	15	22	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		5.0	15	22	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*		12	16	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*		13	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2*		14	20	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*		14	18	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 1*		1.0	3.0	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS96F173M/DS96F175M and across the 0°C to +70°C range for the DS96F173C/DS96F175C. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 4: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 5: Hysteresis is the difference between the positive-going input threshold voltage. V_{TH}, and the negative going input threshold voltage, V_{TL}.

Note 6: Refer to EIA-485 Standard for exact conditions.

Note 7: Only one output at a time should be shorted.

Order Number:

DS96F173CJ
DS96F173MJ
DS96F175CJ
DS96F175MJ
See NS Package Number J16A

MIL-STD-883C

Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the current Reliability Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest version of the RETS please contact your local National Semiconductor sales office or distributor.

Storage Temperature Range (T_{STG})	−65°C to +175°C
Lead Temperature (Soldering, 60 sec.)	300°C
Max. Package Power Dissipation* at 25°C	
Ceramic DIP (J)	1500 mW
Ceramic Flatpak (W)	1034 mW
Ceramic LCC (E)	1500 mW
Supply Voltage	7.0V
Input Voltage, A or B Inputs	±25V
Differential Input Voltage	±25V
Enable Input Voltage	7.0V
Low Level Output Current	50 mA

*Above T_A = 25°C derate J package 10 mW/°C, W package 6.90 mW/°C, E package 11.11 mW/°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC}) DS96F173M/DS96F175M	4.50	5.0	5.50	V
Common Mode Input Voltage (V_{CM})	−7		+12	V
Differential Input Voltage (V_{ID})			|12|	V
Output Current HIGH (I_{OH})			−400	μA
Output Current LOW (I_{OL})			11	mA
Operating Temperature (T_A) DS96F173M/DS96F175M	−55	25	125	°C

Electrical Characteristics

Over recommended supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{TH}	Differential-Input High Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V			0.2	V
V_{TL}	Differential-Input (Note 4) Low Threshold Voltage	V_{CC} = 4.5V, 5.5V V_{CM} = 0V, 12V, −12V		−0.2		V
V_{IH}	Enable Input Voltage HIGH			2.0		V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA, V_{CC} = 4.5V			−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV I_{OH} = −400 μA	−55°C to +125°C	2.5		V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV	I_{OL} = 8.0 mA		0.45	V
I_{OZ}	High-Impedance State Output	V_O = 0.4V, 2.4V, V_{CC} = 5.5V			±20	μA
I_I	Line Input Current (Note 6)	Other Input = 0V	V_I = 12V		1.0	mA
			V_I = −7.0V		−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V, V_{CC} = 5.5V			20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V, V_{CC} = 5.5V			−100	μA
R_I	Input Resistance			10		kΩ
I_{OS}	Short Circuit Output Current	(Note 7)		−15	−85	mA
I_{CC}	Supply Current	No Load	Outputs Enabled or Disabled		50	mA
I_{CCX}						

MIL-STD-883C

Switching Characteristics V_{CC} = 5.0V

Symbol	Parameter	Conditions	T_A = 25°C		T_A = −55°C	T_A = 125°C	Units
			Typ	Max	Max	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	V_{ID} = −2.5V to +2.5V, C_L = 15 pF, *Figure 1* V_{CM} = 0V	15	22	30	30	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output		15	22	30	30	ns
t_{ZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 2*	12	16	27	27	ns
t_{ZL}	Output Enable Time to Low Level	C_L = 15 pF, *Figure 3*	13	18	27	27	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 2* (Note 13)	14	20	27	27	ns
		C_L = 20 pF, *Figure 2* (Note 13)	14	30	37	37	ns
t_{LZ}	Output Disable Time from Low Level	C_L = 5.0 pF, *Figure 3*	14	18	30	30	ns
$\lvert t_{PLH} - t_{PHL} \rvert$	Pulse Width Distortion (SKEW)	*Figure 1*	1	3	5.0	5.0	ns

SMD Number:

DS96F173MJ	**5962-9076602 MEA**
DS96F173MW	**5962-9076602 MFA**
DS96F173ME	**5962-9076602 M2A**
DS96F175MJ	**5962-9076601 MEA**
DS96F175MW	**5962-9076601 MFA**
DS96F175ME	**5962-9076601 M2A**

Order Number:

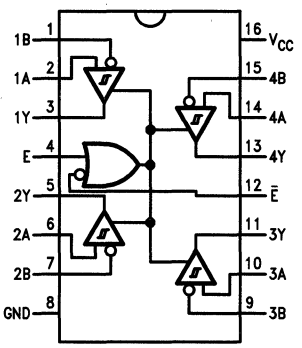
883 Marking	SMD Marking
DS96F173MJ/883	**DS96F173MJ-SMD**
DS96F175MJ/883	**DS96F175MJ-SMD**
See NS Package Number J16A	
DS96F173ME/883	**DS96F173ME-SMD**
DS96F175ME/883	**DS96F175ME-SMD**
See NS Package Number E20A	
DS96F173MW/883	**DS96F173MW-SMD**
DS96F175MW/883	**DS96F175MW-SMD**
See NS Package Number W16A	

For Complete Military 883 Specifications, see RETS Data Sheet.

Connection Diagrams

16-Lead Ceramic Dual-In-Line Package
NS Package Number J16A

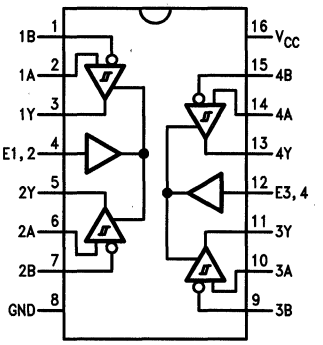
DS96F173



TL/F/9627–1

Top View

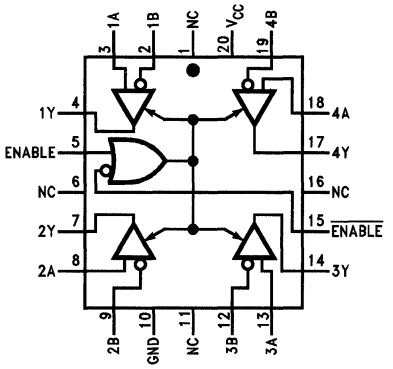
DS96F175



TL/F/9627–2

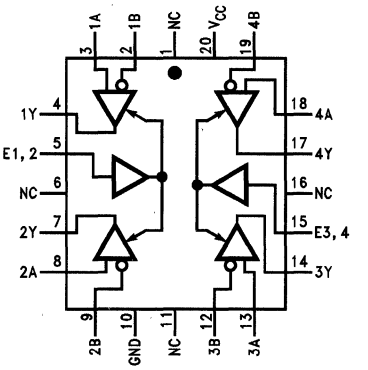
Top View

20-Lead Ceramic Leadless Chip Carrier
NS Package Number E20A



TL/F/9627–12

Top View

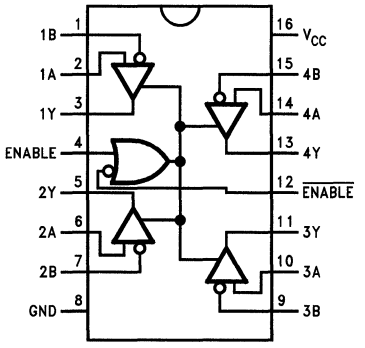


TL/F/9627–13

Top View

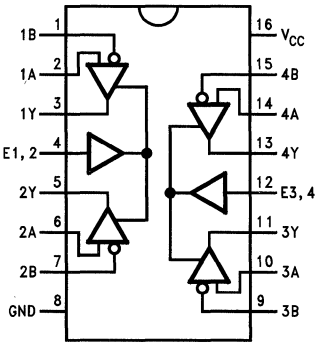
*NC—No Connection

16-Lead Ceramic FlatPak
NS Package Number W16A



TL/F/9627–14

Top View

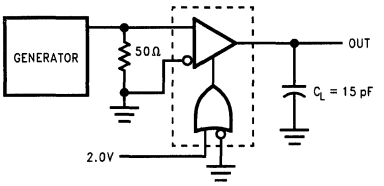


TL/F/9627–15

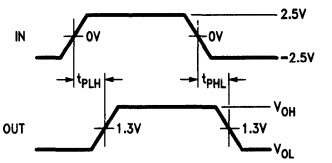
Top View

Order Numbers are located at the end of the respective Electrical Tables.

Parameter Measurement Information

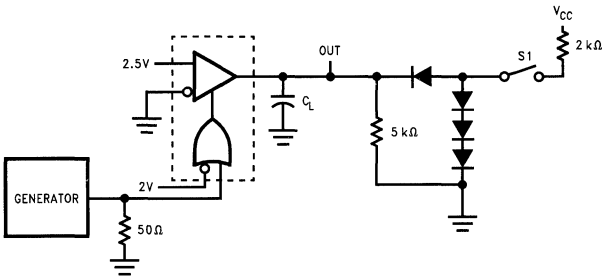


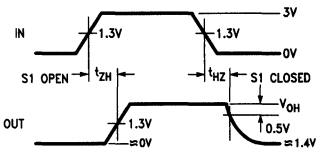
TL/F/9627-3



TL/F/9627-4

FIGURE 1. t_{PLH}, t_{PHL} (Notes 8, 9)

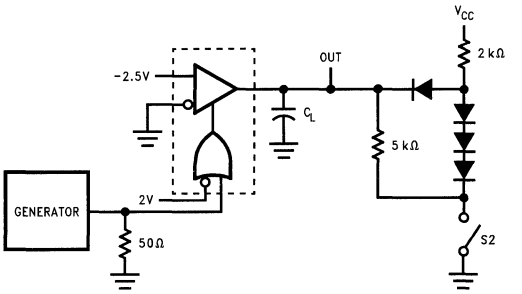


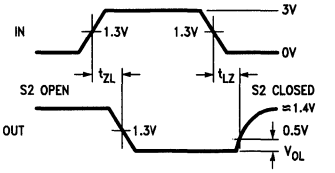


TL/F/9627-5

TL/F/9627-6

FIGURE 2. t_{HZ}, t_{ZH} (Notes 8, 9, 11 and 12)





TL/F/9627-7

TL/F/9627-8

FIGURE 3. t_{ZL}, t_{LZ} (Notes 8, 9, 11 and 12)

Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 9: C_L includes probe and stray capacitance.

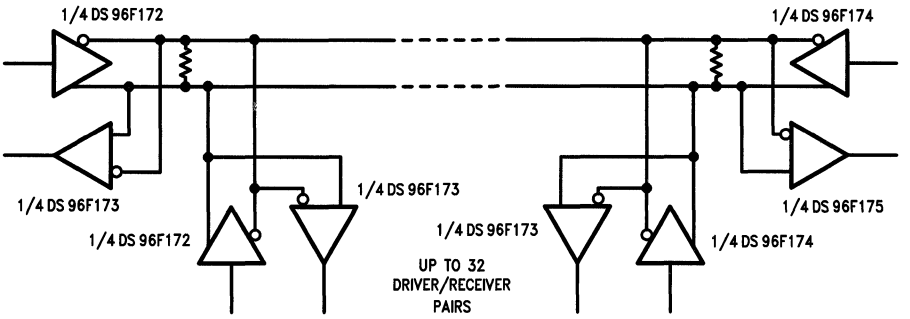
Note 10: DS96F173 with active high and active low Enables are shown. DS96F175 has active high Enable only.

Note 11: All diodes are 1N916 or equivalent.

Note 12: To test the active low Enable $\overline{E}$ of DS96F173, ground E and apply an inverted input waveform to $\overline{E}$. DS96F175 has active high enable only.

Note 13: Testing at 20 pF assures conformance to 5 pF specification.

Typical Application



TL/F/9627–9

FIGURE 4

Note: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

National Semiconductor

DS96176
RS-485/RS-422 Differential Bus Transceiver

General Description

The DS96176 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

The DS96176 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at junction temperature of approximately 160°C. The receiver features a typical input impedance of 15 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

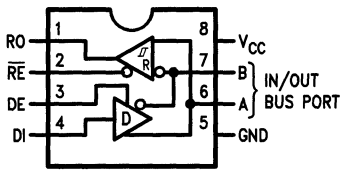
The DS96176 can be used in transmission line applications employing the DS96172 and the DS96174 quad differential line drivers and the DS96173 and DS96175 quad differential line receivers.

Features

- Bidirectional transceiver
- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission
- TRI-STATE driver and receiver enables
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- Driver output capability ±60 mA Maximum
- Thermal shutdown protection
- Driver positive and Negative current-limiting
- High impedance receiver input
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead DIP



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Top View

Order Number DS96176CJ or DS96176CN
See NS Package Number J08E or N08E

Function Table

Driver

Input	Enable	Outputs	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A-B	$\overline{RE}$	R
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Lead Temperature	
Ceramic DIP (soldering, 60 sec.)	300°C
Molded DIP (soldering, 10 sec.)	265°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1300 mW
Molded Package	930 mW
Supply Voltage	7.0V
Differential Input Voltage	+15V/−10V
Enable Input Voltage	5.5V

*Derate cavity package 8.7 mW/°C above 25°C; derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at Any Bus Terminal (Separately or Common Mode)	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{OH}	Output Voltage HIGH	I_{OH} = −20 mA			3.1		V
V_{OL}	Output Voltage LOW	I_{OL} = 20 mA			0.85		V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1* and *2*		1.5	2.0		
$\Delta\|V_{OD2}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 54Ω V_{CM} = 0V *Figure 1* and *2*				±0.2	V
		R_L = 100Ω *Figure 1*					
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω, *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current (Note 4) (Includes Receiver I_I)	Output Disabled	V_O = 12V			1.0	mA
			V_O = −7.0V			−0.8	
I_{IH}	Input Current HIGH	V_I = 2.4V				20	μA
I_{IL}	Input Current LOW	V_I = 0.4V				−100	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA		−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V			50		mV
V_{IH}	Enable Input Voltage HIGH			2.0			V
V_{IL}	Enable Input Voltage LOW					0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA				−1.5	V
V_{OH}	Output Voltage HIGH	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 3*		2.7			V
V_{OL}	Output Voltage LOW	V_{ID} = −200 mV, *Figure 3*	I_{OL} = 8,0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High Impedance State Output	V_O = 0.45V to 2.4V				±20	μA
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			40	mA
			Outputs Disabled				

Driver Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 6*		25	35	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 7*		25	35	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 7*		29	35	ns

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS96176. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: The algebraic convention, where the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage V_{T+}, and the negative-going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standard RS-485 for exact conditions.

Note 9: Only one output at a time should be shorted.

Parameter Measurement Information

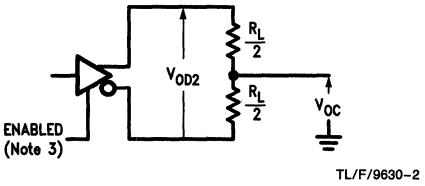

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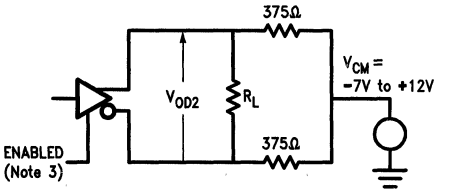
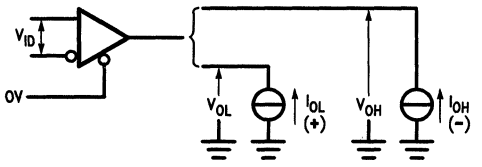
FIGURE 1. Driver V_{OD} and V_{OC}



TL/F/9630–3

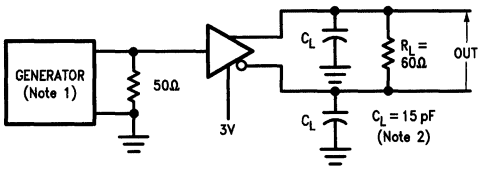
FIGURE 2. Driver V_{OD} with Varying Common Mode Voltage



TL/F/9630–4

FIGURE 3. Receiver V_{OH} and V_{OL}

Parameter Measurement Information (Continued)



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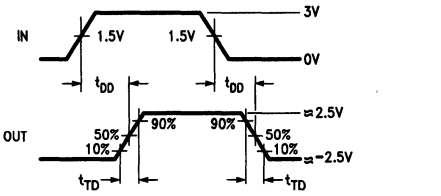
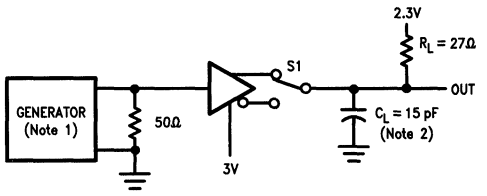


TL/F/9630–6

FIGURE 4. Driver Differential Output Delay and Transition Times



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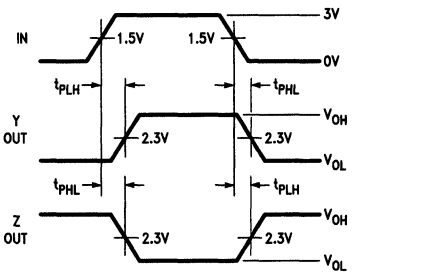

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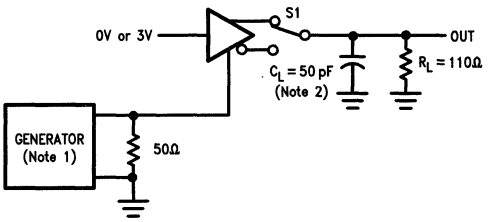
FIGURE 5. Driver Propagation Times



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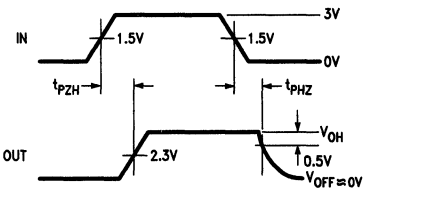

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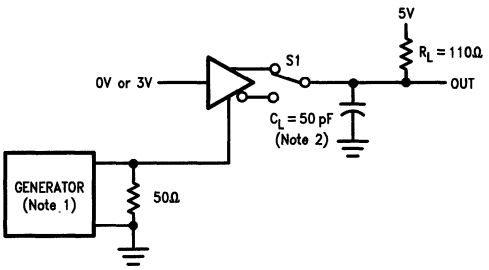
FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})



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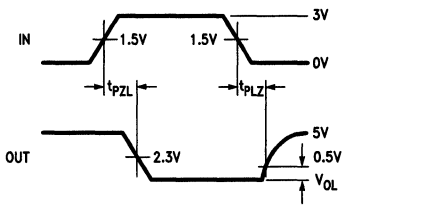

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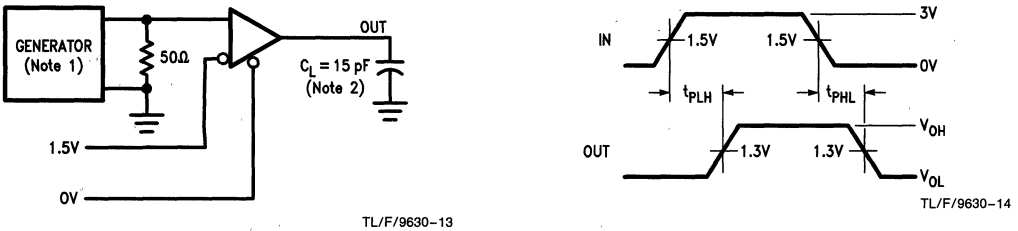
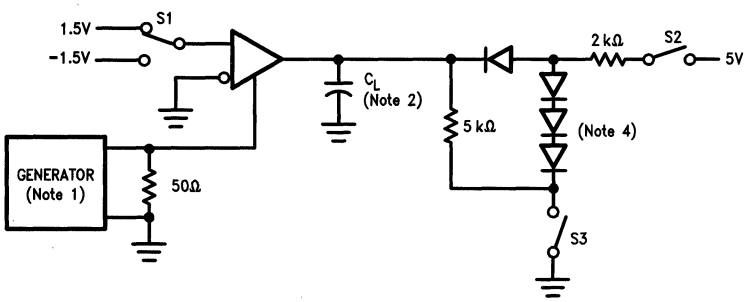
FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)



TL/F/9630–13 TL/F/9630–14

FIGURE 8. Receiver Propagation Delay Times



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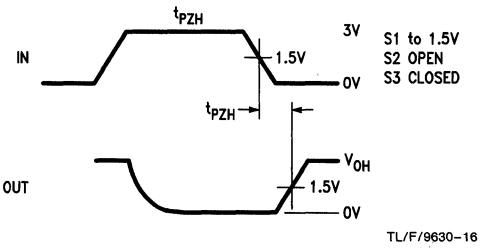

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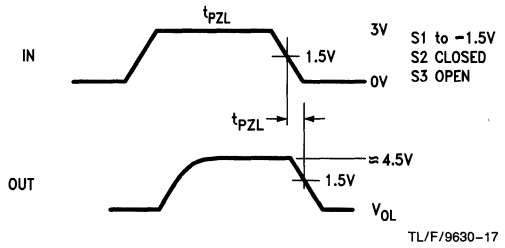

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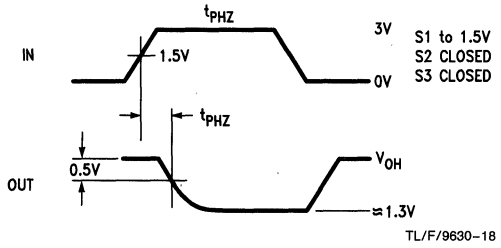

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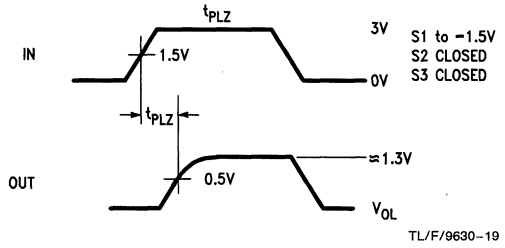

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FIGURE 9. Receiver Enable and Disable Times

Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, 50% duty cycle, $t_r \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96176 Driver enable is Active-High.

Note 4: All diodes are 1N916 or equivalent.

Typical Application

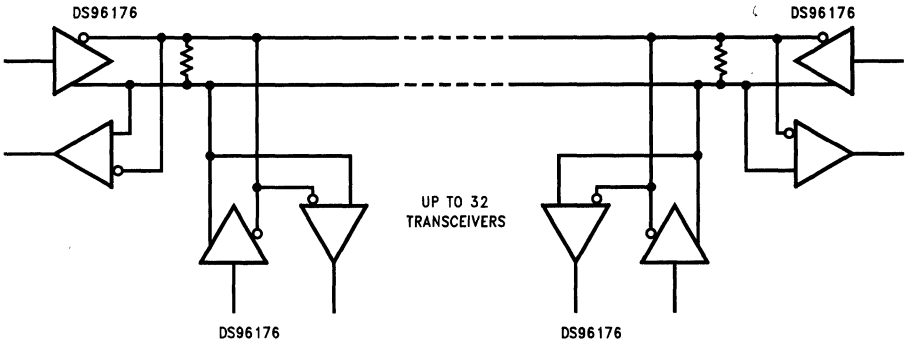

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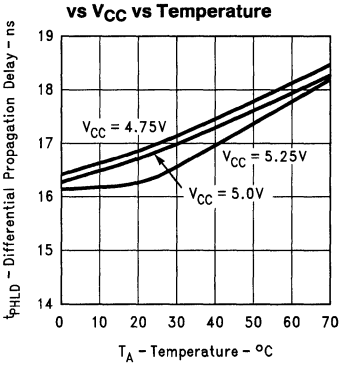
FIGURE 10

Note:

The line length should be terminated at both ends of its characteristic impedance.
Stub lengths off the main line should be kept as short as possible.

Typical Performance Characteristics

Driver Differential Propagation Delay vs V_{CC} vs Temperature



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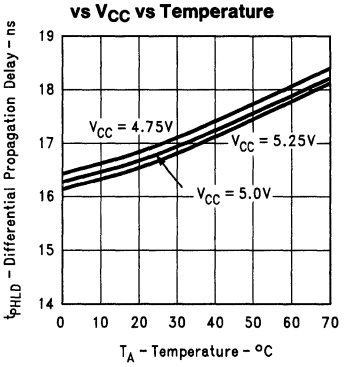
Driver Differential Propagation Delay vs V_{CC} vs Temperature



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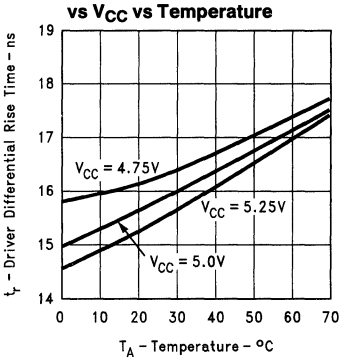
Driver Differential Rise Time vs V_{CC} vs Temperature



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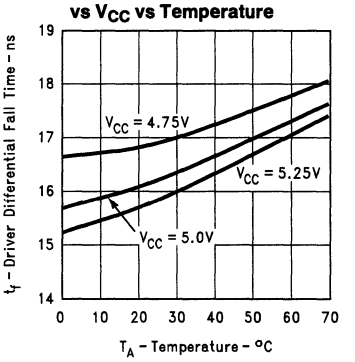
Driver Differential Fall Time vs V_{CC} vs Temperature



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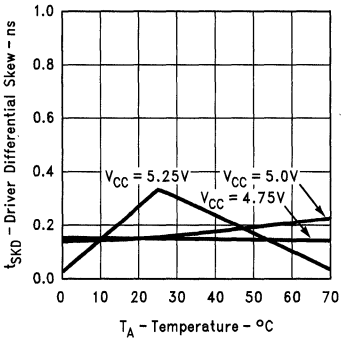
Typical Performance Characteristics (Continued)

Driver Skew vs V_{CC} vs Temperature
($|t_{PLDH}-t_{PHLD}|$)



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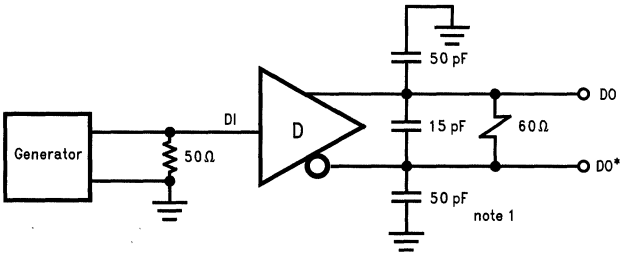

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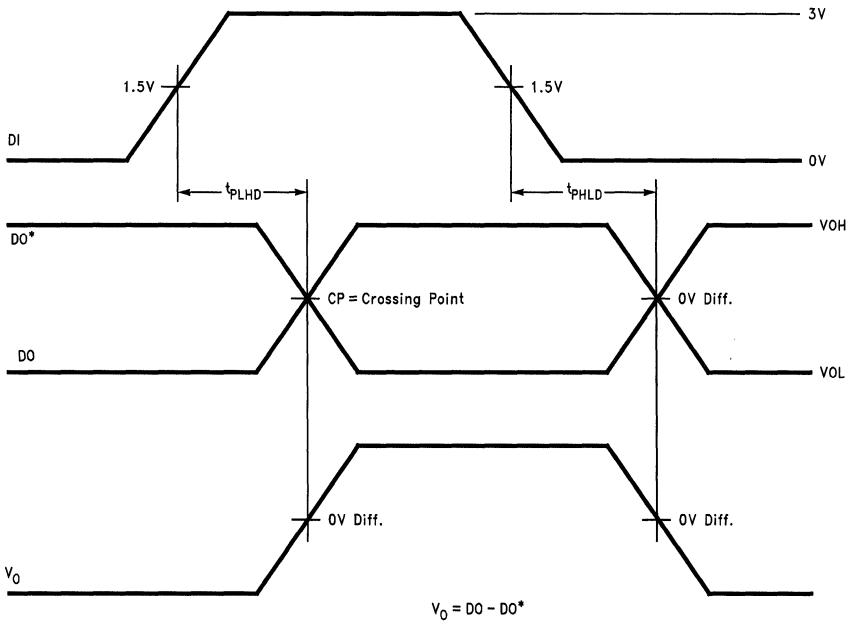
FIGURE 11. Typical Curve Driver Propagation Delay Test Circuit



TL/F/9630–28

FIGURE 12. Typical Curve Driver Differential Propagation Delay Timing

Typical Performance Curves

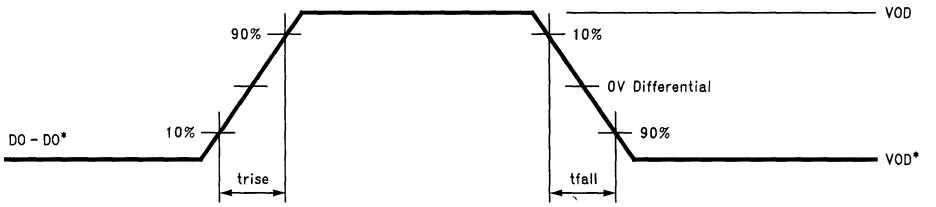


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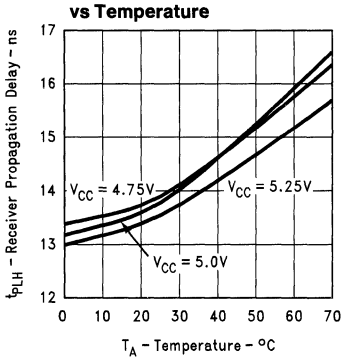
FIGURE 13. Typical Curve Driver Differential Rise and Fall Times

Receiver Propagation Delay vs V_{CC} vs Temperature



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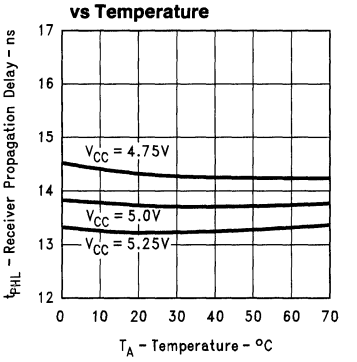
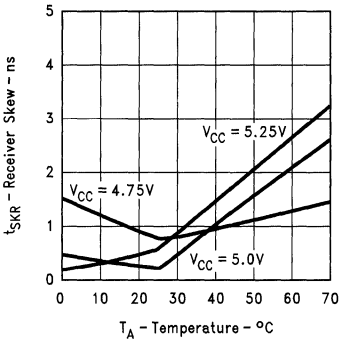
Receiver Propagation Delay vs V_{CC} vs Temperature



TL/F/9630–31

Receiver Skew vs V_{CC} vs Temperature ($|t_{PLH}-t_{PHL}|$)



TL/F/9630–32

Typical Performance Curves (Continued)

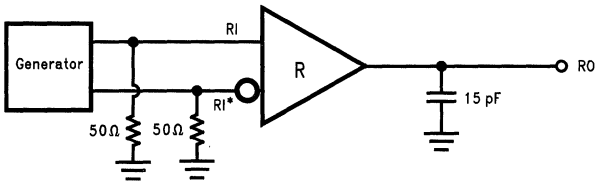


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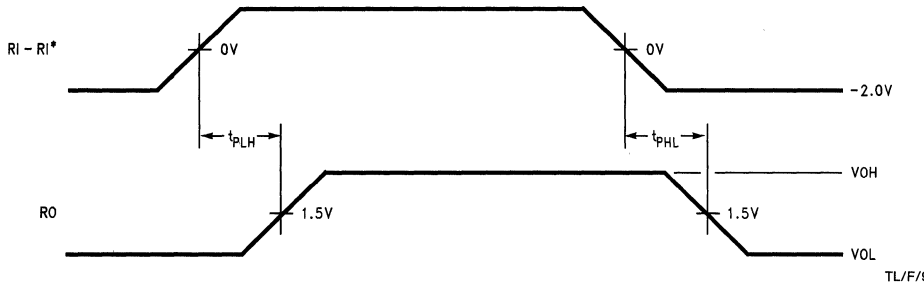
FIGURE 14. Typical Curve Receiver Differential Propagation Delay Test Circuit



TL/F/9630–34

FIGURE 15. Typical Curve Receiver Propagation Delay Timing

National Semiconductor

DS96177
RS-485/RS-422 Differential Bus Repeater

General Description

The DS96177 Differential Bus Repeater is a monolithic integrated device designed for one-way data communication on multipoint bus transmission lines. This device is designed for balanced transmission bus line applications and meets EIA Standard RS-485 and RS-422A. The device is designed to improve the performance of the data communication over long bus lines. The DS96177 has an active high Enable.

The DS96177 features positive and negative current limiting and TRI-STATE® outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

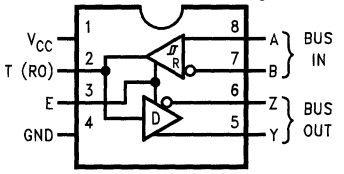
The DS96177 is designed for optimum performance when used on transmission buses employing the DS96172 and DS96174 differential line drivers, DS96173 and DS96175 differential line receivers, or DS96176 differential bus transceivers.

Features

- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission on long bus lines in noisy environments
- TRI-STATE outputs
- Bus voltage range −7.0V to +12V
- Positive and negative current limiting
- Driver output capability ±60 mA max
- Driver thermal shutdown protection
- Receiver input high impedance
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead Dual-In-Line Package



TL/F/9644–1

Top View

Order Number DS96177CN
See NS Package Number N08E

Function Table

Differential Inputs	Enable	Outputs		
A–B	E	T	Y	Z
$V_{ID} \geq 0.2V$	H	H	H	L
$V_{ID} \leq -0.2V$	H	L	L	H
X	L	Z	Z	Z

Note: T is an output pin only, monitoring the BUS (RO).

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Molded Package: 930 mW

Supply Voltage: 7.0V

Input Voltage: 5.5V

*Derate molded DIP package 7.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Voltage at any Bus Terminal (Separately or Common Mode) (V_I or V_{CM})	−7.0		12	V
Differential Input Voltage (V_{ID})			±12	V
Output Current HIGH (I_{OH})				
Driver			−60	mA
Receiver			−400	μA
Output Current LOW (I_{OL})				
Driver			60	mA
Receiver			16	mA
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified (Notes 2 and 3)

DRIVER SECTION

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage	I_I = −18 mA				−1.5	V
$\|V_{OD1}\|$	Differential Output Voltage	I_O = 0 mA				6.0	V
$\|V_{OD2}\|$	Differential Output Voltage	R_L = 100Ω, *Figure 1*		2.0	2.25		V
		R_L = 54Ω, *Figure 1* and *2*		1.5	2.0		
$\Delta\|V_{OD2}\|$	Change in Magnitude of Differential Output Voltage (Note 4)	R_L = 100Ω, *Figure 1*				±0.2	V
		R_L = 54Ω *Figure 1* and *2*	V_{CM} = 0V				
V_{OC}	Common Mode Output Voltage (Note 5)	R_L = 54Ω or 100Ω *Figure 1*				3.0	V
$\Delta\|V_{OC}\|$	Change in Magnitude of Common Mode Output Voltage (Note 4)					±0.2	V
I_O	Output Current with Power Off	V_{CC} = 0V, V_O = −7.0V to +12V				±100	μA
I_{OZ}	High Impedance State Output Current	V_O = −7.0V to +12V			±50	±200	μA
I_{IH}	Input Current HIGH	V_I = 2.7V				20	μA
I_{IL}	Input Current LOW	V_I = 0.5V				−100	μA
I_{OS}	Short Circuit Output Current (Note 9)	V_O = −7.0V				−250	mA
		V_O = 0V				−150	
		V_O = V_{CC}				150	
		V_O = 12V				250	
I_{CC}	Supply Current	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

RECEIVER SECTION

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold Voltage	V_O = 2.7V, I_O = −0.4 mA			0.2	V
V_{TL}	Differential Input Low Threshold Voltage (Note 6)	V_O = 0.5V, I_O = 8.0 mA	−0.2			V
$V_{T+} - V_{T-}$	Hysteresis (Note 7)	V_{CM} = 0V		50		mV
V_{IH}	Enable Input Voltage HIGH		2.0			V
V_{IL}	Enable Input Voltage LOW				0.8	V
V_{IC}	Enable Input Clamp Voltage	I_I = −18 mA			−1.5	V

Electrical Characteristics (Continued)

Over recommended temperature, common mode input voltage, and supply voltage ranges, unless otherwise specified

RECEIVER SECTION (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, *Figure 3*		2.7			V
V_{OL}	Low Level Output Voltage	V_{ID} = −200 mV, *Figure 3*	I_{OL} = 8.0 mA			0.45	V
			I_{OL} = 16 mA			0.50	
I_{OZ}	High-Impedance State Output	V_O = 0.4V				−360	μA
		V_O = 2.4V				20	
I_I	Line Input Current (Note 8)	Other Input = 0V	V_I = 12V			1.0	mA
			V_I = −7.0V			−0.8	
I_{IH}	Enable Input Current HIGH	V_{IH} = 2.7V				20	μA
I_{IL}	Enable Input Current LOW	V_{IL} = 0.4V				−100	μA
R_I	Input Resistance				12		kΩ
I_{OS}	Short Circuit Output Current	(Note 9)		−15		−85	mA
I_{CC}	Supply Current (Total Package)	No Load	Outputs Enabled			35	mA
			Outputs Disabled			40	

Drive Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DD}	Differential Output Delay Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{TD}	Differential Output Transition Time	R_L = 60Ω, *Figure 4*		15	25	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 27Ω, *Figure 5*		12	20	ns
t_{PZH}	Output Enable Time to High Level	R_L = 110Ω, *Figure 6*		25	45	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 110Ω, *Figure 7*		25	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 110Ω, *Figure 6*		20	25	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 110Ω, *Figure 7*		29	35	ns

Receiver Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{ID} = 0V to 3.0V, C_L = 15 pF, *Figure 8*		16	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			16	25	ns
t_{PZH}	Output Enable Time to High Level	C_L = 15 pF, *Figure 9*		15	22	ns
t_{PZL}	Output Enable Time to Low Level			15	22	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5.0 pF, *Figure 9*		14	30	ns
t_{PLZ}	Output Disable Time from Low Level			24	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the 0°C to +70°C range for the DS96177. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into the device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD}, V_{OC} respectively, that occur when the input is changed from a high level to a low level.

Note 5: In EIA Standards RS-422A and RS-485, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

Note 6: The algebraic convention, when the less positive (more negative) limit is designated minimum, is used in this data sheet for common mode input voltage and threshold voltage levels only.

Note 7: Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 8: Refer to EIA Standards RS-485 for exact conditions.

Note 9: Only one output at a time should be shorted.

Parameter Measurement Information

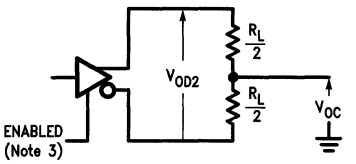


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FIGURE 1. Driver V_{OD2} and V_{OC}

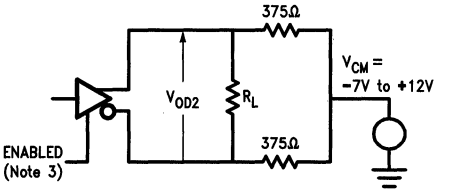

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FIGURE 2. Driver V_{OD2} with Varying Common Mode Voltage

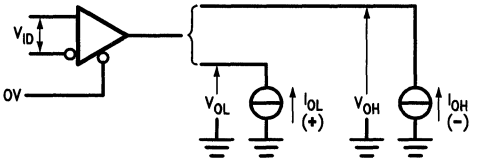

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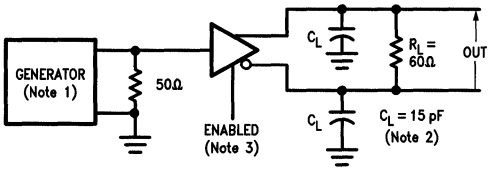
FIGURE 3. Receiver V_{OH} and V_{OL}



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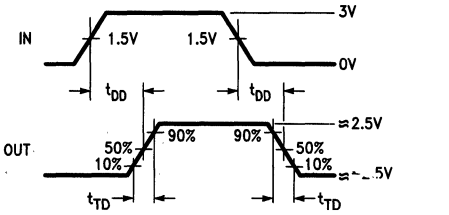

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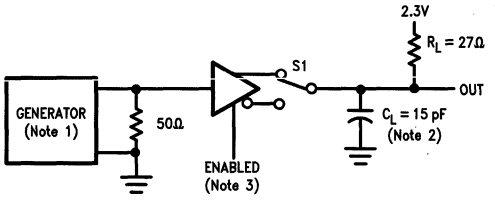
FIGURE 4. Driver Differential Output Delay and Transition Times



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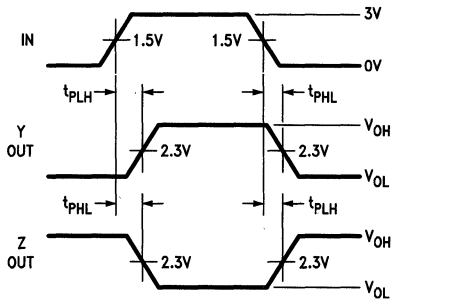

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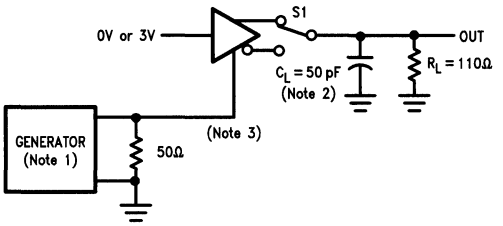
FIGURE 5. Drive Propagation Times

Parameter Measurement Information (Continued)



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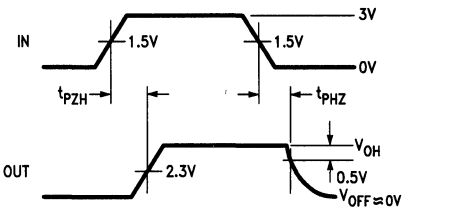

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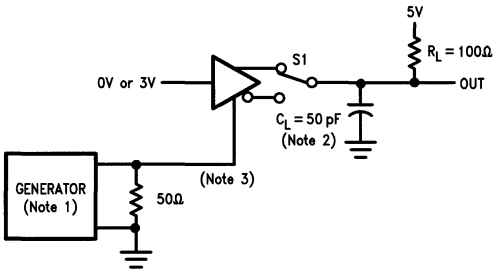
FIGURE 6. Driver Enable and Disable Times (t_{PZH}, t_{PHZ})



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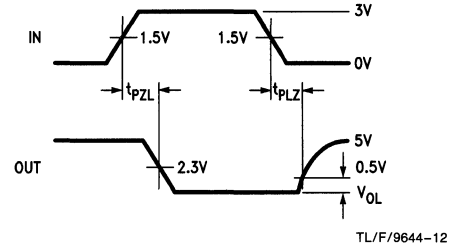

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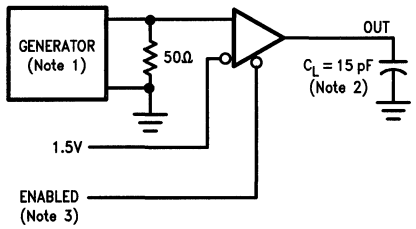
FIGURE 7. Driver Enable and Disable Times (t_{PZL}, t_{PLZ})



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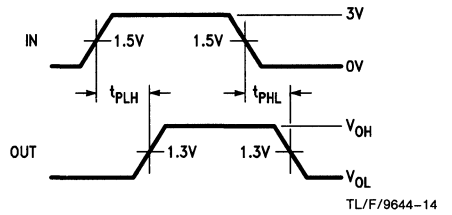

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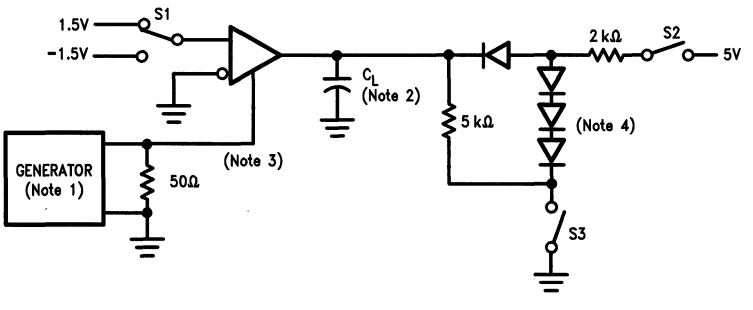
FIGURE 8. Receiver Propagation Delay Times

Parameter Measurement Information (Continued)



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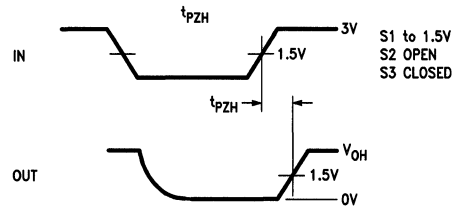

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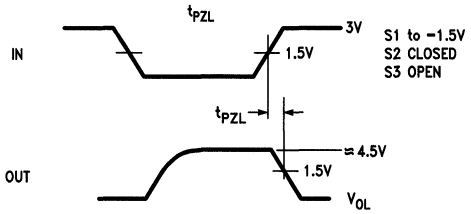

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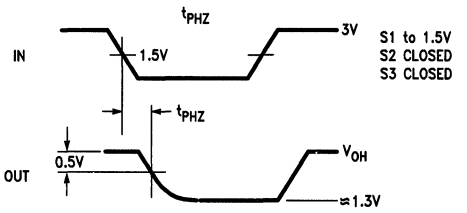

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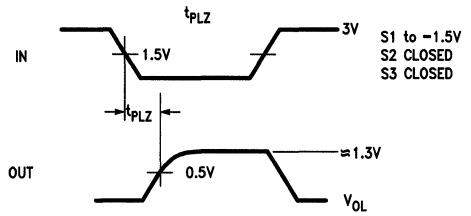

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FIGURE 9. Receiver Enable and Disable Times

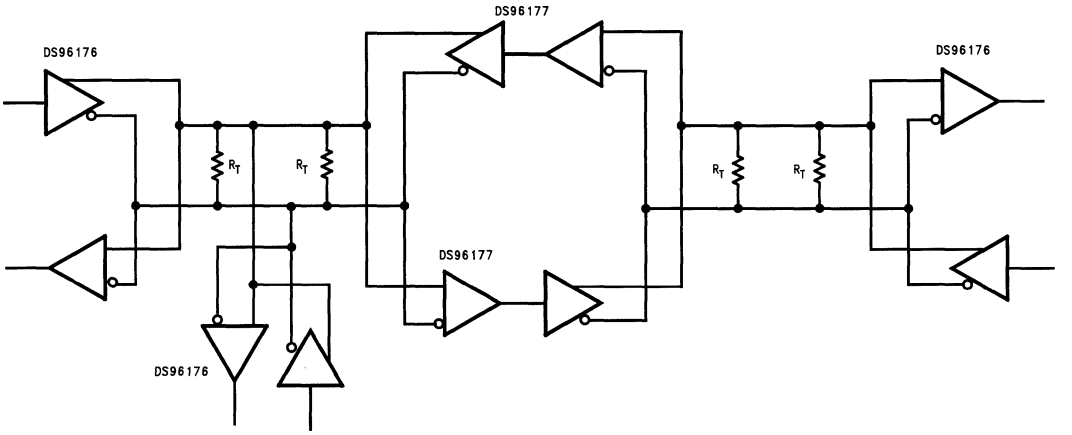
Note 1: The input pulse is supplied by a generator having the following characteristics: PRR = 1.0 MHz, duty cycle ≈ 50%, $t_r \leq 6.0$ ns, $t_f \leq 6.0$ ns, $Z_O = 50\Omega$.

Note 2: C_L includes probe and stray capacitance.

Note 3: DS96177 Enable is active high.

Note 4: All diodes are 1N916 or equivalent.

Typical Application



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Notes:

The line length should be terminated at both ends in its characteristic impedance.

Stub lengths off the main line should be kept as short as possible.

Repeater control logic not shown

FIGURE 10

Section 5

LVDS RS-644 Circuits

Section 5 Contents

LVDS Introduction

Low Voltage Differential Signaling (LVDS) is a new technology addressing the needs of today's high performance data transmission applications. It is designed to meet the needs of future applications since the power supply may be as low as 2V. This technology is based on the TIA/EIA-644 and IEEE 1596.3 standards.

LVDS technology features a low voltage differential signal of 330 mV (250 mV MIN and 400 mV MAX) and fast transition times. This allows the products to address high data rates easily exceeding 450 Mbit/s for some devices such as the DS90CR583/4. Additionally, the low voltage swing minimizes power dissipation while providing all the benefits of differential transmission.

The LVDS technology is used in simple (quad) drivers and receivers as well as more complex interface communications devices. The FPD (Flat Panel Display) Link and Channel Link chipsets multiplex and demultiplex TTL signal lines to provide a narrow, high speed LVDS interface. The QuickRing™ (QR1001) Enhanced Datastream Controller provides additional logic to support communications protocol and a ring architecture.

Included in this section are the following related products:

- DS90C031 LVDS Quad CMOS Differential Line Driver
- DS90C032 LVDS Quad CMOS Differential Line Receiver
- DS90CR561/2/3/4 18-Bit Color Flat Panel Display Link
- DS90CF561/2/3/4 18-Bit Color Flat Panel Display Link
- DS90CR581/2/3/4 24-Bit Color Flat Panel Display Link
- DS90CF581/2/3/4 24-Bit Color Flat Panel Display Link
- DS90CR211/2 21-Bit Channel Link
- DS90CR281/2 28-Bit Channel Link
- QR1001 QuickRing Enhanced Data Stream Controller

These products, the first in a planned series, introduce LVDS technology and provide designers with new alternatives to solving high speed I/O interface problems.

National Semiconductor

DS90C031
LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11 mW typical.

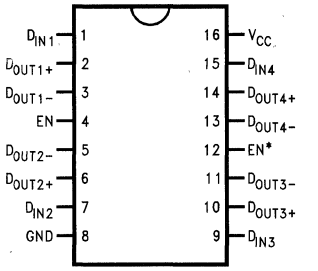
The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- ±350 mV differential signaling
- Ultra low power dissipation
- 400 ps maximum differential skew (5V, 25°C)
- 3.5 ns maximum propagation delay
- Industrial operating temperature range
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C31, MB571 (PECL) and 41LG (PECL)
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with proposed TIA LVDS standard

Connection Diagram

Dual-In-Line



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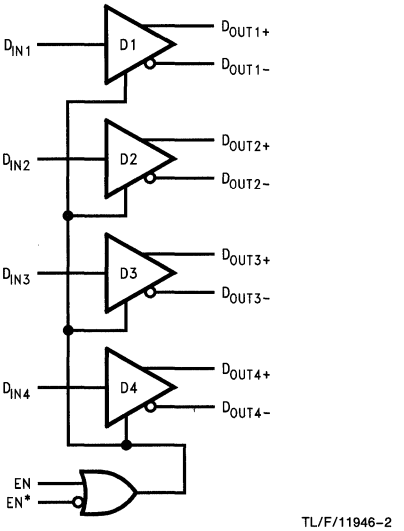
Order Number DS90C031TM
See NS Package Number M16A

Functional Diagram and Truth Tables



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DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**$D_{OUT}+$**	**$D_{OUT}-$**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (D_{IN})	−0.3V to (V_{CC} + 0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} + 0.3V)
Output Voltage ($D_{OUT}+$, $D_{OUT}-$)	−0.3V to (V_{CC} + 0.3V)
Short Circuit Duration ($D_{OUT}+$, $D_{OUT}-$)	Continuous
Maximum Package Power Dissipation @ +25°C M Package	1068 mW
Derate M Package	8.5 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥3,500V (Note 7)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Notes 2 and 3).

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
V_{OD1}	Differential Output Voltage	R_L = 100Ω (*Figure 1*)	$D_{OUT}-$, $D_{OUT}+$	250	345	450	mV
ΔV_{OD1}	Change in Magnitude of V_{OD1} for Complementary Output States				4	35	|mV|
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States				5	25	|mV|
V_{OH}	Output Voltage High	R_L = 100Ω			1.41	1.60	V
V_{OL}	Output Voltage Low			0.90	1.07		V
V_{IH}	Input Voltage High		D_{IN}, EN, EN*	2.0		V_{CC}	V
V_{IL}	Input Voltage Low			GND		0.8	V
I_I	Input Current	V_{IN} = V_{CC}, GND, 2.5V, or 0.4V		−10	±1	+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V (Note 8)	$D_{OUT}-$, $D_{OUT}+$		−3.5	−5.0	mA
I_{OZ}	Output TRI-STATE Current	EN = 0.8V and EN* = 2.0V, V_{OUT} = 0V or V_{CC}		−10	±1	+10	μA
I_{CC}	No Load Supply Current Drivers Enabled	D_{IN} = V_{CC} or GND	V_{CC}		1.7	3.0	mA
		D_{IN} = 2.5V or 0.4V			4.0	6.5	mA
I_{CCL}	Loaded Supply Current Drivers Enabled	R_L = 100Ω All Channels V_{IN} = V_{CC} or GND (all inputs)			15.4	21.0	mA
I_{CCZ}	No Load Supply Current Drivers Disabled	D_{IN} = V_{CC} or GND EN = GND, EN* = V_{CC}			2.2	4.0	mA

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Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (Notes 3, 4, 6, 9)

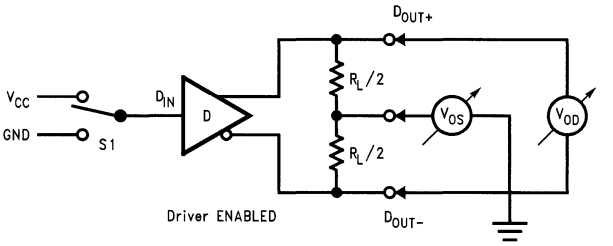
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (*Figures 2* and *3*)	1.0	2.0	3.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	2.1	3.0	ns
t_{SKD} $\lvert t_{PHLD} - t_{PLHD} \rvert$	Differential Skew		0	80	400	ps
t_{SK1}	Channel to Channel Skew	Note 4	0	300	600	ps
t_{TLH}	Rise Time	R_L = 100Ω, C_L = 5 pF (*Figures 2* and *3*)		0.35	1.5	ns
t_{THL}	Fall Time			0.35	1.5	ns
t_{PHZ}	Disable Time High to Z	(*Figures 4* and *5*)		2.5	10	ns
t_{PLZ}	Disable Time Low to Z			2.5	10	ns
t_{PZH}	Enable Time Z to High			2.5	10	ns
t_{PZL}	Enable Time Z to Low			2.5	10	ns

Switching Characteristics

V_{CC} = +5.0V ±10%, T_A = −40°C to +85°C (Notes 3–6, 9)

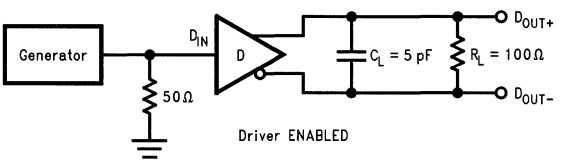
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω, C_L = 5 pF (*Figures 2* and *3*)	0.5	2.0	3.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.5	2.1	3.5	ns
t_{SKD} $\lvert t_{PHLD} - t_{PLHD} \rvert$	Differential Skew		0	80	900	ps
t_{SK1}	Channel to Channel Skew	Note 4	0	0.3	1.0	ns
t_{SK2}	Chip to Chip Skew	Note 5			3.0	ns
t_{TLH}	Rise Time	R_L = 100Ω, C_L = 5 pF (*Figures 2* and *3*)		0.35	2.0	ns
t_{THL}	Fall Time			0.35	2.0	ns
t_{PHZ}	Disable Time High to Z	(*Figures 4* and *5*)		2.5	15	ns
t_{PLZ}	Disable Time Low to Z			2.5	15	ns
t_{PZH}	Enable Time Z to High			2.5	15	ns
t_{PZL}	Enable Time Z to Low			2.5	15	ns

Parameter Measurement Information



TL/F/11946–3

FIGURE 1. Driver V_{OD} and V_{OS} Test Circuit



TL/F/11946–4

FIGURE 2. Driver Propagation Delay and Transition Time Test Circuit

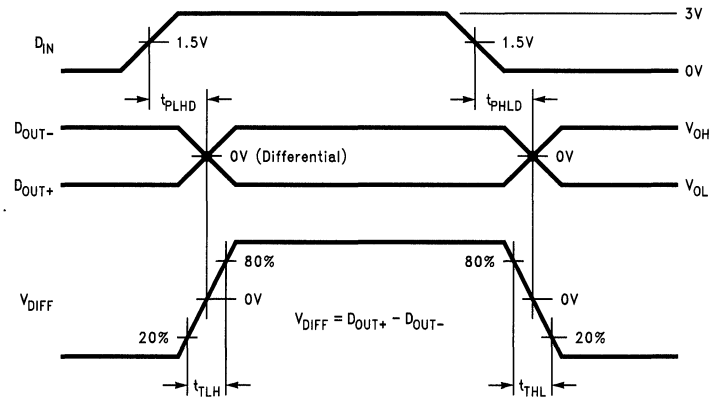


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FIGURE 3. Driver Propagation Delay and Transition Time Waveforms

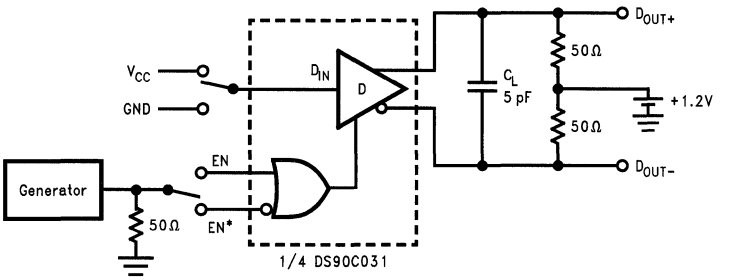

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FIGURE 4. Driver TRI-STATE Delay Test Circuit

Parameter Measurement Information (Continued)

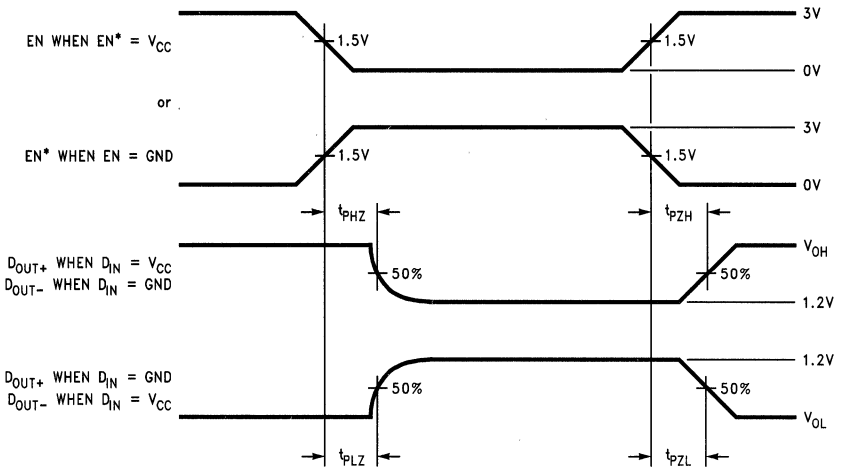

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FIGURE 5. Driver TRI-STATE Delay Waveform

Typical Application

Balanced System

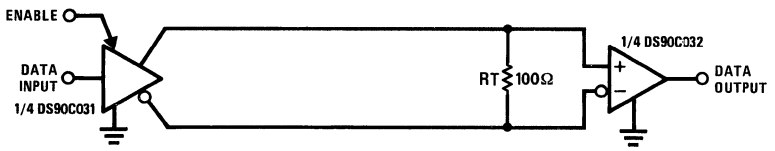

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FIGURE 6. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 6*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multireceiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C031 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The typical output current is mere 3.4 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode **requires** (as discussed above) that a resistive termination be employed to terminate the signal and to complete the loop as shown in *Figure 6*. AC or unterminated configurations are not allowed. The 3.4 mA loop current will develop a differential voltage of 340 mV across the 100Ω termination resistor which the receiver detects with a 240 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (340 mV−100 mV = 240 mV)). The signal is centered around +1.2V (Driver Offset, V_{OS}) with respect to ground as shown in *Figure 7*. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 680 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz−50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires >80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

The footprint of the DS90C031 is the same as the industry standard 26LS31 Quad Differential (RS-422) Driver.

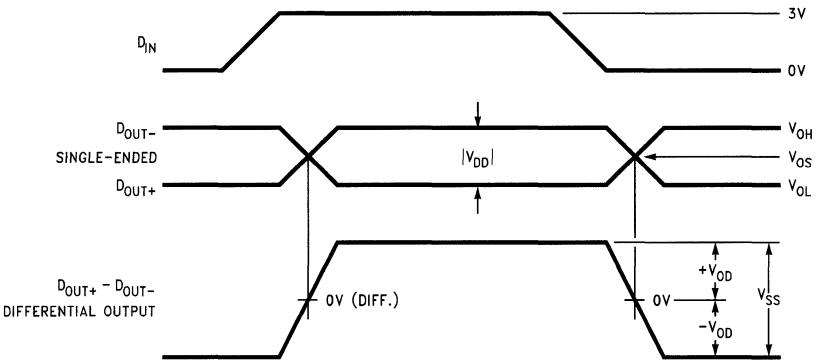

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FIGURE 7. Driver Output Levels

Pin Descriptions

Pin No.	Name	Description
1, 7, 9, 15	D_{IN}	Driver input pin, TTL/CMOS compatible
2, 6, 10, 14	$D_{OUT}+$	Non-inverting driver output pin, LVDS levels
3, 5, 11, 13	$D_{OUT}-$	Inverting driver output pin, LVDS levels
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ±10%
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40°C to +85°C	SOP/M16A	DS90C031TM

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.

Note 4: Channel to Channel Skew is defined as the difference between the propagation delay of the channel and the other channels in the same chip with an event on the inputs.

Note 5: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Note 6: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, $t_r \leq 6$ ns, and $t_f \leq 6$ ns.

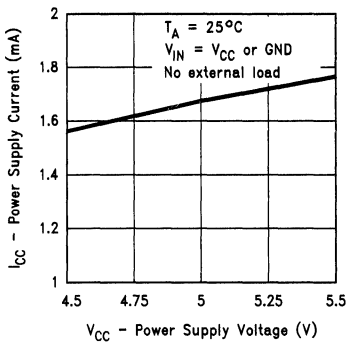
Note 7: ESD Ratings: HBM (1.5 kΩ, 100 pF) ≥ 3,500V
EIAJ (0Ω, 200 pF) ≥ 250V

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

Note 9: C_L includes probe and jig capacitance.

Typical Performance Characteristics

Power Supply Current vs Power Supply Voltage



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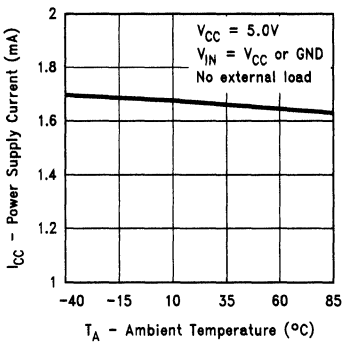
Power Supply Current vs Temperature



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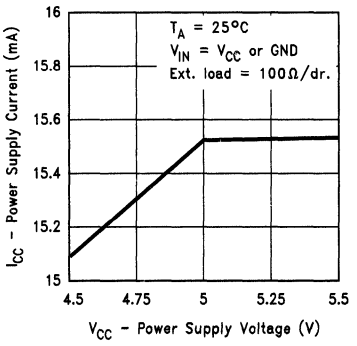
Power Supply Current vs Power Supply Voltage



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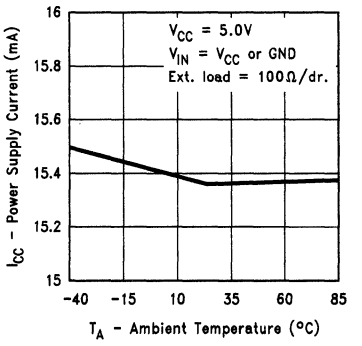
Power Supply Current vs Temperature



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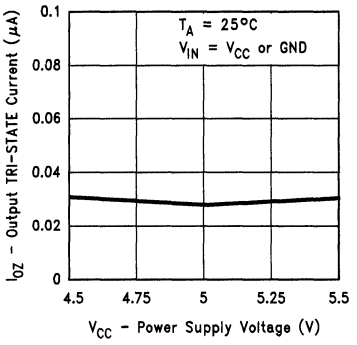
Output TRI-STATE Current vs Power Supply Voltage



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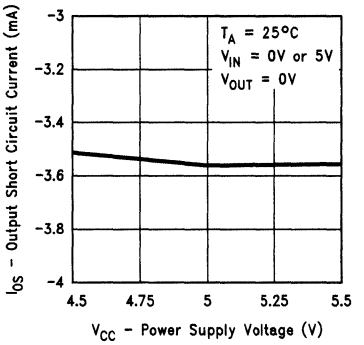
Output Short Circuit Current vs Power Supply Voltage



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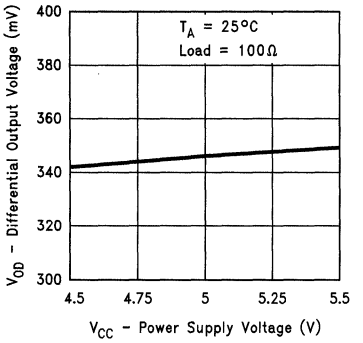
Typical Performance Characteristics (Continued)

Differential Output Voltage vs Power Supply Voltage



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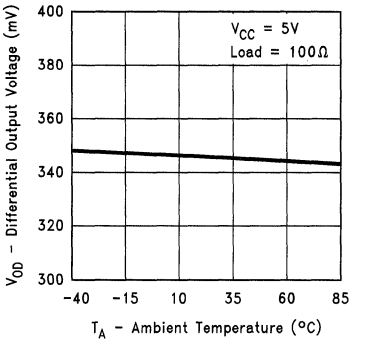
Differential Output Voltage vs Ambient Temperature



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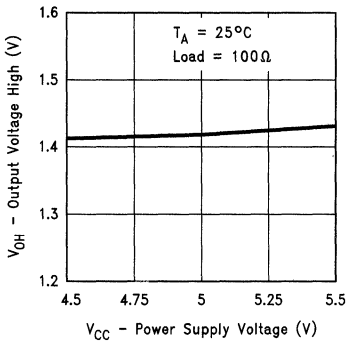
Output Voltage High vs Power Supply Voltage



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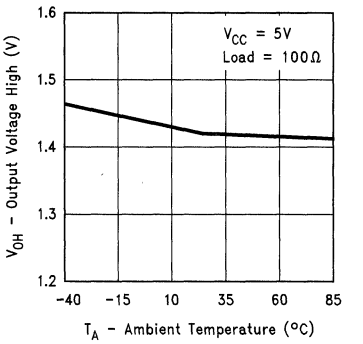
Output Voltage High vs Ambient Temperature



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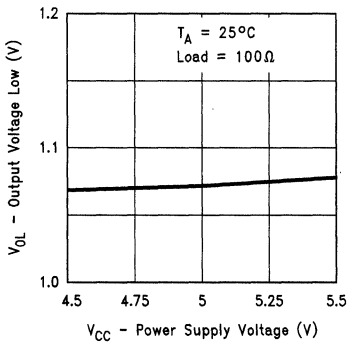
Output Voltage Low vs Power Supply Voltage



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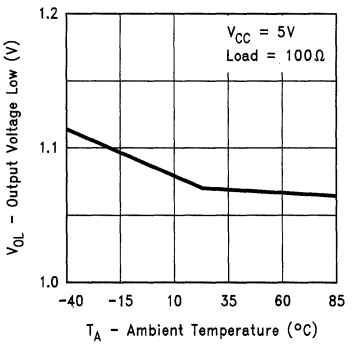
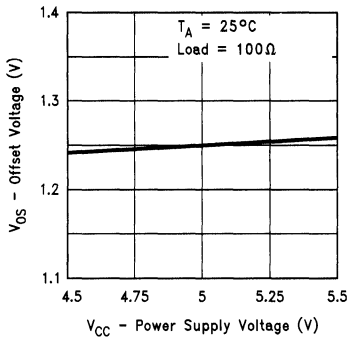
Output Voltage Low vs Ambient Temperature



TL/F/11946–21

Typical Performance Characteristics (Continued)

Offset Voltage vs Power Supply Voltage



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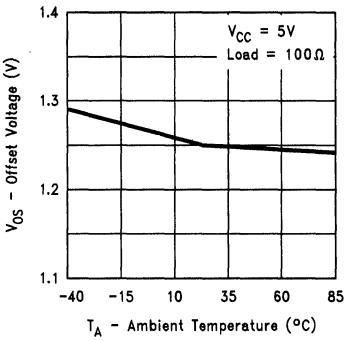
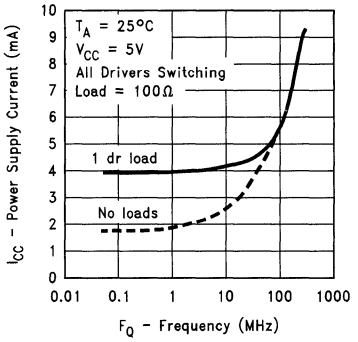
Offset Voltage vs Ambient Temperature



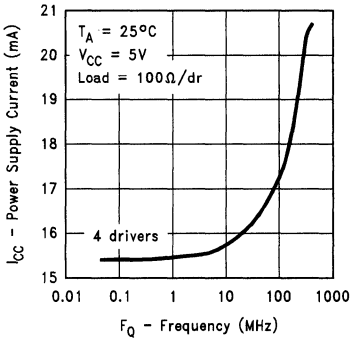
TL/F/11946-23

Power Supply Current vs Frequency



TL/F/11946-24

Power Supply Current vs Frequency



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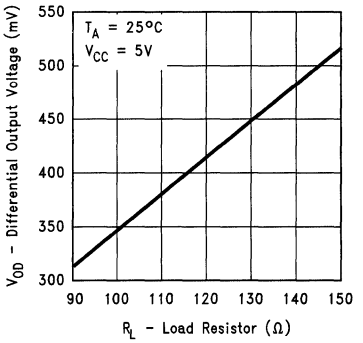
Differential Output Voltage vs Load Resistor



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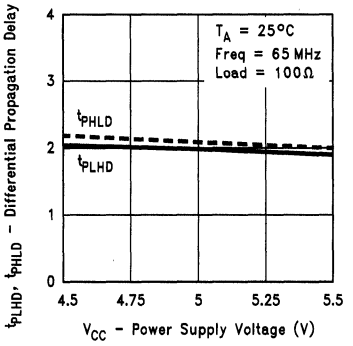
Typical Performance Characteristics (Continued)

Differential Propagation Delay vs Power Supply Voltage



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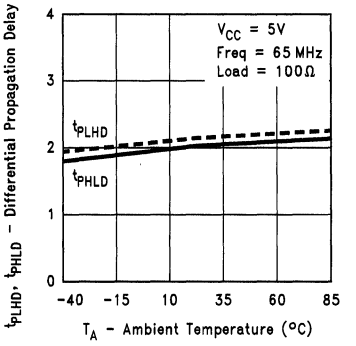
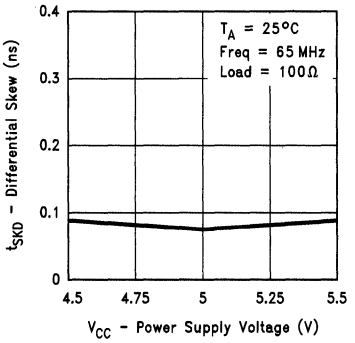
Differential Propagation Delay vs Ambient Temperature



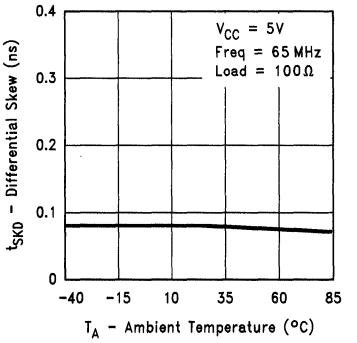
TL/F/11946–28

Differential Skew vs Power Supply Voltage



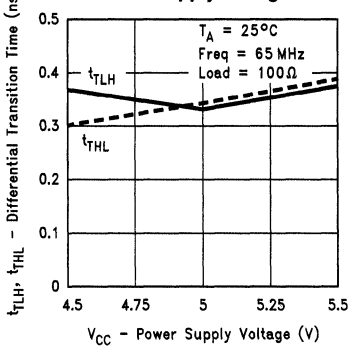
TL/F/11946–29

Differential Skew vs Ambient Temperature



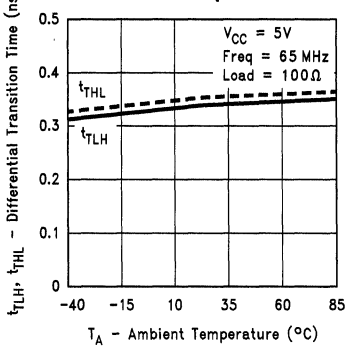
TL/F/11946–30

Differential Transition Time vs Power Supply Voltage



TL/F/11946–31

Differential Transition Time vs Ambient Temperature



TL/F/11946–32

National Semiconductor

ADVANCE INFORMATION

DS90LV031
3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 100 Mbps (50 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11 mW typical.

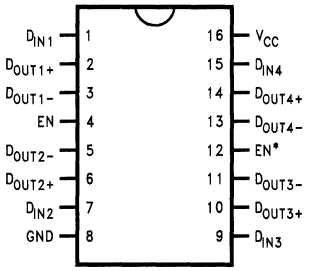
The DS90LV031 and companion line receiver (DS90LV032) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- 3.3V power supply design
- >100 Mbps (50 MHz) switching rates
- ±350 mV differential signaling
- Ultra low power dissipation
- TBD ps maximum differential skew (3.3V, 25°C)
- TBD ns maximum propagation delay
- Industrial operating temperature range (−40°C to +85°C)
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C31, MB571 (PECL), 41LG (PECL), and DS90C031
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with TIA/EIA-644 LVDS standard

Connection Diagram

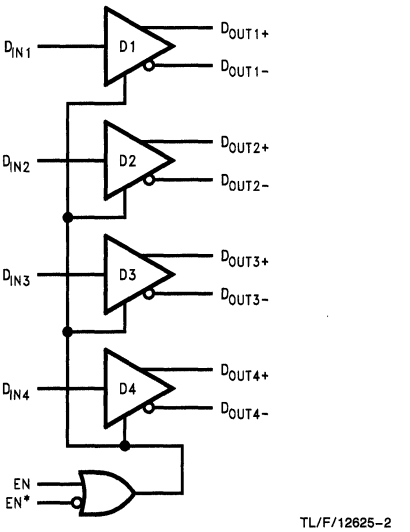
Dual-In-Line



TL/F/12625–1

Order Number DS90LV031TM
See NS Package Number M16A

Functional Diagram and Truth Tables



TL/F/12625–2

DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**$D_{OUT}+$**	**$D_{OUT}-$**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

National Semiconductor

DS90C032
LVDS Quad CMOS Differential Line Receiver

General Description

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C032 accepts low voltage (350 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100Ω) input Failsafe. Receiver output will be High for all failsafe conditions.

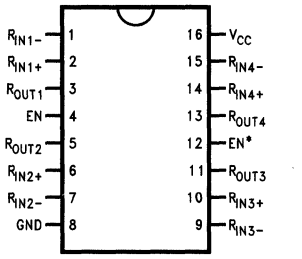
The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power psuedo-ECL devices for high speed point to point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- Accepts small swing (350 mV) differential signal levels
- Ultra low power dissipation
- 600 ps maximum differential skew (5V, 25°C)
- 6.0 ns maximum propagation delay
- Industrial operating temperature range
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C32A, MB570 (PECL) and 41LF (PECL)
- Supports OPEN, short and terminated input failsafe
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with proposed TIA LVDS standard

Connection Diagram

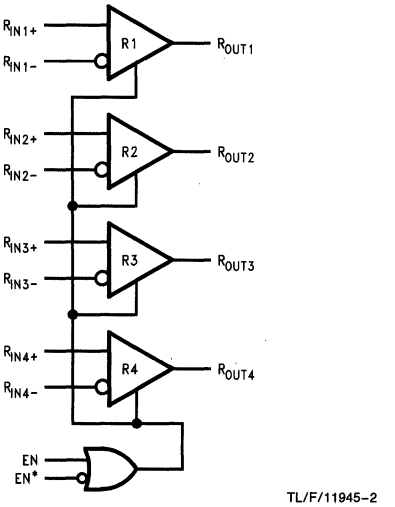
Dual-In-Line



TL/F/11945–1

Order Number
DS90C032TM
See NS Package Number M16A

Functional Diagram and Truth Tables



TL/F/11945–2

RECEIVER

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Failsafe OPEN/SHORT or Terminated	H

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Input Voltage (RIN+, RIN−)	−0.3V to (V_{CC} +0.3V)
Enable Input Voltage (EN, EN*)	−0.3V to (V_{CC} +0.3V)
Output Voltage (ROUT)	−0.3V to (V_{CC} +0.3V)
Maximum Package Power Dissipation @ +25°C	
M Package	1025 mW
Derate M Package	8.2 mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)	+260°C
Maximum Junction Temperature	+150°C
ESD Rating (HBM 1.5 kΩ, 100 pF)	≥ 3,500V (Note 7)

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)	−40	25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 2).

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V		$R_{IN}+$, $R_{IN}-$			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V		−10	±1	+10	μA
		V_{IN} = 0V			−10	±1	+10	μA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	3.8	4.9		V
		I_{OH} = −0.4 mA, Input terminated			3.8	4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.07	0.3	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V (Note 8)			−15	−60	−100	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}			−10	±1	+10	μA
V_{IH}	Input High Voltage			EN, EN*	2.0			V
V_{IL}	Input Low Voltage						0.8	V
I_I	Input Current				−10	±1	+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current	EN, EN* = V_{CC} or GND, Inputs Open		V_{CC}		3.5	10	mA
	Receivers Enabled	EN, EN* = 2.4 or 0.5, Inputs Open				3.7	11	mA
I_{CCZ}	No Load Supply Current Receivers Disabled	EN = GND, EN* = V_{CC} Inputs Open				3.5	10	mA

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (Notes 3–5, 9)

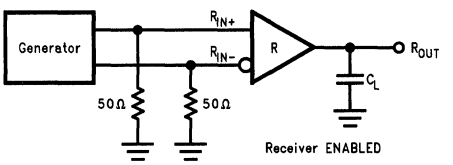
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV	1.5	3.40	5.0	ns
t_{PLHD}	Differential Propagation Delay Low to High	*(Figures 1 and 2)*	1.5	3.48	5.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$		0	80	600	ps
t_{SK1}	Channel to Channel Skew	(Note 5)	0	0.6	1.0	ns
t_{TLH}	Rise Time	*(Figures 1 and 2)*		0.5	2.0	ns
t_{THL}	Fall Time			0.5	2.0	ns
t_{PHZ}	Disable Time High to Z	*(Figures 3 and 4)*		10	15	ns
t_{PLZ}	Disable Time Low to Z			10	15	ns
t_{PZH}	Enable Time Z to High			4	10	ns
t_{PZL}	Enable Time Z to Low			4	10	ns

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40°C to +85°C (Notes 3–6, 9)

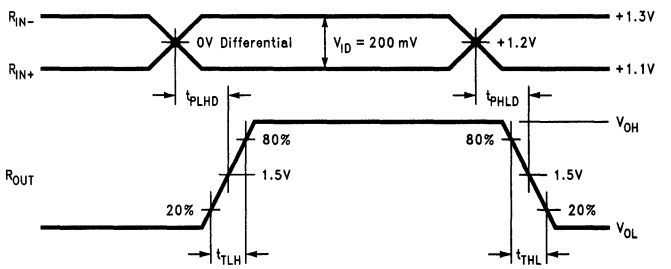
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV	1.0	3.40	6.0	ns
t_{PLHD}	Differential Propagation Delay Low to High	*(Figures 1 and 2)*	1.0	3.48	6.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$		0	0.08	1.2	ns
t_{SK1}	Channel to Channel Skew	(Note 5)	0	0.6	1.5	ns
t_{SK2}	Chip to Chip Skew	(Note 6)			5.0	ns
t_{TLH}	Rise Time	*(Figures 1 and 2)*		0.5	2.5	ns
t_{THL}	Fall Time			0.5	2.5	ns
t_{PHZ}	Disable Time High to Z	*(Figures 3 and 4)*		10	20	ns
t_{PLZ}	Disable Time Low to Z			10	20	ns
t_{PZH}	Enable Time Z to High			4	15	ns
t_{PZL}	Enable Time Z to Low			4	15	ns

Parameter Measurement Information



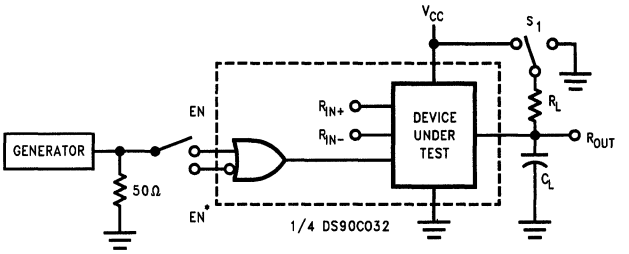
TL/F/11945–3

FIGURE 1. Receiver Propagation Delay and Transition Time Test Circuit



TL/F/11945–4

FIGURE 2. Receiver Propagation Delay and Transition Time Waveforms



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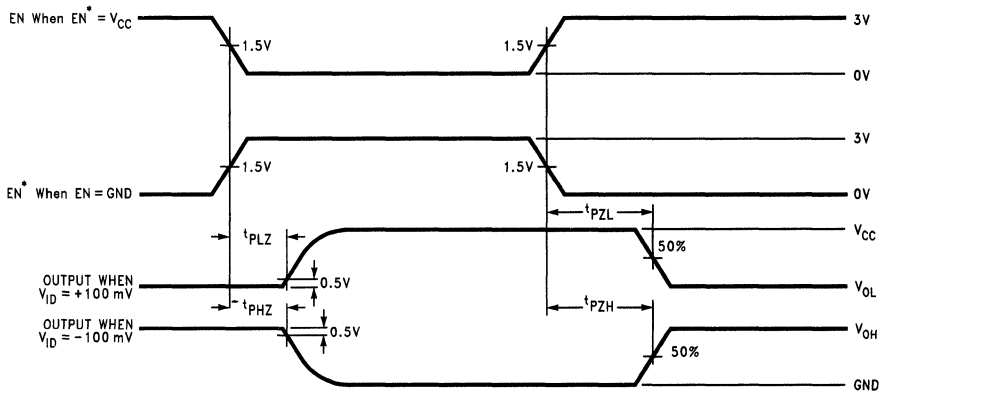
C_L includes load and test jig capacitance.
S_1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

FIGURE 3. Receiver TRI-STATE Delay Test Circuit

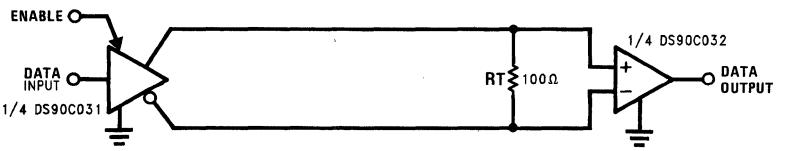


TL/F/11945–6

FIGURE 4. Receiver TRI-STATE Delay Waveforms

Typical Application

Balanced System



TL/F/11945–7

FIGURE 5. Point-to-Point Application

Applications Information

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 5.* This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multireceiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DS90C032 differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

The receiver also supports a failsafe feature which provides a stable (known state) high output voltage for any of the following conditions:

1. **Open Input Pins.** The DS90C032 is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or other voltages. The internal circuitry will guarantee a high, stable output state.
2. **Terminated Input.** If the driver is in a TRI-STATE condition, or if the driver is in a power-off condition, or if the driver is even disconnected (cable unplugged), the receiver output will again be in a high state, even with the end of cable 100Ω termination resistor across the input pins.
3. **Shorted Inputs.** If a cable fault condition occurs that shorts the twisted pair conductors together, thus resulting in a 0V differential input voltage to the receiver, the receiver output will remain in a high state.

The footprint of the DS90C032 is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

Pin Descriptions

Pin No.	Name	Description
2, 6, 10, 14	$R_{IN}+$	Non-inverting receiver input pin
1, 7, 9, 15	$R_{IN}-$	Inverting receiver input pin
3, 5, 11, 13	R_{OUT}	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ±10%
8	GND	Ground pin

Ordering Information

Operating Temperature	Package Type/ Number	Order Number
−40°C to +85°C	SOP/M16A	DS90C032TM

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.

Note 4: Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0%–100%) ≤ 1 ns for R_{IN} and t_r and t_f ≤ 6 ns for EN or EN*.

Note 5: Channel to Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

Note 6: Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

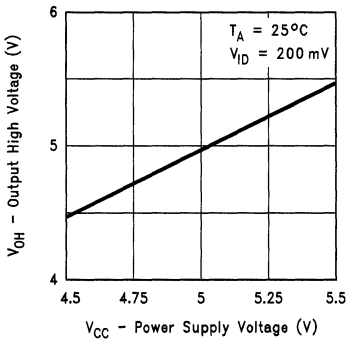
Note 7: ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 3,500V
EIAJ (0Ω, 200 pF) ≥ 250V

Note 8: Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Note 9: C_L includes probe and jig capacitance.

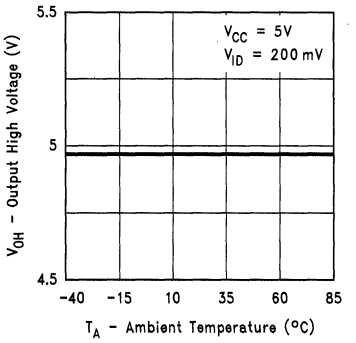
Typical Performance Characteristics

Output High Voltage vs Power Supply Voltage



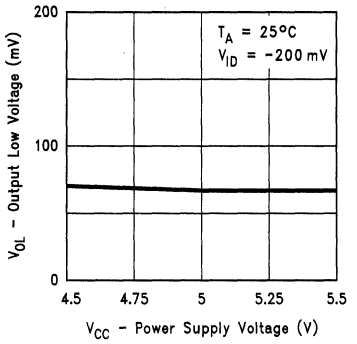
TL/F/11945–8

Output High Voltage vs Ambient Temperature



TL/F/11945–9

Output Low Voltage vs Power Supply Voltage



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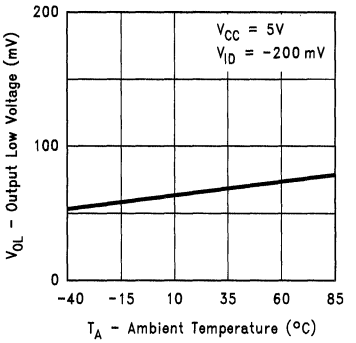
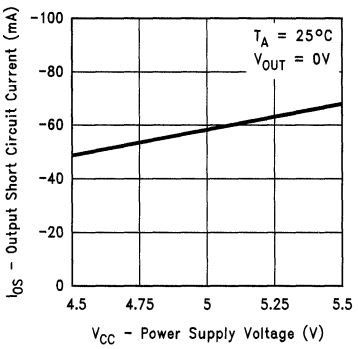
Output Low Voltage vs Ambient Temperature



TL/F/11945–11

Output Short Circuit Current vs Power Supply Voltage



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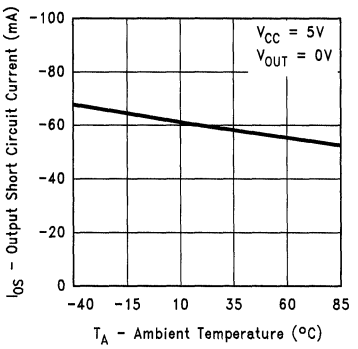
Output Short Circuit Current vs Ambient Temperature



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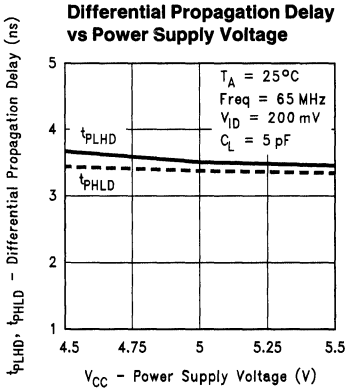
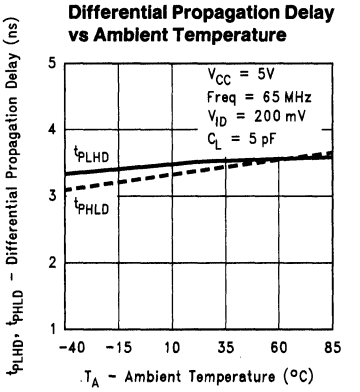
Typical Performance Characteristics (Continued)

Differential Propagation Delay vs Power Supply Voltage



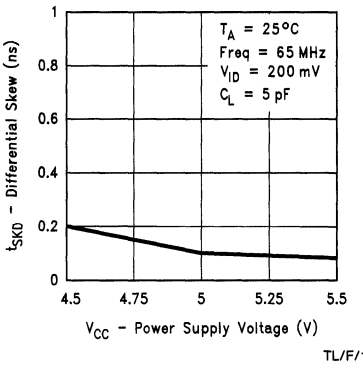
TL/F/11945–14

Differential Propagation Delay vs Ambient Temperature



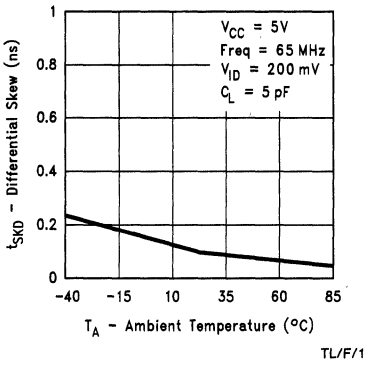
TL/F/11945–15

Differential Skew vs Power Supply Voltage



TL/F/11945–16

Differential Skew vs Ambient Temperature



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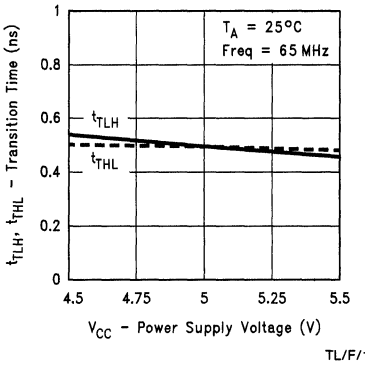
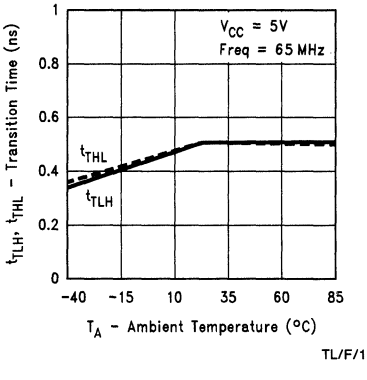
Transition Time vs Power Supply Voltage



TL/F/11945–18

Transition Time vs Ambient Temperature



TL/F/11945–19

National Semiconductor

ADVANCE INFORMATION

DS90LV032
3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 100 Mbps (50 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV032 accepts low voltage (350 mV) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100Ω) input Failsafe. Receiver output will be High for all failsafe conditions.

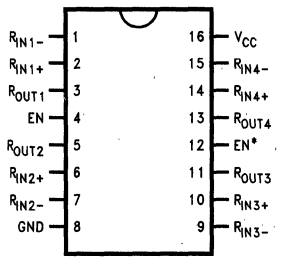
The DS90LV032 and companion line driver (DS90LV031) provide a new alternative to high power psuedo-ECL devices for high speed point to point interface applications.

Features

- 3.3V power supply design
- > 100 Mbps (50 MHz) switching rates
- Accepts small swing (350 mV) differential signal levels
- Ultra low power dissipation
- TBD ps maximum differential skew (3.3V, 25°C)
- TBD ns maximum propagation delay
- Industrial operating temperature range (−40°C to +85°C)
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C32A, MB570 (PECL), 41LF (PECL), and DS90C032
- Supports OPEN, short and terminated input failsafe
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with TIA/EIA-644 LVDS standard

Connection Diagram

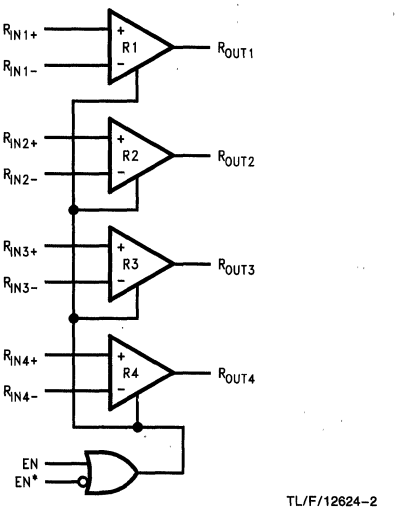
Dual-In-Line



TL/F/12624–1

Order Number
DS90LV032TM
See NS Package Number M16A

Functional Diagram and Truth Tables



TL/F/12624–2

RECEIVER

ENABLES		INPUTS	OUTPUT
EN	**EN***	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Failsafe OPEN/SHORT or Terminated	H

National Semiconductor

PRELIMINARY

DS90CR211/DS90CR212
21-Bit Channel Link

General Description

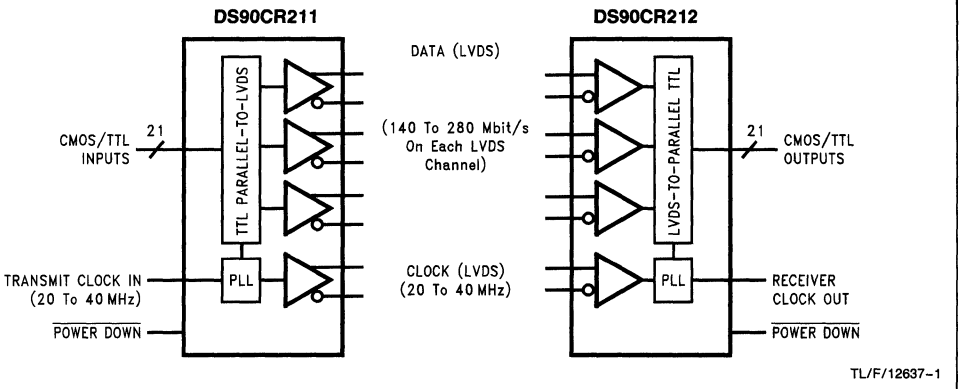
The DS90CR211 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR212 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 21 bits of TTL data are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 105 Megabytes per second.

The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, 5 4-bit nibbles plus 1 control, or 2 9-bit (byte + parity) and 3 control.

Features

- Up to 105 Mbyte/s bandwidth
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Narrow bus reduces cable size

Block Diagrams



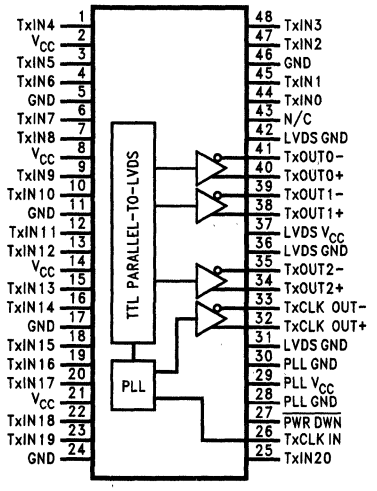
TL/F/12637-1

Order Number DS90CR211MTD
See NS Package Number MTD48

Order Number DS90CR212MTD
See NS Package Number MTD48

Connection Diagrams

DS90CR211



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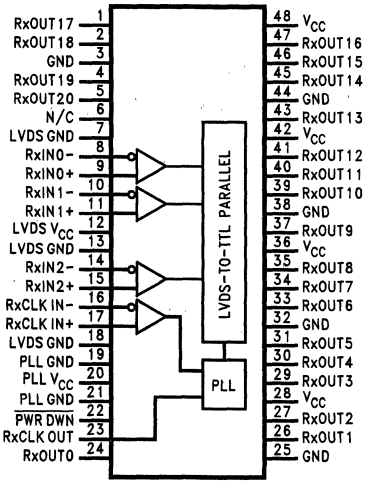
DS90CR212



TL/F/12637-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Ouput Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C

Maximum Power Dissipation @ +25°C

MTD48 (TSSOP) Package:	
DS90CR211	1.98W
DS90CR212	1.89W
Package Derating: DS90CR211	16 mW/°C above +25°C
DS90CR212	15 mW/°C above +25°C

This device does not meet 2000V ESD rating (Note 4).

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	V
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 2)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 2)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 2)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 3)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 3)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 4)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 5)*				350	ps
TSSPW	Tx Sub-Symbol Pulse Width *(Figure 5)*	f = 20 MHz	5.5	7	8	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 6)*		25	T	50	ns
TCIH	TxCLK IN High Time *(Figure 6)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 6)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 6)*		8			ns
THTC	TxIN Hold to TxCLK IN *(Figure 6)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 7)*		25	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Continued)

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 7)*	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RCOL	RxCLK OUT Low Time *(Figure 7)*	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RSRC	RxCLK Setup to RxCLK OUT *(Figure 7)*	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxCLK Hold to RxCLK OUT *(Figure 7)*	f = 20 MHz	16			ns
		f = 40 MHz	6			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 8)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 10)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 11)*				10	ms

5

AC Timing Diagrams

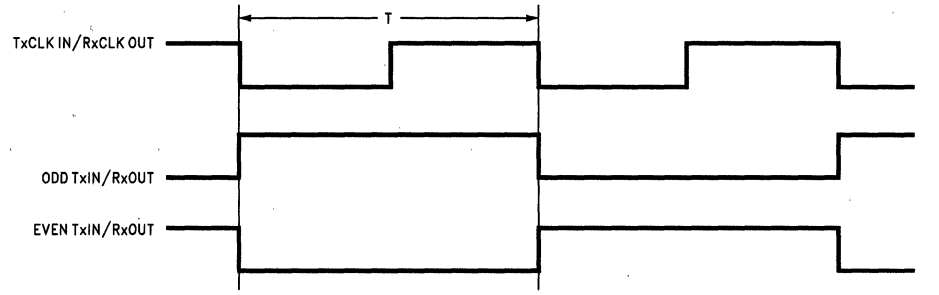


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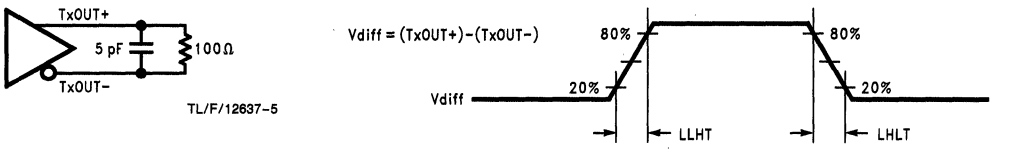
FIGURE 1. "WORST CASE" Test Pattern



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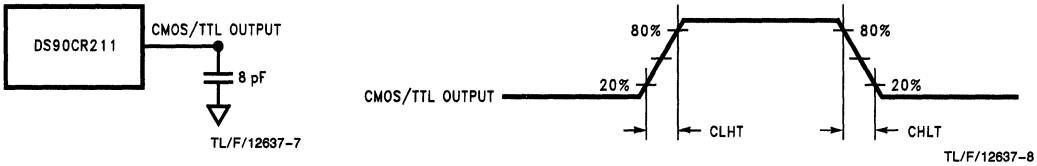
TL/F/12637-6

FIGURE 2. DS90CR211 (Transmitter) LVDS Output Load and Transition Timing



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TL/F/12637-8

FIGURE 3. DS90CR212 (Receiver) CMOS/TTL Output Load and Transition Timing

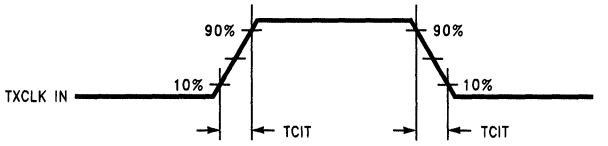

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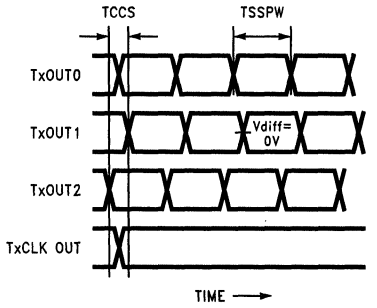
FIGURE 4. DS90CR211 (Transmitter) Input Clock Transition Time



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Note 1: Measurements at Vdiff = 0V

Note 2: TCCS measured between earliest and latest initial LVDS edges.

Note 3: TxCLK OUT Differential Low → High Edge

FIGURE 5. DS90CR211 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

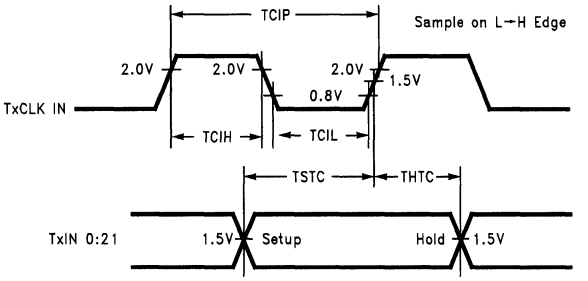

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FIGURE 6. DS90CR211 Setup/Hold and High/Low Times

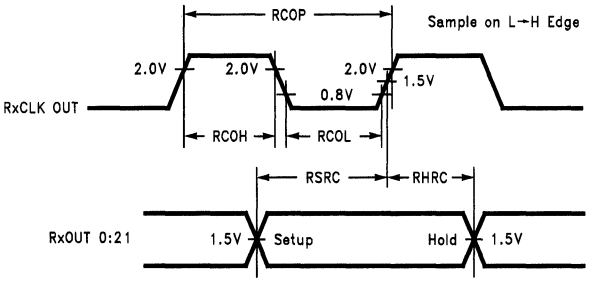

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FIGURE 7. DS90CR212 Setup/Hold and High/Low Times

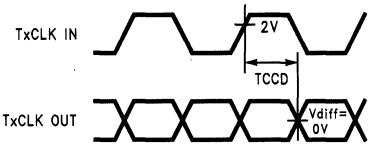

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FIGURE 8. DS90CR211 (Transmitter) Clock In to Clock Out Delay

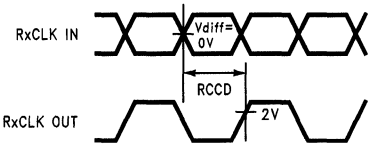

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FIGURE 9. DS90CR212 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

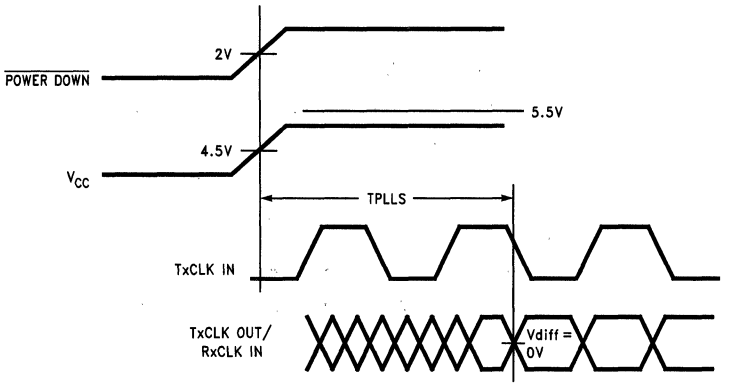

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FIGURE 10. DS90CR211 (Transmitter) Phase Lock Loop Set Time

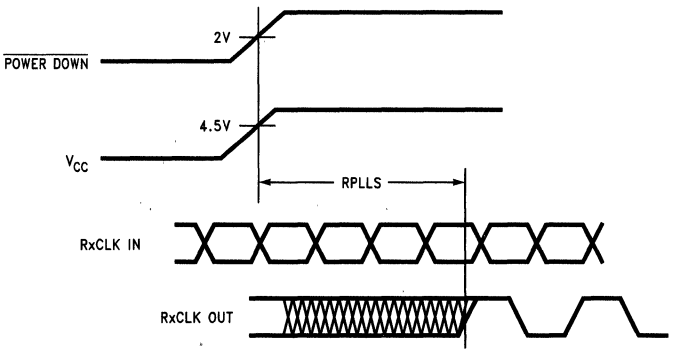

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FIGURE 11. DS90CR212 (Receiver) Phase Lock Loop Set Time

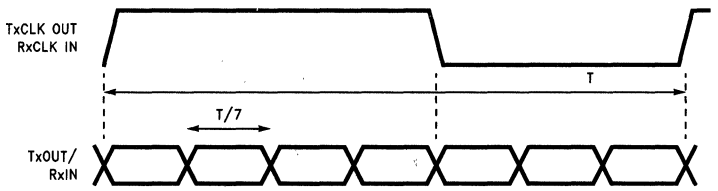

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FIGURE 12. Seven Bits of LVDS in One Clock Cycle

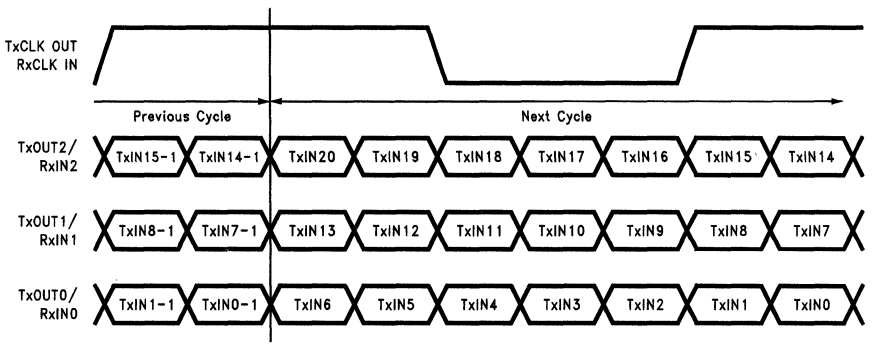

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FIGURE 13. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR211)

DS90CR211 Pin Description—Channel Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL Level inputs
TxOUT+	O	3	Positive LVDS differential data output
TxOUT−	O	3	Negative LVDS differential data output
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR212 Pin Description—Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN−	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level outputs
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

National Semiconductor

PRELIMINARY

DS90CR281/DS90CR282
28-Bit Channel Link

General Description

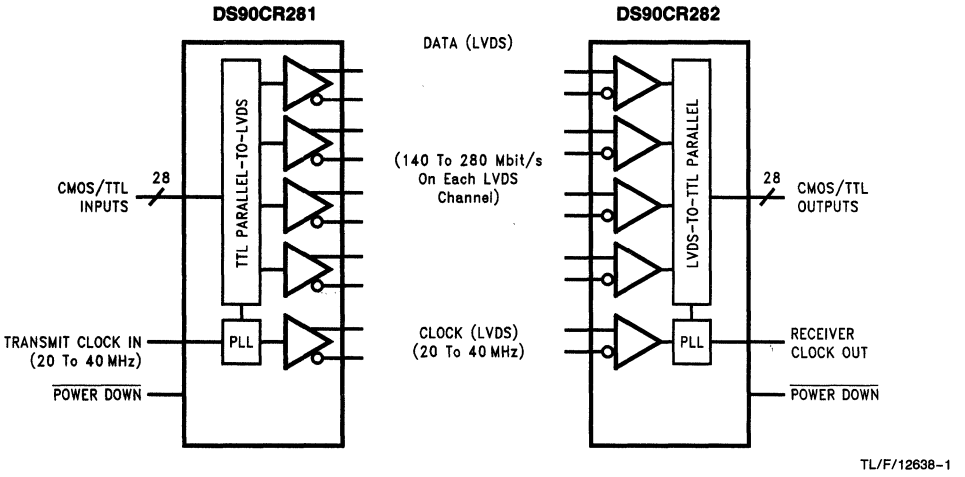
The DS90CR281 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR282 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 28 bits of TTL data are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second.

The 28 CMOS/TTL inputs can support a variety of signal combinations. For example, 7 4-bit nibbles or 3 9-bit (byte + parity) and 1 control.

Features

- Up to 140 Mbyte/sec bandwidth
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Rising edge data strobe
- Narrow bus reduces cable size

Block Diagrams



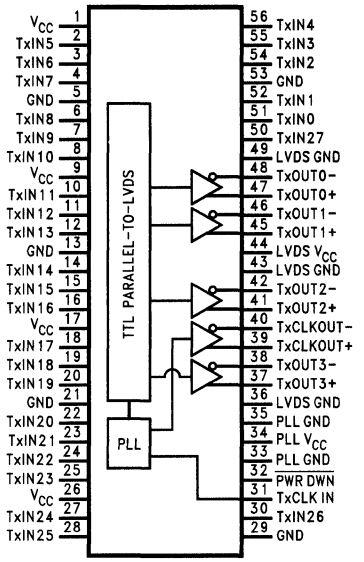
TL/F/12638–1

Order Number DS90CR281MTD
See NS Package Number MTD56

Order Number DS90CR282MTD
See NS Package Number MTD56

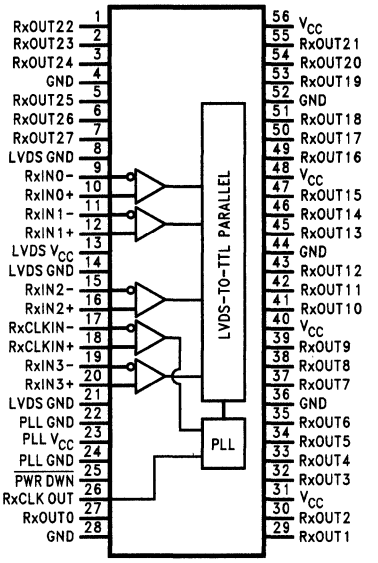
Connection Diagrams

DS90CR281



TL/F/12638-2

DS90CR282



TL/F/12638-3

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Ouput Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C

Maximum Package Power Dissipation @ +25°C

MTD56(TSSOP) Package:	
DS90CR281	1.63W
DS90CR282	1.61W

Package Derating: DS90CR281 12.5 mW/°C above +25°C
DS90CR282 12.4 mW/°C above +25°C

This device does not meet 2000V ESD rating (Note 4).

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	V
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	µA
		V_{IN} = 0V				±10	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 2)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 2)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 2)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 3)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 3)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 4)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 5)*				350	ps
TSSPW	Tx Sub-Symbol Pulse Width *(Figure 5)*	f = 20 MHz	5.5	7	8	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 6)*		25	T	50	ns
TCIH	TxCLK IN High Time *(Figure 6)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 6)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 6)*		8			ns
THTC	TxIN Hold to TxCLK IN *(Figure 6)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 7)*		25	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Continued)

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 7)*	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RCOL	RxCLK OUT Low Time *(Figure 7)*	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 7)*	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 7)*	f = 20 MHz	16			ns
		f = 40 MHz	6			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 8)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 10)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 11)*				10	ms

AC Timing Diagrams

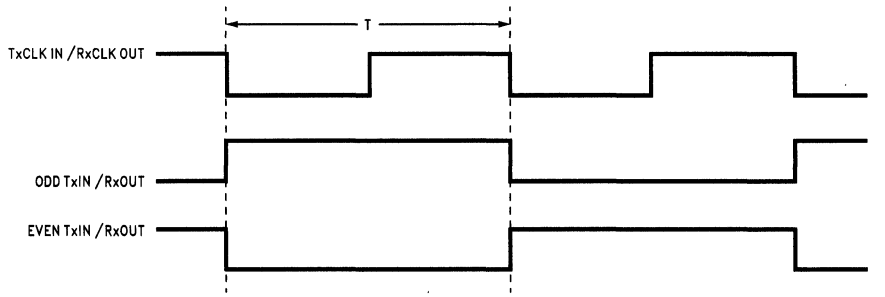


FIGURE 1. "WORST CASE" Test Pattern

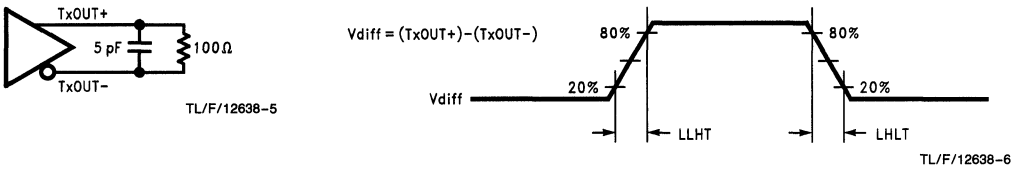


FIGURE 2. DS90CR281 (Transmitter) LVDS Output Load and Transition Timing

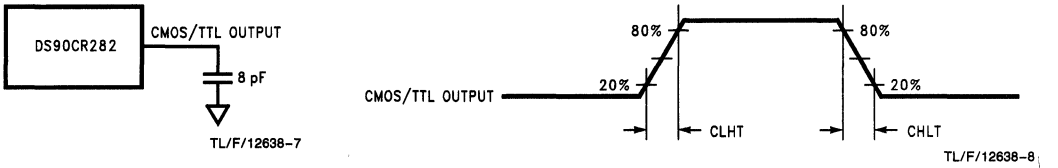


FIGURE 3. DS90CR282 (Receiver) CMOS/TTL Output Load and Transition Timing

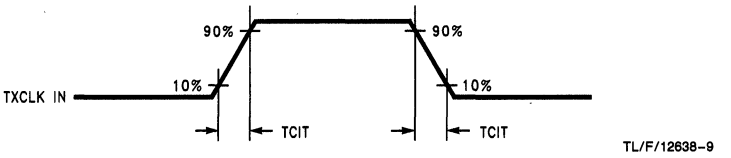
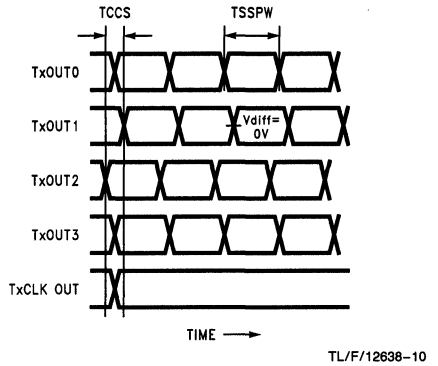


FIGURE 4. DS90CR281 (Transmitter) Input Clock Transition Time



Note 1: Measurements at V_{diff} = 0V
Note 2: TCCS measured between earliest and latest initial LVDS edges.
Note 3: TxCLK OUT Differential Low → High Edge

FIGURE 5. DS90CR281 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

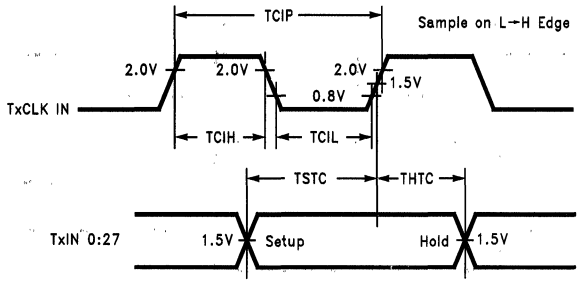


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FIGURE 6. DS90CR281 (Transmitter) Setup/Hold and High/Low Times

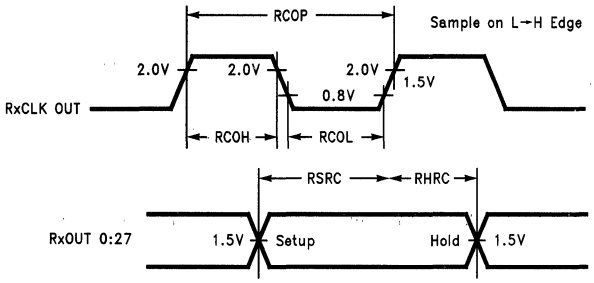

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FIGURE 7. (Receiver) DS90CR282 Setup/Hold and High/Low Times

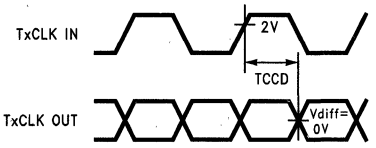

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FIGURE 8. DS90CR281 (Transmitter) Clock In to Clock Out Delay

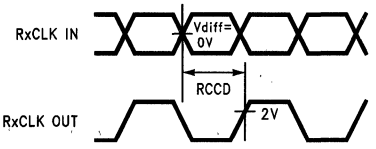

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FIGURE 9. DS90CR282 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

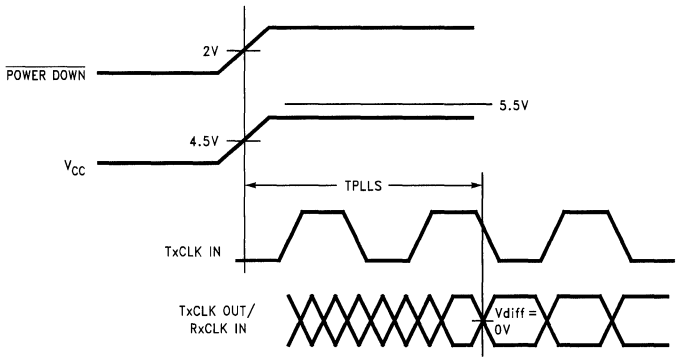

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FIGURE 10. DS90CR281 (Transmitter) Phase Lock Loop Set Time

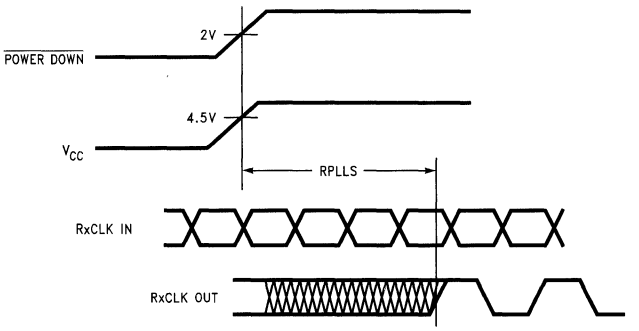

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FIGURE 11. DS90CR282 (Receiver) Phase Lock Loop Set Time

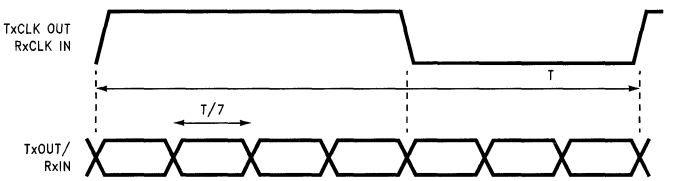

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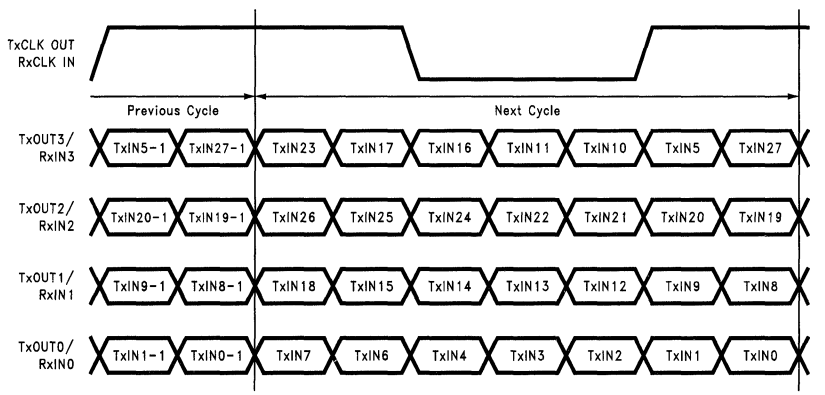
FIGURE 12. Seven Bits of LVDS in One Clock Cycle



TL/F/12638–18

FIGURE 13. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR281)

DS90CR281 Pin Description—Channel Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL Level inputs
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR282 Pin Description—Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs
RxIN−	I	4	Negative LVDS differential data inputs
RxOUT	O	28	TTL level outputs
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

National Semiconductor

DS90CR561/DS90CR562
LVDS 18-Bit Color Flat Panel Display (FPD) Link

General Description

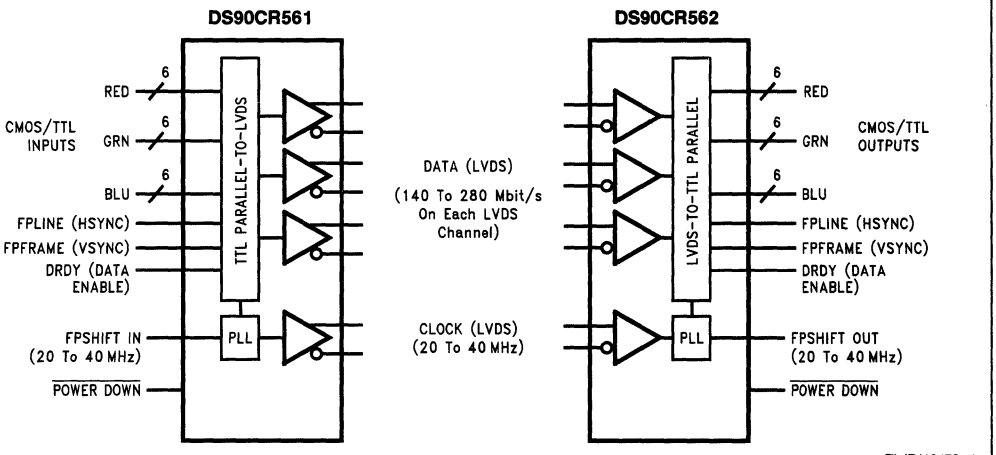
The DS90CR561 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR562 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 105 Megabytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 105 Megabyte/sec bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams

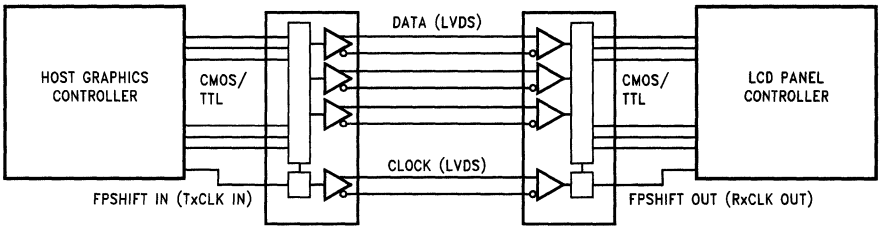


TL/F/12470–1

Order Number DS90CR561MTD
See NS Package Number MTD48

Order Number DS90CR562MTD
See NS Package Number MTD48

Application



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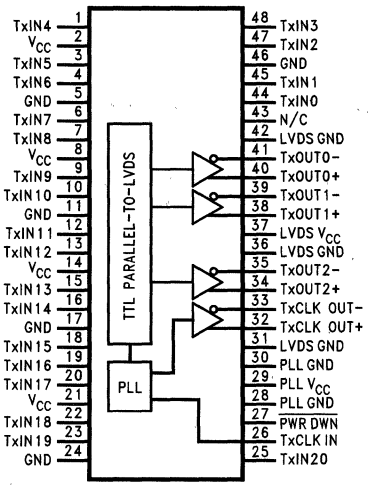
Connection Diagrams

DS90CR561



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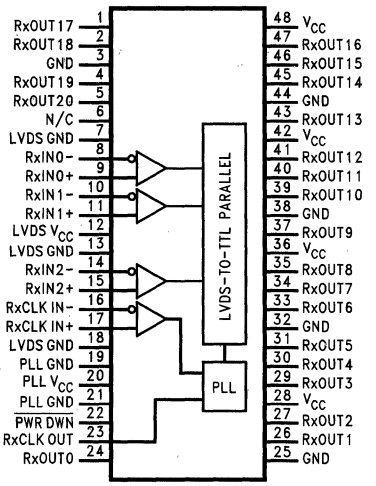
DS90CR562



TL/F/12470–4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Ouput Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C

Maximum Power Dissipation @ +25°C

MTD48 (TSSOP) Package:	
DS90CR561	1.98W
DS90CR562	1.89W
Package Derating: DS90CR561	16 mW/°C above +25°C
DS90CR562	15 mW/°C above +25°C

This device does not meet 2000V ESD rating (Note 4)

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complimentary Output States					35	V
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = OV, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	Tx Sub-Symbol Pulse Width *(Figure 6)*	f = 20 MHz	5.5	7	8	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		25	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*		8			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		25	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Continued)

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RSRC	RxCLK Setup to RxCLK OUT *(Figure 8)*	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxCLK Hold to RxCLK OUT *(Figure 8)*	f = 20 MHz	16			ns
		f = 40 MHz	6			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

5

AC Timing Diagrams

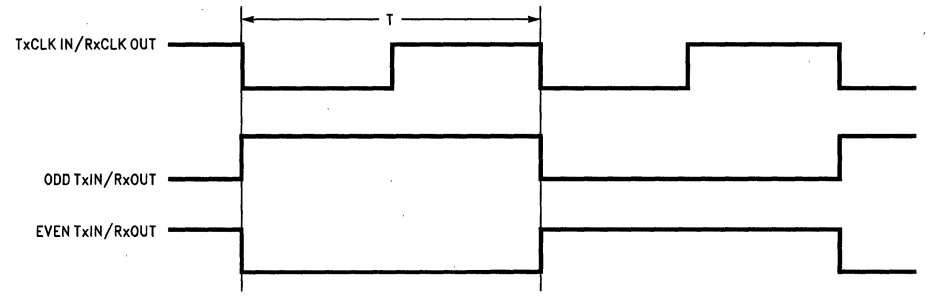


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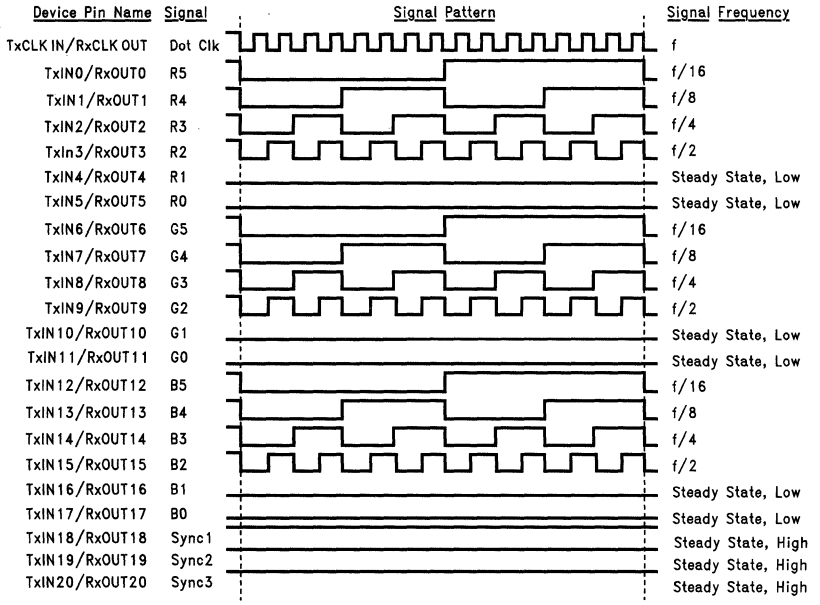
FIGURE 1. "Worst Case" Test Pattern



TL/F/12470–6

FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of device digital circuitry, LVDS I/O and TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a rising edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

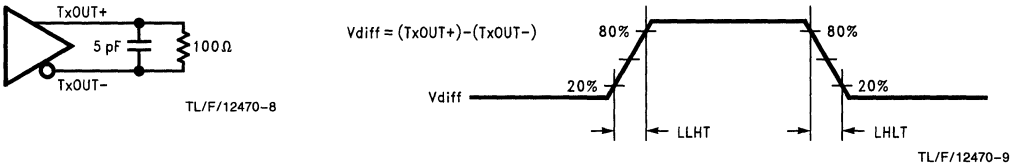


FIGURE 3. DS90CR561 (Transmitter) LVDS Output Load and Transition Timing

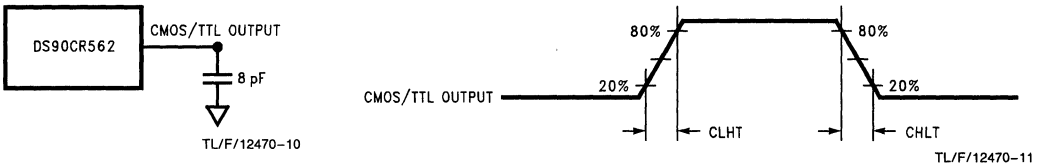


FIGURE 4. DS90CR562 (Receiver) CMOS/TTL Output Load and Transition Timing

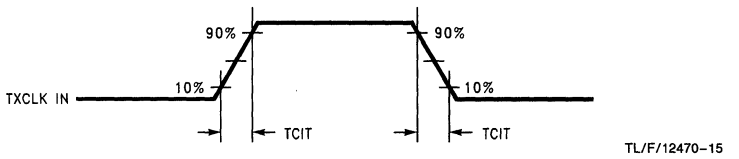
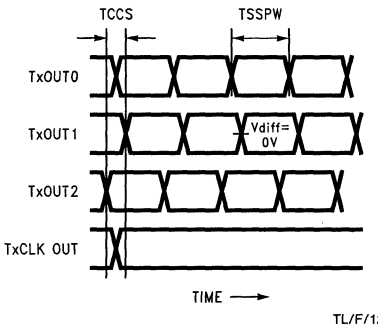


FIGURE 5. DS90CR561 (Transmitter) Input Clock Transition Time



Note 1: Measurements at Vdiff = 0V

Note 2: TCCS measured between earliest and latest initial LVDS edges.

Note 3: TxCLK OUT Differential High → Low Edge for DS90CF561
TxCLK OUT Differential Low → High Edge for DS90CR561

FIGURE 6. DS90CR561 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

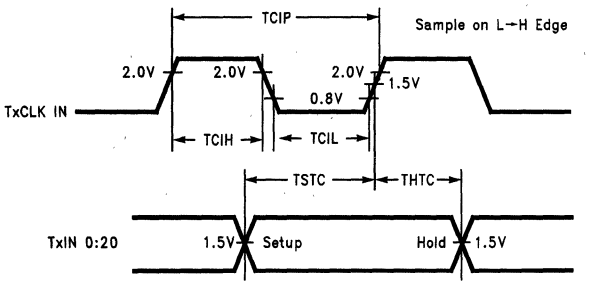


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FIGURE 7. DS90CR561 Setup/Hold and High/Low Times

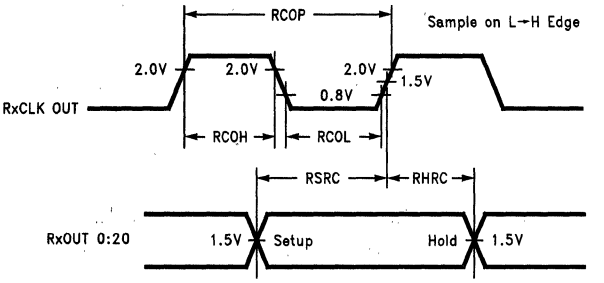

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FIGURE 8. DS90CR562 Setup/Hold and High/Low Times

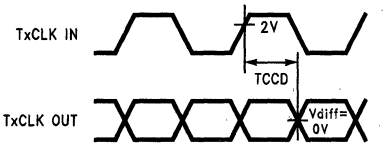

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FIGURE 9. DS90CR561 (Transmitter) Clock In to Clock Out Delay

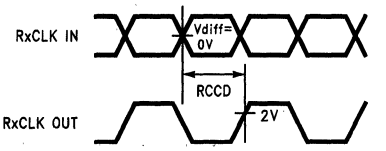

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FIGURE 10. DS90CR562 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

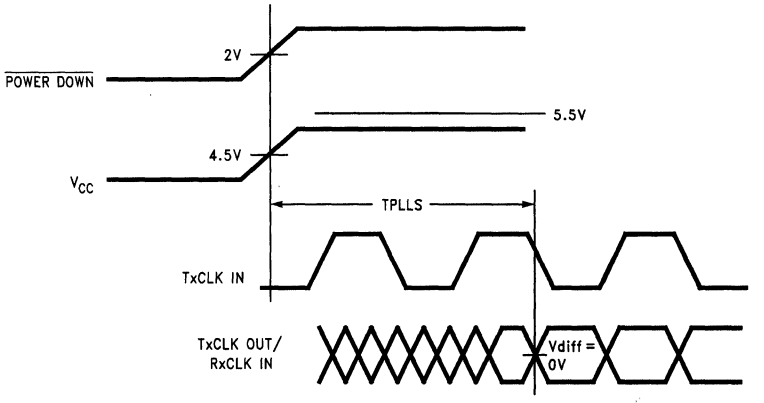

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FIGURE 11. DS90CR561 (Transmitter) Phase Lock Loop Set Time

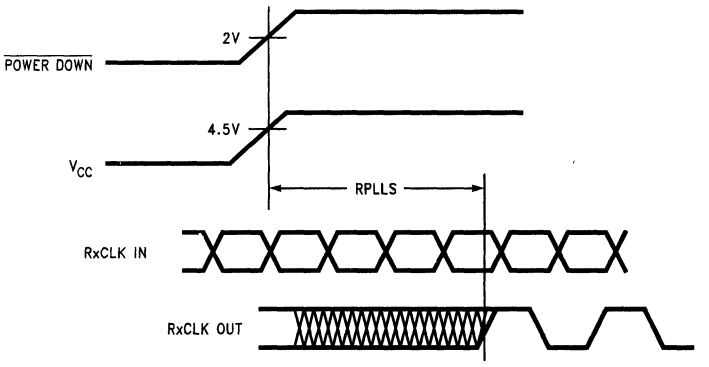

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FIGURE 12. DS90CR562 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

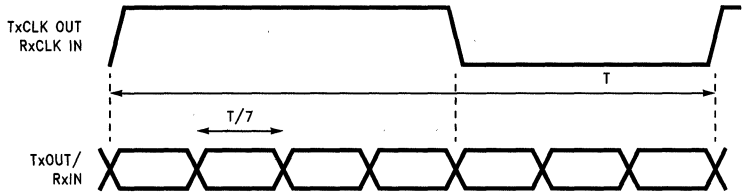

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FIGURE 13. Seven Bits of LVDS in One Clock Cycle

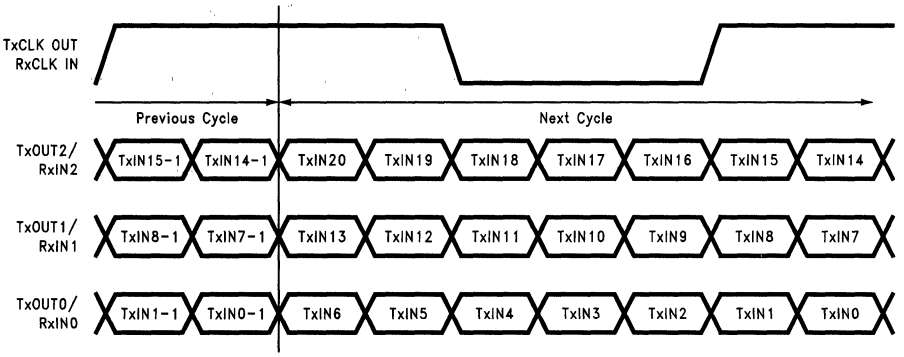

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FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR561)

DS90CR561 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL Level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY). (Also referred to as HSYNC, VSYNC and DATA ENABLE.)
TxOUT+	O	3	Positive LVDS differential data output
TxOUT−	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR562 Pin Description—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN−	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY). (Also referred to as HSYNC, VSYNC and DATA ENABLE.)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The rising edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

National Semiconductor

DS90CF561/DS90CF562
LVDS 18-Bit Color Flat Panel Display (FPD) Link

General Description

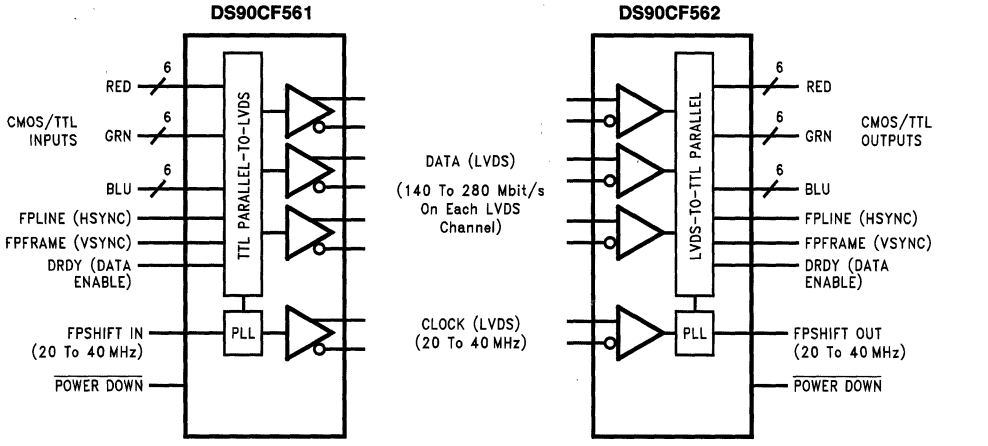
The DS90CF561 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CF562 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 105 Megabytes per second. These devices are offered with falling edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 105 Megabyte/sec bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power down mode
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Falling edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



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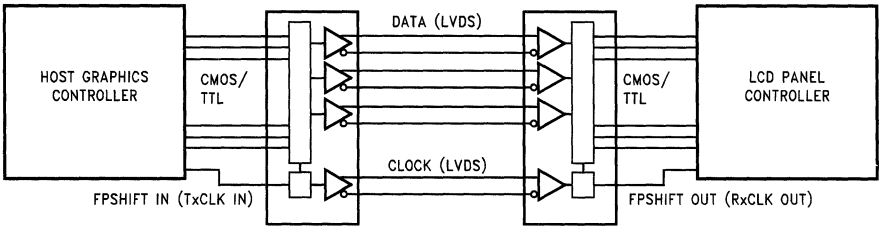
Order Number DS90CF561MTD
See NS Package Number MTD48

Order Number DS90CF562MTD
See NS Package Number MTD48

Application



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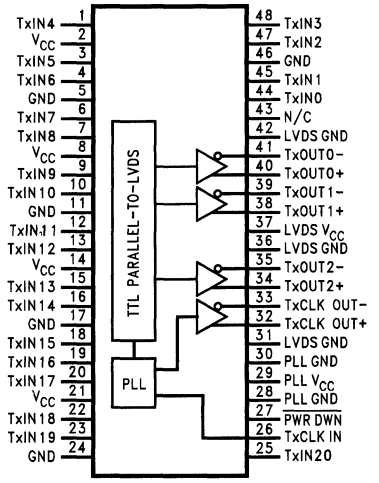
Connection Diagrams

DS90CF561



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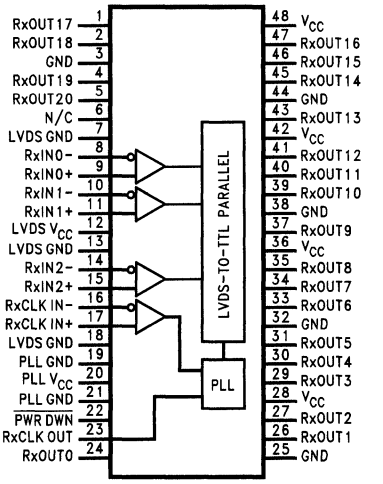
DS90CF562



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Ouput Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C

Maximum Power Dissipation @ +25°C

MTD48 (TSSOP) Package:	
DS90CF561	1.98W
DS90CF562	1.89W
Package Derating: DS90CF561	16 mW/°C above +25°C
DS90CF562	15 mW/°C above +25°C

This device does not meet 2000V ESD rating (Note 4).

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complimentary Output States					35	V
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	Tx Sub-Symbol Pulse Width *(Figure 6)*	f = 20 MHz	5.5	7	8	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		25	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*		8			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		25	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Continued)

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 20 MHz	16			ns
		f = 40 MHz	6.5			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

AC Timing Diagrams

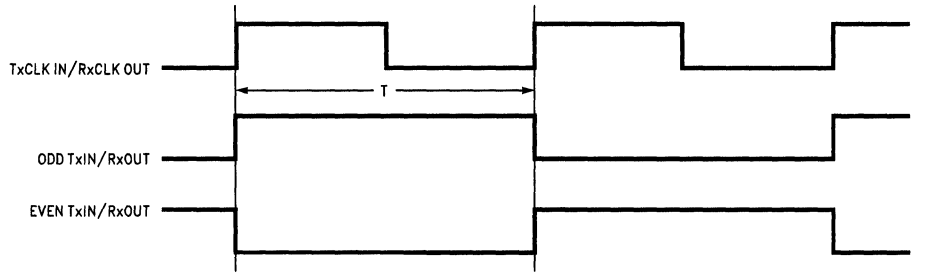

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FIGURE 1. "Worst Case" Test Pattern

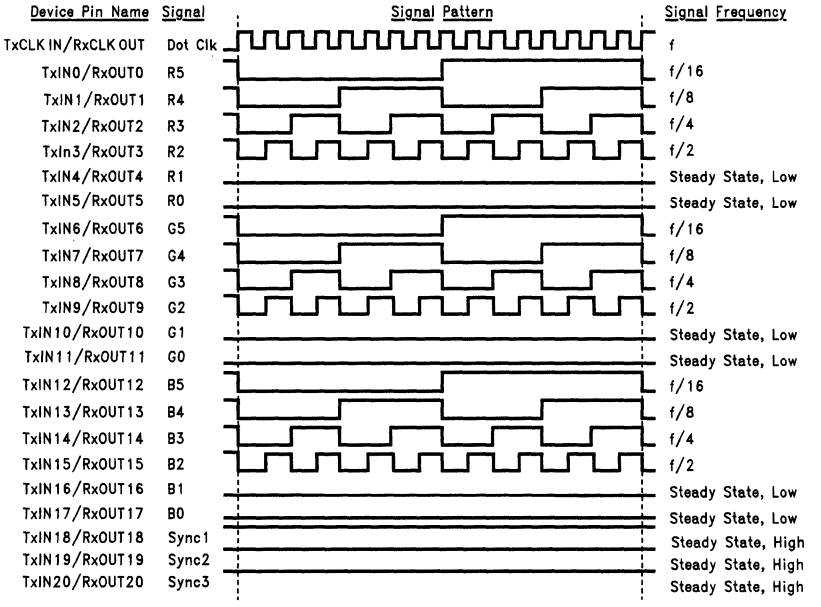

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FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of device digital circuitry, LVDS I/O and TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

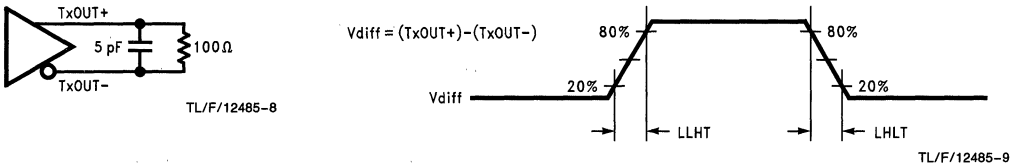


FIGURE 3. DS90CF561 (Transmitter) LVDS Output Load and Transition Timing

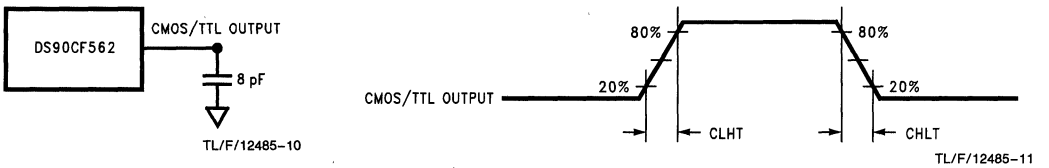


FIGURE 4. DS90CF562 (Receiver) CMOS/TTL Output Load and Transition Timing

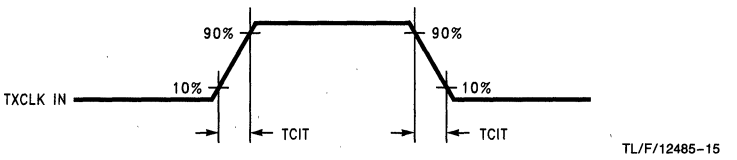
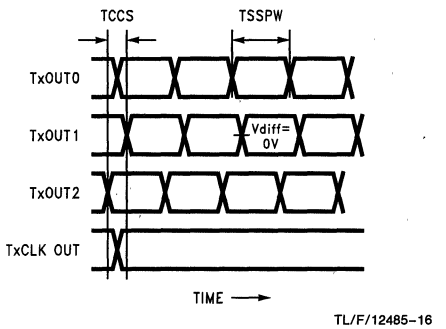


FIGURE 5. DS90CF561 (Transmitter) Input Clock Transition Time



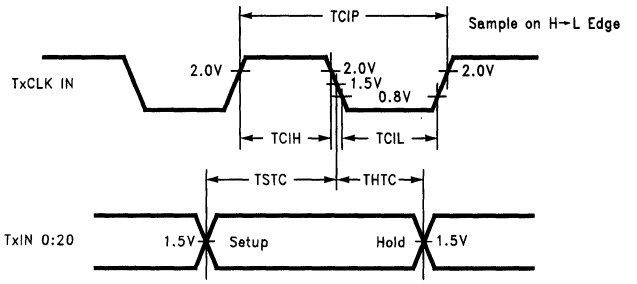
Note 1: Measurements at Vdiff = 0V

Note 2: TCCS measured between earliest and latest initial LVDS edges.

Note 3: TxCLK OUT Differential High → Low Edge for DS90CF561
TxCLK OUT Differential Low → High Edge for DS90CR561

FIGURE 6. DS90CF561 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)



TL/F/12485–12

FIGURE 7. DS90CF561 (Transmitter) Setup/Hold and High/Low Times

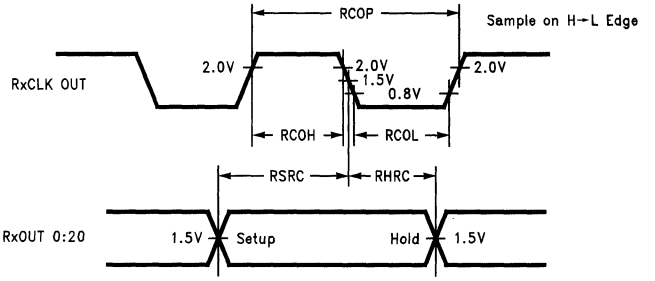


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FIGURE 8. DS90CF562 (Receiver) Setup/Hold and High/Low Times

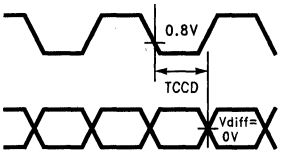

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FIGURE 9. DS90CF561 (Transmitter) Clock In to Clock Out Delay

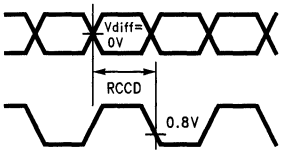

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FIGURE 10. DS90CF562 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

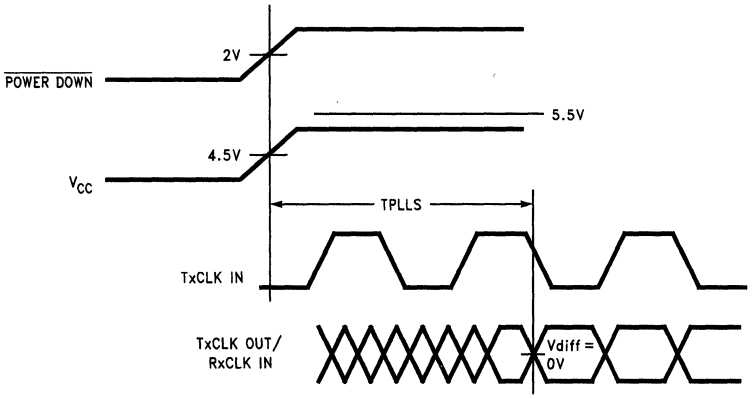

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FIGURE 11. DS90CF561 (Transmitter) Phase Lock Loop Set Time

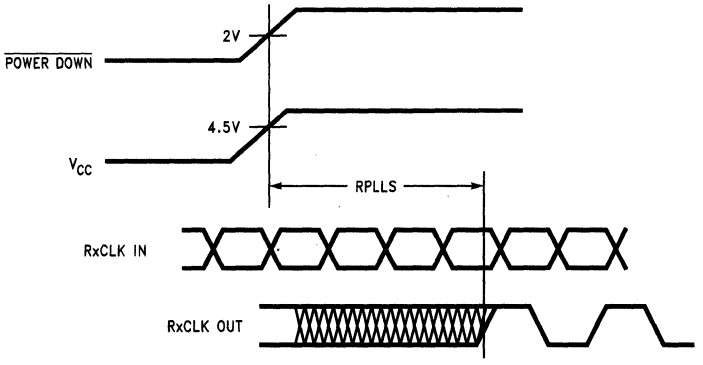

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FIGURE 12. DS90CF562 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

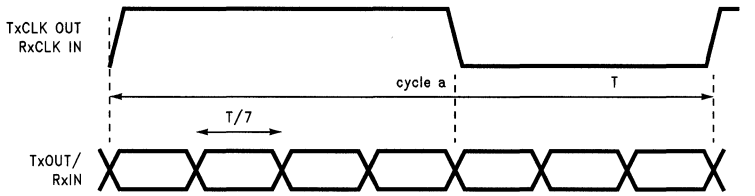

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FIGURE 13. Seven Bits of LVDS in One Clock Cycle

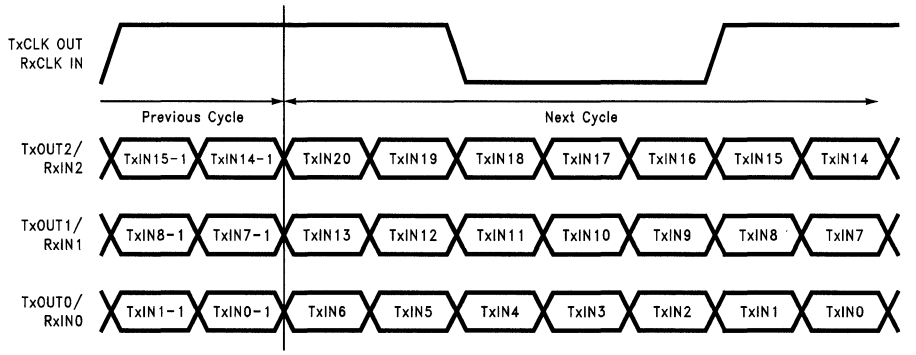

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FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF561)

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DS90CF561 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY). (Also referred to as HSYNC, VSYNC and DATA ENABLE.)
TxOUT+	O	3	Positive LVDS differential data output
TxOUT−	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CF562 Pin Description—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN−	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY). (Also referred to as HSYNC, VSYNC and DATA ENABLE.)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

National Semiconductor

DS90CR581/DS90CR582
LVDS 24-Bit Color Flat Panel Display (FPD) Link

General Description

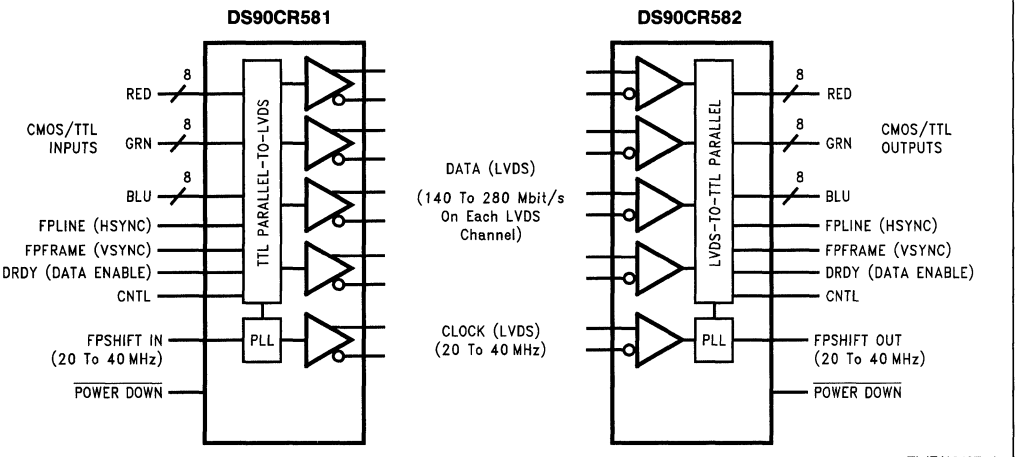
The DS90C581 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90C582 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CNTL) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second.

The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 140 Megabyte/sec Bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



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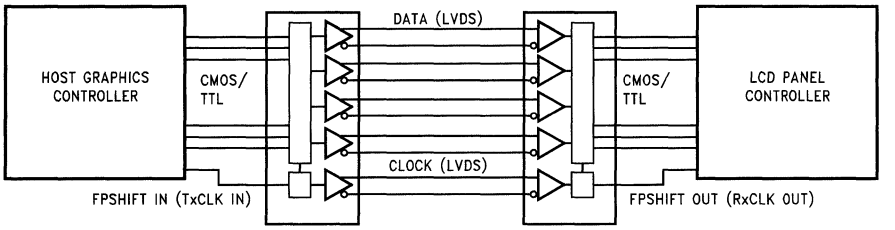
Order Number DS90CR581MTD
See NS Package Number MTD56

Order Number DS90CR582MTD
See NS Package Number MTD56

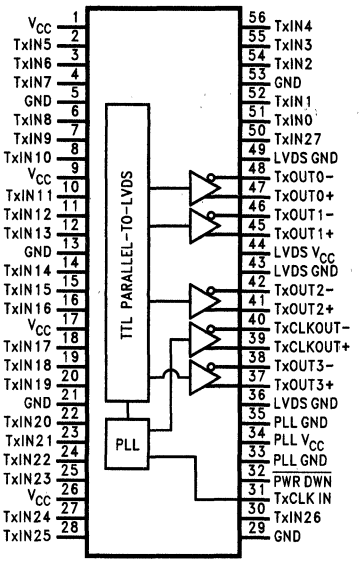
Application



TL/F/12487–2

Connection Diagrams

DS90CR581



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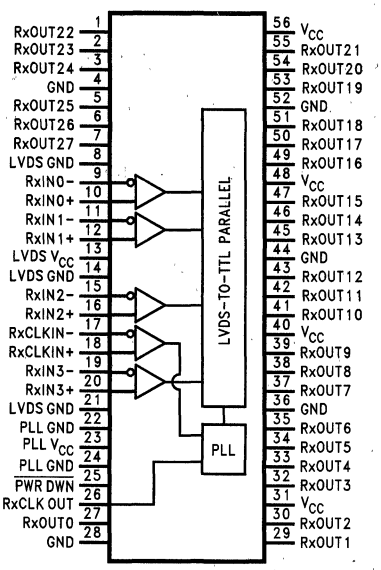
DS90CR582



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3 to +6V
CMOS/TTL Input Voltage	−0.3 to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C

Maximum Package Power Dissipation @ +25°C

MTD56 (TSSOP) Package: DS90CR581	1.63W
DS90CR582	1.61W
Package Derating: DS90CR581	12.5 mW/°C above +25°C
DS90CR582	12.4 mW/°C above +25°C

This device does not meet 2000V ESD rating. (Note 4)

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complimentary Output States					35	mV
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew *(Note A) (Figure 6)*				350	ps
TSSPW	Tx Sub-Symbol Pulse Width *(Figure 6)*	f = 20 MHz	5.5	7	8	ns
RCCS	RxIN Channel-to-Channel Skew *(Note B)*				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		25	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*		8			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		25	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Continued)

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 20 MHz	16			ns
		f = 40 MHz	6.5			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

5

AC Timing Diagrams

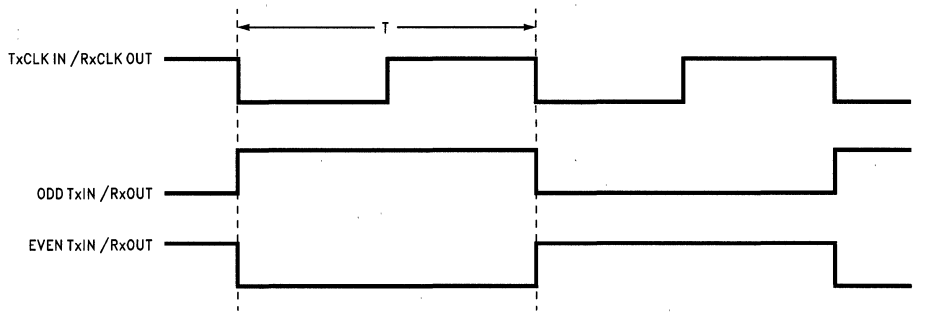

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FIGURE 1. "Worst Case" Test Pattern

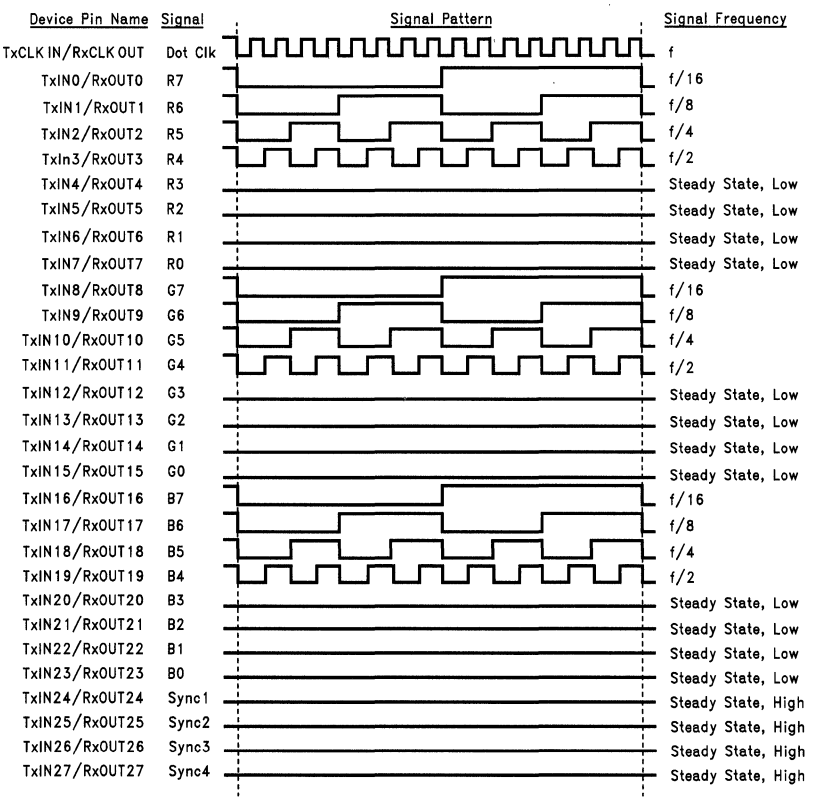

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FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *2* show a rising edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

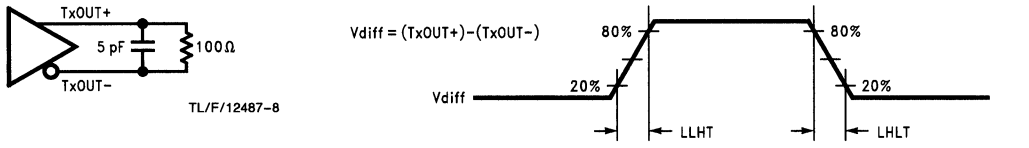


FIGURE 3. DS90CR581 (Transmitter) LVDS Output Load and Transition Timing

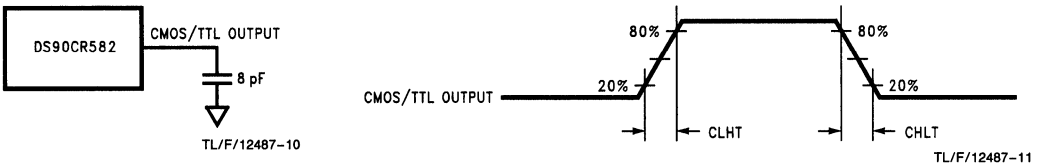


FIGURE 4. DS90CR582 (Receiver) CMOS/TTL Output Load and Transition Timing

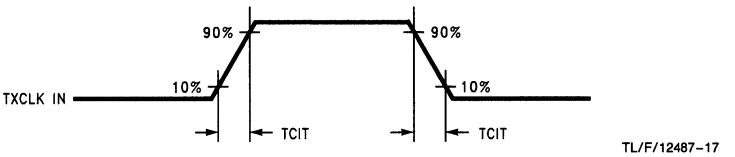
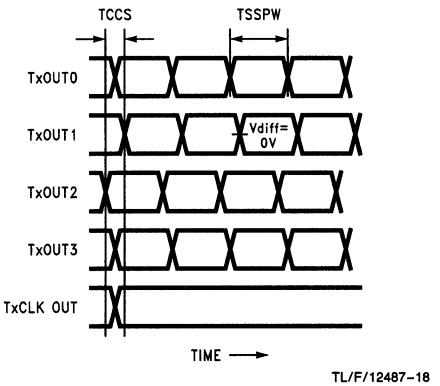


FIGURE 5. DS90CR581 (Transmitter) Input Clock Transition Time



Note 1: Measurements at V_{diff} = 0V

Note 2: TCCS measured between earliest and latest initial LVDS edges.

Note 3: TxCLK OUT Differential High → Low Edge for DS90CF561
TxCLK OUT Differential Low → High Edge for DS90CR561

FIGURE 6. DS90CR581 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

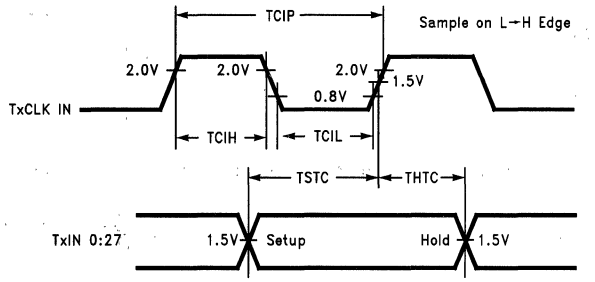


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FIGURE 7. DS90CR581 (Transmitter) Setup/Hold and High/Low Times

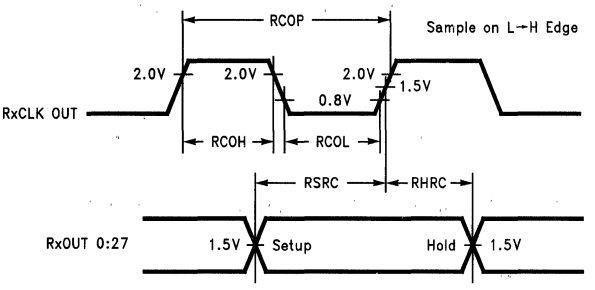

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FIGURE 8. DS90CR582 (Receiver) Setup/Hold and High/Low Times

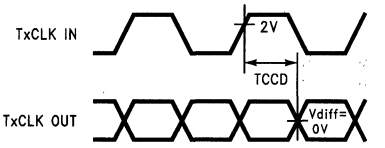

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FIGURE 9. DS90CR581 (Transmitter) Clock In to Clock Out Delay

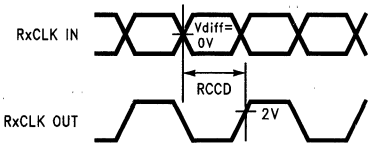

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FIGURE 10. DS90CR582 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

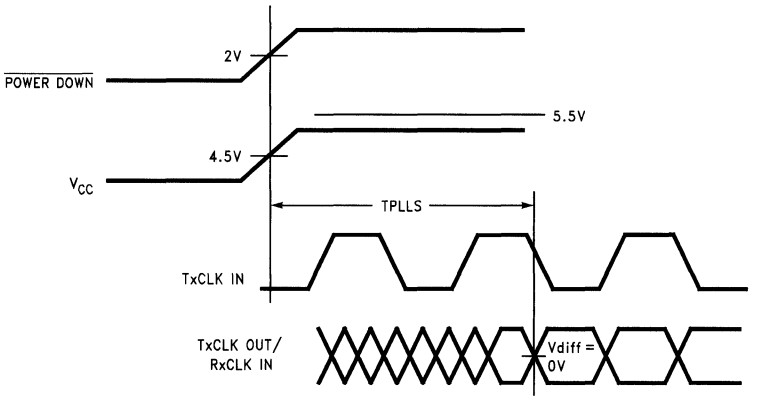

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FIGURE 11. DS90CR581 (Transmitter) Phase Lock Loop Set Time

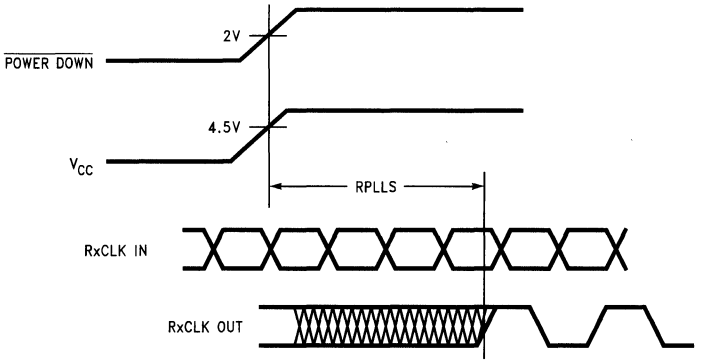

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FIGURE 12. DS90CR582 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

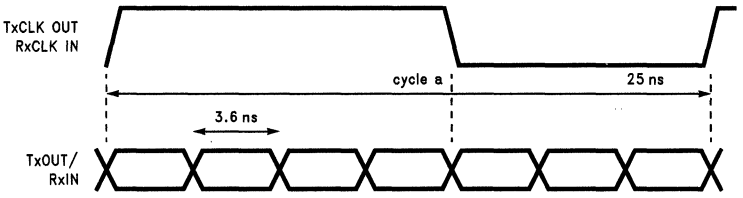

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FIGURE 13. Seven Bits of LVDS in One Clock Cycle

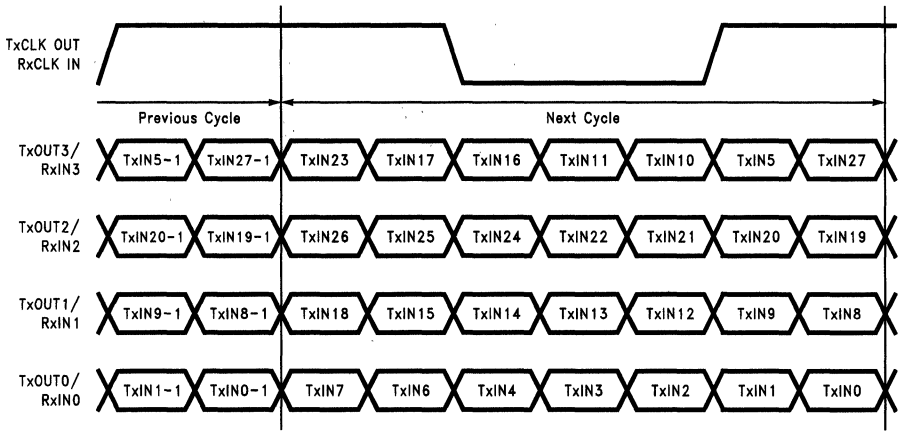

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FIGURE 14. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR581)

DS90CR581 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL Level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR582 Pin Description—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs
RxIN−	I	4	Negative LVDS differential data inputs
RxOUT	O	28	TTL Level outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The rising edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

National Semiconductor

DS90CF581/DS90CF582
LVDS 24-Bit Color Flat Panel Display (FPD) Link

General Description

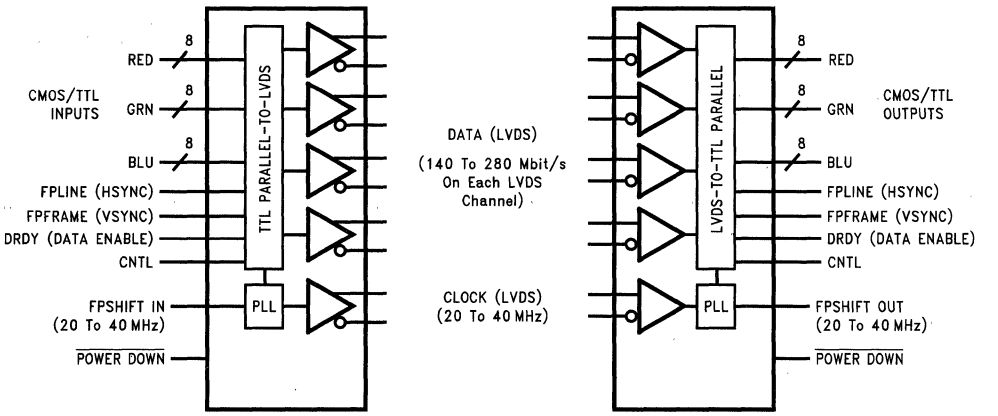
The DS90CF581 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CF582 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CNTL) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second. The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 140 Megabyte/sec Bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Falling edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams

DS90CF581 **DS90CF582**



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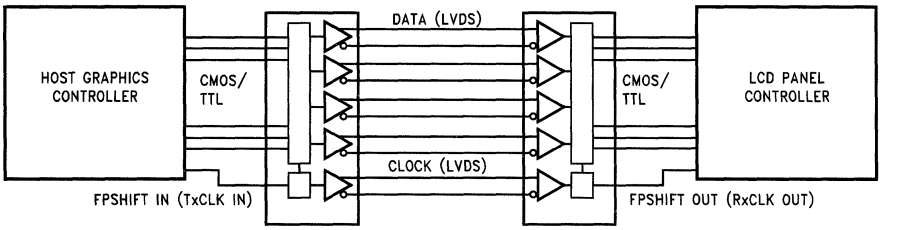
Order Number DS90CF581MTD
See NS Package Number MTD56

Order Number DS90CF582MTD
See NS Package Number MTD56

Application



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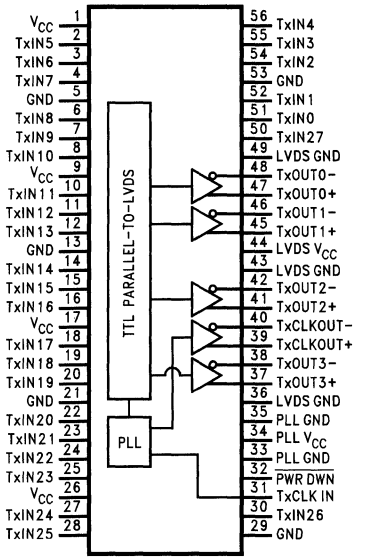
Connection Diagrams

DS90CF581



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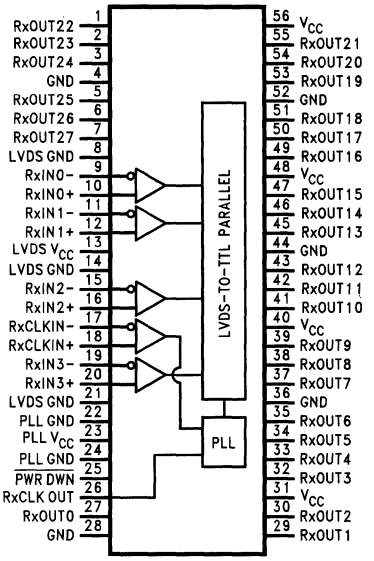
DS90CF582



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3 to +6V
CMOS/TTL Input Voltage	−0.3 to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3 to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	continuous
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	+260°C

Maximum Package Power Dissipation @ +25°C

MTD56 (TSSOP) Package:	DS90CF581	1.63W
	DS90CF582	1.61W
Derate Package:	DS90CF581	12.5 mW/°C above +25°C
	DS90CF582	12.4 mW/°C above +25°C

This device does not meet 2000V ESD rating. (Note 4)

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complimentary Output States					35	mV
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	Tx Sub-Symbol Pulse Width *(Figure 6)*	f = 20 MHz	5.5	7	8	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		25	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*		8			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		25	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified (Continued)

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 20 MHz	21.5			ns
		f = 40 MHz	10.5			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 20 MHz	19			ns
		f = 40 MHz	6			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 20 MHz	14			ns
		f = 40 MHz	4.5			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 20 MHz	16			ns
		f = 40 MHz	6.5			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

AC Timing Diagrams

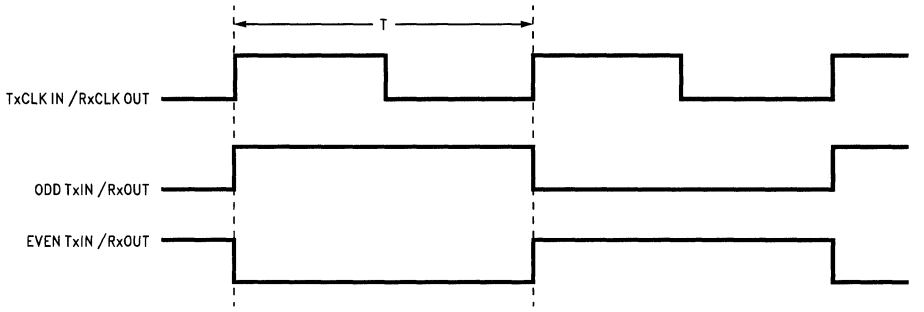

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FIGURE 1. "WORST CASE" Test Pattern

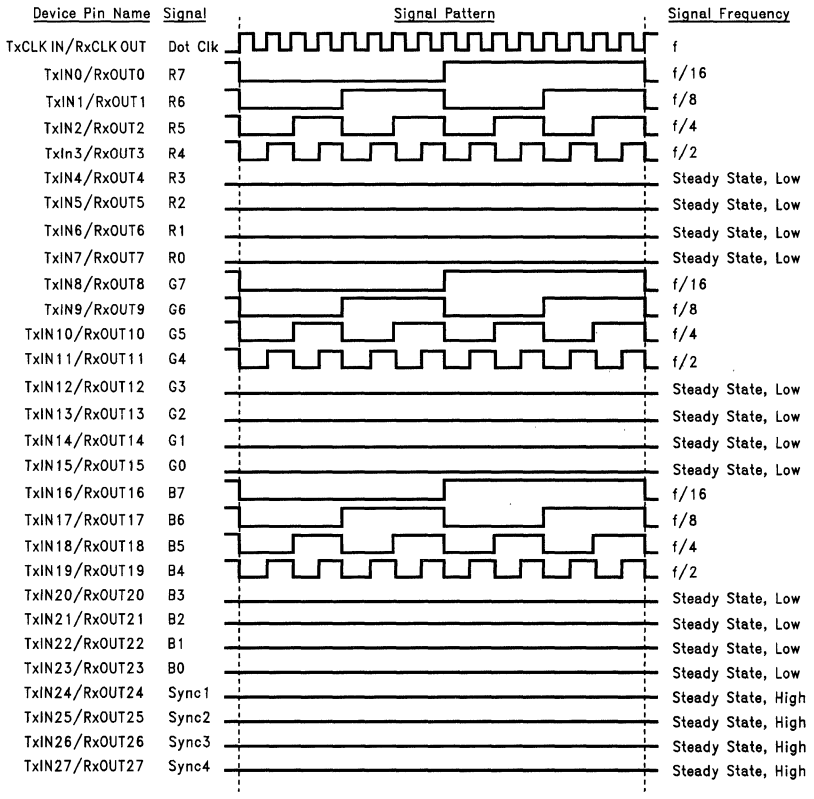

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FIGURE 2. "16 GRAYSCALE" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

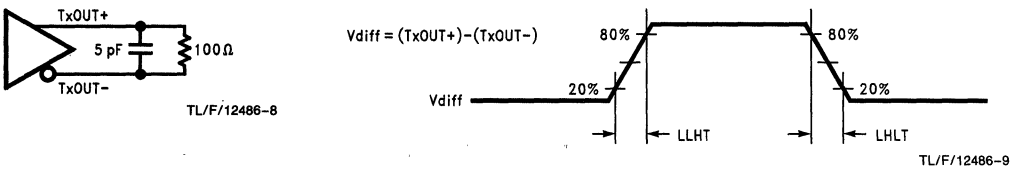


FIGURE 3. DS90CF581 (Transmitter) LVDS Output Load and Transition Timing

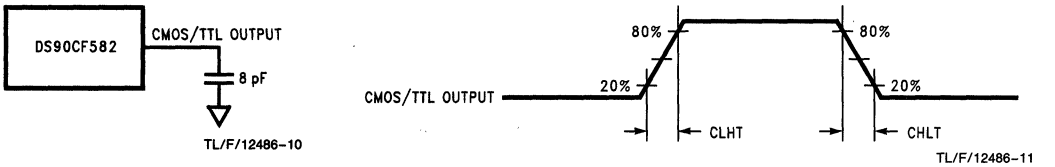


FIGURE 4. DS90CF582 (Receiver) CMOS/TTL Output Load and Transition Timing

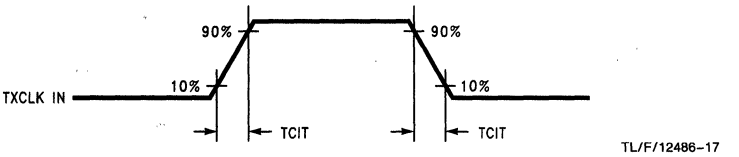
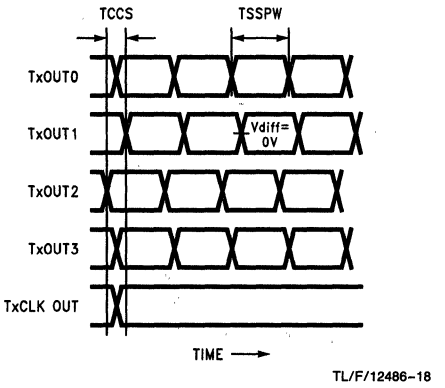


FIGURE 5. DS90CF581 (Transmitter) Input Clock Transition Time



Note 1: Measurements at V_{diff} = 0V

Note 2: TCCS measured between earliest and latest initial LVDS edges.

Note 3: TxCLK OUT Differential High → Low Edge for DS90CF561
TxCLK OUT Differential Low → High Edge for DS90CR561

FIGURE 6. DS90CF581 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

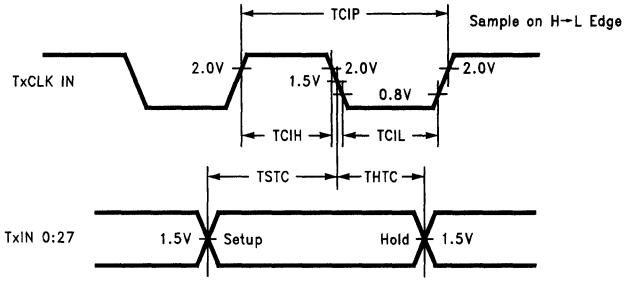


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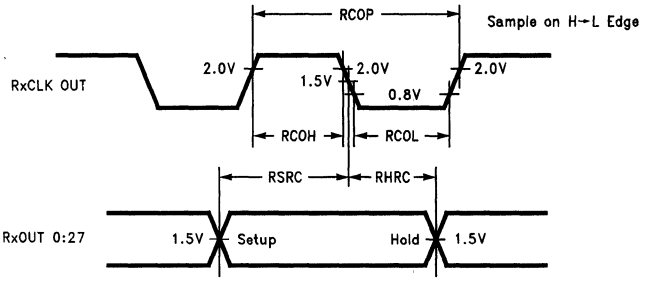
FIGURE 7. DS90CF581 (Transmitter) Setup/Hold and High/Low Times



TL/F/12486–13

FIGURE 8. DS90CF582 (Receiver) Setup/Hold and High/Low Times

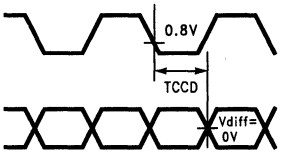


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FIGURE 9. DS90CF581 (Transmitter) Clock In to Clock Out Delay

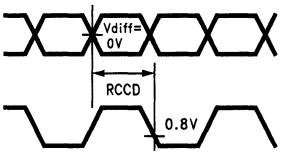

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FIGURE 10. DS90CF582 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

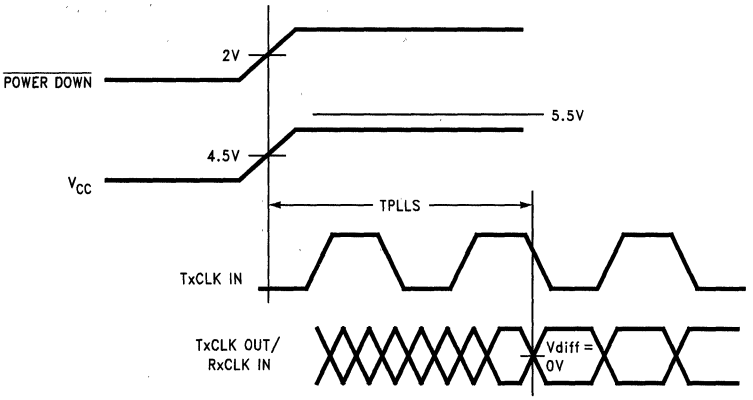

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FIGURE 11. DS90CF581 (Transmitter) Phase Lock Loop Set Time

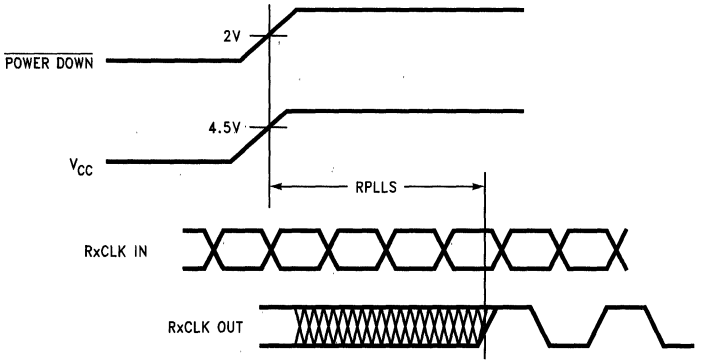

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FIGURE 12. DS90CF582 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

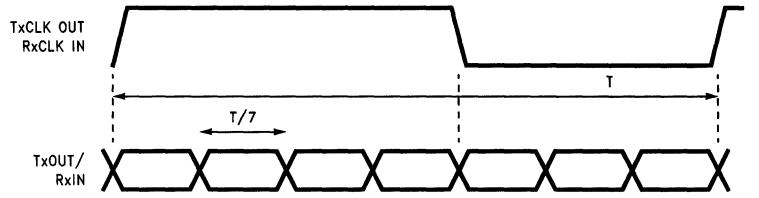

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FIGURE 13. Seven Bits of LVDS In One Block Cycle

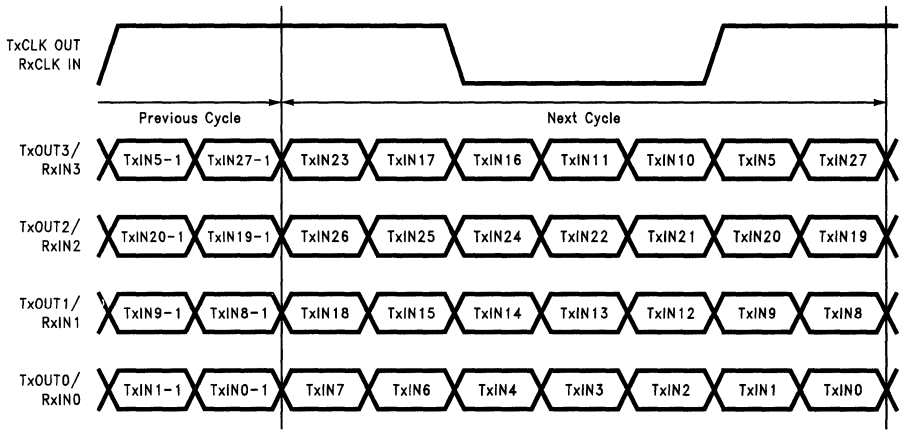

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FIGURE 14. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF581)

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DS90CF581 Pin Description—FPD Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe.
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATE the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CF582 Pin Description—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATE the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

National Semiconductor

PRELIMINARY

DS90CR563/DS90CR564
LVDS 18-Bit Color Flat Panel Display (FPD) Link—65 MHz

General Description

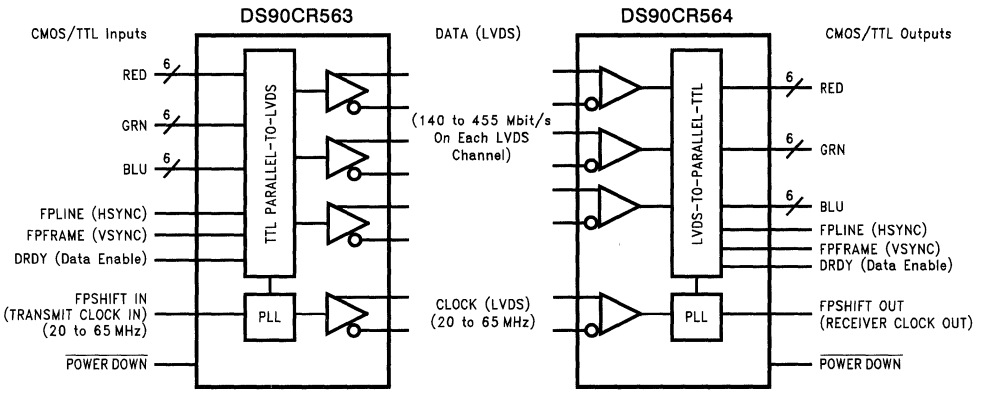
The DS90CR563 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR564 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 171 Mbytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 171 Mbytes/s bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



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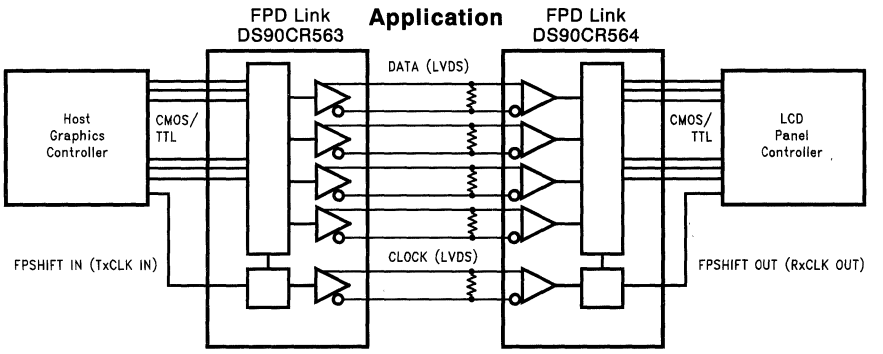
Order Number DS90CR563MTD
See NS Package Number MTD48

Order Number DS90CR564MTD
See NS Package Number MTD48



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C

Maximum Power Dissipation @ 25°C
MTD48 (TSSOP) Package:

DS90CR563	TBD W
DS90CR564	TBD W

Package Derating:

DS90CR563	TBD W/°C above +25°C
DS90CR564	TBD W/°C above +25°C

This device does not meet 2000V ESD rating (Note 4).

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	mV
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	TxSub-Symbol Pulse Width *(Figure 6)*	f = 65 MHz	1.7	2.1	2.5	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		15	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*	f = 65 MHz	TBD			ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		15	T	50	ns
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 65 MHz	TBD			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 65 MHz	TBD			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

AC Timing Diagrams

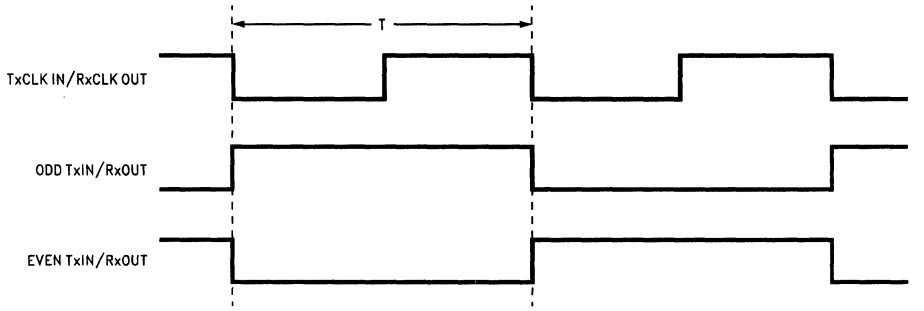

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FIGURE 1. "Worst Case" Test Pattern

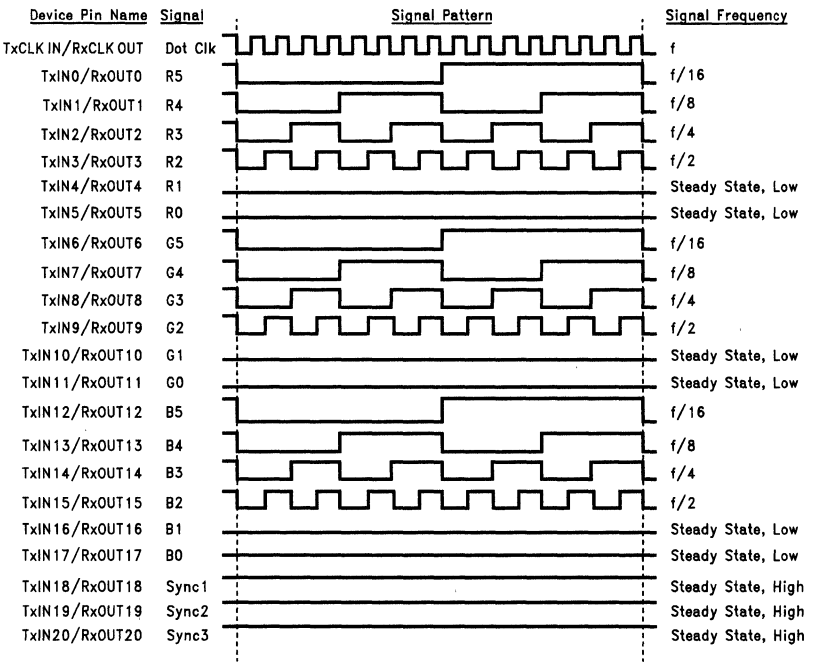

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FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a rising edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

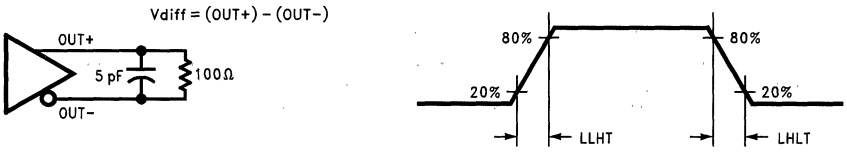

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FIGURE 3. DS90CR563 (Transmitter) LVDS Output Load and Transition Times

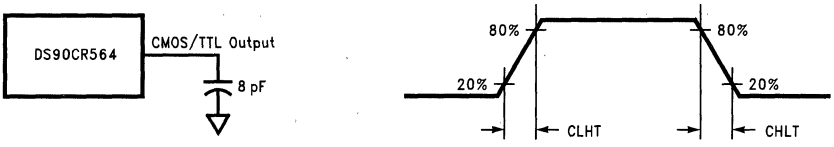

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FIGURE 4. DS90CR564 (Receiver) CMOS/TTL Output Load and Transition Times

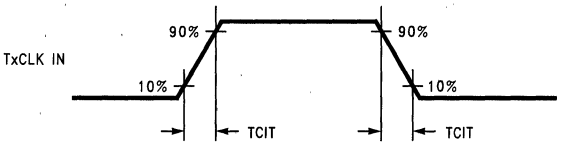

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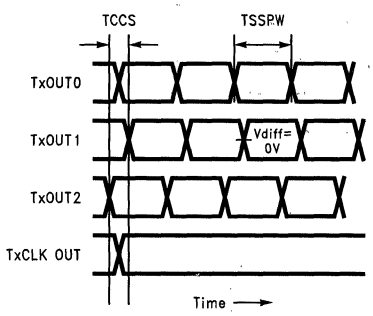
FIGURE 5. DS90CR563 (Transmitter) Input Clock Transition Time



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Note 1: Measurements at Vdiff = 0V

Note 2: TCSS measured between earliest and latest LVDS edges.

Note 3: TxCLK Differential Low → High Edge

FIGURE 6. DS90CR563 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

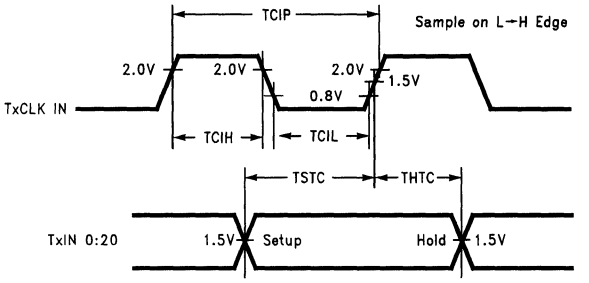

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FIGURE 7. DS90CR563 (Transmitter) Setup/Hold and High/Low Times

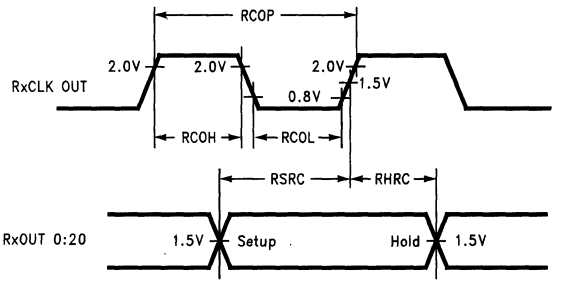

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FIGURE 8. DS90CR564 (Receiver) Setup/Hold and High/Low Times

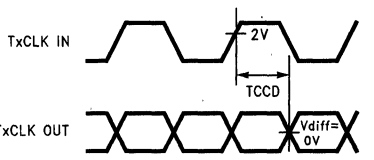

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FIGURE 9. DS90CR563 (Transmitter) Clock In to Clock Out Delay

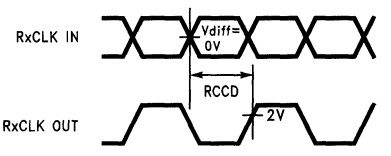

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FIGURE 10. DS90CR564 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

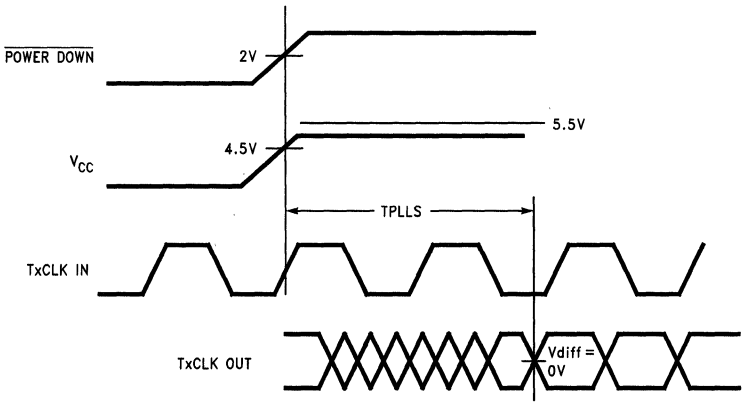

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FIGURE 11. DS90CR563 (Transmitter) Phase Lock Loop Set Time

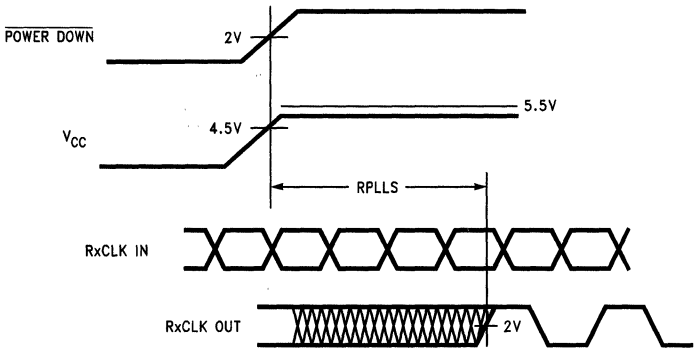

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FIGURE 12. DS90CR564 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

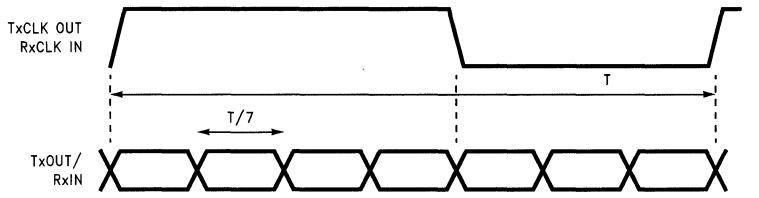

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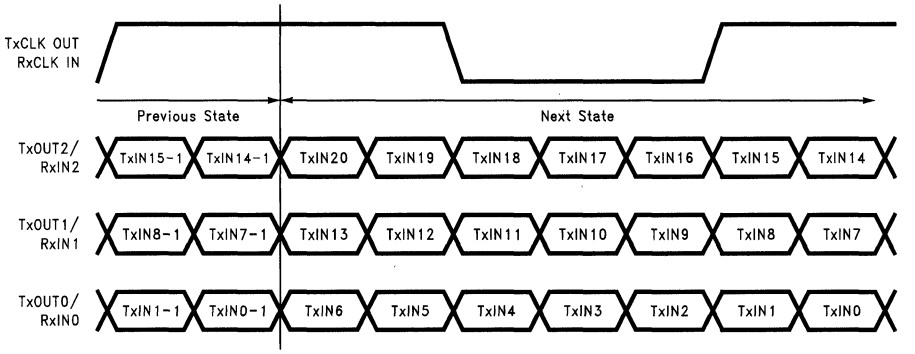
FIGURE 13. Seven Bits of LVDS in One Clock Cycle



TL/F/12617–18

FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS (DS90CR563)

5

DS90CR563 Pin Descriptions—FPD Link Transmitter

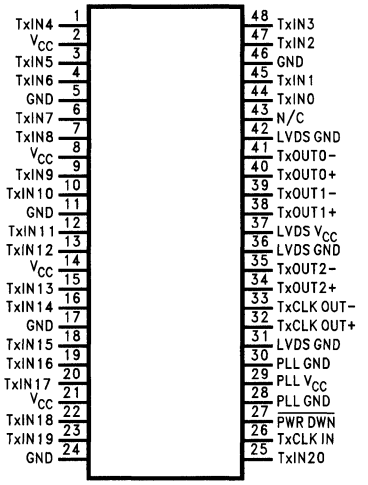
Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY) (also referred to as HSYNC, VSYNC, Data Enable)
TxOUT+	O	3	Positive LVDS differential data output
TxOUT−	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR564 Pin Descriptions—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN−	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines (FPLINE, FPFRAME, DRDY) (also referred to as HSYNC, VSYNC, Data Enable)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The rising edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

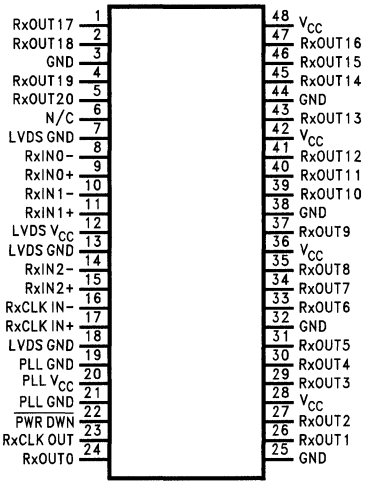
Connection Diagrams

DS90CR563



TL/F/12617–15

DS90CR564



TL/F/12617–16

5

National Semiconductor

PRELIMINARY

DS90CF563/DS90CF564
LVDS 18-Bit Color Flat Panel Display (FPD) Link—65 MHz

General Description

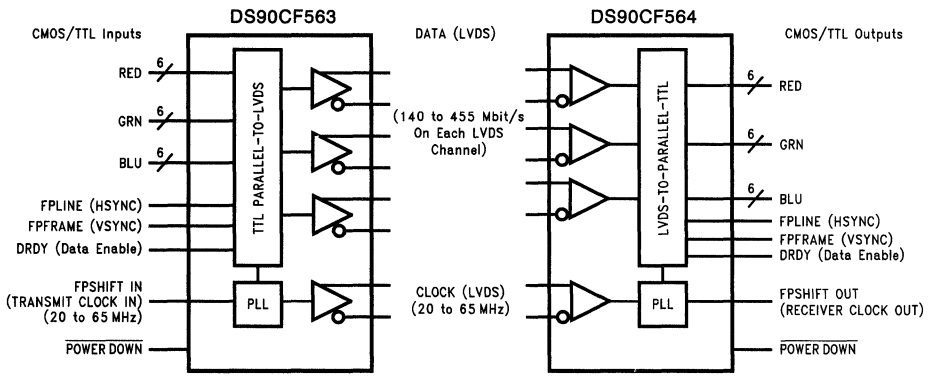
The DS90CF563 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CF564 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 18 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 171 Mbytes per second. These devices are offered with falling edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 171 Mbytes/s bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Falling edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

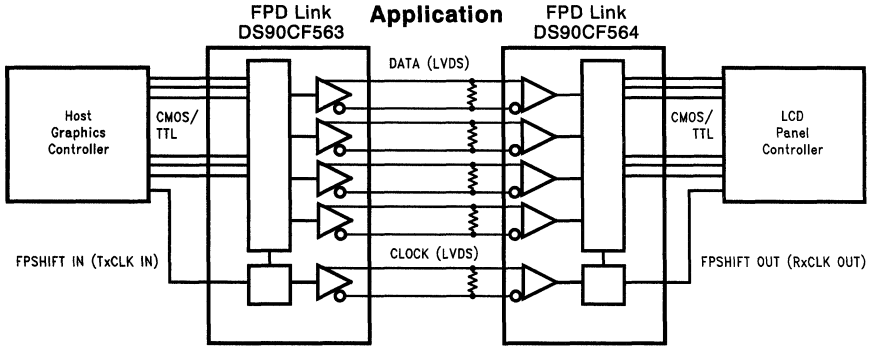
Block Diagrams



TL/F/12615–1

Order Number DS90CF563MTD
See NS Package Number MTD48

Order Number DS90CF564MTD
See NS Package Number MTD48



TL/F/12615–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C

Maximum Power Dissipation @ 25°C

MTD48 (TSSOP) Package:	
DS90CF563	TBD W
DS90CF564	TBD W
Package Derating:	
DS90CF563	TBD W/°C above +25°C
DS90CF564	TBD W/°C above +25°C

This device does not meet 2000V ESD rating (Note 4)

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	mV
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	μA
		V_{IN} = 0V				±10	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CLHT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	TxSub-Symbol Pulse Width *(Figure 6)*	f = 65 MHz	1.7	2.1	2.5	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		15	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*	f = 65 MHz	TBD			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		15	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 65 MHz	TBD			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 65 MHz	TBD			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

AC Timing Diagrams

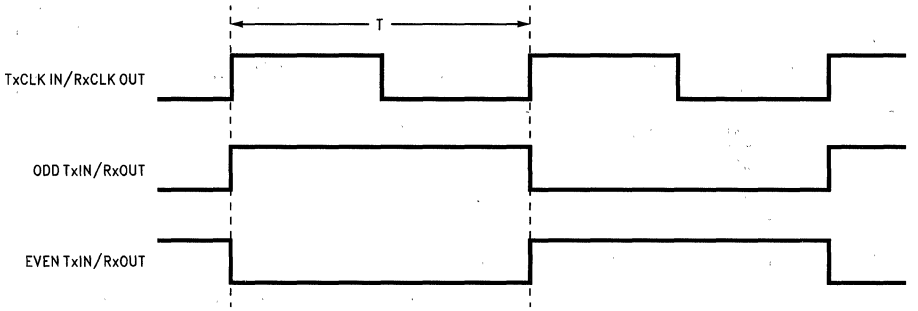


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FIGURE 1. "Worst Case" Test Pattern

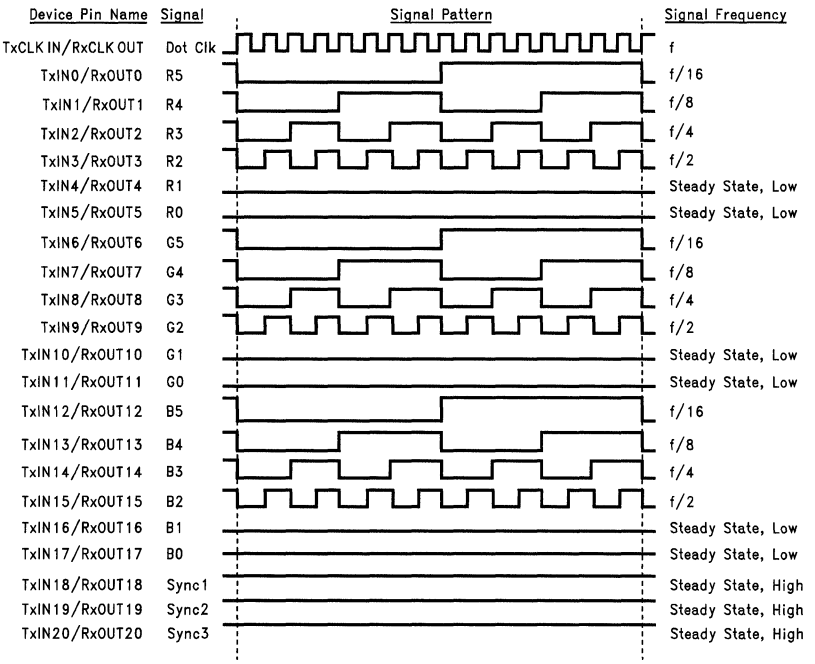

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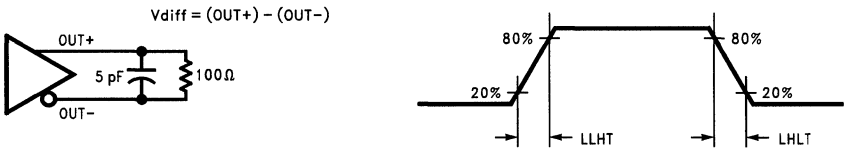
FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)



TL/F/12615–5

FIGURE 3. DS90CF563 (Transmitter) LVDS Output Load and Transition Times

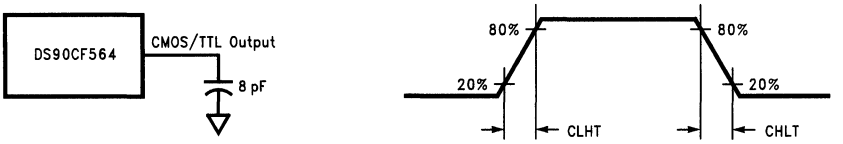


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FIGURE 4. DS90CF564 (Receiver) CMOS/TTL Output Load and Transition Times

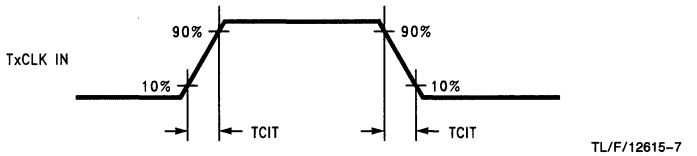

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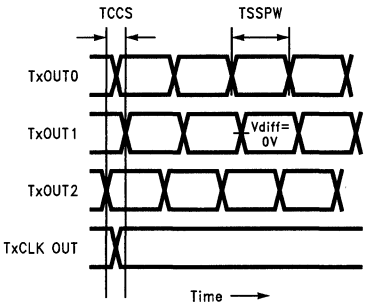
FIGURE 5. DS90CF563 (Transmitter) Input Clock Transition Time



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Note 1: Measurements at Vdiff = 0V
Note 2: TCSS measured between earliest and latest LVDS edges.
Note 3: TxCLK Differential High → Low Edge

FIGURE 6. DS90CF563 (Transmitter) Channel-to-Channel Skew and Pulse Width

5

AC Timing Diagrams (Continued)

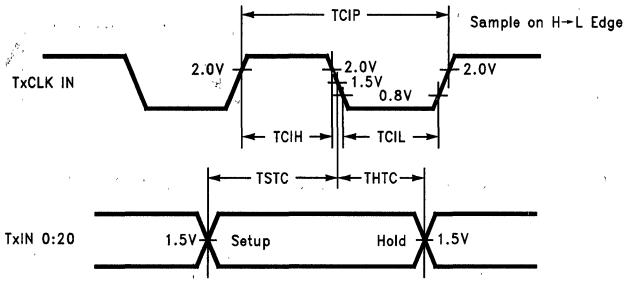

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FIGURE 7. DS90CF563 (Transmitter) Setup/Hold and High/Low Times

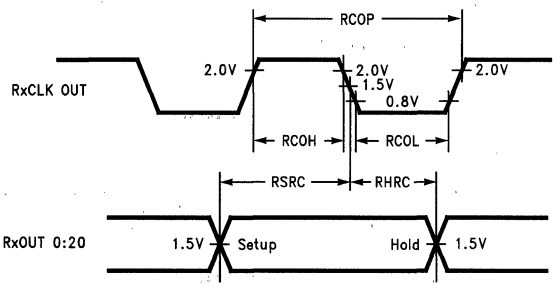

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FIGURE 8. DS90CF564 (Receiver) Setup/Hold and High/Low Times

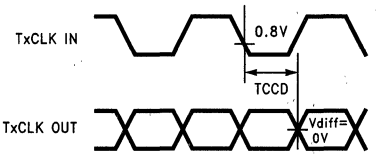

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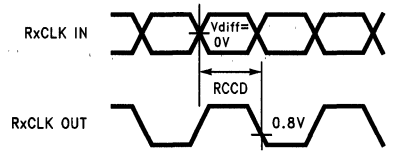
FIGURE 9. DS90CF563 (Transmitter) Clock In to Clock Out Delay



TL/F/12615–12

FIGURE 10. DS90CF564 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

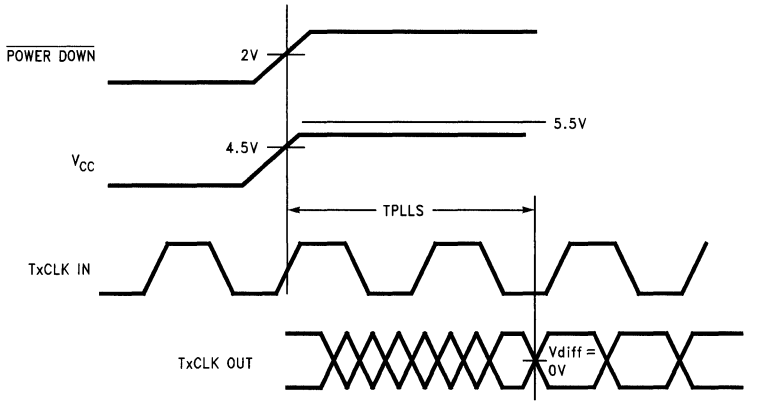


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FIGURE 11. DS90CF563 (Transmitter) Phase Lock Loop Set Time

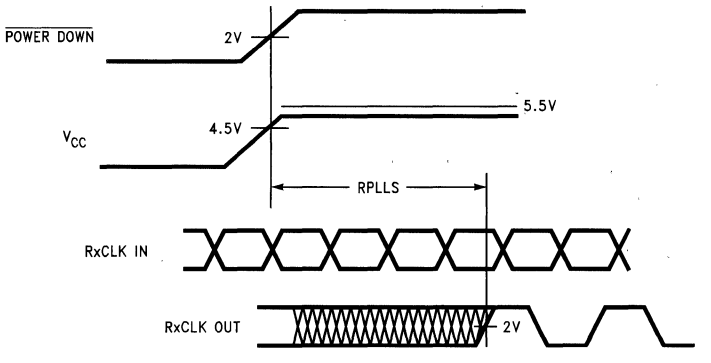

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FIGURE 12. DS90CF564 (Receiver) Phase Lock Loop Set Time

5

AC Timing Diagrams (Continued)

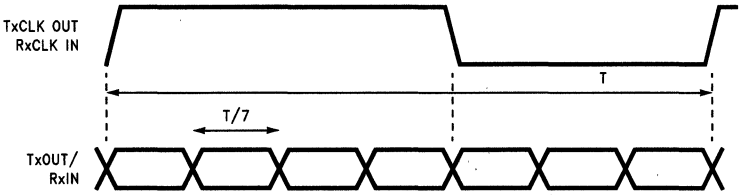

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FIGURE 13. Seven Bits of LVDS in One Clock Cycle

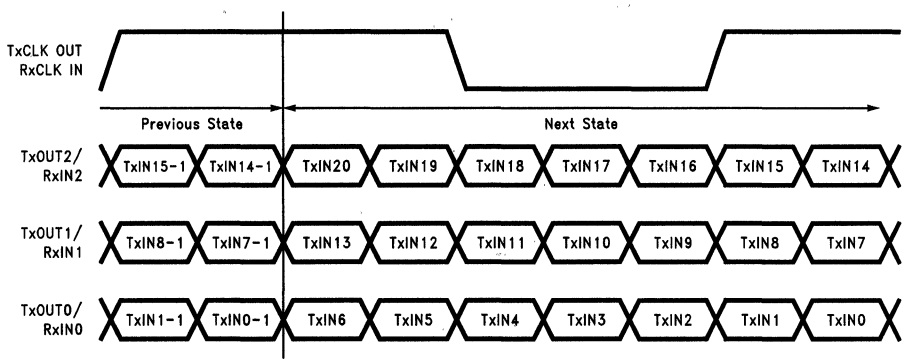

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FIGURE 14. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF563)

DS90CF563 Pin Description FPD Link Transmitter

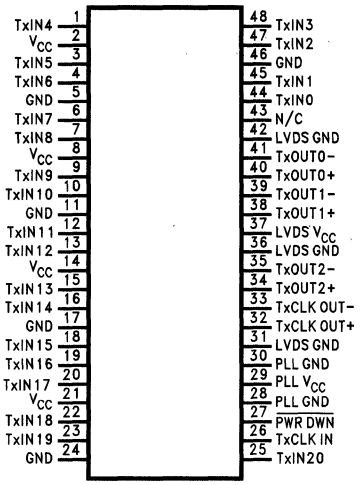
Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable)
TxOUT+	O		Positive LVDS differential data output
TxOUT−	O	3	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The falling edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CF564 Pin Description FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs
RxIN−	I	3	Negative LVDS differential data inputs
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

Connection Diagrams

DS90CF563



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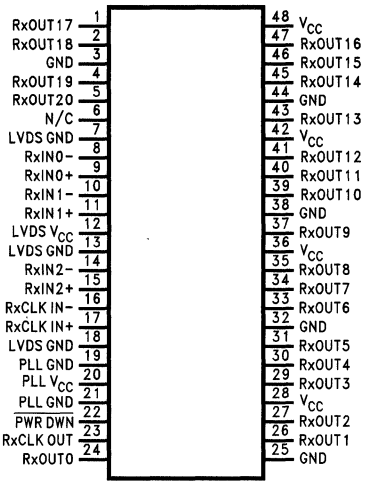
DS90CF564



TL/F/12615–16

National Semiconductor

PRELIMINARY

DS90CR583/DS90CR584
LVDS 24-Bit Color Flat Panel Display (FPD) Link—65 MHz

General Description

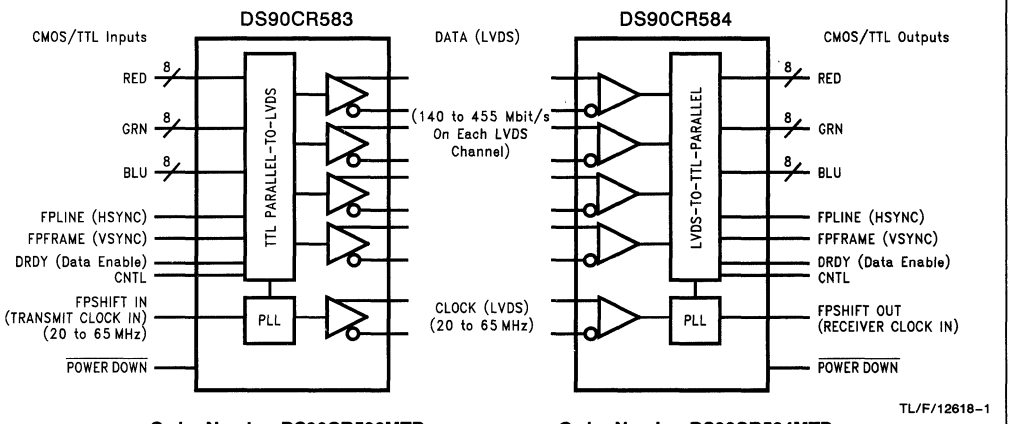
The DS90CR583 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR584 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CONTROL) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes per second. These devices are offered with rising edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 227 Mbytes/s bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



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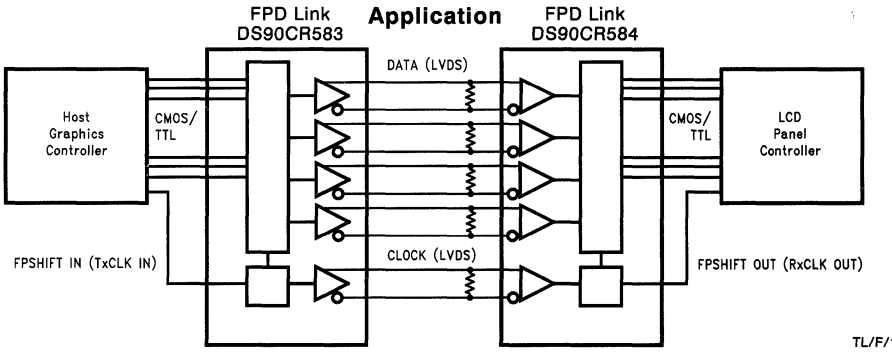
Order Number DS90CR583MTD
See NS Package Number MTD56

Order Number DS90CR584MTD
See NS Package Number MTD56



TL/F/12618-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C

Maximum Power Dissipation @ 25°C
MTD56 (TSSOP) Package:

DS90CR583	TBD W
DS90CR584	TBD W

Package Derating:

DS90CR583	TBD W/°C above +25°C
DS90CR584	TBD W/°C above +25°C

This device does not meet 2000V ESD rating (Note 4)

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	mV
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	µA
		V_{IN} = 0V				±10	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	TxSub-Symbol Pulse Width *(Figure 6)*	f = 65 MHz	1.7	2.1	2.5	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		15	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*	f = 65 MHz	TBD			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		15	T	50	ns

Note A: This limit based on bench characterization.

Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 65 MHz	TBD			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 65 MHz	TBD			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

AC Timing Diagrams

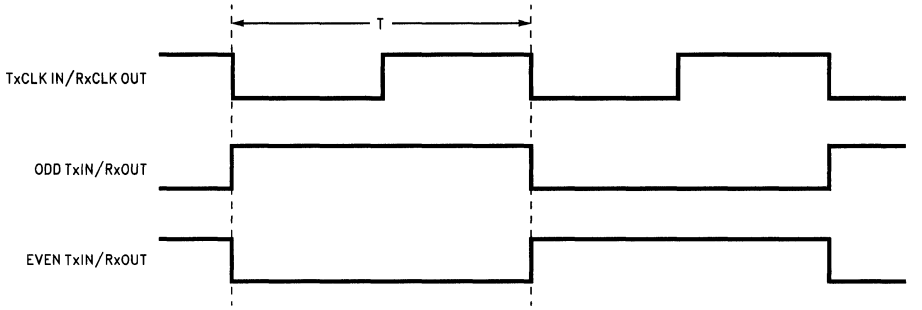


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FIGURE 1. "Worst Case" Test Pattern

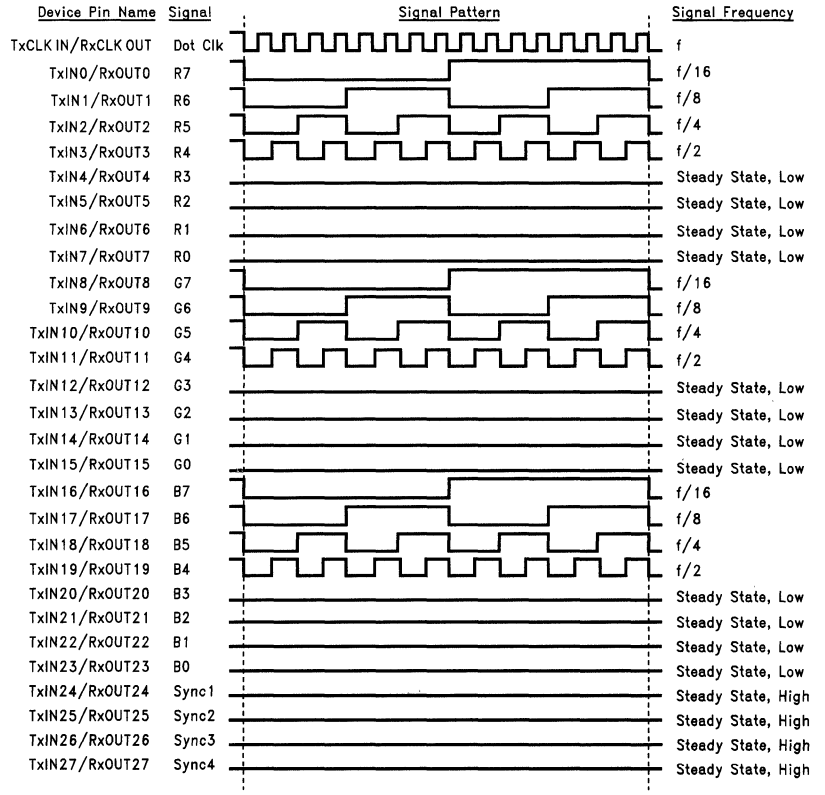

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FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a rising edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

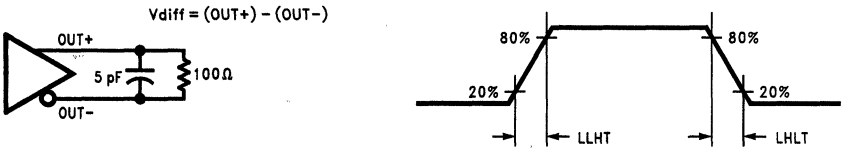

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FIGURE 3. DS90CR583 (Transmitter) LVDS Output Load and Transition Times

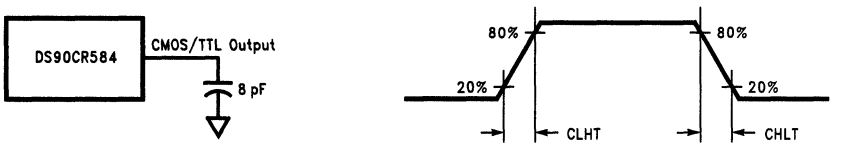

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FIGURE 4. DS90CR584 (Receiver) CMOS/TTL Output Load and Transition Times

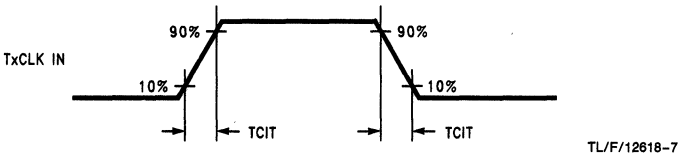

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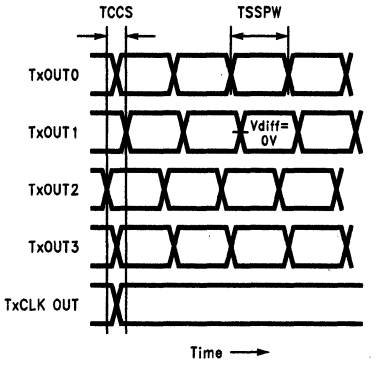
FIGURE 5. DS90CR583 (Transmitter) Input Clock Transition Time



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Note 1: Measurements at Vdiff = 0V
Note 2: TCSS measured between earliest and latest LVDS edges.
Note 3: TxCLK Differential Low → High Edge

FIGURE 6. DS90CR583 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

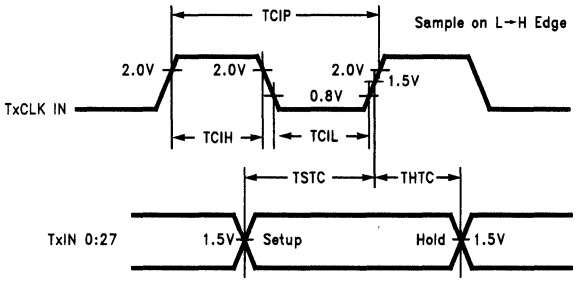

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FIGURE 7. DS90CR583 (Transmitter) Setup/Hold and High/Low Times

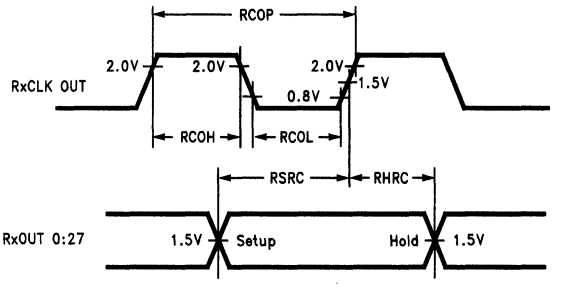

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FIGURE 8. DS90CR584 (Receiver) Setup/Hold and High/Low Times

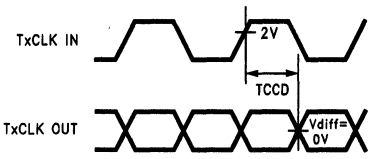

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FIGURE 9. DS90CR583 (Transmitter) Clock In to Clock Out Delay

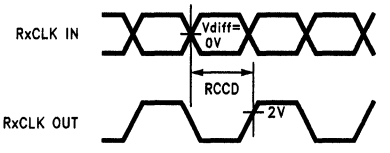

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FIGURE 10. DS90CR584 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

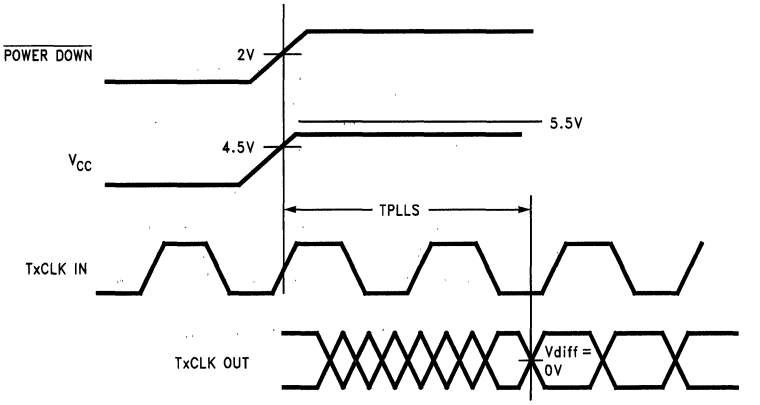

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FIGURE 11. DS90CR583 (Transmitter) Phase Lock Loop Set Time

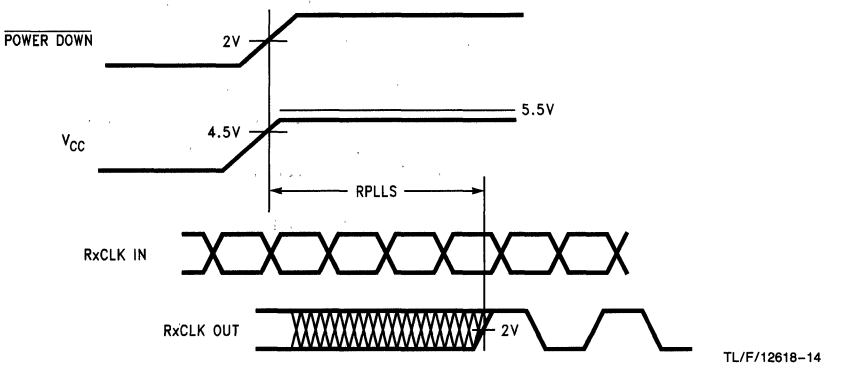

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FIGURE 12. DS90CR584 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams

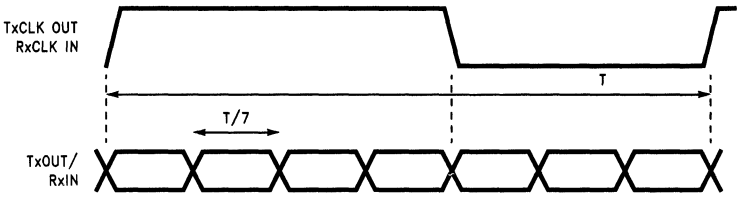

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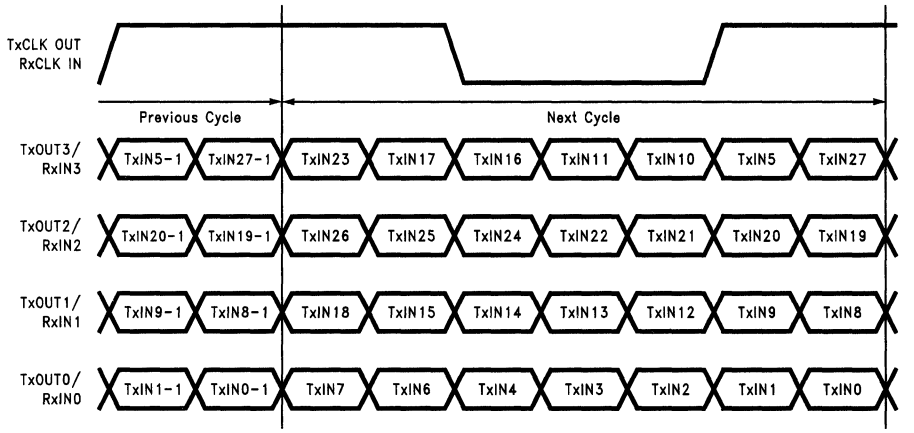
FIGURE 13. Seven Bits of LVDS in One Clock Cycle



TL/F/12618–18

FIGURE 14. Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR583)

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DS90CR583 Pin Descriptions—FPD Link Transmitter

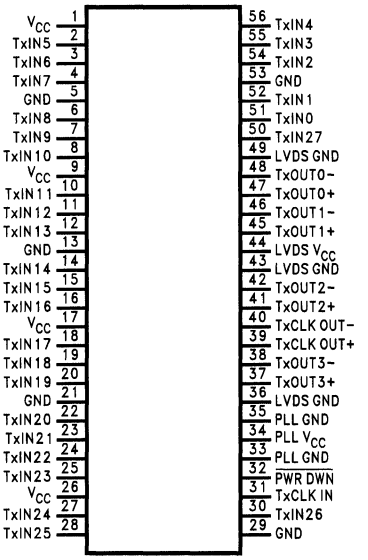
Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CR584 Pin Descriptions—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs
RxIN−	I	4	Negative LVDS differential data inputs
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The rising edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

Connection Diagrams

DS90CR583



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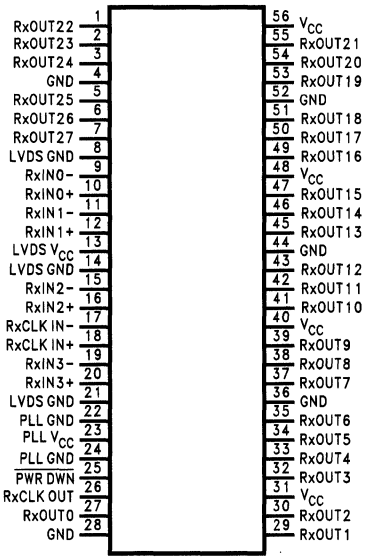
DS90CR584



TL/F/12618–16

5

National Semiconductor

PRELIMINARY

DS90CF583/DS90CF584
LVDS 24-Bit Color Flat Panel Display (FPD) Link—65 MHz

General Description

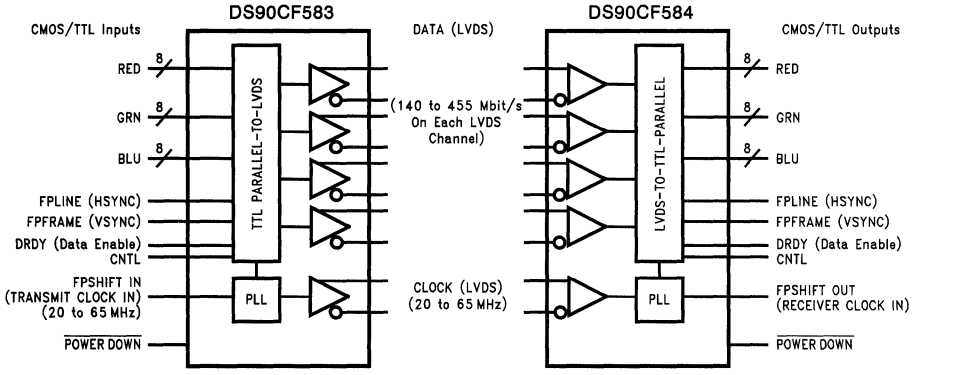
The DS90CF583 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signalling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CF584 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CONTROL) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes per second. These devices are offered with falling edge data strobes for convenient interface with a variety of graphics and LCD panel controllers.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

- Up to 227 Mbytes/s bandwidth
- Narrow bus reduces cable size
- 345 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power-down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Falling edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



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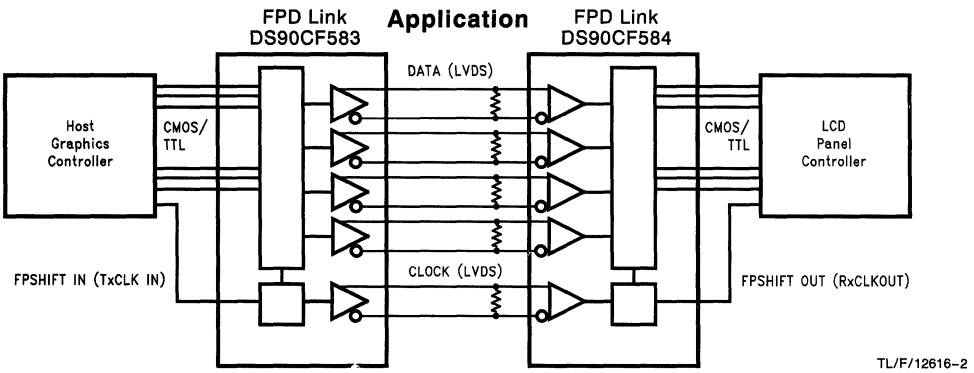
Order Number DS90CF583MTD
See NS Package Number MTD56

Order Number DS90CF584MTD
See NS Package Number MTD56



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
CMOS/TTL Input Voltage	−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage	−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration	Continuous
Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec)	+260°C

Maximum Power Dissipation @ 25°C
MTD56 (TSSOP) Package:

DS90CF583	TBD W
DS90CF584	TBD W

Package Derating:

DS90CF583	TBD W/°C above +25°C
DS90CF584	TBD W/°C above +25°C

This device does not meet 2000V ESD rating (Note 4).

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	4.5	5.0	5.5	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS							
V_{IH}	High Level Input Voltage			2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA		3.8	4.9		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA			0.1	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V			±5.1	±10	µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V				−120	mA
LVDS DRIVER DC SPECIFICATIONS							
V_{OD}	Differential Output Voltage	R_L = 100Ω		250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complementary Output States					35	mV
V_{CM}	Common Mode Voltage			1.1	1.25	1.375	V
ΔV_{CM}	Change in V_{CM} between Complementary Output States					35	mV
V_{OH}	High Level Output Voltage				1.3	1.6	V
V_{OL}	Low Level Output Voltage			0.9	1.07		V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω			−2.9	−5	mA
I_{OZ}	Output TRI-STATE® Current	$\overline{\text{Power Down}}$ = 0V, V_{OUT} = 0V or V_{CC}			±1	±10	µA
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V			±10	µA
		V_{IN} = 0V				±10	µA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)
PLL V_{CC} ≥ 1000V
All other pins ≥ 2000V
EIAJ (0Ω, 200 pF) ≥ 150V

Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current, Worst Case	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern *(Figures 1, 3)*	f = 32.5 MHz		34	46	mA
			f = 37.5 MHz		36	48	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTG}	Transmitter Supply Current, 16 Grayscale	R_L = 100Ω, C_L = 5 pF, 16 Grayscale Pattern *(Figures 2, 3)*	f = 32.5 MHz		27	42	mA
			f = 37.5 MHz		28	43	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCTZ}	Transmitter Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current, Worst Case	C_L = 8 pF, Worst Case Pattern *(Figures 1, 4)*	f = 32.5 MHz		55	75	mA
			f = 37.5 MHz		60	80	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRG}	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern *(Figures 2, 4)*	f = 32.5 MHz		35	55	mA
			f = 37.5 MHz		37	58	mA
			f = 65 MHz		TBD	TBD	mA
I_{CCRZ}	Receiver Supply Current, Power Down	$\overline{\text{Power Down}}$ = Low			1	10	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time *(Figure 3)*			0.75	1.5	ns
LHLT	LVDS High-to-Low Transition Time *(Figure 3)*			0.75	1.5	ns
CLHT	CMOS/TTL Low-to-High Transition Time *(Figure 4)*			3.5	6.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time *(Figure 4)*			2.7	6.5	ns
TCIT	TxCLK IN Transition Time *(Figure 5)*				8	ns
TCCS	TxOUT Channel-to-Channel Skew (Note A) *(Figure 6)*				350	ps
TSSPW	TxSub-Symbol Pulse Width *(Figure 6)*	f = 65 MHz	1.7	2.1	2.5	ns
RCCS	RxIN Channel-to-Channel Skew (Note B)				700	ps
TCIP	TxCLK IN Period *(Figure 7)*		15	T	50	ns
TCIH	TxCLK IN High Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time *(Figure 7)*		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN *(Figure 7)*	f = 65 MHz	TBD			ns
THTC	TxIN Hold to TxCLK IN *(Figure 7)*		2.5	2		ns
RCOP	RxCLK OUT Period *(Figure 8)*		15	T	50	ns

Note A: This limit based on bench characterization.

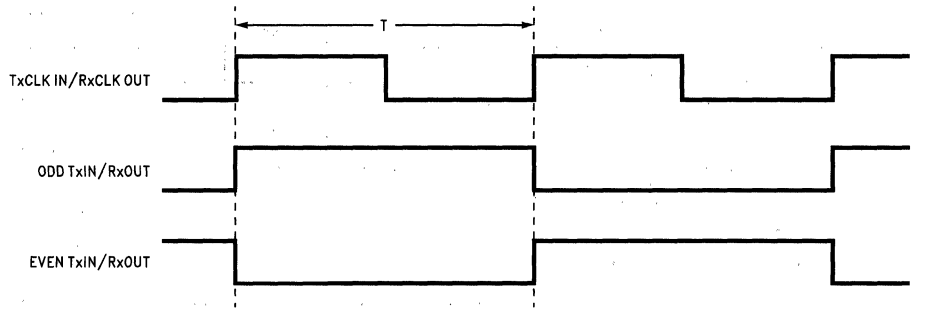
Note B: This limit assumes a maximum cable skew of 350 ps.

Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

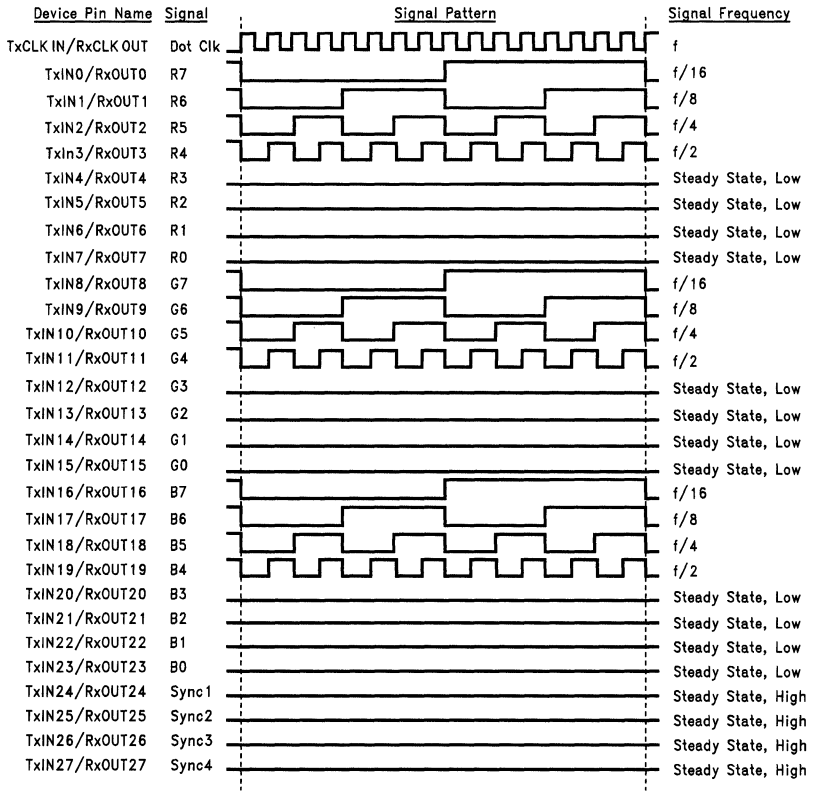
Symbol	Parameter		Min	Typ	Max	Units
RCOH	RxCLK OUT High Time *(Figure 8)*	f = 65 MHz	TBD			ns
RCOL	RxCLK OUT Low Time *(Figure 8)*	f = 65 MHz	TBD			ns
RSRC	RxOUT Setup to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
RHRC	RxOUT Hold to RxCLK OUT *(Figure 8)*	f = 65 MHz	TBD			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 9)*		5		9.7	ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 5.0V *(Figure 10)*		7.6		11.9	ns
TPLLS	Transmitter Phase Lock Loop Set *(Figure 11)*				10	ms
RPLLS	Receiver Phase Lock Loop Set *(Figure 12)*				10	ms

AC Timing Diagrams



TL/F/12616–3

FIGURE 1. "Worst Case" Test Pattern



TL/F/12616–4

FIGURE 2. "16 Grayscale" Test Pattern

Note 1: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 2: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 3: *Figure 1* and *Figure 2* show a falling edge data strobe (TxCLK IN/RxCLK OUT).

AC Timing Diagrams (Continued)

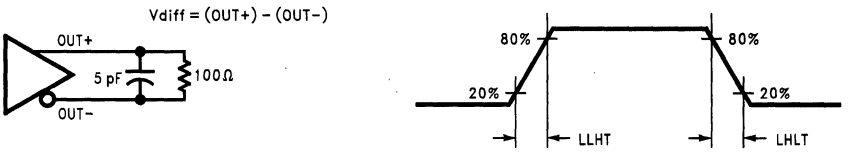


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FIGURE 3. DS90CF583 (Transmitter) LVDS Output Load and Transition Times

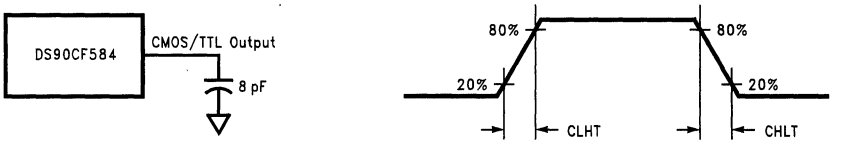

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FIGURE 4. DS90CF584 (Receiver) CMOS/TTL Output Load and Transition Times

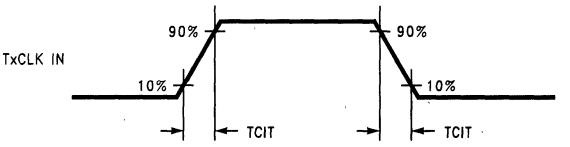

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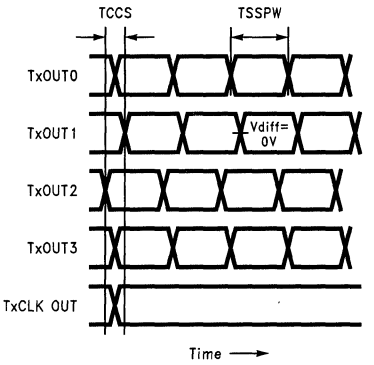
FIGURE 5. DS90CF583 (Transmitter) Input Clock Transition Time



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Note 1: Measurements at Vdiff = 0V
Note 2: TCSS measured between earliest and latest LVDS edges.
Note 3: TxCLK Differential High → Low Edge

FIGURE 6. DS90CF583 (Transmitter) Channel-to-Channel Skew and Pulse Width

AC Timing Diagrams (Continued)

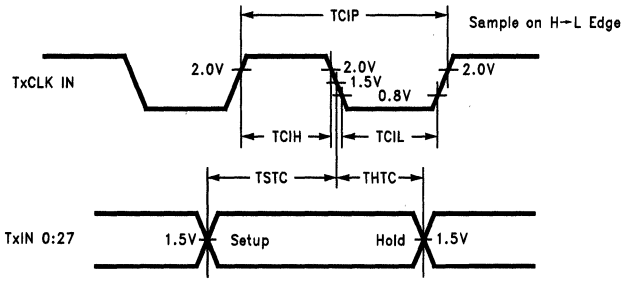

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FIGURE 7. DS90CF583 (Transmitter) Setup/Hold and High/Low Times

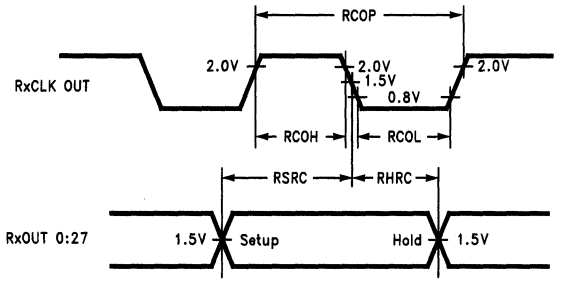

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FIGURE 8. DS90CF584 (Receiver) Setup/Hold and High/Low Times

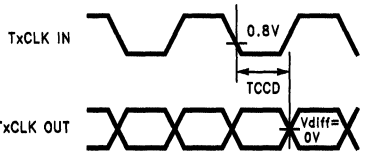

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FIGURE 9. DS90CF583 (Transmitter) Clock In to Clock Out Delay

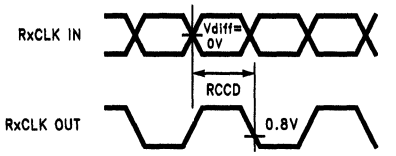

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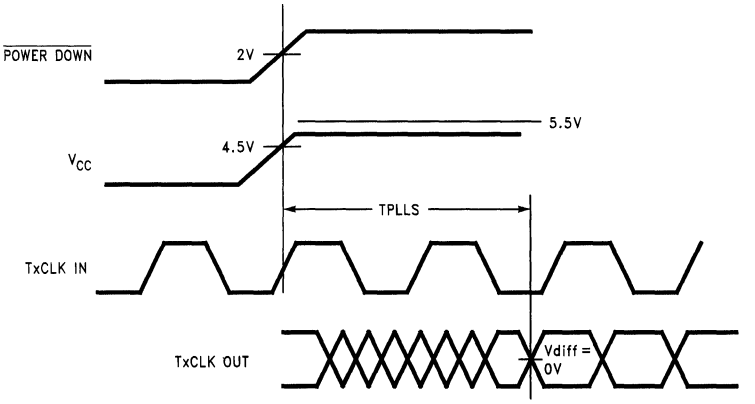
FIGURE 10. DS90CF584 (Receiver) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)



TL/F/12616–13

FIGURE 11. DS90CF583 (Transmitter) Phase Lock Loop Set Time

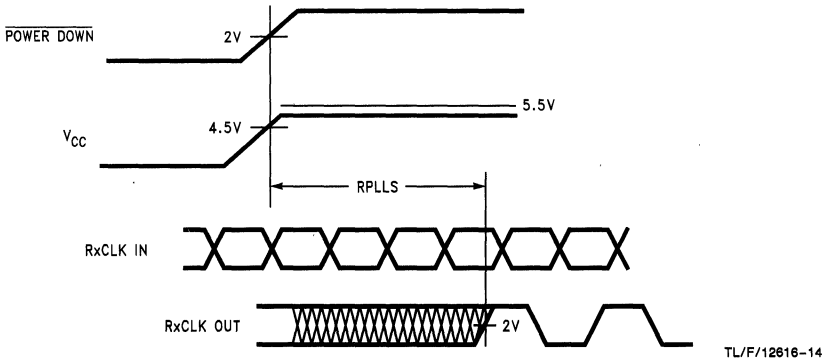


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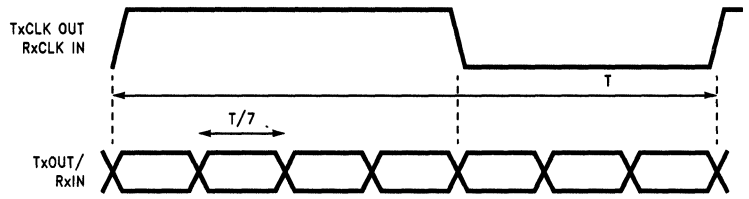
FIGURE 12. DS90CF584 (Receiver) Phase Lock Loop Set Time

AC Timing Diagrams (Continued)



TL/F/12616–17

FIGURE 13. Seven Bits of LVDS in One Clock Cycle

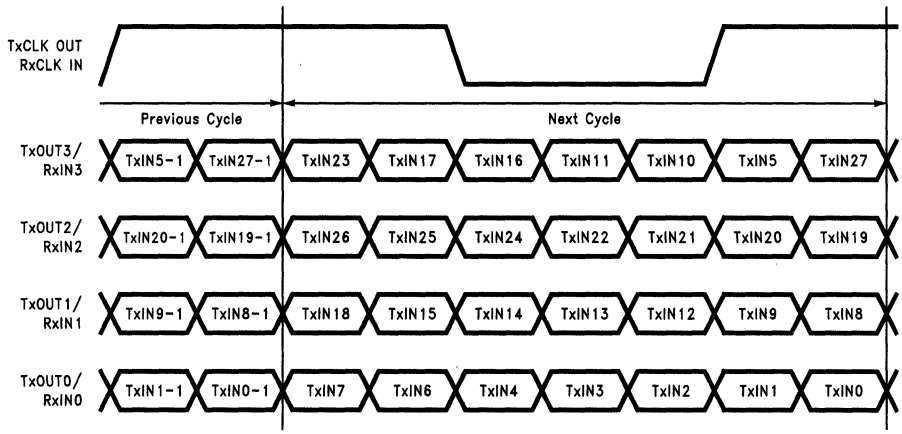


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FIGURE 14. Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CF583)

DS90CF583 Pin Descriptions—FPD Link Transmitter

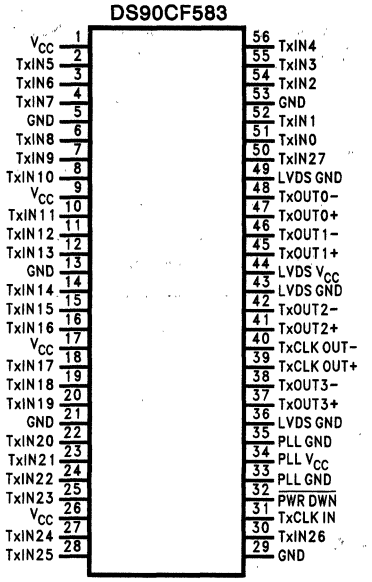
Pin Name	I/O	No.	Description
TxIN	I	28	TTL level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
TxOUT+	O	4	Positive LVDS differential data output
TxOUT−	O	4	Negative LVDS differential data output
FPSHIFT IN	I	1	TTL level clock input. The rising edge acts as data strobe
TxCLK OUT+	O	1	Positive LVDS differential clock output
TxCLK OUT−	O	1	Negative LVDS differential clock output
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL inputs
GND	I	5	Ground pins for TTL inputs
PLL V_{CC}	I	1	Power supply pin for PLL
PLL GND	I	2	Ground pins for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs
LVDS GND	I	3	Ground pins for LVDS outputs

DS90CF584 Pin Descriptions—FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs
RxIN−	I	4	Negative LVDS differential data inputs
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY and CNTL (also referred to as HSYNC, VSYNC, Data Enable, CNTL)
RxCLK IN+	I	1	Positive LVDS differential clock input
RxCLK IN−	I	1	Negative LVDS differential clock input
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down
V_{CC}	I	4	Power supply pins for TTL outputs
GND	I	5	Ground pins for TTL outputs
PLL V_{CC}	I	1	Power supply for PLL
PLL GND	I	2	Ground pin for PLL
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs
LVDS GND	I	3	Ground pins for LVDS inputs

Connection Diagrams

DS90CF583



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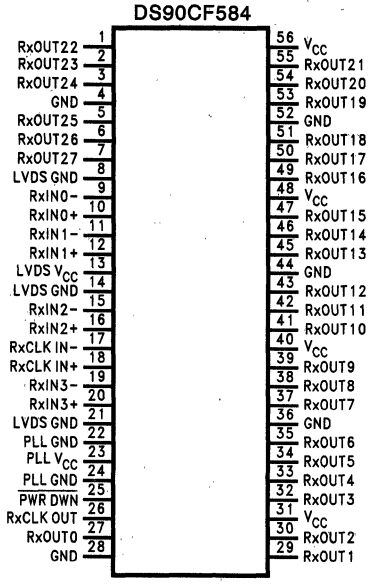
DS90CF584



TL/F/12616–16

Section 6
Special Interface Circuits

Section 6 Contents

National Semiconductor

PRELIMINARY

DS36C200
Dual High Speed Bi-Directional Differential Transceiver

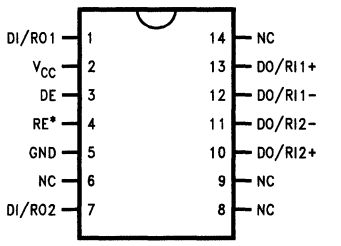
General Description

The DS36C200 is a dual transceiver device optimized for high data rate and low power applications. This device provides a single chip solution for a dual high speed bi-directional interface. Also, both control pins may be routed together for single bit control of datastreams. Both control pins are adjacent to each other for ease of routing them together. The DS36C200 is compatible with IEEE 1394 physical layer and may be used as an economical solution with some considerations. Please reference the application information on 1394 for more information. The device is in a 14-lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 210 mV. The receiver offers ±100 mV threshold sensitivity, in addition to common mode noise protection.

Features

- Optimized for DSS to DVHS interface link
- IEEE 1394 signaling
- Operates above 100 Mbps
- Bi-directional transceivers
- 14-lead SOIC package
- Ultra low power dissipation
- ±100 mV receiver sensitivity
- Low differential output swing typical 210 mV

Connection Diagram



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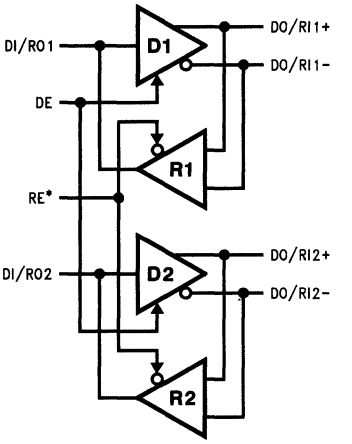
Order Number DS36C200M
See NS Package Number M14A

Functional Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.3V to +6V
Enable Input Voltage (DE, RE*)	−0.3V to (V_{CC} + 0.3V)
Voltage (DI/RO)	−0.3V to (V_{CC} + 0.3V)
Voltage (DO/RI±)	−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation @ +25°C	
M Package	TBD mW
Derate M Package	TBD mW/°C above +25°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 4 sec.)	+260°C
ESD Rating (HBM 1.5 kΩ, 100 pF) (Note 4)	≥2.5 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	0		2.4	V
Operating Free Air Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3 and 7)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS							
V_{OD}	Output Differential Voltage	R_L = 55Ω *Figure 1*	DO+, DO−	172	210	TBD	mV
ΔV_{OD}	V_{OD} Magnitude Change			0	4	35	mV
V_{OH}	Output High Voltage				1.36	1.6	V
V_{OL}	Output Low Voltage			0.9	1.15		V
V_{OS}	Offset Voltage			0.9	1.25	1.6	V
ΔV_{OS}	Offset Magnitude Change			0	5	25	mV
I_{OZD}	TRI-STATE® Leakage	V_O = V_{CC} or GND		0	±1	±10	μA
I_{OXD}	Power-Off Leakage	V_O = V_{CC} = GND = 0V		0	±1	±10	μA
I_{OSD}	Output Short Circuit Current				−6	−9	mA
DIFFERENTIAL RECEIVER CHARACTERISTICS							
V_{TH}	Input Threshold High		RI+, RI−			+100	mV
V_{TL}	Input Threshold Low			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, or 0V		−10	±1	+10	μA
V_{OH}	Output High Voltage	I_{OH} = −400 μA	RO	3.8	4.9		V
		Inputs Open		3.8	4.9		V
		Inputs Terminated, R_t = 55Ω		3.8	4.9		V
		Inputs Shorted, V_{OD} = 0V			4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA, V_{ID} = −200 mV			0.3	0.5	V
I_{OSR}	Output Short Circuit Current	V_{OUT} = 0V		−15	−60	−100	mA

Electrical Characteristics (Continued)

Over supply voltage and operating temperature ranges, unless otherwise specified (Notes 2, 3 and 7)

Symbol	Parameter	Conditions	Pin	Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V_{IH}	Input High Voltage		DI, DE RE*	2.0		V_{CC}	V
V_{IL}	Input Low Voltage			GND		0.8	V
I_{IH}	Input High Current	$V_{IN} = V_{CC}$ or 2.4V			±1	±10	μA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			±1	±10	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA		−1.5	−0.8		V
I_{CCD}	Power Supply Current	No Load; DE = RE* = V_{CC}	V_{CC}		3	7	mA
		$R_L = 55\Omega$; DE = RE* = V_{CC}			10	TBD	mA
I_{CCR}		DE = RE* = 0V			5	7	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} amd V_{ID}.

Note 3: All typicals are given for $V_{CC} = +5.0$V and $T_A = +25°C$.

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF) ≥ 2.5 kV
EIAJ (0Ω, 200 pF) ≥ TBD

Note 5: C_L includes probe and fixture capacitance.

Note 6: Generator waveform for all tests unless otherwise specified: f = 1 MHz, $Z_O = 50\Omega$, $t_r \leq 1$ ns, $t_f \leq 1$ ns (0%–100%).

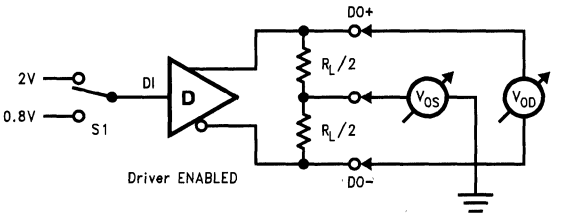
Note 7: The DS36C200 is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.

Switching Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified (Note 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIFFERENTIAL DRIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 55Ω, C_L = 50 pF *(Figures 2 and 3)*	1.5	3.4	6	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	3.50	6	ns
t_{SKD}	Differential Skew $\|t_{PHLD}-t_{PLHD}\|$		0.1	0.1	2	ns
t_{TLH}	Transition Time Low to High		0	0.5	2	ns
t_{THL}	Transition Time High to Low		0	0.5	2	ns
t_{PHZ}	Disable Time High to Z	R_L = 55Ω *(Figures 4 and 5)*	0.3	5	20	ns
t_{PLZ}	Disable Time Low to Z		0.3	5	20	ns
t_{PZH}	Enable Time Z to High		0.3	10	30	ns
t_{PZL}	Enable Time Z to Low		0.3	10	30	ns
DIFFERENTIAL RECEIVER CHARACTERISTICS						
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 50 pF, V_{ID} = 200 mV *(Figures 6 and 7)*	1.5	3.4	6	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	3.5	6	ns
t_{SKD}	Differential Skew $\|t_{PHLD}-t_{PLHD}\|$		0.1	0.1	2	ns
t_r	Rise Time		0	0.5	2.5	ns
t_f	Fall Time		0	0.5	2.5	ns
t_{PHZ}	Disable Time High to Z	C_L = 5 pF *(Figures 8 and 9)*	1	10	20	ns
t_{PLZ}	Disable Time Low to Z		1	10	20	ns
t_{PZH}	Enable Time Z to High		0.3	10	30	ns
t_{PZL}	Enable Time Z to Low		0.3	10	30	ns

Parameter Measurement Information



TL/F/12621–3

FIGURE 1. Differential Driver DC Test Circuit

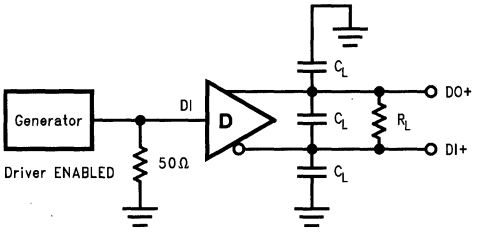


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FIGURE 2. Differential Driver Propagation Delay and Transition Time Test Circuit

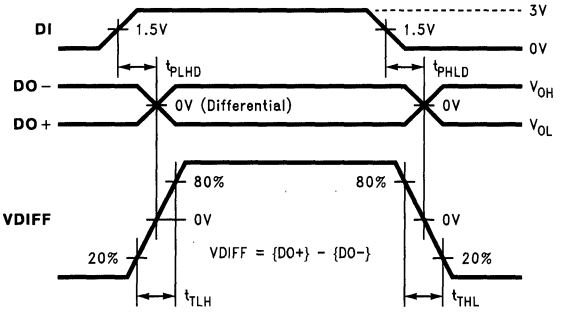

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FIGURE 3. Differential Driver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (Continued)

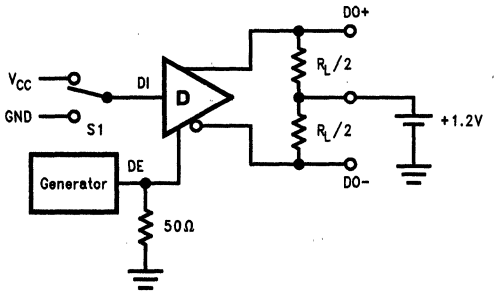

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FIGURE 4. Driver TRI-STATE Delay Test Circuit

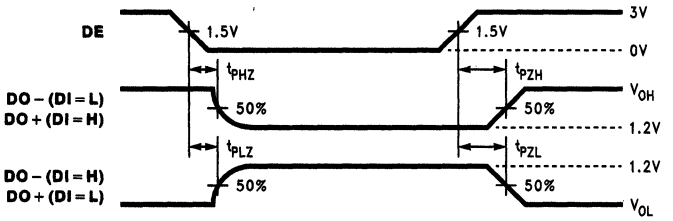

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FIGURE 5. Driver TRI-STATE Delay Waveforms

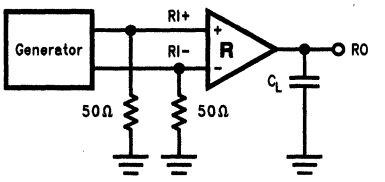

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FIGURE 6. Receiver Propagation Delay and Transition Time Test Circuit

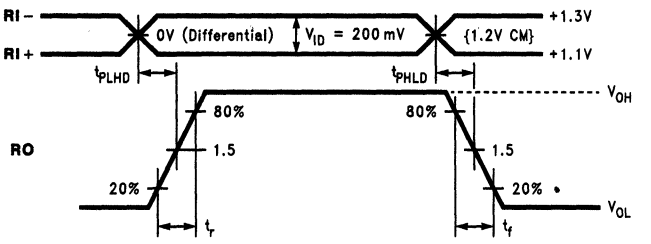

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FIGURE 7. Receiver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (Continued)

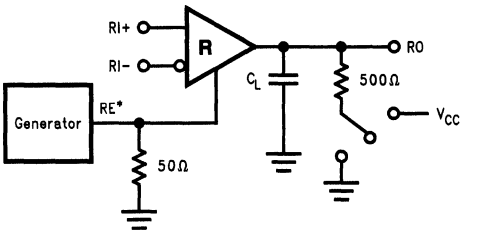

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FIGURE 8. Receiver TRI-STATE Delay Test Circuit

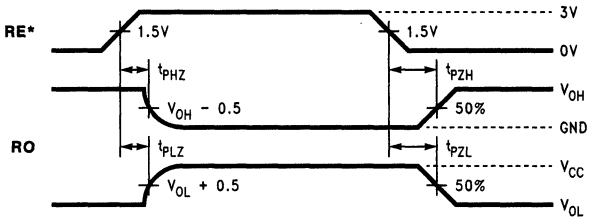

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FIGURE 9. Receiver TRI-STATE Delay Waveforms

Application Information

TRUTH TABLES

The DS36C200 has two enable pins DE and RE*, however, the driver and receiver should never be enabled simultaneously. Enabling both could cause multiple channel contention. It is recommended to route the enables together on the PC board. This will allow a single bit [DE/RE*] to control the chip. This DE/RE* bit toggles the DS36C200 between Receive mode and Transmit mode. When the bit is asserted HIGH the device is in Transmit mode. When the bit is asserted LOW the device is in Receive mode. The mode determines the function of the I/O pins: DI/RO, DO/RI+, and DO/RI−. Please note that some of the pins have been identified by its function in the corresponding mode in the three tables below. For example, in Transmit mode the DO/RI+ pin is identified as DO+. This was done for clarity in the tables only and should not be confused with the pin identification throughout the rest of this document. Also note that a logic low on the DE/RE* bit corresponds to a logic low on both the DE pin and the RE* pin. Similarly, a logic high on the DE/RE* bit corresponds to a logic high on both the DE pin and the RE* pin.

Receive Mode

Input(s)		Input/Output	
DE	RE*	[RI+] − [RI−]	RO
L	L	> +100 mV	H
L	L	< −100 mV	L
L	L	100 mV > & > −100 mV	X

Transmit Mode

Input(s)		Input/Output		
DE	RE*	DI	DO+	DO−
H	H	L	L	H
H	H	H	H	L
H	H	2 > & > 0.8	X	X

H = Logic high level

L = Logic low level

X = Indeterminant state

TABLE I. Device Pin Descriptions

Pin #	Name (In mode only)	Mode	Description
3	DE	Transmit	Driver Enable: When asserted low driver is disabled. And when asserted high driver is enabled.
1, 7	DI		TTL/CMOS driver input pins
10, 13	DO+		Noninverting driver output pin
11, 12	DO−		Inverting driver output pin
4	RE*	Receive	Receiver Enable: When asserted low receiver is enabled. And when asserted high receiver is disabled.
1, 7	RO		Receiver output pin
10, 13	RI+		Positive receiver input pin
11, 12	RI−		Negative receiver input pin
5	GND	Transmit and Receive	Ground pin
2	V_{CC}		Positive power supply pin, +5V ±10%

IEEE 1394

The DS36C200 drives and receives IEEE 1394 physical layer signal levels. The current mode driver is cabpable of driving a 55Ω load with V_{OD} between 172 mV and TBD mV. The DS36C200 is not designed to work with a link layer controller IC requiring full 1394 physical layer compliancy to the standard. No clock generator, no arbitration, and no encode/decode logic is provided with this device. For a 1394 link where speed sensing, bus arbitration, and other functions are not required, a controller and the DS36C200 will provide a cost effective, high speed dedicated link. This is shown in *Figure 10A*. In applications that require fully compliant 1394 protocol, a link layer controller and physical layer controller will be required as shown in *Figure 10B*. The physical layer controller supports up to three DC36C200 devices (not shown).

Application Information (Continued)

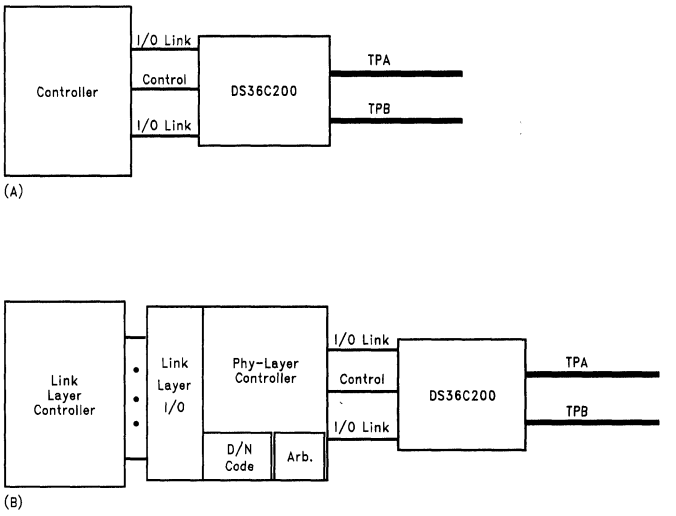

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FIGURE 10. (A) Dedicated IEEE 1394 Link
(B) Full IEEE 1394 Compliant Link

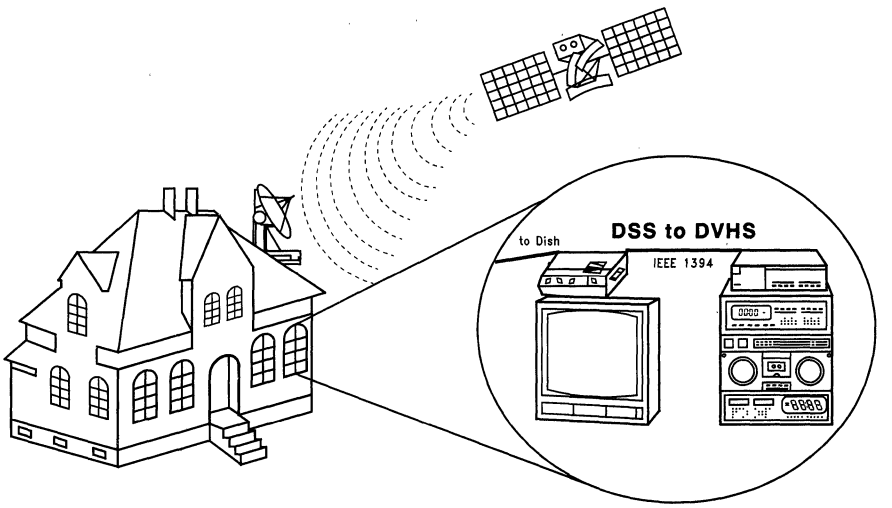

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FIGURE 11. Typical in Home Application

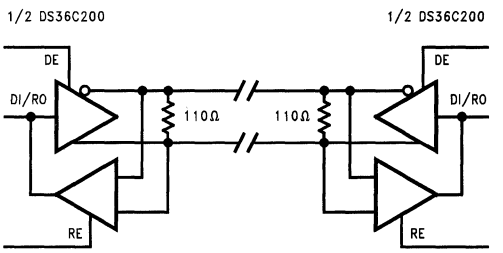

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FIGURE 12. Typical Interface Connection (Note 7)

National Semiconductor

ADVANCE INFORMATION

DS36C250
Controller Area Network (ISO/DIS 11898) Transceiver

General Description

The DS36C250 is a low power differential, bus transceiver designed to meet the requirements of the ISO/DIS 11898 Controller Area Network (CAN) Standard for multipoint data communication. The DS36C250 also meets the requirements of CAN V2.0..

The DS36C250 transceiver is composed of three major functional blocks: a transmitter with differential output, a differential input receiver and a voltage reference. Data to be transmitted over the CAN bus (CAN_H and CAN_L) is input to the DS36C250 on the TxD pin. Data received over the CAN bus is output via the RxD pin. The CAN bus data signal consists of a sequence of large and small amplitude differential voltages. A positive (or large) differential voltage represents the so-called "dominant" (or active) bit value. When the CAN bus voltage corresponds to the dominant bit, the CAN_H voltage is more positive than the CAN_L voltage. A zero differential voltage (CAN_H = CAN_L $\approx V_{CC}/2$) represents the "recessive" (or passive) bit value. Data signals applied to TxD or output from RxD are logically low-true. The signal polarity on CAN_H is inverted with respect to that of TxD or RxD. Additionally, each transceiver supplies current at a voltage equal to V_{REF} to maintain the CAN bus (CAN_H and CAN_L) at approximately $V_{CC}/2$ when the bus is in the recessive (passive) state.

The DS36C250 transmitter is designed to reduce EMI from the CAN bus. The CAN bus output rise and fall times are controlled by extracting current from the R_S pin. The control element can be as simple as a single resistor connected from the R_S pin to ground.

The DS36C250 is designed to resist fault conditions occuring on the CAN bus. The CAN bus I/O pins are designed to withstand overvoltages up to 25V. The receiver design allows operation over a common mode range of −7V to +12V. The transmitter has thermal and current limiting in the output driver stage. Additionally, the device outputs withstand shorts to either V_{CC} or ground. The device is fully specified over the automotive temperature range (−40°C to +125°C). The DS36C250 is form, fit and function compatible with other CAN transceivers while offering improved characteristics and performance.

Features

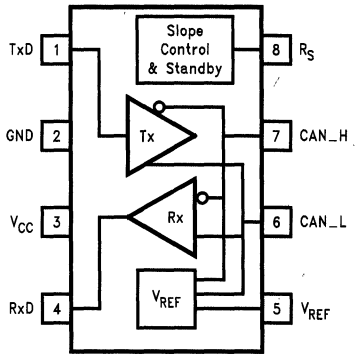
- Meets CAN V2.0B and ISO/DIS-11898 Standards
- Adjustable transmitter slew rate for low EMI/RFI
- Data rates up to 1M bit/s
- Low standby power
- Wide common mode range: −7V to +12V
- CAN bus pins withstand up to 25V
- Automotive temperature range −40°C to +125°C
- Industry standard function and pinout (Philips PCA82C250)
- Available in JEDEC SOIC-8 and mini-DIP packages

Product Application

- DS36C250 is suitable for all ISO/DIS 11898 and CAN V2.0B automotive and industrial applications.

Connection and Logic Diagram

SOIC-8 and Mini-DIP



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Pin Descriptions

Pin #	Name	Description
1	TxD	Transmitter Input, Inverted with Respect to CAN_H
2	GND	Circuit Ground (0V)
3	V_{CC}	Positive Power Supply Input (+5V, ±10%)
4	RxD	Receiver Output, Inverted with Respect to CAN_H
5	V_{REF}	CAN Bus Reference Voltage Source $V_{CC}/2$
6	CAN_L	CAN Bus Low-Side Driver Output/ Receiver Input
7	CAN_H	CAN Bus High-Side Driver Output/ Receiver Input
8	R_S	CAN Bus Output Slope Control, Standby Mode Control

Truth Table (Z = transmitter output off or floating)

TRANSMITTER				
TxD	**CAN_H**	**CAN_L**	**RxD**	**CAN BUS STATE**
0	HIGH	LOW	0	Dominant
1	Z	Z	1	Recessive
unconnected	Z	Z	1	Recessive
RECEIVER				
1	HIGH	LOW	0	Dominant
1	Z	Z	1	Recessive

R_S Functions

FORCED CONDITION AT R_S	MODE	VOLTAGE OR CURRENT AT R_S
$V_{Rs} > 0.75V_{CC}$	Standby	$I_{Rs} < \lvert 10\ \mu A \rvert$
$-10\ \mu A < I_{Rs} < -200\ \mu A$	Slope Control	$0.4V_{CC} < V_{Rs} < 0.6V_{CC}$
$V_{Rs} < 0.3V_{CC}$	High-Speed	$I_{Rs} -500\ \mu A$

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) +12.0V
Input Voltage (TxD, R_S) −0.5V to (V_{CC} +0.5V)
Common Mode Voltage (CAN_H, CAN_L) (Note 8) ±20.0V
Input Voltage (CAN_H, CAN_L) (Note 8) ±25.0V
Output Voltage (RxD) −0.5V to (V_{CC} + 0.5V)
Output Current (V_{REF}) ±100 μA
Maximum Package Power Dissipation @ +25°C
M Package TBD mW, derate TBD mW/°C above +25°C
N Package TBD mW, derate TBD mW/°C above +25°C
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering 4 sec.) +260°C
ESD Capability
(Class 2 per MIL-STD-883C, test method 3015) >2 kV

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
CAN Bus Voltage (V_{CM})	−7.0		+12.0	V
Operating Free Air Temperature (T_A)	−40	25	125	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 2 and 3).

DEVICE DC POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
I_{CC}	Power Supply Current	No Load, not Standby, V_{Rs} = 0V, TxD = V_{IL}			200	500	μA
I_{CDom}	Supply Current, Dominant	TxD = V_{IL} For R_L, see Note 9			40	70	mA
I_{CCRec}	Supply Current, Recessive	TxD = V_{IH}, R_L = 60Ω			12	18	mA
I_{CCStby}	Supply Current, Standby	TxD = V_{IH}, V_{Rs} = V_{IH}				150	μA
DRIVER DC CHARACTERISTICS							
V_{IH}	High Level Input Voltage		TxD	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		TxD	0.0		0.8	V
I_{IH}	High Level Input Current	V_{IH} = V_{CC}	TxD			2	μA
I_{IL}	Low Level Input Current	V_{IL} = 0V	TxD			−2	μA
$V_{CANdiff}$	Differential Output Voltage, V_{CAN_H}−V_{CAN_L}	Dominant, R_L = 60Ω Recessive, R_L = 60Ω	*Figure 1*	1.5 −500		3.0 50	V mV
$V_{CANHdom}$ $V_{CANLdom}$	Driver Output Voltage	Dominant, R_L = 60Ω	CAN_H, *Figure 2* CAN_L, *Figure 2*	2.75 0.5		4.5 2.25	V V
$V_{CANHrec}$ $V_{CANLrec}$	Driver Output Voltage	Recessive, R_L = 60Ω	CAN_H, *Figure 2* CAN_L, *Figure 2*	2.0 2.0		3.0 3.0	V V
V_{BAL}	Differential Output Voltage Balance	Dominant, R_L = 60Ω	*Figure 4*		|TBD|		|mV|
I_{OSD}	Driver Output Short-Circuit Current	V_{CAN_H} = −7 to +12V $V_{CAN\_H\ or\ L}$ = 0V V_{CAN_L} = −7V to +12V	*Figure 3*	0 0	−190 100 190	−250 +250	mA mA mA
RECEIVER DC CHARACTERISTICS							
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	RxD, *Figure 5*	3.5	4.6		V
V_{OL}	Low Level Output Voltage	I_{OL} = +4 mA	RxD, *Figure 5*		0.3	0.5	V
I_{OSH}	Output Short Circuit Current	V_O = GND	RxD	−7	−35	−85	mA
I_{OSL}	Output Short Circuit Current	V_O = V_{CC}	RxD	7	35	85	mA
V_{Tdom}	Differential Input Dominant Threshold Voltage	−7V ≤ V_{CM} ≤ +12V	*Figure 11*	0.9		5.0	V
V_{Trec}	Differential Input Recessive Threshold Voltage	−7V ≤ V_{CM} ≤ +12V	*Figure 11*	−1.0		0.5	V
I_{IN}	Input Current (Note 4)	Other Input = V_{CC}/2, V_{CC} = 0V or +5V ±10%	V_I = +12V V_I = −7		TBD TBD	0.5 −0.4	mA mA

Electrical Characteristics (Continued)

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Notes 2 and 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
RECEIVER DC CHARACTERISTICS (Continued)							
V_{HYS}	Hysteresis	$V_{CM} = 0V$	Note 5, *Figure 13*		150		mV
R_{IN}	Input Resistance	$-7V \leq V_{CM} \leq +12V$		TBD	68		kΩ
R_{INdiff}	Differential Input Resistance				TBD		kΩ
RECEIVER AC CHARACTERISTICS							
C_{IN}	Input Capacitance, TxD				TBD		pF
$C_{IN(CAN)}$	Input Capitance, CAN__H or CAN__L				TBD		pF
C_{INdiff}	Differential Input Capacitance, CAN__H to CAN__L				TBD		pF
REFERENCE OUTPUT DC CHARACTERISTICS							
V_{REF}	Reference Output Voltage	$I_L = \pm 50\ \mu A$		$0.45V_{CC}$	$0.5V_{CC}$	$0.55V_{CC}$	V
I_{REF}	Reference Output Current					± 100	μA
SLOPE CONTROL/STANDBY DC CHARACTERISTICS							
V_{Rs}	Slope Control Input Voltage for F_{max}					$0.3\ V_{CC}$	V
I_{Rs}	Slope Control Input Current for F_{max}	$V_{Rs} = 0V$				−500	μA
$V_{standby}$	Slope Control Input Voltage for Standby Mode			$0.75\ V_{CC}$			V
I_{slope}	Slope Control Mode Current Range			−10		−200	μA
V_{slope}	Slope Control Mode Voltage Range			$0.4\ V_{CC}$		$0.6\ V_{CC}$	V

Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified (Note 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
F_{MAX}	Maximum Operating Frequency	I_{Rs} = max.			1		MHz
t_{bit}	Minimum Bit Time	I_{Rs} = max.			1		μs
DRIVER SWITCHING CHARACTERISTICS							
t_{offTxD}	Differential Propagation Delay Dom. to Rec.	R_L = 60Ω, C_L = 100 pF	*Figures 6 & 9*		40	80	ns
t_{onTxD}	Differential Propagation Delay Rec. to Dom.	V_{Rs} = 0V	*Figures 6 & 9*		TBD	50	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$	V_{Rs} = 0V	*Figure 10,* (Note 6)		TBD	TBD	ns
t_r t_f	Rise Time Fall Time	V_{Rs} = 0V or I_{Rs} < −500 μA	*Figure 12*		TBD TBD		ns ns
t_r t_f	Rise Time Fall Time	I_{Rs} = −100 μA	*Figure 12*		TBD TBD		ns ns
t_r t_f	Rise Time Fall Time	I_{Rs} = −20 μA	*Figure 12*		TBD TBD		ns ns
RECEIVER SWITCHING CHARACTERISTICS							
t_{offRxD}	Delay TxD = V_{IH} to RxD = V_{OH}	I_{Rs} = max	*Figures 7 & 9*		TBD	160	ns
t_{onRxD}	Delay TxD = V_{IL} to RxD = V_{OL}	I_{Rs} = max	*Figures 7 & 9*		TBD	130	ns
t_{PHL}	Propagation Delay $V_{CANdiff}$ Dominant to RxD = V_{OL}	C_L = 15 pF	*Figures 7 & 9*			80	ns
t_{PLH}	Propagation Delay $V_{CANdiff}$ Recessive to RxD = V_{OH}	C_L = 15 pF	*Figures 7 & 9*			80	ns
t_{SKR}	Skew, $\lvert t_{PHL} - t_{PLH} \rvert$		*Figure 8,* (Note 6)		10	TBD	ns
t_{WAKE}	Wake-Up from Standby	via Pin 8				20	μs
t_{dRxDL}	CAN Bus Dominant to RxD = V_{OL}	Standby Mode V_{Rs} = V_{IH}				3	μs

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to mean that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions. All voltages are measured with respect to pin 2 (GND).

Note 2: Positive current is defined as flowing into device pins. Negative current is defined as flowing out of device pins. All voltages are referenced to ground (equal to zero volts) with the exception of $V_{CANdiff}$, V_{BAL}, V_{Tdom}, V_{Trec}, V_{HYS}.

Note 3: Typical values are stated for: V_{CC} = +5.0V and T_A = +25°C.

Note 4: I_{IN} includes both the receiver input current and driver recessive-state leakage current.

Note 5: Hysteresis is defined as $V_{HYS} = V_{TH} - V_{TL}$. (*Figure 13*).

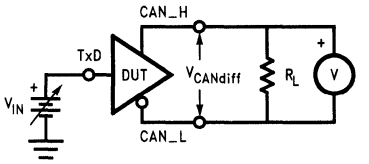
Note 6: Signal skews are defined as the largest magnitude difference between and without regard to the sequence of the specified edges.

Note 7: C_L includes probe and jig capacitances.

Note 8: The voltage applied between the CAN_H and CAN_L pins may not exceed | 25V D.C. |.

Note 9: $I_{CCdcm(typ)}$ is measured using the 60Ω CAN bus termination. $I_{CCdcm(max)}$ is measured using a 45Ω load which represents the parallel equivalent of 128 inputs (typical R_{IN}) and the CAN bus termination.

Parameter Measurement Information



TL/F/12614–2

FIGURE 1. Driver $V_{CANdiff}$ Dominant and Recessive

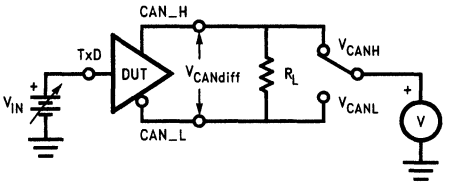


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FIGURE 2. Driver V_{CANH} and V_{CANL} Dominant and Recessive

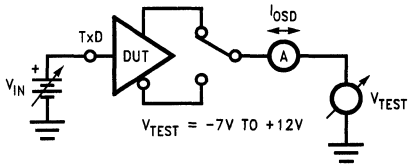

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FIGURE 3. Driver I_{OSD}

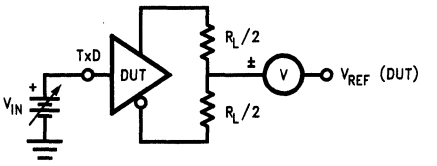

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FIGURE 4. Driver Differential Output Voltage Balance (V_{BAL})

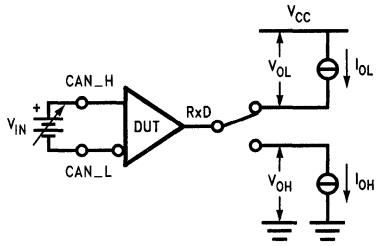

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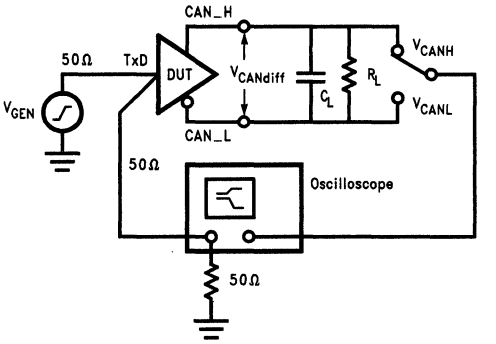
FIGURE 5. Receiver V_{OL}/I_{OL} and V_{OH}/I_{OH}



TL/F/12614–5

FIGURE 6. Driver Differential Propagation Delay Test Circuit

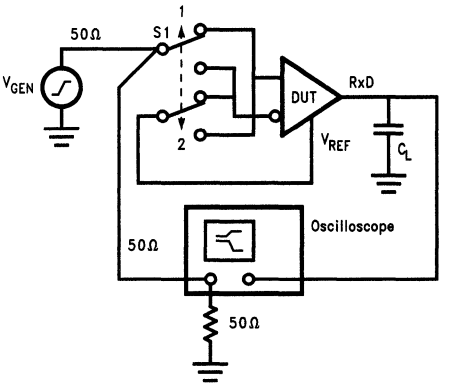


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FIGURE 7. Receiver Differential Propagation Delay Test Circuit

Parameter Measurement Information (Continued)

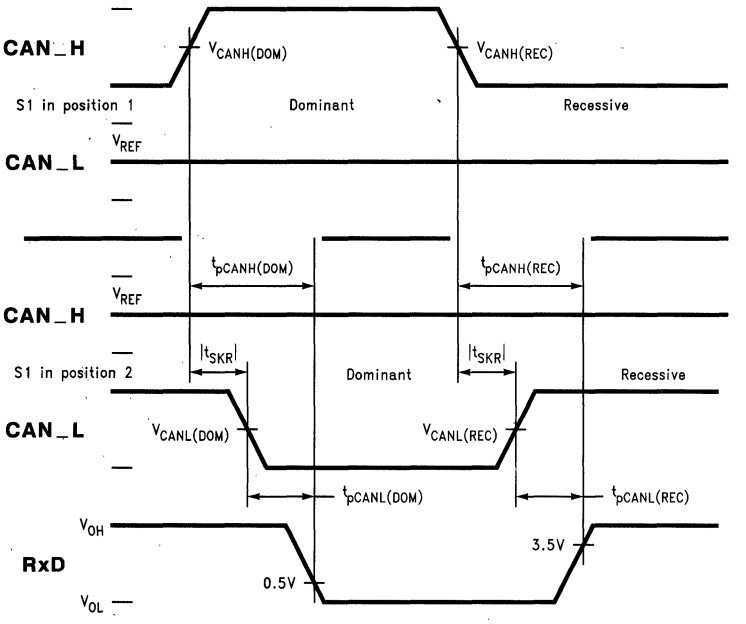

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FIGURE 8. Receiver Skew Timing

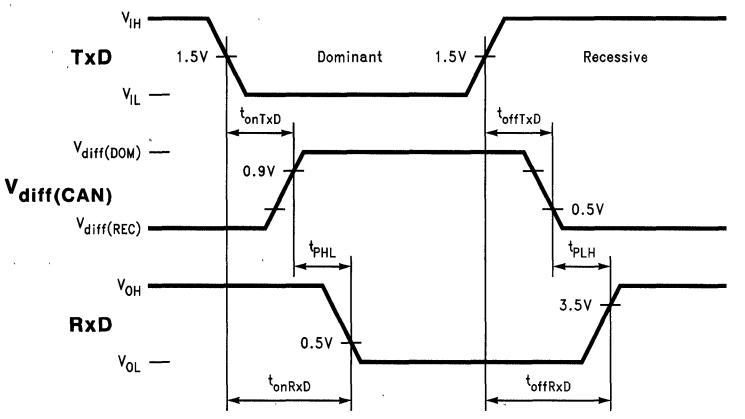

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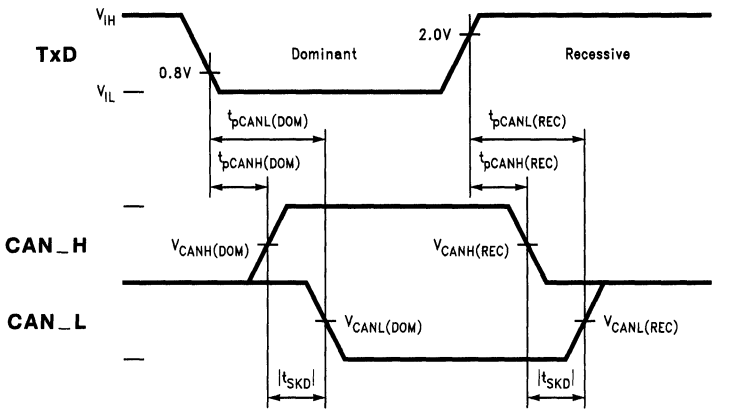
FIGURE 9. Propagation Delays

Parameter Measurement Information (Continued)



TL/F/12614–11

FIGURE 10. Driver Skew Timing

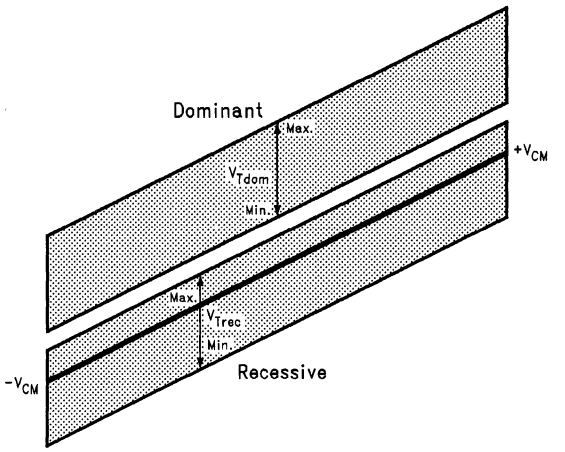


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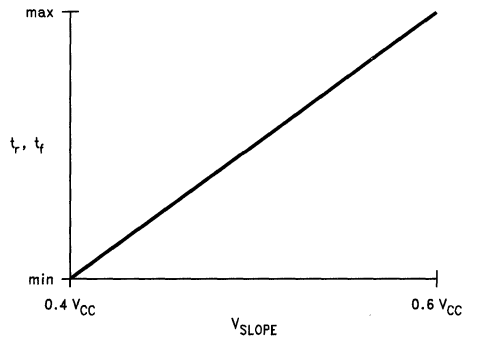
FIGURE 11. Differential Input Threshold



TL/F/12614–14

FIGURE 12. Driver Slew Rate vs R_S Pin Control Voltage

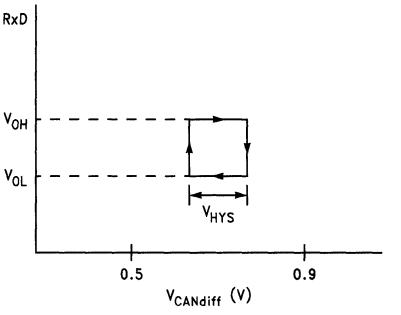


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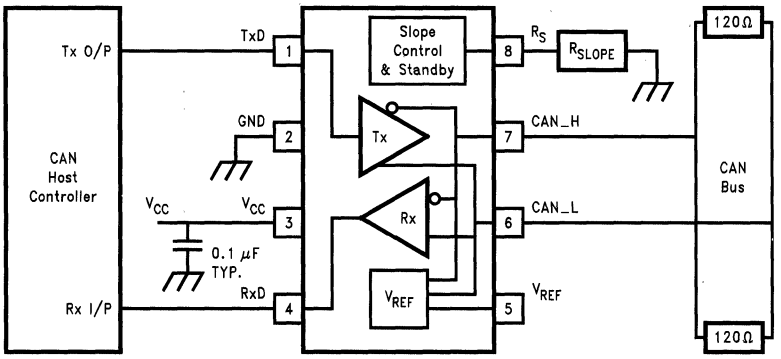
FIGURE 13. Hysteresis

Applications Information

Typical Application with Host Control



DS36C250

TL/F/12614–13

CAN BUS OUTPUT SLEW RATE CONTROL

The slew-rate of the CAN bus outputs is controlled by the amount of current flowing in pin 8, the R_S pin. Grounding pin 8, called high-speed mode, defeats the slew rate control circuitry and causes the CAN bus outputs to slew at their maximum rates. For lower speed operation and slope control, current is sunk from pin 8. This can be done using a resistor or other equivalent means. The output signal slopes will be proportional to the amount of current extracted from pin 8. When the current flowing in pin 8 is reduced to zero, the part enters the low-current, standby mode. In standby, the transmitter is switched off and the receiver placed in a powered-down mode. If dominant bits are detected on the CAN bus while the device is in standby mode, RxD will go to a low logic level. The host should then re-activate the transceiver to a normal operating mode by increasing current flow out of pin 8. Messages received while in standby mode will be lost because of the slowed response of the receiver and should be re-transmitted after the receiver is in a normal operating mode.

CAN BUS OUTPUT THERMAL, VOLTAGE AND CURRENT LIMITING

The DS36C250 incorporates thermal limiting and overcurrrent/voltage protection in the CAN bus outputs. Thermal limiting in the transmitter outputs restricts the maximum junction temperature to less than 150°C. Receiver operation is maintained during transmitter thermal limiting. Current and voltage limiting are incorporated in the design to protect against fault conditions which may occur on the CAN bus outputs such as shorts to large positive and negative battery voltages, shorts to ground, electrical transients, load dump, etc.

CAN BUS OUTPUT RECESSIVE-MODE REFERENCE POTENTIAL

The DS36C250 sources current to the CAN bus lines at a reference potential approximately equal to $V_{CC}/2$ when it is in the recessive mode (and not in the standby mode). The amount of current supplied by one or more devices connected to a properly CAN bus allows the connection of a maximum of 128 devices to the network. *Note: It should be understood that the amount of current contributed to the network by any one of N devices connected to the network will be approximately I/N; where I is the current source capability of a single device into the terminated network.*

EMI/RFI

The design of the transmitter and its output signals CAN_H and CAN_L minimizes production of both EMI/RFI and common-mode noise signals.

NETWORK SIZE LIMITS

The maximum number of network nodes in a normal CAN automotive application is 30. The DS36C250 is designed to have equivalent performance in networks having 128 nodes. In order to achieve this, particular attention has been given to parameters affecting the equivalent load that the device presents to the bus. The critical parameters include: transmitter output leakage current, receiver input resistance (and impedance), reference current source impedance, and pin reactances.

Section 7

General Purpose Drivers

Section 7 Contents

National Semiconductor

DS1692/DS3692 TRI-STATE® Differential Line Drivers

General Description

The DS1692/DS3692 are low power Schottky TTL line drivers electrically similar to the DS1691A/DS3691 but tested to meet the requirements of MIL-STD-188-114A (see Application Note AN-216). MIL-STD-188-114A type 1 driver specifications can be met by adding an external three resistor voltage divider to the output of the DS3692/1692. The DS3692/1692 feature 4 buffered outputs with high source and sink current capability with internal short circuit protection.

With the mode select pin low, the DS1692/DS3692 are dual differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ±5V supply.

Multipoint applications in differential mode with waveshaping capacitors is not allowed.

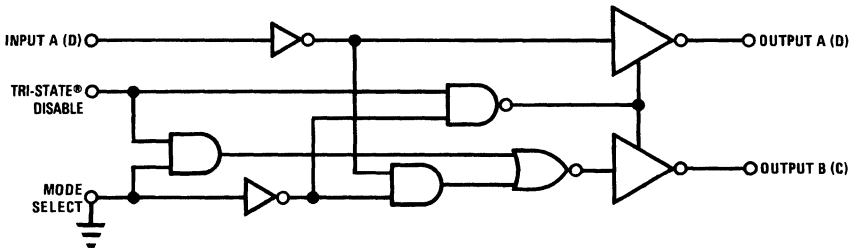
Features

- Short circuit protection for both source and sink outputs
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption

  Differential mode I_{CC} = 9 mA/driver typ

  I_{EE} = 5 mA/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Adaptable as MIL-STD-188-114A type 1 driver

Logic Diagram (½ Circuit Shown)



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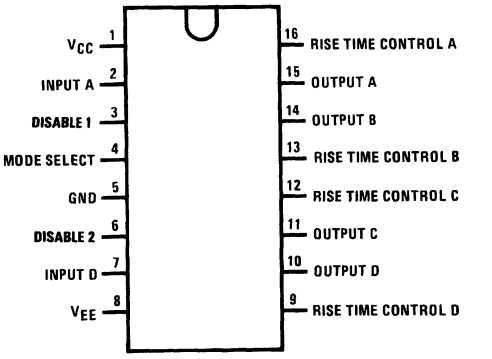
Connection Diagram



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Top View

Order Number DS1692J, DS3692J, DS3692M or DS3692N
See NS Package Number J16A, M16A* or N16A

*Contact Product Marketing for availability.

Truth Table

Inputs			Outputs	
Mode	A (D)	Disable1 (2)	A (D)	B (C)
0	0	0	0	1
0	0	1	TRI-STATE	TRI-STATE
0	1	0	1	0
0	1	1	TRI-STATE	TRI-STATE

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1692			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3692			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1692	−55	+125	°C
DS3692	0	+70	°C

Electrical Characteristics DS1692/DS3692 (Notes 2, 3 and 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DS1692, V_{CC} = 5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2V	2.5	3.6		V
			V_{IN} = 0.8V	−2.5	−3.6		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	R_L = 100Ω V_{CC} ≥ 4.75V	V_{IN} = 2V	2	2.6		V
			V_{IN} = 0.8V	−2	−2.6		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T}\rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
I_{OX}	TRI-STATE Output Current	V_O ≤ −10V			−0.002	−0.15	mA
		V_O ≥ 15V			0.002	0.15	mA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA
DS1692, V_{CC} = 5V ±10%, V_{EE} = −5V ±10%, DS3692, V_{CC} = 5V ±5%, V_{EE} = −5 ±5%, MODE SELECT ≤ 0.8V							
V_O $\overline{V_O}$	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2.4V	7	8.5		V
			V_{IN} = 0.4V	−7	−8.5		V
V_T $\overline{V_T}$	Differential Output Voltage $V_{A,B}$	R_L = 200Ω	V_{IN} = 2.4V	6	7.3		V
			V_{IN} = 0.4V	−6	−7.3		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, R_L = 200Ω			0.02	0.4	V
I_{OX}	TRI-STATE Output Current		V_O = 10V		0.002	0.15	mA
			V_O = −10V		−0.002	−0.15	mA
I_S^+ I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

Electrical Characteristics (Notes 2 and 3) $V_{EE} \leq 0V$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
I_{XA} I_{XB}	Output Leakage Current Power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = 15V$		0.01	0.15	mA
			$V_O = -15V$		−0.01	−0.15	mA

Switching Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_f	Differential Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 1)*		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
V_{CC} = 5V, V_{EE} = −5V, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_f	Differential Output Fall Time	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PDH}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 1)*		190	300	ns
t_{PZL}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF *(Figure 2)*		80	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1692 and across the 0°C to +70°C range for the DS3692. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Time Waveforms

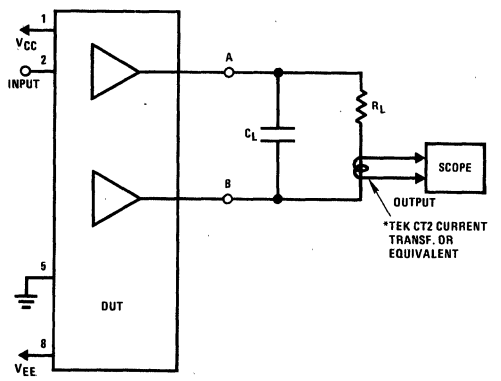

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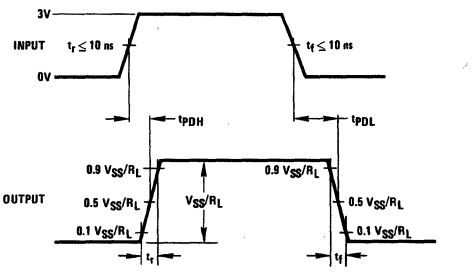
FIGURE 1. Differential Connection



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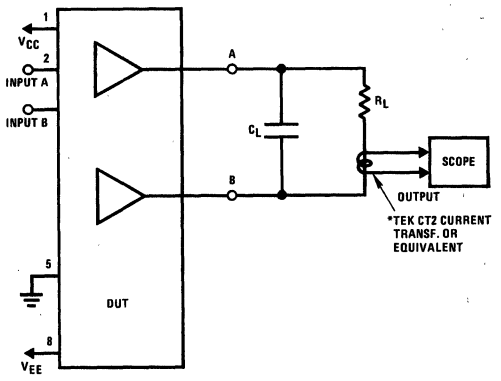

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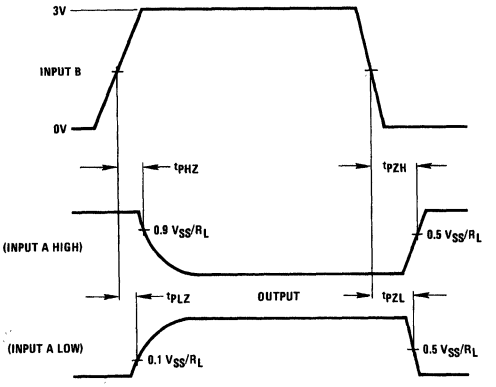

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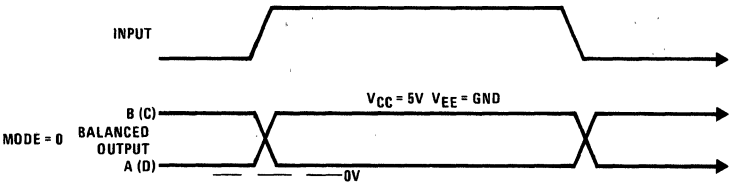
FIGURE 2. TRI-STATE Delays for DS1692/DS3692

Switching Waveforms



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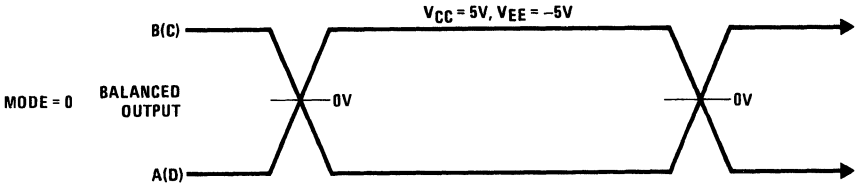


TL/F/5784–8

National Semiconductor

DS75110A
Dual Line Drivers

General Description

The DS75110A is a dual line driver with independent channels, common supply and ground terminals featuring constant current outputs. These drivers are designed for optimum performance when used with the DS75107, DS75108 line receivers.

The output current of the DS75110A is nominally 12 mA and may be switched to either of two output terminals with the appropriate logic levels at the driver input.

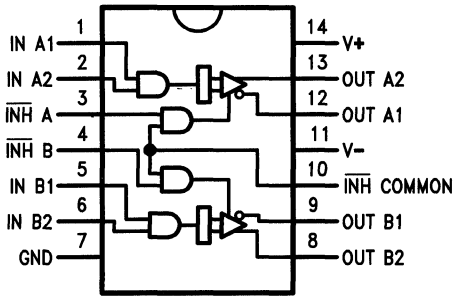
Separate or common control inputs are provided for increased logic versatility. These control or inhibit inputs allow the output current to be switched off (inhibited) by applying low logic levels to the control inputs. The output current in the inhibit mode, $I_{O(Off)}$, is specified so that minimum line loading is induced. This is highly desirable in system applications using party line data communications.

Features

- Improved stability over supply voltage and temperature ranges
- Constant current, high impedance outputs
- High speed: 15 ns max propagation delay
- Standard supply voltages
- Inhibitor available for driver selection
- High common mode output voltage range (−3.0V to 10V)
- TTL input compatibility

Connection Diagram

14-Lead Dual-In-Line Package and SO-14 Package



TL/F/9619–1

Top View

Order Number DS75110AM or DS75110AN
See NS Package Number M14A or N14A

Function Table

Inputs				Outputs	
Logic		Inhibitor			
1	2	A/B	$\overline{INH}$	A1/B1	A2/B2
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	Off	On
X	L	H	H	Off	On
H	H	H	H	On	Off

H = High, L = Low, X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range
- Ceramic DIP: −65°C to +175°C
- Molded DIP and SO-14: −65°C to +150°C

Lead Temperature
- Ceramic DIP (Soldering, 60 sec.): 300°C
- Molded DIP and SO-14 (Soldering, 10 sec.): 265°C

Maximum Power Dissipation* at 25°C
- Molded Package: 1040 mW
- SO Package: 930 mW

*Derate molded DIP package 8.3 mW/°C above 25°C; derate SO package 7.5 mW/°C above 25°C.

Suppy Voltage	±7.0V
Input Voltage (Any Input)	5.5V
Output Voltage (Any Output)	−5.0V to +12V

Recommended Operating Conditions

	DS75110A			Units
	Min	Typ	Max	
Positive Supply Voltage (V^+)	4.75	5.0	5.25	V
Negative Supply Voltage (V^-)	−4.75	−5.0	−5.25	V
Positive Common Mode Voltage (V_{CM}^+)	0		10	V
Negative Common Mode Voltage (V_{CM}^-)	0		−3.0	V
Operating Temperature (T_A)	0	25	70	°C

Electrical Characteristics

Over recommended operating temperature range, unless otherwise specified. (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input Voltage HIGH			2.0			V
V_{IL}	Input Voltage LOW					0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA		−0.9	−1.5	V
$I_{O(On)}$	On-State Output Current		V_{CC} = Max, V_O = 10V		12	15	mA
			V_{CC} = Min, V_O = −3.0V	6.5	12		
$I_{O(Off)}$	Off-State Output Current (Inhibited Only)		V_{CC} = Min, V_O = 10V			100	μA
I_I	Input Current At Maximum Input Voltage	A, B or C Inputs	V_{CC} = Max, V_I = 5.5V			1.0	mA
		D Input				2.0	
I_{IH}	Input Current HIGH	A, B or C Input	V_{CC} = Max, V_I = 2.4V			40	μA
		D Input				80	
I_{IL}	Input Current LOW	A, B or C Input	V_{CC} = Max, V_I = 0.4V			−3.0	mA
		D Input				−6.0	
$I^+_{(On)}$	Positive Supply Current with Driver Enabled		V_{CC} = Max, A & B Inputs at 0.4V, C & D Inputs at 2.0V		23	35	mA
$I^-_{(On)}$	Negative Supply Current with Driver Enabled				−34	−50	mA
$I^+_{(Off)}$	Positive Supply Current with Driver Inhibited		V_{CC} = Max, A, B, C & D Inputs at 0.4V		21		mA
$I^-_{(Off)}$	Negative Supply Current with Driver Inhibited				−17		mA

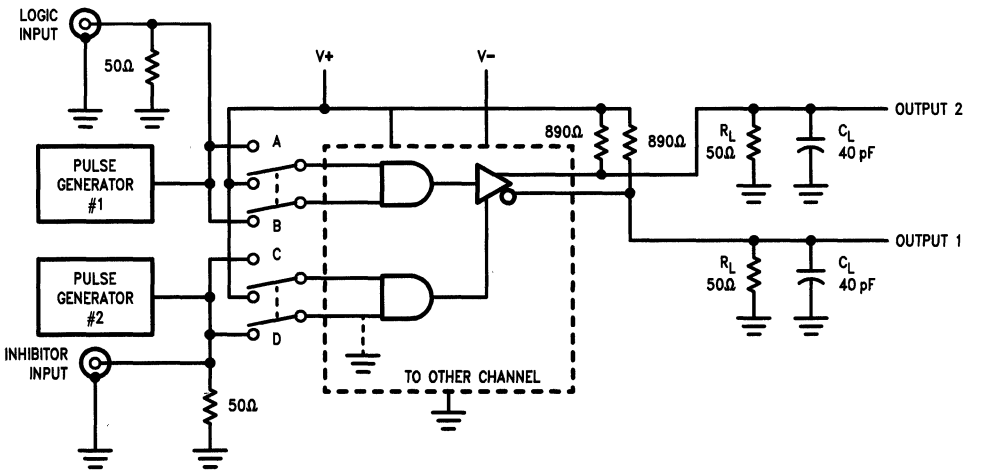
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across 0°C to +70°C range for the DS75110. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

Switching Characteristics $V_{CC} = \pm 5V, T_A = 25°C$

Symbol	Parameter	Conditions	From (Input)	To (Output)	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, LOW to HIGH	C_L = 40 pF, R_L = 50Ω See Test Circuit	A or B	1 or 2		9.0	15	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					9.0	15	ns
t_{PLH}	Propagation Delay Time, LOW to HIGH		C or D	1 or 2		16	25	ns
t_{PHL}	Propagation Delay Time, HIGH to LOW					13	25	ns



TL/F/9619–3

Note 1: The pulse generators have the following characteristics:
$t_r = t_f = 10$ ns ±5.0 ns, $t_{W1} = 500$ ns, PRR = 1.0 MHz, $t_{W2} = 1.0$ µs, PRR = 500 kHz, $Z_O = 50\Omega$.

Note 2: C_L includes probe and jib capacitance.

Note 3: For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 2. AC Test Circuit

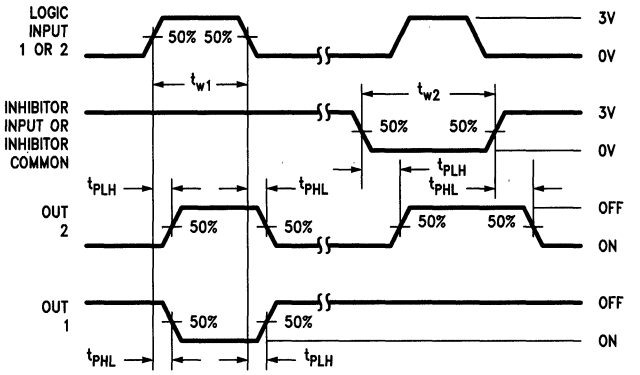


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FIGURE 3. AC Waveforms

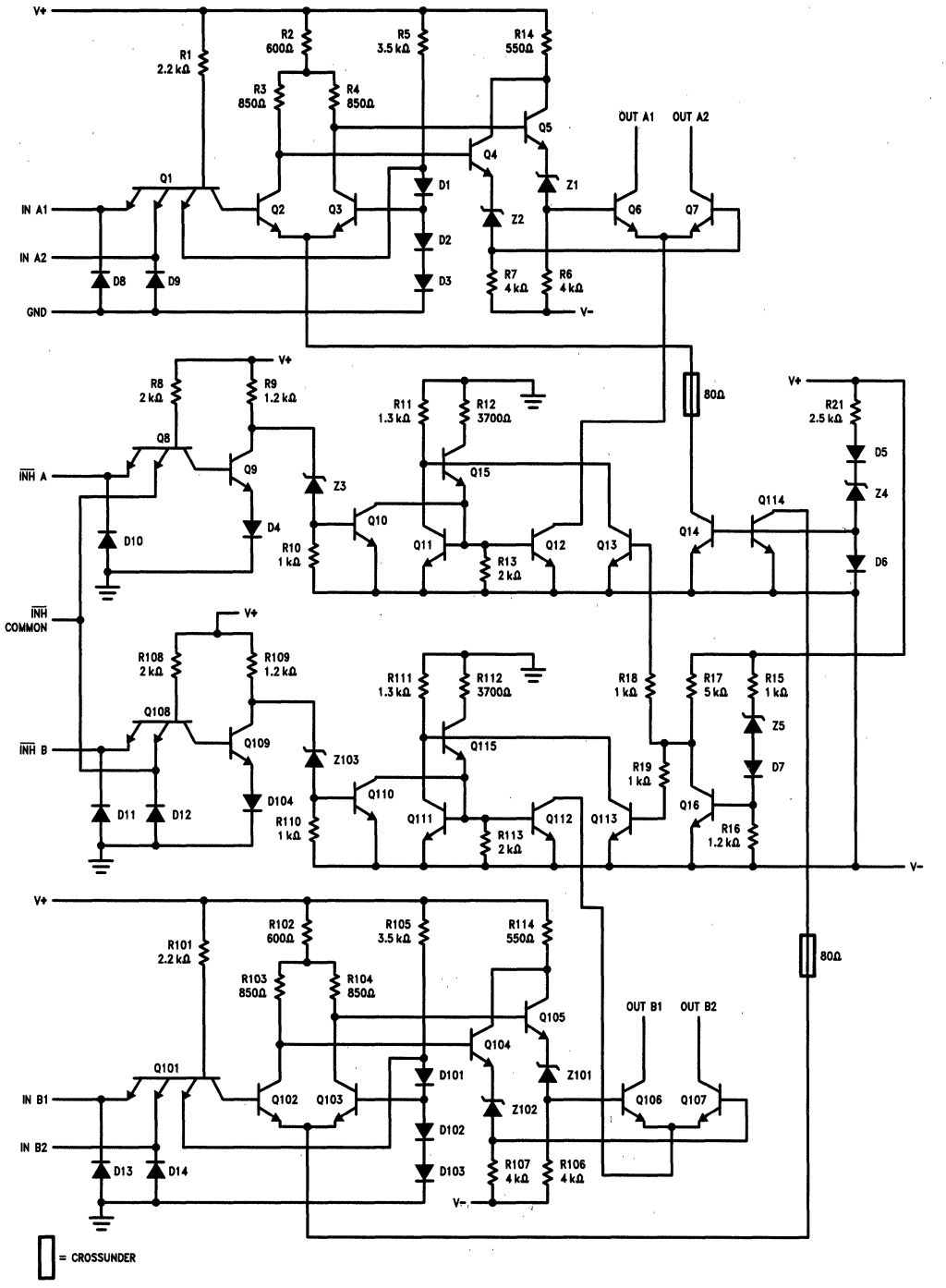

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FIGURE 1. Equivalent Circuit

Typical Applications

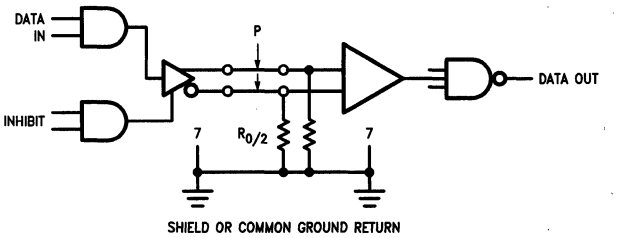

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FIGURE 4. Simplex Operation

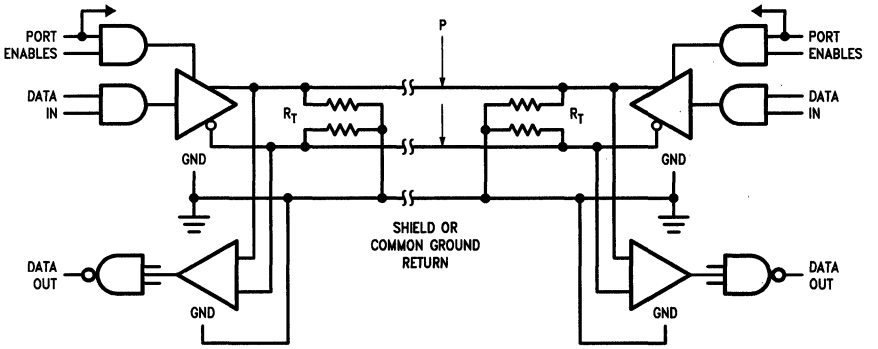

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FIGURE 5. Half-Duplex Operation

Note 1: All drivers are DS75110A. Receivers are DS75107 or DS75108. Twisted-pair or coaxial transmission line should be used for minimum noise and cross talk.

Note 2: When only one driver in a package is being used, the outputs of the other driver should either be grounded or inhibited to reduce power dissipation.

National Semiconductor

DS55113/DS75113 Dual TRI-STATE® Differential Line Driver

General Description

The DS55113/DS75113 dual differential line drivers with TRI-STATE outputs are designed to provide all the features of the DS55114/DS75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

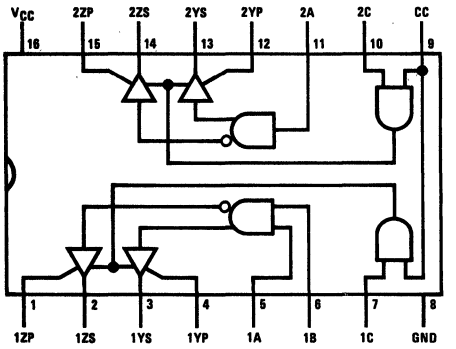
The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

Features

- Each circuit offers a choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- High-impedance output state for party-line applications
- Short-circuit protection
- High current outputs
- Single-ended or differential AND/NAND outputs
- Common and individual output controls
- Clamp diodes at inputs
- Easily adaptable to DS55114/DS75114 applications

Connection Diagram

Dual-In-Line Package



Positive logic: $Y = AB$
$Z = \overline{AB}$

Output is OFF when C or CC is low

TL/F/5785–1

Top View
Order Number DS55113J, DS75113M or DS75113N
See NS Package Number J16A, M16A or N16A

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS55113J/883
See NS Package Number J16A

Truth Table

Inputs				Outputs	
Output Control		Data		AND	NAND
C	CC	A	B*	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H*
H	H	X	L	L	H
H	H	H	H	H	L

H = high level
L = low level
X = irrelevant
Z = high impedance (OFF)
*B input and 4th line of truth table applicable only to driver number 1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 1) 7V

Input Voltage 5.5V

OFF-State Voltage Applied to Open-Collector Outputs 12V

Maximum Power Dissipation* at 25°C

- Cavity Package 1433 mW
- Molded DIP Package 1362 mW
- SO Package 1002 mW

Operating Free-Air Temperature Range

- DS55113 −55°C to +125°C
- DS75113 0°C to +70°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C (Note 2).

Storage Temperature Range −65°C to +150°C

Lead Temperature (1/16" from case for 60 seconds): J Package 300°C

Lead Temperature (1/16" from case for 4 seconds): N Package 260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS55113	4.5	5.5	V
DS75113	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55113	−55	125	°C
DS75113	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Conditions (Note 3)			DS55113 Min	DS55113 Typ (Note 4)	DS55113 Max	DS75113 Min	DS75113 Typ (Note 4)	DS75113 Max	Units
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage							0.8			0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output Clamp Voltage		V_{CC} = Max, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-State Open-Collector Output Current		V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-State (High-Impedance-State) Output Current		V_{CC} = Max, Output Controls at 0.8V	T_A = 25°C, V_O = 0 to V_{CC}				±10			±10	μA
				T_A = Max	V_O = 0V			−150			−20	
					V_O = 0.4V			±80			±20	
					V_O = 2.4V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input Current at Maximum Input Voltage	A, B, C	V_{CC} = Max, V_I = 5.5V					1			1	mA
		CC						2			2	
I_{IH}	High Level Input Current	A, B, C	V_{CC} = Max, V_I = 2.4V					40			40	μA
		CC						80			80	
I_{IL}	Low Level Input Current	A, B, C	V_{CC} = Max, V_I = 0.4V					−1.6			−1.6	mA
		CC						−3.2			−3.2	

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions (Note 3)		DS55113			DS75113			Units
				Min	Typ (Note 4)	Max	Min	Typ (Note 4)	Max	
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V		−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	All Inputs at 0V, No Load T_A = 25°C	V_{CC} = Max		47	65		47	65	mA
			V_{CC} = 7V		65	85		65	85	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters with the exception of OFF-state open-collector output current are measured with the active pull-up connected to the sink output.

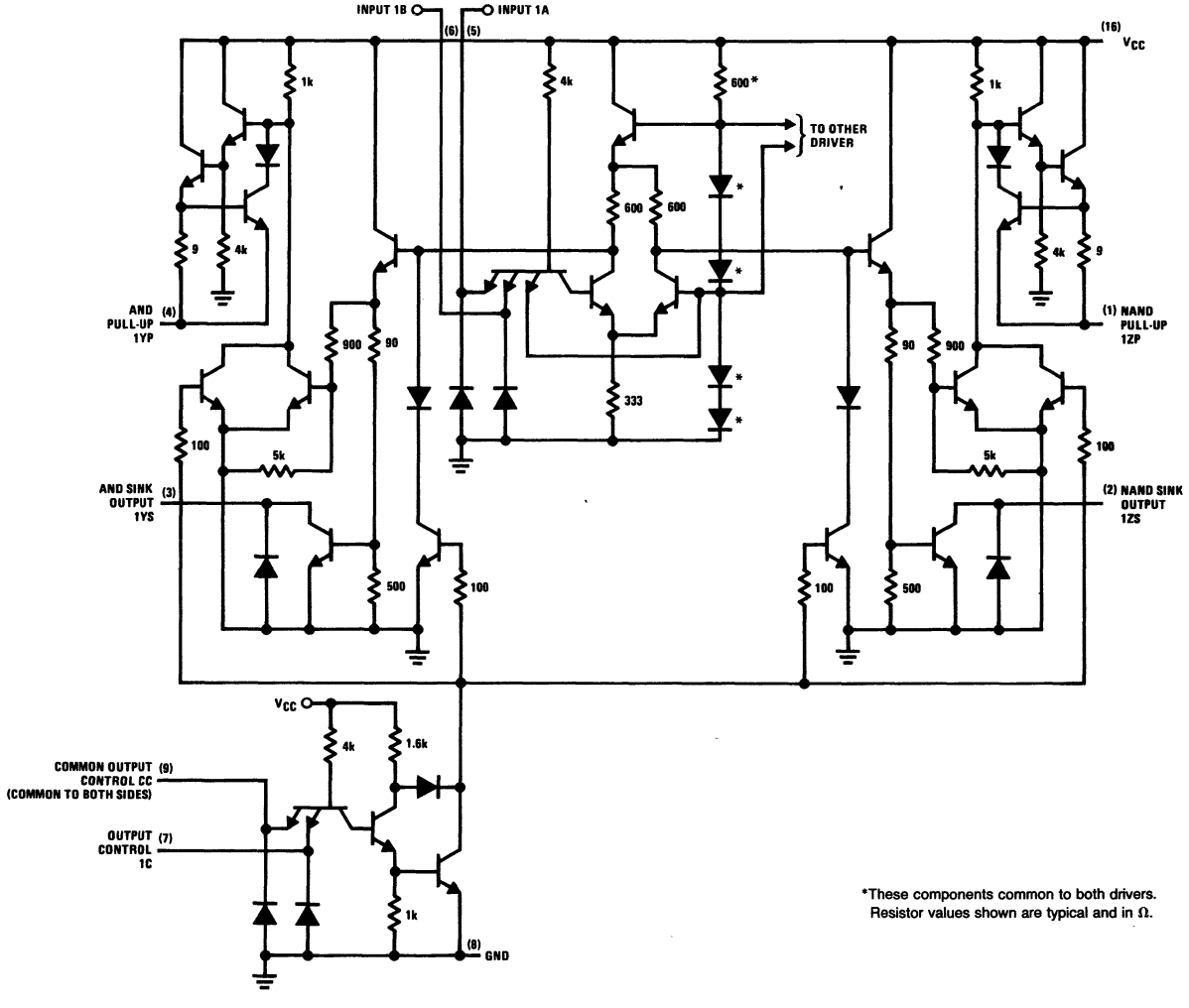
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

Symbol	Parameter	Conditions	DS55113			DS75113			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to High-Level Output	*(Figure 1)*		13	20		13	30	ns
t_{PHL}	Propagation Delay Time, High-to Low-Level Output			12	20		12	30	ns
t_{PZH}	Output Enable Time to High Level	R_L = 180Ω, *(Figure 2)*		7	15		7	20	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 250Ω, *(Figure 3)*		14	30		14	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 180Ω, *(Figure 2)*		10	20		10	30	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 250Ω, *(Figure 3)*		17	35		17	35	ns

Schematic Diagram (One side shown only)



*These components common to both drivers.
Resistor values shown are typical and in Ω.

TL/F/5785–2

AC Test Circuits and Switching Time Waveforms

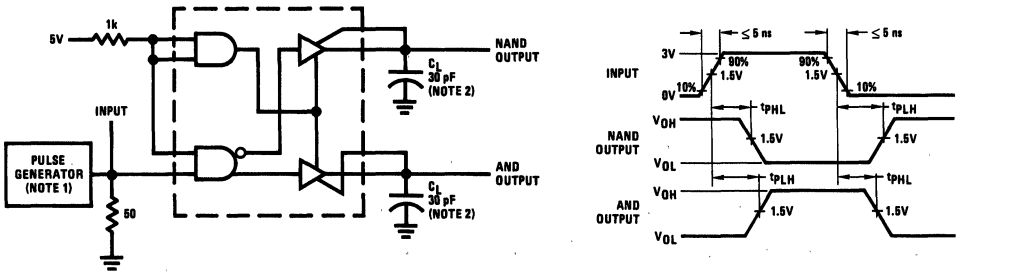


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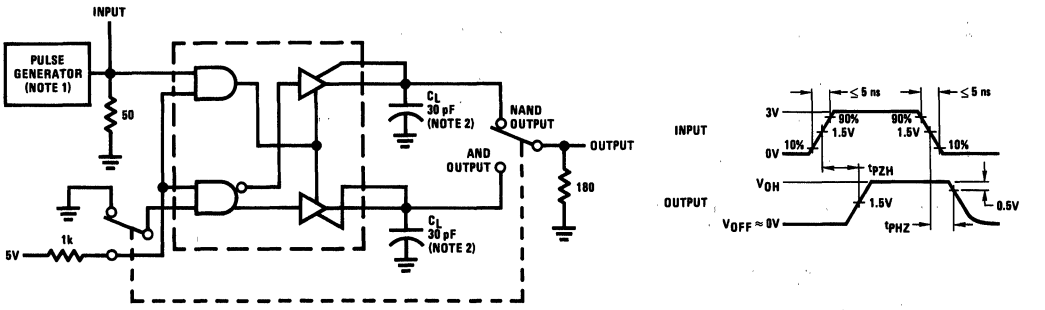
FIGURE 1. t_{PLH} and t_{PHL}



TL/F/5785–4

FIGURE 2. t_{PZH} and t_{PHZ}

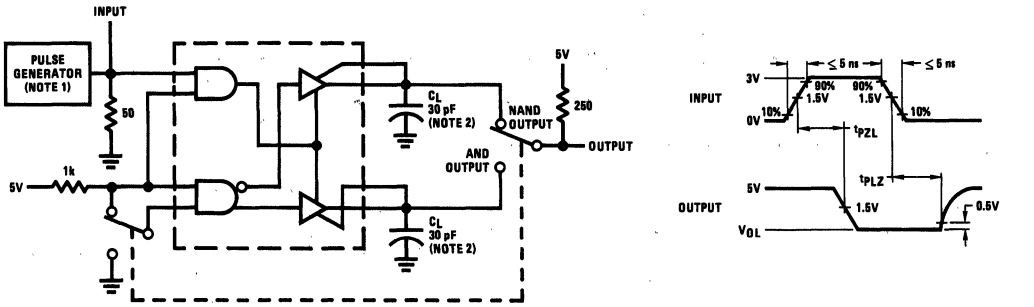


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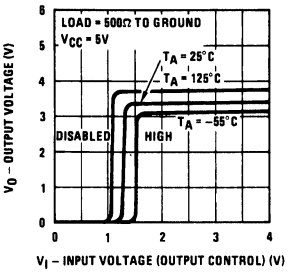
FIGURE 3. t_{PZL} and t_{PLZ}

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 500 kHz, t_W = 100 ns.

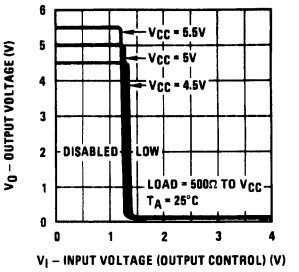
Note 2: C_L includes probe and jig capacitance.

Typical Performance Characteristics*

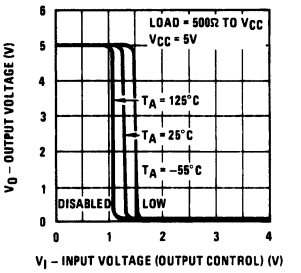
Output Voltage vs Output Control Voltage



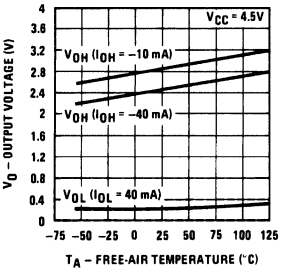
Output Voltage vs Output Control Voltage



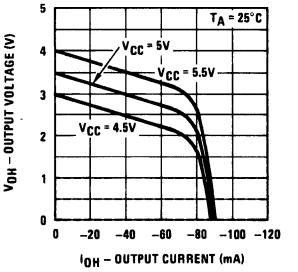
Output Voltage vs Output Control Voltage



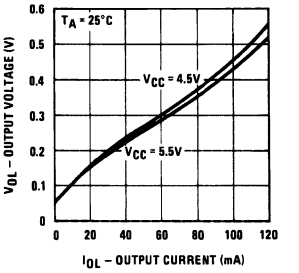
Output Voltage vs Free-Air Temperature



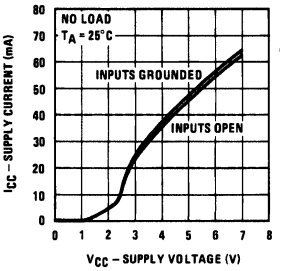
High Level Output Voltage vs Output Current



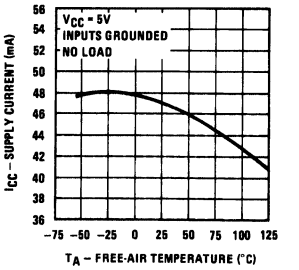
Low Level Output Voltage vs Output Current



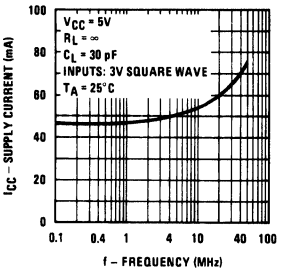
Supply Current (Both Drivers) vs Supply Voltage



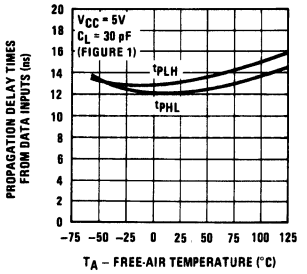
Supply Current (Both Drivers) vs Free-Air Temperature



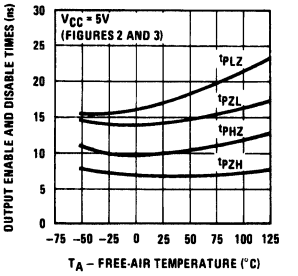
Supply Current (Both Drivers) vs Frequency



Propagation Delay Times from Data Inputs vs Free-Air Temperature



Output Enable and Disable Times vs Free-Air Temperature



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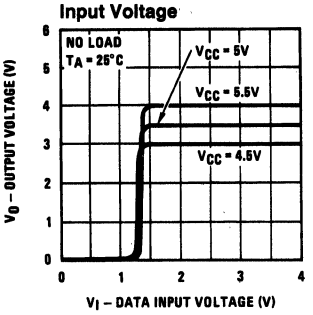
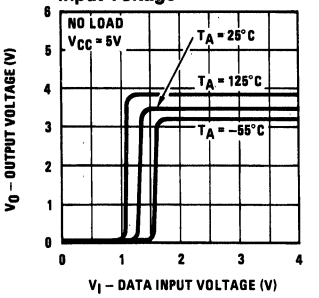
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

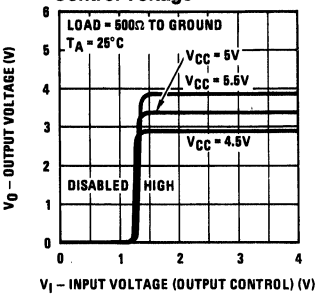
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



Output Voltage vs Output Control Voltage



TL/F/5785–6

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor

DS75114 Dual Differential Line Drivers

General Description

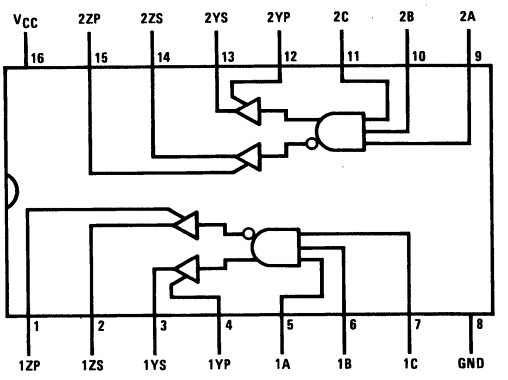
The DS75114 dual differential line driver is designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

Features

- Each circuit offers a choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- Designed to be interchangeable with Fairchild 9614 line drivers
- Short-circuit protection of outputs
- High current outputs
- Clamp diodes at inputs and outputs to terminate line transients
- Single-ended or differential AND/NAND outputs
- Triple inputs

Connection Diagram

Dual-In-Line Package



TL/F/5786–1

Top View

Positive logic: $Y = ABC$

$Z = \overline{ABC}$

Order Number DS75114N
See NS Package Number N16A

Truth Table

Inputs			Outputs	
A	B	C	Y	Z
H	H	H	H	L
All Other Input Combinations			L	H

H = high level

L = low level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55114	−55°C to +125°C
DS75114	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature ($\frac{1}{16}$" from case for 60 seconds): J Package	300°C
Lead Temperature ($\frac{1}{16}$" from case for 4 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C (Note 2).

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS75114	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS75114	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)			DS75114 Min	DS75114 Typ (Note 4)	DS75114 Max	Units
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V		I_{OH} = −10 mA	2.4	3.4		V
		V_{IL} = 0.8V		I_{OH} = −40 mA	2	3.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.2	0.45	V
V_{OK}	Output Clamp Voltage	V_{CC} = 5V, I_O = 40 mA, T_A = 25°C				6.1	6.5	V
		V_{CC} = Max, I_O = −40 mA, T_A = 25°C				−1.1	−1.5	V
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°				μA
				T_A = 125°C				μA
			V_{OH} = 5.25V	T_A = 25°C		1	100	μA
				T_A = 70°C			200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	−1.6	mA
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0V			−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	Inputs Grounded, No Load, T_A = 25°C		V_{CC} = Max		37	50	mA
				V_{CC} = 7V		47	70	mA

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters, with the exception of OFF-state open-collector output current, are measured with the active pull-up connected to the sink output.

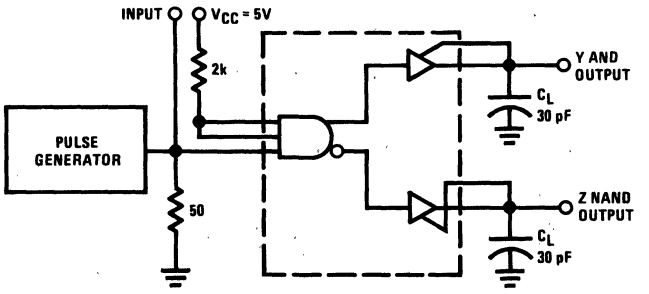
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	DS75114			Units
			Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 30 pF, *(Figure 1)*		15	30	ns
t_{PHL}	Propagation Delay Time High-to-Low-Level Output			11	30	ns

AC Test Circuit and Switching Time Waveforms



TL/F/5786–3

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_w = 100 ns, PRR = 500 kHz.

Note 2: C_L includes probe and jig-capacitance.

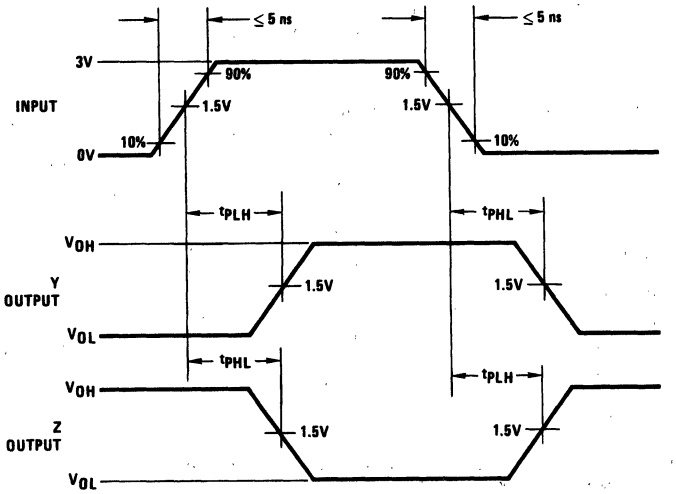


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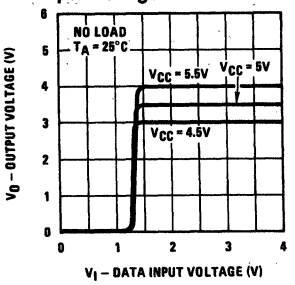
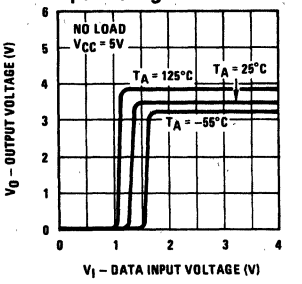
FIGURE 1. (Notes 1, 2)

Typical Performance Characteristics*

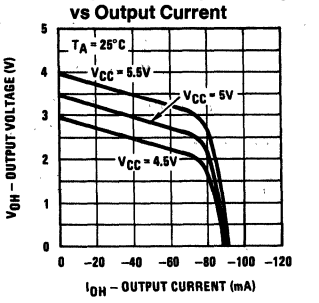
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



High Level Output Voltage vs Output Current



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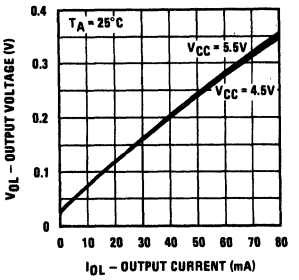
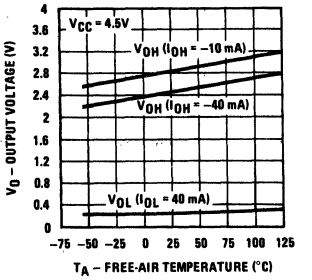
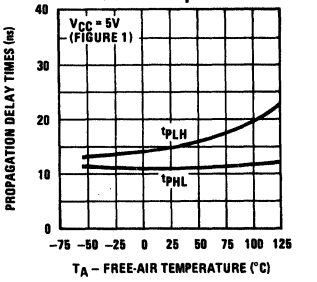
Low Level Output Voltage vs Output Current



Output Voltage vs Free-Air Temperature

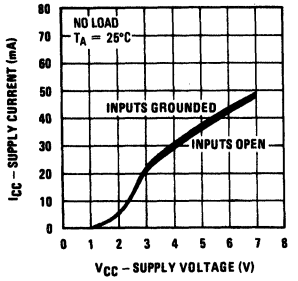


Propagation Delay Times vs Free-Air Temperature

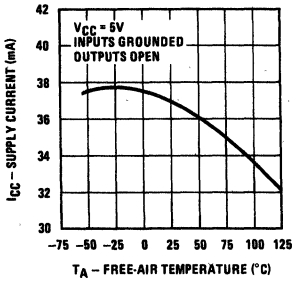


TL/F/5786–6

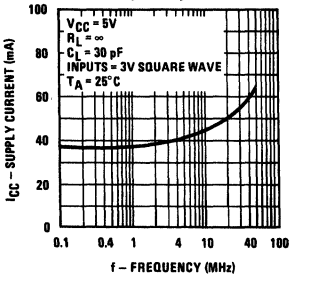
Supply Current (Both Drivers) vs Supply Voltage



Supply Current (Both Drivers) vs Free-Air Temperature



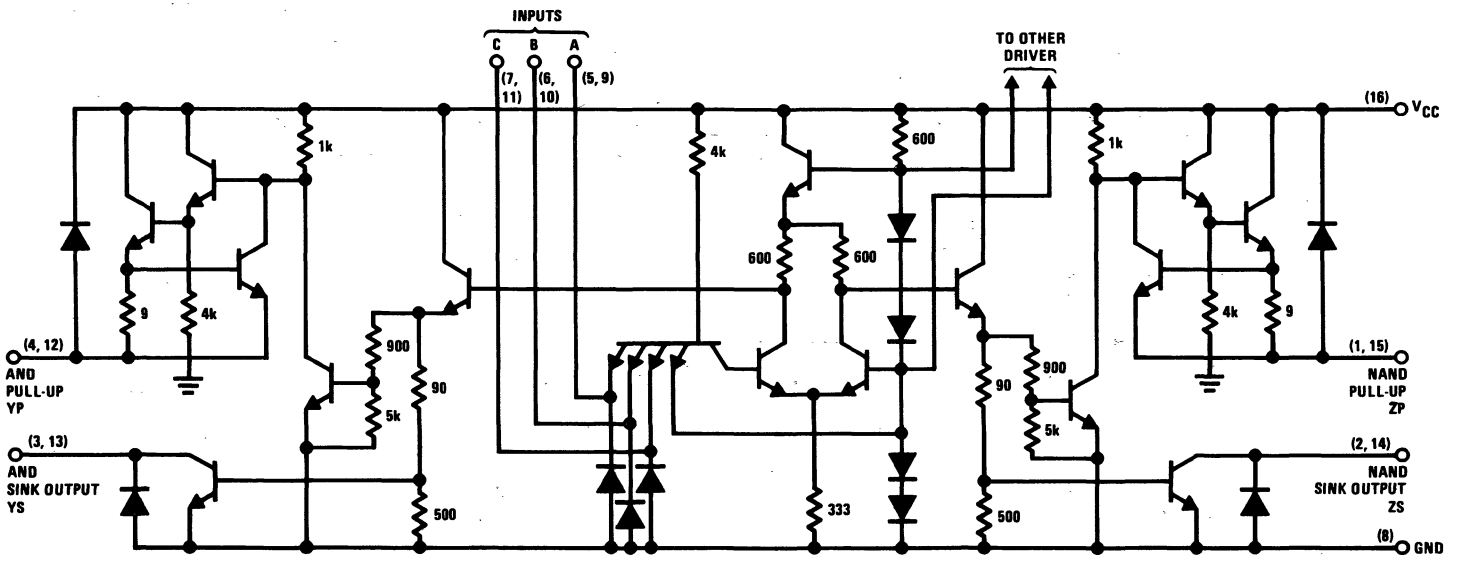
Supply Current (Both Drivers) vs Frequency



TL/F/5786–7

*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Schematic Diagram (Each Driver)



Resistor values shown are typical and in ohms.

TL/F/5786–2

National Semiconductor

DS75121 Dual Line Drivers

General Description

The DS75121 is a monolithic dual line driver designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50Ω to 500Ω. It is compatible with standard TTL logic and supply voltage levels.

The DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

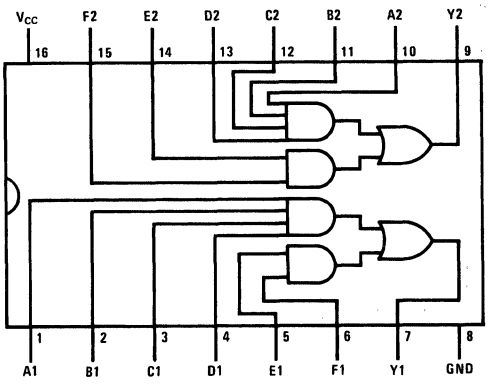
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Designed for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN75121 and the 8T13

Connection Diagram

Dual-In-Line Package

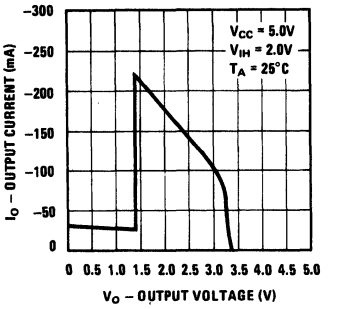


TL/F/5788–1

Top View
Order Number DS75121N
See NS Package Number N16A

Typical Performance Characteristics

Output Current vs Output Voltage



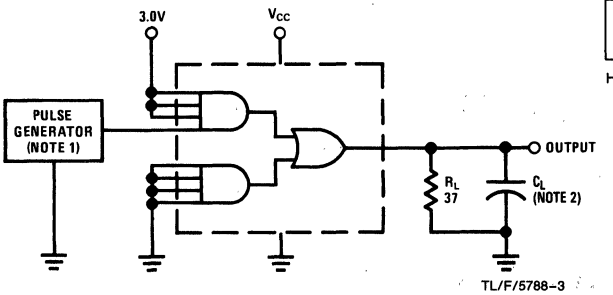
TL/F/5788–2

Truth Table

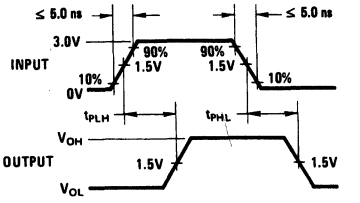
Inputs						Output
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = High Level, L = Low Level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



TL/F/5788–3



TL/F/5788–4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, t_r = t_f = 5.0 ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Maximum Power Dissipation* at 25°C Molded Package	1280 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS75121	0	+75	°C

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	μA
I_{IH}	High Level Input Current	V_I = 4.5V			40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See AC Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

DS75123 Dual Line Driver

General Description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

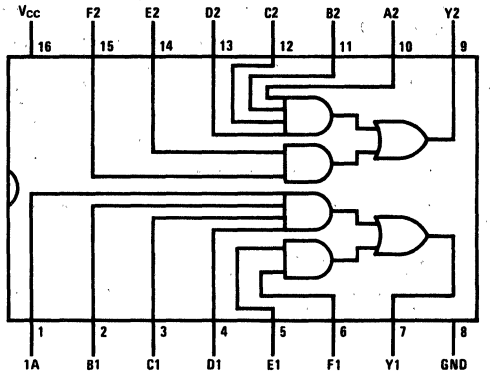
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

Connection Diagram

Dual-In-Line Package



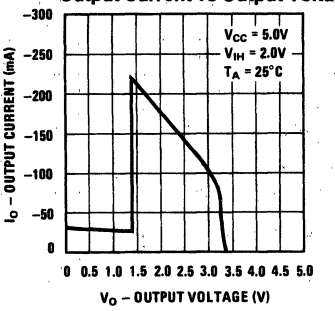
TL/F/5790–1

Top View

Order Number DS75123N
See NS Package Number N16A

Typical Performance Characteristics

Output Current vs Output Voltage



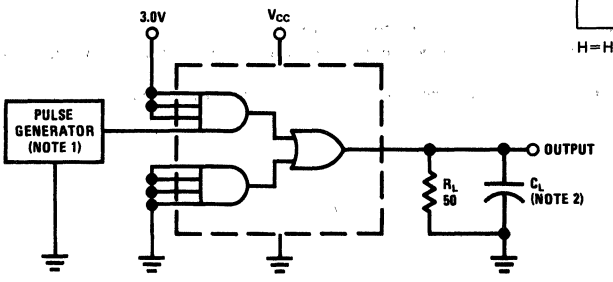
TL/F/5790–3

Truth Table

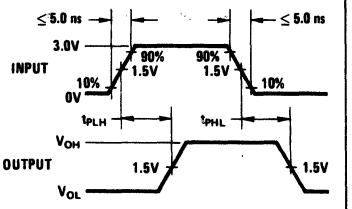
INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = High level, L = Low level, X = Irrelevant

AC Test Circuit and Switching Time Waveforms



TL/F/5790–2



TL/F/5790–4

Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Maximum Power Dissipation* at 25°C Molded Package	1280 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
V_{OH}	High Level Output Voltage	V_{CC} = 5.0V, V_{IH} = 2.0V, I_{OH} = −59.3 mA, (Note 4)	T_A = 25°C	3.11			V
			T_A = 0°C to +75°C	2.9			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, V_{OH} = 2.0V, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	V_{IL} = 0.8V, I_{OL} = −240 μA, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0, V_O = 3.0V				40	μA
I_{IH}	High Level Input Current	V_I = 4.5V				40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open				60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 50Ω, (See AC Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 50Ω, (See AC Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

DS7830/DS8830 Dual Differential Line Driver

General Description

The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

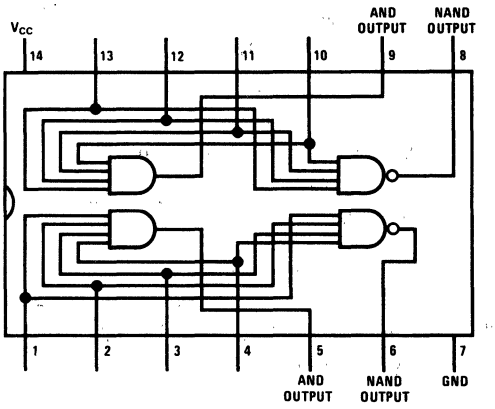
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Connection Diagram

Dual-In-Line and Flat Package



TL/F/5799–2

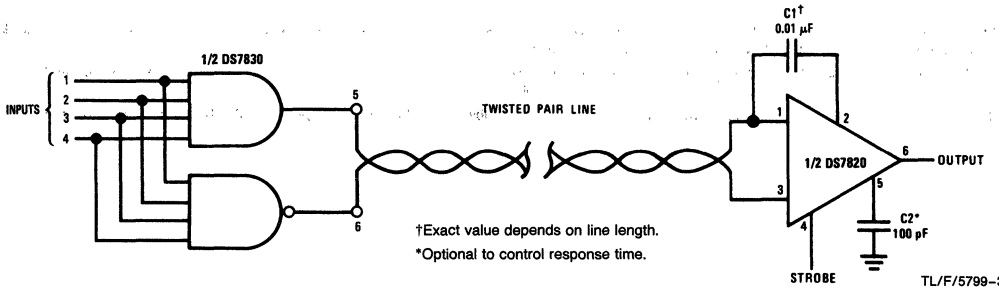
Top View

Order Number DS8830N
See NS Package Number N14A

For Complete Military 883 Specificatons, See RETS Data Sheet.
Order Number DS7830J/883 or DS7830W/883
See NS Package Number J14A

Typical Application

Digital Data Transmission



†Exact value depends on line length.
*Optional to control response time.

TL/F/5799–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Output Short Circuit Duration (125°C)	1 second
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS8730	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V	I_{OUT} = −0.8 mA	2.4			V
			I_{OUT} = 40 mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	I_{OUT} = 32 mA		0.2	0.4	V
			I_{OUT} = 40 mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				120	μA
		V_{IN} = 5.5V				2	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−4.8	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V, T_A = 125°C, (Note 4)		−40	−100	−120	mA
I_{CC}	Supply Current	V_{IN} = 5.0V, (Each Driver)			11	18	mA
V_I	Input Clamp	V_{CC} = Min, I_{IN} = − 12 mA			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay AND Gate	R_L = 400Ω, C_L = 15 pF *(Figure 1)*		8	12	ns
t_{pd0}				11	18	ns
t_{pd1}	Propagation Delay NAND Gate	R_L = 400Ω, C_L = 15 pF *(Figure 1)*		8	12	ns
t_{pd0}				5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

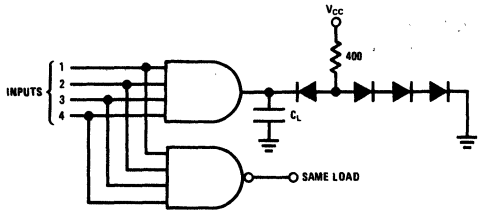
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



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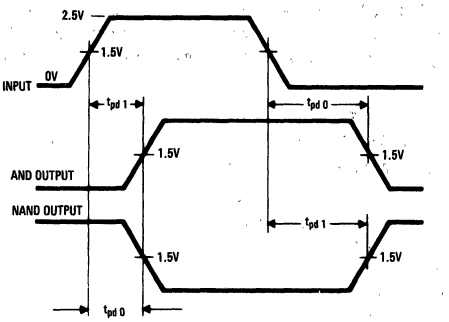
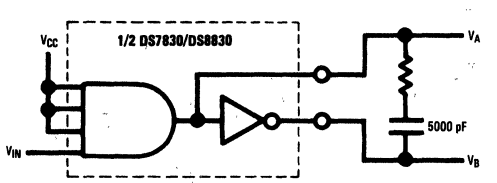


f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty cycle = 50%

TL/F/5799–9

FIGURE 1



TL/F/5799–8

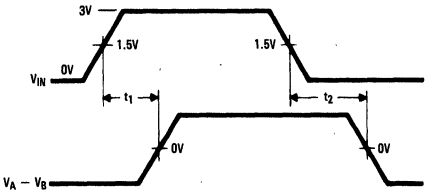


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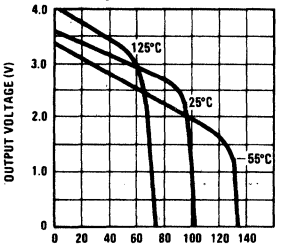
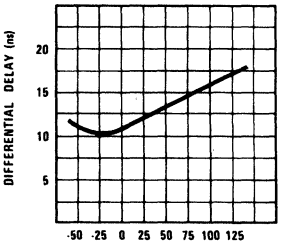
FIGURE 2

Typical Performance Characteristics

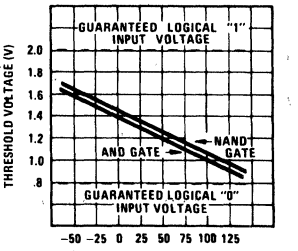
Output High Voltage (Logical "1") vs Ouput Current



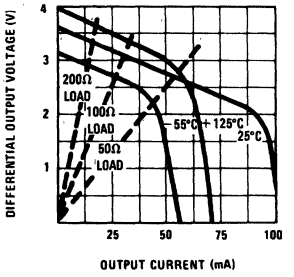
Differential Delay vs Temperature



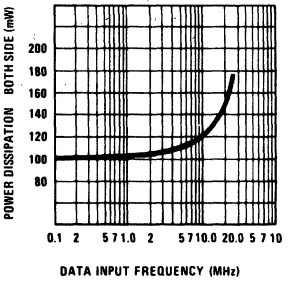
Threshold Voltage vs Temperature



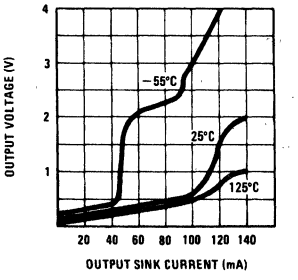
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) vs Differential Output Current



Power Dissipation (No Load) vs Data Input Frequency



Output Low Voltage (Logical "0") vs Output Current



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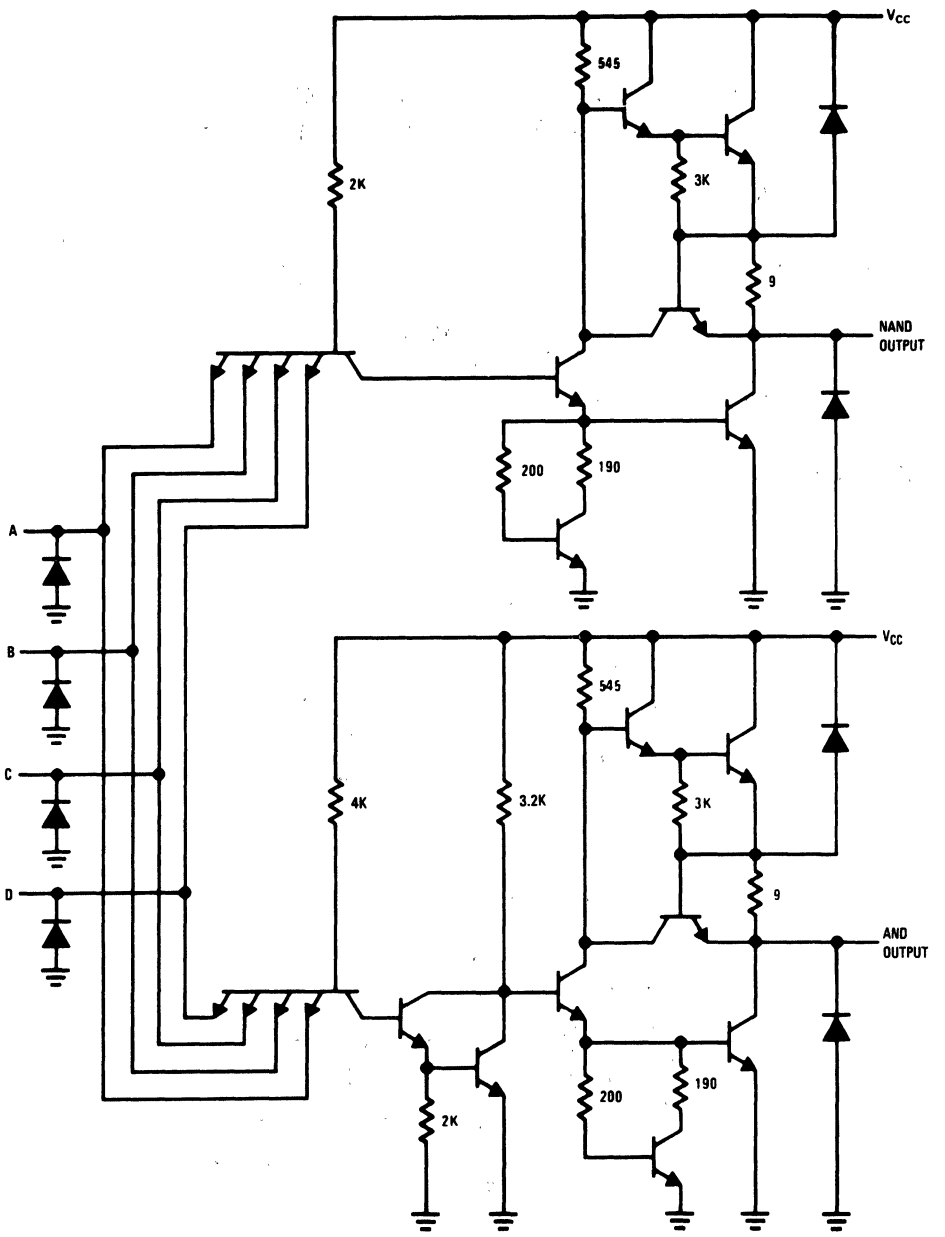
Schematic Diagram



TL/F/5799–1

*2 Per Package

National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

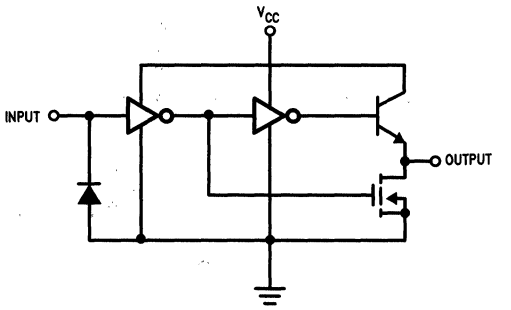
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low output ON resistance — 20Ω (typ.)

Logic Diagrams

1/4 MM78C29/MM88C29



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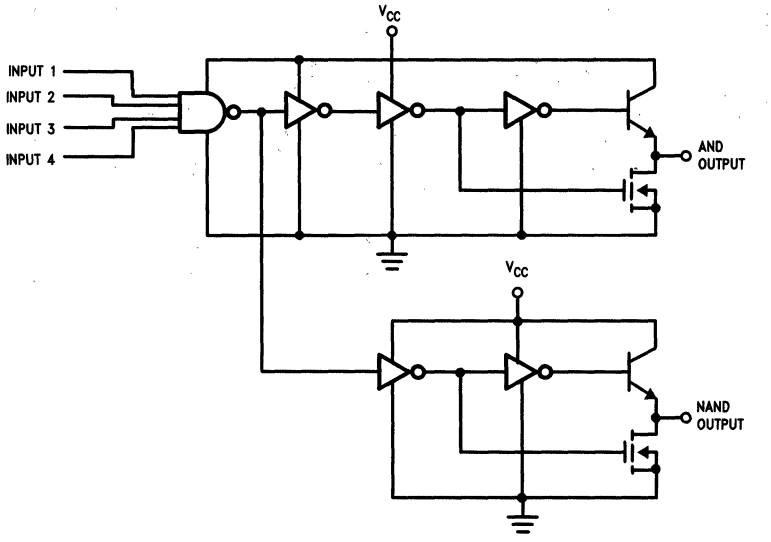
1/2 MM78C30/MM88C30



TL/F/5908–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +16V
Operating Temperature Range	
MM78C29/MM78C30	−55°C to +125°C
MM88C29/MM88C30	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Average Current at Output	
MM78C30/MM88C30	50 mA
MM78C29/MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature	
(Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	100	mA
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V, V_{CC} ≥ 4.5V, T_j = 25°C T_j = 125°C	 −57 −32	 −80 −50		 mA mA
	MM88C29/MM88C30	V_{OUT} = V_{CC} − 1.6V, V_{CC} ≥ 4.75V, T_j = 25°C T_j = 85°C	 −47 −32	 −80 −60		 mA mA
	MM78C29/MM88C29 MM78C30/MM88C30	V_{OUT} = V_{CC} − 0.8V V_{CC} ≥ 4.5V	−2	−20		mA
I_{SINK}	Output Sink Current MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.5V, T_j = 25°C T_j = 125°C	 11 8	 20 14		 mA mA
		V_{OUT} = 0.4V, V_{CC} = 10V, T_j = 25°C T_j = 125°C	 22 16	 40 28		 mA mA
	MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V, T_j = 25°C T_j = 85°C	 9.5 8	 22 18		 mA mA
		V_{OUT} = 0.4V, V_{CC} = 10V, T_j = 25°C T_j = 125°C	 19 15.5	 40 33		 mA mA
I_{SOURCE}	Output Source Resistance MM78C29/MM78C30	V_{OUT} = V_{CC} − 1.6V, V_{CC} ≥ 4.5V, T_j = 25°C T_j = 125°C		 20 32	 28 50	 Ω Ω
	MM88C29/MM88C30	V_{OUT} = V_{CC} − 1.6V, V_{CC} ≥ 4.75V, T_j = 25°C T_j = 85°C		 20 27	 34 50	 Ω Ω

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DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (Continued)						
I_{SINK}	Output Sink Resistance MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.50V, T_j = 25°C T_j = 125°C		 20 28	 36 50	 Ω Ω
		V_{OUT} = 0.4V, V_{CC} = 10V, T_j = 25°C T_j = 125°C		 10 14	 18 25	 Ω Ω
	MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V, T_j = 25°C T_j = 85°C		 18 22	 41 50	 Ω Ω
		V_{OUT} = 0.4V, V_{CC} = 10V, T_j = 25°C T_j = 85°C		 10 12	 21 26	 Ω Ω
	Output Resistance Temperature Coefficient Source Sink			 0.55 0.40		 %/°C %/°C
θ_{JA}	Thermal Resistance MM78C29/MM78C30 (D-Package)			100		°C/W
	MM88C29/MM88C30 (N-Package)			150		°C/W

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0" MM78C29/MM88C29	 (See *Figure 2*) V_{CC} = 5V V_{CC} = 10V		 80 35	 200 100	 ns ns
	MM78C30/MM88C30	V_{CC} = 5V V_{CC} = 10V		110 50	350 150	ns ns
t_{pd}	Differential Propagation Delay Time to Logical "1" or "0" MM78C30/MM88C30	R_L = 100Ω, C_L = 5000 pF (See *Figure 1*) V_{CC} = 5V V_{CC} = 10V		 400 150		 ns ns
C_{IN}	Input Capacitance MM78C29/MM88C29 MM78C30/MM88C30	 (Note 3) (Note 3)		 5.0 5.0		 pF pF
C_{PD}	Power Dissipation Capacitance MM78C29/MM88C29 MM78C30/MM88C30	 (Note 3) (Note 3)		 150 200		 pF pF

*AC Parameters are guaranteed by DC correlated testing.

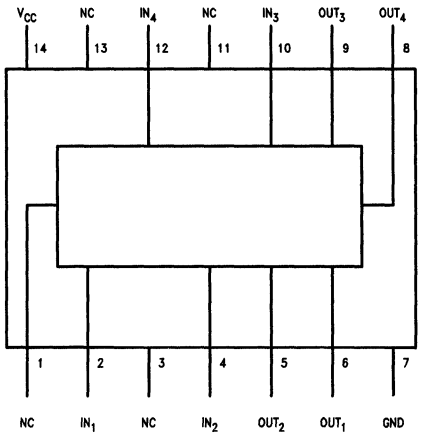
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90 (CMOS Logic Databook).

Connection Diagrams

Dual-In-Line Package
MM78C29/MM88C29



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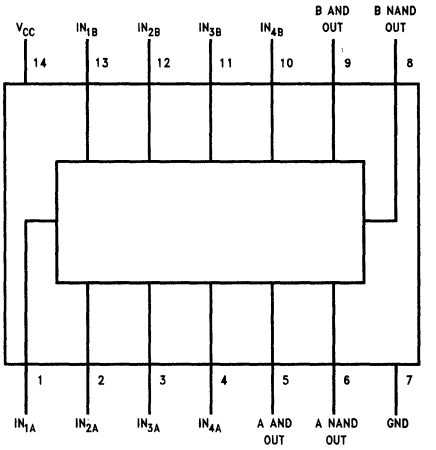
Top View

Order Number MM88C29M or MM88C29N

Dual-In-Line Package
MM78C30/MM88C30



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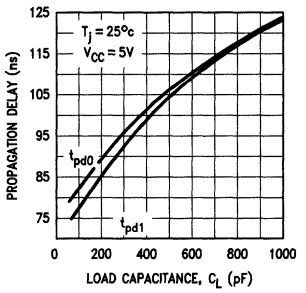
Top View

Order Number MM88C30M or MM88C30N

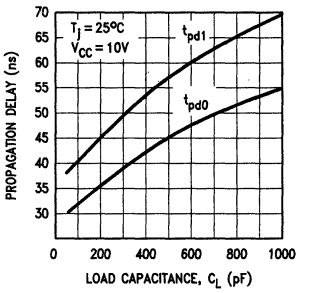
For Complete Military 883 Specifications, see RETS Data Sheet.
Order Number MM78C29J/883, MM78C29W/883, MM78C30J/883 or MM78C30W/883

Typical Performance Characteristics

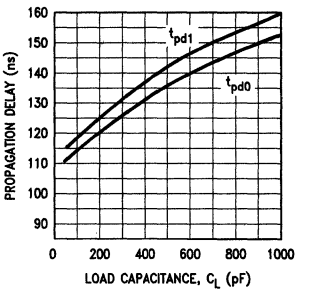
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



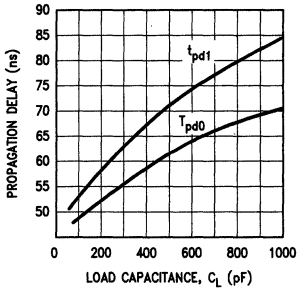
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



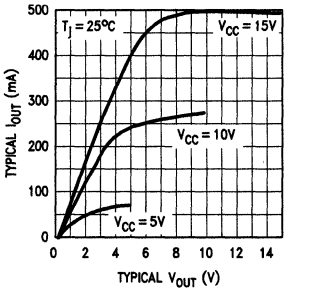
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



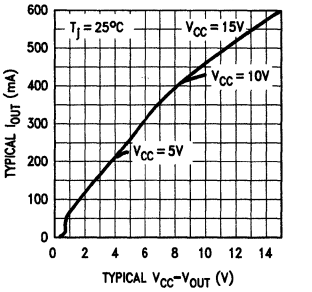
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



Typical Sink Current vs Output Voltage



Typical Source Current vs Output Voltage



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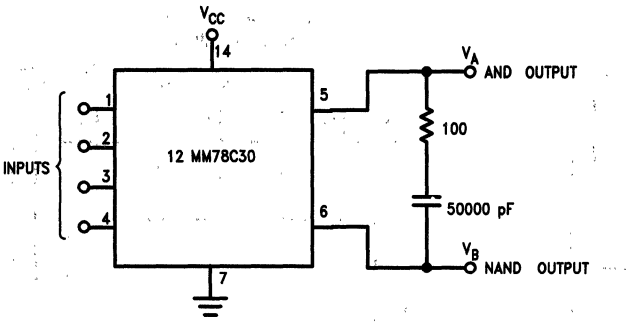
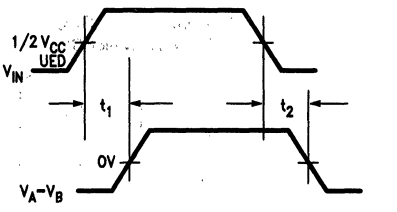
AC Test Circuits

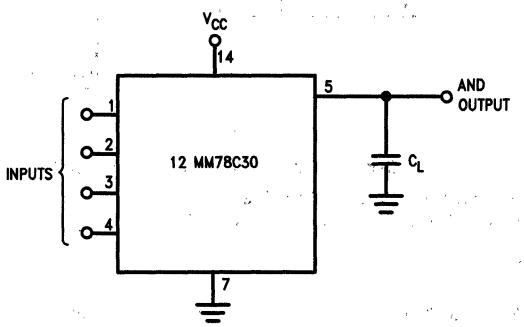


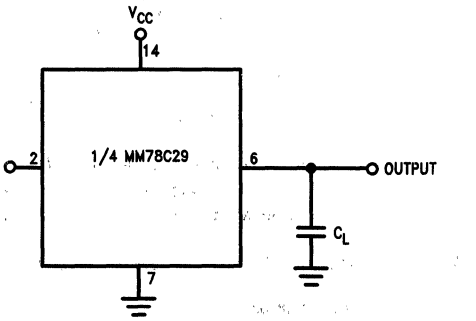


TL/F/5908–7

TL/F/5908–6

FIGURE 1





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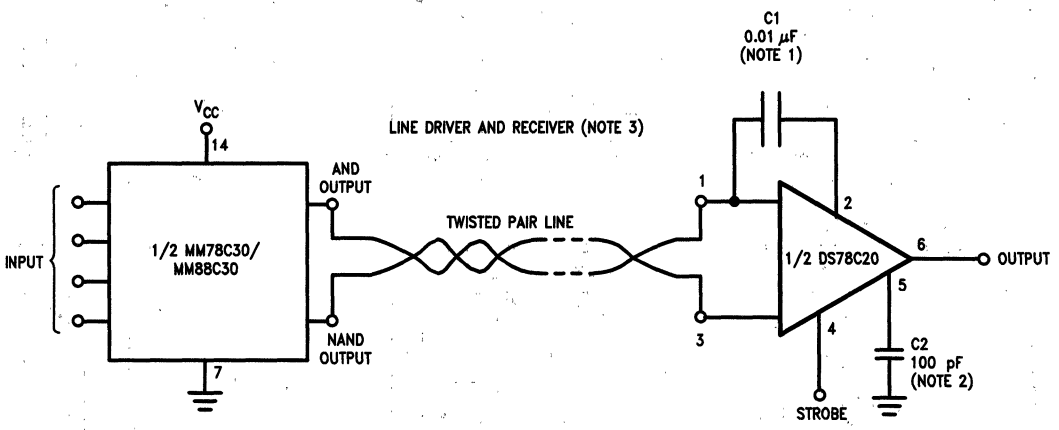
TL/F/5908–9

FIGURE 2

Typical Applications

Digital Data Transmission



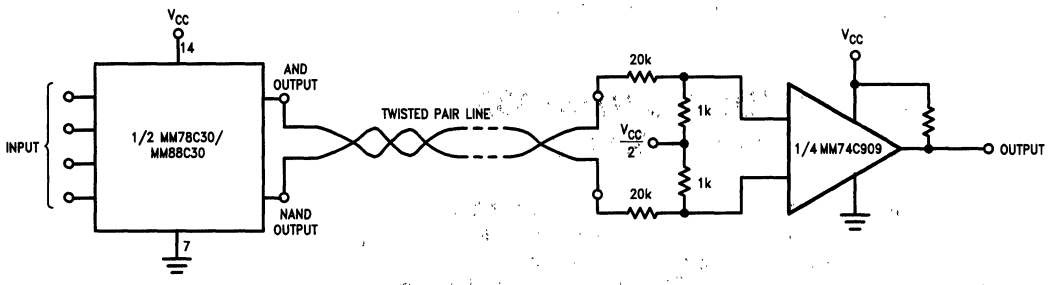
TL/F/5908–10

Note 1: Exact value depends on line length.

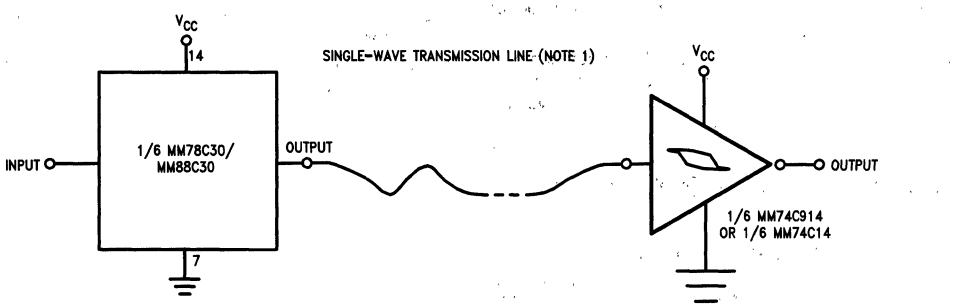
Note 2: Optional to control response time.

Note 3: V_{CC} = 4.5V to 5.5V for the DS7820, V_{CC} = 4.5V to 15V for the DS78C20.

Typical Applications (Continued)



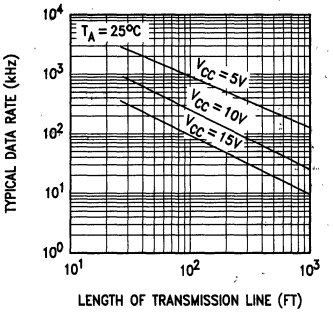
TL/F/5908–11



TL/F/5908–12

Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



TL/F/5908–13

Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

National Semiconductor

DS7831/DS8831/DS7832/DS8832
Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

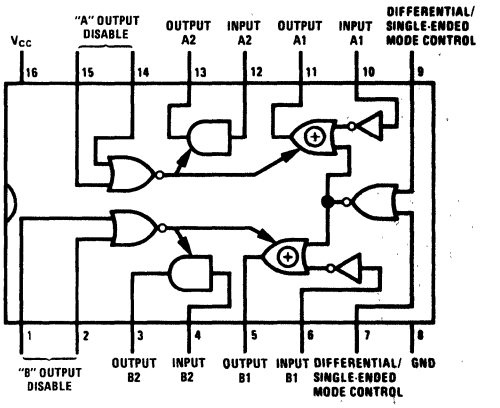
The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

Connection and Logic Diagram

Dual-In-Line Package



TL/F/5800–1

Top View

Order Number DS8831N, DS8832J or DS8832N
See NS Package Number J16A or N16A

For Complete Military 883 Specificatons,
See RETS Data Sheet.
Order Number DS7831J/883, DS7831W/883,
DS7832J/883 or DS7832W/883
See NS Package Number J16A or W16A

Truth Table (Shown for A Channels Only)

"A" Output Disable		Differential/ Single-Ended Mode Control		Input A1	Output A1	Input A2	Output A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X	X 1	X	X	X	High Impedance State	X	High Impedance State

X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7831/DS7832	4.5	5.5	V
DS8831/DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831/DS7832	−55	+125	°C
DS8831/DS8832	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831/DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831/DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831/DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831/DS7832, V_{IN} = 5.5V				1	mA
			DS8831/DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max in TRI-STATE				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC} + 1.5	V

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	(See *Figures 4* and *5*)		13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)			6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)			14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)			18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for $T_A = 125°C$ only. Only one output should be shorted at a time.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the output disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

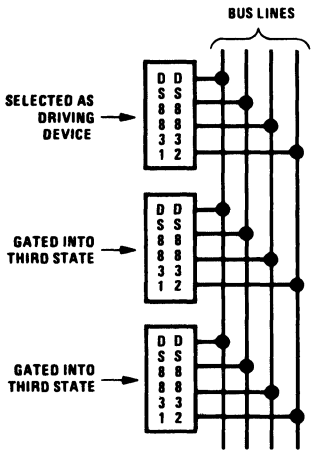
To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs.

The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

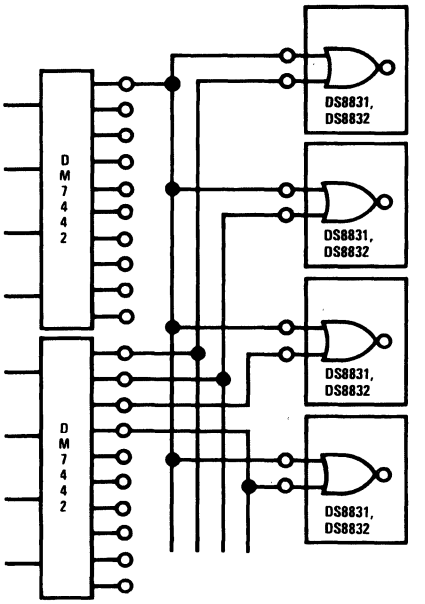
When operating in a bus-organized system with outputs tied directly to outputs of other DS7831/DS8831's, DS7832/DS8832's *(Figure 1)*, all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2)*.

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3)*.



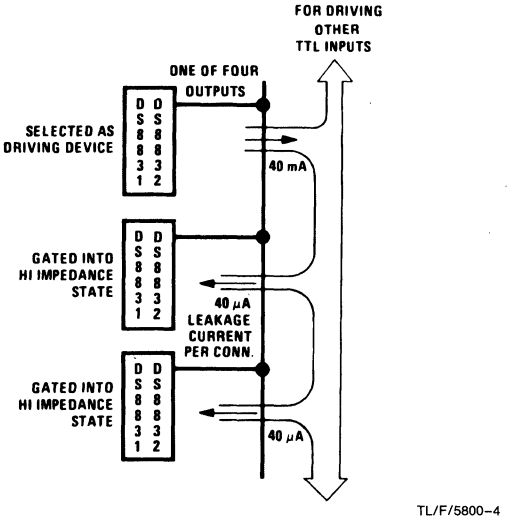
TL/F/5800–2

FIGURE 1



TL/F/5800–3

FIGURE 2

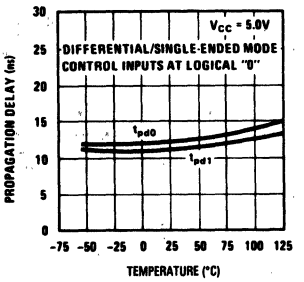


TL/F/5800–4

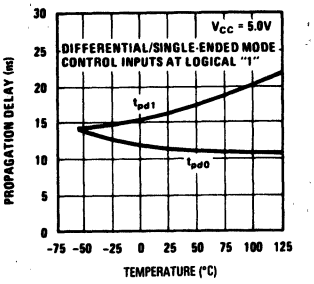
FIGURE 3

Typical Performance Characteristics

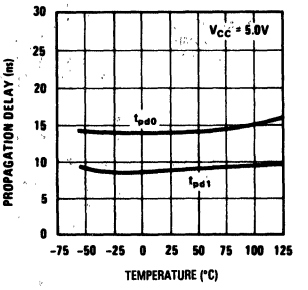
Propagation Delay from Input to Output (Channel 1)



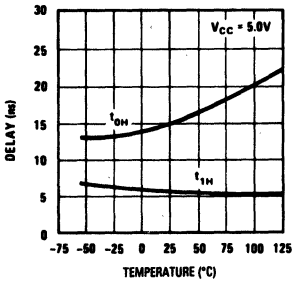
Propagation Delay from Input to Output (Channel 1)



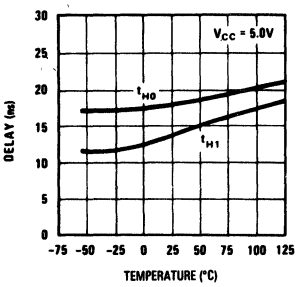
Propagation Delay from Input to Output (Channel 2)



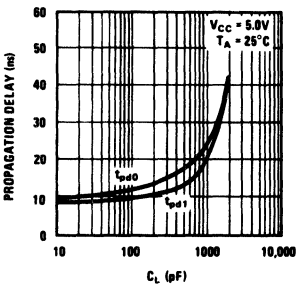
Delay from Disable to High Impedance State



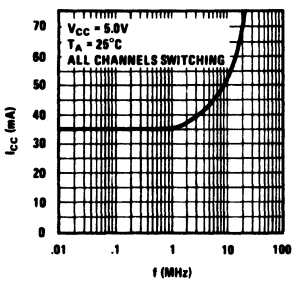
Delay from Disable to Low Impedance State



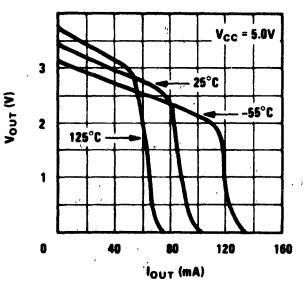
Propagation Delay vs Load Capacitance



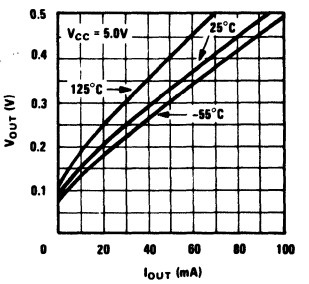
Total Supply Current vs Frequency



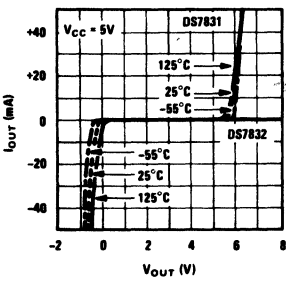
Logical "1" Output Voltage vs Source Current



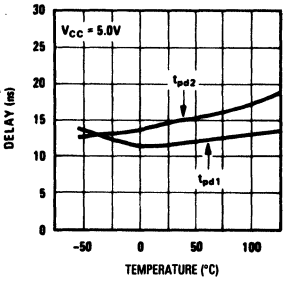
Logical "0" Output Voltage vs Sink Current



I_{OUT} vs V_{OUT} High Impedance Output State



Propagation Delay in Differential Mode



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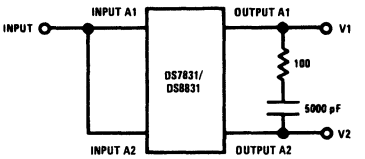
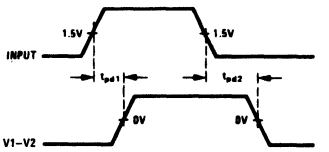
Typical Performance Characteristics (Continued)





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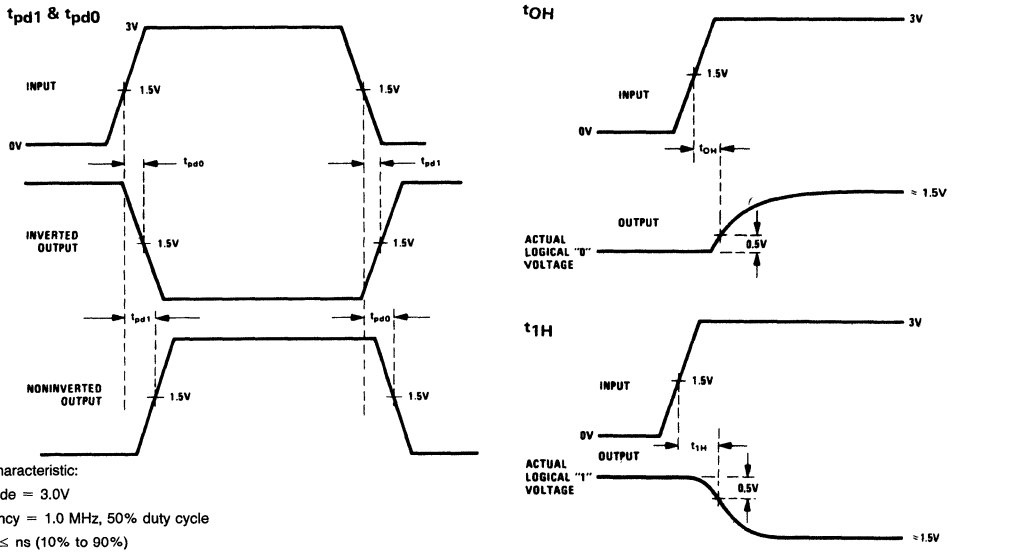
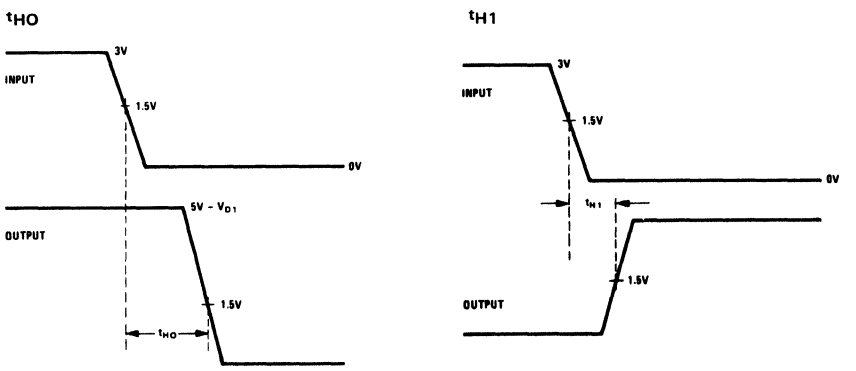
Switching Time Waveforms



Input characteristic:
Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq$ ns (10% to 90%)

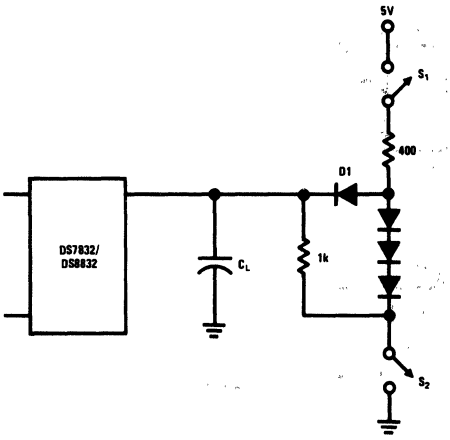
TL/F/5800–7



TL/F/5800–8

FIGURE 4

AC Load Circuit



TL/F/5800–9

FIGURE 5

Symbol	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{0H}	closed	closed	*5 pF
t_{1H}	closed	closed	*5 pF
t_{H0}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance

Section 8

General Purpose Receivers

Section 8 Contents

National Semiconductor

DS1603/DS3603 TRI-STATE® Dual Receivers

General Description

The DS1603/DS3603 are dual differential TRI-STATE line receivers designed for a broad range of system applications. They feature a high input impedance and low input current which reduces the loading effects on a digital transmission line, making them ideal for use in party line systems and general purpose applications like transducer preamplifiers, level translators and comparators.

The receivers feature a ±25 mV input sensitivity specified over a ±3V common mode range. Input protection diodes are incorporated in series with the collectors of the differential stage. These diodes are useful in applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off thus avoiding signal clamping. In addition, TTL compatible strobe and control lines are provide for flexibility in the application.

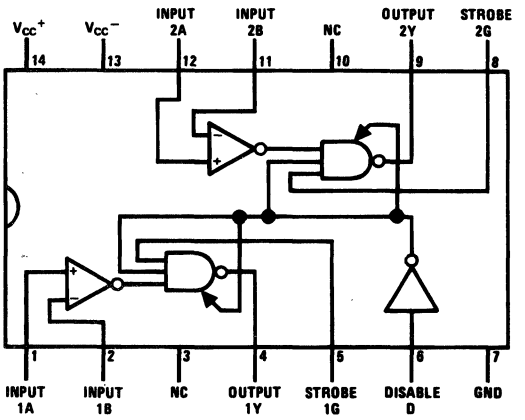
The DS1603/DS3603 are pin compatible with the DS75107, DS75108 and DS75208 series of dual line receivers.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±25 mV input sensitivity
- ±3V input common-mode range
- High-input inpedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses

Connection Diagram

Dual-In-Line Package



TL/F/5781–2

Top View

Order Number DS3603N
See NS Package Number N14A

For Complete Military 883 Specifications, See RETS Data Sheet.
Order Number: DS1603J/883 or DS1603W/883
See NS Package Number J14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}^+)	7V
Supply Voltage (V_{CC}^-)	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS1603			DS3603		
	Min	**Nom**	**Max**	**Min**	**Nom**	**Max**
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

Electrical Characteristics $T_{MIN} \le T_A \le T_{MAX}$ (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into 1A, 1B, 2A or 2B	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current into 1A, 1B, 2A or 2B	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current into 1G, 2G or D	V_{CC}^+ = Max, V_{CC}^- = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC}^+			1	mA
I_{IL}	Low Level Input Current into D	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current into 1G or 2G	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(G)}$ = 0.4V	$V_{IH(D)}$ = 2V			−40	μA
			$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC}^+ = Min, V_{CC}^- = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC}^+ = Min, V_{CC}^- = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC}^+ = Max, V_{CC}^- = Max, $V_{IL(D)}$ = 0.8V (Note 4)		−18		−70	mA
I_{CCH}^+	High Logic Level Supply Current from V_{CC}^+	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C			28	40	mA
I_{CCH}^-	High Logic Level Supply Current from V_{CC}^-	V_{CC}^+ = Max, V_{CC}^- = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC}^+ = Min, V_{CC}^- = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603 and across the 0°C to +70°C range for the DS3603. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All current into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

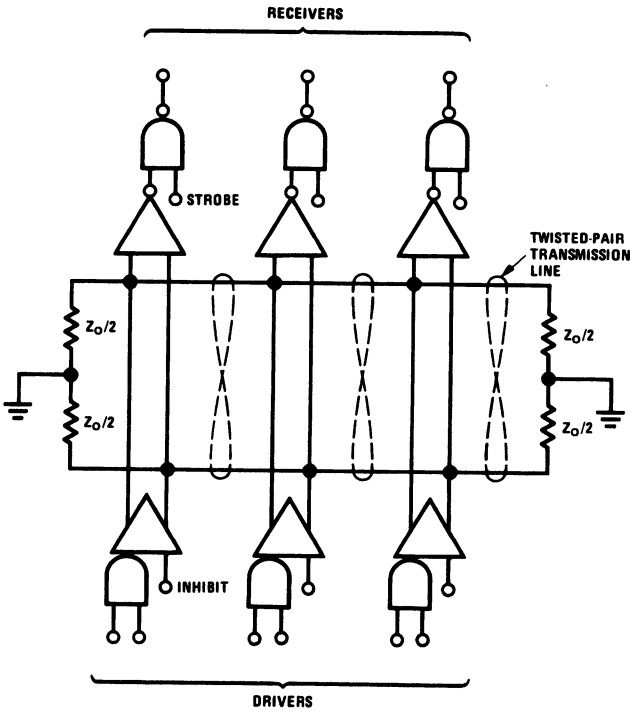
Switching Characteristics $V_{CC}^+ = 5V, V_{CC}^- = -5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, from Strobe Input G to Output	$R_L = 390\Omega, C_L = 50$ pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, from Strobe Input G to Output	$R_L = 390\Omega, C_L = 50$ pF		8	15	ns
t_{1H}	Disable Low-to-High to Output High to Off	$R_L = 390\Omega, C_L = 5$ pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	$R_L = 390\Omega, C_L = 5$ pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	$R_L = 1k$ to 0V, $C_L = 50$ pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	$R_L = 390\Omega, C_L = 50$ pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Typical Application

Line Receiver Used in a Party-Line or Data-Bus System



Line receivers are DS75107/DS75108 or DS3603

Line drivers are SN75109/μA75110/DS75110 or DS8831

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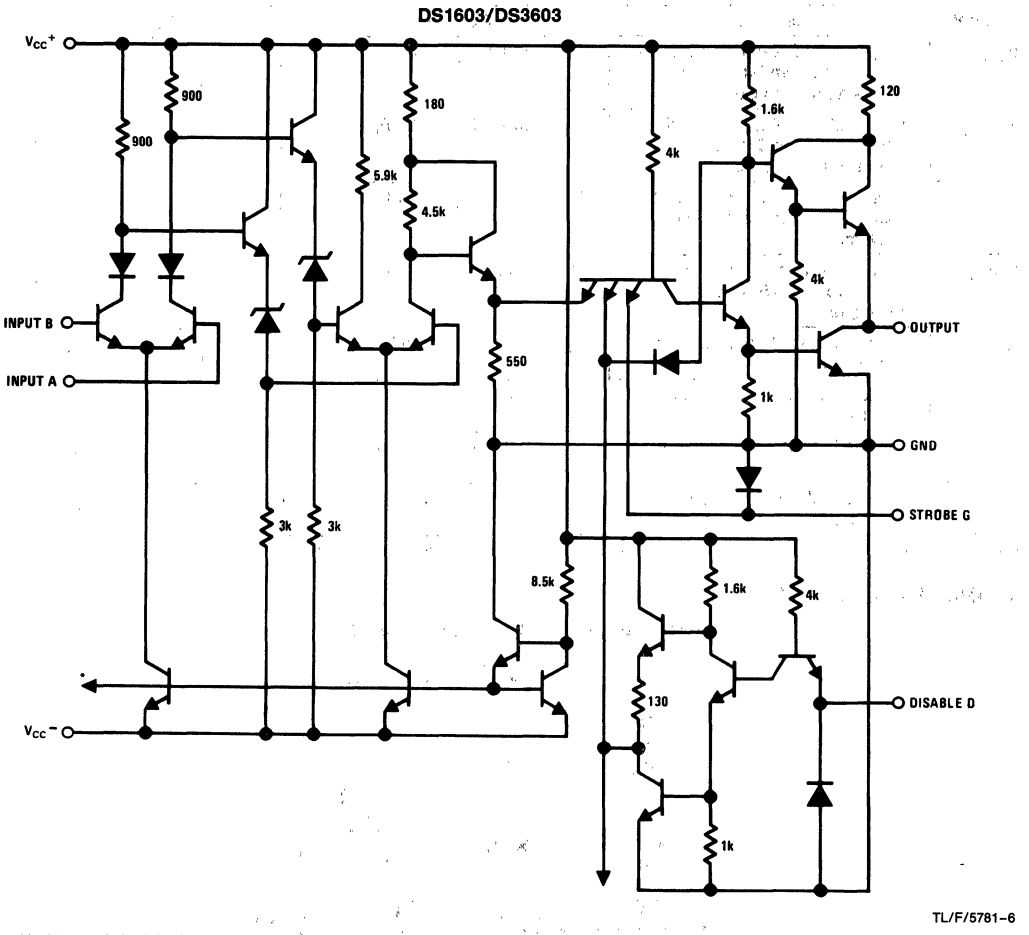
Schematic Diagram (Note 1)



Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

National Semiconductor

DS1652/DS3650/DS3652
Quad Differential Line Receivers

General Description

The DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

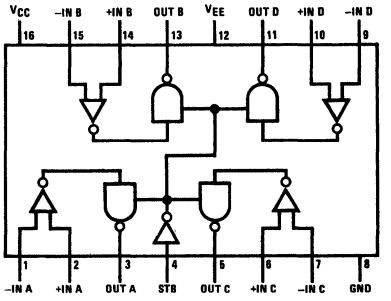
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration, the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



TL/F/5782-1

Top View

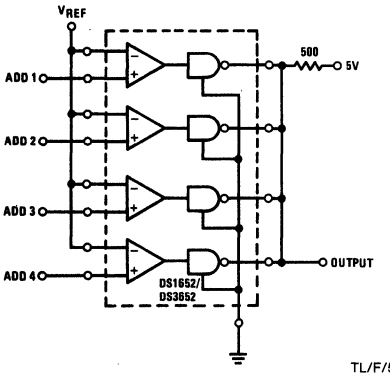
Order Number DS3650M, DS3652M or DS3650N
See NS Package Number M16A or N16A

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS1652J
See NS Package Number J16A

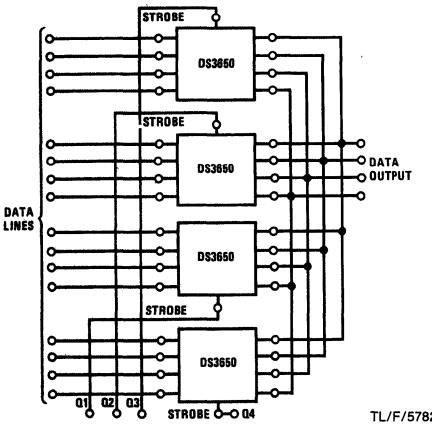
Typical Applications

Implied "AND" Gating



TL/F/5782-2

Wired "OR" Data Selecting Using TRI-STATE Logic



TL/F/5782-3

Truth Table

Input	Strobe	Output	
		DS3650	DS1652/ DS3652
$V_D \geq 25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	−7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded DIP Package	1476 mW
SO Package	1051 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded DIP package 11.8 mW/°C above 25°C; derate SO package 8.41 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range Input to GND, V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V, DS1652			100	µA
			$V_{IH(S)}$ = 2.4V, DS3650, DS3652			40	µA
			$V_{IH(S)}$ = V_{CC}			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS3650	2.4			V
I_{CEX}	High Level Output Leakage Current	*(Figure 1)*	DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V
			DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS3650			40	µA

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

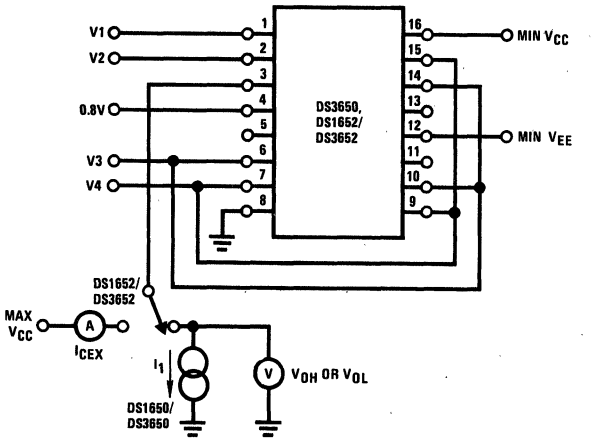
Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics (V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits



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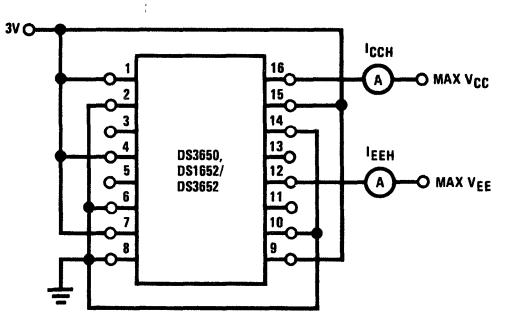
	V1		V2		V3		V4		I_1
	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	DS3650	DS1652/ DS3652	
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		−0.4 mA −0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	+16 mA +16 mA

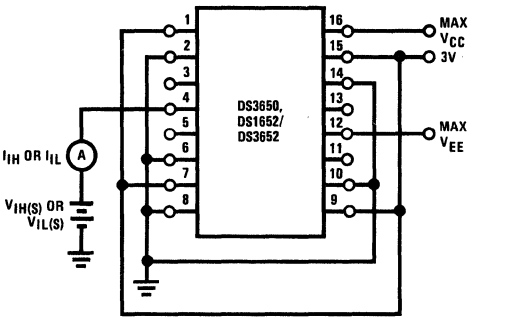
Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}



TL/F/5782–5

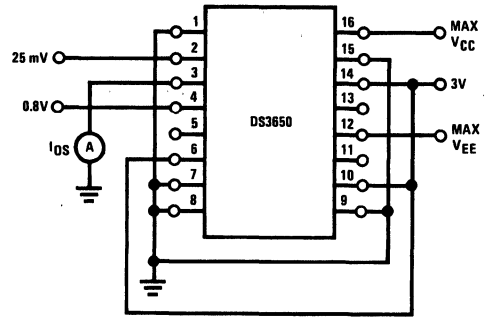
FIGURE 2. I_{CCH} and I_{EEH}



TL/F/5782–6

FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$

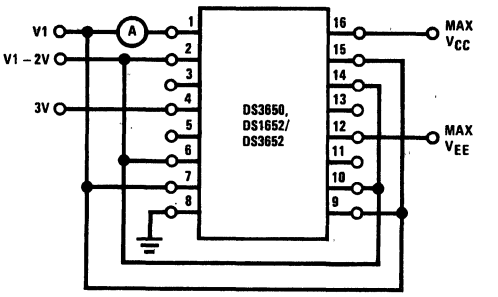
Electrical Characteristic Test Circuits (Continued)



TL/F/5782–7

Note: Channel A shown under test, other channels are tested similiarly. Only one output shorted at a time.

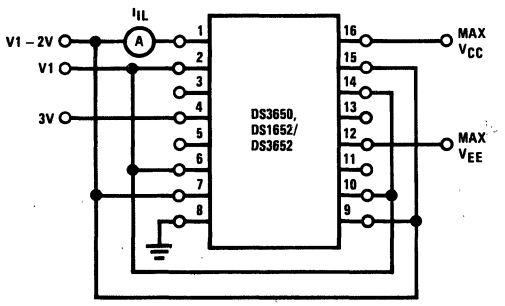
FIGURE 4. I_{OS}



TL/F/5782–8

Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

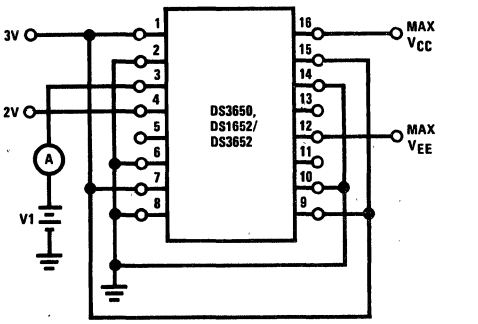
FIGURE 5. I_{IH}



TL/F/5782–9

Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to −3V.

FIGURE 6. I_{IL}



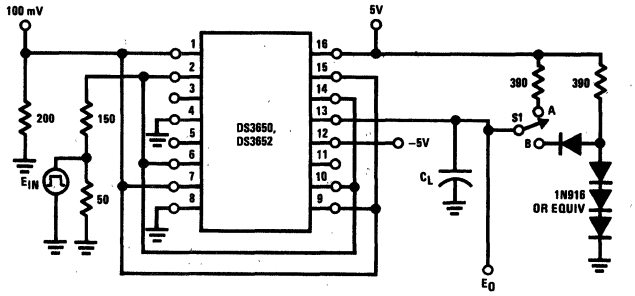
TL/F/5782–10

Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

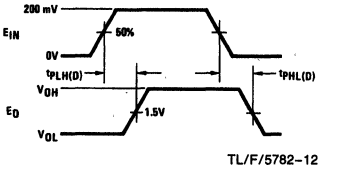
FIGURE 7. I_{OFF}

8

AC Test Circuits and Switching Time Waveforms



TL/F/5782–11



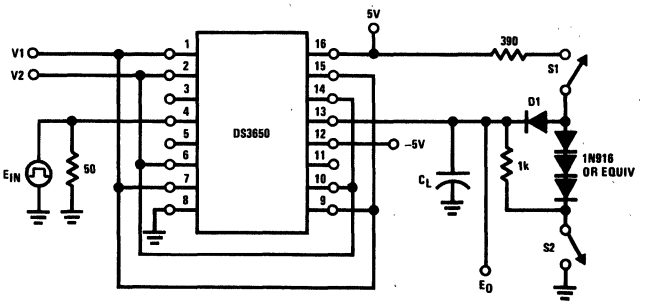
TL/F/5782–12

Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured
10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

Note: Output of Channel B shown under test, other channels are tested similarly.

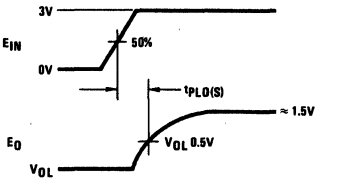
S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

FIGURE 8. Receiver Propagation Dealy $t_{PLH(D)}$ and $t_{PHL(D)}$

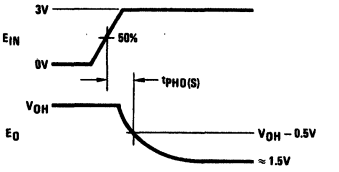


TL/F/5782–13

Note: Output of Channel B shown under test, other channels are tested similiarly.



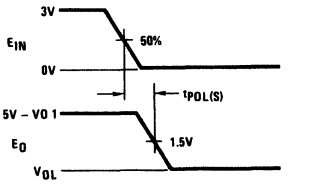
TL/F/5782–14



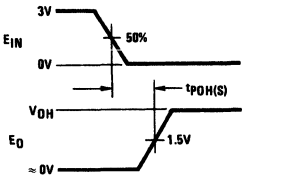
TL/F/5782–15

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%



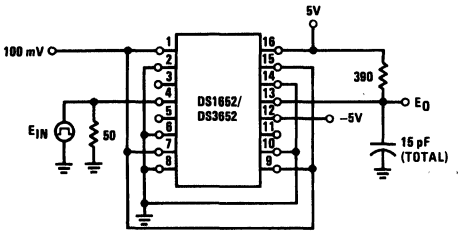
TL/F/5782–16



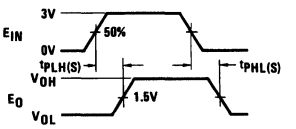
TL/F/5782–17

FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5782–18



TL/F/5782–19

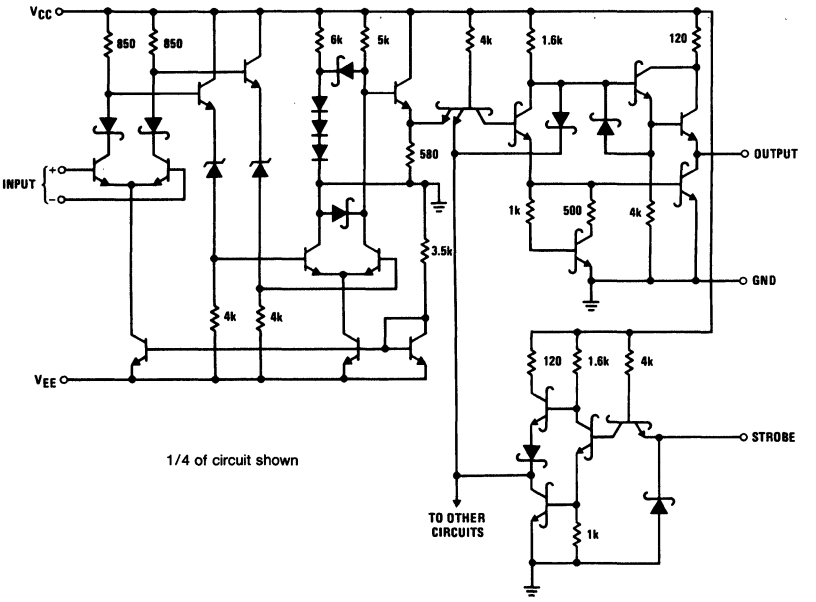
Note: Output of Channel B shown under test, other channels are tested similarly.

Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% and 90%
PRR = 1 MHz
Duty Cycle = 500 ns

FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams

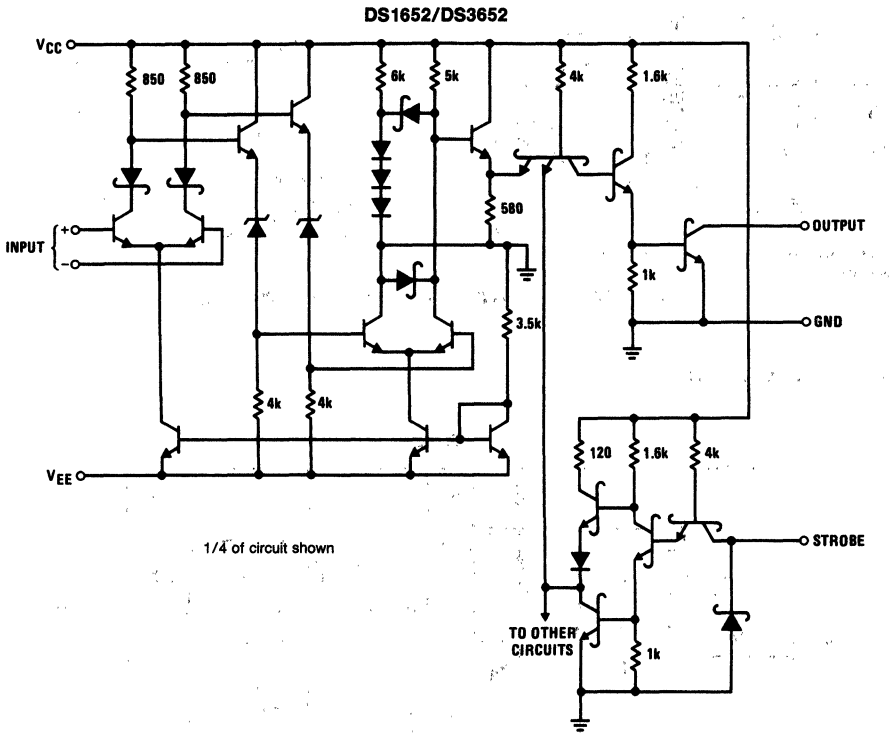
DS3650



1/4 of circuit shown

TL/F/5782–20

Schematic Diagrams (Continued)



1/4 of circuit shown

TL/F/5782–21

National Semiconductor

DS55107/DS75107/DS75108/DS75208 Dual Line Receivers

General Description

The products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers of MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the SN55109/SN75109 and μA75110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75208 make it ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators.

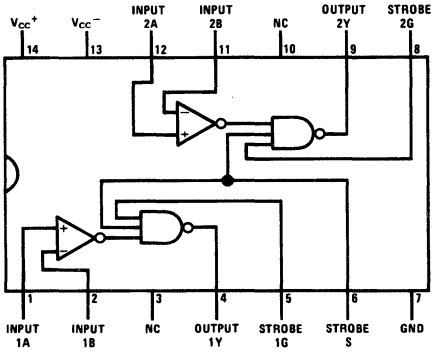
Input protection diodes are incorporated in series with the collectors of the differential input stage. These diodes are useful in certain applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagram

Dual-In-Line Package



TL/F/9446–1

Top View

Order Number DS75107M, DS75107N, DS75107AM, DS75107AN, DS75108M, DS75108N or DS75208N
See NS Package Number M14A or N14A

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS55107AJ/883
See NS Package Number J14A

Selection Guide

Temperature → / Package →	$-55°C \le T_A \le +125°C$ Cavity Dip	$0°C \le T_A \le +70°C$ Cavity or Molded Dip	
Input Sensitivity → / Output Logic ↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-Up	DS55107	DS75107	
TTL Open Collector		DS75108	DS75208

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_{CC}+$	7V
Supply Voltage, $V_{CC}-$	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS55107			DS75107, DS75108, DS75208		
	Min	Nom	Max	Min	Nom	Max
Supply Voltage $V_{CC}+$	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage $V_{CC}-$	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55107 and across the 0°C to +70°C range for the DS75107, DS75108 and DS75208. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

DS55107/DS75107, DS75108 Electrical Characteristics $T_{MIN} \le T_A \le T_{MAX}$ (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into A1, B1, A2 or B2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current into A1, B1, A2 or B2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current into G1 or G2	$V_{CC}+$ = Max, $V_{CC}-$ = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ Max $V_{CC}+$			1	mA
I_{IL}	Low Level Input Current into G1 or G2	$V_{CC}+$ = Max, $V_{CC}-$ = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current into S	$V_{CC}+$ = Max, $V_{CC}-$ = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max $V_{CC}+$			2	mA
I_{IL}	Low Level Input Current into S	$V_{CC}+$ = Max, $V_{CC}-$ = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{LOAD} = −400 μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	$V_{CC}+$ = Min, $V_{CC}-$ = Min V_{OH} = Max $V_{CC}+$, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	$V_{CC}+$ = Max, $V_{CC}-$ = Max, (Notes 2 and 3)		−18		−70	mA
$I_{CCH}+$	High Logic Level Supply Current from V_{CC}	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
$I_{CCH}-$	High Logic Level Supply Current from V_{CC}	$V_{CC}+$ = Max, $V_{CC}-$ = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	$V_{CC}+$ = Min, $V_{CC}-$ = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics $V_{CC+} = 5V, V_{CC-} = -5V, T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, from Differential Inputs A and B to Output	$R_L = 390\Omega, C_L = 50$ pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, from Strobe Input G or S to Output	$R_L = 390\Omega, C_L = 50$ pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, from Strobe Input G or S to Output	$R_L = 390\Omega, C_L = 50$ pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Note 2: Only one output at a time should be shorted.

Note 3: DS55107/DS75107 only.

Note 4: DS75108 only.

DS75208

Electrical Characteristics $0°C \le T_A \le +70°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{IH}	High Level Input Current into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min, V_{OH} = Max V_{CC+}				250	μA
I_{CCH+}	High Logic Level Supply Current from V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current from V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

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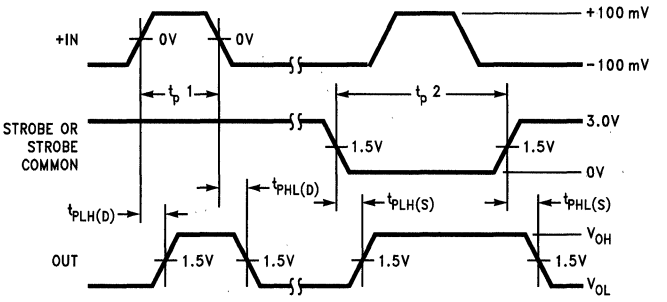
Switching Characteristics $V_{CC+} = 5V, V_{CC-} = -5V, T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, from Differential Inputs A and B to Output	$R_L = 470\Omega$, $C_L = 15$ pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, from Differential Inputs A and B to Output	$R_L = 470\Omega$, $C_L = 15$ pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, from Strobe Input G or S to Output	$R_L = 470\Omega$, $C_L = 15$ pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, from Strobe Input G or S to Output	$R_L = 470\Omega$, $C_L = 15$ pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.

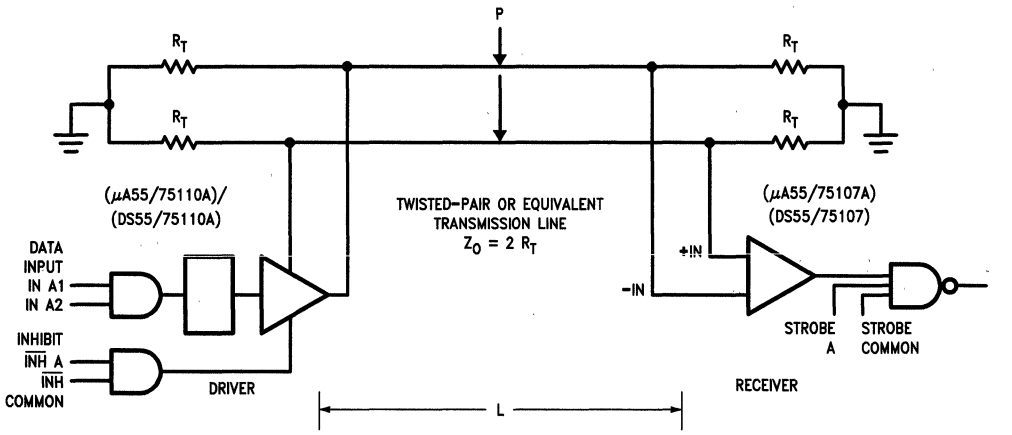
Voltage Waveforms



TL/F/9446–12

Typical Applications

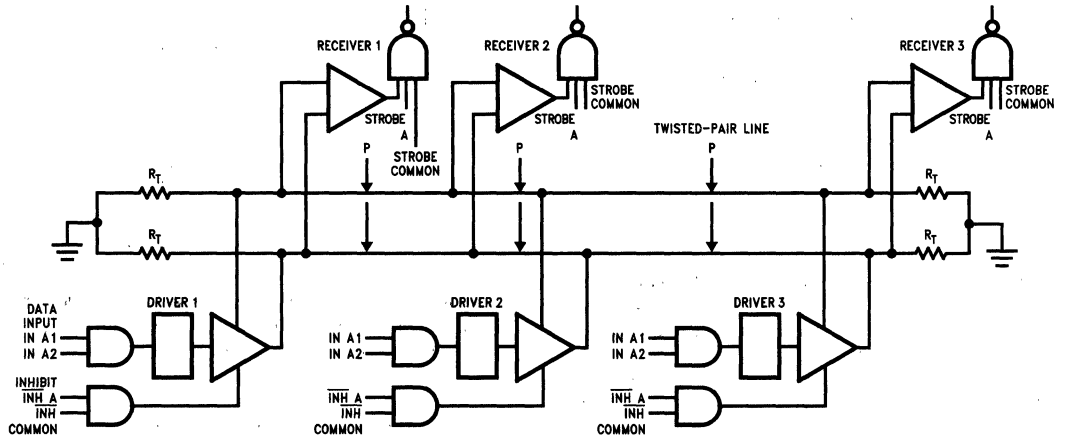
Basic Balanced-Line Transmission System



TL/F/9446–2

Typical Applications (Continued)

Data-Bus or Party-Line System



TL/F/9446–3

APPLICATION

The DS55107, DS75107 dual line circuits are designed specifically for use in high speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver output circuit allows terminated transmission lines to be driven at normal line impedances. High speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) ns, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver input logic levels. The voltage difference is approximately:

$$V_{DIFF} \cong \tfrac{1}{2} I_{O(on)} \times R_T \quad (1)$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \cong I_{O(on)} \times R_T \quad (2)$$

The strobe feature of the receivers and the inhibit feature of the drivers allow the DS55107, DS75107 dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time multiplexed on the transmission line. The DS55107, DS75107 device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

The DS55107, DS75107 dual line circuits may also be used in unbalanced or single line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environment noise is not severe.

The receiver threshold level is established by applying a DC reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal

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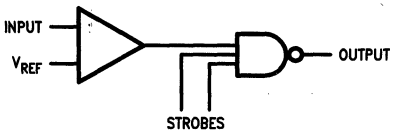
Typical Applications (Continued)

swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3.0V to +3.0V. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

Unbalanced or Single-Line Systems



TL/F/9446–4

Precautions in the Use of DS1603, DS3603, DS55107, DS75107, DS75108 and DS75208 Dual Line Receivers

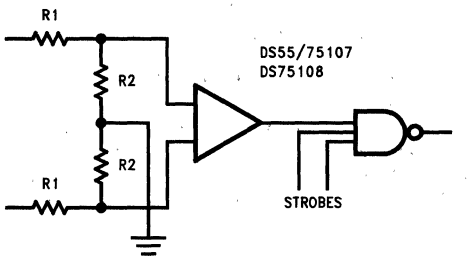
The following precaution should be observed when using or testing DS55107, DS75107 line circuits.

When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3.0V and +3.0V, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers.

The DS55107, DS75107 and DS75108 line receivers feature a common mode input voltage range of ±3.0V. This satisfies the requirements for all but the noisiest system applications. For these severe noise environments, the common mode range can be extended by the use of external input attenuators. Common mode input voltages can in this way be reduced to ±3.0V at the receiver input terminals. Differential data signals will be reduced proportionately. Input sensitivity, input impedance and delay times will be adversely affected.

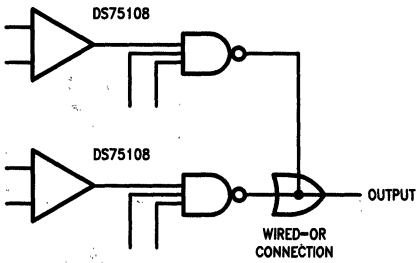
The DS75108 line receivers feature an open-collector-output circuit that can be connected in the DOT-OR logic configuration with other DS75108 outputs. This allows a level of logic to be implemented without addtional logic delay.

Increasing Common Mode Input Voltage Range of Receiver



TL/F/9446–5

DS75108 Wired-OR Output Connections

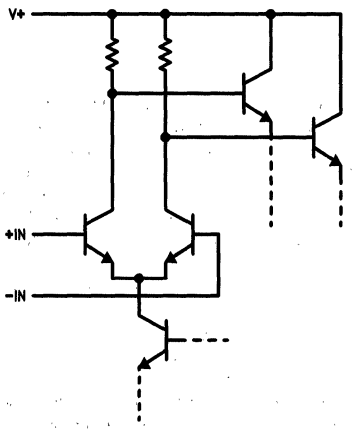


TL/F/9446–6

Circuit Differences Between "A" and Standard Devices

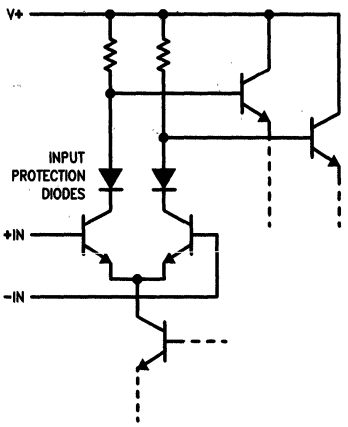
The difference between the "A" and standard devices is shown in the following schematics of the input stage.

"A" Devices



TL/F/9446–7

Standard Devices

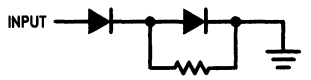


TL/F/9446–8

Typical Applications (Continued)

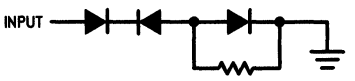
The input protection diodes are useful in certain party-line systems which may have multiple V+ power supplies and, in which case, may be operated with some of the V+ supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

"A" Devices



TL/F/9446–9

Standard Devices



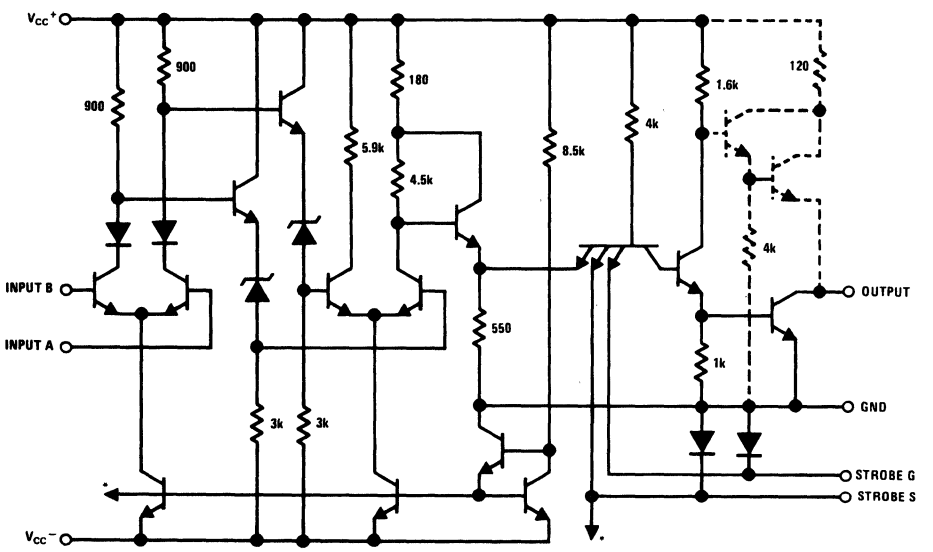
TL/F/9446–10

This would be a problem in specific systems which might possibly have the transmission lines biased to some potential greater than 1.4V. Since this is not a widespread application problem, both the "A" and standard devices will be available. The ratings and characteristic specifications of the "A" devices are the same as those of the standard devices.

The DS55107A feature the "A" device input stage.

Schematic Diagrams

DS55107/DS75107, DS75108, DS75208



TL/F/9446–11

Note 1: ½ of the dual circuit is shown.

Note 2: *Indicates connections common to second half of dual circuit.

Note 3: Components shown with dash lines are applicable to the DS55107, DS75207 and DS75107 only.

National Semiconductor

DS75115/DS9615 Dual Differential Line Receiver

General Description

The DS75115/DS9615 is a dual differential line receiver designed to sense differential signals from data transmission lines. Designed for operation over military and commercial temperature ranges, the DS75115/DS9615 can typically receive ±500 mV differential data with ±15V common-mode noise. Outputs are open-collector and give TTL compatible signals which are a function of the polarity of the differential input signal. Active output pull-ups are also available, offering the option of an active TTL pull-up through an external connection.

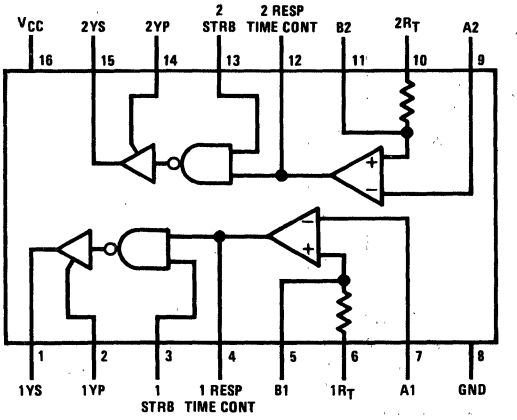
Response time may be controlled with the use of an external capacitor. Each channel may be independently controlled and optional input termination resistors are also available.

Features

- Single 5V supply
- High common-mode voltage range
- Each channel individually strobed
- Independent response time control
- Uncommitted collector or active pull-up option
- TTL compatible output
- Optional 130Ω termination resistors
- Direct replacement for 9615

Connection Diagram

Dual-In-Line Package



TL/F/5787–1

Top View

Order Number DS75115N
See NS Package Number N16A

For Complete Military 883 Specifications, See RETS Datasheet.
Order Number DS9615MJ/883, DS9615ME/883

Function Table

Strobe	Diff. Input	Output
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} (Note 1) 7V

Input Voltage at A, B and R_T Inputs ±25V

Input Voltage at Strobe Input 5.5V

Off-State Voltage Applied to Open-Collector Outputs 14V

Maximum Power Dissipation* at 25°C

Cavity Package 1433 mW

Molded Package 1362 mW

Operating Free-Air Temperature Range

DS9615M −55°C to +125°C

DS57115 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature ($1/16$ inch from case for 4 seconds) 260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS9615M	4.5	5.5	V
DS75115	4.75	5.25	V
High Level Output Current (I_{OH})		−5	mA
Low Level Output Current (I_{OL})		15	mA
Operating Temperature (T_A)			
DS9615M	−55	125	°C
DS75115	0	70	°C

Electrical Characteristics (Notes 2, 3 and 5)

Symbol	Parameter	Conditions		DS75115 Min	DS75115 Typ	DS75115 Max	Units
V_{TH}	Differential Input High-Threshold Voltage	V_O = 0.4V, I_{OL} = 15 mA, V_{IC} = 0V			200	500	mV
V_{TL}	Differential Input Low-Threshold Voltage	V_O = 2.4V, I_{OH} = −5 mA, V_{IC} = 0V			−200	−500	mV
V_{ICR}	Common-Mode Input Voltage Range	V_{ID} = ±1V		15 to −15	24 to −19		V
$V_{IH(STROBE)}$	High-Level Strobe Input Voltage			2.4			V
$V_{IL(STROBE)}$	Low-Level Strobe Input Voltage					0.4	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{ID} = −0.5V, I_{OH} = −5 mA	T_A = Min	2.4			V
			T_A = 25°C	2.4	3.4		
			T_A = Max	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{ID} = 0.5V, I_{OL} = 15 mA			0.22	0.45	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, Other Input at 5.5V	T_A = Min			−0.9	mA
			T_A = 25°C		−0.5	−0.7	
			T_A = Max			−0.7	
I_{SH}	High Level Strobe Current	V_{CC} = Min, V_{ID} = −0.5V, V_{STROBE} = 4.5V	T_A = 25°C		0.5	5	µA
			T_A = Max			10	
I_{SL}	Low Level Strobe Current	V_{CC} = Max, V_{ID} = 0.5V, V_{STROBE} = 0.4V	T_A = 25°C		−1.15	−2.4	mA
I_4, I_{12}	Response Time Control Current (Pin 4 or Pin 12)	V_{CC} = Max. V_{ID} = 0.5V, V_{RC} = 0V	T_A = 25°C	−1.2	−3.4		mA
$I_{O(OFF)}$	Off-State Open-Collector Output Current	V_{CC} = Min, V_{OH} = 12V, V_{ID} = −4.5V	T_A = 25°C				µA
			T_A = Max				
		V_{CC} = Min, V_{OH} = 5.25V, V_{ID} = −4.75V	T_A = 25°C			100	
			T_A = Max			200	

8

Electrical Characteristics (Notes 2, 3 and 5) (Continued)

Symbol	Parameter	Conditions		DS75115			Units
				Min	Typ	Max	
R_T	Line Terminating Resistance	V_{CC} = 5V	T_A = 25°C	74	130	179	Ω
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_O = 0V, V_{ID} = −0.5V, (Note 4)	T_A = 25°C	−14	−40	−100	mA
I_{CC}	Supply Current (Both Receivers)	V_{CC} = Max, V_{ID} = 0.5V, V_{IC} = 0V	T_A = 25°C		32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for the actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS9615M and across the 0°C to +70°C range for the DS75115. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

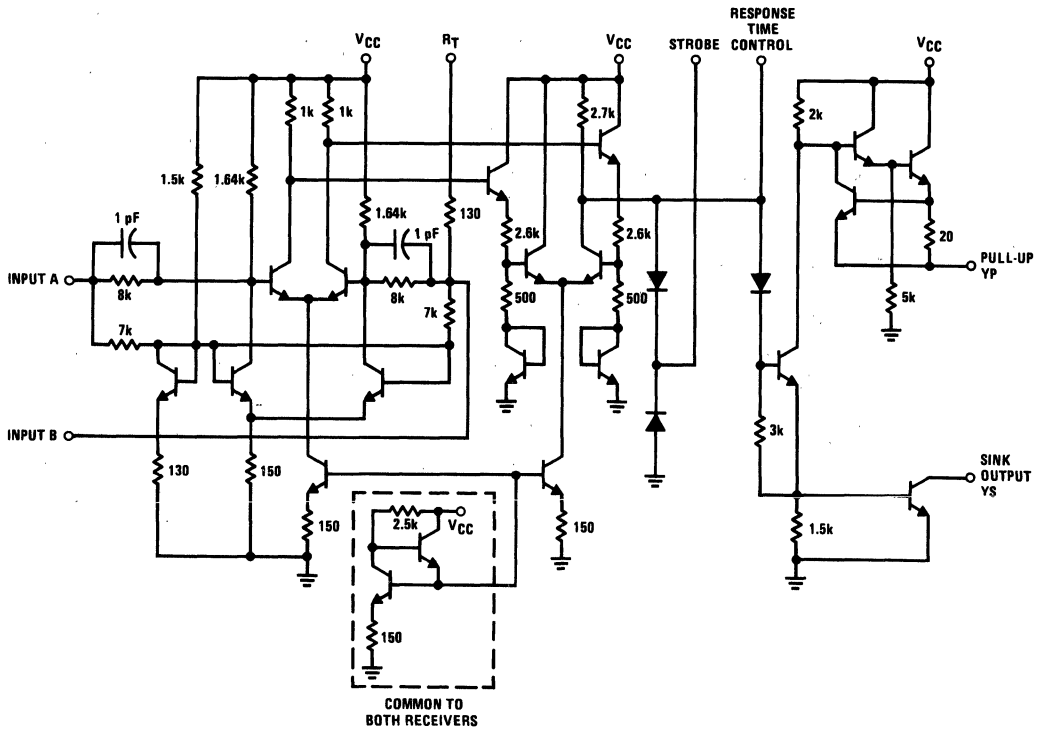
Note 4: Only one output at a time should be shorted.

Note 5: Unless otherwise noted, V_{STROBE} = 2.4V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

Symbol	Parameter	Conditions	DS75115			Units
			Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 3.9 kΩ, *(Figure 1)*		18	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 390Ω, *(Figure 1)*		20	75	ns

Schematic Diagram



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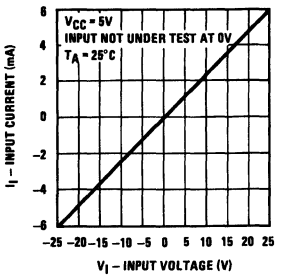
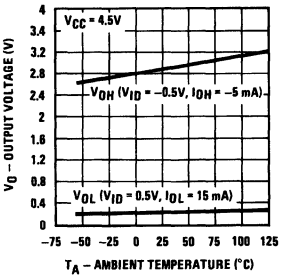
Typical Performance Characteristics (Note 3)

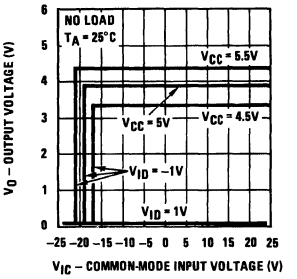
Input Current vs Input Voltage



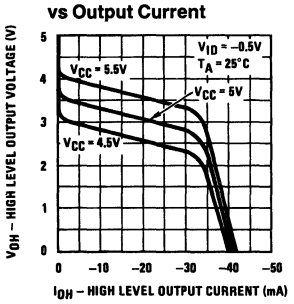
Output Voltage vs Temperature



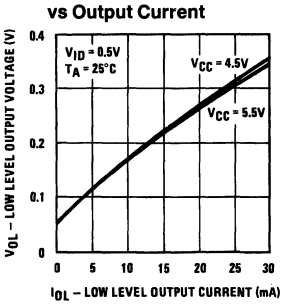
Output Voltage vs Common-Mode Input Voltage



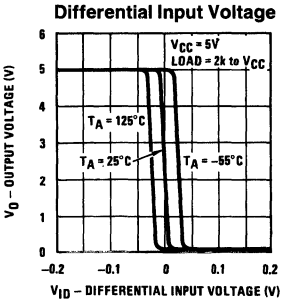
High Level Output Voltage vs Output Current



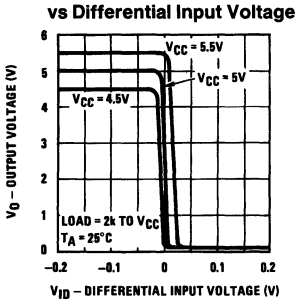
Low Level Output Voltage vs Output Current



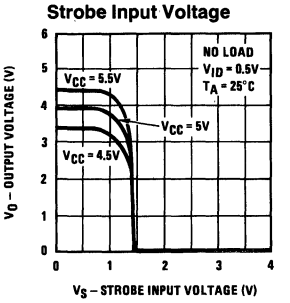
Output Voltage vs Differential Input Voltage



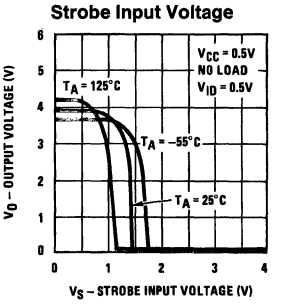
Output Voltage vs Differential Input Voltage



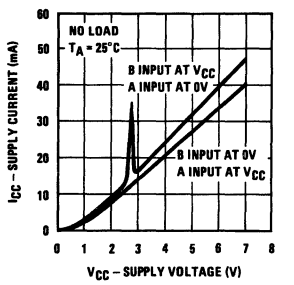
Output Voltage vs Strobe Input Voltage



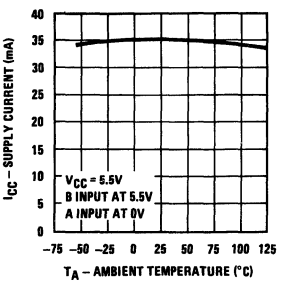
Output Voltage vs Strobe Input Voltage



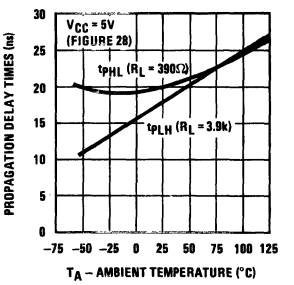
Supply Current (Both Receivers) vs Supply Voltage



Supply Current (Both Receivers) vs Temperature



Propagation Delay Times vs Temperature



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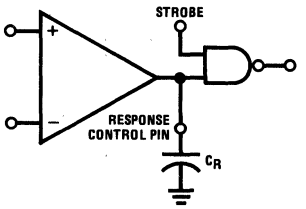
Frequency Response Control



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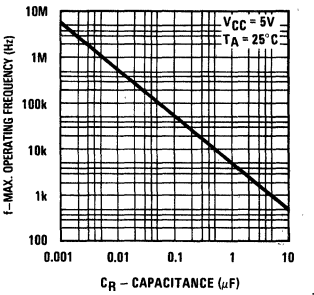
Note: C_R (response control) > 0.01 μF may cause slowing of rise and fall times of the output.

Frequency Response as a Function of Capacitance



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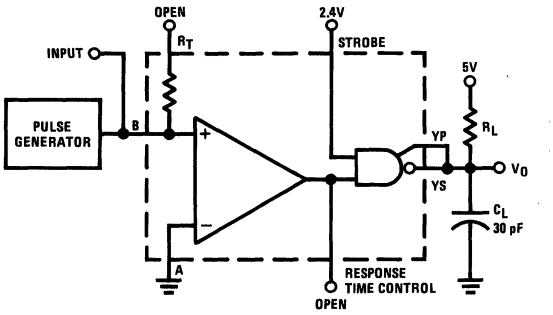
AC Test Circuit and Switching Time Waveforms



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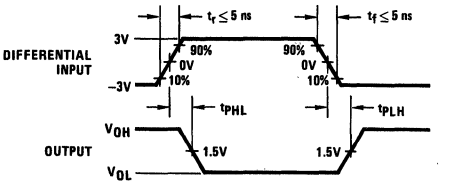

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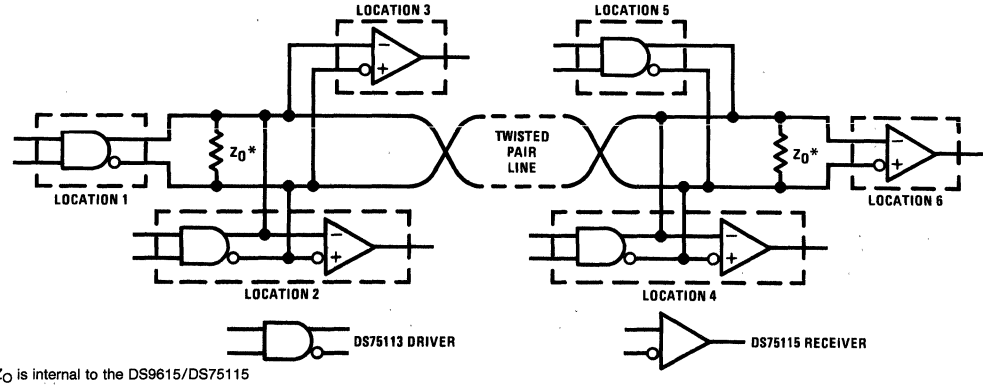
FIGURE 1. Propagation Delay Time (Notes 1, 2)

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 500 kHz/t_W = 100 ns

Note 2: C_L includes probe and test fixture capacitance

Typical Application

Basic Party-Line or Data-Bus Differential Data Transmission



*Z_O is internal to the DS9615/DS75115

A capacitor may be connected in series with Z_O to reduce power dissipation.

TL/F/5787–3

National Semiconductor

DS55122
Triple Line Receiver

General Description

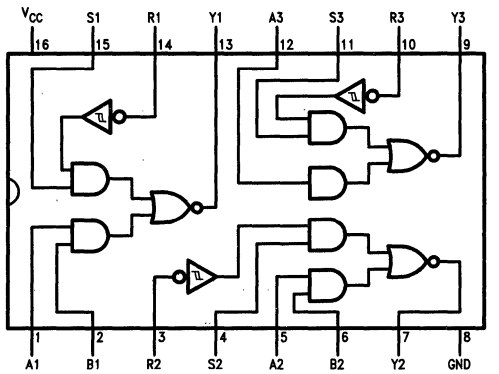
The DS55122 is a triple line receiver designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS55122 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed—typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series standard loads
- Plug-in replacement for the SN55122

Connection Diagram

Dual-In-Line Package



TL/F/10816–1

Top View

For Complete Military 883 Specifications, see RETS Data Sheet.

Order Number DS55122J/883 or DS55122W/883
See NS Package Number J16A or W16A

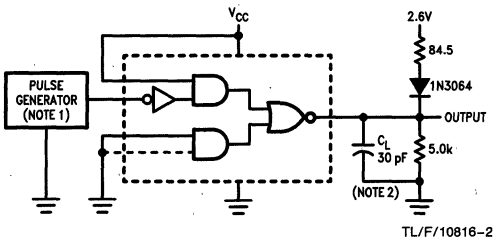
Truth Table

Inputs				Output
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

† B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

AC Test Circuit and Switching Time Waveforms



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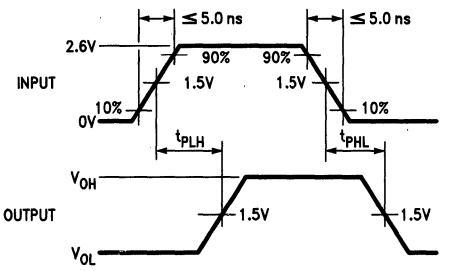

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Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, $t_r = t_f$ = 5.0 ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	6.0V
Input Voltage	
R Input	6.0V
A, B, or S Input	5.5V
Output Voltage	6.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C (J)	1433 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Operating Temperature (T_A)			
DS55122	−55	+125	°C
High Level Output Current (I_{OH})		−500	μA
Low Level Output Current (I_{OL})		16	mA

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	A, B, R, or S		2.0			V
V_{IL}	Low Level Input Voltage	A, B, R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.3	0.6		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Clamp at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1.0	mA
V_{OH}	High Level Output Voltage	I_{OH} = −500 μA	V_{IH} = 2V, V_{IL} = 0.8V, (Note 4)	2.6			V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 7)	2.6			V
V_{OL}	Low Level Output Voltage	I_{OL} = 16 mA	V_{IH} = 2.0V, V_{IL} = 0.8V, (Note 4)			0.4	V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 8)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.8V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125°C for DS55122 and 0°C to +75°C for DS75122, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

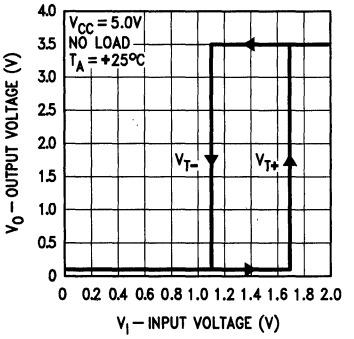
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 7: Receiver input was at a high level immediately before being reduced to 1.45V.

Note 8: Receiver input was at a low level immediately before being raised to 1.45V.

Typical Performance Characteristics

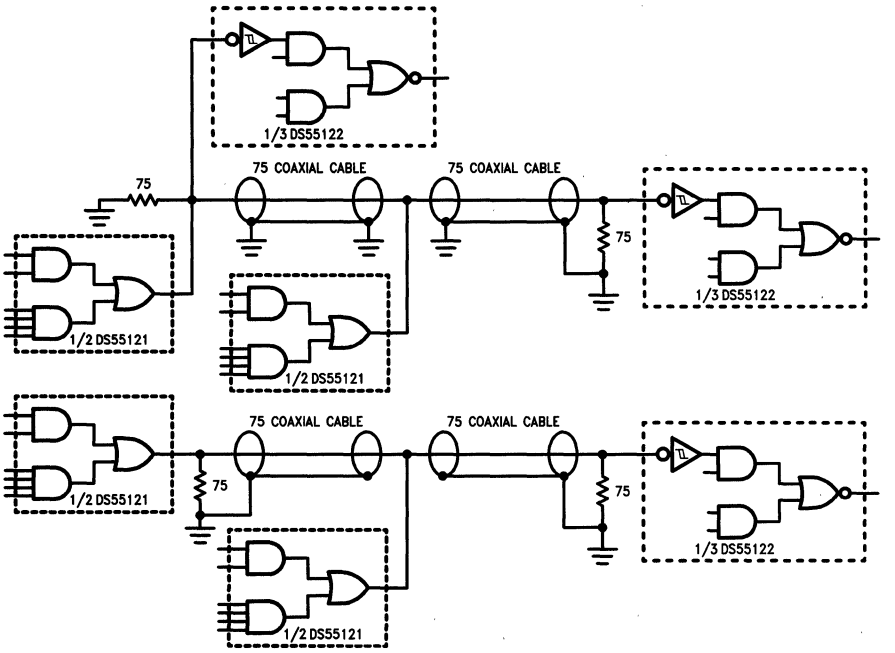
Output Voltage vs Receiver Input Voltage



TL/F/10816–4

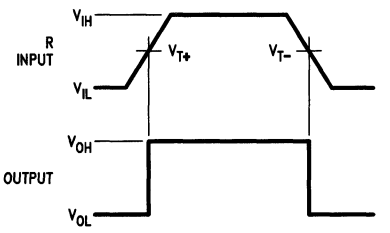
Typical Applications

Single-Ended Party Line Circuits



TL/F/10816–5

Pulse Squaring



The high gain and built-in hystersis of the DS55122 line receiver enables it to be used as a Schmitt trigger in squaring up pulses.

TL/F/10816–6

National Semiconductor

DS75124 Triple Line Receiver

General Description

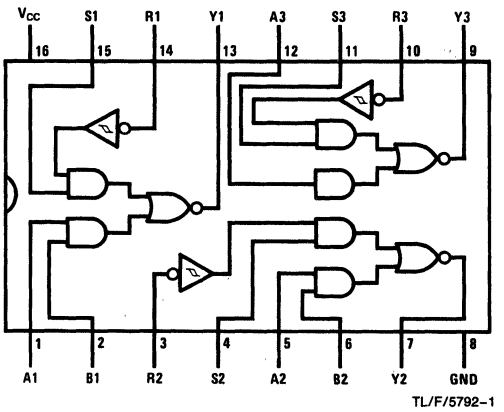
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5792–1

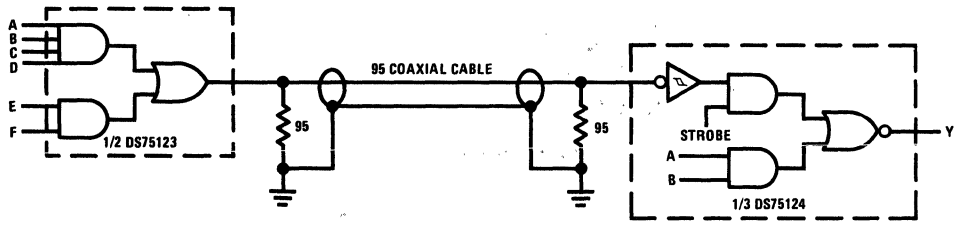
Top View

Order Number DS75124N
See NS Package Number N16A

Inputs				Output
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only

Typical Application



TL/F/5792–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C	
Molded Package	1362 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	A, B, or S	2.0			V
		R	1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S			0.8	V
		R			0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)	0.2	0.4		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S			−1.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S			1	mA
		R, V_I = 7.0V			5.0	mA
		R, V_I = 6.0V, V_{CC} = 0V			5.0	mA
V_{OH}	High Level Output Voltage	V_{IH} = V_{IHMIN}, V_{IL} = V_{ILMAX}, I_{OH} = −800 μA, (Note 4)	2.6			V
V_{OL}	Low Level Output Voltage	V_{IH} = V_{IHMIN}, V_{IL} = V_{ILMAX}, I_{OL} = 16 mA, (Note 4)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S			40	μA
		V_I = 3.11V, R			170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)	−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V			72	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See AC Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

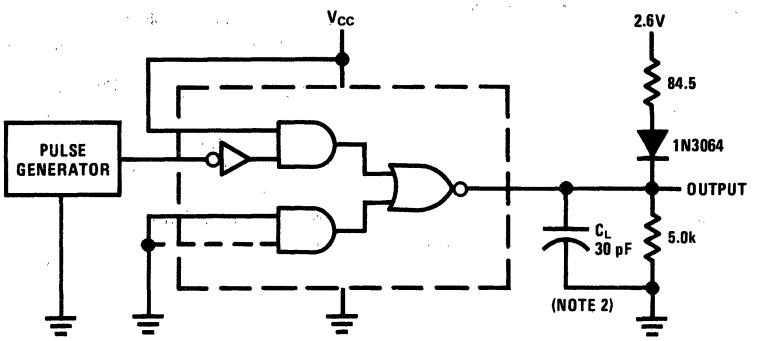
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

AC Test Circuit and Switching Time Waveforms



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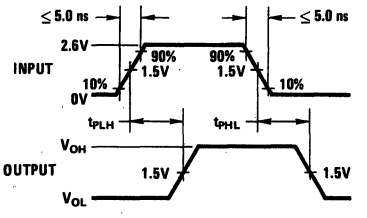
Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%

Note 2: C_L includes probe and jig capacitance.



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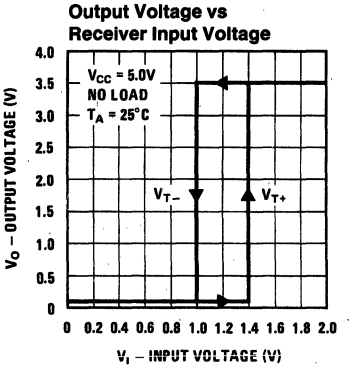
Typical Performance Characteristics



TL/F/5792–5

National Semiconductor

DS75129 Eight-Channel Line Receivers

General Description

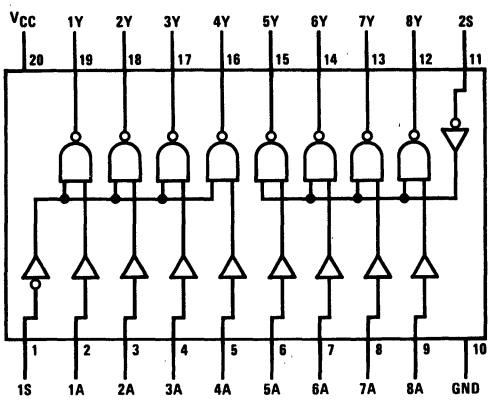
The DS75129 is an eight-channel line receiver designed to satisfy the requirements of the input-output interface specification for IBM 360/370. The device features common strobes for each group of four receivers. The DS75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The DS75129 is characterized for operation from 0°C to 70°C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from a single 5V supply
- High speed—low propagation delay
- Ratio specification—t_{PLH}/t_{PLH}
- Common strobe for each group of four receivers
- DS75129 strobe—active-low

Connection Diagram

DS75129
Dual-In-Line Package



positive logic: Y = $\overline{AS}$.

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Top View

Order Number DS75129N
See NS Package Number N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage Range	−0.15V to 7V
Strobe Input Voltage	7V
Maximum Power Dissipation* at 25°C (Note 2)	
Molded Package	1687 mW
Operating Free-Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

*Derate molded package 13.5 mW/°C above 25°C.

Lead Temperature	260°C
1/16 Inch from Case for 4 Seconds: N Package	

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Symbol	Parameter		Conditions	Min	Typ (Note 5)	Max	Units
V_{IH}	High-Level Input Voltage	A		1.7			V
		S		2			
V_{IL}	Low-Level Input Voltage	A				0.7	V
		S				0.7	
V_{OH}	High-Level Output Voltage		V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = 0.4 mA	2.4	3.1		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
V_I	Input Clamp Voltage	S	V_{CC} = 4.5V, I_I = −18 mA			−1.5	V
I_{IH}	High-Level Input Current	A	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
		S	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL}	Low-Level Input Current	A	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
		S	V_{CC} = 5.5V, V_I = 0.4V			−0.4	
I_{OS}	Short-Circuit Output Current (Note 4)		V_{CC} = 5.5V, V_O = 0V	−18		−60	mA
r_I	Input Resistance		V_{CC} = 4.5V, 0V, or Open, ΔV, = 0.15V to 4.15V	7		20	kΩ
I_{CC}	Supply Current		V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 0.7V		19	31	mA
			V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 4V		32	53	

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, in App Note AN-336.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

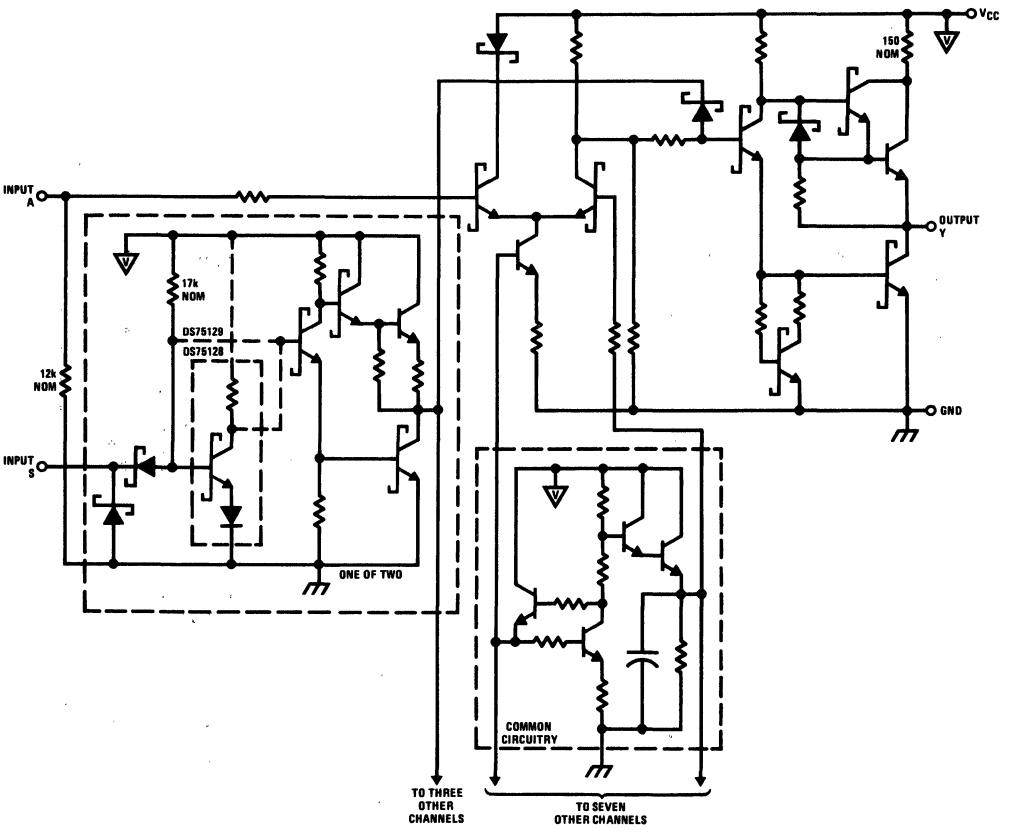
Note 4: Only one output should be shorted at a time.

Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter		Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	A	R_L = 400Ω, C_L = 50 pF, See *Figure 1*	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	A		10	18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	S			20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	S			16	30	ns
t_{PLH} / t_{PHL}	Ratio of Propagation Delay Times	A		0.5	0.8	1.3	
t_{TLH}	Transition Time, Low-to-High-Level Output			1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level Output			1	3	12	ns

Schematic Diagram (each receiver)



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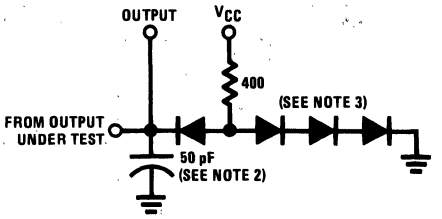
AC Test Circuit and Switching Time Waveforms



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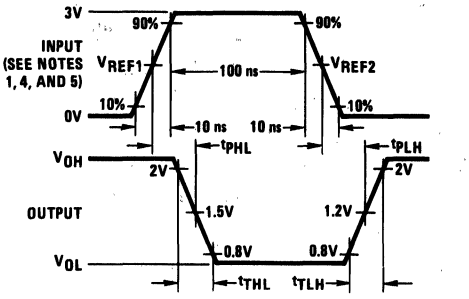

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Note 1: Input pulses are supplied by a generator having the following characteristics: $Z_O = 50\Omega$, PRR = 5 MHz.

Note 2: Includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

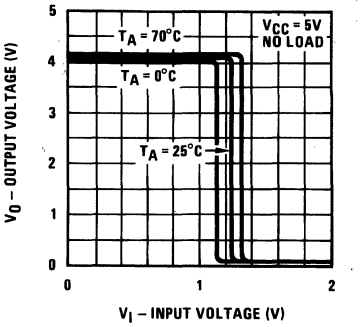
Note 4: The strobe inputs of DS75129 are in-phase with the output.

Note 5: $V_{REF1} = 0.7V$ and $V_{REF2} = 1.7V$ for testing data (A) inputs, $V_{REF1} = V_{REF2} = 1.3V$ for strobe inputs.

FIGURE 1

Typical Characteristics

Voltage Transfer Characteristics From A Inputs



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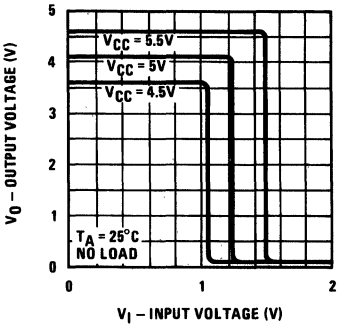
Voltage Transfer Characteristics From A Inputs



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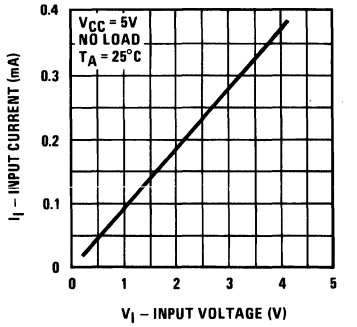
Input Current vs Input Voltage, A Inputs



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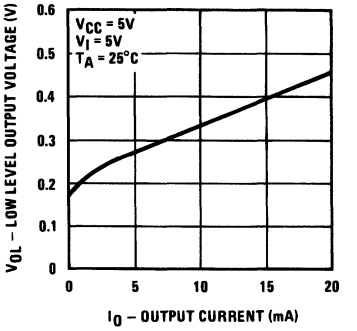
Low-Level Output Voltage vs Output Current



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National Semiconductor

DS7820/DS8820 Dual Line Receiver

General Description

The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

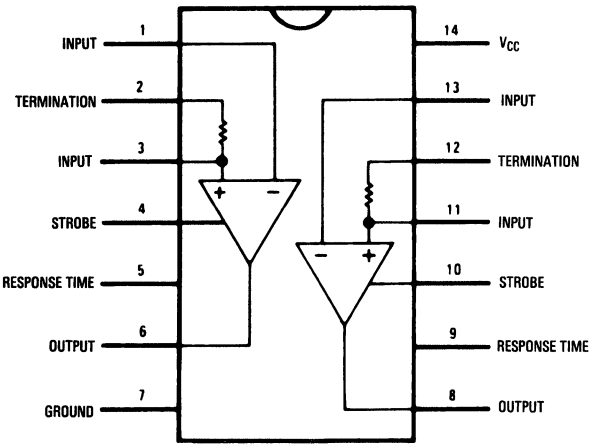
The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fan out of two with TTL integrated circuits
- Strobe low forces output to "1" state

Connection Diagram

Dual-In-Line Package



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Top View

Order Number DS7820J or DS8820N
See NS Package Number J14A or N14A

For Complete Military 883 Specifications, See RETS Data Sheet.
Order Number: DS7820J/883 or DS7820W/883
See NS Package Number J14A or W14B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Maximum Power Dissipation* at 25°C

Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{TH}	Input Threshold Voltage	V_{CM} = 0V	−0.5	0	0.5	V
		−15V ≤ V_{CM} ≤ 15V	−1.0	0	1.0	V
V_{OH}	High Output Level	I_{OUT} ≤ 0.2 mA	2.5		5.5	V
V_{OL}	Low Output Level	I_{SINK} ≤ 3.5 mA	0		0.4	V
R_I^-	Inverting Input Resistance		3.6	5.0		kΩ
R_I^+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C	120	170	250	Ω
t_r	Response Time	C_{DELAY} = 0 pF		40		ns
		C_{DELAY} = 100 pF		150		ns
I_{ST}	Strobe Current	V_{STROBE} = 0.4V		−1.0	−1.4	mA
		V_{STROBE} = 5.5V			5.0	μA
I_{CC}	Power Supply Current	V_{IN} = 15V		3.2	6.0	mA
		V_{IN} = 0V		5.8	10.2	mA
		V_{IN} = −15V		8.3	15.0	mA
I_{IN}^+	Non-Inverting Input Current	V_{IN} = 15V		5.0	7.0	mA
		V_{IN} = 0V	−1.6	−1.0		mA
		V_{IN} = −15V	−9.8	−7.0		mA
I_{IN}^-	Inverting Input Current	V_{IN} = 15V		3.0	4.2	mA
		V_{IN} = 0V		0	−0.5	mA
		V_{IN} = −15V	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

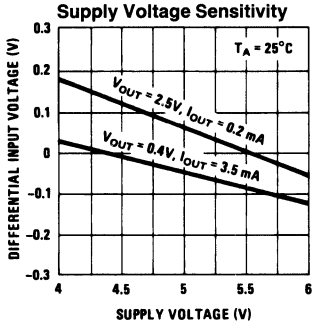
Note 2: These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, −15V ≤ V_{CM} ≤ 15V and −55°C ≤ T_A ≤ +125°C for the DS7820 or 0°C ≤ T_A ≤ +70°C for the DS8820 unless otherwise specified; typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0 unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

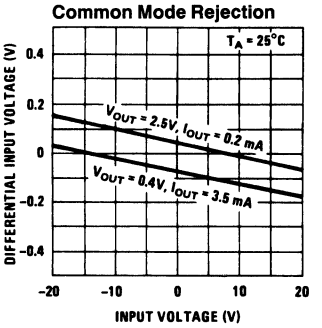
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

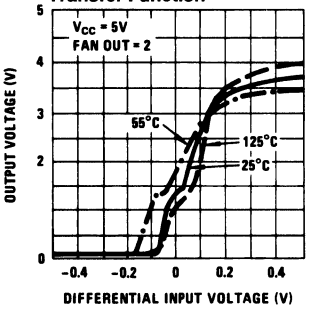
Supply Voltage Sensitivity



Common Mode Rejection



Transfer Function



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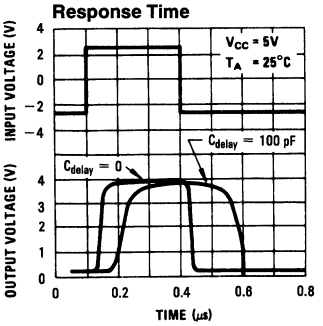
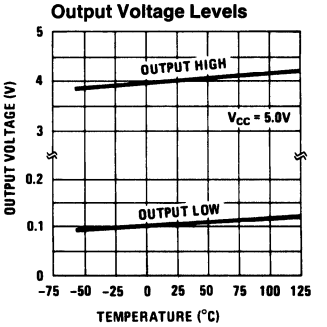
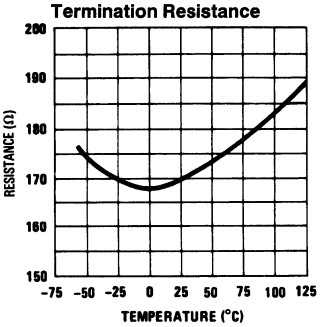
Response Time



Output Voltage Levels



Termination Resistance



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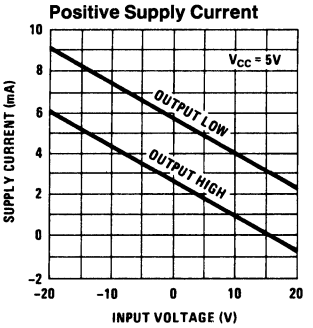
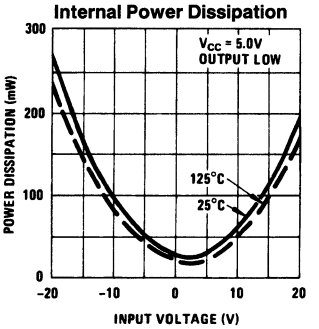
Positive Supply Current



Internal Power Dissipation



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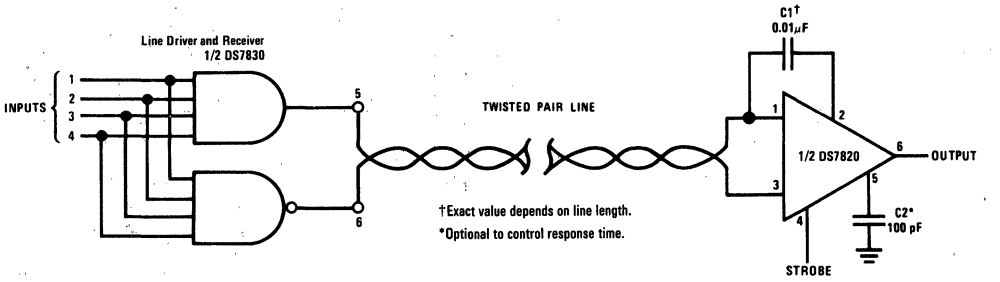
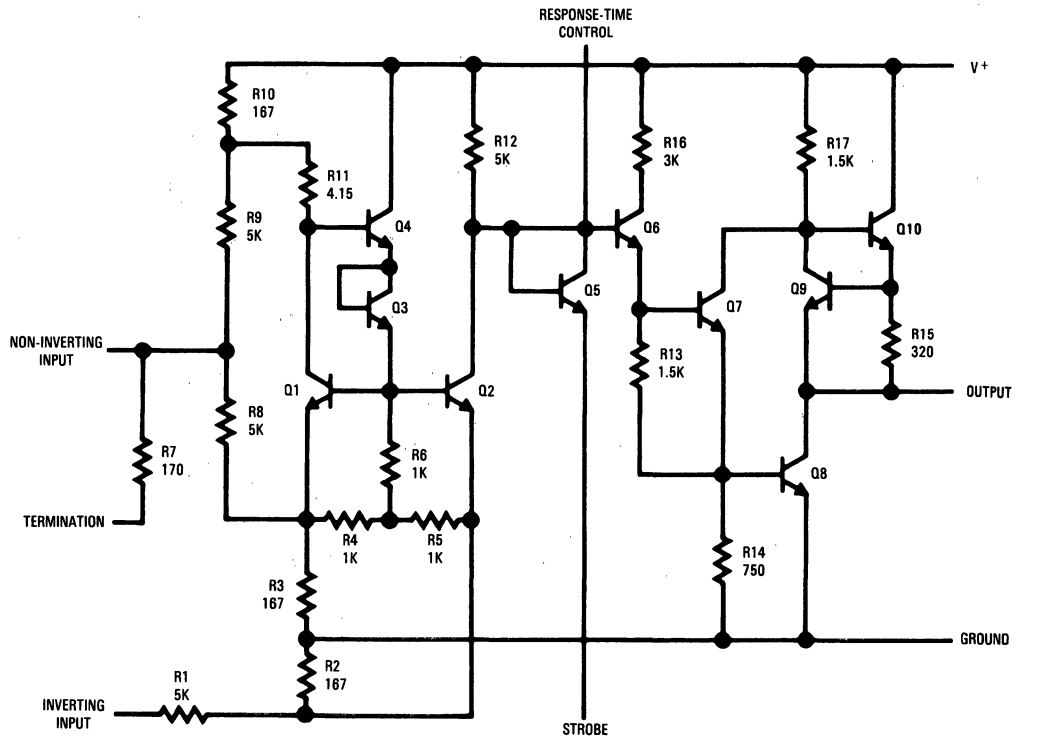
Typical Application



TL/F/5796–3

Schematic Diagram



TL/F/5796–1

National Semiconductor

DS7820A/DS8820A Dual Line Receiver

General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

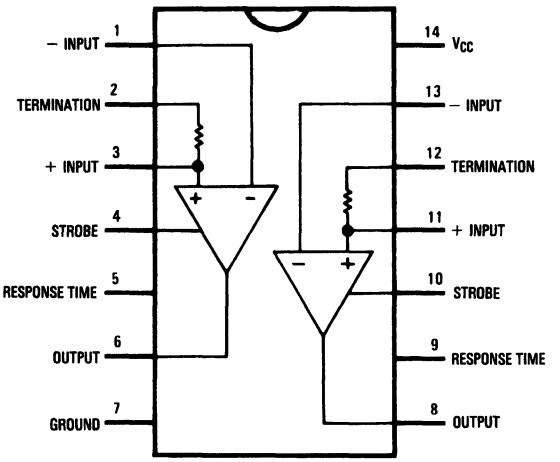
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to +125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

Connection Diagram

Dual-In-Line Package



Note: Pin 7 connected to bottom of cavity package. TL/F/5797–2

Top View

Order Number DS7820AJ or DS8820AN
See NS Package Number J14A or N14A

For Complete Military 883 Specificatons, See RETS Data Sheet.
Order Number DS7820AJ/883 or DS7820AW/883
See NS Package Number J14A or W14B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$	$-3V \leq V_{CM} \leq +3V$			0.06	0.5	V
			$-15V \leq V_{CM} \leq +15V$			0.06	1.0	V
		$I_{OUT} = +16\ mA$, $V_{OUT} \leq 0.4V$	$-3V \leq V_{CM} \leq +3V$			−0.08	−0.5	V
			$-15V \leq V_{CM} \leq +15V$			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$			120	170	250	Ω
I_I^-	Inverting Input Current	$V_{CM} = 15V$				3.0	4.2	mA
		$V_{CM} = 0V$				0	−0.5	mA
		$V_{CM} = -15V$				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	$V_{CM} = 15V$				5.0	7.0	mA
		$V_{CM} = 0V$				−1.0	−1.6	mA
		$V_{CM} = -15V$				−7.0	−9.8	mA
I_{CC}	Power Supply Current One Side Only	I_{OUT} = Logical "0"	$V_{DIFF} = -1V$	$V_{CM} = 15V$		3.9	6.0	mA
				$V_{CM} = -15V$		9.2	14.0	mA
			$V_{DIFF} = -0.5V$, $V_{CM} = 0V$			6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\ \mu A$, $V_{DIFF} = 1V$			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = +16\ mA$, $V_{DIFF} = -1V$			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	$I_{OUT} = +16\ mA$, $V_{OUT} \leq 0.4V$, $V_{DIFF} = -3V$			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	$I_{OUT} = -400\ \mu A$, $V_{OUT} \geq 2.5V$, $V_{DIFF} = -3V$					0.9	V
I_{SH}	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	$V_{STROBE} = 0.4V$, $V_{DIFF} = -3V$				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	$V_O = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$			−2.8	−4.5	−6.7	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820A or $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq +70°C$ for the DS8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0V$ unless stated differently.

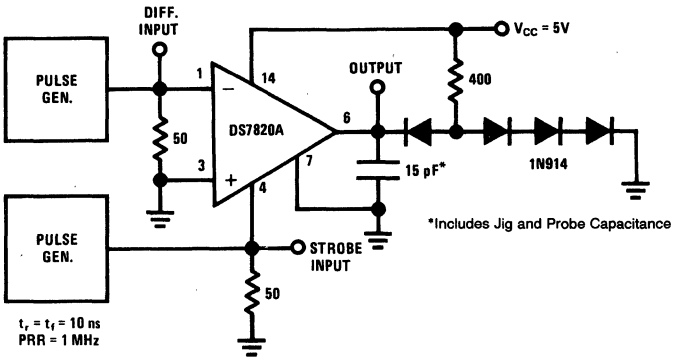
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

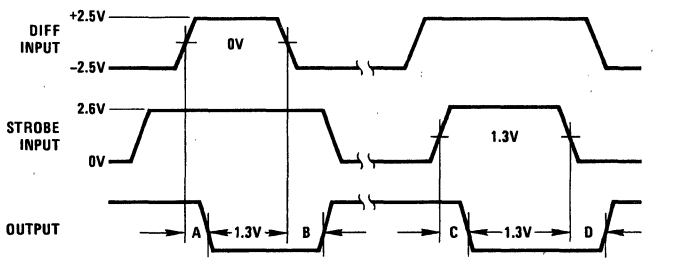
Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay, Differential Input to "0" Output	$R_L = 400\ \Omega$, $C_L = 15$ pF, see *Figure 1*		30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output			27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output			16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output			18	30	ns

AC Test Circuit and Waveforms



TL/F/5797–7



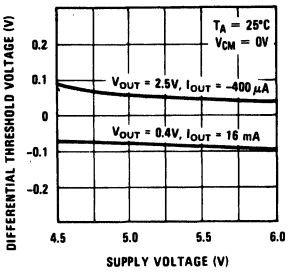
TL/F/5797–8

A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

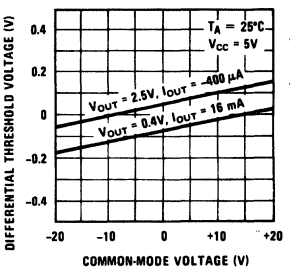
FIGURE 1

Typical Performance Characteristics (Note 3)

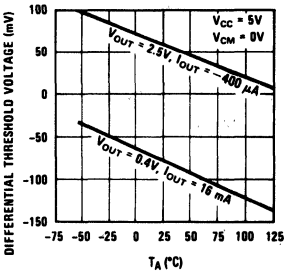
Supply Voltage Sensitivity



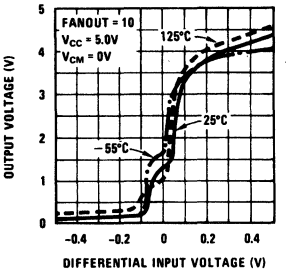
Common-Mode Voltage Sensitivity



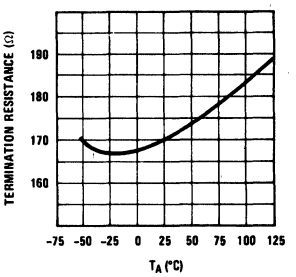
Temperature Sensitivity



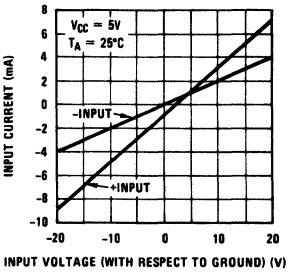
Transfer Function



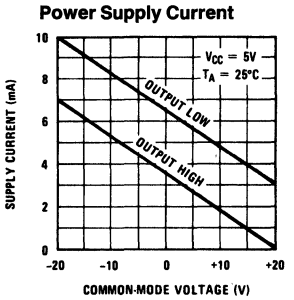
Termination Resistance



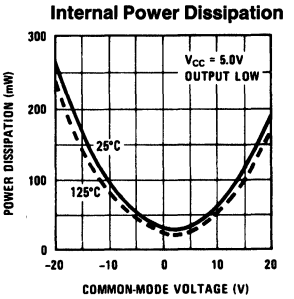
Input Characteristics



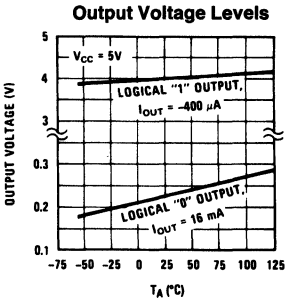
Power Supply Current



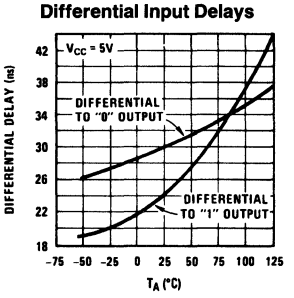
Internal Power Dissipation



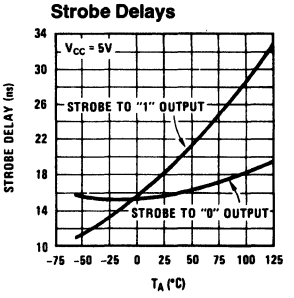
Output Voltage Levels



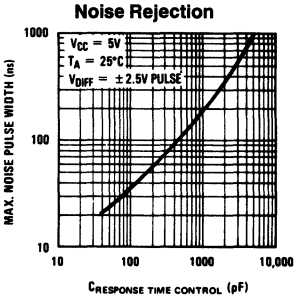
Differential Input Delays



Strobe Delays

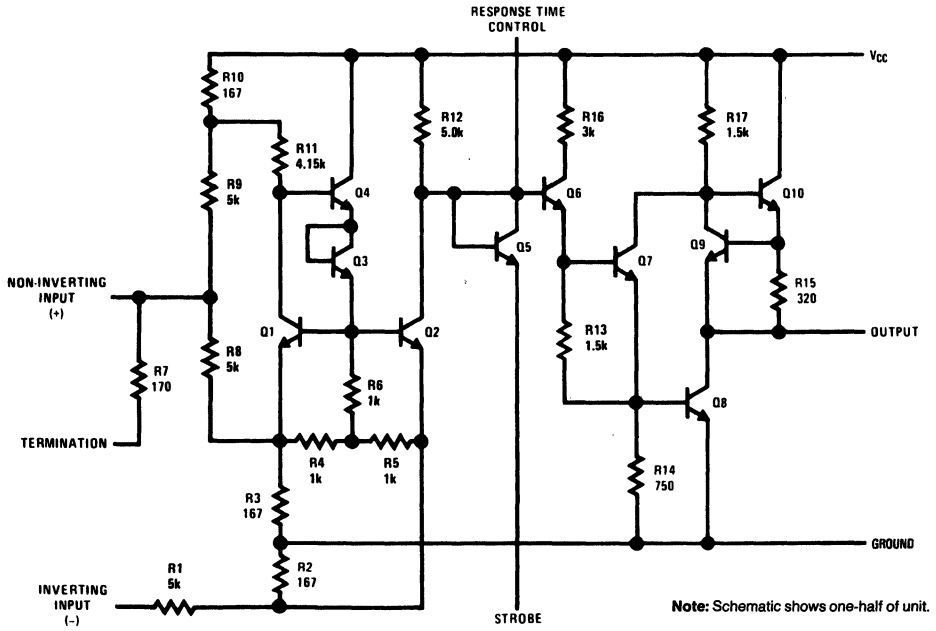


Noise Rejection



TL/F/5797–6

Schematic Diagram

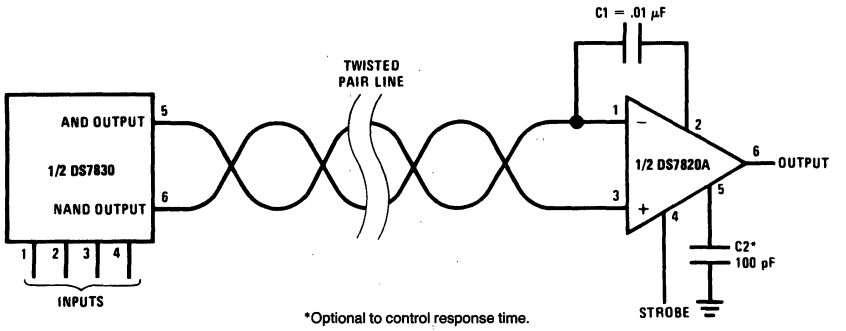


Note: Schematic shows one-half of unit.

TL/F/5797–1

Typical Applications

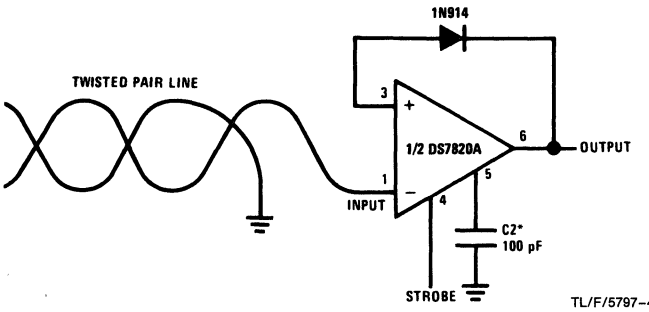
Differential Line Driver and Receiver



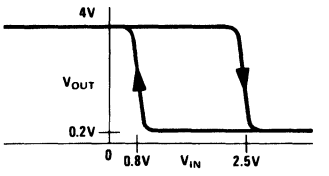
*Optional to control response time.

TL/F/5797–3

Single Ended (EIA-RS232C) Receiver with Hysteresis



TL/F/5797–4



TL/F/5797–5

(Output = "1" for Open Input)

National Semiconductor

DS9622 Dual Line Receiver

General Description

The DS9622 is a dual line receiver designed to discriminate a worst case logic swing of 2V from a ±10V common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors.

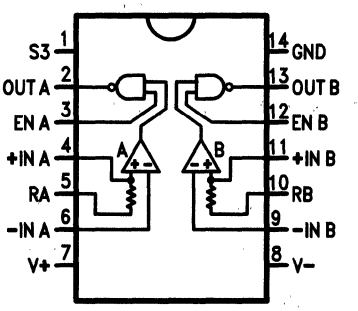
The DS9622 allows the choice of output states with the input open, without affecting circuit performance by use of S3. A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to 12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

Features

- TTL compatible threshold voltage
- Input terminating resistors
- Choice of output state with inputs open
- TTL compatible output
- High common mode
- Wired-OR capability
- Enable inputs
- Logic compatible supply voltages

Connection Diagram

14-Lead DIP



TL/F/9760–2

Top View

For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS9622ME/883,
DS9622MJ/883 or DS9622MW/883
See NS Package Number E20A, J14A or W14B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range	−65°C to +175°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Internal Power Dissipation (Note 5)	400 mW
V^+ to GND	−0.5V to +7.0V
Input Voltage	±15V
Voltage Applied to Outputs for Output High State	−0.5V to +13.2V
V^- to GND	−0.5V to −12V
Enable to GND	−0.5V to +15V

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Temperature, T_A	−55	+125	°C

Electrical Characteristics (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Max	Units
V_{OL}	Output Voltage LOW	$V^+ = S3 = 4.5V, V^- = -11V$, $V_{DIFF} = 2.0V, I_{OL} = 12.4$ mA, EN = Open			0.4	V
V_{OH}	Output Voltage HIGH	$V^+ = 4.5V, V^- = -9.0V$, $S3 = 0V, V_{DIFF} = 1.0V$, $I_{OH} = -0.2$ mA, EN = Open		2.8		V
I_{CEX}	Output Leakage Current	$V^+ = 4.5V, V^- = -11V$, $S3 = 0V, V_{DIFF} = 1.0V$, $V_O = 12V$, EN = Open			200	μA
I_{OS}	Output Short Circuit Current (Note 4)	$V^+ = 5.0V, V^- = -10V$, $V_{DIFF} = 1.0V, V_O = S3 = 0V$, EN = Open		−3.1	−1.4	mA
I_R(EN)	Enable Input Leakage Curent	$V^+ = S3 = 4.5V, V^- = -11V$, I_N = Open, EN = 4.0V			5.0	μA
I_F(EN	Enable Input Forward Current	$V^+ = 5.5V, V^- = -9.0V$ V_I = Open, EN = S3 = 0V		−1.5		mA
I_F(+IN)	+Input Forward Current	$V^+ = 5.0V, V^- = -10V$, $V_I^+ = 0V, V_I^- = GND$, EN = S3 = Open		−2.3		mA
I_F(−IN)	−Input Forward Curent	$V^+ = S3 = 5.0V, V^- = -10V$, $V_I^+ = GND, V_I^- = 0V$, EN = Open		−2.6		mA
V_{IL}(EN)	Input Voltage LOW	$4.5V \le V^+ \le 5.5V$, $-11V \le V^- \le -9.0V$, EN = Open	+25°C		1.0	V
			+125°C		0.7	V
			−55°C		1.3	V
V_{TH}	Differential Input Threshold Voltage	$4.5V, \le V^+ \le 5.5V$, $-11V \le V^- \le -9.0V$, EN = Open		1.0	2.0	V
V_{CM}	Common Mode Voltage	$V^+ = 5.0V, V^- = -10V$, $1.0V \le V_{DIFF} \le 2.0V$	25°C	−10	+10	V
R_T	Terminating Resistance		25°C	91	215	Ω
I^+	Positive Supply Current	$V^+ = S3 = V_I^+ = 5.5V$, $V^- = 11V, V_I^- = 0V$	25°C		22.9	mA
I^-	Negative Supply Current			−11.1		mA
SWITCHING CHARACTERISTICS $T_A = 25°C$						
t_{PLH}	Propagation Delay to High Level	$V^+ = 5.0V$, $V^- = -10V$, $0V \le V_I \le 3.0V$, $C_L = 30$ pF (See *Figure 1*)	$R_L = 3.9$ kΩ		50	ns
t_{PHL}	Propagation Delay to Low Level		$R_L = 390Ω$		50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified Min/Max limits apply across the −55°C to +125°C temperature range. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Rating applies to ambient temperatures up to +125°C. Above 125°C ambient, derate linearity at 120°C/W.

Switching Time Test Circuit and Waveforms

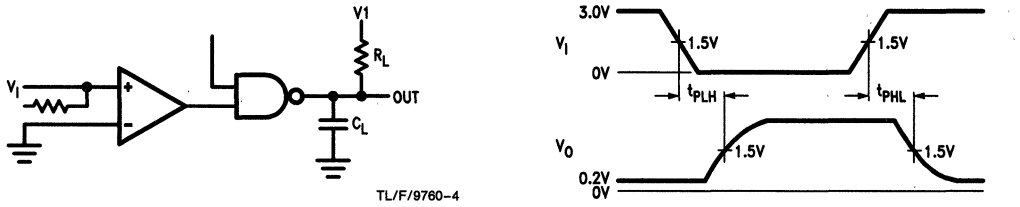
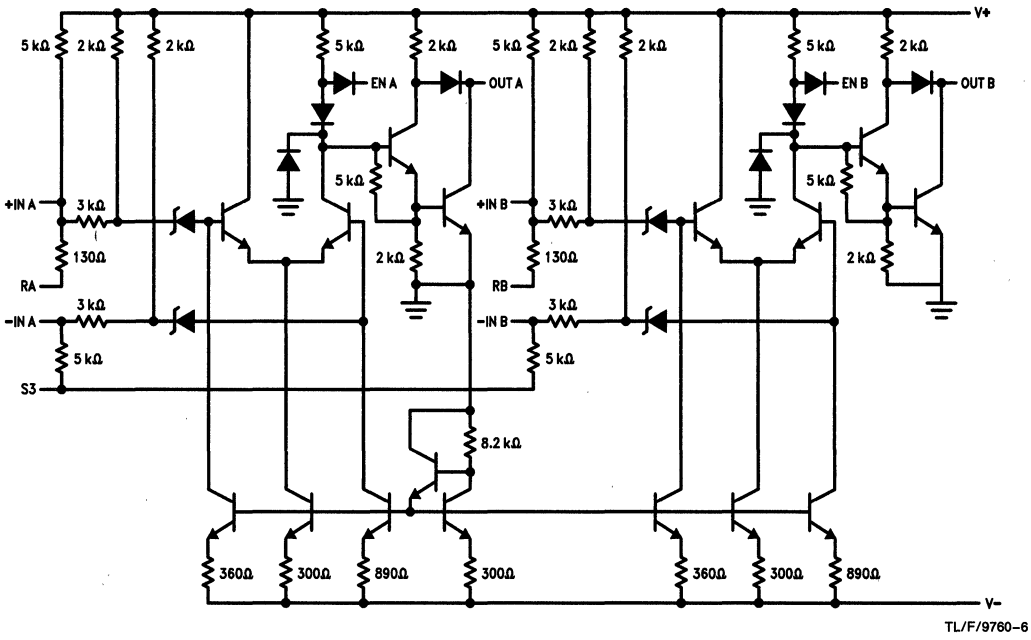


FIGURE 1

Equivalent Circuit



Typical Applications

When S3 is connected to V−, open inputs cause output to be high. When V+ = 5V, V− = −10V and S3 is connected to ground, open inputs cause output to be low.

Section 9

Bus Circuits Introduction

Section 9 Contents

Bus Circuits Introduction

A bus is a common communication medium, such as a printed circuit trace, that is time shared by several elements of a system. A popular example of this is the traditional Backplane. This is illustrated in *Figure 1*. Multiple cards plug into a chassis (cage) and communicate to each other via the connecting PCB (Backplane) located across the back of the cage. This Card to Backplane interface is further illustrated in *Figure 2*. Note that the Bus Circuits are located next to the connector and interface the PCB to the Backplane. Single-ended bus circuits included in this databook may be further categorized into Backplane Transceiver Logic (BTL) circuits, open-collector circuits and TRI-STATE® circuits.

When not transmitting, a bus driver should be capable of presenting a high impedance output in order to allow other drivers to freely use the bus. This is achieved by using either an open-collector (open drain) or TRI-STATE outputs.

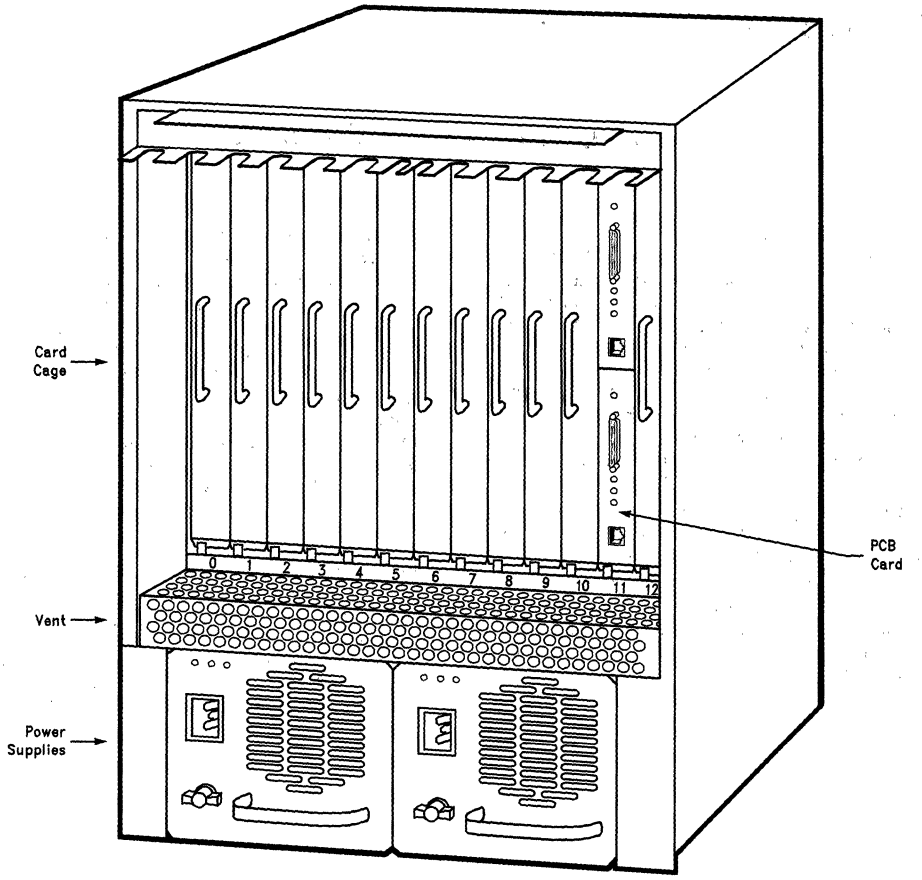
Open-collector drivers may be connected in a wired-or configuration which is very useful for polling and bus arbitration. These devices require pull-up resistors, which can also serve as bus terminators.

TRI-STATE drivers, on the other hand, do not require bus termination for short bus runs on PC boards or Backplanes.

A single-ended bus is susceptible to noise, including ground noise and crosstalk. For this reason the bus should not be extended beyond the subsystem's enclosure without special care. Line lengths in excess of 10 feet are not recommended without the use of noise reduction techniques, such as slew rate control, high receiver thresholds and noise filtering. Devices such as National Semiconductor's DS3662 and DS3862 Trapezoidal bus transceivers and DS3896 and DS3897 BTL transceivers are specifically designed for reducing crosstalk and noise susceptibility on high-speed busses.

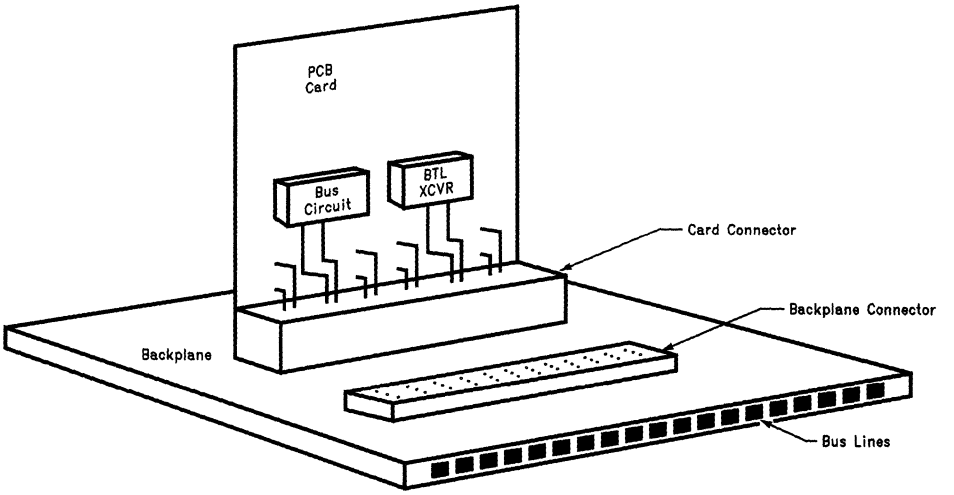
BTL TRANSCEIVERS

The BTL devices are designed for driving high-speed microcomputer backplane buses. These devices use BTL (Backplane Transceiver Logic) technology and incorporate low output capacitance, tight receiver thresholds, and small signal swings with the ability to drive a bus with a loaded impedance of less than 18Ω. This excellent drive capability is achieved while still maintaining high levels of noise immunity.



TL/F/11162–1

FIGURE 1. Backplane Application



TL/F/11162–2

FIGURE 2. PCB-Backplane Interface

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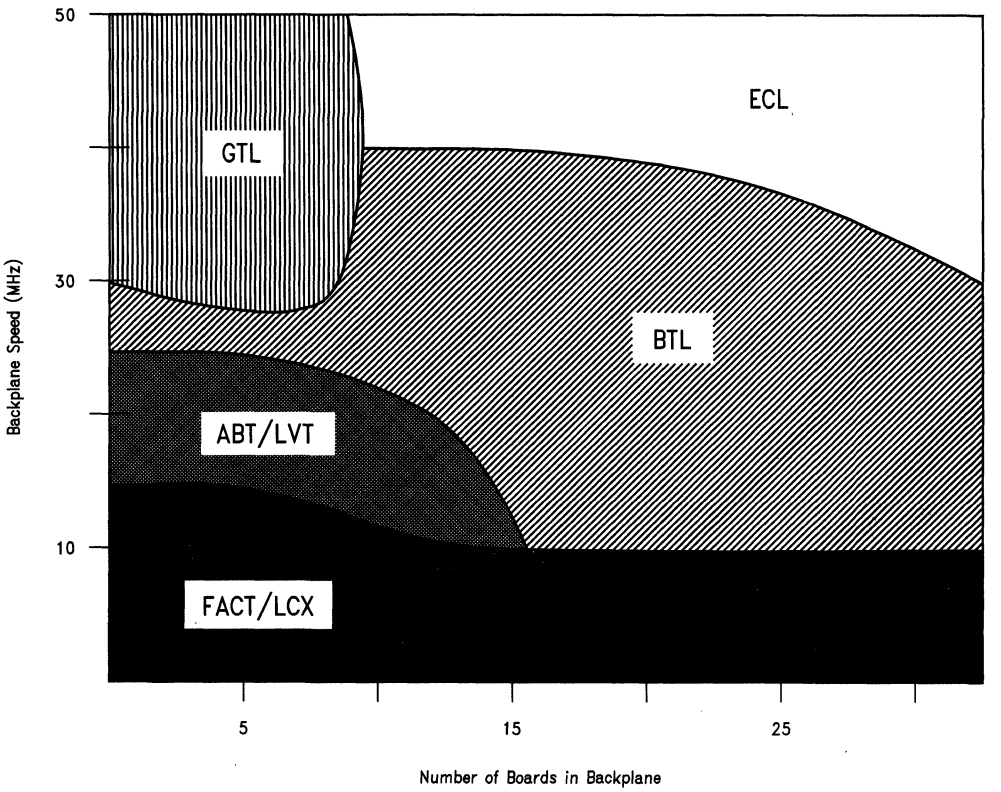
Backplane Technology Relative Selection Guide



TL/F/11464–1

Note: This selection chart is to be used as a pointer towards the technology most appropriate for an application based on number of modules and performance. This does not include such issues as cost and reliability.

Bus Circuits—Selection Guide

BTL TRANSCEIVERS

Device	Temp. Range (C, M)	Function	Channels/ Package	Max Supply Current I_{CC} (mA)	t_{rise}/t_{fall} Min (ns)	Prop Delay Typ (ns)	Package	Comments	Page No.
TRAPEZOIDAL DEVICES									
DS3890	C	Driver	8	100	3	9	N	Trapezoidal Signal Control	10-35
DS3892	C	Receiver	8	80	x	12	N, M	Trapezoidal Signal Control	10-35
DS3896	C	Transceiver	8	135	3	9	N, M	Trapezoidal Signal Control	10-46
DS3897	C	Transceiver	4	80	3	9	N, J, M	Trapezoidal Signal Control	10-46
TURBO DEVICE									
DS3893A	C	Transceiver	4	95	1	3.5	V	Turbotransceiver	10-41
BTL/Futurebus+ DEVICES									
DS3883A	C	Transceiver	9	62	1	3.5	V, VB, VF, W	Data Transceiver	10-5
DS3884A	C, M	Transceiver	6	65	1	3	V, VF, W	Integrated Glitch Filters	10-14
DS3886A	C, M	Transceiver	9	62	1	4.5	V, VB, VF, W	Integrated Latches	10-22
DS38C86A	C	Transceiver	9				V, VF	Low Power CMOS	10-33
PI-BUS DEVICE									
DS1776	M	Transceiver	8	37	2	10	E, J	Non-Inverting, 883 Qualified, Low Power	10-53

Characteristics of BTL Devices

1. One volt signal swings
2. 50 mA–100 mA drivers
3. Tight receiver thresholds, 1.47V–1.62V
4. Less than 5 pF output capacitance
5. All BTL transceiver/driver outputs are inverting unless indicated

Package Designators: J = Ceramic DIP V = PLCC VF = PQFP VB = PQFP
N = Plastic DIP M = SOIC W = Flatpak E = LCC

Temp. Range Designators: C = Commercial 0°C to +70°C
M = Military −55°C to +125°C

Bus Circuits—Selection Guide (Continued)

OPEN-COLLECTOR BUS CIRCUITS

Device Number		Circuits/ Package	Driver/ Receiver/ Transceiver	Bus Driver		Bus Receiver				Comments	Page No.
Commercial 0°C to +70°C	Military −55°C to +125°C			Propagation Delay (ns)	V_{OL} (V)/ I_{OL} (mA)	Propagation Delay (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (V)		
DS26S10C	DS26S10M	4	Transceiver	10	0.8/100	10	1.75/−100	2.25/100			11-21
DS26S11C	DS26S11M	4	Transceiver	10	0.8/100	10	1.75/−100	2.25/100		Input to Bus is Non-Inverting	11-21
DS3662		4	Transceiver	20	0.9/100	25	1.50/400	1.9/100		Trapezoidal Transceiver	11-27
DS3862		8	Transceiver	12	0.9/100	15	1.50/10	1.9/10		Trapezoidal Transceiver	11-36
DS8640	DS7640	4	Receiver			23	1.2/−50	1.8/50		Quad NOR Receiver	11-50
DS8641		4	Transceiver	30	0.7/50	30	1.2/−100	1.8/100			11-52
DS8836	DS7836	4	Receiver			20	1.05/−50	2.65/50	1	Quad NOR Receiver	11-63
DS8837	DS7837	6	Receiver			20	1.05/−50	2.65/50	1		11-65
DS8838	DS7838	4	Transceiver	25	0.8/50	30	1.05/−100	2.65/100	1		11-68

TRI-STATE® BUS CIRCUITS

Device Number		Circuits/ Package	Driver/ Receiver/ Transceiver	Bus Driver			Bus Receiver				Comments	Page No.
Commercial 0°C to +70°C	Military −55°C to +125°C			Propagation Delay Typ (ns)	V_{OL} (V)/ I_{OL} (mA)	V_{OH} (V)/ I_{OH} (mA)	Propagation Delay Typ (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (mV)		
DP8303A		8	Transceiver	10	0.5/50	3.9/−5	10	0.8/−250	2/80		Bidirectional Inverting	11-3
DP8304B	DP7304B	8	Transceiver	10	0.5/50	3.6/−5	15	0.8/−250	2/80		Bidir. Non-Inverting IEEE 488	11-8
DP8307A		8	Transceiver	10	0.5/50	3.6/−5	10	0.8/−250	2/80		Bidirectional Inverting	11-13
DP8308		8	Transceiver	11	0.5/50	3.6/−5	15	0.8/−250	2/80		Bidirectional Non-Inverting	11-17
DS3667		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400		11-31
DS75160A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	11-42
DS75161A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	11-42
DS75162A		8	Transceiver	20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	IEEE 488 GPIB	11-42
DS8833	DS7833	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Non-Inverting TRI-STATE Receiver	11-55
DS8834	DS7834	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Inverting	11-59
DS8835	DS7835	4	Transceiver	14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Inverting TRI-STATE Receiver	11-55

Note: Unless otherwise specified, bus circuits listed above are TTL compatible and use 5V supplies.

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Bus Circuits—Cross Reference Guide

The Bus Circuits Cross Reference Guide is provided as an aid in identifying replacement part numbers. Direct replacements feature identical pin-outs and very similar electrical specifications. Similar replacements also feature the same pin-out, and similar electrical specifications. Consult the data sheets for recommended operating conditions and package availability. Before replacing a specific product, it is recommended to compare electrical, functional, and mechanical specifications. Interchangeability between devices is not guaranteed. Manufacturers' most current data sheets take precedence over this guide. An asterisk (*) represents National's closest replacement.

AMD to National		
Device	**Direct**	**Similar**
AM26S10	DS26S10	
AM26S11	DS26S11	
AM26S12		DS8838*
DP8303	DP8303A	
DP8304B	DP8304B	
DP8307	DP8307	
DP8308	DP8308	
DS8838	DS8838	

Motorola to National		
Device	**Direct**	**Similar**
DS8641	DS8641	
MC3438	DS8838	
MC8T26A	DS8834	
MC74F3893A	DS3893A	

Signetics to National		
Device	**Direct**	**Similar**
N8T34	DS8834	
N8T37	DS8837	
N8T38	DS8838	
N8T380		DS8640*
N8T380		DS8836*

TI to National		
Device	**Direct**	**Similar**
SN75160B	DS75160A	
SN75161B	DS75161A	
SN75162	DS75162A	
SN75162B	DS75162A	
SN75ALS053	DS3893A	
SN75ALS056	DS3896	
SN75ALS057	DS3897	

Intel to National		
Device	**Direct**	**Similar**
P8286	DP8304B	
P8287	DP8303A	

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Application Note—Selection Guide
Bus Circuits

Application Note Number AN-XXXX	Title	Devices Referenced	Related Standard Area
AN-259	The Bus Optimizer	DS3662	
AN-336	Understanding Integrated Circuit Package Power Capabilities		All
AN-337	Reducing Noise on Microcomputer Buses	DS3662	
AN-450	Small Outline (SO) Package Surface Mounting Methods		All
AN-514	Timing Analysis of Synchronous and Asynchronous Buses	DS3896 DS3893	BTL
AN-725	PI-Bus	DS1776	PI-Bus
AN-738	Signals in the Futurebus+ Backplane		BTL
AN-744	Futurebus+ Wired-OR Glitch Effects and Filter	DS3884	BTL
AN-829	IEEE 1194.1 BTL Enabling Technology for High Speed Bus Applications		BTL
AN-834	Live Insertion with BTL Transceivers	DS388X	BTL
AN-835	Futurebus+ BTL Grounding Scheme	DS388X	BTL
AN-839	BTL Power Dissipation Calculation	DS388X	BTL

National Semiconductor

PI-Bus Overview

Dan Mansur

PI-Bus, Parallel Interface Bus, has evolved over the late 1980's to become the backplane of choice for avionics applications. National Semiconductor has utilized its BTL experience and supports the PI-Bus standard by offering a BiCMOS Octal PI-Bus transceiver.

PI-Bus Standard

The PI-Bus standard initially was developed under the Very High Speed Integrated Circuits (VHSIC) program, a program that funds development of advanced semiconductor technology for military use. In an effort to reduce redundant development of avionics subsystems, the U.S. Congress mandated that certain new aircraft programs will need to coordinate technology requirements. To this end, the Joint Integrated Avionics Working Group (JIAWG) was created of armed service and industry representatives to coordinate and standardize duplicative efforts.

The principle output of JIAWG regarding hardware was the creation of a common modular avionics architecture that could be configured to any aircraft. Known as the Advanced Avionics Architecture, it prescribes a bus oriented approach using various combinations of modules to achieve the different avionic needs. The current version of this architecture is known as Common Avionics Baseline III (CAB III) and is also incorporated in the Society of Automotive Engineers' (SAE) specifications. Development is also underway within Aeronautical Radio, Inc. (ARINC) to make PI-Bus the standard avionics backplane for commercial aircraft.

This architecture addresses those functions which could be implemented with common hardware and common computer programs to allow adaptation to either air-to-air or air-to-ground missions. The architecture features a building-block design, using standardized modules that can be plugged into a rack and linked by high speed data busses. Instead of line-replaceable units, the new approach features line-replaceable modules or, as they are now called, common modules.

Applications for the PI-Bus systems include flight control, communications, target acquisitions, weapon delivery, battlefield management, navigation, electronic countermeasures, stores management and radar management. Specific mandated programs include the U.S. Navy Advanced Tactical Aircraft (ATA), the U.S. Air Force Advanced Tactical Fighter (ATF), the U.S. Army Light Helicopter Experiment (LHX). Several existing airframes, such as the F-15 or the F-16, will be retrofitted. In addition, PI-Bus systems are expected to rapidly migrate into the commercial avionics as well.

PI-Bus Backplane Features

The PI-Bus backplane is a linear, multidrop synchronous bus with supports digital message communications between up to 32 modules residing in a single backplane. Messages are transferred datum serial and bit parallel using data size of 16 bits (single word) or 32 bits (double word).

PI-Bus standard uses a master-slave communications protocol which allows the current bus master to read data from one slave or write data to any number of slaves in a single message sequence. Messages may be routed to a particular module using either logical or physical addressing. A number of independent messages may be transmitted during a bus master's tenure. This message formats provide a 32-bit virtual addressing range for each module.

The PI-Bus protocol specifies a set of bus state transitions which control the bus to operate in a pipeline manner at the maximum clock rate allowed by the bus signal propagation delay. Master-Slave handshaking is provided with minimum performance penalty by operating the slave modules in synchronization with the master and using the bus state look-ahead.

National's PI-Bus Transceiver

National's octal PI-Bus transceiver was designed to meet the low power requirements of the military by combining the company's leading BTL (Backplane Transceiver Logic) with an advanced BiCMOS process.

BTL transceivers feature a nominal 1V signal swing for low power consumption, with receivers having precise thresholds for maximum noise immunity, and drivers with low power capacitance to minimize bus loading. These features combine to allow higher bus-data-transfer rates and improved overall system reliability. They also eliminate performance-degrating settling-time delays.

National's patented design and BiCMOS process enable the DS1776 to operate at approximately one-fourth the power of competing devices. The reduced power consumption is reflected in the worst-case current (I_{CC}) requirement of only 37 mA for the DS1776, compared with 145 mA for competing devices. This low power solution can offer up to 1 Amp per board savings, reducing the concerns of avionics manufacturers regarding excessive power consumption in the limited space available.

National Semiconductor

Futurebus+ Overview

David Hawley

Standardized by the IEEE, Futurebus+ promises a maximum data-transfer rate of better than 50 million transfers/s, a 500 percent improvement over current 32-bit buses. What's more, Futurebus+ is extendable to 256 bits.

This bus offers a lot to system designers. Its extremely high data-transfer rate makes it attractive for high-performance I/O operations, such as FDDI or high-resolution graphics. The fine task scheduling provided by the arbitration protocol is a requirement for real-time systems.

Also, its cache coherence, message passing, and split-transaction support allow the design of efficient multiprocessing systems. The standard has generated significant technological advances throughout its long development, starting 10 years ago as the original Futurebus. These include the creation of Backplane Transceiver Logic to boost bus performance, the development of high-performance asynchronous and source-synchronous data-transfer protocols, and the formulation of a unified theory of cache coherence. As it has the possibility of becoming a universal standard bus, it deserves close consideration by anyone designing a backplane-based system.

The performance of Futurebus+ can be expected to vary from system to system, depending largely on the data-transfer mode supported. The asynchronous, full-handshake mode (similar to that of the old Futurebus) uses burst transfers and can be expected to peak between 20 million and 25 million transfers/s. A new source-synchronous mode should operate at over 50 million transfers/s with the next generation of silicon support. Because Futurebus+ supports data-path widths of 32, 64, 128, and 256 bits, a raw data-transfer rate of 1.6 Gbytes/s is conceivable. Even at 32 bits, the 200-Mbytes/s source-transfer rate is five times the peak of VMEbus or Multibus II.

Documents on the use of Futurebus+ in real-time and high-availability systems and those that describe special requirements for industrial and military operating environments are specified by IEEE. Standard bridges are also being specified to VMEbus and Multibus II. Refer to IEEE 896.2 and 896.3 for specific implementation application profile definitions and recommendations.

Futurebus+ has been endorsed by vendors of existing 32-bit buses, including the VME International Trade Association and the Multibus Manufacturer's Group. It also has been selected by the U.S. Navy as one of the standards for future computer contracts.

The high speed of Futurebus+ is due to backplane transceiver logic, which was first produced by National Semiconductor in 1984. BTL was designed specifically to drive backplane transmission lines and provides the fastest possible bus interface in a CMOS or TTL environment. Its characteristics are the foundation upon which the Futurebus+ protocol rests.

With this interface technology, a bus designer can guarantee that a signal will cross the input thresholds of every receiver on the backplane on the incident edge of the propagating wavefront. A BTL bus never has to wait for reflections to settle before signals can be sampled. This allows Futurebus to implement much more efficient and high-performance data-transfer protocols than any TTL-based competitor.

Arbitration

The Futurebus+ specification carefully works out an arbitration procedure designed to optimize the scheduling of requests from multiple modules and to prevent more than one module from trying to transfer data on the bus at the same time. Futurebus+ provides a large number of priority levels for accurate real-time task scheduling, as well as a fairness protocol that allows an even allocation of bus bandwidth to multiple modules. The arbitration takes place on its own independent set of lines in parallel with transfers on the data bus. The Futurebus arbitration mechanism provides a number of other facilities, including error detection and recovery, parking, bus-master identification, emergency messages, and a live insertion-and-withdrawal mechanism for board replacement in high-availability systems.

Data Transfer

Each transaction on Futurebus+ consists of a broadcast connection or address transfer, followed by one of a variety of data transfer types, and finally a broadcast disconnection. The connection phase is used to transmit addresses and commands from the master to the slaves, to return status to the master from the slaves, and for all participating modules to establish their data-transfer capabilities. Those modules that have been selected can participate in the data-transfer handshake, as can any caching modules that have chosen to "snarf" (induce data broadcast) or intervene. The disconnection phase is used to transfer information only during split transactions, when it provides the identity of the requester and the status of the response.

Cache Coherence

The Futurebus+ cache protocols allow this specialized memory to perform its three main functions automatically and completely transparent to the software. The first function is to convert a microprocessor's semirandom reads and writes into efficient burst transfers on the bus. The second is to provide the microprocessor with a fast local window into the system memory space. The third is to provide the basis for a multiprocessing architecture.

An action by one cache affects every other cache in such a way that a consistent view of shared data is maintained. Futurebus+ provides the transaction set necessary to implement this shared-memory system efficiently.

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NEWBRIDGE MICROSYSTEMS

The National Semiconductor/Newbridge Microsystems Futurebus + Partnership

National Semiconductor and Newbridge Microsystems are partners in the development of a high performance Futurebus+ Interface Chipset. This partnership provides end users with the design, applications and manufacturing expertise of both National Semiconductor and Newbridge Microsystems. Newbridge Microsystems is the primary designer, and sales and marketing channel for the Logical Interface Futurebus+ Engine (LIFE™). National Semiconductor manufactures the LIFE chip for Newbridge Microsystems. The design, manufacture, marketing and support for the transceivers are provided solely by National Semiconductor.

Contact us if you have any questions or comments about our products.

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Additional National Technical Documentation Available on Futurebus +

Documents can be obtained from National's customer support centers (listed on the back cover of this databook).

DS3885	Datasheet	BTL Arbitration Transceiver
DS3875	Datasheet	Futurebus+ Arbitration Controller
AN-1036	Ap. Note	What is Futurebus+?
AN-668	Ap. Note	Futurebus+ Asynchronous Slave Memory Design
AN-742	Ap. Note	DS3885 Arbitration Transceiver
AN-751	Ap. Note	Futurebus+ I/O Board Design
AN-833	Ap. Note	Futurebus+ Chip Set Pin Connections
AN-836	Ap. Note	Futurebus+ Protocol Controller Design for a MC68040 Based Board
AN-837	Ap. Note	A Complete Solution for Futurebus+ and Arbitration Schemes
AN-838	Ap. Note	Designing a Futurebus+ Central Arbiter

Section 10

BTL Bus Circuits

Section 10 Contents

Backplane Transceiver Logic (BTL) Introduction

Since 1985, BTL has grown from a new bus driving technology to the industry standard, (IEEE1194.1) for driving high performance backplane buses. The evolution of BTL resulted from the need to replace TTL devices which are not suited to drive heavily loaded backplanes at very fast and reliable data rates. In order to see why BTL is the technology of choice, one must first look at the problems BTL was designed to solve.

The TTL Bus Driving Problem

BTL was invented by National Semiconductor Corporation and first introduced in 1985 to solve the bus driving problem created by deficiencies in TTL drivers. TTL devices are not suited to drive characteristically low impedance buses which result from a capacitive load in each backplane card slot in a running computer system. Typical TTL bus drivers have an output capacitance of 12 pF–20 pF per transceiver. This, when coupled with the capacitive loading resulting from the connectors, holes, vias and printed circuit traces results in a lumped slot capacitance of 20 pF–25 pF.

The high output capacitance of each board results in a low characteristic impedance for the backplane signal lines. In order to drive a signal through the threshold region, a high current drive is required. Most TTL devices specify a sink current of 64 mA–200 mA. This large current drive that is needed by these TTL devices results in the high transceiver output capacitance. In order to have incident wave switching of a signal with these parts, (i.e., do not have to wait for reflections to force signal transition through threshold), even more current drive than that which is specified in devices today is required to transition a line through TTL's 3V signal swing. The TTL bus driving problem arises when attempting incident wave switching. A TTL device must have higher drive current than presently available. Increasing this drive current also brings about an increased output capacitance for the device. This scenario increases the overall bus loading and once again lowers the characteristic impedance of the backplane which requires even more current drive *(Figure 1)*.

The result of this cyclic problem was a compromise that had to be made in performance. A bus using TTL driving logic must rely upon reflections at the bus terminations in order to send the signal completely through from one logical signal level to another. The performance hit is evident by looking at the specifications for VMEbus which requires a 35 ns settling delay for reflections before a board can review the data or control lines that transitioned on the bus. The only delay incorporated in a BTL system is based upon the actual performance of the BTL drivers and receivers and time for a signal to propagate down a backplane.

The BTL Solution to the Bus Driving Problem

The endless cycle described above is the problem faced by system and transceiver designers in their quest to obtain the highest level of system performance that is physically possible.

Since 1985, BTL has been adopted by many proprietary backplane bus designers and has become the backplane driver of choice in heavily loaded high speed systems. BTL is also specified as the physical layer for Futurebus+ systems.

BTL incorporates a unique transceiver design which limits the amount of output capacitance for the transceiver *(Figure 2)*.

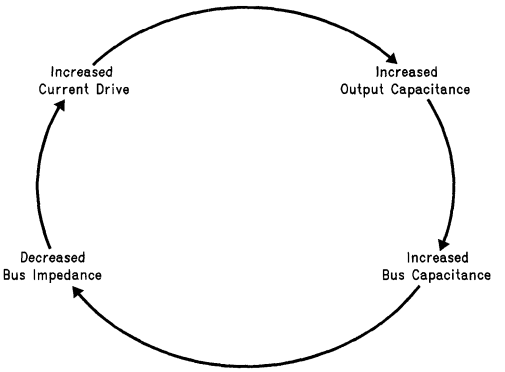

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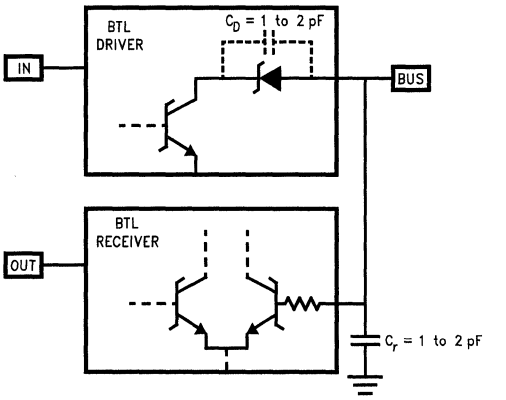
FIGURE 1. TTL Bus Driving Problem



TL/F/11152–2

FIGURE 2. The BTL Transceiver

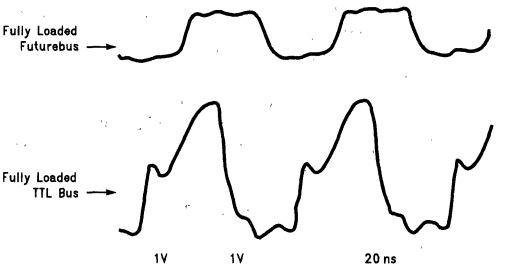
The BTL transceiver solves the output capacitance problem by inserting a Schottky diode in series with the driving transistor. This isolates the driver capacitance to that of the reverse biased Schottky diode, and the result becomes a driver capacitance of 1 pF–2 pF. Another 1 pF–2 pF for a BTL receiver puts the total BTL device capacitance at <5 pF as required by the IEEE P1194 specification. The 5 pF capacitance specification is very crucial for transceiver manufacturers to meet. Any excess capacitance taken up by a transceiver would result in system designers having to layout their boards with BTL transceiver to connector stub lengths that physically are not capable with any sized package.

This reduced transceiver output capacitance is only part of the BTL solution. BTL also specifies a 1V signal swing with tightly controlled receiver thresholds. The 1V swing with the BTL required 80 mA drive current, enables an incident wave switching to occur and does not require reflections to pass a signal through the threshold region. The 1V signal swing also enables reduced power consumption. The tight receiver thresholds are required in order to guarantee accurate noise margin which are critical since a signal only switches between 1V and 2.1V. As a result, any BTL transceiver must have a separate ground and V_{CC} pins which are only connected to separate receiver threshold control circuitry, otherwise noise margins can not be reliably controlled.

A BTL backplane bus is also terminated at both ends to 2.1V, with resistors selected to match the bus impedance. A TTL bus with a 3V signal swing, high current drivers and such a large output capacitance can not be equally matched which also results in a less reliable signal.

The end result of the BTL solution to the TTL bus driving problem can be seen in the actual backplane waveforms below *(Figure 3)*.

Slot Spacing 1.0" and Number of Slots = 18



TL/F/11152–3

FIGURE 3. Actual BTL vs TTL Waveforms

The clean, reliable waveforms with incident wave switching has caught the eye of many proprietary system designers, and also BTL is undoubtedly the bus transceiver of choice for high performance systems.

National Semiconductor

DS3883A BTL 9-Bit Data Transceiver

General Description

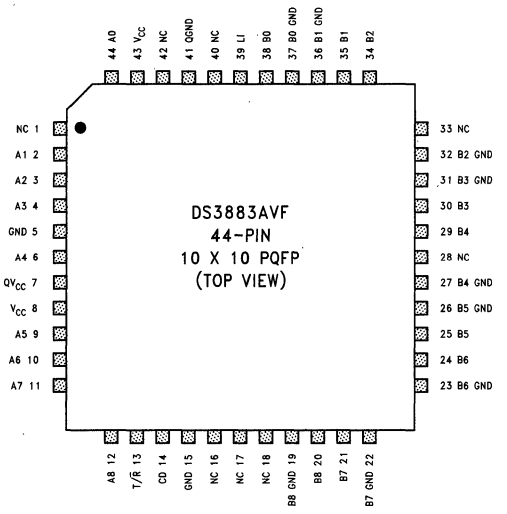
The DS3883A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3883A, is a BTL 9-bit Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. Utilization of the DS3883A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

The DS3883A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The combined output capacitance of the driver and receiver input is less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.
(Continued)

Features

- 9-bit Inverting BTL transceiver meets IEEE 1194.1 standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low bus-port voltage swing (typically 1V) at 80 mA
- Open collector bus-port output allows Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible driver and control inputs
- Built in bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Exceeds 2 kV ESD (Human Body Model)
- Individual bus-port ground pins minimize ground bounce
- Product offered in PLCC and PQFP package styles
- 7 x 7 PQFP requires 50% less PCB space than 10 x 10 PQFP
- Tight skew (1 ns typical)

Connection Diagrams



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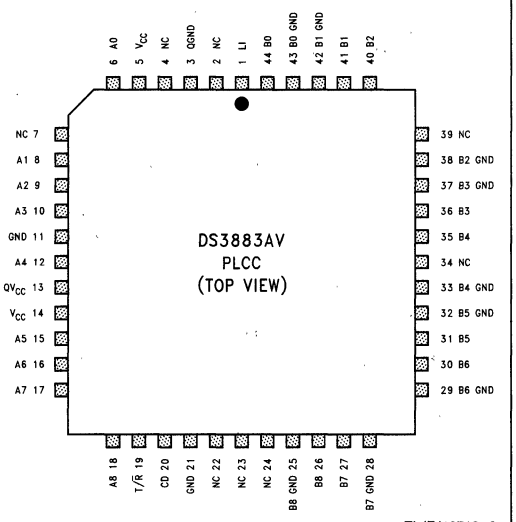

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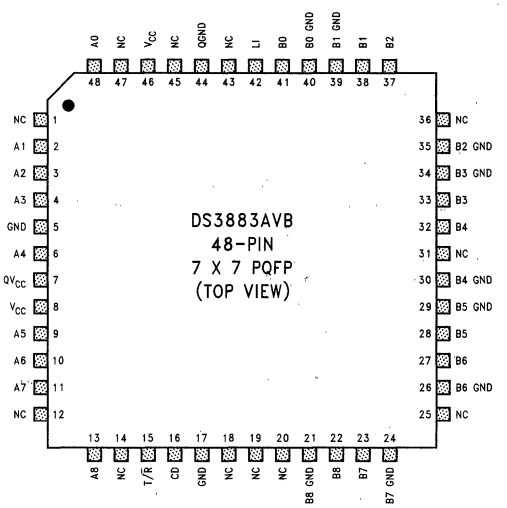
Connection Diagrams (Continued)



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(Note: NC = No Connect)

Order Number DS3883AV, DS3883AVF or DS3883AVB
See NS Package Number V44A, VF44B orVBH48A

General Description (Continued)

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. BTL eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's control and driver inputs are designed with high impedance PNP input structures and are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The DS3883A supports live insertion as defined in 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V_{CC} pin. The DS3883A also provides glitch free power up/down protection during power sequencing.

The DS3883A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two logic V_{CC} pins on the DS3883 that provide the supply voltage for the logic and control circuitry. Multiple power pins reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

Additionally, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS3883A. They are the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3883, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power-up/down sequencing.

When CD (Chip Disable) is high, An and Bn are in a high impedance state. To transmit data (An to Bn) the T/$\overline{R}$ signal is high. To receive data (Bn to An) the T/$\overline{R}$ signal is low.

Additional transceivers included in the Futurebus+ family are the DS3884A BTL Handshake Transceiver featuring selectable Wired-OR glitch filtering; the DS3885 BTL Arbitration Transceiver with arbitration competition logic for the AB<7:0>/$\overline{ABP}$ signal lines; and the DS3886A BTL 9-bit Latching Data Transceiver featuring edge triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

The Logical Interface Futurebus+ Engine (LIFE) is a high performance Futurebus+ Protocol Controller designed for IEEE P896.1. The LIFE will handle all handshaking signals between the Futurebus+ and the local bus interface. The LIFE supports the Futurebus+ compelled mode data transfer as both master and slave. The LIFE can be configured to operate in compliance to IEEE 896.2 Profile B mode. The LIFE incorporates a DMA controller and 64-bit FIFO's for fast queuing. The DS3883A is offered in 44-pin PLCC, 44-pin PQFP, and 48-pin PQFP high density package styles.

The 48-pin PQFP is a 7 x 7 space savings package that requires 50% less PCB space than the 44-pin 10 x 10 PQFP package.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage		6.5V
Control Input Voltage		6.5V
Driver Input and Receiver Output		5.5V
Receiver Input Current		±15 mA
Bus Termination Voltage		2.4V
Power Dissipation at 25°C	PLCC (V44A)	2.5W
	PQFP (VF44B)	1.3W
	PQFP (VBH48A)	1.59W
Derate PLCC Package (V44A)		20 mW/°C
Derate PQFP Package (VF44A)		11.1 mW/°C
Derate PQFP Package (VBH48A)		12.8 mW/°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)		260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.06	2.14	V
Operating Free Air Temperature	0	70	°C

DC Electrical Characteristics (Notes 2 and 3) T_A = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT (CD, T/$\overline{R}$, An)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			250	µA
I_{IH}	Input High Current	$V_{IN} = 2.4V$, AN = CD = 0.5V, T/$\overline{R}$ = 2.4V			40	µA
I_{IL}	Input Low Current	$V_{IN} = 0.5V$, AN = CD = 0.5V, T/$\overline{R}$ = 2.4V			−100	µA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT (Bn)						
V_{OLB}	Output Low Bus Voltage (Note 5)	An = T/$\overline{R}$ = 2.4V, CD = 0.5V I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OFF}	Output Off Low Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 0.75V, CD = 0.5V			−200	µA
	Output Off High Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 2.1V, CD = 0.5V			200	µA
	Output Off Low Current—Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 0.75V			−50	µA
	Output Off Low Current—Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 2.1V			50	µA
V_{TH}	Receiver Input Threshold	T/$\overline{R}$ = CD = 0.5V	1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, I_{Bn} = 1 mA, CD = T/$\overline{R}$ = 0V An = 0V	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, I_{Bn} = 10 mA, CD = T/$\overline{R}$ = 0V An = 0V	2.9	3.9	5.0	V
V_{CLN}	Negative Clamp Voltage	$I_{CLAMP} = -12$ mA, CD = T/$\overline{R}$ = 0.5V			−1.2	V
RECEIVER OUTPUT (An)						
V_{OH}	Voltage Output High	Bn = 1.1V, T/$\overline{R}$ = CD = 0.5V, $I_{OH} = -2$ mA	2.4	3.2		V
V_{OL}	Voltage Output Low	T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 24 mA		0.35	0.5	V
		T/$\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 8 mA		0.35	0.4	V
I_{OZ}	TRI-STATE® Leakage Current	An = 2.4V, CD = 2.4V, T/$\overline{R}$ = 0.5V			10	µA
		An = 0.5V, CD = 2.4V, T/$\overline{R}$ = 0.5V			−10	µA
I_{OS}	Output Short Circuit Current	Bn = 1.1V, T/$\overline{R}$ = CD = 0.5V (Note 4)	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CC}	Supply Current: Includes V_{CC}, QV_{CC} and LI	T/$\overline{R}$ = All An Inputs = 2.4V, CD = 0.5V			62	mA
		CD = T/$\overline{R}$ = 0.5V, All Bn Inputs = 2.1V			53	mA

DC Electrical Characteristics (Notes 2 and 3) T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENT (Continued)						
I_{LI}	Live Insertion Current	T/$\overline{R}$ = CD = An = 0.5V, Bn = Open, V_{CC} = QV_{CC} = 5.5V			2.2	mA
		T/$\overline{R}$ = All An = 2.4V, CD = 0.5V, Bn = Open V_{CC} = QV_{CC} = 5.5V			4.5	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed V_{CC} + 0.5V and shall not exceed the absolute maximum rating at any time, including power-up and power-down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions: V_{CC} = 5V and T_A = 25°C, unless otherwise stated.

Note 4: Only one output should be shorted at a time, and duration of the short should not exceed one second.

Note 5: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Note 6)

This AC table applies to DS3883AVF (10 x 10 PQFP) and DS3883AV (PLCC) only.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *2*)	1	3.5	6	ns
t_{PLH}				1	3.5	6	ns
t_{PHL}	CD to Bn	Enable Time	T/$\overline{R}$ = An = 3V (*Figures 1* and *3*)	3	6	9	ns
t_{PLH}		Disable Time		2.5	5	8	ns
t_{PHL}	T/$\overline{R}$ to Bn	Enable Time	(*Figures 8* and *9*) CD = 0V	9	13.5	18	ns
t_{PLH}		Disable Time		2	6	10	ns
t_r	Transition Time—Rise/Fall 20% to 80%		(*Figures 1* and *2*) CD = 0V, T/$\overline{R}$ = 3V (Note 10)	1	2.5	4.5	ns
t_f				1	2	4.5	ns
SR	Slew Rate is Calculated from from 1.3V to 1.8V		(*Figures 1* and *2*) (Note 10) CD = 0V T/$\overline{R}$ = 3V			0.5	V/ns
t_{SKEW}	An to Bn Skew (Same Package)		(Note 7)		1	3.5	ns
RECEIVER							
t_{PHL}	Bn to An		CD = T/$\overline{R}$ = 0V (*Figures 4* and *5*)	2	4	7	ns
t_{PLH}				1.5	4.5	7.5	ns
t_{PLZ}	CD to An	Disable Time	Bn = 2.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	4	8	12	ns
t_{PZL}		Enable Time		2.5	6	9	ns
t_{PHZ}		Disable Time	Bn = 1.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	3	6.5	10	ns
t_{PZH}		Enable Time		2	6	10	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	CD = 0V Bn = 2.1V (*Figures 8* and *9*)	3	7	12	ns
t_{PZL}		Enable Time		4	10	16	ns
t_{PHZ}		Disable Time	Bn = 1.1V, CD = 0V (*Figures 6* and *7*)	2	6.5	10	ns
t_{PZH}		Enable Time		3	7	11	ns
t_{SKEW}	Bn to An Skew (Same Package)		(Note 7)		1	3.5	ns
PARAMETERS NOT TESTED							
C_{output}	BTL Output Capacitance		(Note 8)		5		pF
t_{NR}	Noise Rejection		(Note 9)		1		ns

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Note 6)

This AC table applies to DS3883AVB (7 x 7 PQFP) only.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *2*)	0.5	2	5.5	ns
t_{PLH}				0.5	3	5.5	ns
t_{PHL}	CD to Bn	Enable Time	T/$\overline{R}$ = An = 3V (*Figures 1* and *3*)	2	5	9	ns
t_{PLH}		Disable Time		2	4	7.5	ns
t_{PHL}	T/$\overline{R}$ to Bn	Enable Time	(*Figures 8* and *9*) CD = 0V	9.5	12	17	ns
t_{PLH}		Disable Time		0.5	5	10	ns
t_r	Transition Time—Rise/Fall 20% to 80%		(*Figures 1* and *2*) CD = 0V, T/$\overline{R}$ = 3V (Note 10)	0.5	1.5	4.5	ns
t_f				0.5	1.5	4.5	ns
SR	Slew Rate is Calculated from from 1.3V to 1.8V		(*Figures 1* and *2*) (Note 10) CD = 0V T/$\overline{R}$ = 3V		0.4	0.85	V/ns
t_{SKEW}	An to Bn Skew (Same Package)		(Note 7)		1	3.5	ns
RECEIVER							
t_{PHL}	Bn to An		CD = T/$\overline{R}$ = 0V (*Figures 4* and *5*)	1.5	4	7	ns
t_{PLH}				1.5	4	7.5	ns
t_{PLZ}	CD to An	Disable Time	Bn = 2.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	5	7	12	ns
t_{PZL}		Enable Time		1	5	9	ns
t_{PHZ}		Disable Time	Bn = 1.1V, T/$\overline{R}$ = 0V (*Figures 6* and *7*)	2.5	6.5	10	ns
t_{PZH}		Enable Time		1.5	4.5	10	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	CD = 0V Bn = 2.1V (*Figures 8* and *9*)	3.5	6.5	12	ns
t_{PZL}		Enable Time		6	10	16	ns
t_{PHZ}		Disable Time	Bn = 1.1V, CD = 0V (*Figures 6* and *7*)	1	6	11	ns
t_{PZH}		Enable Time		2	5	11	ns
t_{SKEW}	Bn to An Skew (Same Package)		(Note 7)		0	3.5	ns
PARAMETERS NOT TESTED							
C_{output}	BTL Output Capacitance		(Note 8)		5		pF
t_{NR}	Noise Rejection		(Note 9)		1		ns

Note 6: Input waveforms shall have a rise/fall time of 3 ns. Propagation delays are measured with a single output switching.

Note 7: t_{SKEW} is an absolute value defined as differences seen in propagation delays between drivers in the same package with identical load conditions.

Note 8: The parameter is tested using TDR techniques described in 1194.0 BTL backplane Design Guide.

Note 9: This parameter is tested during device characterization. The measurement revealed that the part will reject 1 ns pulse widths.

Note 10: Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5 V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1V DC.

Pin Description

Pin Name	Number of Pins	Input/ Output	Description
A0–A8	9	I/O	TTL TRI-STATE receiver output and driver input
B0–B8	9	I/O	BTL receiver input and driver output
B0GND–B8GND	9	NA	Parallel driver grounds reduce ground bounce due to high current switching of driver outputs. (Note 11)
CD	1	I	Chip Disable
GND	2	NA	Ground for switching circuits. (Note 11)
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 12)
NC	8	NA	No Connect
QGND	1	NA	Ground for receiver input bandgap reference and non-switching circuits. (Note 11)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits. (Note 12)
T/$\overline{R}$	1	I	Transmit/$\overline{\text{Receive}}$—transmit (An to Bn), receive (Bn to An)
V_{CC}	2	NA	V_{CC} supply for switching circuits. (Note 12)

Note 11: The multiplicity of parallel ground paths reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance. (i.e., ground plane with power pins and many signal pins connected to the backplane ground.) If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

Note 12: The same considerations for ground are used for V_{CC} in reducing lead inductance (see Note 11). QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Truth Table

CD	T/$\overline{R}$	An	Bn (BTL)
H	X	Z	H
L	L	L	H
L	L	H	L
L	H	H	L
L	H	L	H

X = High or low logic state

Z = High impedance state

L = Low state

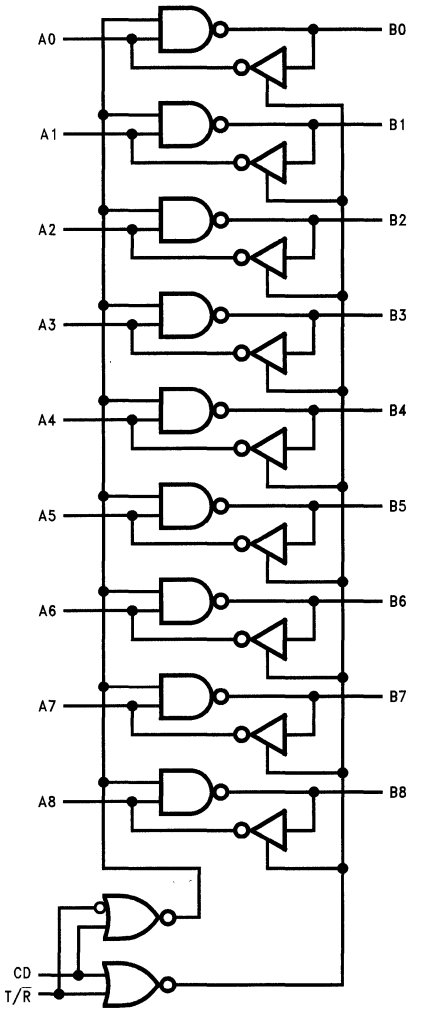
H = High state

Package Thermal Characteristics

Linear Feet per Minute Air Flow (LFPM)	θ_{JA} (°C/W)		
	44-Pin PQFP	48-Pin PQFP	44-Pin PLCC
0	82	76	45
225	68	60	35
500	60	54	30
900	53	48	26

Note: The above values are typical values and are different from the Absolute Maximum Rating values, which include guardbands.

Logic Diagram



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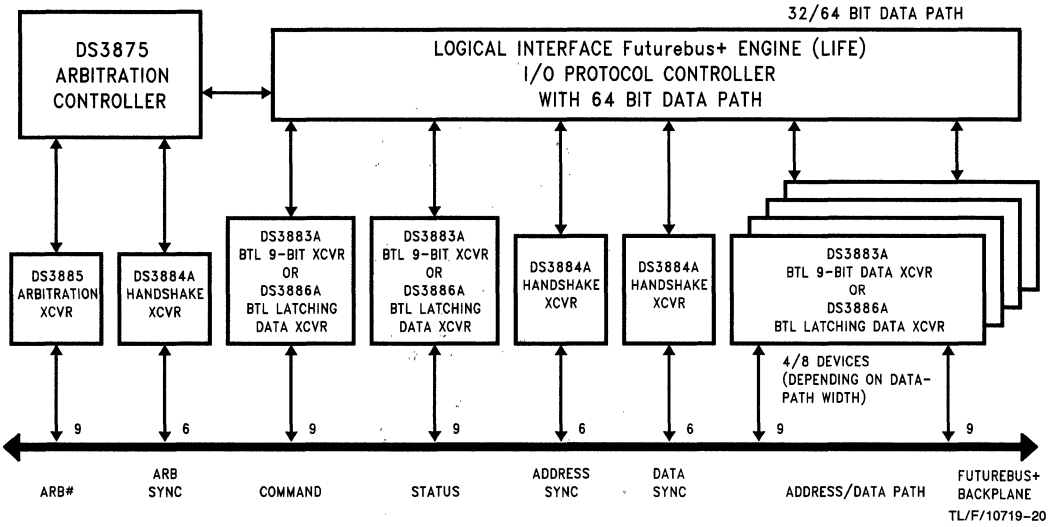
Typical Application



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Test Circuit and Timing Waveforms

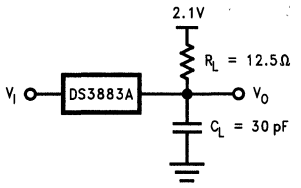

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FIGURE 1. Driver Propagation Delay Set-Up

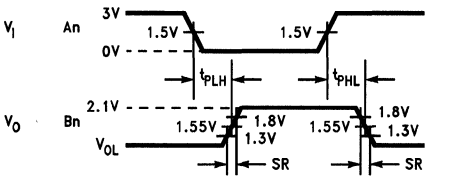

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FIGURE 2. Driver: An to Bn, SR

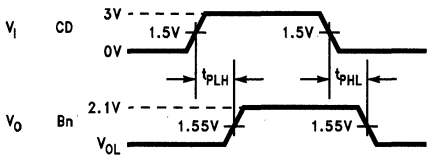

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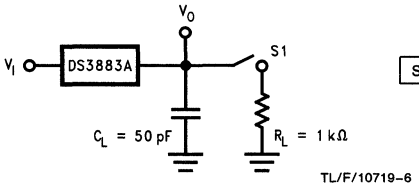
FIGURE 3. Driver: CD to Bn



Switch Position

	t_{PLH}	t_{PHL}
S1	Open	Close

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FIGURE 4. Receiver Propagation Delay Set-Up

Test Circuit and Timing Waveforms (Continued)

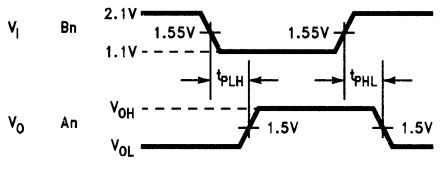

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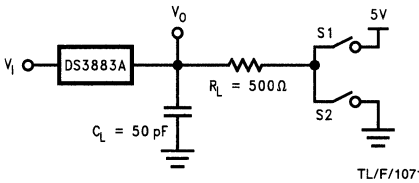
FIGURE 5. Receiver: Bn to An



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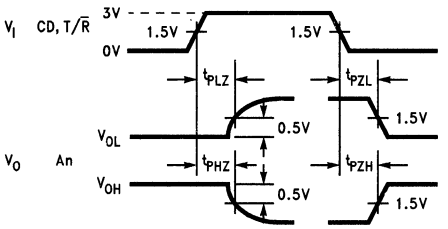
Switch Position

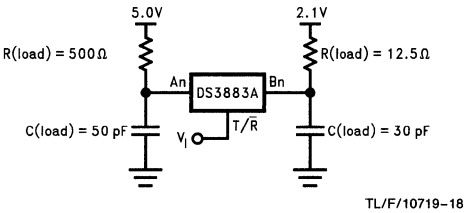
	t_{PZL} t_{PLZ}	t_{PZH} t_{PHZ}
S1	Close	Open
S2	Open	Close

FIGURE 6. Receiver Enable/Disable Set-Up



TL/F/10719–9

FIGURE 7. Receiver: CD to An, T/$\overline{R}$ to An (t_{PHZ} and t_{PZH} only)



TL/F/10719–18

FIGURE 8. T/$\overline{R}$ to An, T/$\overline{R}$ to Bn

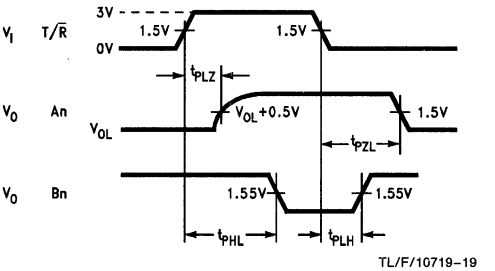


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FIGURE 9.
T/$\overline{R}$ to Bn (t_{PHL} and t_{PLH} only),
T/$\overline{R}$ to An (t_{PZL} and t_{PLZ} only)

National Semiconductor

PRELIMINARY

DS3884A
BTL Handshake Transceiver MIL-STD-883

General Description—(MIL Only)

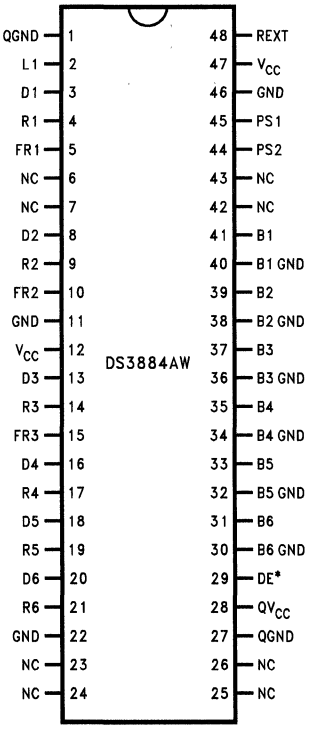
The DS3884A is pin to pin and functionally compatible with the DS3884. The DS3884A is a speed and power enhanced version of the DS3884. There are two minor differences between the DS3884 and DS3884A.

The external resistor used in the DS3884A is different from that used in the DS3884. REXT for the DS3884 is 6.2k while REXT for the DS3884A is 15 kΩ. The available filter settings for the DS3884A are 5 ns, 10 ns, 14 ns, 20 ns, while the settings for the DS3884 are 5 ns, 7.5 ns, 15 ns, and 25 ns.

Features

- Fast propagation delay
- 6-bit BTL transceiver
- Selective receiver glitch filtering (FR1–FR3)
- Meets 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80 mA
- TTL compatible driver and control inputs
- Separate TTL I/O
- Open collector bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- Built in Bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Individual Bus-port ground pins
- Product offered in glass sealed CERPAK

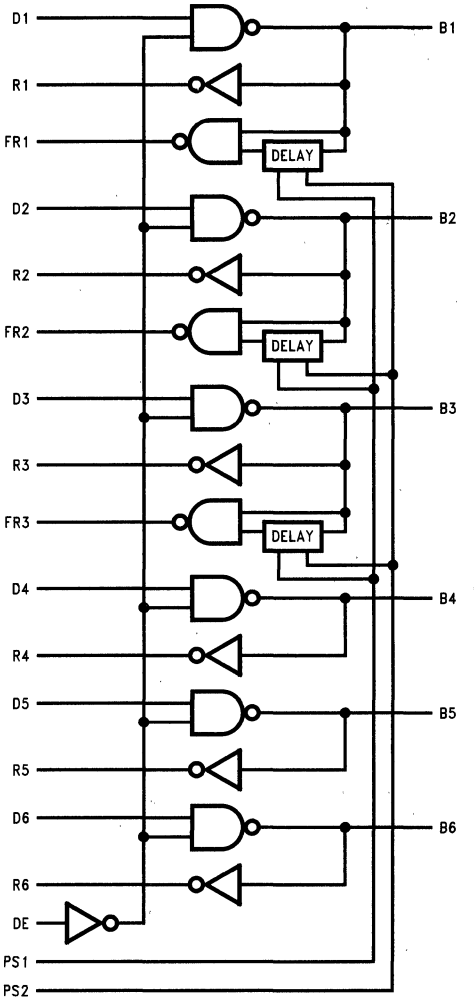
Connection Diagram



TL/F/11976–1

Order Number DS3884AW/883
See NS Package Number WA48A

Logic Diagram



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General Description (Continued)

The DS3884A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3884A is a BTL 6-bit Handshake Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL). Utilization of the DS3884A simplifies the implementation of all handshake signals which require Wired-OR glitch filtering. Three of the six bits have an additional parallel Wired-OR filtered receive output giving a total of nine receiver outputs.

In Wired-OR applications, the glitch generated as drivers are released from the bus, is dependent upon the backplane and parasitic wiring components causing the characteristics of the glitch to vary in pulse width and amplitude. To accommodate this variation the DS3884A features two pins defined as PS1 and PS2 which allow selection of a 5 ns, 10 ns, 14 ns and 24 ns filter setting to optimize glitch filtering for a given situation. The REXT pin is issued in conjunction with the filtering circuitry and requires a 15 kΩ resistor to ground. For additional information on Wired-OR glitch, reference Application Note AN-774.

The DS3884A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The combined output capacitance of the driver and receiver input is typically less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The device's unique driver circuitry meets a maximum slew rate of 0.5V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level.

Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. Output pins FR1–FR3 are the filtered outputs and R1–R6 are the unfiltered outputs. All receiver outputs are fully TTL compatible.

The DS3884A supports live insertion as defined for Futurebus+ through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V_{CC} pin. The DS3884A also provides power up/down glitch free protection during power sequencing.

The DS3884A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two V_{CC} pins on the DS3884A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage difference should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry. Additionally, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS3884A. They are the logic ground (GND), BTL grounds (B1GND–B6GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B1GND–B6GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exist on the DS3884A, it is important to note that any voltage difference between ground pins, QGND, GND or B1GND–B6GND should not exceed ±5V including power up/down sequencing.

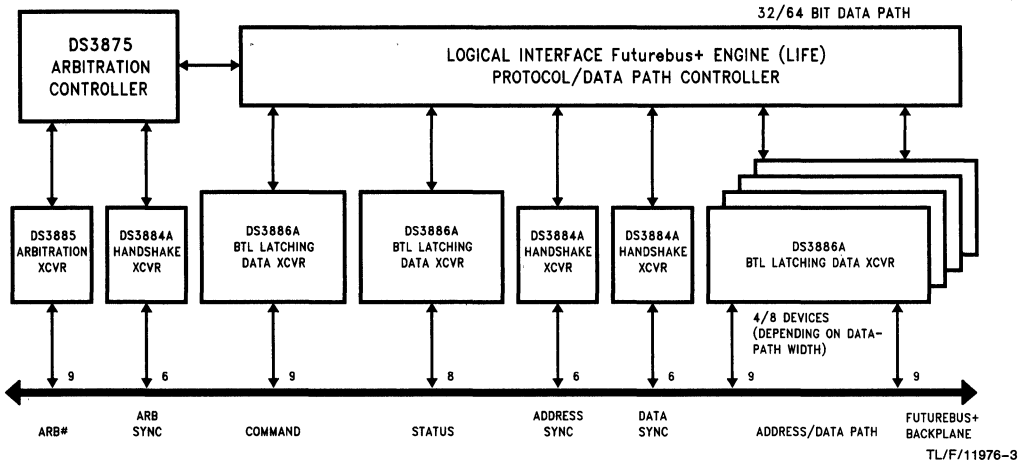
Additional transceivers included in the military Futurebus+ family are; the DS3885 BTL Arbitration Transceiver with arbitration competition logic for the AB<7:0>/$\overline{ABP}$ signal lines, and the DS3886A BTL 9-bit Latching Data Transceiver featuring edge triggered latches in the driver which may be bypassed during a fall-through mode and a transparent latch in the receiver.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

The Logical Interface Futurebus+ Engine (LIFE) is a high performance Futurebus+ Protocol Controller designed for IEEE 896.1-1991. The LIFE will handle all handshaking signals between the Futurebus+ and the local bus interface. The Protocol Controller supports the Futurebus+ compelled mode data transfer as both master and slave. The Protocol Controller can be configured to operate in compliance to IEEE 896.2 Profile B mode. The LIFE is 896.5 compatible. The LIFE incorporates a DMA controller and 64-bit FIFO's for fast queuing.

All of the transceivers are offered in 48-pin Cerpak high density package styles.

Typical Application



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Absolute Maximum Ratings (Note 1)

The 883 specifications are written to reflect the Reliability Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	±15 mA
Bus Termination Voltage	2.4V
Power Dissipation at 125°C	0.58W
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

Supply Voltage, V_{CC}	4.5V–5.5V
Bus Termination Voltage (V_T)	2.06V–2.14V
Operating Free Air Temperature	−55°C to +125°C

DC Electrical Characteristics (Notes 2 and 3) T_A = −55°C to +125°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (Dn, DE*, PS1 and PS2)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			100	µA
I_{IH}	Input High Current	$V_{IN} = 2.4V$			40	µA
I_{IL}	Input Low Current	$V_{IN} = 0.5V$			−100	µA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage (Note 5)	Dn = 2.4V, DE* = 0V, I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OLBZ}	Output Low Bus Current	Dn = 0.5V, DE* = 2.4V, Bn = 0.75V			100	µA
I_{OHBZ}	Output High Bus Current	Dn = 0.5V, DE* = 2.4V, Bn = 2.1V			100	µA
I_{OLB}	Output Low Bus Current	Dn = 0.5V, DE* = 0V, Bn = 0.75V			220	µA
I_{OHB}	Output High Bus Current	Dn = 0.5V, DE* = 0V, Bn = 2.1V			350	µA
V_{TH}	Receiver Input Threshold	DE* = 2.4V	1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, I_{Bn} = 1 mA	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, I_{Bn} = 10 mA	2.9	3.9	5.0	V
V_{CLN}	Negative Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V
RECEIVER OUTPUT: (FRn and Rn)						
V_{OH}	Voltage Output High	Bn = 1.1V, DE* = 2.4V, $I_{OH} = -2$ mA	2.4	3.2		V
V_{OL}	Voltage Output Low	Bn = 2.1V, DE* = 2.4V, I_{OL} = 24 mA		0.35	0.5	V
		Bn = 2.1V, DE* = 2.4V, I_{OL} = 8 mA		0.35	0.4	V
I_{OS}	Output Short Circuit Current	Bn = 1.1V, DE* = 2.4V (Note 4)	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CC}	Supply Current: Includes V_{CC}, QV_{CC} and LI	DE* = 0.5V, All Dn = 2.4V		50	90	mA
		DE* = 2.4V, All Bn = 2.1V		50	80	mA
I_{LI}	Live Insertion Current	DE* = 2.4V, All Dn = 0.5V		1	3	mA
		DE* = 0.5V, All Dn = 2.4V		2	5	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

DC Electrical Characteristics (Notes 2 and 3) $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Continued)

Note 2: All input and/or output pins shall not exceed V_{CC} plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power-down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. Alternatively, a current limiting resistor can be used when pulling-up the inputs to prevent damage. The current into any input/output pin shall be no greater than 50 mA. Exception, LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}. Furthermore, the difference between V_{CC} and QV_{CC} should never be greater than 0.5V at any time including power-up.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions.: $V_{CC} = 5V$ and $T_A = 25°C$ unless otherwise stated.

Note 4: Only one output should be shorted at a time, and duration of the short should not exceed one second.

Note 5: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

AC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Note 6)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	Dn to Bn	Prop. Delay	DE* = 0V *(Figures 1, 2)*	1		7	ns
t_{PLH}				1		6	ns
t_{PHL}	DE* to Bn	Enable Time	Dn = 3V *(Figures 1, 3)*	2	4	9	ns
t_{PLH}		Disable Time		2	4	7	ns
t_r	Transition Time—Rise/Fall 20% to 80%		*(Figures 1, 2)*	1	2	3.5	ns
t_f				1	2	4.5	ns
SR	Skew Rate is Calculated from 1.3V to 1.8V		(Note 11)			0.5	V/ns
t_{skew}	Skew between Drivers in the Same Package		(Note 7)		1	5	ns
RECEIVER							
t_{PHL}	Bn to Rn	Prop. Delay	DE* = 3V *(Figures 4, 5)*	2		6	ns
t_{PLH}				2		6	ns
t_{skew}	Skew between Receivers in Same Package		(Note 7)			3	ns
FILTERED RECEIVER							
t_{PHL}	Bn to FRn	Prop. Delay	PS1 = 0V PS2 = 0V DE* = 3V *(Figures 4, 5)*, $R_{EXT} = 15\ k\Omega$	6	13	17	ns
			PS1 = 0V PS2 = 3V DE* = 3V *(Figures 4, 5)*, $R_{EXT} = 15\ k\Omega$	11	16	23	ns
			PS1 = 3V PS2 = 0V DE* = 3V *(Figures 4, 5)*, $R_{EXT} = 15\ k\Omega$	16	21	29	ns
			PS1 = 3V PS2 = 3V DE* = 3V *(Figures 4, 5)*, $R_{EXT} = 15\ k\Omega$	22	33	49	ns
t_{PLH}	Bn to FRn	Prop. Delay	DE* = 3V *(Figures 4, 5)* (Note 8) $R_{EXT} = 15\ k\Omega$	2		8	ns
t_{GR}	Glitch Rejection		PS1 = 0V PS2 = 0V DE* = 3V *(Figures 4, 6)*, $R_{EXT} = 15\ k\Omega$	5		16	ns
			PS1 = 0V PS2 = 3V DE* = 3V *(Figures 4, 6)*, $R_{EXT} = 15\ k\Omega$	10		21	ns
			PS1 = 3V PS2 = 0V DE* = 3V *(Figures 4, 6)*, $R_{EXT} = 15\ k\Omega$	14		27	ns
			PS1 = 3V PS2 = 3V DE* = 3V *(Figures 4, 6)*, $R_{EXT} = 15\ k\Omega$	20		47	ns

AC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Note 6) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FILTERED RECEIVER TIMING REQUIREMENTS						
t_s	PSn to Bn Set-Up Time	(*Figure 7*), $R_{EXT} = 15\ k\Omega$	250			ns
PARAMETERS NOT TESTED						
Coutput	Capacitance at Bn	(Note 9)		5		pF
t_{NR}	Noise Rejection	(Note 10)		1		ns

Note 6: Input waveforms shall have a rise/fall time of 3 ns.

Note 7: t_{skew} is an absolute value defined as differences seen in propagation delays between drivers in the same package with identical load conditions.

Note 8: Filtered receiver t_{PLH} is independent of filter setting.

Note 9: The parameter is tested using TDR techniques described in P1194.0 BTL Backplane Design Guide.

Note 10: This parameter is tested during device characterization. The measurements revealed that the part will reject 1 ns pulse width.

Note 11: Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1V DC.

Pin Descriptions

Pin Name	Number of Pins	Input/ Output	Description
B1–B6	6	I/O	BTL receiver input and driver output
B1GND–B6GND	6	NA	Driver output ground reduces bounce due to high current switching of driver outputs (Note 12)
DE*	1	I	Driver Enable Low
D1–D6	6	I	TTL Driver Input
FR1–FR3	3	O	TTL Filtered Receiver Output
GND	3	NA	Ground reference for switching circuits. (Note 12)
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 13)
NC	8	NA	No Connect
PS1, PS2	2	I	Pulse Width Selection pin determines glitch filter setting (Note 14)
R1–R6	6	O	TTL Receiver Output
REXT	1	NA	External Resistor pin. External resistor is used for internal biasing of filter circuitry. The 15 kΩ resistor shall be connected between REXT and GND. The resistor shall have a tolerance of 1% and a temperature coefficient of 100 ppm/°C or better.
QGND	2	NA	Ground reference for receiver input bandgap reference and non-switching circuits (Note 12)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits (Note 13)
V_{CC}	2	NA	V_{CC} supply for switching circuits (Note 13)

Note 12: the multiplicity of grounds reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low inductance (i.e., ground plane with power pins and many signal pins connected to the backplane ground). If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

Note 13: The same considerations for ground are used for V_{CC} in reducing lead inductance (see Note 12). QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Note 14: See AC characteristics for filter setting.

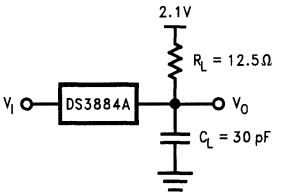
Truth Table

DE*	Dn	FRn	Rn	Bn
H	X	H	H	L
H	X	L	L	H
L	H	H	H	L
L	L	L	L	H

Note 1: X: High or low logic state
Note 2: L: Low state
Note 3: H: High state
Note 4: L-H: Low to high transition

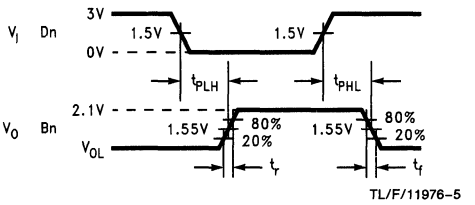
Glitch Filter Table

PS1	PS2	Filter Setting
L	L	5 ns
L	H	10 ns
H	L	14 ns
H	H	20 ns



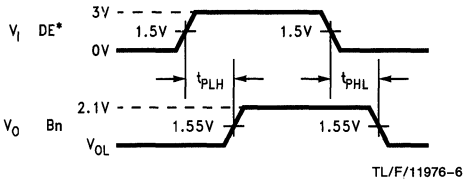
TL/F/11976–4

FIGURE 1. Driver Propagation Delay Set-Up



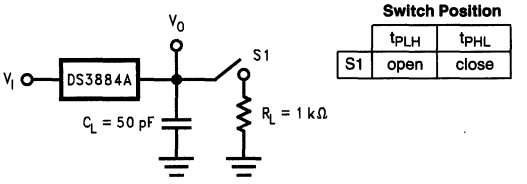
TL/F/11976–5

FIGURE 2. Driver: Dn to Bn



TL/F/11976–6

FIGURE 3. Driver: DE* to Bn

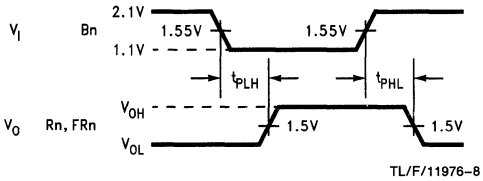


Switch Position

	t_{PLH}	t_{PHL}
S1	open	close

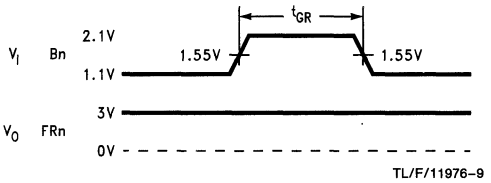
TL/F/11976–7

FIGURE 4. Receiver Propagation Delay Set-Up



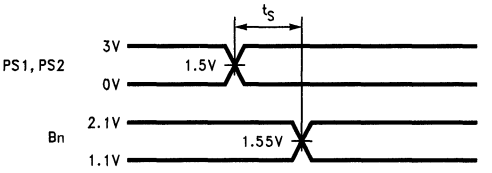
TL/F/11976–8

FIGURE 5. Receiver: Bn to FRn, Bn to Rn



TL/F/11976–9

FIGURE 6. Receiver: t_{GR}, FRn(min) = 2V



TL/F/11976–10

FIGURE 7. Receiver: PSn to Bn

National Semiconductor

DS3886A
BTL 9-Bit Latching Data Transceiver

General Description

The DS3886A is a higher speed, lower power, pin compatible version of the DS3886.

The DS3886A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3886A is a BTL 9-Bit Latching Data Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. The DS3886A incorporates an edge-triggered latch in the driver path which can be bypassed during fall-through mode of operation and a transparent latch in the receiver path. Utilization of the DS3886A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

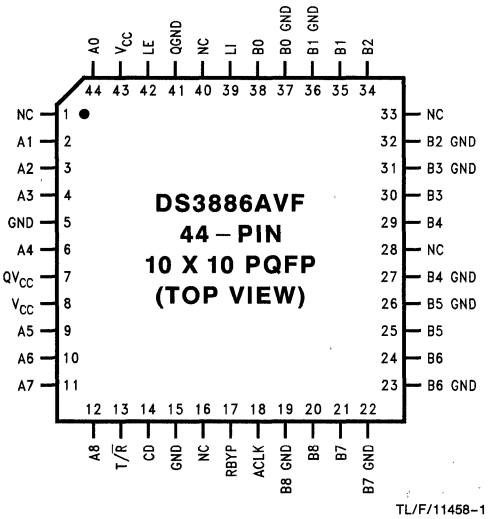
The DS3886A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with it's collector to isolate the transistor output capacitance from the bus, thus reducing the bus loading in the inactive state. The combined output capacitance of the driver output and receiver input is less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

(Continued)

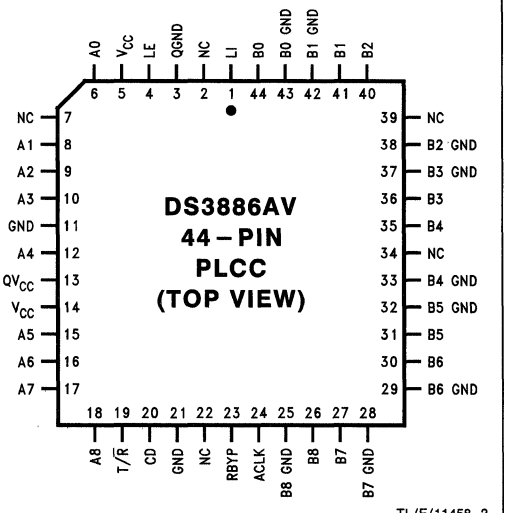
Features

- Fast propagation delay (3ns typ)
- 9-BIT BTL Latched Transceiver
- Driver incorporates edge triggered latches
- Receiver incorporates transparent latches
- Meets IEEE 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports Live Insertion
- Glitch free Power-up/down protection
- Typically less than 5 pF Bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80 mA
- Exceeds 2 KV ESD testing (Human Body Model)
- Open collector Bus-port outputs allows Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible Driver and Control inputs
- Built in Bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Individual Bus-port ground pins
- Product offered in PLCC and PQFP package styles
- 7 x 7 PQFP requires 50% less PCB space than 10 x 10 PQFP
- Tight skew (0.5 ns typical)

Connection Diagrams



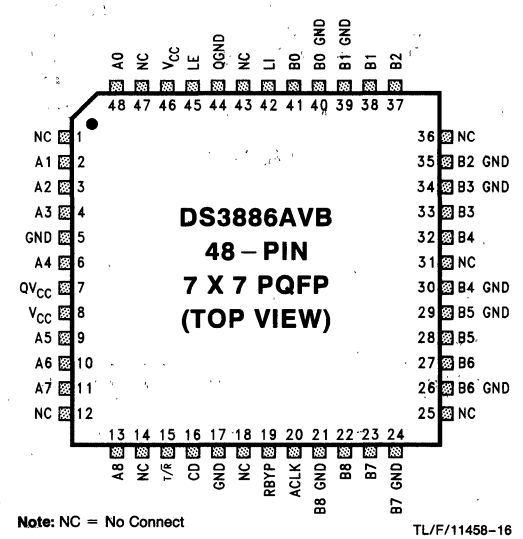
TL/F/11458–1



TL/F/11458–2

(Continued next page)

Connection Diagrams (Continued)



Note: NC = No Connect

TL/F/11458–16

Order Number DS3886AV, DS3886AVB or DS3886AVF
See NS Package Number V44A, VBH48A or VF44B

General Description (Continued)

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control, allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE and fully TTL compatible.

The DS3886A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the V_{CC} pin. The DS3886A also provides glitch free power up/down protection during power sequencing.

The DS3886A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two Logic V_{CC} pins on the DS3886A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn) the $T/\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} +0.5V.

There are three different types of ground pins on the DS3886A; the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3886A, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power up/down sequencing.

Additional transceivers included in the Futurebus+ family are; the DS3884A BTL Handshake Transceiver featuring selectable Wired-OR glitch filtering and the DS3885 BTL Arbitration Transceiver with arbitration competition logic for the AB<7:0>/ABP* signal lines, and the DS3883A BTL 9-Bit Data Transceiver.

The DS3875 Arbitration Controller included in the Futurebus+ family supports all the required and optional modes for Futurebus+ arbitration protocol. It is designed to be used in conjunction with the DS3884A and DS3885 transceivers.

The Logical Interface Futurebus+ Engine (LIFE) is a high performance Futurebus+ Protocol Controller designed for IEEE 896.1 - 1991. The LIFE will handle all handshaking signals between the Futurebus+ and the local bus interface. The Protocol Controller supports the Futurebus+ compelled mode data transfer as both master and slave. The Protocol Controller can be configured to operate in compliance to IEEE 896.2 Profile B mode. The LIFE incorporates a DMA controller and 64-bit FIFO's for fast queuing.

The DS3886A is offered in 44-pin PLCC, 44-pin PQFP, and 48-pin PQFP high density package styles.

The 48-pin PQFP is a 7 x 7 space saving package that requires 50% less PCB space than the 44-pin 10 x 10 PQFP package.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.5V
Control Input Voltage	6.5V
Driver Input and Receiver Output	5.5V
Receiver Input Current	±15 mA
Bus Termination Voltage	2.4V
Power Dissipation at 25°C	
PLCC (V44A)	2.5W
PQFP (VF44B)	1.3W
PQFP (VBH48A)	1.59W
Derate PLCC Package (V44A)	20 mW/°C
Derate PQFP Package (VF44B)	11.1 mW/°C
Derate PQFP Package (VBH48A)	12.8 mW/°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Bus Termination Voltage (V_T)	2.06	2.14	V
Operating Free Air Temperature	0	70	°C

DC Electrical Characteristics (Notes 2 and 3) T_A = 0° to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT (CD, T/$\overline{R}$, An, ACLK, LE and RBYP)						
V_{IH}	Minimum Input High Voltage		2.0			V
V_{IL}	Maximum Input Low Voltage				0.8	V
I_I	Input Leakage Current	$V_{IN} = V_{CC} = 5.5V$			250	μA
I_{IH}	Input High Current	$V_{IN} = 2.4V$, An = CD = 0.5V, T/$\overline{R}$ = 2.4V			40	μA
I_{IL}	Input Low Current	$V_{IN} = 0.5V$, An = CD = 0.5V, T/$\overline{R}$ = 2.4V			−10	μA
I_{IL}	Input Low Current	An Port, An = 0.5V, CD = 0.5V T/R = 2.4V, RBYp = 2.4V			−100	μA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT (Bn)						
V_{OLB}	Output Low Bus Voltage (Note 5)	An = T/$\overline{R}$ = 2.4V, CD = 0.5V, I_{OL} = 80 mA	0.75	1.0	1.1	V
I_{OFF}	Output Off Low Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 0.75V, CD = 0.5V			−200	μA
	Output Off High Current	An = 0.5V, T/$\overline{R}$ = 2.4V, Bn = 2.1V, CD = 0.5V			200	μA
	Output Off Low Current-Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 0.75V			−50	μA
	Output Off High Current-Chip Disabled	An = 0.5V, T/$\overline{R}$ = CD = 2.4V, Bn = 2.1V			50	μA
V_{TH}	Receiver Input Threshold	T/$\overline{R}$ = CD = 0.5V	1.47	1.55	1.62	V
V_{CLP}	Positive Clamp Voltage	V_{CC} = Max or 0V, Bn = 1 mA	2.4	3.4	4.5	V
		V_{CC} = Max or 0V, Bn = 10 mA	2.9	3.9	5.0	V
V_{CLN}	Negative Clamp Voltage	$I_{CLAMP} = -12$ mA			−1.2	V

DC Electrical Characteristics (Notes 2 and 3) $T_A = 0°$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER OUTPUT (An)						
V_{OH}	Voltage Output High	Bn = 1.1V, $I_{OH} = -2mA$, $T/\overline{R}$ = CD = 0.5V	2.4	3.2		V
V_{OL}	Voltage Output Low	$T/\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 24 mA		0.35	0.5	V
		$T/\overline{R}$ = CD = 0.5V, Bn = 2.1V, I_{OL} = 8 mA		0.30	0.4	V
I_{OZ}	TRI-STATE® Leakage Current	V_{IN} = 2.4V, CD = 2.4V, $T/\overline{R}$ = 0.5V, Bn = 0.75V			10	μA
		V_{IN} = 0.5V, CD = 2.4V, $T/\overline{R}$ = 0.5V, Bn = 0.75V			−10	μA
I_{OS}	Output Short Circuit Current	Bn = 1.1V, $T/\overline{R}$ = CD = 0.5V (Note 4)	−40	−70	−100	mA
SUPPLY CURRENT						
I_{CCT}	I_{CCT}—Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 2.1V$)	$T/\overline{R}$ = All An = 3.4V, CD = 0.5V ACLK = LE = RBYP = 3.4V		55	62	mA
	Supply Current: Sum of V_{CC}, QV_{CC} and LI	$T/\overline{R}$ = 0.5V, All Bn = 2.1V, LE = CD = 0.5V ACLK = RBYP = 3.4V		45	53	mA
I_{LI}	Live Insertion Current	$T/\overline{R}$ = An = CD = ACLK = 0.5V		1.5	2.2	mA
		$T/\overline{R}$ = All An = RBYB = 2.4V, CD = ACLK = 0.5V		3	4.5	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All input and/or output pins shall not exceed V_{CC} plus 0.5V and shall not exceed the absolute maximum rating at anytime, including power-up and power down. This prevents the ESD structure from being damaged due to excessive currents flowing from the input and/or output pins to QV_{CC} and V_{CC}. There is a diode between each input and/or output to V_{CC} which is forward biased when incorrect sequencing is applied. Alternatively, a current limiting resistor can be used when pulling-up the inputs to prevent damage. The current into any input/output pin shall be no greater than 50 mA. Exception, LI and Bn pins do not have power sequencing requirements with respect to V_{CC} and QV_{CC}. Furthermore, the difference between V_{CC} and QV_{CC} should never be greater than 0.5V at any time including power-up.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified. All typical values are specified under these conditions: V_{CC} = 5V and $T_A = 25°C$, unless otherwise stated.

Note 4: Only one output should be shorted at a time, and duration of the short should not exceed one second.

Note 5: Referenced to appropriate signal ground. Do not exceed maximum power dissipation of package.

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 6)

This AC table applies to DS3886AVF (10 x 10 PQFP) and DS3886AV (PLCC) only.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, $T/\overline{R}$ = RBYP = 3V (*Figures 1* and *2*)	1	3	5	ns
t_{PLH}	Fall-through mode			1.5	3	5	ns
t_{PHL}	ACLK to Bn	Propagation Delay	CD = RBYP = 0V, $T/\overline{R}$ = 3V (*Figures 1* and *4*)	1.7	4	6.5	ns
t_{PLH}	Latch mode			2	4	6.5	ns
t_{PHL}	CD to Bn	Enable Time	$T/\overline{R}$ = 3V, An = 3V (*Figures 1* and *3*)	3	5	9	ns
t_{PLH}		Disable Time		2.5	5	6.7	ns
t_{PHL}	$T/\overline{R}$ to Bn	Enable Time	CD = 0V (*Figures 10* and *11*), RBYP = 3V	9	13	18	ns
t_{PLH}		Disable Time	CD = 0V (*Figures 10* and *11*), RBYP = 3V	2	5	8	ns
t_r	Transition Time-Rise/Fall 20% to 80%		CD = RBYP = 0V, $T/\overline{R}$ = 3V (*Figures 1* and *3*) (Note 10)	1	2	3.5	ns
t_f				1	2	4	
SR	Slew Rate is calculated from 1.3V to 1.8V		CD = RBYP = 0V, $T/\overline{R}$ = 3V (*Figures 1* and *2*) (Note 10)		0.85	0.5	V/ns
t_{skew}	ACLK to Bn	Same Package	(Note 7)		0.8	3	ns
	An to Bn	Same Package	(Note 7)		0.8	3	ns

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 6) (Continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER TIMING REQUIREMENTS *(Figure 4)*							
t_S	An to ACLK	Set-up Time	CD = RBYP = 0V, T/$\overline{R}$ = 3V	3			ns
t_H	ACLK to An	Hold Time	CD = RBYP = 0V, T/$\overline{R}$ = 3V	1			ns
t_{pw}	ACLK Pulse Width		CD = RBYP = 0V, T/$\overline{R}$ = 3V	3			ns
RECEIVER							
t_{PHL}	Bn to An	Propagation Delay	CD = T/$\overline{R}$ = 0V, LE = 3V (*Figures 5* and *6*)	3	4.5	6	ns
t_{PLH}	Bypass Mode			3	4.5	6.5	ns
t_{PHL}	LE to An	Propagation Delay	CD = T/$\overline{R}$ = 0V (*Figures 5* and *7*)	3.5	5.5	10	ns
t_{PLH}	Latch Mode			4.5	5.5	8.5	ns
t_{PLZ}	CD to An	Disable Time	LE = 3.0V, Bn = 2.1V, T/$\overline{R}$ = 0V (*Figures 8* and *9*)	3	5	10	ns
t_{PZL}		Enable Time		2.5	6	8	ns
t_{PHZ}		Disable Time	LE = 3.0V, Bn = 1.1V, T/$\overline{R}$ = 0V (*Figures 8* and *9*)	4	6	8.5	ns
t_{PZH}		Enable Time		2.5	5	8.5	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	LE = 3.0V, Bn = 2.1V, CD = 0V (*Figures 10* and *11*)	3	7.5	12	ns
t_{PZL}		Enable Time		5	9.5	15	ns
t_{PHZ}		Disable Time	LE = 3.0V, Bn = 1.1V, CD = 0V (*Figures 8* and *9*)	3	6	9	ns
t_{PZH}		Enable Time		3	6	9	ns
t_{skew}	LE to An	Same Package	(Note 7)		0.5	3	ns
	Bn to An	Same Package	(Note 7)		0.5	2.5	ns
RECEIVER TIMING REQUIREMENTS *(Figure 7)*							
t_S	Bn to LE	Set-up Time	CD = T/$\overline{R}$ = 0V	3			ns
t_H	LE to Bn	Hold Time	CD = T/$\overline{R}$ = 0V	1			ns
t_{pw}	LE Pulse Width		CD = T/$\overline{R}$ = 0V	5			ns
PARAMETERS NOT TESTED							
C_{output}	Capacitance at Bn		(Note 8)		5		pF
t_{NR}	Noise Rejection		(Note 9)		1		ns

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Note 6)

This AC table applies to DS3886AVB (7 x 7 PQFP) only.

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER							
t_{PHL}	An to Bn	Propagation Delay	CD = 0V, T/$\overline{R}$ = RBYP = 3V (*Figures 1* and *2*)	1	2.2	5	ns
t_{PLH}	Fall-through mode			1	2.6	5	ns
t_{PHL}	ACLK to Bn	Propagation Delay	CD = RBYP = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *4*)	1.5	3	6.5	ns
t_{PLH}	Latch mode			2	4	6.5	ns
t_{PHL}	CD to Bn	Enable Time	T/$\overline{R}$ = 3V, An = 3V (*Figures 1* and *3*)	3	4.8	8.5	ns
t_{PLH}		Disable Time		2.5	4.3	6.5	ns
t_{PHL}	T/$\overline{R}$ to Bn	Enable Time	CD = 0V (*Figures 10* and *11*), RBYP = 3V	9	15.5	18	ns
t_{PLH}		Disable Time	CD = 0V (*Figures 10* and *11*), RBYP = 3V	2	5.7	8.5	ns
t_r	Transition Time-Rise/Fall 20% to 80%		CD = RBYP = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *3*) (Note 10)	1	1.7	3.5	ns
t_f				1	1.4	4	
SR	Slew Rate is calculated from 1.3V to 1.8V		CD = RBYP = 0V, T/$\overline{R}$ = 3V (*Figures 1* and *2*) (Note 10)		0.85	0.7	V/ns
t_{skew}	ACLK to Bn	Same Package	(Note 7)		0.8	3	ns
	An to Bn	Same Package	(Note 7)		0.8	3	ns

AC Electrical Characteristics T_A = 0°C to +70°C, V_{CC} = 5V ±10% (Note 6) (Continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
DRIVER TIMING REQUIREMENTS *(Figure 4)*							
t_S	An to ACLK	Set-up Time	CD = RBYP = 0V, T/$\overline{R}$ = 3V	3			ns
t_H	ACLK to An	Hold Time	CD = RBYP = 0V, T/$\overline{R}$ = 3V	1			ns
t_{pw}	ACLK Pulse Width		CD = RBYP = 0V, T/$\overline{R}$ = 3V	3			ns
RECEIVER							
t_{PHL}	Bn to An	Propagation Delay	CD = T/$\overline{R}$ = 0V, LE = 3V (*Figures 5* and *6*)	3	4.4	6	ns
t_{PLH}	Bypass Mode			3	4.9	6.5	ns
t_{PHL}	LE to An	Propagation Delay	CD = T/$\overline{R}$ = 0V (*Figures 5* and *7*)	3.5	6	8	ns
t_{PLH}	Latch Mode			3.5	5.5	7	ns
t_{PLZ}	CD to An	Disable Time	LE = 3.0V Bn = 2.1V, T/$\overline{R}$ = 0V (*Figures 8* and *9*)	3	5.7	10	ns
t_{PZL}		Enable Time		2.5	6.8	8	ns
t_{PHZ}		Disable Time	LE = 3.0V Bn = 1.1V, T/$\overline{R}$ = 0V (*Figures 8* and *9*)	4	6.5	9	ns
t_{PZH}		Enable Time		2.5	5	8.5	ns
t_{PLZ}	T/$\overline{R}$ to An	Disable Time	LE = 3.0V, Bn = 2.1V CD = 0V (*Figures 10* and *11*)	3	6.6	12	ns
t_{PZL}		Enable Time		4.5	8.2	15	ns
t_{PHZ}		Disable Time	LE = 3.0V Bn = 1.1V, CD = 0V (*Figures 8* and *9*)	3	6.2	9	ns
t_{PZH}		Enable Time		3	5.3	9	ns
t_{skew}	LE to An	Same Package	(Note 7)		0.5	3	ns
	Bn to An	Same Package	(Note 7)		0.5	2.5	ns
RECEIVER TIMING REQUIREMENTS *(Figure 7)*							
t_S	Bn to LE	Set-up Time	CD = T/$\overline{R}$ = 0V	3			ns
t_H	LE to Bn	Hold Time	CD = T/$\overline{R}$ = 0V	1			ns
t_{pw}	LE Pulse Width		CD = T/$\overline{R}$ = 0V	5			ns
PARAMETERS NOT TESTED							
C_{output}	Capacitance at Bn		(Note 8)		5		pF
t_{NR}	Noise Rejection		(Note 9)		1		ns

Note 6: Input waveforms shall have a rise and fall time of 3 ns.

Note 7: t_{skew} is an absolute value defined as differences seen in propagation delay between drivers in the same package with identical load conditions.

Note 8: The parameter is tested using TDR techniques described in P1194.0 BTL Backplane Design Guide.

Note 9: This parameter is tested during device characterization. The measurements revealed that the part will typically reject 1 ns pulse width.

Note 10: Futurebus+ transceivers are required to limit bus signal rise and fall times to no faster than 0.5 V/ns, measured between 1.3V and 1.8V (approximately 20% to 80% of nominal voltage swing). The rise and fall times are measured with a transceiver loading equivalent to 12.5Ω tied to +2.1 V_{DC}.

Pin Description

Pin Name	Number of Pins	Input/ Output	Description
A0–A8	9	I/O	TTL TRI-STATE receiver output and driver input
ACLK	1	I	Clock input for latch
B0–B8	9	I/O	BTL receiver input and driver output
B0GND–B8GND	9	NA	Driver output ground reduces ground bounce due to high current switching of driver outputs. (Note 11)
CD	1	I	Chip Disable
GND	2	NA	Ground reference for switching circuits. (Note 11)
LE	1	I	Latch Enable
LI	1	NA	Power supply for live insertion. Boards that require live insertion should connect LI to the live insertion pin on the connector. (Note 12)
NC	5	NA	No Connect
QGND	1	NA	Ground reference for receiver input bandgap reference and non-switching circuits. (Note 11)
QV_{CC}	1	NA	V_{CC} supply for bandgap reference and non-switching circuits. (Note 12)
RBYP	1	I	Register bypass enable
T/$\overline{R}$	1	I	Transmit/$\overline{\text{Receive}}$ — Transmit (An to Bn) Receive (Bn to An)
V_{CC}	2	NA	V_{CC} supply for switching circuits. (Note 12)

Note 11: The multiplicity of grounds reduces the effective inductance of bonding wires and leads, which then reduces the noise caused by transients on the ground path. The various ground pins can be tied together provided that the external ground has low iductance (i.e., ground plane with power pins and many signal pins connected to the backplane ground). If the external ground floats considerably during transients, precautionary steps should be taken to prevent QGND from moving with reference to the backplane ground. The receiver threshold should have the same ground reference as the signal coming from the backplane. A voltage offset between their grounds will degrade the noise margin.

Note 12: The same considerations for ground are used for V_{CC} in reducing lead inductance (see Note 11). QV_{CC} and V_{CC} should be tied together externally. If live insertion is not supported, the LI pin can be tied together with QV_{CC} and V_{CC}.

Truth Table

CD	T/$\overline{R}$	LE	RBYP	ACK	An	Bn
H	X	X	X	X	Z	H
L	H	X	H	X	L	H
L	H	X	H	X	H	L
L	H	X	L	X	X	Bn_0
L	H	X	L	L-H	H	L
L	H	X	L	L-H	L	H
L	L	H	X	X	H	L
L	L	H	X	X	L	H
L	L	L	X	X	An_0	X

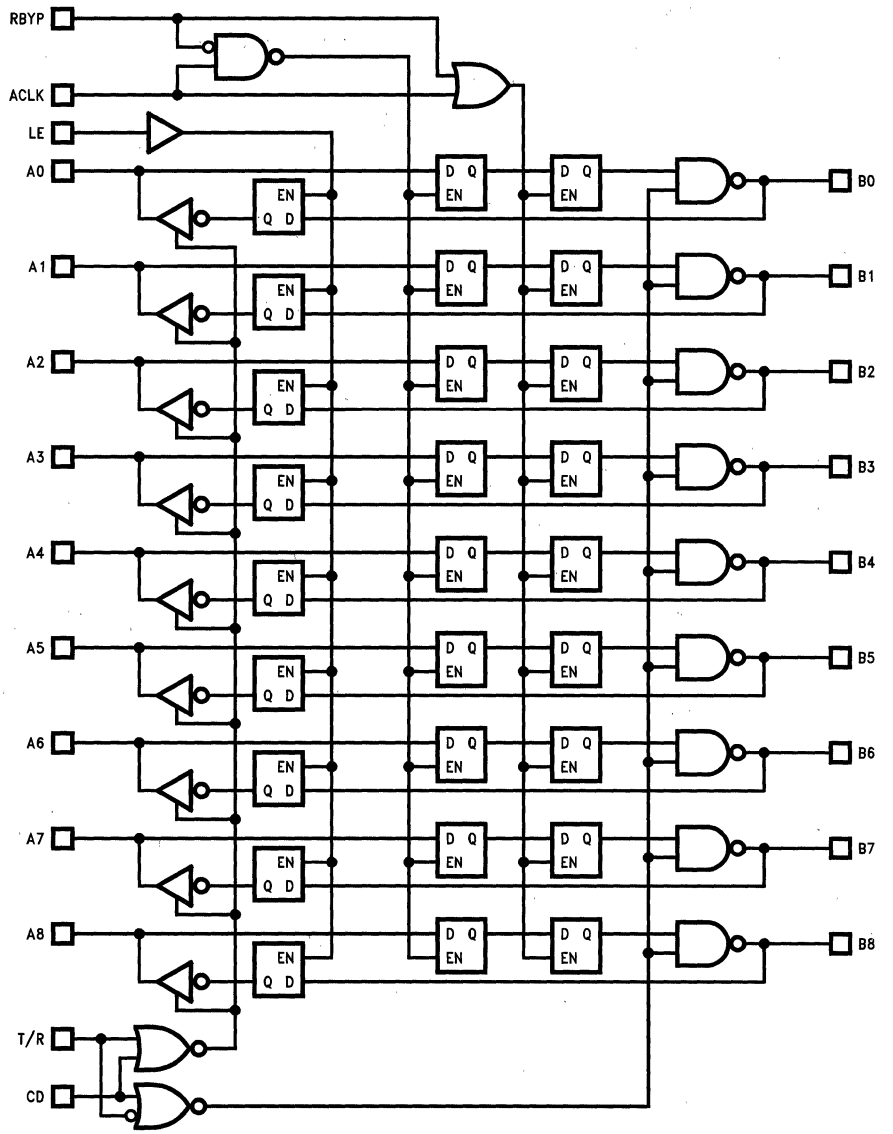
X = High or low logic state
Z = High impedance state
L = Low state
H = High state
L-H = Low to high transition
An_0 = no change from previous state
Bn_0 = no change from previous state
BTL = high and low state are nominally 2.1V and 1.0V, respectively.
TTL = high and low state are nominally 2.4V and 0.5V, respectively.

Package Thermal Characteristics

Linear Feet per Minute Air Flow (LFPM)	θ_{JA} (°C/W)		
	44-Pin PQFP	44-Pin PLCC	48-Pin PQFP
0	82	45	76
225	68	35	60
500	60	30	54
900	53	26	48

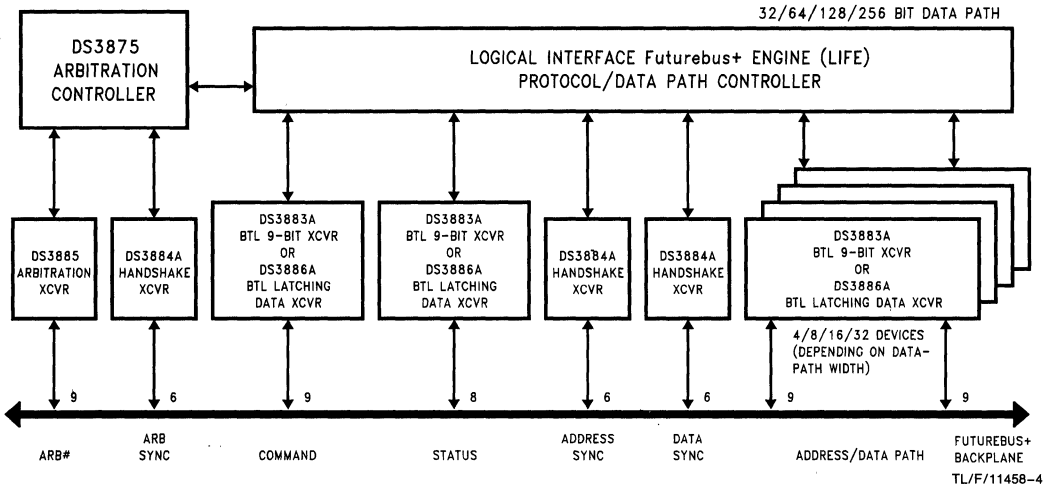
Note: The above values are typical values and are different from the Absolute Maximum Rating values, which include guardbands.

Logic Diagram



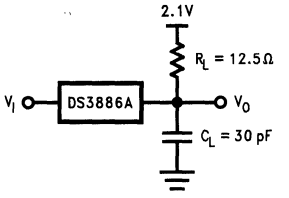
TL/F/11458–3

Typical Application



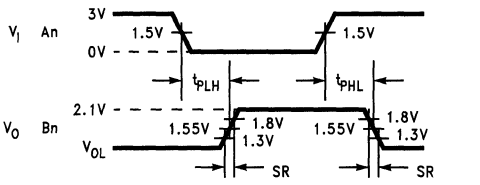
TL/F/11458–4

Test Circuits and Timing Waveforms



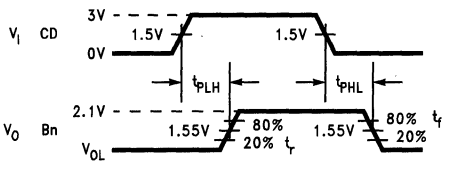
TL/F/11458–5

FIGURE 1. Driver Propagation Delay Set-up



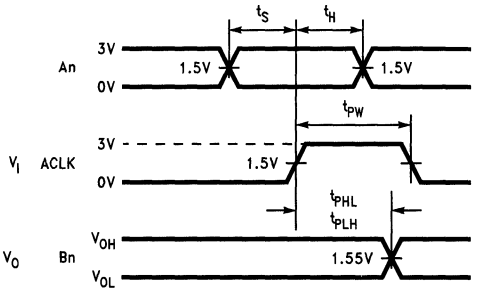
TL/F/11458–6

FIGURE 2. Driver: An to Bn, CD to An



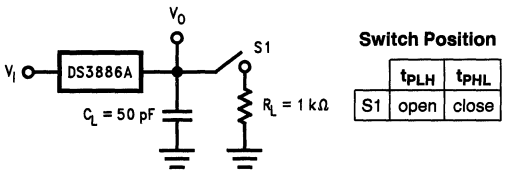
TL/F/11458–7

FIGURE 3. Driver: CD to Bn



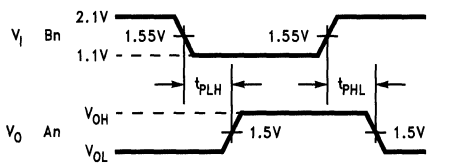
TL/F/11458–8

FIGURE 4. Driver: ACLK to Bn, t_S, t_H, t_{PW}



TL/F/11458–9

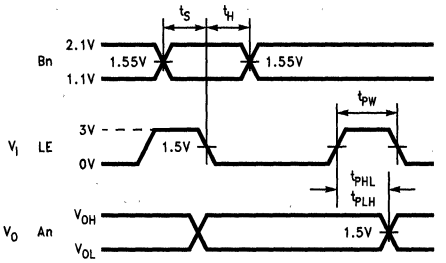
FIGURE 5. Receiver Propagation Delay Set-up



TL/F/11458–10

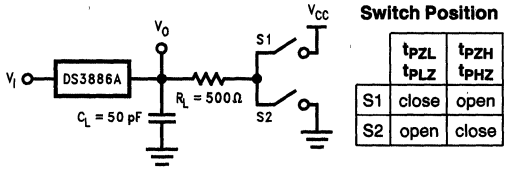
FIGURE 6. Receiver: Bn to An

Test Circuits and Timing Waveforms (Continued)



TL/F/11458–11

FIGURE 7. Receiver Enable/Disable Set-up



Switch Position

	t_{PZL} t_{PLZ}	t_{PZH} t_{PHZ}
S1	close	open
S2	open	close

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FIGURE 8. Receiver: Enable/Disable Set-up

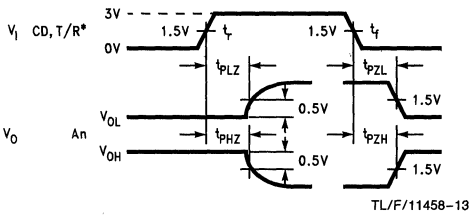

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FIGURE 9. Receiver: CD to An, T/$\overline{R}$ to An (t_{PHZ} and t_{PZH} only)

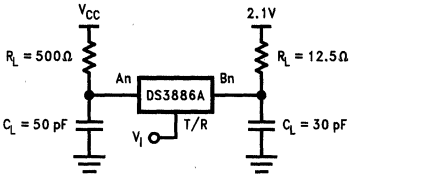

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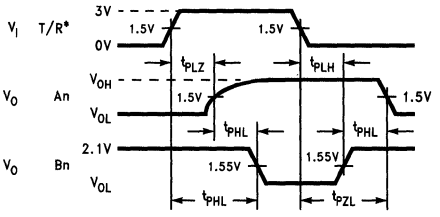
FIGURE 10. T/$\overline{R}$ to An, T/$\overline{R}$ to Bn



TL/F/11458–15

FIGURE 11. T/$\overline{R}$ to Bn (t_{PHL} and t_{PLH} only), T/$\overline{R}$ to An (t_{PZL} and t_{PLZ} only)

National Semiconductor

ADVANCE INFORMATION

DS38C86A CMOS BTL 9-Bit Edge Latched/Registered Data Transceiver

General Description

The DS38C86A is one in a series of transceivers designed specifically for the proprietary bus interfaces implemented in CMOS technology, these transceivers deliver all of the performance of their Bi-CMOS counterparts with less then half of the power supply current. The DS38C86A is a CBTL 9-Bit Latching Data Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL). The DS38C86A allows data transmission from A(port) TTL to B(port) BTL or from B(port) BTL to A(port) TTL depending on the logic level of T/$\overline{R}$ pin. Buffer, register and D-type latch configurations are available for the drive direction, while Buffer and D-type latch configurations are available for the receive direction.

The DS38C86A driver output configuration is an open drain which allows Wired-OR connection on the bus. A unique design reduces the bus loading to typically 3 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

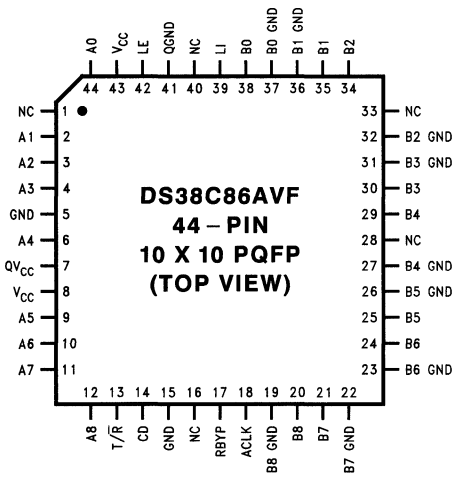
Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum

(Continued)

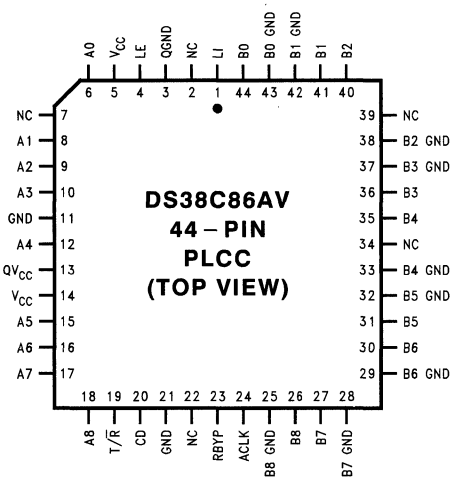
Features

- >50% less I_{CC} than BiCMOS DS3886A
- Fast propagation delay
- 9-Bit inverting BTL latched transceiver
- Driver incorporates edge triggered latches
- Receiver incorporates transparent latches
- Meets IEEE 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically 3 pF bus-port capacitance
- Low Bn bus-port voltage swing (typically 1V) at 80 mA
- Exceeds 2 kV ESD testing (Human Body Model)
- Open drain bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible driver and control inputs
- Built in bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Individual bus-port ground pins
- Product offered in PQFP 7 x 7, PQFP 10 x 10 and PLCC package style
- The 7 x 7 PQFP requires 50% less PCB space than 10 x 10
- Tight skew

Connection Diagrams



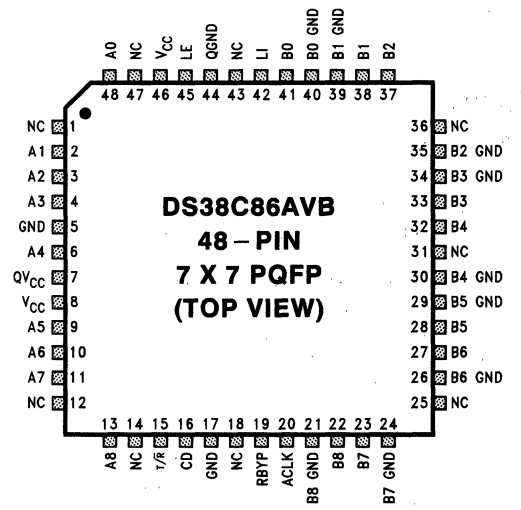
TL/F/12623–1



TL/F/12623–2

This datasheet contains the design specification for product development. Specifications may change in any manner without notice.

Connection Diagrams (Continued)



TL/F/12623–3

Order Number DS38C86AV, DS38C86AVB or DS38C86AVF
See NS Package Number V44A, VBH48A or VF44B

General Description (Continued)

noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control, allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The DS38C86A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the V_{CC} pin. The DS38C86A also provides glitch free power-up/down protection during power sequencing.

The DS38C86A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are three Logic V_{CC} pins on the DS38C86A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn) the $T/\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS38C86A; the logic ground (GND), BTL grounds (B0GND–B7GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B7GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS38C86A, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B7GND should not exceed ±0.5V including power-up/down sequencing.

National Semiconductor

DS3890 BTL Octal Trapezoidal Driver
DS3892 BTL Octal TRI-STATE® Receiver

General Description

The DS3890 and DS3898 are designed specifically to overcome problems associated with driving densely populated backplanes. These products provide significant improvement in both speed and data integrity in comparison to conventional bus drivers and receivers. Their low output capacitance, low voltage swing and noise immunity features make them ideal for driving low impedance busses with minimum power dissipation.

The DS3890 features an open collector outputs that generate precise trapezoidal waveforms with typical rise and fall times of 6 ns which are relatively independent of capacitive loading conditions. These controlled output characteristics significantly reduce noise coupling to adjacent lines.

To minimize bus loading, the DS3890 also features a schottky diode in series with the open collector outputs that isolates the driver output capacitance in the disabled state. With this type of configuration the output low voltage is typically "1V". The output high level is intended to be 2 volts. This is achieved by terminating the bus with a pull up resistor. Both devices can drive an equivalent DC load of 18.5Ω (or greater) in the defined configuration.

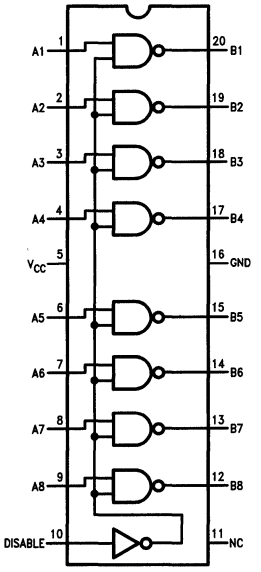
(General Description to be continued)

Features

- Driver output capacitance less than 5 pF
- 1 volt bus signal reduces power consumption
- Trapezoidal driver waveforms (t_r, t_f, typically 6 ns) reduces noise coupling to adjacent lines
- Precise receiver threshold track the bus logic high level to maximize noise immunity in both logic high ahd low states
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection
- TTL compatible driver and control inputs and receiver output
- BTL compatible

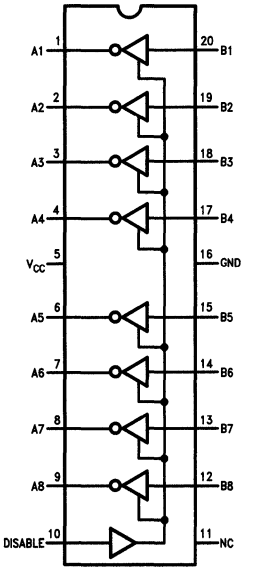
Logic and Connection Diagrams

DS3890 Octal Trapezoidal Driver



TL/F/8700–1

DS3892 Octal TRI-STATE Receiver



TL/F/8700–2

Order Numbers DS3892M, DS3890N or DS3892N
See NS Package Number M20B or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Temperature (T_A)	0	70	°C

DS3890 Electrical Characteristics (Notes 2 and 3)

DRIVER AND CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL} An	V_{CC}=Max V_{IN}=0.4V		−1	−1.6	mA
I_{IL} Dis	V_{CC}=Max V_{IN}=0.4V		−180	−400	μA
I_{IH}	V_{CC}=Max V_{IN}=2.4V			40	μA
I_I	V_{CC}=Max V_{IN}=5.25V			1	mA
V_{CL}	V_{CC}=Min I_{IN}=−12 mA		−0.9	−1.5	V

DRIVER OUTPUT

V_{OL}	V_{CC}=Min R_L=18.5Ω	0.75	1.0	1.2	V
I_{OH}	V_{CC}=Max V_{OUT}=2V	−20	10	100	μA
I_O	V_{CC}=0V V_{OUT}=2V			100	μA
I_{IL}	V_{CC}=Max V_{OUT}=0.75V		−100	−250	μA
I_{CC} Low	V_{CC}=Max		50	80	mA
I_{CC} High				100	mA

DS3892 Electrical Characteristics (Notes 2 and 3)

CONTROL INPUTS

Symbol	Conditions	Min	Typ	Max	Units
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IL}	V_{CC}=Max V_{IN}=0.4V		−180	−400	μA
I_{IH}	V_{CC}=Max V_{IN}=2.4V			40	μA
I_I	V_{CC}=Max V_{IN}=5.25V			1	mA
V_{CL}	V_{CC}=Min I_{IN}=−12 mA		−0.9	−1.5	V

RECEIVER

V_{OL}	V_{CC}=Min I_{OL}=16 mA		0.35	0.5	V
V_{OH}	V_{CC}=Min I_{OH}=−400 μA	2.4	3.2		V
I_{OS}	V_{CC}=Max V_{OUT}=0V	−20	−70	−100	mA
V_{TH} Rec	V_{CC}=5V	1.47	1.55	1.62	V
I_{IH} Rec	V_{CC}=Max V_{IN}=2V		10	100	μA
I_I Rec	V_{CC}=0V V_{IN}=2V			100	μA
I_{IL} Rec	V_{CC}=Max V_{IN}=0.75V			100	μA
I_{CC} Low	V_{CC}=Max			80	mA
I_{CC} High				60	mA

DS3890 Switching Characteristics *(Figure 1)*

$0°C \leq T_A \leq 70°C$, $4.75V \leq V_{CC} \leq 5.25V$ unless otherwise specified

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	An to Bn		9	15	ns
T_{dHL}			9	15	ns
T_{dLH}	Dis to Bn		10	18	ns
T_{dHL}			12	20	ns
T_r & T_f	Bn rise and fall time	3	6	10	ns

DS3892 Switching Characteristics *(Figures 2, 3 and 4)*

Symbol	Conditions	Min	Typ	Max	Units
T_{dLH}	Bn to An		12	18	ns
T_{pHL}			10	18	ns
T_{dLZ}	Dis to An		10	18	ns
T_{dZL}			8	15	ns
T_{dHZ}			4	8	ns
T_{dZH}			7	12	ns
TNR	Receiver noise rejection	3	6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The Table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive values; all currents out of the device are shown as negative; all voltages are referenced to ground unless otherwise specified. All values shown as max or min are classified on absolute value basis and apply to the full operating temperature and V_{CC} range.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

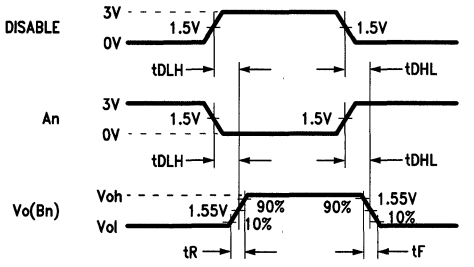
General Descriptions (Continued)

The DS3892 receiver inputs incorporate a low pass filter in conjunction with high speed comparator to further enhance the noise immunity. Both devices provide equal rejection to both positive and negative noise pulses (typically 6 ns) on the bus.

The DS3890 features TTL compatible inputs while the DS3892 inputs are BTL compatible. The control inputs on all devices are TTL compatible.

BTL "Backplane Transceiver Logic" is a new logic signaling method developed by IEEE P896 Future Bus Standards Committee. This standard was adopted to enhance the performance of Backplane Busses. BTL compatible bus interface circuits feature low capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard overcomes some of the fundamental limitations of TTL bus transceivers in heavily loaded backplane bus applications. Devices designed to this standard provide significant improvements in switching speed and data integrity.

AC Switching Waveforms



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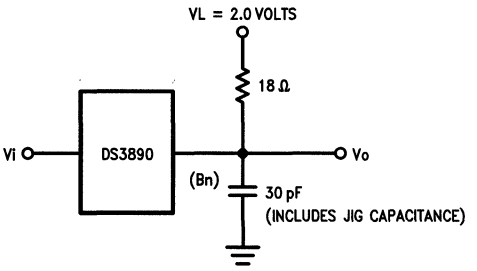
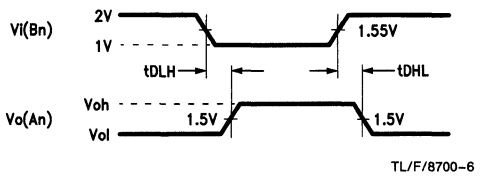


Note: $t_R = t_F < 10$ ns from 10% to 90%

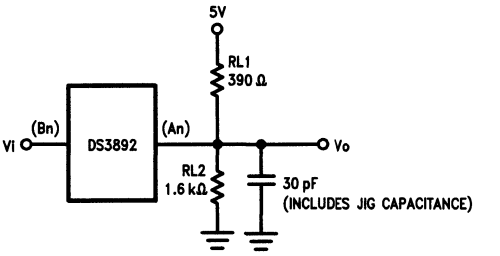
TL/F/8700–5

FIGURE 1
Driver Propagation Delays

AC Switching Waveforms (Continued)



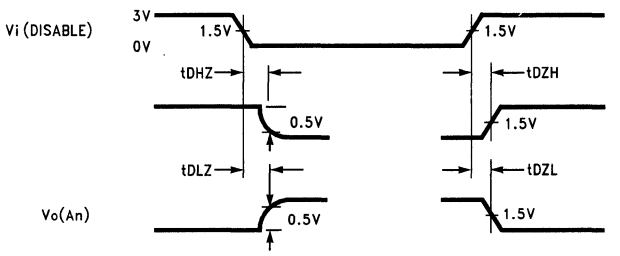
TL/F/8700–6



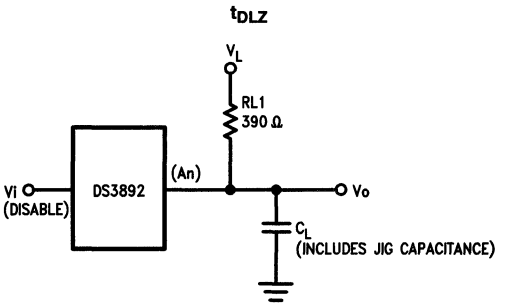
Note: $t_R = t_F < 10$ ns from 10% to 90%

TL/F/8700–7

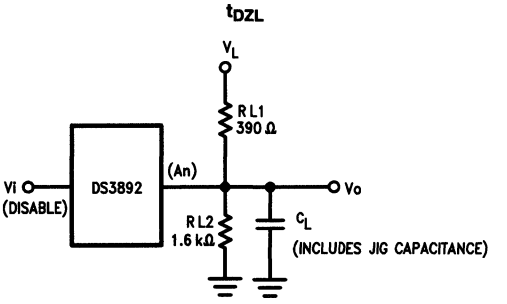
FIGURE 2. Receiver Propagation Delays



TL/F/8700–8

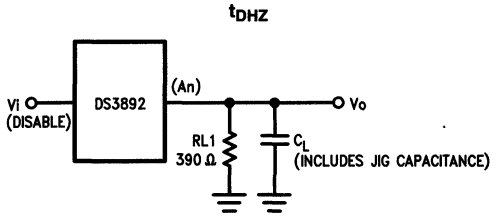


TL/F/8700–14



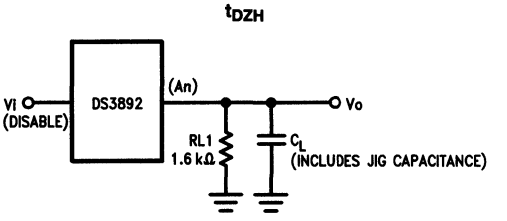
Note: $t_R = t_F < 5$ ns from 10% to 90%

TL/F/8700–9



Note: $t_R = t_F < 5$ ns from 10% to 90%

TL/F/8700–15

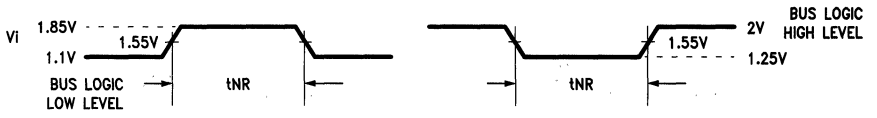


TL/F/8700–16

FIGURE 3. Propagation Delay from Disable Pin to An

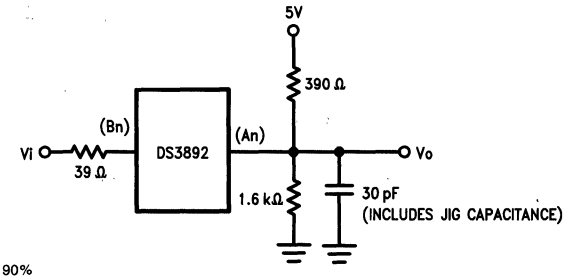
10

AC Switching Waveforms (Continued)



TL/F/8700–10

High **Low**



Note: $t_R = t_F < 2$ ns from 10% to 90%

TL/F/8700–11

FIGURE 4

Receiver Noise Immunity:
"No Response at Output" Input Waveforms

National Semiconductor

DS3893A BTL TURBOTRANSCEIVER™

General Description

The TURBOTRANSCEIVER is designed for use in very high speed bus systems. The bus terminal characteristics of the TURBOTRANSCEIVER are referred to as "Backplane Transceiver Logic" (BTL). BTL is a new logic signaling standard that has been developed to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard eliminates the settling time delays, that severely limit the TTL bus performance, to provide significantly higher bus transfer rates.

The TURBOTRANSCEIVER is compatible with the requirements of the proposed IEEE 896 Futurebus draft standard. It is similar to the DS3896/97 BTL TRAPEZOIDAL Transceivers but the trapezoidal feature has been removed to improve the propagation delay. A stripline backplane is therefore required to reduce the crosstalk induced by the faster rise and fall times. This device can drive a 10Ω load with a typical propagation delay of 3.5 ns for the driver and 5 ns for the receiver.

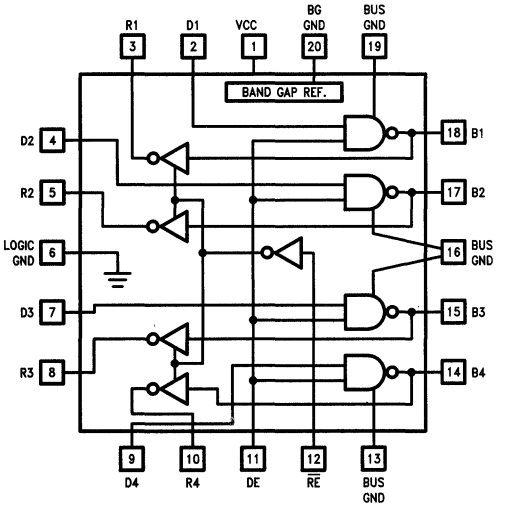
When multiple devices are used to drive a parallel bus, the driver enables can be tied together and used as a common control line to get on and off the bus. The driver enable delay is designed to be the same as the driver propagation delay in order to provide maximum speed in this configuration. The low input current on the enable pin eases the drive required for the common control line.

The bus driver is an open collector NPN with a Schottky diode in series to isolate the transistor output capacitance from the bus when the driver is in the inactive state. The active output low voltage is typically 1V. The bus is intended to be operated with termination resistors (selected to match the bus impedance) to 2.1V at both ends. Each of the resistors can be as low as 20Ω.

Features

- Fast single ended transceiver (typical driver enable and receiver propagation delays are 3.5 ns and 5 ns)
- Backplane Transceiver Logic (BTL) levels (1V logic swing)
- Less than 5 pF bus-port capacitance
- Drives densely loaded backplanes with equivalent load impedances down to 10Ω
- 4 transceivers in 20 pin PCC package
- Specially designed for stripline backplanes
- Separate bus ground returns for each driver to minimize ground noise
- High impedance, MOS and TTL compatible inputs
- TRI-STATE® control for receiver outputs
- Built-in bandgap reference provides accurate receiver threshold
- Glitch free power up/down protection on all outputs
- Oxide isolated bipolar technology

Connection and Logic Diagram



TL/F/8698–1

Order Number DS3893AV
See NS Package Number V20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.5V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Driver Output Receiver Input Clamp Current	±15 mA
Power Dissipation at 70°C	900 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 3 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.5	5.5	V
Bus Termination Voltage (V_T)	2.0	2.2	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics (Notes 2, 3 and 4) T_A = 0 to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND CONTROL INPUT: (DE, $\overline{RE}$, Dn)						
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_I	Input Leakage Current	DE = $\overline{RE}$ = Dn = V_{CC}			100	µA
I_{IH}	Input High Current	DE = $\overline{RE}$ = Dn = 2.5V			20	µA
I_{IL}	Dn Input Low Current	Dn = 0.5V, DE = V_{CC} = Max			−200	µA
	DE Input Low Current	DE = 0.5V, Dn = V_{CC} = Max			−500	µA
	$\overline{RE}$ Input Low Current	$\overline{RE}$ = 0.5V, V_{CC} = Max			−100	µA
V_{CL}	Input Diode Clamp Voltage	I_{clamp} = −12 mA			−1.2	V
DRIVER OUTPUT/RECEIVER INPUT: (Bn)						
V_{OLB}	Output Low Bus Voltage	Dn = DE = V_{IH} *(Figure 2)* R_T = 10Ω, V_T = 2.2V	0.75	1.0	1.2	V
		Dn = DE = V_{IH} *(Figure 2)* R_T = 18.5Ω, V_T = 2.14	0.75	1.0	1.1	V
I_{ILB}	Output Bus Current (Power On)	Dn = DE = 0.8V, V_{CC} = Max Bn = 0.75V	−250		100	µA
I_{IHB}	Output Bus Current (Power Off)	Dn = DE = 0.8V, V_{CC} = 0V Bn = 1.2V			100	µA
V_{OCB}	Driver Output Positive Clamp	V_{CC} = Max or 0V, Bn = 1 mA			2.9	V
		V_{CC} = Max or 0V, Bn = 10 mA			3.2	V
V_{OHB}	Output High Bus Voltage	V_{CC} = Max, Dn = 0.8V *(Figure 2)* V_T = 2.0V, R_T = 10Ω	1.90			V
V_{TH}	Receiver Input Threshold		1.47	1.55	1.62	V
RECEIVER OUTPUT: (Rn)						
V_{OH}	Voltage Output High	Bn = 1.2V, I_{oh} = −3 mA, $\overline{RE}$ = 0.8V	2.5V			V
V_{OL}	Voltage Output Low	Bn = 2V, I_{ol} = 6 mA, $\overline{RE}$ = 0.8V		0.35	0.5	V
I_{OZ}	TRI-STATE Leakage	V_o = 2.5V, $\overline{RE}$ = 2V			20	µA
		V_o = 0.5V, $\overline{RE}$ = 2V			−20	µA
I_{OS}	Output Short Circuit Current (Note 5)	Bn = 1.2V, V_o = 0V $\overline{RE}$ = 0.8V, V_{CC} = Max	−80	−120	−200	mA
I_{CC}	Supply Current	Dn = DE = $\overline{RE}$ = V_{IH}, V_{CC} = Max		70	95	mA

Note 1: "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

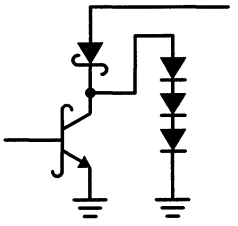
Note 4: Unused inputs should not be left floating. Tie unused inputs to either V_{CC} or GND thru a resistor.

Note 5: Only one output at a time should be shorted.

Switching Characteristics T_A = 0 to +70°C, V_{CC} = 5V ±10%

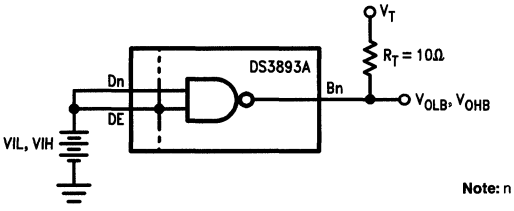
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER: (*Figures 3* and *6*)						
t_{PHL}	Driver Input to Output	V_T = 2V R_T = 10Ω, C_L = 30 pF, DE = 3V	1	3.5	7	ns
t_{PLH}	Driver Input to Output	V_T = 2V, R_T = 10Ω, C_L = 30 pF, DE = 3V	1	3.5	7	ns
t_r	Output Rise time	V_T = 2V, R_T = 10Ω, C_L = 30 pF, DE = 3V	1	2	5	ns
t_f	Output Fall Time	V_T = 2V, R_T = 10Ω, C_L = 30 pF, DE = 3V	1	2	5	ns
t_{skew}	Skew Between Drivers in Same Package	(Note 1)		1		ns
DRIVER ENABLE: (*Figures 3* and *6*)						
t_{PHL}	Enable Delay	V_T = 2V, R_T = 10Ω, C_L = 30 pF, Dn = 3V	1	3.5	7	ns
t_{PLH}	Disable Delay	V_T = 2V, R_T = 10Ω, C_L = 30 pF, Dn = 3V	1	3.5	7	ns
RECEIVER: (*Figures 4* and *7*)						
t_{PHL}	Receiver Input to Output	C_L = 50 pF, $\overline{RE}$ = DE = 0.3V, S3 Closed	2	5	8	ns
t_{PLH}	Receiver Input to Output	C_L = 50 pF, $\overline{RE}$ = DE = 0.3V, S3 Open	2	5	8	ns
t_{skew}	Skew Between Receivers in Same Package	(Note 1)		1		ns
RECEIVER ENABLE: (*Figures 5* and *8*)						
t_{ZL}	Receiver Enable to Output Low	C_L = 50 pF, R_L = 500, DE = 0.3V S2 Open Bn = 2V	2	6	12	ns
t_{ZH}	Receiver Enable to Output High	C_L = 50 pF, R_L = 500, DE = 0.3V S1 Open Bn = 1V	2	5	12	ns
t_{LZ}	Receiver Disable From Output Low	C_L = 50 pF, R_L = 500, DE = 0.3V S2 Open Bn = 2V	1	5	8	ns
t_{HZ}	Receiver Disable From Output High	C_L = 50 pF, R_L = 500, DE = 0.3V S1 Open Bn = 1V	1	4	8	ns

Note 1: t_D and t_R skew is an absolute value, defined as differences seen in propagation delays between each of the drivers or receivers in the same package of the same delay, V_{CC}, temperature and load conditions.



TL/F/8698–12

FIGURE 1. Equivalent Bus Output



Note: n = 1, 2, 3, 4

TL/F/8698–2

FIGURE 2. Driver Output Voltage

AC Test Circuits

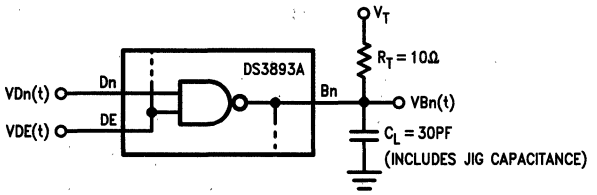


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FIGURE 3

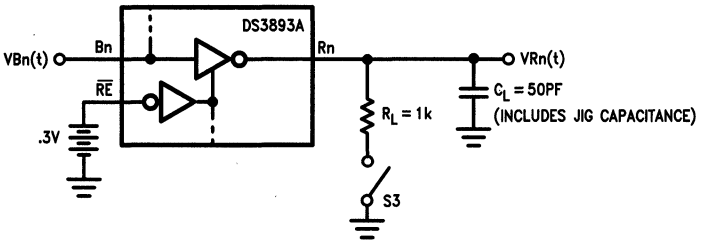

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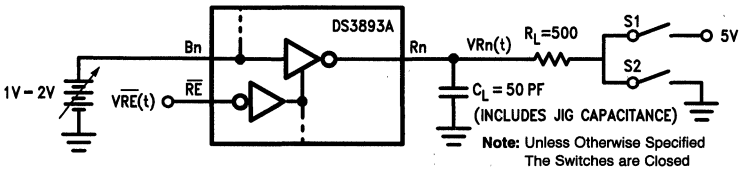
FIGURE 4



Note: Unless Otherwise Specified
The Switches are Closed

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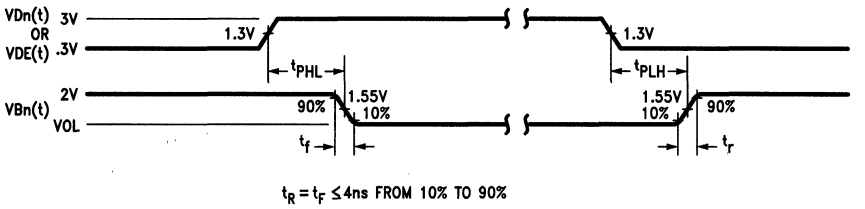
FIGURE 5

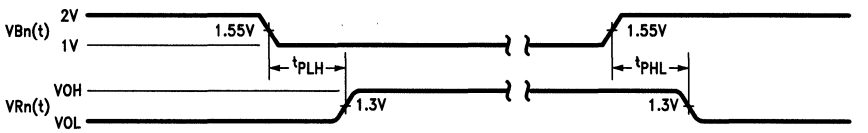
Switching Time Waveforms



$t_R = t_F \leq 4$ns FROM 10% TO 90%

TL/F/8698–6

FIGURE 6. Driver Propagation Delay

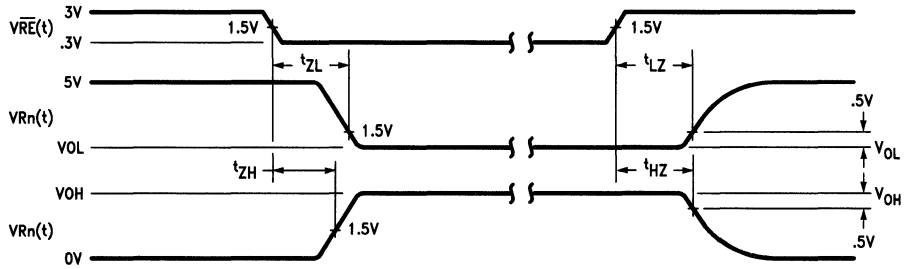


$t_R = t_F \leq 4$ns FROM 10% TO 90%

TL/F/8698–7

FIGURE 7. Receiver Propagation Delay

Switching Time Waveforms (Continued)



Note: $t_R = t_F \leq 4$ ns From 10% to 90%

Note: n = 1, 2, 3, 4

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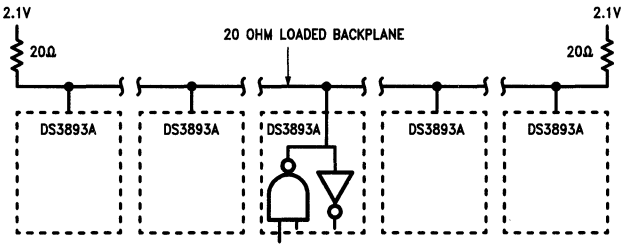
FIGURE 8. Receiver Enable and Disable Times

Typical Application



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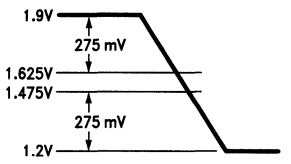
Application Information

Due to the high current and very high speed capability of the TURBOTRANSCEIVER's driver output stage, circuit board layout and bus grounding are critical factors that affect the system performance.

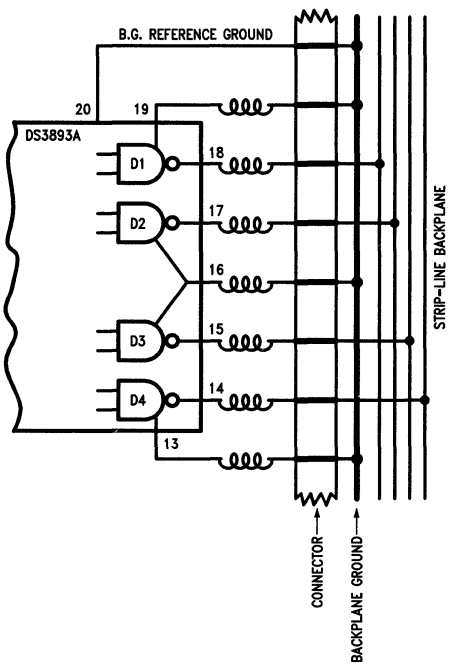
Each of the TURBOTRANSCEIVER's bus ground pins should be connected to the nearest backplane ground pin with the shortest possible path. The ground pins on the connector should be distributed evenly through its length.

Although the bandgap reference receiver threshold provides sufficient DC noise margin *(Figure 9)*, ground noise and ringing on the data paths could easily exceed this margin if the series inductance of the traces and connectors are not kept to a minimum. The bandgap ground pin should be returned to the connector through a separate trace that does not carry transient switching currents. The transceivers should be mounted as close as possible to the connector. It should be noted that even one inch of trace can add a significant amount of ringing to the bus signal.



TL/F/8698–10

FIGURE 9. Noise Margin



TL/F/8698–11

FIGURE 10

National Semiconductor

DS3896/DS3897 BTL Trapezoidal™ Transceivers

General Description

These advanced transceivers are specifically designed to overcome problems associated with driving a densely populated backplane, and thus provide significant improvement in both speed and data integrity. Their low output capacitance, low output signal swing and noise immunity features make them ideal for driving low impedance buses with minimum power consumption.

The DS3896 is an octal high speed schottky bus transceiver with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. The separate driver disable pins (En) feature internal pull ups and may be left open if not required. On the other hand, the DS3896 provides high package density for data/address lines.

The open collector drivers generate precise trapezoidal waveforms, which are relatively independent of capacitive loading conditions on the outputs. This significantly reduces noise coupling to adjacent lines. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity and provide equal rejection to both negative and positive going noise pulses on the bus.

To minimize bus loading, these devices also feature a schottky diode in series with the open collector output that isolates the driver output capacitance in the disabled state. The output low voltage is typically "1V" and the output high level is intended to be 2V. This is achieved by terminating the bus with a pull up resistor to 2V at both ends. The device can drive an equivalent DC load of 18.5Ω (or greater) in the above configuration.

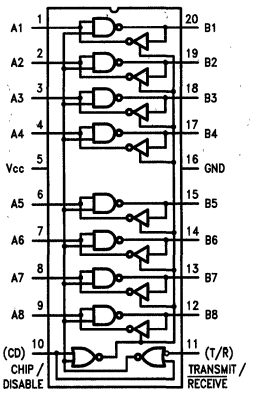
These signalling requirements, including a 1 volt signal swing, low output capacitance and precise receiver thresholds are referred to as Bus Transceiver Logic (BTL).

Features

- 8 bit DS3896 transceiver provides high package density
- 4 bit DS3897 transceiver provides separate driver input and receiver output pins
- BTL compatible
- Less than 5 pF output capacitance for minimal bus loading
- 1 Volt bus signal swing reduces power consumption
- Trapezoidal driver waveforms (t_r, $t_f \cong 6$ ns typical) reduce noise coupling to adjacent lines
- Temperature insensitive receiver thresholds track the bus logic high level to maximize noise immunity in both high and low states
- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs and receiver outputs

Logic Diagrams

DS3896N, M



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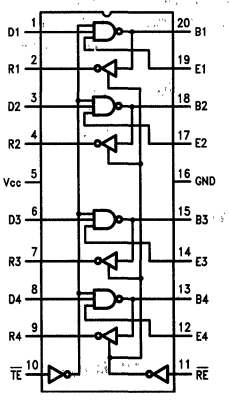
DS3897N, M



TL/F/8510–2

Order Numbers DS3896M, DS3896N, DS3897M or DS3897N
See NS Package Number M20B or N20A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Power Dissipation at 70°C N Package	1480 mW
M Package	TBD mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Termination Voltage	1.90	2.10	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics: (Note 2 and 3) (0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs: (An, Dn, En, CD, T/$\overline{R}$, $\overline{RE}$, $\overline{TE}$)						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	An = Dn = En = V_{CC}			1	mA
I_{IH}	Logical "1" Input Current	An = Dn = En = 2.4V			40	μA
I_{IHC}	Logical "1" Input Current	CD = T/$\overline{R}$ = $\overline{RE}$ = $\overline{TE}$ = 2.4V			80	μA
I_{IL}	Logical "0" Input Current	An = Dn = En = 0.4V		−1	−1.6	mA
I_{ILC}	Logical "0" Input Current	CD = T/$\overline{R}$ = $\overline{RE}$ = $\overline{TE}$ = 0.4V		−180	−400	μA
V_{CL}	Input Diode Clamp Voltage	Iclamp = −12 mA		−0.9	−1.5	V
Driver Output/Receiver Input: (Bn)						
V_{OLB}	Low Level Bus Voltage	An = Dn = En = T/$\overline{R}$ = 2V, VL = 2V RL = 18.5Ω, CD = $\overline{TE}$ = 0.8V (*Figure 1*)	0.75	1.0	1.2	V
I_{IHB}	Maximum Bus Current (Power On)	An = Dn = En = 0.8V, V_{CC} = 5.25V Bn = 2V		10	100	μA
I_{ILB}	Maximum Bus Current (Power Off)	An = Dn = En = 0.8V, V_{CC} = 0V Bn = 2V			100	μA
V_{TH}	Receiver Input Threshold	V_{CC} = 5V	1.47	1.55	1.62	V
Receiver Output: (An, Rn)						
V_{OH}	Logical "1" Output Voltage	Bn = 1.2V, I_{OH} = −400 μA CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	Bn = 2V, I_{OL} = 16 mA CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V		0.35	0.5	V
I_{OS}	Output Short Circuit Current	Bn = 1.2V CD = T/$\overline{R}$ = $\overline{RE}$ = 0.8V	−20	−70	−100	mA
I_{CC}	Supply Current (DS3896)	V_{CC} = 5.25V		90	135	mA
I_{CC}	Supply Current (DS3897)	V_{CC} = 5.25V		50	80	mA

Note 1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristic" provide conditions for actual device operation.

Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. All typicals are given for V_{CC} = 5V and T_a = 25°C.

DS3896 Switching Characteristics

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	An to Bn	CD = 0.8V, T/$\overline{R}$ = 2.0V, VL = 2V	5	9	15	ns
t_{DHL}		*(Figure 2)*	5	9	15	ns
t_{DLHC}	CD to Bn	An = T/$\overline{R}$ = 2.0V, VL = 2V	5	10	18	ns
t_{DHLC}		*(Figure 2)*	5	12	20	ns
t_{DLHT}	T/$\overline{R}$ to Bn	VCI = An, VC = 5V, *(Figure 5)*	5	15	25	ns
t_{DHLT}		CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 18Ω, RL2 = NC, VL = 2V	5	22	35	ns
t_R	Driver Output Rise Time	CD = 0.8V, T/$\overline{R}$ = 2V, VL = 2V	3	6	10	ns
t_F	Driver Output Fall Time	*(Figure 2)*	3	6	10	ns
Receiver:						
t_{RLH}	Bn to An	CD = 0.8V, T/$\overline{R}$ = 0.8V	5	12	18	ns
t_{RHL}		*(Figure 3)*	5	10	18	ns
t_{RLZC}	CD to An	Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 5 pF RL1 = 390Ω, RL2 = NC, VL = 5V *(Figure 4)*	5	10	18	ns
t_{RZLC}		Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k, VL = 5V *(Figure 4)*	5	8	15	ns
t_{RHZC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 4)*	2	4	8	ns
t_{RZHC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF *(Figure 4)*	3	7	12	ns
t_{RLZT}	T/$\overline{R}$ to An	VCI = Bn, VC = 2V, RC = 18Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 5)*	5	10	18	ns
t_{RZLT}		VCI = Bn, VC = 2V, RC = 18Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = 1.6k, CL = 30 pF *(Figure 5)*	14	24	40	ns
t_{RHZT}		VCI = Bn, VC = 0V, RC = 18Ω, CD = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF *(Figure 5)*	2	4	8	ns
t_{RZHT}		VCI = Bn, VC = 0V, RC = 18Ω, CD = 0.8V, VL = 0V, RL1 = NC RL2 = 1.6k, CL = 30 pF *(Figure 5)*	2	8	15	ns
t_{NR}	Receiver Noise Rejection Pulse Width	*(Figure 6)*	3	6		ns

Note: NC means open

DS3897 Switching Characteristics

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	Dn, En to Bn	$\overline{TE}$ = 0.8V, $\overline{RE}$ = 2.0V, VL = 2V	5	9	15	ns
t_{DHL}		*(Figure 2)*	5	9	15	ns
t_{DLHT}	$\overline{TE}$ to Bn	An = $\overline{RE}$ = 2.0V, VL = 2V, *(Figure 2)*	5	10	18	ns
t_{DHLT}		RC = 390Ω, VCI = An, VC = 5V, CL = 30 pF RL1 = 18Ω, RL2 = NC, VL = 2V *(Figure 5)*	5	12	20	ns
t_R	Driver Output Rise Time	CD = 0.8V, T/$\overline{R}$ = 2V, VL = 2V	3	6	10	ns
tF	Driver Output Fall Time	*(Figure 2)*	3	6	10	ns

DS3897 Switching Characteristics (Continued)

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Receiver:						
t_{RLH}	Bn to Rn	$\overline{TE}$ = 2.0V, $\overline{RE}$ = 0.8V (*Figure 3*)	5	10	18	ns
t_{RHL}			5	12	18	ns
t_{RLZR}	$\overline{RE}$ to Rn	Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 5 pF RL1 = 390Ω, RL2 = NC (*Figure 4*)	5	10	18	ns
t_{RZLR}		Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6k (*Figure 4*)	5	8	15	ns
t_{RHZR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 4*)	2	4	8	ns
t_{RZHR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V, RL1 = NC, RL2 = 1.6k, CL = 30 pF (*Figure 4*)	3	7	12	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 6*)	3	6		ns
Driver plus Receiver:						
t_{DRLH}	Dn to Rn	$\overline{TE}$ = $\overline{RE}$ = 0.8V (*Figure 7*)	10	20	30	ns
t_{DRHL}			10	20	30	ns

Note: NC means open

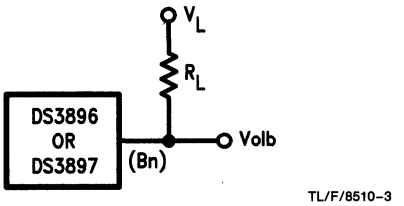
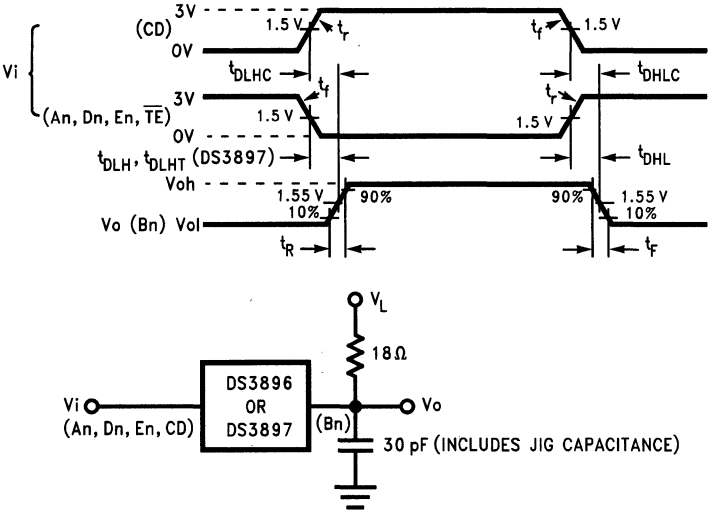
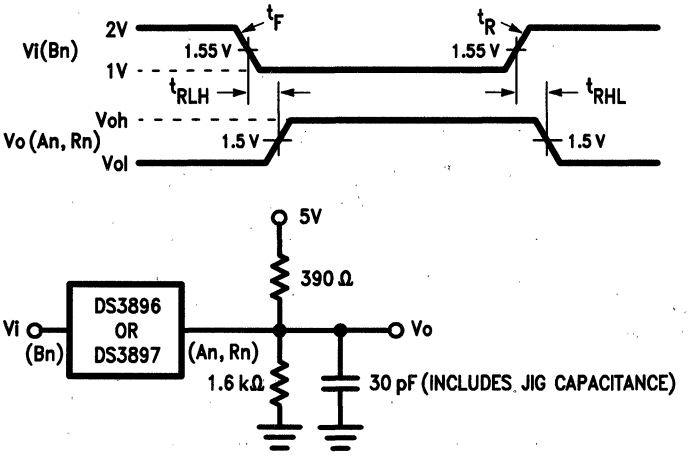


FIGURE 1. Driver Output Low Voltage Test



Note: t_r = t_f ≤ 5 ns from 10% to 90%

FIGURE 2. Driver Propagation Delays



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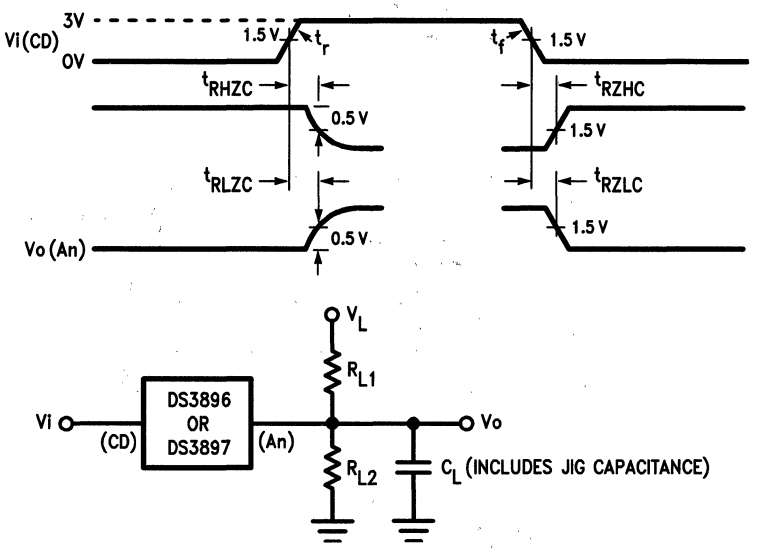
Note: $t_R = t_F \leq 10$ ns from 10% to 90%

FIGURE 3. Receiver Propagation Delays



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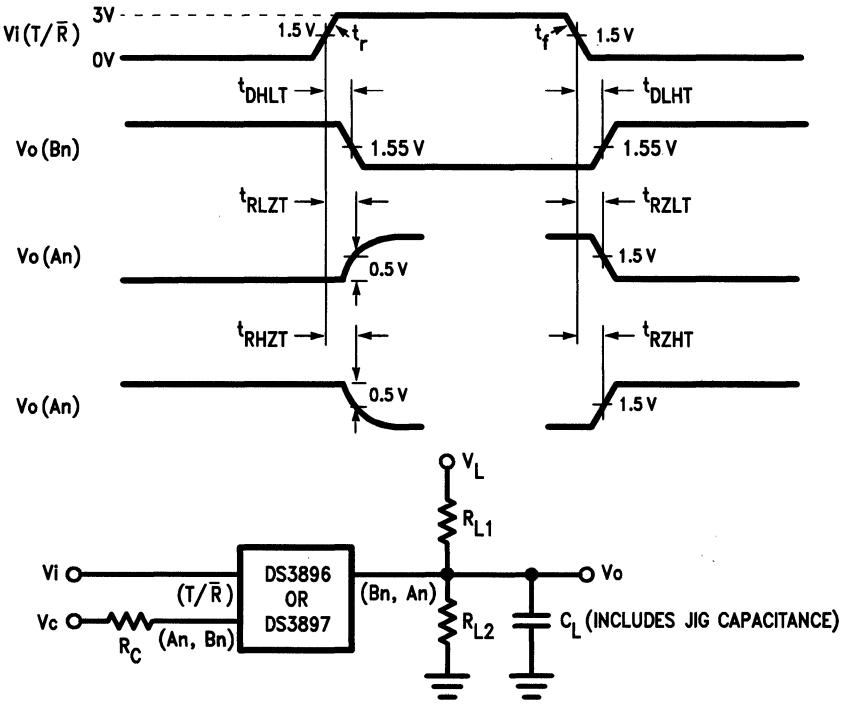
Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. Propagation Delay from CD pin to An



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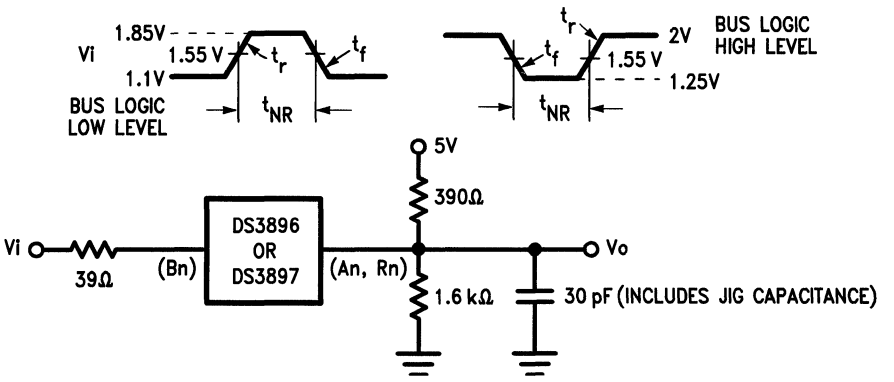
Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 5. Propagation Delay from T/R pin to An or Bn



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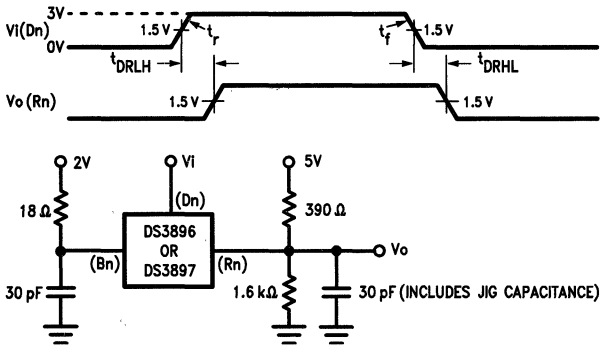
Note: $t_r = t_f = 2$ ns from 10% to 90%

FIGURE 6. Receiver Noise Immunity: "No Response at Output" Input Waveforms



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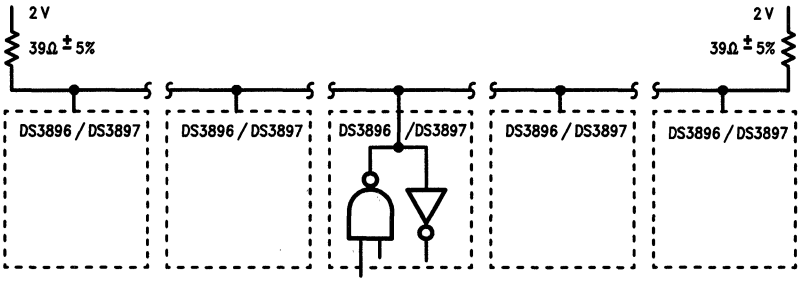
Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 7. Driver Plus Receiver Delays

Typical Application



TL/F/8510–10

National Semiconductor

DS1776 PI-Bus Transceiver

General Description

The DS1776 is an octal PI-bus Transceiver. The A to B path is latched. B outputs are open collector with series Schottky diode, ensuring minimum B output loading. B outputs also have ramped rise and fall times (2.5 ns typical), ensuring minimum PI-bus ringing. B inputs have glitch rejection circuitry, 4 ns typical.

Designed using National's Bi-CMOS process for both low operating and disabled power. AC performance is optimized for the PI-Bus inter-operability requirements.

The DS1776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. This bus has a loaded characteristic impedance range of 20Ω to 50Ω and is terminated on each end with a 30Ω to 40Ω resistor.

The DS1776 is an octal bidirectional transceiver with open collector B and TRI-STATE® A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

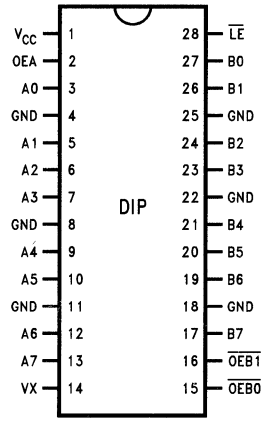
A separate high level control voltage (V_X) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, V_X is tied to V_{CC}.

Features

- Mil-Std-883C qualified
- Similar to BTL
- Low power I_{CCL} = 41 mA max
- B output controlled ramp rate
- B input noise immunity, typically 4 ns
- Available in 28-pin DIP, Flatpak and CLCC
- Pin and function compatible with Signetics 54F776

Pin Configurations

Pin Configuration



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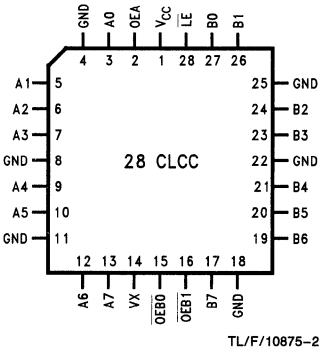
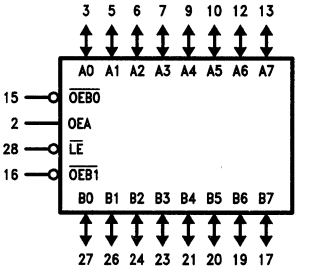
Pin Configuration



TL/F/10875–2

Logic Symbol



TL/F/10875–3

Order Number DS1776E/883 or DS1776J/883
See NS Package E28A or J28B

MIL-STD-883C

DEVICE SPECIFICATIONS

Absolute Maximum Ratings (Notes 1 and 2)

The 883 specifications are written to reflect the Rel Electrical Test Specifications (RETS) established by National Semiconductor for this product. For a copy of the latest RETS please contact your local National Semiconductor sales office or distributor.

Supply Voltage (V_{CC})	−0.5V to +7.0V
V_X, V_{OH} Output Level Control Voltage (A Outputs)	−0.5V to +7.0V
$\overline{OEB}$n, OEA, $\overline{LE}$ Input Voltage (V_I)	−0.5V to +7.0V
A0–A7, B0–B7 Input Voltage (V_I)	−0.5V to +5.5V
Input Current (I_I)	−40 mA to +5 mA
Voltage Applied to Output in High Output State (V_O)	−0.5V to +V_{CC}V
A0–A7 Current Applied to Output in Low Output State (I_O)	40 mA
B0–B7 Current Applied to Output in Low Output State (I_O)	200 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temperature (Soldering 10 Sec.)	260°C
ESD Tolerance: C_{ZAP} = 120 pF, R_{ZAP} = 1500Ω	0.5 kV

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Operating Temp. Range (T_A)	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		50	ns

PI Bus Transceiver DS1776

DC Electrical Characteristics V_{CC} = 5V ±10% (Unless Otherwise Specified)

DC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = −55°C

Symbol	Parameter		Conditions (Notes 3 & 5)		Temp. Group	Min	Typ (Note 4)	Max	Units
V_{IH}	High Level Input Voltage	Except Bn			1, 2, 3	2			V
		Bn				1.6			V
V_{IL}	Low Level Input Voltage	Except Bn			1, 2, 3			0.8	V
		Bn						1.45	V
I_{OH}	High Level Output Current	An	V_{IN} = V_{IH} V_{OH} = V_{CC} − 2.0V		1, 2, 3			−3	mA
	High Level Output Current	Bn	V_{CC} = Max, OEA = $\overline{LE}$ V_{IH} = 2.0V, V_{OH} = 2.1V					100	µA
I_{OL}	Low Level Output Current	An	V_{IN} = V_{IL} V_{OL} = 0.5V		1, 2, 3			20	mA
		Bn	V_{OL} = 1.15V					100	mA
I_{IK}	Input Clamp Current	Except An			1, 2, 3			−18	mA
		An						−40	mA
I_{OZ}	TRI-STATE Output Leakage Current	An Bn			1, 2, 3			±70	µA
V_{OH}	High Level Output Voltage	An	V_{CC} = Min, V_{IH} = 1.9V	I_{OH} = − 3 mA V_X = V_{CC}	1, 2, 3	2.5		V_{CC}	V
				I_{OH} = −0.4 mA V_X = 3.13V to 3.47V		2.5		V_X	V

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions. Unless otherwise specified, V_X = V_{CC} for all test conditions.

Note 4: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 5: Due to test equipment limitations, actual test conditions are for V_{IH} = 1.9V and for V_{IL} = 1.2V, however the specified test limits and conditions are guaranteed.

MIL-STD-883C

PI Bus Transceiver DS1776 (Continued)

DC Electrical Characteristics V_{CC} = 5V ±10% (Unless Otherwise Specified)

DC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = −55°C (Continued)

Symbol	Parameter		Conditions (Notes 3 & 5)		Temp. Group	Min	Typ (Note 4)	Max	Units
V_{OL}	Low Output Level Voltage	An	V_{CC} = Min, V_{IL} = 1.2V	I_{OL} = 20 mA, $V_X = V_{CC}$				0.5	V
		Bn	V_{CC} = Min, V_{IL} = 0.8V	I_{OL} = 100 mA I_{OL} = 4 mA	1, 2, 3	0.4		1.15	V
V_{IK}	Input Clamp Voltage	An Except An	V_{CC} = Min, I_I = −40 mA V_{CC} = Min, I_I = −18 mA		1, 2, 3			−0.5 −1.2	V V
I_{IH2}	Input Current at Max Input Voltage	$\overline{OEBn}$, OEA, $\overline{LE}$	V_{CC} = Min, V_I = 7.0V		1, 2, 3		1	100	µA
		An	V_{CC} = Min, V_I = 5.5V				0.01	1	mA
		Bn	V_{CC} = Min, V_I = 5.5V				0.01	1	mA
I_{IH1}	Input Current at Max Input Voltage	$\overline{OEB}$, OEA, $\overline{LE}$ B0–B7	V_{CC} = Max, V_I = 2.7V V_{CC} = Max, V_I = 2.1V					20 100	µA µA
I_{IL}	Low Level Input Current	$\overline{OEB}$, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 0.5V		2, 3	−40			µA
					1	−20			µA
		Bn	V_{CC} = Max, V_I = 0.3V		1, 2, 3	−100			µA
I_{OZH} + I_{IH}	TRI-STATE Output Current, High Level Voltage Applied	An	V_{CC} = Max, V_O = 2.7V		1, 2, 3			70	µA
I_{OZH} + I_{IL}	TRI-STATE Output Current, Low Level Voltage Applied	An	V_{CC} = Max, V_O = 0.5V		1, 2, 3	−70			µA
I_X	High Level Control Current		V_{CC} = Max, $V_X = V_{CC}$, $\overline{LE}$ = OEA = $\overline{OEBn}$ = 2.7V An = 2.7V, Bn = 2.0V		1, 2, 3	−100		100	µA
			V_{CC} = Max, V_X = 3.14V & 3.47V, $\overline{LE}$ = OEA = $\overline{OEBn}$ = 2.7V, An = 2.7V, Bn = 2.0V		1, 2, 3	−10		10	mA
I_{OS}	Short-Circuit Output Current (Note 6)	An	V_{CC} = Max, Bn = 1.9V, OEA = 2.0V, $\overline{OEBn}$ = 2.7V		1, 2, 3	−60	−75	−150	mA
I_{CC}	Supply Current	I_{CCH}	V_{CC} = Max, V_{IH} (A) = 5.0V		1, 2			37	mA
		I_{CCH}			3			41	mA
		I_{CCL}	V_{CC} = Max, V_{IL}(A) = 0.3V		1, 2, 3			38	mA
		I_{CCZ}	V_{CC} = Max, V_{IL}(A) = 0.3V		1, 2, 3			35	mA
I_{OFF}	Power Off Output Current		Bn = 2.1V, V_{CC} = 0.0V, V_{IL} = Max or V_{IH} = Min		1, 2, 3			100	µA

Note 6: Not more than one output should be shorted at a time. For testing I_{OS}, the use of high speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature above normal and thereby cause invalid readings in other parameter tests. In any squence of parameter test, I_{OS} tests should be performed last.

MIL-STD-883C

PI Bus Transceiver DS1776

AC Electrical Characteristics V_{CC} = 5V ± 10% (Unless otherwise specified)

AC testing temp. groups: 1 = +25°C, 2 = +125°C, 3 = −55°C

Path	Parameter	Conditions	Temp. Group	Min	Max	Units
B-TO-A PATH						
t_{PLH}	Propagation Delay B to A	Waveform 1, 2	1, 2, 3	4.5	17	ns
t_{PHL}				6	17	ns
t_{PZH}	Output Enable OEA to A	Waveform 3, 4	1, 2, 3	4	17	ns
t_{PZL}				4	17	ns
t_{PHZ}	Output Disable OEA to A	Waveform 3, 4	1, 2, 3	2	12	ns
t_{PLZ}				2	13	ns
A-TO-B PATH						
t_{PLH}	Propagation Delay A to B	Waveform 1, 2	1, 3	2	13	ns
			2	2	17	ns
t_{PHL}			1, 2, 3	2.5	13	ns
t_{PLH}	Propagation Delay $\overline{LE}$ to B	Waveform 1, 2	1, 3	2	16	ns
			2	2	22	ns
t_{PHL}			1, 2, 3	2	16	ns
t_{PLH}	Enable/Disable $\overline{OEBn}$ to B	Waveform 1, 2	1, 3	2	13	ns
			2	2	16	ns
t_{PHL}			1	3.5	14	ns
			2	3.5	13	ns
			3	3.5	16	ns
t_{TLH}	Transition Time, B Side	1.3V to 1.7V	1, 3	0.5	5.5	ns
			2	0.5	10	ns
t_{THL}		1.7V to 1.3V	1	0.5	5.5	ns
			2	0.5	7	ns
			3	0.5	10	ns
SETUP/HOLD/PULSE WIDTH SPECS						
t_S	A to $\overline{LE}$ Setup	Waveform 5	1, 2, 3	7		ns
t_H	A to $\overline{LE}$ Hold	Waveform 5	1, 2, 3	0		ns
t_W	$\overline{LE}$ Pulse Width Low	Waveform 5	1, 2, 3	12		ns

Description

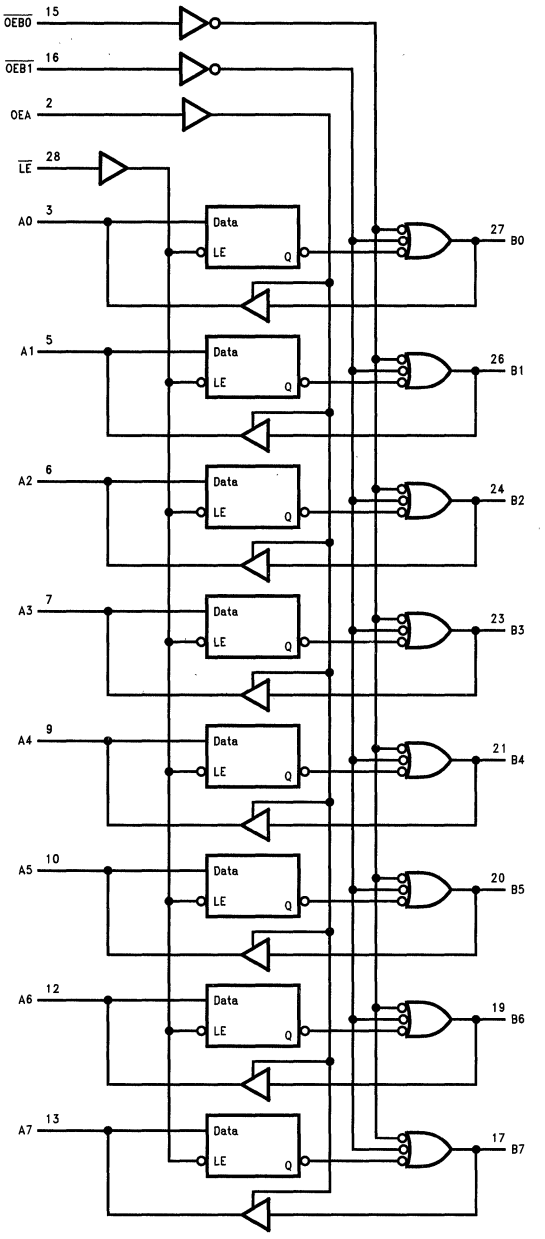
PIN DESCRIPTION

TABLE I. Pin Description

Symbol	Pins	Type	Name and Function
A0	3	I/O	TTL Level, latched input/TRI-STATE output (with V_X control option)
A1	5	I/O	
A2	6	I/O	
A3	7	I/O	
A4	9	I/O	
A5	10	I/O	
A6	12	I/O	
A7	13	I/O	
B0	27	I/O	Data input with special threshold circuitry to reject noise/Open Collector output, High current drive
B1	26	I/O	
B2	24	I/O	
B3	23	I/O	
B4	21	I/O	
B5	20	I/O	
B6	19	I/O	
B7	17	I/O	
$\overline{OEB0}$	15	I	Enables the B outputs when both pins are low
$\overline{OEB1}$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X (V_X = V_{CC} for normal use)

Description (Continued)

FUNCTION DESCRIPTION



TL/F/10875–4

V_{CC} = Pin 1
V_X = Pin 14
GND = Pins 4, 8, 11, 18, 22, 25

FIGURE 1. Functional Logic Diagram

Description (Continued)

TABLE II. Function Table

Inputs						Latch State	Outputs		Mode
An	Bn (Note 3)	$\overline{LE}$	OEA	$\overline{OEB0}$	$\overline{OEB1}$		An	Bn	
H	X	L	L	L	L	H	Z	H	A TRI-STATE, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Qn	Z	Qn	A TRI-STATE, Latched Data to B
—	—	L	H	L	L	(Note 1)	(Note 1)	(Note 1)	Feedback: A to B, B to A
—	H	H	H	L	L	H (Note 2)	H	off (Note 2)	Preconditioned Latch Enabling Data Transfer from B to A
—	L	H	H	L	L	H (Note 2)	L	off (Note 2)	
—	—	H	H	L	L	Qn	Qn	Qn	Latch State to A and B
H	X	L	L	H	X	H	Z	off	B off and A TRI-STATE
L	X	L	L	H	X	L	Z	off	
X	X	H	L	H	X	Qn	Z	off	
—	H	L	H	H	X	H	H	off	B off, Data from B to A
—	L	L	H	H	X	L	L	off	
—	H	H	H	H	X	Qn	H	off	
—	L	H	H	H	X	Qn	L	off	
H	X	L	L	X	H	H	Z	off	B off and A TRI-STATE
L	X	L	L	X	H	L	Z	off	
X	X	H	L	X	H	Qn	Z	off	
—	H	L	H	X	H	H	H	off	B off, Data from B to A
—	L	L	H	X	H	L	L	off	
—	H	H	H	X	H	Qn	H	off	
—	L	H	H	X	H	Qn	L	off	

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
— = Input not externally driven
Z = High Impedance (off) state
Qn = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
Note 1: Condition will cause a feedback loop path; A to B and B to A.
Note 2: The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB0}$ and $\overline{OEB1}$, are Low and $\overline{LE}$ is high.
Note 3: Precaution should be taken to ensure that the B inputs do not float. If they do, they are equal to a Low state.
off = Applies to "B" (OC) outputs only. Indicates that the outputs are turned off.

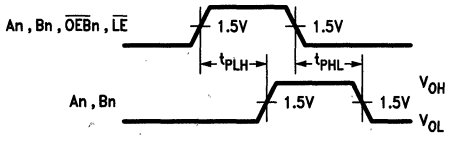
CONTROLLER POWER SEQUENCING OPERATION

The DS1776 has a design feature which controls the output transitions during power up (or down). There are two possible conditions that occur.

1. When $\overline{LE}$ = Low and $\overline{OEBn}$ = Low, the B outputs are disabled until the $\overline{LE}$ circuit can take control. This feature ensures that the B outputs will follow the A inputs and allow only one transition during power up (or down).
2. If $\overline{LE}$ = High or $\overline{OEBn}$ = High, then the B outputs still remain disabled during power up (or down).

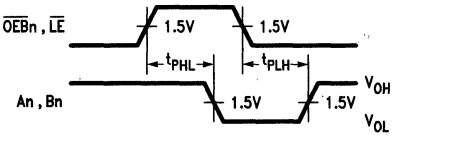
Switching Characteristics

AC WAVEFORMS



TL/F/10875–5

Waveform 1: Propagation Delay for Data to Output

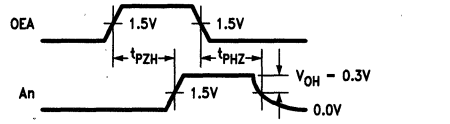


TL/F/10875–6

Waveform 2: Propagation Delay for Data to Output

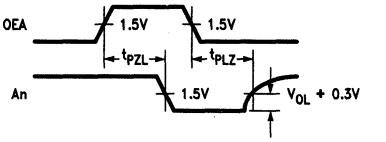
Switching Characteristics (Continued)

AC WAVEFORMS (Continued)



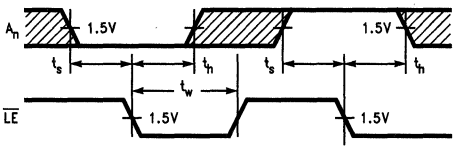
TL/F/10875–7

Waveform 3: TRI-STATE Output Enable Time to High Level and Output Disable Time from High Level



TL/F/10875–8

Waveform 4: TRI-STATE Output Enable Time to Low Level and Output Disable Time from Low Level



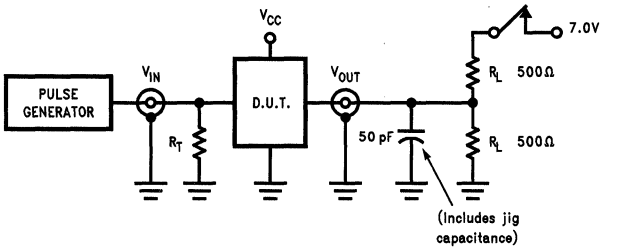
TL/F/10875–9

Waveform 5: Data Setup and Hold Times and LE Pulse Widths

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

Test Circuit for TRI-STATE Outputs on A Side

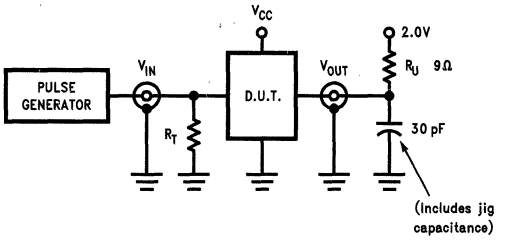


TL/F/10875–10

Switch Position

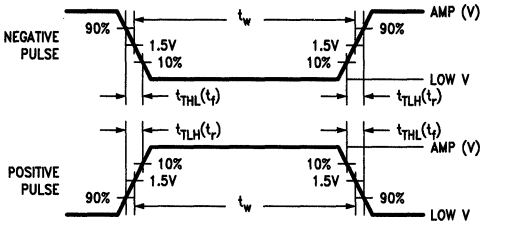
Test	Switch
t_{PLZ}, t_{PZL}	Closed
All Other	Open

Test Circuit for TRI-STATE Outputs on B Side



TL/F/10875–12

Input Pulse Definition



TL/F/10875–11

DEFINITIONS

R_L = Load resistor 500Ω
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
R_U = Pull up resistor

	Input Pulse Characteristics					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Side	3.0V	0.0V	1 MHz	500 ns	2 ns	2 ns
B Side	2.0V	1.0V	1 MHz	500 ns	2 ns	2 ns

Section 11

General Purpose Bus Circuits

Section 11 Contents

National Semiconductor

DP8303A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

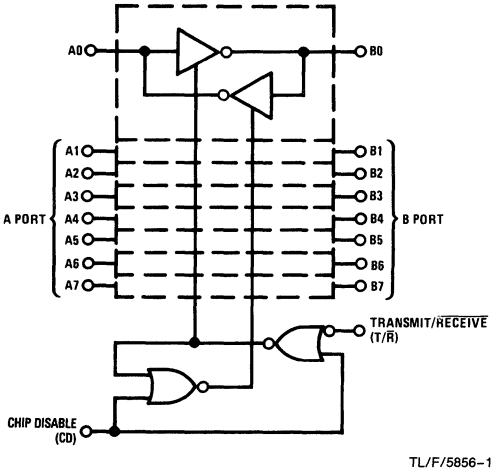
This family of high speed Schottky 8-bit TRI-STATE bidirectional transceivers are designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Features

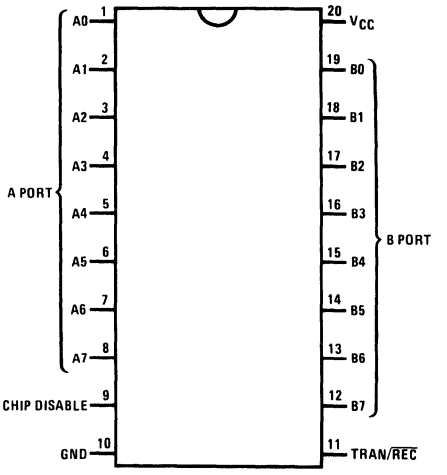
- 8-bit directional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



TL/F/5856–1

Dual-In-Line Package



TL/F/5856–2

Top View
Order Number DP8303AN
See NS Package Number N20A

Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C.

Storage Temperature	−65°C to +150°C
Lead Temperature (soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP8303A	4.75	5.25	V
Temperature (T_A)			
DP8303A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V				0.7	V
V_{OH}	Logical "1" Output Voltage	CD = T/$\overline{R}$ = V_{IL}, V_{IL} = 0.5V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} − 0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}, V_{IL} = 0.5V	I_{OL} = 16 mA		0.35	0.5	V
			I_{OL} = 8 mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max, (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}				0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IL} = 0.5V	I_{OH} = −0.4 mA	V_{CC} − 1.15	V_{CC} −0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 0.4V			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN}, V_{CC} = Max			70	100	mA
		CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2V, V_{CC} = Max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 30 pF		20	30	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 5k, C4 = 30 pF		19	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 7	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	20 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PLZB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		25 16	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5kΩ, C4 = 45 pF		22 14	35 25	ns ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT/RECEIVE MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		23	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		23	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 1k, C3 = 300 pF S2 = 0, R3 = 300Ω, C2 = 5 pF		27	35	ns

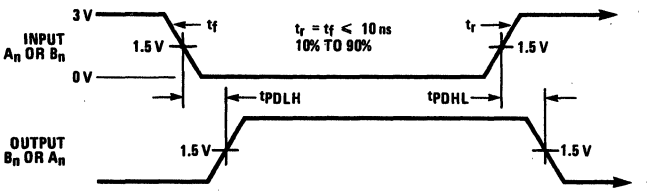
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

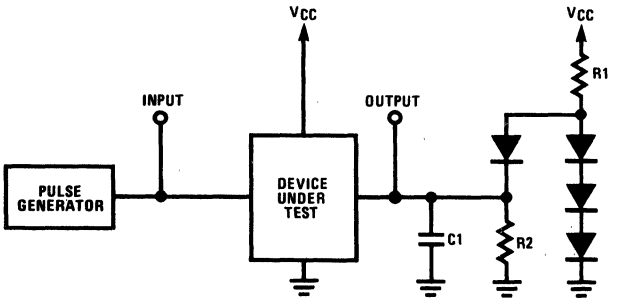
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



TL/F/5856–3



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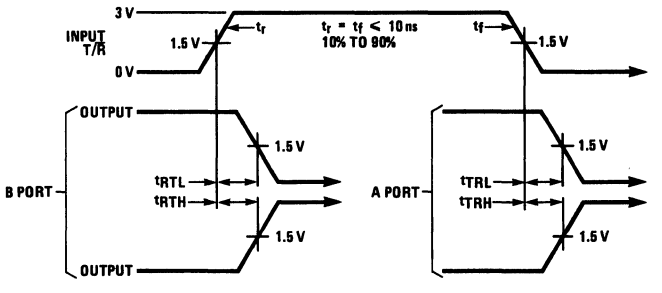
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)



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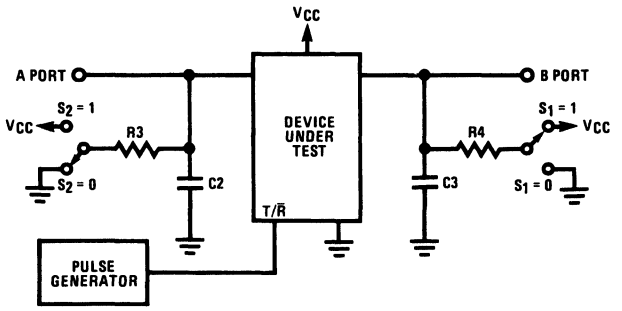
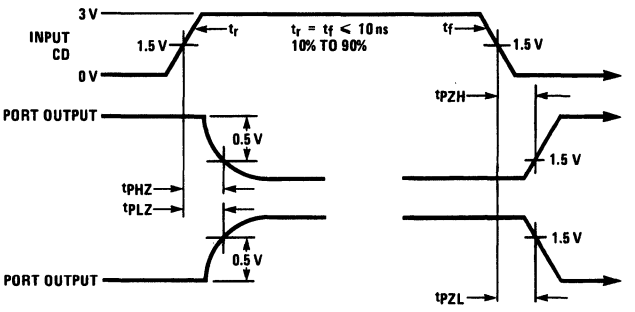


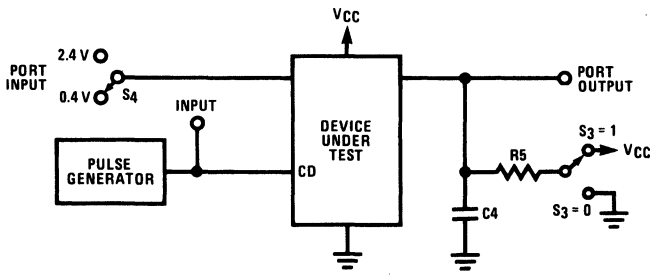
TL/F/5856–6

Note: C2 ad C3 include test fixture capacitance.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port



TL/F/5856–7



TL/F/5856–8

Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

National Semiconductor

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

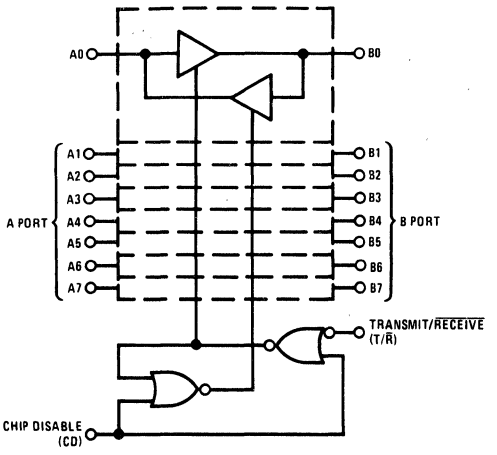
The DP73048B/DP8304B are high speed Schottky 8-bit TRI-STATE bidirectional transceivers designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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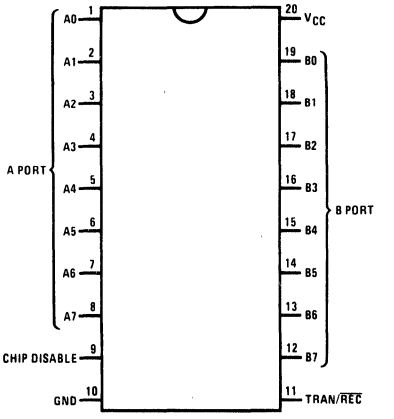
Dual-In-Line Package



TL/F/8793–2

Top View

Order Number DP7304BJ, DP8304BJ, DP8304BN or DP8304BWM
See NS Package Number J20A, N20A or M20B

Logic Table

Inputs		Resulting Conditions	
Chip Disable	**Transmit/$\overline{\text{Receive}}$**	**A Port**	**B Port**
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7304B	4.5	5.5	V
DP8304B	4.75	5.25	V
Temperature (T_A)			
DP7304B	−55	125	°C
DP8304B	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OL} = 16 mA (8304B)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = Max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = Max (Note 4)		−25	−50	−150	mA

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DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
B PORT (B0–B7) (Continued)							
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = Max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA
CONTROL INPUTS CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8304B			0.8	V
			DP7304B			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN} = 0.4V, V_{CC} = Max			70	100	mA
		CD = V_{INA} = 0.4V, T/$\overline{R}$ = 2V, V_{CC} = Max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 1k, CR = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 30 pF		27	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V *(Figure C)* S3 = 0, R5 = 5k, C4 = 30 pF		19	25	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 18 11	 23 18	 ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 16 11	 23 18	 ns ns

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
B PORT DATA/MODE SPECIFICATIONS (Continued)						
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		 32 16	 40 22	 ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V *(Figure C)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		 26 14	 35 22	 ns ns
TRANSMIT/$\overline{\text{RECEIVE}}$ MODE SPECIFICATIONS						
t_{TRL}	Propagation Delay from Transmit Mode to $\overline{\text{Receive}}$ a Logical "0", T/$\overline{R}$ to A Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 100Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to $\overline{\text{Receive}}$ a Logical "1", T/$\overline{R}$ to A Port	CD = 0.4V, *(Figure B)* S1 = 1, R4 = 100Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		28	40	ns
t_{RTH}	Propagation Delay from $\overline{\text{Receive}}$ Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port	CD = 0.4V *(Figure B)* S1 = 0, R4 = 1k, C3 = 300 pF S2 = 1, R3 = 300Ω, C2 = 5 pF		28	40	ns

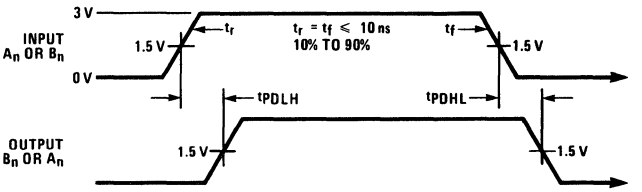
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

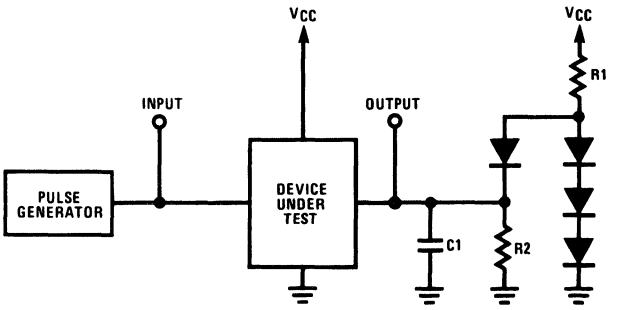
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



TL/F/8793–3

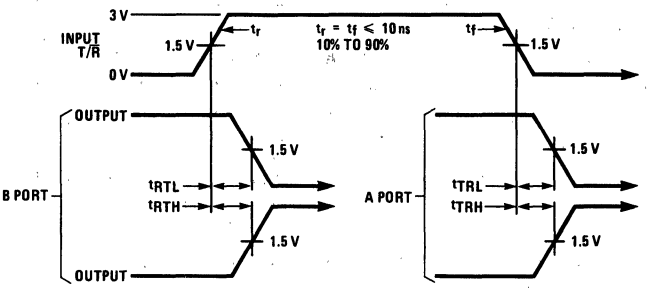


TL/F/8793–4

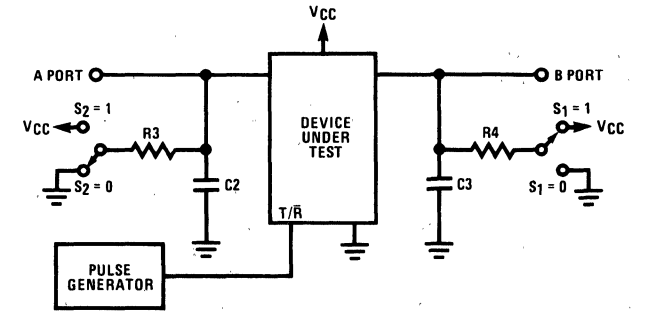
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (Continued)



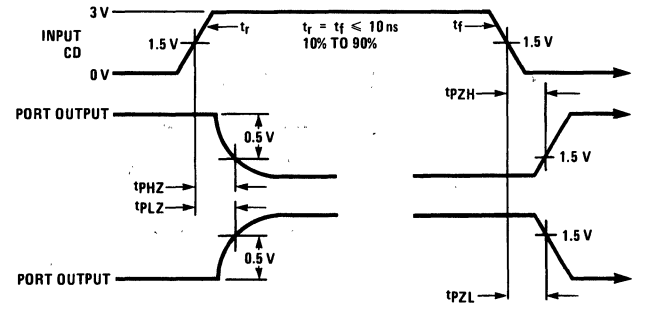
TL/F/8793–5



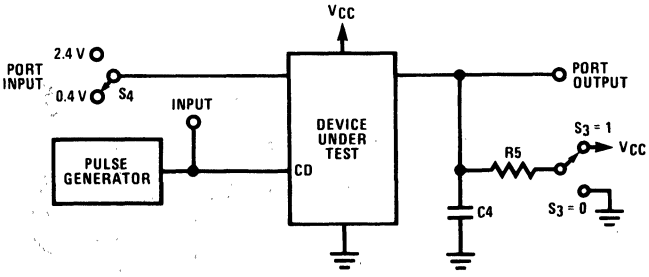
TL/F/8793–6

Note: C2 and C3 include test fixture capacitance.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port



TL/F/8793–7



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Note: C4 includes test fixture capacitance.

Port input is in a fixed logical condition. See AC table.

FIGURE C. Propagation Delay to/from TRI-STATE from CD to A Port or B Port

National Semiconductor

DP8307A 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

General Description

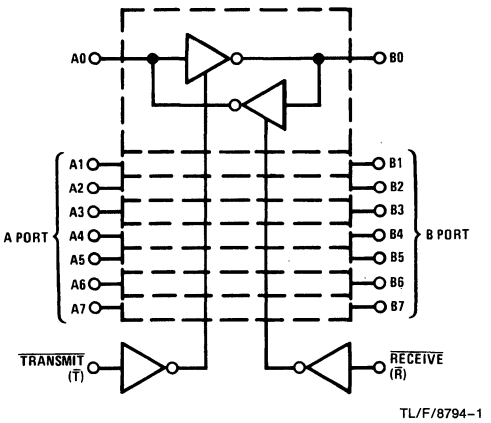
The DP8307A is a high speed Schottky 8-bit TRI-STATE bidirectional transceiver designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, it features glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8303A and DP7304B/DP8304B are featured with Transmit/$\overline{\text{Receive}}$ (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP8307A and DP7308/DP8308 is featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high votlage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{\text{T}}$ and $\overline{\text{R}}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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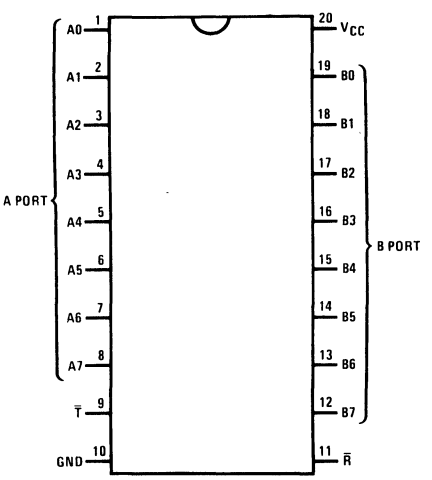
Dual-In-Line Package



TL/F/8794–2

Top View

Order Number DP8307AN
See NS Package Number N20A

Logic Table

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Lead Temperature (soldering, 4 sec.)	260°C
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$				0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IL} = 0.5V$	$I_{OH} = -0.4$ mA	$V_{CC} - 1.15$	$V_{CC} - 0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA		0.35	0.5	V
			$I_{OL} = 8$ mA		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_O = 0V$, V_{CC} = Max, (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V$, V_{CC} = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$				0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IL} = 0.5V$	$I_{OH} = -0.4$ mA	$V_{CC} - 1.15$	$V_{CC} - 0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_O = 0V$, V_{CC} = Max, (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V$, V_{CC} = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 2.0V, V_{CC} = Max			70	100	mA
		$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2V, V_{CC} = Max			100	150	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 30 pF		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 5k, C4 = 30 pF		24	35	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 8	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	23 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 18	40 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (*Figure B*) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		25 16	35 25	ns ns

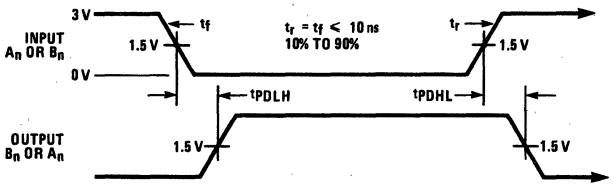
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



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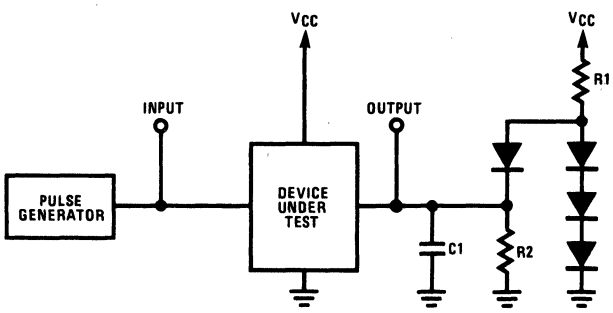

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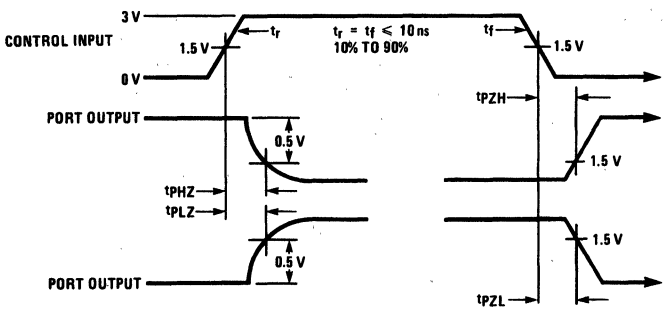
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



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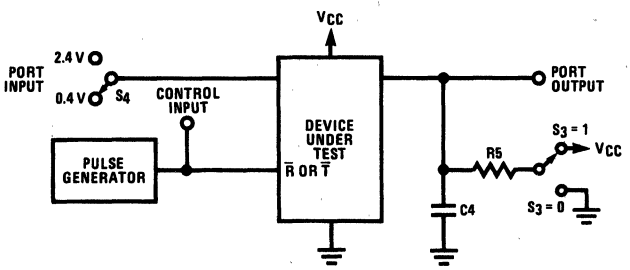

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Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor

DP8308 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

General Description

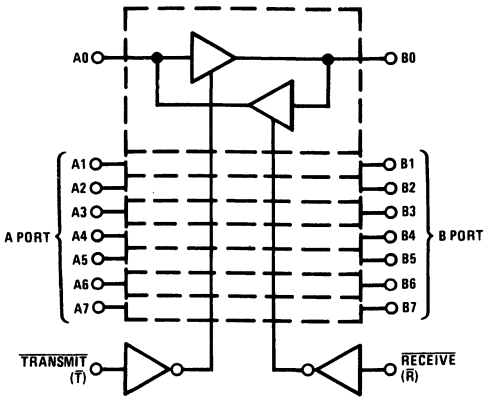
The DP8308 is a high speed Schottky 8-bit TRI-STATE bidirectional transceiver designed to provide bidirectional drive for bus oriented microprocessor and digital communications systems. It is capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, it features glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

DP8308 is featured with $\overline{\text{Transmit}}$ ($\overline{T}$) and $\overline{\text{Receive}}$ ($\overline{R}$) control inputs.

Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



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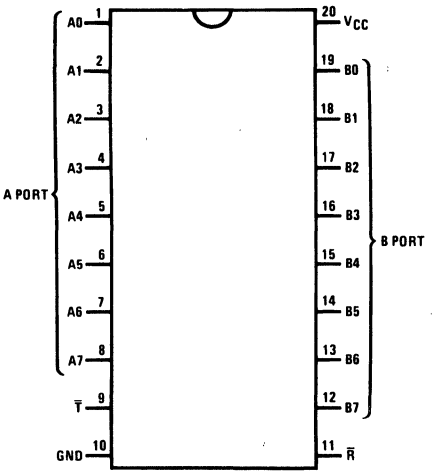
Dual-In-Line Package



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Top View

Order Number DP8308N
See NS Package Number N20A

Logic Table

Control Inputs		Resulting Conditions	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 4 sec.)	260°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7308	4.5	5.5	V
DP8308	4.75	5.25	V
Temperature (T_A)			
DP7308	−55	+125	°C
DP8308	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
A PORT (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA (8308)		0.35	0.5	V
			$I_{OL} = 8$ mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_O = 0V$, V_{CC} = Max (Note 4)		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V$, V_{CC} = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B PORT (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_O = 0V$, V_{CC} = Max (Note 4)		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V$, V_{CC} = Max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

DC Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
CONTROL INPUTS $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8308			0.8	V
			DP7308			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = Max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
POWER SUPPLY CURRENT							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 0.4V, V_{CC} = Max			70	100	mA
		$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2V, V_{CC} = Max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
A PORT DATA/MODE SPECIFICATIONS						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V *(Figure A)* R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 30 pF		24	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V *(Figure B)* S3 = 0, R5 = 5k, C4 = 30 pF		21	30	ns
B PORT DATA/MODE SPECIFICATIONS						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 18 11	 23 18	 ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V *(Figure A)* R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		 16 11	 23 18	 ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		 25 17	 35 25	 ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V *(Figure B)* S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		 24 17	 35 25	 ns ns

AC Electrical Characteristics (Continued)

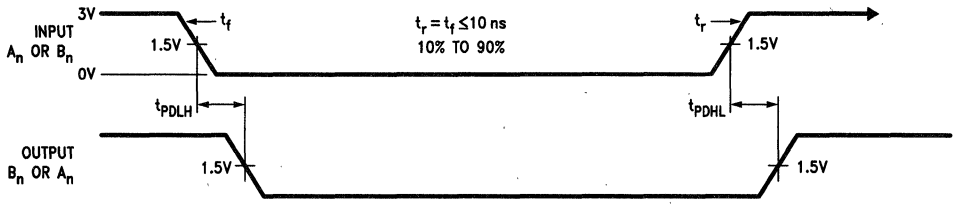
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



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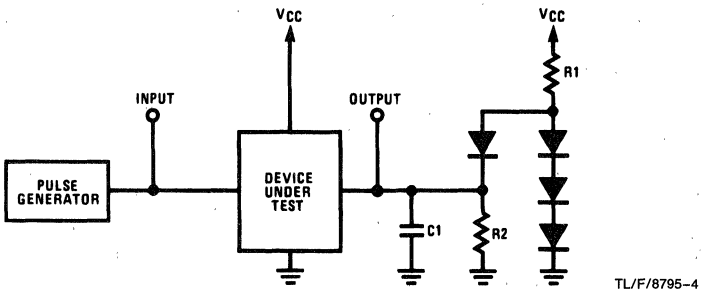

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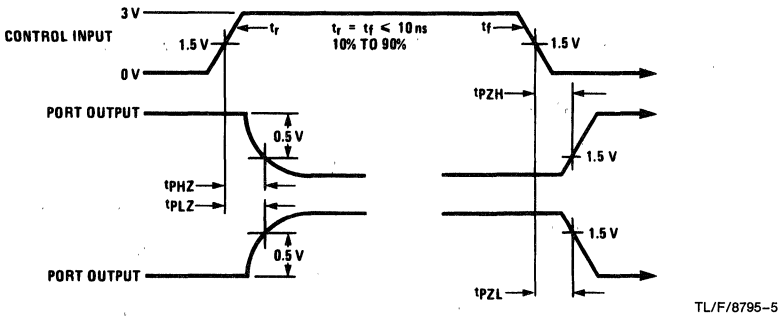
Note: C1 includes test fixture capacitance.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port



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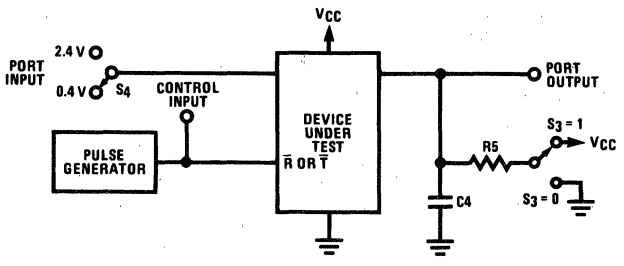

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Note: C4 includes test fixture capacitance. Port input is in a fixed logical condition. See AC Table.

FIGURE B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor

DS26S10C/DS26S10M/DS26S11C/DS26S11M Quad Bus Transceivers

General Description

The DS26S10 and DS26S11 are quad Bus Transceivers consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

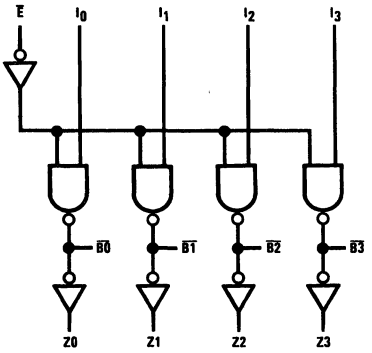
The DS26S10 and DS26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

- Input to bus is inverting on DS26S10
- Input to bus is non-inverting on DS26S11
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic Diagrams

DS26S10



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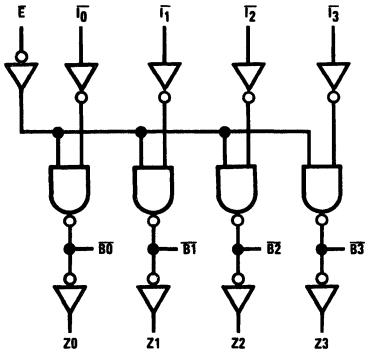
DS26S11



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5 mA

Maximum Power Dissipation* at 25°C

Cavity Package	1433 mW
Molded Package	1362 mW
PLCC Package	TBD mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C, derate PLCC package TBD mW/°C above 25°C.

Operating Conditions

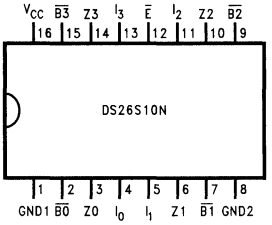
	Min	Max	Units
Supply Voltage (V_{CC})			
DS26S10C, DS26S11C	4.75	5.25	V
DS26S10M, DS26S11M	4.5	5.5	V
Temperature (T_A)			
DS26S10C, DS26S11C	0	+70	°C
DS26S10M, DS26S11M	−55	+125	°C

Electrical Characteristics (Unless otherwise noted)

Symbol	Parameter	Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1 mA, V_{IN} = V_{IL} or V_{IH}	Military	2.5	3.4		V
			Commercial	2.7	3.4		V
V_{OL}	Output Low Voltage (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input High Level (Except Bus)	Guaranteed Input Logical High for All Inputs		2.0			V
V_{IL}	Input Low Level (Except Bus)	Guaranteed Input Logical Low for All Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 2.7V	Enable			20	μA
			Data			30	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = Max, (Note 3)	Military	−20		−55	mA
			Commercial	−18		−60	mA
I_{CCL}	Power Supply Current (All Bus Outputs Low)	V_{CC} = Max, Enable = GND	DS26S10		45	70	mA
			DS26S11			80	mA

Connection Diagrams

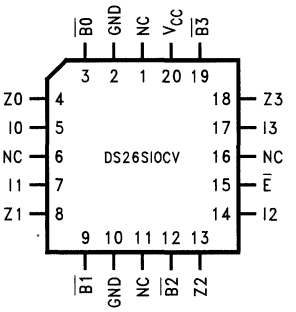
Dual-In-Line Package



TL/F/5802–3

Top View
Order Number DS26S10CJ, DS26S10MJ or DS26S10CN
See NS Package Number J16A or N16A

Plastic Chip Carrier

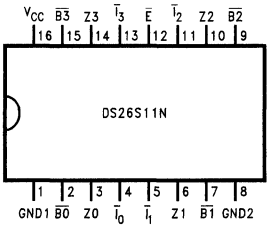


TL/F/5802–12

Top View

Order Number DS26S10CV
See NS Package Number V20A

Dual-In-Line Package



TL/F/5802–4

Top View
Order Number DS26S11CJ, DS26S11MJ or DS26S11CN
See NS Package Number J16A or N16A

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Bus Input/Output Characteristics

Symbol	Parameter	Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OL}	Output Low Voltage	V_{CC} = Min	Military	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Commercial	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8V			−50	μA
			Military	V_O = 4.5V			200	
			Commercial	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4V, V_{CC} = Max		Military	2.4	2.0		V
				Commercial	2.25	2.0		
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4V, V_{CC} = Min		Military		2.0	1.6	V
				Commercial		2.0	1.75	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{PLH}	Data Input to Bus	R_B = 50Ω, C_B = 50 pF (Note 1)	DS26S10		10	15	ns
t_{PHL}	Data Input to Bus				10	15	ns
t_{PLH}	Data Input to Bus		DS26S11		12	19	ns
t_{PHL}	Data Input to Bus				12	19	ns
t_{PLH}	Enable Input to Bus		DS26S10		14	18	ns
t_{PHL}	Enable Input to Bus				13	18	ns
t_{PLH}	Enable Input to Bus		DS26S11		15	20	ns
t_{PHL}	Enable Input to Bus				14	20	ns
t_{PLH}	Bus to Receiver Out	R_B = 50Ω, R_L = 280Ω, C_B = 50 pF (Note 1), C_L = 15 pF			10	15	ns
t_{PHL}	Bus to Receiver Out				10	15	ns
t_r	Bus	R_B = 50Ω, C_B = 50 pF (Note 1)		4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1: Includes probe and jig capacitance.

Truth Tables

DS26S10

Inputs		Outputs	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

DS26S11

Inputs		Outputs	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

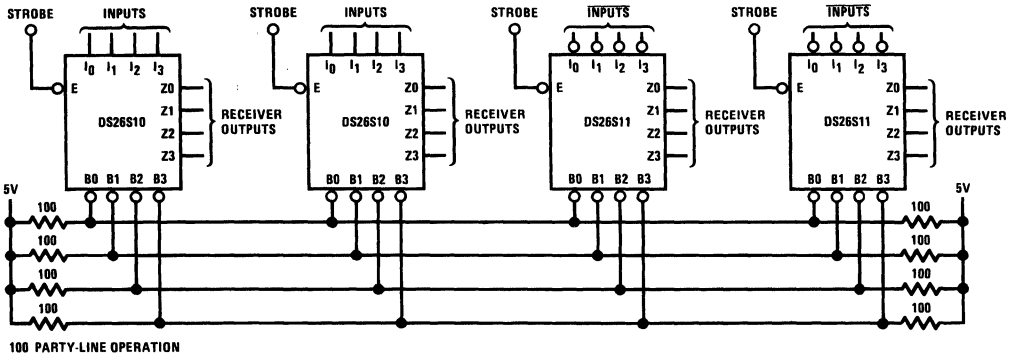
H = High voltage level

L = Low voltage level

X = Don't care

Y = Voltage level of bus (assumes control by another bus transceiver)

Typical Application



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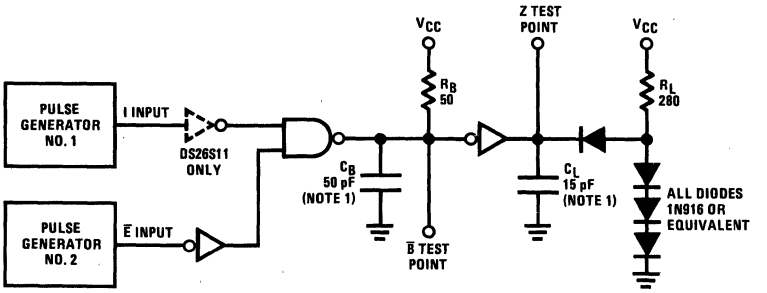
AC Test Circuit and Switching Time Waveforms



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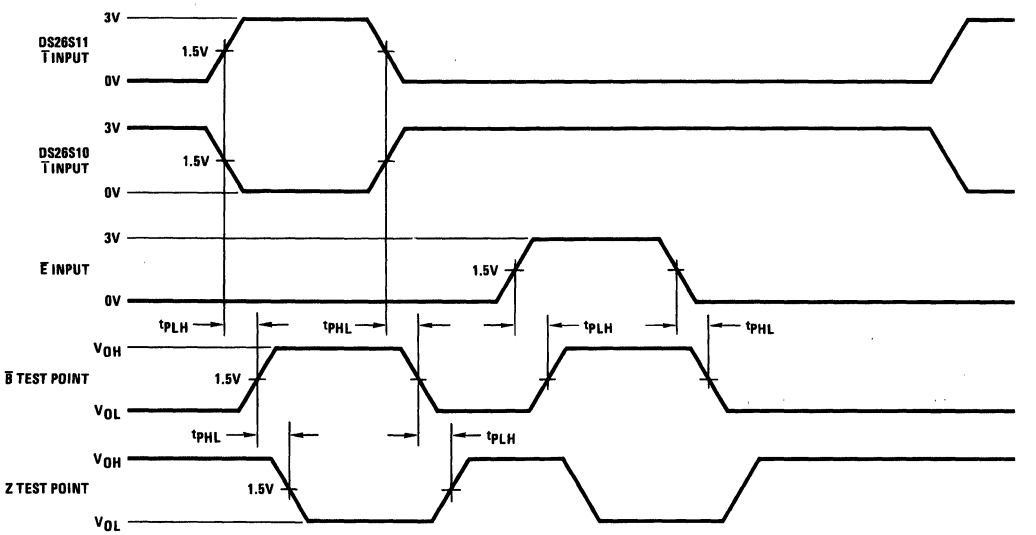
Note 1: Includes probe and jig capacitance.



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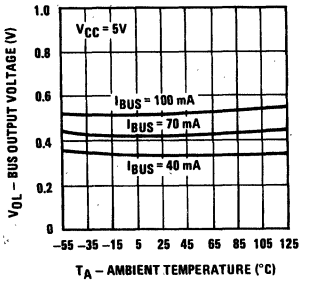
Typical Performance Characteristics

Typical Bus Output Low Voltage vs Ambient Temperature



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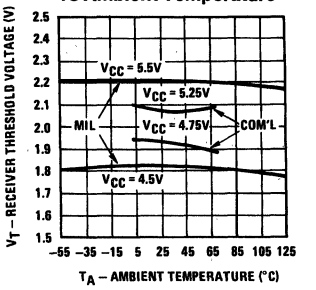
Receiver Threshold Variation vs Ambient Temperature



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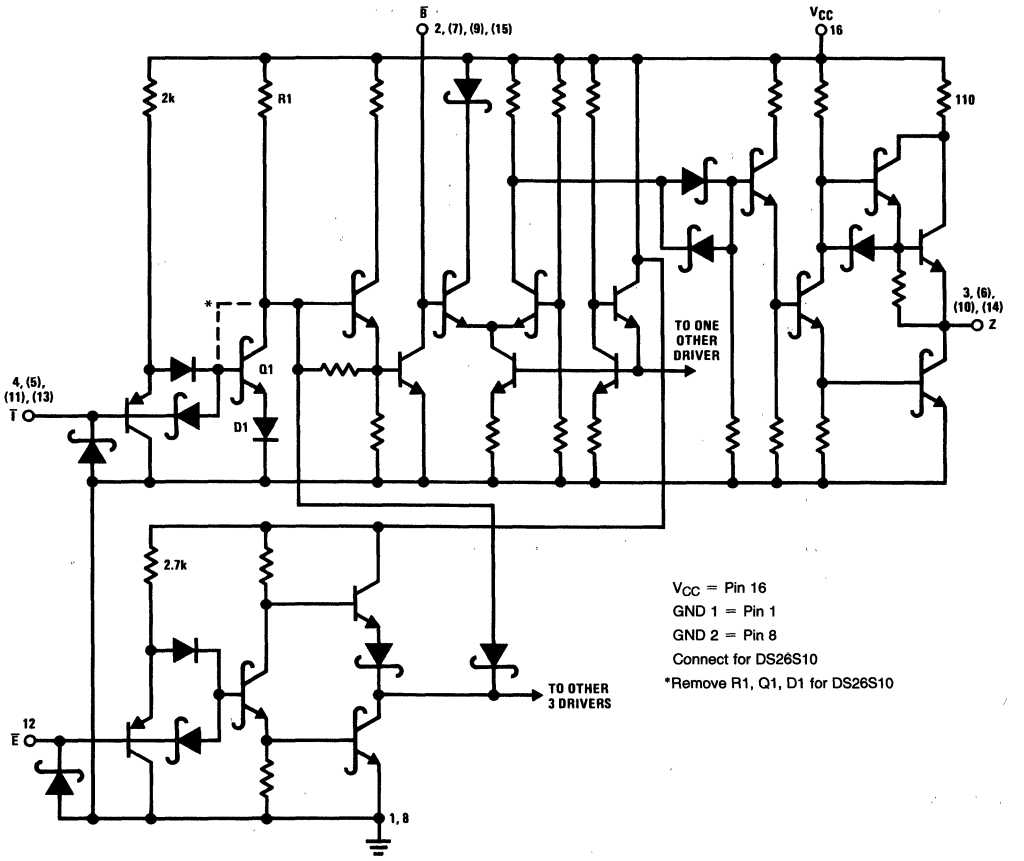
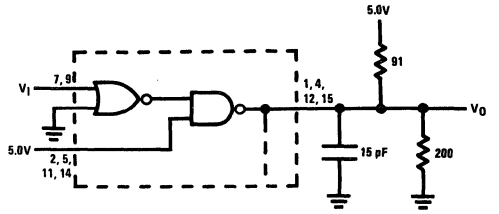
Schematic Diagram



TL/F/5802–10

AC Test Circuits and Switching Waveforms



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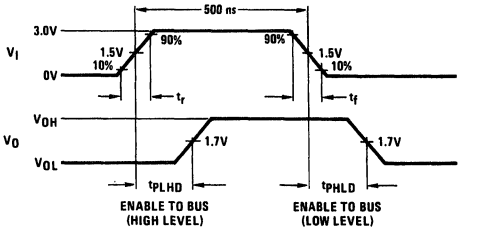
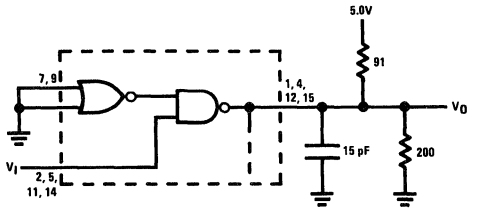


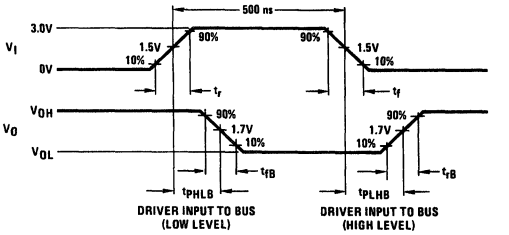
TL/F/5803–3

Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 1. Disable Delays



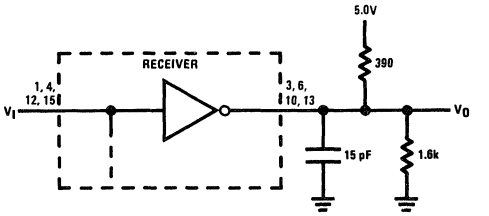
TL/F/5803–4



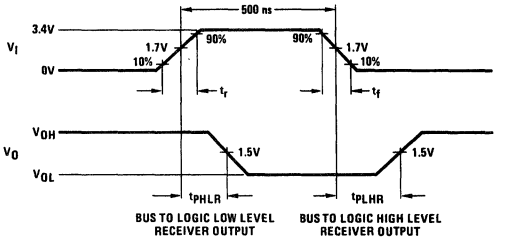
TL/F/5803–5

Note: $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 2. Driver Propagation Delays



TL/F/5803–6



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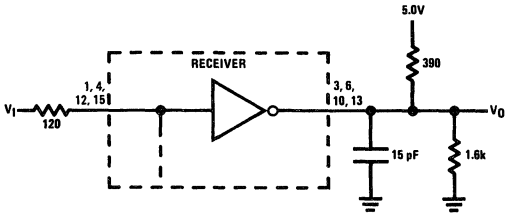
Note: $t_r = t_f = 15$ ns. Pulse width = 500 ns measured between 1.7V levels. f = 1 MHz.

FIGURE 3. Receiver Propagation Delays



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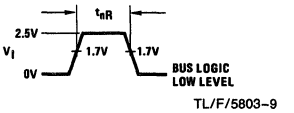

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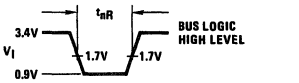
$t_r = t_f = 2.5$ ns

(a) Receiver Output (V_O) to Remain Greater than 2.2V



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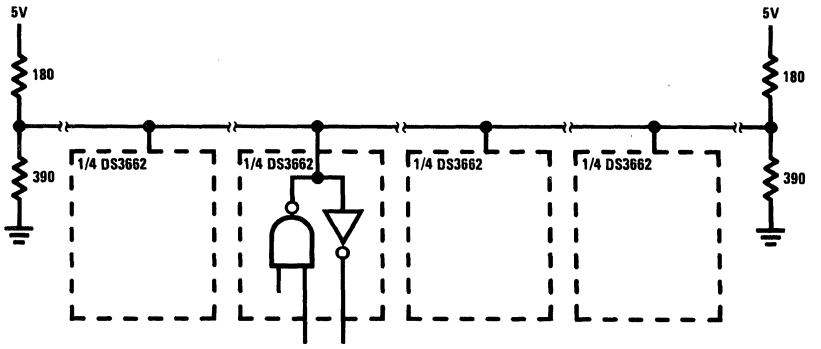
$t_r = t_f = 2.5$ ns

(b) Receiver Output (V_O) to Remain Less than 0.7V

FIGURE 4. Receiver Noise Immunity: "No Response at Output" Input Waveforms

Typical Application

120Ω Unified Data Bus



TL/F/5803–11

National Semiconductor

DS3667 TRI-STATE® Bidirectional Transceiver

General Description

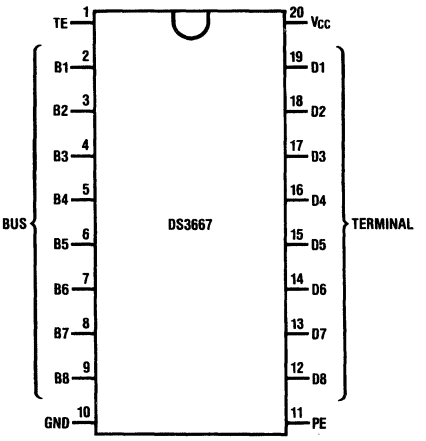
The DS3667 is a high-speed Schottky 8-channel bidirectional transceiver designed for digital information and communication systems. Pin selectable totem-pole/open collector outputs are provided at all driver outputs. This feature, together with the Dumb Mode which puts both driver and receiver outputs in TRI-STATE at the same time, means higher flexibility of system design. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. A power up/down protection circuit is included at all outputs to provide glitch-free operation during V_{CC} power up or down.

Features

- 8-channel bidirectional non-inverting transceivers
- Bidirectional control implemented with TRI-STATE output design
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- Pin selectable totem-pole/open collector outputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- Power up/down protection (glitch-free)
- Dumb Mode capability

Connection Diagram

Dual-In-Line Package



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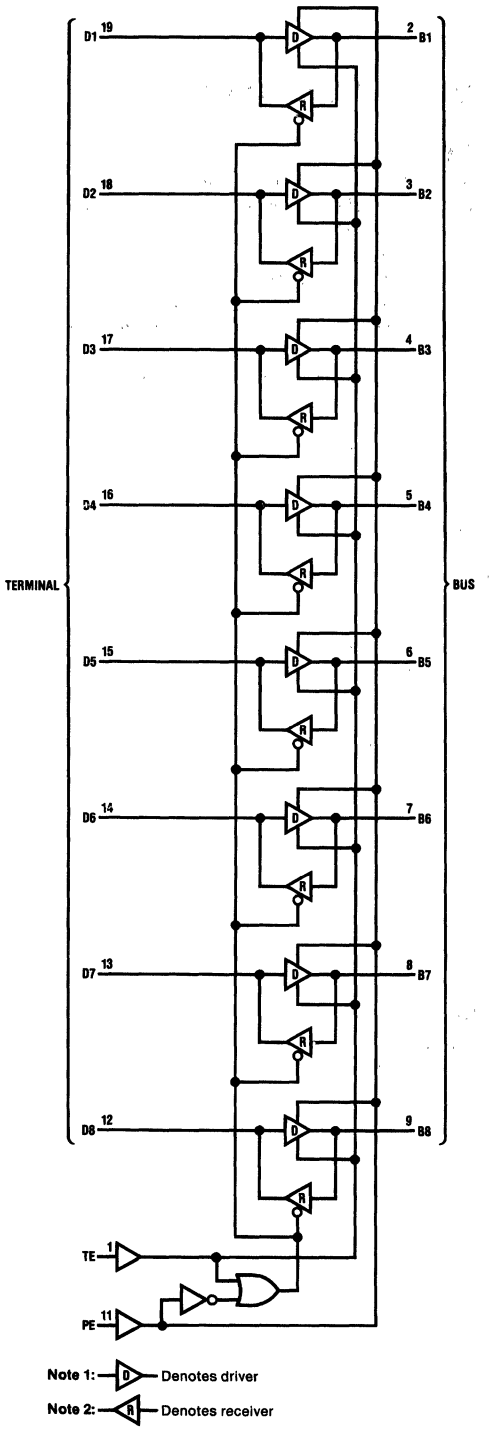
Top View

Order Number DS3667N
See NS Package Number N20A

Logic Diagram



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Functional Truth Table

Control Input Level		Data Transceivers		
TE	PE	Mode	Bus Port	Terminal Port
H	H	T	Totem-Pole Output	Input
H	L	T	Open Collector Output	Input
L	H	R	Input	Output
L	L	D	TRI-STATE	TRI-STATE

H: High Level Input
L: Low Level Input
T: Transmitting Mode
R: Receiving Mode
D: Dumb Mode

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C Molded Package	1832 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		I_I = −18 mA		−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus		400	500		mV
V_{OH}	High Level Output Voltage	Terminal	I_{OH} = −800 μA	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA	2.5	3.4		
V_{OL}	Low Level Output Voltage	Terminal	I_{OL} = 16 mA		0.3	0.5	V
		Bus	I_{OL} = 48 mA		0.4	0.5	
I_{IH}	High Level Input Current	TE, PE	V_I = 5.5V		0.2	100	μA
			V_I = 2.7V		0.1	20	
		Terminal and Bus	V_I = 4V			200	
I_{IL}	Low Level Input Current	Terminal and TE, PE	V_I = 0.5V		−10	−100	μA
		Bus			−0.4	−1.0	mA
I_{OS}	Short Circuit Output Current	Terminal	V_I = 2V, V_O = 0V (Note 4)	−15	−35	−75	mA
		Bus		−50	−120	−200	
I_{CC}	Supply Current		Transmit, TE = 2V, PE = 2V, V_I = 0.8V		75	100	mA
			Receive, TE = 0.8V, PE = 2V, V_I = 0.8V		65	90	
C_{IN}	Bus-Port Capacitance	Bus	V_{CC} = 0V, V_I = 0V, f = 10 kHz (Note 5)		20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operations.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This parameter is guaranteed by design. It is not a tested parameter.

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C (Note 1)

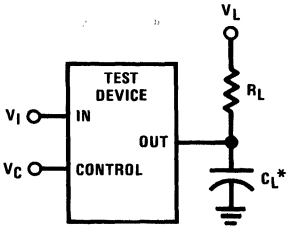
Symbol	Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V R_L = 38.3Ω C_L = 30 pF *(Figure 1)*		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V R_L = 240Ω C_L = 30 pF *(Figure 2)*		15	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20	ns
t_{PZH}	Output Enable Time to High Level	TE (Notes 2 and 3)	Bus	V_I = 3.0V V_L = 0V R_L = 480Ω C_L = 15 pF *(Figure 1)*		19	30	ns
t_{PHZ}	Output Disable Time to High Level					15	20	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V V_L = 2.3V R_L = 38.3Ω C_L = 15 pF *(Figure 1)*		24	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Enable Time to High Level	TE, PE (Notes 2 and 3)	Terminal	V_I = 3.0V V_L = 0V R_L = 3 kΩ C_L = 15 pF *(Figure 1)*		19	35	ns
t_{PHZ}	Output Disable Time to High Level					17	25	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V V_L = 5V R_L = 280Ω C_L = 15 pF *(Figure 1)*		27	40	ns
t_{PLZ}	Output Disable Time to Low Level					17	30	ns
t_{PZH}	Output Pull-Up Enable Time	PE (Notes 2 and 3)	Bus	V_I = 3V V_L = 0V R_L = 480Ω C_L = 15 pF *(Figure 1)*		10	20	ns
t_{PHZ}	Output Pull-Up Disable Time					10	20	ns

Note 1: All typical values are for T_A = 25°C, V_{CC} = 5V.

Note 2: Refer to Functional Truth Table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations



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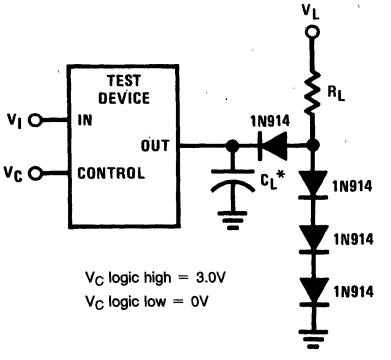
V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



V_C logic high = 3.0V
V_C logic low = 0V

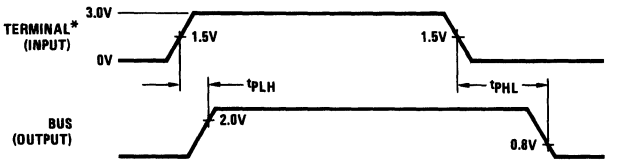
TL/F/5245–4

*C_L includes jig and probe capacitance

FIGURE 2

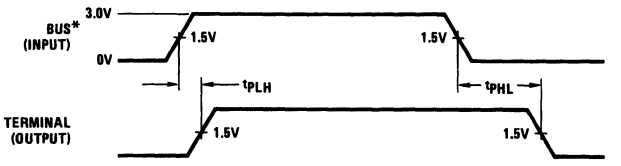
Switching Waveforms

Transmit Propagation Delays



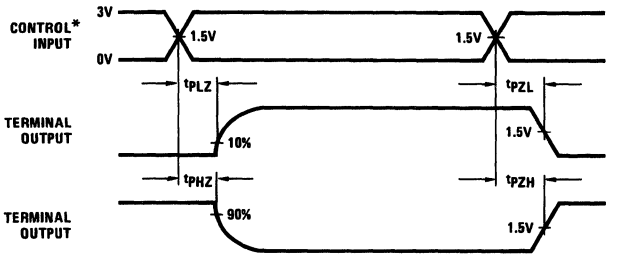
TL/F/5245–5

Receive Propagation Delays



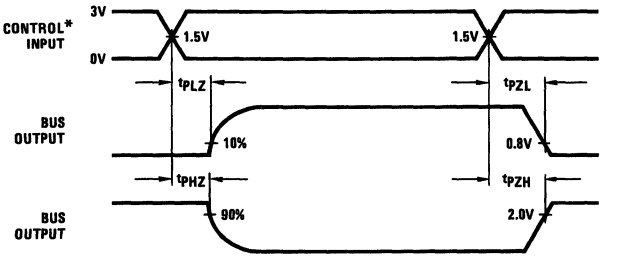
TL/F/5245–6

Terminal Enable/Disable Times



TL/F/5245–7

Bus Enable/Disable Times



TL/F/5245–8

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

National Semiconductor

DS3862 Octal High Speed Trapezoidal Bus Transceiver

General Description

The DS3862 is an octal high speed schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 9 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

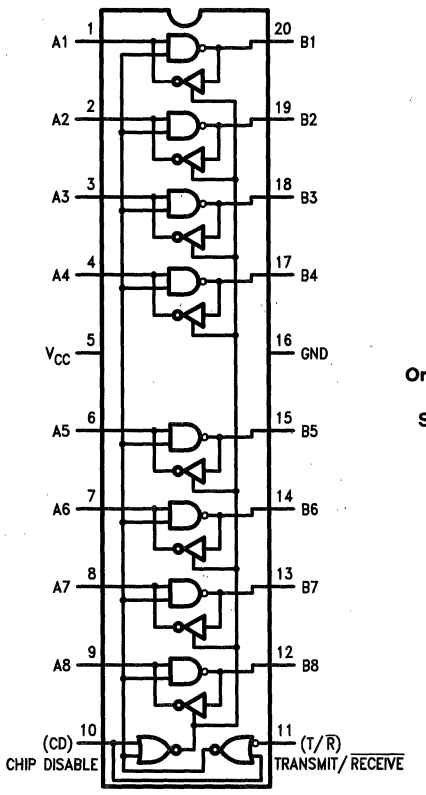
The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends.

Features

- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level and respond symmetrically to positive and negative going pulses
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs, and receiver outputs
- Control logic is the same as the DS3896

Logic and Connection Diagram

DS3862



TL/F/8539–1

Order Number DS3862J, DS3862N or DS3862WM
See NS Package Number J20A, N20A or M20B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	5.5V
Power Dissipation	1400 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs:						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	An = V_{CC}			1	mA
I_{IH}	Logical "1" Input Current	An = 2.4V			40	μA
I_{IHC}	Logical "1" Input Current	CD = $T/\overline{R}$ = 2.4V			80	μA
I_{IL}	Logical "0" Input Current	An = 0.4V		−1	−1.6	mA
I_{ILC}	CD & $T/\overline{R}$ Logical "0" Input Current	CD = $T/\overline{R}$ = 0.4V		−180	−400	μA
V_{CL}	Input Diode Clamp Voltage	Iclamp = −12 mA		−0.9	−1.5	V
Driver Output/Receiver Input						
V_{OLB}	Low Level Bus Voltage	An = $T/\overline{R}$ = 2V, Ibus = 100 mA		0.6	0.9	V
I_{IHB}	Logical "1" Bus Current	An = 0.8V, Bn = 4V, V_{CC} = 5.25V and 0V		10	100	μA
I_{ILB}	Logical "0" Bus Current	An = 0.8V, Bn = 0V, V_{CC} = 5.25V and 0V			100	μA
V_{TH}	Input Threshold	V_{CC} = 5V	1.5	1.7	1.9	V
Receiver Output						
V_{OH}	Logical "1" Output Voltage	Bn = 0.9V, I_{oh} = −400μA	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	Bn = 4V, I_{ol} = 16 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	Bn = 0.9V	−20	−70	−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V		90	135	mA

Note 1: "Absolute Maximum Ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that device should be operated at these limits. The table of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

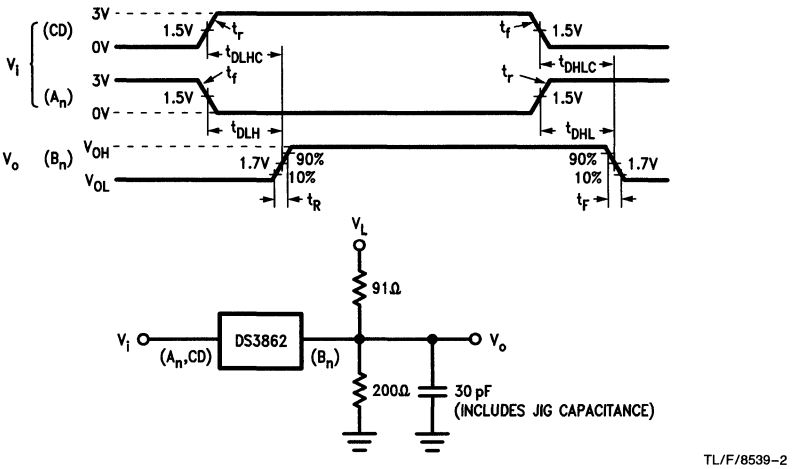
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

Switching Characteristics $0°C \le T_A \le 70°C$, $4.75V \le V_{CC} \le 5.25V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t_{DLH}	An to Bn	CD = 0.8V, T/$\overline{R}$ = 2.0V, VL = 5V (*Figure 1*)		12	20	ns
t_{DHL}				12	20	ns
t_{DLHC}	CD to Bn	An = T/$\overline{R}$ = 2.0V, VL = 5V, (*Figure 1*)		12	20	ns
t_{DHLC}				15	25	ns
t_{DLHT}	T/$\overline{R}$ to Bn	VCI = An, VC = 5V, (*Figure 2*) CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 91Ω, RL2 = 200Ω, VL = 5V		20	30	ns
t_{DHLT}				25	40	ns
t_R	Driver Output Rise Time	CD = 0.8V, T/$\overline{R}$ = 2V, VL = 5V (*Figure 1*)	4	9	20	ns
t_F	Driver Output Fall Time		4	9	20	ns
Receiver:						
t_{RLH}	Bn to An	CD = 0.8V, T/$\overline{R}$ = 0.8V (*Figure 3*)		15	25	ns
t_{RHL}				15	25	ns
t_{RLZC}	CD to An	Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 5 pF RL1 = 390Ω, RL2 = NC, VL = 5V (*Figure 4*)		15	25	ns
t_{RZLC}		Bn = 2.0V, T/$\overline{R}$ = 0.8V, CL = 30 pF RL1 = 390Ω, RL2 = 1.6K, VL = 5V (*Figure 4*)		10	20	ns
t_{RHZC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 4*)		5	10	ns
t_{RZHC}		Bn = 0.8V, T/$\overline{R}$ = 0.8V, VL = 0V, RL1 = NC, RL2 = 1.6K, CL = 30 pF (*Figure 4*)		8	15	ns
t_{RLZT}	T/$\overline{R}$ to An	VCI = Bn, VC = 3.4V, RC = 39Ω CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 2*)		20	30	ns
t_{RZLT}		VCI = Bn, VC = 3.4V, RC = 39Ω, CD = 0.8V, VL = 5V, RL1 = 390Ω, RL2 = 1.6K, CL = 30 pF (*Figure 2*)		30	45	ns
t_{RHZT}		VCI = Bn, VC = 0V, RC = 39Ω CD = 0.8V, VL = 0V, RL1 = 390Ω, RL2 = NC, CL = 5 pF (*Figure 2*)		5	10	ns
t_{RZHT}		VCI = Bn, VC = 0V, RC = 39Ω, CD = 0.8V, VL = 0V, RL1 = NC RL2 = 1.6K, CL = 30 pF (*Figure 2*)		10	20	ns
t_{NR}	Receiver Noise Rejection Pulse Width	(*Figure 5*)	9	12		ns

Note: NC means open

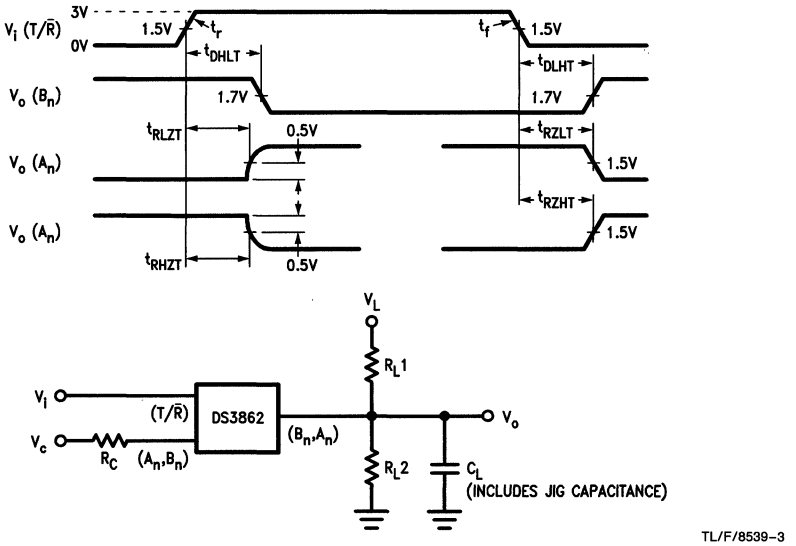
Switching Waveforms



TL/F/8539–2

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 1. Driver Propagation Delays

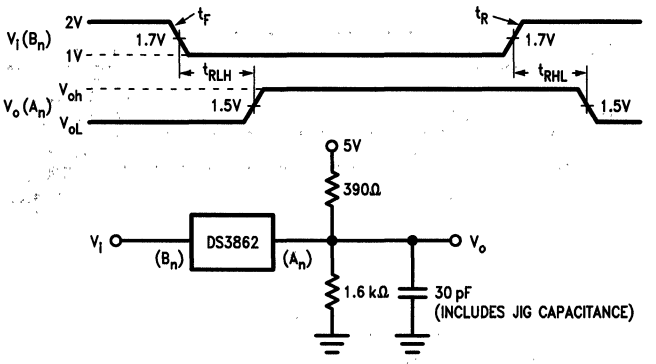


TL/F/8539–3

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 2. Propagation Delay From T/$\overline{R}$ Pin to An or Bn.

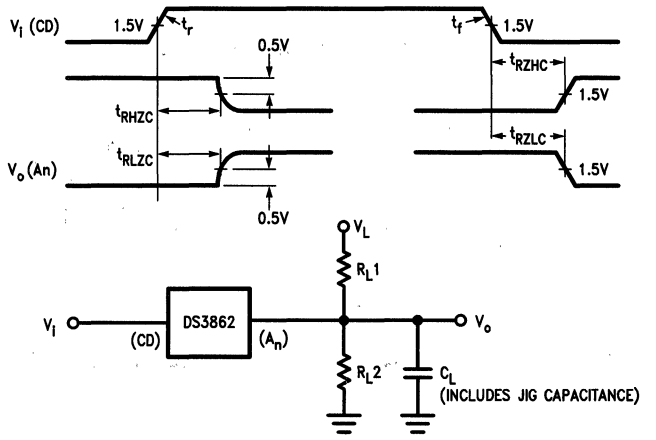
Switching Waveforms (Continued)



TL/F/8539–4

Note: $t_R = t_F \leq 10$ ns from 10% to 90%

FIGURE 3. Receiver Propagation Delays

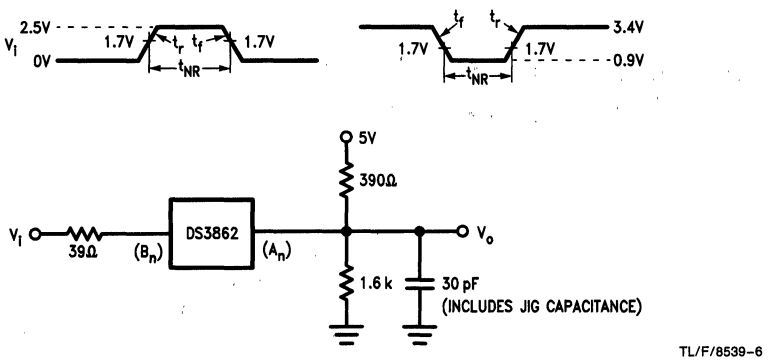


TL/F/8539–5

Note: $t_r = t_f \leq 5$ ns from 10% to 90%

FIGURE 4. Propagation Delay From CD Pin to An

Switching Waveforms (Continued)

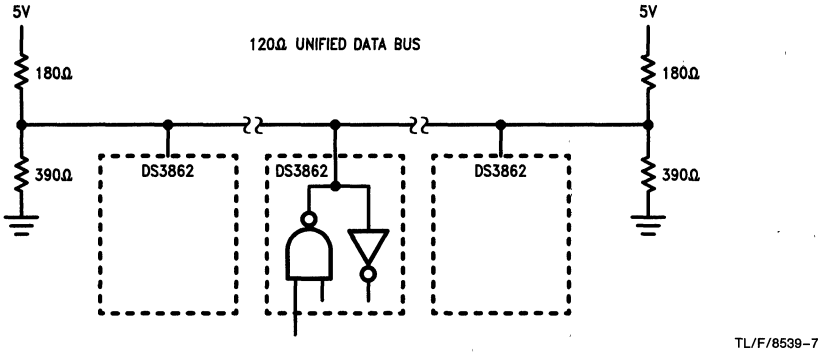


TL/F/8539–6

Note: $t_r = t_f = 2$ ns from 10% to 90%

FIGURE 5. Receiver Noise Immunity: No Response at Output Input Waveform.

Typical Application



TL/F/8539–7

National Semiconductor

DS75160A/DS75161A/DS75162A IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed.

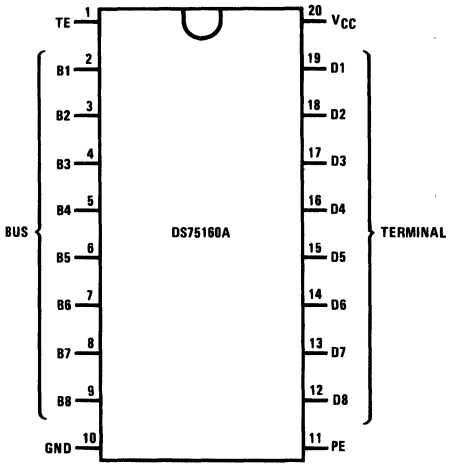
The General Purpose Interface Bus is comprised of 16 signal lines — 8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system, or with DS75162A in a multi-controller system.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Pin selectable open collector mode on DS75160A driver outputs
- Accommodates multi-controller systems

Connection Diagrams

Dual-In-Line Package

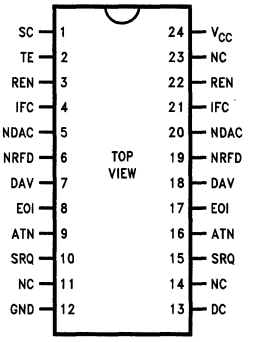


TL/F/5804–1

Top View

Order Number DS75160AN or DS75160AWM
See NS Package Number M20B or N20A

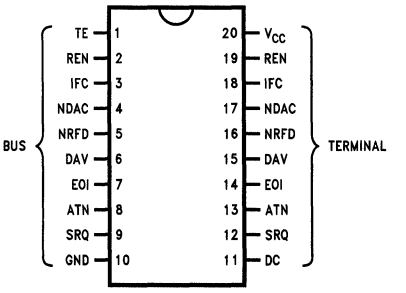
Dual-In-Line Package



TL/F/5804–15

Order Number DS75162AWM, DS75162AN
See NS Package Number M24B or N24B

Dual In-Line Package



TL/F/5804–16

Order Number DS75161AN or DS75161AWM
See NS Package Number M20B or N20B

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C
Maximum Power Dissipation* at 25°C Molded Package	1897 mW

*Derate molded package 15.2 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	$I_{OH} = -800\ \mu A$		2.7	3.5		V
		Bus (Note 5)	$I_{OH} = -5.2$ mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OH} = 48$ mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and TE, PE, DC, SC Inputs	$V_I = 5.5V$			0.2	100	μA
			$V_I = 2.7V$			0.1	20	
I_{IL}	Low-Level Input Current		$V_I = 0.5V$			−10	−100	μA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)} = 0$ (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)} = -1.5V$ to 0.4V	−1.3			mA
				$V_{I(bus)} = 0.4V$ to 2.5V	0		−3.2	
				$V_{I(bus)} = 2.5V$ to 3.7V			2.5 −3.2	
				$V_{I(bus)} = 3.7V$ to 5V	0		2.5	
				$V_{I(bus)} = 5V$ to 5.5V	0.7		2.5	
			$V_{CC} = 0V$, $V_{I(bus)} = 0V$ to 2.5V				40	μA
I_{OS}	Short-Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)		−15	−35	−75	mA
		Bus (Note 5)			−35	−75	−150	
I_{CC}	Supply Current	DS75160A	Transmit, TE = 2V, PE = 2V, $V_I = 0.8V$			85	125	mA
			Receive, TE = 0.8V, PE = 2V, $V_I = 0.8V$			70	100	
		DS75161A	TE = 0.8V, DC = 0.8V, $V_I = 0.8V$			84	125	
		DS75162A	TE = 0.8V, DC = 0.8V, SC = 2V, $V_I = 0.8V$			85	125	
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 5V$ or 0V, $V_I = 0V$ to 2V, f = 1 MHz			20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This characteristic does not apply to outputs on DS75161A and DS75162A that are open collector.

Switching Characteristics V_{CC} = 5.0V ±5%, T_A = 0°C to 70°C (Note 1)

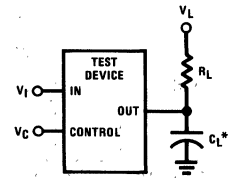
Symbol	Parameter	From	To	Conditions	DS75160A			DS75161A			DS75162A			Units
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	V_L = 2.3V R_L = 38.3Ω C_L = 30 pF *Figure 1*		10	20		10	20		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20		14	20		14	20	ns
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	V_L = 5.0V R_L = 240Ω C_L = 30 pF *Figure 2*		14	20		14	20		14	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20		10	20		10	20	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Bus	V_I = 3.0V V_L = 0V R_L = 480Ω C_L = 15 pF *Figure 1*		19	32		23	40		23	40	ns
t_{PHZ}	Output Disable Time From High Level					15	22		15	25		15	25	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V V_L = 2.3V R_L = 38.3Ω C_L = 15 pF *Figure 1*		24	35		28	48		28	48	ns
t_{PLZ}	Output Disable Time From Low Level					17	25		17	27		17	27	ns
t_{PZH}	Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Terminal	V_I = 3.0V V_L = 0V R_L = 3 kΩ C_L = 15 pF *Figure 1*		17	33		18	40		18	40	ns
t_{PHZ}	Output Disable Time From High Level					15	25		22	33		22	33	ns
t_{PZL}	Output Enable Time to Low Level			V_I = 0V V_L = 5V R_L = 280Ω C_L = 15 pF *Figure 1*		25	39		28	52		28	52	ns
t_{PLZ}	Output Disable Time From Low Level					15	27		20	35		20	35	ns
t_{PZH}	Output Pull-Up Enable Time (DS75160A Only)	PE (Note 2)	Bus	V_I = 3V V_L = 0V R_L = 480Ω C_L = 15 pF *Figure 1*		10	17		NA			NA		ns
t_{PHZ}	Output Pull-Up Disable Time (DS75160A Only)					10	15		NA			NA		ns

Note 1: Typical values are for V_{CC} = 5.0V and T_A = 25°C and are meant for reference only.

Note 2: Refer to Functional Truth Tables for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations

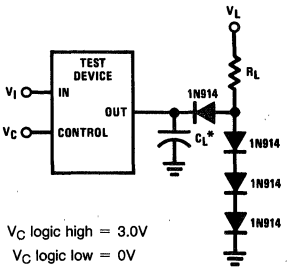


TL/F/5804–8

V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



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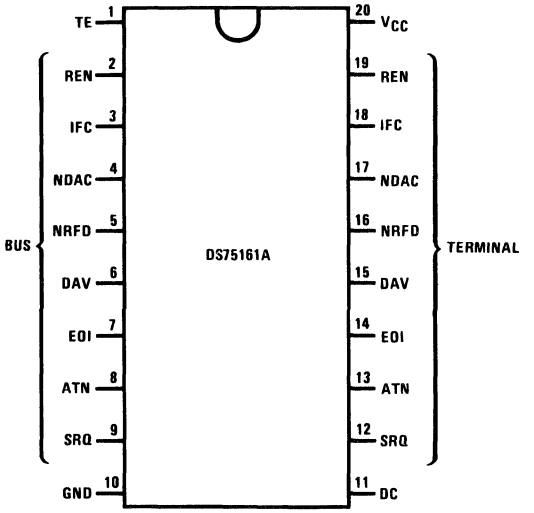
V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 2

Connection Diagrams (Continued)

Dual-In-Line Package



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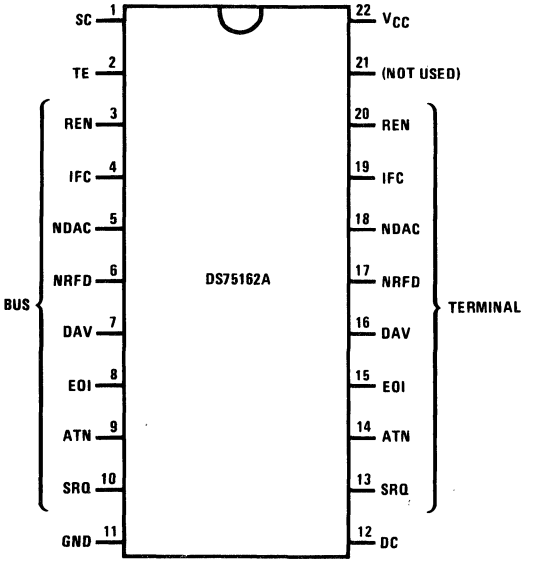
Top View

Dual-In-Line Package



TL/F/5804–3

Top View

Order Number DS75161AN, DS75162AN or DS75161AWM
See NS Package Number M20B, N20A or N22A

Functional Description

DS75160A

This device is an 8-channel bi-directional transceiver with one common direction control input, denoted TE. When used to implement the IEEE-488 bus, this device is connected to the eight data bus lines, designated DIO_1–DIO_8. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when V_{CC} = 0V. The bus port outputs also have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When this control input, denoted PE, is in the high state, the bus outputs operate in the high-speed totem-pole mode. When PE is in the low state, the bus outputs operate as open collector outputs which are necessary for parallel polling.

DS75161A

This device is also an 8-channel bi-directional transceiver which is specifically configured to implement the eight management signal lines of the IEEE-488 bus. This device, paired with the DS75160A, forms the complete 16-line interface between the IEEE-488 bus and a single controller instrumentation system. In compliance with the system organization of the management signal lines, the SRQ, NDAC, and NRFD bus port outputs are open collector. In contrast to the DS75160A, these open collector outputs are a fixed configuration. The direction control is divided into three groups. The DAV, NDAC, and NRFD transceiver directions are controlled by the TE input. The ATN, SRQ, REN, and IFC transceiver directions are controlled by the DC input. The EOI transceiver direction is a function of both the TE and DC inputs, as well as the logic level present on the ATN channel. The port connections to the bus lines have internal terminators identical to the DS75160A.

DS75162A

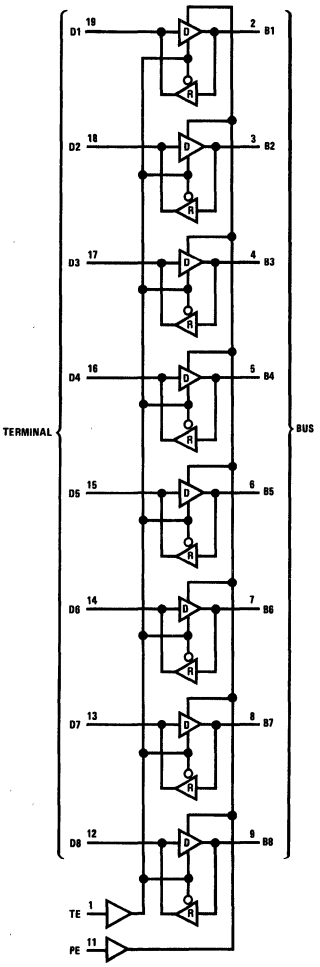
This device is identical to the DS75161A, except that an additional direction control input is provided, denoted SC. The SC input controls the direction of the REN and IFC transceivers that are normally controlled by the DC input on the DS75161A. This additional control function is instrumental in implementing multiple controller systems.

Table of Signal Line Abbreviations

Signal Line Classification	Mnemonic	Definition	Device
Control Signals	DC	Direction Control	DS75161A/ DS75162A
	PE	Pull-Up Enable	DS75160A
	TE	Talk Enable	All
	SC	System Controller	DS75162A
Data I/O Ports	B1–B8	Bus Side of Device	DS75160A
	D1–D8	Terminal Side of Device	
Management Signals	ATN	Attention	DS75161A/ DS75162A
	DAV	Data Valid	
	EOI	End or Identify	
	IFC	Interface Clear	
	NDAC	Not Data Accepted	
	NRFD	Not Ready for Data	
	REN	Remote Enable	
	SRQ	Service Request	

Logic Diagrams

DS75160A



Note 1: D Denotes driver

Note 2: R Denotes receiver

Note 3: Driver and receiver outputs are totem-pole configurations

Note 4: The driver outputs of DS75160A can have their active pull-ups disabled by switching the PE input (pin 11) to the logic low state. This mode configures the outputs as open collector.

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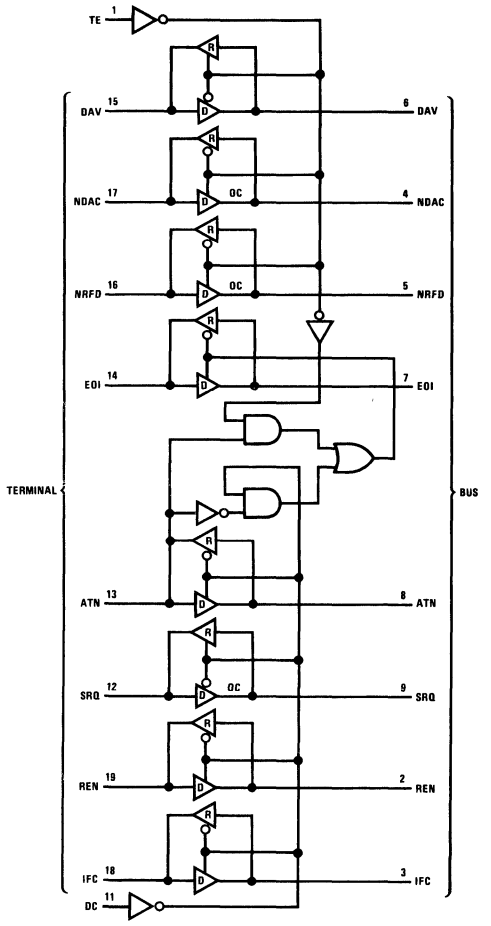
Logic Diagrams (Continued)

DS75161A



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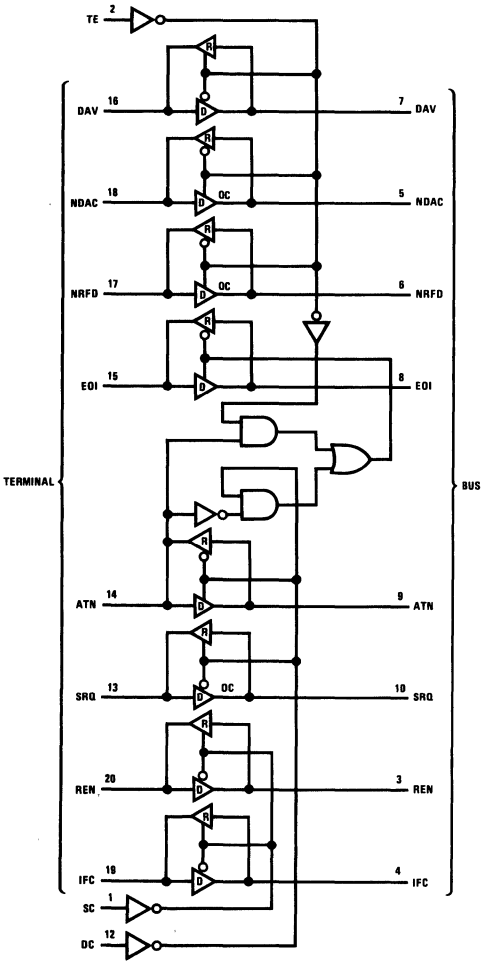
DS75162A



TL/F/5804–6

Note 1: Denotes driver

Note 2: Denotes receiver

Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

TL/F/5804–7

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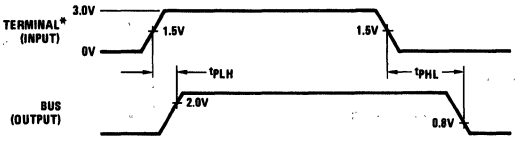
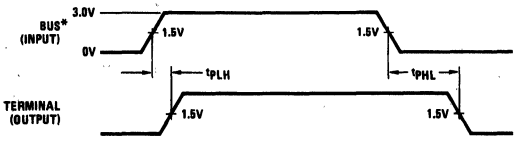
Switching Waveforms

Transmit Propagation Delays



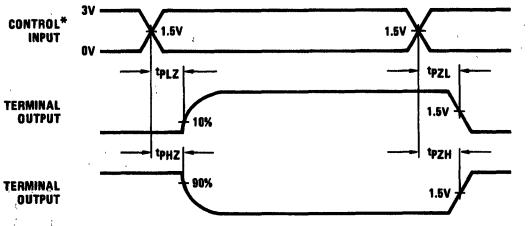
TL/F/5804–10

Receive Propagation Delays



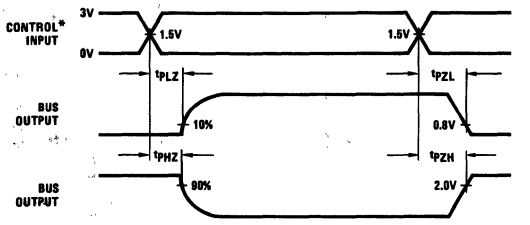
TL/F/5804–11

Terminal Enable/Disable Times



TL/F/5804–12

Bus Enable/Disable Times

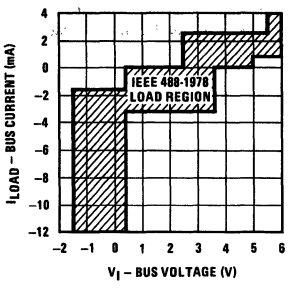


TL/F/5804–13

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

Bus Port Load Characteristics



TL/F/5804–14

Refer to Electrical Characteristics table

Functional Truth Tables

DS75160A

Control Input Level		Data Transceivers	
TE	**PE**	**Direction**	**Bus Port Configuration**
H	H	T	Totem-Pole Output
H	L	T	Open Collector Output
L	X	R	Input

DS75161A

Control Input Level			Transceiver Signal Direction							
TE	**DC**	**ATN***		**EOI**	**REN**	**IFC**	**SRQ**	**NRFD**	**NDAC**	**DAV**
H	H		R		R	R	T	R	R	T
H	L		T		T	T	R	R	R	T
L	H		R		R	R	T	T	T	R
L	L		T		T	T	R	T	T	R
H	X	H		T						
L	X	H		R						
X	H	L		R						
X	L	L		T						

DS75162A

Control Input Level				Transceiver Signal Direction							
SC	**TE**	**DC**	**ATN***		**EOI**	**REN**	**IFC**	**SRQ**	**NRFD**	**NDAC**	**DAV**
H	H	H		R		T	T	T	R	R	T
H	H	L		T		T	T	R	R	R	T
H	L	H		R		T	T	T	T	T	R
H	L	L		T		T	T	R	T	T	R
L	H	H		R		R	R	T	R	R	T
L	H	L		T		R	R	R	R	R	T
L	L	H		R		R	R	T	T	T	R
L	L	L		T		R	R	R	T	T	R
X	H	X	H		T						
X	L	X	H		R						
X	X	H	L		R						
X	X	L	L		T						

H = High level input

L = Low level input

X = Don't care

T = Transmit, i.e., signal outputted to bus

R = Receive, i.e., signal outputted to terminal

*The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic.

National Semiconductor

DS7640/DS8640 Quad NOR Unified Bus Receiver

General Description

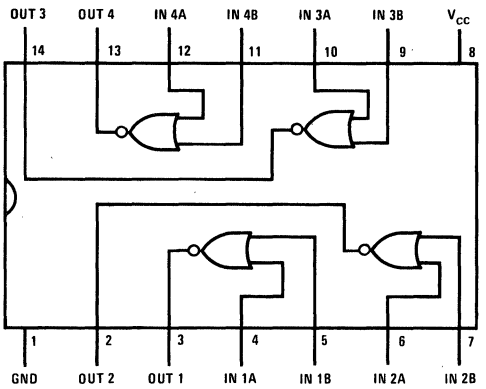
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (30 μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

Connection Diagram

Dual-In-Line Package



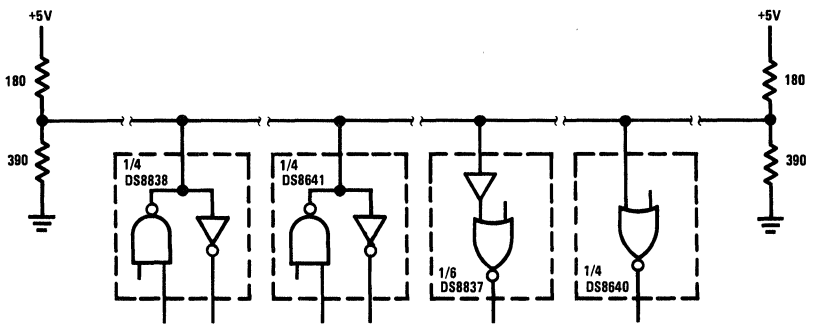
TL/F/5805–1

Top View

Order Number DS7640J or DS8640N
See NS Package Number J14A or N14A

Typical Application

120Ω Unified Data Bus



TL/F/5805–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	μA
			$V_{CC} = 0V$		1.0	50	μA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	μA
V_{OH}	Output Voltage	$I_{OH} = -400\ \mu A$, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply to $V_{CC} = 5V$, $T_A = 25°C$.

National Semiconductor

DS8641 Quad Unified Bus Transceiver

General Description

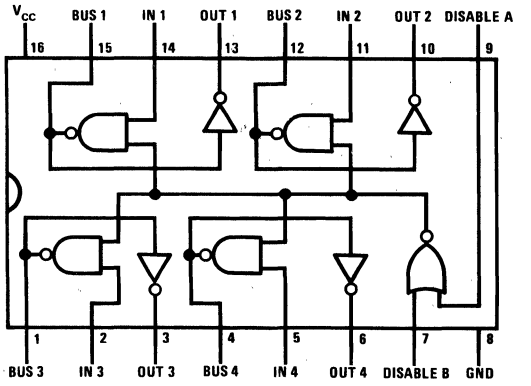
The DS8641 is a quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30 μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Connection Diagram

Dual-In-Line Package



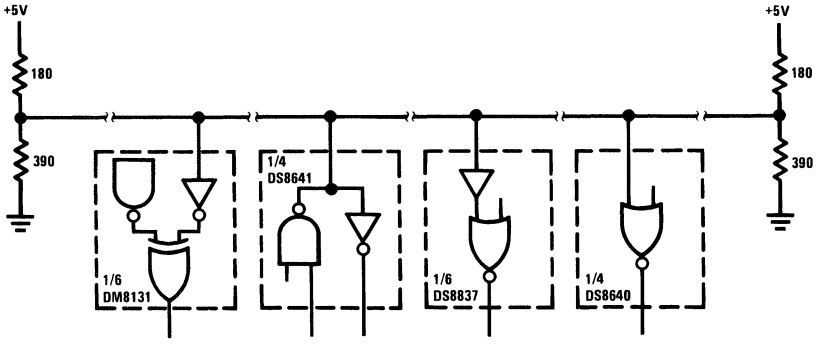
TL/F/5806–1

Top View

Order Number DS8641N
See NS Package Number N16A

Typical Application

120Ω Unified Data Bus



TL/F/5806–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS8641	0	+70	°C

*Derate molded package 10.9 mW/°C above 25°C.

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$			1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$			−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{DIS} = -12$ mA, $I_{IN} = -12$ mA, $I_{BUS} = -12$ mA, $T_A = 25°C$		−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT						
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 50$ mA		0.4	0.7	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = V_{MAX}$		30	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$		2	100	μA
V_{IH}	High Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OL} = 16$ mA	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OH} = -400$ μA		1.50	1.30	V
RECEIVER OUTPUT						
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA	2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA		0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)	−18		−55	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$, (per Package)		50	70	mA

Switching Characteristics $T_A = 25°C$, $V_{CC} = 5V$, unless otherwise indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD}	Propagation Delays (Note 7)	(Note 5)				
	Disable to Bus "1"			19	30	ns
	Disable to Bus "0"			15	30	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			17	25	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8641. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 7: The following apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise specified.

National Semiconductor

DS7833/DS8833/DS7835/DS8835
Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and common inverter receiver disable control.

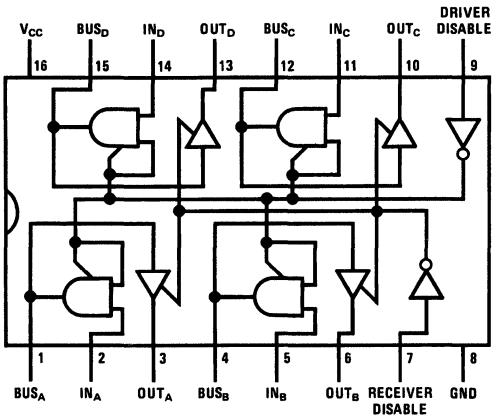
The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

Features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80 μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω DC—terminated buses
- Compatible with Series 54/74

Connection Diagram

Dual-In-Line Package

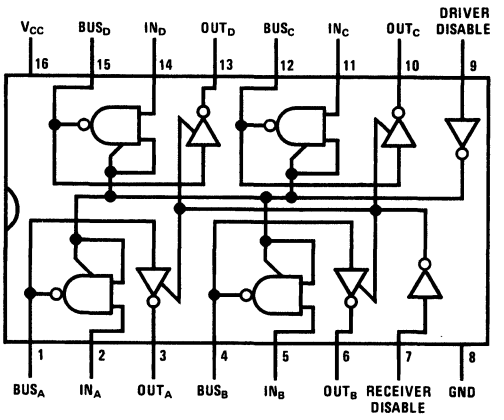


TL/F/5808–1

Top View

Order Number DS7833J or DS8833N
See NS Package Number J16A or N16A

Dual-In-Line Package



TL/F/5808–2

Top View

Order Number DS7835J or DS8835N
See NS Package Number J16A or N16A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 4 sec.)	260°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DS7833/DS7835	4.5	5.5	V
DS8833/DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833/DS7835	−55	+125	°C
DS8833/DS8835	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltages	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min	DS7833, DS8833, DS8835				0.8	V
			DS7835				0.7	
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
I_{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I_S	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V				−2.0	−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OT}	Output Disabled Current	V_{CC} = Max, Disable	V_{OUT} = 2.4V				40	μA
		Inputs = 2.0V	V_{OUT} = 0.4V				−40	μA

Electrical Characteristics (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER OUTPUT (Continued)							
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)	DS7833, DS7835	28	−40	−70	mA
			DS8833, DS8835	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max	DS7833, DS8833		84	116	mA
			DS7835, DS8835		75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7833, DS7835 and across the 0°C to +70°C range for the DS8833, DS8835. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Input	*(Figure 2)*	DS7833/DS8833		24	45	ns
			DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Input	*(Figure 2)*	DS7833/DS8833		12	30	ns
			DS7835/DS8835		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		8.0	20	ns
			Receiver		6.0	15	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		20	35	ns
			Receiver		13	25	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		24	40	ns
			Receiver		16	35	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 5.0 pF, (*Figures 1* and *2*)	Driver		19	35	ns
			Receiver DS7833/DS8833		15	30	ns
			Receiver DS7835/DS8835		33	50	ns

AC Test Circuits

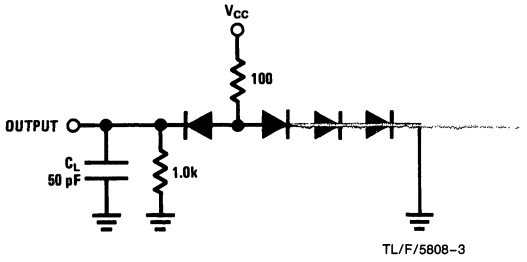

FIGURE 1. Driver Output Load

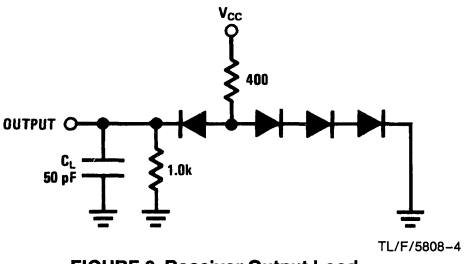

FIGURE 2. Receiver Output Load

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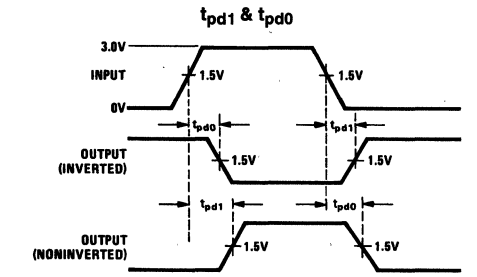
Switching Time Waveforms

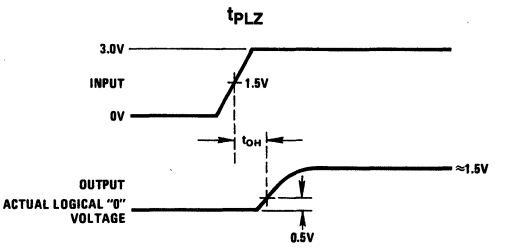


TL/F/5808–5

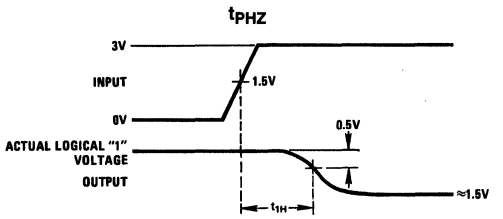
f = 1 MHz

$t_r = t_f \leq 10$ ns (10% to 90%)

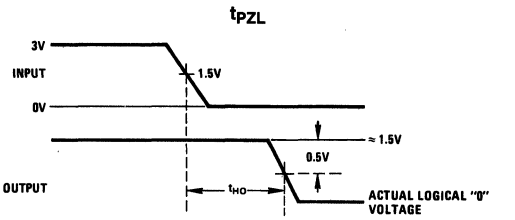
DUTY CYCLE = 50%



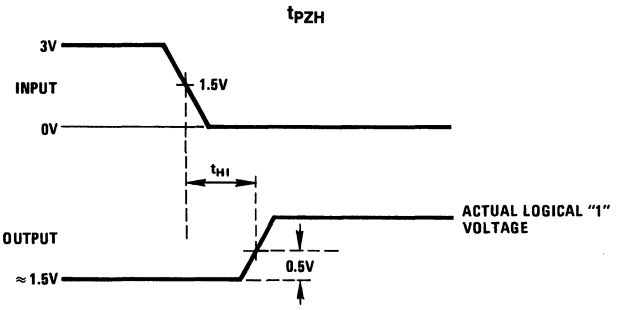
TL/F/5808–6



TL/F/5808–7



TL/F/5808–8



TL/F/5808–9

National Semiconductor

DS7834/DS8834 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated DC or AC, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 employs TTL outputs on the receiver.

The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

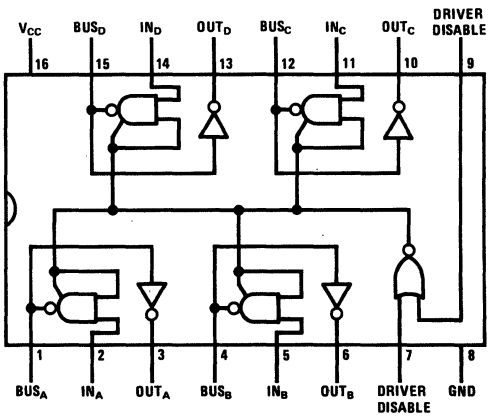
Features

■ Receiver hysteresis	400 mV typ
■ Receiver noise immunity	1.4V typ
■ Bus terminal current for normal V_{CC} or V_{CC} = 0V	80 μA max
■ Receivers	
Sink	16 mA at 0.4V max
Source	2.0 mA (Mil) at 2.4V min
	5.2 mA (Com) at 2.4V min
■ Drivers	
Sink	50 mA at 0.5V max
	32 mA at 0.4V max
Source	10.4 mA (Com) at 2.4V min
	5.2 mA (Mil) at 2.4V min

- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100Ω DC-terminated Buses
- Compatible with Series 54/74

Connection Diagram

Dual-In-Line Package



TL/F/5809–1

Top View

Order Number DS7834J, or DS8834N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7834	4.5	5.5	V
DS8834	4.75	5.25	V
Temperature (T_A)			
DS7834	−55	+125	°C
DS8834	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IND}	Driver Diasbled Input Low Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage	V_{CC} = Max		DS7834	1.4	1.75	2.1	V
				DS8834	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage	V_{CC} = Min		DS7834	0.8	1.35	1.6	V
				DS8834	0.8	1.35	1.5	V
I_{BH}	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max, Disable Input = 2.0V			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{SUS} = 0.4V, Disable Input = 2.0V					−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7834	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS7834	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7834	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8834	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7834	−28	−40	−70	mA
				DS8834	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS7834 and across the 0°C to +70°C range for the DS8834. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

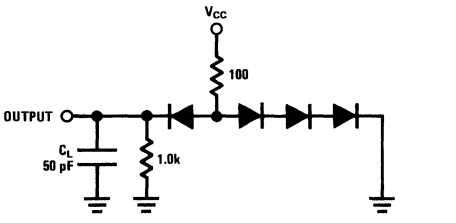
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

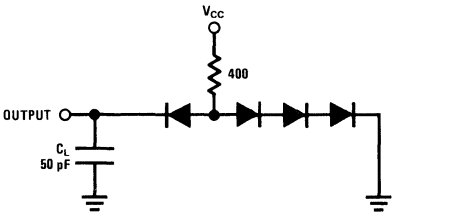
Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7834/DS8834		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7834/DS8834		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Output	*(Figure 2)*	DS7834/DS8834		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Output	*(Figure 2)*	DS7834/DS8834		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1* and *2)* Driver Only			8	20	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1* and *2)* Driver Only			20	35	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1* and *2)* Driver Only			24	40	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1* and *2)* Driver Only			19	35	ns

AC Test Circuit



TL/F/5809–3

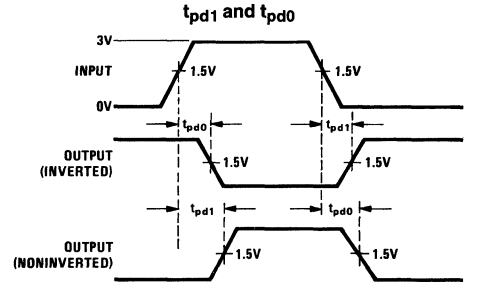
FIGURE 1. Driver Output Load



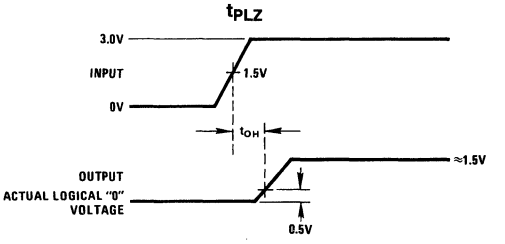
TL/F/5809–4

FIGURE 2. Receiver Output Load

Switching Time Waveforms



TL/F/5809–5



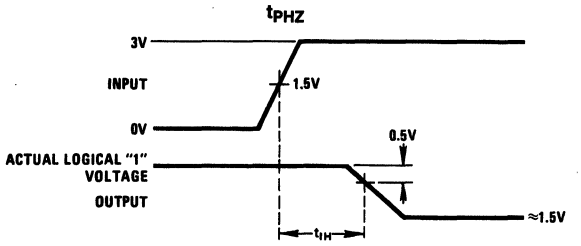
TL/F/5809–6

f = 1 MHz

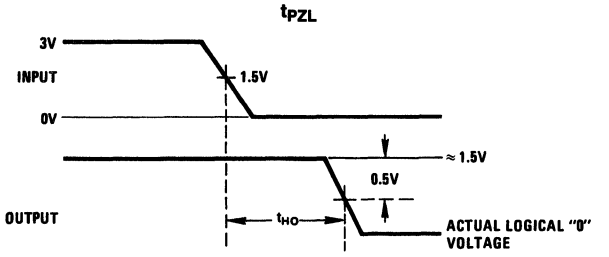
$t_r = t_f \leq 10$ ns (10% to 90%)

Duty Cycle = 50%

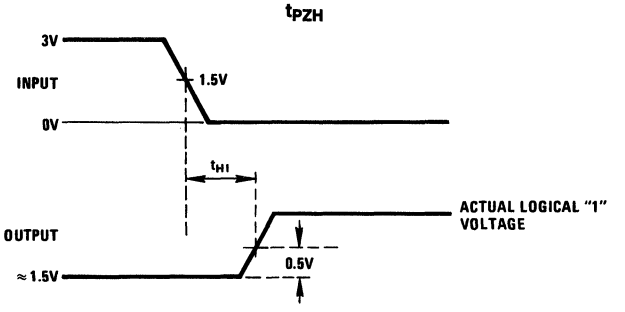
Switching Time Waveforms (Continued)



TL/F/5809–7



TL/F/5809–8



TL/F/5809–9

Truth Table

Disable Input	Driver Input (IN_X)	Receiver Input/ Bus Output (BUS_X)	Receiver Output (OUT_X)	Mode of Operation
DS7834/DS8834				
1	X		$\overline{BUS}$	Receive Bus Signal
0	1	0	1	Drive Bus
0	0	1	0	Drive Bus

X = Don't care

National Semiconductor

DS7836/DS8836 Quad NOR Unified Bus Receiver

General Description

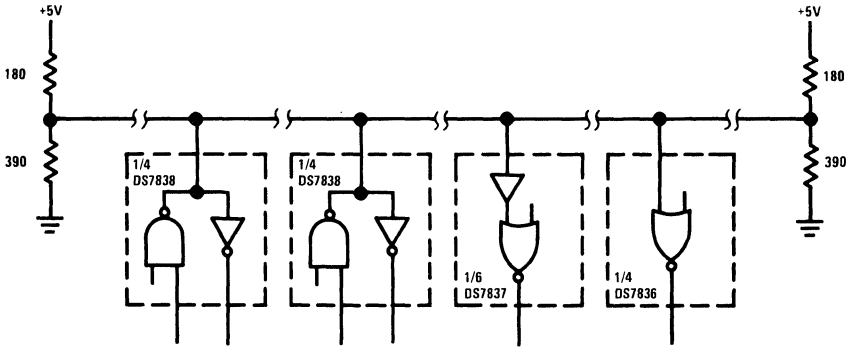
The DS7836/DS8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Performance is optimized for systems with bus rise and fall times ≤ 1.0 μs/V.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

Typical Application

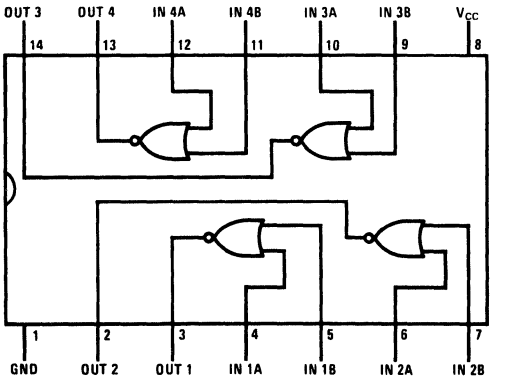
120Ω Unified Data Bus



TL/F/5810–1

Connection Diagram

Dual-In-Line Package



TL/F/5810–2

Top View

Order Number DS7836J or DS8836N
See NS Package Number J14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7.0V
Current Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 4 seconds)	260 °C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS7836	4.5	5.5	V
DS8836	4.75	5.25	V
Temperature (T_A)			
DS7836	−55	+125	°C
DS8836	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
V_{TH}	High Level Input Threshold	V_{CC} = Max		DS7836	1.65	2.25	2.65	V
				DS8836	1.80	2.25	2.50	V
V_{IL}	Low Level Input Threshold	V_{CC} = Min		DS7836	0.97	1.30	1.63	V
				DS8836	1.05	1.30	1.55	V
I_{IN}	Maximum Input Current	V_{IN} = 4V	V_{CC} = Max			15	50	μA
			V_{CC} = 0V			1	50	μA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, I_{OUT} = −400 μA			2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, I_{OUT} = 16 mA				0.25	0.4	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.5V, V_{OUT} = 0V, V_{CC} = Max, (Note 4)			−18		−55	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, (Per Package)				25	40	mA
V_{CL}	Input Clamp Diode Voltage	I_{IN} = −12 mA, T_A = 25°C				−1	−1.5	V

Switching Characteristics V_{CC} = 5V, T_A = 25°C unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	(Notes 4 and 5)	Input to Logical "1" Output		20	30	ns
			Input to Logical "0" Output		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7836 and across the 0°C to +70°C range for the DS8836. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor

DS7837/DS8837 Hex Unified Bus Receiver

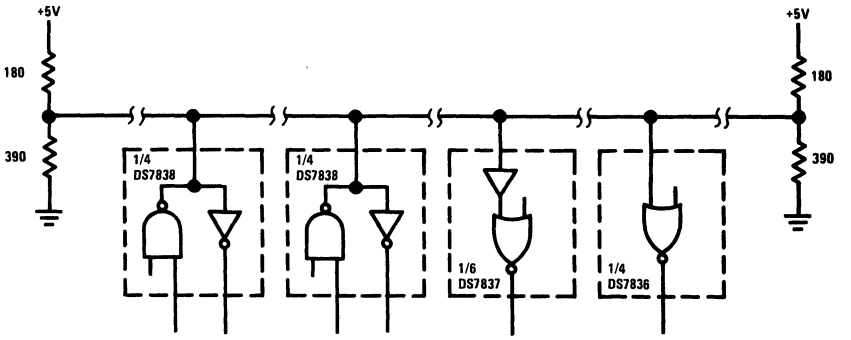
General Description

The DS7837/DS8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are TTL compatible. Performance is optimized for systems with bus rise and fall times ≤1.0 μs/V.

Features

- Low receiver input current for normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

Typical Application



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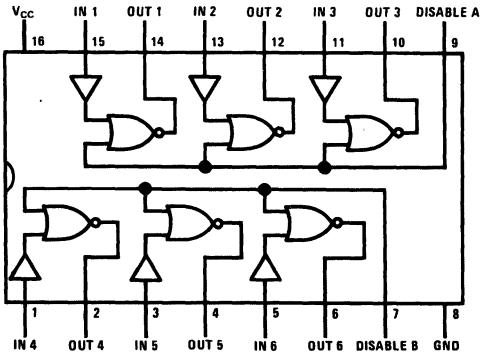
Connection Diagram

Dual-In-Line Package



TL/F/5811–2

Top View

Order Number DS7837J, DS8837M or DS8837N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DS7837	−55°C to +125°C
DS8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW
Lead Temperature (Soldering, 4 seconds)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})			
DS7837	4.5	5.5	V
DS8837	4.75	5.25	V
Temperature (T_A)			
DS7837	−55	+125	°C
DS8837	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	High Level Receiver Threshold	V_{CC} = Max	DS7837	1.65	2.25	2.65	V
			DS8837	1.80	2.25	2.50	V
V_{TL}	Low Level Receiver Threshold	V_{CC} = Min	DS7837	0.97	1.30	1.63	V
			DS8837	1.05	1.30	1.55	V
I_{IH}	Maximum Receiver Input Current	V_{IN} = 4V	$V_{CC} = V_{MAX}$		15.0	50.0	μA
			V_{CC} = 0V		1.0	50.0	μA
I_{IL}	Logical "0" Receiver Input Current	V_{IN} = 0.4V, $V_{CC} = V_{MAX}$			1.0	50.0	μA
V_{IH}	Logical "1" Input Voltage		Disable	2.0			V
V_{IL}	Logical "0" Input Voltage		Disable			0.8	V
I_{IH}	Logical "1" Input Current	Disable Input	V_{IND} = 2.4V			80.0	μA
			V_{IND} = 5.5V			2.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 4V, V_{IND} = 0.4V, Disable Input				−3.2	mA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, V_{IND} = 0.8V, I_{OH} = −400 μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, V_{IND} = 0.8V, I_{OH} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{IN} = 0.5V, V_{IND} = 0V, V_{OS} = 0V, $V_{CC} = V_{MAX}$, (Note 4)		−18.0		−55.0	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, V_{IND} = 0V, (Per Package)			45.0	60.0	mA
V_{CL}	Input Clamp Diode	V_{IN} = −12 mA, V_{IND} = −12 mA, T_A = 25°C			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{pd}	Propagation Delays	V_{IND} = 0V, Receiver	Input to Logical "1" Output, (Note 5)		20	30	ns
			Input to Logical "0" Output, (Note 6)		18	30	ns
		Input = 0V, Disable, (Note 7)	Input to Logical "1" Output		9	15	ns
			Input to Logical "0" Output		4	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified *min/max* limits apply across the −55°C to +125°C temperature range for the DS7837 and across the 0°C to +70°C range for the DS8837. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor

DS7838/DS8838 Quad Unified Bus Transceiver

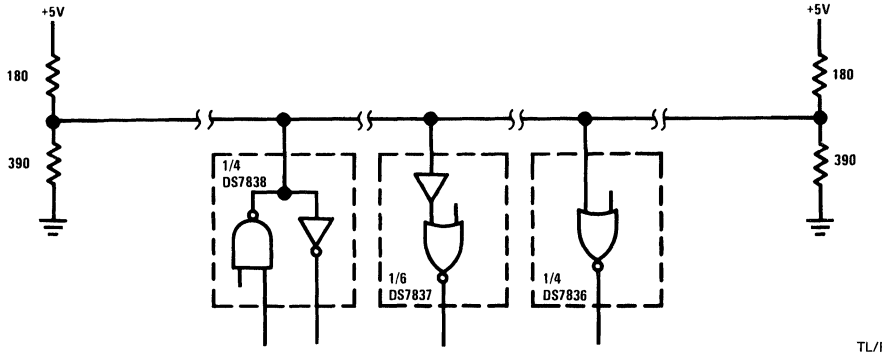
General Description

The DS7838/DS8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times ≤ 1.0 μs/V.

Features

- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20 μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Typical Application



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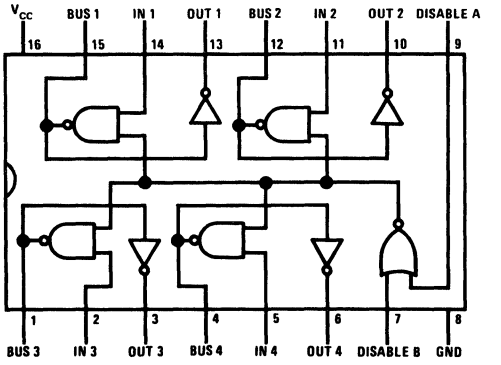
Connection Diagram

Dual-In-Line Package



TL/F/5812–2

Top View

Order Number DS7838J, DS8838M or DS8838N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature, (Soldering, 4 sec.)	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded DIP package 10.9 mW/°C above 25°C; derate SO package 8.01 mW/°C above 25°C.

Maximum Power Dissipation* at 25°C

Cavity Package	1433 mW
Molded DIP Package	1362 mW
SO Package	1002 mW

Operating Conditions

Operating Temperature Range	
DS7838	−55°C to +125°C
DS8838	0°C to +70°C
Supply Voltage (V_{CC})	
DS7838	$4.5V \le V_{CC} \le 5.5V$
DS8838	$4.75V \le V_{CC} \le 5.25V$

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \le V_{CC} \le V_{MAX}$, $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$				1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$				40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{DIS} = -12$ mA, $I_{IN} = -12$ mA, $I_{BUS} = -12$ mA, $T_A = 25°C$			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 50$ mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = V_{MAX}$			20	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			2	100	μA
V_{IH}	High Level Receiver Threshold	$V_{IND} = 0.8V$, $I_{OL} = 16$ mA, V_{CC} = Max	DS7838	1.65	2.25	2.65	V
			DS8838	1.80	2.25	2.50	V
V_{IL}	Low Level Receiver Threshold	$V_{IND} = 0.8V$, $V_{OH} = -400$ μA, V_{CC} = Min	DS7838	0.97	1.30	1.63	V
			DS8838	1.05	1.30	1.55	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA		2.4			V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$, (Per Package)			50	70	mA

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3) (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVER OUTPUT (Continued)						
t_{pd}	Propagation Delays (Note 8)					
	Disable to Bus "1"	(Note 5)		19	30	ns
	Disable to Bus "0"	(Note 5)		15	23	ns
	Driver Input to Bus "1"	(Note 5)		17	25	ns
	Driver Input to Bus "0"	(Note 5)		9	15	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output	(Note 7)		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7838 and across the 0°C to +70°C range for the DS8838. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.5V$ to $V_{BUS} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 6: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 1.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 7: Fan-out of 10 load, $C_{LOAD} = 15$ pF total. Measured from $V_{IN} = 2.3V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3.0V pulse.

Note 8: These apply for $V_{CC} = 5V$, $T_A = 25°C$ unless otherwise speicified.

Section 12

System Considerations

Section 12 Contents

Chapter 1
Transmission Line Concepts

Introduction

The interactions between wiring and circuitry in high-speed systems are more easily determined by treating the interconnections as transmission lines. A brief review of basic concepts is presented and simplified methods of analysis are used to examine situations commonly encountered in digital systems. Since the principles and methods apply to any type of logic circuit, normalized pulse amplitudes are used in sample waveforms and calculations.

Simplifying Assumptions

For the great majority of interconnections in digital systems, the resistance of the conductors is much less than the input and output resistance of the circuits. Similarly, the insulating materials have very good dielectric properties. These circumstances allow such factors as attenuation, phase distortion, and bandwidth limitations to be ignored. With these simplifications, interconnections can be dealt with in terms of characteristic impedance and propagation delay.

Characteristic Impedance

The two conductors that interconnect a pair of circuits have distributed series inductance and distributed capacitance between them, and thus constitute a transmission line. For any length in which these distributed parameters are constant, the pair of conductors have a characteristic impedance Z_0. Whereas quiescent conditions on the line are determined by the circuits and terminations, Z_0 is the ratio of transient voltage to transient current passing by a point on the line when a signal charge or other electrical disturbance occurs. The relationship between transient voltage, transient current, characteristic impedance, and the distributed parameters is expressed as follows:

$$\frac{V}{I} = Z_0 = \sqrt{\frac{L_0}{C_0}} \qquad (1\text{-}1)$$

where L_0 = inductance per unit length, C_0 = capacitance per unit length. Z_0 is in ohms, L_0 in Henries, C_0 in Farads.

Propagation Velocity

Propagation velocity v and its reciprocal, delay per unit length δ, can also be expressed in terms of L_0 and C_0. A consistent set of units is nanoseconds, microhenries and picofarads, with a common unit of length.

$$v = \frac{1}{\sqrt{L_0 C_0}} \qquad \delta = \sqrt{L_0 C_0} \qquad (1\text{-}2)$$

Equations 1-1 and *1-2* provide a convenient means of determining the L_0 and C_0, of a line when delay, length and impedance are known. For a length l and delay T, δ is the ratio T/l. To determine L_0 and C_0, combine *Equations 1-1* and *1-2*.

$$L_0 = \delta Z_0 \qquad (1\text{-}3)$$

$$C_0 = \frac{\delta}{Z_0} \qquad (1\text{-}4)$$

More formal treatments of transmission line characteristics, including loss effects, are available from many sources.[1-3]

Termination and Reflection

A transmission line with a terminating resistor is shown in *Figure 1-1*. As indicated, a positive step function voltage travels from left to right. To keep track of reflection polarities, it is convenient to consider the lower conductor as the voltage reference and to think in terms of current flow in the top conductor only. The generator is assumed to have zero internal impedance. The initial current I_1 is determined by V_1 and Z_0.

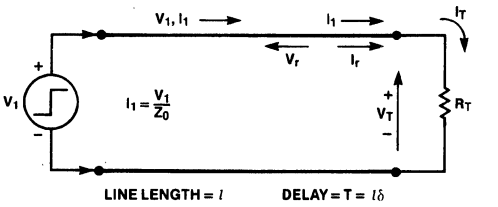


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FIGURE 1-1. Assigned Polarities and Directions for Determining Reflections

If the terminating resistor matches the line impedance, the ratio of voltage to current traveling along the line is matched by the ratio of voltage to current which must, by Ohm's law, always prevail at R_T. From the viewpoint of the voltage step generator, no adjustment of output current is ever required; the situation is as though the transmission line never existed and R_T had been connected directly across the terminals of the generator. From the R_T viewpoint, the only thing the line did was delay the arrival of the voltage step by the amount of time T.

When R_T is not equal to Z_0, the initial current starting down the line is still determined by V_1 and Z_0 but the final steady state current, after all reflections have died out, is determined by V_1 and R_T (ohmic resistance of the line is assumed to be negligible). The ratio of voltage to current in the initial wave is not equal to the ratio of voltage to current demanded by R_T. Therefore, at the instant the initial wave arrives at R_T, another voltage and current wave must be generated so that Ohm's law is satisfied at the line-load interface. This *reflected* wave, indicated by V_r and I_r in *Figure 1-1*, starts to return toward the generator. Applying

Termination and Reflection (Continued)

Kirchoff's laws to the end of the line at the instant the initial wave arrives, results in the following.

$$I_1 + I_r = I_T = \text{current into } R_T \qquad (1\text{-}5)$$

Since only one voltage can exist at the end of the line at this instant of time, the following is true:

$$V_1 + V_r = V_T$$

$$\text{thus} \quad I_T = \frac{V_T}{R_T} = \frac{V_1 + V_r}{R_T} \qquad (1\text{-}6)$$

$$\text{also} \quad I_1 = \frac{V_1}{Z_0} \text{ and } I_r = -\frac{V_r}{Z_0}$$

with the minus sign indicating that V_r is moving toward the generator.

Combining the foregoing relationships algebraically and solving for V_r yields a simplified expression in terms of V_1, Z_0 and R_T.

$$\frac{V_1}{Z_0} - \frac{V_r}{Z_0} = \frac{V_1 + V_r}{R_T} = \frac{V_1}{R_T} + \frac{V_r}{R_T}$$

$$V_1\left(\frac{1}{Z_0} - \frac{1}{R_T}\right) = V_r\left(\frac{1}{R_T} + \frac{1}{Z_0}\right) \qquad (1\text{-}7)$$

$$V_r = V_1\left(\frac{R_T - Z_0}{R_T + Z_0}\right) = \rho_L V_1$$

The term in parenthesis is called the coefficient of reflection ρ. With R_T ranging between zero (shorted line) and infinity (open line), the coefficient ranges between -1 and $+1$ respectively. The subscript L indicates that ρ refers to the coefficient at the load end of the line.

Equation 1-7 expresses the amount of voltage sent back down the line, and since

$$V_T = V_1 + V_r \qquad (1\text{-}8)$$

$$\text{then} \quad V_T = V_1 (1 + \rho_L).$$

V_T can also be determined from an expression which does not require the preliminary step of calculating ρ_L. Manipulating $(1 + \rho_L)$ results in

$$1 + \rho_L = 1 + \frac{R_T - Z_0}{R_T + Z_0} = 2\left(\frac{R_T}{R_T + Z_0}\right)$$

Substituting in *Equation 1-8* gives

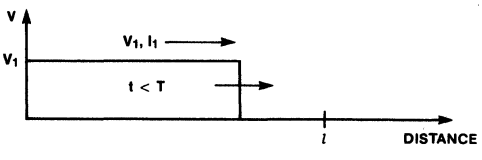
$$V_T = 2\left(\frac{R_T}{R_T + Z_0}\right) V_1 \qquad (1\text{-}9)$$

The foregoing has the same form as a simple voltage divider involving a generator V_1 with internal impedance Z_0 driving a load R_T, except that the amplitude of V_T is doubled.

The arrow indicating the direction of V_r in *Figure 1-1* correctly indicates the V_r direction of travel, but the direction of I_r flow depends on the V_r polarity. If V_r is positive, I_r flows toward the generator, opposing I_1. This relationship between the polarity of V_r and the direction of I_r can be deduced by noting in *Equation 1-7* that if V_r is positive it is because R_T is greater than Z_0. In turn, this means that the initial current I_r is larger than the final quiescent current, dictated by V_1 and R_T. Hence, I_r must oppose I_1 to reduce the line current to the final quiescent value. Similar reasoning shows that if V_r is negative, I_r flows in the same direction as I_1.

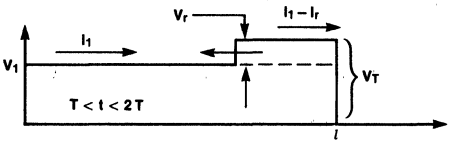
It is sometimes easier to determine the effect of V_r on line conditions by thinking of it as an independent voltage generator in series with R_T. With this concept, the direction of I_r is immediately apparent; its magnitude, however, is the ratio of V_r to Z_0, i.e., R_T is already accounted for in the magnitude of V_r. The relationships between incident and reflected signals are represented in *Figure 1-2* for both cases of mismatch between R_T and Z_0.

The incident wave is shown in *Figure 1-2a*, before it has reached the end of the line. In *Figure 1-2b*, a positive V_r is returning to the generator. To the left of V_r the current is still I_1, flowing to the right, while to the right of V_r the net current in the line is the difference between I_1 and I_r. In *Figure 1-2c*, the reflection coefficient is negative, producing a negative V_r. This, in turn, causes an increase in the amount of current flowing to the right behind the V_r wave.



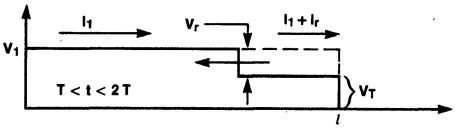
TL/F/12654–2

a. Incident Wave



TL/F/12654–3

b. Reflected Wave for $R_T > Z_0$



TL/F/12654–4

c. Reflected Wave for $R_T < Z_0$

FIGURE 1-2. Reflections for $R_T \neq Z_0$

Source Impedance, Multiple Reflections

When a reflected voltage arrives back at the source (generator), the reflection coefficient at the source determines the response to V_r. The coefficient of reflection at the source is governed by Z_0 and the source resistance R_S.

$$\rho_S = \frac{R_S - Z_0}{R_S + Z_0} \quad (1\text{-}10)$$

If the source impedance matches the line impedance, a reflected voltage arriving at the source is not reflected back toward the load end. Voltage and current on the line are stable with the following values.

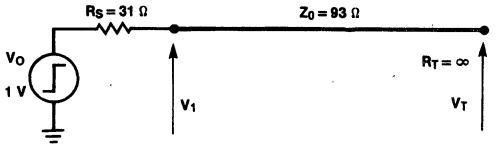
$$V_T = V_1 + V_r \text{ and } I_T = I_1 - I_r \quad (1\text{-}11)$$

If neither source impedance nor terminating impedance matches Z_0, multiple reflections occur; the voltage at each end of the line comes closer to the final steady state value with each succeeding reflection. An example of a line mismatched on both ends is shown in *Figure 1-3*. The source is a step function of 1V amplitude occurring at time t_0. The initial value of V_1 starting down the line is 0.75V due to the voltage divider action of Z_0 and R_S. The time scale in the photograph shows that the line delay is approximately 6 ns. Since neither end of the line is terminated in its characteristic impedance, multiple reflections occur.

The amplitude and persistence of the ringing shown in *Figure 1-3* become greater with increasing mismatch between the line impedance and source and load impedances. Reducing R_S *(Figure 1-3)* to 13Ω increases ρ_S to −0.75V, and the effects are illustrated in *Figure 1-4*. The initial value of V_T is 1.8V with a reflection of 0.9V from the open end. When this reflection reaches the source, a reflection of 0.9V × −0.75V starts back toward the open end. Thus, the second increment of voltage arriving at the open end is negative going. In turn, a negative-going reflection of 0.9V × −0.75V starts back toward the source. This negative increment is again multiplied by −0.75 at the source and returned toward the open end. It can be deduced that the difference in amplitude between the first two positive peaks observed at the open end is

$$V_T - V'_T = (1 + \rho_L)\, V_1 - (1 + \rho_L)\, V_1\, \rho^2_L\, \rho^2_S = (1 + \rho_L)\, V_1\, (1 - \rho^2_L\, \rho^2_S). \quad (1\text{-}12)$$

The factor $(1 - \rho^2_L\, \rho^2_S)$ is similar to the damping factor associated with lumped constant circuitry. It expresses the attenuation of successive positive or negative peaks of ringing.



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$$\rho_S = \frac{31 - 93}{31 + 93} = -0.5 \qquad \rho_L = \frac{\infty - 93}{\infty + 93} = +1$$

$$\text{Initially: } V_1 = \frac{Z_0}{Z_0 + R_S} \bullet V_0 = \frac{93}{124} \bullet 1 = 0.75V$$

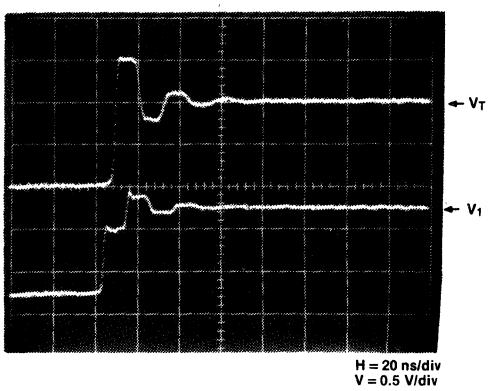

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FIGURE 1-3. Multiple Reflections Due to Mismatch at Load and Source

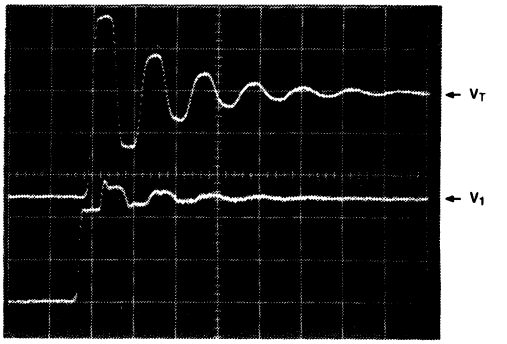

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FIGURE 1-4. Extended Ringing when R_S of *Figure 1-3* is Reduced to 13Ω

Lattice Diagram

In the presence of multiple reflections, keeping track of the incremental waves on the line and the net voltage at the ends becomes a bookkeeping chore. A convenient and systematic method of indicating the conditions which combines magnitude, polarity and time utilizes a graphic construction called a lattice diagram.[4] A lattice diagram for the line conditions of *Figure 1-3* is shown in *Figure 1-5*.

The vertical lines symbolize discontinuity points, in this case the ends of the line. A time scale is marked off on each line in increments of 2T, starting at t_0 for V_1 and T for V_T. The diagonal lines indicate the incremental voltages traveling between the ends of the line; solid lines are used for positive voltages and dashed lines for negative. It is helpful to write the reflection and transmission multipliers ρ and (1 + ρ) at each vertical line, and to tabulate the incremental and net voltages in columns alongside the vertical lines. Both the lattice diagram and the waveform photograph show that V_1 and V_T asymptotically approach 1V, as they must with a 1V source driving an open-ended line.

Lattice Diagram (Continued)

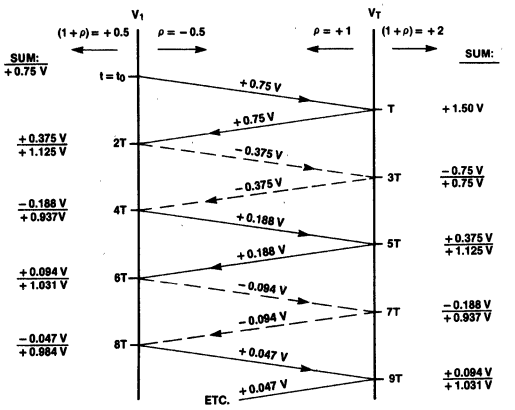

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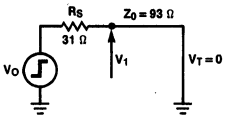
FIGURE 1-5. Lattice Diagram for the Circuit of *Figure 1-3*

Shorted Line

The open-ended line in *Figure 1-3* has a reflection coefficient of +1 and the successive reflections tend toward the steady state conditions of zero line current and a line voltage equal to the source voltage. In contrast, a shorted line has a reflection coefficient of −1 and successive reflections must cause the line conditions to approach the steady state conditions of zero voltage and a line current determined by the source voltage and resistance.

Shorted line conditions are shown in *Figure 1-6a* with the reflection coefficient at the source end of the line also negative. A negative coefficient at both ends of the line means that any voltage approaching either end of the line is reflected in the opposite polarity. *Figure 1-6b* shows the response to an input step-function with a duration much longer than the line delay. The initial voltage starting down the line is about +0.75V, which is inverted at the shorted end and returned toward the source as −0.75V. Arriving back at the source end of the line, this voltage is multiplied by $(1 + \rho_S)$, causing a −0.37V net change in V_1. Concurrently, a reflected voltage of +0.37V (−0.75V times ρ_S of −0.5) starts back toward the shorted end of the line. The voltage at V_1 is reduced by 50% with each successive round trip of reflections, thus leading to the final condition of zero volts on the line.

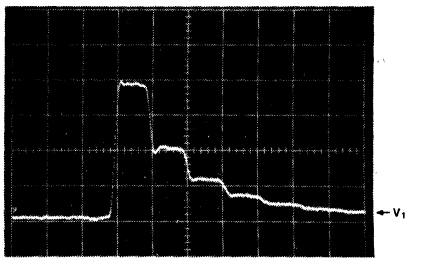
When the duration of the input pulse is less than the delay of the line, the reflections observed at the source end of the line constitute a train of negative pulses, as shown in *Figure 1-6c*. The amplitude decreases by 50% with each successive occurrence as it did in *Figure 1-6b*.



TL/F/12654–9

$\rho_S = -0.5$ $\quad \rho_L = \dfrac{0 - 93}{0 + 93} = -1$

a. Reflection Coefficients for Shorted Line



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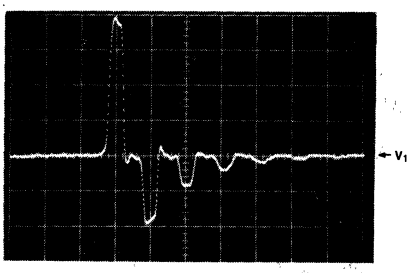
b. Input Pulse Duration ≫ Line Delay



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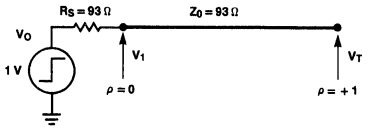
c. Input Pulse Duration < Line Delay

FIGURE 1-6. Reflections of Long and Short Pulses on a Shorted Line

Series Termination

Driving an open-ended line through a source resistance equal to the line impedance is called series termination. It is particularly useful when transmitting signals which originate on a PC board and travel through the backplane to another board, with the attendant discontinuities, since reflections coming back to the source are absorbed and ringing thereby controlled. *Figure 1-7* shows a 93Ω line driven from a 1V generator through a source impedance of 93Ω. The photograph illustrates that the amplitude of the initial signal sent down the line is only half of the generator voltage, while the voltage at the open end of the line is doubled to full amplitude ($1 + \rho_L = 2$). The reflected voltage arriving back at the source raises V_1 to the full amplitude of the generator signal. Since the reflection coefficient at the source is zero, no further changes occur and the line voltage is equal to the generator voltage. Because the initial signal on the line is only half the normal signal swing, the loads must be connected at or near the end of the line to avoid receiving a 2-step input signal.



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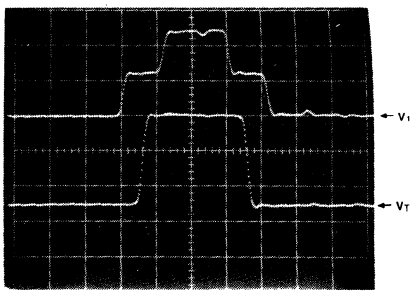

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FIGURE 1-7. Series Terminated Line and Waveforms

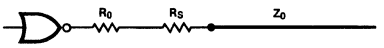

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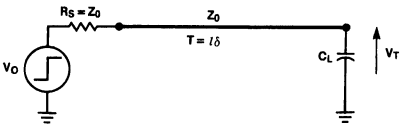
FIGURE 1-8. Logic Element Driving a Series Terminated Line

Extra Delay with Termination Capacitance

Designers should consider the effect of the load capacitance at the end of the line when using series termination. *Figure 1-9* shows how the output waveform changes with increasing load capacitance. *Figure 1-9b* shows the effect of load capacitances of 0, 12, 24, 48 pF. With no load, the delay between the 50% points of the input and output is just the line delay T. A capacitive load at the end of the line causes an extra delay ΔT due to the increase in rise time of the output signal.



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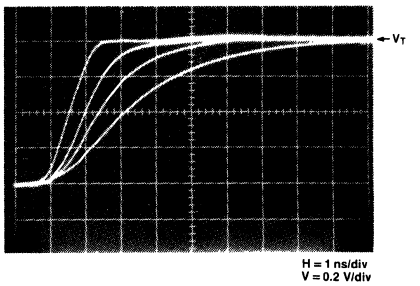
a. Series Terminated Line with Load Capacitance



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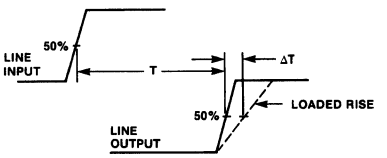
b. Output Rise Time Increase with Increasing Load Capacitance



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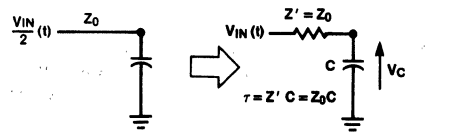
c. Extra Delay ΔT Due to Rise Time Increase

FIGURE 1-9. Extra Delay with Termination Capacitance

Extra Delay with Termination Capacitance (Continued)



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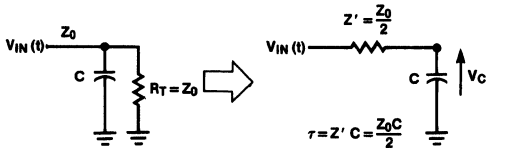
a. Thevenin Equivalent for Series Terminated Case



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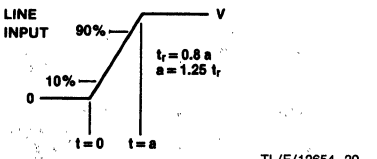
b. Thevenin Equivalent for Parallel Terminated Case



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$$v_{in}(t) = \frac{V}{a}\,[\,tu(t) - (t-a)u(t-a)]$$

$$u(t) = \frac{0 \text{ for } t < O}{1 \text{ for } t > O}$$

$$u(t-a) = \frac{0 \text{ for } t < a,}{1 \text{ for } t > a}$$

$$V_{IN}(S) = \frac{V}{as^2}(1 - e^{-as})$$

$$V_C(S) = \frac{V}{ar} \bullet \frac{1}{s^2(s + 1/\tau)}(1 - e^{-as})$$

$$v_c(t) = \frac{V}{a}[t - \tau(1 - e^{-t/\tau})]\,u(t)$$

$$-\frac{V}{a}[(t-a)$$

$$-\tau(1 - e^{-\frac{t-a}{\tau}})]\,u(t-a)$$

c. Equations for Input and Output Voltages

FIGURE 1-10. Determining the Effect of End-of-Line Capacitance

The increase in propagation delay can be calculated by using a ramp approximation for the incident voltage and characterizing the circuit as a fixed impedance in series with the load capacitance, as shown in *Figure 1-10*. One general solution serves both series and parallel termination cases by using an impedance Z′ and a time constant τ, defined in *Figure 1-10a* and *1-10b*. Calculated and observed increases in delay time to the 50% point show close agreement when τ is less than half the ramp time. At large ratios of τ/a (where a = ramp time), measured delays exceed calculated values by approximately 7%. *Figure 1-11*, based on measured values, shows the increase in delay to the 50% point as a function of the Z′C time constant, both normalized to the 10% to 90% rise time of the input signal. As an example of using the graph, consider a 100Ω series terminated line with 30 pF load capacitance at the end of the line and a no-load rise time of 3 ns for the input signal. From *Figure 1-10a*, Z′ is equal to 100Ω; the ratio $Z'C/t_r$ is 1. From the graph, the ratio $\Delta T/t_r$ is 0.8. Thus the increase in the delay to the 50% point of the output waveform is 0.8 t_r, or 2.4 ns, which is then added to the no-load line delay T to determine the total delay.

Had the 100Ω line in the foregoing example been parallel rather than series terminated at the end of the line, Z′ would be 50Ω. The added delay would be only 1.35 ns with the same 30 pF loading at the end. The added delay would be only 0.75 ns if the line were 50Ω and parallel terminated. The various trade-offs involving type of termination, line impedance, and loading are important considerations for critical delay paths.

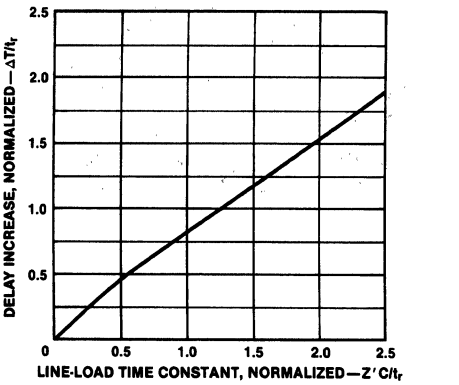

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FIGURE 1-11. Increase in 50% Point Delay Due to Capacitive Loading at the End of the Line, Normalized to T_r

Distributed Loading Effects on Line Characteristics

When capacitive loads such as inputs are connected along a transmission line, each one causes a reflection with a polarity opposite to that of the incident wave. Reflections from two adjacent loads tend to overlap if the time required for the incident wave to travel from one load to the next is equal to or less than the signal rise time.[5] *Figure 1-12a* illustrates an arrangement for observing the effects of capacitive loading, while *Figure 1-12b* shows an incident wave followed by reflections from two capacitive loads. The two capacitors causing the reflections are separated by a distance requiring a travel time of 1 ns. The two reflections return to the source 2 ns apart, since it takes 1 ns longer for the incident wave to reach the second capacitor and an additional 1 ns for the second reflection to travel back to the source. In the upper trace of *Figure 1-12b*, the input signal rise time is 1 ns and there are two distinct reflections, although the trailing edge of the first overlaps the leading edge of the second. The input rise time is longer in the middle trace, causing a greater overlap. In the lower trace, the 2 ns input rise time causes the two reflections to merge and appear as a single reflection which is relatively constant (at $\approx -10\%$) for half its duration. This is about the same reflection that would occur if the 93Ω line had a middle section with an impedance reduced to 75Ω.

With a number of capacitors distributed all along the line of *Figure 1-12a*, the combined reflections modify the observed input waveform as shown in the top trace of *Figure 1-12c*. The reflections persist for a time equal to the 2-way line delay (15 ns), after which the line voltage attains its final value. The waveform suggests a line terminated with a resistance greater than its characteristic impedance ($R_T >$ Z_0). This analogy is strengthened by observing the effect of reducing R_T from 93Ω to 75Ω, which leads to the middle waveform of *Figure 1-12c*. Note that the final (steady state) value of the line voltage is reduced by about the same amount as that caused by the capacitive reflections. In the lower trace of *Figure 1-12c* the source resistance R_S is reduced from 93Ω to 75Ω, restoring both the initial and final line voltage values to the same amplitude as the final value in the upper trace. From the standpoint of providing a desired signal voltage on the line and impedance matching at either end, the effect of distributed capacitive loading can be treated as a reduction in line impedance.

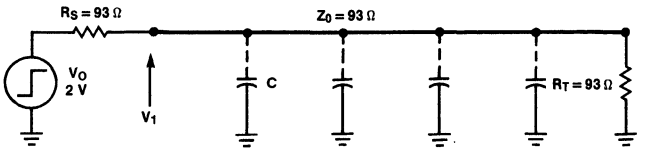
The reduced line impedance can be calculated by considering the load capacitance C_L as an increase in the intrinsic line capacitance C_0 along that portion of the line where the loads are connected.[6] Denoting this length of line as l, the distributed value C_D of the load capacitance is as follows.

$$C_D = \frac{C_L}{l}$$

C_D is then added to C_0 in *Equation 1-1* to determine the reduced line impedance Z_0.

$$Z'_0 = \sqrt{\frac{L_0}{C_0 + C_D}} = \sqrt{\frac{L_0}{C_0\left(1 + \frac{C_D}{C_0}\right)}} \qquad (1\text{-}13)$$

$$Z'_0 + \frac{\sqrt{\frac{L_0}{C_0}}}{\sqrt{1 + \frac{C_D}{C_0}}} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}}$$



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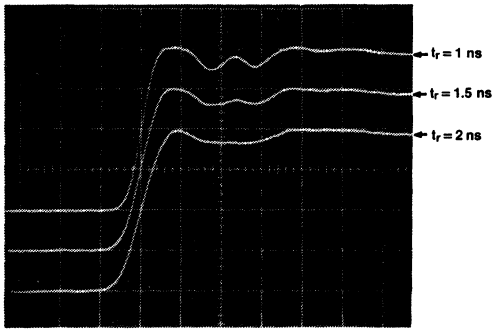
a. Arrangement for Observing Capacitive Loading Effects



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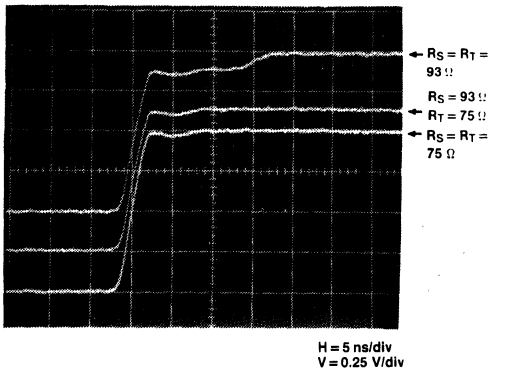
b. Capacitive Reflections Merging as Rise Time Increases



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c. Matching the Altered Impedance of a Capacitively Loaded Line

FIGURE 1-12. Capacitive Reflections and Effects on Line Characteristics

Distributed Loading Effects on Line Characteristics (Continued)

In the example of *Figure 1-12c*, the total load capacitance is 33 pF while the total intrinsic line capacitance /C_0 is 60 pF. (Note that the ratio C_D/C_0 is the same as $C_L//C_0$.) The calculated value of the reduced impedance is thus

$$Z'_0 = \frac{93}{\sqrt{1+\frac{33}{60}}} = \frac{93}{\sqrt{1.55}} = 75\Omega \qquad (1\text{-}14)$$

This correlates with the results observed in *Figure 1-12c* when R_T and R_S are reduced to 75Ω.

The distributed load capacitance also increases the line delay, which can be calculated from *Equation 1-2*.

$$\delta' = \sqrt{L_0(C_0+C_D)} = \sqrt{L_0C_0}\sqrt{1+\frac{C_D}{C_0}} = \delta\sqrt{1+\frac{C_D}{C_0}} \qquad (1\text{-}15)$$

The line used in the example of *Figure 1-12c* has an intrinsic delay of 6 ns and a loaded delay of 7.5 ns which checks with *Equation 1-15*.

$$/\delta' = /\delta\sqrt{1.55} = 6\sqrt{1.55} = 7.5\text{ ns} \qquad (1\text{-}16)$$

Equation 1-15 can be used to predict the delay for a given line and load. The ratio C_D/C_0 (hence the loading effect) can be minimized for a given loading by using a line with a high intrinsic capacitance C_0.

A plot of Z' and δ' for a 50Ω line as a function of C_D is shown in *Figure 1-13*. This figure illustrates that relatively modest amounts of load capacitance will add appreciably to the propagation delay of a line. In addition, the characteristic impedance is reduced significantly.

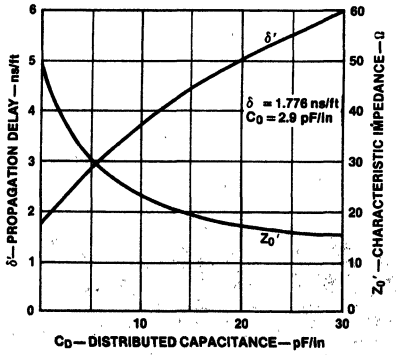

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FIGURE 1-13. Capacitive Loading Effects on Line Delay and Impedance

Worst case reflections from a capacitively loaded section of transmission line can be accurately predicted by using the modified impedance of *Equation 1-9*.[6] When a signal originates on an unloaded section of line, the effective reflection coefficient is as follows.

$$\rho = \frac{Z'_0 - Z_0}{Z'_0 + Z_0} \qquad (1\text{-}17)$$

Mismatched Lines

Reflections occur not only from mismatched load and source impedances but also from changes in line impedance. These changes could be caused by bends in coaxial cable, unshielded twisted-pair in contact with metal, or mismatch between PC board traces and backplane wiring. With the coax or twisted-pair, line impedance changes run about 5% to 10% and reflections are usually no problem since the percent reflection is roughly half the percent change in impedance. However, between PC board and backplane wiring, the mismatch can be 2 or 3 to 1. This is illustrated in *Figure 1-14* and analyzed in the lattice diagram of *Figure 1-15*. Line 1 is driven in the series terminated mode so that reflections coming back to the source are absorbed.

The reflection and transmission at the point where impedances differ are determined by treating the downstream line as though it were a terminating resistor. For the example of *Figure 1-14*, the reflection coefficient at the intersection of lines 1 and 2 for a signal traveling to the right is as follows.

$$\rho_{12} = \frac{Z_2 - Z_1}{Z_2 + Z_1} = \frac{93-50}{143} = +0.3 \qquad (1\text{-}18)$$

Thus the signal reflected back toward the source and the signal continuing along line 2 are, respectively, as follows.

$$V_{1r} = \rho_{12}V_1 = +0.3V_1 \qquad (1\text{-}19a)$$

$$V_2 = (1+\rho_{12})V_1 = +1.3V_1 \qquad (1\text{-}19b)$$

At the intersection of lines 2 and 3, the reflection coefficient for signals traveling to the right is determined by treating Z_3 as a terminating resistor.

$$\rho_{23} = \frac{Z_3 - Z_2}{Z_3 + Z_2} = \frac{39-93}{132} = -0.41 \qquad (1\text{-}20)$$

When V_2 arrives at this point, the reflected and transmitted signals are as follows.

$$V_{2r} = \rho_{23}V_2 = -0.41\,V_2 = (-0.41)(1.3)V_1 = -0.53\,V_1 \qquad (1\text{-}21a)$$

$$V_3 = (1+\rho_{23})V_2 = 0.59\,V_2 = (0.59)(1.3)V_1 = 0.77\,V_1 \qquad (1\text{-}21b)$$

Voltage V_3 is doubled in magnitude when it arrives at the open-ended output, since ρ_L is +1. This effectively cancels the voltage divider action between R_S and Z_1.

$$V_4 = (1+\rho_L)V_3 = (1+\rho_L)(1+\rho_{23})V_2 = (1+\rho_L)(1+\rho_{23})(1+\rho_{12})V_1 = (1+\rho_L)(1+\rho_{23})(1+\rho_{12})\frac{V_0}{2} \qquad (1\text{-}22)$$

$$V_4 = (1+\rho_{23})(1+\rho_{12})V_0$$

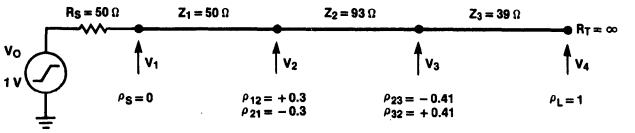
Thus, *Equation 1-22* is the general expression for the initial step of output voltage for three lines when the input is series terminated and the output is open-ended.

Mismatched Lines (Continued)

Note that the reflection coefficients at the intersections of lines 1 and 2 and lines 2 and 3 in *Figure 1-15* have reversed signs for signals traveling to the left. Thus the voltage reflected from the open output and the signal reflecting back and forth on line 2 both contribute additional increments of output voltage in the same polarity as V_O. Lines 2 and 3 have the same delay time; therefore, the two aforementioned increments arrive at the output simultaneously at time 5T on the lattice diagram *(Figure 1-15)*.

In the general case of series lines with different delay times, the vertical lines on the lattice diagram should be spaced apart in the ratio of the respective delays. *Figure 1-16* shows this for a hypothetical case with delay ratios 1:2:3. For a sequence of transmission lines with the highest impedance line in the middle, at least three output voltage increments with the same polarity as V_O occur before one can occur of opposite polarity. On the other hand, if the middle line has the lowest impedance, the polarity of the second increment of output voltage is the opposite of V_O. The third increment of output voltage has the opposite polarity, for the time delay ratios of *Figure 1-16*.

When transmitting logic signals, it is important that the initial step of line output voltage pass through the threshold region of the receiving circuit, and that the next two increments of output voltage augment the initial step. Thus in a series terminated sequence of three mismatched lines, the middle line should have the highest impedance.



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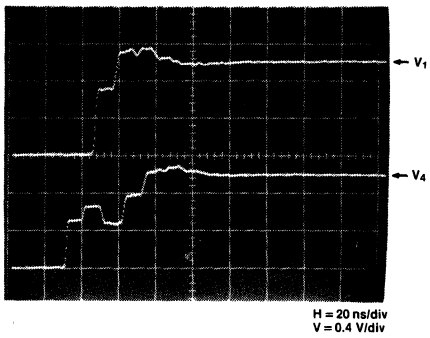

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FIGURE 1-14. Reflections from Mismatched Lines

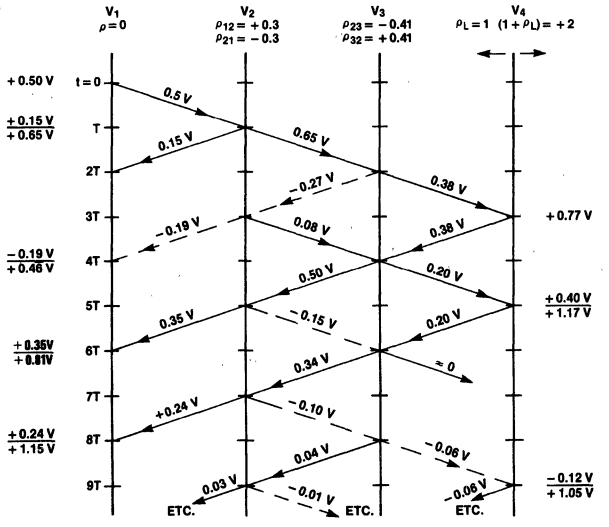

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FIGURE 1-15. Lattice Diagram for the Circuit of *Figure 1-14*

Mismatched Lines (Continued)

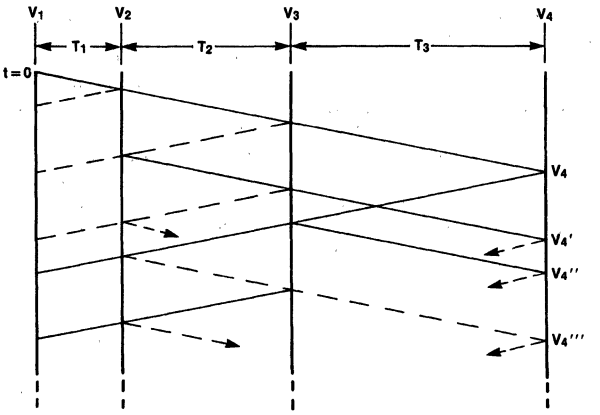

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FIGURE 1-16. Lattice Diagram for Three Lines with Delay Ratios 1:2:3

Rise Time versus Line Delay

When the 2-way line delay is less than the rise time of the input wave, any reflections generated at the end of the line are returned to the source before the input transition is completed. Assuming that the generator has a finite source resistance, the reflected wave adds algebraically to the input wave while it is still in transition, thereby changing the shape of the input. This effect is illustrated in *Figure 1-17*, which shows input and output voltages for several comparative values of rise time and line delay.

In *Figure 1-17b* where the rise time is much shorter than the line delay, V_1 rises to an initial value of 1V. At time T later, V_T rises to 0.5V, i.e., $1 + \rho_L = 0.5$. The negative reflection arrives back at the source at time 2T, causing a net change of −0.4V, i.e., $(1 + \rho_S)(-0.5) = -0.4$.

The negative coefficient at the source changes the polarity of the other 0.1V of the reflection and returns it to the end of the line, causing V_T to go positive by another 50 mV at time 3T. The remaining 50 mV is inverted and reflected back to the source, where its effect is barely distinguishable as a small negative change at time 4T.

In *Figure 1-17c*, the input rise time (0% to 100%) is increased to such an extent that the input ramp ends just as the negative reflection arrives back at the source end. Thus the input rise time is equal to 2T.

The input rise time is increased to 4T in *Figure 1-17d*, with the negative reflection causing a noticeable change in input slope at about its midpoint. This change in slope is more visible in the double exposure photo of *Figure 1-17e*, which shows V_1 (t_r still set for 4T) with and without the negative reflection. The reflection was eliminated by terminating the line in its characteristic impedance.

The net input voltage at any particular time is determined by adding the reflection to the otherwise unaffected input. It must be remembered that the reflection arriving back at the input at a given time is proportional to the input voltage at a time 2T earlier. The value of V_1 in *Figure 1-17d* can be calculated by starting with the 1V input ramp.

$$V_1 = \frac{1}{t_r} \bullet t \quad \text{for } 0 \le t \le 4T \tag{1-23}$$

$$= 1V \quad \text{for } t \ge 4T$$

The reflection from the end of the line is

$$V_r = \frac{\rho_L (t - 2T)}{t_r}; \tag{1-24}$$

the portion of the reflection that appears at the input is

$$V'_r = \frac{(1 + \rho_S)\,\rho_L (t - 2T)}{t_r}; \tag{1-25}$$

the net value of the input voltage is the sum.

$$V'_1 = \frac{t}{t_r} + \frac{(1 + \rho_S) + \rho_L (t - 2T)}{t_r} \tag{1-26}$$

The peak value of the input voltage in *Figure 1-17d* is determined by substituting values and letting t equal 4T.

$$V'_1 = 1 + \frac{(0.8)(-0.5)(4T - 2T)}{t_r} \tag{1-27}$$

$$= 1 - 0.4\,(0.5) = 0.8V$$

After this peak point, the input ramp is no longer increasing but the reflection is still arriving. Hence the net value of the input voltage decreases. In this example, the later reflections are too small to be detected and the input voltage is thus stable after time 6T. For the general case of repeated reflections, the net voltage $V_{1(t)}$ seen at the driven end of the line can be expressed as follows, where the signal caused by the generator is $V_{1(t)}$.

Rise Time versus Line Delay (Continued)

$V'_{1(t)} = V_{1(t)}$
for $0 < t < 2T$

$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)}$
for $2T < t < 4T$

$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)}$ (1-28)
for $4T < t < 6T$

$V'_{1(t)} = V_{1(t)} + (1 + \rho_S)\,\rho_L\,V_{1(t-2T)} + (1 + \rho_S)\,\rho_S\rho_L^2\,V_{1(t-4T)} + (1 + \rho_S)\,\rho_S^2\rho_L^3\,V_{1(t-6T)}$
for $6T < t < 8T$, etc.

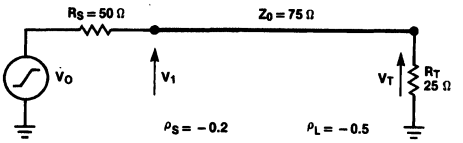
The voltage at the output end of the line is expressed in a similar manner.

$V_{T(t)} = 0$
for $0 < t < T$

$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)}$
for $T < t < 3T$

$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L\,V_{1(t-3T)}$ (1-29)
for $3T < t < 5T$

$V_{T(t)} = (1 + \rho_L)\,V_{1(t-T)} + (1 + \rho_L)\,\rho_S\rho_L V_{1(t-3T)} + (1 + \rho_L)\,\rho_S^2\rho_L^2\,V_{1(t-5T)}$
for $5T < t < 7T$, etc.



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a. Test Arrangement for Rise Time Analysis

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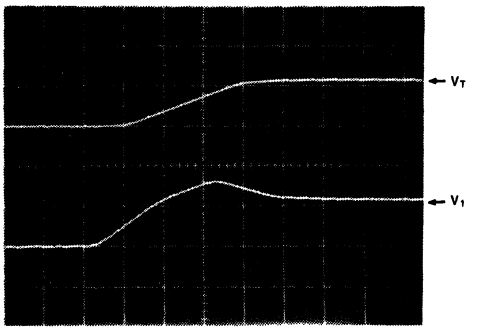
b. Line Voltages for $t_r \ll T$



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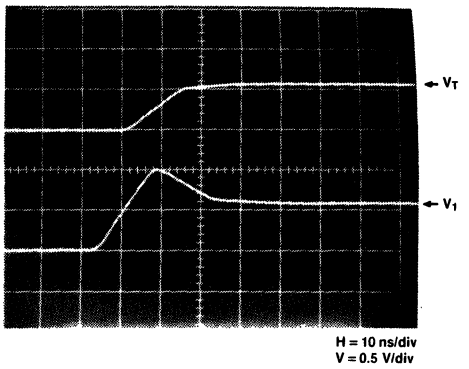
d. Line Voltages for $t_r = 4T$



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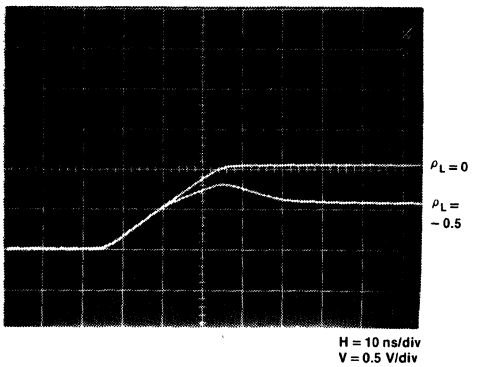
c. Line Voltages for $t_r = 2T$



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e. Input Voltage with and without Reflection

FIGURE 1-17. Line Voltages for Various Ratios of Rise Time to Line Delay

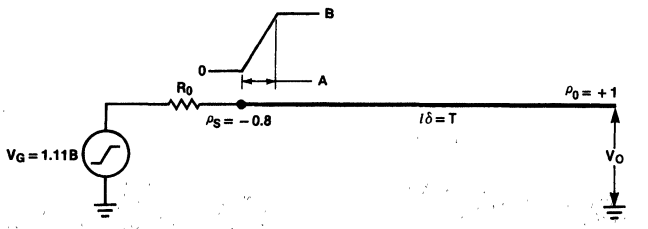
Ringing

Multiple reflections occur on a transmission line when neither the signal source impedance nor the termination (load) impedance matches the line impedance. When the source reflection coefficient ρ_S and the load reflection coefficient ρ_L are of opposite polarity, the reflections alternate in polarity. This causes the signal voltage to oscillate about the final steady state value, commonly recognized as ringing.

When the signal rise time is long compared to the line delay, the signal shape is distorted because the individual reflections overlap in time. The basic relationships among rise time, line delay, overshoot and undershoot are shown in a simplified diagram, *Figure 1-18*. The incident wave is a ramp of amplitude B and rise duration A. The reflection coefficient at the open-ended line output is +1 and the source reflection coefficient is assumed to be −0.8, i.e., $R_0 = Z_0/9$.

Figure 1-18b shows the individual reflections treated separately. Rise time A is assumed to be three times the line delay T. The time scale reference is the line output and the first increment of output voltage V_O rises to 2B in the time interval A. Simultaneously, a positive reflection (not shown) of amplitude B is generated and travels to the source, whereupon it is multiplied by −0.8 and returns toward the end of the line. This negative-going ramp starts at time 2T (twice the line delay) and doubles to −1.6B at time 2T + A.

The negative-going increment also generates a reflection of amplitude −0.8B which makes the round trip to the source and back, appearing at time 4T as a positive ramp rising to +1.28B at time 4T + A. The process of reflection and re-reflection continues, and each successive increment changes in polarity and has an amplitude of 80% of the preceding increment.



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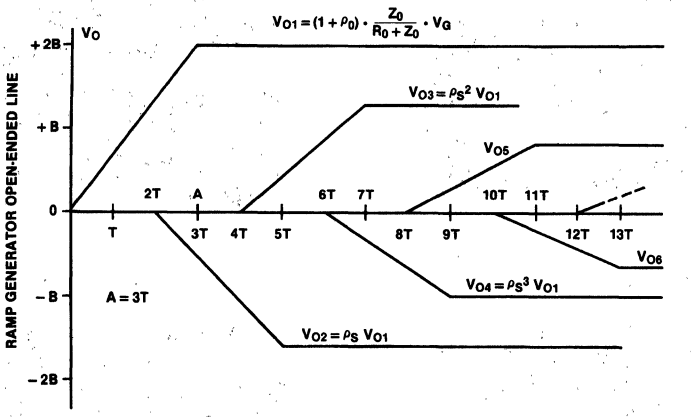
a. Ramp Generator Driving Open-Ended Line



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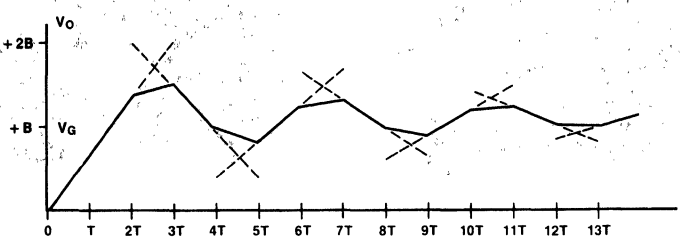
b. Increments of Output Voltage Treated Individually



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c. Net Output Signal Determined by Superposition

FIGURE 1-18. Basic Relationships Involved in Ringing

Ringing (Continued)

In *Figure 1-18c*, the output increments are added algebraically by superposition. The starting point of each increment is shifted upward to a voltage value equal to the algebraic sum of the quiescent levels of all the preceding increments (i.e., 0, 2B, 0.4B, 1.68B, etc.). For time intervals when two ramps occur simultaneously, the two linear functions add to produce a third ramp that prevails during the overlap time of the two increments.

It is apparent from the geometric relationships, that if the ramp time A is less than twice the line delay, the first output increment has time to rise to the full 2B amplitude and the second increment reduces the net output voltage to 0.4B. Conversely, if the line delay is very short compared to the ramp time, the excursions about the final value V_G are small.

Figure 1-18c shows that the peak of each excursion is reached when the earlier of the two constituent ramps reaches its maximum value, with the result that the first peak occurs at time A. This is because the earlier ramp has a greater slope (absolute value) than the one that follows.

Actual waveforms such as produced by ECL or TTL do not have a constant slope and do not start and stop as abruptly as the ramp used in the example of *Figure 1-18*. Predicting the time at which the peaks of overshoot and undershoot occur is not as simple as with ramp excitation. A more rigorous treatment is required, including an expression for the driving waveform which closely simulates its actual shape. In the general case, a peak occurs when the sum of the slopes of the individual signal increment is zero.

Summary

The foregoing discussions are by no means an exhaustive treatment of transmission line characteristics. Rather, they are intended to focus attention on the general methods used to determine the interactions between high-speed logic circuits and their interconnections. Considering an interconnection in terms of distributed rather than lumped inductance and capacitance leads to the line impedance concept, i.e., mismatch between this characteristic impedance and the terminations causes reflections and ringing.

Series termination provides a means of absorbing reflections when it is likely that discontinuities and/or line impedance changes will be encountered. A disadvantage is that the incident wave is only one-half the signal swing, which limits load placement to the end of the line. With parallel termination, i.e., at the end of the line, loads can be distributed along the line.

References

1. Metzger, G. and Vabre, J., *Transmission Lines with Pulse Excitation*, Academic Press, (1969).
2. Skilling, H., *Electric Transmission Lines*, McGraw-Hill, (1951).
3. Matick, R., *Transmission Lines for Digital and Communication Networks*, McGraw-Hill, (1969).
4. Millman, J. and Taub, H., *Pulse Digital and Switching Waveforms*, McGraw-Hill, (1965).
5. "Time Domain Reflectometry", *Hewlett-Packard Journal*, Vol. 15, No. 6, (February 1964).
6. Feller, A., Kaupp H., and Digiacoma, J., "Crosstalk and Reflections in High-Speed Digital Systems", *Proceedings, Fall Joint Computer Conference*, (1965).

National Semiconductor

Chapter 2
System Considerations

Introduction

All of National's Interface device input and output impedances are designed to accommodate various methods of driving and terminating interconnections. Controlled wiring impedance makes it possible to use simplified equivalent circuits to determine limiting conditions. Specific guidelines and recommendations are based on assumed worst-case combinations. Many of the recommendations may seem conservative, compared to typical observations, but the intent is to help the designer achieve a reliable system in a reasonable length of time with a minimum amount of redesign.

PC Board Transmission Lines

Strictly speaking, transmission lines may not always be required in all situations but, when used, they provide the advantages of predictable interconnect delays as well as reflection and ringing control through impedance matching. Two common types of PC board transmission lines are microstrip and stripline, *Figure 2-1*. Stripline requires multilayer construction techniques; microstrip uses ordinary double-clad boards. Other board construction techniques are wire wrap, stitch weld and discrete wired.

Stripline, *Figure 2-1b*, is used where packing density is a high priority because increasing the interconnect layers provides short signal paths. Boards with as many as 22 layers have been used in logic systems.

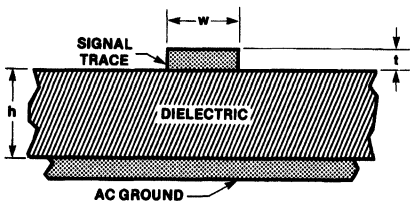
Microstrip offers easier fabrication and higher propagation velocity than stripline, but the routing for a complex system may require more design effort. Signal routing is simplified and an extra voltage plane is obtained by bonding two microstrip structures back to back, *Figure 2-1c*.

Microstrip

Equation 2-1 relates microstrip characteristic impedance to the dielectric constant and dimensions.[1] Electric field fringing requires that the ground extend beyond each edge of the signal trace by a distance no less than the trace width.

$$Z_0 = \left(\frac{60}{\sqrt{0.475\,\epsilon_r + 0.67}}\right) \ln\left(\frac{4h}{0.67\,(0.8\,w + t)}\right) = \left(\frac{87}{\sqrt{\epsilon_r + 1.41}}\right) \ln\left(\frac{5.98\,h}{0.8\,w + t}\right) \quad \textbf{(2-1)}$$

where h = dielectric thickness, w = trace width, t = trace thickness, ϵ_r = board material dielectric constant relative to air.



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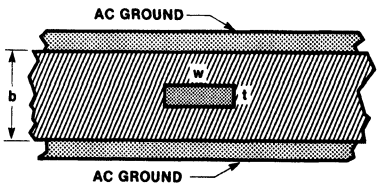
a. Microstrip



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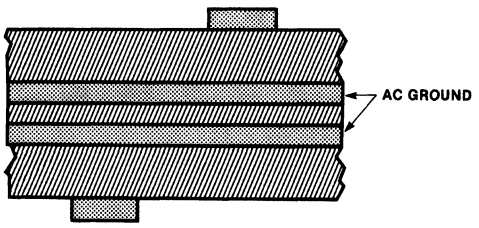
b. Stripline



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c. Composite Microstrip

FIGURE 2-1. Transmission Lines on Circuit Boards

PC Board Transmission Lines (Continued)

Equation 2-1 was developed from the impedance formula for a wire over ground plane transmission line, Equation 2-2.

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4h}{d}\right) \qquad \textbf{(2-2)}$$

where d = wire diameter, h = distance from ground to wire center.

Comparing Equation 2-1 and 2-2, the term 0.67 (0.8 w + t) shows the equivalence between a round wire and a rectangular conductor. The term 0.475 ϵ_r + 0.67 is the *effective* dielectric constant for microstrip ϵ_e, considering that a microstrip line has a compound dielectric consisting of the board material and air. The effective dielectric constant is determined by measuring propagation delay per unit of line length and using the following relationship.

$$\delta = 1.0167 \bullet \sqrt{\epsilon_e}\ \text{ns/ft} \qquad \textbf{(2-3)}$$

where δ = propagation delay, ns/ft.

Propagation delay is a property of the dielectric material rather than line width or spacing. The coefficient 1.0167 is the reciprocal of the velocity of light in free space. Propagation delay for microstrip lines on glass-filled G-10 epoxy boards is typically 1.77 ns/ft, yielding an effective dielectric constant of 3.03.

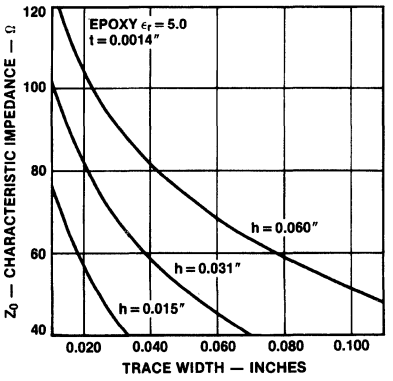

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FIGURE 2-2. Microstrip Impedance Versus Trace Width, G-10 Epoxy

Using ϵ_r = 5.0 in Equation 2-1, *Figure 2-2* provides microstrip line impedance as a function of width for several G-10 epoxy board thicknesses. *Figure 2-3* shows the related C_0 values, useful for determining capacitive loading effects on line characteristics, (Equation 1-15).

System designers should ascertain tolerances on board dimensions, dielectric constant and trace width etching in order to determine impedance variations. If conformal coating is used the effective dielectric constant of microstrip is increased, depending on the coating material and thickness.

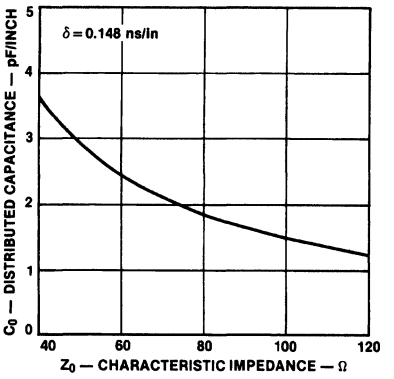

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FIGURE 2-3. Microstrip Distributed Capacitance Versus Impedance, G-10 Epoxy

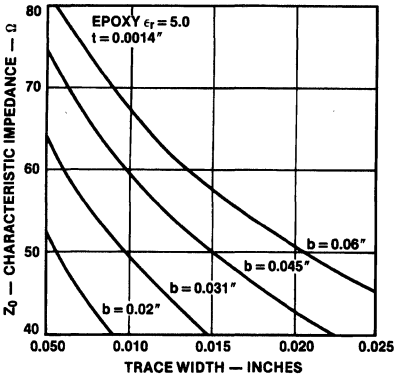
Stripline

Stripline conductors are totally embedded. As a result, the board material determines the dielectric constant. G-10 epoxy boards have a typical propagation delay of 2.26 ns/ft. Equation 2-4 is used to calculate stripline impedances.[1,2]

$$Z_0 = \left(\frac{60}{\sqrt{\epsilon_r}}\right) \ln\left(\frac{4b}{0.67\,\pi\,(0.8\,w + t)}\right) \qquad \textbf{(2-4)}$$

where b = distance between ground planes, w = trace width, t = trace thickness, w/(b-t) < 0.35 and t/b < 0.25.

Figure 2-4 shows stripline impedance as a function of trace width, using Equation 2-4 and various ground plane separations for G-10 glass-filled epoxy boards. Related values of C_0 are plotted in *Figure 2-5*.



TL/F/12655–6

FIGURE 2-4. Stripline Impedance Versus Trace Width, G-10 Epoxy

12

PC Board Transmission Lines (Continued)

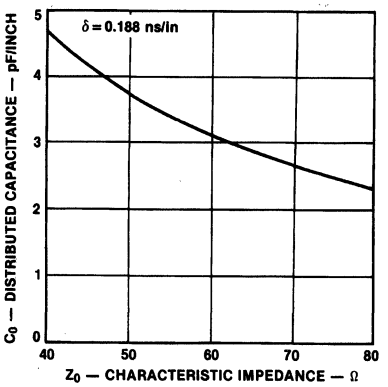


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FIGURE 2-5. Stripline Distributed Capacitance Versus Impedance, G-10 Epoxy

Wire Wrap

Wire-wrap boards are commercially available with several voltage planes, positions for Dual-In-Line Packages (DIP), terminating resistors, and decoupling capacitors. The devices are mounted on socket pins and interconnected with twisted pair wiring. One wire at each end of the twisted pair is wrapped around a signal pin, the other around a ground pin. The #30 insulated wire is uniformly twisted to provide a nominal 93Ω impedance line. Positions for Single-In-Line Package (SIP) terminating resistors are close to the inputs to provide good termination characteristics.

Discrete Wired

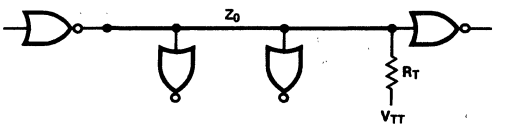
Custom Multiwire* boards are available with integral power and ground planes. Wire is placed on a controlled thickness above the ground plane to obtain a nominal impedance line of 55Ω. Then holes are drilled through the wire and board. Copper is deposited in the drilled holes by an additive-electrolysis process which bonds each wire to the wall of the holes. Devices are soldered on the board to make connection to the wires.

Parallel Termination

Terminating a line at the receiving end with a resistance equal to the characteristic line impedance is called parallel termination, *Figure 2-6a*. A pair of resistors connected in series between V_{CC} and ground supply can provide the Thevenin equivalent of a single resistor to the termination supply voltage, *Figure 2-6b*. The average power dissipation in the Thevenin equivalent resistors is about 10 times the power dissipation in the single resistor. For either parallel termination method, decoupling capacitors are required between the supply and ground.

*Multiwire is a registered trademark of the Multiwire Corporation.

a. Parallel Termination



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b. Thevenin Equivalent of R_T and V_{TT}

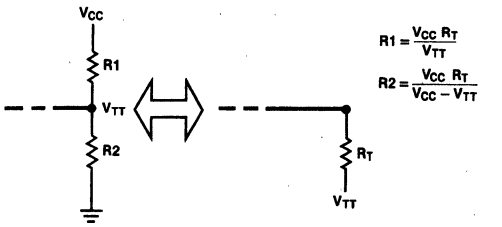

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FIGURE 2-6. Parallel Termination

The magnitude of reflections from the terminated end of the line depends on how well the termination resistance R_T matches the line impedance Z_O. The ratio of the reflected voltage to the incident voltage V_i is the reflection coefficient ρ.

$$\frac{V_r}{V_i} = \rho = \frac{R_T - Z_0}{R_T + Z_0} \qquad \textbf{(2-5)}$$

The initial signal swing at the termination is the sum of the incident and reflected voltages. The ratio of termination signal to incident signal is thus:

$$\frac{V_T}{V_i} = 1 + \rho = \frac{2R_T}{R_T + Z_0} \qquad \textbf{(2-6)}$$

The degree of reflections which can be tolerated varies in different situations, but to allow for worst-case circuits, a good rule of thumb is to limit reflections to 15% to prevent excursions into the threshold region of the inputs connected along the line. The range of permissible values of R_T as a function of Z_0 and the reflection coefficient limitations can be determined by rearranging Equation 2-5.

$$R_T = Z_0 \frac{1 + \rho}{1 - \rho} \qquad \textbf{(2-7)}$$

Using 15% reflection limits as examples, the range of the R_T/Z_0 ratio is as follows.

$$\frac{1.15}{0.85} > \frac{R_T}{Z_0} > \frac{0.85}{1.15} \quad 1.35 > \frac{R_T}{Z_0} > 0.74 \qquad \textbf{(2-8)}$$

The permissible range of the R_T/Z_0 ratio determines the tolerance ranges for R_T and Z_0. For example, using the foregoing ratio limits, R_T tolerances of ±10% allow Z_0 tolerance limits of +22% and −19%; R_T tolerances of ±5% allow Z_0 tolerance limits of +28% and −23%.

Input Impedance

The input impedance of integrated circuits is predominately capacitive. A single-function input has an effective value of about 5 pF, as determined by its effect on reflected and transmitted signals on transmission lines.

Capacitive loads connected along a transmission line increase the propagation delay of a signal along the line. The modified delay can be determined by treating the load capacitance as an increase in the intrinsic distributed capacitance of the line, discussed in Chapter 1. The intrinsic capacitance of any stubs which connect the inputs to the line should be included in the load capacitance. The intrinsic capacitance per unit length for G-10 epoxy boards is shown in *Figure 2-3* and *2-5* for microstrip and stripline respectively. For other dielectric materials, the intrinsic capacitance C_0 can be determined by dividing the intrinsic delay δ (Equation 2-3) by the line impedance Z_0.

The length of a stub branching off the line to connect an input should be limited to insure that the signal continuing along the line past the stub has a continuous rise, as opposed to a rise (or fall) with several partial steps. The point where a stub branches off the line is a low impedance point. This creates a negative coefficient of reflection, which in turn reduces the amplitude of the incident wave as it continues beyond the branch point. If the stub length is short enough, however, the first reflection returning from the end of the stub adds to the attenuated incident wave while it is still rising. The sum of the attenuated incident wave and the first stub reflection provides a step-free signal, although its rise time will be longer than that of the original signal. Satisfactory signal transitions can be assured by restricting stub lengths according to the recommendations for unterminated lines *(Figure 2-10)*. The same considerations apply when the termination resistance is not connected at the end of the line; a section of line continuing beyond the termination resistance should be treated as an unterminated line and its length restricted accordingly.

Series Termination

Series termination requires a resistor between the driver and transmission line, *Figure 2-7*. The receiving end of the line has no termination resistance. The series resistor value should be selected so that when added to the driver source resistance, the total resistance equals the line impedance. The voltage divider action between the net series resistance and the line impedance causes an incident wave of half amplitude to start down the line. When the signal arrives at the unterminated end of the line, it doubles and is thus restored to a full amplitude. Any reflections returning to the source are absorbed without further reflection since the line and source impedance match. This feature, source absorption, makes series termination attractive for interconnection paths involving impedance discontinuities, such as occur in backplane wiring.

A disadvantage of series termination is that driven inputs must be near the end of the line to avoid receiving a 2-step signal. The initial signal at the driver end is half amplitude, rising to full amplitude only after the reflection returns from the open end of the line. In *Figure 2-7*, one load is shown connected at point D, aways from the line end. This input receives a full amplitude signal with a continuous edge if the distance l to the open end of the line is within recommended lengths for unterminated line.

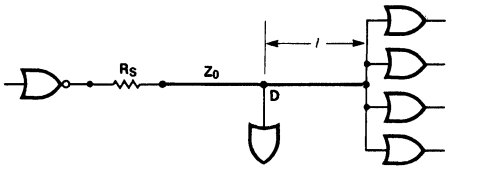

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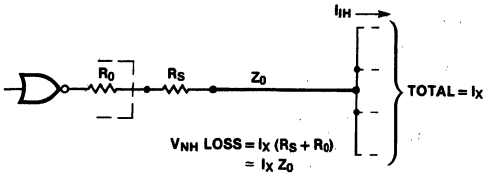
FIGURE 2-7. Series Termination

The signal at the end has a slower rise time that the incident wave because of capacitive loading. The increase in rise time effectively increases the line propagation delay. This added delay as a function of the product line impedance and load capacitance is discussed in Chapter 1.

Unterminated Lines

Lines can be used without series or parallel termination if the line delay is short compared to the signal rise time. Ringing occurs because the reflection coefficient at the open (receiving) end of the line is positive (nominally +1) while the reflection coefficient at the driving end is negative (approximately −0.8). These opposite polarity reflection coefficients cause any change in signal voltage to be reflected back and forth, with a polarity change each time the signal is reflected from the driver. Net voltage change on the line is thus a succession of increments with alternating polarity and decreasing magnitude. The algebraic sum of these increments if the observed ringing. The general relationships among rise time, line delay, overshoot and undershoot are discussed in Chapter 1, using simple waveforms for clarity.

Excessive overshoot on the positive-going edge of the signal drives input transistors into saturation. Although this does not damage an input, it does cause excessive recov-



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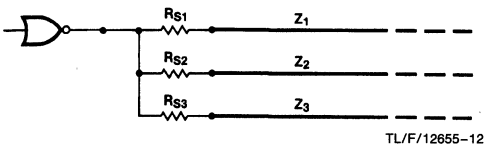
a. Noise Margin Loss Due to Load Input Current



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b. Driving Several Lines from one Output

FIGURE 2-8. Loading Considerations for Series Termination

ery times and makes propagation delays unpredictable. Undershoot (following the overshoot) must also be limited to prevent signal excursions into the threshold region of the loads. Such excursions could cause exaggerated transition times at the driven circuit outputs, and could also cause multiple triggering of sequential circuits. Signal swing, exclusive of ringing, is slightly greater on unterminated lines than on parallel terminated lines.

Unterminated Lines (Continued)

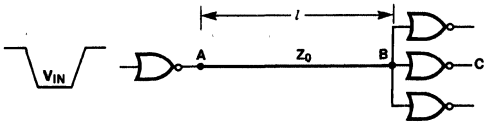
For worst case combinations of driver output and load input characteristics, a 35% overshoot limit insures that system speed is not compromised either by saturating an input on overshoot or extending into the threshold region on the following undershoot.

For distributed loading, ringing is satisfactorily controlled if the 2-way modified line delay does not exceed the 10% to 90% rise time of the driver output. This relationship can be expressed as follows, using the symbols from Chapter 1 and incorporating the effects of load capacitance on line delay.

$$t_r = 2T' = 2\ell\delta' = 2\ell\delta\sqrt{1 + \frac{C_L}{\ell C_0}}$$

Rearranging terms yields the quadratic equation:

$$\ell^2_{max} + \frac{C_L}{C_0}\ell_{max} + \frac{t_r^2}{4\delta^2} = 0 \qquad \textbf{(2-14)}$$



TL/F/12655–13

a. Unterminated Line

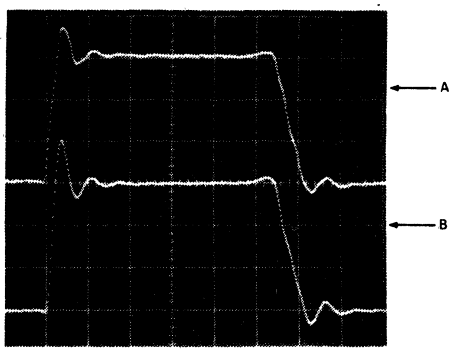


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FIGURE 2-9. Line Voltages Showing Stair-step Trailing Edges on Unterminated Line

The many combinations of line impedance and load make it practically impossible to define just when stub length begins to cause noticeable steps in the signal. A rough rule-of-thumb would be to limit the stub length to less than ½ of a rise time.

Data Bussing

Data bussing involves connecting two or more outputs and one or more inputs to the same signal line, *(Figure 2-10)*. Any one of the several drivers can be enabled and can apply data to the line. Load inputs connected to the line thus receive data from the selected source. This method of steering data from place to place simplifies wiring and tends to minimize package count. Only one of the drivers can be enabled at a given time; all other driver outputs must be in the LOW or CUT-OFF state. Termination resistors matching the line impedance are connected to both ends of the line to prevent reflections. An output driving the line sees an impedance equal to half the line impedance.

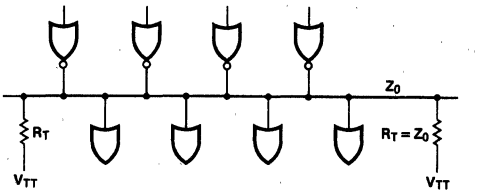

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FIGURE 2-10. Data Bus or Party Line

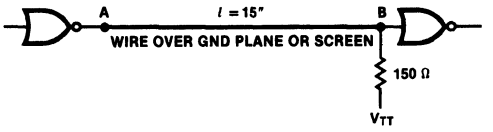
In some instances a single termination is satisfactory for a data bus, provided certain conditions are fulfilled. The single termination is connected in the middle of the line. This requires that for each half of the line, from the termination to the end, the line length and loading must comply with the same restrictions as unterminated lines to limit overshoot and undershoot to acceptable levels. The termination should be connected as near as possible to the electrical mid-point of the line, in terms of the modified line delay from the termination to either end. Another restriction is that the time between successive transitions, i.e., the nominal bit time, should not be less than 15 ns. This allows time for the major reflections to damp out and limits additive reflections to a minor level.

Backplane Interconnections

Several types of interconnections can be used to transmit a signal between logic boards. The factors to be considered when selecting a particular interconnection for a given application are cost, impedance discontinuities, predictability of propagation delay, noise environment, and bandwidth. Single-ended transmission over an ordinary wire is the most economical but has the least predictable impedance and propagation delay. At the opposite end of the scale, coaxial cable is the most costly but has the best electrical characteristics. Twisted pair and similar parallel wire interconnection cost and quality fall in between.

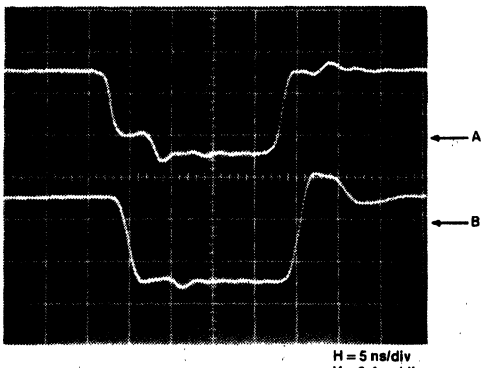
For single-wire transmission through the backplane, a ground plane or ground screen should be provided to establish a controlled impedance. A wire over a ground plane or screen has a typical impedance of 150Ω with variations on the order of ±33%, depending primarily on the distance from ground and the configuration of the ground. *Figure 2-12* illustrates the effects of impedance variations with a

Backplane Interconnections (Continued)



TL/F/12655–16

a. Wire over Ground Plane or Screen



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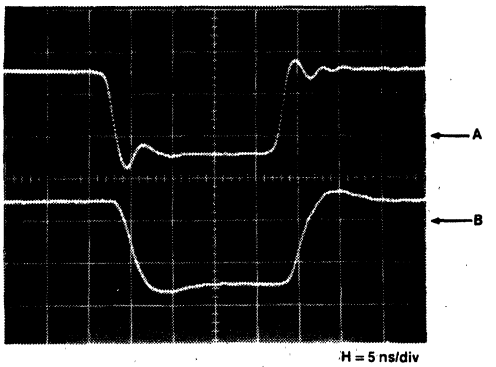
b. Wire in Contact with Ground Plane



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c. Wire Spaced 1/8" from Ground Screen

FIGURE 2-12. Parallel Terminated Backplane Wire

15-inch wire parallel terminated with 150Ω to V_{TT}. *Figure 2-12b* shows source and receiver waveforms when the wire is in contact with a continuous ground plane. The negative-going signal at the source shows an initial step of only 80% of a full signal swing. This occurs because the quiescent HIGH-state current I_{OH} multiplied by the impedance of the wire (approximately 90Ω) is less than the normal signal swing, and this condition allows the driver to turn off. The negative-going signal at the receiving end is greater by 25% ($1 + \rho = 1.25$). The receiving end mismatch causes a negative-going reflection which returns to the source and establishes the V_{OL} level. The positive-going signal at the source shows a normal signal swing, with the receiving end exhibiting approximately 25% overshoot.

Figure 2-12c shows waveforms for a similar arrangement, but with the wire about 1/8 inch from a ground screen. The impedance of the wire is greater than 150Ω termination, but small variations in impedance along the wire cause intermediate reflections which tend to lengthen the rise and fall times of the signal. As a result, the received signal does not exhibit pronounced changes in slope as would be expected if a 200Ω constant impedance line were terminated with 150Ω.

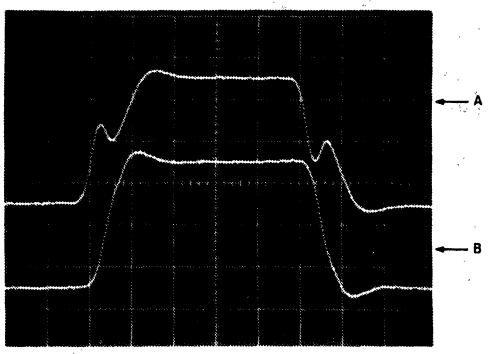
Series source resistance can also be used with single wire interconnections to absorb reflection. *Figure 2-13a* shows a 16-inch wire with a ground screen driven through a source resistance of 100Ω. The waveforms *(Figure 2-13b)* show that although reflections are generated, they are largely absorbed by the series resistor, and the signal received at the load exhibits only slight changes and overshoot. Series termination techniques can also be used when the signal into the wire comes from the PC board transmission line. *Figure 2-14a* illustrates a 12-inch wire over a ground screen, with 12-inch microstrip lines at either end of the wire. The output is heavily loaded (fan-out of 8) and the combination of impedances produces a variety of reflections at the input to the first microstrip line, shown in the upper trace of *Figure 2-14b*. The lower trace shows the final output; a comparison between the two traces shows the effectiveness of damping in maintaining an acceptable signal at the output. *Figure 2-14c* shows the signals at the input to the driving gate and at the output of the load gate, with a net through-put time of 8.5 ns. The circuit in *Figure 2-14a* is a case of mismatched transmission lines, discussed in Chapter 1.

Signal propagation along a single wire tends to be fast because the dielectric medium is mostly air. However, impedance variations along a wire cause intermediate reflections which tend to increase rise and fall times, effectively increasing propagation delay. Effective propagation delays are in the range of 1.5 to 2.0 ns per foot of wire. Load capacitance at the receiving end also increases rise and fall time (Chapter 1), further increasing the effective propagation delay.

Backplane Interconnections (Continued)

TL/F/12655–19

a. Wire over Ground Screen



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b. Series Terminated Waveform

FIGURE 2-13. Series Terminated Backplane Wire

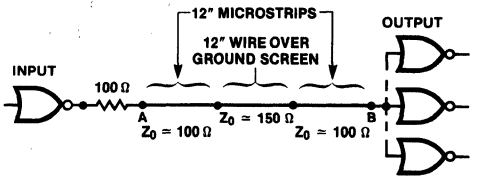
Better control of line impedance and faster propagation can be achieved with a twisted pair. A twisted pair of AWG 26 Teflon* insulated wires, two twists per inch, exhibits a propagation delay of 1.33 ns/ft and an impedance of 115Ω. Twisted pair lines are available in a variety of sizes, impedances and multiple-pair cables. *Figure 2-15a* illustrates single-ended driving and receiving. In addition to improved propagation velocity, the magnetic fields of the two conductors tend to cancel, minimizing noise coupled into adjacent wiring.

Differential line driving and receiving using a line driver and line receiver is illustrated in *Figure 2-15b*. Differential operation provides high noise immunity, since common mode input voltages are rejected. The differential mode is recommended for communication between different parts of a system, because it effectively nullifies ground voltage differences. For long runs between cabinets or near high power transients, interconnections using shielded twisted pair are recommended.

Twisted pair lines can be used to implement party line type data transfer in the backplane, as indicated in *Figure 2-15c*. Only one driver should be enabled at a given time; the other outputs must be in an off state.

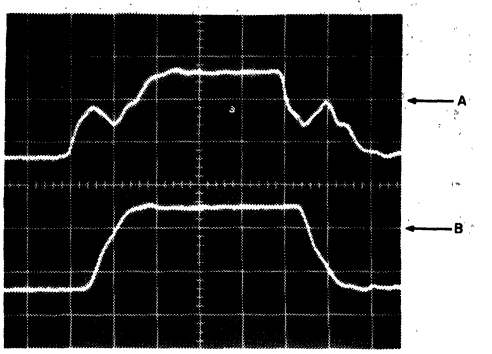
In the differential mode, a twisted pair can send high-frequency symmetrical signals, such as clock pulses, of 100 MHz over distances of 50 to 100 feet. For random data, however, bit rate capability is reduced by a factor of four or five due to line rise effects on time jitter.[3] (Also see AN-806, AN-807 and AN-808.)

*Teflon is a registered trademark of E.I. du Pont de Nemours Company.



TL/F/12655–21

a. Backplane Wire Interconnecting PC Board Lines



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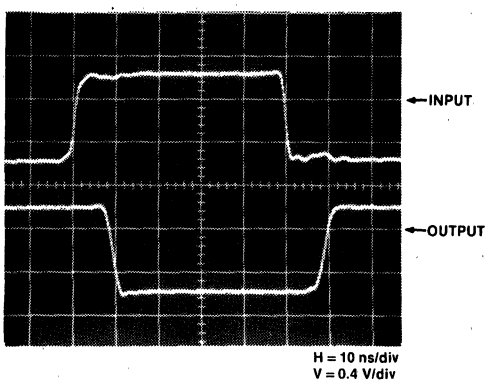
b. Signals into the First Microstrip and at the Loads



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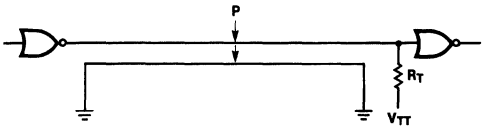
c. Input to Driving Gate and Output of Load Gate

FIGURE 2-14. Signal Path with Sequence of Microstrip, Wire, Microstrip

Coaxial cable offers the highest frequency capability. In addition, the outer conductor acts as a shield against noise, while the uniformity of characteristics simplifies the task of matching time delays between different parts of the system. In the single-ended mode, *Figure 2-16a,* 50 MHz signals can be transferred over distances of 100 feet. For 100 MHz operation, lengths should be 50 feet or less. In the differential

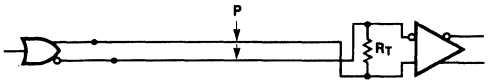
Backplane Interconnections (Continued)

mode, *Figures 2-16b, c,* the line receiver can recover smaller signals, allowing 100 MHz signals to be transferred up to 100 feet. The dual cable arrangement of *Figure 2-16c* provides maximum noise immunity. The delay of coaxial cables depends on the type of dielectric material, with typical delays of 1.52 ns/ft for polyethylene and 1.36 ns/ft for cellular polyethylene.



TL/F/12655–24

a. Single-ended Twisted Pair



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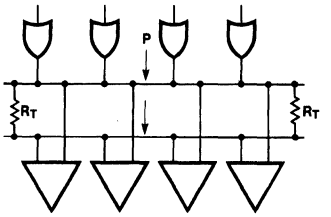
b. Differential Transmission Reception



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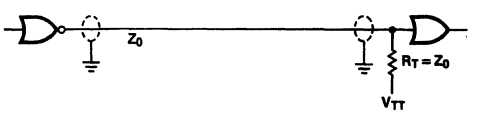
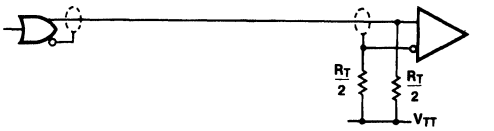
c. Backplane Data Bus

FIGURE 2-15. Twisted Pair Connections



TL/F/12655–27

a. Single-Ended Coaxial Transmission



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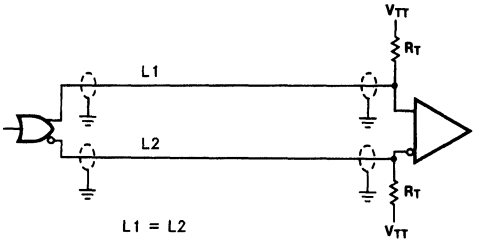
b. Differential Coaxial Transmission



TL/F/12655–29

c. Differential Transmission with Grounded Shields

FIGURE 2-16. Coaxial Cable Connections

References

1. Kaupp, H. R., "Characteristics of Microstrip Transmission Lines," *IEEE Transaction on Electronic Computers*, Vol. EC-16 (April, 1967).
2. Harper, C. A., *Handbook of Wiring, Cabling and Interconnections for Electronics.* New York: McGraw-Hill, 1972.
3. True, K. M., "Data Transmission Lines and Their Characteristics," AN-806.
4. True, K. M., "Reflections: Computations and Waveforms," AN-807.
5. True, K. M., "Long Transmission Lines and Data Signal Quality," AN-808.
6. Goldie, John, "FAILSAFE Biasing of Differential Buses," AN-847.
7. Vo, Joe, "A Comparison of Differential Termination Techniques," AN-903.
8. Fowler, Bill, "Transmission Line Characteristics," AN-108.

National Semiconductor

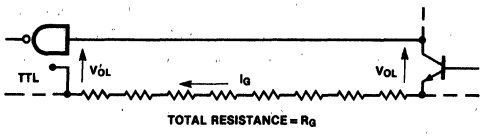
Chapter 3
Power Distribution and Thermal Considerations

Introduction

High-speed circuits generally consume more power than similar low-speed circuits. At the system level, this means that the power supply distribution system must handle the larger current flow; the larger power dissipation places a greater demand on the cooling system. The direct current (DC) voltage drop along ground busses affects noise margins for all types of circuits.

Logic Circuit Ground

The negative potential ground in circuits is the reference voltage for output voltages and input thresholds. When two circuits are connected in a single-ended mode, any difference in ground potentials decreases the noise margins. This effect for TTL circuits is illustrated in *Figure 3-1*. The following analysis assumes some average value of current flowing through the distributed resistance along the ground path between two circuits. For the indicated direction of I_G, the shift in ground potential *decreases* the LOW-state noise margin of the TTL circuits. If I_G is flowing in the opposite direction, it *increases* these noise margins, but *decreases* the noise margins when the drivers are in the opposite state. Logic boards which use microstrip or stripline techniques generally have large areas of ground metal. This causes the ground resistance to be quite low and thus minimizes noise margin loss between pairs of circuits on the same board.



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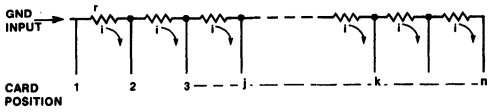
TTL

$V'_{OL} = V_{OL} = +I_G R_G$

$I_G R_G = (V'_{OL} - V_{OL})$ = Noise Margin Decrease

FIGURE 3-1. Effect of Ground Resistance on Noise Margins

In practice, two communicating circuits might be located on widely separated PC cards with other PC cards in between. The net resistance then includes the incremental resistance of the ground distribution bus from card to card, while the ground current is successively increased by the contribution from each card. *Figure 3-2* illustrates a distribution bus for a row of cards with incremental resistances along the bus.



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r = Incremental Bus Resistance between Positions
i = Average Ground Current per Card

FIGURE 3-2. Ground Shift Along a Row of PC Cards

The ground shift can be estimated by first determining an average value of current per card based on the number of packages, the mix of SSI and MSI, and the number and types of terminations. With n cards in the row, an average ground current (i) per card, and an incremental bus resistance (r) between card positions, the bus voltage drops between the various positions can be determined as follows:

between positions 1 and 2: $v_{1-2} = (n-1)\,ir$

between positions 1 and 3: $v_{1-3} = (n-1)\,ir + (n-2)\,ir$

between positions 1 and 4: $v_{1-4} = (n-1)\,ir + (n-2)\,ir + (n-3)\,ir$

between 1 and n:

$$v_{1-n} = ir\{(n-1) + (n-2) + (n-3) + \ldots + [n-(n-1)]\}$$
$$= ir[1 + 2 + 3 + \ldots + (n-1)]$$
$$v_{1-n} = ir \sum_{1}^{n-1} n$$

For a row of 15 cards, for example, the total ground shift between positions 1 and 15 is expressed as in Equation 5-1.

$$v_{1-15} = ir \sum_{1}^{14} n = ir\,(1 + 2 + 3 + \ldots + 13 + 14) \quad (3\text{-}1)$$
$$= 105\ ir$$

Logic Circuit Ground (Continued)

The ground shift between any two card positions j and k can be determined as follows for the general case.

$$v_{j-k} = (n - j)\,ir + [n - (j + 1)]\,ir + [n - (j + 2)]\,ir + \ldots + \{n - [j + (k\text{-}j\text{-}1)]\}\,ir$$

$$= (k - j)\,nir - ir\{j + (j + 1) + (j + 2) + \ldots + [j + (k\text{-}j\text{-}1)]\} \quad (3\text{-}2)$$

$$v_{j-k} = (k - j)\,nir - ir\sum_{j}^{k-1} n = ir\left[(k - j)\,n - \sum_{j}^{k-1} n\right]$$

In a row of 15 cards, the ground shift between positions four and nine, for example, is determined as follows.

$$v_{j-k} = ir\,[(9 - 4)\,15 - (4 + 5 + 6 + 7 + 8)] \quad (3\text{-}3)$$
$$= ir\,(75 - 30) = 45\,ir$$

The ground shift between the same number of positions further down the row is less because of the decreasing current along the row. Consider the ground shift between card positions 10 and 15.

$$v_{10-15} = ir\,[(15 - 10)15 - (10 + 11 + 12 + 13 + 14)] \quad (3\text{-}4)$$
$$= ir\,(75 - 60) = 15\,ir$$

These examples illustrate several principles the designer should consider regarding the ground distribution bus and assignment of card positions. The bus resistance should be kept as low as possible by making the cross-sectional areas as large as practical. Logic cards which represent the heaviest current drain should be located nearest the end where ground comes into the row of cards. Cards with single-ended logic wiring between them should be assigned to positions as close together as possible. Conversely, if the ground shift between two card positions represents an unacceptable loss of noise margin, then the differential transmission and reception method i.e., twisted pair, should be used for logic wiring between them, thereby eliminating ground shift as a noise margin factor.

Conductor Resistances

Conductors with large cross-sectional areas are required to maintain low voltage drops along power busses. For convenience, *Figure 3-3* lists the resistance per foot and the cross-sectional area for more common sizes of annealed copper wire. Other characteristics and a complete list of sizes can be found in standard wire tables. A useful rule-of-thumb regarding resistances and, hence, areas is: as gauge numbers increase, resistance doubles with every third gauge number; e.g., the resistance per foot of #10 wire is 1 mΩ, for #13 wire it is 2 mΩ. Similarly, the resistance per foot of #0 wire is 0.078 mΩ, which is half that of #2 wire.

For calculations involving conductors having rectangular cross sections, it is often convenient to work with sheet resistance, particularly for power distribution on PC cards. Copper resistivity is usually given in ohm-centimeters, indicating the resistance between opposing faces of a 1 cm cube. The sheet resistance of a conductor is obtained by dividing the resistivity by the conductor thickness. These relationships follow.

AWG B & S Gauge	Resistance mΩ Per Foot	Cross-Sectional Area Square Inches
#2	0.156	5.213×10^{-2}
#6	0.395	2.062×10^{-2}
#10	0.999	8.155×10^{-3}
#12	1.588	5.129×10^{-3}
#18	6.385	1.276×10^{-3}
#22	16.14	5.046×10^{-4}
#26	40.81	1.996×10^{-4}
#30	103.2	7.894×10^{-5}

FIGURE 3-3. Resistance and Cross-Sectional Area of Several Sizes of Annealed Copper Wire

Copper resistivity = $\rho = 1.724 \times 10^{-6}\ \Omega$cm @ 20°C

Resistance of a conductor = $\rho\frac{l}{A} = \rho\frac{l}{tw}$

where: l = length t = thickness w = width

Sheet resistance $\rho_S = \frac{\rho}{t}\ \Omega$ per $\frac{l}{w}$

The length/width ratio (l/w) is dimensionless; therefore, the resistance of a length of conductor of uniform thickness can be calculated by first determining the number of "squares," then multiplying by the sheet resistance. For example, a conductor one-eighth inch wide and three inches long has 24 squares; its resistance is 24 times the sheet resistance. Since many thickness dimensions are given in inches, it is convenient to express the resistivity in ohm-inch, as follows.

$\rho(\Omega\text{in.}) = \rho(\Omega\text{cm}) \div 2.54 = 6.788 \times 10^{-7}\ \Omega$in.

The use of sheet resistance and the "squares" concept is illustrated by calculating the resistance of the conductor shown in *Figure 3-4*. Assume the conductor is a 1 oz. copper cladding with a 0.0012 inch minimum thickness on a PC card.

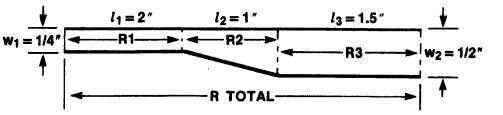

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FIGURE 3-4. Conductor of Uniform Thickness but Non-Uniform Cross Section

Sheet resistance = $\rho_S = \frac{\rho}{t}$

$= 5.657 \times 10^{-4}\ \Omega$ per square

The number of squares S for the rectangular sections are as follows.

$$S1 = \frac{l_1}{w_1} = 8 \qquad S_3 = \frac{l_3}{w_2} = 3$$

The middle average segment of the conductor has a trapezoidal shape. The average of w_1 and w_2 can be used as the effective width, within 1% accuracy, if the w_2/w_1 ratio is 1.5 or less. Otherwise, a more exact result is obtained as follows.

$$S_2 = \frac{l_2}{w_2 - w_1}\ln\left(\frac{w_2}{w_1}\right) = 4\ln 2 = 2.77\ \text{squares} \quad (3\text{-}5)$$

Total $R = R_1 + R_2 + R_3 = \rho_s(S_1 + S_2 + S_3)$

$= 7.51\ m\Omega$

Conductor Resistances (Continued)

As another example, assume that a 1 oz. trace must carry a 200 mA current six inches with a voltage drop less than 10 mV.

$$R_{max} = \frac{V_{max}}{I} = \frac{0.01}{0.2} = 0.05\Omega$$

$$0.05 = \rho_s \frac{l}{w} \qquad (3\text{-}6)$$

$$\frac{w}{l} = 20\,\rho_s$$

$$w = 120\,\rho_s = (120)\,5.657 \times 10^{-4} = 67.9 \times 10^{-3}$$

$\therefore$ minimum trace width, w = 68 mils

At a higher current level, consider the voltage drop in a conductor 20 mils thick, 1.25 inches wide and 3 feet long carrying a 50A current.

$$\rho_s = \frac{6.788 \times 10^{-7}}{2 \times 10^{-2}} = 3.364 \times 10^{-5}\ \Omega \text{ per square}$$

$$V = IR - (50)\,(3.364 \times 10^{-5})\,\frac{36}{1.25} \qquad (3\text{-}7)$$

$$= 0.0484 = 48.4 \text{ mV}$$

Sheet resistances for various copper thicknesses are listed in *Figure 3-5*. Standard thicknesses and tolerances for copper cladding are tabulated in *Figure 3-6* and resistance per foot as a function of width is shown in *Figure 3-7*.

Weight or Thickness	Sheet Resistance Ω per Square	Thickness	Sheet Resistance Ω per Square
2 oz.	2.715×10^{-4}	0.02 in.	3.364×10^{-5}
3 oz.	1.886×10^{-4}	0.05 in.	1.358×10^{-5}
5 oz.	1.077×10^{-4}	1/16 in.	1.086×10^{-5}
0.01 in.	6.788×10^{-5}	1/4 in.	2.715×10^{-6}

FIGURE 3-5. Sheet Resistance for Various Thicknesses of Copper

Nominal Thickness		Nominal Weight	Tolerances By	
in.	mm	oz/ft²	Weight, %	in.
0.0007	0.0178	½	+10	+0.0002
0.0014	0.0355	1	+10	+0.0004 −0.0002
0.0028	0.0715	2	+10	+0.0007 −0.0003
0.0042	0.1065	3	+10	+0.0006
0.0056	0.1432	4	+10	+0.0006
0.0070	0.1780	5	+10	+0.0007
0.0084	0.2130	6	+10	+0.0008
0.0098	0.2460	7	+10	+0.001
0.014	0.3530	10	+10	+0.0014
0.0196	0.4920	14	+10	+0.002

FIGURE 3-6. Thickness and Tolerances for Copper Cladding

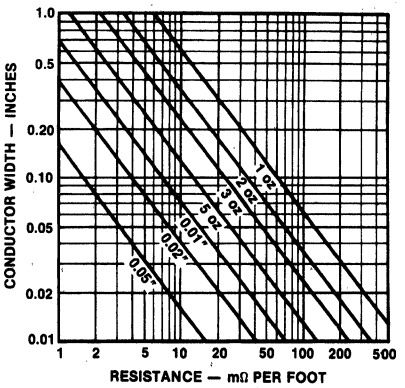

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FIGURE 3-7. Conductor Resistance vs Thickness and Width

Temperature Coefficient

The resistances in *Figures 3-3, 3-5,* and *3-7*, as well as those used in the sample calculations, are 20°C values. Since copper resistivity has a temperature coefficient of approximately 0.4%/°C, the resistance at a temperature (T) can be determined as follows.

$$R_T = R_{20°C}\,[1 + 0.004\,(T + 20°C)]$$

At 55°C: (3-8)

$$R = R_{20°C}\,[1 + 0.004\,(55°C - 20°C)] = 1.14\,R_{20°C}$$

When specifying power bus dimensions for PC cards containing many IC packages, designers should bear in mind that excessive current densities can cause the copper temperature to rise appreciably. *Figure 3-8* illustrates the ohmic heating effect of various current densities.[1]

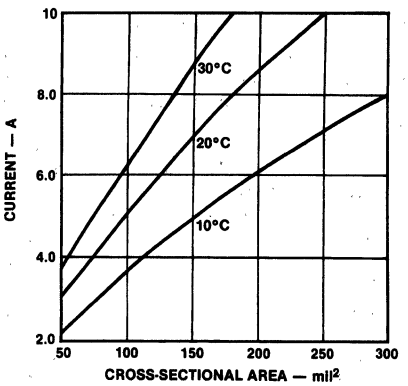

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FIGURE 3-8. Temperature Rise with Current Density in PC Board Traces

Distribution Impedance

Power busses should have low AC impedance, as well as low DC resistance, to prevent propagation of extraneous disturbances along the distribution system. As far as current or voltage changes are concerned, power and ground busses appear as transmission lines; thus their impedances can be affected by shape, spacing and dielectric. The effect of geometry on impedance is illustrated in the two arrangements of *Figure 3-9*. The same cross-sectional area of copper is used, but the two round wires have an impedance of about 75Ω while the flat conductors have an impedance determined as follows.

$$Z_0 = \frac{377\,d}{\sqrt{\epsilon}\,h} \text{ for } \frac{d}{h} < 0.1$$

With a Mylar®* or Teflon®* dielectric (ϵ = 2.3) two mils thick, impedance of the flat conductor pair is only 0.5Ω. Power line impedance can be reduced by periodically connecting RF-type capacitors across the line.

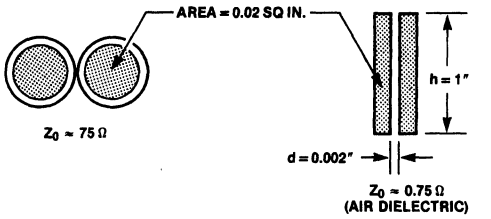

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FIGURE 3-9. Effect of Geometry on Power Bus Impedance

*Mylar and Teflon are registered trademarks of E.I. du Pont de Nemours Company.

Ground on PC Cards

It is essential to assign one layer of copper cladding almost exclusively to ground. This provides low-impedance, non-interfering return paths for the current changes which travel along signal traces when the IC outputs change state. These currents flow from the V_{CC} pins of the IC packages, through the output transistors, then into the loads and the stray capacitances. These stray capacitances exist from an output to ground and to other signal lines. Thus, displacement currents through stray capacitances flow in many paths, but must ultimately return through ground to the output transistor where they originated. To reduce the length and impedance of the return path, the ground metal should cover as large an area as possible and one decoupling capacitor should be provided for every one to two IC packages. Additional capacitors may be needed for multiple output devices. These capacitors should be ceramic, monolithic or other RF types in the 0.01 μF to 0.1 μF range.

The load current returning to an IC package through ground metal is predictable, both in magnitude and in the return path. Since the magnetic and capacitive coupling between a signal trace and the underlying ground provides the transmission line characteristic, it follows that the load current flowing through the signal trace is accompanied by a ground return current equal in magnitude but opposite in direction. For example, in a 50Ω terminator I_{OL} is 5.9 mA, I_{OH} is 20.9 mA. Then signal change will cause about 15 mA current change and, as this current change propagates along the signal trace, a current of −15 mA advances along the ground directly underneath the signal trace. Therefore, if there is an interruption in the ground, the return current is forced to go around it. When it is necessary to interrupt the ground plane, the interruptions should be kept as short as possible; every effort should be made to locate them away from overlying signal lines. When the ground plane is interrupted for short signal lines between packages, these lines should be at right angles to signal lines on the other side to minimize coupling. The V_{CC} plane can also act as the return side of transmission lines, as long as de-coupling capacitors to ground are placed in the immediate areas where the signal return current must continue through ground.

Several connections along the edge of a PC card should be assigned to ground to accommodate backplane signal ground. These should be spaced at one-half to one inch intervals to minimize the average path length for signal return currents and to simulate a distributed connection to the backplane signal ground.

Not enough emphasis can be placed on the requirement for a good ground. All input signals are referenced to ground. Any variation from one side of the board to the other affects the noise margins.

Backplane Construction

In order to take complete advantage of the speeds inherent in modern logic it is desirable to construct the backplane as a multilayer printed circuit board. Generally, two internal layers are devoted to ground and V_{CC} and the signals occupy the outside layers. Where power densities are very high, it may be necessary to supplement the power layers with external busses (see Backplane Interconnections, *Chapter 2*).

If it is necessary to use wires to augment the interconnection provided by the traces, less critical signals should use the wires. The wires will exhibit an impedance which can be calculated with the wire-over-ground formula

$$Z_0 = \frac{138}{\sqrt{\epsilon}} \text{Log}_{10} \frac{4h}{d} \qquad (3\text{-}9)$$

where d is diameter, h is distance to ground, and ϵ is dielectric constant.

Bear in mind that if the ground plane is buried inside the board, then both h and ϵ are made up of multiple components.

Reference

1. Harper, C.A., Editor, *Handbook of Wiring, Cabling and Interconnecting for Electronics*, McGraw-Hill, 1972.

National Semiconductor

Chapter 4

Decoupling Requirements

National Semiconductor's Line Drivers, as with other high-performance, high-drive devices, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with Interface products.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. *Figure 4-1* displays various V_{CC} and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50Ω and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in *Figure 4-2* to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100Ω bus from a point somewhere in the middle.

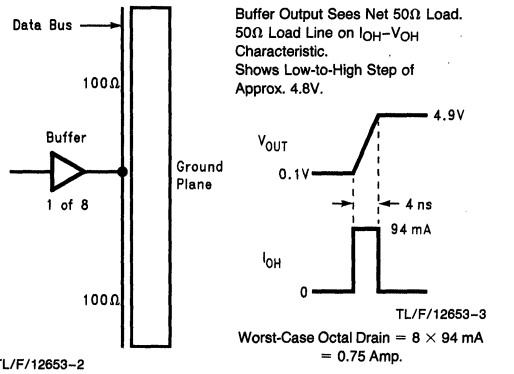


FIGURE 4-2. Octal Buffer Driving a 100Ω Bus

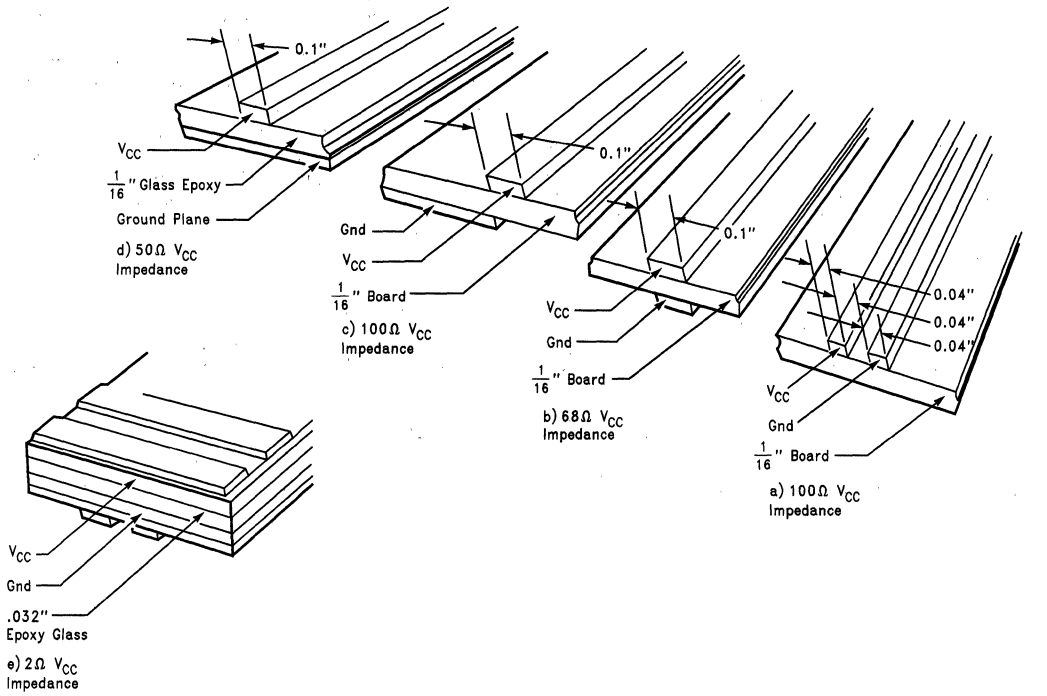


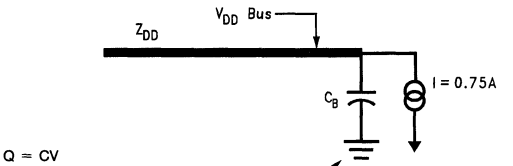
FIGURE 4-1. Power Distribution Impedances

Decoupling Requirements (Continued)

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in *Figure 4-3*.

In this example, if the V_{CC} droop is to be kept below 30 mV and the edge rate equals 4 ns, a 0.10 μF capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the devices, placing one capacitor for every package as shown in *Figure 4-4*.



$Q = CV$
$I = C\Delta V/\Delta t$
$C = I\Delta t/\Delta V$
$\Delta t = 4 \times 10^{-9}$

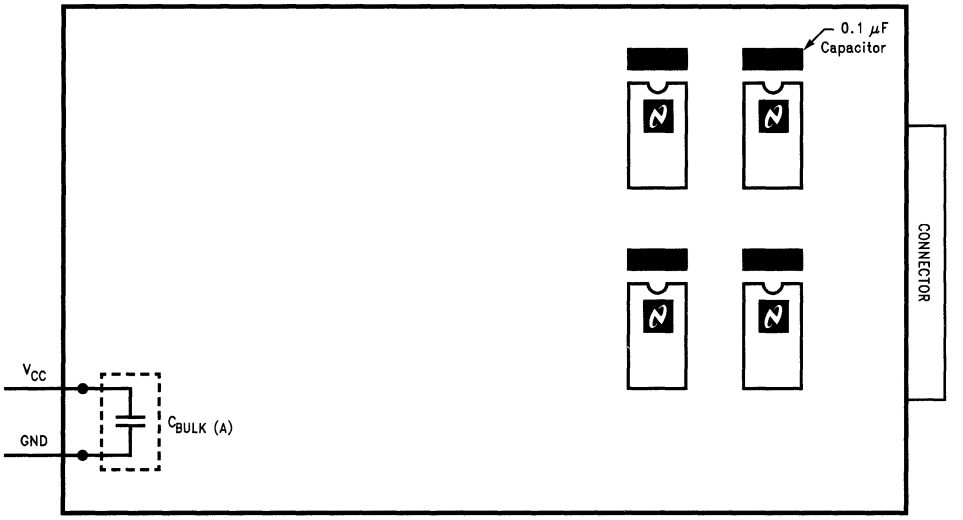
$$C = \frac{0.750 \times 4 \times 10^{-9}}{0.03} = 100 \times 10^{-9} = 0.100\ \mu F$$

Select $C_B \geq 0.10\ \mu F$

FIGURE 4-3. Formula for Calculating Decoupling Capacitors

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.



- Need to decouple board at the point of power supply entry
- This capacitor (A) will smooth low frequency bulk switching noise
- A large value electrolytic capacitor is typically used (50 μF–100 μF)

FIGURE 4-4. Board-Level Decoupling Capacitor

Section 13
Modeling Support

Section 13 Contents

National Semiconductor

An Introduction to IBIS Modeling

(I/O Buffer Information Specification)

Syed B. Huq

INTRODUCTION

With time to market becoming shorter and shorter, system designers are struggling to release a product from concept to reality in a tightly budgeted time. The need to simulate before prototyping is very essential and the ability to simulate and simulate accurately has heightened even more. But in order to simulate a system level board, all components on the board need to be modeled. Unfortunately many device models are not readily available from vendors.

IBIS (I/O Buffer Information Specification) is a Behavioral Modeling Specification that is gaining world wide popularity as a standard format to generate device models. IBIS solves many of the problems that prevented system designers from obtaining semiconductor vendor's SPICE models.

This application note discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

ABOUT IBIS...

I/O Buffer Information Specification is a fast and accurate behavioral method of modeling input/output buffers based on V/I curve data derived from measurement or full circuit simulation. It uses a standardized software parsable format in the form of an ASCII file to store the Behavioral Information needed to model device characteristics of integrated circuits.

IBIS can be used by almost any Simulators/EDA tools in the industry. A wide range of Industry leaders support the IBIS open forum. Below is a partial list of vendors supporting the IBIS method of model generation.

Cadence Design Systems (SigNoise)
Quantic Laboratories (Greenfield)
MicroSim Corporation (PSPICE)
Integrity Engineering (SimnetX)
Interconnectix Inc. (IS)
Mentor Graphics Corp. (Accusim)
INCASES (FREACS)
Tanner Research (TSPICE)
Zuken-Redac
HyperLynx (LineSim PRO)
Meta-Software (HSPICE)
IntuSoft (IS_SPICE)
Anacad (Eldo)
Contec Microelectronics (ContecSPICE)
Quad Design Technology (XTK/TLC)
Symmetry Design Systems (MODPEX)
UniCAD Canada (UniSolve)

HISTORY OF IBIS

The originator of IBIS was Intel. Presently the standard is being driven by the IBIS forum with over 35 members consisting of EDA vendors, Computer manufacturers, Semiconductor vendors and Universities.

IBISv1.0 was released in April 1993. IBISv1.0 is capable of modeling standard TTL or CMOS type of I/O structure. In June 1993 at the DAC (Design Automation Conference) show in Dallas, IBISv1.1 was released. The major changes were the addition of more comments to the original specification.

IBISv2.0 was ratified in June 1994 at the DAC conference in San Diego. IBISv2.0 is a considerable improvement over IBISv1.1. Some of the added features are, Multiple rail support (ex. V+ and V− supply for RS-232), ECL, Terminator models, Open drain, Open collector, Differential I/O, Controlled slew rate and Definitions of complex package parameters to name a few.

IBISv2.1 added more comments to clarify v2.0 and has been ratified December 1994. Today IBIS is an approved standard within EIA (Electronic Industry Association) and is also known under ANSI/EIA-656.

The software parser (known as the *"Golden Parser"*) validates the IBIS model file. The *Golden Parser* checks the syntax of the IBIS model file to confirm that the data format meets the IBIS specification. The object code of the parser is available for free from the forum. Simulator vendors may also purchase the source code for a fee.

IBIS is backwards compatible. So all models created today using the present version of the specification are guaranteed to work with future versions of IBIS. The IBIS forum is continually defining new and improved ways of modeling complex and unique I/O structures.

ADVANTAGES OF IBIS

The IBIS model file protects proprietary information about the modeled circuit as no process or circuit design information is disclosed. A SPICE model on the other hand can disclose substantial information that Semiconductor vendors consider to be confidential such as circuit nodal connections and process parameters. IBIS models are accurate, as non-linear aspects of I/O structures as well as package parasitic and ESD structures are considered in the model parameters. Since IBIS is behavioral, the simulation time for an IBIS model can run 25× faster than a structural model (SPICE). IBIS does not have non-convergence issues like SPICE and can practically run on any Industry wide platforms as most EDA vendors support the IBIS specification. One of the most popular uses of IBIS is for Signal Integrity Analysis on system boards. The models are very easy to create as they can be made from bench measurements or from simulation data.

Following is a behavioral block diagram of IBIS (*Figure 1*) and the pieces needed to create an Input and an Output model.

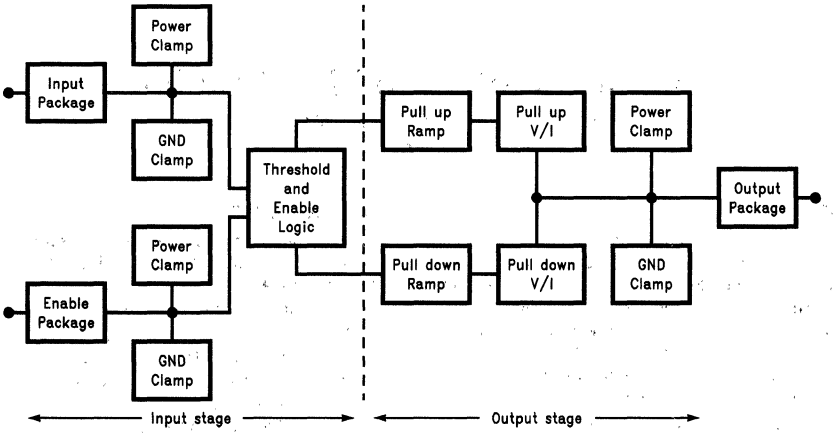


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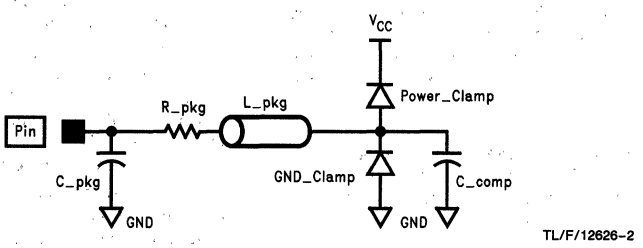
FIGURE 1. Behavioral Diagram of IBIS

INPUT STRUCTURE MODEL

Information needed to model the Input Structure is shown in *Figure 2.* C_pkg, R_pkg and L_pkg are the package parameters. Power_Clamp and GND_Clamp defines the ESD structures on the Inputs. The V/I curve data defines these clamp structures. C_comp is the input capacitance of the input pin.

OUTPUT STRUCTURE MODEL

Information needed to model the output structure is shown in *Figure 3.* Pullup defines V_{OH}/I_{OH}, Pulldown defines the V_{OL}/I_{OL} and Ramp defines the dV/dt of the Rising and Falling waveforms.



TL/F/12626–2

FIGURE 2. Input/Enable Structure Model

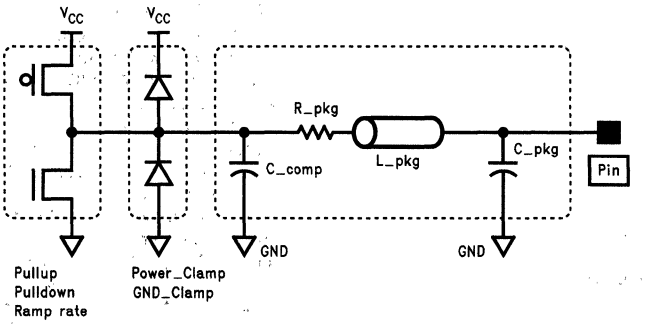


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FIGURE 3. Output Structure Model

The Pullup and Pulldown data are created from the V/I curves. The remaining parameters are similar to the Input structure except that they define the package parasitic of the output pin as well as the output capacitance of the output pin.

The Pullup and Power_clamp data are "V_{CC} relative", meaning that the voltage values are referenced to V_{CC} and not ground. So the voltages in the tables are derived from the equation: $V_{table} = V_{CC} - V_{output}$. V_{CC} relative data is necessary for the simulator as the Pullup structure depends on the voltage between the output and V_{CC} and not the voltage between the output and ground pin.

An Interconnect engineer can create a slow and a fast model using IBIS. The slow model is useful to determine flight time and the fast model is useful to analyze overshoot, undershoot, crosstalk, etc. By combining min I_{OH}/I_{OL} with max ramp time and max package parameters, a slow model is generated. To create a fast model, the max I_{OH}/I_{OL}, min ramp and minimum package information is used.

MODEL GENERATION FLOW

The following steps are used in generating an IBIS model. All necessary V/I and other parameters need to be either measured on the bench, obtained from simulation or provided by the semiconductor vendor.

Measurements of package parameters can be made through TDR (Time Domain Reflectometry) techniques if they are not available from the semiconductor vendor. V/I data can be collected using a curve tracer or programmable supply with sinking and sourcing capabilities. Clamp curves can be generated by putting the device in TRI-STATE® and sweeping the I/O. For non TRI-STATE devices, the V/I curves are the summation of the Clamp and Pullup/Pulldown.

The required data is: R_pkg, L_pkg, C_pkg and C_comp for all Inputs and Outputs and Enables. Power_Clamp and GND_Clamp (ESD structures if present) for I/O. Pullup, Pulldown and Ramp rates for Outputs.

The Interconnect engineer then creates the IBIS ASCII file following the format defined in the IBIS standard. This can be done on a UNIX or DOS text editor. An example of a sample IBISv2.1 model file is shown later.

The ASCII model file is then checked by the *"Golden Parser"* for possible syntax errors. If passed, the model is then imported into a simulator and validated for accuracy. Now the model is ready for use. *Figure 4* shows this flow in a graphical form.

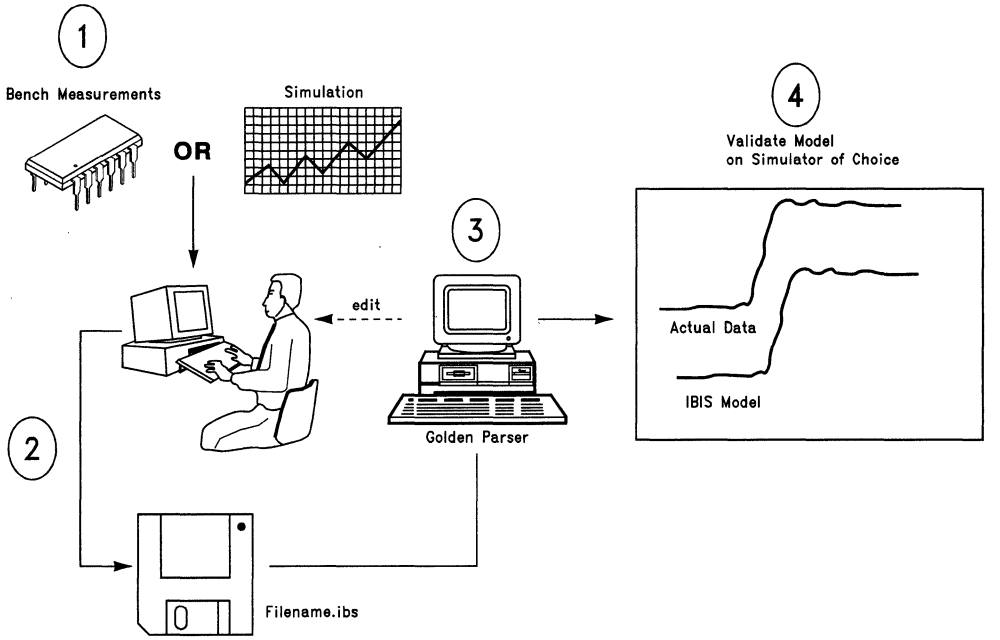

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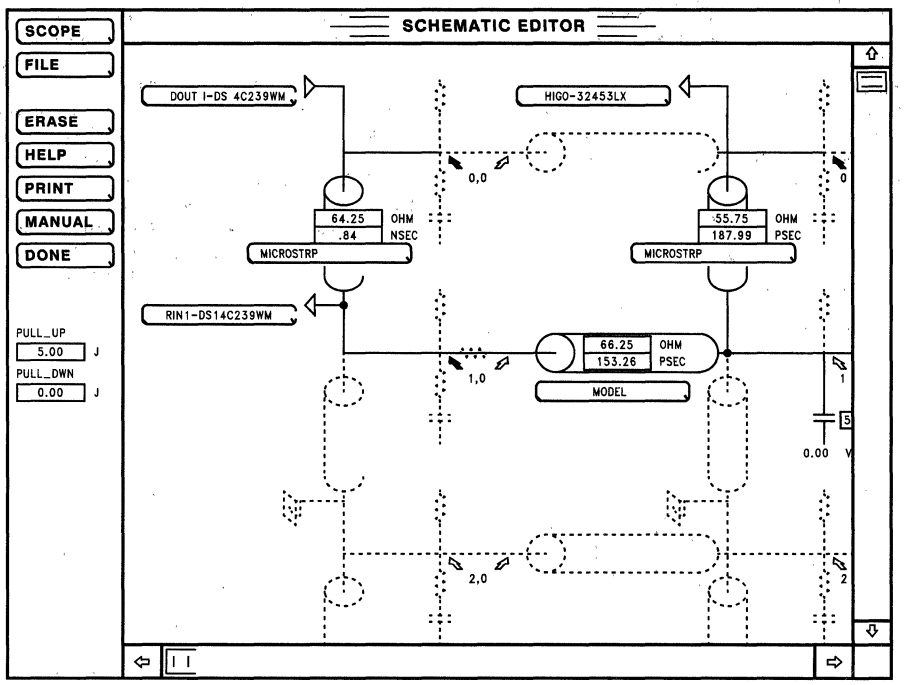
FIGURE 4. IBIS Model Generation Flow

MODEL VALIDATION ON SIMULATOR

Interface Applications has generated IBIS models and has used LineSim PRO (HyperLynx) simulator for model validation. LineSim PRO can simulate a system board by using different transmission elements with different characteristics and connecting them together. These transmission elements can be microstrip, strip-line or cables/connectors.

Figure 5 shows a typical Driver output driving a microstrip line 12 inches long with a Receiver on the other end. *Figure 6* shows the simulated Rise time of the receiver output. Measurements can be made on the simulated waveform to make sure they match the data previously collected for the particular device.



TL/F/12626–5

FIGURE 5. Schematic Editor of LineSim PRO

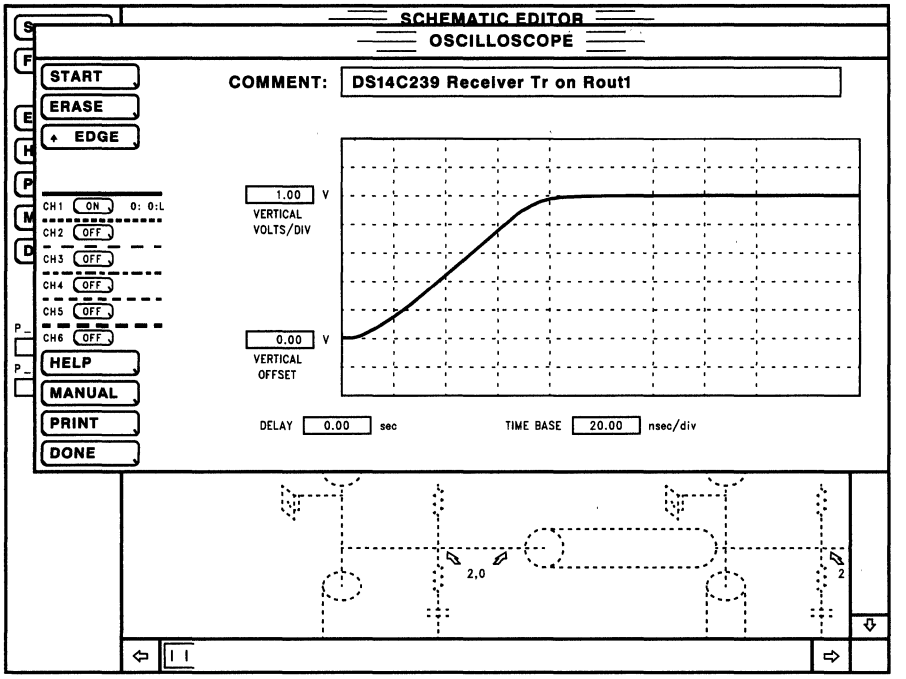


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FIGURE 6. Rise Time Simulation

The Interconnect engineer may use any simulator of choice that supports the IBIS format for model validation.

FUTURE TRENDS OF IBIS

Since its formation in 1993, IBIS has improved it's specification by many folds. More complex modeling features and possibly timing analysis may be added to future IBIS specifications. DIE (Die Information Exchange) forum which specifies DIE information for MCM applications references IBIS as the Signal Integrity Analysis specification. FMF (Free Model Forum), OMF (Open Model Forum), CFI (CAD Framework Initiative) are some of the other forums that references IBIS for behavioral modeling.

NATIONAL AND IBIS

Interface applications is actively generating IBIS models for its products. Interface Applications actively participates in IBIS forum meetings and was very instrumental in adding the Differential I/O specification to IBISv2.1.

CONCLUSION

IBIS modeling is accurate, easy to create and compatible on a wide rage of Simulation platforms. It solves the *"NO MODELS AVAILABLE"* problem in the industry. IBIS has created a common Industry format for modeling using Behavioral information and does not disclose any propietary process parameters or circuit design details.

National Semiconductor

Sample IBIS Model

```
|*************************************************************************
|            National Semiconductor Corporation
|              Interface Products Group
|               IBIS Model of DS26C31TN
|                 16L DIP Package
|*************************************************************************
|
[IBIS Ver]    2.1
[Comment char]                |_char
[File name]   ds26c31.ibs
[File Rev]    1.0
[Date]        2/09/95
[Source]      File originated at National Semiconductor Corporation.
              Interface Products group. All data based on
              Empirical Measurements(Bench).
[Notes]       File created by SBH.
[Disclaimer]
```


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```
Contact National at ATTN:INTERFACE APPLICATIONS/IBIS MODELS.
2900 Semiconductor Drive, M/S A2595, Santa Clara, CA 95052-8090
|
[Disclaimer] IBIS Open Forum disclaims all warranties. See DISCLAIM.TXT
 in vhdl.org:/pub/IBIS/models for the full disclaimer.
|
|*****************************************************************************
[Copyright]    Copyright 1994, National Semiconductor, All Rights Reserved
[Component]    DS26C31TN
[Manufacturer] National Semiconductor Corp
[Package]
|                 typ         min         max
R_pkg             50.0m       NA          NA
L_pkg             1.37nH      NA          NA
C_pkg             0.26pF      NA          NA
|
|*****************************************************************************
|
[Pin]  signal_name    model_name R_pin    L_pin    C_pin
|
1      DIN1           DS26C31T_DIN
2      DOUT1+         DS26C31T_DOUT
3      DOUT1-         DS26C31T_DOUT
4      EN             DS26C31T_EN
5      DOUT2-         DS26C31T_DOUT
6      DOUT2+         DS26C31T_DOUT
7      DIN2           DS26C31T_DIN
8      GND            GND
9      DIN3           DS26C31T_DIN
10     DOUT3+         DS26C31T_DOUT
11     DOUT3-         DS26C31T_DOUT
12     EN*            DS26C31T_EN
13     DOUT4-         DS26C31T_DOUT
14     DOUT4+         DS26C31T_DOUT
15     DIN4           DS26C31T_DIN
16     VCC            POWER
|
[Diff_pin]  inv_pin   vdiff   tdelay_typ   tdelay_min   tdelay_max
|
| The '+' pin is Diff_pin and the '-' pin is the inv_pin
|
2        3     NA     0 0 0
6        5     NA     0 0 0
10      11     NA     0 0 0
14      13     NA     0 0 0
```

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```
|
|*******************************************************************************
|              Driver Input  MODEL
|*******************************************************************************
|
[Model]        DS26C31T_DIN
Model_type     Input
|Signals       DIN1,DIN2,DIN3,DIN4
Vinh = 2.0
Vinl = 0.8
|                typ          min          max
C_comp         1.0pF        NA           NA
|
|*******************************************************************************
|
|                              typ          min          max
[Temperature Range]          25.0         NA           NA
[Voltage range]              5.0V         4.5V         5.5V
|
|*******************************************************************************
|
|
[Power_clamp]
|-------------------------------------------------------------
| Note that the[POWER_clamp]voltage table is referenced to Vcc
| and is calculated using Vtable=Vcc - Vmeasured.
|-------------------------------------------------------------
|    Voltage      I(typ)      I(min)      I(max)
|
       0.00V      0.0mA       NA          NA
      -0.20V      0.0mA       NA          NA
      -0.36V      0.0mA       NA          NA
      -0.50V      0.0mA       NA          NA
      -0.63V      0.06mA      NA          NA
      -0.66V      0.23mA      NA          NA
      -0.70V      0.66mA      NA          NA
      -0.73V      1.44mA      NA          NA
      -0.75V      1.88mA      NA          NA
      -0.77V      3.06mA      NA          NA
      -0.78V      4.42mA      NA          NA
      -5.00V      578.34mA    NA          NA
|
```

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[GND_clamp]

Voltage	I(typ)	I(min)	I(max)
5.00V	2.29mA	NA	NA
-0.08V	0.4mA	NA	NA
-0.60V	0.2mA	NA	NA
-0.66V	0.0mA	NA	NA
-0.68V	-0.4mA	NA	NA
-0.70V	-1.6mA	NA	NA
-0.72V	-2.2mA	NA	NA
-0.74V	-2.8mA	NA	NA
-0.76V	-4.6mA	NA	NA
-0.78V	-6.4mA	NA	NA
-0.80V	-8.6mA	NA	NA
-0.82V	-11.2mA	NA	NA
-0.84V	-13.6mA	NA	NA
-0.86V	-18.6mA	NA	NA
-0.88V	-23.6mA	NA	NA
-0.90V	-28.0mA	NA	NA
-0.92V	-35.2mA	NA	NA
-0.94V	-41.0mA	NA	NA
-0.96V	-47.8mA	NA	NA
-0.98V	-59.8mA	NA	NA
-1.00V	-63.8mA	NA	NA
-1.02V	-72.4mA	NA	NA
-1.04V	-83.2mA	NA	NA
-5.00V	-2221.6mA	NA	NA

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```
|*******************************************************************************
|              Driver Enable  MODEL
|*******************************************************************************
|
[Model]        DS26C31T_EN
Model_type     Input
|Signals       EN,EN*
Vinh = 2.0
Vinl = 0.8
|                typ          min          max
C_comp           1.0pF        NA           NA
|
|*******************************************************************************
|
|                           typ          min          max
[Temperature Range]         25.0         NA           NA
[Voltage range]              5.0V         4.5V         5.5V
|
|*******************************************************************************
[GND_clamp]
|    Voltage          I(typ)        I(min)        I(max)
|
       5.00V          0.0mA         NA            NA
       0.00mV         0.0mA         NA            NA
    -300.0mV          0.0mA         NA            NA
    -400.0mV          0.0mA         NA            NA
    -500.0mV          0.0mA         NA            NA
    -600.0mV          0.0mA         NA            NA
    -660.0mV          0.0mA         NA            NA
    -730.0mV         -1.6mA         NA            NA
    -790.0mV         -4.8mA         NA            NA
    -820.0mV         -8.4mA         NA            NA
    -840.0mV        -12.2mA         NA            NA
    -855.0mV        -15.8mA         NA            NA
    -880.0mV        -19.2mA         NA            NA
    -900.0mV        -24.8mA         NA            NA
    -940.0mV        -35.8mA         NA            NA
   -1050.0mV        -71.6mA         NA            NA
   -1075.0mV        -79.6mA         NA            NA
   -1090.0mV        -87.0mA         NA            NA
   -1120.0mV        -96.0mA         NA            NA
    -5.00V         1260.0mA         NA            NA

|
|
```

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```
[Power_clamp]
|------------------------------------------------------------
| Note that the[POWER_clamp]voltage table is referenced to Vcc
| and is calculated using Vtable=Vcc - Vmeasured.
|------------------------------------------------------------
|    Voltage      I(typ)       I(min)      I(max)
|
|
       0.0V       0.0mA        NA          NA
      -0.52V      0.0mA        NA          NA
      -0.66V      0.6mA        NA          NA
      -0.70V      1.6mA        NA          NA
      -0.80V      9.5mA        NA          NA
      -0.92V     24.8mA        NA          NA
      -1.00V     33.0mA        NA          NA
      -1.06V     48.4mA        NA          NA
      -5.00V   1059.67mA       NA          NA

|*****************************************************************************
|              Driver Output MODEL
|*****************************************************************************
|
[Model]       DS26C31T_DOUT
Model_type    3-state
| Signals     DOUT1+,DOUT1-,DOUT2+,DOUT2-,DOUT3+,DOUT3-,DOUT4+,DOUT4-
Vmeas = 1.3V       |Reference voltage for timing measurements
Cref = 40pF        |Timing specification test load capacitance value
Rref = 100         |Note: 100 Ohm between the two driver outputs
Vref = 0           |Timing specification test load voltage; GND
| variable         typ          min         max
|
C_comp             3.0pF        NA          NA
|
|*****************************************************************************
|
|                          typ          min         max
[Temperature Range]       25.0         NA          NA
[Voltage range]           5.0V         4.5V        5.5V
|
|*****************************************************************************
|
```

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[Pulldown]

Voltage	I(typ)	I(min)	I(max)
10.00V	129.4mA	NA	NA
7.02V	114.5mA	NA	NA
6.72V	113.0mA	NA	NA
6.32V	112.0mA	NA	NA
6.08V	111.0mA	NA	NA
5.44V	110.0mA	NA	NA
4.80V	109.5mA	NA	NA
4.44V	109.0mA	NA	NA
4.14V	108.0mA	NA	NA
3.58V	106.5mA	NA	NA
3.14V	105.0mA	NA	NA
2.74V	103.0mA	NA	NA
2.66V	102.5mA	NA	NA
2.56V	101.5mA	NA	NA
2.42V	100.5mA	NA	NA
2.30V	99.5mA	NA	NA
2.20V	98.0mA	NA	NA
2.12V	97.0mA	NA	NA
2.08V	96.0mA	NA	NA
2.02V	95.0mA	NA	NA
1.92V	94.0mA	NA	NA
1.86V	92.0mA	NA	NA
1.76V	90.0mA	NA	NA
1.68V	88.0mA	NA	NA
1.56V	86.0mA	NA	NA
1.50V	83.5mA	NA	NA
1.44V	81.0mA	NA	NA
1.38V	79.5mA	NA	NA
1.32V	77.0mA	NA	NA
1.28V	75.0mA	NA	NA
1.22V	73.5mA	NA	NA
1.06V	66.5mA	NA	NA
0.96V	62.0mA	NA	NA
0.88V	57.0mA	NA	NA
0.78V	53.0mA	NA	NA
0.70V	47.0mA	NA	NA
0.60V	42.5mA	NA	NA
0.54V	38.0mA	NA	NA
0.46V	32.5mA	NA	NA
0.40V	29.0mA	NA	NA
0.32V	24.0mA	NA	NA
0.26V	19.0mA	NA	NA
0.18V	12.5mA	NA	NA
0.10V	7.5mA	NA	NA
0.00V	0.5mA	NA	NA
-0.02V	-2.5mA	NA	NA
-0.12V	11.5mA	NA	NA
-0.18V	-14.5mA	NA	NA
-0.34V	-28.5mA	NA	NA
-0.42V	-34.5mA	NA	NA

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-0.46V	38.5mA	NA	NA
-0.52V	-47.5mA	NA	NA
-0.56V	-53.0mA	NA	NA
-0.60V	-58.0mA	NA	NA
-0.66V	-63.5mA	NA	NA
-0.68V	-99.0mA	NA	NA
-0.70V	115.0mA	NA	NA
-0.72V	-129.0mA	NA	NA
-5.00V	3125.0mA	NA	NA

|
[Pullup]

Voltage	I(typ)	I(min)	I(max)

| Note that the[Pullup]voltage table is referenced to Vcc
| and is calculated using Vtable=Vcc - Vmeasured.

-5.00V	0.6mA	NA	NA
-4.88V	0.6mA	NA	NA
-4.50V	0.6mA	NA	NA
-4.22V	0.6mA	NA	NA
-4.10V	0.6mA	NA	NA
-4.00V	0.6mA	NA	NA
-3.92V	0.6mA	NA	NA
-3.82V	0.6mA	NA	NA
-3.62V	0.6mA	NA	NA
-3.46V	0.6mA	NA	NA
-3.36V	0.6mA	NA	NA
-3.30V	0.6mA	NA	NA
-3.10V	0.6mA	NA	NA
-3.05V	0.6mA	NA	NA
-2.98V	0.6mA	NA	NA
-2.50V	0.6mA	NA	NA
-2.00V	0.6mA	NA	NA
-1.42V	0.6mA	NA	NA
-1.00V	0.6mA	NA	NA
-0.10V	0.6mA	NA	NA
0.00V	0.6mA	NA	NA
0.40V	0.6mA	NA	NA
0.58V	0.6mA	NA	NA
0.72V	0.6mA	NA	NA
0.82V	0.4mA	NA	NA
0.92V	0.2mA	NA	NA
0.96V	0.0mA	NA	NA
0.98V	-0.8mA	NA	NA
1.02V	-1.2mA	NA	NA
1.04V	-1.6mA	NA	NA
1.06V	-2.2mA	NA	NA
1.08V	-3.0mA	NA	NA
1.12V	-3.6mA	NA	NA
1.16V	-5.0mA	NA	NA
1.18V	-6.2mA	NA	NA
1.20V	-7.0mA	NA	NA
1.22V	-7.8mA	NA	NA
1.26V	-8.8mA	NA	NA

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1.28V	-9.8mA	NA	NA
1.30V	-10.8mA	NA	NA
1.32V	-12.6mA	NA	NA
1.34V	-13.6mA	NA	NA
1.40V	-15.0mA	NA	NA
1.44V	-17.4mA	NA	NA
1.48V	-20.2mA	NA	NA
1.52V	-21.6mA	NA	NA
1.56V	-23.6mA	NA	NA
1.60V	-25.4mA	NA	NA
1.66V	-27.2mA	NA	NA
1.70V	-28.6mA	NA	NA
1.76V	-30.4mA	NA	NA
1.82V	-32.4mA	NA	NA
1.90V	-34.0mA	NA	NA
1.94V	-35.8mA	NA	NA
2.00V	-37.4mA	NA	NA
2.02V	-39.2mA	NA	NA
2.08V	-41.0mA	NA	NA
2.14V	-42.8mA	NA	NA
2.20V	-44.4mA	NA	NA
2.26V	-45.8mA	NA	NA
2.32V	-47.4mA	NA	NA
2.40V	-49.0mA	NA	NA
2.44V	-50.2mA	NA	NA
2.56V	-53.2mA	NA	NA
2.66V	-55.6mA	NA	NA
2.76V	-57.8mA	NA	NA
2.92V	-61.4mA	NA	NA
3.08V	-64.4mA	NA	NA
3.20V	-66.6mA	NA	NA
3.26V	-67.6mA	NA	NA
10.00V	179.93mA	NA	NA

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```
[GND_clamp]
|    Voltage        I(typ)        I(min)        I(max)
|-------------------------------------------------------------
| Outputs in Tri-state.
|-------------------------------------------------------------
|

        5.00V       6.7mA        NA          NA
      265.0mV       -0.4mA       NA          NA
       90.0mV       -0.8mA       NA          NA
      -30.0mV       -1.0mA       NA          NA
     -270.0mV       -1.2mA       NA          NA
     -540.0mV       -1.6mA       NA          NA
     -705.0mV       -2.0mA       NA          NA
     -850.0mV       -3.0mA       NA          NA
     -940.0mV       -4.4mA       NA          NA
    -1025.0mV       -5.8mA       NA          NA
    -1180.0mV       -9.2mA       NA          NA
    -1230.0mV       -10.8mA      NA          NA
    -1305.0mV       -13.8mA      NA          NA
    -1365.0mV       -16.6mA      NA          NA
    -1415.0mV       -19.6mA      NA          NA
    -1500.0mV       -25.4mA      NA          NA
    -1570.0mV       -31.8mA      NA          NA
    -1615.0mV       -39.0mA      NA          NA
       -5.00V       -649.2mA     NA          NA

|
[POWER_clamp]
    Voltage       I(typ)        I(min)        I(max)
|-------------------------------------------------------------
| Note that the[POWER_clamp]voltage table is referenced to Vcc
| and is calculated using Vtable=Vcc - Vmeasured.
| Outputs in Tri-state.
|-------------------------------------------------------------
     -9.80V      0.0mA         NA          NA
     -5.00V      0.0mA         NA          NA
      0.0V       0.0mA         NA          NA
      4.0V       0.0mA         NA          NA
      5.0V       0.0mA         NA          NA
|
|*****************************************************************************
|
[Ramp]
|                    typ         min          max
dV/dt_r          4.5/0.75n     NA          NA
dV/dt_f          4.6/0.90n     NA          NA
R_load = 100Ohm | Note: This 100 Ohm is across the two driver output
|
|
[End]
```

TL/F/12627–10

National Semiconductor

Listing of Available IBIS Models

Following is a listing of available IBIS models from the Interface Products Group. More and more models are being added on a regular basis. For an up to date listing in our library, visit the National Web site at:

http://www.natsemi.com

or the anonymous ftp site at **vhdl.org(198.31.14.3)** under

pub/ibis/models/national

File Name	Device ID	IBIS Version	Notes
ds26c31.ibs	DS26C31	2.1	RS-422 Quad Diff Line Drv
ds26c32.ibs	DS26C32	2.1	RS-422 Quad Diff Line Drv
90c031tm.ibs	DS90C031TM	2.1	LVDS Quad Diff Line Drv
90c032tm.ibs	DS90C032TM	2.1	LVDS Quad Diff Line Drv
38c86av.ibs	DS38C86A	1.1	CMOS BTL 9-Bit Xcvr(Demo)
89c386me.ibs	DS89C386TMEA	2.1	12 Ch CMOS Line Rcvr
89c387me.ibs	DS89C387TMEA	2.1	12 Ch CMOS Line Drv
36c278n.ibs	DS36C278N	2.1	Low Power CMOS RS-485
36c278m.ibs	DS36C278M	2.1	Low Power CMOS RS-485
36c279n.ibs	DS36C279N	2.1	CMOS RS-485 w/Sleep-Mode
36c279m.ibs	DS36C279M	2.1	CMOS RS-485 w/Sleep-Mode
36c280n.ibs	DS36C280N	2.1	CMOS RS-485 w/Slew Rate
36c280m.ibs	DS36C280M	2.1	CMOS RS-485 w/Slew Rate
ds34c87n.ibs	DS34C87N	2.1	CMOS RS-485 Quad Line Drv
ds34c87m.ibs	DS34C87M	2.1	CMOS RS-485 Quad Line Drv
36c200m.ibs	DS36C200M	2.1	LVDS Dual Xcvr Pair
89lv21n.ibs	DS89LV21N	2.1	+3.3V RS-422
89lv21m.ibs	DS89LV21M	2.1	+3.3V RS-422

National Semiconductor Corporation also provides IBIS models from various other product lines including, CGS(Clock Generation and Support). GTL, Super I/O, Dram Controllers and many more.

National Semiconductor

Conversion of IBIS Models to Simulator Specific Format

Majority of all EDA tools in the industry support IBIS models. Some common Simulator syntax information is shown below to convert an IBIS model to the Simulator specific internal format. Consult your user guide for more information.

XTK(Quad Design)

Quad Design's XTK tool can read an IBIS model and create its own internal model file. XTK's utility **ibis2xtk** allows the user to read an IBIS model and convert that to a .typ or a .min or a .max file based on the IBIS model. Use the following syntax or consult your XTK user's guide for more information.

```
% ibis2xtk filename.ibs <ret>
```

The output file will contain both the pin definitions (.tlp) and loadspec information (.dev) to be used by XTK.

Consult your XTK user's guide for more information or contact customersupport@qdt.com

LineSimPRO/BoardSim(HyperLynx)

Either LineSimPRO (DOS version) or BoardSim (Windows) can read an IBIS model in its native form. There is no translation required for reading an IBIS model into the simulator.

(Click on)

`Schematic` (This will load the schematic editor)

(Click on)

`Driver` or `Receiver` graphical box

(Click on)

`Select` → `Library` (To load any .ibs file)

Consult your LinesimPRO user's guide for more information or contact support@hyperlynx.com or http://www.hyperlynx.com

IS(Interconnectix)

When using the Interconnectix' Interconnect Synthesis product(IS), you can load IBIS models directly into the tool without translating them. Follow the procedure described below.

1. Execute the

   `File > Import > Models` menu item.

The `Model Loader` dialog box opens.

2. Select the `library path`, then select the `Library Part Model` and click on the `Load` button to load the model into the design. The model is now available for use within the design.

From within IS, you can assign individual IBIS models to part instances or pin instances using the Model Picker:

1. Open the `Parts sheet` within the IS Design Editor.
2. In either the `Design Part Models` or `Pin Models` column, click on the button within the cell of the spreadsheet to open the Model Picker dialog box.
3. Select the `Design Part number.` A list of available pin models is displayed.
4. If you are assigning a pin model to an individual pin instance, also select the Pin Model.

For technical support, contact Interconnectix Inc at support@icx.com or on the Web: http://www/icx.com.

PSPICE(MicroSim)

The **Parts** program is a semi-automatic aid for determining the model parameters for standard devices, such as bipolar transistors, and the subcircuit definitions for more complex models, such as operational amplifiers. MicroSim's PSPICE can convert an IBIS model to a .MOD format by using the utility supplied within **Parts**.

(Click on)

`Parts` → `Part` → `IBIS translator`

IBIS translator allows you to translate a model definition in IBIS model format to a PSPICE model definition. Once you select a file to be translated in the IBIS Translator dialog box, click OK. A PSPICE model file in a ".mod" format will be created in the same working directory.

Consult your PSPICE user's guide for more information or contact tech.support@microsim.com.

Quantic(Greenfield)

Following steps will allow the conversion of an IBIS model into Quantic tools.

1. Use IBIS to quantic program on IBIS file to produce model and component data.
2. Use Phidias/Database manager to load model and component into database.
3. Reference component by correct name from layout data.
4. Simulate for Signal Integrity Analysis.

Consult your Quantic user's guide for more information or contact ventham@quantic.mb.ca.

HSPICE(Meta-Software)

Meta-Software's utility called **Meta I/O** reads an IBIS model and converts that to a SPICE behavioral model format.

Consult your user's guide for more information.

ContecSPICE(Contec Micro Electronics)

Using a utility called **Ibis2csp** a user can convert an IBIS model to ContecSPICE format.

Run the utility

```
% ibis2csp.
```

This will envoke the IBIS-Translator Window

(Click on) `File` → `Load` and enter your .ibs filename

(Clickon) `Translation` → `Translate`

Consult your user's guide for more information or fred@contec.contec.com.

Signoise(Cadence)

DF/SigNoise, the signal integrity analysis tool from Cadence Design Systems, has the ability to translate an IBIS file into its native device model format. To run the translation, type the following in a terminal window:

```
ibis2signoise in=infile [out=outfile] [defaults=def__file]
```

where:

"infile" is the input file name.
"outfile" is the (optional) output name file name
(it defaults to "infile.dml").
"def__file" is the (optional) file specifying
default values for many items (it
defaults to "defaultDevice.values").

Incases

The IBIS-to-INCASES converter creates INCASES macromodels, corresponding reference lists, and other information for the components that are described in IBIS data files in a fully automatic way. The related data is placed on the UNIX file system in a special directory structure.

The graphical user interface of the IBIS-to-INCASES converter provides all necessary functions to generate the macromodels for signal integrity and radiation analysis using INCASES simulation tools.

From the Main Menu of IBIS-to-INCASES converter

Push the button "open. . ." to load a valid IBIS file with the help of a file selection form.

The selected IBIS model file will be read in and checked.

Consult your user's guide for more information or contact:
INCASES Engineering GmbH
Vattmannstrasse 3
D-33100 Paderborn, Germany

National Semiconductor

Downloading IBIS Models from the Internet

IBIS models may be downloaded from the Internet by following any one of the methods described below:

Using the World Wide Web

Using a web browser, open the following URL: http://www.national.com

Using File Transfer Protocol (FTP)

ftp to vhdl.org or ftp to 198.31.14.3 and login as anonymous. Using your E-mail ID as password, change directory using the cd command to /pub/ibis/models/national

Use "get" command to download the files.

Using a Dial-Up Modem

Use any communication software on your PC (Ex. QuikLink, Procomm, LapLink. Terminal(Windows) etc.) and dial (415) 335-0110

Login as guest
Password: just hit return

You will see the Welcome message from VHDL and it will prompt for password again. Enter your E-mail id at this time.

Typical Model Setup:

Baudrate = up to 14.4

Databit = 8

Stop = 1

Parity = None

Flow = Xon/Xoff

You can download files using "kermit", "zmodem" or "sz" etc.

National Semiconductor

Industry Support On IBIS

A listing of Web sites are provided for the user interested to learn more about IBIS and sharewares available to edit, create and translate IBIS models.

North Carolina State University (NCSU)

Using **s2ibis,** a shareware from North Carolina State University, SPICE based models can be converted to IBIS format. **s2ibis** can be used with PSPICE, HSPICE or other SPICE engines.

http://www2.ncsu.edu/eos/project/erl__html

NCSU also provides other utilities, cookbook and related informations.

Hyperlynx, Inc

Provides a great **winibis** utility for DOS Windows for viewing, editing and checking IBIS model files.

http://www.hyperlynx.com

Interconnectix, Inc.

Various utilities, documents and links to other IBIS related home pages available.

http://www.icx.com

Free Model Foundation (FMF)

In future, various types of free behavioral models including IBIS will be provided through this web site. FMF is a non-profit corporation that hopes to provide free, unencrypted, source-code and IBIS simulation models over the Internet.

http://www.vhdl.org/vi/fmf

Section 14

Line Drivers and Receivers Application Notes

Section 14 Contents

National Semiconductor

Application Note—Selection Guide
Line Drivers and Receivers

Application Note Number AN-XXXX	Title	Devices Referenced	TIA/EIA Standards Referenced	ITU-T (CCITT) Related Recommendations
AN-22	Integrated Circuits for Digital Data Transmission	DS7830/DS8830, DS7820/DS8820		
AN-108	Transmission Line Characteristics	DS7820/DS8820		
AN-214	Transmission Line Drivers and Receivers for EIA Standards, RS-422 and RS-423	DS3691, DS88LS120	422 423	V.11 V.10
AN-216	Summary of Well Known Interface Standards		ALL	
AN-336	Understanding Integrated Circuit Package Power Capabilities			
AN-409	Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard	DS3695/DS3696, DS3697/DS3698	485	
AN-438	Low Power RS-232C Driver and Receiver in CMOS	DS14C88, DS14C89A	232	V.28
AN-450	Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability			
AN-454	Automotive Multiplex Wiring	DS75176B DS3695	485	
AN-457	High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Programs	DS8921/A, DS8922/A, DS8923/A	422	V.11
AN-643	EMI/RFI Board Design			
AN-702	Build a Directional-Sensing Bidirectional Repeater	DS75176B, DS96175C	485	
AN-759	Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications		422 485	V.11
AN-805	Calculating Power Dissipation for Differential Line Drivers	DS26LS31, DS96F172	422 485	V.11
AN-806	Data Transmission Lines and Their Characteristics			
AN-807	Reflections: Computations and Waveforms			
AN-808	Long Transmission Lines and Data Signal Quality			
AN-847	FAILSAFE Biasing of Differential Buses	DS3695, DS96172, DS96F172	422 485	V.11
AN-876	Inter-Operation of the DS14C335 with +5V UARTs	DS14C335	232	V.28
AN-878	Increasing System ESD Tolerance for Line Drivers and Receivers used in RS-232 Interfaces	DS1488, DS1489A	232	V.28

Application Note—Selection Guide—Line Drivers and Receivers (Continued)

Application Note Number AN-XXXX	Title	Devices Referenced	TIA/EIA Standards Referenced	ITU-T (CCITT) Related Recommendations
AN-903	A Comparison of Differential Termination Techniques		422 485	V.11
AN-904	An Introduction to the Differential SCSI Interface	DS36954	485	
AN-905	Transmission Line Rapidesigner Operation and Applications Guide		All	
AN-912	Common Data Transmission Parameters and their Definitions		All	
AN-914	Understanding Power Requirements in RS-232 Applications	DS14C335	232 562	
AN-915	Automotive Physical Layer SAE J1708 and the DS36277	DS36277 DS75176B	485	
AN-916	A Practical Guide to Cable Selection		All	
AN-917	Popular Connector Pin Assignments for Data Communication		All	
AN-967	Local Talk™ Physical Layer Alternatives	DS8925/26 DS8935/36	422 423	V.11 V.10
AN-971	An Overview of LVDS Technology	DS90C031 DS90C032	644	
AN-972	Inter-operation of Interface Standards		All	
AN-977	LVDS Signal Quality: Jitter Measurements using Eye Patterns Test Report #1	DS90C031 DS90C032	644	
AN-979	The Practical Limits of RS-485	DS75176B DS3695	485	
AN-1031	TIA/EIA-422-B Overview		422	V.11
AN-1032	An Introduction to FPD-Link	DS90CR561/2 DS90CF561/2 DS90CR581/2 DS90CF581/2	644	
AN-1034	An Optimized DCE Interface for V.34 Modems using the DS8933 and DS8934 Line Driver and Receivers	DS8933 DS8934	423	V.10
AN-1035	PCB Design Guidelines for LVDS Technology		644	

Integrated Circuits for Digital Data Transmission

National Semiconductor
Application Note 22

INTRODUCTION

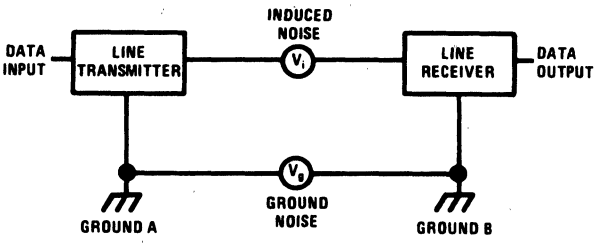
It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in *Figure 1a*, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

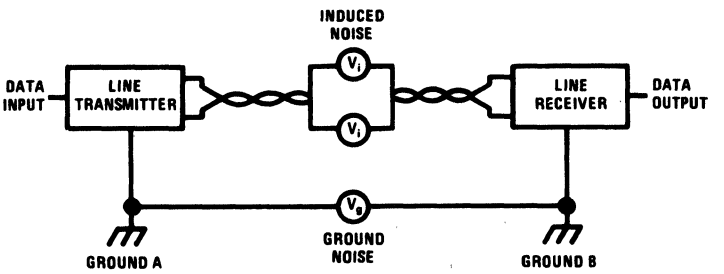
The differential transmission scheme diagrammed in *Figure 1b* solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.



a. Single-Ended System

TL/F/7188–1



b. Difference System

TL/F/7188–2

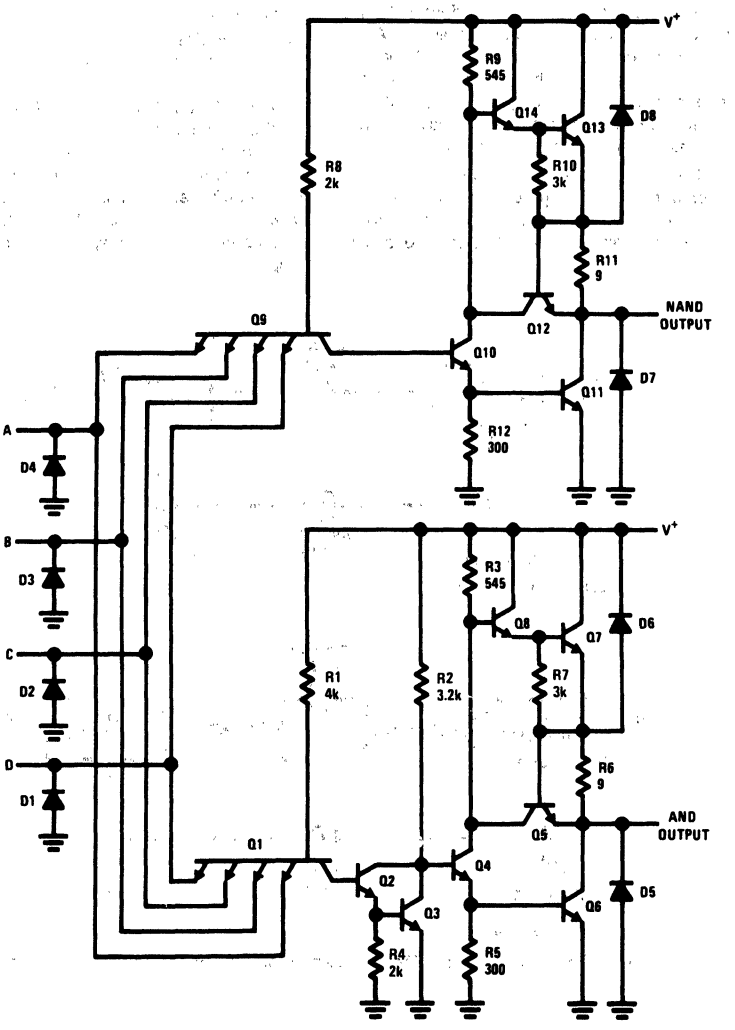
FIGURE 1. Comparing Differential and Single-Ended Data Transmission

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp sever voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

As can be seen from the upper half of *Figure 2*, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to



TL/F/7188–3

FIGURE 2. Schematic Diagram of the DS7830 Line Driver

the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

The lower half of the transmitter in *Figure 2* is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to *Figure 2*, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

*J. Kalb, "Design Considerations for a TTL Gate", *National Semiconductor* TP-6, May, 1968.

The AND output is similarly protected by R6 and Q5, which limits the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the differential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

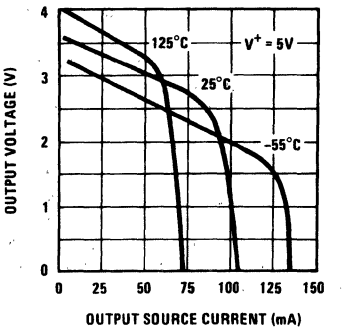


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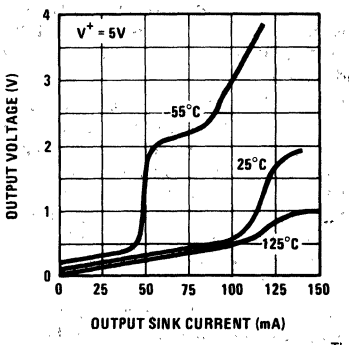
FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. *Figure 3* shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of over-heating the integrated circuit.



TL/F/7188–5

FIGURE 4. Low-State Output Current as a Function of Output Current

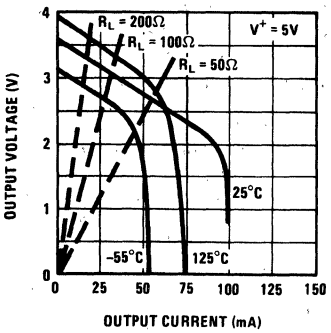


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FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

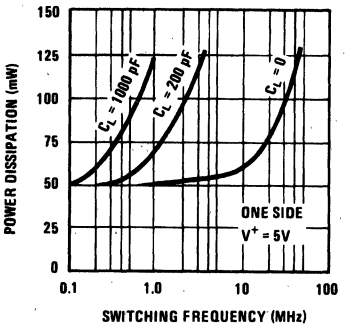
Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is more pronounced at −55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in *Figures 3* and *4* demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under gross overload conditions. *Figure 5* shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the fall off of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω. This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in



TL/F/7188–7

FIGURE 6. Power Dissipation as a Function of Switching Frequency

power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 kHz and 10 MHz. The figure shows that, with no capacitive loading, the power increases with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in *Figure 7*. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

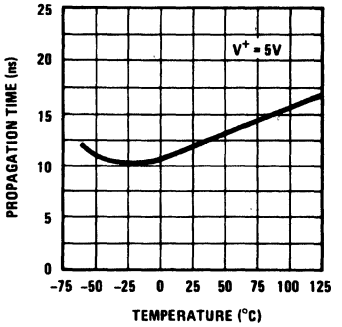


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FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in *Figure 8*.

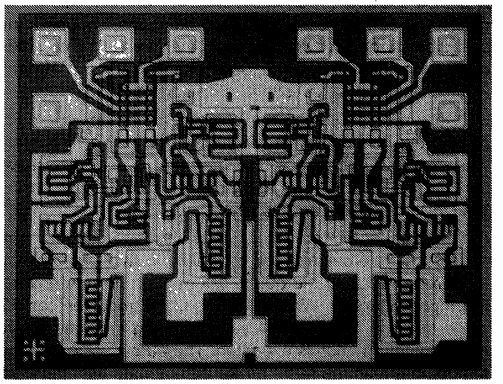

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FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handed easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced DC amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. this output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11} \quad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11} \quad (2)$$

The output voltage at the collector of Q2 will be:

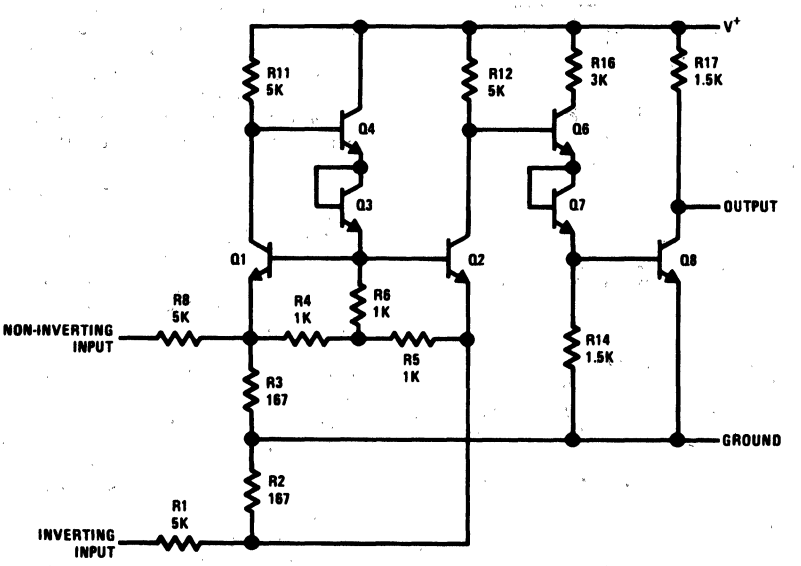
$$V_{C2} = V^+ - I_{C2}R12 \quad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}) \quad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}$$



TL/F/7188–10

FIGURE 9. Simplified Schematic of the Line Receiver

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of this circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in *Figure 10*, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the output will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

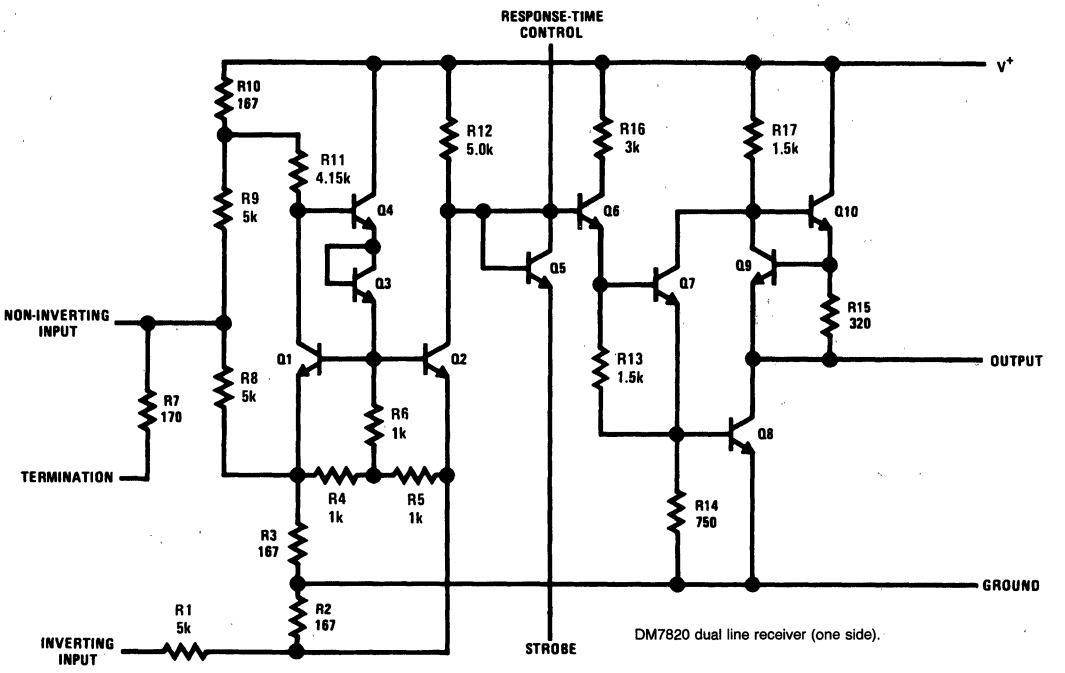


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FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5k, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in *Figure 11*.

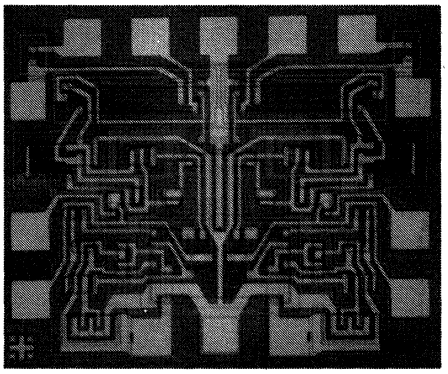

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FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in *Figures 12* through *18*. *Figure 12* illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

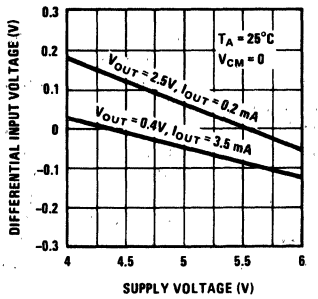

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FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

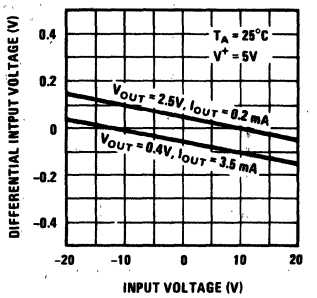

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FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

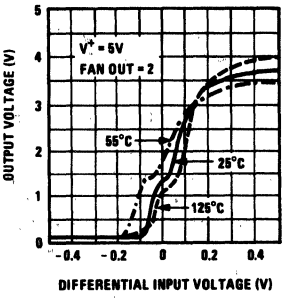

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FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in *Figure 14*. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at −55°C. However, the voltage available remains well above the 2.5V required by digital logic.

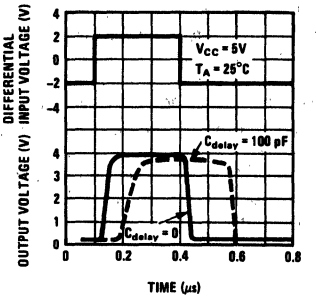

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FIGURE 15. Response Time with and without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in *Figure 16*. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a DC difference between the grounds of the transmitter and the receiver. It is important to note that *Figure 16* gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

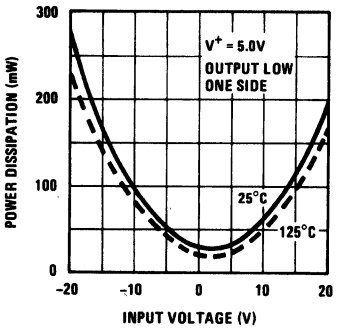

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FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

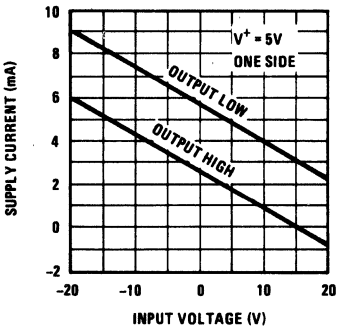

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FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in *Figure 18*. Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

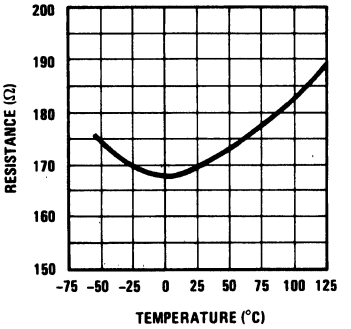

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FIGURE 18. Variation of Termination Resistance with Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in *Figure 19*. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide DC isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

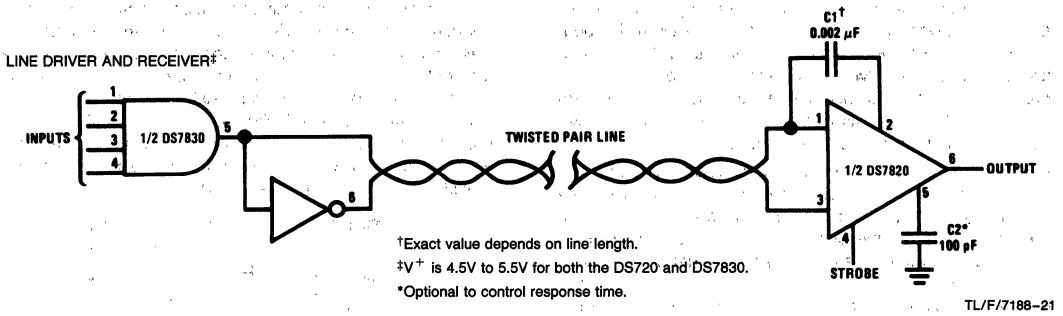

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FIGURE 19. Interconnection of the Line Driver and Line Receiver

The effect of termination mismatches on the transmission line is shown in *Figure 20*. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

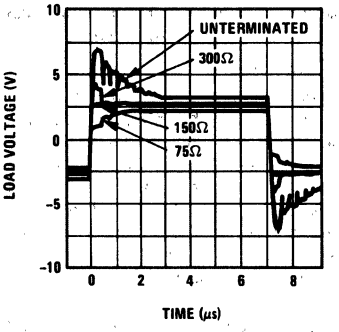

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FIGURE 20. Transmission Line Response with Various Termination Resistances

Figure 21 gives the line-transmission characteristics with various termination resistances when a DC isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient reponse is nearly the same as a DC terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the DC signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

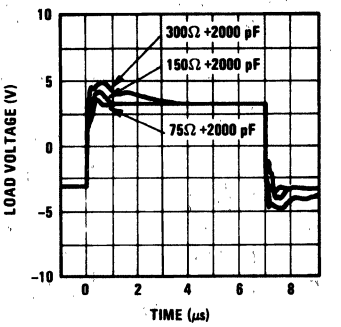

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FIGURE 21. Line Response for Various Termination Resistances with a DC Isolation Capacitor

The effect of different values of DC isolation capacitors is illustrated in *Figure 22*. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

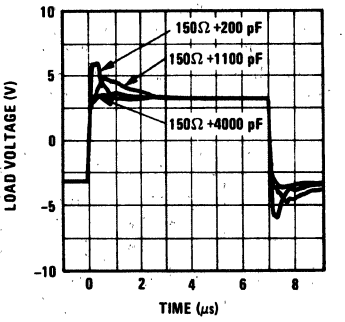

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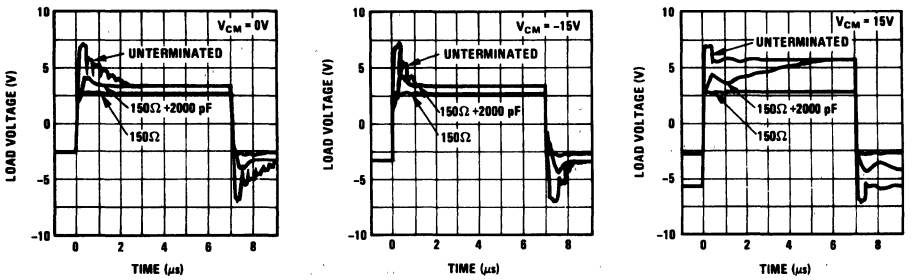
FIGURE 22. Response of Terminated Line with Different DC Isolation Capacitors



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a. V_{CM} = 0V b. V_{CM} = −15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

In *Figure 23*, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal DC state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in *Figure 23b*. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a DC isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a DC coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in *Figure A-1*. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9//R10 + R11 + R3//R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3//R11}{R8 + R3//R1} V_{IN}}{R9//R10 + R11 + R3//R8} + \frac{(V_{IN} - V^+)\frac{R10//R11}{R9 + R10//R11}}{R9//R10 + R11 + R3//R8} \quad (A.1)$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A.1), R8 = R9, R3 = R10, R10 ≪ R11, R9 ≫ R10, R3 ≪ R11, R8 ≫ R3 and

$$\frac{R3}{R4 + 2R6 + R3} \ll 3$$

so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad (A.2)$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2}R12 \quad (A.3)$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A.3) becomes

$$V_{C2} = V^+ - \frac{R12\left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad (A.4)$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3)\frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad (A.5)$$

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A.4),

$$V_{C2} = 2.83V_{BE} + 0.081V^+, \quad (A.6)$$

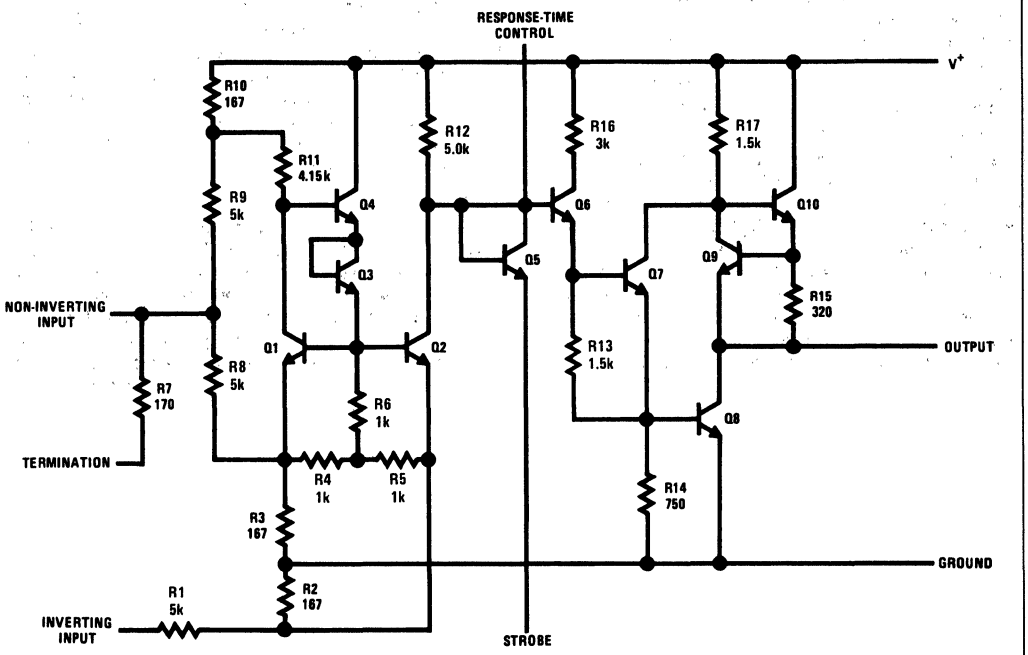

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FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

An equivalent circuit of the input stage is given in *Figure A-2.* Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\,R2}{R1\,(0.9\,R2 + R_{E2})}\,\Delta V_{IN} \qquad (A.7)$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\,\alpha\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})}\,\Delta V_{IN} \qquad (A.8)$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\,R2\,R12}{R1\,(0.9\,R2 + R_{E2})} \qquad (A.9)$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}} \qquad (A.10)$$

where

$$I_{C2} = \frac{V^+ - 3V_{BE}}{R12} \qquad (A.11)$$

so

$$R_{E2} = \frac{kT\,R12}{q\,(V^+ - 3V_{BE})} \qquad (A.12)$$

Therefore, at 25°C where V_{VE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A.6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q}\log_e \frac{I_{C1}}{I_{C2}} \qquad (A.13)$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^+ - V_{OL} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}, \qquad (A.14)$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^+ - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} + I_{SINK} \qquad (A.15)$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^+ - V_{OH} - V_{BE9} - V_{BE10}}{R17} + \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} - I_{SOURCE}, \qquad (A.16)$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A.15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15} - \frac{V_{BE}}{2R14} - I_{SOURCE} \qquad (A.17)$$

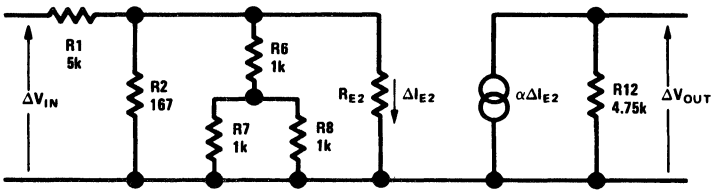

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FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

From (A.13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \quad \text{(A.18)}$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{V1}} \log_e \frac{I_{OL}}{I_{OH}} \quad \text{(A.19)}$$

where A_{V1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0.4V, I_{SOURCE} = 40 μA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at −55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A.18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Transmission Line Characteristics

National Semiconductor
Application Note 108
Bill Fowler

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise sources which will require more noise immunity than required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solutions used vary considerably. Two widely used example methods of the solution are shown in *Figure 1*. The two methods illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

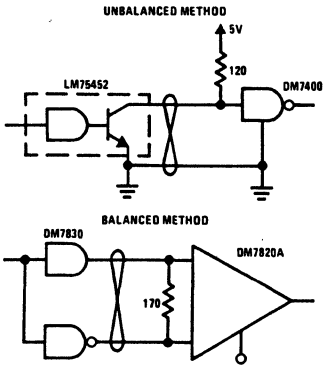

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FIGURE 1

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2*.

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3*. Some noise may be induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

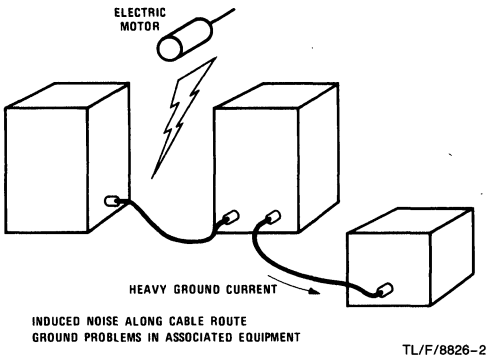

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FIGURE 2. External Noise Sources

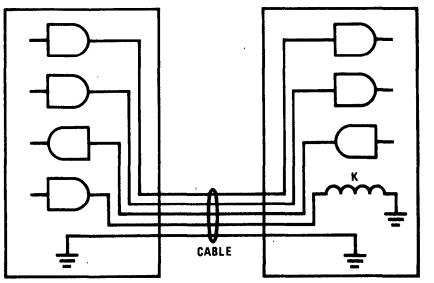

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FIGURE 3. Internal Noise Sources

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and the timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

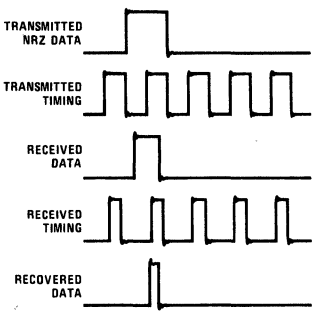

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FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

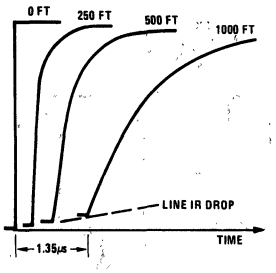

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FIGURE 5. Signal Response at Receiver

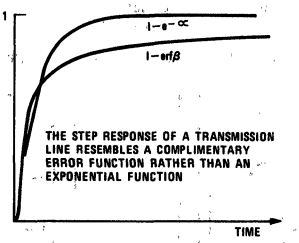

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FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final DC value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7*. The signal doesn't reach one logic level before the signal changes to another level. If the signal has a ½ (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is ⅛ as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

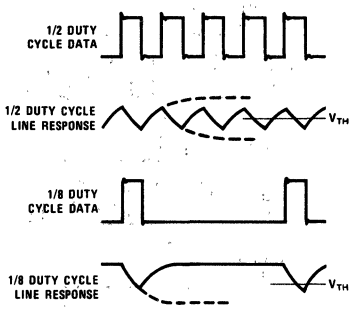

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FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8,* the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

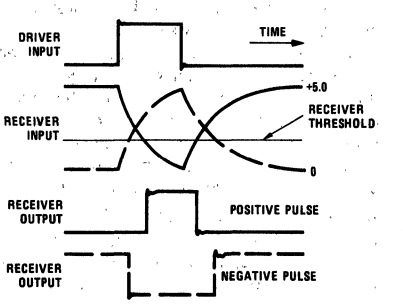

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FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

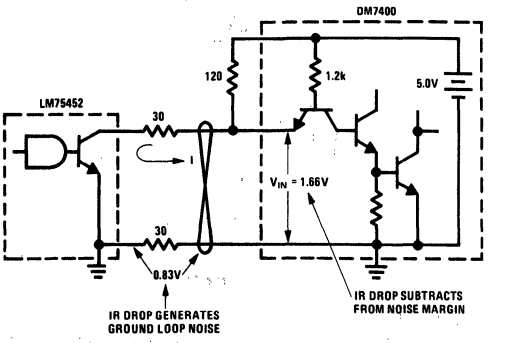

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FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

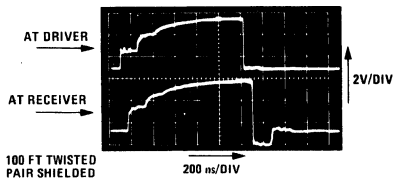

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FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left then is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final DC value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final DC value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

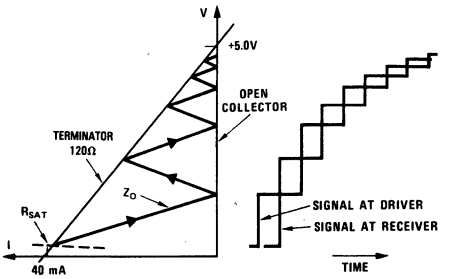

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FIGURE 11. Line Reflection Diagram of Rise Time

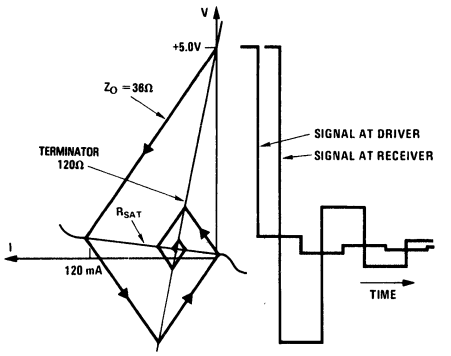

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FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.

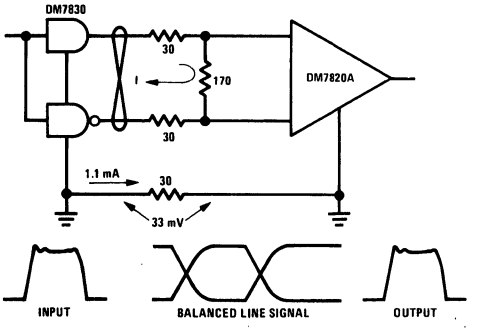

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FIGURE 13. Cross Talk of Signals

The circuit used for a line receiver in the balanced method is a differential amplifier. *Figure 14* shows a noise transient induced equally on lines A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on lines A and B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

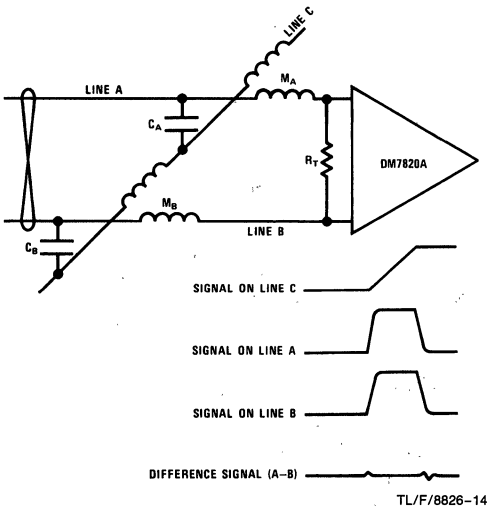

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FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balanced method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced

method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

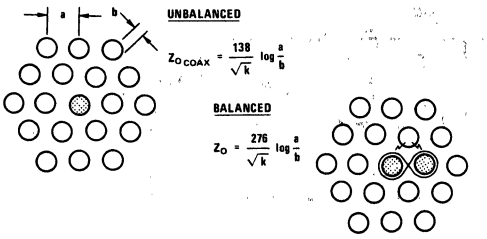

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FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalanced and balanced line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

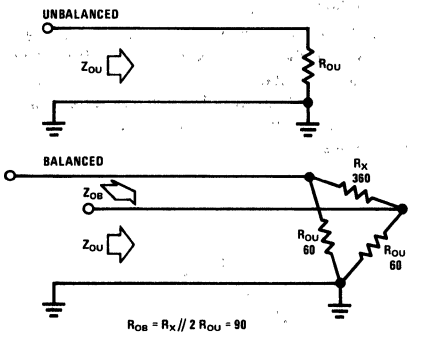

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FIGURE 16. Impedance Measurement

MEASURED PERFORMANCE

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1.* The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

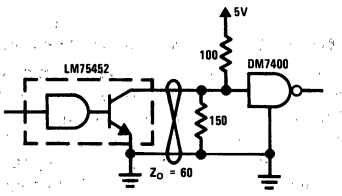

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FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18.* The graph shows the different performances of the DM7820A line receiver and the DM7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

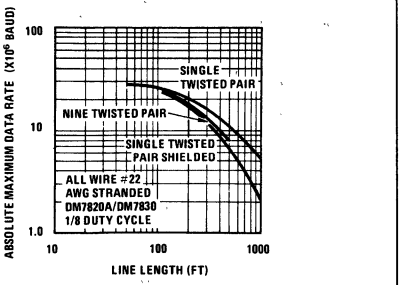

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FIGURE 18. Data Rate vs Cable Type

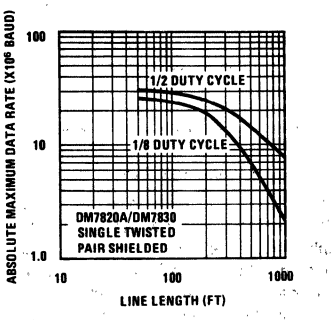

FIGURE 19. Data Rate vs Duty Cycle

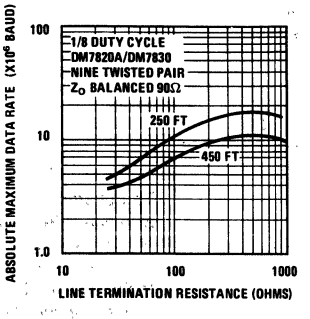

FIGURE 20. Data Rate vs Line Termination

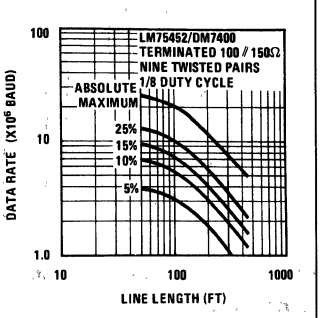

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FIGURE 21. Data Rate vs Distortion of LM75452, DM7400

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* show the Data Rate versus the Line Length for various percentages of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

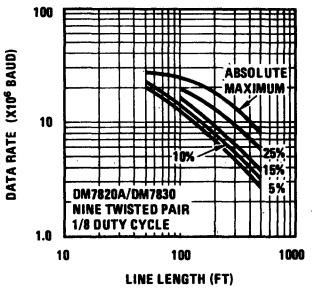

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FIGURE 22. Data Rate vs Distortion of DM7820A, DM7830

Data Rate versus the Line Length for various percentage of timing distortion using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23*. In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

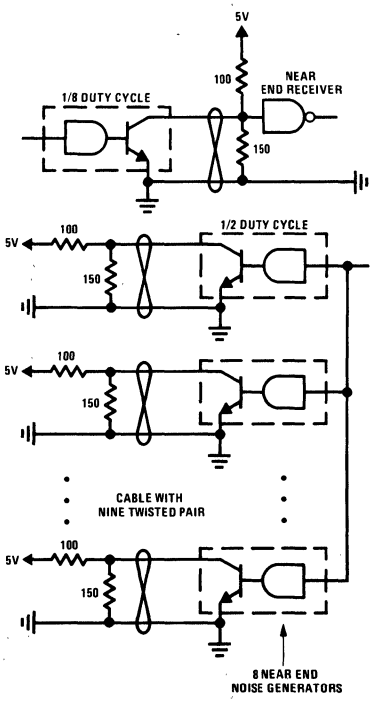

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FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

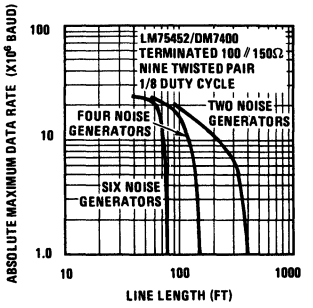

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FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

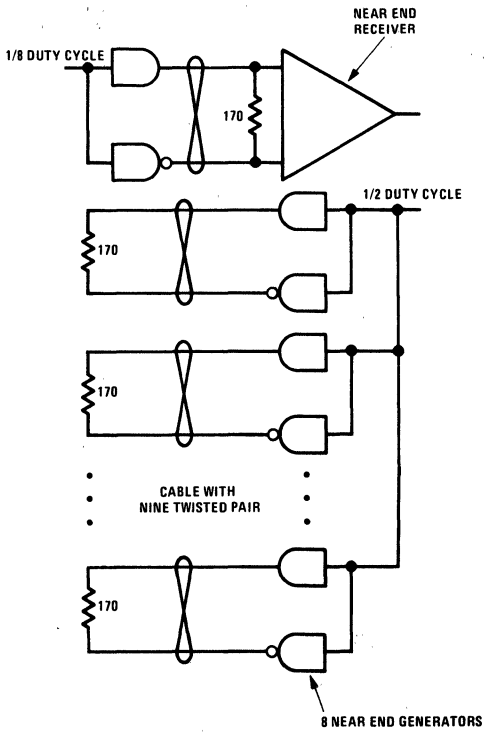

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FIGURE 25. Signal Cross Talk Experiment Using DS7830, DS7820A

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitation. This application note shows that the balanced method is preferable for long lines in noisy electrical environments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates.

DEFINITION OF BAUD RATE

Baud Rate ≡ modulation rate of the channel and is defined as the reciprocal of the minimum pulse width.

Bits/sec (bps) ≡ information rate of the channel and is defined as the number of bits transmitted in one second.

Note: For Non-Return to Zero (NRZ) coding, the baud rate is equal to the bit rate. For Manchester coding, the baud rate is equal to twice the bit rate.

REFERENCES

IC's for Digital Data Transmission, Widlar and Kubinec, *National Semiconductor Application Note AN-22.*

RADC TR73-309, Experimental Analysis of the Transmission of Digital Signals over Twisted Pair Cable, Hendrickson and Evanowski, *Digital Communication Section Communications and Navigation Division,* Rome Air Development Center, Griffis Air Force Base, New York.

Fast Pulse Techniques, Thad Dreher, E-H Research Laboratories, Inc., *The Electronic Engineer,* Aug. 1969.

Transient Analysis of Coaxial Cables, Considering Skin Effects, Wigingtom and Nahmaj, *Proceedings of the IRE,* Feb. 1957.

Relection and Crosstalk in Logic, Circuit Interconnection, John De Falco, Honeywell, Inc., *IEEE Spectrum,* July 1970.

Transmission Line Drivers and Receivers for TIA/EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott
John Goldie

INTRODUCTION

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

THE REQUIREMENTS

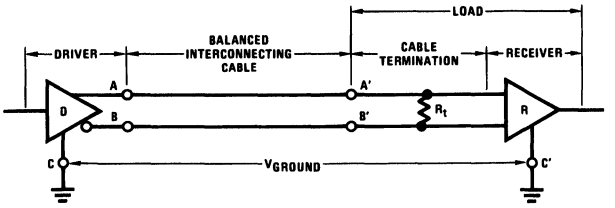
The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and TIA/EIA standards TIA/EIA-422-B (balanced) and TIA/EIA-423-B (unbalanced). In this application note the generic terms of RS-422 and RS-423 will be used to represent the respective TIA/EIA standards. A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1) The cable length
2) The data signaling rate
3) The characteristic of the interconnection cable
4) The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figures 1a* and *1b* are the digital interface for balanced *(1a)* and unbalanced *(1b)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

1) The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2) It is necessary to minimize interference with other signals, such as data versus clock.
3) The interconnecting cable is too long electrically for unbalanced operation *(Figure 2)*.



Legend:
R_t = Optional cable termination resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

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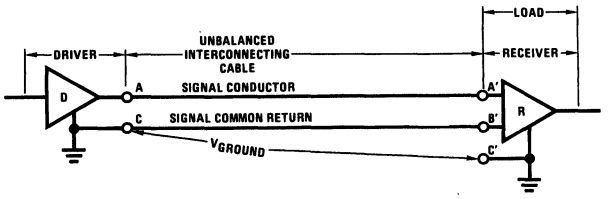
FIGURE 1a. Balanced Digital Interface Circuit



Legend:
R_t = Transmission line termination and/or receiver input impedance
V_{GROUND} = Ground potential difference
A, C = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

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FIGURE 1b. Unbalanced Digital Interface Circuit

CABLE LENGTH

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of data signaling rate. *Figure 2* is a composite of the guidelines provided by RS-422 and RS-423 for data signaling rate versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100Ω load, with rise and fall times equal to or less than one half unit interval at the applied data rate.

The maximum cable length between driver and load is a function of the data signaling rate. But it is influenced by:

1) A maximum common noise range of ±7 volts
   A) The amount of common-mode noise
      Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
   B) Ground potential differences between driver and load.
   C) Cable balance
      Differential noise caused by imbalance between the signal conductor and the common return (ground)
2) Cable termination
   At rates above 200 kbps or where the rise time is 4 times the one way propagation delay time of the cable
3) Tolerable signal distortion

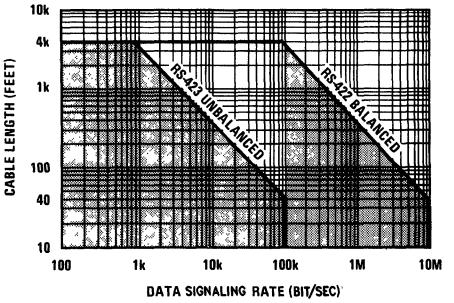

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FIGURE 2. Data Signaling Rate vs Cable Length

DATA SIGNALING RATE

The TIA/EIA Standards recommend that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the data signaling rate on these circuits is below 100 kbps, and balanced voltage digital interface on circuits up to 10 Mbps. The voltage digital interface drivers and receivers meeting the electrical characteristics of this standard need not meet the entire data signaling range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower data signaling rates.

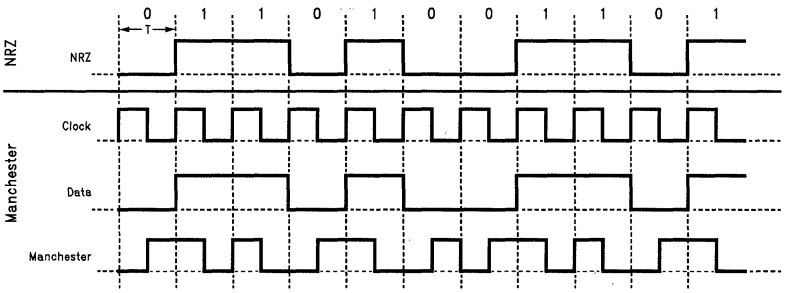
As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is ½ (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were ⅛ (12.5%) the signal would be considerably distorted.

CHARACTERISTICS

Driver Unbalanced (RS-423)

The unbalanced driver characteristics as specified by RS-423 are as follows:

1) A driver circuit should be a low impedance (50Ω or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4V to 6V.
2) With a test load of 450Ω connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the open circuit voltage magnitude (≥ 3.6V) for either binary state.
3) During transitions of the driver output between alternating binary states, the signal measured across a 450Ω test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the sig-



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	Baud	Bits per Second	Hertz
CLOCK	—	—	1/T
NRZ	1/T	1/T	—
Manchester	2/T	1/T	—

Note: bps (bits per second) - Data Information Rate "the number of bits passed along in one second."
baud-Modulation Rate "the reciprocal of the minimum pulse width."
For NRZ bps = bauds

FIGURE 3a. Definition of Baud, Bits per Second (bps), Hertz (Hz) for NRZ and Manchester Coding

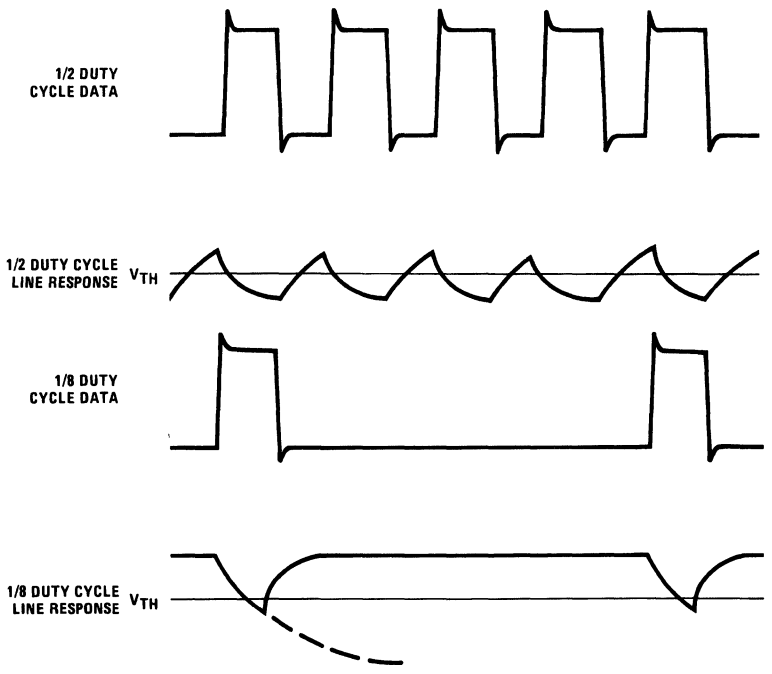
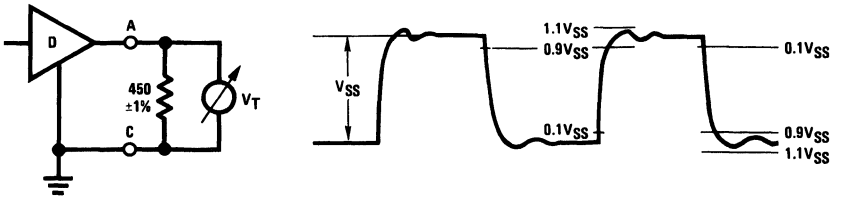


FIGURE 3b. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_{\overline{t}}|$

V_{SS} = Difference in steady state voltages

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FIGURE 4. Unbalanced Driver Output Signal Waveform

nal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed |6V|, nor be less than |3.6V|. V_{SS} is defined as the voltage difference between the two steady state values of the driver output.

Driver Balanced (RS-422)

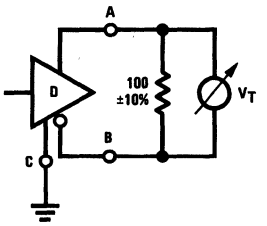
The balanced driver characteristics as specified by RS-422 are as follows:

1) A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2V to 10V.
2) With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0V or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4V. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0V. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4V.
3) During transitions of the driver output between alternating binary states, the differential signal measured across a 100Ω test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 10% of the unit interval or 20 ns, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6V, nor less than 2V.

Interconnecting Cable

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100Ω to frequencies greater than 100 kHz, and a DC series loop resistance not exceeding 240Ω. The cable may be composed of twisted or untwisted pair (flat cable) and is not further specified within the standards.

1) Conductor size of the 2 wires 24 AWG or larger, and wire resistance not to exceed 30Ω per 1000 feet per conductor.
2) Mutual pair capacitance between 1 wire in the pair to the other should be less than 20 pF/ft.



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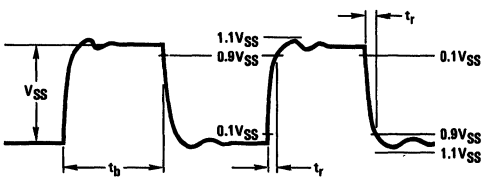

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t_b = Time duration of the unit interval at the applicable modulation rate.

$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns

$t_r \leq 20$ ns when $t_b < 200$ ns

V_{SS} = Difference in steady state voltages

$V_{SS} = |V_t - V_t|$

FIGURE 5. Balanced Driver Output Signal Waveform

Receiver

The receiver characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. The electrical characteristics of a single receiver without termination or optional fail-safe provisions are specified as follows:

1) Over an entire common-mode voltage range of −7V to +7V, the receiver shall not require a differential input voltage of more than 200 mV to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2) To maintain correct operation for differential input signal voltages ranging between 200 mV and 6V in magnitude.
3) The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal plus 7V common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4) The total load including up to 10 receivers shall not have a resistance less than 90Ω for balanced, and 450Ω for unbalanced at its input points and shall not require a differential input voltage of greater than 200 mV for all receivers to assume the correct binary state.

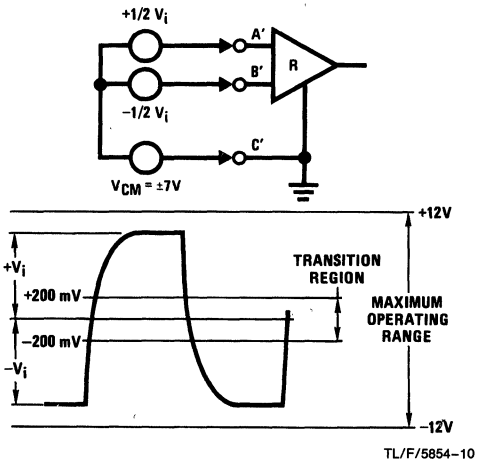

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FIGURE 6. Receiver Input Sensitivity Measurement

SIGNAL RISE TIME

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum data signaling rate. Below 1 kbps the time to reach 90% V_{SS} shall be between 100 μs and 300 μs. If a driver is to operate over a range of data signaling rates and employ a fixed amount of wave shaping which meets the specification for the maximum data signaling rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 7* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

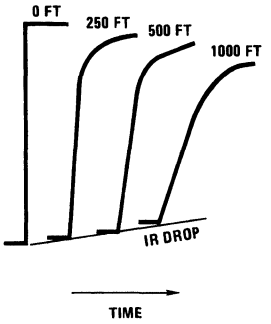

FIGURE 7. Signal Rise Time on Transmission Line vs Line Length

DS1691A, DS78LS120

The Driver

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of both standards. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers *(Figure 8)* or 4 independent unbalanced drivers *(Figure 9)*. When configured for unbalanced operation *(Figure 10)* a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 11* is the typical rise time vs external capacitor used for wave shaping. Note that the rise time control capacitors are connected betwen the control pins and the respective outputs.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 is connected V_{CC} = 5V V_{EE} = −5V. For applications with greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114. This mode is also allowed by the "B" revision of RS-422 (TIA/EIA-422-B) which relaxed to open circuit voltage from 6V to 10V in magnitude.

When configured as balanced drivers *(Figure 8)*, each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques. If the driver is used in multi-point applications (multiple drivers) the use of the response control capacitors is not allowed.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (see *Figure 12*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7V. The DS1691/DS3691 driver is tested to a common-mode range of ±10V and will operate within the requirements of such a system (see *Figure 12*, bottom waveform).

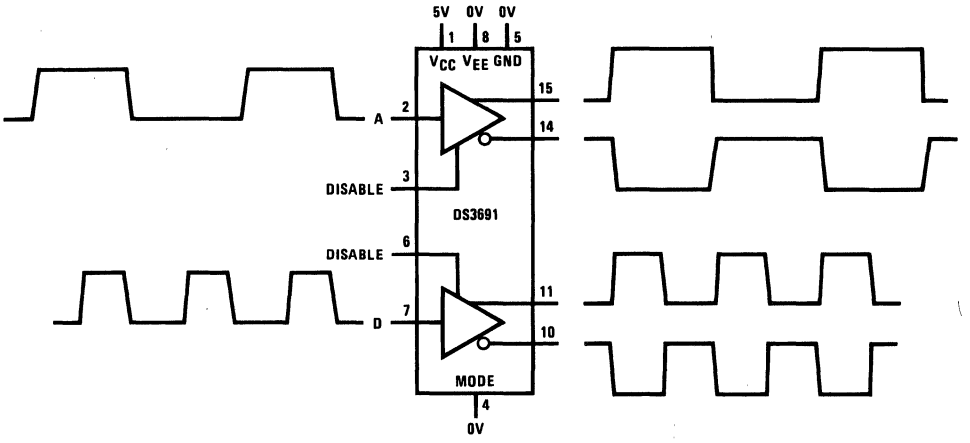

FIGURE 8. DS3691 Connected for Balanced Mode Operation

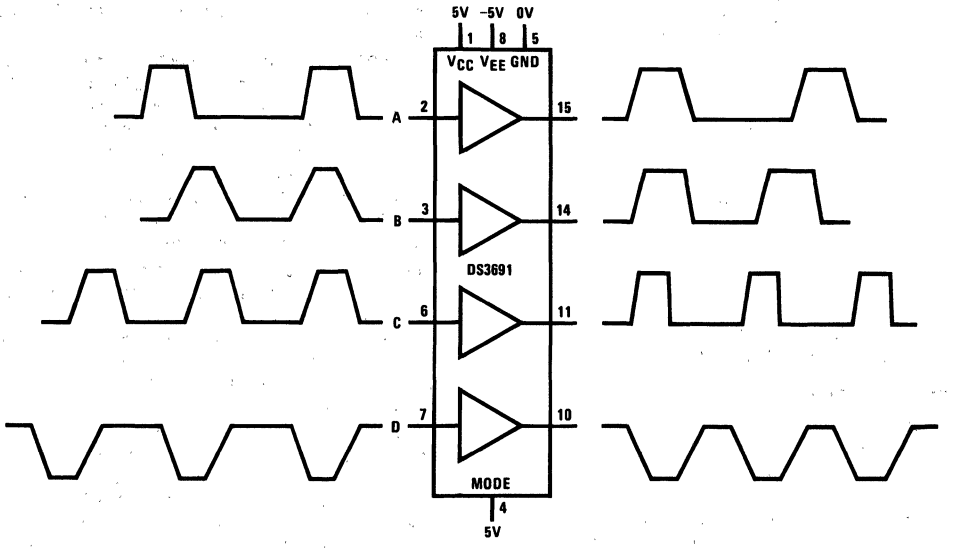

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FIGURE 9. DS3691 Connected for Unbalanced Mode Operation (Non-inverting)

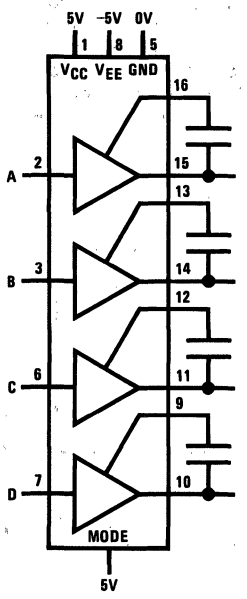

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FIGURE 10. Using an External Capacitor to Control Rise Time of DS3691

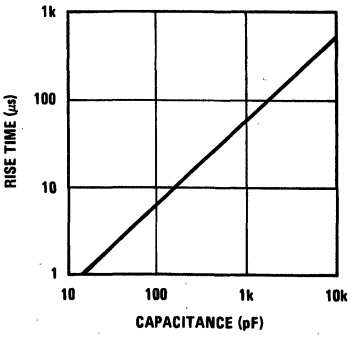

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FIGURE 11. DS3691 Rise Time vs External Capacitor

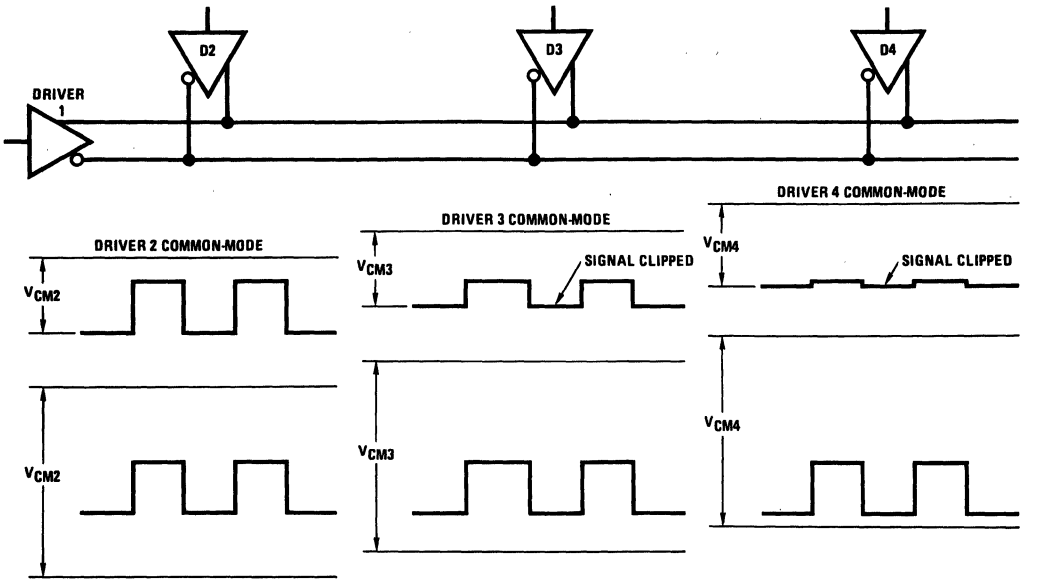

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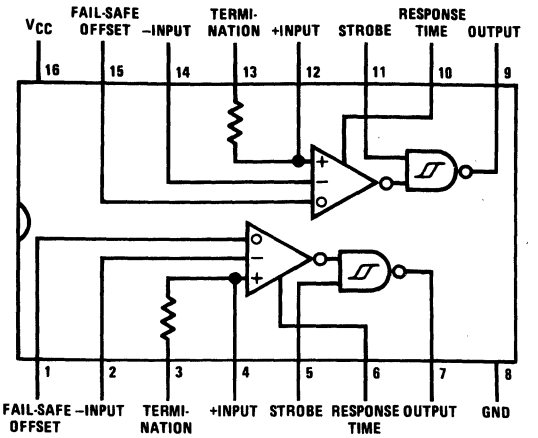
FIGURE 12. Comparison of Drivers without TRI-STATE Common-Mode Output Range (top waveforms) to DS3691 (bottom waveforms)



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Top View

FIGURE 13. DS78LS120/DS88LS120 Dual Differential Line Receiver

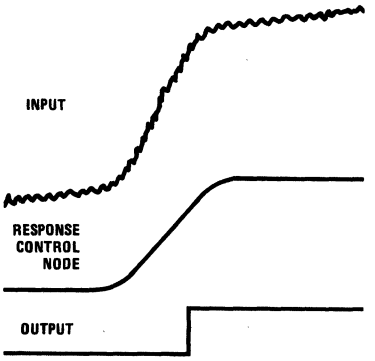
DS78LS120/DS88LS120

The Receiver

The DS78LS120/DS88LS120 are high peformance, dual differential TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysteresis built into the output gate *(Figure 14)*. The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not affect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 15*. The combination of the filter followed by hysteresis will optimize performance in a worst case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.



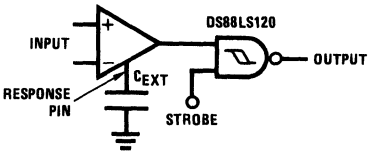


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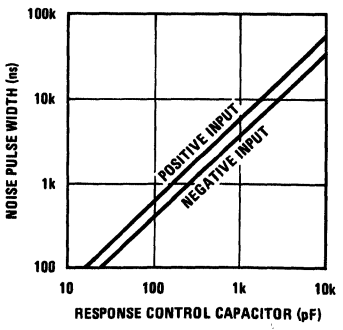
FIGURE 14. Application of DS88LS120 Receiver Response Control and Hysteresis



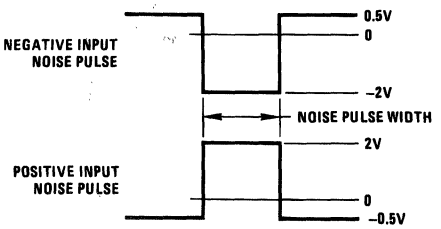


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FIGURE 15. Noise Pulse Width vs Response Control Capacitor

FAIL-SAFE OPERATION

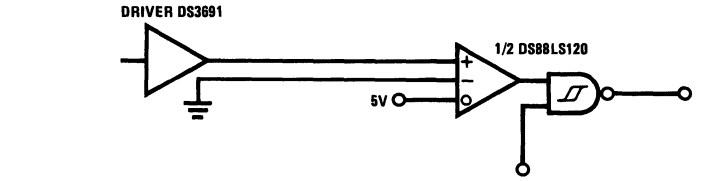
Some communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 mV and an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (see *Figure 16*).

It is recommended that the receiver be terminated in 500Ω or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5V, offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (see *Figure 17*).



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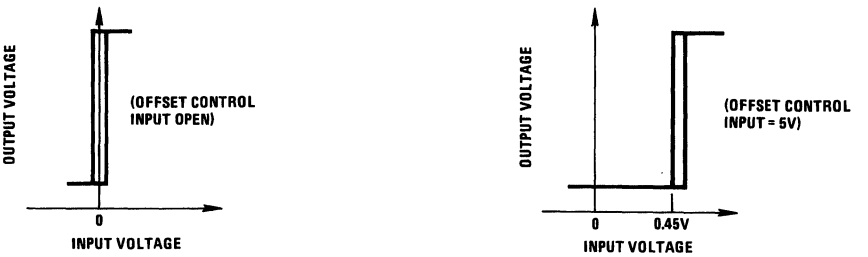

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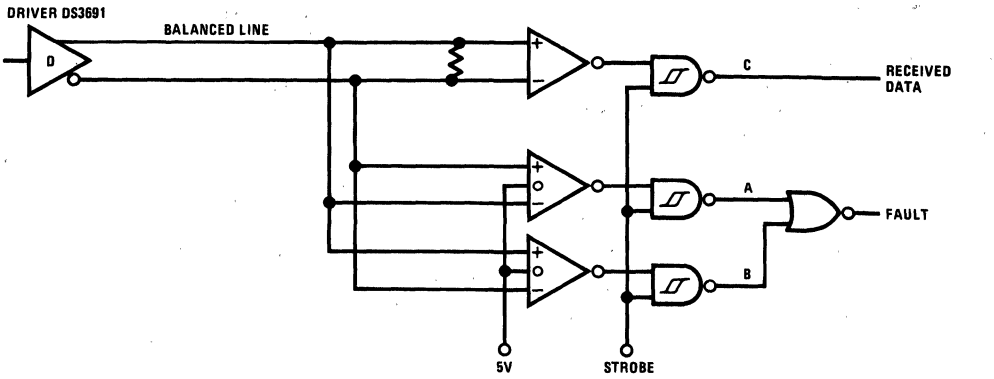
FIGURE 16. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines



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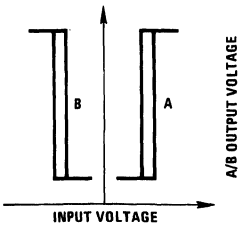

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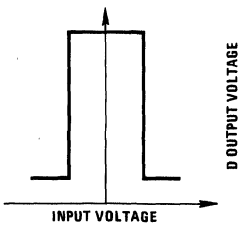

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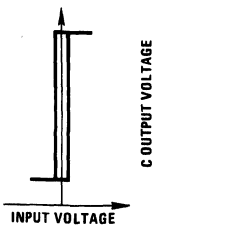

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FIGURE 17. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

CONCLUSION

This application note provides a brief overview of TIA/EIA-422-B and TIA/EIA-423-B. At the time of publication of this application note the Rev. B standards were draft standard proposals only. For complete/current information on the respective standards the reader is referenced to the respective standards, as minor differences may exist between this document and the final versions.

Summary of Well Known Interface Standards

National Semiconductor
Application Note 216
John Goldie

FORWARD

Designing an interface between systems is not a simple or straight-forward task. Parameters that must be taken into account include: data rate, data format, cable length, mode of transmission, termination, bus common mode range, connector type, and system configuration. Noting the number of parameters illustrates how complex this task actually is. Additionally, the interface's compatibility with systems from other manufacturers is also critically important. Thus, the need for standardized interfaces becomes evident. Interface Standards resolve both the compatibility issue, and ease the design through the use of non-custom standardized Drivers and Receivers.

INTRODUCTION

This application note provides a short summary of popular Interface Standards. In most cases, a table of the major electrical requirements and a typical application is illustrated. Interface Standards from the following standardization organizations are covered in this application note:

- TIA/EIA Telecommunications Industry Association/Electronics Industry Association
- CCITT International Telegraph and Telephone Consultative Committee—now replaced by the ITU International Telecommunications Union
- MIL-STD United States Military Standards
- FED-STD Federal Telecommunications Standard Committee
- Other selected interface standards

There are two basic modes of operation for line drivers (generators) and receivers. The two modes are Unbalanced (Single-ended) and Balanced (Differential).

UNBALANCED (SINGLE-ENDED) DATA TRANSMISSION

Unbalanced data transmission uses a single conductor, with a voltage referenced to signal ground (common) to denote logical states. In unbalanced communication only one line is switched. The advantage of unbalanced data transmission is when mulitple channels are required, a common ground can be used (see *Figure 1*). This minimizes cable and connector size, which helps to minimize system cost. The disadvantage of unbalanced data transmission is in its inability to reliably send data in noisy environments. This is due to very limited noise margins. The sources of system noise can include externally induced noise, cross talk, and ground potential differences.

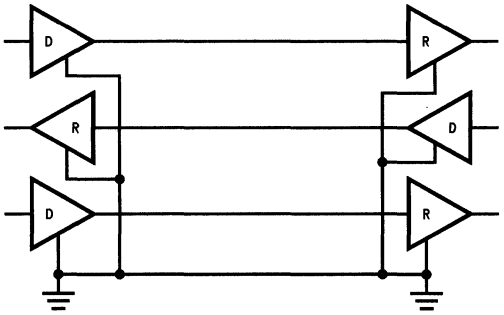

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FIGURE 1. Unbalanced Data Transmission-3 Channel, 4 Line

BALANCED (DIFFERENTIAL) DATA TRANSMISSION

Balanced data transmission requires two conductors per signal. In balanced communication two lines are switched. The logical states are referenced by the difference of potential between the lines, not with respect to ground. This fact makes differential drivers and receivers ideal for use in noisy environments (See *Figure 2*). Differential data transmission nullifies the effects of coupled noise and ground potential differences. Both of these are seen as common mode voltages (seen on both lines), not differential, and are rejected by the receivers. In contrast to unbalanced drivers, most balanced drivers feature fast transition times allowing for operation at higher data rates.

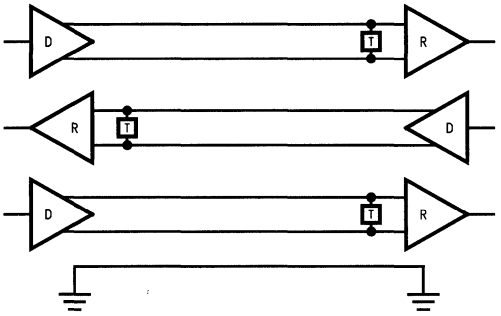

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FIGURE 2. Balanced Data Transmission-3 Channel, 7 Line and Ground

TIA/EIA DATA TRANSMISSION STANDARDS

The Electronic Industry Association (EIA) and the Telecommunications Industry Association (TIA) are industry trade associations that have developed standards to simplify interfaces in data communication systems. The standards are intended for use in Data Terminal Equipment/Data Circuit-terminating Equipment (DTE/DCE) Interfaces. The classic example of the DTE/DCE interface is the "terminal to modem serial interface". However, the standards are not limited to use in DTE/DCE interfaces alone. In fact, many of the standards are commonly used in a wide variety of applications. Examples include Hard Disk Drive Interfaces, Factory Control Busses, and generic I/O Busses. Previously, EIA labeled the standards with the prefix "RS", which stood for recommended standard. This has been replaced with "TIA/EIA", to help in identifying the source of the standard. The letter suffix represents the revision level of the standard. For example, TIA/EIA-232-E represents the fifth revision of RS-232.

TIA/EIA Data Transmission Standards cover the following areas: Complete Interface Standards, Electrical Only Standards, and Signal Quality Standards. Complete standards define functional, mechanical, and electrical specifications. Electrical only standards, as their name implies only defines electrical specifications. They are intended to be referenced by complete standards. Signal Quality Standards define terms and methods for measuring signal quality. Examples of each type are listed below.

- Complete DTE/DCE Interface Standards
  - EIA/TIA-232-E
  - EIA/TIA-530-A
  - EIA/TIA-561
  - EIA/TIA-574
  - TIA/EIA-613
- Electrical Only Standards
  - Unbalanced Standards
    - EIA/TIA-232-E (Section 2)
    - TIA/EIA-423-B (draft)
    - EIA/TIA-562
  - Balanced Standards
    - TIA/EIA-422-B (draft)
    - EIA-485
    - TIA/EIA-612
- Signal Quality Standards
  - EIA-334-A
  - EIA-363
  - EIA-404-A

TIA/EIA—UNBALANCED (SINGLE-ENDED) STANDARDS

EIA/TIA-232-E (RS-232)

EIA/TIA-232-E is the oldest and most widely known DTE/DCE Interface Standard. It is a complete standard specifying the mechanical (connector(s)), electrical (driver/receiver characteristics), and functional (definition of circuits) requirements for a serial binary DTE/DCE Interface. Under the electrical section, the standard specifies an unbalanced, unidirectional, point-to-point interface. The drivers feature a controlled slew rate, this allows the cable to be seen as a lumped load, rather than a transmission line. This is due to the fact that the driver's transition time is substantially greater than the cable delay (velocity $\times$ length). The maximum capacitive load seen by the driver is specified at 2,500 pF. The standard allows for operation up to 20 kbps (19.2 kbps). For higher data rates EIA/TIA-562 or TIA/EIA-423-B are recommended. *Figure 3* illustrates a typical application, and Table I lists the major electrical requirements.

Key Features of the standard are:

- Single-Ended
- Point-to-Point Interface
- Large Polar Driver Output Swing
- Controlled Driver Slew Rate
- Fully Defined Interface
- 20 kbps Maximum Data Rate

TABLE I. EIA/TIA-232-E Major Electrical Specifications

Parameter	Limit & Units
Driver Loaded Output Voltages (3 kΩ)	$\geq \lvert 5.0V \rvert$
Driver Open Circuit Voltage	$\leq \lvert 25V \rvert$
Driver Short Circuit Current	$\leq \lvert 100\ mA \rvert$
Maximum Driver Slew Rate	$\leq 30\ V/\mu s$
Driver Output Resistance (Power Off)	$\geq 300\Omega$
Receiver Input Resistance	3 kΩ to 7 kΩ
Maximum Receiver Input Voltage	±25V
Receiver Thresholds	±3V

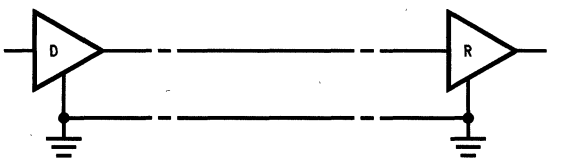

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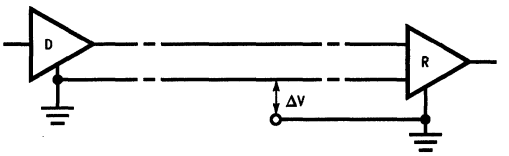
FIGURE 3. Typical EIA/TIA-232-E Application

TIA/EIA-423-B

TIA/EIA-423-B while similar to EIA/TIA-232-E features a reduced driver output swing, and supports higher data rates. This standard specifies an unbalanced driver and a balanced receiver. It is an electrical standard, specifying driver and receiver requirements only. The receivers' requirements are identical to the receivers' requirements specified in TIA/EIA-422-B standard. TIA/EIA-423-B is intended to be referenced by complete standards, such as EIA/TIA-530-A. TIA/EIA-423-B specifies a unidirectional, multidrop (up to ten receivers) interface. Advantages over EIA/TIA-232-E include: multiple receiver operation, faster data rates, and common power supplies (typically ±5V). *Figure 4* illustrates a typical application, and Table II lists the major electrical requirements.

Note: RS-423-A is currently being revised; once approved it will become TIA/EIA-423-B. This is expected by the end of 1993. This section is based on the proposed draft standard.



TL/F/5855–4

FIGURE 4. Typical TIA/EIA-423-B Application

Key Features of the standard are:

- Unbalanced Driver and Balanced Receivers
- Multi-Drop (multiple receivers)
- Wave Shape Control (Driver Output)
- ±7V Receiver Common Mode Range
- ±200 mV Receiver Sensitivity
- 100 kbps Maximum Data Rate (@40 feet)
- 4000 Foot Maximum Cable Length (@ 1 kbps)

TABLE II. TIA/EIA-423-B Major Electrical Specifications

Parameter	Limit & Units
Driver Output Voltage (450Ω Load)	≥ |3.6V|
Driver Open Circuit Voltage	≥ |4.0V| & ≤ |6.0V|
Driver Short Circuit Current	≤ |150 mA|
Transition Time	Controlled
Driver Output Leakage Current	≤ |100 μA|
Receiver Specifications	See TIA/EIA-422-B

EIA/TIA-562

EIA/TIA-562 is a new electrical standard which is very similar to EIA/TIA-232-E, but supports higher data rates (64 kbps). It is an electrical only standard, which is intended to be referenced by complete standards, such as EIA/TAI-561. EIA/TIA-562 specifies an unbalanced, unidirectional, point-to-point interface. This standard supports interoperability with EIA/TIA-232-E devices. *Figure 5* illustrates a typical application, and Table III lists the major electrical requirements.

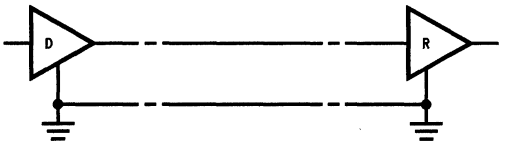


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FIGURE 5. Typical EIA/TIA-562 Application

Key Features of the standard are:

- Unbalanced Driver and Receiver
- Point-to-Point
- Inter-Operability with EIA/TIA-232-E Devices
- 64 kbps Maximum Data Rate

TABLE III. EIA/TIA-562 Major Electrical Specifications

Parameter	Limit & Units
Driver Loaded Output Voltage (Min. Level)	≥ | 3.3V |
Driver Open Circuit Output Voltage	≤ | 13.2V |
Driver Loaded Output Voltage (3 kΩ)	≥ | 3.7V |
Driver Short Circuit Current	≤ | 60 mA |
Driver Transition Time	Controlled
Maximum Driver Slew Rate	≤ 30 V/μs
Driver Output Resistance (Power Off)	≥ 300Ω
Receiver Input Resistance	3 kΩ to 7 kΩ
Maximum Receiver Input Voltage	±25V
Receiver Thresholds	±3V

TIA/EIA BALANCED (DIFFERENTIAL) STANDARDS

TIA/EIA-422-B

TIA/EIA-422-B is an electrical standard, specifying a balanced driver and balanced receivers. The receivers' requirements are identical to the receivers' requirements specified in TIA/EIA-423-B. This standard specifies a unidirectional, single driver, multiple receivers, terminated, balanced interface. *Figure 6* illustrates a point-to-point typical application with termination located at the receiver input (end of cable). *Figure 7* illustrates a fully loaded TIA/EIA-422-B interface. Again termination is located at the end of the cable, also stub length should be minimized to limit reflections. Table IV lists the major electrical requirements of the TIA/EIA-422-B Standard.

NOTE: RS-422-A is currently being revised; once approved it will become TIA/EIA-422-B. This is expected by the end of 1993. This section is based on the proposed draft standard.

Key Features of the standard are:

- Balanced Interface
- Multi-Drop (Multiple Receiver Operation)
- 10 Mbps Maximum Data Rate (@ 40 feet)
- 4000 Foot Maximum Cable Length (@ 100 kbps)

TABLE IV. TIA/EIA-422-B Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Voltage	≤ | 10V |
Driver Loaded Output Voltage	≥ | 2.0V |
Balance of Loaded Output Voltage	≤ 400 mV
Driver Output Offset Voltage	≤ 3.0V
Balance of Offset Voltage	≤ 400 mV
Driver Short Circuit Current	≤ |150 mA |
Driver Leakage Current	≤ | 100 μA |
Driver Output Impedance	≤ 100Ω
Receiver Input Resistance	≥ 4 kΩ
Receiver Thresholds	±200 mV
Receiver Internal Bias	≤ 3.0V
Maximum Receiver Input Current	3.25 mA
Receiver Common Mode Range	±7V (±10V)
Receiver Operating Differential Range	±200 mV to ±6V
Maximum Differential Input Voltage	±12V

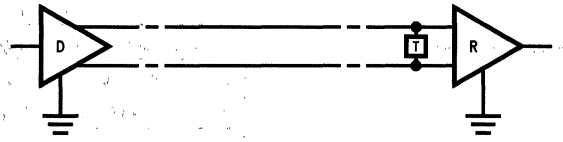

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FIGURE 6. Typical TIA/EIA-422-B Point-to-Point Application

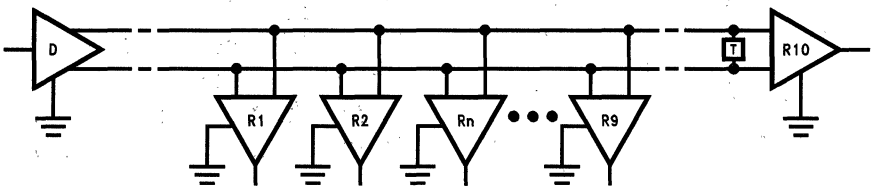

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FIGURE 7. Typical TIA/EIA-422-B Multidrop Application

EIA-485

EIA-485 is an electrical standard, specifying balanced drivers and receivers. It provides all the advantages of TIA/EIA-422-B along with supporting multiple driver operation. EIA-485 is the only TIA/EIA standard that allows for multiple driver operation. This fact allows for multipoint (party line) configurations. The standard specifies a bi-directional (half duplex), multipoint interface. *Figure 8* illustrates a typical multipoint application, and Table V lists the major electrical requirements.

Key Features are:

- Balanced Interface
- Multipoint Operation
- Operation From a Single +5V Supply
- −7V to +12V Bus Common Mode Range
- Up to 32 Transceiver Loads (Unit Loads)
- 10 Mbps Maximum Data Rate (@ 40 feet)
- 4000 Foot Maximum Cable Length (@ 100 kbps)

TABLE V. EIA-485 Major Electrical Specifications

Parameter	Limit & Units
Driver Open Circuit Voltage	≤ | 6.0V |
Driver Loaded Output Voltage	≥ | 1.5V |
Balance of Driver Loaded Output Voltage	≤ | 200 mV |
Maximum Driver Offset Voltage	3.0V
Balance of Driver Offset Voltage	≤ | 200 mV |
Driver Transition Time	≤ 30% Tui
Driver Short Circuit Current (−7V to +12V)	≤ | 250 mA |
Receiver Thresholds	±200 mV
Maximum Bus Input Current +12V/−7V	≤1.0 mA/≤ 0.8 mA

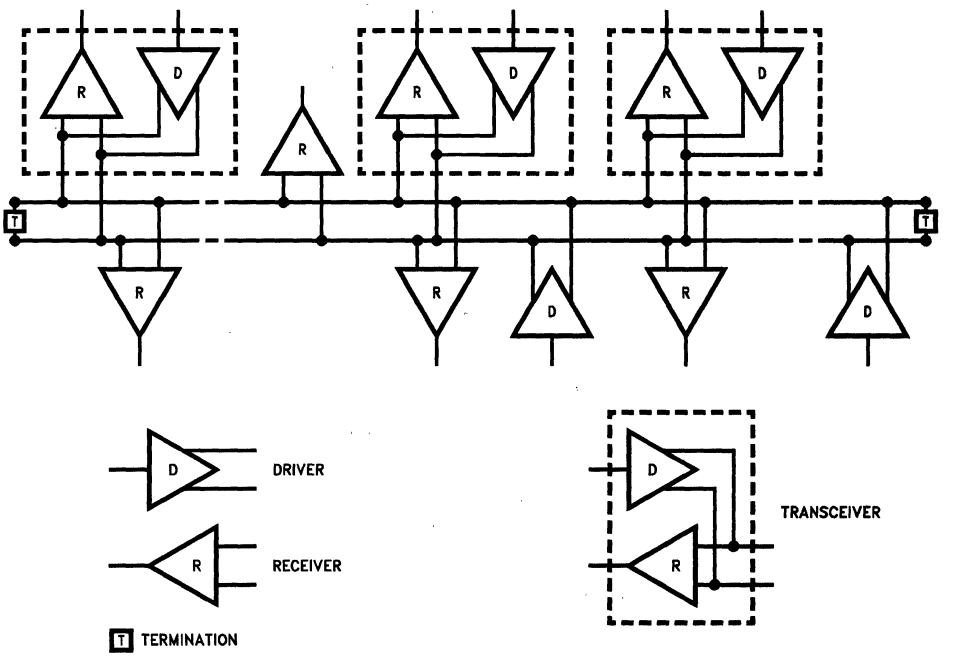

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FIGURE 8. Typical EIA-485 Application

TIA/EIA BALANCED (DIFFERENTIAL) STANDARDS

TIA/EIA-612

TIA/EIA-612 is an electrical standard, specifying a balanced driver and balanced receiver. This standard specifies data rates up to 52 Mbps using ECL technology. This standard specifies a unidirectional, point-to-point interface. *Figure 9* illustrates a typical application with termination located at the receiver input (end of cable). Table VI lists the major electrical requirements of the TIA/EIA-612 Standard. This Standard is referenced by TIA/EIA-613, and together implement a HSSI (High Speed Serial Interface).

TABLE VI. TIA/EIA-612 Major Electrical Specifications

Parameter	Limit and Units
Driver Open Circuit Voltage	$\leq \lvert 1.5V \rvert$
Driver Loaded Output Voltage	$\geq \lvert 590\ mV \rvert$
Balance of Loaded Output Voltage	$\leq \lvert 100\ mV \rvert$
Driver Output Offset Voltage	$\leq 0V$ and $\geq -1.6V$
Balance of Offset Voltage	$\leq \lvert 100\ mV \rvert$
Driver Short Circuit Current	$\leq 50\ mA$
Receiver Thresholds	$\pm 150\ mV$
Receiver Input Range	$-0.5V$ to $-2.0V$
Receiver Input Current	$\leq 350\ \mu A$
Maximum Differential Input Voltage	$\leq 1.5V$

OTHER EIA/TIA STANDARDS

EIA-334-A

EIA-334-A defines signal quality terms for synchronous serial DTE/DCE interfaces. This standard is referenced by the complete synchronous standards.

EIA-363

EIA-363 defines signal quality terms for non-synchronous serial DTE/DCE interfaces. This standard is referenced by the complete non-synchronous standards.

EIA-366-A

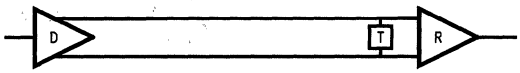
EIA-366-A defines a complete interface between Data Terminal Equipment (DTE) and Automatic Calling Equipment (ACE). The electrical requirements for the drivers and receivers are identical to those in EIA/TIA-232-E.

EIA-404-A

EIA-404-A defines signal quality for start-stop non-synchronous DTE/DCE interfaces.

EIA-408

EIA-408 defines a complete parallel interface between Data Terminal Equipment (DTE) and Numerical Control Equipment (NCE). The interface is limited to short distances and utilizes TTL type drivers and receivers. The drivers are required to sink 48 mA with a VOL of $\leq 0.4V$, and source 1.2 mA with a V_{OH} of $\geq 2.4V$. Short circuit protection is also recommended.



TL/F/5855–15

FIGURE 9. Typical TIA/EIA-612 and TIA/EIA-644 Point-to-Point Application

TIA/EIA-644

TIA/EIA-644 is an electrical standard, specifying a balanced driver and a balanced receiver(s). This standard specifies data rates up to 655 Mbps using LVDS (Low Voltage Differential Signaling) technology. This standard specifies a unidirectional, point-to-point interface. Multiple receivers are supported under certain application limitations. *Figure 9* illustrates the typical point-to-point application with termination (required) located at the receiver input (end of cable). Table VII list the major electrical requirements of the TIA/EIA-644 Standard. This Standard is intended to be referenced by other standards which specify the complete interface.

TABLE VII. TIA/EIA-644 Major Electrical Specifications

Parameter	Limit and Units
Driver Output Voltage	$247\ mV \leq Vdiff \leq 454\ mV$
Driver Offset Voltage	$1.125V \leq V_{OS} \leq 1.375$
Driver Short Circuit Current	$\leq 24\ mA$
Receiver Thresholds	$\pm 100\ mV$
Receiver Input Range	$0V$ to $+2.4V$
Receiver Differential Input Range	100 mV to 600 mV
Receiver Input Current	$\pm 20\ \mu A$

EIA-449

EIA-449 is a complete standard specifying a general purpose DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 37 position connector. This standard references TIA/EIA-422-B and TIA/EIA-423-B standards for line driver and receiver requirements and characteristics. The standard supports data rates up to 2 Mbps. The size of the specified connector has prevented wide spread acceptance of this standard. New designs are utilizing EIA/TIA-530-A instead of EIA-449.

EIA/TIA-530-A

EIA/TIA-530-A is a complete standard specifying a high speed DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 25 position connector. This standard references TIA/EIA-422-B and TIA/EIA-423-B standards for line driver and receiver requirements and characteristics. The standard supports data rates up to 2.1 Mbps. Two connector options are provided; a common 25 position D connector, and a smaller 26 position connector.

Note: Connector pinout differences exists between EIA-530 and EIA/TIA-530-A.

EIA/TIA-561

EIA/TIA-561 is a complete standard specifying a non-synchronous DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing & Control) and a small 8 position connector (MJ8). This standard references EIA/TIA-562 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 38.4 kbps.

EIA/TIA-574

EIA/TIA-574 is a complete standard specifying a non-synchronous DTE/DCE serial interface. It is a complete standard specifying the function of the lines (Data, Timing, & Control) and a 9 position connector. This standard references EIA/TIA-562 standard for line driver and receiver requirements and characteristics. The standard supports data rates up to 38.4 kbps.

TIA/EIA-613

TIA/EIA-613 is a complete standard specifying a general purpose DTE/DCE interface for data rates up to 52 Mbps. This standard specifies functional and connector specifications and references TIA/EIA-612 for electrical characteristics. Together TIA/EIA-612 and TIA/EIA-613 implement a HSSI interface.

CCITT STANDARDS (ITU)

CCITT (International Telegraph and Telephone Consultative Committee) creates and maintains standards which are intended to help standardize international telecommunication services. These standards are recommended technical practices and approaches, however, in some countries they can be considered mandatory. CCITT reviews its standards on a 4 year cycle. Many of the Interface standards are located in volume eight of the CCITT "V" series. This volume is titled "Data Communication over the Telephone Network". Some of the Interface standards are also covered in the "X" series. The CCITT prefix has been replaced by ITU for International Telecommunications Union and the term CCITT will eventually be phased out. A cross reference is provided in Table VIII.

TABLE VIII. V and X Series Cross Reference

V Series	X Series
V.10	X.26
V.11	X.27

Recommendation V.10

Recommendation V.10 defines the electrical characteristics for an unbalanced interface. This recommendation specifies an unbalanced driver and a balanced receiver. With the exception of generator (driver) open circuit output voltage specification, V.10 generator (driver) requirements are very similar to the TIA/EIA-423-B standard. In V.10 the driver is loaded with a 3.9 kΩ resistor to ground, while in the TIA/EIA-423-B standard the driver is unloaded. The V.10 receiver is specified with ±300 mV thresholds, while the TIA/EIA-423-B receiver supports a tighter specification of ±200 mV. Other smaller differences also exist. Therefore, for exact conditions and requirements consult the respective standards.

Recommendation V.11

Recommendation V.11 defines the electrical characteristics for a balanced Interface. V.11 specifies a balanced driver and balanced receivers. With the exception of generator (driver) open circuit output voltage specification, V.11 generator (driver) requirements very similar to the TIA/EIA-422-B

standard. V.11 requires a 3.9 kΩ differential load for the driver's open circuit output, while TIA/EIA-422-B test conditions require no load (open circuit). The Receiver specifications are also very similar, with the exception of the input threshold specification. Recommendation V.11 requires thresholds of ±300 mV while TIA/EIA-422-B requires a tighter specification of ±200 mV. Other smaller differences also exist. Therefore, for exact conditions and requirements consult the respective standards.

Recommendation V.24

Recommendation V.24 defines the function of interchange circuits for DTE/DCE interfaces. Circuit class (Data, Timing, or Control), direction, and definition are all defined in this recommendation. V.24 is intended to be referenced by other recommendations.

Recommendation V.28

Recommendation V.28 defines the electrical characteristics for an unbalanced Interface. This standard specifies driver output and receiver input characteristics. The standard is very similar to the Electrical section (2) of the EIA/TIA-232-E standard. The one notable exception in the generator (driver) requirements is the slew rate specification. The EIA/TIA-232-E lower limit for slew rate is 3 V/μs (@20 kbps), (measured between the +3V and −3V level), while in V.28 the lower limit is 4 V/μs (@20 kbps). Both standards specify the same upper limit of 30 V/μs under light loading conditions. EIA/TIA-232-E defines the complete interface, while V.28 only defines the electrical section of EIA/TIA-232-E. The complete interface standard is covered by CCITT Recommendations V.28 (electrical), V.24 (functional), and ISO 2110 & 4902 (mechanical). For complete specifications refer to CCITT Recommendation V.28.

Recommendation V.35

Recommendation V.35 is actually a modem standard that also defines a balanced interface. While many applications operate at data rates substantially higher than 48 kbps (typically > 1 Mbps), the interface is only defined to operate up to 48 kbps. For low speed control lines the standard recommends the use of V.28 generators (drivers) and receivers. For use on high speed data and timing lines the standard recommends the use of unique V.35 balanced generators (drivers). The drivers feature a small swing of ±0.55V across a termination load of 100Ω. The generator is also specified to have polar swings around ground, yielding a 0V offset voltage. Most implementations use differential current mode drivers with external resistors to implement V.35 balanced generators. V.35 has been rescinded, and V.10 and V.11 generators are recommended as replacements.

US MILITARY STANDARDS

MIL STD 188C (Low Level)

Military Standard 188C (MIL-STD-188C) is similar to EIA/TIA-232-E in the fact that it specifies an unbalanced point-to-point interface. However, the driver's requirements are slightly different. The driver is still required to develop a | 5V | level. The maximum driver output level is specified at | 7V |, and the match between V_{OL} and V_{OH} levels must be within 10% of each other. The driver's slew rate is specified to be between 5% and 15% of the applicable modulation rate. Most drivers require an external capacitor to control the slew rate. *Figure 10* illustrates a typical application, and Table IX lists the major electrical specification of MIL-STD-188C.

TABLE IX. MIL-STD-188C
Major Electrical Specifications

Parameter	Limit & Units
Unloaded Driver Output Level	±5V Min., ±7V Max.
Driver Output Resistance (Power ON) ($I_O \leq 10$ mA)	100Ω Max.
Driver Output Short Circuit Current	±100 mA
Driver Output Slew Rate	5% to 15% of Modulation Rate
Receiver Input Resistance	≥6 kΩ
Receiver Input Thresholds	±100 μA

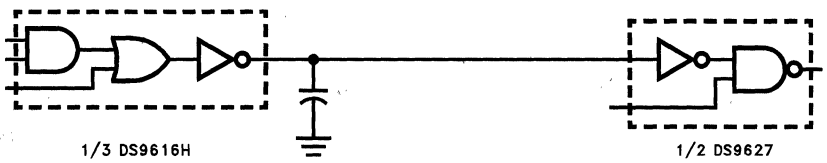


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FIGURE 10. Typical MIL-STD-188C Application

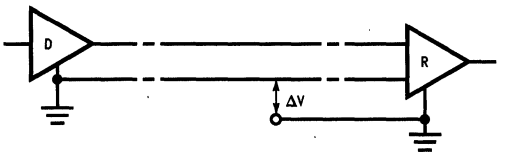

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FIGURE 11. MIL STD 188-114A Unbalanced Typical Application

MIL STD 188-114A

Military Standard 188-114 specifies four different interfaces; three balanced and one unbalanced. The balanced interfaces are divided into three types, two of which are voltage mode, and one of which is current mode. See *Figures 11, 12* and *13*. Voltage mode, type 1, defines an interface for data rates up to 100 kbps. An additional requirement of type 1 is a polar (around ground) output swing. This provides a zero offset output voltage. Voltage mode, type 2, drivers operate up to 10 Mbps and require the same parameters as EIA/TIA-422-A drivers. Additionally, type 2, drivers can have an output offset up to 3V. Current mode, type 3, drivers operate beyond 10 Mbps. The receiver specified for type 1 & 2 balanced, and unbalanced drivers are identical to the receivers specified in TIA/EIA-422-B and TIA/EIA-423-B standards.

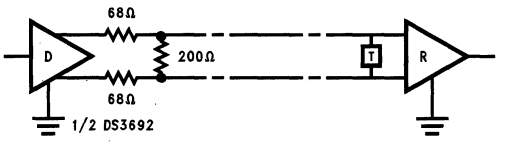

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FIGURE 12. MIL STD 188-114A Balanced, Type 1 Typical Application

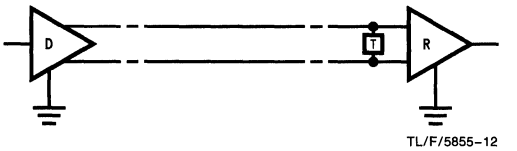

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FIGURE 13. MIL STD 188-114A Balanced, Type 2 Typical Application

MIL STD 1397

Military Standard 1397 specifies two interfaces. These are termed "slow" and "fast". The slow interface operates up to 42 kbps, while the fast interface is defined to operate up to 250 kbps. Comparators and/or discretes components are used to implement drivers and receivers.

FEDERAL TELECOMMUNICATIONS STANDARDS

Federal Standards are from the Federal Telecommunications Standards Committee, which is an advisory committee that adopts TIA/EIA interface standards.

FED STD 1020A

The FEDSTD 1020A is identical to TIA/EIA-423-B. It is intended for United States, non-military government use.

FED STD 1030A

The FEDSTD 1030A is identical to TIA/EIA-422-B. It is intended for United States, non-military government use.

OTHER STANDARDS

IEEE488

The IEEE (Institute of Electrical and Electronics Engineers) also has a standard developing arm. Generally the IEEE standards deal with complete Bus specifications. IEEE488 is a complete Bus standard covering the electrical, mechanical, and functional specification of a parallel instrumentation bus. The bus is commonly used for communication of lab test equipment and machinery control. The standard allows for 15 devices to be connected together, over cable lengths up to 60 feet. The standard defines 16 lines composed of 3 control, 5 management, and 8 data lines. The major electrical specifications are summarized in Table X.

TABLE X. Major IEEE488 Electrical Requirements

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Driver Output Voltage	$I_{OH} = -5.2$ mA	2.4		V
V_{OL}	Driver Output Voltage	$I_{OL} = 48$ mA		0.4	V
I_{OZ}	Driver Output Leakage Current	$V_O = 2.4V$		±40	μA
I_{OH}	Driver Output Current Open Collector	$V_O = 5.25V$		250	μA
V_{IH}	Receiver Input Voltage		2.0		V
V_{IL}	Receiver Input Voltage			0.8	V
I_{IH}	Receiver Input Current	$V_{IN} = 2.4V$		40	μA
I_{IL}	Receiver Input Current	$V_{IN} = 0.4V$		−1.6	mA
I_{CL}	Receiver Clamp Current	$V_{IN} = -1.5V$		12	mA
RL_1	Termination Resistor	$V_{CC} = 5V \pm 5\%$	2850	3150	Ω
RL_2	Termination Resistor	V = GND	5890	6510	Ω

GA-22-6974-0

IBM specification GA-22-6974-0 specifies the electrical characteristics, format of information, and the control scheme of an unbalanced interface. This interface is mainly used on 360/370 equipment and allows up to 10 I/O ports. This unbalanced interface employs 95Ω terminated coax cable. Drivers normally feature open-emitter designs, and short-circuit limiting. Receivers normally feature hysteresis to prevent output oscillations for slow rising inputs in noisy environments. Care should be taken to limit cable lengths such that noise is limited to less than 400 mV. *Figure 14* illustrates a typical application, and Table XI lists the major electrical requirements.

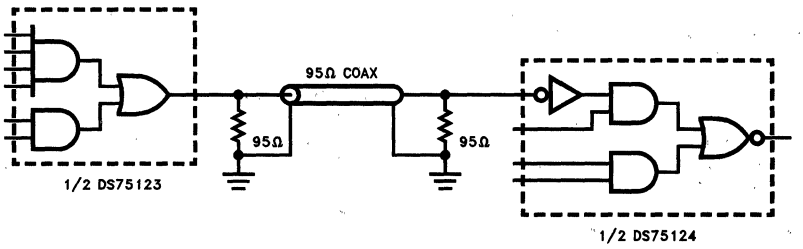

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FIGURE 14. GA-22-6974-0 Typical Application

TABLE XI. Major Electrical Requirements of GA-22-6974-0

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA		7	V
V_{OH}		I_{OH} = 30 μA		5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11		V
V_{OL}		I_{OL} = −240 μA		0.15	V
V_{IH}	Receiver Input Threshold			1.7	V
V_{IL}			0.7		V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V		−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24		mA
	Receiver Input Voltage Range				
V_{IN}	Power ON		−0.15	7	V
V_{IN}	Power OFF		−0.15	6	V
R_{IN}	Receiver Input Impedance	0.15V ≤ V_{IN} ≤ 3.9V	7.4		kΩ
I_{IN}	Receiver Input Current	V_{IN} = 0.15V		240	μA
Z_O	Cable Impedance		83	101	Ω
R_O	Cable Termination	PD ≤ 390 mW	90	100	Ω
	Noise (Signal and Ground)			400	mV

CONCLUSION

This application note provides a brief overview of various interface standards from several standardization organizations. It is only intended to point out the major requirements of each standard and to illustrate a typical application. When selecting or designing a standardized interface it is highly recommended to carefully review the complete standard.

Standards can be ordered from the respective organizations or from:

Global Engineering Documents
2805 McGraw Avenue
P.O. Box 19539
Irvine, CA 92714
USA
(800) 854-7179

Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard

National Semiconductor
Application Note 409
Sivakumar Sivasothy

INTRODUCTION

The Electronics Industries Association (EIA), in 1983, approved a new balanced transmission standard called RS-485. The EIA RS-485 standard addresses the problem of data transmission, where a balanced transmission line is used in a party-line configuration. It is similar in many respects to the popular EIA RS-422 standard; in fact RS-485 may be considered the outcome of expanding the scope of RS-422 to allow multipoint—multiple drivers and receivers sharing the same line—data transmission. The RS-485 standard, like the RS-422 standard, specifies only the electrical characteristics of the driver and the receiver to be used at the line interface; it does not specify or recommend any protocol. The protocol is left to the user.

The EIA RS-485 standard has found widespread acceptance and usage since its ratification. Users are now able to configure inexpensive local area networks and multi-drop communication links using twisted pair wire and the protocol of their choice. They also have the flexibility to match cable quality, signalling rate and distance to the specific application and thus obtain the best tradeoff between cost and performance. The acceptance of the RS-485 standard is also reflected by the fact that other standards refer to it when specifying multipoint data links. The ANSI (American National Standards Institute) standards IPI (Intelligent Peripheral Interface) and SCSI (Small Computer Systems Interface) have used the RS-485 standard as the basis for their voltage mode differential interface class. The IPI standard specifies the interface between disc drive controllers and host adapters and requires a data rate of 2.5 megabaud over a 50 meters NRZ data link. The SCSI standard specifies the interface between personal computers, disc drives and printers at data rates up to a maximum of 4 megabaud over 25 meters.

It is not possible to use standard gate structures and meet the requirements of RS-485. The modifications necessary to comply with the DC requirements of the standard, tend to exact a heavy toll on speed and other AC characteristics like skew. However, it is possible to vastly improve the ac performance by employing special design techniques. The DS3695 family of chips made by National Semiconductor meets all the requirements of EIA RS-485, and still provides ac performance comparable with most existing RS-422 devices. The chip set consists of four devices; they are the DS3695/DS3696 transceivers and the DS3697/DS3698 repeaters. National's RS-485 devices incorporate several features in addition to those specified by the RS-485 standard. These features provide greater versatility, easier use and much superior performance. This article discusses the requirements of a multi-point system, and the way in which RS-485 addresses these requirements. It also explains the characteristics necessary and desirable in the multi-point drivers and receivers, so that these may provide high performance and comply with generally accepted precepts of data transmission practice.

WHY RS-485?

Until the introduction of the RS-485 standard, the RS-422 standard was the most widely accepted interface standard for balanced data transmission. The RS-422 drivers and re-

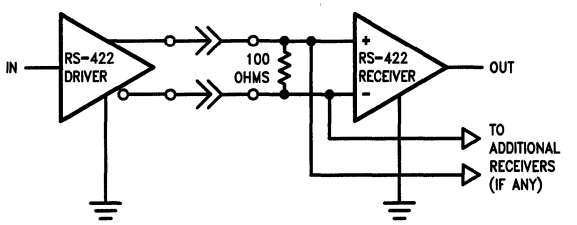

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FIGURE 1a. An RS-422 Configuration

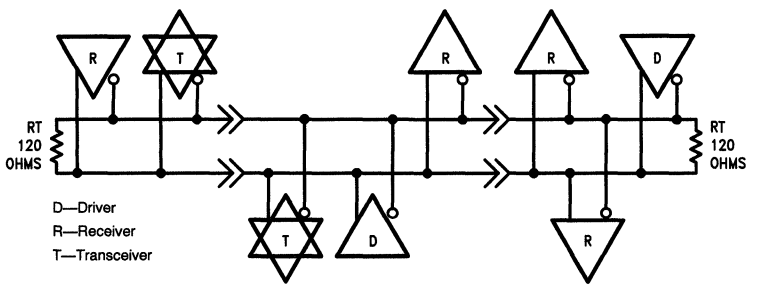

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FIGURE 1b. A Typical RS-485 Party-Line Configuration

ceivers were intended for use in the configuration shown in *Figure 1a*. The driver is at one end of the line; the termination resistor (equal to 100Ω) and up to 10 receivers reside at the other end of the line. This approach works well in simplex (unidirectional) data transmission applications, but creates problems when data has to be transmitted back and forth between several pieces of equipment. If several Data Terminal Equipments (DTEs) have to communicate with one another over long distances using RS-422 links, two such balanced lines have to be established between each pair of DTEs. The hardware cost associated with such a solution would normally be unacceptable.

A party line is the most economical solution to the above problem. RS-422 hardware could conceivably be used to implement a party line if the driver is provided with TRI-STATE® capability, but such an implementation would be subjected to severe restrictions because of inadequacies in the electrical characteristics of the driver. The biggest problem is caused by ground voltage differences. The common mode voltage on a balanced line is established by the enabled driver. The common mode voltage at the receiver is the sum of the driver offset voltage and the ground voltage difference between the driver and the receiver. In simplex systems only the receiver need have a wide common mode range. Receiver designs that provide a wide common mode range are fairly straightforward. In a party-line network several hundred feet long, in which each piece of equipment is earthed at a local ac outlet, the ground voltage difference between two DTEs could be as much as a few volts. In such a case both the receiver and the driver must have a wide common mode range. Most RS-422 drivers are not designed to remain in the high impedance state over a wide enough common mode range, to make them immune to even small ground drops.

Classical line drivers are vulnerable to ground drops because of their output stage designs. A typical output stage is shown in *Figure 2a*. Two such stages driven by complementary input signals, may be used to provide the complementary outputs of a differential line driver. Transistors Q1 and Q4 form a Darlington pull up for the totem pole output stage; Q2 is the pull down transistor. The phase splitter Q3 switches current between the upper and lower transistors to obtain the desired output state. DSUB is the diode formed by the collector of Q2 and the grounded substrate of the integrated circuit. The output in *Figure 2a* can be put into the high impedance state by pulling down the bases of transistors Q3 and Q4. Unfortunately, the high impedance state cannot be maintained if the output is pulled above the power supply voltage or below ground voltage. In party-line applications, where ground voltage differences of a few volts will be common, it is essential that the drivers be able to hold the high impedance state while their outputs are taken above V_{CC} and below ground.

The output in *Figure 2a* can be taken high until the emitter-base junction of Q1 breaks down. Thereafter, the output will be clamped to a zener voltage plus a base-collector diode voltage above V_{CC}; V_{CC} could be zero if the device is powered off. If the output is taken below ground, it will cause the substrate diode, DSUB, associated with Q2 to turn on and clamp the output voltage at a diode drop below ground. If a disabled driver turns on and clamps the line, the signal put out by the active driver will get clipped and distorted. It is also possible for ground drops to cause dangerously large substrate currents to flow and damage the devices as illustrated in *Figure 2b*. *Figure 2b* depicts two drivers A and B; it shows the pull down transistors (Q2A and Q2B) and their associated substrate diodes (DSUB-A and DSUB-B) for the two drivers A and B. Here driver A is ON in the low output state; driver B is disabled, and therefore, should neither source nor sink current. The ground of driver A is 3 volts lower than that of driver B. Consequently, the substrate diode DSUB-B sees a forward bias voltage of about 2.7V (the collector-emitter voltage of Q2A will be about 0.3V), which causes hundreds of milliamperes of current to flow out of it.

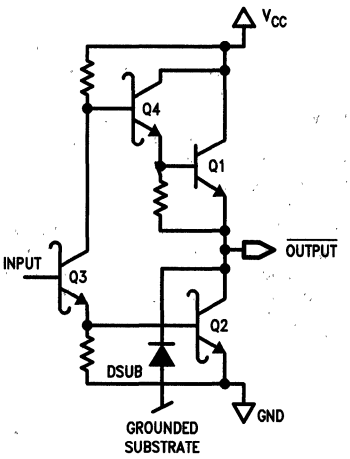

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FIGURE 2a. Driver Output Stage (not RS-485)

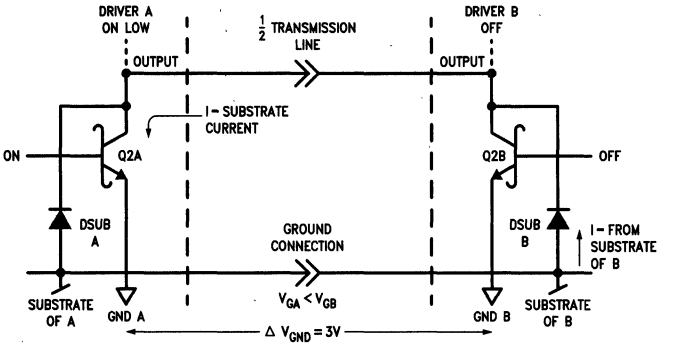

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FIGURE 2b. Two DCEs Separated by a Ground Drop

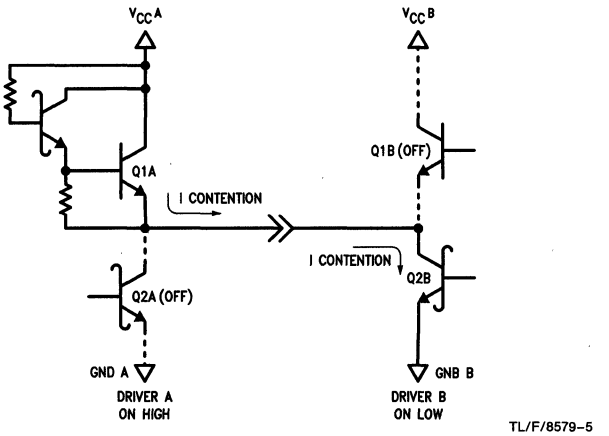

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FIGURE 2c. Bus Contention

Another problem is line contention, i.e. two drivers being 'ON' simultaneously. Even if the protocol does not allow two drivers to be on at the same time, such a contingency could arise as a result of a fault condition. A line contention situation, where two drivers are on at the same time, is illustrated in *Figure 2c*. Here, drivers A and B are 'ON' simultaneously; driver A is trying to force a high level on the line whereas driver B is trying to force a low level. Transistors Q1A and Q2B are 'ON' while transistors Q2A and Q1B are 'OFF'. As a result, a large current is sourced by Q1A and sunk by Q2B; the magnitude of this current is limited only by the parasitic resistances of the two devices and the line. The problem is compounded by any ground drop that may exist between the two contending drivers. This large contention current can cause damage to one or both of the contending drivers. Most RS-422 drivers are not designed to handle line contention.

A multi-point driver should also be capable of providing more drive than a RS-422 driver. The RS-422 driver is only required to drive one 100Ω termination resistor, and ten receivers each with an input impedance no smaller than 4 kΩ. A party-line, however, would have to be terminated at both ends; it should also be able to drive more devices to be useful and economical.

Because of the above limitations, it is quite impractical to use RS-422 hardware to interconnect systems on a party-line. Clearly, a new standard had to be generated to meet the more stringent hardware requirements of muti-point data links.

THE RS-485 STANDARD

The RS-485 standard specifies the electrical characteristics of drivers and receivers that could be used to implement a balanced milti-point transmission line (party-line). A data exchange network using these devices will operate properly in the presence of reasonable ground drops, withstand line contention situations and carry 32 or more drivers and receivers on the line. The intended transmission medium is a 120Ω twisted pair line terminated at both ends in its characteristic impedance. The drivers and receivers can be distributed between the termination resistors as shown in *Figure 1b*.

The effects of ground voltage differences are mitigated by expanding the common mode voltage (V_{CM}) range of the driver and the receiver to $-7V < V_{CM} < +12V$. A driver forced into the high impedance state, should be able to have its output taken to any voltage in the common mode range and still remain in the high impedance state, whether powered on or powered off. The receiver should respond properly to a 200 mV differential signal super-imposed on any common mode voltage in this range. With a 5V power supply, the common mode voltage range specified by RS-485 has a 7V spread from either supply terminal. The system will therefore perform properly in the presence of ground drops and longitudinally coupled extraneous noise, provided that the sum of these is less than 7 volts.

The output drive capability of the driver and the input impedance of the receiver are increased to accommodate two termination resistors and several devices (drivers, receivers and transceivers) on the line. The RS-485 standard defines a 'unit load' so that the load presented to the line by each device can be expressed in terms of unit loads (a 12 kΩ resistor, with one end tied to any voltage between ground and $V_{CC}/2$, will satisfy the requirements of a unit load). It was anticipated that most manufacturers would design their drivers and receivers such that the combined load of one receiver and one disabled driver would be less than one unit load. This would require the RS-485 receiver to have three times the input resistance of a RS-422 receiver. The required receiver sensitivity is ±200 mV—the same as for RS-422. The driver is required to provide at least 1.5V across its outputs when tied to a terminated line populated with 32 transceivers. Although this output voltage is smaller than the 2.0V specified for RS-422, a careful design of the driver, with special regard to ac performance, can allow the user to operate a multi-point network at data rates and distances comparable to RS-422.

RS-485 has additional specifications to guarantee device safety in the event of line contention or short circuits. An enabled driver whose output is directly shorted to any voltage in the common mode range, is required to limit its current output to ±250 mA. Even with such a current limit, it is possible for a device to dissipate as much as 3 Watts (if the device draws 250 mA while shorted to 12 volts). Power dissipation of such a magnitude will damage most ICs; therefore, the standard requires that manufacturers include some additional safeguard(s) to protect the devices in such situations.

The ±250 mA current limit also serves another purpose. If a contending driver is abruptly turned off, a voltage transient, of magnitude $I_C Z/2$, is reflected along the line as the line discharges its stored energy (I_C is the contention current and Z is the characteristic impedance of the line). This voltage transient must be small enough to avoid breaking down the output transistors of the drivers on the line. If the contention current is limited to 250 mA, the magnitude of this voltage transient, on a 120Ω line, is limited to 15V, a value that is a good compromise between transistor breakdown voltage and speed.

AC PERFORMANCE

To achieve reliable transmission at high data rates over long distances, the driver should have optimum ac characteristics. The response should be fast and the output transients sharp and symmetrical.

(1) **Propagation Delay:** The propagation delay through the driver should be small compared to the bit interval so that the data stream does not encounter a bottle-neck at the driver. If the propagation delay is comparable to the bit interval, the driver will not have time to reach the full voltage swing it is capable of. In lines a few hundred feet long, the line delay would impose greater limits on data throughput than the driver propagation delay. However, a fast driver would be desirable for short haul networks such as those in automobile vehicles or disc drives; in the latter case high data throughput would be essential. Driver propagation delays less than 20 ns would be very good for a wide range of applications.

(2) **Transition Time:** For distortion free data transmission, the signal at the farthest receiver must have rise and fall times much smaller than the bit interval. Signal distortion results from driver imbalance, receiver threshold offset and skew. RS-485 limits the DC imbalance in the driver output to ±0.2V i.e., 13% of worst-case signal amplitude. Usually, the greatest distortion is caused by offset in the receiver threshold. In a long line in which a 1.5V driver output signal amplitude is attenuated by the loop resistance to about 0.4V, a 200 mV offset in the receiver threshold can cause severe pulse width distortion if the rise time is comparable to the bit interval. For lines longer than about five hundred feet, the rise time would be dominated by the line and not the driver. In short-haul networks, the transient response of the driver can significantly affect signal distortion; a faster transient creates less distortion and hence permits a smaller bit interval and a higher baud rate. A rise time less than 20 ns will be a good target spec., for it will permit a baud rate of 10 Meg over 50′ of standard twisted pair wire with less than 5% distortion.

The driver should provide the above risetime and propagation delay numbers while driving a reasonable capacitance, say 100 pF from each output, in addition to the maximum resistive load of 54Ω. A properly terminated transmission line appears purely resistive to the driver. Most manufacturers take this into account and specify their driver delays with 15 pF loads. However, if any disabled transceivers are situated close to the driver (such that the round trip delay is less than the rise time), the input capacitances of these transceivers will appear as lumped circuit loads to the driver. The driver output rise time will then be affected by all other devices in such close proximity. In the case of high speed short-haul networks, where rise time and propagation delay are critical, several devices could be clustered in a short span. In such an instance, specifying propagation delays with 15 pF loads is quite meaningless. A 100 pF capacitive load is more reasonable; even if we allocate a generous 20 pF per transceiver, it allows up to six transceivers to be clustered together in an eight foot span (the eight foot span is the approximate round trip distance travelled by the wavefront in one rise time of 20 ns).

(3) **Skew:** The ideal differential driver will have the following waveform characteristics: the propagation delay times from the input to the high and low output states will be equal; the rise and fall times of the complementary outputs will be equal and the output waveforms will be perfectly symmetrical.

If the propagation delay to the low output state is different from the propagation delay to the high output state, there is said to be 'propagation skew' between output states. If a square wave input is fed into a driver with such skew, the output will be distorted in that it will no longer have a 50% duty cycle.

If the mid-points of the waveforms from the two complementary driver outputs are not identical, there is said to be SKEW between the complementary outputs. This type of skew is undesirable because it impairs the noise immunity of the system and increases the amount of electromagnetic emission.

Figure 3a shows the differential signal from a driver that has no skew. *Figure 3b* shows the case when there is 80 ns of skew. The first signal makes its transition uniformly and passes rapidly through 0V. The second waveform flattens out for tens of nanoseconds near 0V. Unfortunately, this flat region occurs near the receiver threshold. A common mode noise spike hitting the inputs of a slightly unbalanced receiver would create a small differential noise pulse at the receiver inputs. If this noise

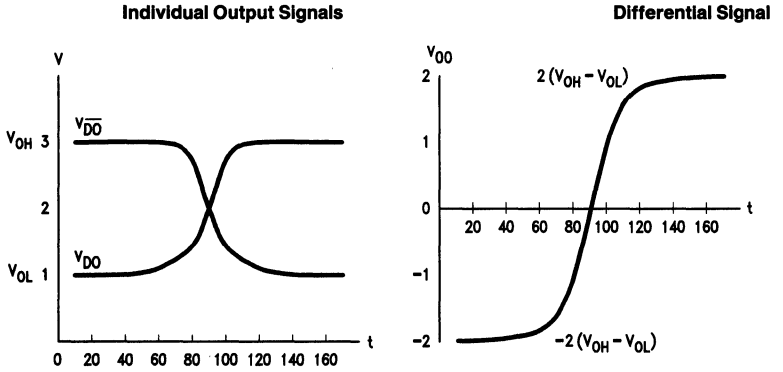

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FIGURE 3a. Transients with no Skew

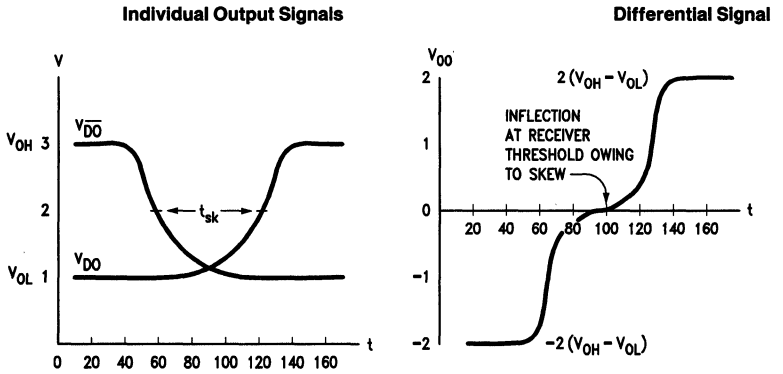

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FIGURE 3b. Skewed Transients

pulse occurs when the driver transition is flat near 0V, there will be a glitch at the receiver output. A glitch could also occur if a line reflection reaches the receiver input when the driver transition is temporarily flat. Skew is insidious in that it can cause erroneous outputs to occur at random. It can also increase the amount of electromagnetic interference (EMI) generated by the transmission system. If the complementary outputs are perfectly symmetrical, and the twisted pair medium is perfectly balanced, the radiation from one wire is cancelled exactly by the radiation from the other wire. If there is skew between the outputs, there will be net radiation proportional to the skew.

(4) **Balance:** The impedance seen looking into each of the complementary inputs of the transceiver should be identical. If there is any imbalance at these nodes, the common mode rejection will be degraded. Any DC imbalance, due to a mismatch in the receiver input resistances, will manifest itself as an offset in the receiver threshold, and can be easily detected during testing. AC imbalance is more difficult to detect, but it can hurt noise immunity at high frequencies. A sharp common mode noise spike striking an unbalanced receiver will cause a spurious differential signal. If the receiver is fast enough (as it is bound to be in most cases), it will respond to this noise signal. It is best to keep the imbalance below 4 pF. This number is reasonable to achieve; in addition, the combined imbalance of 32 transceivers will still provide sufficient immunity from h.f. interference.

DESIGN CONSIDERATIONS

The driver poses the greatest design challenge. Its speed, drive and common mode voltage requirements are best met using a bipolar process. National Semiconductor uses an established Schottky process with a 5μ deep epitaxial layer. NPN transistors are fabricated with LVCEO values greater than 15V to satisfy the breakdown requirements. It will be seen that lateral PNP transistors are crucial to the driver. The 5μ EPI process provides adequate lateral PNP transistors, and NPN transistors of sufficient speed.

Figure 4 shows the driver output circuit used by National. It is a standard totem pole output circuit modified to provide a common mode range that exceeds the supply limits. If the driver output is to be taken to -7V while the driver is in TRI-STATE, precautions must be taken to prevent the substrate diodes from turning on. This is achieved in the lower output transistor Q1 by including Schottky diode S1 in series. The only way to isolate the upper half of the totem pole from the substrate is by using a lateral PNP transistor. In *Figure 4,* a lateral PNP transistor is used to realize current source IG. Lateral PNP transistors are, however, notoriously slow; the trick therefore is not to use the PNP transistor in the switching path. In the circuit shown, the PNP transistor is a current source which feeds NPN transistor Q2 and therefore, does not participate in the switching function. This allows National's driver to have 15 ns propagation delays and 10 ns rise times. A Darlington stage cannot be used instead of Q2 because it would reduce the voltage swing below the 1.5V specification. Consequently, the rise time is bound to be significantly larger than the fall time, resulting in a large skew. National's driver uses a patented circuit with a plurality of discharge paths, to slow down the fall time so that it matches the rise time, and to keep the two transition times on track over temperature. This keeps the skew small (2 ns typical at 25°C) over the entire operating temperature range. The symmetry of the complementary outputs of National's DS3695 driver can be seen from the photographs in *Figure 5.* The lateral PNP transistor which has been kept out of the switching path has nevertheless got to be turned on or off when the driver is respectively enabled or disabled. Another patented circuit is used to hasten turn-on and turn-off of the lateral PNP transistors so that these switch in 25 ns instead of in 100 ns. Consequently, the driver can be enabled or disabled in 35 ns.

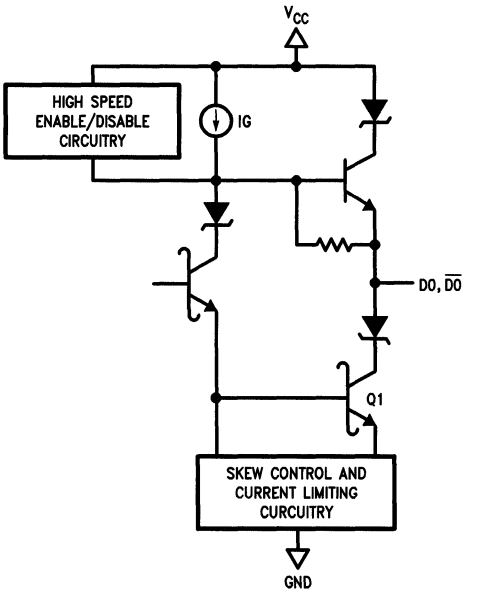

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FIGURE 4

Differential Output of National's RS-485 Driver

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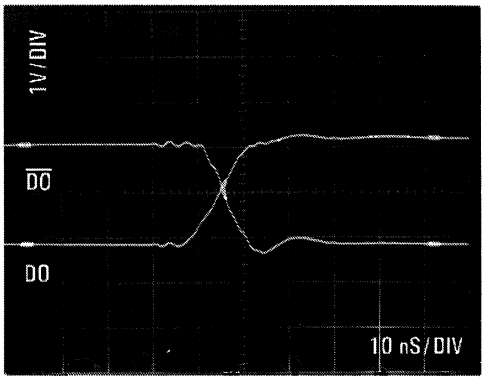
Complementary Outputs of National's RS-485 Driver



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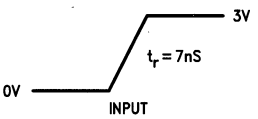

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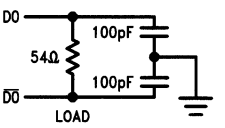

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FIGURE 5

The devices must be protected in fault conditions and contention situations. One way of doing this is by sensing current and voltage to determine power, and then if necessary, turning the device off or limiting its output current to prevent damage. This method has the advantage of fast detection of a fault and rapid recovery from one. However, too many contingencies have to be accounted for; the corresponding circuitry will increase the die size and the cost beyond what would be acceptable in many low cost applications. National preferred the simpler and inherently more reliable thermal shutdown protection scheme. Here, the device is disabled when the die temperature exceeds a certain value. This method is somewhat slower (order of milliseconds), but fast enough to protect the part. A fault would usually result from a breakdown in network protocol or from a hardware failure. In either case it is immaterial how long the device takes to shut down or recover as long as it stays undamaged. It would be useful to be notified of the occurrence of a fault in any particular channel, so that remedial action may be taken. Two of National's devices, the DS3696 receiver and the DS3698 repeater, provide a fault reporting pin which can flag the processor or drive an alarm LED in the event of a fault. National also decided to make its devices as single transceivers housed in 8 pin mini DIP packages. If thermal shutdown protection is employed, it is pointless to have dual or quad versions because a faulty channel will shut down a good one. Since most RS-485 applications will employ single channel serial data, the 8 pin package will give optimum flexibility, size and economy.

The receiver has 70 mV (typical) hysteresis for improved noise immunity. Hysteresis can contribute some distortion, especially in short lines, if the rise and fall times are different. However, this is more than adequately compensated for by the noise immunity it provides with long lines where rise times are slow. The matched rise and fall times with National's drivers assure low pulse width distortion even at short distances and high data rates.

Low Power RS-232C Driver and Receiver in CMOS

National Semiconductor
Application Note 438
Gordon W. Campbell

This article sets out to describe the new innovative low power CMOS RS-232C driver and receiver IC's introduced by National Semiconductor with particular reference to the EIA RS-232C standard. Comparison will also be made with existing bipolar driver and receiver circuits.

The DS14C88 and DS14C89A are monolithic MOS circuits utilizing a standard CMOS process. Important features are a wide operating voltage range (4.5V–12.6V), together with ESD and latch up protection and proven reliability.

The Electronics Industries Association released Data Terminal Equipment (DTE) to Data Communications Equipment (DCE) interface standards to cover the electrical, mechanical and functional interface between/among terminals (i.e. teletypewriters, CRT's etc.) and communications equipment (i.e. modems, cryptographic sets etc.).

The EIA RS-232C is the oldest and most widely known DTE/DCE standard. Its European version is CCITT V.24 specification. It provides for one-way/non-reversible, single ended (unbalanced) non-terminated line, serial digital data transmission.

The DS14C88 quad CMOS driver and its companion circuit, the DS14C89A quad CMOS receiver, combine to provide an efficient low power system for RS-232C or CCITT V.24 applications.

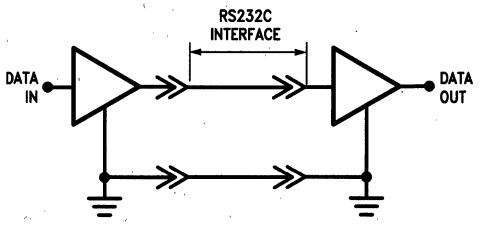

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FIGURE 1. EIA RS-232C Application

THE DRIVER

The DS14C88 quad CMOS line driver is a pin replacement of the existing bipolar circuit DS1488/MC1488.

The DS14C88 is fabricated in CMOS technology and therefore has an inherent advantage over the bipolar DS1488/MC1488 line driver in terms of current consumption. Under worst case static conditions, the DS14C88 is a miser when it comes to current consumption. In comparison with the DS1488/MC1488 line driver, a current consumption reduction to 500 μA max versus 25 mA can be achieved.

The RS-232C specification states that the required driver output voltage is defined as being between +5V and +15V and is positive for a logic "0" (+5V to +15V) and negative for a logic "1" (−5V to −15V). These voltage levels are defined when driver is loaded ($3000\Omega < R_L < 7000\Omega$). The DS14C88 meets this voltage requirement by converting HC or TTL/LSTTL levels into RS-232C levels through one stage of inversion.

In applications where strict compliance to RS-232C voltage levels is not essential, a ±5V power supply to the driver may be used. The output voltage of the DS14C88 will be high enough to be recognized by either the 1489 or 14C89A receiver as valid data.

The RS-232C specification further states that, during transitions, the driver output slew rate must not exceed 30V/μs. The inherent slew rate of the equivalent bipolar circuit DS1488/MC1488 is much too fast and requires the connection of one external capacitor (330–400 pF) to each driver output in order to limit the slew rate to the specified value. However, the DS14C88 does not require any external components. The DS14C88 has a novel feature in that unique internal slew rate control circuitry has been incorporated which eliminates the need for external capacitors; to be precise, a saving of four capacitors per package. The 14C88 minimizes RFI and transition noise spikes by typically setting the slew rate at 5V–6V/μs. This will enable optimum noise performance, but will restrict data rates to below 40k baud.

The DS14C88 can also withstand an accidental short circuit from a conductor in the interconnecting cable to any one of four outputs in a package without sustaining damage to itself or its associated equipment.

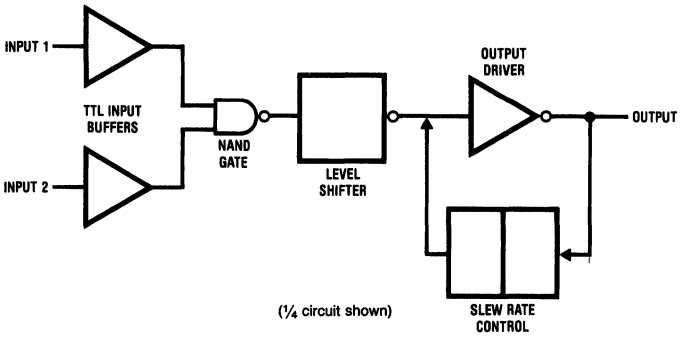

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FIGURE 2. DS14C88 Line Driver Block Diagram

THE RECEIVER

The DS14C89A quad CMOS line receiver is a pin replacement of the existing bipolar circuit DS1489/MC1489/DS1489A/MC1489A.

The DS14C89A is fabricated in CMOS technology giving it an inherent advantage over the bipolar DS1489/MC1489/DS1489A/MC1489A circuits in terms of power consumption. Under worst case static conditions a power consumption reduction of 97% (900 μA against 26 mA) is achieved.

The RS-232C specification states that the required receiver input impedance as being between 3000Ω and 7000Ω for input signals between 3.0V and 25.0V. Furthermore, the receiver open circuit bias voltage must not be greater than +2V.

The DS14C89A meets these requirements and is able to level shift voltages in the range of −30V to +30V to HC or TTL/LSTTL logic levels through one stage of inversion. A voltage of between −3.0V and −25.0V is detected as a logic "1" and a voltage of between +3.0V and +25.0V is detected as logic "0".

The RS-232C specification states that the receiver should interpret an open circuit or power off condition (source impedance of driver must be 300Ω or more to ground) as an OFF condition. In order to meet this requirement the input threshold of the DS14C89A is positive with respect to ground resulting in an open circuit or "power off" condition being interpreted as a logic "0" at the input.

Although the DS14C89A is pin replacement for the bipolar circuits DS1489/MC1489/DS1489A/MC1489A, its performance characteristics are modeled on the DS1489A/MC1489A.

The response control input on each of the bipolar circuits facilitates the rejection of noise signals by means of an external capacitor between each response control pin and ground.

When communicating between components of a data processing system in a hostile environment, spurious data such as ground shifts and noise signals may be introduced and it can become difficult to distinguish between a valid data signal and those signals introduced by the environment.

The DS14C89A eliminates the need for external response control capacitors and overcomes the effects of spurious data by means of unique internal noise filtering circuitry. *Figure 4* shows typical turn on threshold versus response control capacitance for existing bipolar devices. Note the curve for the DS14C89A CMOS device. The DS14C89A will not recognize any input signal whose pulse width is less than 1 μs, regardless of the voltage level of that input signal. Noise rejection in the bipolar parts depends on the voltage level of the noise transients. Therefore, in hostile environments the CMOS parts offer improved noise rejection properties. The DS14C89A has an internal comparator which provides input hysteresis for noise rejection. The DS14C89A has a typical turn-on voltage of 2.0V and a typical turn-off voltage of 1.0V resulting in 1.0V of hysteresis.

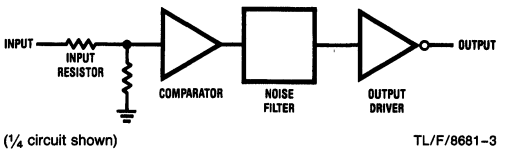

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FIGURE 3. DS14C89A Line Receiver Block Diagram

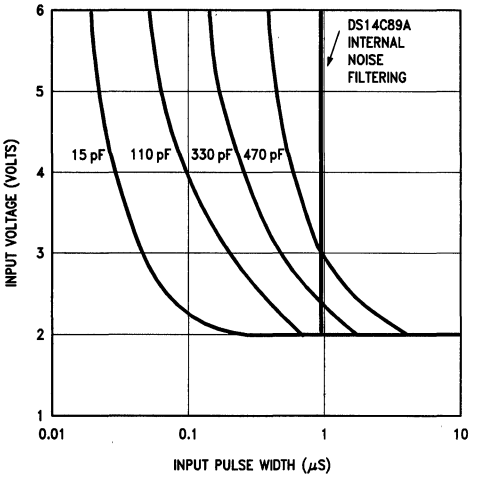

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FIGURE 4

TYPICAL APPLICATIONS

Obviously the major advantage of these CMOS devices is that with the large reduction of operating current, it is now possible to implement the "FULL" RS-232 interface in remote or portable equipment. Imagine that previously a designer, using a CMOS μP, RAM, ROM, and peripherals, could implement a complete system that consumes between 200 and 300 mW, but just adding the RS-232 interface (one driver, and one receiver) would add another 450 to 700 mW to the total system power consumption. This would severely shorten the battery life. The CMOS driver and receiver would only add about 40–50 mW.

In addition, the CMOS devices provide better noise rejection in harsh EMI environments, thus better data integrity. At the same time the internal slew rate limiting of the driver reduces the output transition time along the cable interface, hence reducing RFI emission, and easing the ability for portable (or non-portable) systems to meet FCC noise emission regulations. Also, since space is a premium in remote and portable systems, by integrating the function of the external capacitors on-chip (eliminating 8 capacitors), and designing these into S.O. packages, significant reduction in board space can be achieved.

For example, *Figure 5* shows a small CMOS system utilizing a CMOS NSC800 microprocessor, NSC858 CMOS UART, CMOS RAM/ROM, and a clock timer. This system runs off a 9V battery so a DC–DC converter is used to generate −9V for the RS-232 interface. In this design a standard DC–DC convert IC is used to generate a −9V supply from the single +9V battery.

As a second example, a "cheater" RS-232 interface is sometimes implemented. This interface is compatible with the current RS-232 driver/receiver products, but rather than using a ±(9–15)V supply, a ±5V supply is used. The drivers will not meet the RS-232 output voltage level specifications, but will correctly drive either the CMOS or bipolar receivers. The DC–DC converter circuit in *Figure 5* may be used to implement this. While for non-portable applications this can be done with the old bipolar 1488/89s, the DC–DC

converter is somewhat simpler with the CMOS parts due to the much reduced current consumption.

The RS-232 driver/receivers are also useful in non-power sensitive multi-user computers. Imagine a 16 terminal cluster controller for a multi-user computer system, *Figure 6.* This controller would require 16 drivers and 16 receivers with a total power of 8 watts when using the bipolar devices. The CMOS devices need only 400 mW.

Also proper noise rejection for receivers and slew rate limiting for the driver would require 128 capacitors for the bipolar parts, but they are unnecessary in the CMOS implementation.

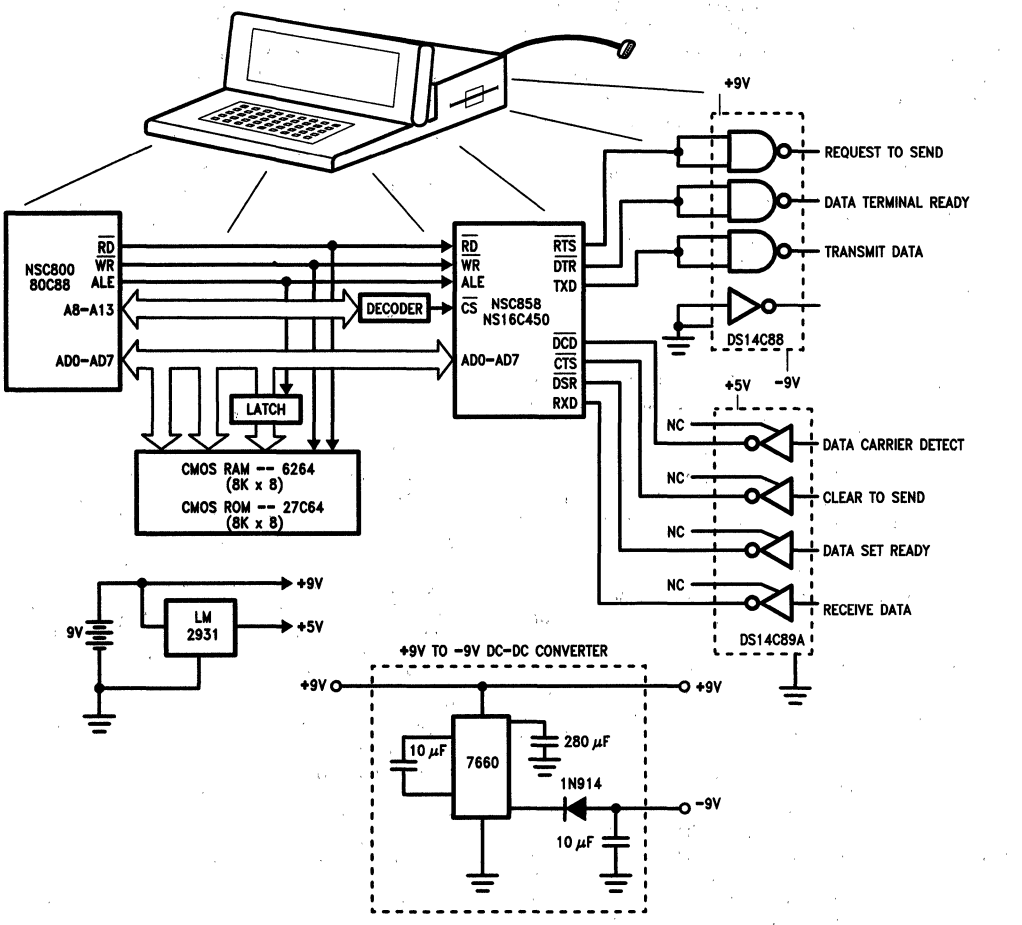

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FIGURE 5. Typical portable system application using CMOS μP, ROM, RAM, and UART. RS-232 interface is shown using 7660 supply inverter and CMOS Receiver/Driver.

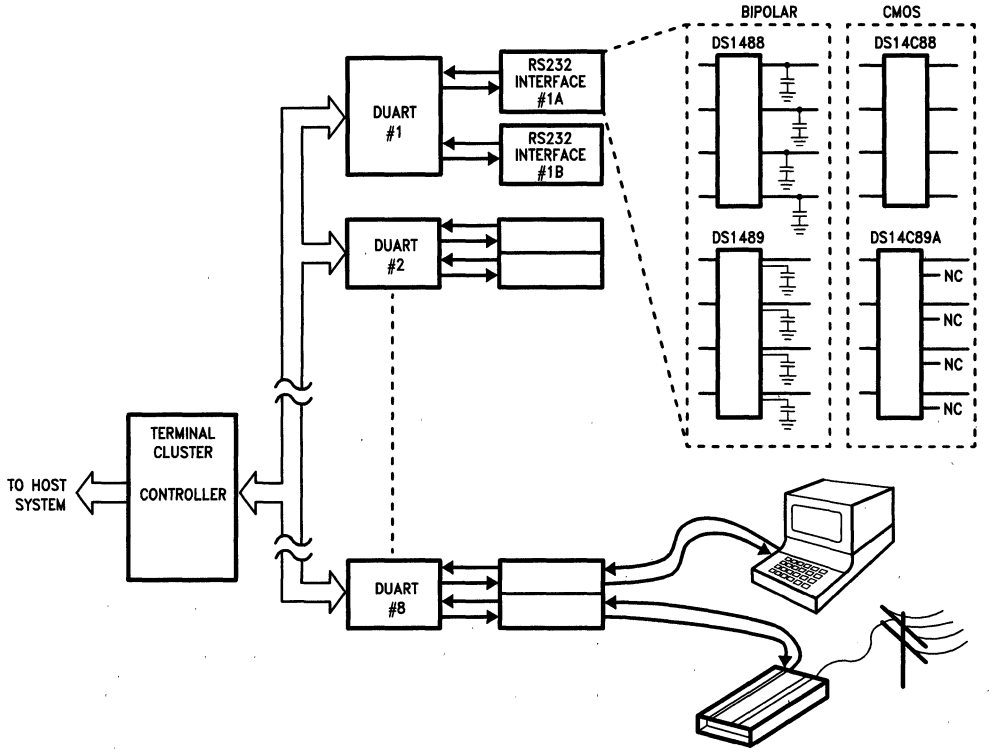

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FIGURE 6. A multi-terminal application showing a comparison of Bipolar vs CMOS solutions.

Automotive Multiplex Wiring

National Semiconductor
Application Note 454
Abdul H. Aleaf

INTRODUCTION

The evolutionary development of vehicle electronic systems has rapidly increased the number of individual wires in the vehicle. The conventional wiring harness will not provide solutions to the problems such as reducing size and weight in addition to meeting cost and reliability objectives. Several approaches have been taken to provide long term solutions. None has succeeded. Miniaturization of cables and wires is one example of a temporary solution.

Multiplexing on the other hand has been regarded as a technique which allows considerable savings to be made in the size and cost of the harness. It can also enhance reliability by reducing the number of electrical connections.

In a multiplex system the control functions will be distributed around the vehicle and complex interconnections between diagnostic terminals, sensors, instruments and switches will not add to the harness complexity. With all its advantages it has not been implemented on a production car yet. The reason has been economical feasibility and lack of suitable semiconductor components for power switching. But, with the rapid technology advances in power FETs and introduction of low cost microcomputers, multiplex wiring can be regarded as a logical successor to conventional wiring systems. Extended development efforts are necessary to introduce a reliable system at reasonable cost.

The Microcontroller Applications Group at National Semiconductor has taken a step towards this goal. A low end multiplex wiring system focusing on asynchronous serial communication in a multi node network has been developed. This paper describes the development of this system on an abstract model which forms the basis for analysis of communication protocol and various node functions.

SYSTEM CONFIGURATION

Figure 1 presents a general view of the system. The system is a centralized single master multiple slave-node scheme. All units are connected together by a balanced twisted pair. The expandable interconnection of different subsystems is achieved with 9600 Baud communication over a standard UART bus. The bus handles the interface between a master controller and the intelligent nodes.

The approach to have a centralized control system offers several advantages as compared against a non-centralized system. It prevents the problem of bus monopolization by a faulty node and is potentially cheaper due to the need for only one complex node (master). The master-slave architecture also prevents bus contention problems.

The master is a COP420L. The COP420L is a 4-bit microcontroller with a software UART that handles asynchronous communication with other processors at speeds up to 9600 Baud.

The use of 4-bit 49¢ microcontrollers (COP413L) at the nodes not only provides intelligence which reduces the required bus bandwidth, it also reduces the incremental cost associated with automotive multiplexing. All standard nodes are identical. One standard program is used. This uniformity contributes to the system flexibility and expandability. External standard nodes may be added to the system to control additional functions. Node types and addresses are selected via external wire jumpers or switches. The slave nodes consist of four remote units to handle functions such as headlamps, tail lamps, etc. These nodes are the front right, front left, rear right and rear left nodes. Incorporated into the system are also a keyboard node, a EIC node and a display node.

The keyboard node may call for a control action at any time. This node is being continuously monitored by the master controller which receives status and processes the command or information.

Overall system intelligence and flexibility is increased by dedicating a node to NS455 the Terminal Management Processor. This node takes the responsibility to display information on a 4″ flat CRT display.

An Electronic Instrument Cluster (EIC) system is a completely independent system. It typically performs all functions associated with the automobile dashboard such as vehicle speed, odometers to accumulate mileage, gauges to display engine temperature, fuel level and so on. It also indicates error conditions such as high engine temperatures, low fuel level etc. The multiplex wiring system uses a standard slave node as a bridge between the two independent systems. The slave node monitors error conditions from the EIC system and passes them to the master node upon request. It becomes relatively simple to allow the master to access all activity in the EIC system via additional commands to the slave node serving the EIC system:

THE COMMUNICATION PROTOCOL

The master unit addresses the remote units sequentially and receives a status reply from each individual node. Data communication is via the standard UART format. It has a start bit, eight data bits, an even parity bit and one stop bit.

Information to be transmitted from the master to a slave node is organized as a frame. Each frame contains the address of destination and command or data. The information in a frame is transmitted as byte format. Address/data differentiation is done by means of a flag. The byte is an address byte if the MSB is set ("1"), otherwise it is a data byte.

Two different types of addressing schemes have been incorporated into the communication protocol; node addressing and class addressing. A class of nodes is formed by grouping together slave nodes with common functions. Commands may be executed either by specific individual nodes or by slave classes. All nodes of the same class execute the command simultaneously. The system implementation at National involved four classes with seven slave nodes per class. So, the total number of nodes possible in this system is 28.

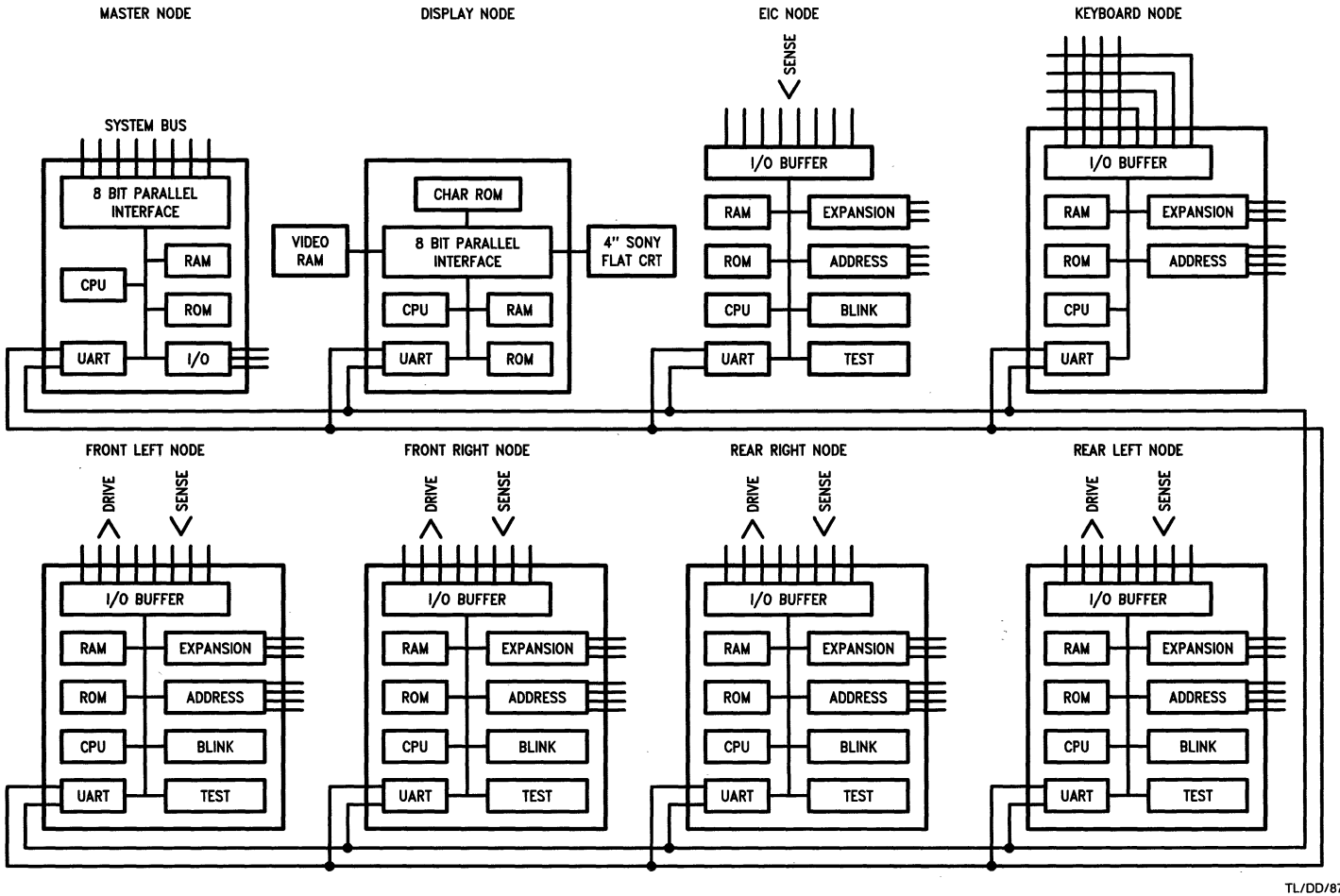

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FIGURE 1. Block Diagram

The partitioning between the class address and node address reduces the density of bus traffic significantly by eliminating repetative command transmission to individual node class. Lower bus traffic implies that lower transmission bit rate can be used, allowing additional noise immunity. Another advantage of the class addressing is the provision of synchronization for control signals such as HAZARD, LEFT/RIGHT turns.

Error correction is incorporated into the communication protocol. The UART error flags such as PARITY and FRAMING ERRORS protect the system at the physical layer. At the system level, the nodes simply avoid sending an acknowledgement to the master when an error is detected. The master times out and sends the command again.

THE MASTER NODE

The master controller is the heart of the system. Its responsibility is to generate the controlling commands and synchronize the system. It transmits to the remote units and listens to them to get the vehicle status and acts accordingly. Circuit complexity is reduced by implementing extensive software programming in the master controller. This means that the burden is essentially on the master and must be engineered to very high standards of reliability. The device used in the implementation as the master is the COP1430. It is a cost effective 4-bit single chip microcontroller. It features on chip UART which handles asynchronous communications at speeds up to 9600 Baud.

THE SLAVE NODES

The standard slave nodes are based upon the COP413L. The COP413L is a low cost 4-bit microcontroller which may be customized in production. A system such as multiplex wiring requires power consumption to be absolutely minimal. Another basic requirement is that the system should be cost effective. These two facts directed us to use the COP413L at the standard slave node. The COP413L is a low cost (49¢!) low power microcontroller from NSC drawing less than 7 mA at 4.5V to 5.5V. The device contains an 8-bit bidirectional I/O port and a serial expansion port. The CMOS version of COP413L will also be available.

THE DISPLAY NODE

This node can serve as a condition monitoring unit for the vehicle. A considerable quantity of diagnostic information collected from transducers, switches, sensors and various loads are fed to this unit to be displayed on a CRT display. The node is based on a Terminal Management Processor the NS455. The NS455 is a CRT controller on chip. The messages are updated over the serial I/O line by the master controller. The communication format is:

a) The node receives the address.

b) If address matches the local node address, send the copy command

c) Receive new address and execute.

OUTPUT STAGES

The power FETs used for local switching throughout the system are IRF541$_{(4)}$. These N-channel FETs provide much better drive circuit specification as compared to bipolar output stages. They also feature all of the well established advantages of MOSFET such as voltage control, very fast switching, and very low on state resistance. Another advantage is the lower cost as compared to comparibly rated p-channel devices.

TRANSMISSION MEDIUM

A balanced twisted pair is used for bus medium which provides high noise immunity. The transceiver selected for the bus is DS3695 *(Figure 2)*. This device is a high speed differential TRI-STATE® Bus/line transceiver designed to meet EIA standard for multipoint bus transmission. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a standard thermal shutdown circuit, which forces the driver outputs into the high impedance state.

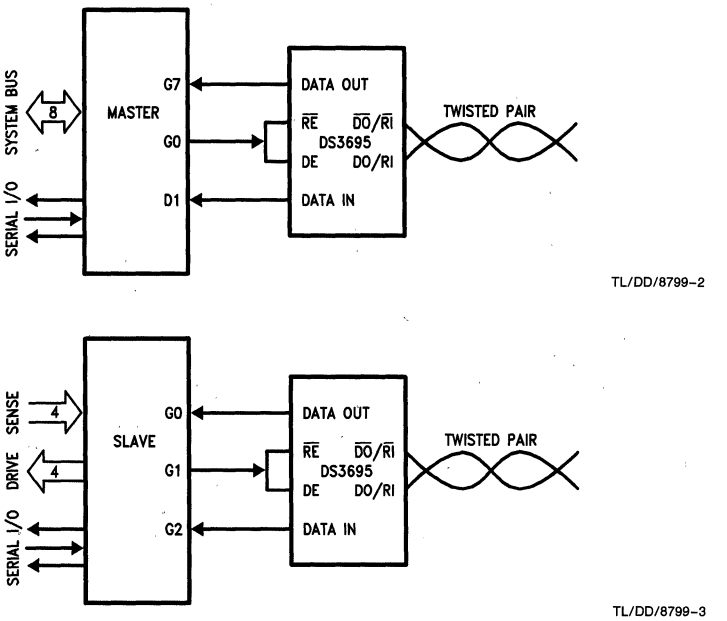

FIGURE 2. Bus Interface

CONCLUSIONS

Multiplex wiring system potentially seems to be a good replacement for conventional wiring system. Reduced complexity, increased flexibility and diagnostic capability could be achieved by incorporating microcontroller devices at nodes within the wiring system. The 4-bit microcontrollers selected are available in a price range, as low as 49¢, that will allow multiplex wiring to compare favorably on a cost-performance basis with the conventional harness.

REFERENCES

1. Michael W. Lowndes and Paul E. V. Phillips, "The Motorcar Multiplex Systems", IEE Conference on Automotive Electronics, 229, England, Nov. 1983.
2. R. F. Robins/W. J. Brittain/M. R. Lunt, "A Car Multiplex Wiring System with Self Coding Control Modules", IEE Conference on Automotive Electronics, 229, Ford Motor Company, UK, Nov. 1983.
3. Booth, J. A., 1983 "Vehicle Interconnection Systems for the Future", IEE Conference on Automotive Electronics, London, Nov. 1983.
4. International Rectifier, HEXFET Databook, 1985.

High Speed, Low Skew RS-422 Drivers and Receivers Solve Critical System Timing Problems

National Semiconductor
Application Note 457
Toan Tran
Larry Kendall

In system design, due to the distributed intelligence ability of the microprocessor, it is a common practice to have the peripheral circuits physically separated from the host processor with data communications being handled over cables. Usually, these cables are measured in hundreds or thousands of feet. Signals transmitted on these lines (or cables) are exposed to electrical noise sources which may require large noise immunity. The requirements for transmission lines and noise immunity are covered in E.I.A. standard RS-422.

The object of this application note is to describe the design requirement of RS-422 standard and to show that National's DS8921, DS8922 and DS8923 Differential Driver and Receiver pair meet all of those requirements. Special circuit design techniques are used to achieve small skew on complementary signals of the driver outputs. In fact, these devices are designed specifically for applications which must meet stringent timing constraints including the ESDI Disk Drive standard. Additionally, the DS8921 series meet the requirement of ST506 and ST412HP standards.

BALANCED VOLTAGE DIGITAL INTERFACE CIRCUITS (RS-422) REQUIREMENT

Balanced circuits are normally used in data, timing, or control applications where the data signaling rate approaches speeds of 10 Mbit/s. In addition, balanced data transmission techniques should be used whenever the following conditions exist:

1. The interconnecting cable is too long for effective unbalanced operation.
2. The interconnecting cable is exposed to a noise source which may cause a voltage sufficient to indicate a change of binary state at the load.
3. It is necessary to minimize interference with other signals.

Figure 1 below is a balanced circuit connection.

There are three major controlling factors in balanced voltage digital interface:

1. The cable length
2. The modulation rate
3. The characteristics of the Driver and Receiver

CABLE LENGTH

There is no maximum cable length specified in the RS-422 standard. Guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* below is the guideline provided by RS-422 for data modulation rate versus cable length.

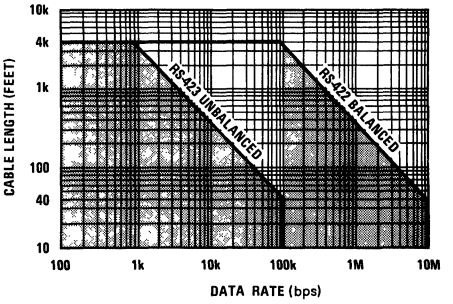

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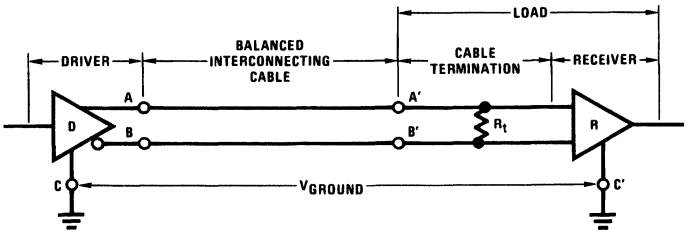
FIGURE 2. Data Modulation Rate vs Cable Length

The curve is based on empirical data using a 24 AWG, copper conductor, twisted pair cable terminated for worst case in a 100Ω load, with rise and fall time equal or less than one half unit interval at the applied modulation rate.

Even though the maximum cable length between driver and load is a function of data signaling rate, it is also influenced by the tolerable signal distortion, the amount of longitudinally coupled noise and ground potential difference introduced between the generator and load circuit grounds.



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Legend:

R_t = Optional cable transmission resistance/receiver input impedance.

V_{GROUND} = Ground potential difference

A, B = Driver interface

A', B' = Load Interface

C = Driver circuit ground

C' = Load circuit ground

FIGURE 1. RS-422 Balanced Digital Interface Circuit

MODULATION RATE

The balanced (or differential) voltage mode interface will normally be utilized on data, timing or control circuits operating at up to 10 Mbps. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates. The DS8921 family of devices meets or exceeds all of the recommended RS-422 performance specifications.

RS-422 CHARACTERISTICS

A. The Driver

The balanced driver characteristics are specified in RS-422 as follows:

1. A driver circuit should result in a low impedance (100Ω or less) balanced voltage source that will produce a differential voltage to the interconnecting cable in the range of 2V to 6V.
2. With a test load of 2 resistors, 50Ω each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the two output terminals shall be equal to or greater than 2V, or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT is reversed ($\overline{VT}$).
3. During transitions of the driver output between alternating binary states, the differential voltage measured across 100Ω load shall monotonically change between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 ns, whichever is greater. Thereafter, the signal voltage shall not change more than 10% of V_{SS} from the steady state value until the binary state occurs.

B. The Receiver

The electrical characteristics of the receiver are specified in RS-422 as follows:

1. The receiver shall not require a differential input voltage more than 200 mV to correctly assume the intended binary state, over an entire common-mode voltage range of −7 to +7V. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7V.
2. The receiver shall maintain correct operation for a differential input signal ranging between 200 mV and 6V in magnitude.
3. The maximum voltage between either receiver input terminal and receiver circuit ground shall not exceed 10V (3V signal +7V common-mode) in magnitude. Also, the receiver shall tolerate a maximum differential signal of 12V applied across its input terminals without being damaged.
4. The total load (up to 10 receivers) shall not have a resistance more than 90Ω at its input points.

DS8921, DS8922 AND DS8923

The DS8921 is a single differential line driver and receiver pair. Whereas, the DS8922 and DS8923 are dual differential line driver and receiver pairs. The difference between the DS8922 and DS8923 is in the TRI-STATE® control *(Figure 3)*.

These devices are designed to meet the full specifications of RS-422. The driver features high source and sink current capability.

The receiver will discriminate a ±200 mV input signal over a full common-mode range of ±7V. Switching noise which may occur on input signal can be eliminated by the built-in hysteresis (50 mV typical, and 15 mV min.). An input fail-safe circuit is provided so that if the receiver inputs are open, the output will assume the logical one state.

These devices have power up/down circuitry that will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or down operation.

The most attractive feature of these devices is the small skew beween the complementary outputs of the driver, typically about 0.5 ns. This small skew specification is often necessary to meet tight system timing requirements.

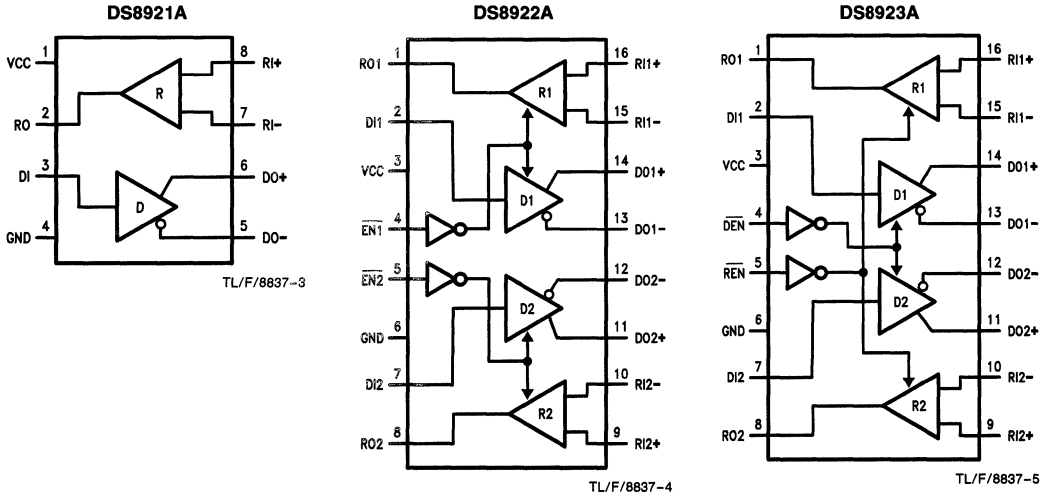
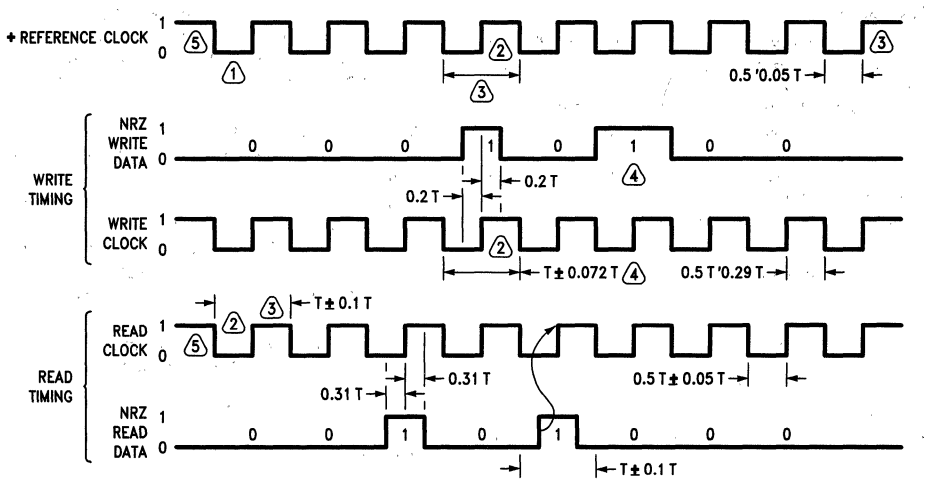


FIGURE 3. DS8921A, DS8922A and DS8923A Connection Diagrams



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Note 1. All times in ns measured at I/O connector of the drive. T is the period of the clock signals and is the inverse of the reference or read clock frequency.

Note 2. Similar period symmetry shall be in ±4 ns between any two adjacent cycles during reading and writing.

Note 3. Except during a head change or PLO synchronization the clock variances for spindle speed and circuit tolerances shall not vary more than −5.5% to +5.0%. Phase relationship between reference clock and NRZ write data or write clock is not defined.

Note 4. The write clock must be the same frequency as the drive supplied reference clock (i.e., the write clock is the controller received and retransmitted drive reference clock).

Note 5. Reference clock is valid when read gate is inactive. Read clock is valid when read gate is active and PLO synchronization has been established.

FIGURE 4. ESDI Timing Diagrams

DM74AS74 Switching Characteristics

over recommended operating free air temperature range (Note 1). All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Parameter	From	To	Conditions	DM74AS74			Units
				Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500Ω C_L = 50 pF	105			MHz
T_{PLH}	Preset or clear	Q or Q		3.3		7.5	ns
T_{PHL}				3.5		10.5	ns
T_{PLH}	Clock	Q or Q		3.5		8	ns
T_{PHL}				4.5		9	ns

FIGURE 5. 1 ns Clock Skew

ESDI ENHANCED SMALL DEVICE INTERFACE

The ESDI specification requires that the read and Reference Clock must meet the symmetry shown in *Figure 4.* This necessitates the use of National's DS8921A/22A/23A series of transceivers.

All specifications are in % T, where $T = \frac{1}{F}$, the ESDI specification is assumed to be a 10 Mbits/second standard, T = 100 ns.

Given this, the negative pulse width measured at the drive connector must equal 0.5T ±0.05T (50 ns ±5 ns). The best available RS-422 driver, other than the DS8921A Family, is specified at ±4 ns differential skew. If the clock is from a high speed 74AS74 device, shown in *Figure 5*, it will have a typical skew of 1 ns.

This combination of 4 ns +1 ns uses all of the ESDI specified 5 ns and leaves no margin for noise. Use of the DS8921A, 22A, or 23A, specified at ±2.75 ns max. differential skew would allow up to ±2.25 ns for clock skew and noise. This is as close a guarantee to meeting the ±5 ns spec. of ESDI, as is possible with todays advanced testing systems.

One other consideration is the relationship between Read Clock and Read Data. *Figure 4* shows that the positive edge of Read Clock must be 0.31T (31 ns) after the leading edge of Read Data, and 0.31T (31 ns) before the trailing edge of Read Data.

The Read Clock positive edges will be used to strobe Read Data into the controller after both signals go through their respective cable lines and receivers. Use of the DS8922A/23A assures minimum skew between these two signals. Because both drivers, or both receivers, are on the same piece of silicon an optimum match is achieved.

The above is applicable to an ESDI controller as well as the Drive itself. The controller receives the Reference Clock and uses both positive and negative edges to generate WRITE CLOCK. The negative edge of WRITE CLOCK is used to strobe out WRITE DATA and the positive edge will strobe WRITE DATA into the Drive.

The WRITE CLOCK positive edge has to be centered within WRITE DATA after it is received by the Drive. The transmitted WRITE CLOCK and WRITE DATA must be as closely matched as possible.

National's DS8921A, 22A, and DS8923A devices offer the combination of tightly spec'd parameters and drivers and receivers on one chip to meet various system timing constraints.

EMI/RFI Board Design

National Semiconductor
Application Note 643
Joe Cocovich

INTRODUCTION

The control and minimization of Electro-Magnetic Interference (EMI) is a technology that is, out of necessity, growing rapidly. EMI will be defined shortly but, for now, you might be more familiar with the terms Radio Noise, Electrical Noise, or Radio Frequency Interference (RFI). The technology's explorations include a wide frequency spectrum, from dc to 40 GHz. It also deals with susceptibility to EMI as well as the emissions of EMI by equipment or components. Emission corresponds to that potential EMI which comes out of a piece of equipment or component. Susceptibility, on the other hand, is that which couples from the outside to the inside.

In HPC designs to date, we have looked at noise situations ranging from 2 MHz to 102 MHz. EMI, in some cases, can affect radio reception, TV reception, accuracy of navigation equipment, etc. In severe cases, EMI might even affect medical equipment, radar equipment, and automotive systems.

This Application Note will define ElectroMagnetic Interference and describe how it relates to the performance of a system. We will look at examples of Inter-system noise and Intra-system noise and present techniques that can be used to ensure ElectroMagnetic Compatibility throughout a system and between systems.

We will investigate and study the sources of noise between systems through wire-harness and backplane cables and connectors. Active circuit components can be contributors of noise and be susceptible to it. The fast switching times of CMOS devices fabricated in today's technology can cause incredible noise in a system. This noise typically is made up of crosstalk, power supply spiking, transient noise, and ground bounce.

The minimization and suppression of EMI can be obtained by utilizing proper control techniques. Intra-system noise, noise within a single module, sometimes can be controlled with methods such as filtering, shielding, careful selection of components, and following good wiring and grounding procedures. Controlling noise between systems, Inter-system noise, uses subtler techniques such as frequency management and time management, etc.

Appropriate time and resources should be spent during the design of a system or systems to insure that no problems will be encountered due to effects of EMI. Design guidelines will be presented that can be used to increase ElectroMagnetic Compatibility between systems by reducing the effects of noise between them. Above all, don't forget that the development tools used are also systems and are important to consider in your planning.

A brief look will be taken at the environment and tools required for different levels of noise testing. Relative risk-costs between preparing for EMC or excluding EMI concerns from the project will be listed.

DESCRIPTION OF NOISE

ElectroMagnetic Interference

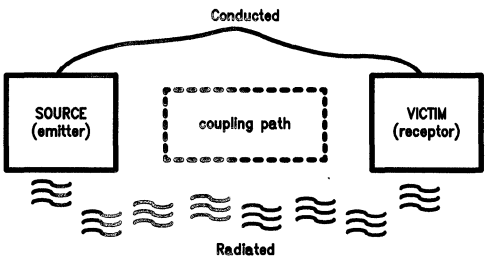
EMI is a form of electrical-noise pollution. Think of the time when an electric drill or some other power tool jammed a nearby radio with buzzing or crackling noises. Sometimes it got so bad that it prevented you from listening to the radio while the tool was in use. Or the ignition of an automobile idling outside your house caused interference to your TV picture making lines across the screen or even losing sync altogether making the picture flip. These examples are quite annoying but not catastrophic.

More serious, how about a sudden loss in telephone communication caused by electrical interference or noise while you are negotiating an important business deal? Now EMI can be economically damaging.

The results of EMI incidences can be even farther reaching than these examples. Aircraft navigation errors resulting from EMI or interruption of air traffic controller service and maybe even computer memory loss due to noise could cause two aircraft to collide resulting in the loss of lives and property.

These were just a few examples to help you identify the results of EMI in a familiar context. To help understand an ElectroMagnetic Interference situation, the problem can be divided into three categories. They are the source, the victim, and the coupling path. Secondary categories involve the coupling path itself. It the source and victim are separated by space with no hard wire connection, then the coupling path is a radiated path and we are dealing with radiated noise. If the source and victim are connected together through wires, cables, or connectors, then the coupling path is a conducted path and we are dealing with conducted noise. Incidentally, both types of noise can exist at the same time.

ElectroMagnetic Interference Situation



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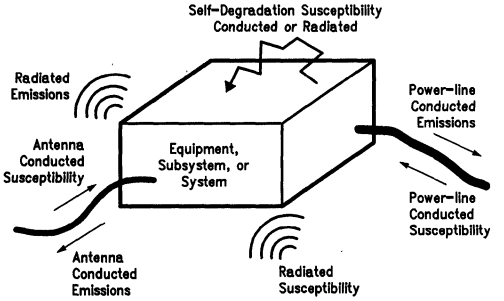
ElectroMagnetic Compatibility

If you think about the examples given, one can understand that EMI or electrical noise is of national concern. The Government and certain industry bodies have issued specifications with which all electrical, electromechanical, and electronic equipment must comply. These specifications and limitations are an attempt to ensure that proper EMC techniques are followed by manufactures during the design and fabrication of their products. When these techniques are properly applied, the product can then operate and perform with other equipment in a common environment such that no degradation of performance exists due to internally or externally conducted or radiated electromagnetic emissions. This is defined as ElectroMagnetic Compatibility or EMC.

Inter-System EMI

For the purpose of this Application Note, when the source of noise is a module, board, or system and the victim is a different and separate module, board, or system under the control of a different user, that is considered to be an inter-system interference situation. Examples of inter-system interference situations could be a Personal Computer interfereing with the operation of a TV or an anti-lock brake module in a car causing interference in the radio. This type of interference is more difficult to contain because, as mentioned earlier, the systems are generally not under the control of a single user. However, design methods and control techniques used to contain the intra-system form of EMI, which are almost always under the control of a single user, will inherently help reduce the inter-system noise.

Intra-System EMI Manifestations



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This Application Note will address problems and solutions in the area of intra-system noise. Intra-system interference situations are when the sources, victims, and coupling paths are entirely within one system or module or PC board. Systems may provide emissions that are conducted out power lines or be susceptible to emissions conducted in through them. Systems may radiate emissions through space as well as be susceptible to radiated noise. Noise conducted out antenna leads turns into radiated noise. By the same token, radiated noise picked up by the antenna is turned into conducted noise within the system. A perfect example is ground loops on a printed circuit board. These loops make excellent antennas. The system itself is capable of degrading performance due to its own internal generation of conducted and radiated noise and its susceptibility to it.

Some results of EMI within a system: Noise on power line causing false triggering of logic circuits, rapidly changing signals causing "glitches" on adjacent steady state signal lines (crosstalk) causing erratic operation, mutiple simultaneously switching logic outputs propagating ground bounce noise throughout system, etc.

Coupling Paths

The modes of coupling an emitter source to a receptor victim can become very complicated. Remember, each EMI situation can be classified into two categories of coupling, conducted and radiated. Coupling can also result from a combination of paths. Noise can be conducted from an emitter to a point of radiation at the source antenna, then picked up at the receptor antenna by induction, and re-conducted to the victim. A further complication that multiple coupling paths presents is that it makes it difficult to determine if eliminating a suspected path has actually done any good. If two or more paths contribute equally to the problem, eliminating only one path may provide little apparent improvement.

Conducted Interference

In order to discuss the various ways in which EMI can couple from one system to another, it is necessary to define a few terms. When dealing with conducted interference, there are two varieties that we are concerned with. The first variety is differential-mode interference. That is an interference signal that appears between the input terminals of a circuit. The other variety of conducted interference is called common-mode interference. A common-mode interference signal appears between each input terminal and a third point; that third point is called the common-mode reference. That reference may be the equipment chassis, an earth ground, or some other point.

Let's look at each type of interference individually. In *Figure 1* we show a simple circuit consisting of a signal source, V_S, and a load, R_L. In *Figure 2* we show what happens when differential-mode interference is introduced into the circuit by an outside source. As is shown, an interference voltage, V_D, appears between the two input terminals, and an interference current, I_D, flows in the circuit. The result is noise at the load. If, for instance, the load is a logic gate in a computer, and the amplitude of V_D is sufficiently high, it is possible for the gate to incorrectly change states.

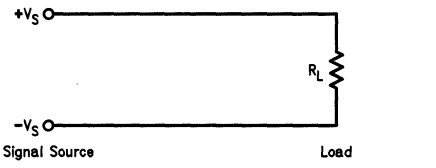

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FIGURE 1

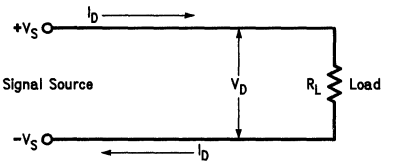

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FIGURE 2. Differential-Mode Interference

Figure 3 shows what happens when a ground loop is added to our circuit. Ground loops, which are undesirable current paths through a grounded body (such as a chassis), are usually caused by poor design or by the failure of some component. In the presence of an interference source, common-mode currents, I_C, and a common-mode voltage, V_C, can develop, with the ground loop acting as the common-mode reference. The common-mode current flows on both input lines, and has the same instantaneous polarity and direction (the current and voltage are in phase), and returns through the common-mode reference. The common-mode voltage between each input and the common-mode reference is identical.

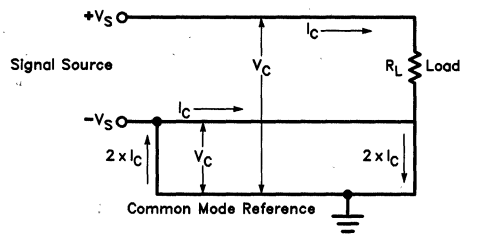

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FIGURE 3. Common-Mode Interference

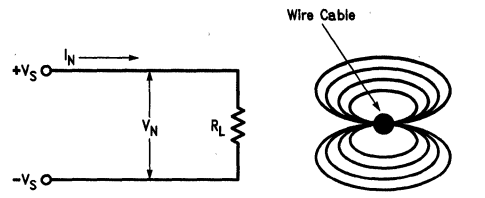

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FIGURE 4. Field-to-Cable Coupling

Radiated Interference

Radiated coupling itself can take place in one of several ways. Some of those include field-to-cable coupling, cable-to-cable coupling, and common-mode impedance coupling. Let's look at those types of coupling one at a time.

The principle behind field-to-cable coupling is the same as that behind the receiving antenna. That is, when a conductor is placed in a time-varying electromagnetic field, a current is induced in that conductor. That is shown in *Figure 4*. In this figure, we see a signal source, V_S, driving a load, R_L. Nearby there is a current carrying wire (or other conductor). Surrounding the wire is an electromagnetic field induced by the current flowing in the wire. The circuit acts like a loop antenna in the presence of this field. As such, an interference current, I_N, and an interference voltage, V_N, are induced in the circuit. The magnitude of the induced interference signal is roughly proportional to the frequency of the incoming field, the size of the loop, and the total impedance of the loop.

Cable-to-cable coupling occurs when two wires or cables are run close to one another. *Figure 5* shows how cable-to-cable coupling works. *Figure 5a* shows two lengths of cable (or other conductors) that are running side-by-side. Because any two conducting bodies have capacitance between them, called stray capacitance, a time-varying signal in one wire can couple via that capacitance into the other wire. That is referred to as capacitive coupling. This stray capacitance, as shown in *Figure 5c* makes the two cables behave as if there were a coupling capacitor between them. Another mechanism of cable-to-cable coupling is mutual inductance. Any wire carrying a time-varying current will develop a magnetic field around it. If a second conductor is placed near enough to that wire, that magnetic field will induce a similar current in the second conductor. That type of coupling is called inductive coupling. Mutual inductance, as shown in *Figure 5b*, makes the cables behave as if a poorly wound transformer were connected between them. In cable-to-cable coupling, either or both of those mechanisms may be responsible for the existance of an interference condition. Though there is no physical connection between the two cables, the properties we have just described make it possible for the signal on one cable to be coupled to the other.

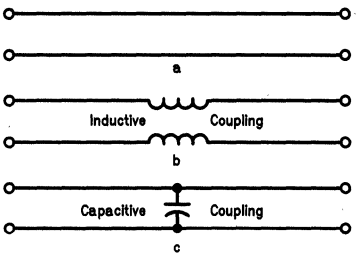

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FIGURE 5. Cable-to-Cable Coupling

Either or both of the above-mentioned properties cause the cables to be electromagnetically coupled such that a time-varying signal present on one will cause a portion of that signal to appear on the other. The "efficiency" of the coupling increases with frequency and inversely with the distance between the two cables. One example of cable-to-cable coupling is telephone "crosstalk", in which several phone conversations can be overheard at once. The term crosstalk is now commonly used to describe all types of cable-to-cable coupling.

Common-mode impedance coupling occurs when two circuits share a common bus or wire. In *Figure 6* we show a circuit that is susceptible to that type of coupling. In that figure a TL092 op-amp and a 555 timer share a common return or ground. Since any conductor (including a printed circuit board trace) is not ideal, that ground will have a non-zero impedance, Z. Because of that, the current, I, from pin 1 of the 555 will cause a noise voltage, V_N, to develop; that voltage is equal to $I \times Z$. That noise voltage will appear in series with the input to the op-amp. If that voltage is sufficient amplitude, a noise condition will result.

While not all inclusive, these coupling paths account for, perhaps, 98% of all intra-system EMI situations.

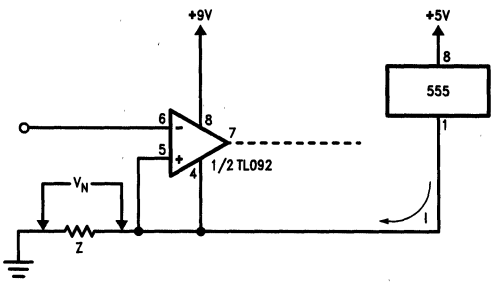

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FIGURE 6. Common-Mode Impedance Coupling

NOISE SOURCES

In this Application Note, we will look at sources of EMI which involve components that may conduct or radiate electromagnetic energy. These sources, component emitters, are different from the equipment and subsystems we have

been talking about. Component emitters are sources of EMI which emanate from a single element rather than a combination of components such as was previously described. Actually, these component emitters require energy and connecting wires from other sources to function. Therefore, they are not true sources of EMI, but are EMI Transducers. They convert electrical energy to electrical noise.

Cables and Connectors

The three main concerns regarding the EMI role of cables are conceptualized in *Figure 7*. They act as (1) radiated emission antennas, (2) radiated susceptibility antennas, and (3) cable-to-cable or crosstalk couplers. Usually, whatever is done to harden a cable against radiated emission will also work in reverse for controlling EMI radiated susceptibility. The reason for the word usually, is that when differential-mode radiated emission or susceptibility is the failure mode, twisting leads and shielding cables reduces EMI. If the failure mechanism is due to common-mode currents circulating in the cable, twisting leads has essentially no effect on the relationship between each conductor and the common-mode reference. Also cable shields may help or aggravate EMI depending upon the value of the transfer impedance of the cable shield. Transfer impedance is a figure of merit of the quality of cable shield performance defined as the ratio of coupled voltage to surface current in ohms/meter. A good cable shield will have a low transfer impedance. The effectiveness of the shield also depends on whether or not the shield is terminated and, if so, how it is terminated.

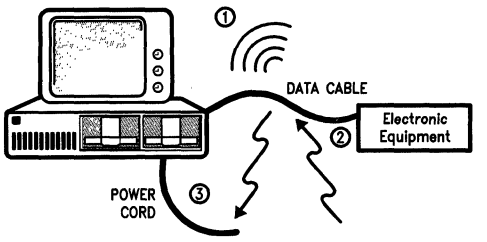

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FIGURE 7. Cables and Connectors

Connectors usually are needed to terminate cables. When no cable shields or connector filters or absorbers are used, connectors play essentially no role in controlling EMI. The influence of connector types, however, can play a major role in the control of EMI above a few MHz. This applies especially when connectors must terminate a cable shield and/or contain lossy ferrites or filter-pins.

Connectors and cables should be viewed as a system to cost-effectively control EMI rather than to consider the role of each separately, even though each offers specific interference control opportunities.

Components

Under conditions of forward bias, a semiconductor stores a certain amount of charge in the depletion region. If the diode is then reverse-biased, it conducts heavily in the reverse direction until all of the stored charge has been removed as shown in *Figure 8*. The duration, amplitude, and configuration of the recovery-time pulse (also called switching time or period) is a function of the diode characteristics and circuit parameters. These current spikes generate a broad spectrum of conducted transient emissions. Diodes with mechanical imperfections may generate noise when physically agitated. Such diodes may not cause trouble if used in a vibration-free environment.

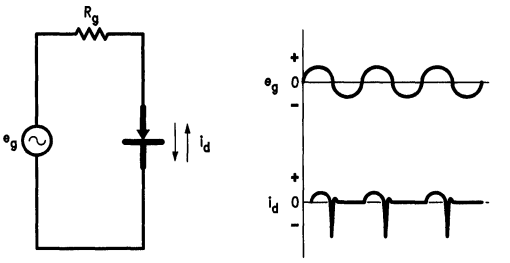

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FIGURE 8. Diode Recovery Periods and Spikes

Power Supply Noise

Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. It these transients become too large, they can cause logic errors because the supply voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. The switching transient caused by an unloaded output changing state typically equals 20 mA peak. Using the circuit shown in *Figure 9*, you can measure and display these switching transients under different load conditions.

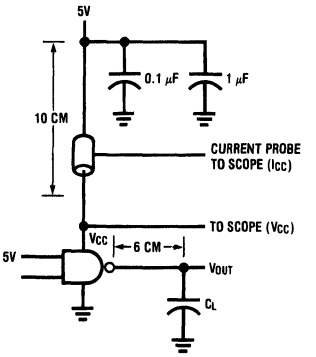

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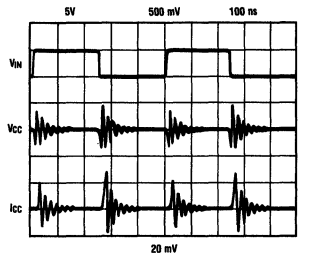
FIGURE 9

Figure 10a shows the current and voltage spikes resulting from switching a single unloaded (C_L = 0 in *Figure 9*) NAND gate. These current spikes, seen at the switching edges of the signal on V_{IN}, increase when the output is loaded. *Figures 10b*, *10c*, and *10d* show the switching transients when the load capacitance, C_L, is 15 pF, 50 pF, and 100 pF, respectively. The large amount of ringing results from the test circuit's transmission line effects. This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back again. Even for medium-size loads, load capacitance current becomes a major current contributor.



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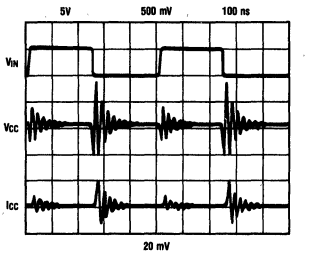
a



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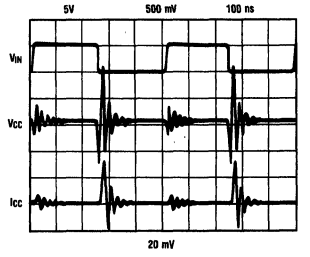
b



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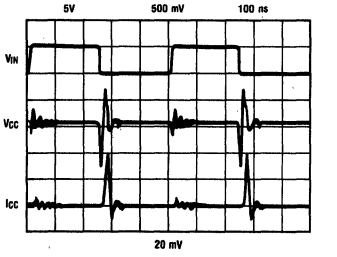
c



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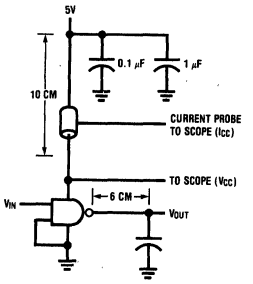
d

FIGURE 10

Although internal logic generates current spikes when switching, the bulk of a spike's current comes from output circuit transitions. *Figure 11* shows the I_{CC} current for a NAND gate, as shown in the test circuit, with one input switching and the other at ground resulting in no output transitions. Note the very small power-supply glitches provoked by the input-circuit transitions.



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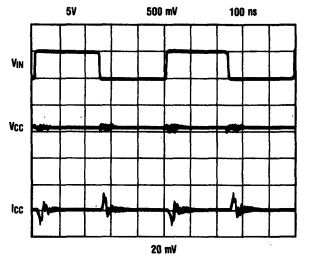

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FIGURE 11

High-Speed CMOS Logic Switching

The magnitude of noise which can be tolerated in a system relates directly to the worst case noise immunity specified for the logic family. Noise immunity can be described as a device's ability to prevent noise on its input from being transferred to its output. It is the difference between the worst case output levels (V_{OH} and V_{OL}) of the driving circuit and the worst case input voltage requirements (V_{IH} and V_{IL}, respectively) of the receiving circuit.

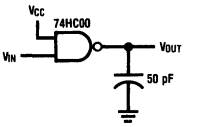
Using *Figure 12* as a guide, it can be seen that for TTL (LS or ALS) devices the worst case noise immunity is typically 700 mV for the high logic level and 300 mV for the low logic level. For HCMOS devices the worst case noise immunity is typically 1.75V for high logic levels and 800 mV for low logic levels. AC high speed CMOS logic families have noise immunity of 1.75V for high logic levels and 1.25V for low logic levels. ACT CMOS logic families have noise immunity of 2.9V for high logic levels and 700 mV for low logic levels.

Logic Family Comparisons

Characteristic	Symbol	LS/ALS TTL	HCMOS	AC	ACT
Input Voltage (Limits)	V_{IH} (Min)	2.0V	3.15V	3.15V	2.0V
	V_{IL} (Max)	0.8V	0.9V	1.35V	0.8V
Output Voltage (Limits)	V_{OH} (Min)	2.7V	$V_{CC}-0.1$	$V_{CC}-0.1$	$V_{CC}-0.1$
	V_{OL} (Max)	0.5V	0.1V	0.1V	0.1V

FIGURE 12

To illustrate noise margin and immunity, *Figure 13* shows the output that results when you apply several types of simulated noise to a 74HC00's input. Typically, even 2V or more input noise produces little change in the output. The top trace shows noise induced on the high logic level signal and the bottom trace shows noise induced on the low logic level signal.



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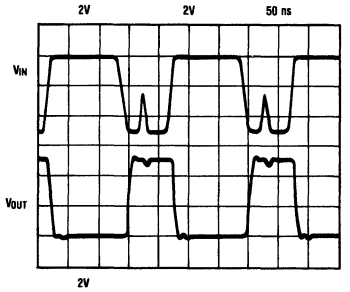

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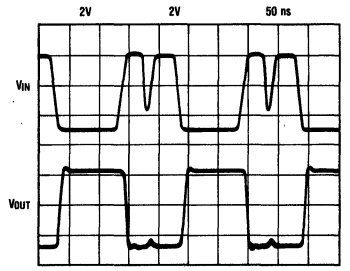

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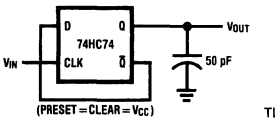
FIGURE 13

Figure 14 shows how noise affects a 74HC74's clock input. Again, no logic errors occur with 2V or more of noise on the clock input.

When using high speed CMOS, even with its greater noise immunity, crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.



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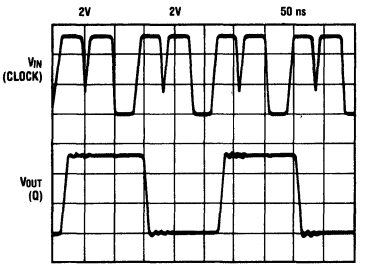

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FIGURE 14

Signal Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Our discussion on cable-to-cable coupling described crosstalk as appearing due to the distributed capacitive coupling and the distributed inductive coupling between two signal lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 15*. It should be noted that the near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of the near and far end crosstalk waveforms as shown in the figure. It also can be noted that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it.

The amplitude of the noise generated on the undriven sense line is directly related to the edge rates of the signal on the driven line. The amplitude is also directly related to

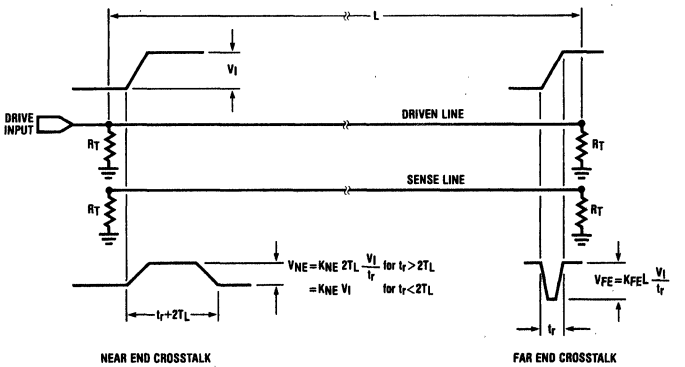

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FIGURE 15. Crosstalk

the proximity of the two lines. This is factored into the coupling constants K_{NE} and K_{FE} by terms that include the distributed capacitance per unit length, the distributed inductance per unit length, and the length of the line. The lead-to-lead capacitance and mutual inductance thus created causes "noise" voltages to appear when adjacent signal paths switch.

Several useful observations that apply to a general case can then be made:

- The crosstalk always scales with the signal amplitude V_I.
- Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.
- Far end crosstalk width is always t_r.
- For $t_r < 2\ T_L$, where t_r is the transition time of the signal on the driven line and T_L is the propagation or bus delay down the line, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is K_{NE} which is a function of physical layout only.
- The higher the value of 't_r' (slower transition times) the lower the percentage of crosstalk (relative to signal amplitude).

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than about three times the propagation delay of the line. Significant transmission line properties may be exhibited, for example, where devices having edge rates of 3 ns are used to drive traces of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Signal Interconnects

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = Z_o/(1 + C_t/C_i)^{**}0.5$$

$$t_{pde} = t_{pd} * (1 + C_t/C_i)^{**}0.5$$

where C_i = intrinsic line capacitance

C_t = additional capacitance due to gate loading.

These formulas indicate that the loading of lines *decreases* the effective impedance of the line and *increases* the propagation delay. As was mentioned earlier, lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced. One of these parasitic electrical characteristics is the inductance found in all leadframe materials.

Figure 16 shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

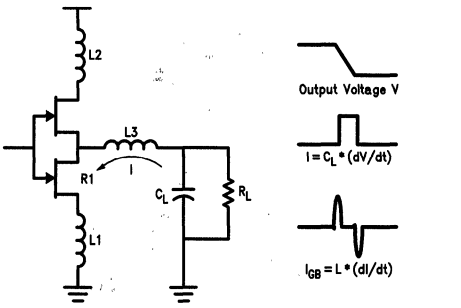

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FIGURE 16. Ground Bounce

The three waveforms shown represent how ground bounce is generated. The top waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and C_L, the load capacitance. In order to change the output from a HIGH to a LOW, current must flow to discharge the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = -C_L * (dV/dt)$]. This current, as it changes, causes a voltage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is $V = L(dI/dt)$. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{GB} = L1 * (dI/dt)$]. This induced voltage creates what is known as ground bounce.

Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground. External to the device, ground bounce causes input thresholds to shift and output levels to change.

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce though, has a much smaller amplitude and therefore does not present the same concern.

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60–70 pF, increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load itself. Moving the load away from the output also reduces the ground bounce.

- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away due to effectively lower L1 and L3.
- Voltage: lowering V_{CC} reduces ground bounce.

Ground bounce produces several symptoms:

- Altered device states.
- Propagation delay degradation.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.

NOISE SUPPRESSION TECHNIQUES

EMI control techniques involve both hardware implementations and methods and procedures. They may also be divided into intra-system and inter-system EMI control. Our major concern in this Application Note is intra-system EMI control, however, an overview of each may be appropriate at this time.

Figure 17 illustrates the basic elements of concern in an intra-system EMI problem. The test specimen may be a single box, an equipment, subsystem, or system (an ensemble of boxes with interconnecting cables). From a strictly nearsighted or selfish point-of-view, the only EMI concern would appear to be degradation of performance due to self jamming such as suggested at the top of the figure. While this might be the primary emphasis, the potential problems associated with either (1) susceptibility to outside conducted and/or radiated emissions or (2) tendency to pollute the outside world from its own undesired emissions, come under the primary classification of intra-system EMI. Corresponding EMI-control techniques, however, address themselves to both self-jamming and emission/susceptibility in accordance with applicable EMI specifications. The techniques that will be discussed include filtering, shielding, wiring, and grounding.

Inter-system EMI distinguishes itself by interference between two or more discrete and separate systems or platforms which are frequently under independent user control. Culprit emissions and/or susceptibility situations are divided into two classes: (1) antenna entry/exit and (2) back-door entry/exit. More than 95% of inter-system EMI problems involve the antenna entry/exit route of EMI. We can group inter-system EMI-control techniques by four fundamental categories: frequency management, time management, location management, and direction management.

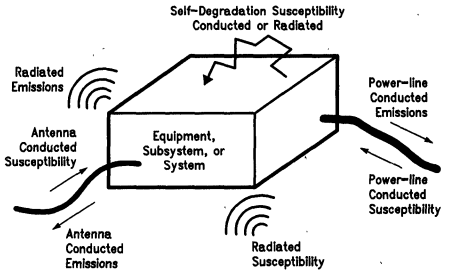

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FIGURE 17. Intra-System EMI Manifestations

The first step in locating a solution is to identify the problem as either an inter-system or intra-system EMI situation. Generally, if the specimen has an antenna and the problem develops from what exits or enters the antenna from another specimen or ambient, then the problem is identified as an inter-system EMI one. Otherwise, it is an intra-system EMI situation which we will discuss now.

Intra-System EMI-Control Techniques

Shielding

Shielding is used to reduce the amount of electromagnetic radiation reaching a sensitive victim circuit. Shields are made of metal and work on the principle that electromagnetic fields are reflected and/or attenuated by a metal surface. Different types of shielding are needed for different types of fields. Thus, the type of metal used in the shield and the shield's construction must be considered carefully if the shield is to function properly. The ideal shield has no holes or voids, and, in order to accommodate cooling vents, buttons, lamps, and access panels, special meshes and "EMI-hardened" components are needed.

Once a printed-circuit board design has been optimized for minimal EMI, residual interference can be further reduced if the board is placed in a shielded enclosure. A box's shielding effectiveness in decibels depends on three main factors: its skin, the control of radiation leakage through the box's apertures or open areas (like cooling holes), and the use of filters or shields at entry or exit spots of cables.

A box skin is typically fabricated from sheet metal or metallized plastic. Normally sheet metal skin that is 1 mm thick is more than adequate; it has a shielding effectiveness of more than 100 dB throughout the high-frequency spectrum from 1 MHz to 20 GHz. Conductive coatings on plastic boxes are another matter. Table I shows that at 10 MHz the shielding effectiveness can be as low as 27 dB if a carbon composite is used, or it can run as high as 106 dB for zinc sprayed on plastic by an electric arc process. Plastic filled materials or composites having either conductive powder, flakes, or filament are also used in box shielding; they have an effectiveness similar to that of metallized plastics.

TABLE I

Shielding Material	Surface Resistance,* Ohms/Square	Shielding Effectiveness, dB		
		At 10 MHz	At 100 MHz	At 1 GHz
Silver Acrylic Paint	0.004	67	93	97
Silver Epoxy Paint	0.1	59	81	87
Silver Deposition	0.05	57	82	89
Nickel Composite	3.0	35	47	57
Carbon Composite	10.0	27	35	41
Arc-Sprayed Zinc	0.002	106	92	98
Wire Screen (0.64 mm Grid)	N.A.	86	66	48

*Effectiveness of shielding materials with 25-μm thickness and for frequencies for which the largest dimension of the shielding plate is less than a quarter of a wavelength.

In many cases shielding effectiveness of at least 40 dB is required of plastic housings for microcontroller-based equipment to reduce printed-circuit board radiation to a level that meets FCC regulations in the United States or those of the VDE in Europe. Such skin shielding is easy to achieve. The problem is aperture leakage. The larger the aperture, the greater its radiation leakage because the shield's natural attenuation has been reduced. On the other hand, multiple small holes matching the same area as the single large aperture can attain the same amount of cooling with little or no loss of attenuation properties.

Filtering

Filters are used to eliminate conducted interference on cables and wires, and can be installed at either the source or the victim. *Figure 18* shows an AC power-line filter. The values of the components are not critical; as a guide, the capacitors can be between 0.01 and 0.001 μF, and the inductors are nominally 6.3 μH. Capacitor C1 is designed to shunt any high-frequency differential-mode currents before they can enter the equipment to be protected. Capacitors C2 and C3 are included to shunt any common-mode currents to ground. The inductors, L1 and L2, are called common-mode chokes, and are placed in the circuit to impede any common-mode currents.

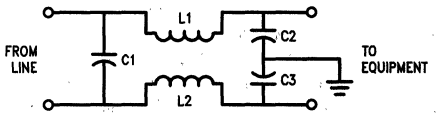

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FIGURE 18. Filtering

Wiring

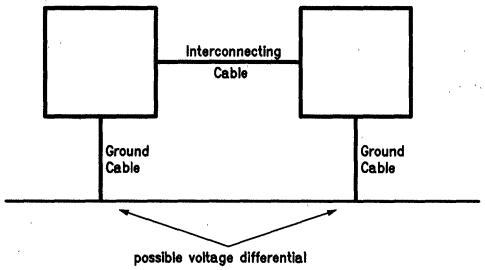
Now that the equipment in each box can be successfully designed to combat EMI emission and susceptibility separately, the boxes may be connected together to form a system. Here the input and output cables and, to a lesser extent, the power cable form an "antenna farm" that greatly threatens the overall electromagnetic compatibility of the system. Most field remedies for EMI problems focus on the coupling paths created by the wiring that interconnects systems. By this time most changes to the individual equipment circuits are out of the question.

Let us address five coupling paths that are encountered in typical systems comprised of two or more pieces of equipment connected by cables. These should adequately cover most EMI susceptibility problems. They are:

- *A common ground impedance coupling*—a conducting path in which a common impedance is shared between an undesired emission source and the receptor.
- *A common-mode, radiated field-to-cable coupling,* in which electromagnetic fields penetrate a loop formed by two pieces of equipment, a cable connecting them, and a ground plane.
- *A differential-mode, radiated field-to-cable coupling,* in which the electromagnetic fields penetrate a loop formed by two pieces of equipment and an interconnecting transmission line or cable.
- *A crosstalk coupling,* in which signals in one transmission line or cable are capacitively or inductively coupled into another transmission line.
- *A conductive path* through power lines feeding the equipment.

The first coupling path is formed when two pieces of equipment are connected to the same ground conductor at different points, an arrangement that normally produces a voltage difference between the two points. If possible, connecting both pieces of equipment to a single-point ground eliminates this voltage. Another remedy is to increase the impedance along a loop that includes the path between the ground connections of the two boxes. Examples include the isolation of printed-circuit boards from their cabinet or case, the use of a shielded isolation transformer in the signal path, or the insertion of an inductor between one or both boxes and the ground conductor. The use of balanced circuits, differential line drivers and receivers, and absorbing ferrite beads and rods on the interconnecting cable can further reduce currents produced by this undesirable coupling path.

Common Ground Impedance Coupling



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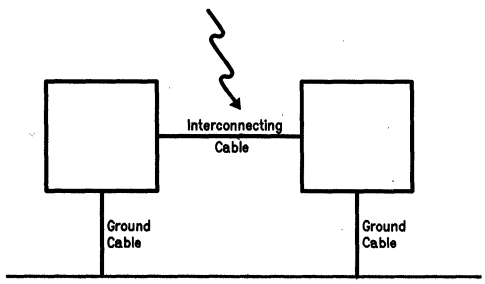
A balanced circuit is configured so its two output signal leads are electrically symmetrical with respect to ground, as the signal increases on one output the signal on the other decreases. Differential line drivers produce a signal that is electrically symmetrical with respect to ground from a single-ended circuit in which only one lead is changing with respect to ground. Ferrite beads, threaded over electrical conductors, substantially attentuate electromagnetic interference by turning radio-frequency energy into heat, which is dissipated in them.

In the second coupling path, a radiated electromagnetic field is converted into a common-mode voltage in the ground plane loop containing the interconnect cable and both boxes. This voltage may be reduced if the loop area is trimmed.

Common-Mode, Radiated Field-to-Cable Coupling



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The third coupling path produces a differential-mode voltage that appears across the input terminals of the EMI receptor. One way of controlling this is to cancel or block the pickup of differential-mode radiation. In a balanced transmission line, this is done by use of twisted-wire pairs and a shielded cable.

As for crosstalk, the fourth coupling path—the reduction of capacitive coupling can be achieved by the implementation of at least one of these steps:

- Reducing the spacing between wire pairs in either or both of the transmission lines.
- Increasing the separation between the two transmission lines.
- Reducing the frequency of operation of the source, if possible.
- Adding a cable shield over either or both transmission lines.
- Twisting the source's or receptor's wire pairs.
- Twisting both wire pairs in opposite directions.

The fifth coupling path conductively produces both common-mode and differential-mode noise pollution on the power mains. Among several remedies that can suppress the EMI here are the filters and isolation transformers.

There are only about 50 common practical remedies that can be used in most EMI situations. Of these, about 10 suffice in 80 percent of the situations. Most engineers are aware of at least some of these remedies—for example, twisting wires to reduce radiation pickup.

In order to attack the EMI problem, one can make use of the information contained in Table II. First, decide what coupling path has the worst EMI interference problem. From the 11 most common coupling paths listed at the top of the table, find the problem coupling path. Using the numbers found in that table entry, locate the recommended remedy or remedies from the 12 common EMI fixes identified at the bottom of the table. This procedure should be repeated until all significant coupling paths have been properly controlled and the design goal has been met.

Inter-System EMI Control Techniques

There are many EMI controls that may be carried out to enhance the chances of inter-system EMC. They can be grouped into four categories which we will discuss briefly. The following discussion is not intended to be complete but merely provide an overview of some EMI control techniques available to the intersystem designer and user.

Frequency management suggests both transmitter emission control and improvement of receptors against spurious responses. The object is to design and operationally maintain transmitters so that they occupy the least frequency spectrum possible in order to help control electromagnetic pollution. For example, this implies that long pulse rise and fall times should be used. Quite often one of the most convenient, economic and rapid solutions to an EMI problem in the field, is to change frequency of either the victim receiver or the culprit source.

In those applications where information is passed between systems, a possible time management technique could be utilized where the amount of information transferred is kept to a minimum. This should reduce the amount of time that the receptor is susceptible to any EMI. In communication protocols, for example, essential data could be transmitted in short bursts or control information could be encoded into fewer bits.

Location management refers to EMI control by the selection of location of the potential victim receptor with respect to all other emitters in the environment. In this regard, separation distance between transmitters and receivers is one of the most significant forms of control since interfering source emissions are reduced greatly with the distance between them. The relative position of potentially interfering transmitters to the victim receiver are also significant. If the emitting source and victim receiver are shielded by obstacles, the degree of interference would be substantially reduced.

Direction management refers to the technique of EMI control by gainfully using the direction and attitude of arrival of electromagnetic signals with respect to the potential victim's receiving antenna.

TABLE II. Electromagnetic Interference Coupling Paths

Radiated Field to Interconnecting Cable (Common-Mode)	**2, 7, 8, 9, 11**	**Radiated Field to Box**	**12, 13**
Radiated Field to Interconnecting Cable (Differential-Mode)	**2, 5, 6**	**Box to Radiated Field**	**12, 13**
Interconnecting Cable to Radiated Field (Common-Mode)	**1, 3, 9, 11**	**Box-to-Box Radiation**	**12, 13**
Interconnecting Cable to Radiated Field (Differential-Mode)	**1, 3, 5, 6, 7**	**Box-to-Box Conduction**	**1, 2, 7, 8, 9**
Cable-to-Cable Crosstalk	**1, 2, 3, 4, 5, 6, 10, 11**	**Power Mains to Box Conduction**	**4, 11**
		Box to Power Mains Conduction	**4**

Electromagnetic Interference Fixes

1. **Insert Filter In Signal Source**
2. **Insert Filter in Signal Receptor**
3. **Insert Filter in Power Source**
4. **Insert Filter in Power Receptor**
5. **Twist Wire Pair**
6. **Shield Cable**
7. **Use Balanced Circuits**
8. **Install Differential Line Drivers and Receivers**
9. **Float Printed Circuit Board(s)**
10. **Separate Wire Pair**
11. **Use Ferrite Beads**
12. **Use a Multilayer Instead of a Single-Layer Printed Circuit Boards**

DESIGN GUIDELINES

The growth of concern over electromagnetic compatibility (EMC) in electronic systems continues to rise in the years since the FCC proclaimed that there shall be no more pollution of the electromagnetic spectrum. Still, designers have not yet fully come to grips with a major source and victim of electromagnetic interference—the printed circuit board. The most critical stage for addressing EMI is during the circuit board design. Numerous tales of woe can be recounted about the eleventh hour attempt at solving an EMI problem by retrofit because EMC was given no attention during design. This retrofit ultimately costs much more than design stage EMC, holds up production, and generally makes managers unhappy. With these facts in mind, let's address electromagnetic compatibility considerations in printed circuit board design.

Logic Selection

Logic selection can ultimately dictate how much attention must be given to EMC in the total circuit design. The first guideline should be: use the slowest speed logic that will do the job. Logic speed refers to transition times of output signals and gate responses to input signals. Many emissions and susceptibility problems can be minimized if a slow speed logic is used. For example, a square wave clock or signal pulse with a 3 ns rise time generates radio frequency (100 MHz and higher) energy that is gated about on the PC board. It also means that the logic can respond to comparable radio frequency energy if it gets onto the boards.

The type of logic to be used is normally an early design decision, so that control of edge speeds and, hence, emissions and susceptibility is practical early. Of course, other factors such as required system performance, speed, and timing considerations must enter into this decision. If possible, design the circuit with a slow speed logic. The use of slow speed logic, however, does not guarantee that EMC will exist when the circuit is built; so proper EMC techniques should still be implemented consistently during the remainder of the circuit design.

Component Layout

Component layout is the second stage in PC board design. Schematics tell little or nothing about how systems will perform once the board is etched, stuffed, and powered. A circuit schematic is useful to the design engineer, but an experienced EMC engineer refers to the PC board when troubleshooting. By controlling the board layout in the design stage, the designer realizes two benefits: (1) a decrease in EMI problems when the circuit or system is sent for EMI or quality assurance testing; and (2) the number of EMI coupling paths is reduced, saving troubleshooting time and effort later on.

Some layout guidelines for arranging components according to logic speed, frequency, and function are shown in *Figure 19*. These guidelines are very general. A particular circuit is likely to require a combination and/or tradeoffs of the above arrangements. Isolation of the I/O from digital circuitry is important where emissions or susceptibility may be a problem. For the case of emissions, a frequently encountered coupling path involves a digital energy coupling through I/O circuitry and signal traces onto I/O cables and wires, where the latter subsequently radiate. When susceptibility is a problem, it is common for the EMI energy to couple from I/O circuits onto sensitive digital lines, even though the I/O lines may be "opto-coupled" or otherwise supposedly isolated. In both situations, the solution often lies in the proper electrical and physical isolation of analog and low speed digital lines from high speed circuits. When high speed signals are designed to leave the board, the reduction of EMI is usually performed via shielding of I/O cables and is not considered here.

Therefore, a major guideline in laying out boards is to isolate the I/O circuitry from the high speed logic. This method applied even if the logic is being clocked at "only" a few MHz. Often, the fundamental frequency is of marginal interest, with the harmonics generated from switching edges of the clock being the biggest emission culprits. Internal system input/output PCB circuity should be mounted as close to the edge connector as possible and capacitive filtering of these lines may be necessary to reduce EMI on the lines.

High speed logic components should be grouped together. Digital interface circuitry and I/O circuitry should be physically isolated from each other and routed on separate connectors, if possible as shown in *Figure 19d*.

- No High Frequency Signals to the Backplane

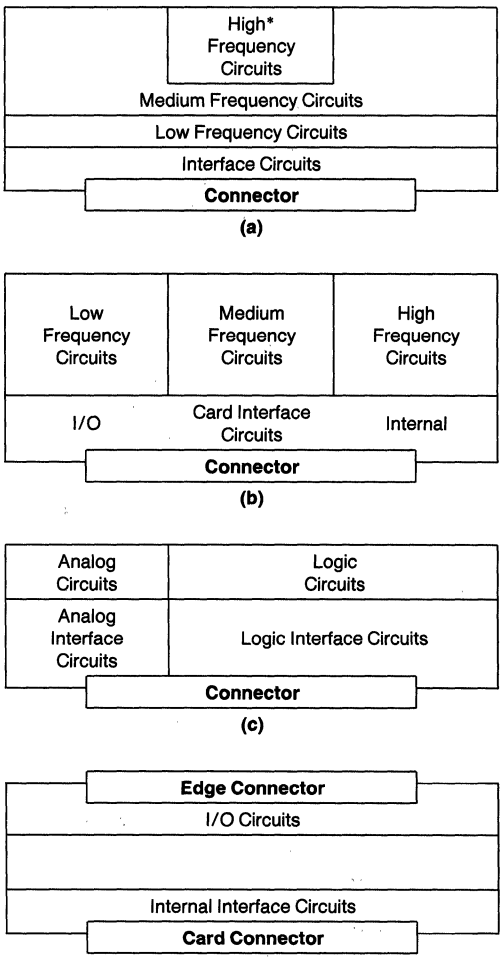

FIGURE 19. Board Layout

Power Supply Bussing

Power supply bussing is the next major concern in the design phase. Isolated digital and analog power supplies must be used when mixing analog and digital circuitry on a board. The design preferably should provide for separate power supply distribution for both the analog and digital circuitry. Single point common grounding of analog and digital power supplies should be performed at one point and one point only—usually at the motherboard power supply input for multi-card designs, or at the power supply input edge connector on a single card system. The fundamental feature of good power supply bussing, however, is low impedance and good decoupling over a large range of frequencies. A low impedance distribution system requires two design features: (1) proper power supply and return trace layout and (2) proper use of decoupling capacitors.

At high frequencies, PCB traces and the power supply busses ($+V_{CC}$ and 0V) are viewed as transmission lines with associated characteristic impedance, Z_O, as modeled in *Figure 20*. The goal of the designer is to maximize the capacitance between the lines and minimize the self-inductance, thus creating a low Z_O. Table III shows the characteristic impedance of various two-trace configurations as a function of trace width, W, and trace separation, h.

TABLE III

W/h or D/W	#1 Parallel Strips*	#2 Strip Over Ground Plane*	#3 Strips Side by Side**
0.5	377	377	NA
0.6	281	281	NA
0.7	241	241	NA
0.8	211	211	NA
0.9	187	187	NA
1.0	169	169	0
1.1	153	153	25
1.2	140	140	34
1.5	112	112	53
1.7	99	99	62
2.0	84	84	73
2.5	67	67	87
3.0	56	56	98
3.5	48	48	107
4.0	42	42	114
5.0	34	34	127
6.0	28	28	137
7.0	24	24	146
8.0	21	21	153
9.0	19	19	160
10.0	17	17	166
12.0	14	14	176
15.0	11.2	11.2	188
20.0	8.4	8.4	204
25.0	6.7	6.7	217
30.0	5.6	5.6	227
40.0	4.2	4.2	243
50.0	3.4	3.4	255

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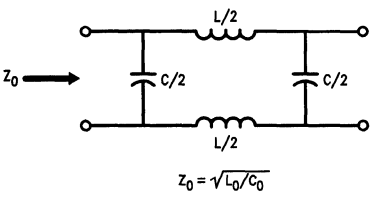
*Mylar dielectric assumed: DC = 5.0 D ≫ nearby ground plane

**Paper base phenolic or glass epoxy assumed: DC = 4.7

$Z01 = (377/\sqrt{DC}) \times (h/W)$, for $W > 3h$ and $h > 3t$

$Z02 = (377/\sqrt{DC}) \times (h/W)$, for $W > 3h$

$Z03 = (120/\sqrt{DC})\ \text{ln}\ (D/W + \sqrt{D/W^2 - 1})$ for $W \gg t$



TL/DD/10562-29

where L_O and C_O are, respectively, the distributed inductance and capacitance per unit length of the line

FIGURE 20

Any one of the three configurations may be viewed as a possible method of routing power supply (or signal) traces. The most important feature of Table III is the noticeable difference in impedance between the parallel strips and strip over ground plane compared with the side-by-side configurations.

As an example of the amount of voltage that can be generated across the impedance of a power bus, consider TTL logic which pulls a current of approximately 16 mA from a supply that has a 25Ω bus impedance (this assumes no decoupling present). The transient voltage is approximately $dV = 0.016 \times 25\Omega = 400$ mV, which is equal to the noise immunity level of the TTL logic. A 25Ω (or higher) impedance is not uncommon in many designs where the supply and return traces are routed on the same side of the board in a side-by-side fashion. In fact, it is not uncommon to find situations where the power supply and return traces are routed quite a distance from each other, thereby increasing the overall impedance of the distribution system. This is obviously a poor layout.

Power and ground planes offer the least overall impedance. The use of these planes leads the designer closer to a multi-layer board. At the very least, it is recommended that all open areas on the PC board be "landfilled" with a 0V reference plane so that ground impedance is minimized.

Multi-layer boards offer a considerable reduction in power supply impedance, as well as other benefits. As shown in Table III, the impedance of a multi-layer power/ground plane bus grows very small (on the order of an ohm or less), assuming a W/h ratio greater than 100. Multi-layer board designs also pay dividends in terms of greatly reduced EMI, and they provide close control of line impedances where impedance matching is important. In addition, shielding benefits can be realized. For high-density, high-speed logic applications, the use of a multi-layer board is almost mandatory. The problem with multi-layer boards is the increased cost of design and fabrication and increased difficulty in board repair.

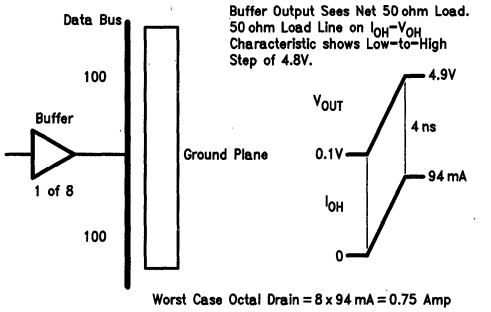
Decoupling

High-speed CMOS has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with CMOS devices in system performance and EMC performance.

Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance.

For most power distribution networks, the typical impedance can be between 50 and 100Ω. This impedance appears in series with the load impedance and will cause a droop in the

V_{CC} at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example presented in *Figure 21* used to help calculate the amount of decoupling necessary. This circuit utilizes an octal buffer driving a 100Ω bus from a point somewhere in the middle.

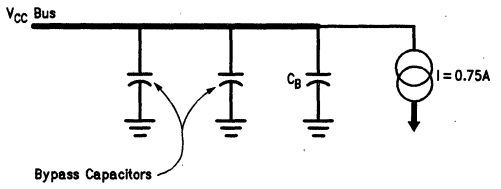


TL/DD/10562–31

FIGURE 21

Being in the middle of the bus, the driver will see two 100Ω loads in parallel, or an effective impedance of 50Ω. To switch the line from rail to rail, a drive of 94 mA is needed (4.8V/50Ω) and more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage drop across the impedance of the power lines, causing the actual V_{CC} at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will be to lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current demands. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in *Figure 22*.

In this example, if the V_{CC} droop is to be kept below 0.1V and the edge rate equals 4 ns, we can calculate the value of the decoupling capacitor by use of the charge on a capacitor equation: Q = CV. The capacitor must supply the high demand current during the transition period and is represented by I = C (dV/dt). Rearranging this somewhat yields C = I (dt/dV).



TL/DD/10562–32

Q = CV charge on capacitor
I = C dV/dt
C = I dt/dV = 750 mA × 4 ns / 0.1V = 0.030 μF
Select C_B = 0.047 μF or greater

FIGURE 22

Now, I = 750 mA assuming all 8 outputs switch simultaneously for worst case conditions, dt = switching period or 4 ns, and dV is the specified V_{CC} droop of 0.1V. This yields a calculated value of 0.030 μF for the decoupling capacitor. So, a selection of 0.047 μF or greater should be sufficient.

It is good practice to distribute decoupling capacitors evenly throughout the logic on the board, placing one capacitor for every package as close to the power and ground pins as possible. The parasitic induction in the capacitor leads can be greatly reduced or eliminated by the use of surface mount chip capacitors soldered directly onto the board at the appropriate locations. Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Proper Signal Trace Layout

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

For those situations where lines must run parallel as in address and data buses, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing.

There are several termination schemes which may be used. They are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula:

$$V_W = V_{CC} * Z_{oe} / (Z_{oe} + R_S + Z_S)$$

Series Termination

TL/DD/10562–33

$$V_w = V_{CC} \times Z_{oe}/(Z_{oe} + R_S + Z_S)$$

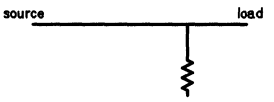
where R_S is the series resistor
Z_S is the output impedance of the driver
Z_{oe} is the equivalent line impedance

The amplitude will be one-half the voltage swing if R_S (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance (Z_{oe}). The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has

propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground depending on which bus the resistor is connected to. While this feature is not desirable for driving CMOS inputs because the trip levels are typically $V_{CC}/2$, it can be useful for driving TTL inputs where level shifting is desirable in order to interface with CMOS devices.

Parallel Termination

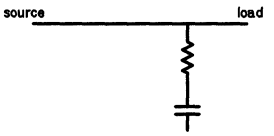


TL/DD/10562–34

AC parallel terminations work well for applications where the increase in bus delays caused by series terminations are undesirable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin terminations are not generally recommended due to their power consumption.

AC Parallel Termination



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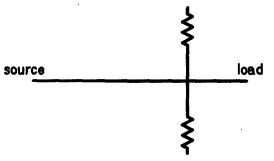
Thevenin Termination



TL/DD/10562–36

Like parallel terminations, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally be independent of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that output lines with Thevenin terminations should not be left floating since this will cause the undriven input levels to float between V_{CC} and ground, increasing power consumption.

Ground Bounce

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

- First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs. Ground bounce glitches may cause spurious inputs that will alter the state of non-clocked logic.
- Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

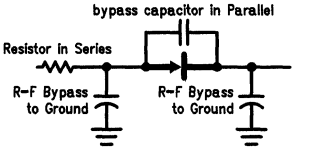
When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Choose package outputs that are as close to the ground pin as possible to drive asynchronous TTL-level inputs.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Components

The interference effect by rectifier diodes, typically found in power supply sections of PC boards, can be minmized by one or more of the following measures:

- Placing a bypass capacitor in parallel with each rectifier diode.
- Placing a resistor in series with each rectifier diode.
- Placing an R-F bypass capacitor to ground from one or both sides of each rectifier diode.
- Operating the rectifier diodes well below their rated current capability.



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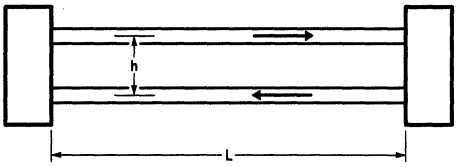
Connectors



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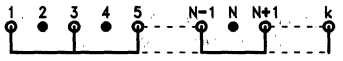
Cables and Connectors

Several options are available to reduce EMI from a typical ribbon cable used to interconnect pieces of equipment. These include:

- Reduce spacing between conductors (h in the figure) by reducing the size of wires used and reducing the insulation thickness.
- Join alternate signal returns together at the connectors at each end of the cable.
- Twist parallel wire pairs in ribbon cables.
- Shield ribbon cable with metal foil cover (superior to braid).
- Replace discrete ribbon cable with stripline flexprint cable.

In the case of joining alternate signal returns, wire N is carryig the signal current, i_n, whereas its mates, N−1 and N+1 wires are each carrying one half of the return currents, i_{n-1} and i_{n+1}, respectively. Thus, radiation from pair N and N−1 is out of phase with radiation from pair N and N+1 and will tend to cancel. In practice, however, the net radiation is reduced by 20–30 dB with 30 dB being a good default value.

Alternating Signal Returns Minimizes Radiation



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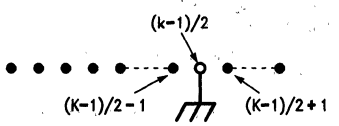
The opposite of this is to conserve signal returns by only using one, or two, wires to service N data lines in a ribbon cable. For data lines farther from the return line, the differential mode radiation becomes so great that this cable tends to maximize EMI radiation. Another disadvantage of this approach is poor impedance control in the resulting transmission line. This could result in distortion of pulses and cause reflections, especially for high-speed logic, and common return impedance noise in this single ground wire.

Single Signal Return Maximizes Radiation



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Ideally, connectors should have negligible resistance for obvious reasons other than EMI control. They should provide foolproof alignment to minimize the possibility of contact damage over time and use which would increase the resistance and be prone to vibration and shock. Adequate force to provide good mating between contacts which will insure low resistance and limit likelihood of damage. Connectors should mate with little friction to minimize the effects of continual disconnections and connections increasing the contact resistance with use as the contacts wear out. A contamination free design should be used to avoid corrosion and oxidation increasing resistance and susceptibility to shock and vibration causing intermittent contact.

Special Considerations with Development Tools

The following set of guidelines have been compiled from the experiences of the Development Systems Group and the Microcontroller Applications Group in Santa Clara. They should be considered *additional* techniques and guidelines to be followed concurrently with the standard ones already presented. Some are general and some may be specific to development systems use.

Ground bounce prevention and minimization techniques presented in this Application Note should be strictly adhered to when using '373 type transparent latches on the HPC's external address/data bus. Multiple simultaneously switching outputs could produce ground bounce significant enough to cause false latching. Observe good EMI planning by locating the latches as close to the HPC as possible. The use of multi-layer printed circuit boards with good ground planes and following appropriate layout techniques is also essential, especially if emulation will be done at frequencies above 10 MHz. With the foregoing discussions about "antenna farms", radiated noise, and ideal connector characteristics, it becomes obvious that wire-wrap boards and the use of IC sockets is absolutely out of the question. The concern here is not so much EMI affecting the outside world but EMI strangling the operation of the module itself.

The inputs to the buffers in a '244 type octal buffer package are placed adjacent or side-by-side outputs of other buffers in the package. This configuration would tend to maximize the crosstalk or noise coupling from the inputs to the outputs. On the other hand, the buffer inputs in a '544 type package are on one side of the package and the outputs are on the other. The use of these package types in high speed designs can facilitate board layout to help reduce the effects of crosstalk.

Use extra heavy ground wires between emulator and target board. Rely on the ground returns in the emulator cable for reduction of differential-mode noise radiated from the cable but heavy-duty help is required for reducing power line impedance in the integrated development system.

Unused HPC inputs, most importantly NMI and RDY/$\overline{\text{HLD}}$, must be tied to V_{CC} directly or through a pull-up resistor. This not only tends to reduce power consumption, but will avoid noise problems triggering an unwanted action.

In order to reduce the effects of noise generated by high speed signal changes, a sort of Frequency Management technique might be applied. If possible, develop application hardware and software at a slower crystal operating frequency. If ringing, crosstalk, or other combinations of radiated and conducted noise problems exist, the result may be to move the problem from one point in the affected signal waveform to a different point. Thus, apparent "noise glitches" that caused a latch to erroneously trigger when the input data was still changing, may now come at a time when they are non-destructive such as at a point when the input data is now stable.

Some applications require driving the HPC clock input, CKI, with an external signal. The emulator tools are all clocked using a crystal network with the HPC so that the generation of the system timing is contained on the tool itself. Consequently, there is no connection between the emulator cable connector on the tool and the CKI pin at the HPC. However, when the emulator cable is now inserted into the target board, the target board's clock signal travelling along the cable couples noise onto adjacent signal lines causing symptoms pointing to an apparent failure of the emulator tool. The recommendation is to disable the clock drive to the CKI pin at the HPC pad on the target board whenever the emulator tool is connected. The emulator tools supply the system clock so there is no need for the clock on the target and signal crosstalk on the emulator cable can be greatly reduced with minimal implementation. If one insists that the emulator tool and the target be synchronous, then bring the clock signal from the target to the emulator tool external to the emulator cable via twisted wire pair or coax cable. Remove the clock drive connection to CKI at the target to prevent the signal from entering the cable. Finally, remove crystal components on emulator tool to prevent problems with the signal.

Connecting boards and modules together to make a totally unique system in which EMC was practiced is necessary to ensure little problem with the environment. But, connecting

an emulator tool makes it an entirely new and unique system, both in physical and electrical properties. Treat the emulator tool as part of the system during the design phase and development phase.

NOISE MEASUREMENT

The basic purpose of FCC Part 15J is to minimize the jamming of commercial broadcasting systems by computer devices. Toward this end, the FCC has established test limits, for both conducted and radiated emissions, which must be met. These two tests together span the frequency range from 450 kHz to 1000 MHz. To accomplish FCC Part 15J testing requires the following equipment and associated support items:

- EMC Receivers or Spectrum Analyzers to cover the frequency range from 450 kHz to 1000 MHz.
- Dipole antennas (2) to cover the frequency range from 30 MHz to 1000 MHz.
- Masts or supports which will allow antenna elevation to be increased to at least 4 meters and also allow the polarization to be changed.
- Line impedance stabilization networks (LISN) built in accordance with CISPR requirements. These are 50Ω, 50 μH devices and are inserted between power mains and test item to permit making repeatable conducted EMI measurements.
- Power line filters.
- An appropriate test site.

Environment

The most controversial item on the test requirement list is the appropriate test site. The FCC required emission limits are comparable with the ambient RF level. These low limits and the noisy ambient would indicate that the tests should be made in a shielded enclosure. Unfortunately, all shielded enclosures introduce significant errors into the radiated measurements because of room reflections, room resonances, and antenna loading. To reduce the magnitude of these problems, the FCC has specified that measurements should be made at an open-field test site. Open-field test sites frequently have high ambient levels especially in the FM broadcast band. They may also have ground reflection variations as a function of soil moisture.

The FCC will permit the use of anechoic shielded enclosures which have reduced reflections, provided an error analysis is made to show correlation of interior RF levels with those of an open-field test site. The cost of an anechoic enclosure is its major drawback. For measurements other than for certification, the test site does not have to be in accordance with government regulations. There are also alternatives where an agency or private company will perform the tests for you at their facility for a nominal fee.

Many manufacturers are using shielded enclosures that they have constructed on site or purchased from one of the shielded enclosures manufacturers. The measurement requirement is that the RF ambient levels should be 6 dB or more below the specifications limits. This may require 20 dB worth of aluminum foil or 160 dB worth of electrical seals. Only a site survey can provide that answer. In any case, some margin of safety should be made, 6–10 dB, plus periodic check for reflection problems.

Instrumentation

After the appropriate test site has been obtained, whether a room or a quiet open field, then the testing can begin. If the equipment to be tested is not floor standing, the test sample is placed on a non-conducting stand 80 cm high and at least 40 cm from the wall of the enclosure. Antennas are then set up so that radiated emission levels can be measured. The test sample should be loaded with full electrical and mechanical loads and operated in a manner that closely approximates normal operation. During operation of the equipment under test, the EMI measuring equipment is used to determine the amplitude of the radiated emission.

At NSC, we have a spectrum analyzer than can be attached to a Personal Computer that runs software to control experiments and report results. It automatically marks the computer display with FCC limits for quick comparison with the amplitude of the emissions signal. This setup is outside the shielded enclosure and can be used to determine if the equipment under test is failing any FCC requirements.

If the test sample fails, we can move inside the room and use near-field probes to help pinpoint the source of emissions. The spectrum analyzer samples the signal generated by the source at many different frequencies. The scale across the bottom of the screen is frequency and the scale along the side is signal amplitude in dBuV/m. Thus, we can quickly determine where the peak amplitude of the generated noise is located, read what level that is, and at what frequency it is being generated.

A little analysis and thought should then allow you to determine what signal could be the culprit. For example, if the noise problem is at 16 MHz and the system clock is 16 MHz, then the basic clock signal is causing the problem. If the noise problem is at even multiples of 16 MHz it could be caused by rise and fall times on the 16 MHz clock or overshoot and undershoot on that clock. In the case of the HPC, since it generates a clock output that is the system clock divided by 2 (CK2 = CKI/2), the noise frequency generated at the multiple of the 16 MHz signal could also be due to CK2 or any device that is clocked by that signal. Unfortunately for the investigator, everything else inside the part is clocked by CK2, which includes bus transitions and input sampling.

Cost

Basically, the risks of no EMI control will include the following:

- Vehicle/System Performance Degradation
- Degradation to outside world equipment
- Personal Hazards
- Ordinance Hazards
- Acceptance Delays

The sum which can mean anything from a minor system or equipment performance compromise to the total cancellation of a project.

The cost of EMI control will vary and include the following:

- Government procurement requirements
- Company proposal preparation
- EMI Control Plan
- Test Plan
- EMI Tests and Reports

A rough guideline that can be used might be:

1%–3%% of $100 Million projects
3%–7% of $1 Million to $10 Million projects
7%–12% of small items

SUMMARY

The design and construction of an electromagnetically compatible printed circuit board does not necessarily require a big change in current practices. On the contrary, the implementation of EMC principles during the design process can fit in with the ongoing design. When EMC is designed into the board, the requirements to shield circuitry, cables, and enclosures, as well as other costly eleventh hour surprises, will be drastically reduced or even eliminated. Without EMC in the design stage, production can be held up and the cost of the project increases.

REFERENCES

1. Atkinson, Kenn-Osburn, John-White, Donald, *Taming EMI in Microprocessor Systems,* **IEEE Spectrum,** December 1985, pp 30–37
2. Balakrishnan, R. V., *Reducing Noise on Microcomputer Buses,* **National Semiconductor Application Note 337,** May 1983
3. Brewer, Ron W., *Test Methodology to Determine Levels of Conducted and Radiated Emissions from Computer Systems,* **EMC Technology,** July 1982, p 10
4. Engineering Staff, Don White Consultants, Inc., *The Role of Cables & Connectors in Control of EMI,* **EMC Technology,** July 1982, pp 16–26
5. Fairchild Semiconductor, *Design Considerations,* **Fairchild Advanced CMOS Technology Logic Data Book,** 1987, pp 4–3 to 4–12
6. Fairchild Semiconductor, *Understanding and Minimizing Ground Bounce,* **Application Note DU-6,** August 1987
7. Interference Control Technology, *Introduction to EMI/RFI/EMC,* **Course Notebook on Electromagnetic Compatibility,** August 1988
8. Violette, Michael F. and J.L., *EMI Control in the Design and Layout of Printed Circuit Boards,* **EMC Technology,** March-April 1986, pp 19–32
9. Violette, Michael F., *Curing Electromagnetic Interference,* **Radio-Electronics,** November 1985, pp 50–56
10. Wakeman, Larry, *High-Speed-CMOS Designs Address Noise and I/O Levels,* **National Semiconductor Application Note 375,** September 1984
11. White, Donald R. J., *EMI Control Methods and Techniques,* **Electromagnetic Interference and Compatibility — Vol 3,** copyright 1988 by Interference Control Technologies

Build a Direction-Sensing Bidirectional Repeater

National Semiconductor
Application Note 702
Gary Murdock
John Goldie

When designing an EIA-485 control bus to link widely separated machinery and process controllers, devising a scheme to control the repeaters can be one of the more awkward tasks. In long buses, bus segments are joined with repeaters if the distance exceeds the maximum allowed by one cable segment.

Usually the buses are of a master-slave configuration—a bus network can consist of a master, two slaves, and two repeaters, for instance *(Figure 1)*. Amplifying control signals and making sure that they're clearly received by the slaves is one task performed by the repeaters. Repeaters can also increase the number of slaves per cable segment, extending the control bus's reach. To ensure that signals travel through repeaters correctly in both master-to-slave and slave-to-master directions, though, the repeaters must be switched.

Controlling the switching can be a cumbersome task. One way to handle it is to generate a repeater-reversing signal at the slave location and carry it over a dedicated control line to the repeaters. The catch is that the repeater control line needs to be very long—the length of the cable segment, in fact. Handling direction control remotely introduces delays and increases the possibility of errors. Ideally, control of the repeater switching would occur locally, at the repeaters themselves. Designers can achieve this local control and get rid of repeater lines by building a smart, direction-sensing repeater.

CONTROLLING REPEATERS

To see the advantages of direction-sensing repeaters, look at a design that uses repeater control lines *(Figure 2)*. Based on the repeater control circuit used by the Intel Bitbus, this design is for twisted-pair cable. (Sometimes ribbon cable can be used instead). The differential line drivers and receivers are designed for multipoint applications and meet the EIA-485 standard.

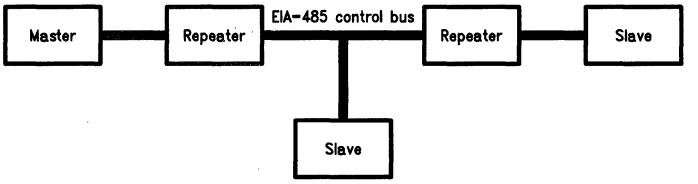

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FIGURE 1. Repeaters Extend the Length of the Twisted-Pair Bus by Transmitting the Signal on to the Next Cable Segment

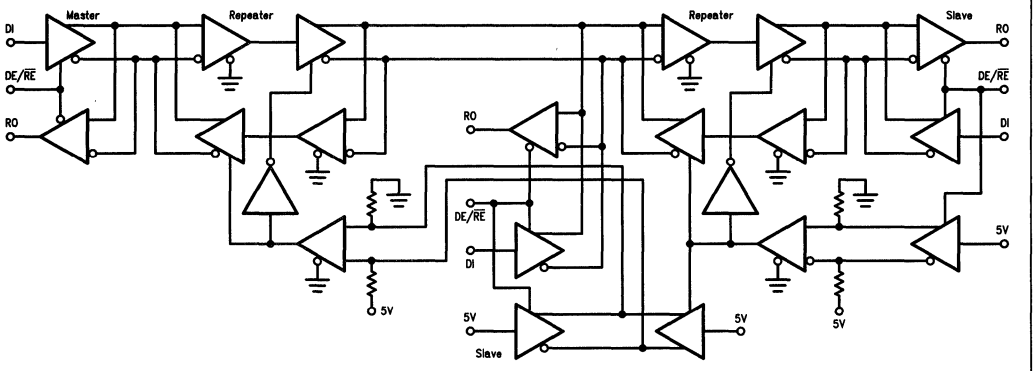

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FIGURE 2. Repeater Direction Can Be Switched from the Slave's End with a Biased Repeater-Control Line

Bias resistors on the control line typically enable the repeater in the direction away from the master. In this case, the master is the talker and the data flows in the master-to-slave direction. When a slave responds to a poll from the master, it drives its direction control line—DE/$\overline{RE}$—high. This drives the slave's repeater control line high, overriding the low state normally imposed by the bias resistors. The orientation of each repeater between the slave and the master is switched to the slave-to-master direction. All other repeaters stay enabled in the direction away from the master—letting slaves talk to any other slave, if the protocol allows it. The repeater control line is actively driven to only one state (high), so that if more than one slave tries to drive the control line at the same time, contention current is minimized.

Eliminating the repeater control line in the network greatly simplifies the circuit *(Figure 3)*. Here, a local data direction-sensing control circuit switches repeater direction. The circuit switches the repeater in the right direction by sensing which side of the data line is active first. If the master side is active first, the repeater is enabled in the master-to-slave direction, and vice versa. If the master and slave are active simultaneously, neither direction is enabled.

Two line-sense circuits work in the local control circuit. One monitors the master side of the data line, the other the slave side. The data line is active when driven to a differential high or low. The data line is inactive when all drivers connected to it are in TRI-STATE®. Resistors bias the sense circuit receiver inputs to produce high receiver outputs when the data line is inactive. When the data line is driven, the bias is overridden and the receivers respond to the signals on the data line. One output switches to the same state as the data line, and the other output switches to the complementary state. An active line sends complementary inputs to the AND gate and switches the sense circuit output low. An inactive data line produces high inputs to the AND gate (because of the resistor bias) and switches the output high. Data direction is determined by detecting which sense-circuit output (master or slave) goes low first.

The direction-sensing repeater design divides into six functional blocks *(Figure 4)*. The first block—block a—is a bidirectional repeater. Block b senses the state of the data line on each side of the repeater. It checks for either a driven state (active) or a high impedance state (inactive). Block c determines the enable signals according to the line states. Block d generates pulses used for masking, clocking, and error signals. Block e filters, generates a pulse, and detects a valid line state change. Block f latches in the most current line state information and generates the enable signals to the repeaters.

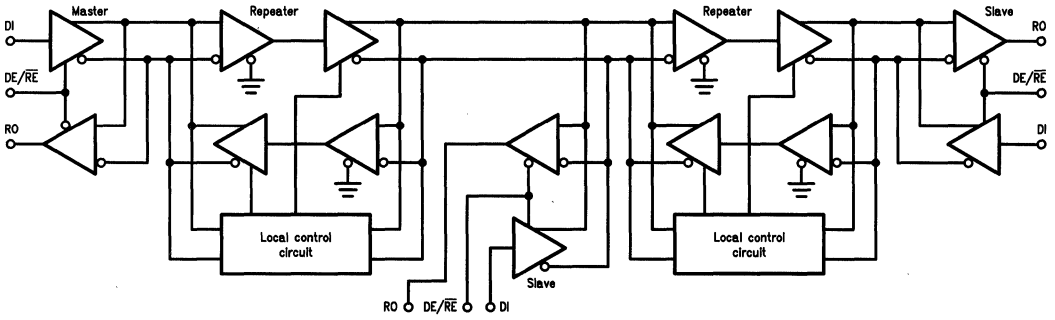

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FIGURE 3. Switching Repeater Direction Locally Avoids a Cumbersome and Costly Repeater Control Line

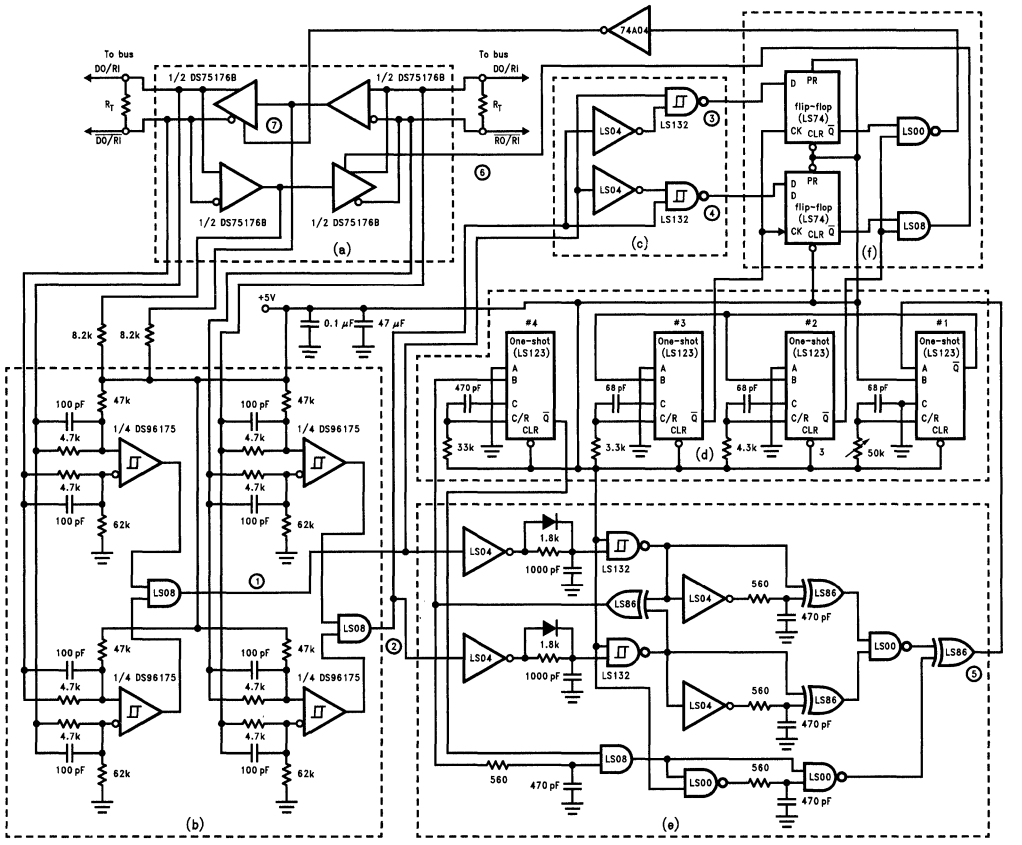

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FIGURE 4. Direction-Sensing Circuity Switches the Repeater in the Direction that Data Is Being Transmitted

The bidirectional repeater consists of two standard-pinout EIA-485 transceivers. The inverter inverts the enable line on one of the transceivers, so that two standard transceivers can be used. The "active-low" receiver enables are permanently enabled by hard-wiring them to ground. The driver enables are set by the output of the LS00 and LS08 gates. Data lines must be terminated on each side of the repeater to bias the line for the line-sense circuits. The termination resistor should be selected to match the transmission line's characteristic impedance—100Ω to 120Ω is typical for twisted pair.

In block b, an EIA-485 quad receiver senses the line to determine whether it's active or inactive. Each receiver pair monitors one side of the transmission line. The quad receiver's enable should be hard-wired ON. Resistors bias the receiver input to a positive differential voltage that produces a high ouptut when all drivers are in TRI-STATE mode. The receiver outputs are combined with an AND gate. A falling edge at the AND gate output indicates an active line, and a rising edge indicates a return to the Z line state.

The logic in block c—standard gates and the LS132 NAND gate—prevents the repeater from being enabled in case of collision. If both data lines become active at the same time, logic will disable transmission in both directions. In addition to the NAND function, the LS132 gate's inputs have hysteresis to increase noise immunity. This yields a jitter-free output from a slow input signal.

When drivers on each side of the repeater drive the line simultaneously, a collision occurs. To prevent this, the logic in block c keeps both repeater drivers off until the lines on both sides have returned to the inactive state. When a collision occurs, a low appears at signal locations 1 and 2. The logic sets the D flip-flop inputs high, however, so repeater disables—instead of enables—are generated.

When signals 1 and 2 are high, the D flip-flop inputs are high, and both repeater drivers are disabled. If either 1 or 2 is low while the other is high, an enable signal travels to one of the repeater drivers, depending upon which line is low. A valid line state change causes block d to generate a clock pulse that will latch the D flip-flops. After the repeater has turned on, signals 1 and 2 go low, since data is passing through the repeater. Because data transitions don't change the line state—it stays active—no new clock pulse is generated and the enables aren't updated.

TRIGGERING ONE-SHOTS

Block d includes four retriggerable LS123 one-shots for timing functions. The first one-shot is triggered when a valid line state change is detected. Its output trips the second and third one-shots on the same edge. The second one-shot's output is used as an enable mask, while the output of the third generates the clock pulse that latches in the latest enable bits. The fourth one-shot senses errors. It is activated when a collision occurs.

The one-shot's output pulse widths are set by external capacitors and resistors. Standard 74123 one-shots shouldn't be substituted for the LS123 devices, because the LS123 IC's clear pin is also a trigger. Also, the resistor and capacitor should be as close to the device pins as possible, to minimize stray capacitance and noise pickup. In this application, these can affect the one-shots' time constants.

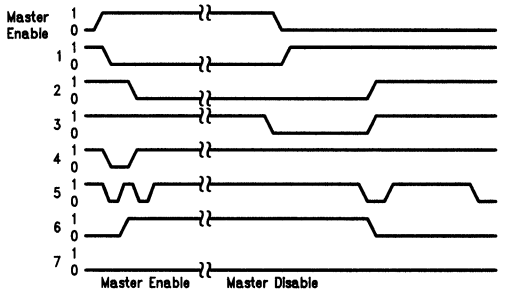
The first one-shot's resistor value is adjustable with a 50K trim pot to adjust the output pulse width. This one-shot is triggered on power-up, or by a valid line state change. Its output triggers the next two one-shots. The one-shot's output pulse is set wide enough to mask out the second pulse, caused when the data line on the other side of the repeater becomes active. When one side becomes active, a pulse is genered at point 5, triggering the first one-shot. When the repeater is enabled, the repeater drives the other side of the line. The newly active side of the line generates a second pulse, as it has changed from inactive to active. The second pulse at point 5 retriggers the first one-shot, preventing a new clock pulse. Consequently, the second and third one-shots aren't triggered.

The output of the second one-shot disables both repeater enable lines for about 200 ns. This disable inserts a minimum inactive state between every repeater direction switch, preventing it from toggling. After the minimum interval, however, the repeater can change direction. The third one-shot generates the D flip-flop clock pulse upon a valid line state change. The fourth one-shot sends an error signal to disable the repeater. The error occurs when the repeater isn't enabled between the time that one side of the transmission line becomes active and the time the other side becomes active. This scenario is also a collision, and is related to the propagation delay of the local control circuit. In this case, the enables to the repeater are kept off.

Block e filters and converts a valid line state change into a pulse, which triggers the first one-shot. The first low-pass filter cleans up spikes from the output of the line-sense circuits. Spikes appear from the difference in switching thresholds between receivers in the sense circuit. For a short time, receiver outputs are in the same state, causing a glitch at points 1 and 2 on every other signal transition. The width of the spikes depends on the data line signal transition time. For a short line, the data line capacitance is small, the signal transitions are fast, and the pulses out of the LS08 are very narrow. In most applications, though, the data line between repeaters is long, so transition time is much slower. In this case, the pulses at the LS08 output are wider. These pulses must be filtered out before they mislead the repeater into switching direction.

The first low-pass filter performs this function, with component values for a repeater linking two 1000-meter cable segments and a data rate of 200 kbaud. This filter also controls the length of time required to enable and disable the repeater. The difference between these two times is the delay of the low-pass filter. The enable time—375 ns from LS04 output to LS132 output—is shorter than the disable time—about 3.5 μs—because during enable, the capacitor charges through the diode *(Figure 5)*.

The final block masks the enable bits to the repeater when the second one-shot is triggered by the first. A latch holds the repeater direction enable bits when a valid line change has occurred. The enable lines are automatically masked for 200 ns, guaranteeing return to the inactive state and disabling the repeater when the D flip-flops are changing states.



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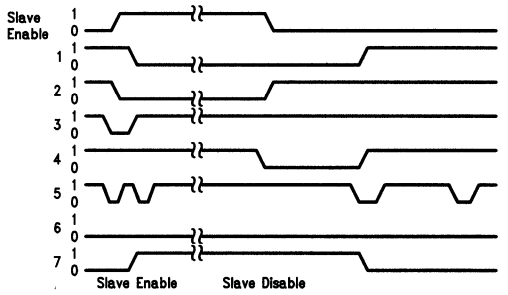

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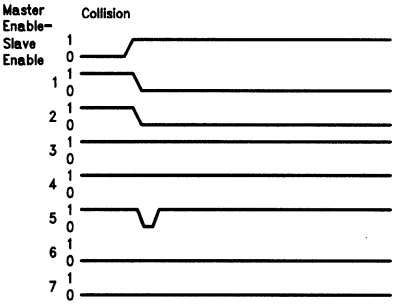

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FIGURE 5. Signals at different points in the circuit vary according to the data line conditions. There are five possible cases: Master Enable, Master Disable, Slave Enable, Slave Disable, and Collision (master and slave attempting to enable simultaneously).

To understand the timing in the master enable case, assume the master is located on the left side of the repeater and the slave on the right (*Figure 4,* again). First, both lines on either side of the repeater are inactive. The line-sense circuit outputs are high and Enables 6 and 7 are low. Next, the master drives the line high. The rising-edge line ME is the driving master's enable line. As soon as the master drives the line high, the sense circuit on the master side detects an active line state. The output of the LS08 gate pulls low, indicating the inactive-to-active state change. Lines 3 and 4 show the D flip-flop input signals. When 4 is low, the repeater is enabled in the master-to-slave direction.

On line 5, two pulses appear. The first occurs when the master side of the line changes from inactive to active. The first one-shot is triggered, generating a clock pulse. The D flip-flop latches its inputs and one repeater driver is enabled. Line 7 stays low, disabling the repeater in the direction towards the master. Line 6 becomes enabled, as a result of the master side becoming active first. The pulse created when the slave side becomes active is the second pulse on line 5. The second pulse doesn't generate a clock pulse; it retriggers the first one-shot. This one-shot can be adjusted so that the second pulse occurs within the output pulse of the first trigger. This guarantees that a new clock pulse won't be generated and keeps the repeater enabled in the same direction.

When the master has completed transmission, it is disabled and lets go of the line. The line-sense circuit detects the state change, data is latched into the D flip-flops, and enable lines 6 and 7 are pulled low.

In the slave enable case the same timing cycle takes place, with the roles of sense lines 1 and 2 and enable lines 6 and 7 reversed. When collision occurs, lines 3 and 4 stay high and neither direction is enabled. The line-sense circuits on both sides of the repeater detect a state change—from inactive to active—upon collision. The logic in block c, however, keeps the repeater disabled. The second pulse usually seen on line 5 doesn't occur, because the repeater is disabled in both directions. Both sides must return to the inactive state before the repeater can be enabled again in either direction.

Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications

National Semiconductor
Application Note 759
John Goldie

INTRODUCTION

EIA-485 is a unique interface standard because, of all the EIA Standards, only EIA-485 allows for multiple driver operation. At first glance EIA-485 and EIA-422-A appear to be very similar. Thus, EIA-485 is commonly confused with EIA-422-A. EIA-485 components (drivers and receivers) are backward compatible with EIA-422-A devices and may be interchanged. However, EIA-422-A drivers should not be used in EIA-485 applications. This application note describes the differences between EIA-422-A and EIA-485 devices.

EIA-422-A drivers face three major problems if they are used in multipoint (multiple driver) applications. The first deals with the common mode range of the drivers. The TRI-STATE® common mode range for a EIA-422-A driver is −250 mV to +6V. If a ground potential difference exists between drivers as shown in *Figure 1,* the disabled driver can come out of its high impedance state and clamp the line to one diode drop below ground. The second problem deals with contention between active drivers. Faults may occur that cause two drivers to be enabled at the same time. If this happens and the drivers are in opposite states, high currents will flow between devices. The maximum package power dissipation ratings for the devices can be easily exceeded, thermally damaging the devices. The third problem deals with drive current. For bi-directional data flow, the line should be terminated with a resistor at both ends of the cable. Therefore drivers are required to source/sink twice the current required by an EIA-422-A termination (single resistor).

PROBLEM #1—COMMON MODE RANGE

A typical bipolar EIA-422-A output structure is shown in *Figure 2.* Associated with the classical totem pole output structure is the parasitic substrate diode formed between the EPI layer and the substrate. This parasitic diode limits the negative common mode range of the driver's output. Given the case when the driver on the left is disabled (high impedance state), the driver on the right is active, and the two drivers are referenced to local grounds a fault can occur. If a ground potential difference exists between the two grounds (V_{CM}), the disabled driver can clamp the line. An example of this occurs when the disabled driver's ground is two volts higher in potential than the active driver's ground. If the output voltage goes below its ground by one diode drop, the parasitic diode becomes forward biased. For this example, assume a V_{OL} of 0.5V, and a V_{CM} of +2V. The active driver's V_{OL} is 0.5V, but with respect to the disabled driver's ground it becomes −1.5V. Clearly the EPI/SUB diode is forward biased and the line is clamped to −0.7V instead of the driven level. Data flow is not guaranteed, if the line is clamped. EIA-485 driver output structures, shown in *Figure 3,* include a Schottky diode in both the source and sink side of the output structure. This diode isolates the EPI/SUB diode from the output pin, and eliminates the possibility of the parasitic diode from turning on and clamping the data line. The common mode range is now −7V to +12V (7V from either rail). The adverse affects of this diode are minimal. The driver's V_{OL} is a Schottky diode drop higher, and V_{OH} is one diode drop lower. However, the driver's output will remain in a high impedance state for applied voltages between −7V and +12V.

PROBLEM #2—CONTENTION BETWEEN DRIVERS

If by hardware or software error two drivers are enabled at the same time, a fault occurs. In applications that use multiple drivers, protection from this fault should be considered. This fault can be more damaging to the drivers if the two active drivers are separated by a large ground potential difference. For example, transceiver one (T1) shown in *Figure 1* is referenced to earth ground GND1 (0V). While T2's ground potential (GND2) is 7V higher in magnitude with respect to GND1. If the two drivers are in opposite states, then a 12V difference exists between the drivers ($12V = V_{CM} + V_{CC}$). A large current will flow, and the maximum package power dissipation rating would be exceeded. EIA-422-A drivers do not have contention protection built in, since they are intended for use in single driver/multiple receiver applications. Power dissipation increases if multiple drivers are involved. EIA-485 line drivers are protected from this contention problem through the use of short circuit cur-

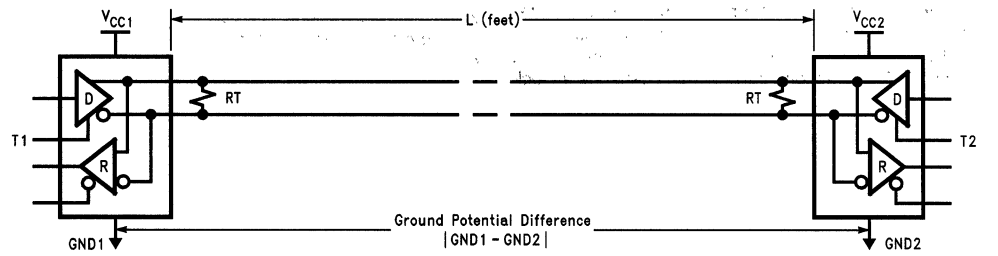

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FIGURE 1. Typical Multiple Driver Application

rent limiting over a wide common mode range. Most EIA-485 drivers have a thermal shutdown feature (although not required by EIA-485). If an active EIA-485 driver output is shorted to any voltage between −7V and +12V, the resulting current will be less than 250 mA. Realizing that drivers can be thermally damaged, ALL National Semiconductor's EIA-485 drivers feature thermal shutdown protection (TS). For example, a worse case fault occurs if the driver is shorted to +12V, and the resulting current is 250 mA. The power dissipated on the device is simply current multiplied by voltage (P=IV): 12V (250 mA) = 3W. Three watts clearly exceeds the rated maximum package power dissipation specification for all common packages. However, the thermal shutdown feature senses this fault and disables the drivers output. Hence, the 250 mA current drops to 0 mA; the device cools down and is automatically reset. If the fault is still present, the device will cycle into and out of thermal shutdown until the fault is removed. Some of National's devices feature an open collector pin that reports the occurrence of a thermal shutdown (DS3696 for example). EIA-422-A drivers would commonly incur damage when this fault occurs.

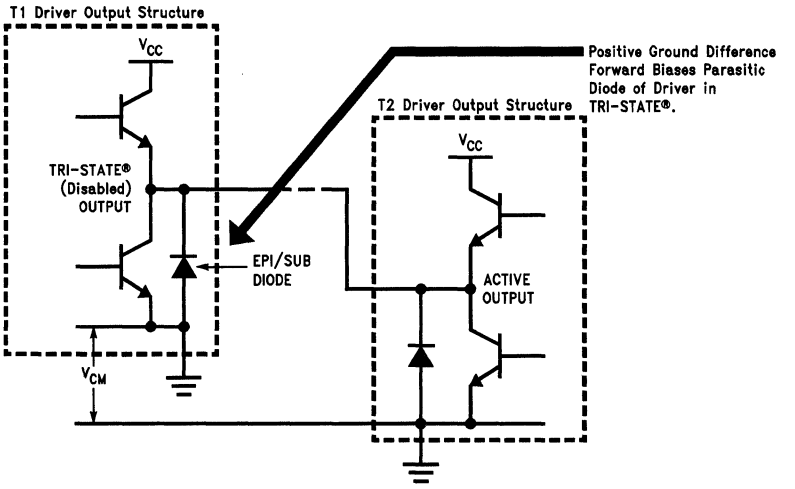

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FIGURE 2. EIA-422-A Driver Output Structures Have A Limited Common Mode Range

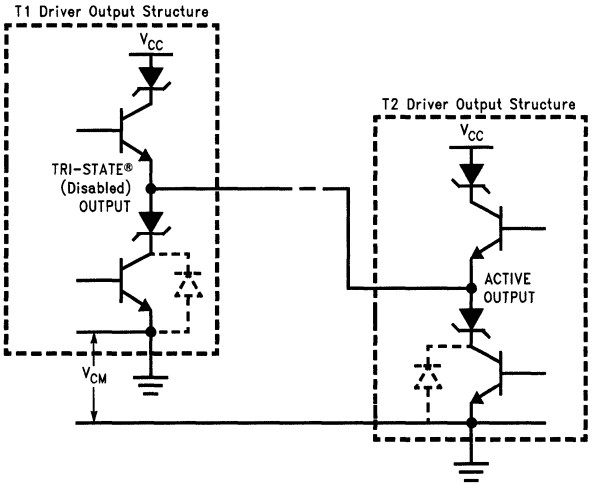

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FIGURE 3. EIA-485 Driver Output Supports −7V to +12V Common Mode Range

PROBLEM #3—DRIVE CURRENT

The third problem deals with the drivers load current capability. EIA-422-A drivers are rated at ±20 mA minimum, while EIA-485 devices have ±55 mA minimum drive capability. Current sourced by the driver either flows through the termination resistor(s), or into receiver input structures. In multiple driver applications, two termination resistors (RT) are required (one at each end of the cable), a driver would see these two resistors in parallel, resulting in a 60Ω load (assuming the termination resistors are 120Ω each). Receiver input structures are also seen in parallel by the driver, and the EIA-422-A receiver input impedance is also too low to be used in applications requiring a high number of receivers. To overcome these problems EIA-485 drivers have roughly three times the drive capability of EIA-422-A drivers. In addition EIA-485 receivers feature a higher input impedance, which is typically three times the EIA-422-A limit of 4 kΩ.

CONCLUSIONS

EIA-485 drivers are the best choice for multipoint (multiple driver) applications as shown in *Figure 4*. They can tolerate ground potential differences of up to 7V from either rail. They are contention safe and thermally protected. Finally, the drivers can handle up to 32 transceiver loads compared to EIA-422-A's limit of ten receivers. National offers a wide range of EIA-485 devices: Transceivers, Repeaters, Quad Drivers, Quad Receivers and Quad Transceivers are all offered. Select devices are available in the Industrial and Military temperature ranges. National also offers MIL-883C qualified Quad Drivers, Quad Receivers and Transceiver (see the selection guide located in the front of chapter one of the Interface Databook for a complete listing of all EIA-485 Devices).

REFERENCES

1. EIA Standard EIA-485 (RS-485), Standard for Electrical Characteristics of Generators and Receivers for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C.
2. EIA Standard EIA-422-A (EIA RS-422-A), Electrical Characteristics of Balanced Voltage Digital Interface Circuits, EIA, Washington, D.C.
3. Application Note 409, Transceivers and Repeaters Meeting the EIA RS-485 Interface Standard, Interface Databook, National Semiconductor, Santa Clara, CA.

EIA Standards can be obtained for a fee from:

Electronic Industries Association
EIA Engineering Department/Standard Sales Office
2001 Pennsylvania Avenue, N.W.
Washington, D.C. 20006
Tel: (202) 457-4988

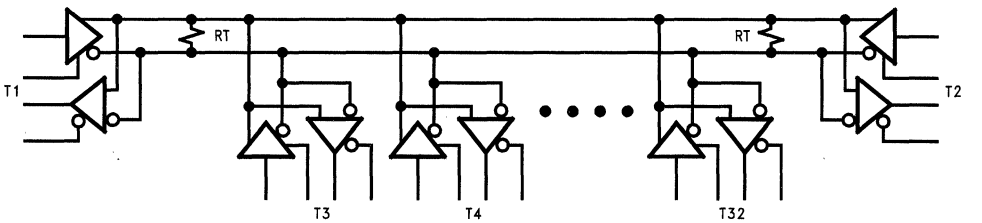

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FIGURE 4. Typical EIA-485 Multipoint Application

Calculating Power Dissipation for Differential Line Drivers

National Semiconductor
Application Note 805
Joe Vo

INTRODUCTION

In many board and system level designs, it is often necessary to determine the total power dissipated by the individual components of that application. This determination of total device power dissipation is important for two reasons. First, it can be used to select the power supply best suited to satisfy the needs of the application. And second, a power dissipation calculation facilitates the analysis of how the board or system's operating conditions might adversely affect the reliability of, or otherwise damage, the on board components.

The purpose of this application note is to provide end users with a sample power dissipation calculation for typical TIA/EIA-422 and TIA/EIA-485 differential line drivers. Other topics which will be addressed by this application note include worst case power dissipation, and packaging/thermal considerations.

CONTRIBUTIONS TO TOTAL DEVICE POWER DISSIPATION

Under normal operating conditions, the total device power dissipation is determined primarily by output load current and quiescent current. These current terms are modified by external loading conditions, device switching frequency, power supply voltage and ambient operating temperature. The following discussion of device power dissipation will take all these factors into consideration.

The power dissipated by a device in its quiescent state and that dissipated by the outputs when the device is switching constitute the primary contributions to total device power dissipation. Quiescent power dissipation is defined as the product of power supply voltage (V_{CC}) and power supply current (I_{CC}).

(1) $$PD_{QUIESCENT} = (V_{CC})(I_{CC})$$

The power dissipation by the outputs, takes into account the power dissipated by the output structures of the device when the outputs are driving a load. When the device output is in the LOW state, the output sinks a sufficient amount of load current to develop a V_{OL} with respect to ground. Conversely, when the device output is in the HIGH state, the output sources a load current sufficient to develop a V_{OH} with a respect to ground. The power dissipated, then, by a single channel is:

(2) $$PD_{OUTPUT} = I_{OH}(V_{CC} - V_{OH}) + I_{OL}(V_{OL})$$

where, I_{OH} = HIGH level output current
I_{OL} = LOW level output current

The general expression to describe the dissipated power for all outputs is:

(3) $$PD_{OUTPUTS} = (\#\text{ of channels})[I_{OH}(V_{CC} - V_{OH} + I_{OL}(V_{OL}))]$$

Together, the sum of quiescent power dissipation and power dissipation at the device outputs approximates the total power dissipated by the device.

(4) $$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$

A more comprehensive total device power dissipation calculation, however, might also incorporate the contribution to device power dissipation from the device's switching frequency. Therefore, Equation (4) could be changed to look like the following.

(5) $$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS} + C_{OUT}(V_{CC})^2(f)$$

where, C_{OUT} = device output capacitive load
f = device switching frequency

For this application note, the last term of Equation (5) was intentionally omitted. These are several reasons for this omission. First, switching frequency does not lend itself well to this general discussion of power dissipation since it varies from application to application. Second, in terms of the quiescent and output power dissipation components, the magnitude of the CV^2f term on total device power dissipation is negligibly small for most line drivers. And third, *Figure 1* demonstrates that switching frequency will not heavily impact quiescent device power dissipation (see Equation 1) since the magnitude of the change in I_{CC} due to switching frequency is small.

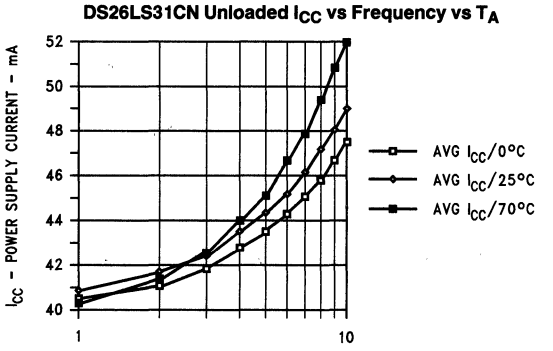

FIGURE 1. Supply Current vs Switching Frequency vs Temperature

TYPICAL POWER DISSIPATION CALCULATIONS USING THE DS26LS31CN

To better illustrate a total power dissipation calculation in a typical TIA/EIA-422 application, consider the DS26LS31CN (molded DIP package) Quad Differential Line Driver operating under following conditions:

V_{CC} = 5.0V
Ambient Operating Temperature = 25°C
Switching Frequency = 1 MHz
Duty Cycle = 50%
Measured V_{OH} = 3.2V
Measured V_{OL} = 0.3V
Termination Resistor = 100Ω

Figure 2 indicates that the I_{CC} typically associated with a V_{CC} of 5.0V, at room temperature, is approximately 39 mA. *Figure 1* indicated that a device, operating at room temperature, switching at 1 MHz will generate an I_{CC} of approximately 41 mA. Note in both *Figures 1* and *2* that the change in I_{CC} with respect to switching frequency and the change in I_{CC} with respect to V_{CC}, respectively, is rather small. Also note that in both figures there is little I_{CC} dependence on temperature.

For this typical calculation, 41 mA will be used for $I_{CCtypical}$ since it is a better representation of actual device operating conditions.

From (1), the static power dissipation is:

$$PD_{QUIESCENT} = (V_{CCtypical}\ (I_{CCtypical})$$
$$= (5.0V)\ (41.0\ mA)$$
$$= 205.0\ mW$$

Given that the measured V_{OH} is 3.2V, one can extract the corresponding I_{OH} from *Figure 3*. The I_{OH} required to develop a V_{OH} of 3.2V is approximately 30 mA.

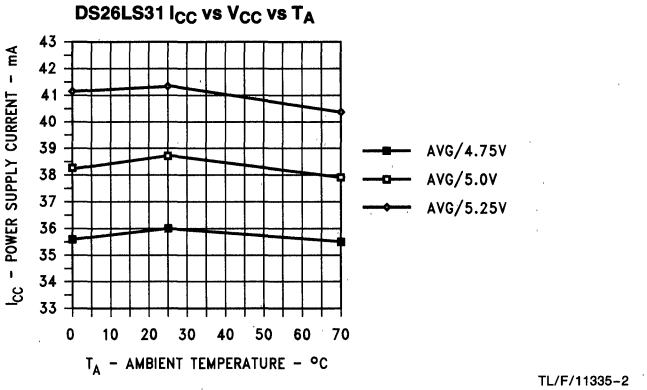

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FIGURE 2. Supply Current vs Supply Voltage vs Temperature

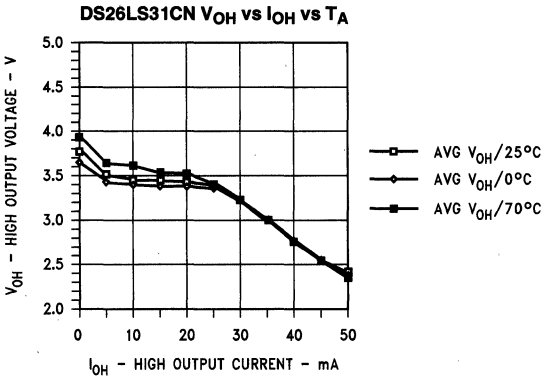

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FIGURE 3. High Output Voltage vs High Output Current vs Temperature

From *Figure 4*, one can likewise obtain an I_{OL} of approximately 30 mA given a measured V_{OL} of 0.3V.

The outputs, then, of the DS26LS31CN dissipate power according to the following relationship:

$$PD_{OUTPUTS} = (\#\text{ of Channels})\,[I_{OH}(V_{CC} - V_{OH}) + I_{OL}(V_{OL})]$$
$$= (4)\,[30\text{ mA}(5.0V - 3.2V) + 30\text{ mA}(0.3V)]$$
$$= (4)\,[54.0\text{ mW} + 0.9\text{ mW}]$$
$$= 252.0\text{ mW}$$

From the given typical operating conditions, the total power dissipated by the DS26LS31CN is:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 205.0\text{ mW} + 252.0\text{ mW}$$
$$= 457.0\text{ mW}$$

WORST CASE POWER DISSIPATION CALCULATIONS

While a typical power dissipation calculation is informative, a board or system level designer will invariably be forced to also perform a worst case calculation. With the exception of several minor changes, the same procedure is followed for both typical and worst case power dissipation calculations.

Starting with static power dissipation, this calculation must now use the maximum values for both power supply voltage (V_{CCmax}) and power supply current (I_{CCmax}). The I_{CCmax} used is normally that specified by the data sheet. However, if the application were to force the device beyond its 10 MHZ operating window, the I_{CCmax} could exceed the data sheet specifications of 60 mA (see *Figure 1*). In either case, the larger current value must be used for I_{CCmax} in the worst case quiescent power calculation.

The next step is to calculate the power dissipation from the device outputs. To do so, place the device under the worst case board or system conditions, and measure the resulting V_{OH} and V_{OL} levels. Given these worst case V_{OH} and V_{OL} values, one can extract the corresponding worst case I_{OH} and I_{OL} values with the help of *Figures 3* and *4*, respectively. A substitution of these values into Equation (3) will then yield the worst case power dissipation due to the device outputs.

An alternative method to calculate the power dissipated by the device outputs requires that a differential output voltage versus output current (V_{OD} vs I_O) curve be generated. Keeping in mind that $V_{OD} \equiv V_{OH} - V_{OL}$, a V_{OD} vs I_O curve can be developed by "subtracting" the V_{OL} vs I_{OL} curve from the V_{OH} vs I_{OH} curve. On the resulting V_{OD} vs I_O curve, draw a load line corresponding to the worst case loading conditions. This will then yield the output differential voltage and output currents being sourced and sunk by the device under a worst case loading condition. A substitution of these quantities into Equation (6) will yield the power being dissipated by the device outputs.

(6) $$PD_{DIFFERENTIAL\ OUTPUTS} = (\#\text{ of channels})\,[I_O(V_{CC} - V_{OD})]$$

As an example, consider the output voltage versus output current curves previously given for the DS26LS31CN (*Figures 3* and *4*). The V_{OD} vs I_O curve for the DS26LS31CN, as illustrated in *Figure 5*, can be drawn by "subtracting" *Figure 4* from *Figure 3*.

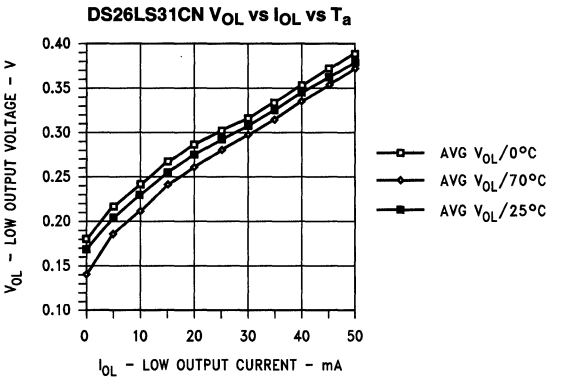

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FIGURE 4. Low Output Voltage vs Low Output Current vs Temperature

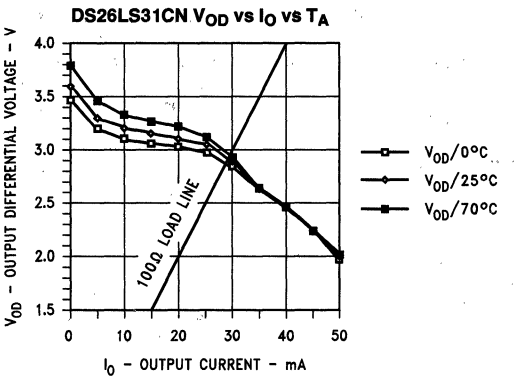

FIGURE 5. Output Differential Voltage vs Output Current vs Temperature

A sample worst case load line of 100Ω superimposed upon *Figure 5* reveals the corresponding worst case operating point for the DS26LS31CN; that is, it reveals the device's output differential voltage and output current given a sample worst case output load. When substituted into Equation (6), these voltage and current quantities will yield the worst case power dissipation at the device outputs.

The sum of the worst case quiescent and output power dissipation components will approximate the total worst case device power dissipation.

POWER CALCULATION FOR TIA/EIA-485 DIFFERENTIAL LINE DRIVERS

Let's first compare a typical TIA/EIA-422 output structure to a typical TIA/EIA-485 output structure. As shown in *Figure 6*, the presence of Schottky diodes in the output stage of an TIA/EIA-485 device clearly differentiates it from a similar TIA/EIA-422 device. The addition of the Schottky diodes to the TIA/EIA-485 output stage enable it to safely operate in multipoint (multiple driver) applications over a −7V to +12V common mode range versus the −250 mV to +6V common mode range of TIA/EIA-422. However, the Schottky diodes in the TIA/EIA-485 outputs have the net effect of raising the value of V_{OL} by one diode drop and decreasing the value of V_{OH} by the same amount. This change in output voltage levels will, in turn, affect the amount of power being dissipated in the output stage.

Despite the fact that the output structure of an TIA/EIA-422 line driver differs from that of the TIA/EIA-485 line driver, the procedure outlined earlier to calculate power dissipation is applicable for both TIA/EIA-422 devices and TIA/EIA-485 devices. Quiescent and output power dissipation calculations for an TIA/EIA-485 line driver will again employ Equations (1) and (3) respectively.

As with the sample power calculation for the TIA/EIA-422 device, the sum of the quiescent and output power components will yield the total approximated power dissipated by the TIA/EIA-485 device.

As an example, consider the worst case power dissipation of the DS96F172CJ (ceramic DIP package). Other than the fact that the DS96F172CJ is an TIA/EIA-485 device, it is pin for pin compatible with the DS26LS31CN. As outlined earlier, the first step is to calculate the quiescent power dissipa-

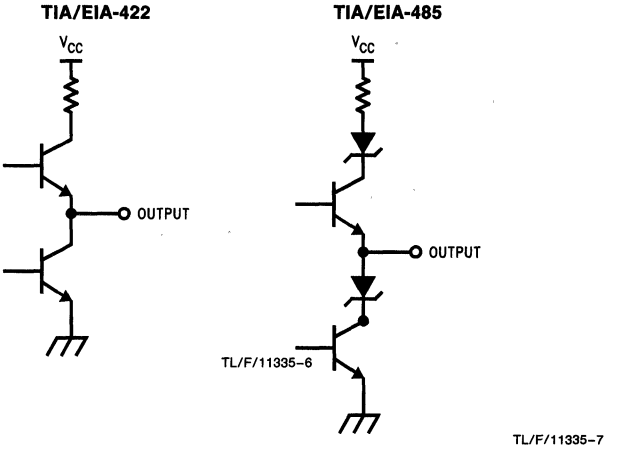

FIGURE 6. TIA/EIA-422 and TIA/EIA-485 Output Structures

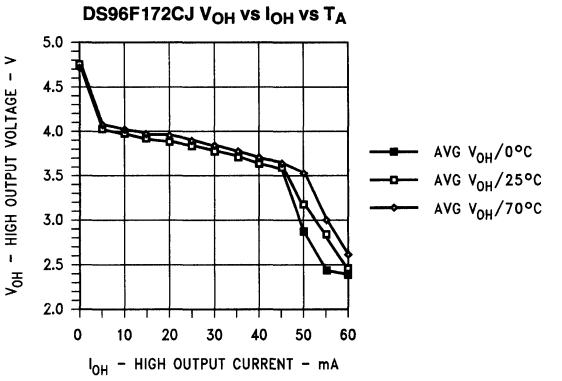

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FIGURE 7. High Output Voltage vs High Output Current vs Temperature

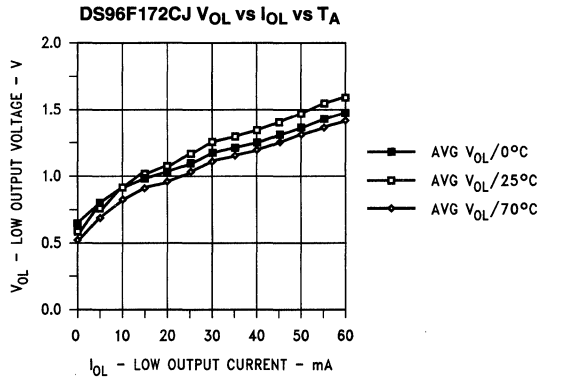

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FIGURE 8. Low Output Voltage vs Low Output Current vs Temperature

tion. From Equation (1), the worst case quiescent power dissipation is:

$$PD_{QUIESCENTmax} = (V_{CCmax})\ (I_{CCmax})$$
$$= (5.25V)\ (50\ mA)$$
$$= 262.5\ mW$$

The next step is to calculate the power dissipated at the device outputs under a worst case load condition. Again, there are two ways to do this. First, one can measure the worst case output voltage levels and reference them with *Figures 7* and *8* to extract the corresponding worst case output currents.

A substitution of these resulting quantities into Equation (3) will yield the power dissipated at the device outputs given a worst case load. The second method to calculate output power dissipation involves drawing a worst case load line on the differential output voltage versus output current curve. In the case of the DS96F172CJ, the worst case load line is assumed to be 60Ω. This assumption was made because in a typical TIA/EIA-485 application, both ends of the transmission line are terminated with 120Ω and so the TIA/EIA-485 driver is effectively loaded with 60Ω. In *Figure 9* a 60Ω load line has been superimposed upon the differential output versus output current curve and consequently, worst case values of output current and differential output voltage (under the given load) have been obtained.

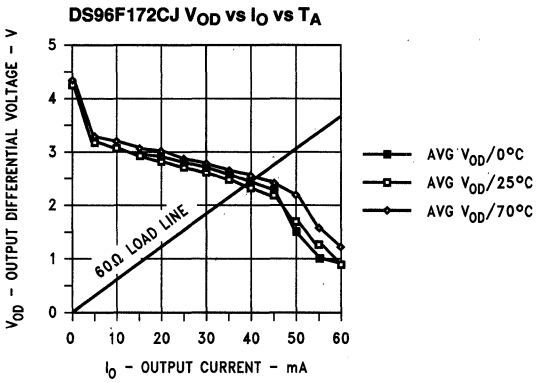

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FIGURE 9. Output Differential Voltage vs Output Current vs Temperature

At room temperature, the worst case power dissipation at the device outputs is (from Equation (6)):

$$PD_{DIFFERENTIAL\ OUTPUTS} = (\#\ of\ channels)\ [I_O\ (V_{CC} - V_{OD})]$$
$$= (4)\ [39\ mA\ (5.25V - 2.4V)]$$
$$= 444.6\ mW$$

The only remaining task is to sum together the quiescent and output power dissipation terms to obtain a total worst case power dissipation. From (4), the DS96F172CJ operating at room temperature, under a worst case load of 60Ω, will dissipate:

$$PD_{TOTAL} = PD_{QUIESCENT} + PD_{OUTPUTS}$$
$$= 262.5\ mW + 444.6\ mW$$
$$= 707.1\ mW$$

PACKAGING AND THERMAL CONSIDERATIONS

Having calculated the total power dissipated by the device, the next logical step is to ascertain that the power dissipated does not thermally damage the device. To do so, the following equation is used:

(7) $$T_J = [PD_{TOTAL}(\theta_{JA})] + T_A$$

where, θ_{JA} = Thermal Resistance from Junction to Ambient (°C/W)

PD_{TOTAL} = Total Power Dissipated by Device (W)

T_J = Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The only variable which remains unknown is θ_{JA}. θ_{JA} information for the available package types of most devices can be found in the respective device's data sheet. Keep in mind that the data sheet often refers to θ_{JA} in terms of derate factors. Determining θ_{JA} involves taking the inverse of the derate factor.

(8) $$\theta_{JA} = 1/\text{Derate Factor}$$

For example, all the information is now available for a sample calculation of the DS26LS31CN's junction temperature using the operating conditions specified earlier. The data sheet of the DS26LS31CN specifies a derate factor, for the plastic DIP package, of 11.9 mW/°C. From (8), the θ_{JA} is:

$$\theta_{JA} = 1/\text{Derate Factor}$$
$$= 1/(0.0119\ W/°C)$$
$$= 84.0\ °C/W$$

The thermal resistance from junction to ambient for the DS26LS31CN is now known. Also known are the ambient operating temperature and the total power dissipated (obtained earlier). From (7), the junction temperature is:

$$T_J = [(PD_{TOTAL})\ (\theta_{JA})] + T_A$$
$$= [(0.457W)\ (84.0°C/W)] + 25°C$$
$$= 63.4°C$$

The maximum allowable junction temperature for plastic DIP packages is 150°C. The junction temperature of the DS26LS31CN operating under the conditions specified earlier, by the typical power dissipation calculation, is well within the allowed maximum. Applications where the maximum

allowable junction temperature is exceeded should be avoided since this condition may thermally damage the device and package.

Looking at this thermal analysis from a slightly different perspective, Equation (7) can be rewritten as:

(9) $$PD_{PACKAGEmax} = (T_{Jmax} - T_A)/\theta_{JA}$$

By substituting 150°C for the maximum allowable junction temperature, the maximum allowable package power dissipation at 25°C can be calculated using the θ_{JA} for the DS26LS31CN plastic DIP (N) package.

$$PD_{PACKAGE_{max\ @\ 25°C}} = (T_{Jmax} - T_A)/\theta_{JA}$$
$$= (150°C - 25°C)/84.0°C/W$$
$$= 1.48W$$

To calculate the maximum allowable package power dissipation at 70°C, the 1.48W maximum at 25°C must be derated using the following procedure:

(10) $$PD_{PACKAGE_{max\ @\ 70°C}} = PD_{PACKAGE_{max\ @\ 25°C}} - (\text{Derate})\ (\Delta T_A)$$
$$= 1.48W - (0.0119W/°C)\ (45°C)$$
$$= 0.94W$$

This sample calculation illustrates that as ambient temperature increases, the DS26LS31CN is able to dissipate less power before the maximum allowable junction temperature specification is violated. Keep in mind that this thermal analysis also applies to TIA/EIA-485 devices such as the DS96F172CJ.

It should be noted that this general thermal analysis is applicable to all other packages and device types assuming that the maximum power dissipation and θ_{JA} are known.

SUMMARY

A method for calculating the total power dissipated by an TIA/EIA-422 driver was presented. This method is also applicable to similar devices conforming to the TIA/EIA-485 standard. Samples calculations for the DS26LS31CN and the DS96F172CJ were presented. Worst case considerations were also discussed. And finally, the relationship between power dissipation and thermal/packaging limitations was introduced.

SPECIAL NOTES

Figure 1: Ten samples from three data codes.

Figure 2: Ten samples from three data codes. Outputs unloaded and V_{CC} = 5.0V.

Figures 3, 4, 5: Ten samples from three date codes. V_{CC} = 5.0V

Figures 7, 8, 9: Ten samples from two date codes. V_{CC} = 5.0V

The graphical data referenced in this application note are not intended to guarantee performance as they only represent typical values.

REFERENCES

HC-CMOS Power Dissipation, K. Karakotsios, National Semiconductor, 1988 CMOS Logic Data Book, Application Note AN-303.

Understanding Integrated Circuit Package Power Capabilities, C. Carinalli and J. Huljev, National Semiconductor, 1990 Interface Data Book, Application Note AN-336.

Data Transmission Lines and Their Characteristics

National Semiconductor
Application Note 806
Kenneth M. True

OVERVIEW

This application note discusses the general characteristics of transmission lines and their derivations. Here, using a transmission line model, the important parameters of characteristics impedance and propagation delay are developed in terms of their physical and electrical parameters. This application note is a revised reprint of section two of the Fairchild Line Driver and Receiver Handbook. This application note, the first of a three part series (see AN-807 and AN-808), covers the following topics:

- Transmission Line Model
- Input Impedance of a Transmission Line
- Phase Shift and Propagation Velocity for the Transmission Line
- Summary—Characteristics Impedance and Propagation Delay

INTRODUCTION

A data transmission line is composed of two or more conductors transmitting electrical signals from one location to another. A parallel transmission line is shown in *Figure 1*. To show how the signals (voltages and currents) on the line relate to as yet undefined parameters, a transmission line model is needed.

TRANSMISSION LINE MODEL

Because the wires A and B could not be ideal conductors, they therefore must have some finite resistance. This resistance/conductivity is determined by length and cross-sectional area. Any line model, then, should possess some series resistance representing the finite conductivity of the wires. It is convenient to establish this resistance as a per-unit-length parameter.

Similarly, the insulating medium separating the two conductors could not be a perfect insulator because some small leakage current is always present. These currents and dielectric losses can be represented as a shunt conductance per unit length of line. To facilitate development of later equations, conductance is the chosen term instead of resistance.

If the voltage between conductors A and B *is not variable* with time, any voltage present indicates a static electric field between the conductors. From electrostatic theory it is known that the voltage V produced by a static electric field E is given by

$$V = \int E \bullet dl \tag{1}$$

This static electric field between the wires can only exist if there are free charges of equal and opposite polarity on both wires as described by Coulomb's law.

$$E = \frac{q}{4\pi\epsilon r^2} \tag{2}$$

where E is the electric field in volts per meter, q is the charge in Coulombs, ϵ is the dielectric constant, and r is the distance in meters. These free charges, accompanied by a voltage, represent a capacitance (C = q/V); so the line model must include a shunt capacitive component. Since total capacitance is dependent upon line length, it should be expressed in a capacitance per-unit-length value.

It is known that a current flow in the conductors induces a magnetic field or flux. This is determined by either Ampere's law

$$\int H \bullet dl = I \tag{3}$$

or the Biot-Savart law

$$dB = \frac{\mu I dl \times r}{4\pi r^3} \tag{4}$$

where r = radius vector (meters)
l = length vector (meters)
I = current (amps)
B = magnetic flux density (Webers per meter)
H = magnetic field (amps per meter)
μ = permeability

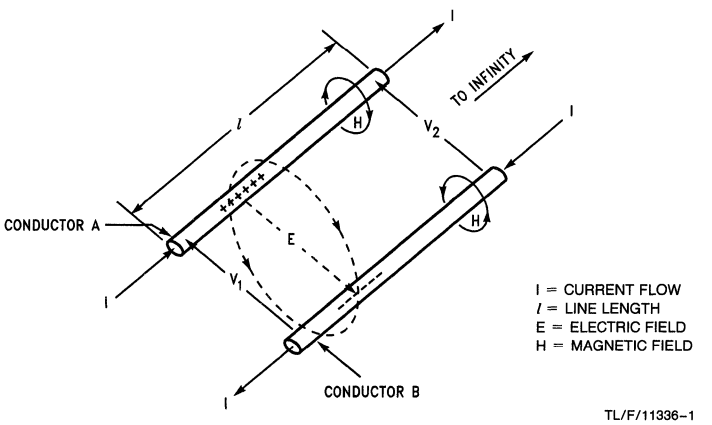

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FIGURE 1. Infinite Length Parallel Wire Transmission Line

If the magnetic flux (ϕ) linking the two wires *is variable* with time, then according to Faraday's law

$$V = \frac{d\phi}{dt} \quad (5)$$

A small line section can exhibit a voltage drop—in addition to a resistive drop—due to the changing magnetic flux (ϕ) within the section loop. This voltage drop is the result of an inductance given as

$$V = L\frac{di}{dt} \quad (6)$$

Therefore, the line model should include a series inductance per-unit-length term. In summary, it is determined that the model of a transmission line section can be represented by two series terms of resistance and inductance and two shunt terms of capacitance and conductance.

From a circuit analysis point of view, the terms can be considered in any order, since an *equivalent* circuit is being generated. *Figure 2* shows three possible arrangements of circuit elements.

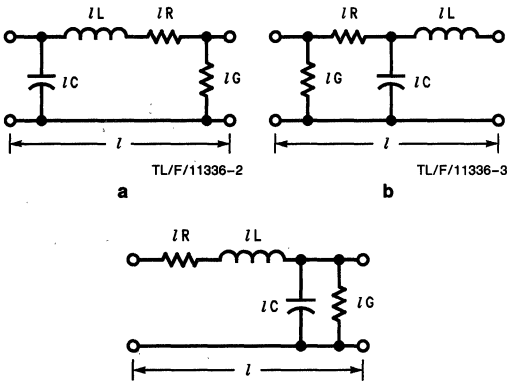


FIGURE 2. Circuit Elements

For consistency, the circuit shown in *Figure 2c* will be used throughout the remainder of this application note. *Figure 3* shows how a transmission line model is constructed by series connecting the short sections into a ladder network.

Before examining the pertinent properties of the model, some comments are necessary on applicability and limitations. A *real* transmission line does not consist of an infinite number of small lumped sections—rather, it is a distributed network. For the lumped model to accurately represent the transmission line (see *Figure 3*), the section length must be quite small in comparison with the shortest wavelengths (highest frequencies) to be used in analysis of the model. Within these limits, as differentials are taken, the section length will approach zero and the model should exhibit the same (or at least very similar) characteristics as the actual distributed parameter transmission line. The model in *Figure 3* does not include second order terms such as the increase in resistance due to skin effect or loss terms resulting from non-linear dielectrics. These terms and effects are discussed in the references rather than in this application note, since they tend to obscure the basic principles under consideration. For the present, assume that the signals applied to the line have their minimum wavelengths a great deal longer than the section length of the model and ignore the second order terms.

INPUT IMPEDANCE OF A TRANSMISSION LINE

The purpose of this section is to determine the input impedance of a transmission line; i.e., what amount of input current I_{IN} is needed to produce a given voltage V_{IN} across the line as a function of the LRCG parameters in the transmission line, (see *Figure 4*).

Combining the series terms lR and lL together simplifies calculation of the series impedance (Z_s) as follows

$$Z_s = l(R + j\omega L) \quad (7)$$

Likewise, combining lC and lG produces a parallel impedance Z_p represented by

$$Z_p = \frac{1}{Y_p} = \frac{1}{l(G + j\omega C)} \quad (8)$$

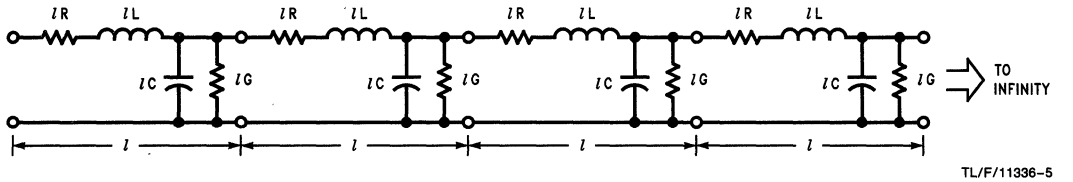


FIGURE 3. A Transmission Line Model Composed of Short, Series Connected Sections

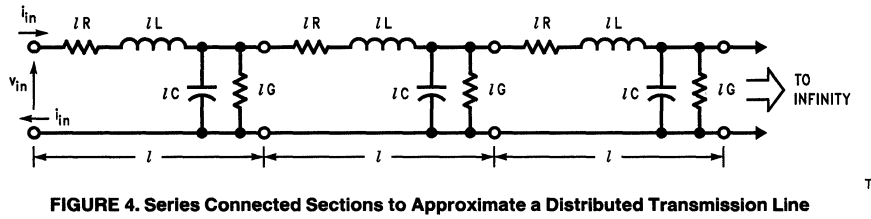


FIGURE 4. Series Connected Sections to Approximate a Distributed Transmission Line

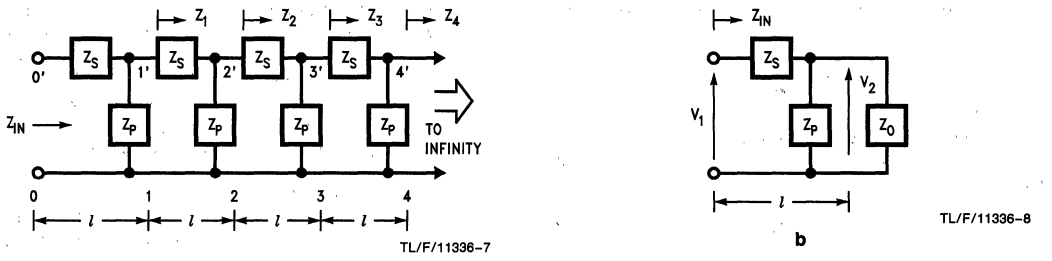


FIGURE 5. Cascaded Network to Model Transmission Line

Since it is assumed that the line model in *Figure 5a* is infinite in length, the impedance looking into any cross section should be equal, that is $Z_1 = Z_2 = Z_3$, etc. So *Figure 5a* can be simplified to the network in *Figure 5b* where Z_0 is the characteristic impedance of the line and Z_{in} must equal this impedance ($Z_{in} = Z_0$). From *Figure 5b*,

$$Z_{in} = Z_s + \frac{Z_0 Z_p}{Z_0 + Z_p} = Z_0 \tag{9}$$

Multiplying through both sides by $(Z_0 + Z_p)$ and collecting terms yields

$$Z_0^2 - Z_s Z_0 - Z_s Z_p = 0 \tag{10}$$

which may be solved by using the quadratic formula to give

$$Z_0 = \frac{Z_s \pm \sqrt{Z_s^2 + 4Z_s Z_p}}{2} \tag{11}$$

Substituting in the definition of Z_s and Z_p from Equations 7 and 8, Equation 11 now appears as

$$Z_0 = \frac{l(R + j\omega L)}{2} \pm \frac{1}{2}\sqrt{l^2 (R + j\omega L)^2 + 4\frac{R + j\omega L}{G + j\omega C}} \tag{12}$$

Now, as the section length is reduced, all the parameters (lR, lL, lG, and lC) decrease in the same proportion. This is because the per-unit-length line parameters R, L, G, and C are constants for a given line. By sufficiently reducing l, the terms in Equation 12 which contain l as multipliers will become negligible when compared to the last term

$$\frac{R + j\omega L}{G + j\omega C}$$

which remains constant during the reduction process. Thus Equation 12 can be rewritten as

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} = \sqrt{Z_s Z_p} \tag{13}$$

particularly when the section length l is taken to be very small. Similarly, if a high enough frequency is assumed,

$$\frac{\omega}{2\pi} > 100\ \text{kHz}$$

such that the ωL and ωC terms are much larger respectively than the R and G terms, $Z_s = j\omega lL$ and $Z_p = 1/j\omega l C$ can be used to arrive at a lossless line value of

$$Z_0 = \sqrt{\frac{L}{C}} \tag{14}$$

In the lower frequency range,

$$\frac{\omega}{2\pi} \cong 1\ \text{kHz}$$

the R and G terms dominate the impedance giving

$$Z_0 = \sqrt{\frac{R}{G}} \tag{15}$$

A typical twisted pair would show an impedance versus applied frequency curve similar to that shown in *Figure 6*. The Z_0 becomes constant above 100 kHz, since this is the region where the ωL and ωC terms dominate and Equation 13 reduces to Equation 14. This region above 100 kHz is of primary interest, since the frequency spectrum of the fast rise/fall time pulses sent over the transmission line have a fundamental frequency in the 1-to-50 MHz area with harmonics extending upward in frequency. The expressions for Z_0 in Equations 13, 14 and 15 do not contain any reference to line length, so using Equation 14 as the normal characteristic impedance expression, allows the line to be replaced with a resistor of $R_0 = Z_0\ \Omega$ neglecting any small reactance. This is true when calculating the initial voltage step produced on the line in response to an input current step, or an initial current step in response to an input voltage step.

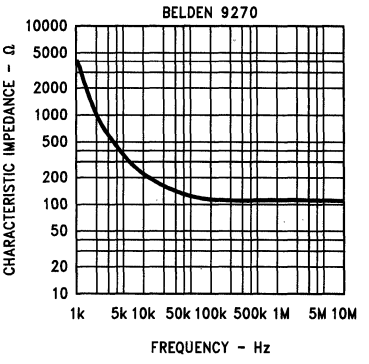


FIGURE 6. Characteristics Impedance versus Frequency

Figure 7 shows a 2V input step into a 96Ω transmission line (top trace) and the input current required for line lengths of 150, 300, 450, 1050, 2100, and 3750 feet, respectively (second set of traces). The lower traces show the output voltage waveform for the various line lengths. As can be seen, maximum input current is the same for all the different line lengths, and depends only upon the input voltage and the characteristic resistance of the line. Since $R_0 = 96\Omega$ and $V_{IN} = 2V$, then $I_{IN} = V_{IN}/R_0 \cong 20$ mA as shown by *Figure 7*.

A popular method for estimating the input current into a line in response to an input voltage is the formula

$$C(dv/dt) = i$$

where C is the total capacitance of the line (C = C per foot × length of line) and dv/dt is the slew rate of the input signal. If the 3750-foot line, with a characteristic capacitance per unit length of 16 pF/ft is used, the formula $C_{total} = (C \times l)$ would yield a total lumped capacitance of 0.06 μF. Using this C(dv/dt) = *i* formula with (dv/dt = 2V/10 ns) as in the scope photo would yield

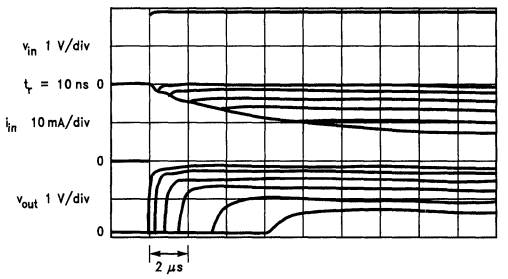
$$I = \frac{2V}{10\ ns} \times 0.06\ \mu F = 12A$$

This is clearly not the case! Actually, since the line impedance is approximately 100Ω, 20 mA are required to produce 2V across the line. If a signal with a rise time long enough to encompass the time delay of the line is used ($t_r \gg \tau$), then the C(dv/dt) = *i* formula will yield a resonable estimate of the peak input current required. In the example, if the dv/dt is 2V/20 μs ($t_r = 20\ \mu s > \tau = 6\ \mu s$), then $i = 2V/20\ \mu s \times 0.06\ \mu F = 6$ mA, which is verified by *Figure 8*.

Figure 8 shows that C(dv/dt) = *i* only when the rise time is greater than the time delay of the line ($t_r \gg \tau$). The maximum input current requirement will be with a fast rise time step, but the line is essentially resistive, so $V_{IN}/I_{IN} = R_0 = Z_0$ will give the actual drive current needed. These effects will be discussed later in Application Note 807.

PHASE SHIFT AND PROPAGATION VELOCITY FOR THE TRANSMISSION LINE

There will probably be some phase shift and loss of signal v_2 with respect to v_1 because of the reactive and resistive parts of Z_s and Z_p in the model (*Figure 5b*). Each small section of the line (*l*) will contribute to the total phase shift and amplitude reduction if a number of sections are cascaded as in *Figure 5a*. So, it is important to determine the phase shift and signal amplitude loss contributed by each section.



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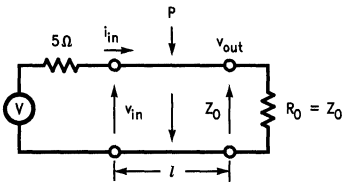

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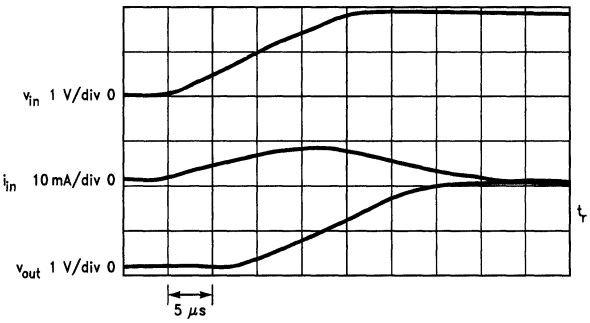
l = 150, 300, 450, 1050, 2100, 3750 ft.
24 AWG TWISTED PAIR $R_0 \cong 96\Omega$

FIGURE 7. Input Current Into a 96Ω Transmission Line for a 2V Input Step for Various Line Lengths



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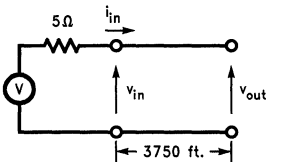

$t_r = 20\ \mu s$
$R_0 = 96\Omega$, $\delta = 1.6$ ns/ft.

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FIGURE 8. Input Current Into Line with Controlled Rise Time $t_r > 2\tau$

Using *Figure 5b*, v_2 can be expressed as

$$v_2 = v_1 \frac{Z_pZ_0}{Z_p + Z_0} \quad \frac{1}{Z_s + Z_p Z_0/(Z_p + Z_0)} \tag{16}$$

or

$$\frac{v_1}{v_2} = \frac{Z_s(Z_p + Z_0) + Z_pZ_0}{Z_pZ_0} \tag{17}$$

and further simplification yields

$$\frac{v_1}{v_2} = 1 + Z_s\left[\frac{1}{Z_0} + \frac{1}{Z_p}\right] \tag{18}$$

Remember that a per-unit-length constant, normally called γ is needed. This shows the reduction in amplitude and the change in the phase per unit length of the sections.

$$\gamma_l = \alpha_l = j\beta_l \tag{19}$$

Since

$$v_2 = v_1 {}^{-\gamma_l} = v_1 {}^{-\alpha_l} + v_1 {}^{-j\beta_l} \tag{20}$$

where $v_1 {}^{\alpha_l}$ is a signal attenuation and $v_1 {}^{-j\beta_l}$ is the change in phase from v_1 to v_2,

$$\ln\left[\frac{v_1}{v_2}\right] = \ln(\alpha_l + j\beta_l) = \alpha_l + j\beta_l = \gamma_l \tag{21}$$

Thus, taking the natural log of both sides of Equation 18

$$\ln\left[\frac{v_1}{v_2}\right] = \ln\left[1 + Z_s\left(\frac{1}{Z_0} + \frac{1}{Z_p}\right)\right] \tag{22}$$

Substituting Equation 13 for Z_0 and Y_p for $1/Z_p$

$$\gamma_l = \ln\left[1 + Z_s\left(\sqrt{\frac{Y_p}{Z_s}} + Y_p\right)\right] \tag{23}$$

Now when allowing the section length l to become small,

$$Y_p = l(G + j\omega C)$$

will be very small compared to the constant $\sqrt{Y_p/Z_s} = 1/Z_0$, since the expression for Z_0 does not contain a reference to the section length l. So Equation 23 can be rewritten as

$$\gamma_l = \ln\left(1 + Z_s\sqrt{\frac{Y_p}{Z_s}}\right) = \ln(1 + \sqrt{Y_pZ_s}) \tag{24}$$

By using the series expansion for the natural log:

$$\ln(1 + \zeta) = \zeta - \frac{\zeta^2}{2} + \frac{\zeta^3}{3} \ldots \text{ etc.} \tag{25}$$

$$\cong \zeta \text{ for small } \zeta$$

and keeping in mind the $\sqrt{Z_sY_p}$ value will be much less than one because the section length is allowed to become very small, the higher order expansion terms can be neglected, thereby reducing Equation 24 to

$$\gamma_l = \sqrt{Z_sY_p} = l\sqrt{(R + j\omega L)(G + j\omega C)} \tag{26}$$

If Equation 26 is divided by the section length,

$$\gamma = \frac{\gamma_l}{l} = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{27}$$

the propagation constant per unit length is obtained. If the resistive components R and G are further neglected by assuming the line is reasonably short, Equation 26 can be reduced to read

$$\gamma_l = j\beta_l = j\omega l\sqrt{LC} \tag{28}$$

Equation 28 shows that the lossless transmission line has one very important property: signals introduced on the line have a constant phase shift per unit length with no change in amplitude. This progressive phase shift along the line actually represents a wave traveling down the line with a velocity equal to the inverse of the phase shift per section. This velocity is

$$v = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}} \tag{29}$$

for lossless lines. Because the LRCG parameters of the line are independent of frequency except for those upper frequency constraints previously discussed, the signal velocity given by Equation 29 is also independent of signal frequency. In the practical world with long lines, there is in fact a frequency dependence of the signal velocity. This causes sharp edged pulses to become rounded and distorted. More on these long line effects will be discussed in Application Note 807.

SUMMARY—Characteristic Impedance and Propagation Delay

Every transmission line has a characteristic impedance Z_0, and both voltage and current at any point on the line are related by the formula

$$Z_0 = \frac{v}{i}$$

In terms of the per-unit-length parameters LRCG,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

Since $R \ll j\omega L$ and $G \ll j\omega C$ for most lines at frequencies above 100 kHz, the characteristic impedance is best approximated by the lossless line expression

$$Z_0 \cong \sqrt{\frac{L}{C}}$$

The propagation constant, γ, shows that signals exhibit an amplitude loss and phase shift with the latter actually a velocity of propagation of the signal down the line. For lossless lines, where the attenuation is zero, the phase shift per unit length is

$$\beta = \frac{\beta_l}{l} = \omega\sqrt{LC}$$

This really represents a signal traveling down the line with a velocity

$$\nu = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}$$

This velocity is independent of the applied frequency.

The larger the LC product of the line, the slower the signal will propagate down the line. A time delay per unit length can also be defined as the inverse of ν

$$\delta = \frac{1}{\nu} = \sqrt{LC} \tag{30}$$

and a total propagation delay for a line of length l as

$$\tau = l\delta = l\sqrt{LC} \tag{31}$$

For a more detailed discussion of characteristic impedances and propagation constants, the reader is referred to the references below.

REFERENCES

Hamsher, D.H. (editor); *Communications System Engineering Handbook;* Chapter 11, McGraw-Hill, New York, 1967.

Reference Data for Radio Engineers, fifth edition; Chapter 22; Howard T. Sams Co., New York, 1970.

Matrick, R.F.; *Transmission Lines for Digital and Communications Networks;* McGraw-Hill, New York, 1969.

Metzger, G. and Vabre, J.P.; *Transmission Lines with Pulse Excitation;* Academic Press, New York, 1969.

Reflections: Computations and Waveforms

National Semiconductor
Application Note 807
Kenneth M. True

OVERVIEW

In this application note, the logical progression from the ideal transmission line to the real world of the long transmission line with its attendant losses and problems is made; specifically, the methods to determine the practicality of a certain length of line at a given data rate is discussed. Transmission line effects on various data formats are examined as well as the effects of several types of sources (drivers) on signal quality. A practical means is given to measure signal quality for a given transmission line using readily available test equipment. This, in turn, leads to a chart that provides the designer a way to predict the feasibility of a proposed data-transmission circuit when twisted-pair cable is used. This application note is a revised reprint of section three of the Fairchild Line Driver and Receiver Handbook. This application note, the second of a three-part series (see AN-806 and AN-808), covers the following topics:

- The Initial Wave
- Cut Lines and a Matched Load
- Kirchoff's Laws and Line-Load Boundary Conditions
- Fundamental Principles
- Tabular Method for Reflections—The Lattice Diagram
- Limitations of the Lattice Diagram Method
- Reflection Effects for Voltage-Source Drivers
- Reflection Effects for Matched-Source Drivers
- Reflection Effects for Current-Source Drivers
- Summary—Which are the Advantageous Combinations?
- Effect of Source Rise Time on Waveforms

INTRODUCTION

In AN-806 it was determined that transmission lines have two important properties: one, a characteristic impedance relating instantaneous voltages and currents of waves traveling along the line and, two, a wave propagation velocity or time delay per unit length. In this chapter, both Z_0 and δ are used to compute the line voltages and currents at any point along the line and at any time after the line signal is applied. Also, concepts of reflections and reflection coefficients are explored along with calculating methods for voltages and currents.

THE INITIAL WAVE

Application Note AN-806 also showed that for most practical purposes, where fast rise and fall time signals are concerned, the characteristic impedance of the line actually behaves as a pure resistance ($R_0 = \sqrt{L/C}$).

Figure 1a shows a generator comprised of a voltage source (magnitude V), a source resistance of R_S ohms, and a switch closing at time t = 0 connected to a lossless, infinite length transmission line having a characteristic resistance, R_0. Because the relationship of V_{IN} to I_{IN} is known as $V_{IN} = R_0 I_{IN}$, the lossless transmission line can be replaced with a resistor as shown in *Figure 1b*. The loop equation is

$$I_{IN}(R_S + R_0) = V \quad (1)$$

Substituting V_{IN}/R_0 for I_{IN} and collecting terms shows

$$V_{IN} = V\left(\frac{R_0}{R_0 + R_S}\right) \quad (2)$$

This shows that both source and characteristic resistances act as voltage dividers for the source voltage V. *Figure 2* shows voltage and current steps for the various source resistances. Source resistances of less than R_0 produce initial voltage steps on the line which are greater than half the compliance of the source voltage, V. A matched source ($R_S = R_0$) produces voltage steps exactly half of V and source resistances greater than R_0 produce an initial voltage step less than one half V in magnitude. Generators can be classified into three categories:

- Voltage source types where $R_S < R_0$
- Matched source types where $R_S = R_0$
- Current source types where $R_S > R_0$

Waveforms of these types will be discussed more fully in AN-808 on long line effects. Suffice to say that initial voltage wave amplitude depends greatly on source resistance. Voltage source type drivers produce higher amplitude initial voltage waves in the line than either matched source or current source type drivers.

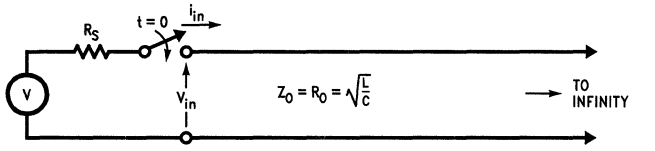

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FIGURE 1a. Generator Driving an Infinite Transmission Line

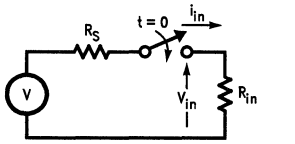

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FIGURE 1b. Thevenin Equivalent for Initial Wave

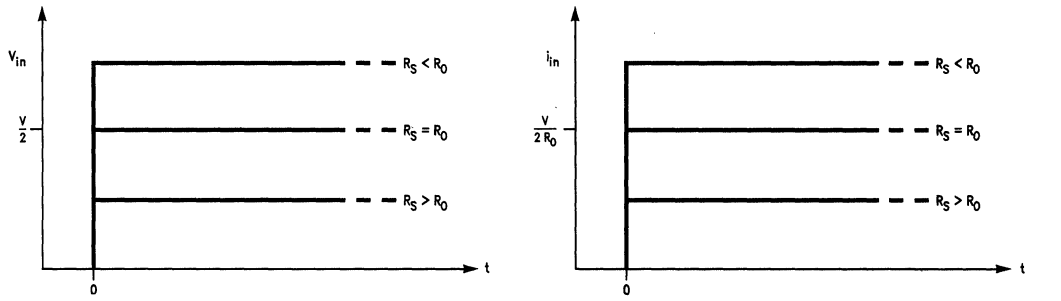

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FIGURE 2. Voltage/Current Steps for Three Source Resistances

CUT LINES AND A MATCHED LOAD

In examining an infinite, lossless line *(Figure 3)*, it is already known that the ratio of line voltage to current is equal to the characteristic resistance of that line. The line is lossless, and the same voltages and currents should appear at point x down the line after a time delay of $x\delta$. If the line at point x is cut, and a resistor of value R_0 is inserted, there would not be a difference between the cut, terminated finite line and the infinite line. The v_x and i_x waves see the same impedance (R_0) they were launched into at time $t = 0$, and indeed, the waves are absorbed into R_L ($= R_0$) after experiencing a time delay of $\tau = x\delta$. So, from an external viewpoint, an infinite-length lossless line behaves as a finite-length lossless line terminated in its characteristic resistance.

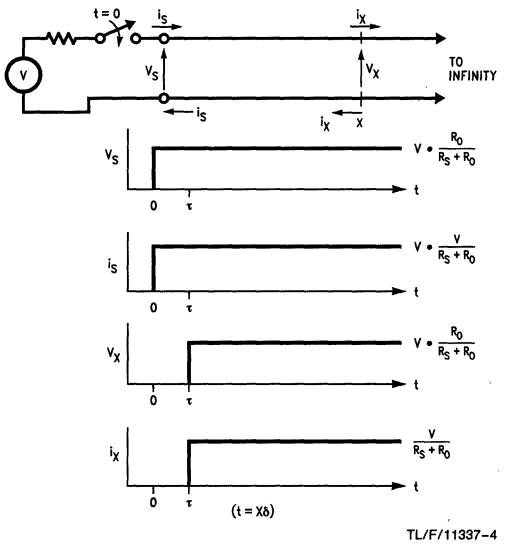

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FIGURE 3. Voltages and Current on an Infinite Length Line

KIRCHOFF's LAWS AND LINE-LOAD BOUNDARY CONDITIONS

The principle of energy conservation, widely known and accepted in the sciences, applies as well to transmission line theory; therefore, energy (as power) must be conserved at boundaries between line and load. This is expressed in an English language equation as follows.

$$\left[\begin{array}{c}\text{Power available at}\\ \text{the line end}\end{array}\right] = \left[\begin{array}{c}\text{Power absorbed}\\ \text{by the load}\end{array}\right] + \left[\begin{array}{c}\text{Power not absorbed}\\ \text{by the load}\end{array}\right]$$

Figure 4 shows power available at the line end is derived by the following formula. (This is assuming in-phase current and voltage.)

$$P_x = i_x \bullet v_x = \frac{v_x^2}{R_0} \quad (3)$$

The power *absorbed* by the load will be

$$P_L = v_L \bullet i_L = \frac{v_L^2}{R_L} \quad (4)$$

while power *not absorbed* by the load is represented by

$$P_r = v_r \bullet i_r = \frac{v_r^2}{R_0} \quad (5)$$

Here, the r subscript stands for reflected (not absorbed) power, voltage or current, respectively.

Applying Kirchoff's laws to point x in *Figure 4*, the current to the load is

$$i_L = i_x - i_r \quad (6)$$

and voltage across the load is

$$v_L = i_L R_L = v_x + v_r \quad (7)$$

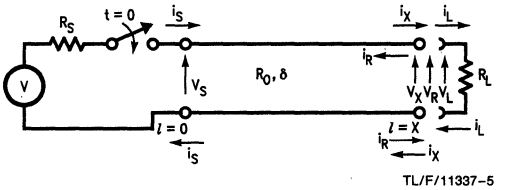

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FIGURE 4. Boundary Conditions at the Line/Load Interface

To find the ratio of v_r to v_x so that it can be ascertained how much power is absorbed by the load, and how much is not absorbed (therefore, reflected), substitute v_x/R_0 for i_x and v_r/R_0 for i_r into Equation 6.

$$i_L = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{8}$$

Rearranging Equation 7 and substituting for i_L in Equation 8 yields

$$\frac{v_x + v_r}{R_L} = \frac{v_x}{R_0} - \frac{v_r}{R_0} \tag{9}$$

The minus sign associated with v_r/R_0 means, in this case, that the reflected voltage wave v_r travels in the $-x$ direction toward the generator.

Collecting like terms of Equation 9 yields

$$v_x\left(\frac{1}{R_0} - \frac{1}{R_L}\right) = v_r\left(\frac{1}{R_0} - \frac{1}{R_L}\right) \tag{10}$$

So,

$$v_r = v_x \frac{\left(\frac{R_L - R_0}{R_0 R_L}\right)}{\left(\frac{R_L + R_0}{R_0 R_L}\right)} = v_x\left(\frac{R_L - R_0}{R_0 + R_L}\right) \tag{11}$$

and the desired relation for v_r/v_x is

$$\frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{12}$$

This ratio is defined as the voltage reflection coefficient of the load ρ_{VL}

$$\rho_{VL} \equiv \frac{v_r}{v_x} = \frac{R_L - R_0}{R_0 + R_L} \tag{13}$$

A similar derivation for currents shows

$$\rho_{IL} = -\frac{R_L - R_0}{R_L + R_0} = -\rho_{VL} \tag{14}$$

For the remainder of this application note and AN-808, the v or i subscript on the reflection coefficient is dropped, and ρ_L is assumed to be the *voltage* reflection coefficient of the load. Similarly, applying Kirchoff's laws to the source-line interface, the voltage reflection coefficient of the source is

$$\rho_S = \frac{R_S - R_0}{R_S + R_0} \tag{15}$$

The current reflection coefficient of the source has the same magnitude as ρ_S, but is opposite in algebraic sign.

When a traveling wave v_x, i_x meets a boundary such as the line load interface, a reflected wave is instantaneously generated so that Kirchoff's laws are satisfied at the boundary conditions. This is the direct result of the conservation of energy principle. Referring again to *Figure 4*, the effects of three different termination resistance R_L values are shown.

Case 1, $R_L = R_0$

In this case, R_L is equal to the characteristic resistance of the line. Using Equation 13, the voltage reflection coefficient of the load ρ_L is

$$\rho_L = \frac{R_0 - R_0}{R_0 + R_0} = \frac{0}{2R_0} = 0 \tag{16}$$

Since $v_r/v_x = \rho_L$, then $v_r = \rho_L v_x = 0$ and no reflection is generated. This agrees with the discussion of cut lines and matched load where a line terminated in its characteristic impedance behaves the same as an infinite line. All power delivered by the line is absorbed into the load. The waveforms appear as shown in *Figure 5*. The wave starting at the source at time $t = 0$ is reproduced at point x down the line after a time delay of $t = x\delta = \tau$.

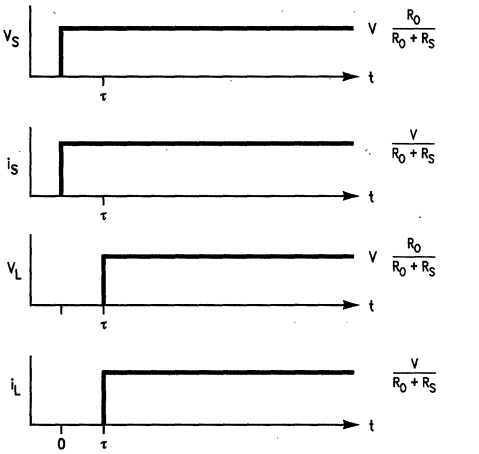

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FIGURE 5. Waveforms for $R_L = R_0$

Case 2, $R_L > R_0$

To simplify this case, assume that $R_S = R_0$. This means that the initial voltage is

$$V\frac{R_0}{R_0 + R_0} = \frac{V}{2} \tag{17}$$

Also assume $R_L = 3\ R_0$, then the load voltage reflection coefficient is

$$\rho_L = \frac{3R_0 - R_0}{3R_0 + R_0} = +\frac{1}{2} \tag{18}$$

The voltage wave arriving at point x at time $t = x\delta$ generates a reflected voltage wave of magnitude

$$v_r = \rho_L v_x = \left(+\frac{1}{2}\right)\left(\frac{V}{2}\right) = \frac{V}{4} \tag{19}$$

and the load voltage is

$$v_L = v_x + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{20}$$

The reflected voltage wave v_r generated at $t = x\delta = \tau$ travels back down the line toward the source arriving at the source at time $t = 2x\delta = 2\tau$. This wave will be absorbed without generating another reflection because R_S was picked to equal R_0, making ρ_S equal to zero. The source voltage is now

$$v_s + v_r = \frac{V}{2} + \frac{V}{4} = \frac{3V}{4} \tag{21}$$

and equilibrium is achieved.

If the circuit in *Figure 4* is analyzed using simple circuit theory and neglecting the transmission line effects, it is easily seen that

$$v_S = v_L = V\frac{R_L}{R_0 + R_L} = \frac{3V}{4} \tag{22}$$

This agrees exactly with Equation 21 and will always be the case. After all reflections cease and the circuit reaches equilibrium, the steady state voltages and currents on the line are the same as those produced using simple dc circuit analysis. Waveforms for $R_L > R_0$ (specifically $R_L = 3\ R_0$) appear in *Figure 6*.

In general, the case where $R_L > R_0$ is viewed in the following manner. Because the line is capable of delivering more power than can be instantaneously absorbed by the load, the excess power is returned to the source and absorbed in the source resistor (assuming $R_S = R_0$).

An upper limit on the voltage reflection coefficient is found by allowing R_L to go to infinity. In this case, Equation 13 goes to $+1$.

Case 3, $R_L < R_0$

In this case, again set $R_S = R_0$ and allow R_L to equal $R_0/3$. The initial wave, as before, is

$$v_S = V\frac{R_0}{R_0 + R_S} = \frac{V}{2} \tag{23}$$

and the load voltage reflection coefficient is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{\frac{R_0}{3} - R_0}{\frac{R_0}{3} + R_0} = -\frac{1}{2} \tag{24}$$

Therefore, the reflected voltage wave v_r is

$$v_r = \rho_L\frac{V}{2} = -\frac{V}{4} \tag{25}$$

which starts propagating back toward the source at time $t = \tau$. The load voltage at time $t = \tau$ is

$$v_x + v_r = \frac{V}{2} + -\frac{V}{4} = +\frac{V}{4} \tag{26}$$

The $(-V/4)$ reflected wave arrives back at the source at time $t = 2\tau$. Because R_S is set equal to R_0, ρ_S is, then, equal to zero and no reflected wave will be generated. The voltage at the source is now

$$v_S + v_r + \rho_S v_r = \frac{V}{2} + -\frac{V}{4} + 0 = \frac{V}{4} \tag{27}$$

From a dc circuit analysis, the steady state voltage is

$$V_{SS} = V\frac{R_L}{R_L + R_0} = \frac{V}{4} \tag{28}$$

This agrees with the result of Equation 27. The waveforms for Case 3 ($R_L < R_0$) appear in *Figure 7*.

An interpretation of the actions occurring when load resistance is less than the characteristic line resistance is as follows: when power available at the line end is less than the power the load can absorb, a signal is sent back to the source saying, in essence, "send more power".

It has been shown that a ratio of line and load resistance (ρ) can be used to calculate the voltages and currents in terms of a wave arriving at the boundary, possibly generating a reflected, reverse-traveling wave to satisfy the conservation of energy principle at the line-to-load boundary. This ratio is

$$\rho_B = \frac{R_B - R_0}{R_B + R_0} \tag{29}$$

where R_B represents the resistance into the boundary, R_B is R_S when considering the source-to-line interface and R_B would be R_L when considering the line-to-load interface. It is obvious that if discussing impedances, then Z_S would be substituted for R_S in Equation 29, and there may be some phase angle between the voltage and current waves.

The forward traveling wave, v_x, plus the reflected wave, v_r, is equal to the load voltage (V_L). Since v_r is ρ_L v_x, this can be expressed as

$$v_x(1 + \rho_L) = v_L \tag{30}$$

This quantity $(1 + \rho)$ can be defined as the voltage *transmission* coefficient of the load and it is known that

$$\frac{v_L}{v_x} = (1 + \rho_L) \tag{31}$$

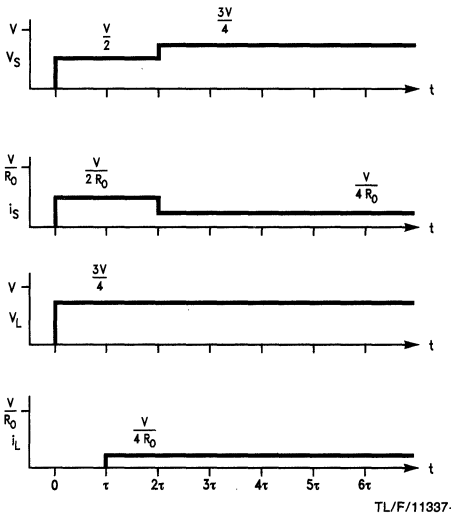

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FIGURE 6. $R_S = R_0$, $R_L = 3R_0$

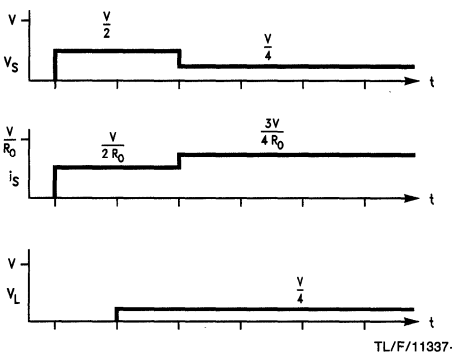

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FIGURE 7. $R_L = \frac{R_0}{3}$

The cases with various load resistances can be summarized.

	Condition		Circuit at time t = τ (one line delay time)
1.	$R_L = R_0$	$\rho_L = 0$	No reflection is produced—circuit reaches steady state immediately.
2.	$R_L > R_0$	$\rho_L > 0$	Positive voltage reflection—wave is sent back toward source. Voltage at load is higher than steady stage voltage (overshoot).
3.	$R_L < R_0$	$\rho_L < 0$	Negative voltage reflection—wave is sent back toward source. Voltage at load is lower than steady state voltage (undershoot).

FUNDAMENTAL PRINCIPLES

Before examining the algorithm for keeping track of reflections, there are two principles to keep in mind.

- Energy (as power) is conserved at boundary conditions (as explored previously)
- The principle of linear superposition applies. This means any arbitrary excitation function can be broken down into step functions, or ramps. The reaction of the circuit to each part can be analyzed, and the results can be added together when finished. This means that a positive pulse of duration t is examined by superimposing two step functions, one positive and one negative, starting after a delay of t *(Figure 8)*. It also means the voltage at any point on the line is the sum of initial voltage plus the sum of all voltage waves that have arrived at or passed through the point up to and including the time of examination. Also, the current on the line is, at any point, the sum of initial current plus any forward or reverse traveling currents passing the point up to and including the time the current is examined.

It has also been established that the steady state solution for voltages and currents on the line can be found by simple dc circuit analysis.

In examining reflection effects for the remainder of this application note, the following conventions are used.

A voltage or current wave traveling *toward* the point of interest will have the subscript "i" for *incident* wave,

A voltage or current wave traveling *away* from the point of interest will have the subscript "r" for *reflected* wave,

The subscript "S" means the parameter applied to the *source* (v_S for the voltage at the source, etc.), and

The subscript "L" means the parameter applied to the *load* (v_L for the voltage at the load, etc.)

Sign conventions for voltage waves and their associated currents are shown in *Figure 9.*

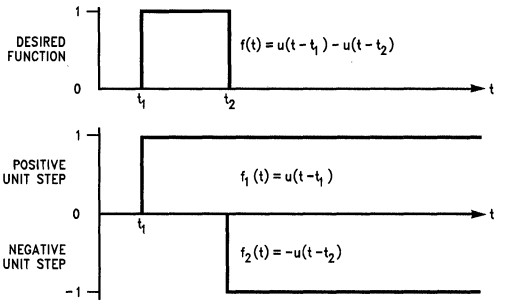

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FIGURE 8. Superposition of Simple Waveforms to Form More Complex Excitations

TABULAR METHOD FOR REFLECTIONS— THE LATTICE DIAGRAM

The waves going up and down the line can be monitored by drawing a time scale, as a vertical line with time increasing in the down direction, to represent the location on the line under examination. Because voltages at the source and load ends of the transmission line are normally of primary interest, two time scales are necessary. Drawing arrows from one time scale to the other as in *Figure 10* shows the direction of travel of the waves during a specific time interval. Since the main concern is only with the waveforms at the line ends, time scales are ruled off in multiples of the time delay of the line τ. If a unit-step type wave is launched from the source at time t = 0+, it is known that the magnitude of the wave will persist unchanged until a wave arrives back from the load after a round trip delay time of two line delays. The source time scale then is incremented in multiples of 2 mτ where m = 0, 1, 2, 3, . . . Likewise, the first wave arrives at the load after a single time delay, so the first increment ruling on the load time scale is τ, or one time delay of the line. Because the subsequent waves arrive back at the load in increments of 2τ, the load time scale is ruled off in multiples of (2m + 1)τ where m = 0, 1, 2, 3, . . . The operation of the lattice diagram is discussed using the example in *Figure 10b* which is the lattice diagram for the associated circuit.

time t = 0− (just before the switch closes)

The voltages at the source and load are equal with a magnitude of $v_{initial}$. Assume that no initial voltage is present. So, in this case, the voltage at the source and load equals zero.

$$V_{initial} = v_S(0-) = V_L(0-) = 0$$

time t = 0+ (just after the switch has closed)

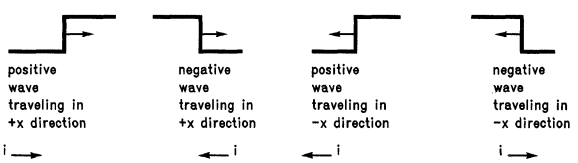

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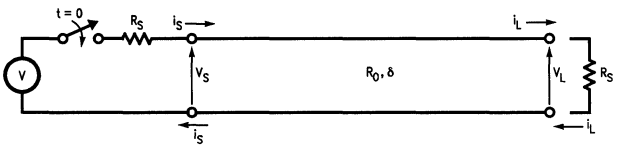
FIGURE 9. Sign Conventions for Waves



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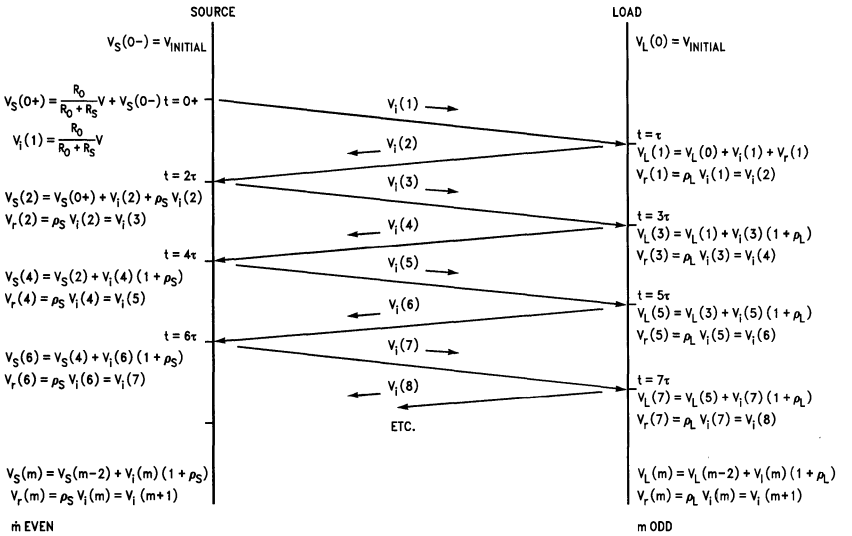
(a) Line Circuit to be Analyzed



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(b) Lattice Diagram

FIGURE 10. Reflection Bookkeeping with the Lattice Diagram

The first wave $v_i(1)$ is launched at the source and begins to travel toward the load end of the line. As previously mentioned, a voltage divider action between R_S and R_0 is used to derive the magnitude of the initial voltage wave.

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

At this time, the voltage at the source is the sum of the initial voltage plus the voltage wave $v_i(1)$ just generated.

$$v_S(0+) = v_S(0-) + v_i(1) = 0 + V\frac{R_0}{R_0 + R_S}$$

Because the switch closure represents a step function, the source voltage remains at this level until a wave returns after reflecting from the load at time $t = 2\tau$.

time $t = \tau$

The incident voltage wave $v_i(1)$ now arrives at the load and generates a reflected voltage wave

$$v_r(1) = \rho_L v_i(i);\ \rho_L = \frac{R_L - R_0}{R_L + R_0}$$

where ρ_L is the voltage reflection coefficient of the load. The reflected voltage wave $v_r(1)$ immediately starts traveling back toward the source becoming the incident voltage wave $v_i(2)$ which arrives back at the source at $t = 2\tau$. The voltage at the load is now the sum of the initial voltage plus the incident voltage wave $v_i(1)$ that just arrived plus the reflected voltage wave that is just departing.

$$\begin{aligned} v_L(1) &= v_L(0-) + v_i(1) + v_r(1) \\ &= 0 + v_i(1) + \rho_L v_i(1) \\ &= v_i(1)(1 + \rho_L) \end{aligned}$$

Again, because of the step function excitation, the load voltage remains unchanged until the new wave arrives at time $t = 3\tau$.

time $t = 2\tau$

$v_i(2)$ now arrives at the source and generates a reflected voltage wave $v_r(2)$ of magnitude

$$v_r(2) = \rho_S v_i(2);\ \rho_S = \frac{R_S - R_0}{R_S + R_0}$$

where ρ_S is the source voltage reflection coefficient.

The reflected voltage wave $v_r(2)$ starts back toward the load end of the line and becomes the incident voltage wave $v_i(3)$ arriving at the load at time $t = 3\tau$. The voltage at the source is now the sum of the voltage that was there plus the incident voltage wave just arrived plus the reflected voltage wave just departed for the load.

$$\begin{aligned} v_S(2) &= v_S(0+) + v_i(2) + v_r(2) \\ &= v\frac{R_0}{R_0 + R_S} + v_i(2) + \rho_S v_i(2) \\ &= v\frac{R_0}{R_0 + R_S} + v_i(2)(1 + \rho_S) \end{aligned}$$

time $t = 3\tau$

$v_i(3)$ arrives at the load generating $v_r(3)$

$$v_r(3) = \rho_L v_i(3)$$

$v_r(3)$ departs back toward the source becoming $v_i(4)$ to the source. The load voltage is now

$$v_L(3) = v_L(1) + v_i(3)\,(1 + \rho_L)$$

time $t = 4\tau$

When $v_i(4)$ arrives at the source and generates $v_r(4)$, then

$$v_r(4) = \rho_S v_i(4)$$

starts back toward the load to become $v_i(5)$ to the load. The load voltage is now

$$v_L(4) = v_L(2) + v_i(4)\,(1 + \rho_L)$$

This process can continue ad infinitum or until no measurable changes are detected. The reflection process at that time is considered complete and the line assumes a steady state condition. Steady state conditions can be found by applying simple dc circuit theory to source load circuits.

Summarizing this lattice diagram method, any time $t = m\tau$ and $m > 1$, the following relationships exist:

If m is odd, the $v_i(m)$ wave is arriving at the load and generates a reflected wave

$$v_r(m) = \rho_L v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the source. The voltage at the load at time $t = m\tau$ will be

$$v_L(m) = v_L(m - 2) + v_i(m)\,(1 + \rho_L)$$

This is the sum of the voltage that was there before the wave arrived, i.e., $v_L(m - 2)$, plus the wave arriving $v_i(m)$ and the reflected wave $v_r(m)$ departing.

If m is even, the $v_i(m)$ wave is arriving at the source and generates a reflected wave

$$v_r(m) = \rho_S v_i(m)$$

This becomes $v_i(m + 1)$ as it starts toward the load. The voltage at the source is now

$$v_S(m) = v_S(m - 2) + v_i(m)\,(1 + \rho_S)$$

This is the sum of the voltage that was present $v_S(m - 2)$ plus the incident wave arriving $v_i(m)$ plus the reflected wave departing $v_r(m)$.

The voltage and current at the source end of the line for a lossless line can be expressed as a summation.

$$v_S(t) = \frac{R_0}{R_S + R_0} \bullet \tag{32}$$

$$\left[e(t)u(t) + (1 + \frac{1}{\rho_S}) \sum_{n=1}^{\infty} \rho_S{}^n \rho_L{}^n e(t - 2n\tau)u(t - 2n\tau)\right]$$

$$i_S(t) = \frac{1}{R_S + R_0} \bullet \tag{33}$$

$$\left[e(t)u(t) + (1 - \frac{1}{\rho_S}) \sum_{n=1}^{\infty} \rho_S{}^n \rho_L{}^n e(t - 2n\tau)u(t - 2n\tau)\right]$$

where e(t) is the generator voltage as a function of time, and u(t) is the unit step function.

Likewise, the load voltage and load current for the lossless line can be expressed as a summation.

$$v_L(t) = \frac{R_0}{R_S + R_0} \bullet \tag{34}$$

$$(1 + \rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n \rho_L{}^n e(t-(2n + 1)\tau)u(t-(2n + 1)\tau)\right]$$

$$i_L(t) = \frac{1}{R_S + R_0} \bullet \tag{35}$$

$$(1 - \rho_L)\left[\sum_{n=0}^{\infty} \rho_S{}^n \rho_L{}^n e(t-(2n + 1)\tau)u(t-(2n + 1)\tau)\right]$$

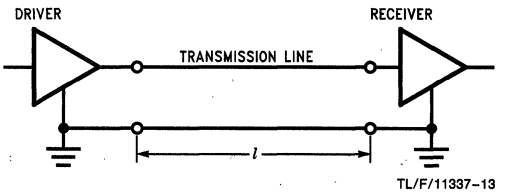
A similar expression of summation can be developed for the voltage (or current) at any point along the line at any time.

Because the lattice diagram is tabular in method, a computer program can be written relieving the designer of bookkeeping and repetitive calculations. A BASIC computer program for lattice diagrams appears in *Figure 13*.

LIMITATIONS OF THE LATTICE DIAGRAM METHOD

Before using the lattice diagram to explore reflection effects with various source and load characteristics, it is necessary to pause at this point and examine the models used by the lattice diagram.

First, both the line driver and receiver are simulated either by a constant input or output resistance. The source has two voltage sources and a switch representing the internal source voltage at a time less than zero and equal to (or greater than) zero. The receiver is represented by a single resistor shunting the line end opposite the driver site. The line itself is represented by its characteristic resistance R_0 and its total one-way time delay (τ). This is equal to length times propagation delay per unit length. This model is shown in *Figure 11*.



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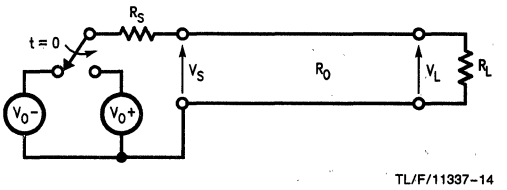

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FIGURE 11. Model Used for Lattice Diagram Method

Because most data communication circuits are voltage types, that is, the receiver senses the line voltage to decide if a logic One or logic Zero is present, the primary interest is in voltages at the source and load as a function of time. Major exceptions include the current loops used in teletypewriters, telegraphs, and burglar alarm systems. The majority of data communications circuits used in computers, peripherals, and general controllers are voltage types.

The lattice diagram method cannot easily use source or receiver current/voltage relationships that are non-linear; i.e., not purely resistive. For non-linear current/voltage characteristics such as found in diodes, a graphic method can be used called the reflection diagram or the Bergeron method.

Note: A French hydraulic engineer, L.J.B. Bergeron developed the method to study the propagation of water hammer effects in hydraulics. See references, AN-806.

Signals exchanged using lattice diagrams are of the unit step variety. When ramps or more complex waves are exchanged, the complexity of the bookkeeping increases dramatically. Additionally, the lines are presumed to be lossless, although a constant line attenuation factor could be accommodated without excessive bookkeeping. These limitations should be kept in mind when examining various source and load resistance combinations and their reflection characteristics.

There are three classes of source resistance, $R_S < R_0$, $R_S = R_0$ and $R_S > R_0$. There are also three classes of load resistance, $R_L < R_0$, $R_L = R_0$ and $R_L > R_0$. This gives nine types of single driver, single receiver line circuits. Each circuit will be examined in turn to determine reflection effects for these combinations with evaluations of each combination for voltage type communications.

REFLECTION EFFECTS FOR VOLTAGE SOURCE DRIVERS

Initial waves launched by a voltage source type driver ($R_S < R_0$) are greater than one-half the magnitude of the internal voltage source. Referring to *Figure 11*, the initial voltage wave is derived as follows.

$$v_i(1) = (V_{0+} - V_{0-}) \bullet \frac{R_0}{R_0 + R_S} \qquad (36)$$

while the voltage at the source at $t = 0+$ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \qquad (37)$$

If the receiver switching point is at the mean of the driver voltage swing, the initial wave always has sufficient magnitude to indicate the correct logic state as it passes the receiver site. This maximizes the noise margins of the receiver.

Since $R_S < R_0$, the source voltage reflection coefficient ρ_S is less than zero. Any voltage waves, then, arriving back at the source are changed in sign, reduced in amplitude (assuming $R_S > 0\Omega$), and sent back toward the load. If the load resistance equals the characteristic line resistance ($R_L = R_0$), the voltage reflection coefficient of the load is

$$\rho_L = \frac{R_L - R_0}{R_L + R_0} = \frac{0}{2R_0} = 0$$

No reflections, therefore, are generated at the load. The voltage wave produced at the source is reproduced at the load after a time delay of $\tau = \ell\,\delta$, and the line assumes a steady state condition. *Figure 12b* illustrates the source and load voltage waveforms for this case.

If R_L is greater than R_0, ρ_L is positive. Waves arriving at the load generate the same polarity reflections as the arriving waves. ρ_S and ρ_L are of opposite signs, so a dampened oscillatory behavior of the load voltage is expected. The oscillation period or *ringing* is 4τ. The overshoot of v_L from $t = \tau$ to 3τ may cause breakdown of the input circuitry of a receiver, depending on the receiver voltage rating. The undershoot at $t = 3\tau$ or 5τ can reduce the noise immunity of a receiver or even cause a logic level misinterpretation—an error in the data. These waveforms are shown in *Figure 12a*.

If R_L is less than R_0, then ρ_L is negative and a wave arriving at the load generates a reflection opposite in polarity to the incident wave. This causes the voltage at the source to overshoot steady state voltage at $t = 0$. Each reflection returning from the load causes the source voltage to continually step down toward the steady state voltage V_{SS}. These steps last for 2τ, or one round trip delay. Load voltage starts an increasing step-up waveform towards V_{SS} at time $t = \tau$, with steps again taking one round trip delay, 2τ. A line receiver placed in the middle of the line sees an entirely different waveform—dampened oscillations much like the load voltage in *Figure 12a*. This is caused by the negative signs of both source and load voltage reflection coefficients. Each time an incident wave arrives at either source or load, the reflected wave generated at that time has a sign opposite to the sign of the incident voltage wave. The voltage at a distance half way down the line is composed of these forward and reverse traveling waves arriving at that point commencing at time $t = 0.5\tau$, and with each new wave passing that point after one line delay (τ). These waveforms are shown in *Figure 12c*.

The optimum load resistance for voltage signal communications on transmission lines driven by a low impedance source ($R_S < R_0$) is equal to the characteristic line resistance. Large signal line voltages are produced and there are no reflection effects complicating the waveforms *(Figure 12b)*.

However, a matched load ($R_L = R_0$) is a dc load on the driver, thus it increases system power dissipation. But, it does preserve signal fidelity and amplitude allowing use of multiple bridging receivers ($R_{in} \gg R_0$) along the line.

The unterminated case ($R_L > R_0$) reduces dc driver loading and also reduces system power dissipation over the matched load case. The unterminated case does, however, allow the load signal to exhibit pronounced overshoot and undershoot around the steady state voltage. If the load signal undershoot places the receiver in its threshold uncertainty region, data errors result. There is a way to "civilize" the voltage waveform of the unterminated line load by trading off signal rise time versus line time delay. This is discussed later.

The final case of $R_S < R_0$ and $R_L < R_0$ is not generally useful in terms of voltage signals produced *(Figure 12c)*. Systems using this case consume more power than the previous two cases and have no particular advantage for voltage mode communications.

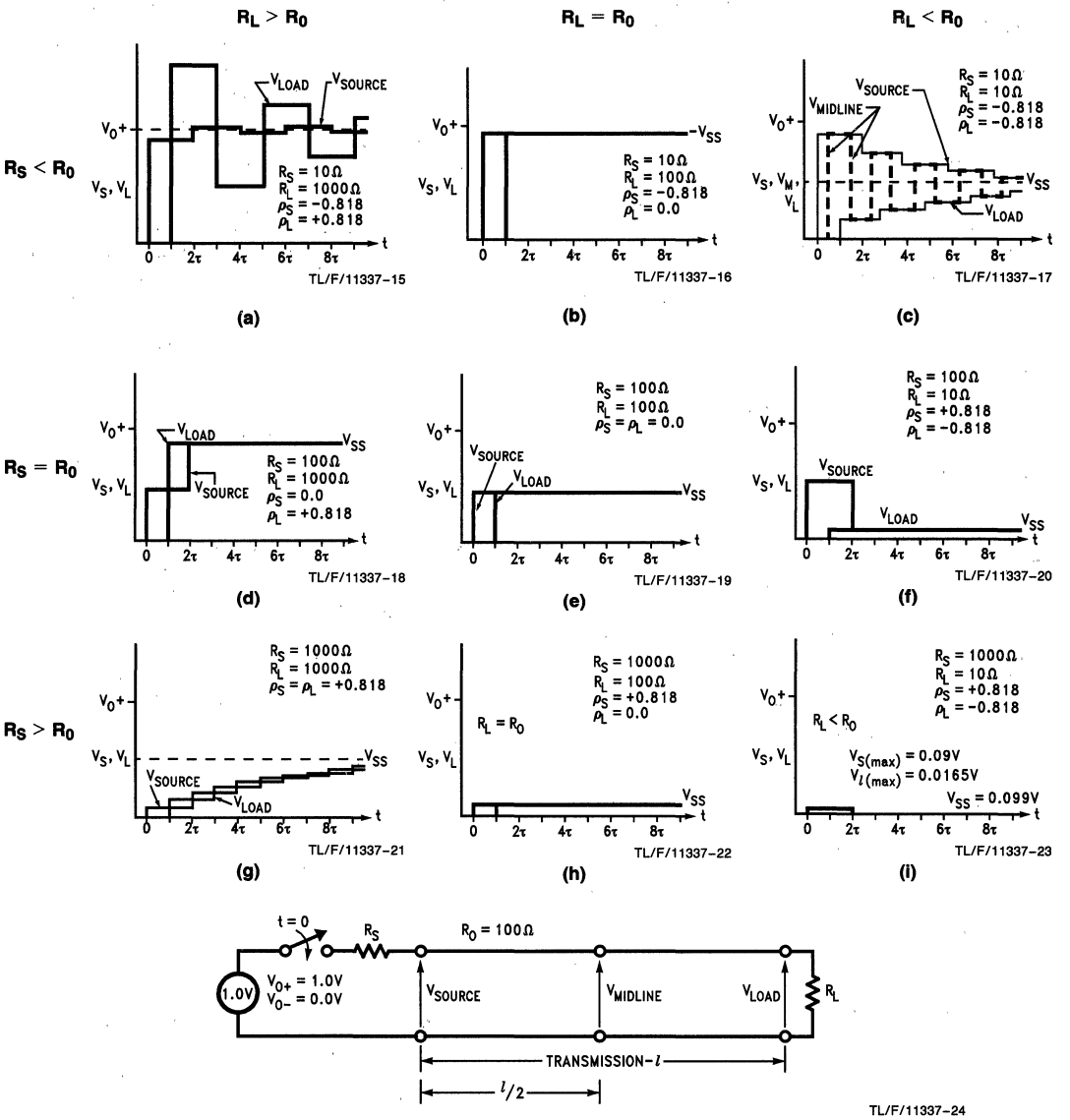


FIGURE 12. Source and Load Voltage Waveforms for Various R_S and R_L

REFLECTION EFFECTS FOR MATCHED-SOURCE DRIVERS

In all three cases under discussion here, the initial voltage produced by the driver onto the line is

$$v_i(1) = (V_{0+} - V_{0-})\frac{R_0}{R_0 + R_S} = \frac{1}{2}(V_{0+} + V_{0-}) \quad (38)$$

since $R_S = R_0$. The voltage at the source at time $t = 0+$ is

$$v_S(0+) = v_S(0-) + v_i(1) = V_{0-} \bullet \frac{R_L}{R_L + R_S} + v_i(1) \quad (39)$$

Assume, for clarity, that initial voltage (V_{0-}) is zero, thus Equation 39 simplifies to

$$v_S(0+) = \frac{V_{0+}}{2} \quad (40)$$

Since $R_S = R_0$, ρ_S is equal to zero. This means that load-generated reflections due to load mismatch are absorbed at the source when, at time $t = 2\tau$, the reflected wave arrives back at the source. The line then assumes a steady state throughout. This back match or series termination effect of a matched source allows a wide latitude in choice of load resistance without sacrificing the signal fidelity of the load voltage waveform.

If the load resistance equals the characteristic line resistance $R_L = R_0$, then ρ_L equals zero and no load site reflections are generated. The initial voltage wave arrives at the load at time $t = \tau$ (one line delay) and voltages (and currents) on the line immediately assume steady state conditions (see *Figure 12e*). The optimum receiver threshold here is one-half the steady state voltage or $V_{0+}/4$. The main advantage over the voltage source type driver with matched load case ($R_S < R_0$, $R_L = R_0$) is that R_S and R_L resistance tolerances may be relaxed without incurring much signal *ringing*. This effect is due primarily to the termination provided by both line ends, rather than just one line end. Any reflected voltage wave on either system is attenuated by the product of ρ_S and ρ_L for each round trip line delay time. Since the $\rho_S\rho_L$ product for the fully matched case is smaller than the $\rho_S\rho_L$ product for the single matched case, the reflections are attenuated and die out in fewer round trips. For example, if 20% tolerance resistors are used in both cases, ρ_S and ρ_L values for the fully matched case become 0.0 ± 0.0909, which is a $\rho_S\rho_L$ product of ± 0.0033. This means that after one round trip (2τ), the reflection amplitude starting back toward the load would be less than 0.33% of the initial wave.

Using $R_S = 10\Omega$, $R_L = 100\Omega$, and $R_0 = 100\Omega$ as for *Figure 12a*, shows the same 20% tolerances applied to the single matched case

$$-0.8519 \le \rho_S \le -0.7857$$
$$-0.0909 \le \rho_L \le +0.0909$$

and

$$|\rho_S\rho_L| \le 0.0774$$

The voltage reflection amplitude after one round trip is a maximum of 7.7% of the initial wave.

The choice between using the single and fully matched system should be carefully considered because the fully matched system does sacrifice signal voltage magnitude to get a decreased dependence on absolute resistor values.

If the load resistance for a matched driver circuit is made much greater than the line resistance, the initial wave arriving at the load at time $t = \tau$ will be almost double since ρ_L will be close to $+1.0$. Because source resistance is set equal to line resistance, ρ_S becomes zero, the reflected voltage wave from the load is absorbed by the source at time $t = 2\tau$, and steady state conditions prevail. Waveforms for this case are shown in *Figure 12d*. This is called *back matching* or *series termination*.

The main advantage of series termination is a great reduction in steady state power consumption when compared with the parallel terminated case ($R_S \ll R_0$, $R_L = R_0$). At the same time, series termination provides the same signal fidelity to a receiver placed at the line end. Compare the load voltage waveforms for the two cases in *Figure 12b* and *12d*. The main disadvantage to series termination is that receivers placed along the line see a waveform similar to that shown for the source in *Figure 12d*. That is, receivers along the line see the $V_{0+}/2$ initial wave as it passes that point on the line, and do not see a full signal swing until the load end reflection passes that point. Consequently, receivers along the line do not see a signal sufficient to produce the valid logic state output until the load reflection returns. Depending on actual line length and receiver characteristics, the receiver may even oscillate, having been placed in its linear operation region. With the benefit, then, of reducing system power, the series termination method has a constraint of allowing only one line receiver located at the line load end. The parallel termination method should be used if other receivers along the line are required.

The final case of matched source drivers is with the use of a load resistance less than the characteristic line resistance. The waveforms for this case are shown in *Figure 12f*. A line receiver with a threshold of $V_0/4$ placed at the source responds like a positive, edge triggered one-shot and produces a pulse in response to a $+V/2$ initial wave of 2τ duration. Aside from its use as a one-shot, this circuit doesn't seem to offer any advantages for voltage mode communications.

REFLECTION EFFECTS FOR CURRENT-SOURCE DRIVERS

The name *current source drivers* is somewhat of a misnomer, and might be more properly called *current-limited voltage source drivers*. True *current source* drivers such as the DS75110A are normally used in conjunction with parallel termination resistors to create a matched source.

The *current source* drivers ($R_S > R_0$) discussed resemble true current sources in the respect that their output resistance is usually much greater than the characteristic line resistance. The initial voltage step produced on the line is thus usually small $v_i(1) = (i_S(1)R_0)$. This is due to the voltage divider action of the driver source resistance and the characteristic line resistance.

Voltage waveforms for a current source type driver either step up to V_{SS}, reach steady state after 2τ, or execute a dampened oscillation around V_{SS}, depending on whether the load resistance R_L is greater, equal, or less than R_0, respectively. The second case $R_L = R_0$ provides signals much the same as the other two cases where $R_L = R_0$, that is, the source voltage steps immediately to V_{SS}, with the load voltage following after one line time delay. Here the amplitude of the signal is much smaller than previous matched load cases. Since the current source type drivers (DS75110A) have high off-state impedances, they allow multiple drivers on the line to produce data bus or party line. Waveforms for the matched load case are shown in *Figure 12h*.

The case $R_L < R_0$ really provides no useful advantage for voltage mode communications. The negative sign for ρ_L and the positive sign for ρ_S lead to dampened oscillatory behavior, or ringing. The maximum perturbation takes place at the source end of the line. Waveforms for this case are similar to those shown in *Figure 12a*, and are shown to scale in *Figure 12i*. With the given values used to produce the figure, the maximum amplitude ringing appears at the source line end.

The $R_L > R_0$ case is of interest because it is representative of DTL driving a transmission line with the output going from LOW to HIGH. DTL has a high value R_S, (2 kΩ or 6 kΩ) in the HIGH logic state. Since both R_S and R_L are greater than R_0, both ρ_S and ρ_L are positive. A small voltage step starts from the source at $t = 0+$; its magnitude is

$$v_i(1) = V\frac{R_0}{R_0 + R_S}$$

Note: Since the input diode is not represented, the representation of DTL input as a single resistor to ground is not strictly correct. For purposes of approximation, this simple representation is used. Treatment of non-linear current/voltage sources and loads is covered by Metzger & Vabre. (op. cit.)

Upon arrival at the load at time $t = \tau$, this initial wave generates a positive voltage reflection since $\rho_L > 0$. The voltage reflection arrives back at the source site at time $t = 2\tau$. Since ρ_S is also positive, another positive voltage reflection is launched back toward the load. The process repeats, and the source and load voltages both execute a step-up approach toward steady state voltage V_{SS}. These waveforms are shown in *Figure 12g*.

In examining voltage at the line midpoint ($x = \ell/2$), a step-up type waveform is seen which is the sum of all the incident voltage waves passing the line midpoint up to the time of examination. The midpoint voltage is expressed as follows.

$$v_m(t) = V_{SS}\,(1 - \exp[-(t + 0.5\tau)/T]) \qquad (41)$$

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref. 2, AN-806) can be used.

for $t = n + 0.5\tau$ with $n = 0, 1, 2, 3$, etc. V_{SS} in Equation 41 is the steady state line voltage

$$V_{SS} = V_{0+} \bullet \frac{R_L}{R_S + R_L}$$

and T is a time constant given by

$$T = -\frac{2\tau}{\ell\, n(\rho_S \rho_L)} \qquad (42)$$

with τ being one line delay ($\tau = \ell\,\delta$).

Note: This equation is presented without derivation, but a procedure similar to that used by Matick (Ref. 2, AN-806) can be used.

Equation 41 provides an exact solution for odd multiples of n ($n = 1, 3, 5 \ldots$, so $t = 1.5\tau, 3.5\tau, 5.5\tau \ldots$), while it approximates $v_m(t)$ for even multiples of n ($n = 0, 2, 4 \ldots$, so $t = 0.5\tau, 2.5\tau, 4.5\tau \ldots$). The closer the $\rho_S\rho_L$ product is to 1, the better Equation 41 predicts $v_m(t)$, particularly for even multiples of n. To illustrate the fitting, the two tables in *Figure 13* are generated by the BASIC language computer program (Table C) and their data is plotted in *Figure 14*.

Designers familiar with DTL circuits should quickly recognize that the waveforms shown in *Figure 14* are very similar to the rising edge waveforms found when a DTL gate output goes from the LOW to HIGH state. This characteristic waveform has usually been attributed to the series RC circuit (a gate output resistance driving a lumped transmission line capacitance). The time constant for this approach, based on the $C(dv/dt) = i$ rule from simple circuit theory, provides only an approximation. The actual cause of the waveform shape, however, is due to reflection effects. Unfortunately, the only way to speed up the rising edge is to reduce source resistance, (providing an initial step greater than the receiving threshold) and terminate the line to eliminate the load reflections.

DTL inability to drive transmission lines at high repetition rates is the direct result of the signal rise time limitation caused by positive reflection coefficients for both the source and load. A transmitted positive pulse may be missed if its duration is less than the time required for the load signal to reach the receiver threshold.

The $R_S > R_0$ and $R_L > R_0$ case provides no definite advantages as voltage mode communication is concerned. This case, in fact, poses a definite hazard to high speed data communications because the reflections cause, in effect, a slow, exponential signal transition. Because line delay is a factor, longer lines will only increase the effect.

TABLE A. (R_S = 2000Ω, R_0 = 100Ω, R_L = 4000Ω)

RHOS = 0.904762 RHOL = 0.951220
TAU = −13.3250 V1(1) = 4.76190H-C2
V_{SS} = 0.666667

TIME	VM(T)	VAPPX	%DIFF
0.5	0.04762	0.04820	+1.220%
1.5	0.09292	0.09292	+0.000%
2.5	0.13390	0.13440	+0.373%
3.5	0.17288	0.17288	+0.000%
4.5	0.20815	0.20858	+0.207%
5.5	0.24170	0.24170	+0.000%
6.5	0.27206	0.27243	+0.136%
7.5	0.30093	0.30093	+0.000%
8.5	0.32705	0.32737	+0.097%
9.5	0.35190	0.35190	+0.000%
10.5	0.37439	0.37466	+0.073%
11.5	0.39577	0.39577	+0.000%
12.5	0.41512	0.41536	+0.057%
13.5	0.43353	0.43353	+0.000%
14.5	0.45018	0.45038	+0.045%
15.5	0.46602	0.46602	+0.000%
16.5	0.48035	0.48053	+0.036%
17.5	0.49399	0.49399	+0.000%
18.5	0.50632	0.50647	+0.030%
19.5	0.51805	0.51805	+0.000%
20.5	0.52867	0.52880	+0.024%
21.5	0.53877	0.53877	+0.000%

TABLE B. (R_S = 500Ω, R_0 = 75Ω, R_L = 10 kΩ)

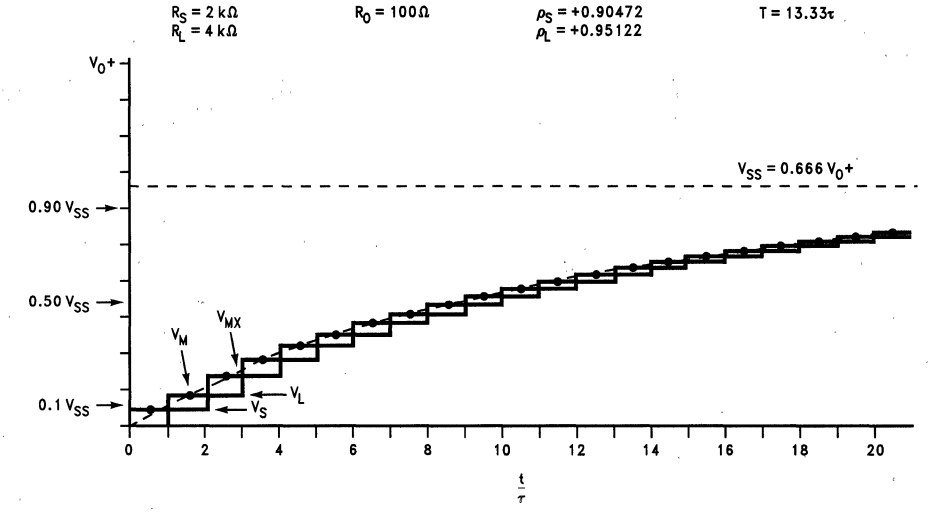
RHOS = 0.739130 RHOL = 0.985112
TAU = −6.30356 V1(1) = 1.30435
V_{SS} = 0.952381

TIME	VM(T)	VAPPX	%DIFF
0.5	0.13043	0.13971	+7.112%
1.5	0.25893	0.25893	+0.000%
2.5	0.35390	0.36066	+1.909%
3.5	0.44746	0.44746	+0.000%
4.5	0.51661	0.52153	+0.952%
5.5	0.58473	0.58473	+0.000%
6.5	0.63509	0.63867	+0.564%
7.5	0.68469	0.68469	+0.000%
8.5	0.72135	0.72396	+0.361%
9.5	0.75747	0.75747	+0.000%
10.5	0.78416	0.78606	+0.242%
11.5	0.81046	0.81046	+0.000%
12.5	0.82990	0.83128	+0.167%
13.5	0.84904	0.84904	+0.000%
14.5	0.86320	0.86420	+0.117%
15.5	0.87714	0.87714	+0.000%
16.5	0.88744	0.88818	+0.083%
17.5	0.89759	0.89759	+0.000%
18.5	0.90510	0.90563	+0.059%
19.5	0.91249	0.91249	+0.000%
20.5	0.91795	0.91834	+0.042%
21.5	0.92334	0.92334	+0.000%

TABLE C. BASIC Program Listing

```
100 PRINT'ENTER RS, R0, RL'1
110 INPUT R1, R0, R2
120 P1=(R1-R0)/(R1+R0)
130 P2=(R2-R0)/(R2+R0)
140 V1=R0/(R1+R0)
150 K1=2./LOG(P1*P2)
160 V9=R2/(R1+R2)
170 PRINT'RHOS='; P1;'RHOL=';P2;'TAU=';K1
180 PRINT 'V1(1)=';V1;'VSS=';V9
190 V=V1
200 PRINT'TIME   VM(T)   VAPPX   %DIFF'
210 FOR T=0.5 TO 20.5 STEP 2.
220 V2=V9*(1.-EXP((T+.5)/K1))
230 P=100.*(V2-V)/V
240 PRINT USING 250,T,V,V2,P
250 :##.# -#.##### -#.##### +###.###%
260 V1=V1*P2
270 V=V+V1
280 REM  SOURCE END
290 V2=V9*(1.-EXP( (T+1.5)/K1 ) )
300 P=100.*(V2-V)/V
310 PRINT USING 250,T+1.,V,V2,P
320 V1=P1*V1
330 V=V+V1
340 NEXT T
350 PRINT
360 PRINT
370 PRINT
380 GOTO 100
390 END
```

FIGURE 13. Comparison of v_m Formula to Computed Midline Voltage



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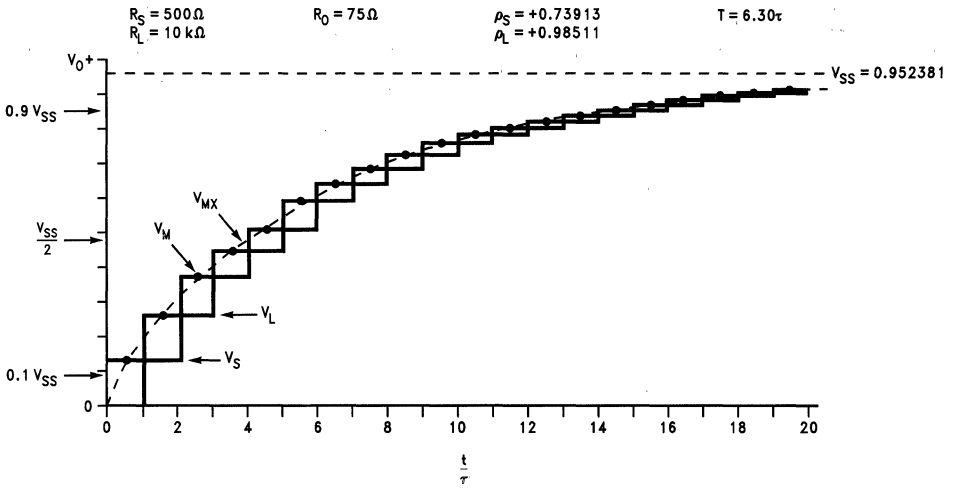

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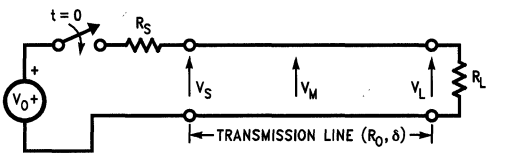

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$$v_{MX}(t) = V_{SS}\left(1 - \exp[-(t + 0.5\tau)/T]\right)$$

$$t = \frac{-2\tau}{\ell n\,(\rho_S\,\rho_L)}$$

FIGURE 14. Approximation of Midline Voltage with $R_S > R_0$ and $R_L > R_0$

SUMMARY—Which are the Advantageous Combinations?

In examining the basic combinations of source, line and load resistances, and typical waveforms characteristic of each case, advantageous combinations can be determined. The primary results are tabulated in *Figure 15*. those combinations generally used in voltage mode communications circuits are as follows.

1. Unterminated case ($R_S \ll R_0$, $R_L \gg R_0$). This situation provides low steady state power dissipation and large signal levels, but also shows pronounced "ringing" effects. The "ringing" can be reduced by controlling signal rise/fall time versus τ, or by clamping diodes to limit load signal excursions. This case is representative of TTL circuits and is thus widely employed.
2. The parallel terminated case ($R_S \ll R_0$, $R_L = R_0$) provides large signal levels, and excellent signal fidelity. However, it is power consuming with most of that power dissipated in the load resistor. This case is useful for cleaning up the reflection effects of Case 1 but, at the same time, does require a driver circuit to have its internal current limits set at greater values than those required to produce the desired signal level into the minimum line resistance used. Thus, this case requires specific line driver devices such as the DS75114/DS9614. Ordinary TTL, except for the above mentioned circuits, has too low a current limit point to adequately drive 50Ω lines.
3. The series terminated or backmatched driver case $R_S = R_0$, $R_L \gg R_0$ provides a low steady state power dissipation system for use with one receiver located at the load end of the line. The positive reflection coefficient of the load is used to approximately double the initial wave arriving at the load. Setting $R_S = R_0$ terminates the reflected wave when it arrives back at the source site after two line delays, and the line then assumes steady state conditions. The use of other receivers located along the line is not recommended, because they will not see the full driver signal swing until the reflection from the load passes their particular bridging points Such receivers could malfunction, as they would see a voltage very close to their threshold, and perhaps even place the line receiver in its linear operating region. This could make the line receiver sensitive to oscillatory, parasitic feedback. If these constraints are acceptable, the series termination method can be used to good advantage in providing the same signal fidelity and signal amplitude as with the parallel termination method, while at the same time, contributing a significant savings in steady state power consumption.
4. The fully matched case $R_S = R_0$, $R_L = R_0$ not only provides excellent signal fidelity all along the line, but also has reduced signal amplitude over that of the parallel terminated case. Additionally, the power consumption is somewhat less than the parallel termination case and the power is divided equally by the source and load. The primary advantage of the fully matched system is that termination resistor tolerances can be relaxed somewhat without incurring large amounts of ringing. This is because both the source and load act as line terminations.

Configuration Name (if any)	(Driver) Source Resistance	(Receiver) Load Resistance	Signal Characteristics	Optimum Receiver Threshold	Line Receivers Allowed at Other Than Load End of Line?	Comments
Unterminated	$\ll R_0$	$\gg R_0$	Ringing Pronounced	0.5 V_{SS}	Yes	Undershoot May Cause Data Errors
Parallel Terminated	$\ll R_0$	$= R_0$	Excellent Fidelity	0.5 V_{SS}	Yes	Load Resistor Consumes Power $P_L = \frac{(V_{SS})^2}{R_L}$
	$\ll R_0$	$\ll R_0$	Awful—Different Signals at Each Point on the Line	NA	No	Not Generally Useful
Series Terminated or Backmatched Driver	$= R_0$	$\gg R_0$	Load Signal Excellent	0.5 V_{SS}	No	Reduced Power Consumption Over Parallel Termination
Fully Matched	$= R_0$	$= R_0$	Excellent Fidelity	0.25 V_{SS}	Yes	Greater Tolerances on Resistors Allowed for Same Fidelity as Parallel Termination
	$= R_0$	$< R_0$	Load Signal Like a One-Shot	NA	NA	Not Generally Useful for Data, is Useful as Pulse Generator
	$\gg R_0$	$\gg R_0$	Exponential Like Signal Waveforms	0.5 V_{SS}	Yes	Low Power Consumption. Increased Delay due to Signal "Rise" Times.
	$\gg R_0$	$= R_0$	Small Signal Amplitude and Excellent Fidelity	0.5 V_{SS}	Yes	Produces Only Small Signal Voltages Compared with Other Methods. Uses Current Sinking Drivers such as the 75110A.
	$\gg R_0$	$< R_0$	Very Small Signal Amplitudes, also Ringing	NA	NA	Not Generally Useful

FIGURE 15. Summary of Effects

EFFECT OF SOURCE RISE TIME ON WAVEFORMS

Previously, it was assumed that the source-produced signal rise time was always much less than the line time delay (τ). Because the waveforms for the source and load voltage were the superposition of incident and reflected waves occurring at their proper times, and because the shape of each wave was a square edged step function, the resultant source and load waveforms were thus also square edged, or *ideal* in nature. In many practical cases, particularly when line length is short, the source excitation possesses a finite, and non-negligible, rise time. Therefore, depending on the ratio of rise time to line delay, it is possible to have a new wave start arriving at the point of interest *before* the previous wave can reach its final value. The net waveform for voltage or current at that point, then, would consist of the superposition of two or more waves during their time of overlap. To study the superposition effect on signal waveforms, the source excitation is represented as a simple linear ramp rise to its final value of V_{0+}, so

$$e(t) = 0 \text{ for } t < 0$$

$$e(t) = V_{0+} \bullet t/t_r \text{ for } 0 \le t \le t_r$$

$$e(t) = V_{0+} \text{ for } t > t_r$$

and where t_r represents the 0-to-100% source rise time. The circuit model and its lattice diagram are shown in *Figure 16*. The values of R_S, R_0 and R_L were chosen to equal those of an actual circuit on hand, allowing the theoretical waveforms, obtained by graphical superposition, to be compared with the measured response of an actual circuit.

Figure 17 shows the load voltage v_L, source voltage v_S and source current i_S waveforms versus time for a circuit with a source rise time very much less than τ. The actual waveforms for v_L, v_S and i_S are composed of the superposition of both incident and reflected waves in their proper time sequence. In the figures, these waves are shown as dotted lines. Each wave represents the sum of the incident wave plus its reflection. The resultant v_L, v_S and i_S waveforms (shown as solid lines) are the superposition of the waves represented by the dotted lines. With the exception of a slight rounding of the edges, the actual waveforms for the circuit, shown in the oscilloscope photograph in *Figure 17*, closely approximate the waveforms predicted by theory.

Source					Load				
t in (τ)	$v_i + v_r$ (V)	$i_i + i_r$ (mA)	v_S (V)	i_S (mA)	t in (τ)	$v_i + v_r$ (V)	$i_i + i_r$ (mA)	v_L (V)	i_L (mA)
0	0.9400	12.53	0.9400	12.53	1	1.8500	0.40	1.8500	0.40
2	0.1224	−22.64	1.0624	−10.10	3	−1.5500	−0.34	0.3000	0.06
4	−0.1026	18.97	0.9599	8.87	5	1.2986	0.28	1.5986	0.35
6	0.0859	−15.90	1.0458	−7.03	7	−1.0881	−0.24	0.5106	0.11
8	−0.0720	13.32	0.9738	6.29	9	0.9116	0.20	1.4222	0.31
10	0.0603	−11.17	1.0341	−4.87	11	−0.7638	−0.17	0.6584	0.14
12	−0.0505	9.36	0.9836	4.48	13	0.6399	0.14	1.2983	0.28
14	0.0424	−7.84	1.0259	−3.36	15	−0.5362	−0.12	0.7622	0.16
16	0.0355	6.57	0.9904	3.21	17	0.4492	0.10	1.2114	0.26

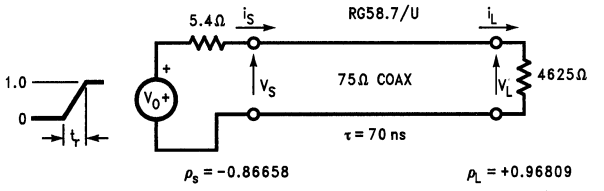

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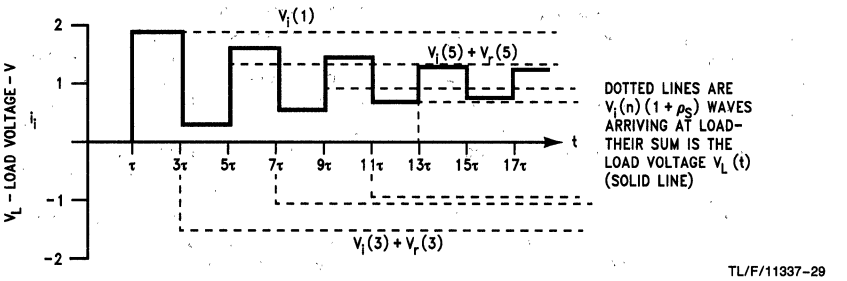
FIGURE 16. Transmission Line Model and Its Lattice Diagram



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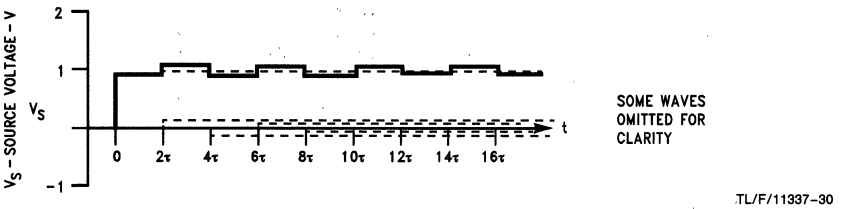

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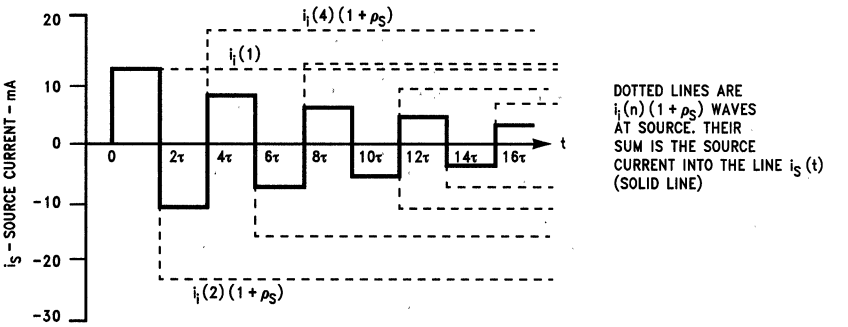

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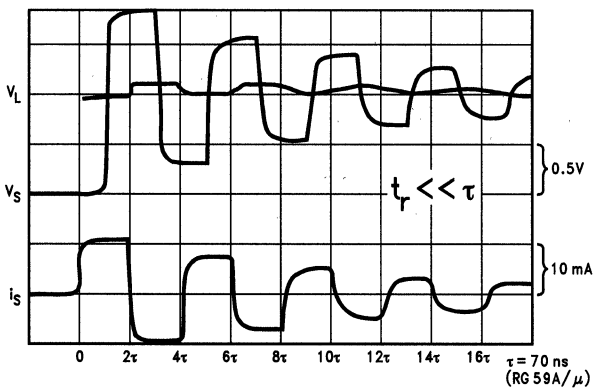

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FIGURE 17. Waveforms for $t_r = 2 \ll \tau$

If the source excitation is adjusted so that its 0-to-100% rise time t_r is equal to 2τ, each of the $v_i + v_r$ and $i_i + i_r$ waveforms must be modified to include this rise time. The waves will have the same final value as predicted by the lattice diagram, but they now require two line time delays to reach this final value. The v_L, v_S and i_S waveforms consist of the superposition of these linear ramps. Because each wave reaches its final value just as a new wave arrives, their superposition converts the square edged v_L, v_S and i_S waveforms into triangular waveforms. This is shown in *Figure 18*. The accompanying oscilloscope plot shows the close correspondence between the actual and theoretical waveforms whereas an additional oscilloscope photograph in *Figure 18* shows the actual waveforms for the case where $t_r = \tau$. Not surprisingly, the $t_r = \tau$ case changes the v_L, v_S and i_S waveforms of the $t_r \ll \tau$ case into trapeziodal forms because each arriving wave reaches its final value well before a new wave arrives.

If the source excitation is adjusted such that its rise time equals three line delays $t_r = 3\tau$, the $v_i + v_r$ and $i_i + i_r$ waves overlap for a period of time equal to τ. That is, each wave reaches only ⅔ of its final value when a new wave starts arriving. Considering the waveform, the load voltage from time τ to 3τ is

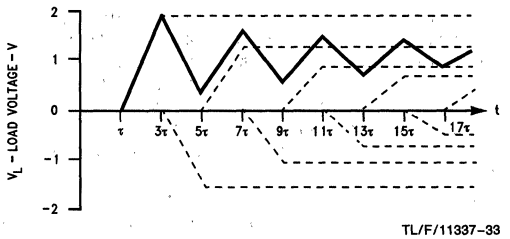
$$v_i(1)\,(1 + \rho_L)\,e\,(t - \tau)$$

Starting at $t = 3\tau$, the wave

$$v_i(3) = v_i(1)\rho_S\rho_L\,e(t - 3\tau).$$

begins arriving from the source, and the load voltage then is the superposition of these two waves. Because $v_i(3)$ is a negative wave ($\rho_S < 0$), the algebraic sum of the last third of the first wave and the first third of the second wave $v_i(3)$ arriving at the load causes the load voltage to reduce in amplitude from the ($t_r \ll \tau$) case. Likewise, the source voltage and source current show reduced amplitudes over the ideal case, due to the overlap period of the waves arriving at the source.

Theoretical and actual waveforms for the $t_r = 3\tau$ case are shown in *Figure 19*. Notice that load voltage perturbations and source current i_S requirements are reduced from those of the $t_r \ll \tau$ case. Similarly, the ratio of t_r to τ can be successively increased. This results in reduced ringing on the load voltage and reduced source current due to the overlapping of more and more $v_i + v_r$ (or $i_i + i_r$) waves. Actual and theoretical waveforms for t_r equal to 4τ, 6τ, and 8τ are shown in *Figures 20*, *21* and *22*, respectively. In each case, as the t_r to τ ratio is increased, the instantaneous source and load voltages become more equal. The source current is also reduced so that the circuit exhibits fewer reflection effects and the transmission line itself can be considered as a simple interconnection from dc circuit theory.



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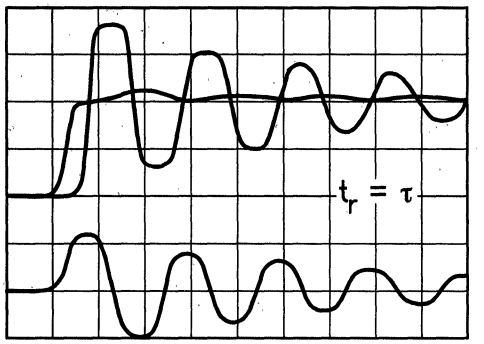

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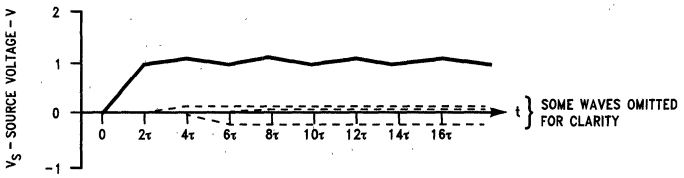

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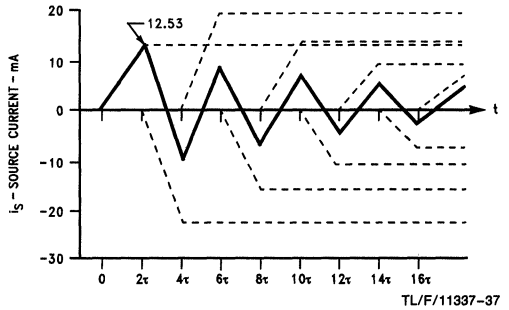

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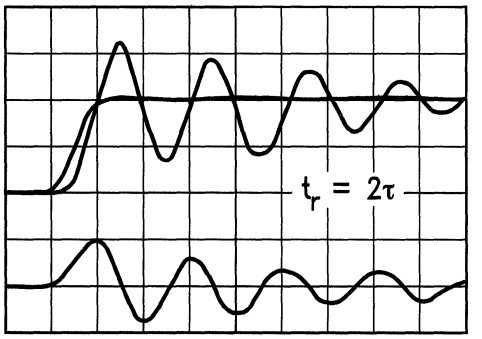

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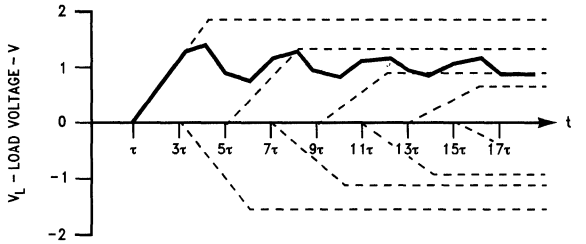
FIGURE 18. Waveforms for $t_r = 2\tau$



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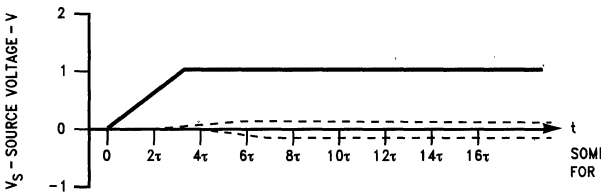

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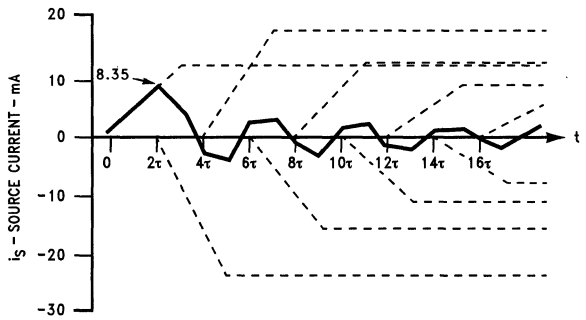

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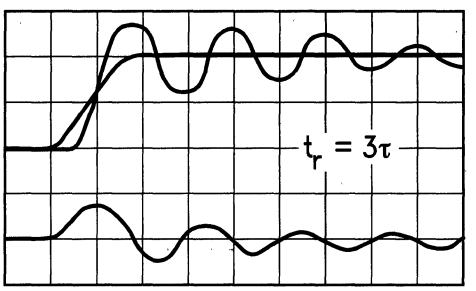

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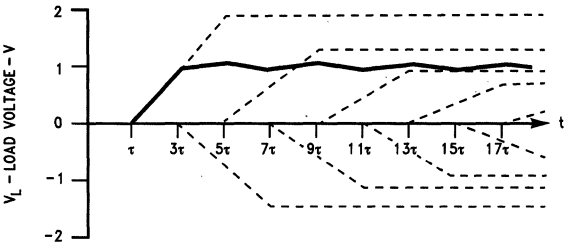
FIGURE 19. Waveforms for $t_r = 3\tau$



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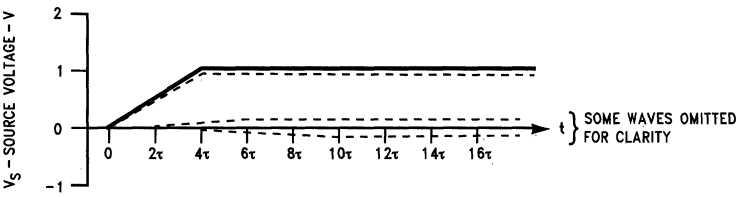

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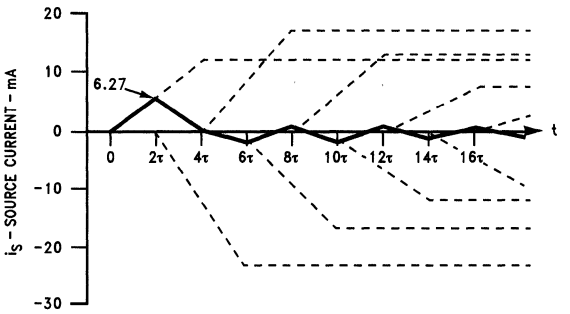

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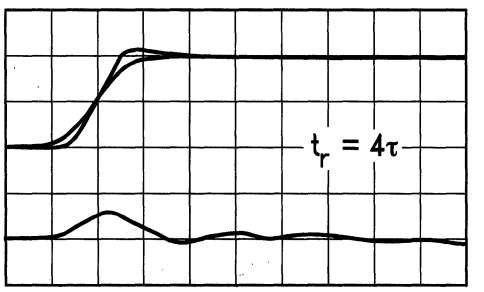

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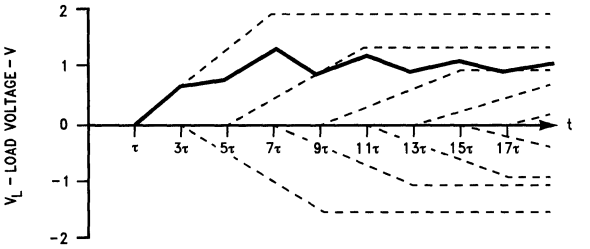
FIGURE 20. Waveforms for $t_r = 4\tau$



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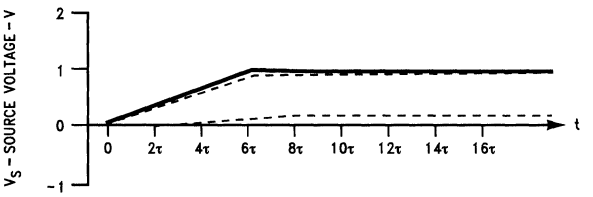

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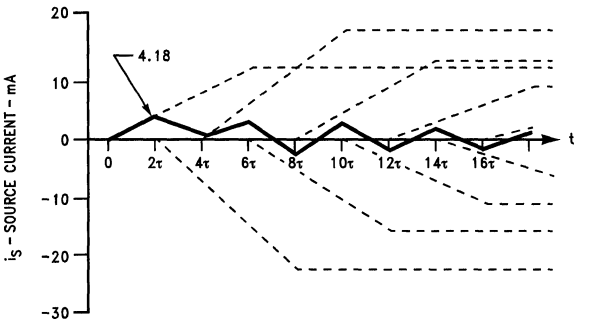

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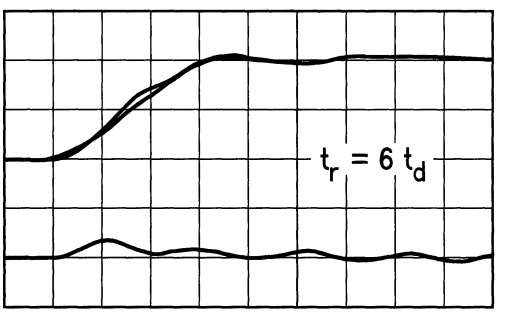

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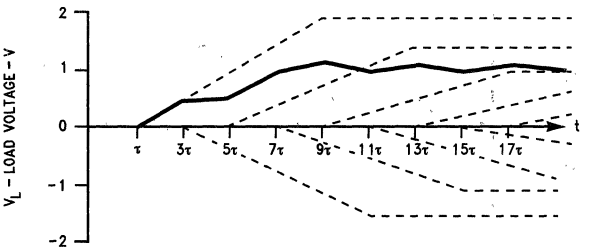
FIGURE 21. Waveforms for $t_r = 6\tau$



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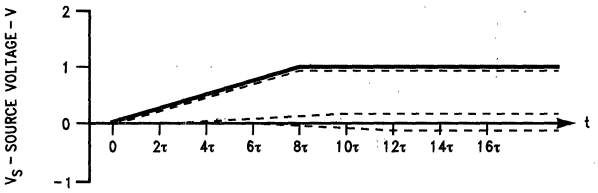

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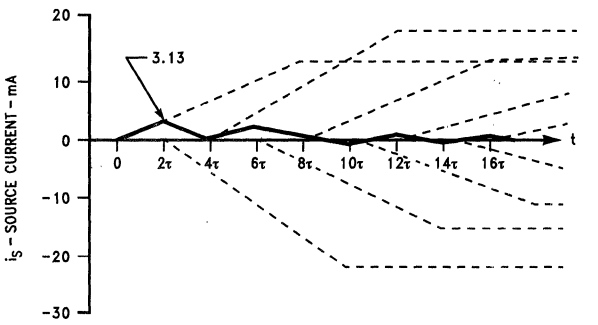

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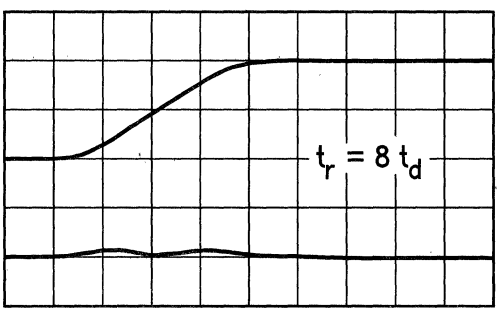

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FIGURE 22. Waveforms for $t_r = 8\tau$

Using the t_r to τ ratio to reduce reflection effects has many practical advantages in digital design. The low source and high input resistance of TTL or ECL circuits allows one gate to drive many receiving gates. The reflection effects of this unterminated combination, however, can cause data errors or at least lead to reduced noise immunity due to the pronounced load voltage undershoot. Since the rise and fall times of these devices are easily measured, a maximum line length can be set such that the resulting t_r to τ ratio provides the desired reduction in ringing. This is the primary basis for the wiring rules of each logic family and, usually, the t_r to τ ratio is chosen somewhere between 3:1 and 4:1. As an example, the rise and fall time for normal TTL is $t_{10\%-90\%} = 6$ ns. When this is converted to an equivalent linear 0% to 100% time, $t_r = 8$ ns. A common propagation delay of 1.7 ns/ft, in combination with the requirement that $t_r = 3\tau$, gives the maximum line length of approximately 18 inches. This corresponds with the published recommendation of the various manufacturers for the 74 series TTL circuits. A similar computation of the rise and fall times for other logic families yields their respective line length recommendations. The faster families require shorter line lengths for the same t_r to τ ratio, and slower logic families allow relatively longer line length. This ratio can also be used to make stubs or taps on lines "disappear". In other words, if the stub's time delay is made very short when compared to the t_r of the signal at the stub line location, the stub reflections will have a minimal effect on the line signals. A stub length to generate a t_r to τ ratio of greater than 8:1 is usually considered adequate to negate the stub reflections.

The third primary application of the t_r to τ ratio for controlling reflection effects is that used in some standard data communications interfaces such as EIA/TIA-232-E (RS-232). Here, driver slew rate is explicitly controlled. This, along with the implied maximum interconnect cable length serves to produce a t_r to τ ratio of 3:1 or greater. This, in turn, reduces the reflection effects inherent in a voltage source driver, unterminated line system. The main disadvantage of using the t_r to τ ratio to control reflection effects is in the overall time for the signal representing the data to rise above the receiver threshold level. With the parallel terminated method, the minimum time delay was τ or one line delay. When the t_r to τ ratio is used, an additional delay time of approximately 0.5 t_r is added to the line delay yielding, therefore, a greater effective signal propagation delay. This increased delay may or may not be acceptable in the desired system so the trade-off between ease of usage of the unterminated case must be weighed against the increased effective signal delay over that delay obtainable with the terminated case.

REFERENCES

See AN-806 and AN-808

Long Transmission Lines and Data Signal Quality

National Semiconductor
Application Note 808
Kenneth M. True

OVERVIEW

This application note explores another important transmission line characteristic, the reflection coefficient. This concept is combined with the material in AN-806 to present graphical and analytical methods for determining the voltages and currents at any point on a line with respect to distance and time. The effects of various source resistances and line termination methods on the transmitted signal are also discussed. This application note is a revised reprint of section four of the Fairchild Line Driver and Receiver Handbook. This application note, the third of a three part series (See AN-806 and AN-807), covers the following topics:

- Factors Causing Signal Wave-Shape Changes
- Influence of Loss Effects on Primary Line Parameters
- Variations in Z_0, $\alpha(\omega)$ and Propagation Velocity
- Signal Quality—Terms
- Signal Quality Measurement—The Eye Pattern
- Other Pulse Codes and Signal Quality

INTRODUCTION

Transmission lines as discussed in AN-806 and AN-807 have always been treated as ideal lossless lines. As a consequence of this simplified model, the signals passing along the lines did not change in shape, but were only delayed in time. This time delay is given as the product of per-unit-length delay and line length ($\tau = \ell\,\delta$). Unfortunately, real transmission lines always possess some finite resistance per unit length due to the resistance of the conductors composing the line. So, the lossless model only represents *short* lines where this resistance term can be neglected. In AN-806 the per-unit-length line parameters, L, R, C, G, were assumed to be both constant and independent of frequency (up to the limits mentioned, of course). But with real lines, this is not strictly correct as four effects alter the per-unit-length parameters, making some of them frequency dependent. These four effects are skin effect, proximity effect, radiation loss effect, and dielectric loss effect. These effects and how they influence the intrinsic line parameters are discussed later in this application note. Since these effects make simple ac analysis virtually impossible, operational (Laplace) calculus is usually applied to various simplified line models to provide somewhat constrained analytical solutions to line voltages and currents. These analytical solutions are difficult to derive, perhaps even more difficult ot evaluate, and their accuracy of prediction depends greatly on line model accuracy. Analytical solutions for various lines (primarily coaxial cables) appear in the references, so only the salient results are examined here.

Engineers designing data transmission circuits are not usually interested in the esoterica of lossy transmission line theory. Instead, they are concerned with the following question: given a line length of x feet and a data rate of n bps, does the system work—and if so—what amount of transition jitter is expected? To answer this question using analytical methods is quite difficult because evaluation of the expressions representing the line voltage or current as a function of position and time is an involved process. The references at the end of this application note provide a starting point to generate and evalute analytical expressions for a given cable.

The effects on the LRCG line parameters, the variations in Z_0, $\alpha(\omega)$, and propagation velocity as a function of applied frequency are discussed later in this application note. Using an empirical approach to answer the "how far—how fast" question involves only easily made laboratory measurements on that selected cable. This empirical approach, using the binary eye pattern as the primary measurement tool, enables the construction of a graph showing the line length/data rate/signal quality trade-offs for a particular cable. The terms describing *signal quality* are discussed later in this application note. The technique of using actual measurements from cables rather than theoretical predictions is not as subject to error as the analytical approach. The only difficulties in the empirical method are the requirements for a high quality, real time (or random sampling) oscilloscope and, of course, the requisite amount of transmission line to be tested.

Also discussed in this application note are commonly used pulse codes.

FACTORS CAUSING SIGNAL WAVE SHAPE CHANGES

In AN-806 and AN-807, it was assumed that the transmission lines were ideal so the step functions propagated along the lines without any change in wave shape. Because a single pulse is actually composed of a continuous (Fourier) spectrum, the phase velocity independence on an applied frequency, and the absence of attenuation (R = 0, G = 0) of the ideal line always allows the linear addition of these frequency components to reconstruct the original signal without alteration. For real lines, unfortunately, the series resistance is not quite zero, and the phase velocity is slightly dependent on the applied frequency. The latter results in *dispersion; i.e.*, the propagation velocity will differ for the various frequencies, while the former results in signal *attenuation* (reduction in amplitude). This attenuation may also be a function of frequency. Attenuation and dispersion cause the frequency components of a signal, at some point down the line, to be quite different from the frequency components of the signal applied to the input of the line. Thus, at some point down the line, the frequency components add together to produce a wave shape that may differ significantly from the input signal wave shape. In many ways, then, a real transmission line may be thought of as a distributed lowpass filter with loss. The fast rise and fall times of the signals become progressively "rounded" due to attenuation and dispersion of the high frequency signal components.

It should be noted that there is a theoretical condition where attenuation is independent of frequency and dispersion is zero. This results in a line causing signal amplitude reduction, but no change in signal wave shape. This condition was first discussed by Heavyside and is called the *distortionless* line. To make a line distortionless, the primary line parameters must satisfy the relation (R/L) = (G/C). Because for real lines (R/L) > (G/C), the distortionless line is only of historical interest, and it is not possible to satisfy the (R/L) = (G/C) condition over a sufficiently wide bandwidth to allow a proper transmission of short duration pulses. Over a limited frequency range such as that encountered in telephony (0 kHz–4 kHz), the L term can be increased by either adding lumped inductances at fixed intervals along the line or by winding a magnetic material (as a thin tape) around the conductors of the line throughout its length. Lumped loading is commonly applied to long telephone circuits to reduce the signal attenuation over a narrow frequency range; however this linearity is at the expense of in-band attenuation and non-linear delay distortion. The distributed loading method has been tried, but the mechanical characteristics of the magnetic materials have made the winding process very difficult. In any event, neither method allows short pulses to retain their wave shapes. The interest in line loading to produce the Heavyside condition for pulse transmission is therefore largely academic.

The following sections discuss the origins of the second-order effects—skin effect, proximity effect, radiation loss effect, and dielectric loss effect—and their influence on the LRCG transmission line parameters.

- Skin Effect: The phenomenon is based on two facts: a current flow in any real conductor produces an electric field given by Ohm's Law; the current distribution and/or magnetic field distribution in a conductor is frequency dependent. For dc current in a single isolated conductor, the current density is uniform across the conductor. When alternating current is used, the current density is not uniform across the conductor. Instead, the current tends to concentrate on the conductor surface. Current density continuously increases from the conductor center to its surface, but for practical purposes, the current *penetration depth*, d, is assumed as a dividing line for current density. The current is assumed to flow in a imaginary cylinder of thickness d with a constant current density throughout the cylinder thickness. Distribution of current densities for both actual and assumed models is shown in *Figure 1*.

  It can be seen that for *classical* skin effects, the penetration depth is given by

$$d = K\frac{1}{\sqrt{f}} \qquad (1)$$

  where $K = 1/\sqrt{\pi\mu\sigma}$, μ = magnetic permeability of the conducting material expressed in henries per unit length, and σ = conductivity of the conducting material. For MKS (SI) units and for a copper conductor

$$\sigma = 5.85 \times 10^7\ (\Omega\ \text{meter})^{-1}$$

$$\mu = 4\pi \times 10^{-7}\ (\text{H/meter})$$

  in which case, d would be the penetration depth expressed in meters.

  Because the skin effect reduces the equivalent conductor cross-sectional area, increasing frequencies cause an increase in the effective resistance per unit length of the line. This in turn leads to signal attenuation increasing with frequency. If the frequency response of a cable is plotted on log-log graph paper, log dB, or Nepers vs log frequency, the curve slope will be 0.5 if the cable losses are primarily governed by *classical* skin effects. The slope of the attenuation curve, along with the attenuation at a particular frequency, can be used to estimate coaxial cable transient response as a function of length.[2, 4]

*See Reference 2 and 4.

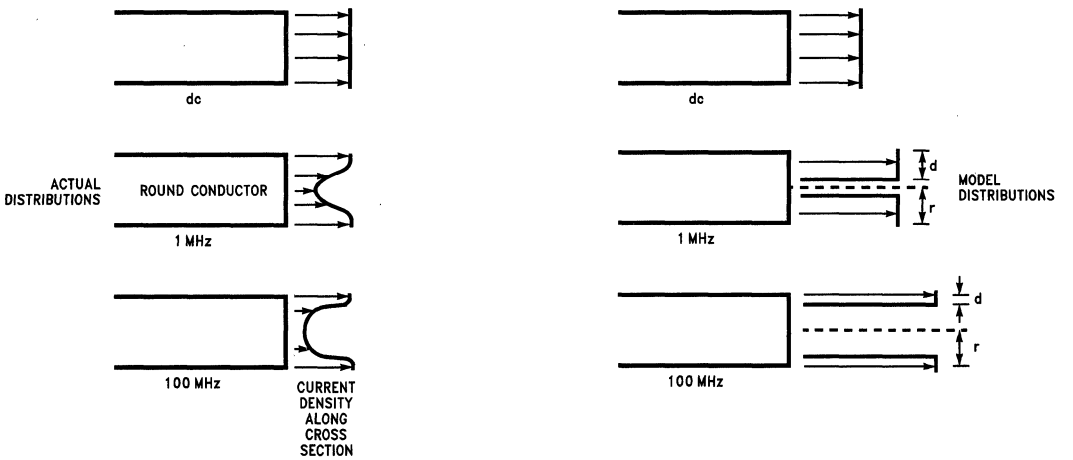

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FIGURE 1. Current Distributions Across and Conductor for Several Frequencies

- Proximity Effect: This is a current density redistribution in a conductor due to the mutual repulsion (or attraction) generated by currents flowing in nearby conductors. The current density at those points on the conductor close to neighboring conductors varies from the current density when the conductor is isolated from other conductors. This current density redistribution reduces the effective cross-sectional area of the conductor, thereby increasing the per-unit-length line resistance. This effect is a function of the conductor diameters, the separation of the conductors from each other, and frequency. The analytical evaluation of the proximity effect is quite complicated and except for certain limited cases*, no general rule of thumb expressions have been proposed. The proximity effect is not present in coaxial cables because of their circular symmetry. The proximity effect is a significant contributor to signal losses particularly in cases of a twisted pair or parallel wire lines.
- Radiation Loss: Radiation losses cause an apparent rise in resistance per unit length increasing with frequency. The mechanism of radiation loss is energy dissipation either as heat or magnetization via eddy currents in nearby metallic or magnetic masses, with the eddy currents induced by line currents. Coaxial cables do not exhibit this effect because the signal magnetic field is confined between the shield and the outside of the center conductor. Ideally, the magnetic field produced by shield current cancels the field produced by current in the center conductor (for points outside the shield).

  Both twisted pair and parallel wire lines exhibit radiation losses and these losses contribute to the effective per-unit-length line resistance. Radiation loss is dependent to a large extent on the characteristics of the materials close to the line; so radiation loss is quite difficult to calculate, but can be measured if necessary.
- Dielectric Loss Effect: Dielectric losses result from leakage currents through the dielectric material. This causes an increase in the shunt conductance per unit length and produces signal attenuation. Fortunately, for most dielectric materials in common use, this loss is very small particularly for frequencies below 250 MHz. For most practical purposes, then, dielectric losses may be neglected as they are usually overshadowed by skin effect losses.

INFLUENCE OF LOSS EFFECTS ON PRIMARY LINE PARAMETERS

Resistance Per Unit Length, R. It is composed of a basic dc resistance term R_{dc} plus the contributions of skin effect, proximity effect and radiation loss effect. For coaxial lines, the proximity and radiation loss effects are negligible in most cases, so the primary contribution is made by the skin effect. Thus the resistance per unit length becomes

$$R = R_{dc} + Ks^m \quad (2)$$

where $0 < m < 1$.

For 2-wire lines (twisted pair, parallel wire), the resistance per unit length is increased by the skin effect. For closely spaced wires, however, the proximity effect also contributes significantly to a resistance increase. Radiation loss should also be included, but is very difficult to calculate because it depends on the surroundings of the line.

Inductance Per Unit Length, L. It can be shown** that, as the frequency is increased, the skin effect, proximity effect, and radiation loss effect cause a reduction in the effective per-unit-length self-inductance of the line.

Capacitance Per Unit Length, C. This depends primarily on the dielectric constant of the insulating medium and conductor geometry. This term is constant over a wide range of frequencies for most dielectrics (Teflon®, Polyethylene). For Polyvinylchloride (PVC) insulation, the relative dielectric constant shows a decrease as frequency increases ($\epsilon_r \approx 4.7$ @ 1 kHz, $\epsilon_r \approx 2.9$ @ 100 MHz). The capacitance per unit length, therefore, will show a decrease corresponding with increasing frequency for PVC insulation and little change for most other dielectrics.

Conductance Per Unit Length, G. Because resistance per unit length usually has a much greater magnitude, this value is negligible. When this term cannot be neglected, it is represented as

$$G = \omega C \tan\phi \quad (3)$$

where C is capacitance per unit length, ω is the angular frequency ($= 2\pi f$) and $\tan\phi$ is a dielectric material coefficient. The angle ϕ is called the dielectric loss angle. This angle is usually quite small (< 0.005 radians) for the majority of dielectrics up to several hundred megahertz.

VARIATIONS IN Z_0, $\alpha(\omega)$, AND PROPAGATION VELOCITY

The variations in the primary line parameters as a function of frequency shown by *Figure 2* have a profound influence on the three secondary line parameters of characteristic impedance, attenuation, and velocity of propagation.

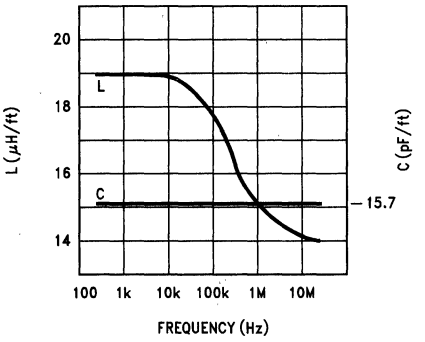
In the expression for the characteristic impedance of a line,

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

at low frequencies, $j\omega L$ is small compared to R, and G is small compared to $j\omega C$. So the characteristic impedance is $\sqrt{R/j\omega C}$. At high frequencies, the increase in R is overshadowed by $j\omega L$ even though L is being reduced. With G still much smaller than $j\omega C$, the characteristic impedance is almost a pure resistance $R_0 = \sqrt{L/C}$. The behavior of the characteristic impedance as a function of frequency ($Z_0 = R_0 - jX_0$) is shown in *Figure 3*.

*See References Arnold[11] and Dwight[12].

**See References 5 and 6



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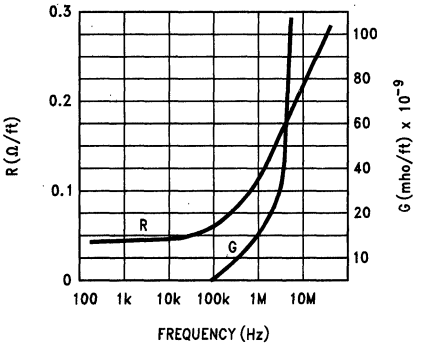

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FIGURE 2. Variations in Primary Parameters as a Function of Frequency (22 AWG Polyethylene Insulated Twisted Pair)

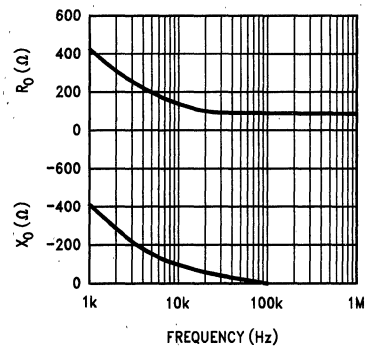

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FIGURE 3. Typical Variation in Z_0 as a Function of Frequencies

Typical behavior of the line attenuation as a function of frequency is shown in *Figure 4*. This line attenuation is the real part of the equation

$$\gamma(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)}.$$

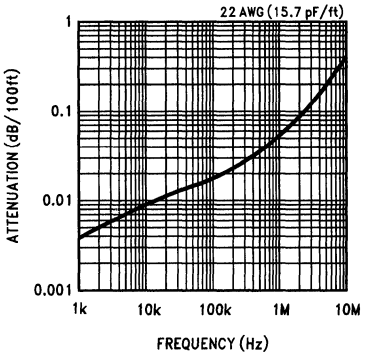

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FIGURE 4. Attenuation vs Frequency

The change in resistance is the primary contributor to the attenuation increase as a function of frequency. For coaxial cables, this resistance increase is due primarily to the skin effect ($R_{SK} = Kf^m$). The slope of the attenuation curve on a log-log graph (log dB vs log frequency), therefore, is essentially linear and, at the same time, equal to m. For twisted pair and parallel wire lines, proximity effects and radiation losses make the curves less linear, but for high frequencies (over 100 kHz), the attenuation expressed in nepers per unit length is approximated by

$$\alpha \cong \frac{R}{2}\sqrt{\frac{C}{L}} \qquad (4)$$

The R term is, of course, the sum of the dc resistance, plus the incremental resistance due to skin, proximity and radiation loss effects. This R term usually varies as follows.

$$R_{SK} = Kf^m$$

where $0.6 \leq m < 1.0$

The signal velocity propagation ($v = \omega/\beta$) is given by the imaginary part of the propagation constant γ. As shown in AN-807, v is a constant given by $v = \sqrt{LC}$ for lossless lines. For real lines, this value is approached at high frequencies. At low frequencies, however, (when ω is small compared to R/L or G/C), then $v_{LF} \cong (C/2)\sqrt{R/G}$ and the velocity is reduced. The propagation velocity as a function of frequency is shown in *Figure 5*. This variation in signal velocity as a function of signal frequency is *dispersion* which was previously discussed.

The signal at a point down the line represents the sum of that original signal's Fourier spectrum. Because both the attenuation and propagation velocity of these Fourier components increase with frequency, the resultant signal shape at that point down the line depends greatly on the winners of the race to get to that point. The high frequency components, with their faster propagation velocities, arrive first, but the increased attenuation minimizes their effect. The low frequency signals arrive later, but the reduced attenuation allows them a greater influence on the resultant signal. In general, the output signal from the line should show a relatively fast rise up to some signal value (20% to 50% of the final value). This is due to arrival of the high frequency components, followed by a more leisurely rise to the final value as the slower, low frequency components arrive.

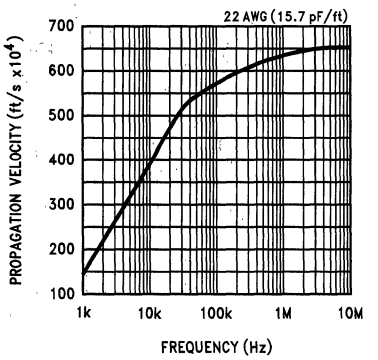

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FIGURE 5. Propagation Velocity vs Frequency

SIGNAL QUALITY—TERMS

Before the concepts presented in the previous sections can be used to answer the "how far—how fast" question, some familiarity with the terms describing data and signal quality is necessary.

The primary objective of data transmission is the transfer of *information* from one location to another. The information here is *digital* in nature; i.e., a finite number of separate states or choices. This is in contrast to *analog* which has an infinite number of separate states or a continuous range of choices. The digital information is *binary* or two-valued; thus two different, recognizable electrical states/levels are used to symbolize the digital information. A binary symbol is commonly called a binary-digit or *bit*. A single binary symbol or bit, by itself, can represent only one of two possible things. To represent alphabetic or numeric characters, a group of bits is arranged to provide the necessary number of unique combinations. This arrangement of bits which is then considered an information unit is called a *byte*. In the same manner that a group of bits can be called a byte, a collection of bytes, considered as a unit, is called a *word*. Selective arrangement of seven bits will provide 2^7 (or 128) distinct character combinations (unique bytes). The American Standard Code for Information Interchange (ASCII) is an excellent example of just such an arrangement—upper and lower case alphabetic, zero to nine numeric, punctuation marks, and miscellaneous information-code control functions.

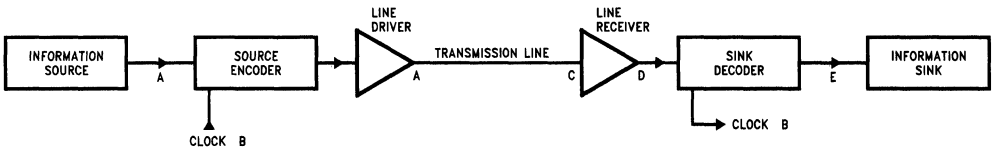
Now with the means for representing information as bits or bytes, and the means for transmission of the bits (symbols) from one location to another (transmission line), the remaining task is to ensure that a particular bit arriving at its destination is interpreted in the proper context. To achieve this, both the sender and receiver of the data must accomplish the five following requirements.

1. Agree upon the nominal rate of transmission; or how many bits are to be emitted per second by the sender.
2. Agree upon a specified information code providing a one-to-one mapping ratio of information-to-bit pattern and vice versa.
3. Establish a particular scheme whereby each bit can be properly positioned within a byte by the receiver of the data (assuming that bit-serial transmission is used).
4. Define the protocol (handshaking) sequences necessary to ensure an orderly flow of information.
5. Agree to the electrical states representing the logic values of each bit and the particular pulse code to be used.

These are by no means all of the points that must be agreed upon by sender and receiver—but these are probably the most important. Items 2, 3 and 4 are more or less "software" type decisions, because the actual signal flow along the transmission line is usually independent of these decisions. Because items 1 and 5 are much more dependent on the characteristics of line drivers, line receivers, and transmission lines, they are the primary concern here.

Figure 6 represents the components of a typical data transmission system. The *information source* can be a computer terminal or a digitized transducer output, or any device emitting a stream of bits at the rate of one bit every t_B seconds. This establishes the *information rate* of the system at $1/t_B$ bits per second. The information source in the figure feeds a *source encoder* which performs logic operations not only on the data, but also on the associated clock and, perhaps, the past data bits. Thus, the source encoder produces a binary data stream controlling the *line driver*. The line driver interfaces the source internal logic levels (TTL, CMOS, etc.) with transmission line current/voltage requirements. The transmission line conveys signals produced by the line driver to the line receiver. The line receiver makes a decision on the signal logic state by comparing the received signal to a decision threshold level, and the *sink decoder* performs logic operations on the binary bit stream recovered by the line receiver. For example, the sink decoder may extract the clock rate from the data or perhaps detect and correct errors in the data. From the optional sink decoder, the recovered binary data passes to the *information sink*—the destination for the information source data.

Assume for the moment that the source encoder and sink decoder are "transparent"; that is, they will not modify the binary data presented to them in any way. Line driver signals, then, have the same timing as the original bit stream. The data source emits a new bit every t_B seconds. The *pulse code* produced by the source encoder and line driver is called Non-Return to Zero (NRZ), a very common signal in TTL logic systems. A sample bit pattern with its NRZ representation is shown in *Figure 7a*. The arrows at the top represent the *ideal instants*, or the times the signal can change state. The term *unit interval* is used to express the time duration of the shortest signaling element. The shortest signaling element for NRZ data is one bit time t_B, so the unit interval for NRZ data is also t_B. The rate at which the signal changes is the *modulation rate* (or signaling speed), and *baud* is the unit of modulation rate. A modulation rate of one baud corresponds to the transmission of one unit interval per second. Thus the modulation rate, in baud, is just the reciprocal of the time for one unit interval. A unit interval of 20 ms, therefore, means the signaling speed is 50 baud. The reason for differentiating between the *information rate* in bits per second (bps) and the *modulation rate* in baud will be clarified after examining some of the other pulse codes later in this application note.



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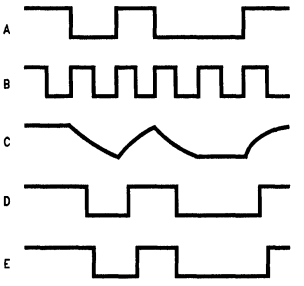

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FIGURE 6. Data Transmission System

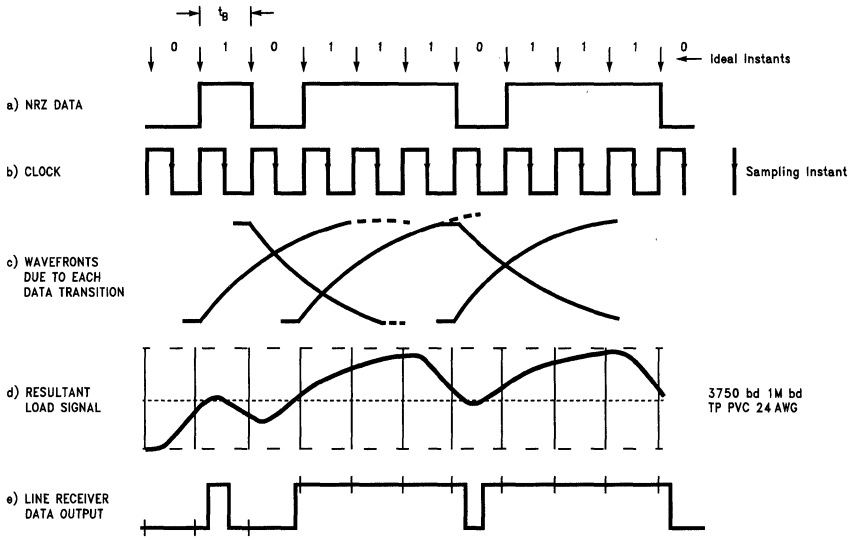

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FIGURE 7. NRZ Signaling

NRZ data should always be accompanied by a clock signal, *Figure 7b*, which tells the receiver when to sample the data signal and thus determine the current logic state. For the example in *Figure 7b*, the falling edge of the clock corresponds to the middle of the data bits, so it could be used to transfer the line receiver data output into a binary latch. The falling edge of the clock is thus the *sampling instant* for the data. The line receiver does have a *decision threshold* or slicing point so that voltages above that threshold level produce one logic state output, while voltages below the threshold produce the other logic state at the receiver output. The receiver may incorporate positive feedback to produce *hysteresis* in its transfer function. This reduces the possibility of oscillation in response to slow rise or fall time signals applied to the receiver inputs.

Previously in this application note, it was stated that the fast rise and fall times of signals, corresponding to the transisions between data bits, are rounded out and slowed down by a real transmission line. Each transition of the signal applied to the line by the line driver is transformed to a rounded out transition by the dispersion and attenuation of the transmission line. The resultant signal at the load end of the line consists of the superposition of these transformed transitions. The waves arriving at the load end of the line are shown in *Figure 7c* and their superposition is shown in *Figure 7d*. It is assumed that the line is terminated in its characteristic resistance so that reflections are not present. The receiver threshold level is shown here, superimposed on the resultant load signal, and the re-converted data output of the line receiver is shown in *Figure 7e* along with the ideal instants for the data transitions (tick marks).

Comparing the original data *(Figure 7a)* to the recovered data *(Figure 7e)* shows that the actual recovered data transitions may be displaced from their ideal instants (tic marks on *Figure 7e*). This time displacement of the transitions is due to a new wave arriving at the receiver site before the previous wave has reached its final value. Since the wave representing a previous data bit is *interfering* with the wave representing the present data bit, this phenomenon is called *intersymbol interference* (in telegraphy it is called *characteristic distortion*). The intersymbol interference can be reduced to zero by making the unit interval of the data signal quite long in comparison to the rise/fall time of the signal at the receiver site. This can be accomplished by either reducing the modulation rate for a given line length, or by reducing the line length for a given modulation rate.

Signal quality is concerned with the variance between the ideal instants of the original data signal and the actual transition times for the recovered data signal.

For synchronous signaling, such as NRZ data, the *isochronous distortion* of the recovered data is the ratio of the unit interval to the maximum measured difference irrespective of sign between the actual and theoretical significant instants.

The isochronous distortion is, then, the peak-to-peak time jitter of the data signal expressed as a percentage of the unit interval. A 25% isochronous distortion means that the peak-to-peak time jitter of the transition is 0.25 unit interval (max).

Another type of received-signal time distortion can occur if the decision threshold point is misplaced from its optimum value. If the receiver threshold is shifted up toward the *One signal level*, then the time duration of the One bits shortens with respect to the duration of the *Zero bits*, and vice versa. This is called *bias distortion* in telegraphy and can be due to receiver threshold offset (bias) and/or asymmetrical output levels of the driver. These effects are shown in *Figure 8*.

Bias distortion and characteristic distortion (intersymbol interference) together are called systemic distortion, because their magnitudes are determined by characteristics within the data transmission system. Another variety of time distortion is called *fortuitous distortion* and is due to factors outside the data transmission system such as noise and crosstalk, which may occur randomly with respect to the signal timing.

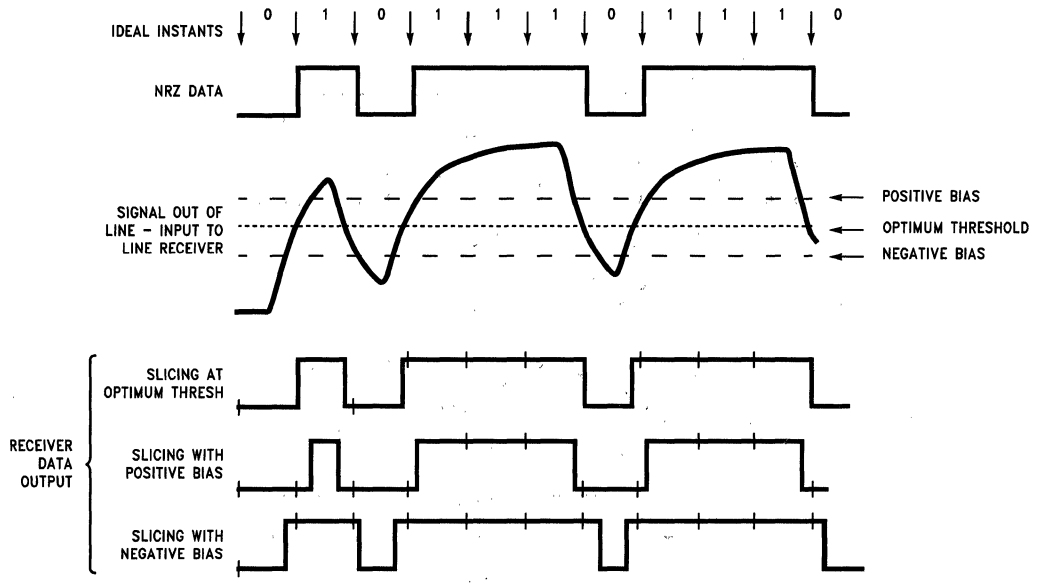

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FIGURE 8. Bias Distortion

SIGNAL QUALITY MEASUREMENT—THE EYE PATTERN

To examine the relative effects of intersymbol interference on random NRZ data and a "dotting"* pattern, see *Figure 9*. The top two waveforms represent the NRZ data and dotting pattern as outputs into two identical long transmission lines. The middle two traces illustrate the resultant signals at the line outputs and the bottom two traces show the data output of the line receivers. The respective thresholds are shown as dotted lines on the middle two traces. The arrows indicate the ideal instants for both data and dotting signals.

Notice that the dotting signal (D) is symmetrical, i.e., every One is preceded by a Zero and vice versa, while the NRZ data is random. The resultant dotting signal out of the line is also symmetrical. Because, in this case, the dotting half-cycle time is less than the rise/fall time of the line, the resultant signal out of the line (E) is a *partial response*—it never reaches its final level before changing. The dotting signal, due to its symmetry, does not show intersymbol interference in the same way that a random NRZ signal does. The intersymbol interference in the dotting signal shows up as a uniform displacement of the transitions as shown in *Figure 9f*. The NRZ data shows intersymbol interference, in its worst light, due to its unpredictable bit sequence. Thus, whenever feasibility of a data transmission system is to be tested, a random data sequence should be used. This is because a symmetrical dotting pattern or clock signal cannot always show the effects of possible intersymbol interference.

A very effective method of measuring time distortion through a data transmission system is based on the eye pattern. The eye pattern, displayed on an oscilloscope, is simply the superposition—over one unit interval—of all the Zero-to-One and One-to-Zero transitions, each preceded and followed by various combinations of One and Zero, and also constant One and Zero levels. The name *eye pattern* comes from the resemblance of the open pattern center to an eye. The diagramatic construction of an eye pattern is shown in *Figure 10*. The data sequence can be generated by a pseudo-random sequence generator (PRSG), which is a digital shift register with feedback connected to produce a maximum length sequence.

*The term dotting pattern is from telegraphy and means an alternating sequence of 1 bits and 0 bits (the "dot dot dot" etc). Note that an NRZ dotting pattern generates a signal which has a 50% duty cycle and a frequency of $\frac{1}{2}\ t_B$ (Hz).

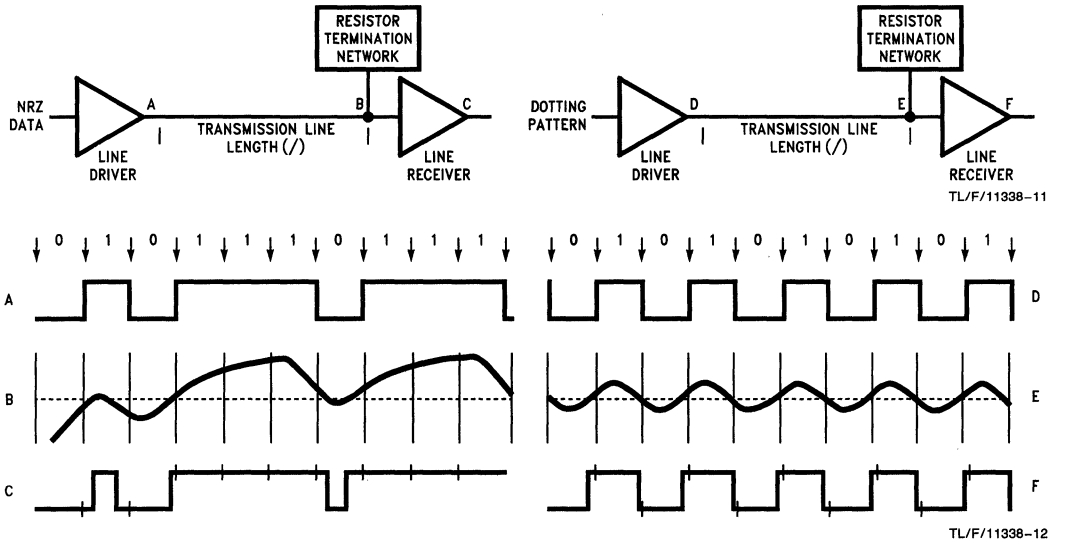

FIGURE 9. Comparison of NRZ Random Data and "Dotting" Signals

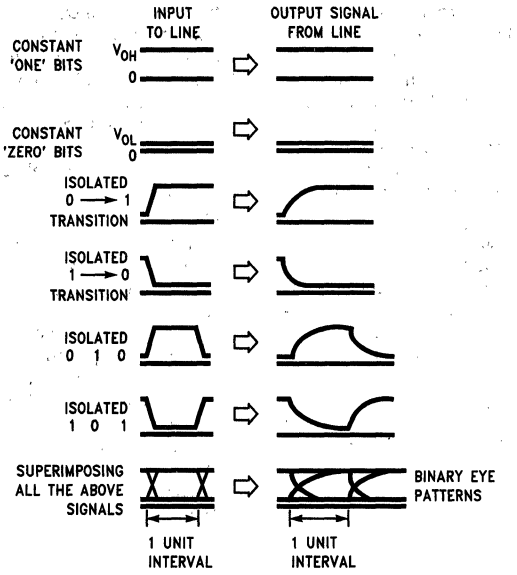

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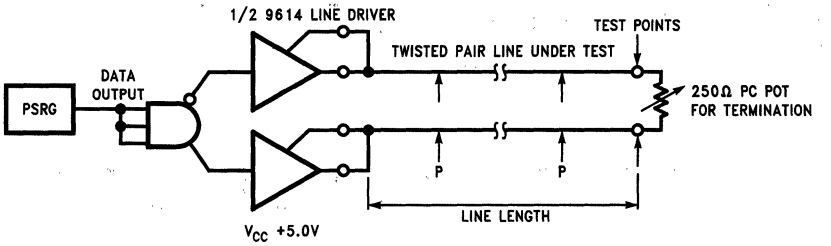
FIGURE 10. Formation of an Eye Pattern by Superposition



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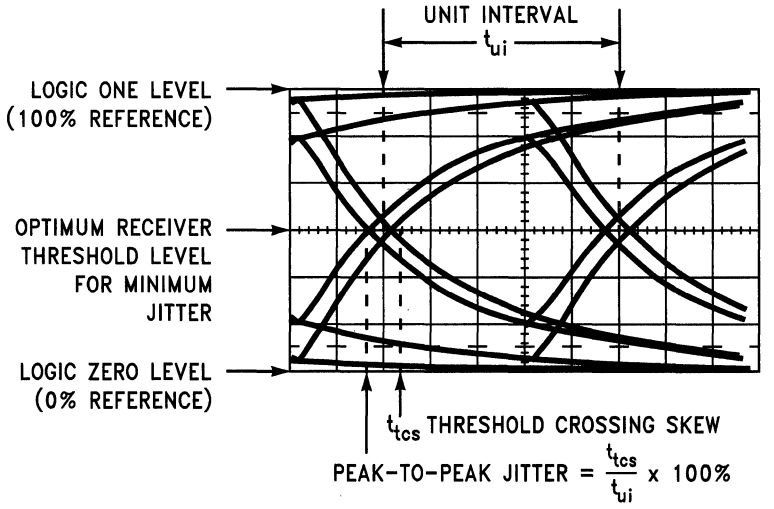
USE DIFFERENTIAL PROBE ACROSS TEST POINTS AND WIDE BANDWIDTH DIFFERENTIAL INPUT OSCILLOSCOPE TO DISPLAY EYE PATTERN.

FIGURE 11. Bench Set-Up to Measure Data Signal Quality

Several features of the eye pattern make it a useful tool for measuring data signal quality. *Figure 13* shows a typical binary eye pattern for NRZ data. The spread of traces crossing the receiver threshold level (dotted line) is a direct measure of the peak-to-peak transition jitter—isochronous distortion in a synchronous system—of the data signal. The rise and fall time of the signal can be conveniently measured by using the built-in 0% and 100% references produced by long strings of Zeros and Ones. The height of the trace above or below the receiver threshold level at the sampling instant is the noise margin of the system. If no clear transition-free space in the eye pattern exists, the eye is closed. This indicates that error-free data transmission is not possible at the data rate and line length with that particular transmission line without resorting to equalizing techniques. In some extreme cases, error-free data recovery may not be possible even when using equalizing techniques.

The eye pattern can also be used to find the characteristic resistance of a transmission line. The 250Ω printed circuit-type potentiometer termination resistor *(Figure 11)* can be adjusted to yield the minimum overshoot and undershoot of the data signal. *Figure 14* shows the NRZ data eye patterns for $R_T > R_O$, $R_T = R_O$ and $R_T < R_O$. The 100% and 0% reference levels are again provided by long strings of Ones and Zeros, and any overshoot or undershoot is easily discernible. The termination resistor is adjusted so that the eye pattern transitions exhibit the minimum perturbations *(Figure 13b)*. The resistor is then removed from the transmission line, and its measured value is the characteristic resistance of the line.



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2100 ft—Terminated
24 AWG Twisted Pair
Cable—PVC Insulation

FIGURE 12. NRZ Data Eye Pattern

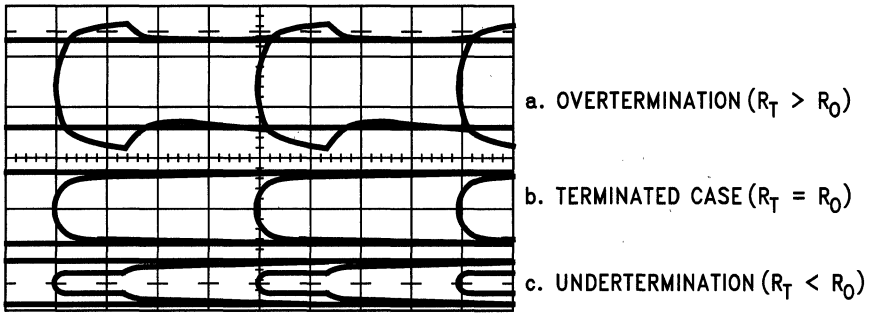

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FIGURE 13. Using Eye Pattern to Determine Characteristic Resistance of Line

By using the eye pattern to measure signal quality at the load end of a given line, a graph can be constructed showing the tradeoffs in signal quality—peak-to-peak jitter—as a function of line length and modulation rate for a specific pulse code. An example graph for NRZ data is shown in *Figure 14*. The graph was constructed using eye pattern measurements on a 24 AWG twisted pair line (PVC insulation) driven by a differential voltage source driver (75114/9614) with the line parallel-terminated in its characteristic resistance (96Ω). The oscilloscope plots in *Figure 15* show the typical eye patterns for NRZ data with various amounts of isochronous distortion. The straight lines represent a "best fit" to the actual measurement points. Since the twisted pair line used was not specifically constructed for pulse service, the graph probably represents a reasonably good worst-case condition insofar as signal quality vs line length is concerned. Twisted pair lines with polyethylene or Teflon® insulation have shown better performance at a given length than the polyvinyl chloride insulation. Likewise, larger conductors (20 AWG, 22 AWG) also

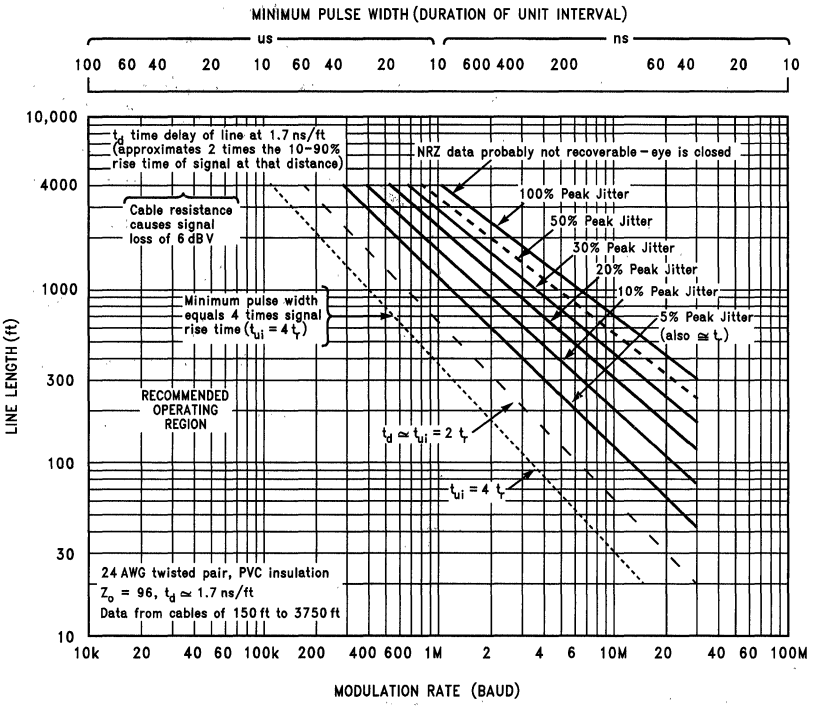

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FIGURE 14. Signal Quality as a Function of Line Length and Modulation Rate for Terminated 24 AWG Twisted Pair (PVC Insulation)

provide better performance at a given length. Thus, the graph in *Figure 14* can be used to estimate feasibility of a data transmission system when the actual cable to be used is unavailable for measurement purposes. The arbitrary cutoff of 4000 feet on the graph was due to the observed signal amplitude loss of 6 dBV (½ voltage) of the 24 AWG line at that distance. The cutoff of 10 Mbaud is based on the propagation delays of the typical TTL line drivers and receivers. Field experience has shown that twisted pair transmission systems using TTL drivers and receivers have operated essentially error-free when the line length and modulation rate are kept to within the recommended operating region shown in *Figure 14*. This has not precluded operation outside this region for some systems, but these systems must be carefully designed with particular attention paid to defining the required characteristics of the line, the driver, and the receiver devices. The use of coaxial cable instead of twisted pair lines almost always yields better performance, i.e., greater modulation rate at a given line length and signal quality. This is because most coaxial cable has a wider bandwidth and reduced attenuation at a given length than twisted pair line (one notable exception is RG 174/U cable).

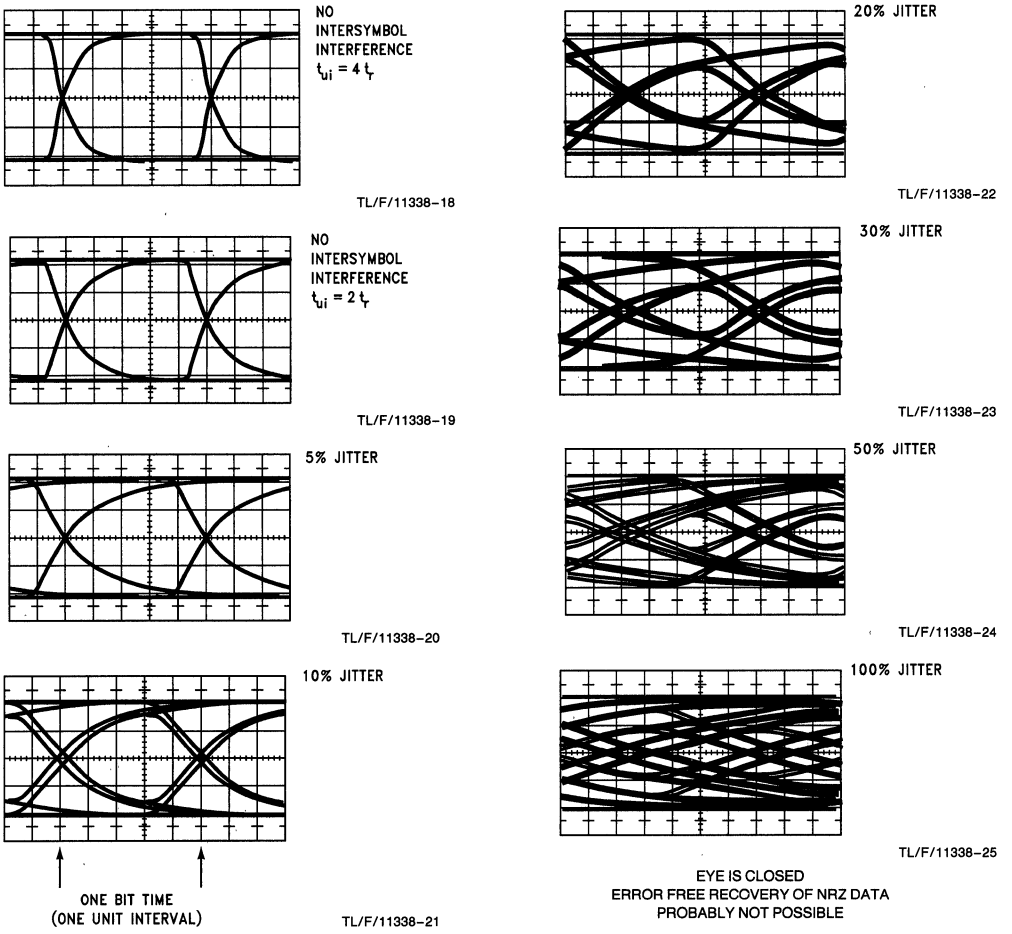


FIGURE 15. Eye Patterns for NRZ Data Corresponding to Various Peak-to-Peak Transition Jitter

It should be remembered that, in some ways, the eye pattern gives the *minimum* peak-to-peak transition jitter for a given line length, type, pulse code, and modulation rate. This is because the eye pattern transition spread is the result of intersymbol interference and reflection effects (if present) and this minimum jitter is only obtainable if the following conditions are met.

- The One and Zero signal levels produced by the line driver are symmetrical, and the line receiver's decision threshold (for NRZ signaling) is set to coincide with the mean of those two levels.
- The line is perfectly terminated in its characteristic resistance to prevent reflections from altering the signal threshold crossings.
- The time delays through driver and receiver devices for both logic states is symmetrical and there is no relative skew in the delays (difference between t_{plh} and t_{phl} propagation delays = 0). This is especially important when the device propagation delays become significant fractions of the unit interval for the applicable modulation rate.

If any one of these conditions is not satisfied, the signal quality is reduced (more distortion). The effects of receiver bias or threshold ambiguity and driver offset can be determined by location of the decision threshold(s) on the oscillograph of the eye pattern for that driver/cable modulation rate combination. For eye patterns displaying more than 20% isochronous distortion, the slope of the signal in the transition region is relatively small. Therefore, a small amount of bias results in a large increase in net isochronous distortion. See *Figure 16* for a graphic illustration of this effect. In the interest of conservative design practices, systems should always be designed with less than 5% transition spread in the eye pattern. This allows the detrimental effects due to bias to be minimized, thus simplifying construction of line drivers and receivers.

OTHER PULSE CODES AND SIGNAL QUALITY

In the preceding sections, the discussion of signal quality has been centered around the use of NRZ signaling, becuase it represents the simplest and most commonly used pulse code. Other pulse codes have been developed which provide one or more of the following desirable features:

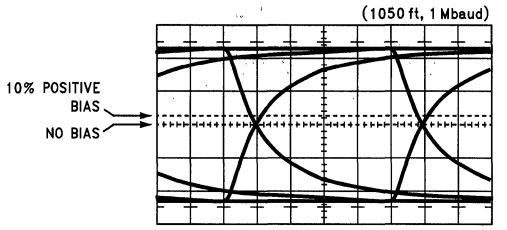
- Compress the overall bandwidth normally required to adequately transmit the signal yet still ensure recovery of the binary data.
- Eliminate the need for a dc response in the transmission medium so that transformer coupling can be used for phantom power distribution on repeated lines. (The elimination of a dc characteristic of the pulse code also allows ac coupling of amplifier circuits).
- Provide a clocking scheme within the signal so that no separate clock channel is required for synchronization.
- Provide built-in error detection.

The following discussion is restricted to the binary class of baseband signals. This simply means that each decision by the line receiver yields one bit of information. The *M*-ary schemes ($M \geq 3$) can encode more than one bit of information per receiver decision*, but these schemes are seldom applied to baseband signaling due to the complexities of the driver and receiver circuits (especially for $M > 3$). *M*-ary schemes, however, are applied to high speed non-baseband data transmission systems using modems. The price to be paid for the increased bit-packing with multi-level signaling is decreased immunity to noise relative to a binary system. This is because a smaller relative threshold displacement (or amount of noise) is required to produce a signal representing another logic state in the *M*-ary schemes.

* It can be shown that, for *M* levels, the information per receiver decision will be $S = \log_2 M$ bits/decision. Thus, three levels theoretically yield 1.58 bits; four levels yield 2 bits of information, eight levels yield 3 bits, etc.

In general, the binary class of pulse codes can be grouped into four categories:

- Non-Return to Zero (NRZ)
- Return to Zero (RZ)
- Phase Encoded (PE) (sometimes called Split Phase)
- Multi-Level Binary (MLB). (The MLB scheme uses three levels to convey the binary data, but each decision by the line receiver yields only one bit of information.)



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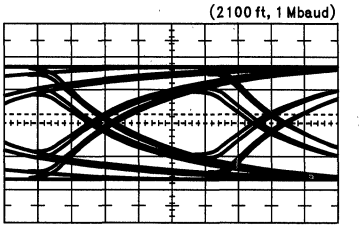

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$$\text{ISOCHRONOUS DISTORTION (ID)} = \frac{t_{tcs}}{t_{ui}} \times 100\%$$

BIAS	1050 ft	2100 ft
0%	5% ID	20% ID
10%	12% ID	36% ID

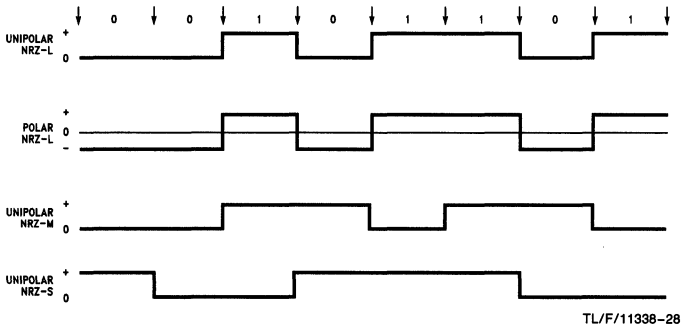
FIGURE 16. Receiver Bias Effect on Total Isochronous Distortion

A secondary differentiation among the pulse codes in concerned with the algebraic signs of the signal levels. If the signal levels have the same algebraic sign for their voltages (or currents) and differ only in their magnitudes, the signaling is called *unipolar*. A very common example of unipolar signaling is TTL or ECL logic. TTL uses two positive voltages to represent its logic states, while ECL uses two negative voltages for its logic states. The complement of unipolar signaling is *polar* signaling. Here, one logic state is represented by a signal voltage or current having a positive sign and the other logic state is represented by a signal with a negative sign. For binary signals, the magnitude of both signals should be equal, ideally. Their only difference should be in the algebraic signs. This allows the receiver to use ground as its decision thershold reference.

Non-Return to Zero (NRZ) Pulse Codes

There are three NRZ pulse codes: NRZ-Level (NRZ-L), NRZ-Mark (NRZ-M), and NRZ-Space (NRZ-S). NRZ-L is the same pulse code as previously discussed. In NRZ-L signaling, data is represented by a constant signal level during the bit time interval, with one signal level corresponding to one logic state, and the other signal level corresponding to the opposite logic state. In NRZ-M or NRZ-S signaling, however, a change in signal level at the start of a bit interval corresponds to one logic state and no change in signal level at the start of a bit interval corresponds to the opposite logic state. For NRZ-M pulse codes, a change in signal level at the start of the bit interval indicates a logic One (Mark), while no change in signal level indicates a logic Zero (Space). NRZ-S is a logical complement to NRZ-M. A change in signal level means a logic Zero and no change means logic One. With NRZ-M and NRZ-S pulse codes, therefore, there is no direct correspondence between signal levels and logic states as there is with NRZ-L signaling. Any of the NRZ pulse codes may, of course, be used in unipolar or polar form. The NRZ codes are shown in *Figure 17*, along with their generation algorithm*, signal levels vs time, and their general power density spectrum.

* The generation algorithm showing the sequence of signal levels on the line, represented by the set $\{b_n\}$, is determined by the sequence of input logic states, represented by the set $\{a_n\}$. See Bennet[14] for detailed usage of this notation.



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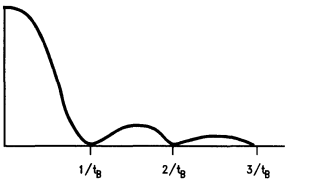

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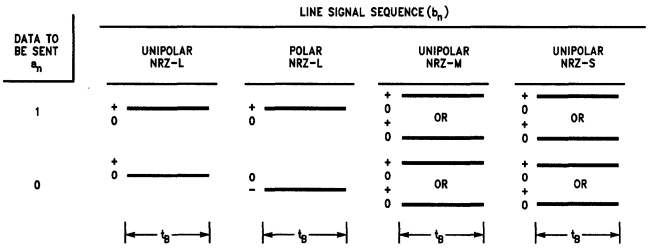
GENERAL POWER SPECTRUM FOR NRZ CODES



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t_{ui}	t_B	t_B	t_B	t_B
$a_n = 1$	$b_n = +$	$b_n = +$	$b_n = (-)\, b_n - 1$	$b_n = b_n - 1$
$a_n = 0$	$b_n = 0$	$b_n = -$	$b_n = b_n - 1$	$b_n = (-)b_n - 1$

FIGURE 17. Non-Return to Zero (NRZ) Pulse Codes

The degradation in signal quality caused by intersymbol interference for NRZ-L signaling was discussed earlier. Since the minimum signaling element (unit interval) for all three NRZ pulse codes is equal to t_B, the previous signal quality discussion for NRZ-L also applies equally to NRZ-M and NRZ-S pulse codes. The following is a capsule summary of the previous discussion on NRZ signal quality.

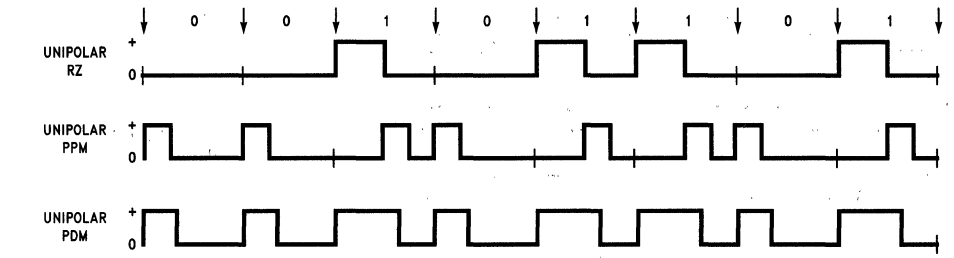
- When t_B is less than the 0%–50% rise or fall time of the signal at the line end, the open space in the eye pattern closes, thereby indicating error-free data transmission is unlikely.
- When t_B is less than the 10%–90% rise or fall time of the line end signal, some intersymbol interference is present and thus, some time jitter in the transitions of the recovered data will be present.

NRZ codes are simple to generate and decode because no precoding or special treatment is required. This simplicity makes them probably the most widely used pulse codes, with NRZ-L the leader by far. NRZ-M has been widely used in digital magnetic recording where it is usually called NRZI for Non-Return to Zero, Invert-on-Ones. In terms of the four desirable features for a pulse code listed at the start of this section, however, non of the NRZ codes are all that great—NRZ codes do possess a strong dc component, and have neither intrinsic clocking, nor error detection features. Even so, their power frequency spectra are used as references for comparison with other pulse codes.

Return to Zero (RZ) Pulse Codes

The RZ group of pulse codes are usually simple combinations of NRZL data and its associated single or double frequency clock. By combining the clock with data, all RZ codes possess some intrinsic synchronization feature. Three representative RZ pulse codes are shown in *Figure 18*. Unipolar RZ is formed by performing a logic AND between the NRZ-L data and its clock. Thus a logic Zero is represented by the absence of a pulse during the bit time interval, and a logic One is represented by a pulse as shown. Pulse Position Modulation (PPM) uses a pulse of $t_B/4$ duration beginning at the start of the bit interval to indicate a logic Zero, and a $t_B/4$ pulse beginning at the middle of the bit interval to indicate a logic One. Pulse Duration Modulation (PDM) uses a $t_B/3$ duration pulse for a logic Zero and a $(\frac{2}{3})$ t_B pulse for a logic One, with the rising edge of both pulses coinciding with the start of the bit interval. PDM with $t_B/4$ pulse widths is also used but better results are usually obtained with the $t_B/3$, 2 $t_B/3$ scheme.

The reason for differentiating between information rate and modulation rate can now be further clarified. Each of the RZ pulse codes in *Figure 18* has the same information rate; i.e., $1/t_B$ bits per second. Their respective minimum signaling elements (unit intervals) however, are all less than t_B so the *modulation rate* for the RZ pulse code is greater than the *information rate*. Remember that with NRZ signaling, the



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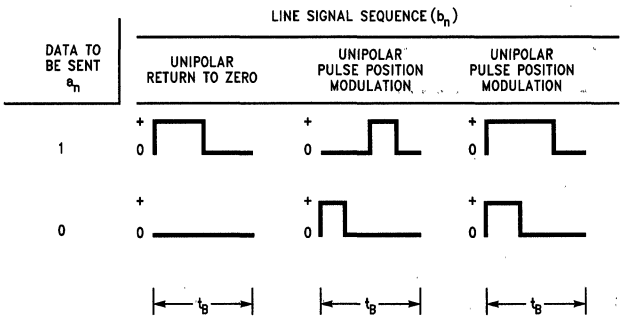

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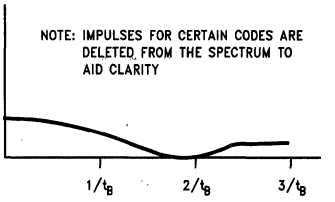

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GENERAL POWER SPECTRUM FOR RZ CODES

t_{ui}	$t_B/2$	$t_B/4$	$t_B/3$
$a_n = 1$	$b_n = (+)\ \{0 \le t < t_B/2$ $b_n = (0)\ \{t_B/2 \le t < t_B$	$b_n = (+)\ \{t_B/2 \le t \le 3t_B/4$ $b_n = (0)\ \begin{cases} 0 \le t < t_B/2 \\ 3t_B/4 < t < t_B \end{cases}$	$b_n = (+)\ \{0 \le t \le 2t_B/3$ $b_n = (0)\ \{2t_B/3 \le t < t_B$
$a_n = 0$	$b_n = (0)$	$b_n = (+)\ \{0 \le t \le t_B/4$ $b_n = (0)\ \{t_B/4 < t < t_B$	$b_n = (+)\{0 \le t \le t_B/3$ $b_n = (0)\{t_B/3 \le t_B$

FIGURE 18. Return to Zero (RZ) Pulse Codes

unit interval and the bit time interval are equal in duration, so the information rate in bps is equal to the modulation rate in bauds. For isochronous NRZ signaling, the measures bps and baud are both synonymous and interchangeable.

Inspection of unipolar RZ signaling reveals that the unit interval is ½ bit interval ($t_{ui} = t_B/2$). When this unit interval is less than the 0%–50% rise or fall time of the line, the data is likely to be unrecoverable. With a fixed modulation rate, the price paid to include clocking information into unipolar RZ is reduced information rate over that for NRZ signaling. Likewise, for PPM with its unit interval of $t_B/4$, the information rate reduces to ¼ that of NRZ data under the same conditions. This is because the maximum modulation rate is determined by the 50% rise time of the line which is constant for a given length and type of line. PDM has a unit interval of $t_B/3$ so, for a given maximum modulation rate, the resulting information rate is ⅓ that of NRZ data.

The preceding argument should not be taken as strictly correct—since the actual intersymbol interference patterns for the three RZ codes discussed differ somewhat from the pattern with NRZ codes. A random sequence of NRZ data can easily consist of a long sequence of Zeros followed by a single One and then a long sequence of Zeros, so the $t_{50\%}$ limit can be accurately applied. Unipolar RZ, in response to the same long data sequence, produces a $t_B/2$ pulse, so the $t_{50\%}$ argument can be applied here too. With PPM and PDM, the maximum time that the line signal can be in one state is quite reduced from the NRZ case. For PPM, this time is 1.25 t_B (010 data sequence) while for PDM, it is 0.67 t_B (see *Figure 18*). With PPM and PDM, then, the line signal may never reach the final signal levels that it does with NRZ data. So, the PPM and PDM signals have a head start, so to speak, in reaching the threshold crossing of the receiver. Because of the reduced time that PDM and PPM signal levels are allowed to remain at one signal level, their signaling may still operate at a modulation rate slightly above that where the NRZ data shows 100% transition jitter. Even with this slight correction to the previous discussion, the RZ group of pulse codes still sacrifice information rate in return for synchronization. The PPM scheme appears to be a poor trade in this respect, since PDM allows a greater information rate while retaining the self-clocking feature. Unipolar RZ, because it provides no clocking for a logic Zero signal, is not generally as useful as PDM for baseband data transmission. However, unipolar RZ is used in older digital magnetic tape recorders.

Examination of RZ codes shows only one more desirable feature than NRZ codes: clocking. RZ codes still have a dc component in their power density spectrum *(Figure 18)* and their bandwidth is extended (first null at $2/t_B$) over that of NRZ (first null $1/t_B$). RZ codes do not have any intrinsic error detection features.

Phase Encoded (PE) Pulse Codes

The PE group of pulse codes uses signal level transitions to carry both binary data and synchronization information. Each of the codes provides at least one signal level transition per bit interval aiding synchronous recovery of the binary data. Simply stated, Biphase-Level (Biϕ-L) code is binary phase shift keying (PSK) and is the result of an Exclusive-OR logic function performed on the NRZ-L data and its clock; it is further required that the resultant signal be phase coherent (i.e., no glitches). Biphase—Mark (Biϕ-M) and Biphase-Space (Biϕ-S) codes are essentially phase coherent, binary frequency shift keying (FSK). In Biϕ-M, a logic One is represented by a constant level during the bit interval (one-half cycle of the lower frequency $1/(2\ t_B)$, while a logic Zero is represented by one-half cycle of the higher frequency $1/t_B$. In Biϕ-S, the logic states are reversed from those in Biϕ-M. Another way of thinking of Biϕ-M or Biϕ-S is as follows.

- Change signal level at the end of each bit interval regardless of the logic state of the data.
- Change signal level at the middle of each bit interval to mean a particular logic state.

In Biϕ-M (sometimes call diphase), a mid-bit interval change in signal level indicates a logic One (Mark), while no change indicates a logic Zero. For Biϕ-S, no signal level change in the middle of the bit interval means a logic One, while a change means a logic Zero.

In Biϕ-L (also called Manchester Code), a positive-going transition at the middle of the bit interval means a logic Zero, while a negative-going transition there indicates a logic One.

The fourth member of the PE family is Delay Modulation (DM)[15, 16] sometimes referred to as Miller code. Here logic One is represented by a mid-bit interval signal level change, and a logic Zero is represented by a signal level change at the end of the bit interval if the logic Zero is followed by another logic Zero. If the logic Zero is immediately followed by a logic One, no signal level transition at the end of the first bit interval is used. The waveforms encoding algorithms, and general power density spectra for the PE pulse code family are shown in *Figure 19*.

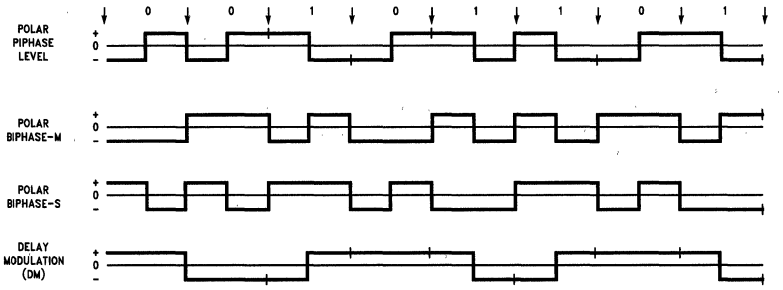
* Delay Modulation[15, 16] has a maximmum of 2 t_B without a signal level transition.

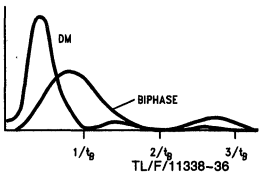
A brief inspection of the signal waveforms for the three Biphase pulse codes reveals that their minimum signaling element has a duration of one-half bit interval ($t_{ui} = t_B/2$); the longest duration of either signal level is one bit interval. Similarly, DM is seen to have a minimum signaling element of one bit interval ($t_{ui} = t_B$) and the maximum duration of either signal level is two bit intervals (produced by a 101 pattern). Biphase codes should exhibit eye closure (they would not be recoverable without equalization) when $t_{ui} \leq t_{0\%-50\%}$. So, a 50% jitter on NRZ signaling approximately corresponds to the Biphase codes non-operation point. Biphase codes, therefore, provide one-half the information rate of NRZ signals at a given maximum modulation rate. This is in exchange for synchronization information and a dc-free spectrum when used in polar form.

DM should have essentially the same intersymbol interference characteristics as NRZ, since the unit interval is the same for both codes. DM may perform slightly better than NRZ, because the maximum duration of either signal level is two bit intervals. Overall, DM is better coding scheme than the Biϕ. It does not require as much bandwidth as Biϕ and still possesses the desirable dc response and synchronization qualities.

Both Biϕ and DM are good choices for digital magnetic recording[16]; Biϕ is widely used in disc memory equipment, and DM is rapidly gaining acceptance where high bit packing densities are desired. Overall scoring, in terms of the four desirable characteristics, shows the PE pulse codes with three primary features; bandwidth compression, no dc, and intrinsic synchronization.

Th Biϕ family does not possess any intrinsic error detection scheme. DM does possess the capability of detecting some—but not all—single bit errors. This detection process is accomplished by checking to see if a single level persists longer than two bit intervals, in which case, an error is indicated. DM detection requires two samples per bit interval.

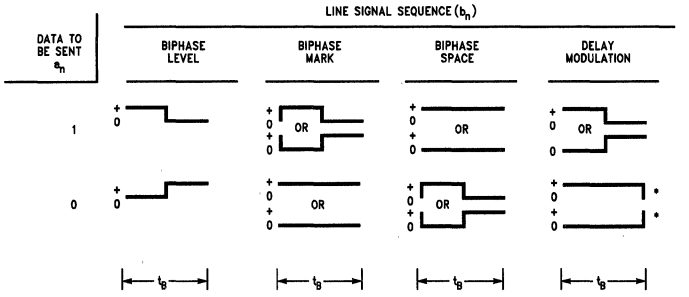




TL/F/11338–36

GENERAL POWER SPECTRUM FOR SPLIT PHASE CODES

TL/F/11338–34



*Transition only if followed by another "0" ($a_{k+1} = 0$)

TL/F/11338–35

t_{ui}	$t_B/2$	t_B2	$t_B/2$	t_B
$a_n = 1$	$b_n = (+)\{0 < t < t_B/2$ $b_n = (-)\{t_B/2 \le t \le t_B$	‡	$b_n = (-)\, b_{n-1}$* *complement of final level of last b_n	if final value of $b_{n-1} = (+)$ then $b_n = (+)\{0 < t < t_B/2$ and $b_n = (-)\{t_B/2 \le t \le t_B$ else, compliment above b_n values for times shown
$a_n = 0$	$b_n = (-)\{0 < t < t_B/2$ $b_n = (+)\{t_B/2 \le t \le t_B$	$b_n = (-)\, b_{n-1}$* *complement of final level of last b_n	‡	if final value of $b_{n-1} = (+)$ then $b_n = (+)\{0 \le t < t_B$ if $a_{n+1} = (0)$ then $b_n = (-)\{t = t_B$ else $b_n = (+)\{t = t_B$ if final value of $b_{n-1} = (-)$ then complement b_n values above

‡ If b_{n-1} final level = (+), then $\begin{cases} b_n = (-)\{0 \le t < t_B/2 \\ b_n = (+)\{t_B/2 \le t < t_B \end{cases}$

If b_{n-1} final level = (−), then $\begin{cases} b_n = (+)\{0 \le t < t_B/2 \\ b_n = (-)\{t_B/2 \le t < t_B \end{cases}$

FIGURE 19. Phase Encoded (PE) Pulse Codes

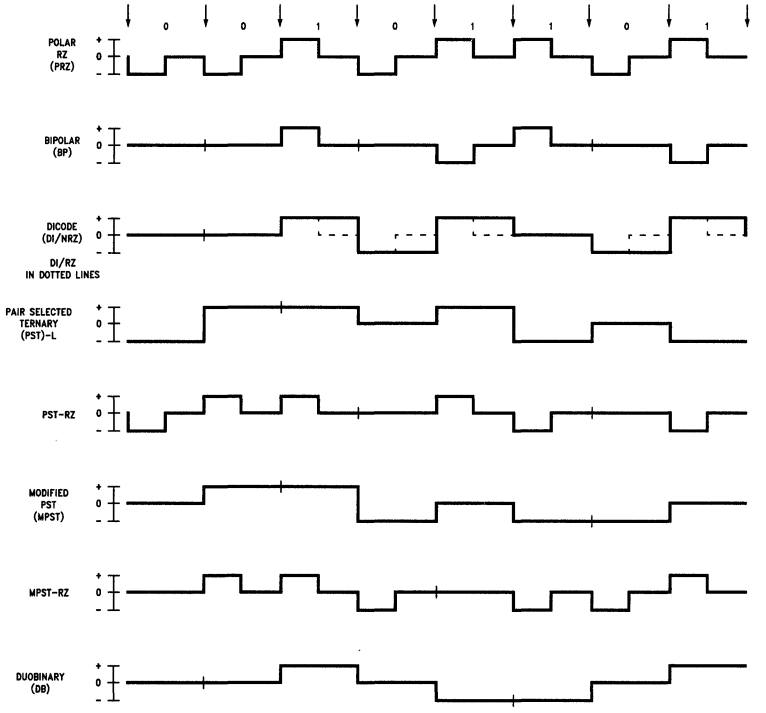
Multi-Level Binary (PLB) Pulse Codes

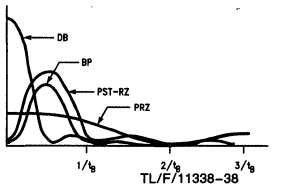
The pulse codes in the MLB groupd discussed have a common characteristic of using three signal levels (expressed in shofthand notation as +, 0, −) to represent the binary information, but each receiver decision yields only one bit of information. These are sometimes called *pseudoternary* codes to distinguish them from true ternary codes wherein each receiver decision can yield 1.58 information bits.

The most straightforward pulse code in the MLB group is polar RZ *(Figure 20)*. Some authors place PRZ in the RZ group, but since PRZ uses three signal levels, it is placed in the MLB group here. A logic One is represented by a positive polarity pulse, and a logic Zero is represented by a negative polarity pulse. Each pulse lasts for one-half bit interval. PRZ has excellent synchronization properties since there is a pulse present during every bit interval.

Bipolar (BP)[17, 18] uses a $t_B/2$ duration pulse to signify a logic One, and no pulse during the bit interval to signify a logic Zero. The polarity of the pulses for a logic One is alternated as shown in *Figure 20*. Bipolar coding is also known as Alternate Mark Inversion. BP is widely used in Bell Systems T1–PCM carrier systems as a pulse code transmitted along a regenerative repeated transmission line. Since BP has no dc component, the regenerative repeaters along the span line may be transformer coupled and powered by a phantom constant current power loop from the central office. The synchronization properties of BP are excellent if the number of Zero bits transmitted in series is constrained. This constraint on the number of sequential Zeros allows clock circuits in each repeater to remain in synchronization. A scheme called Binary with 6 Zeros Substitution (B6ZS) was developed to replace 6 Zeros with a given signal sequence to offset this loss of synchronization[18]. Bipolar coding has a limited capability to detect single errors, all odd errors, and certain even error combinations which violate the mark alternation rule. Another scheme called High Density Bipolar with 3 Zeros substitution (HDB-3) replaces four successive Zeros (no pulses) with three Zeros followed by a pulse whose polarity violates the Mark alternation rule[19]. Subsequent detection of this pattern (three Zeros and pulse violating the polarity coding rule) causes the receiver to substitute four Zeros for the received 0001 pattern.

In Dicode (DI)[20, 21], a polar pulse (either t_B for DI-NRZ or $t_B/2$ for DI-RZ) is sent for every input data transition. The limiting constraint is that the successive pulses must alternate in sign *(Figure 19)*. As in NRZ-M and NRZ-S, the actual polarity of the pulses does not necessarily correspond to





TL/F/11338–38

GENERAL POWER DENSITY SPECTRUM
RANDOM SEQUENCE P(0) = P(1) = 0.5

TL/F/11338–37

FIGURE 20. Multilevel Binary (MLB) or Pseudoternary Pulse Codes

the logic state of the data (a positive pulse may represent either a Zero-to-One or a One-to-Zero transition of the input data). The power spectrum for DI is the same as for BP (no dc component). Bit synchronization for DI can be obtained in the same manner as for BP, but with DI, the number of bits of the same logic state must be controlled in order for the receiver to maintain bit synchronization. DI also has the intrinsic capability of detecting single bit errors (via two successive positive or negative signal levels), all odd, and some even numbers of errors.

Pair Selected Ternary (PST)[18, 22] and Modified PST (MPST)[22] were proposed to minimize the disadvantages of BP coding: loss of synchronization with long strings of Zeros and timing jitter. PST/MPST maintains the strong features of BP: dc free spectrum, single error detection. To produce PST or MPST, the incoming bits are grouped into pairs, and the signal produced on the line is governed by a coding table. Two modes are also used in the coding table with a change in mode occurring after a certain bit pair is transmitted. The features of PST/MPST thus include:

- No dc spectral component,
- No loss of synchronization with long strings of Zeros,
- Intrinsic error detection,
- Simplification of requirements for timing extraction circuits with respect to BP.

MPST coding was developed primarily to speed up the framing process, i.e., selecting which two successive pulses constitute a valid pair, when the probability for a Zero and a One are not equal.

Duobinary[23, 24] is an example of a correlative level coding technique, wherein a correlation exists between successive signal levels. Duobinary uses three signal levels with the middle level corresponding to a logic Zero, and the other two levels corresponding to a logic One. The pseudoternary signal is generated by precoding the input data, which results in constraining the line signal to change only to the neighboring level, i.e., the (+) to (−) and (−) to (+) level changes are not allowed. This precoding process uses controlled intersymbol interference as part of the coding scheme. The benefit is an effective doubling of the bit rate for a given bandwidth and concentration of the power spectrum toward dc *(Figure 20).* Duobinary has the capability to detect single errors which violate the encoding rules. In terms of bandwidth utilization, Duobinary ranks first among all the binary and MLB codes[20], but its strong dc component prohibits the use of ac-coupled transmission media. Synchronization properties are similar to NRZ, thus external clocking must be used to recover the data.

REFERENCES

1. N.S. Nahman and R.L. Wigington; "Transient Analysis of Coaxial Cables Considering Skin Effect", *IRE Proceedings,* Vol. 45, Feb. 1957, pp. 166–174.
2. N.S. Nahman; "A Discussion on the Transient Analysis of Coaxial Cables Considering High Frequency Losses", *IRE Transactions on Circuit Theory,* Vol. CT-9, No. 2, June 1962, pp. 144–152.
3. N.S. Nahman and D.R. Holt; "Transient Analysis of Coaxial Cables Using the Skin Effect Approximation $A + B\sqrt{s}$", *IEEE Transactions on Circuit Theory,* Vol. 19, No. 5, Sept. 1972, pp. 443–451.
4. N.S. Nahman; "A Note on the Transition (Rise) Time Versus Line Length in Coaxial Cables", *IEEE Transactions on Circuit Theory* (correspondence), Vol. CT-20, No. 2, Mar. 1973, pp. 165–167.
5. R.E. Matick; *Transmission Lines for Digital and Communications Networks,* McGraw Hill, New York, 1969.
6. G. Metzger and J.P. Vabre; *Transmission Lines with Pulse Excitation,* Academic Press, New York, 1969.
7. J.T. Kolias; "Interconnection Delays", *Digital Design,* June 1973, pp. 40–45.
8. F. Kirsten; "Pulse Response of Coaxial Cables", *Counting Handbook* (UCRL 3307 Rev.), CC2-1, Lawrence Radiation Laboratory, Jan. 1959.
9. P.C. Magnusson; "Transient Wavefronts on Lossy Transmission Lines—Effect of Source Resistance", *IEEE Transactions on Circuit Theory* (correspondence), Vol. CT-15, Sept. 1968, pp. 290–292.
10. G.L. Turin; "Steady-State and Transient Analysis of Lossy Coaxial Cables", *IRE Proceedings* (correspondence), Vol. 45, June 1957, pp. 878–879.
11. A.H.M. Arnold; "Proximity Effect in Solid and Hollow Round Conductors", *Journal IEE* (London), Vol. 88, pt. II, August 1941, pp. 349–359.
12. H.B. Dwight; "Proximity Effect in Wires and Thin Tubes", *AIEE Transactions,* Vol. 42, Sept. 1923, pp. 961–970.
13. *Standard Wire and Cable Co., Catalog,* Third Edition, Mar. 1971, pp. 62–74.
14. W.R. Bennet; *Introduction to Signal Transmission,* McGraw Hill, New York, 1970.
15. M. Hecht and A. Guida; "Delay Modulation", *Proceedings of IEEE* (letters), Vol. 57, No. 1, July 1969; pp. 1314–1316.
16. A.E. Whitehouse and L.E.M. Warburton; "Information Coding on Magnetic Drums and Discs", *IEE (London), Conference on Computer Science and Technology,* 1969, Pub. No. 55, pp. 237–245.
17. J.S. Mayo; "Pulse Code Modulation", *Electro-Technology,* Nov. 1962, pp. 88–98.
18. *Transmission Systems for Communications,* Bell Telephone Labs., 4th ed., Feb. 1970, Chapter 27, pp. 626–638.
19. J.V. Martens and E. Brading; "30-Channel Pulse Code Modulation System", *ITT Electrical Communication,* Vol. 48, No. 1 and 2, 1973, pp. 11.69–78.
20. R.C. Houts, T.A. Green; "A Comparative Analysis of Digital Baseband Signals", *Technical Report 146–102,* Communications Systems Group, Bureau of Engineering Research, University of Alabama, June 1972.
21. R.C. Houts and T.A. Green; "Comparing Bandwidth Requirements for Binary Baseband Signals", *IEEE Transactions on Communication Technology,* (correspondence) Vol. COM-21, No. 6, June 1973, pp. 776–781.
22. J.M. Sipress; "A New Class of Selected Ternary Pulse Transmission Plans for Digital Transmission Lines", *IEEE Transactions on Communication Technology,* Vol. 13, No. 3, Sept. 1965, pp. 366–372.
23. A. Lender; "The Duobinary Technique for High Speed Data Transmission", *IEEE Transactions on Communication Electronics,* No. 66, May 1963, pp. 214–218.
24. A. Sekey; "An Analysis of the Duobinary Technique", *IEEE Transactions on Communication Technology,* Vol. COM-14, No. 2, Apr. 1966, pp. 126–130.
25. G.S. Eager (et. al); "Transmission Properties of Polyethylene Insulated Cables at Voice and Carrier Frequencies", *AIEE Transactions on Communications Electronics,* Nov. 1959, pp. 618–640.

FAILSAFE Biasing of Differential Buses

National Semiconductor
Application Note 847
John Goldie

OVERVIEW

Multi-Point bus configurations present two potential problems to the system I/O designer that do not commonly occur in Point-to-Point configurations. The two problems that the I/O system designer should take into account are bus contentions and the idle bus state. Bus contention occurs when more than one driver is active at a time during which the state of the bus is undetermined. Contentions may occur either by software or hardware errors. The second problem is an unknown bus state when all drivers are OFF. FAILSAFE biasing solves this problem by biasing the bus to a known state when ALL drivers are in TRI-STATE® (OFF). This application note is devoted to the topic of FAILSAFE biasing of differential buses.

INTRODUCTION

FAILSAFE biasing provides a known state when all drivers are in TRI-STATE (Hi-Z, OFF). This is especially important in bus configurations that employ more than one driver (transceiver), and is commonly known as a Multi-Point application (see *Figure 1*).

Electrical Characteristics Standard TIA/EIA-485 specifies that a maximum of 32 unit loads can be connected to a bus. A transceiver (driver/receiver pair) normally represents one unit load (see *Figure 1*). The bus is a half duplex bi-directional bus, (as data can flow in both directions), but only one driver should be active at a time. Termination is required (in most cases), and is only located at the two extreme ends of the bus. Note, that the termination shown on the left of *Figure 1* also provides a FAILSAFE bias.

BUS STATES

A FAILSAFE biased bus has only two states, HIGH (driven HIGH and FAILSAFE HIGH) and LOW (neglecting the transition region, and bus contentions). The bus can be driven HIGH or LOW by an active driver, or biased to a known state by external pull up and pull down resistors. These resistors provide the FAILSAFE bias, and the termination configuration is also known as a "power termination". The two bus states are shown in *Figure 2*.

In some applications these two states are defined as MARK/SPACE, OFF/ON, or 1/0. The definition of the two states is application dependent. When the signal transitions through the threshold region (±200 mV) the output state of the receiver is undefined. In *Figure 2*, the line is driven LOW, transitions HIGH, then the driver is disabled. The bus however, remains HIGH due to external FAILSAFE biasing.

Without FAILSAFE biasing, the receiver output would be undetermined when all drivers are OFF. The line would settle to only 1 mV–5 mV of each other ($|V_{OA}-V_{OB}|$, due to the internal input impedance network of the receiver), which is within the receiver's threshold limits (≤200 mV). If external noise is coupled onto the line, a false transition could occur, causing an error. In an asynchronous application, this false transition could be interpreted as a framing error, false start bit, or cause a false interrupt.

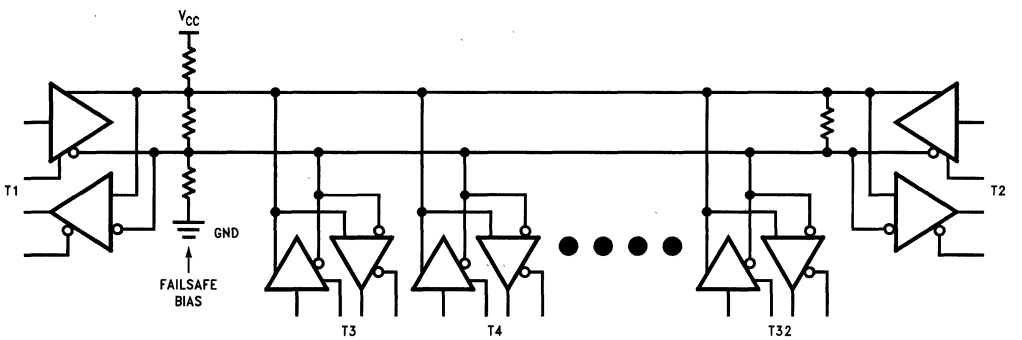


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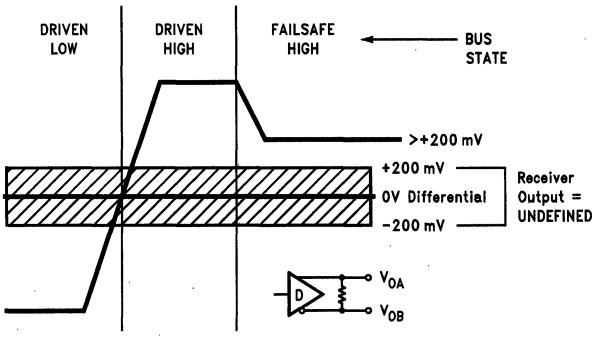
FIGURE 1. Typical Multi-Point Application



Note: Differential Plot $V_{OA} - V_{OB}$, not with respect to GND.

FIGURE 2. Bus States

SERIAL PROTOCOL

A popular format for low speed data transmission is an asynchronous protocol. A typical format is composed of 12 bits. The start bit initiates the timing sequence. This is detected by a transition from HIGH to LOW. Next are eight data bits, followed by an optional parity bit. Lastly, the line is driven HIGH for one or two bits (stop bits), signifying the end of the character. This format is illustrated in *Figure 3*. If another character is to be sent, the next start bit initiates the whole process all over again. However, if this was the last character, the line should remain HIGH until the next start bit, but the active driver is disabled. This presents a problem in multi-point applications, because between data transmissions all drivers are OFF. With no active drivers, the line is floating, and receiver outputs are undetermined. There are several solutions to this problem. One is through the use of alternate protocols (software), while the other is a hardware fix. The hardware fix uses external resistors to bias the line HIGH, when all drivers are off. The remainder of the application note describes the hardware method and the selection of component values.

In a Point-to-Point application (see *Figure 4*), the driver is normally always enabled. In this case the bus has only two states, driven HIGH, and driven LOW. FAILSAFE biasing is not needed, unless the drivers's enabling pin is also switched.

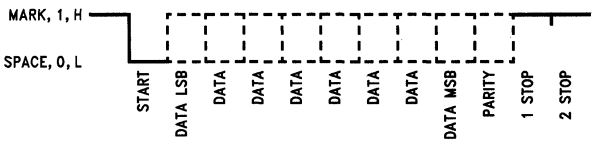


FIGURE 3. Asynchronous-UART Timing Format

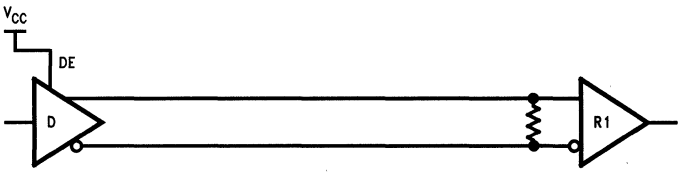


FIGURE 4. Typical Point-to-Point Application

CALCULATING RESISTOR VALUES FOR FAILSAFE BIASING

The external resistors are selected such that they provide at least a 200 mV (maximum receiver threshold) bias across the line, and not substantially load down the active driver.

In addition, the following guidelines should be met. The pull up resistor (Ra) and the pull down resistor (Rd) should be of equal value. This provides symmetrical loading for the driver. Termination resistor Rb should be selected such that it matches the characteristic impedance (Z_O) of the twisted pair cable. If the termination resistor matches the line, Rb = Z_O, there will be no reflections. At the other end of the cable, the equivalent resistance of Rc, Ra and Rd should also match the characteristic impedance of the line. In this case Rc is in parallel with Ra plus Rd (Rc//(Ra + Rd)). For this equivalent resistance to be matched to the line Rc must be greater than Z_O. Rc is typically 10Ω–20Ω greater than Z_O, but the actual value depends upon the values Ra and Rd. The FAILSAFE bias (Vfsb) is the potential dropped across the line. Note that this equation neglects cable resistance (see appendix), and that Rb is in parallel with Rc (Req = Rb // Rc). Therefore, the FAILSAFE bias is simply a voltage divider between Req, Ra, and Rd. The worst case occurs at V_{CC} − 5%, Ra and Rd + % tolerance, and Rc and Rb − % tolerance. Under the worst case conditions the FAILSAFE bias must be greater than 200 mV for the receiver output to be in a guaranteed state.

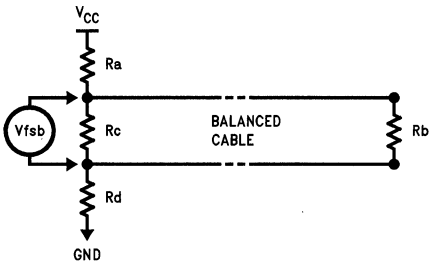


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FIGURE 5. External FAILSAFE Bias Resistors

Example calculations for selecting FAILSAFE bias resistors:

Note: For this example assume the cable has a characteristic impedance (Z_O) of 120Ω.

Step 1 Assume that Rc and Rb are equal and are selected to match Z_O.

$$Rc = Rb = Z_O = 120\Omega$$

Step 2 Calculate the equivalent resistance of Rc//Rb.

$$Rc\ //\ Rb = 120\Omega\ //\ 120\Omega = 60\Omega$$

Step 3 Calculate the Pull up and Pull down resistor values knowing that the FAILSAFE bias is 200 mV, and V_{CC} = 5V.

$V_{fsb} = V_{CC}\,(Req/(Ra + Req + Rd))$

solving for R′ (defined as Ra + Rd)

$R' = ((Req)V_{CC} / V_{fsb}) - Req$

$R' = ((60\Omega)5V/0.2V) - 60\Omega = 1440\Omega$

Since Ra and Rd are equal, Ra = Rd = 1440Ω/2 = 720Ω

Step 4 Recalculate the equivalent resistance of Rc//(Ra + Rd).

$$Rc//(Ra + Rd) = 120\Omega//(720\Omega + 720\Omega) = 110\Omega$$

Since the equivalent resistance is close (within 10%) to the characteristic impedance of the cable (Z_O), no further adjustment of resistor values is required.

However, for the perfectionist, the matched value of Rc can be calculated by setting the following equation to Z_O and solving for Rc.

$$Z_O = Rc\ //\ (Ra + Rd)$$

$$\therefore\ Rc = 131\Omega$$

Now the equivalent resistance (Req = Rc // Rb) becomes 131Ω // 120Ω = 62Ω, which is very close to the original 60Ω. Standard value resistors values can be substituted to ease resistor selection, availability, and cost, before recalculating the FAILSAFE bias potential. Using a 5% tolerance table we find the following standard resistor values:

Ra = 750Ω, Rb = 120Ω, Rc = 130Ω, Rd = 750Ω

In order to verify that the selected values meet the criteria the following calculations should be completed:

1. $Rc//(Ra + Rd) = Z_O$

   $130\Omega//(750\Omega + 750\Omega) = 120\Omega$

2. $Req = Rb//Rc$

   $120\Omega//130\Omega = 62\Omega$

3. $V_{fsb} = V_{CC}\,(Req/(Ra + Req + Rd))$

   $5V(62\Omega/(750\Omega + 62\Omega + 750\Omega)) = 200\ mV$

Based on the example shown above, and a twisted pair cable with characteristic impedance of 120Ω, it has been determined that a 750Ω pull up and pull down resistor will provide a FAILSAFE bias of 200 mV. This value could be decreased slightly to provide a greater bias (>200 mV), and to meet the worst case power supply and resistor tolerance conditions. However, the value of Ra and Rd should not be reduced too low in order to minimize loading seen by the driver. This example illustrated that the largest values used for the pull up (Ra) and pull down (Rd) resistors should be 750Ω. The pull resistors should not be decreased substantially. Because when the driver is active (ON), it is required to develop a minimum of 1.5V across the cable termination. Using low impedance pull resistors further loads down the driver, making the 1.5V differential voltage even more difficult to meet.

Figure 6 illustrates the fully loaded (32 unit loads) TIA/EIA-485 bus with an external FAILSAFE bias network. Note that the FAILSAFE bias (Power Termination) is only located at one end of the bus. The other end employs a single resistor termination. The power termination is commonly located on the Master node of a Master/Slave bus configuration. This assures that the power to the pull up resistor is always on.

Before looking at the driver's load, the receiver's input impedance needs to be modeled to understand its effect upon the driver. The TIA/EIA-485 standard specifies a high receiver input impedance and an Input Voltage vs Input Current curve. An input impedance of 12 kΩ or greater is typically required to meet the V_{IN}/I_{IN} curve. A common mistake is to model the receiver's input impedance as a differential resistance, which is seen between the input pins. The input resistance is correctly modeled as a series resistor to a voltage reference node (AC ground point). The TIA/EIA-485 standard also allows for 32 unit loads to be connected in parallel. Therefore, the driver could see 32 12 kΩ resistors in parallel on each line. This is equivalent to a 375Ω resistor to an internal voltage reference point.

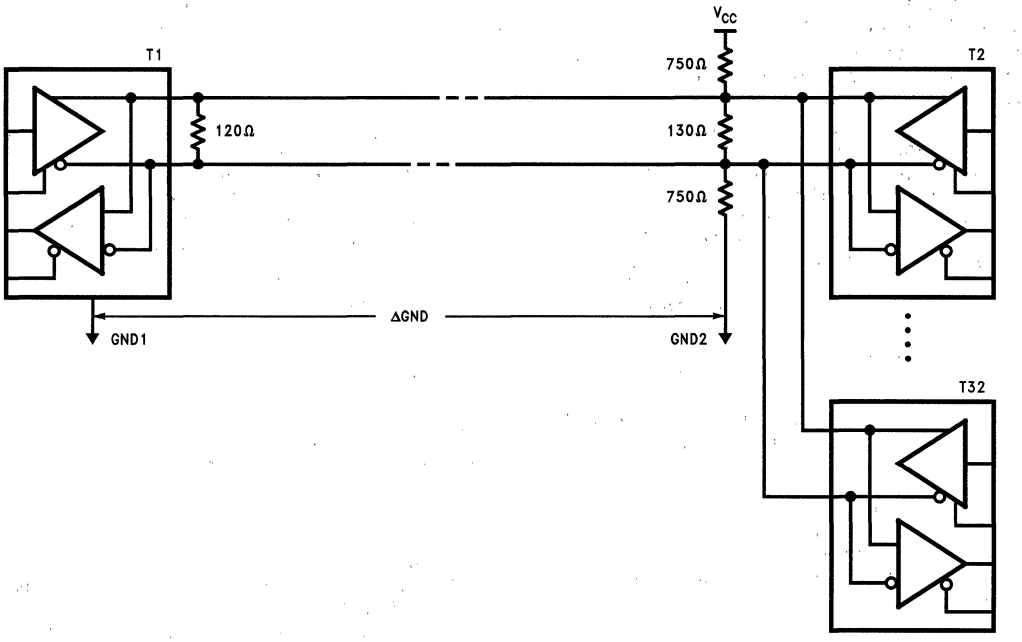

FIGURE 6. Fully Loaded TIA/EIA-485 Bus

The test circuit shown in *Figure 7* models the fully loaded TIA/EIA-485 bus. The 375Ω resistors that model the 32 parallel receiver input impedances, have been changed to 330Ω for two reasons. First, an active driver would also see 31 Tri-stated driver leakage currents (I_{OZ}), which is equivalent to 31 times 100 μA or 3.1 mA. This is equivalent to roughly 3 more unit loads. Therefore, 12 kΩ divided by 35(32 + 3) equals 342Ω. This value is further reduced to 330Ω to select standard value resistors. The dashed box represents 32 receiver loads and 31 passive driver leakage loads. The V_{CM} power supply models the maximum ground shifting specified (allowed) by TIA/EIA-485 (±7V). The differential voltage (VOD), measured across the 62Ω load (120Ω//130Ω), is required to be greater than 1.5V in magnitude by TIA/EIA-485.

Test data taken on three popular National TIA/EIA-485 drivers are shown in Table I. With the common mode voltage varied from −7V to +7V, all of the devices meet the 1.5V minimum differential voltage (VOD column).

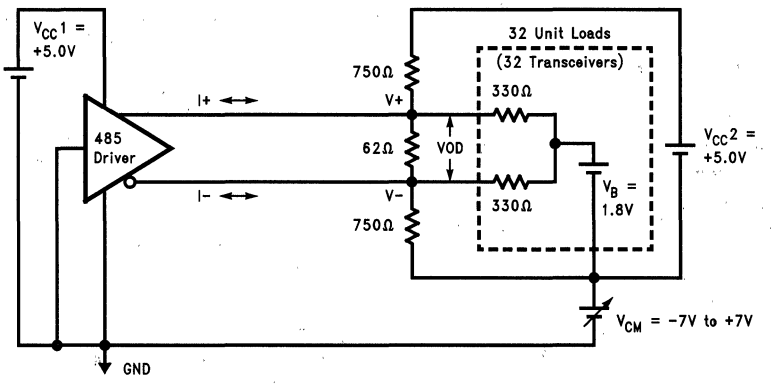

FIGURE 7. Full Load Equivalent Test Circuit

TABLE I. Test Data for TIA/EIA-485 Drivers

Device	V_{CM} (V)	I− (mA)	I+ (mA)	V− (V)	V+ (V)	VOD (V)
DS3695	0	−41.7	+38.4	3.39	1.44	1.95
	−7	−56.1	+23.5	3.18	1.24	1.94
	+7	−13.4	+69.1	3.78	1.77	2.01
DS96172/4	0	−43.4	+42.4	3.25	1.14	2.11
	−7	−59.6	+28.0	3.08	0.94	2.14
	+7	−12.0	+70.4	3.47	1.46	2.01
DS96F172/4	0	−49.5	+45.3	3.67	1.33	2.34
	−7	−63.5	+30.6	3.47	1.14	2.33
	+7	−19.2	+74.2	4.00	1.71	2.29

Note: Current into device pin is defined as positive, current out of device pin is defined as negative, VOD ≥ 1.5V (TIA/EIA-485).

OPEN INPUT FAILSAFE FEATURE

All of National's TIA/EIA-485 receivers support the *OPEN INPUT FAILSAFE* feature. This feature provides a known state (HIGH) on the receiver output for the following cases, which are illustrated in *Figure 8*. The OPEN INPUT FAILSAFE feature is integrated into the input stage of the device. Normally high value (typically 120 kΩ) bias resistors pull the plus input high, and the minus input low. The value is large enough to properly bias the receiver when the inputs are open (non-terminated).

VALID OPEN INPUT CASES:

A. Unterminated Cables—With restrictions on data rate, stub length, and cable length, it is possible to construct an interface without termination resistors. Normally the cable length is very short with respect to the driver's rise time and the reflections that occur die out long before the next transition. For the idle line, the impedance seen acros the receiver input pins is very large (open) and thus the receiver output will be a HIGH state.

B. Unconnected Nodes—In a Multi-Point configuration, up to 32 nodes can be connected to the twisted pair. Termination should only be located at the two extreme ends of the cable. Therefore, if a middle node is disconnected from the cable, the OPEN INPUT FAILSAFE feature will put the receiver output into a stable HIGH state.

C. Unused Channels—If a high integration receiver IC (multichannel) is being used, and all channels are not required, the unused channel(s) inputs can be left as no-connects. The OPEN INPUT FAILSAFE feature will force the unused channel into a stable HIGH state. This prevents the unused channel picking up external noise and oscillating, thereby increasing the power supply current (I_{CC}).

In all three cases, the impedance seen across the receiver input pins is very large or open, (∞) in contrast to a low impedance termination resistor of 150Ω or less. For these cases the receiver output will be HIGH. If the termination resistors were connected across the receiver input pins, then the receiver output is undetermined, unless the bus employs FAILSAFE biasing resistors.

SUMMARY

External FAILSAFE bias resistors can be used to solve the idle line state problem that commonly occurs in Multi-Point applications using asynchronous protocols. This is a well accepted hardware approach to solving the idle line state problem. In fact many complete INTERFACE standards have accepted this method. Examples include the Differential SCSI-1 and 2 (Small Computer System Interface) specifications, as well as the IPI (Intelligent Peripheral Interface) standard. This application note provides guidance to selecting proper resistor values that will provide an adequate FAILSAFE bias (Vfsb) while minimizing the loading effect on the driver.

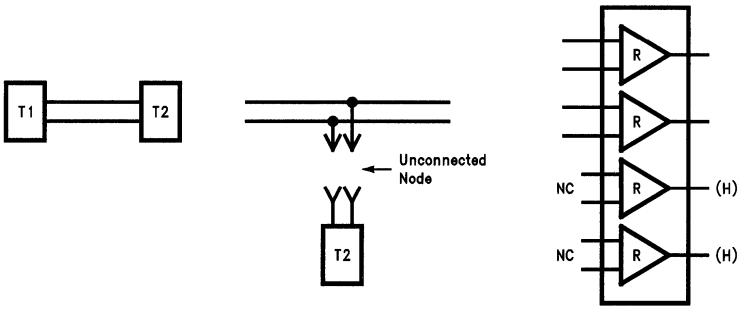

FIGURE 8. Applications of OPEN INPUT FAILSAFE Feature

APPENDIX

A more elaborate calculation that takes into account the DC resistance of the twisted pair cable is provided in this appendix. (See *Figure A-1*). For this example assume the following:

Ra = Pull Up Resistor
Rb = Slave End Cable Termination Resistor
Rc = Master End Cable Termination Resistor
Rd = Pull Down Resistor
Re = Cable DC Resistance
Rf = Cable DC Resistance
Rdcr = Re + Rf
Vfsbm = FAILSAFE Bias Potential @ Master end of cable
Vfsbs = FAILSAFE Bias Potential @ Slave end of cable

and

1. Ra = Rd for symmetrical loading
2. REQ = Rc//(Ra + Rd)
   REQ = (Rc(Ra + Rd))/(Ra + Rc + Rd).

Note A: Assume V_{CC} = 5V ± 5%.

Note B: Resistor Tolerance = ±2%.

Note C: Worst Case occurs at V_{CC} − 5%, Ra and Rd + 2%, Rb and Rc − 2%.

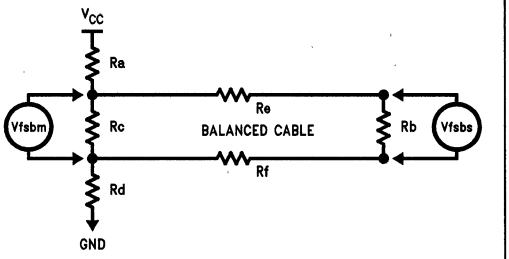

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FIGURE A-1. Cable Model

Equations:

FAILSAFE Bias at the Master end of the cable is:

$$Vfsbm = \frac{Rc//(Rb + Rdcr)}{Ra + Rd + (Rc//(Rb + Rdcr))}V_{CC}$$

$$Vfsbm = \frac{Rc(Rb + Rdcr)}{(Ra + Rd)(Rc + Rb + Rdcr) + Rc(Rb + Rdcr)}V_{CC}$$

The FAILSAFE Bias at the Slave end is simply a voltage divider between the cable DC resistance and the Slave end termination resistor.

$$Vfsbs = \frac{Rb}{Rb + Rdcr}Vfsbm$$

REFERENCES

1. EIA Standard EIA RS-485, Standard for Electrical Characteristics of Generators and Receivers, for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C., 1983.
2. EIA Standard EIA RS-422-A, Electrical Characteristics of Balanced Voltage Digital Interface Circuits, EIA, Washington, D.C., 1978.
3. FAILSAFE Lab Notes, Gary Murdock, National Semiconductor, 1987.

Inter-Operation of the DS14C335 with +5V UARTs

National Semiconductor
Application Note 876
John Goldie
Joe Vo

This application brief describes the inter-operation between the DS14C335 (+3.3V supply TIA/EIA-232 3 x 5 Driver/Receiver) and a +5V UART. The DS14C335, illustrated in *Figure 1,* is ideally suited for notebook and laptop computer applications which either employ one uniform +3.3V supply for all internal components or mixed +3.3V and +5V power supplies. In mixed supply applications, the DS14C335 does NOT require a +5V to +3.3V translator device between it and the UART. This application brief describes how this is accomplished.

Figure 2 illustrates a typical application where the DS14C335 provides the interface between the +5V UART and the RS-232 port. The drivers provide translation from TTL/CMOS voltage levels on the driver input pins to RS-232 compliant driver output voltage levels (>|5V|), while the receivers accept standard RS-232 input levels and translate them back to TTL/CMOS compatible output voltage levels.

Because this application specifies a +5V UART, care must be taken to consider the characteristics of three pins on the DS14C335. They are the:

D_{IN}	Driver Input,
SD	Shutdown,
R_{OUT}	Receiver Output

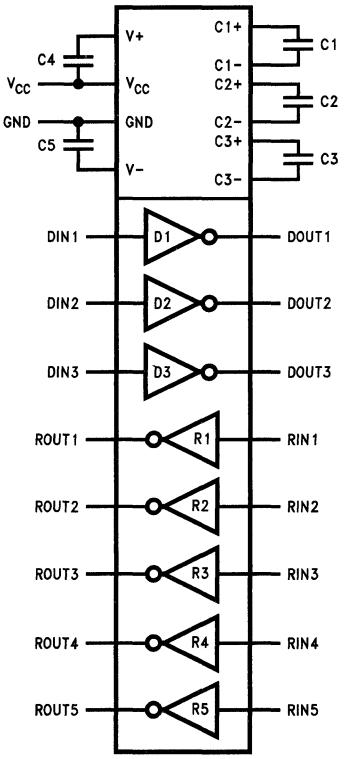

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FIGURE 1. DS14C335 Functional Diagram

14

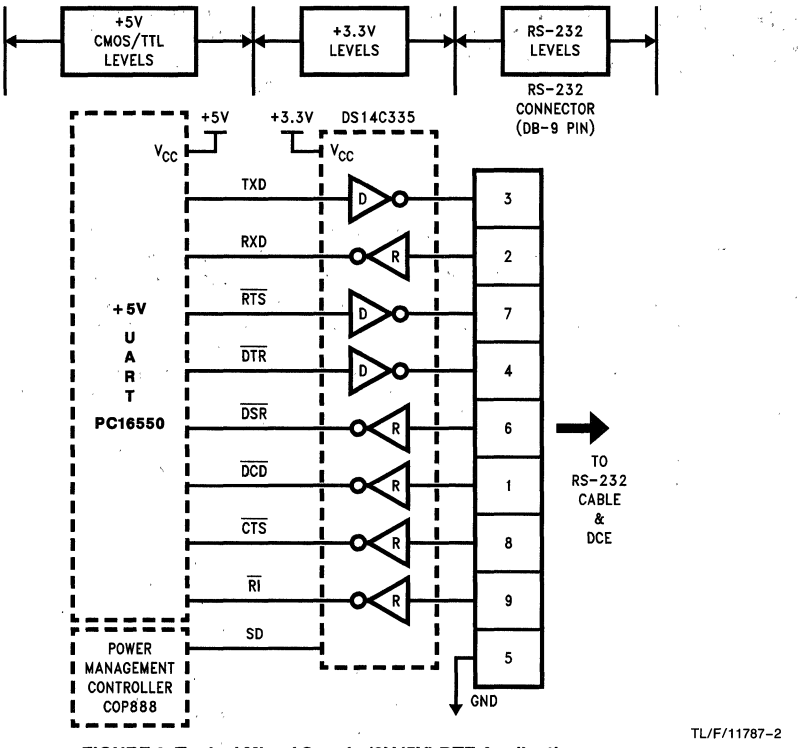

FIGURE 2. Typical Mixed Supply (3V/5V) DTE Application

Let us first examine the input structures of the D_{IN} and SD input pins, as these structures are very similar. The common circuitry is illustrated in *Figure 3* and is composed of two input protection diodes (D1 and D2). In addition, a third diode (D3) exists between the V_{CC} and V+ pins and is normally reversed biased. Diode D1 is situated between the input (D_{IN} or SD) pin and GND to clamp negative input voltages. Diode D2 is situated between the input pin and the V+ pin. When the DS14C335 is active (ON), the V+ pin is typically greater than +9V. External charge pump capacitor C4, holds 6V of charge, and is referenced to the V_{CC} (+3.3V) pin. This creates a potential of greater than +9V on the V+ pin, and is used to power the driver outputs. The input pins (D_{IN} and SD) present standard input current loading to the driving device (UART) since D1 and D2 remain reversed biased between −0.3V and one diode above the V+ pin potential (typically greater than +9V).

The DS14C335 supports another unique feature that allows the CPU to disable the device to save power when RS-232 communication is not required. The DS14C335 is put into shutdown mode, by asserting the SD pin high. This disables the internal charge pump circuit, the drivers, and also 4 of the 5 receivers, droping I_{CC} to typically 1.0 μA (10 μA maximum). One receiver remains active to monitor the Ring Indicator (RI) modem control line, to inform the CPU that a call is coming in from a remote site. In the shutdown mode, the charge pump is disabled, and the charge on C4 eventually drops to one diode below V_{CC}, or the input voltage, whichever is greater. If C4 has discharged to one diode below V_{CC}, and an input voltage is applied that is greater than V_{CC}, C4 will charge up to one diode below that level. However, no DC current flows between the input pin and the +3.3V power supply. The D_{IN} and SD pins still present standard DC loading to the driving logic. Blocking diode D3 prevents a large DC current from flowing between the input pins and the +3.3V supply when the input pin is taken above the device's +3.3V (V_{CC}) power supply pin. This is the classical problem that can occur when directly interfacing a +5V device to some +3.3V devices. A minimal amount of noise is coupled onto the V_{CC} (+3.3V) supply rail if the driver input pin is switched (0V to 5V) while the DS14C335 is in the shutdown mode. However, the magnitude is small, and power supply bypassing capacitors effectively filter out the noise. To prevent noise from coupling onto the V_{CC} rail to begin with, simply hold the driver inputs at a V_{IL} (voltage input low), since with a V_{IL} applied both diodes (D1 and D2) will remain off.

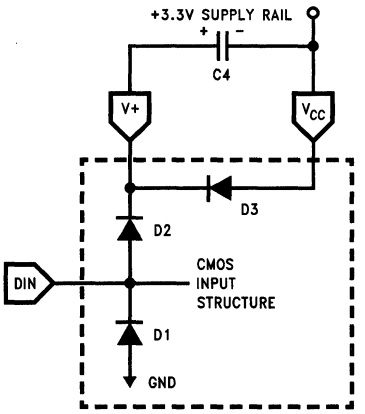

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FIGURE 3. Input Protection Circuitry

This unique input structure allows the driver input pins and shutdown pin to accept any standard TTL/CMOS levels regardless of the DS14C335 mode (active or shutdown) or the fact that the DS14C335 is powered from a +3.3V power supply. The input pins (D_{IN} and SD) present standard loading to the driving logic with input voltages ranging from 0V to +5.5V, in magnitude.

The last pin of concern is the receiver output (R_{OUT}) pin. The R_{OUT} pin must have the drive capability to meet standard TTL/CMOS requirements. The R_{OUT} V_{OH} is specified to be greater than 2.4V at 1 mA. This drive capability should meet all standard TTL/CMOS requirements.

SUMMARY

The DS14C335's unique input structure allows the driver input (D_{IN}) and shutdown (SD) pins to present standard steady state input loading to the driving logic. Valid input voltages can range from −0.3V to greater than +5.5V, thereby enabling the device to be driven by a +5V UART in applications that employ mixed power supplies. The high drive capability of the receiver output meets the requirements of +5V logic levels, or CMOS compliant JEDEC +3.3V levels. These features make the DS14C335 the optimal single chip solution for RS-232 serial ports in +3.3V/+5V or pure +3.3V power supply laptop and notebook computer applications.

Increasing System ESD Tolerance for Line Drivers and Receivers Used in RS-232 Interfaces

National Semiconductor
Application Note 878
John Goldie
Greg Krikorian, Electromer

OVERVIEW

The Data Transmission Applications Group at National Semiconductor investigated field failures of TIA/EIA-232-E (RS-232) DS14C88 Line Drivers and DS14C89A Receivers. The devices are commonly used in computer Input/Output Interfaces, such as a terminal-DTE (Data Terminal Equipment) to modem-DCE (Data Circuit-terminating Equipment) interface. Upon completion of detailed failure analysis on the devices, it was determined that they failed due to electrical over-stress, more commonly known as EOS.

In order to identify the source and type of EOS, a number of DS14C88 and DS14C89A devices were subjected to controlled Electrostatic Discharge—ESD (Electrostatic Discharge) events in the lab using a KeyTek Human Body ESD Simulator, (per IEC801-2 requirements). Additional units were tested with PolyClamp® ESD protection devices to determine their effectiveness and to demonstrate a possible solution for providing greater system ESD tolerance.

The following conclusions have been made as a result of the investigation and bench testing:

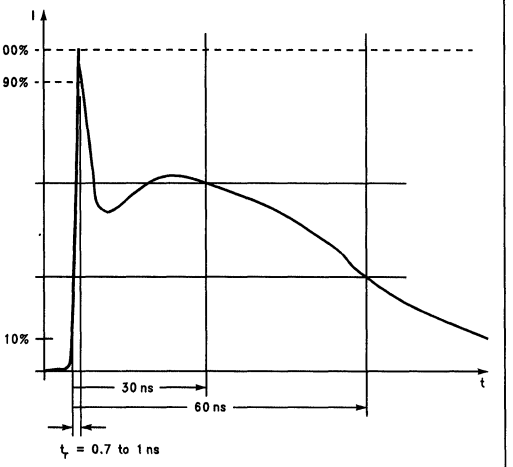
- The pins most commonly damaged are Driver Output and Receiver Input. This implies that the EOS is reaching the IC from the "outside world" via the interface cable and connector. Damage was not seen on driver input or receiver output pins.
- The external source was determined to be an ESD event by matching the failure modes and comparing die photographs of the lab induced failures with the field failures.
- The DS14C88 Line Driver and the DS14C89A Receiver would incur functional failures when subjected to an ESD event below 5,000V without the use of any external ESD protection devices.
- With PolyClamp ESD protection devices installed in the test fixture, all the IC's passed parametric and functional tests at the maximum tested ESD level of 15,000V per IEC 801-2 Specification.

INTRODUCTION

The DS14C88 Quad Line Drivers and the DS14C89A Quad Receivers are predominantly used on TIA/EIA-232-E (RS-232) serial interfaces that connect DTE's to DCE's or other DTE's. The driver outputs and receiver inputs are connected to the outside world through: a printed circuit board (PCB) trace, a connector, and a cable. The driver outputs and receiver inputs are exposed to the outside world (i.e., off the PCB). These devices can be damaged by ESD events that can be directly discharged to the connector pin. To prevent damage to the parts external transient voltage suppression (TVS) diodes have been used in the past to clamp transients to levels that the driver outputs and receiver inputs can withstand. This approach requires a board modification, and a substantial amount of PCB real estate, not to mention cost. This application brief describes a new technology that is available to provide greater ESD system protection without requiring a board modification or any extra PCB real estate. The protection device tested is known as a PolyClamp and is offered by Electromer Corporation. Testing has been conducted on a sample of driver and receiver devices and the remainder of this brief will describe the testing and the results.

TEST FIXTURES AND ESD

Special test fixtures were constructed to replicate a PCB environment. The DS14C88's and DS14C89A's were mounted in standard DIP sockets. Driver output and receiver input pins were connected to a protected 9-pin D Shell connector with the PolyClamp product integrated into the connector shell. For testing, the power supply pins V+ and V− of the DS14C88 device and the V_{CC} pin for the DS14C89A device were grounded. A single positive and a single negative ESD pulse was air discharged to the connector pin which was connected to a driver output or receiver input depending upon the IC under test. The tests were repeated with the supply pins left open. The ESD pulse applied to the connector pins conforms to the IEC801.2 Standard. The energy storage capacitance is 150 pF, while the discharge resistor is 330Ω. The ESD waveform is shown in *Figure 1*.



(Source: Electromer Corporation) TL/F/11789–1

FIGURE 1. Typical Waveform of the Output Current of the ESD Generator

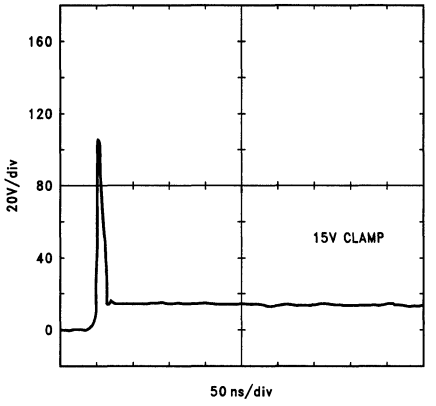
TEST RESULTS

Ten DS14C88 Quad Line Drivers were tested with the PolyClamp product. After the ESD testing, the parts were retested on the ATE (Automatic Test Equipment) final test program to determine if the device incurred any permanent damage or any degraded parameters. The results determined that the PolyClamp protected devices could withstand ESD pulses up to 15,000V, which was the upper limit of the KeyTek ESD simulator. Without the PolyClamp protected connector the DS14C88's failed functional tests after a 2,000V discharge.

Ten DS14C89A Quad Receivers were tested with the PolyClamp product. After the ESD testing, the parts were retested on the ATE final test program to determine if the device incurred any permanent damage or degraded parameters. Again the results determined that the PolyClamp protected devices could withstand ESD pulses up to 15,000V. Without the PolyClamp protected connector the DS14C89A's failed at 1,000V.

The PolyClamp product provides a high level of ESD protection to line driver and receiver integrated circuits.

Characterization testing of the PolyClamp device shows that it provides a 15V DC clamp for a 15,000V IEC801.2 ESD event (see *Figure 2*). In addition, *Figure 2* shows a typical front edge inductive spike of 100V due to test fixtures and inherent lead inductance which is similar to the performance of TVS diodes. Also, after 860 consecutive ESD pulses the PolyClamp protected connector provides the same level of ESD clamping response (see *Figure 3*). Note that the current limiting resistor (330Ω) specified in the IEC test differs from the industry standard Human Body Model (MIL-STD 883C Method 3015), which employs a 1.5 kΩ resistor. The 1.5 kΩ resistor proves a greater current limit, thus the IEC model is a more stringent test.



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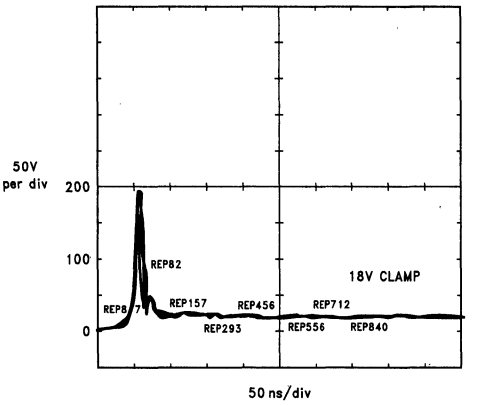
(Source: Electromer Corporation)

FIGURE 2. PolyClamp TVS Device Response to 15 kV ESD Pulse



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(Source: Electromer Corporation)

FIGURE 3. PolyClamp TVS Device Response to 860 Consecutive 15 kV ESD Pulses

CONCLUSIONS

With the use of the PolyClamp protected connectors, protection from ESD events can easily be raised to greater than 15,000V. Additional features of the PolyClamp besides its ESD clamping capability include the following:

- Requires no PCB space—by switching the connector to a protected connector, existing PCBs can be upgraded without a PCB redesign. Many different protected connectors are offered including D-Shells and modular jacks.
- No increase in part count—the protected connector provides ESD clamping for all lines in one piece (the connector), compared to TVS diodes that typically uses 1–2 devices per signal line.
- Economical—in both cost and PCB space compared to other solutions.
- Low capacitance—the protected connector presents a 5 pF typical load to the signal line, minimizing signal distortion.

There are many different ways to protect printed circuit boards and their integrated circuits from ESD and EOS events. These include on-chip enhanced ESD protection of the integrated circuits, TVS diodes, and protected connectors, to name a few. Each of these examples has its own merits and limitations. Enhancements to processes and the development of internal ESD protection circuits has raised integrated circuit tolerance from the several hundreds of volts in some cases to the thousands of volts, but at the expense of die size and cost. TVS diodes require additional PCB space compared to the protected connectors. These two points further illustrate the merits that the protected connectors offer. The PolyClamp protected connectors offer an extremely high level of protection, without additional

PCB space, minimizes part count, and provides a *new* economical solution to increased system level ESD protection.

It should also be noted that protection capability is also offered integrated into common I/O connectors such a D-Sub, MJ, DIN, from AMP Corporation and a similar technology is available from other vendors.

RECOMMENDATIONS

The following guidelines are recommended to reduce the chance of ESD events damaging the line drivers and receivers:

a) When installing or removing the cable, power should be turned off at both ends of the system if possible.

b) Avoid physically touching the connector pins when handling the cable, and wear a ground strap when possible.

c) The use of built-in system level ESD protection devices can extend the level of ESD tolerance.

REFERENCE

For additional information on ESD see also:

Reliability and Electrostatic Discharge, Chapter 10, *Reliability Handbook*, National Semiconductor, 1987

AN-248, Electrostatic Discharge Prevention, *CMOS Logic Databook*, National Semiconductor, 1988

For additional information on Amplimite Products contact:

AMP Incorporated
P.O. Box 3608
Harrisburg, PA 17105
(717) 361-4762
(717) 361-4761 (FAX)

A Comparison of Differential Termination Techniques

National Semiconductor
Application Note 903
Joe Vo

INTRODUCTION

Transmission line termination should be an important consideration to the designer who must transmit electrical signals from any point A to any point B. Proper line termination becomes increasingly important as designs migrate towards higher data transfer rates over longer lengths of transmission media. However, the subject of transmission line termination can be somewhat confusing since there are so many ways in which a signal can be terminated. Therefore, the advantages and disadvantages of each termination option are not always obvious.

The purpose of this application note is to remove some of the confusion which may surround signal termination. This discussion, however, will focus attention upon signal termination only as it applies to differential data transmission over twisted pair cable. Common differential signal termination techniques will be presented and the advantages and disadvantages of each will be discussed.

Each discussion will also include a sample waveform generated by a setup consisting of a function generator whose signals are transmitted across a twisted pair cable by a differential line driver and sensed at the far end by a differential line receiver. This application note will specifically address the following differential termination options:

- Unterminated
- Series/Backmatch
- Parallel
- AC
- Power (Failsafe)
- Alternate Failsafe
- Bi-Directional

For the purposes of discussion, popular TIA/EIA-422 drivers and receivers, such as the DS26LS31 and DS26LS32A, will be used to further clarify differential termination.

UNTERMINATED

The selection of one termination option over another is oftentimes dictated by the performance requirements of the application. The selection criteria may also hinge upon other factors such as cost. From this cost perspective the option of not terminating the signal is clearly the most cost effective solution. Consider *Figure 1,* where a DS26LS31 differential driver and a DS26LS32A differential receiver have been connected (using a twisted pair cable) together without a termination element. Because there is no signal termination element, the DS26LS31 driver's worst case load is the DS26LS32A receiver's minimum input resistance.

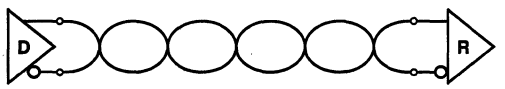

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FIGURE 1. Unterminated Configuration

Since, TIA/EIA-422-A (RS-422) standard defines the DS26LS32A's minimum input resistance to be 4 kΩ, the driver's worst case load, as seen in *Figure 1,* is then 4 kΩ.

In the unterminated configuration, the DS26LS31 driver is only required to source a minimal amount of current in order to drive a signal to the receiver. This minimal DC current sourcing requirement in turn minimizes the driver's on chip power dissipation. In addition, the 4 kΩ driver output load results in a higher driver output swing (than if the driver was loaded with 100Ω) which in turn increases DC noise margin. This increase in noise margin further diminishes the possibility that system noise will improperly switch the receiver. To be sure that there is no confusion, noise margin is defined as the difference between the minimum driver output swing and the maximum receiver sensitivity. On the other hand, if a receiver was used which complies to TIA/EIA-485 (RS-485), the resulting noise margin would be even greater. This is because the minimum input resistance of an RS-485 receiver must be greater than 12 kΩ as compared to 4 kΩ for an RS-422 receiver.

The absence of a termination element at the DS26LS32A's inputs also guarantees that the receiver output is in a known logic state when the transmission line is in the idle or open line state (receiver dependent). This condition is commonly referred to as open input receiver failsafe. This receiver failsafe (Note 1) bias is guaranteed by internal pull up and pull down resistors on the positive and negative receiver inputs, respectively. These pull up and pull down resistors bias the input differential voltage (V_{ID}) to a value greater than 200 mV when the line is, for example, idle (un-driven). This bias is significant in that it represents the minimum guaranteed V_{ID} required to switch the receiver output into a logic high state.

Note 1: A complete discussion of receiver failsafe can be found in Application Note 847 (AN-847).

There are, however, some disadvantages with an unterminated cable. The most significant effect of unterminated data transmission is the introduction of signal reflections onto the transmission line. Basic transmission line theory states that a signal propagating down a transmission line will be reflected back towards the source if the outbound signal encounters a mismatch in line impedance at the far end. In the case of *Figure 1,* the mismatch occurs between the characteristic impedance of the twisted pair (typically 100Ω) and the 4 kΩ input resistance of the DS26LS32A. The result is a signal reflection back towards the driver. This reflection then encounters another impedance mismatch at the driver outputs which in turn generates additional reflections back toward the receiver, and so on. The net result is a number of reflections propagating back and forth between the driver and receiver. These reflections can be observed in *Figure 2.*

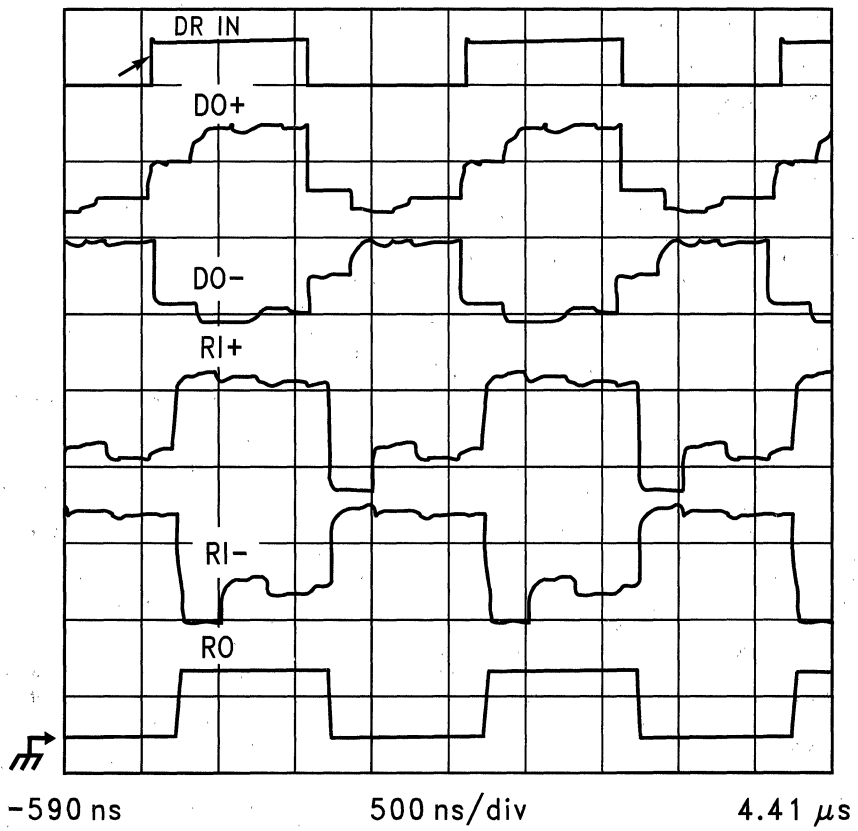

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FIGURE 2. Unterminated Waveforms

The main limitation of unterminated signals can be clearly seen in *Figure 2.* A positive reflection is generated when the signal encounters the large input resistance of the receiver. These reflections propagate back and forth until a steady state condition is reached after several round trip cable delays. The delay is a function of the cable length and the cable velocity. *Figure 2* shows that the reflections settle after three round trips. To limit the effect of these reflections, unterminated signals should only be used in applications with low data rates and short driving distances.

The data being transmitted should, therefore, not make any transitions until after this steady state condition has been reached. A low data rate ensures that reflections have sufficient time to settle before the next signal transition. At the same time, a short cable length ensures that the time required for the reflections to settle is kept to a minimum. The low data rate and short cable length dictated by the lack of termination is probably the most significant shortcoming of the unterminated option.

Low speed is generally characterized to be either signalling rates below 200 kbits/sec or when the cable delay (the time required for an electrical signal to transverse the cable) is substantially shorter than the bit width (unit interval) or when the signal rise time is more than four times the one way propagation delay of the cable (i.e., not a transmission line). As a general rule, if the signal rise time is greater than four times the propagation delay of the cable, the cable is no longer considered a transmission line.

It should be mentioned that most differential data transmission applications provide for some kind of signal termination. This is because most differential applications transmit data at relatively high transfer rates over relatively long distances. In these type of applications, signal termination is critically important. If the application only requires low speed operation over short distances, an unterminated transmission line may be the simplest solution.

SERIES TERMINATION

Another termination option is popularly known as either series or backmatch termination. *Figure 3* illustrates this type of termination. The termination resistors, R_S, are chosen such that their value plus the impedance of the driver's output equal the characteristic impedance of the cable. Now as the driven signal propagates down the transmission line an impedance mismatch is still encountered at the far end of the cable (receiver inputs).

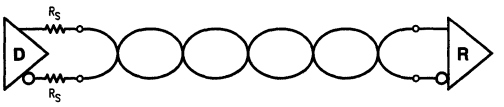

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FIGURE 3. Series Termination Configuration

However, when that signal propagates back to the driver the reflection is terminated at the driver output. There is only one reflection before the driven signal reaches a steady state condition. How long it takes for the driven signal to reach steady state is still dependent upon the length of cable the signal must traverse. As with the unterminated option the driver power dissipation is still minimized due to the light loading presented by the 4 kΩ receiver input resistance. The driver loading remains unchanged from the unterminated option. In both cases the driver is effectively loaded with the receiver's input impedance. DC noise margin has again increased and the open input receiver failsafe feature is still supported for idle and open line conditions.

There are three major disadvantages in using series termination. First, the driver output impedances can vary, due to normal process variations, from one manufacturer to another and from one driver load to another. Should there be a problem which involves replacing line drivers, there is a chance that the designer might have to rework the board in order to ensure that the R_S matches the new driver's output impedance.

Second, series termination is commonly limited to only point to point applications. Consider the following example. If a second receiver (multidrop application) was located halfway between the driver and receiver at the far end of the cable, the noise margin seen by the middle receiver would change between the incident signal and the reflected signal. Such a problem would not exist in a point to point application where only one receiver is used with one driver.

Third, there is still an impedance mismatch at the receiver inputs. Again, this mismatch is caused by a signal propagating down a 100Ω cable suddenly encountering a 4 kΩ receiver input resistance. This impedance mismatch will continue to cause reflections on the transmission line as illustrated in *Figure 4*.

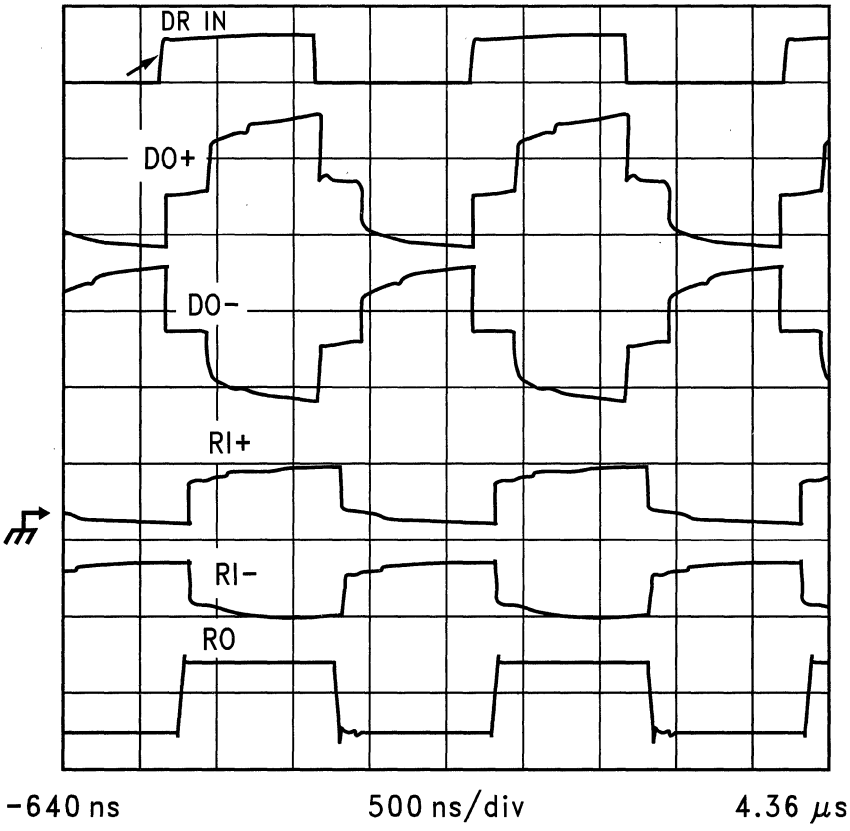

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FIGURE 4. Series Termination Waveforms

Notice the reflections which result when the driven signal encounters an impedance mismatch at the receiver input. The reflection propagates back to the driver and is somewhat terminated by the driver's output impedance. The reflected signal is terminated because the combined impedance of the series resistor (R_S) and the driver's output impedance comes close to matching the characteristic impedance of the cable. In contrast with *Figure 2's* unterminated signal waveform, the waveform seen in *Figure 4* is characterized by only one reflection.

In all it will take the signal one round trip cable delay to be reflected back towards the signal source. Since all reflections should be allowed to settle before the next data transition (to maintain data integrity), it is imperative that the round trip cable delay be kept much less than the time unit interval (TUI—defined to be the minimum bit width or the "distance" between signal transitions). In other words, series termination should be limited to applications where the cable lengths are short (to minimize round trip cable delays) and the data rate is low (to maximize the TUI). And to a lesser degree, the series termination option may not be the ideal choice from a cost perspective in that it requires two additional external components.

PARALLEL TERMINATION

Parallel termination is arguably one of the most prevalent termination schemes today. In contrast to the series termination option, parallel termination employs a resistor across the differential lines at the far (receiver) end of the transmission line to eliminate all reflections. See *Figure 5.*

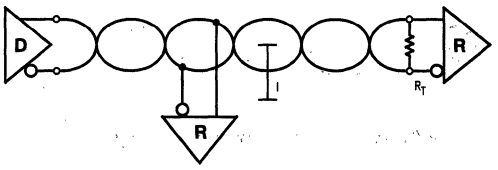

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FIGURE 5. Parallel Termination Configuration

Eliminating all reflections requires that R_T be selected to match the characteristic impedance (Z_O) of the transmission line. As a general rule, however, it is usually better to select R_T such that it is slightly greater than Z_O. Over-termination tends to be more desirable than under-termination since over-termination has been observed to improve signal quality. R_T is typically chosen to be equal to Z_O. When over-termination is used R_T is typically chosen to be up to 10% larger than Z_O. The elimination of reflections permits higher data rates over longer cable lengths. Keep in mind, however, that there is an inverse relationship between data rate and cable length. That is, the higher the data rate the shorter the cable and conversely the lower the data rate the longer the cable. Higher data rates and longer cable lengths translate simply into smaller TUI's and longer cable delays. Unlike series termination where high data rates and long cable lengths can negatively impact data integrity, parallel termination can effectively remove all reflections; thereby removing all concerns about reflections interfering with data transitions. See *Figure 6.*

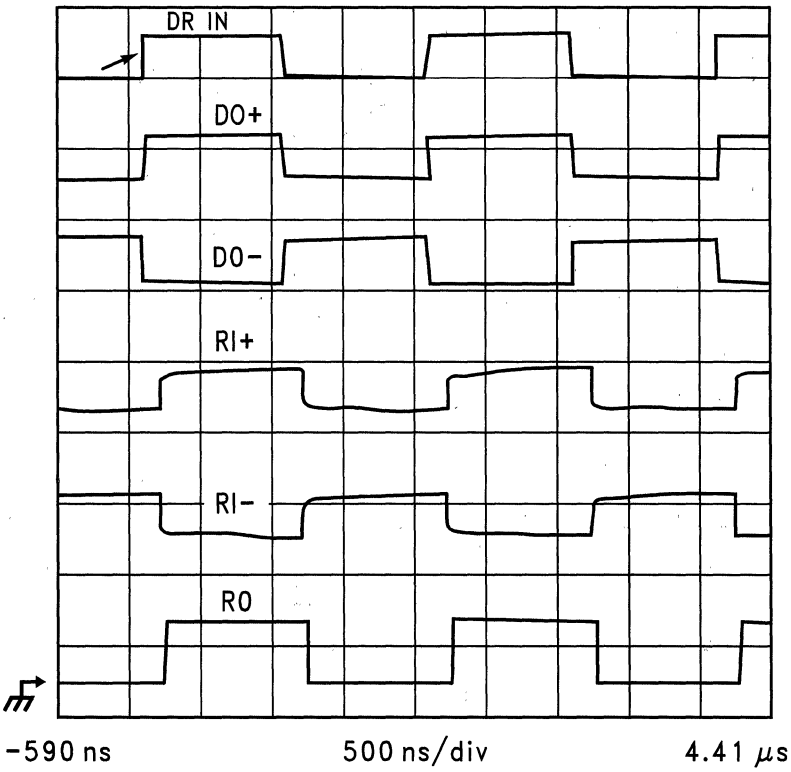

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FIGURE 6. Parallel Termination Waveforms

As seen in *Figure 6* both driver output and receiver input signals are free of reflections. Such results make parallel termination optimal for use in either high speed (10 Mb/s), or long cable length (up to 4000 feet), applications.

Another benefit the parallel termination provides is that both point to point and multidrop applications are supported. Recall that multidrop is defined as a distribution system composed of one driver and up to ten receivers spread out along the cable as defined in the TIA/EIA-422 standard. The parallel termination is located at the far end (opposite the driver) of the cable and effectively terminates the signal at that location, preventing reflections.

There are also disadvantages to parallel termination. Let's examine these disadvantages as they pertain to multidrop configurations. An intrinsic assumption to multidrop operation is that stub lengths, as measured by "l" in *Figure 5*, are minimized. Despite the fact that all receivers are effectively terminated with R_T, long stub lengths will once again reintroduce impedance mis-matches and reflections. So while parallel termination may remove reflections and permit multidrop configurations, it does place a restriction upon the stub lengths associated with these other receivers. Typically stubs should be kept to less that ¼ of the drivers rise time in length to minimize transmission line effects, and reflections.

TIA/EIA-422-A standard does recommend a 100Ω resistor to be used when the differential line is parallel terminated. Therefore, applications which use a TIA/EIA-422-A driver such as the DS26LS31 or DS26C31 are commonly terminated with 100Ω at the far end of the twisted pair cable. While the 100Ω parallel termination eliminates all reflections, the power dissipated by the driver will increase substantially with the addition of this resistor. This increased driver power dissipation is a major disadvantage of parallel termination. The absence of this termination resistor keeps driver power dissipation low for unterminated and series terminated drivers and is a major advantage of these two termination options.

Noise margin will also decrease with parallel termination. The relatively light loading (4 kΩ) of unterminated and series terminated drivers led to larger driver output swings. The heavier driver load (typically 100Ω) brought on by parallel termination reduces the driver's output signal swing. However, even with this reduction, there is ample noise margin left to ensure that the receiver does not improperly switch.

Recall the discussion earlier about receiver failsafe with the unterminated and series options. In both cases, open input receiver failsafe operation was guaranteed because of internal circuitry (receiver dependent) which biases the differential input voltage (V_{ID}) to a value greater than its differential threshold. Since the resulting bias voltage at the receivers inputs (V_{ID}), is greater than +200 mV, the output of the DS26LS32A receiver remains in a stable HIGH state. Unlike unterminated and series options, parallel termination cannot support open input receiver failsafe when the transmission line is in the idle state. This shortcoming of parallel termination is discussed in much greater detail later in the section which describes power and alternate failsafe termination (see AN-847 for more of information on failsafe biasing differential buses).

AC TERMINATION

The effectiveness of parallel termination is oftentimes countered by increased driver power dissipation and receiver failsafe concerns. The DC loop current required by the termination resistor, R_T (see *Figure 5*), is often too large in order to be useful for power conscious applications or for seldomly switched control lines. In asynchronous applications, parallel termination's is not able to guarantee receiver failsafe during idle bus states which in turn makes the system susceptible to errors such as false start bits and framing errors. The primary reason for the AC termination, however, grew out of the need for effective transmission line termination with minimal DC loop current.

A representation of an AC terminated differential line is shown in *Figure 7*.

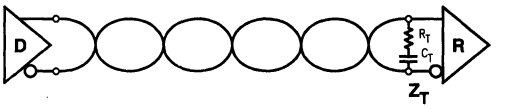

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FIGURE 7. AC Termination Configuration

The value of R_T generally ranges from 100Ω–150Ω (cable Z_O dependent) and is selected to match the characteristic impedance (Z_O) of the cable. C_T, on the other hand, is selected to be equal to the round trip delay of the cable divided by the cable's Z_O.

EQ1: $C_T \leq$ (Cable round trip delay) / Z_O

For this example:

Cable Length	= 100 feet
Velocity	= 1.7 ns/foot
Char. Impedance	= 100Ω

Therefore,

$C_T \leq (100 \text{ ft} \times 2 \times 1.7 \text{ ns/ft})/100\Omega$ or $\leq$ 3,400 pF.

Further, the resulting R_C time constant should be less than or equal to 10% of the unit interval (TUI). In the example provided the maximum switching rate therefore should be less than 300 kHz. This termination should now behave like a parallel termination during transitions, but yield the expanded noise margins during steady state conditions. See *Figure 8*.

Figure 8 illustrates the tradeoff between parallel terminated and unterminated signals. There are no major reflections and driver power dissipation is reduced at the expense of a low pass filtering effect which essentially limits the application of AC termination to low speed control lines. Note that the frequency of the driven signal in *Figure 8* is 300 kHz whereas it was 500 kHz for the other plots. This was done to maintain the ratio between bit time and the R_C time constant. The draft revision of RS-422-A will include AC termination as an alternative to parallel termination.

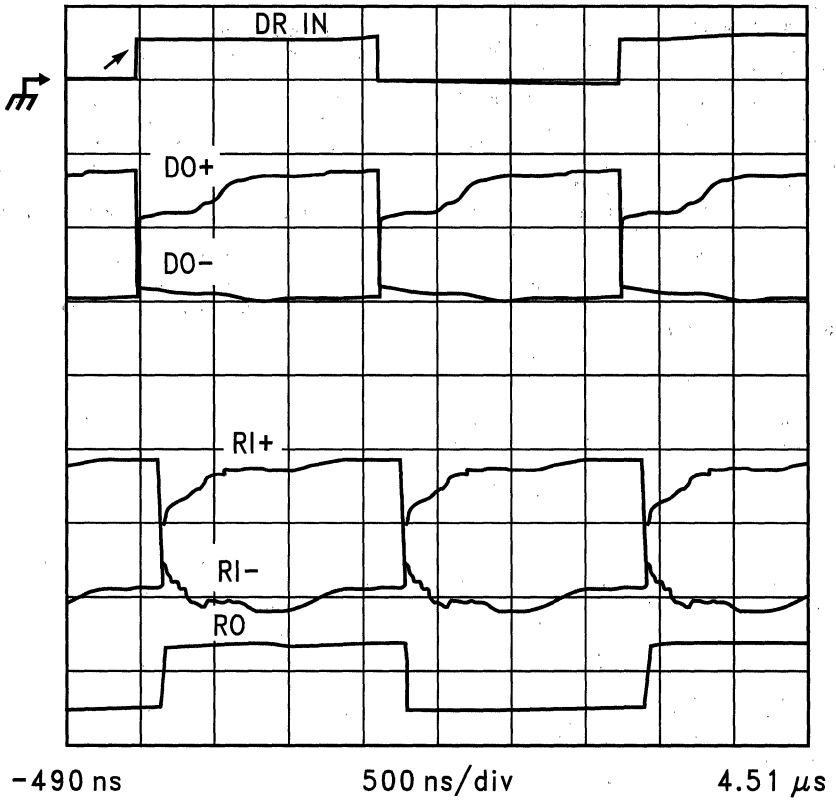

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FIGURE 8. AC Termination Waveforms

The waveforms in *Figure 8* should be viewed together with the following brief explanation of how AC termination works. When the driven signal transitions from one logic state to another, the capacitor C_T behaves as a short circuit and consequently, the load presented to the driver is essentially R_T. However, once the driven signal reaches its intended levels, either a logic HIGH or logic LOW, C_T will behave as an open circuit. DC loop current is now blocked. The driver power dissipation will then decrease. The load presented to the driver also decreases. This is due to the fact that the driver is now loaded with a large receiver input resistance typically greater than 4 kΩ; versus the typical R_T of 100Ω–120Ω. This reduced loading condition increases the signal swing of the driver and results in increased noise margin. The idle bus state also forces C_T into the open circuit mode. Once this takes place, the receiver's internal pull up and pull down resistors will bias the output into a known state. Therefore, besides minimizing DC loop current, preventing line reflections, and increasing noise margin, AC termination also supports open input receiver failsafe.

As with all the previously discussed termination options, there are disadvantages in using AC termination. AC termination introduces a low pass filtering effect on the driven signal which tends to limit the maximum data rate of the application. This data rate limitation is the result of the impact that R_T and C_T, together, have upon the driven signal's rise time. How much the data rate is limited is dependent upon the selection of R_T and C_T. Long R_C time constants will have a greater impact upon the driven signal's maximum data rate, and vice versa. Because of of these data rate limitations, the transmission lines best suited for AC termination are typically low speed control lines where level sensitivity is desired over edge sensitivity. Finally, the part count required by AC termination can put it at a disadvantage in cost conscious applications.

POWER TERMINATION

Recall that AC termination is intended primarily to eliminate the large DC loop current inherent in parallel termination. The power termination, on the other hand, addresses parallel termination's inability to support receiver failsafe during the idle bus state. See *Figure 9* for an illustration of a transmission line terminated using the power option.

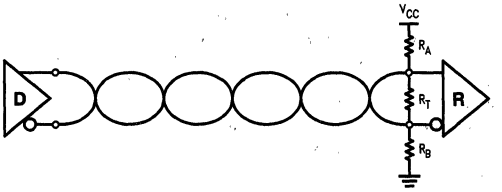

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FIGURE 9. Power Termination Configuration

The lack of R_A and R_B, when the bus is idle, almost assures that the receiver output will not be in a known state. This is due to the insufficient voltage across R_T (on the order of 1 mV–5 mV) as caused by the receiver's internal high value pull up and pull down resistors. The presence of these internal pull up and pull down resistors will guarantee receiver failsafe only for the open input condition. In order to switch the receiver into the logic high state, regardless of whether the bus is open or idle, a minimum of +200 mV (with respect to the inverted receiver input) must be developed across R_T. The sole purpose, then, of R_A and R_B is to establish a voltage divider whereby at least +200 mV will be dropped across R_T. A complete explanation of selection criteria for resistor values (R_A and R_B) can be found in AN-847.

The addition of external receiver failsafe biasing resistors, however, does pose some concerns. The primary drawback relates to the increased driver loading with the addition of R_A and R_B. The increased driver loading decreases the driver's output swing and, in turn, reduces the noise margin. Higher driver power dissipation is also symptomatic of the increased driver loading since the driver must source the additional current required by the external failsafe network. One last concern is that the extra cost and subsequent handling of two additional resistors (excluding R_T) might outweigh power termination's advantages in some applications.

ALTERNATE-FAILSAFE TERMINATION

This version of failsafe termination is essentially an extension of power termination. The addition of R_C and R_D greatly enhances the receiver's ability to operate in harsher environments. See *Figure 10.*

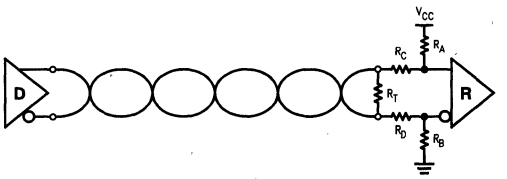

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FIGURE 10. Alternate Failsafe Termination Configuration

The advantages of this failsafe termination point directly to this increased ruggedness. A transmission line terminated using the failsafe option will be able to withstand larger common mode voltages. A careful selection of R_C and R_D will determine how much more common mode voltage a line can endure. This is because R_C and R_D act as a voltage dividers between the receivers input resistance. The TIA/EIA-422-A standard allows for common mode shifting up to 7V in magnitude, however most integrated circuits support absolute maximum rating that exceed the ±7V limit. The DS26LS32A supports a ±25V ABS MAX input rating. Careful selection of resistors can allow common mode voltages in the 35V–45V range on the cable, while still honoring the 25V limit in the receiver input pins. R_C and R_D are typically 4.7 kΩ, while R_A and R_B are 47 kΩ. This provides 9.5 kΩ between the receiver input pins, and also allows the pull up and pull down resistors to be increased in value to 47 kΩ. This capability lends itself well to applications, such as factory control and building to building data transmission, where the common mode range can occasionally exceed ±7V.

Failsafe termination also guarantees receiver failsafe for open, idle, as well as shorted line conditions. Of all the terminations options discussed, the failsafe option is the only one for which receiver failsafe can be guaranteed for shorted differential lines. Shorting the differential lines together merely shorts out R_T. In this short condition, the receiver will still see the series combination of R_C and R_D across its inputs. Receiver failsafe can, therefore, still be supported. The short condition just described yields another benefit of failsafe termination. The increased impedance between V_{CC} and ground, with the addition of R_C and R_D, also results in increased fault or short circuit current limiting.

While the addition of R_C and R_D improves the transmission line's ability to withstand larger common mode voltages, it might also negatively impact the receiver's sensitivity. Consider, for example, a TIA/EIA-422 receiver. The minimum differential input signal (V_{ID}) required to switch the receiver is normally |200 mV|. Depending on the values of R_C and R_D, it may be necessary to develop a minimum of +400 mV across R_T in order to ensure that there is at least 200 mV across the receiver input terminals. The other significant disadvantage with failsafe termination may be the number of resistors required to implement it. Five resistors per line may prove too costly.

BI-DIRECTIONAL TERMINATION

The last type of termination which will be discussed is known as bi-directional termination. *Figure 11* illustrates a typically multipoint application composed of drivers, receivers, and transceivers. Bi-directional termination is parallel termination carried one step further. Bi-directional termination now permits multiple drivers (multipoint configuration) to be connected to the same twisted pair. With multiple drivers connected to the same twisted pair, data can now be transmitted in two directions. Keep in mind, however, that while data transmission can now take place in two directions, only half duplex transmission is allowed (as defined by TIA/EIA-485 standard). Multiple TIA/EIA-485 drivers cannot simultaneously drive the line since this would result in line contention. It should be mentioned that system timing should be carefully inspected to ensure that line contention does not occur. The advantages in using bi-directional termination are almost identical to those with parallel termination.

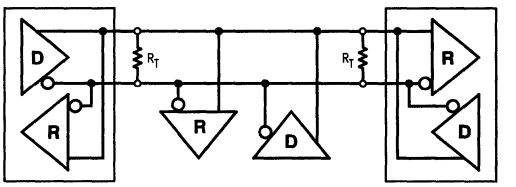

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FIGURE 11. Bi-Directional Termination Configuration

These advantages include the prevention of signal reflections, and the ability to drive long transmission lines at high data rates. As with parallel termination, R_T should be selected so that it matches the characteristic impedance (Z_O) of the twisted pair cable.

The disadvantages in using parallel termination also extend to bi-directional termination. Receiver failsafe cannot be guaranteed due to the interaction between R_T and the receiver's open circuit failsafe network. Stub lengths must be minimized and an R_T must each be placed at both extreme ends of the line in order to minimize transmission line effects. However, when two termination resistors are placed at the far ends of the cable, the effective load of the driver is

now 60Ω (since R_T is typically 120Ω). This "doubling" of the driver load, using bidirectional termination, has two effects. First, it places a greater demand upon the driver's ability to source current. As described above, a multipoint driver must be able to source approximately twice the amount of current that is required from a multidrop driver. A driver expected to meet this increased current demand naturally experiences greater power dissipation. And second, noise margin tends to be reduced since the driver's output levels tend to decrease with increased loading.

CONCLUSION

The advantages and disadvantages of unterminated lines and those with series, parallel, AC, power, failsafe, and bidirectional terminations were contrasted. It should now be clear that there is no one termination scheme which is suited for all applications. Table I provides a summary of the differential termination options discussed in this application note.

TABLE I. Termination Summary

Termination	Signal Quality	Data Rate	Comments
Unterminated	Poor	Low	Low Power
Series	Good	Low	Low Power
Parallel	Excellent	High	Single Resistor
AC	Good	Med.	Ideal for use on control lines
Power	Excellent	High	Failsafe bias for idle line
Alt. Failsafe	Excellent	High	Failsafe for open, shorted, and idle lines
Bi-Directional	Excellent	High	Ideal for bidirectional half duplex operation

The termination scheme used will essentially be dictated by the needs of the system. Specifically, the choice of termination will depend upon the system's data transmission requirements.

SPECIAL NOTES

The waveforms illustrated in this application note were acquired from laboratory testing of TIA/EIA-422 (RS-422) Drivers, and Receivers under the following conditions:

- DS26LS31 Quad Differential Driver
- DS26LS32A Quad Differential Receiver
- Cable = 100', 24AWG, 100Ω, twp cable (Berk-Tek #520382)
- Driver input signal with f = 500 kHz, V_{IH} = 3.0V, V_{IL} = 0V, Duty cycle = 50%
- V_{CC} = 5.0V
- T_A = 25°C

The cable selected for this testing was supplied by Berk-Tek Inc. and represents a typical twisted pair cable commonly used in TIA/EIA-422 applications. Additional information on cables can be obtained from:

Berk-Tek Inc.
132 White Oak Road
New Holland, PA 17557
(717) 354-6200

The RS-422-A standard was developed by the Technical Recommendation (TR30.2) TIA/EIA committee on DTE-DCE Interfaces. Since publication of the revision A, the EIA (Electronic Industries Association) has aligned with the TIA (Telecommunications Industry Association), and future revisions and new standards carry the TIA/EIA prefix, replacing the familiar "RS" (for Recommended Standard) prefix. Revision "B" of RS-422-A is expected in late 1993, and will become TIA/EIA-422-B.

REFERENCES

Transmission Line Characteristics,
B. Fowler, National Semiconductor, Application Note AN-108.

Data Transmission Lines and Their Characteristics,
K. True, National Semiconductor, Application Note AN-806.

Reflections: Computations and Waveforms, K. True, National Semiconductor, Application Note AN-807.

FAILSAFE Biasing of Differential Buses,
J. Goldie, National Semiconductor, Application Note AN-847.

An Introduction to the Differential SCSI Interface

National Semiconductor
Application Note 904
John Goldie

OVERVIEW

The scope of this application note is to provide an introduction to the SCSI Parallel Interface and insight into the differential option specified by the SCSI standards. This application covers the following topics:

- The SCSI Interface
- Why Differential SCSI?
- The SCSI Bus
- SCSI Bus States
- SCSI Options: Fast and Wide
- The SCSI Termination
- SCSI Controller Requirements
- Summary of SCSI Standards
- References/Standards

THE SCSI INTERFACE

The Small Computer System Interface is an ANSI (American National Standards Institute) interface standard defining a peer to peer generic input/output bus (I/O bus). The intention of the SCSI standard is to provide a fast, multipoint parallel bus that is easily upgradeable and keeps pace with advancing technologies.

The SCSI interface is commonly the interconnect of choice for high performance hard disk drives. Being a generic interface, the SCSI bus is not limited to only one type of peripheral. It is also commonly used to interconnect optical drives, tape drives, disk arrays, scanners, printers, and other targets to a wide range of terminals, computers, and other hosts. It is important to also remember that a SCSI bus is not a point to point bus, but rather a multipoint bus, allowing up to eight different devices to be connected to the same daisy chained cable (SCSI-1 and 2 allows up to eight devices while the proposed SCSI-3 standard will allow up to 32 devices). A typical SCSI bus configuration is shown in *Figure 1.*

WHY DIFFERENTIAL SCSI?

In comparison to single-ended SCSI, differential SCSI costs more and has additional power and PC board space requirements. However, the gained benefits are well worth the additional IC cost, PCB space, and required power in many applications. Differential SCSI provides the following benefits over single-ended SCSI:

- **Reliable High Transfer Rates**—easily capable of operating at 10MT/s (Fast SCSI) without special attention to terminations. Even higher data rates are currently being standardized (FAST-20 @ 20MT/s).

The companion Application Note (AN-905) focuses on the features of National's new RS-485 hex transceiver. The DS36BC956 specifically designed for use in differential SCSI applications is also optimal for use in other high speed, parallel, multipoint applications.

- **High Noise Rejection**—the differential transmission scheme provides excellent common mode rejection over a wide bus voltage range.
- **Long Cable Lengths**—cables can be as long as 25 meters in length compared to 3 meters or less for single-ended interfaces.
- **Superior AC Performance**—high performance transceivers with tightly specified and guaranteed AC performance.
- **Fault Tolerance**—current limiting and thermal shutdown protection integrated into the differential driver design.

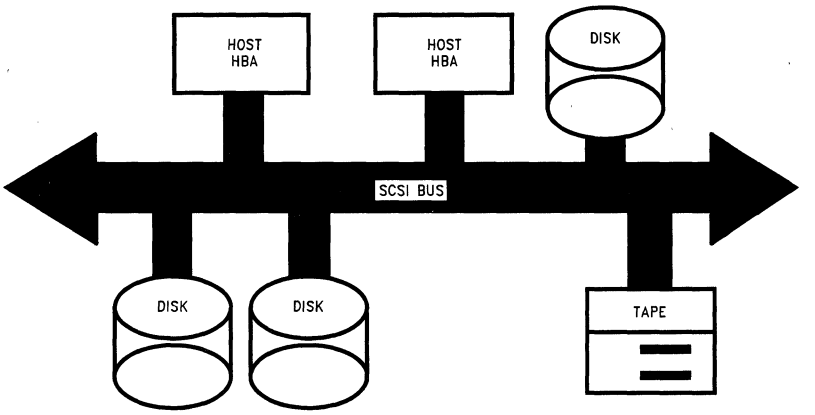

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FIGURE 1. Typical SCSI Bus Configuration-Multiple Hosts/Multiple Targets

Signal quality and long cable runs are the two major enhancements differential SCSI offers over single-ended SCSI. As stated above, differential SCSI allows for cable runs up to 25 meters in length compared to only 3 meters of single-ended SCSI. Differential SCSI is optimal for connecting together terminals with storage arrays located in a separate cooled computer room. The differential transmission scheme offers superior noise rejection and signal quality compared to a TTL single-ended bus.

Differential buses are also immune to minor termination problems that commonly plague the single-ended SCSI bus. These problems can, and commonly do have major impact on single-ended system performance. By expanding the cable length beyond 3 meters, by mixing different cable types (impedance), by using different types of termination, or by using the standard passive termination, system throughput may be reduced as great as 50%. Since it has been determined that the original single-ended termination recommended in the SCSI-1 standard does not provide adequate signal termination performance for Fast SCSI, the SCSI-2 and proposed SCSI-3 standards recommend the use of alternate terminations. There are three popular alternatives to the passive resistive terminators. These are the Boulay termination (voltage regulated), Current Regulated Terminations, and the FPT (forced perfect termination). Each has its own merits and limitations, and in fact the FPT offers good performance but is not sanctioned by the standard. Trouble can arise in single-ended SCSI applications when different types of termination are used on the bus. In addition, some SCSI controllers now provide totem pole outputs on the high speed lines (REQ and ACK) to improve the signal quality on those lines on the de-assert edge (active negation in industry jargon). These active negation drivers can become in contention with the alternative termination techniques and cause thermal problems and data corruption. Single-ended SCSI termination have caused much grief, and discussion in the SCSI standard committee.

In contrast Differential SCSI has not encountered the problems that drove the single-ended interface to develop so many alternative terminations. Differential SCSI uses a standard passive resistor termination (described in detail later in this application note). This terminator remains unchanged from the original SCSI-1 standard to the proposed SCSI-3 physical layer.

National's DS36954 Quad Differential Bus Transceiver is designed for Differential SCSI applications up to 10 MT/s.

THE SCSI BUS

The SCSI bus is composed of a minimum of 18 signal lines. An option is provided to add extra bytes to boost system throughput (Mega Bytes per second (MB/s)) if required by the application. The SCSI 1 and 2 standards define two types of electrical characteristics; single-ended and differential.

Single-ended drivers (typically 48 mA open drain drivers) and receivers are commonly integrated onto the SCSI controller chips. For the differential option, external RS-485 transceivers are required. Integrating the differential transceivers onto the SCSI controller is not feasible due to the additional pins required for differential operation, and the additional power dissipation. Additionally the semiconductor processes commonly used for the controllers are not compatible with the special high speed/high voltage breakdown processes used for RS-485 transceivers.

The single-ended and differential modes are exclusive, and can not inter-operate. Of the 18 lines, 9 are data path (data plus parity) and the others are control. The lines are:

- Data Path
  - — DB(7-0,P)—Data Bus
- Control
  - — REQ—Request
  - — ACK—Acknowledge
  - — BSY—Busy
  - — SEL—Select
  - — C/D—Control/Data
  - — I/O—Input/Output
  - — MSG—Message
  - — ATN—Attention
  - — RST—Reset

The SCSI Standard has two types of devices, which are "Initiators" (typically a host computer); and "Targets" (typically drives). Of the 18 lines, 9 are bi-directional, 7 are unidirectional direction, and 2 are wire-ORed. The data bus (DB0–DB7 and DBP) are the bi-directional lines. Three control lines are Initiator to Target only lines; these are the ACK, ATN, and SEL* lines. Four lines are Target to Initiator only lines; these are the C/D, I/O, REQ, and MSG lines. A pictorial representation of the signal lines is shown in *Figure 2.*

(* SEL can also be a wire-ORed line, but is more commonly implemented as a initiator to target line).

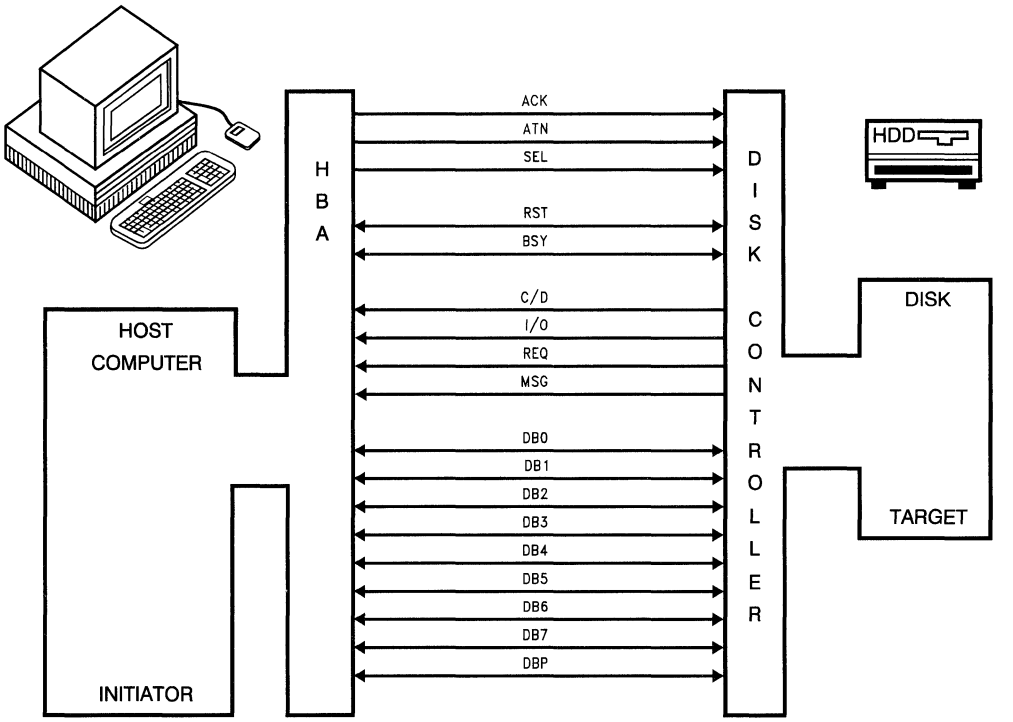

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FIGURE 2. The SCSI Signal Lines

Of the 18 lines, two, REQ and ACK, can operate at switching rates up to 10 MHz. They are defined as handshake lines, that in the asynchronous mode, strobe every byte of data. The maximum defined data transfer rate is 10MT/s for Fast SCSI. This corresponds to a bit width of 100 ns. The data path bits are the second fastest lines on the SCSI bus operating at 10MT/s maximum (5 MHz maximum for a 1-0-1-0 pattern). The other control lines are low speed lines and are level sensitive not edge sensitive. These lines typically only switch between bus states, and a substantial amount of time is provided for settling.

SCSI BUS STATES

The SCSI bus has eight different states which are:

- BUS FREE
- ARBITRATION
- SELECTION
- RESELECTION
- COMMAND
- DATA
- STATUS
- MESSAGE

The SCSI bus state is determined by the state of the SEL, BSY, I/O, MSG, and C/D control lines. Initiators are in control of the bus up to the command phase, and targets control the last three information transfer phases. For example when SEL and BSY are both false, the SCSI bus is in a bus free state.

SCSI OPTIONS: FAST AND WIDE

The FAST option allows for operation at 10MT/s (Mega Transfers per second) compared to the original 5MT/s specified in the original SCSI standard (now commonly referred to as SCSI-1). Single-ended drivers and receivers should be limited to cables less than 3 meters in length and be properly terminated. In contrast, the differential RS-485 transceivers can operate at 10MT/s over 25 meters of cable and due to the differential scheme, offer high noise rejection. The SCSI-2 (draft, 1993) introduced this option to SCSI and has gained wide acceptance.

The WIDE option (also introduced in the SCSI-2 specification) defines extra lines that double or quadruple the system throughput (MB/s). Adding a second byte of data can be accomplished in two different ways. First, one could select the P cable which, with 68 conductors can house both bytes of data and the nine control lines (for a total of 27 lines). The other option specifies two cables (A and B); the A for the first byte and the nine control lines, while the B cable carries the second byte plus an additional REQB and ACKB line (for a total of 29 lines). Since the second option requires two sets of connectors and cables, the P cable has become the more popular of the two, as it saves money and back panel space. The P cable (and Q for Byte 3 and 4) is included in the SCSI-3 Parallel Interface (known as SPI) draft standard, however A and B 50-pin cables are also still allowed. With two bytes of data being transferred, 20MB/s is obtainable. Four bytes achieves a 40MB/s maximum transfer rate. However, the four byte option is not very popular since it again requires two cables (P and Q).

THE SCSI TERMINATION

The differential SCSI bus requires line termination at both ends of the cable. Unlike the single-ended SCSI option, only one type of termination is defined. The line is terminated with a 3 resistor network commonly called a power termination. The three resistors are: 330Ω between the -Signal and the termination voltage (+5V), 150Ω between the signal pair (−Signal and +Signal), and 330Ω from +Signal to ground. The equivalent resistance of this network is 122Ω (150Ω // (330Ω + 330Ω)), and closely approximates the characteristic impedance (Z_O) of the defined cable. The termination network is shown in *Figure 3*.

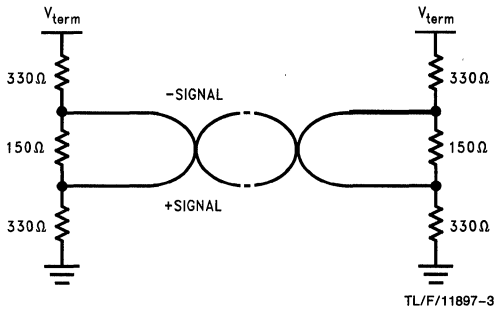


FIGURE 3. The SCSI Differential Termination

By using this termination reflections are minimized and a failsafe bias is provided. When all drivers are in TRI-STATE® (OFF), the resistors bias the line to approximately −1V differential. The SCSI standard defines this as a FALSE state or not-asserted. The minus sign comes from the fact that the +Signal is less in potential than the −Signal by one volt. It does not imply that the voltage is one volt below ground. A common problem that occurs when installing SCSI networks is employing greater than two termination networks. Devices connected in the middle of the bus should not include (enabled) termination networks. The termination networks should only be located at the extreme ends of the cable. Installing three or more terminations loads down the driver's output signal and reduces or eliminates the noise margin.

SCSI CONTROLLER REQUIREMENTS

Not all SCSI controllers support the differential mode. This is due to the fact that the external transceivers require direction control signals.

SUMMARY OF SCSI STANDARDS

This application note provides an introduction and brief overview of the differential option for the SCSI parallel interface. The reader is referenced to the standards listed below for complete, current SCSI specifications. Also, a number of SCSI handbooks are available that cover SCSI basics and protocol details written in plain English compared to the more encrypted standards.

Various manufactures reference different version of the SCSI standard. This creates some confusion to new users. The original version of SCSI released in 1986 is commonly referred to as SCSI or SCSI-1. The ANSI committee has created the second edition of SCSI known as SCSI-2, which is currently in industry ballot (1993). This is still a draft standard until balloting is complete. Approval should occur some time in 1993. Work has started on SCSI-3 also. This proposed standard was broken down into many smaller standards to speed up the ballot/approval process. The parallel interface standard is specified in the SPI document (SCSI Parallel Interface). SCSI-3 differs from SCSI-1 and -2 in the fact that it also specifies alternate physical layers. Currently a serial bus based on a proposed IEEE standard (P1394) is being standardized for small form factor drives and also a fiber physical layer. Table I describes some of the major differences in the physical layers in SCSI-1, 2, and 3 standard and draft standards.

TABLE I. SCSI Standard Comparison

Parameter	SCSI-1	SCSI-2	SCSI-3
Maximum Nodes	8	8	8, 16, and 32
Fast SCSI	NO	YES	YES
Wide SCSI	NO	YES	YES
Maximum Transfer Rate	5MT/s	10MT/s	10MT/s
MB/s-1 Byte	5	10	10
MB/s-2 Byte	X	20	20
MB/s-4 Byte	X	40	40
Document	X3.131 -1986	X3.131 -199x	SPI draft

REFERENCES/STANDARDS

Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems, EIA RS-485-1983, TIA/EIA

Small Computer System Interface (SCSI-1), X3.131-1986, ANSI

Small Computer System Interface (SCSI-2), X3.131-199x, ANSI

SCSI-3 Parallel Interface (SPI), X3T9.2/91-010, Draft Standard, ANSI

Common Data Transmission Parameters and their Definitions

National Semiconductor
Application Note 912
John Goldie

OVERVIEW

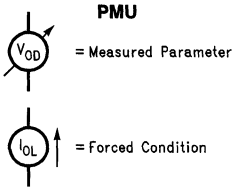
The scope of this application note is to introduce common data transmission parameters and to provide their definitions. This application note is subdivided into five sections, which are:

- Voltage Parameters
- Current Parameters
- Timing Parameters
- Miscellaneous Parameters
- Truth Table Explanations

Each parameter definition typically includes the following information: symbol, full name, description of measurement, measurement diagram, and a list of alternate names where applicable. Due to historical reasons (Fairchild origin, National origin, second sourcing, etc.) some devices use alternate symbols for the same parameters. Whenever possible, a list of common alternate symbols is provided for cross reference. New and future devices from National's Data Transmission Products Group will use the parameters as described in this application note for consistency and clarity reasons and to limit confusion.

This application note will be revised to add new parameters as required by new product definition.

In this application note the following symbols are used in test circuit diagrams. The measured parameter symbol represents a PMU—Precision Measurement Unit located at the test points illustrated in the test circuit. The PMU symbol also includes the parameter's name that is under test. The forced condition represents a forced voltage or current which is required to make the parameter measurement. Once again, it includes the parameter symbol that is being forced.



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VOLTAGE PARAMETERS

Input Voltage Parameters

V_{CL}—Input Clamp Voltage. An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{CM}—Common Mode Voltage. The algebraic mean of the two voltages applied to the referenced terminals, for example the receiver's input terminals. This voltage is referenced to circuit common (ground). This parameter is illustrated in *Figure 1* along with its mathematical equation.

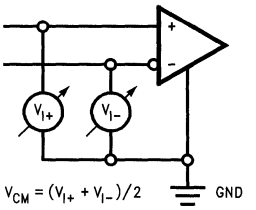

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FIGURE 1. Common Mode Voltage

V_{DIFF}—Differential Input Voltage. The potential difference between the input terminals of the device (receiver) with respect to one of the inputs (typically the inverting input terminal). This parameter may be a positive or negative voltage, and commonly specifies the minimum operating voltage and the absolute maximum differential input voltage. See *Figure 2*. V_{DIFF} is also known as V_{ID} for input differential voltage.

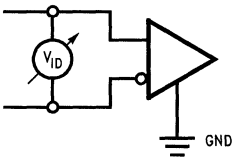

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FIGURE 2. Differential Input Voltage

V_{IH}—High-Level Input Voltage. An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. For example an input voltage between 2.0V and 5.0V in the case of standard TTL logic.

Note: A minimum is specified that is the least positive value of the high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL}—Low-Level Input Voltage. An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables. For example an input voltage between 0.0V and 0.8V in the case of standard TTL logic.

Note: A maximum is specified that is the most positive value of the low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{TH}—Positive-Going Threshold Voltage. The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage rises from a level below the negative-going threshold voltage, V_{TL}. See *Figure 3*. Note that V_{TH} has also been used in the past to specifiy both thresholds in one parameter. In this case, V_{TH} represents the Threshold Voltages and supports a minimum and maximum limit, for example, ±200 mV.

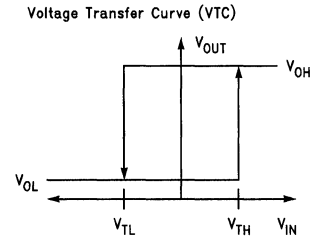

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FIGURE 3. Threshold Voltages

V_{TL}—Negative-Going Threshold Voltage. The voltage level at a transition-operated input that causes operation of the logic element according to specification, as the input voltage falls from a level above the positive-going threshold voltage, V_{TH}. See *Figure 3* above.

V_{HYS}—Hysteresis. The absolute difference in voltage value between the positive going threshold and the negative going threshold. See *Figure 4*. Hysteresis is the most widely symbolized parameter. Alternate symbols include: V_{HY}, $V_{T+}-V_{T-}$, V_{HYST}, ΔV_{TH}, $V_{TH}-V_{TL}$, and V_{HST}.

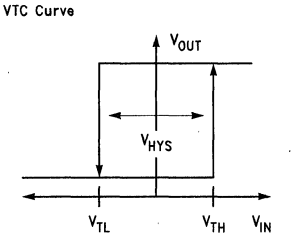

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FIGURE 4. Hysteresis Voltage

OUTPUT VOLTAGE PARAMETERS

V_{OD}—Output Differential Voltage. The output voltage between the output terminals of a differential driver with input conditions applied that, according to the product specification, will establish a voltage level at the output. This voltage is measured with respect to the inverting output of the differential driver. V_{OD} is defined as the voltage at true output (A, $D_{OUT}+$, or DO) minus the voltage at the inverting output (B, $D_{OUT}-$, or DO*). Commonly an alpha-numeric suffix is added to designate specific test conditions. For example the case of different resistive loads. Also a star "*" or over-score bar is used with the parameter to designate the parameters' value with the opposite input state applied. This parameter has also been designated Terminated Output Voltage (V_T) in some datasheets.

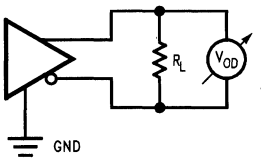

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FIGURE 5. V_{OD} Test Circuit

ΔV_{OD}—Output Voltage Unbalance. The change in magnitude of the differential output voltage between the output terminals of a differential driver with opposite input conditions applied. ΔV_{OD} is defined as: $\Delta V_{OD}=|V_{OD}|-|V_{OD}*|$.

V_{OH}—High Level Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the output. This voltage is measured with respect to circuit common (ground). See *Figure 6*.

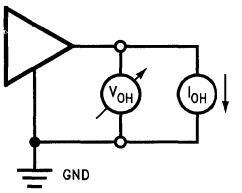

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FIGURE 6. V_{OH} Test Circuit

V_{OL}—Low Level Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the output. This voltage is measured with respect to circuit common (ground). See *Figure 7*.

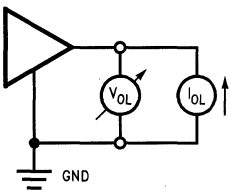

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FIGURE 7. V_{OL} Test Circuit

V_{OS}—Offset Voltage. The center point output voltage between the output terminals of a differential driver with input conditions applied that, according to the product specification, will establish a voltage level at the output. This voltage is measured with respect to the driver's circuit common (ground). Commonly a star "*" or over-score bar is used with the parameter to designate the parameter's value with the opposite input state applied (see *Figure 8*). This parameter is also referred to as V_{OC}—Common Mode Voltage.

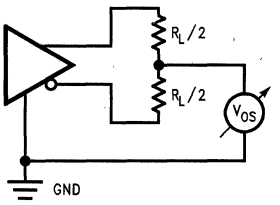

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FIGURE 8. V_{OS} Test Circuit

ΔV_{OS}—Offset Voltage Unbalance. The change in magnitude of the offset voltage at the output terminals of a differential driver with opposite input conditions applied. ΔV_{OS} is defined as:

$$\Delta V_{OS} = |V_{OS}| - |V_{OS}^*|.$$

V_{SS}—Steady State Output Voltage. The steady state differential output voltage is defined as $|V_{OD}| + |V_{OD}^*|$. This is typically a calculated parameter only, based on the formula shown above. The V_{OD} parameter is defined above and illustrated in *Figure 5*. V_{SS} is equal to twice the magnitude of V_{OD} and is shown in *Figure 9*.

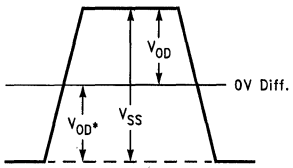

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FIGURE 9. Differential Output Steady State Voltage

V_T—Terminated Output Voltage. The output voltage at an output terminal with input conditions applied that, according to the product specification, will establish a known logic level at the output. This voltage is measured with respect to circuit common (ground) with a stated resistance, and may be a positive or negative voltage. This parameter is typically used in conjunction with single-ended (unbalanced) line drivers. See *Figure 10*.

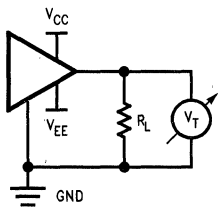

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FIGURE 10. V_T Test Circuit

ΔV_T—Terminated Output Voltage Unbalance. The change in magnitude of the terminated output voltage at the output terminal of a single-ended line driver with opposite input conditions applied. ΔV_T is defined as:

$$\Delta V_T = |V_T| - |V_T^*|.$$

CURRENT PARAMETERS

Note: Current is specified as magnitude value only, with the sign denoting the current direction only. A negative sign defines current flowing out of a device pin, while a positive sign defines current flowing into a device pin. The largest current limit is specified as a maximum, and zero (0) by default is the smallest minimum. All future DTP datasheets will follow this convention, and only some existing datasheets follow this convention.

I_{IH}—High-Level Input Current. The current into (out of) an input when a high-level voltage is applied to that input. Note that current out of a device pin is given as a negative value. Typically this parameter specifies a positive maximum value for bipolar devices.

I_{IL}—Low-Level Input Current. The current into (out of) an input when a low-level voltage is applied to that input. Note that current out of a device pin is given as a negative value.

I_I—Maximum Input Current. The current into (out of) an input when the maximum specified input voltage is applied to that input. Note that current out of a device pin is given as a negative value.

I_{IN}—Input Current. The current into (out of) a receiver input when a specified input voltage, or voltage range is applied to that input. Note that current out of a device pin is given as a negative value. This parameter is typically tested at the maximum voltage specified for the input. For differential receivers the other input (not under test) is held at 0V (in the case of RS-422/3 and 485 receivers).

I_{ING}—Input Current, Power Up Glitch. The current into (out of) an input when a specified input voltage, or voltage range is applied to that input. Note that current out of a device pin is given as a negative value. This parameter applies to transceivers (RS-485) only, and is actually specifying the driver's performance at a specific power supply level. Additionally the driver is biased such that it is enabled, with the specified power supply voltage applied. This parameter assures that the driver is disabled by an internal circuit at the specified power supply level, even though the enable pin is active. If the driver was enabled, I_{OS} current would be observed, instead of the combined measured current of driver TRI-STATE® leakage (I_{OZ}) plus receiver input current (I_{IN}). For example $V_{CC} = 3.0V$ is commonly referenced to represent a single point in a power up/down cycle. (See AN-905 for more information on this parameter).

I_{OS}—Output Short Circuit Current. The current into (out of) an output when that output is short-circuited to circuit common (ground) or any other specified potential, with input conditions as noted, typically such that the output logic level is the furthest potential from the applied voltage. This parameter commonly includes an identifying suffix. For example I_{OSD} represents the output short circuit current of a driver, while I_{OSR} represents the receiver's output short circuit current. Output short circuit current is also designated by the following symbols: I_{O+}, I_{SC}, and I_S. See *Figure 11*.

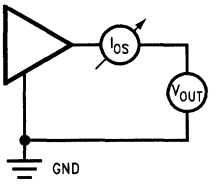

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FIGURE 11. I_{OS} Test Circuit

I_{OZ}—TRI-STATE Output Current. The current into (out of) a TRI-STATE output having input (control) conditions applied that, according to the product specification, will establish a high impedance state at the output. This parameter commonly includes an identifying suffix. For example, I_{OZD} represents the TRI-STATE output current of a driver, while I_{OZR} represents the receiver's TRI-STATE output current. In addition I_{OZH} and I_{OZL} are also commonly used and denote the forced voltage (logic) level. See *Figure 12.*

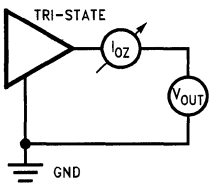

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FIGURE 12. I_{OZ} Test Circuit

I_{OX}—Power Off Leakage Current. The current flowing into (out of) an output with input conditions applied that, according to the product specification, will establish a high impedance state at the output. Commonly a known state is required on the power supply pin as an input condition. For example, power supply terminal (V_{CC}) equal to zero volts may be a required condition of an I_{OX} parameter. See *Figure 13.*

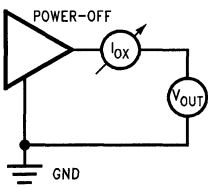

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FIGURE 13. I_{OX} Test Circuit

I_{OD}—Differential Output Current. The current flowing between the output terminals of a differential line driver with an external differential load applied that, according to the product specification, will establish a known state at the output. See *Figure 14.*

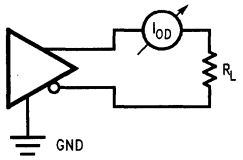

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FIGURE 14. Differential Output Current

I_{OH}—High-Level Output Current. The current into (out of) an output terminal with input conditions applied that, according to the product specification, will establish a logic high level at the corresponding output. Note that current out of a terminal is given as a negative value.

I_{OL}—Low-Level Output Current. The current into (out of) an output terminal with input conditions applied that, according to the product specification, will establish a logic low level at the corresponding output. Note that current out of a terminal is given as a negative value.

I_{CC}—Supply Current. The current into the V_{CC} supply terminal of the integrated circuit. Normally the parameter is measured with all loads removed. It may also include a suffix that denotes that state of the device. For example:

I_{CCD} = Power Supply Current (drivers enabled, receivers disabled)

I_{CCR} = Power Supply Current (receivers enabled, drivers disabled)

I_{CCZ} = Power Supply Current (drivers and receivers disabled)

I_{CCX} = Power Supply Current (sleep or shutdown mode)

I_{EE}—Supply Current. The current into the V_{EE} supply terminal of the integrated circuit. Normally the parameter is measured with all loads removed. It may also include a suffix that denotes that state of the device. Note that current out of a terminal is given as a negative value. For example:

I_{EED} = Power Supply Current (drivers enabled, receivers disabled)

I_{EER} = Power Supply Current (receivers enabled, drivers disabled)

I_{EEZ} = Power Supply Current (drivers and receivers disabled)

I_{EEX} = Power Supply Current (sleep or shutdown mode)

TIMING PARAMETERS

t_{PLH}—Propagation Delay Time, Low-to-High-Level Output. The time between specified reference points on the input and output voltage waveforms with the output changing from a logic low level to a logic high level.

t_{PHL}—Propagation Delay Time, High-to-Low-Level Output. The time between specified reference points on the input and output voltage waveforms with the output changing from a logic high level to a logic low level.

t_{SK}—Propagation Delay Skew. The magnitude difference between complementary propagation delays. Skew is defined as $|t_{PLH} - t_{PHL}|$. This specification is a per channel parameter unless specified otherwise.

t_{PLHD}—Differential Propagation Delay Time, Low-to-High-Level Output. The time between specified reference points on the input and output differential voltage waveforms with the output changing from a logic low level to a logic high level.

t_{PHLD}—Differential Propagation Delay Time, High-to-Low-Level Output. The time between specified reference points on the input and output differential voltage waveforms with the output changing from a logic high level to a logic low level.

t_{SKD}—Differential Propagation Delay Skew. The magnitude difference between complementary differential propagation delays. Skew is defined as $|t_{PLHD} - t_{PHLD}|$. This specification is a per channel parameter unless specified otherwise.

t_{PZH}—Output Enable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from a high impedance (off) state to a logic high level.

t_{PZL}—Output Enable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from a high impedance (off) state to a logic low level.

t_{PHZ}—Output Disable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from logic high level to a high impedance (off) state.

t_{PLZ}—Output Disable Time. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the TRI-STATE output changing from logic low level to a high impedance (off) state.

t_{PSH}—Propagation Delay Time, Sleep-to-High-Level Output. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from an off state to a logic high level.

t_{PSL}—Propagation Delay Time, Sleep-to-Low-Level Output. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from an off state to a logic low level.

t_{PHS}—Propagation Delay Time, High-Level Output to Sleep. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from logic high level to an off state.

t_{PLS}—Propagation Delay Time, Low-Level Output to Sleep. The propagation delay time between the specified reference points on the input (control) and output voltage waveforms with the output changing from logic low level to an off state.

t_r—Rise Time. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from low to high. Note, also commonly specified as transition time (t_{TLH}).

t_f—Fall Time. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from high to low. Note, also commonly specified as transition time (t_{THL}).

t_{TLH}—Transition Time Low to High. The time between two specified reference points on an input waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from low to high. Note, also commonly specified as rise time (t_r).

t_{THL}—Transition Time High to Low. The time between two specified reference points on an output waveform, normally between the 10% and 90% or the 20% and 80% points, that is changing from high to low. Note, also commonly specified as fall time (t_f).

t_{NW}—Noise Pulse Width. The width in time of a pulse applied to a device. The parameter is commonly specified with receivers that feature low pass noise filters. t_{NW} is the pulse width assumed to be noise and guaranteed to be rejected.

MISCELLANEOUS PARAMETERS

SR—Slew Rate. The time between two specified reference points on an output waveform, normally between the ±3V level for TIA/EIA-232 (RS-232) drivers, divided by the voltage difference. Note, this parameter is normally specified in Volts per microsecond (V/μs). A suffix may be added to denote different loading conditions.

R_{IN}—Input Resistance. The slope of the input voltage vs. input current curve of an input when a specified voltage range is applied to that input and the current is measured. Note, that two points must be measured for the parameter to be calculated correctly as R_{IN} is defined as $\Delta V/\Delta I$ not V/I.

R_{OUT}—Output Impedance. The resulting output impedance calculated from measured currents at applied voltages.

TRUTH TABLE EXPLANANTIONS

Symbols generally associated with functional truth tables are listed below:

H or 1 = Logic High Level (steady state)

L or 0 = Logic Low Level (steady state)

Z = TRI-STATE® (high impedance off state)

X = irrelevant (input, including transitions)

REFERENCES

ALS/AS IC Device Testing, ALS/AS Logic Databook. National Semiconductor Corp., 1990

Glossary of Terms, ALS/AS Logic Databook. National Semiconductor Corp., 1990

Understanding Power Requirements in RS-232 Applications

National Semiconductor
Application Note 914
Syed Huq

INTRODUCTION

As the popularity of asynchronous serial communication became widely accepted by the industry, the RS-232 standard gained very wide acceptance. The use of this standard is visible in almost all Industrial, Portable, Desktop, Data Acquistion and Test Measurement applications using a serial port for communication. Even though the standard specifies a maximum data rate for RS-232 of 20 kbps, some applications need for higher speed is overwhelming. More and more applications today require at least 120 kbps to support Laplink®, a popular communication software used by Laptop/Desktop computers for fast file transfer between two computers. RS-232 type Drivers and Receivers must also support this higher data rate to be Laplink compatible.

This application note covers the RS-232 circuit functions, an explanation of hardware handshaking, a step by step analysis of the hardware handshaking between a local and remote terminal, and power requirements/dissipation of the DS14C335.

RS-232 HANDSHAKING CIRCUITS

In a Terminal (DTE-Data Terminal Equipment) to Modem (DCE-Data Circuit Terminating Equipment) application, as shown in *Figure 1*, commonly only eight dedicated lines are required. Even though the standard defines a 25 pin connection, the de-facto 9 pin connector is very popular. These lines are DCD, RXD, TXD, DTR, DSR, RTS, CTS, RI and GND and are shown in *Figure 2*. Lets take a quick look at these dedicated lines along with their respective functions. Note that ON is defined as a positive voltage and OFF is a negative voltages on the cable.

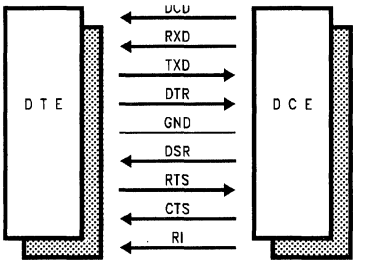

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FIGURE 2. Direction of Flow from DTE/DCE

DCD: DATA CARRIER DETECT (DCE TO DTE)

When this circuit is OFF locally, it indicates to the local terminal that the remote DTE has not switched its RTS circuit ON yet and the local terminal can gain control over the carrier line if needed. When this circuit is ON locally, it indicates to the local terminal that the remote modem has received a RTS ON condition from its terminal and the remote DTE is in control over the carrier line.

RXD: RECEIVE DATA (DCE TO DTE)

Receive data circuit from modem to DTE.

TXD: TRANSMIT DATA (DTE TO DCE)

Transmit data circuit from DTE to modem.

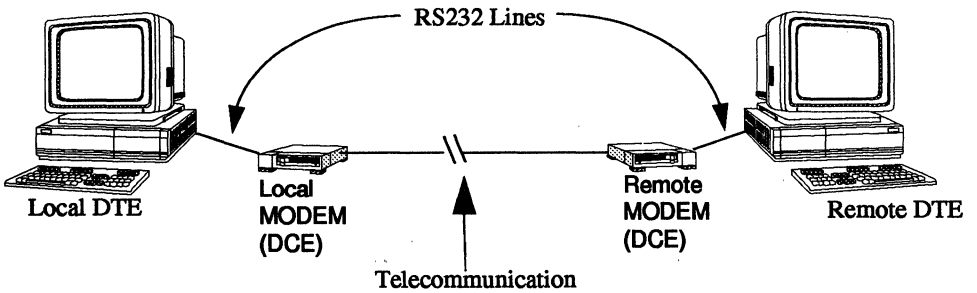

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FIGURE 1. DTE to DCE Interface

DTR: DATA TERMINAL READY (DTE TO DCE)

The DTR pin is generally ON when the terminal is ready to establish communication channel through its modem. By keeping the DTR circuit ON the DTE lets an *"auto answer"* modem accept the call unattended. The DTR circuit is OFF, only when the DTE does not want its modem to accept calls from remote locations. This is known as *local mode.*

DSR: DATA SET READY (DCE TO DTE)

Both modems switch their DSR circuit ON when a communication path has been established between the two sites (local and remote modem).

RTS: REQUEST TO SEND (DTE TO DCE)

When a terminal is ready to transmit data, it switches the RTS circuit ON, indicating to the local modem that it is ready to transmit data. This information also gets passed to the remote modem. The RTS line controls the direction of data transmission. During transmit mode, the line is ON and during receive mode it's OFF.

CTS: CLEAR TO SEND (DCE TO DTE)

When CTS swicthes ON, the local modem is ready to receive data from its DTE and the local modem has control over the telephone lines for data transmission.

RI: RING INDICATOR (DCE TO DTE)

When the modem receives a call, the RI circuit switches ON/OFF in sequence with the phone ringing informing the DTE that a call is coming in. This indicates that a remote modem is requesting a dial-up connection.

GND

Ground, signal common.

HARDWARE HANDSHAKE FLOW

A step by step analysis of handshaking illustrates how each circuit is used to establish communication between a local and a remote site. To keep the subject simple, assumption has been made that transmission is from Local to Remote only.

1. Local DTE switches DTR ON and local modem dials the phone number of the remote modem.
2. If DTR at remote location is ON, the remote modem's RI turns ON/OFF in sequence with the phone ringing, indicating a call coming in.
3. The remote modem returns an answer-back tone to the local modem. Upon detection of this tone, the local modem and the remote modem establishes the on-line connection. At this point both modems switch their DSR pins ON indicating that a connection has been established.
4. The local DTE switches RTS ON indicating that it is ready to send data. This signal gets passed on to the remote modems DCD circuit.
5. The local modem checks to make sure that local DCD is OFF, which indicates that the remote modem is not in control of the carrier line.
6. The local modem then switches CTS ON to the local DTE to inform that it can start sending data. Locally the DCD circuit stays OFF. On the remote modem DCD stays ON. RTS is held ON by the local DTE throughout the duration of the connection.
7. The local DTE sends data through TXD to modem for transmittal.
8. The remote modem receives the data and sends the data to its terminal via the RXD circuit.
9. When data transmittal is finished, local DTE drops RTS, which drops the DCD at remote modem and CTS at local modem. Transmission of data can be discontinued by hanging up the phone line, by the DTE dropping its DTR circuit, by disconnecting the modem cable from the DTE.
10. Now, either DTE is ready to start all over again and gain control of the telecommunication line.

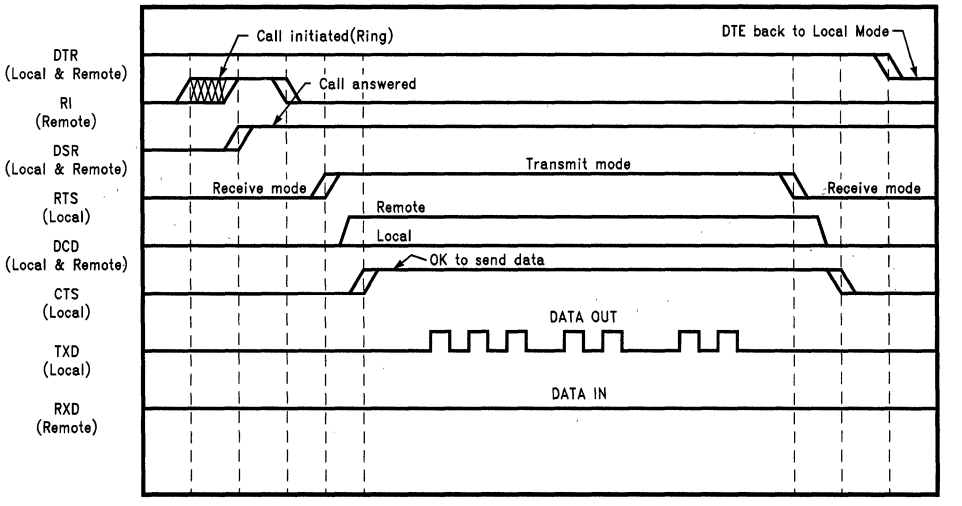

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FIGURE 3. Graphical Illustration of Hardware Handshaking

From the above explanations, in half-duplex communication, we can derive that in transmit mode, only one driver (TXD) is switching (up to 120 kbps) while the other drivers/receivers are at some known steady state (not switching). Similarly, on a receive mode, only one receiver (RXD) is switching while other lines maintain known steady state levels.

POWER CONSUMPTION

Based on the above observations, lets determine how I_{CC}, frequency, internal/external capacitance and load resistance play a role in power consumption for the DS14C335. Total power consumption is the static and the dynamic power combined. CMOS devices typically consume minimal power in a static condition. This can be calculated simply by multiplying I_{CC} with V_{CC}.

Under a loaded condition, the external loading of the driver directly effects the power dissipation of the device and application. The RS-232 driver is normally connected to a cable and a receiver at the far end. Since the transition time of the driver is set to be substantially longer than the cable delay, the cable load represents a lumped capacitive load and a series resistance. The series resistance on short cables (< 200 feet) can be neglected since it is very small compared to the receiver input resistance. This means the cable may be modeled as a lumped capacitive load equal to the capacitance per unit length multiplied by the length of the cable. 1000 pF is commonly used to represent a 20 foot cable, and 2500 pF is used as the maximum specified cable load. The receiver input resistance is specified to be between 3 kΩ and 7 kΩ, 5 kΩ is used as a typical, and 3 kΩ is the worst case from a power point of view. This equivalent load is illustrated in *Figure 4*.

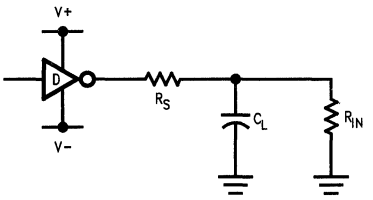

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FIGURE 4. Load Seen by the Driver

Where: R_S = Cable series resistance.

C_L = Cable load capacitance.

R_{IN} = Input resistance of the Receiver.

A channel that is in a steady state is loaded by the receivers input impedance since the cable capacitance has charged up. The output current of the driver is determined by the output voltage of the driver (V_{OH} or V_{OL}) divided by the input resistance of the receiver. For example, a 7V level, across the 3 kΩ load, requires 2.3 mA.

Dynamic power consumption has three major components. The switching current (spike current, also commonly called Conduction Overlap Current) during transitions, external load resistance and external load capacitance transient dissipation.

When the voltages to an NMOS/PMOS pair are in transition, both transistors turn on partially, creating a relatively low impedance path between the supply rails (V+ and V−). This is known as simultaneous conduction and is illustrated in *Figure 5*. As input frequency increases, the period decreases. At some point the output transistors fail to charge and discharge fully causing both upper and lower output transistor to stay on momentarily. This simultaneous conduction increases I_{CC} as the input signal's frequency is increased.

The charging and discharging of the large load capacitance C_L contributes to power consumption as well. The external load capacitance increases power in the same manner as the internal capacitance. A channel that is switching at speed is affected by all the components described previously. These new components contribute to the increased output current sourced or sunk by the driver to charge or discharge the capacitive load. This component of the load current will increase if the external capacitance is increased and also if the switching rate of the device is increased.

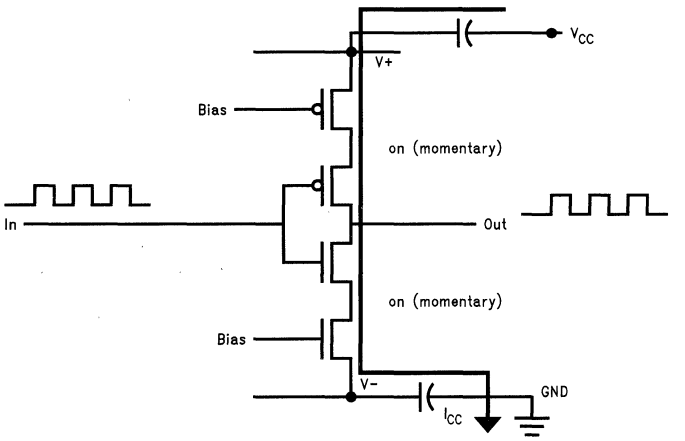

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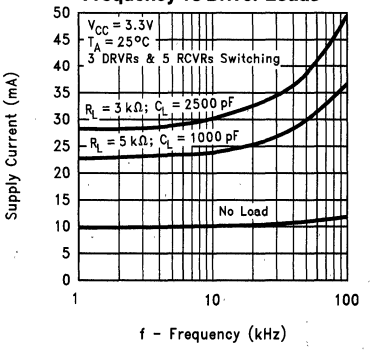
FIGURE 5. Simultaneous Conduction and I_{CC}

DS14C335 AND POWER CONSUMPTION

National's DS14C335 is a 3 X 5 Driver/Receiver combination providing a one-chip solution for a 9 pin RS-232 DTE application. *Graph 1* shows a worst case situation where all 3 drivers and 5 receivers are switching under different loading conditions. Under this worst case condition, at 10 kHz (20 kbps), supply current is 30 mA (2500 pF). Under a no load condition, supply current stays relatively flat. *Graph 2* shows a true RS-232 application where one driver (TXD) is switching while the other two are driver (DTR and RTS) remain High (loaded) as shown in *Figure 3*. At 10 kHz, supply current reads 26 mA (2500 pF), under this real world RS-232 application. Decreasing the capacitive load also decreases the supply current as shown in *Graph 2*. *Graph 3* illustrates one receiver (RXD) switching. Supply current is almost constant under this operating condition.

DS14C335 Supply Current vs Frequency vs Driver Loads



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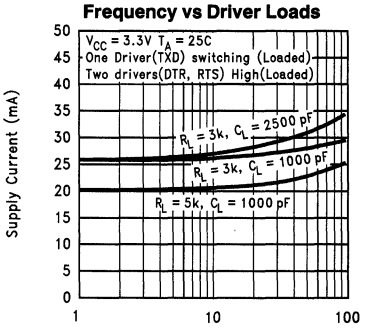
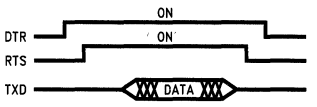
GRAPH 1. All Driver and Receiver Switching

DS14C335 Supply Current vs Frequency vs Driver Loads





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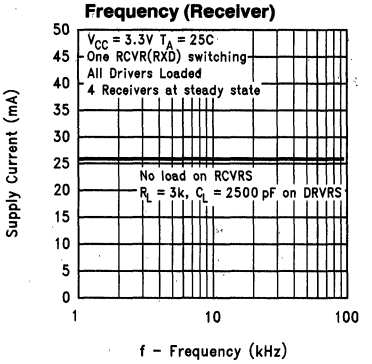
GRAPH 2. One Driver (TXD) Switching

DS14C335 Supply Current vs Frequency (Receiver)



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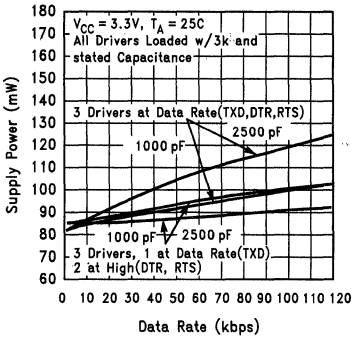
GRAPH 3. One Receiver (RXD) Switching

Looking at the Supply Power vs Data Rate (*Graph 4*) we can see that under multiple driver switching and at a maximum data rate of 120 kbps, the supply power is 120 mW (2500 pF load). With one driver switching and the other two driver output at High (RS-232 Application), the supply power at maximum data rate of 120 kbps drops to 103 mW (2500 pF load).

DS14C335 Supply Power vs Data Rate



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GRAPH 4. Supply Power vs Data Rate

The DS14C335 also offers a SHUTDOWN (SD) feature where the device can be de-activated by applying a logic High on the SD pin. This will lower the supply current to less than 1 μA (typical). In addition, in this mode one receiver (R5) remains active to monitor RI (Ring Indicator). This active receiver can sense incoming calls and inform the power management circuit to activate the device. SHUTDOWN mode saves battery life when the serial port is not used. In this mode, power dissipation is only 3.3 μW allowing battery charge to be used by other active circuitry.

OTHER INDUSTRY STANDARDS (RS-232)

RS-562 is another standard that is gaining popularity in the Industry. RS-562 is compatible to RS-232, however, there are some trade-offs. Table I illustrates a comparison and the major differences between the two standards.

TABLE I. Comparison and Major Differences between RS-232 and RS-562

Specifications	RS-232	RS-562
Mode of Operation	Single-ended	Single-ended
Receiver Input Resistance (Ω)	3 kΩ to 7 kΩ	3 kΩ to 7 kΩ
Receiver Sensitivity	±3V	±3V
Driver Output Current (Powered Off, ±2V)	±6.67 mA (300Ω)	±6.67 mA (300Ω)
Driver Output Short Circuit Current Limit	**≤100 mA**	**≤60 mA**
Number of Drivers and Receivers Allowed	1 Driver 1 Receiver	1 Driver 1 Receiver
Max Cable Length	~50′ (2500 pF)	2500 pF (20 kbps) 1000 pF (64 kbps)
Max Data Rate	**20 kbps**	**64 kbps**
Driver Output	**±5V Min ±15V Max**	**±3.7V Min ±13.2V Max**
Driver Load	3 kΩ to 7 kΩ	3 kΩ to 7 kΩ
Driver Slew Rate	≤30 V/μs	≤30 V/μs

Even though RS-562 standard specifies data rates greater than RS-232, the DS14C335 (RS-232) far exceeds the 64 kbps of RS-562. The most significant difference between the two standards is the noise margin. As shown in *Figure 6*, RS-232 devices have a noise margin of 2V or greater. Typically for DS14C335, the noise margin is 4.5V (7.5V − 3V) whereas RS-562 has a noise margin as low as 700 mV (3.7V − 3V). A lower noise margin (RS-562) means limited rejection of external noise, crosstalk and ground potential differences which can all commonly occur in RS-232 type communication.

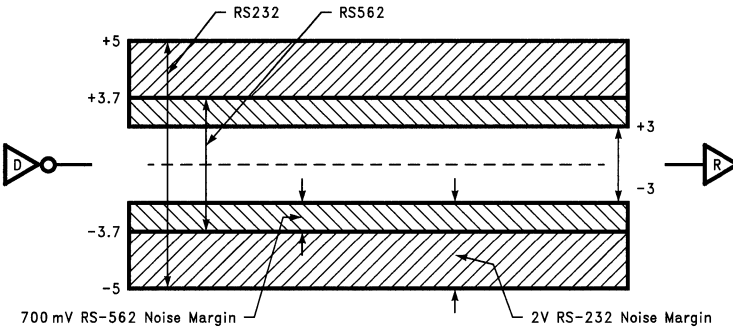

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FIGURE 6. Noise Margin Comparison

CONCLUSION

Design Engineers are plagued with ground shift, noise problems and a noise margin of only 700 mV is not acceptable in many applications. RS-232 guarantees a 2V noise margin and Nationals DS14C335 is the preferred choice for applications requiring data rates pushing 120 kbps. Also, we have observed that in a half-duplex RS-232 DTE to DCE application, the supply current of the device is lower than simultaneous switching of all drivers and receivers as the application only requires one driver (TXD) or one receiver (RXD) switching at a time while the rest of the drivers/receivers maintain known steady state levels. Along with the power dissipation calculations, a discussion of the SHUTDOWN feature was also presented. This SHUTDOWN mode is highly desirable for any application that is battery powered, as it saves battery charge when the serial port is inactive.

REFERENCES

Piecewise analysis and accurate emulation yield precise power estimates, William Hall and Ray Mentzer, National Semiconductor Corp., *EDN March 16, 1992.*

CMOS, the Ideal Logic Family, Stephen Calebotta, National Semiconductor Corp., *Application Note AN-77.*

54C/74C Family Characteristics, Thomas P. Redfern, National Semiconductor Corp., *Application Note AN-90.*

HC-MOS Power Dissipation, Kenneth Karakotsios, National Semiconductor Corp., *Application Note AN-303.*

RS-232 Made Easy: Connecting Computers, Printers, Terminals and Modems, Martin D. Seyer.

Automotive Physical Layer SAE J1708 and the DS36277

National Semiconductor
Application Note 915
Michael Wilson
Todd Nelson

INTRODUCTION

Multiplex (MUX) wiring, or networking, has been introduced in automotive applications to address the increase in complexity and the number of onboard electronic devices in automobiles. Both standardized and proprietary solutions exist to address these issues. A standardized approach may be more desirable as cost and interoperability become important factors to consider for all original equipment manufacturers including automobile manufacturers.

The purpose of this application note is to give a general understanding of the J1708 recommended practice (SAE J1708) and the DS36277 transceiver which is optimized for use with SAE J1708. Additionally, this application note explains the significant differences between the DS36277 and a standard RS-485 transceiver, the DS75176B.

EXPLANATION OF TERMS

Dominant Mode—This is a mode of operation in which one logic state is dominant over any other state on the bus.

Listen Mode—This is a mode of operation in which a receiver is always active (assuming the device is powered) and its output is always in a known state.

DEFINITION OF TIA/EIA-485 AND SAE J1708

This section explains the definition of TIA/EIA-485 (RS-485) and SAE J1708. However, this section does not explain the electrical characteristic specifications of RS-485 or SAE J1708. The provisions for SAE J1708 will be discussed in the next section and for a brief definition of the RS-485 electrical specifications, refer to National application note AN-216.

First, RS-485 is an interface standard that specifies only electrical characteristics for balanced multipoint interface circuits. A complete interface standard will specify electrical, mechanical, and functional characteristics as does the popular interface standard TIA/EIA-232-E (see Table I). Second, SAE J1708 specifies only the functional characteristics for balanced interface circuits. RS-485 is referenced by SAE J1708 for its electrical specifications but with a few modifications. Thus, the end designer of a SAE J1708 application must specify their own mechanical connections.

TABLE I. Definition of RS-485 and SAE J1708

	Mechanical	Functional	Electrical
TIA/EIA-485			✓
SAE J1708		✓	REF. RS-485
TIA/EIA-232-E	✓	✓	✓

THE SAE RECOMMENDED PRACTICE J1708

The Society of Automotive Engineers (SAE) has defined this recommended practice for serial data communications between microcomputer systems in heavy duty vehicle applications. It is also well suited to passenger car applications (as shown in *Figure 1*) and many non-automotive uses. The bus is expected to be used for sharing data. An applications document, like SAE J1587 or SAE J1922, defines the actual data and/or functions to be transmitted. SAE J1708 only defines the hardware and basic software.

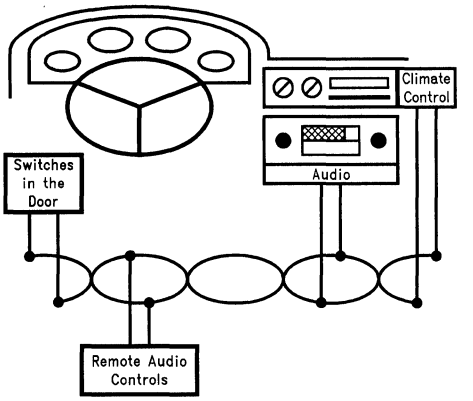

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FIGURE 1. Automobile Controls on a SAE J1708 Bus

The physical media is a two-wire bus using 18-gauge twisted pair with a minimum of 1 twist per inch. The maximum length is intended to be 40m. A maximum of 20 nodes is specified. Deviations from this must be carefully analyzed to determine impact on bus performance over the entire operating range.

Each node may access the bus randomly once the bus is idle for a predetermined access time. If two or more nodes attempt to access the bus at the same time, the contending nodes must arbitrate for the bus. Arbitration is determined by priority, which is set between 1 (top priority) and 8. An applications document shall reference SAE J1708 and define the priority associated with each message. Since there can be up to 20 nodes, it is possible for two contending nodes to have the same priority. When contention exists between two or more nodes, arbitration is determined by the bus access time. This is the time a node is required to wait before it can attempt to access the bus.

The protocol is consistent with standard UART operation. A message consists of a Message Identification character (MID), a data character(s) and a checksum character. The total message length should not exceed 21 characters. A character is defined as 10 bits: the first bit is always the start bit (logic level LOW), followed by eight bits of data and, the tenth bit is the stop bit (logic level HIGH) (see *Figure 2*).

The bit timing equates to a baud rate of 9600. The logic LOW and HIGH levels are encoded as "dominant" and "recessive" which will be described later. The hardware is defined by the RS-485 standard for its electrical characteristics, with some exceptions and modifications.

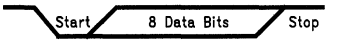

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FIGURE 2. Character Format

J1708 BUS LOADING

The recommended implementation for a SAE J1708 load is shown in *Figure 3*. The recommended implementation for a SAE J1708 system using a standard RS-485 transceiver, such as the DS75176B (see *Figure 4*), is shown in *Figure 7*. The circuitry between the bus and the transceiver differs from RS-485 and is intended to provide several features:

- R1 and R2 provide the bias for the "recessive" state.
- C1 and C2 combine to form a 6 MHz low pass filter, effective for reducing FM interference.
- R2, C1, R4 and C2 combine to form a 1.6 MHz low pass filter, effective for reducing AM interference.
- Since the bus is unterminated, at high frequencies R3 and R4 perform a pseudo-termination. This makes the implementation more flexible as no specific "termination nodes" are required at the ends of the bus.

The resistor and capacitor values are as follows and are shown in *Figure 3:*

Resistor 1 and 2 (R1 and R2)— 4.7 kΩ

Resistor 3 and 4 (R3 and R4)— 47Ω

Capacitor 1 and 2 (C1 and C2)— 2.2 nF

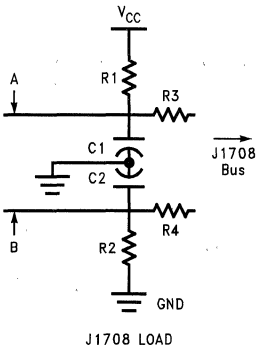

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FIGURE 3. Node Load Circuit

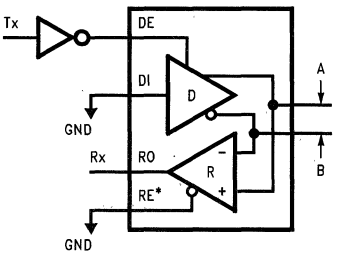

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FIGURE 4. The DS75176B in a SAE J1708 Application

DOMINANT MODE

The drivers used by SAE J1708 are used in a dominant mode application. The driver's input (DI) is tied LOW and the signal (Tx) to be transmitted is tied to the driver's enable. The enable (DE) is active HIGH for the DS75176B while the enable (DE*) for the DS36277 is active LOW. First, this information is very important because this tells us that the driver is only capable of driving LOW. Therefore, a logic level LOW is encoded as "dominant". When the driver is disabled, the bus is pulled high by external bias resistors R1 and R2 (as shown in *Figure 3*). Thus, a logic level HIGH is encoded as "recessive". Second, if the driver's enable is active LOW, then you will transmit positive logic. But, if the driver's enable is active HIGH you will transmit negative logic. SAE J1708 is only defined for positive logic. Therefore, to implement a SAE J1708 application using DS75176B, which has an active HIGH driver enable, an inverter is needed for the driver enable (see *Figures 4* and *6*). However, the active LOW driver enable pin on the DS36277 saves the user an externally needed inverter (see *Figure 5*).

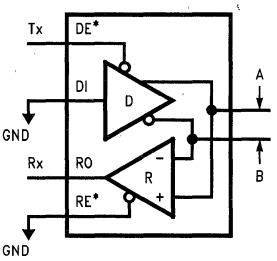

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FIGURE 5. The DS36277 in a SAE J1708 Application

In the case of a SAE J1708 application, a logic LOW can overwrite a logic HIGH. Thus, if contention exists between two drivers with transmitting signals (Tx) in opposite states, the driver driving the "dominant" state wins.

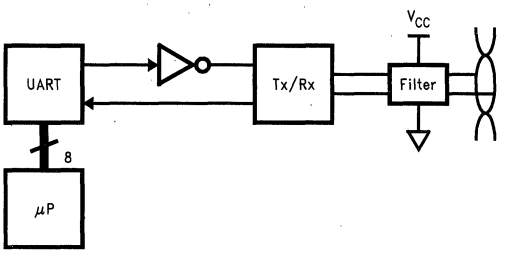

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FIGURE 6. Typical SAE J1708 System Block Diagram

SAE J1708 requires all receivers to listen to every message identification character transmitted to determine if contention exists. Unlike the driver, the receiver's enable (RE*) is always tied LOW (see *Figures 4* and *5*). This means the receiver is always in listen mode (see Explanation of Terms).

The external components shown in *Figure 3* provide the necessary bias for a logic High "recessive" state. SAE J1708 requires no additional external components other than the J1708 load. This means that no parallel termination can be used at the ends of the SAE J1708 bus. The required loading also provides failsafe protection.

FEATURES OF THE DS75176B

The DS75176B offers full compliance with the RS-485 standard and it is compatible with RS-422 and V.11. The device is available with industrial temperature range. Additionally, a thermal shutdown circuit protects the device against thermal overstress due to excessive power dissipation. Furthermore, the receiver has failsafe protection. However, the receiver's output is only guaranteed to be in a logic HIGH state for an open input line condition. The receiver also has ±200 mV threshold levels. The driver has an active HIGH enable while the receiver has an active LOW enable.

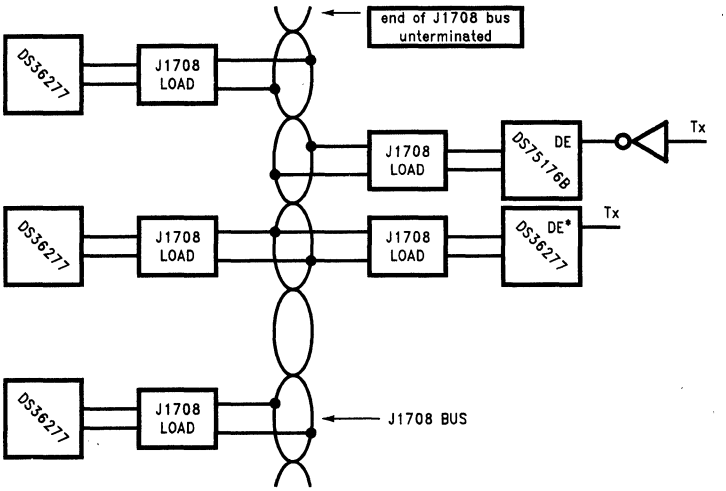

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FIGURE 7. SAE J1708 Typical Bus Configuration and Loading

FEATURES OF THE DS36277

The DS36277 is optimized for use with SAE J1708 electrical applications and the device is still compatible with RS-485, RS-422, and V.11 standards. Like the DS75176B, the device is available with industrial temperature range. Also the device includes thermal shutdown protection; plus the receiver has failsafe protection. Additionally, the receiver has full failsafe defenses that includes shorted and terminated line fault/conditions as well as open line conditions. The receiver's output is guaranteed to be in a logic HIGH state for all three line faults/conditions. The receiver's 0V to −500 mV threshold provides the protection from shorted line faults. Unlike the DS75176B, both the driver and the receiver have an active LOW enable.

The DS36277 also has a very rugged ESD structure that allows it to withstand electrostatic discharges (ESD) up to 7 kV (HBM). The device is also available in SOIC as well as DIP packages.

CONCLUSIONS

Selecting an established physical layer such as J1708 can eliminate many of the challenges of designing a serial communications system. The dominant mode operation allows for a non-destructive arbitration scheme.

J1708 is based on RS-485 electrical specifications and therefore benefits from the ruggedness, low cost and availability of compliant ICs already on the market.

The DS36277 transceiver has been optimized for J1708. It provides failsafe protection against bus faults and eliminates the need for an external inverter.

This application note provides a brief overview of the recommended practice and the interface standard. It is highly recommended to carefully review the complete documents. The documents can be obtained from:

SAE, 400 Commonwealth Dr.
Warrendale, PA 15096-0001

Global Engineering Documents
2805 McGraw Avenue
P.O. Box 19539
Irvine, CA 92174

REFERENCES

1. EIA RS-485, Standard for *Electrical Characteristics of Generators and Receivers for use in Balanced Digital Multipoint Systems,* Electronic Industries Association Engineering Department. Washington D.C. 1983.

2. SAE J1708, *Serial Data Communications Between Microcomputer Systems In Heavy Duty Vehicle Applications.* Society of Automotive Engineers. 1990.

A Practical Guide To Cable Selection

National Semiconductor
Application Note 916
David Hess, Berk-Tek
John Goldie

Berk-Tek

1.0 INTRODUCTION

This application note provides an overview of the various considerations necessary for selecting suitable copper multiconductor or twisted pair cables for use with standard interface devices. It is important that a cable is well matched to the application; as well as, that the various cable selection trade-offs are considered for a cost effective system design. Cable types, constructions, and characteristics are covered and then related to the various device requirements.

2.0 TYPES OF CABLES

The two most basic cable categories are flat and round (see *Figures 1* and *2*). Both flat and round cables are available in multiconductor or twisted pair configurations and each with or without shielding. Shielding of various types is also available in both cases. Flat cables have carefully controlled conductor spacing making them suitable for mass termination. Round cables are suited for long cable runs or where flexibility and compactness are required.

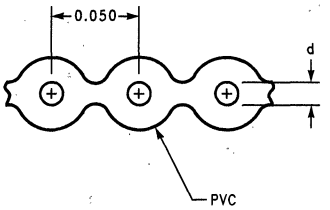

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FIGURE 1. Drawing of Flat Cable, Cross-Section

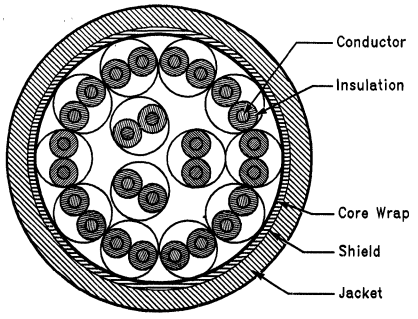

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FIGURE 2. Drawing of Round Cable, Cross-Section

Multiconductor cables are available for basic single-ended, i.e., unbalanced applications. Twisted pair cables are available for differential, i.e., balanced applications *(Figure 3).* Note that a coaxial cable, a single insulated conductor with an overall shield; is, in this context, a "multiconductor" cable with only one conductor (the shield serving the dual purpose of signal return path and signal containment). In a similar sense, a two conductor multiconductor cable, since it is twisted, is equivalent to a single twisted pair cable.

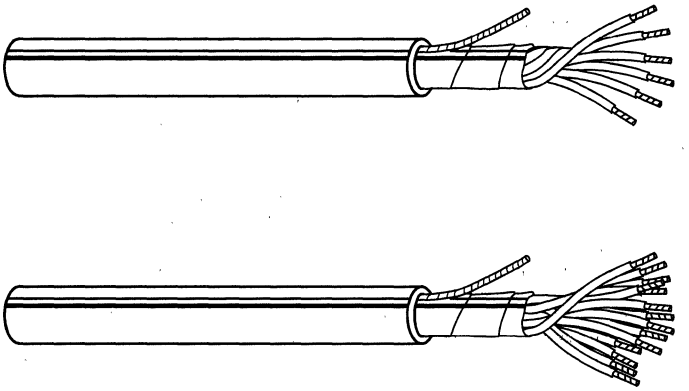

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FIGURE 3. Drawing Comparison of Multiconductor Cable and Twisted Pair Cable

It is common and preferable to use a twisted pair cable for single-ended applications. Some higher speed or longer distance single-ended applications provide a separate return conductor for each data and timing circuit, helping to reduce crosstalk. Note that single-ended applications cannot fully utilize the special capability of a twisted pair. Multiconductor cable should not be used for differential applications where twisted pairs are essential.

It is important to recognize that a twisted pair serves a fundamental electrical purpose. A twisted pair maintains, along its length, the balance necessary for and thus the common mode rejection sought in differential applications. The degree of physical symmetry achieved in constructing a twisted pair of insulated conductors determines how well it is balanced electrically. The double helix configuration of the pair produces symmetrical parasitics for each conductor. Symmetrical parasitics assure that induced noise signals are equal, or "common", to both conductors. This is the primary means of reducing crosstalk between various circuits within a cable. Flat cables constructed with twisted pairs are also available to achieve improved crosstalk characteristics.

Advantages of Flat Cables

By providing a means for mass termination, flat cables are relatively inexpensive to terminate. Connectors are available in configurations with insulation displacement contacts aligned for flat cable termination. The contacts are simultaneously pressed through the insulation onto all of the conductors of a flat cable. The cable conductor to connector contact alignment is critical. The two industry standard conductor centerline spacings are 0.050 and 0.025 inches. Controlling this parameter is a primary concern in producing flat cable and somewhat limits the range of cables' electrical characteristics available.

Advantages of Round Cables

Round cable flexibility is not limited to a single plane, as in the case of flat cable. For long cable runs, especially installed in conduit or raceway, flat cable is impractical. The flexibility of round cables is the result of having the individual elements, single conductors or twisted pairs, "cabled"; that is, they are "laid" at a pitch angle relative to the axis of the cable, forming a helix. The greater the pitch angle the greater the degree of flexibility. Color coding is usually provided as the means of identifying the individual conductors aiding the process of individually terminating each conductor. A round cable is simpler to manufacture with a shield. Capacitance can be reduced with thicker insulation walls, since there are no inherent conductor spacing requirements. Other than the case of simple, flat, strait, unshielded multiconductor cables; round cables have less cross-sectional area for a given number of conductors. More cross-sectional area is required for a shield or jacket on a flat cable.

3.0 CABLE CONSTRUCTION

Overall Construction

Conductors

Standard subminiature D-style connectors are designed to accept conductor sizes ranging typically from 22 AWG down to 26 AWG. Stranded tinned copper is normally used. Stranding provides a considerable improvement in flexibility and protection from conductor breaks due to repeated flexing, i.e., improved flex life. Tin coating on the strands improves environmental resistance by preventing corrosion of the conductor. The tin coating also makes the conductor more suitable for soldering. Standard connector pins are sized to accept the stranded conductor's increased diameter compared to solid conductor diameters.

Solid or non-tinned conductors are not recommended for use with some connectors. Some connector pins are crimped onto the end of the conductor where a small section of the insulation has been removed. This leaves a short section of exposed conductor susceptible to corrosion. Given the minimal space provided within the connector backshell, the added flexibility of stranded conductor makes the job of cramming the terminated conductors into the backshell a lot easier and more reliable. Conductor stranding also increases the overall cable flexibility, easing installa-

tion, and making the cable more likely to withstand the related abuses. If there will be even occasional flexing required in the cable application, stranded conductors are strongly recommended.

Nominal cost savings are gained by eliminating stranding or tin coating, but consideration should be given to the reduction in reliability. Stranding and tin coating have an effect on the signal loss of a transmission line, but these effects are insignificant below frequencies of about 10 MHz. These effects are essentially immeasurable at the frequencies associated with current TIA data communication standards; furthermore, other far more predominant limiting factors arise at data rates greater than 1 Mbps.

For typical serial data links, the de-facto standard gauge size is 24 AWG. TIA/EIA interface standards' recommendations are based on 24 AWG. This is the appropriate size to use with common subminiature D-style connectors. For smaller conductors to be properly captured in crimped contacts, special sized contacts may be required. Overall cable size and weight reduction can be achieved using 26 AWG or smaller conductors at the expense of increased fragility. Note, there are National Electrical Code restrictions that prevent conductors smaller than 24 AWG from being used in premises communication applications. Smaller conductors are recommended for restricted applications, such as equipment cables or where overall cable size must be limited; say for wide parallel data links used in short distances, up to 10 or 20 meters.

Larger conductors cannot provide very much improvement in performance. The overwhelming performance limiting factor in serial data communication systems is noise. An attempt to increase data rate and/or distance by increasing conductor size and thus reducing attenuation, is likely to be offset by crosstalk and other noise limitations. Consider, for instance, that EIA-422-A gives recommendations for transmission up to 1,200 meters (4000 feet) at data rates up to 90 kbps on 24 AWG cable. Typical data communication applications fall within the restrictions imposed by the voltage drop limitations of 24 AWG conductor. Special sized connector contacts may be required for larger conductors.

Copper conductors come in standard sizes according to the American Wire Gauge (AWG) system. A conductor gauge size is based on its cross-sectional area, and thus DC resistance. The overall diameter of the conductor depends on whether it is solid or stranded. Stranding is provided as a means of improving flexibility and flex-life, and the strand bundle is twisted similarly and for the same reasons mentioned above for the overall cable. The basic stranding configuration is 7 strands; 6 around 1. For a given gauge size; the more strands, the more flexible. Stranded conductors are considerably more expensive than solid conductors and the cost increases with greater numbers of finer strands. Stranded conductors utilize standard AWG size strands and numbers of strands. Their size is designated by the largest AWG size less than or equal to the sum cross-sectional area of the individual strands. Note, insulation displacement connector contacts are specifically designed for either solid or stranded conductors.

TABLE I. Conductors Solid Stranded Tinned and Bare from 30 AWG to 20 AWG vs Diameter DCR Weight, etc.

AWG	Stranding	Diameter		Weight		D. C. Resistance @20°C			
						Tin Coated		Bare or Silver Plated	
		inches	mm	lbs./kft.	kg/km	ohms/kft.	ohms/km	ohms/kft.	ohms/km
40	solid	0.0031	0.079	0.0291	0.0433	1158	3799	1080	3540
38	solid	0.0040	0.102	0.0484	0.0720	696	2283	648	2130
36	solid	0.0050	0.127	0.0757	0.113	445	1461	415	1360
34	solid	0.0063	0.160	0.120	0.179	281	920	261	857
32	solid	0.0080	0.203	0.194	0.289	174	571	162	532
32	7/40	0.010	0.254	0.21	0.31	176	577	164	539
30	solid	0.0100	0.254	0.30	0.45	113	371	104	340
30	7/38	0.012	0.305	0.35	0.52	106	348	92.6	303
28	solid	0.0126	0.320	0.48	0.72	70.8	232	65.3	214
28	7/36	0.015	0.381	0.55	0.82	67.5	221	59.3	194
26	solid	0.0159	0.404	0.77	1.14	44.5	146	41.0	135
26	7/34	0.019	0.483	0.87	1.29	42.5	139	37.3	122
24	solid	0.0201	0.511	1.22	1.82	27.2	89.2	25.7	84.2
24	7/32	0.024	0.610	1.38	2.05	25.7	84.2	23.1	75.9
22	solid	0.0253	0.643	1.94	2.89	16.7	54.8	16.2	53.2
22	7/30	0.031	0.787	2.19	3.26	16.6	54.4	14.8	48.6
20	solid	0.0320	0.813	3.10	4.61	10.5	34.4	10.1	33.2
20	7/28	0.038	0.965	3.49	5.19	10.3	33.8	9.33	30.6

The conductor, or individual strands in the case of stranded conductors, can be coated or "bare". Tin is the most common coating. Diffusion of the tin coating into the surface of the copper causes the DC resistance to be somewhat higher than bare conductors, but this is a concern mainly at frequencies above 10 MHz. Tinning, although providing for superior soldering, mainly provides substantial corrosion resistance over bare copper. The very short section of exposed conductor, even inside a connector body, between the end of insulation and, say a crimped on contact pin, can be a point of failure in a cable assembly. Other coatings, silver used to achieve improved soldering and corrosion resistance without the higher resistance penalty, and nickel used for high heat resistance with the higher resistance penalty; are used only in special applications.

INSULATIONS

In addition to providing basic insulating properties, the plastics used to coat the conductors have various signal altering characteristics. The two properties of insulating plastics that affect transmission are the dielectric constant and the dissipation factor. The dielectric constant is a function of the velocity at which energy travels through the dielectric (another name for insulation). The dissipation factor is a function of the rate at which energy is absorbed by the dielectric. Reducing either of these factors results in better signal transmission performance.

The plastic most commonly used for conductor insulation is polyvinylchloride (PVC). Its dielectric properties are good but, generally not good enough for any data communication application more demanding than basic low speed (<100 kbps), short distance (<50 m) links. PVC is normally used for power, control, instrumentation, and audio cables; applications that operate at relatively low frequencies. High performance serial data cables normally use a polyolefin insulation; either polyethylene or polypropylene, because their dielectric properties are far superior to PVC. Even though a data signal may be operating at a fairly low data rate the signal may be made up of pulses with fast rise times. The rise time of the pulse determines the frequency range covered by the signal. Typical data signals have power spectrums well into the 1 MHz to 10 MHz range. The polyolefins' dielectric constants and dissipation factors are low compared to PVC's and, unlike PVC, remain low well into the microwave region of the spectrum.

There is no great disadvantage to using polyolefins compared to PVC. The cost, at most, is only marginally higher. Some cable design precautions must be taken to meet flammability regulations. Polyolefins are far more flammable than PVC, but this can be overcome with a flame retardant outer cable jacket. As will be seen later, polyolefin insulation is essential for good performance with shielded cables.

The only exception to the choice of polyolefin insulation is the case of plenum cables used in premises wiring applications. Fluorinated ethylene/propylene copolymer (FEP), available in Teflon®, is substituted to achieve low smoke and flame producing characteristics to meet special National Electrical Code (NFPA) requirements. The dielectric properties of FEP are slightly superior to polyolefins.

SHIELDS

One problem that arises with long distances is a transmission line's susceptibility to interfering signals. Electro-magnetic interference (EMI) is basically unavoidable and a long transmission line is very susceptible. Long wires make good antennas.

Most of the serial interface standards do not require shielding, although provisions are made for shields within the standard connectors and recommendations for grounding. The standards basically avoid the subject of shielding as one which is outside of their scopes. On the other hand, the primary caution given in the distance and data rate guidelines is that outside interference is not taken into consideration. Shielding can greatly reduce or eliminate the possibility that the system will fail after you have followed all the other guidelines. Regardless of the effects interference may have directly on the serial interface, shielded cable may be required due to the overall system's susceptibility or emissions passed through the enclosure via an interface port. Shielding should be considered for all but very short low speed data circuits; above 10 meters or 100 kbps.

Shields are additional conductors added to cables and are designed to isolate electro-magnetic fields surrounding conductors or pairs within the shield from those outside of the shield. Shields may be placed over individual conductors, twisted pairs, or may be placed over the entire bundle of

TABLE II. Insulation Types vs Qualitative Performance Characteristics Electricals, etc.

Insulation Type	Specific Gravity	Dielectric Constant	Dissipation Factor	Volume Resistivity ohm-cm	Dielectric Strength Volts/Mil	Flammability	Temperature Range °C
PVC (Standard)	1.25–1.38	4–6	0.06–0.10	10^{11}	800–900	Good	−20 to 80
PVC (Premium)	1.38	3–5	0.080–0.085	10^{12}	800–900	Good	−55 to 105
Polyethylene	0.92	2.27	0.0002	$>10^{16}$	1200	Poor	−60 to 80
Polypropylene	0.90	2.24	0.0003	$>10^{16}$	850	Poor	−60 to 80
Cellular Polyethylene	0.50	1.5	0.0002	—	500	Poor	−60 to 80
Flame Retardant Polyethylene	1.30	2.5	0.0015	$>10^{16}$	1000	Fair	−60 to 80
FEP (or TFE)	2.15	2.1	0.0007	$>10^{18}$	1200	Excellent	−70 to 200 (or 260)
Cellular FEP	1.2	1.4	0.0007	—	500	Good	−70 to 200

cable elements or in both locations. Multiple shields within a cable may be electrically isolated from each other with additional insulating layers.

Typical cables use three basic kinds of shields; a tape shield, a braided or served wire shield, or a double shield consisting of a tape plus braided or served wires (see *Figures 4* and *5*). The tape shield always includes an uninsulated "drain" wire in contact with the aluminum, used to terminate the shield. The double shield includes a braided or served layer of wires in contact with the conductive side of a tape shield. Special shields are used for special applications such as corrugated rigid metal tapes used in telecommunications cables, solid tubes used on CATV cables, or woven or expanded metal screens used for flat cables.

The ideal shield is a seamless metallic tube as with the aluminum tubing utilized by the CATV industry on semi-rigid coaxial cable trunk lines; the emphasis is on "semi-rigid". To achieve flexibility a shield is made up of braided or served layers of fine wires or helical wrapped tapes.

Braided shields are made up of groups of fine; 34, 36, or 38 AWG, depending on the overall cable size; usually tinned,

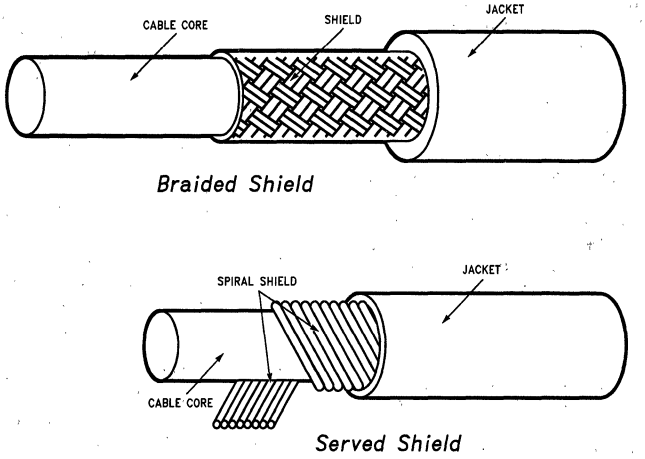

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FIGURE 4. Braid, Serve, Tape Shielding

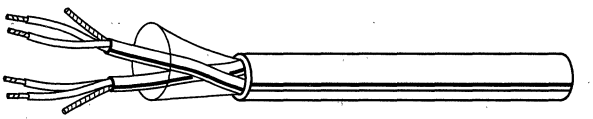

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FIGURE 5. Individual Pair Shields

copper strands; groups of these strands are woven Maypole fashion, in opposite directions, around the cable. Served shields consist of a single layer of strands laid in a single direction around the cable. Served shields are very flexible and are used in applications such as microphone or mouse cables. The small gaps in single layer served shields make them unsuitable for high frequencies (>10 MHz).

Tapes are a thin foil, usually aluminum, laminated to one or both sides of a plastic film, usually polyester or polypropylene. Tapes come in various thicknesses. The aluminum can be 1/3 to 2 mils thick. The plastic film, typically polyester or polypropylene, can be 1/5 to 2 mils thick. Thicknesses are selected by trading off flexibility with shielding effectiveness and signal attenuation in cases where the shield provides signal return path. Effective overlap of the tape is important for reliable performance. Uninsulated drain wires are normally of the same construction as the cable's conductors, but must be tinned to permit direct contact with the aluminum.

A simple model for shielding effectiveness is the shield's DC resistance. A shield is equally effective in both directions, in and out, and its effectiveness is proportional to its surface transfer impedance (which equals shield DCR at 0 Hz). Surface transfer impedance is the frequency dependent voltage/current ratio derived from a current driven on one side of the shield resulting in an induced voltage on the other side of the shield (see *Figure 6*). A detailed explanation of the surface transfer impedance model is outside of the scope of this application note.

Braids and serves have much lower resistances than tape shields. A typical double shield has about 1/5 the resistance of a tape shield, so it will be about 5 times more effective than a tape shield over the same distance. Another way of looking at it; a double shield extends the effectiveness of the tape shield to about 5 times the distance. A tape shield is effective for short cables. A double shield should be used on short distances in very noisy environments. A double shield should be used in any extended distance application, over 100 meters.

Braids are a trade-off between flexibility and ideal tubular conductors. The lower resistance of the braid results in good shielding effectiveness, but only up to a point. The small holes between the crossovers of the braid strands, become large at some frequency. Braids are specified by percent coverage as a means of determining the size of the holes. Closing up the holes, say by specifying 95% coverage, will be effective; two layers of braid can be specified for still greater effectiveness, but all at the expense of flexibility.

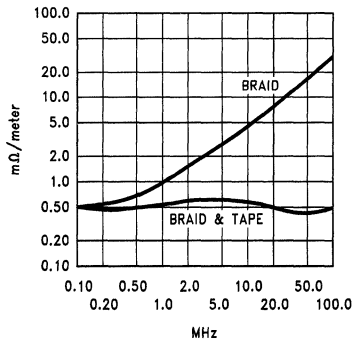

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FIGURE 6. Comparison Graph of Transfer Impedances, Tape Shield vs Braid Shield

A very effective means of closing the holes and lowering the resistance is to use the combination of tape and braid. The double shield achieves low resistance through the additional cross-sectional area of the braid. The tape is overlapped to provide as near to a true tubular performance as possible.

Jackets

The most common cable jacket material is PVC, which has good environmental resistance and can be compounded to have good cold temperature flexibility and meet a range of flammability requirements.

Flammability Requirements

Equipment cables are generally required to meet some level of vertical flames test. The National Electrical Code (NEC) sets standards for the flammability ratings of cables to be installed in buildings. Cables must pass the vertical cable tray flame test to be suitable for general purpose locations. This is the same test generally required for industrial environments. Two special locations are identified by the NEC; riser and plenum, each having respectively greater degrees of flammability requirements. Plenum cable can be used in plenums, risers or general purpose locations, riser cable can only be used in risers and general purpose locations, and general purpose cables are restricted from risers and plenums. In the case of plenum cables, Polyvinylidene Fluoride (PVDF) copolymer, available as Kynar®, jackets may be used for their low smoke and flame producing characteristics.

4.0 CABLE CHARACTERISTICS

Resistance

A DC resistance requirement is the best way to assure that the wire is indeed the size it should be. It also has a specific relationship to the TIA standards. Some requirements include maximum voltage drop for the signals. The cable termination load resistance and the total cable loop resistance determine the maximum permissible cable length for given length for a given voltage drop limitation.

Capacitance

A stated cable capacitance can be one of a number of possible capacitance values that can be measured on any given cable. Depending on how the cable is actually terminated to the generator, these various capacitance values may need to be considered. The different termination possibilities derive from, for instance, unbalanced vs balanced operation. Normally the mutual capacitance of a pair is provided in cable specifications. Mutual capacitance provides a measure of the capacitance that the generators will "see" when terminated to the cable. Another specification, sometimes given, is the capacitance of one wire to all the other wires and shield connected together.

Shielded cables must use insulation with good dielectric properties (i.e., low dielectric constant) to assure that cable capacitances are kept low when a shield is added to the cable. The proximity of two conductors in a cable and the dielectric constant of the insulation between the conductors determine the capacitance measured between the conductors. The addition of a shield around the two conductors introduces two very significant "parasitic" capacitances; those between each conductor and the shield. The conductor to shield capacitances combine with the conductor to conductor capacitance to significantly increase the overall capacitance of the pair.

Impedance, Velocity of Propagation, Attenuation, Rise Time Degradation

These four parameters have a less direct bearing on data communications applications. Sometimes they are specified, but after the basic cable dimensions are given, these parameters essentially depend on the Capacitance and DC Resistance.

The various lumped circuit element parameters; capacitance, inductance, resistance, and conductance of a transmission line, are all interrelated in a single parameter known as the characteristic impedance of a transmission line. This is the impedance that if used to terminate a transmission line, no signal will be reflected back to the source. If there is a mismatch, the bigger it is, the bigger the reflections will be. Impedance matched conditions are sought for all system designs, particularly at high data rates, because the reflections affect the performance of the generators and prevent some of the signal from ever reaching the receiver. The generator and cable termination load of EIA-422-A and EIA-485 are specified in such a way as to closely match the impedance of typical "low capacitance" cables having about 12 to 16 pF/ft mutual capacitance.

Velocity of propagation, the speed at which a signal (an electromagnetic wave) will travel along a cable (a transmission line) is dependent on the properties of the insulation. The dielectric constant of a plastic is actually the inverse of the square root of the velocity of propagation; the speed that electromagnetic radiation will travel through a dielectric compared to the speed of light in a vacuum. The velocity of propagation is normally expressed as a fraction of the speed of light. The actual velocity of propagation is complicated somewhat by the fact that the signal normally travels through a combination of air and plastic, but the result is to make it a little faster than the theoretic speed derived from the insulation dielectric constant alone. The velocity of propagation determines the impedance relative to the capacitance.

The impedance and resistance determine the attenuation vs frequency. This parameter is normally expressed in dB/1000 ft at a given frequency. This is a measure of the amount of signal loss that occurs from the cable. More signal is lost at higher frequencies than at low frequencies. Remember that the rise time of the pulse, not the data rate, determines the frequency range covered by the signal.

Since there is more attenuation at higher frequencies than at lower frequencies, signal pulses are dispersed as they travel down the cable. This property is measured as rise time degradation. Rise time degradation is roughly proportional to cable length. System designers are constantly balancing rise time effects. On one hand, fast rise times produce more crosstalk, that will, if great enough, result in errors. On the other hand, slow rise times that get further degraded will cause receiver errors.

5.0 CABLE APPLICATIONS

Lowering capacitance improves the performance of cables used for both unbalanced and balanced transmission.

Unbalanced transmission is limited by near-end-crosstalk. The unbalanced lines interfere with each other primarily through capacitive coupling between the lines. Lowering any capacitance parameter of a multi-conductor or twisted pair cable will result in proportionally lowering all of the various capacitances within the cable. In the case of unbalanced lines, coupling capacitance, and therefore crosstalk, is lowered proportionally. The mutual capacitance of a paired cable used for unbalanced transmission does not directly indicate the coupling capacitance between lines, but comparing the mutual capacitance of two cables is generally a good indication of their relative crosstalk performance.

Balanced transmission is primarily limited by rise time degradation. The primary cable capacitance of concern, in this case, is the shunt capacitance across the signal generator's two output terminals. Keeping everything else equal, lowering capacitance results in a decrease in attenuation vs frequency proportional to the square root of the capacitance reduction. In the general domain of data rate and distance for current applications, the resulting change in rise time degradation is nearly proportional to the square of the change in attenuation vs frequency. This gives a relation, similar to the unbalanced case, where a comparison of the mutual capacitance of two cables is generally a good indication of their respective proportional rise time performances.

TABLE III. Applications

Application	Multiconductor or Twisted Pair	Number of Conductors or Pairs	AWG Specified	Shielding Requirements	Transmission Characteristics Specified
EIA/TIA-232-E Section 2	Multiconductor	3 to 25	none specified	none required provisions included	2500 pF max total shunt capacitance
TIA/EIA-422-B	Twisted Pair	not specified	none specified guidelines use 24	none specified	none specified, 90–150Ω impedance recommended, guidelines use 100Ω impedance, 66% max. voltage drop
TIA/EIA-423-B	Multiconductor (Twisted Pair Better)	not specified	none specified guidelines use 24	none specified	none specified, guidelines use 100Ω impedance, 66% max. voltage drop
EIA-485	Twisted Pair	not specified	none specified	none specified	none specified, similar to TIA/EIA-422-B, guidelines use 120Ω impedance
EIA/TIA-562	Multiconductor	not specified	none specified	none specified	none specified
TIA/EIA-612 HSSI	Twisted Pair	not specified (companion spec TIA/EIA-613 requires 25)	none specified 28 recommended	shield required	110Ω impedance 4.5 dB max. total attenuation @50 MHz 79 ns max. total delay 2.0 ns/m max. total skew
X3T9.2 SCSI I	Multiconductor or Twisted Pair	50 conductor (flat) 25 pair (round)	28 AWG	required for external	100Ω impedance
X3T9.2 SCSI II	Twisted Pair	"A" Cable: 25 "B, P, Q" Cables: 34 "L" Cable: 55	28 or 30 AWG	required for external	90–132Ω nominal impedance (122Ω typical), 0.095 dB/m max. attenuation @5 MHz 0.20 ns/m max. skew
X3T9.2 SCSI III	Twisted Pair	"P or Q" Cables: 34	30 minimum	required for external	122 (84)Ω nom. impedance differential (single-ended) 0.095 dB/m max. attenuation @5 MHz 5.4 ns/m max. delay 0.15 ns/m max. skew

TABLE III. Applications (Continued)

Application	Multiconductor or Twisted Pair	Number of Conductors of Pairs	AWG Specified	Shielding Requirements	Transmission Characteristics Specified
X3T9.3 IPI (ISO 9318)	Multiconductor flat or Twisted Pair round	50 conductor (flat) 25 pair (round)	26 or 28 AWG	required for round	120Ω impedance 0.095 dB/m max. attenuation @5 MHz 5.4 ns/m max. delay 0.49 ns/m max. skew
X3T9.3 HIPPI	Twisted Pair	25	28 AWG	two shields required	108Ω impedance 0.28 dB/m max. attenuation @50 MHz 0.13 ns/m max. skew

6.0 SUMMARY

The range of cable types and basic options available for data communications applications is limited, making the basic cable design selection reasonably easy. The scope of the basic selection criteria is covered by the choices, flat or round, multiconductor or twisted pairs, and shielded or non-shielded. Basic attributes of the application; distance, environment, and flexibility requirements determine the basic cable type selected. Cable construction details, conductor size, stranding and coating, insulation type, shield options, and jacket types are determined by more specific application considerations; connector type, signal speeds, emissions and susceptibility, work and abuse, flammability, life expectancy and cost. Every cable has inherent electrical characteristics, which can be expressed in several ways, but are interrelated and dependent upon a few simple parameters. A cable's electrical characteristics determine its suitability for use with particular interface components.

Author Biography:

David Hess, V.P. Technology, Berk-Tek, Inc., 132 White Oak Road, New Holland, Pennsylvania 17757, has worked for 17 years in product engineering and product development in the fields of copper and optical fiber data communication cables, participates in various data communications standards committees in TIA/EIA and ANSI X3T9, holds a B.S. degree in Mathematics from Pennsylvania State University and is a member of IEEE.

Popular Connector Pin Assignments for Data Communication

National Semiconductor
Application Note 917
John Goldie
Syed Huq

INTRODUCTION

This application note provides a graphical reference to popular connector pin assignments (pin outs) that are commonly used in telecom and computing applications.

In the field of data communication, the cable and connector play a critical part in the system's performance along with the line driver and receiver integrated circuits. Together the components (PCBs, ICs, cables, and connectors) form a channel, which all information must pass through. This channel forms a true chain, and a fault in any link may break the chain.

As stated in the introduction, this application note focuses on the connectors, and more specifically the pin assignments of the connectors. When equipment is built by a manufacturer and is intended to interwork with equipment from different manufacturers the use of an industry standard is critical. To properly inter-operate, the two pieces of equipment must support the same protocol (functional specifications), electrical levels, mechanical dimensions of the connector, and most importantly the connector's pin assignment. Since industry standards, TIA/EIA (Telecommunications Industry Association/Electronic Industries Association) for example, commonly specify or reference all three areas: Functional, Electrical, and Mechanical specifications, the chance of success is greatly increased when hooking up the two pieces of equipment.

A substantial amount of standardization work has been done in the telecommunications and computing area for interface standards. In addition to the connector pin outs, this application note also provides a short description of the standard or historical perspective. The reader is referenced to the actual standards from complete information on the standard.

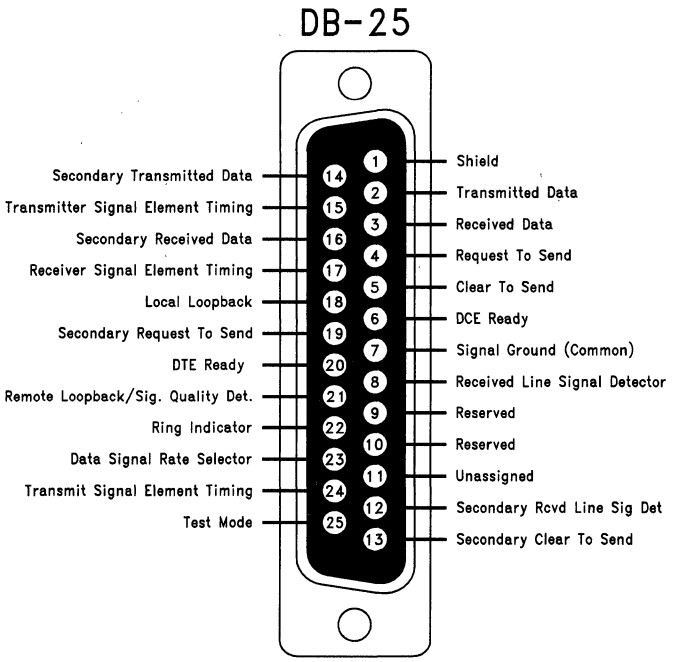

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FIGURE 1. RS-232 DB-25

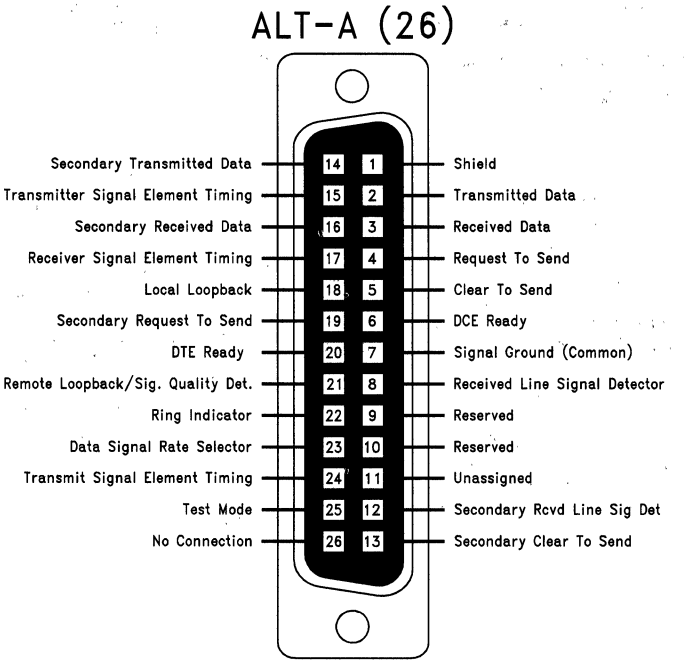

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FIGURE 2. RS-232 ALT-A

RS-232

RS-232 is one of the most popular interface standards in the world. Originally intended for DTE/DCE interfacing, this standard has been used in a wide range of applications including telecom, computing, test and measurement, and industrial control applications. Now in its fifth revision (E), RS-232 is still very popular, and new devices (line drivers and receivers) are being developed to support the standard. The correct name of the standard is EIA/TIA-232-E which has replaced the more common RS-232 nomenclature. This standard specifies two connectors, the standard DB-25, also a new smaller alternate connector with 26 pins. The original version of RS-232 dates back to the early 1960s and is known as a complete standard as it specifies all functional, electrical, and mechanical specifications. There is also a very popular 9 pin defacto version of this standard commonly employed on personal computers that was developed by IBM®. The two full (25 line) connector pin outs are shown on *Figures 1* and *2*. See *Figure 7* for an illustration of the defacto 9 pin implementation, now standardized as EIA/TAI-574.

RS-449

RS-449 was intended to replace RS-232 at one time. It also specifies a DTE/DCE interface, but references the RS-422-A and RS-423-A standards for electrical specifications. This standard specified a DB-37 pin connector along with an additional DB-9 pin connector when additional lines were required. The 37 pin connector proved too large for many applications and limited the acceptance of this interface. RS-449 is mainly found in high-end telecom applications but rarely elsewhere. It has been replaced with a new standard that specifies the common DB-25 connector (EIA/TIA-530-A). The pin out of the DB-37 pin connector is shown in *Figure 3.*

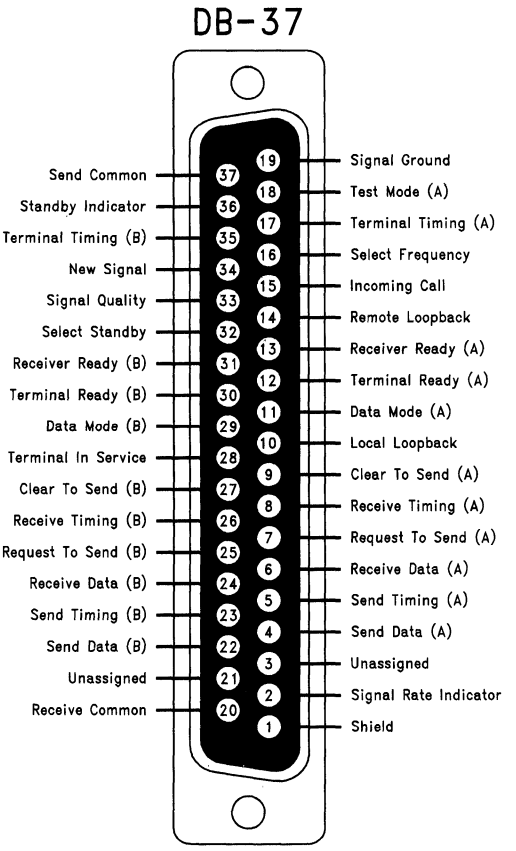

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FIGURE 3. RS-449 DB-37

EIA-530 AND EIA/TIA-530-A

EIA-530 is an extension of RS-449 but is based on the DB-25 connector. This standard specifies both functional and mechanical specifications, and references RS-422-A and RS-423-A standards for electrical specifications. This connector is the same one commonly used in EIA/TIA-232-E (RS-232) applications. This standard has been revised (denoted by the letter suffix — "A"), which altered the pin assignments slightly from EIA-530. Both pin assignments are shown in *Figures 4* and *5*.

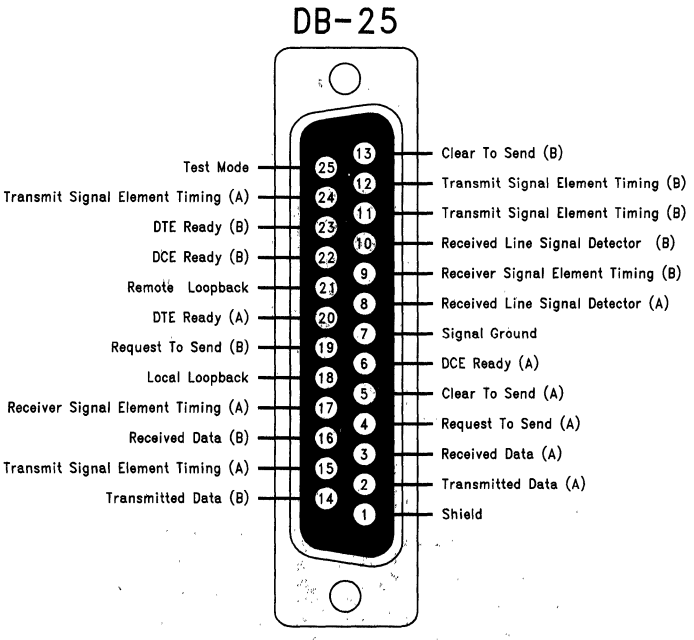

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FIGURE 4. EIA-530 DB-25

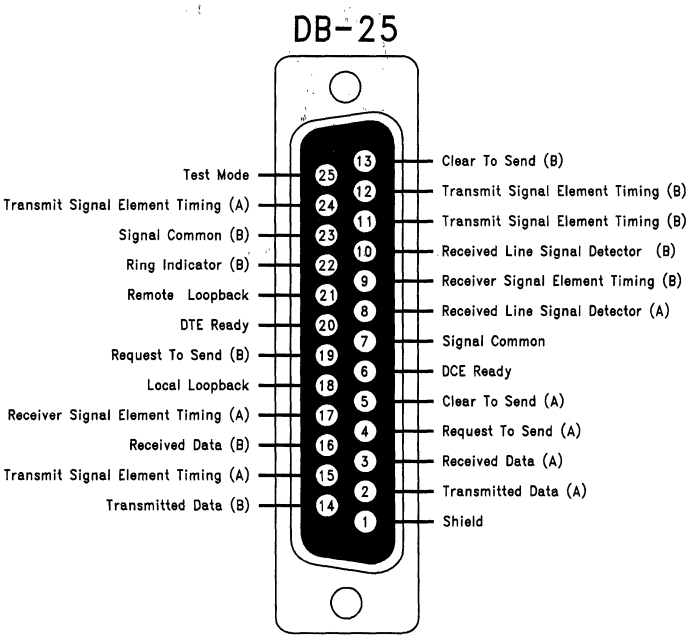

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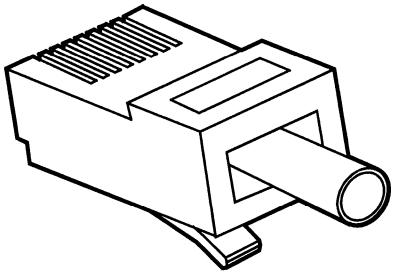
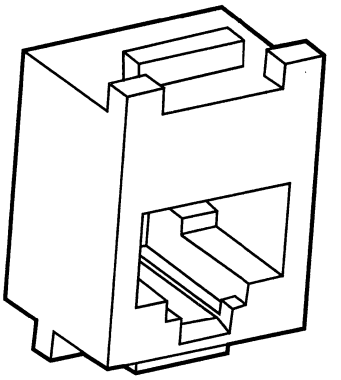
FIGURE 5. EIA/TIA-530-A DB-25

EIA/TIA-561

EIA/TIA-561 is a new standard released in 1990 and specifies a small 8 position interface for non-synchronous interface between DTEs and DCEs. The uniqueness of this standard is the fact that it does not specify a DB style connector, but rather a modular receptacle and plug type connector. This standard references the companion standard EIA/TIA-562 for electrical levels (similar to RS-232 but lower power and faster). The plug and jack are shown in *Figure 6.*



Plug



Receptacle

TL/F/11940–6

1. Ring Indicator
2. Received Line Signal Detector
3. DTE Ready
4. Signal Common
5. Received Data
6. Transmitted Data
7. Clear to Send
8. Request to Send/Ready for Receiving

FIGURE 6. EIA/TIA-561 MJ-8

EIA/TIA-574

EIA/TIA-574 was developed due to confusion arising between the official RS-232 interface and the exceedingly popular defacto 9-pin version developed by IBM. This standard specifies the DB-9 interface, however, it recommends the use of the RS-562 standard instead of RS-232 electrical levels. It is noted that EIA/TIA-562 can inter-operate with RS-232 drivers and receivers in many applications. This standard supplies the minimum number of lines for non-synchronous serial data interchange between DTEs and DCEs. The connector pin out is shown in *Figure 7.*

V.35

Recommendations V.35 was developed by the CCITT (International Telegraph and Telephone Consultative Committee) as a high speed modem standard that also specified the DTE/DCE interface. This standard used RS-232 type line drivers and receivers for control circuits, and its own unique differential drivers and receivers for high speed data and timing lines. This recommendation specifies a unique connector and is shown in *Figure 8.* It should also be noted that the CCITT has been replaced with the ITU (International Telecommunications Union) and new standards will adopt the ITU prefix instead of CCITT.

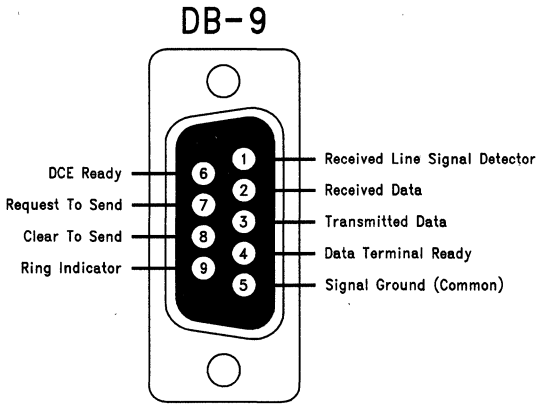


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FIGURE 7. EIA/TIA-574 DB-9

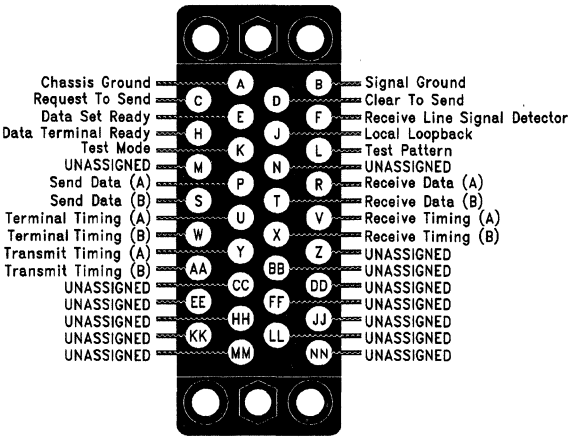

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FIGURE 8. CCITT V.35

IEEE-488

The IEEE (Institute of Electrical and Electronic Engineers) also standardizes many interfaces in the area of computing and instrumentation. IEEE-488 is a complete standard specifying all functional, electrical, and mechanical specifications for a 16 line parallel bus for instrumentation. This interface is commonly found on test, and measurement equipment that feature computerized programming and control. This standard is also known under the acronym as GPIB (General Purpose Interface Bus). The pin out of the standardized connector is shown in *Figure 9.*

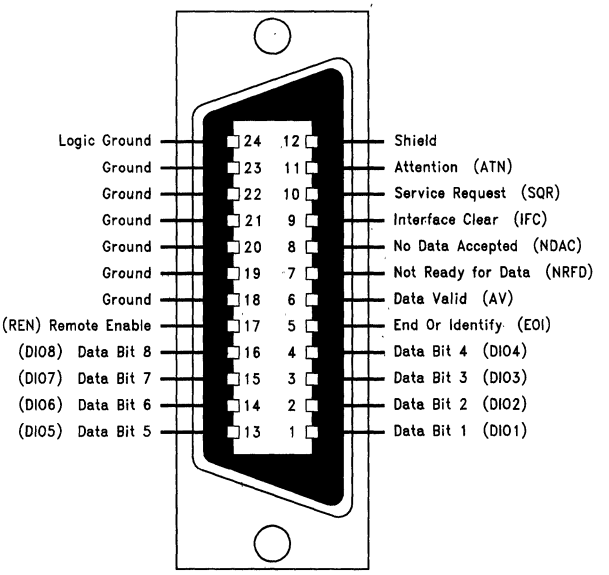

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FIGURE 9. IEEE-488

CENTRONICS PORT AND IBM PC PARALLEL PORT

These two defacto standards both specify parallel interface that are commonly used in computing applications (computer to peripheral-printer). Both are defacto standards, and support similar functions but different pin outs and mechanical specifications. There is active work by the IEEE to standardize this interface (Computer to peripheral-parallel port). The two connectors are shown in *Figures 10* and *11*.

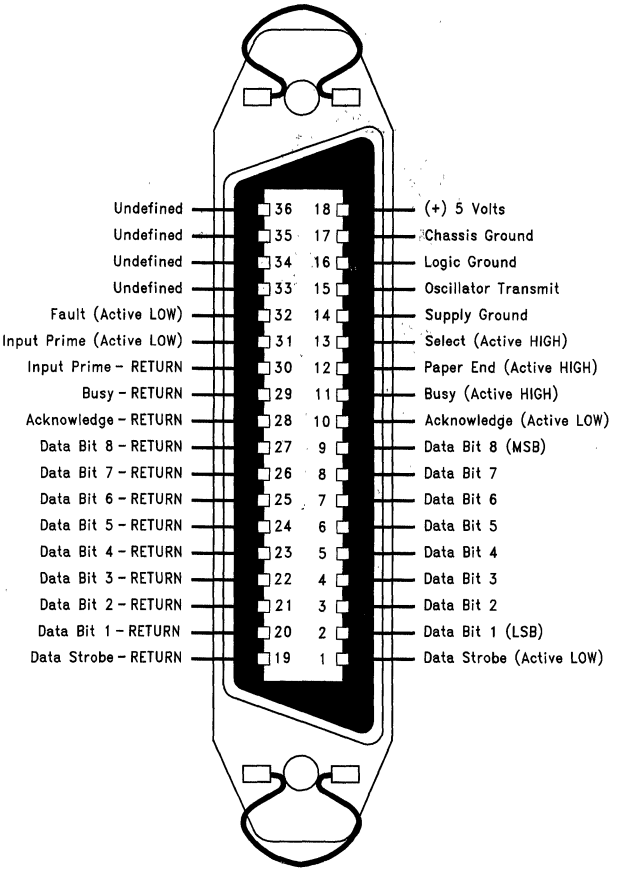

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FIGURE 10. Centronics Port

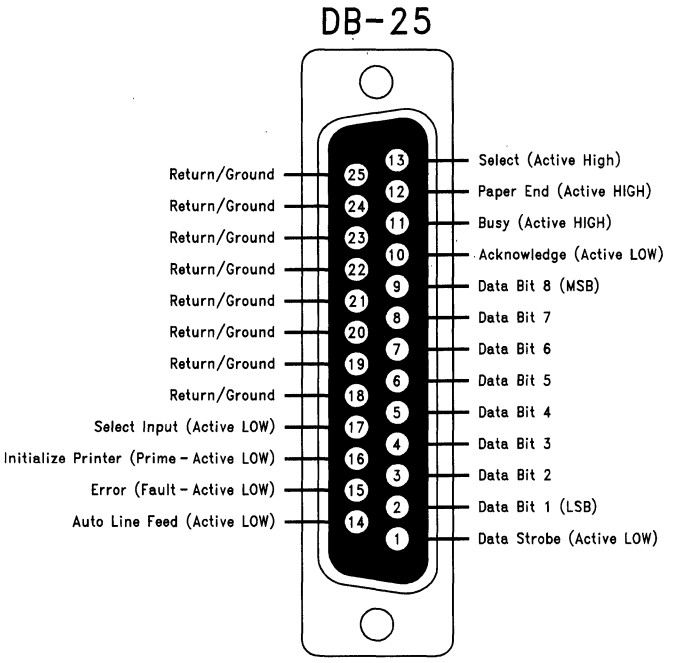

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FIGURE 11. IBM PC Parallel Port

SUMMARY

By selecting an industry standard, the problem of getting signals from one board or box to another is greatly reduced. This is especially true when inter-operation between systems built by different manufacturers is required (open system).

Interface standards from the TIA/EIA and other standards groups greatly resolve this interfacing problem. This application note provides insight into those standards by providing a graphical representation of the connectors referenced in the standards. As always, whenever designing a system to an industry standard, a thorough review of the most recent revision of the standard is highly recommended.

REFERENCE

Most standards are available from:

Global Engineering Documents
Irvine, CA, USA
714-261-1455 or 800-854-7179

Various connector, cable and data communication products are available from:

South Hills Datacom
Pittsburgh, PA, USA
Toll-Free: 800-245-6215
Local: 412-921-9000
FAX: 412-921-2254

LocalTalk™ Physical Layer Alternatives

National Semiconductor
Application Note 967
Todd Nelson

INTRODUCTION

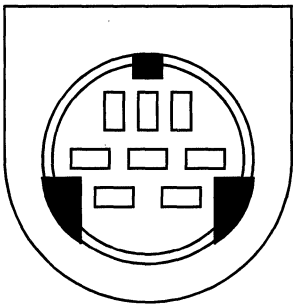
This application note discusses three approaches to the LocalTalk physical layer. One approach uses the TIA/EIA-422-B (RS-422) standard over a twisted pair wire medium. Another uses the RS-422 drivers and receivers but the bus is transformer-coupled over standard phone cables. The third approach is compatible with TIA/EIA-232-E (RS-232) in a point to point environment.

The analysis focused on driver supply current and maximum switching frequency. While all three approaches utilize the same drivers and receivers, the load presented is different. Therefore, the affects on current and frequency are different.

The DS8925 LocalTalk Dual Driver/Triple Receiver is used for the analysis of all applications.

LocalTalk Port Requirements

The LocalTalk physical layer is partially defined by RS-422. In addition to the electrical characteristics described by RS-422, LocalTalk specifies a data rate of 230.4 kbits per second over a maximum distance of 300 meters. Typically, LocalTalk uses the mini 8-pin connector, see *Figure 1.*



TL/F/12312–1

FIGURE 1

The bits are encoded using a frequency modulation technique called FM-0. In this method, the bit-time is nominally 4.34 μs. A "1" is defined as one transition during the bit-time; a "0" will have two transitions, as shown in *Figure 2.*

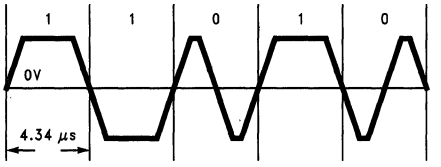


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FIGURE 2

Historically, the line drivers and receivers used were the 26LS30 and 26LS32. The National devices were the DS3691 and DS26LS32A respectively. Since RS-422 and LocalTalk define a multi-drop serial bus, each connecting node will require a differential driver (TXD, transmit data) and a differential receiver (RXD, receive data). Additionally, a typical host port will also have single-ended signals for handshaking (HSKi and HSKo) and possibly a general purpose input (GPi). The single-ended signals conform to TIA/EIA-423-B (RS-423) and are interoperable with RS-232.

The DS8925 integrates the 26LS30 and 26LS32 functions in one economical bipolar device for LocalTalk applications. The differential driver is RS-422 compliant and, when measured single-ended, each output is also RS-423 compliant.

Twisted-Pair Application

The standard RS-422 implementation utilizes a twisted-pair wire with 100Ω parallel termination. Such an implementation is for point-to-point communication. In a multi-user environment, control of the bus must be established before point-to-point communication can begin. The DS8925 includes single-ended channels for this process.

Transformer-Coupled Application

Often the link is transformer-coupled and carried on standard telephone cable. In this type of application, only the transmit and receive data lines are used. The transformer is a 1:1 turns ratio transformer and provides isolation between the drivers and the cable. RS-422 was not intended for multi-point applications; in case of contention the transformer isolates the drivers from the bus.

RS-232 Application

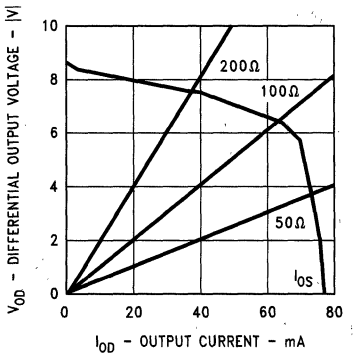
Many types of peripherals can be connected to a LocalTalk host and only need the proper software drivers, such as a PostScript™ printer. While not being strictly compliant, most LocalTalk hosts are compatible with the standard so that a RS-232 peripheral device can communicate. The differential driver on the DS8925 used in the previous two applications is also designed and specified for single-ended communication.

When configured for a RS-232 application, the differential driver and receiver are used single-endedly. Since the driver is RS-423 compliant it will provide the ±3.7V signal, the unused driver output is left open. The differential receiver can detect RS-232 signals at the "−" input if the "+" input is referenced to ground.

Affects of Loading on Supply Current

The DS8925 will provide twice the normal RS-422 output voltage when supplied with V_{CC} = +5V and V_{EE} = −5V. The output current is dependent on the load, up to the point that short-circuit limiting (I_{OS}) occurs. *Figure 3* shows the DC differential output current of the DS8925 and the intersecting load lines.

Differential Driver Output Voltage vs Output Current

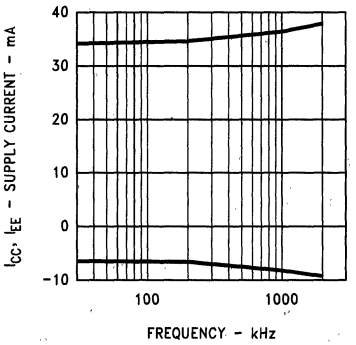


TL/F/12312–3

FIGURE 3

The other element of interest is the supply current due to the switching frequency of the driver. The total current required will be the no-load switching current plus the dynamic current determined by the load. *Figure 4* shows the no-load current versus switching frequency for the DS8925.

No-Load Supply Current vs Frequency



TL/F/12312–4

FIGURE 4

Driving up to 1 MHz requires almost 45 mA (no-load). This is the base-line for comparison. The differences will be due to the load: the resistive component and the capacitive component.

The total supply current required to drive the 100Ω terminated twisted-pair is about 150 mA. The difference between this and the no-load current is due to the 100Ω parallel termination (about 65 mA) and the capacitance in the cable (about 40 mA).

Driving the transformer-coupled cable up to 1 MHz requires about 50 mA total supply current. The transformer presents a high impedance to the driver, thus the total supply current is only slightly more than the no-load current at this frequency.

Frequency modulation (FM) has little effect on the 100Ω terminated application, but this is very important to the transformer. FM assures at least one transition per bit, unlike a Non-Return to Zero (NRZ) scheme. Without transitions, a string of identical bits (i.e., 00000000) could generate a wave form that appears to be low frequency and thus the transformer would generate a proportionally low amplitude output. With FM, identical bits appear as a 50% duty cycle wave form. The worst case for FM is alternating bits (i.e., 10101010) because the pulse width changes with each bit. See *Figure 5.* This was verified in testing and although the amplitude is affected, the impact is not significant.

Affect of Modulation on Transformer

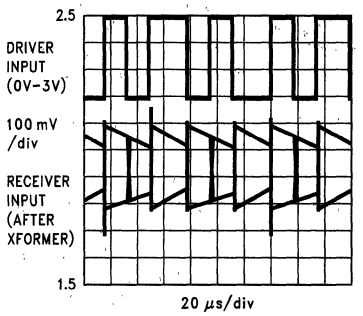


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FIGURE 5

The RS-232 application requires about 45 mA total supply current to drive a signal at 1 MHz. The loading for RS-232 is 3 kΩ from the signal to ground and the voltage level is guaranteed to be $\leq \pm 3.7$V. With the second driver driven either LOW or HIGH, the total current does not change. The only change is that I_{EE} is nearly 1 mA greater than I_{CC} when the second driver is LOW, the opposite is true when it is HIGH.

Affects of Loading on Data Rate

The data rate for this device becomes limited by the slew rate before the affects of loading occur. As noted above, there is considerable difference between the current required to drive the different types of loads. The switching current is less of a factor at these low frequencies. The main factor affecting the differential data rate is the slope of the differential output. At about 2 MHz the rise and fall times take up nearly the entire period. Above this frequency, the amplitude is reduced and the wave appears triangular. This is the case at the driver's output with either of the first two types of load.

Since the driver has very large amplitude, typically 9V with no load, the amplitude can be significantly reduced before the receiver fails to detect the transitions. The test set-up performed up to 6 MHz and still detected valid data at the receiver. LocalTalk is intended to operate below 1 MHz; therefore, physical layer loading should not affect data rate performance.

RS-232 is specified up to 20 kbits/s, but many applications exceed 100 kbits/s. The test set-up performed over 4 MHz and still met the minimum output levels. Beyond 4 MHz, the amplitude decreases and would not meet RS-232 levels. Again, this was due to the edge rates and not the loading.

Maximum cable length testing was not performed. However, RS-422 defines a maximum cable length of 1200 meters. LocalTalk is defined to be less than 300 meters. RS-232 is limited to about 15 meters (defined in terms of cable capacitance).

Transformer Set-Up

The bench fixture for testing the transformer-coupled physical layer was assembled from available "tel-net" adapter products. The transformer and RJ-11 connectors were left attached to their PCB and connected to the fixture. The terminators provided with the adapters were used at each end and a 25-foot length of standard residential phone cable was used between the two nodes. The fixture used two socketed DS8925s and had provisions for inserting loads in series prior to the adapter. See *Figure 6.* Only the differential driver and differential receiver were used on each device.

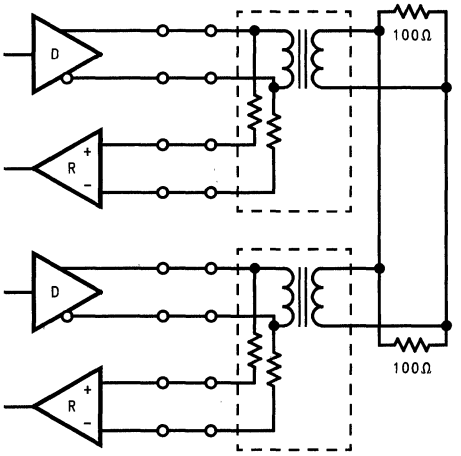

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FIGURE 6

Radio Frequency Interference (RFI) filters were inserted in the transformer application. There was very little affect on supply current or data rate because of the high impedance presented by the transformer. Such filters would reduce the supply current required for the 100Ω parallel terminated application as this increases the total impedance.

The fixture has the capability to have each device referenced to a separate ground, to test ground offset. No degradation was observed.

The signals could be probed at the driver outputs and receiver inputs. Most information was gathered at the first device's driver input compared to the second device's receiver output, or by monitoring the supply current to each device.

CONCLUSION

The DS8925 was used for all analysis because it was designed for both RS-422 and RS-423. The results showed that this type of device can meet the requirements of many different implementations of LocalTalk.

All of the applications that were analyzed exceed the data rate expectations by a significant amount. The transformer-coupled and RS-232 applications require much less total supply current than the 100Ω terminated application. Alternative devices exist for each implementation, but most of the current is due to the loading. Therefore, a single device such as the DS8925 can effectively support all of these applications.

REFERENCES

"Guide to the Macintosh® Family Hardware" second edition, Addison-Wesley Publishing Company, Inc.

"Inside AppleTalk", Addison-Wesley Publishing Company, Inc.

An Overview of LVDS Technology

National Semiconductor
Application Note 971
Syed B. Huq

INTRODUCTION

Recent growth in high-end processors, multi-media, virtual reality and networking has demanded more bandwidth than ever before. But the point-to-point physical layer interfaces have not been able to deal with moving information at the data rates required. Some of today's biggest challenges that remain to be solved include: the ability to transfer data fast, lower power systems than currently available, and economical solutions to overcome the physical layer bottleneck. Data Transmission standards like RS-422, RS-485, SCSI and others all have their own limitations most notably in transferring raw data across a media. Not anymore. Low Voltage Differential Signaling (LVDS) is a high speed (>155.5 Mbps), low power general purpose interface standard that solves the bottleneck problems while servicing a wide range of application areas.

This application note explains the key advantages and benefits of LVDS technology. Throughout this application note the DS90C031 (LVDS Quad CMOS Differential Line Driver) and the DS90C032 (LVDS Quad CMOS Differential Line Receiver) will be used to illustrate the key points.

STANDARDS OVERVIEW

There are two key industry standards that define LVDS. One is a IEEE (Institute for Electrical and Electronics Engineering) standard and the other is a TIA (Telecommunication Industry Association) recommended standard.

IEEE 1596.3 SCI-LVDS

SCI originally referenced a differential ECL interface within the SCI (Scalable Coherent Interface) 1596-1992 IEEE standard. But, this only addressed the high data rates required and did not address the low power concerns. Thus, SCI-LVDS was defined as a subset of SCI, and is specified in IEEE 1596.3 standard. SCI-LVDS specifies signaling levels (electrical specifications) for the high speed/low power physical layer interface. It also defines the encoding for packet switching used in SCI data transfers. Packets are constructed from 2-byte (doublet) symbols. This is the fundamental 16-bit symbol size. No media is specified and the data rate can be in the order of 500 MT/s based on serial or parallel transmission of 1, 4, 8, 16, 32, 64,.... bits.

SCI-LVDS also supports RamLink for super low power data transmission in a restricted environment. The IEEE 1596.3 standard was approved in March 1994. National Semiconductor held the Chairperson position for this standard.

TIA PN-3357

This is a proposed standard under the Data Transmission Interface committee TR30.2. The Electrical characteristics of the TIA standard are similar to SCI-LVDS. This standard defines driver output and receiver input characteristics. Functional specifications and/or Protocols are not within the scope of the TIA standard. It specifies a recommended maximum data rate of 655 Mbps and a theoretical maximum of 1.923 Gbps based on a loss-less media. Minimum media specifications are also defined within the standard. It also discusses failsafe operation of the receiver under fault conditions and other configurations issues such as multi-receiver operation. National Semiconductor also holds the editor position for this standard.

Both the IEEE and the TIA standards allow for external termination or internal termination with the resistor(s) integrated within the Receiver package.

LOW VOLTAGE DIFFERENTIAL SIGNALING

LVDS technology uses differential data transmission. The differential scheme has a tremendous advantage over single-ended schemes as it is less susceptible to common mode noise. Noise coupled onto the interconnect is seen as common mode modulations by the receivers and is rejected. The receivers respond only to differential voltages.

LVDS technology is not dependent on a specific power supply, such as +5V. This means there is an easy migration path to lower supply voltages such as +3.3V or even +2.7V while still maintaining the same signaling levels and performance. Technologies like ECL or PECL are more dependent on the supply voltage. This feature is highly desirable in any application that foresees moving to lower supply voltages without substantial redesign or worrying about mixed voltage operation (+5V/+3.3V) on system boards.

To achieve high data rate, low power, and to reduce EMI effects, signaling levels have to be reduced. The DS90C031/C032 chipset's limitation on data rate is mainly dependent on the technology driving the LVDS drivers. The aggregate bandwidth that LVDS technology can drive is in the Gbps range with a loss-less media. Data rates in the 500–600 Mbps are possible and this limitation is primarily dependent on the media being driven.

SIGNALING LEVELS

As the name implies, LVDS features a low voltage swing compared to other industry data transmission standards. The signaling levels are illustrated in *Figure 1,* and a comparison to PECL levels is also shown as reference. Because of the low swing advantage, LVDS achieves a high aggregate bandwidth in point-to-point applications.

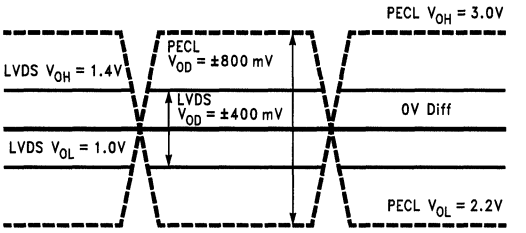

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FIGURE 1. PECL vs LVDS Signal Swing

It is impossible to achieve high data rates and provide low power without utilizing low voltage swings. LVDS signaling levels are smaller (50%) than PECL levels as shown in *Figure 1.* EMI effects are also reduced as the signaling swings are much smaller than traditional CMOS, TTL or even PECL.

LVDS TERMINATION

LVDS uses a constant current mode driver to obtain its many features. The value of the current source for the DS90C031 is a maximum of 4.5 mA. The transmission media must be terminated to its characteristic impedance to prevent reflections. Typically this is between 100Ω–120Ω and is matched to the actual cable. *A termination resistor is required* to generate the Differential Output Voltage (V_{OD}) across the resistive termination load at the receiver input (see *Figure 2a*). Data transmission from the driver to receiver without the termination is not recommended. The simplicity of the LVDS termination scheme makes it easy to implement in most applications. The user may also use a cable damping resistor as shown in *Figure 2b* with a capacitor to ground. It is recommended to have a single 100Ω termination between the driver outputs, and the use of surface mount components is also recommended to reduce the effects of parasitics. Proper termination not only avoids reflection problems but also reduces unwanted electromagnetic emissions. ECL and PECL require more complex terminations than the "one" resistor solution for LVDS. PECL drivers require 220Ω pull down resistors from each driver output to ground along with the 100Ω across the driver outputs as shown in *Figure 2c.*

COMMON MODE RANGE

An LVDS receiver can tolerate a minimum of ±1V ground shift between the driver's ground and the receiver's ground. Note that LVDS has a typical driver offset voltage of +1.2V, and the summation of ground shifting, driver offset voltage and any longitudinally coupled noise is the common mode voltage seen on the receiver input pins with respect to the receiver ground. The common mode range of the receiver is +0.2V to +2.2V, and the recommended receiver input voltage range is from ground to +2.4V. For example, if a driver has a V_{OH} of 1.4V and a V_{OL} of 1.0V, and a +1V ground shift is present (driver ground+1V higher than receiver), this will become +2.4V (1.4+1.0) as V_{IH} and +2.0V (1.0+1.0) as V_{IL} on the receiver inputs (+2.2V V_{CM}). Similarly, with a −1V ground shift and the same driver levels results as 0.4V (1.4−1.0) V_{IH} and 0.0V (1.0−1.0) V_{IL} on the receiver inputs (+0.2V V_{CM}). This is shown graphically in *Figure 3.*

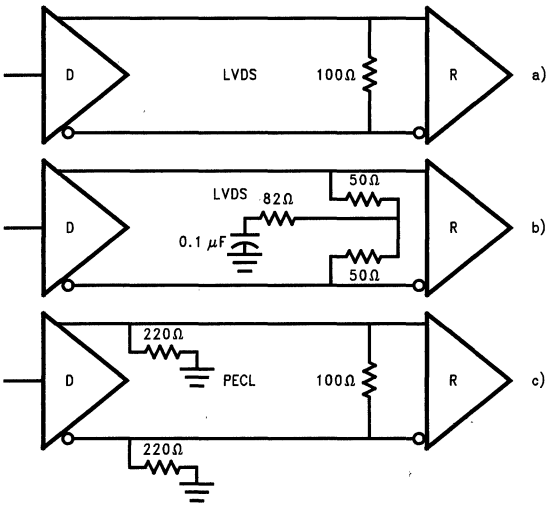

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FIGURE 2a, b, c. Termination Schemes

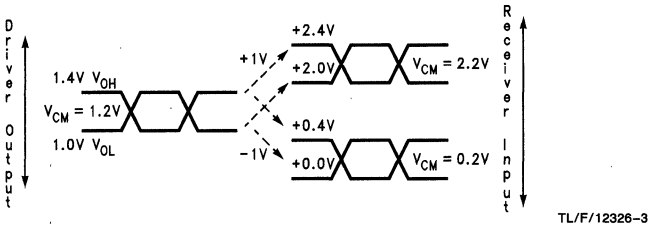

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FIGURE 3. Common Mode Voltage Range

FAILSAFE FEATURE

Failsafe is a receiver feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. This occurs when the inputs of the receiver are either open, shorted or terminated.

In some applications, not all receivers of the Quad DS90C032 may be used. In this case, the unused receiver inputs should be left *open*. If the receiver does not support failsafe and the inputs are left *open* (See *Figure 4a*), any external noise above the receiver threshold can trigger the output and cause can error on the communication line. Since the DS90C032 supports open input failsafe, the receiver output will provide an output High for this case.

Another fault condition can occur if the cable gets accidentally *shorted* (See *Figure 4b*). Due to environmental hazard conditions or poorly planned construction work, it is not uncommon to short a communication line by cutting through the cable. Under the above condition, the receiver output will also be at logic High and not in an unknown state.

Another case could occur if the driver is either powered off, in TRI-STATE® or even removed from the line while the receiver stays powered on with inputs *terminated* by the 100Ω termination resistor.

The receiver output will provide a logic high under all the above mentioned conditions.

Because all three (open, short and terminated) failsafe conditions are supported on the receiver, external biasing resistors are not required. This saves valuable board space, cost and design headaches compared to receivers that do not support failsafe. A receiver without failsafe can go into oscillation under certain fault conditions described above.

POWER ON/OFF REQUIREMENTS

On a point-to-point application, it is important to understand the behavior of the DS90C031 driver and the DS90C032 receiver under different conditions, such as power on/off. As shown in *Figure 5,* the driver is ON and the receiver is OFF, current flows from the driver output to the receiver input. This is not recommended as the ESD protection diode on the receiver input stage turns on and clamps the line to a diode drop above GND. This is the case where power supplies present a low impedance path to GND when powered off. But even when this occurs the driver limits the current flowing through the diode to less than 5 mA (short circuit current), preventing any thermal problems.

On the other hand, if the driver is OFF and the receiver is ON as shown in *Figure 6,* there is no leakage path from driver output to receiver input or from the receiver input to the driver output (and the line is not clamped). Under this condition, the failsafe feature of the receiver will guarantee a logic High output.

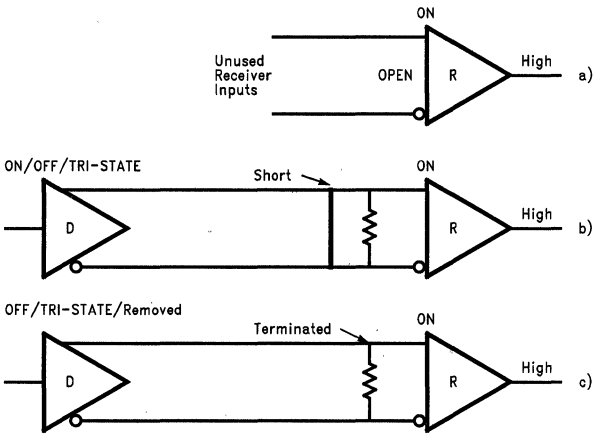

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FIGURE 4a, b, c. Failsafe Operation

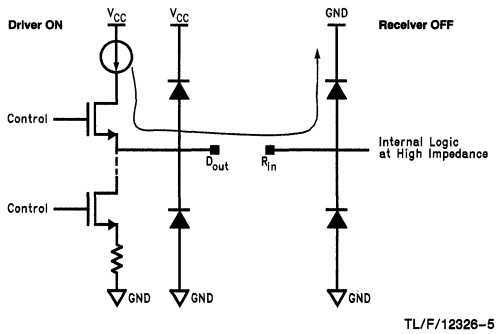

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FIGURE 5. Driver ON and Receiver OFF

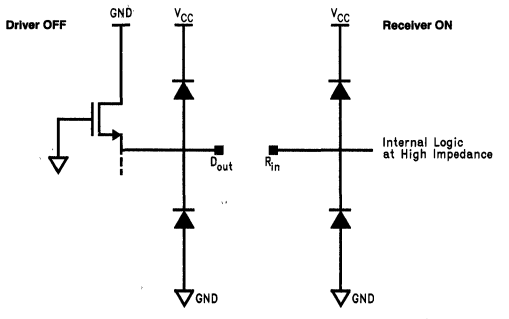

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FIGURE 6. Driver OFF and Receiver ON

POINT-TO-POINT CONFIGURATIONS

For interfaces where the transition time of the driver is substantially shorter than the time delay of the media, the interconnection must be considered a distributed load, not a lumped load. The distributed elements of a transmission line (media) can greatly affect signal quality.

More explicitly, transmission line theory dictates that if the transition (rise or fall) time of the driver is less than four times the line delay, the media must be treated as a distributed load, not a lumped load, and careful attention must be paid to any impedance discontinuities and stubs. For a given driver, if $t_r < 4\ t_d$ (where t_r = driver rise time, t_d = delay of the line) or $t_d > \frac{1}{4}\ t_r$ the line should be considered as a lossy line. This is usually true if the t_r of drivers are in the sub nanosecond range. A quick calculation will clarify this rule of thumb. For example: the DS90C031 driver has a typical t_r of 350 ps, and a microstrip built with FR-4 material has a t_d of 147 ps for one inch of PC trace. This calculates that, an inch of FR-4 microstrip will act as a transmission line ($350 < 4*147$) when driven by the DS90C031 driver. *Figure 7* includes a stub between the termination resistor and the receiver input, this length must not be longer than one inch in length, and should be kept as short as possible. Stub lengths of 1 inch or greater will cause the propagating signal to bounce off the high impedance end of the stubs and degrade the signal. Multiple reflections can travel up and down the line causing ringing, overshoot and undershoot which reduces the noise margin too.

The fast t_r of the DS90C031 allows the driver to achieve a higher bandwidth, but transmission line characteristics can easily crop up on a system board if not handled properly at these edge rates. To make the device work to its fullest capability, the LVDS DS90C031 and the DS90C032 should be operated in a point-to-point configuration with minimum discontinuities on the transmission line. This ensures no stub problems on the line. The media ***must*** be terminated by a 100Ω line-line termination at the far end. A 100Ω termination terminates the two differential line in its characteristic impedance and also provides the differential voltage (V_{OD}) for the current mode driver. Under the above conditions the driver can drive a twp (twisted pair) wire over 10m at speeds in excess of 155.5 Mbps (77.7 MHz).

BI-DIRECTIONAL APPLICATION ON ONE TWP

In a bi-directional application data can flow in only one direction at a time (see *Figure 8*) over the single twisted pair, however the bus needs to be terminated at both ends. This requires two 100Ω terminating resistors, assuming the cable impedance is 100Ω (one direction at a time). In *Figure 8,* Rt1 terminates the signal when D1 is driving, and Rt2 terminates the signal when D2 is driving. But, since the drivers are current mode (~4 mA), the two resistors in parallel will load down the driver ($100 \parallel 100 = 50\Omega$) which cuts the signal in half. This reduces systems noise margin to only 25 mV, as the minimum driver V_{OD} is now 125 mV, and the receiver threshold is 100 mV.

Another issue to be considered for a bi-directional configuration is that the DS90C032 receivers on the line in *Figure 8* must be left powered ON all the time. If they are powered OFF while a driver on the bus is ON, the internal protection diodes of the receiver input structure can turn ON and clamp the line to a diode drop above GND. This will disrupt the bus.

Since the driver output swing is severely attenuated due to dual parallel termination load, the bi-directional approach over one twp is not recommended. A separate twp should be used for the opposite direction.

A possible solution is to use 200Ω resistors in place of the 100Ω resistors at both ends of the cable to solve the loading problem. Even though this setup will obtain the correct V_{OD}, the line will not be properly terminated. Most cables are not available with 200Ω differential impedance. Typical cables are between 100Ω to 150Ω. This mismatch in impedance creates positive reflections which degrades signal quality severely. Once again, this setup is also not recommended.

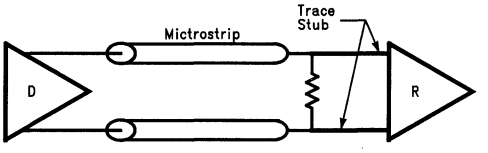

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FIGURE 7. A Point-to-Point Configuration Using LVDS

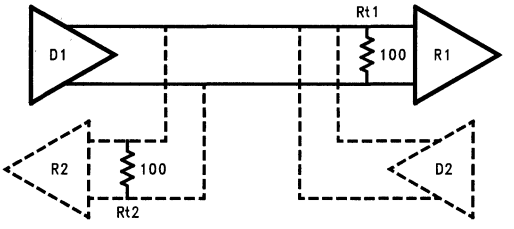

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FIGURE 8. Bi-Directional Application over One Pair of Twp

MULTI-DROP CONFIGURATION

In a multidrop configuration (see *Figure 9*), 10 receivers or more can be tied to the bus. Unused receivers (DS90C032) should be disabled and not powered OFF as explained previously. A powered OFF receiver input presents a low impedance to the bus. When the receiver is powered ON, the receiver input presents a high impedance and multiple parallel receivers on the bus will not adversely load down the line. Also, the stubs between the line and each receiver have the potential to create reflections if they are too long, or cause an impedance discontinuity.

SIGNAL QUALITY ACROSS CABLE

There are numerous ways of determining signal quality on the transmission media. Bit Error Rate (BER), Jitter, Eye Pattern, ratio of rise time and unit interval are some of the different ways designers use to determine signal quality. In this article, Eye pattern will be used to demonstrate signal quality for LVDS driver and receiver.

In order to create an Eye pattern, a PRBS (Pseudo Random Bit Sequence) of 511 ($2^9 - 1$) bits NRZ data was used to drive the LVDS driver inputs. The LVDS driver was connected to a LVDS receiver with a 10m, 25 pair, 28AWG, twp cable (SCSI grade cable). The Eye was plotted on the differential driver output at 155.5 Mbps and also at the receiver input at the end of the cable (see *Figures 10a* and *10b*).

A random data pattern is more prone to Inter Symbol Interference (ISI). There is a greater chance of errors occurring from Inter Symbol Interference as duration of pulses get shorter and shorter. A bit arriving at the receiver input might not have enough time to cross the threshold before the arrival of the next bit, resulting in lost data.

A PRBS with a pattern depth of 511 bits or 2047 ($2^{11} - 1$) or 32767 ($2^{15} - 1$) minimum should be used to generate Eye pattern. The Eye pattern is then used to characterize inter symbol interference issues. The opening of the Eye determines the signal quality, and jitter can be measured at the crossing point. Other Industry standards, SONET/SDH for example, specifies Eye patterns for signal quality analysis. LVDS technology demonstrates a wide eye opening at 155.5 Mbps over the 10m top cable. Also refer to application note AN-808 "Long Transmission Line and Data Signal Quality" for more discussions on signal quality.

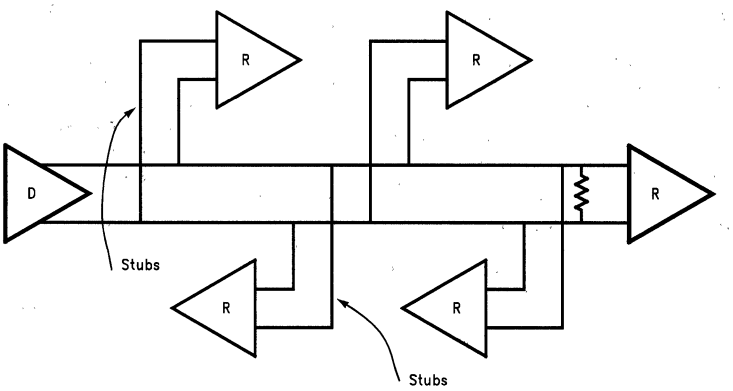

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FIGURE 9. Multi-Drop Configuration for LVDS

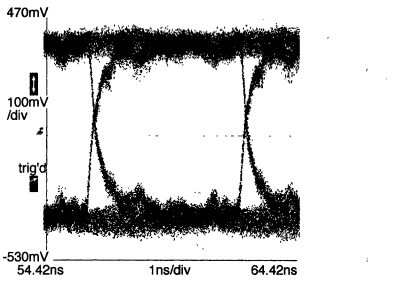

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FIGURE 10a. Eye Pattern at Driver Output

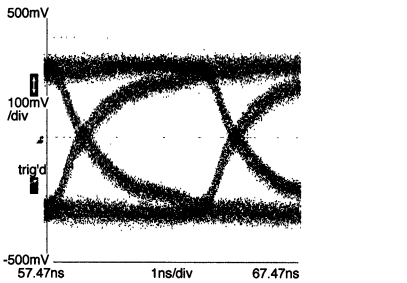

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FIGURE 10b. Eye Pattern at Receiver Inputs with 10m Cable

LVDS ASIC CELL

LVDS ASIC cells are low in power, operate at high data rates and are implemented using CMOS technology. These are characteristics that ASIC designers look for to satisfy their design requirements.

LVDS ASIC Leaf cells and Macro cells are available through National Semiconductor's SCLO8 ASIC library. The leaf cell is the smallest form of cell available for ASIC designs and the Macro cell combines different combinations of the Leaf cell. *Figure 11* illustrates the use of LVDS ASIC cells within an ASIC Core device.

The receiver leaf cell has inputs to the external world and the receiver cell output is an internal node to the ASIC Core. The driver cell's outputs are external to the world while the driver's input in an internal node.

The ASIC cells are fully compatible with the SCI-LVDS and the TIA LVDS standards.

By MUX'ing and DeMUX'ing signal lines within the ASIC core, higher data rates can be achieved that are impossible with standard TTL/CMOS. The data rate of the LVDS DS90C031/C032 is mainly limited by the technology that drives it. ASICs can achieve data rates beyond 622 Mbps by transporting data through LVDS I/O's.

CONCLUSION

LVDS technology solves the ever increasing data rate problem while decreasing power dissipation and can be widely used in Telecom, Routers, Intelligent Hubs, LCD displays, Copiers and numerous other exciting applications. LVDS technology provides the best solution for power budget requirements in today's designs. This high speed interface allows designers to implement a simple point-to-point link without complex termination issues. ASIC availability allows for the integration of standard controller functions and single chip solutions. LVDS technology provides solutions for what designers are looking for in a Physical Layer point-to-point interface.

REFERENCES

To order a copy of IEEE SCI standard contact:
IEEE Service Center at 1-800-678-4333(U.S)

To be part of the SCI Technical Discussions Reflector:
Send Email to sci@hplsci.hpl.hp.com

For TIA standard documentation contact:
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For a copy of National Semiconductor's SCL08 ASIC Library contact:
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Santa Clara, CA 95052-8090

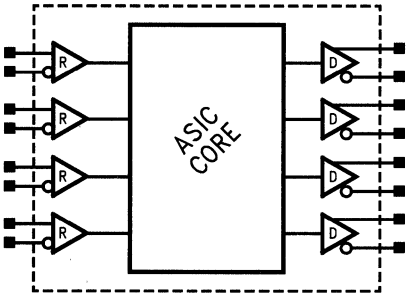

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FIGURE 11. ASIC Cell Implementation of LVDS

Inter-Operation of Interface Standards

National Semiconductor
Application Note 972
J. Goldie

INTRODUCTION

When communication is required between systems that support *different* interfaces is required, a detailed study of driver output and receiver input characteristics is required to determine if direct "electrical" inter-operation is possible. The results of this study may also conclude that some translation devices are required for inter-operation. This may include passive devices or active devices, and even perhaps a repeater circuit. This application note focuses on the simplest way to gain electrical inter-operation between devices conforming to different Interface standards. Compatibility of various protocol and mechanical dimensions of connectors is beyond the scope of this application note, but must also be investigated to determine if inter-operation is possible. The following cases are covered, along with a discussion on important electrical characteristics of standard drivers and receivers.

- **Single-ended to Differential**
  - RS-232 to RS-422
  - TTL to RS-422
- **Differential to Single-ended**
  - RS-422 to RS-232 (unipolar)
  - RS-422 to RS-232 (polar)
  - RS-422 to TTL
  - RS-485 to TTL
- **Single-ended to Single-ended**
  - TTL to RS-232
  - RS-232 to TTL
- **Differential to Differential**
  - ECL to RS-422
  - RS-422 to RS-485

DRIVER OUTPUT AND RECEIVER INPUT CHARACTERISTICS

Before any connection is made, a careful review of the driver output electrical characteristics, and the receiver input electrical characteristics should be completed. For the driver, the following parameters should be reviewed: driver output levels (minimum and maximum), and typical driver loading. For the receiver, the following parameters should be reviewed: input thresholds (sensitivity), input voltage range, and input resistance. Once these parameters have been reviewed, a decision upon what intermediate circuitry between the driver and receiver is required if any. The following pairs of parameters should be compared to determine if they are directly compatible: driver load to receiver input resistance, driver output levels to receiver input voltage range, and driver output levels to receiver thresholds.

CASE ONE: SINGLE-ENDED TO DIFFERENTIAL

When interfacing a single-ended driver to a differential receiver it is important to establish that the maximum output voltage of the single-ended driver does not exceed the recommended input voltage rating of the differential receiver. If it does not, then a direct connection is possible from a maximum voltage level point of view. If it does a simple resistor voltage divider should be inserted to attenuate the signal down to acceptable levels. A second check must be done to make sure that the minimum driver level, after the divider network if employed, is still greater than the receiver's sensitivity. The divider network, should be selected such that the total load presented to the driver is that of a single-ended receiver. Two examples are provided.

RS-232 TO RS-422

Depending upon the RS-232 driver that has been specified, driver output levels may be as high as ±15V, and for some RS-422 receivers the maximum input range is specified at ±10V. For this case, a divider network is required. A simple 3 kΩ in series with a 2 kΩ will provide the required attenuation and the correct load. It attenuates the signal 40%, dropping the ±15V to ±9V on the high side, and ±5V (driver minimum output level) to ±3V (which is greater than the receivers thresholds of ±200 mV). In addition the RS-232 driver also sees a 5 kΩ load of the divider network as it should. If the RS-422 receivers can withstand a ±15V input signal, the attenuator circuit is not required from a voltage level point perspective, but may still be desirable. This is due to the fact that many RS-422 (or RS-485) receiver's input impedance is in the range of 18 kΩ, which would cause a faster driver transition time and possibly an EMI and or crosstalk issue. *Figure 1* illustrates inter-operation between the RS-232 driver with a divider network to a RS-422 differential receiver. Note, that one receiver input is referenced to ground. Depending upon the input referenced to ground, a logic NOT may be achieved by tying the + input to ground, and connection to the divider network with the − input. Historically, this divider network has been termed an L-Pad in TIA/EIA documents and other international standards.

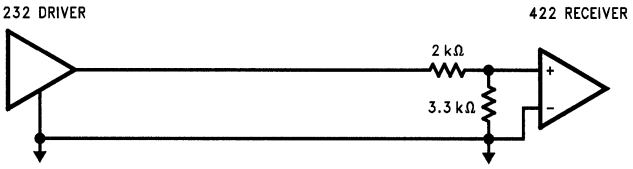

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FIGURE 1. RS-232 to RS-422

TTL TO RS-422

Since differential receivers are basically modified comparitors, they detect logical states by the difference in potential between their input pins, not with respect to circuit ground. Due to this fact, they can also accept standard TTL or CMOS levels if the other input is appropriately referenced. For TTL levels, one input should be tied to +1.5V, and the resulting thresholds will be +1.7V, and +1.3V. In other words, any levels greater that or equal to +1.7V will be a logic HIGH, and any level less than or equal to +1.3V a LOW, if the reference voltage was applied to the − input. Receivers normally have internal references between +2V and +3V, but it is not recommended that you float the reference input and rely on the internal reference due to the following reasons. First, the internal reference voltage is not normally specified in a datasheet, thus tolerances are not guaranteed or supported. Secondly, the input is a high impedance input, and depending upon the environment, it may pick up external noise and shift the thresholds around. A voltage regulator, or a simple resistor divider may be used depending upon the accuracy required. If a resistor divider is used, remember to take into account the input impedance of the receiver, which can be model (1st level) as a resistor to the internal bias voltage. These two values may be measured with a curve tracer. By sweeping voltage on the reference input, the resulting slope of the line (V_{IN} vs. I_{IN}) is the input impedance, and the crossing of the X axis is the zero current point or internal reference voltage. Note, that this test must be done with the receiver powered up to measure the reference voltage. *Figure 2* illustrates the inter-operation between standard TTL logic and a differential RS-422 receiver.

CASE TWO: DIFFERENTIAL TO SINGLE-ENDED

Differential to single-ended poses a more difficult problem to solve. Since single-ended receivers, RS-232 for example, essentially detect positive or negative voltage with respect to ground, an active solution is required to gain inter-operation with a single supply differential drivers. The following cases are provided as examples.

RS-422 to RS-232

RS-422 drivers (unipolar) are commonly powered from a single +5V power supply, thus both output states are positive voltages (V_{OL} and V_{OH}). RS-232 receivers as discussed detect positive and negative voltages, therefore to obtain inter-operation the circuit illustrated in *Figure 3* can be used. The PNP transistor is used as a switch, that when it is ON, the receiver input voltage is basically a $V_{CE(SAT)}$ below the driver's V_{OH} level. This is typically greater than +3V, and is a valid RS-232 input level. When the driver is in the opposite state, the PNP is off, the receiver input is pulled to ground by its internal input resistor. Note, RS-232 specifies the receiver thresholds are between −3V and +3V, however most receiver support TTL like thresholds centered around +1.5V, and guarantee a failsafe HIGH output state for an open input state (pulled low by internal input resistor). In the circuit shown in *Figure 3,* the resistor (R1) limits the base current and prevents the PNP from entering deep saturation, the diode (D1) prevents break down of the emitter base junction when the PNP is off. An additional resistor (R2) may be inserted to pull the RS-232 input to a voltage (below −3V) if required, but this also requires a negative supply and is typically not necessary. *Figure 3* illustrates this case of inter-operation.

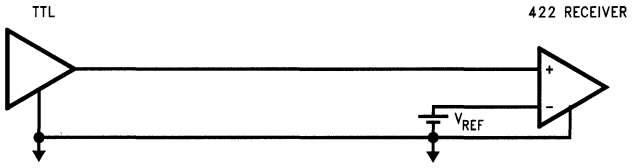

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FIGURE 2. TTL to RS-422

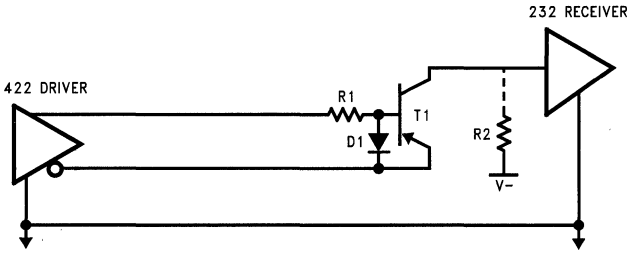

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FIGURE 3. RS-422 to RS-232—with Active Device

However, this active circuitry may not be required if the two systems share the same ground reference, are located close together, are in a relativity noise free environment and the RS-232 receiver provides a TTL threshold. This is due to the fact that RS-422 driver output levels are quite similar to standard TTL levels, however, driver output curves should be consulted to determine that the drivers V_{OH} level will be detected by the RS-232 receiver as a valid V_{IH}, and the V_{OL} as a V_{IL} respectively. These output levels can be determined by superimposing a 5 kΩ load line over the driver V_{OH}/I_{OH} curve. If the resulting driver V_{OH} is greater than the receivers V_{IH}, then inter-operation is possible. Similarly the output low case should be checked. RS-422 drivers are voltage mode drivers, and both outputs are not required to inter-operate with the single-ended receiver. Therefore, select the output which provides the desired logic (true or inverting), and leave the other output "open". Do not tie the unused output to ground, as that could yield an output short circuit condition (I_{OS}) which is undesirable from a power dissipation consideration. *Figure 4* illustrates the direct connection example.

RS-422 TO RS-232

RS-422 drivers are also available that are powered from polar (±5V) power supplies. If this is the case then once again a direct connection to a RS-232 receiver is possible. This is possible since the V_{OH} of the driver is typically between +3V and V_{CC}, while the V_{OL} of the driver is between −3V and V_{EE}, in both the output levels are greater in magnitude than the RS-232 receivers thresholds. *Figure 5* illustrates this second case of direct inter-operation.

RS-422 TO TTL

As discussed above, RS-422 driver output levels are quite similar to standard TTL levels, however, driver output curves should be consulted to determine that the drivers V_{OH} level will be detected by the TTL input as a valid V_{IH}, and the V_{OL} as a V_{IL} respectively. In almost all cases a direct connection will be possible. RS-422 drivers are voltage mode drivers, and both outputs need not be used. Simply pick the output (true or inverting), and leave the other output "open". Do not tie the unused output to ground, as that could yield an output short circuit condition (I_{OS}) which is undesirable from a power dissipation consideration. *Figure 6* illustrates the inter-operation of a RS-422 driver with a standard TTL input.

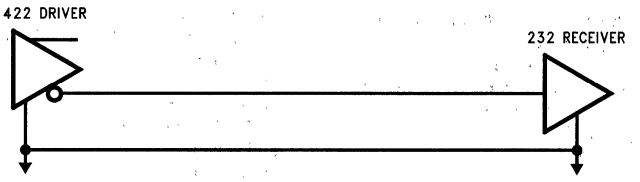

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FIGURE 4. RS-422 to RS-232—Direct Connection

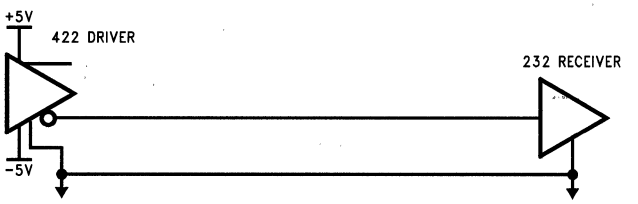

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FIGURE 5. RS-422 to RS-232

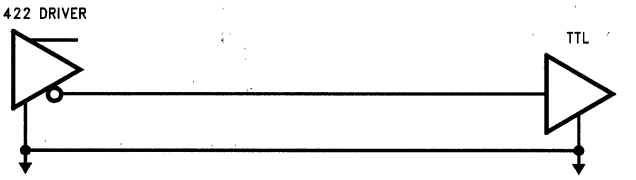

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FIGURE 6. RS-422 to TTL

RS-485 TO TTL

RS-485 driver output levels are NOT similar to standard TTL levels, however, direct inter-operation may be possible. Again, driver output curves should be consulted to determine that the drivers V_{OH} level will be detected by the TTL input as a valid V_{IH}, and the V_{OL} as a V_{IL} respectively. Since the RS-485 outputs include blocking diodes, the V_{OH} levels are lower than standard TTL levels, and the V_{OL} levels are a diode higher than standard levels. Once again, RS-485 drivers are voltage mode drivers, and both outputs need not be used. Simply select the desired output (true or inverting), and leave the other output "open". Do not tie the unused output to ground, as that could yield an output short circuit condition (I_{OS}) which is undesirable from a power dissipation consideration. If the driver output levels do not meet the TTL input V_{IH} and V_{IL} specifications, a RS-485 receiver should be used to receive the RS-485 levels and correctly translate them to TTL compatible levels. *Figure 7* illustrates this connection.

CASE THREE: SINGLE-ENDED TO SINGLE-ENDED

Single-ended to Single-ended is once again simply comparing output levels to thresholds and input voltage ranges. In some cases, a direct connection is possible, as described in the following examples.

TTL TO RS-232

TTL output levels can directly inter-operate with certain RS-232 receivers. This is true since most RS-232 receivers support a tighter threshold specification than required by the RS-232 standard. The RS-232 standard specifies that the thresholds are between +3V and −3V, however, most thresholds are centered around +1.5V. If this is the case, then standard TTL levels (High > 2.0V and Low < 0.8V) will be detected correctly. One note of caution is that the TTL gate will be loaded with the 5 kΩ load instead of a standard TTL input load. The TTL gate driving the RS-232 receiver must have adequate drive capability to obtain the correct levels with the RS-232 receiver load. This connection is illustrated in *Figure 8.*

RS-232 TO TTL

RS-232 output levels are polar, and therefore they swing around ground. This negative swing typically prevents direct inter-operation to TTL inputs which prefer positive voltages only. To clamp off the negative swing a diode may be used to clip the negative swing but will load down the driver when the diode is forward biased. This is typically acceptable if the driver employed provides a relatively tight current limit in the range of 10 mA. *Figure 9* illustrates this inter-operation with a diode clamp.

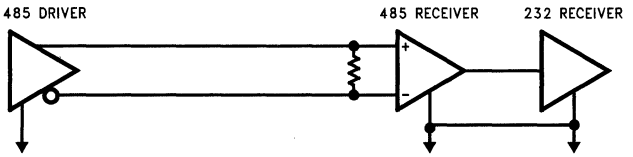

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FIGURE 7. RS-485 to TTL

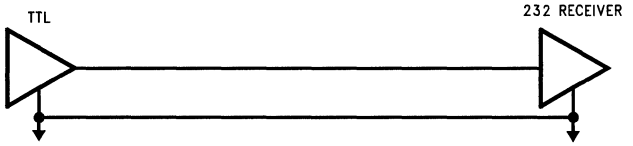

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FIGURE 8. TTL to RS-232

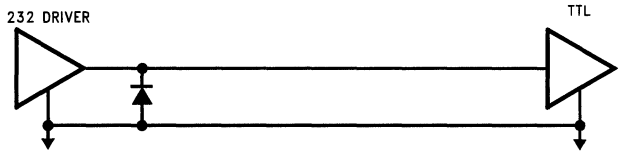

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FIGURE 9. RS-232 to TTL

CASE FOUR: DIFFERENTIAL TO DIFFERENTIAL

As in the other three cases described, driver output levels need to be compared to receiver input thresholds and input voltage ranges. If they agree, then a direct connection is possible. If the levels are not compatible then a repeater/translator circuit will be required.

ECL TO RS-422

Differential ECL or even Pseudo ECL (PECL) will typically directly inter-operate with a RS-422 receiver. This is possible since a RS-422 receiver provides a tight threshold specification of ±200 mV, and a wide common mode range of ±10V. Differential ECL output levels are normally between ±500 mV to ±800 mV which are detectable by the receiver. Since the receiver supports a positive and negative common mode range ECL or PECL signals may be received. *Figure 10* illustrates a ECL to RS-422 (or RS-485) connection.

RS-422 TO RS-485

Direct connection of RS-422 to RS-485 is always possible. RS-485 can be considered a subset of RS-422 which supports multipoint (multiple drivers) applications. RS-422 and RS-485 receivers are virtually identical, except for the fact that the RS-485 receiver present a input impedance that is typically 3 times the RS-422 receiver. For this reason, the RS-422 driver can now drive at least 32 receiver loads opposed to the RS-422 limit of 10. Recall that RS-422 is limited to single driver/multiple receiver applications, and only RS-485 devices (drivers) should be employed in true multipoint (multiple driver) applications. *Figure 11* illustrates a RS-422 driver driving up to 32 RS-485 receivers in a multidrop uni-directional application.

SUMMARY

In many cases direct inter-operation is possible between different interface standards. In cases where that is not possible, typically simple circuitry can be inserted between the two devices to alter or clamp the levels to levels that are compatible with the other device. In the extreme case, where simple circuitry can not solve the problem, a repeater may be used. For example, if an "A" driver needs to inter-operate with a "B" receiver, a repeater may be inserted between the two that includes a "A" receiver and a "B" driver. For example, this may be desirable for interfacing a RS-422 driver to a ECL differential receiver since most ECL receivers can not accept positive (above ground) input voltages. This method should be a solution of last resort due to the added cost of the active devices, and the repeater itself. The methods described above are preferred, as they provide direct, or inter-operation with only simple circuitry. As a final word of caution, always review the respective device specifications to determine if inter-operation is possible before connecting the two together.

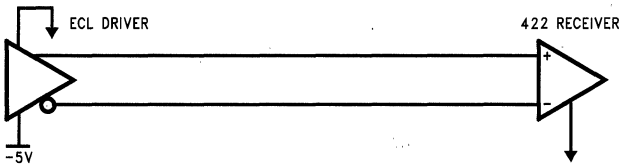

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FIGURE 10. ECL to RS-422

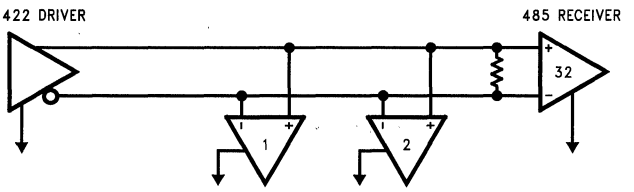

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FIGURE 11. RS-422 to RS-485

Table I lists key generic electrical characteristics of common interface standards.

TABLE I. Electrical Characteristics Comparison of Common Interface Standards

Parameter	RS-232	RS-422	RS-423	RS-485
Maximum Driver Output Level	±25V No Load ±15V 7 kΩ Load	±10V No Load ±6V Diff.	±6V No Load	±6V No Load ±6V Diff.
Minimum Driver Output Level	±5V 3 kΩ Load	±2V 100Ω Load	±3.6V 450Ω Load	±1.5V 54Ω Load
Standard Driver Load	3 kΩ–7 kΩ 5 kΩ Typical	100Ω	>4 kΩ Typical 450Ω Minimum	54Ω
Receiver Input Voltage Range	±15V	±10V	±10V	±10V
Receiver Thresholds	±3V +1.5V Typical	±0.2V	±0.2V	±0.2V
Receiver Input Impedance	3 kΩ–7 kΩ 5 kΩ Typical	≥4 kΩ	≥4 kΩ	~ >12 kΩ
MODE	Single Ended	Differential	Single Ended	Differential

REFERENCES

EIA/TIA Standard EIA/TIA-232-E, Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data interchange, EIA/TIA, Washington, D.C.

TIA/EIA Standard TIA/EIA-422-B, Electrical Characteristics of Balanced Voltage Digital Interface Circuits, TIA, Washington, D.C.

TIA/EIA Standard TIA/EIA-423-B, Electrical Characteristics of Unbalanced Voltage Digital Interface Circuits, TIA, Washington, D.C.

EIA Standard EIA RS-485, Standard for Electrical Characteristics of Generators and Receivers for use in a Balanced Digital Multipoint Systems, EIA, Washington, D.C.

Application Note #216, Summary of Well Known Interface Standards, Interface Databook, National Semiconductor, Santa Clara, CA

Application Note #759, Comparing EIA-485 and EIA-422-A Line Drivers and receivers in Multipoint Applications, Interface Databook, National Semiconductor, Santa Clara, CA

LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report # 1

National Semiconductor
Application Note 977
John Goldie
Syed Huq

LVDS SIGNAL QUALITY

This report provides data rate versus cable length recommendations for LVDS drivers and receivers in a typical application for a particular twisted pair cable. The questions of: How Far? and How Fast? seem simple to answer at first, but after detailed study their answers become quite complex. This is not a simple device parameter specification. But rather, a system level question, and to be answered correctly a number of other parameters besides the switching characteristics of the drivers and receivers must be known. This includes the measurement criteria for signal quality that has been selected, and also the pulse coding that will be used (NRZ for example). Additionally, other system level components should be known too. This includes details about the cable, connector, and information about the printed circuit board (PCB). Since the purpose is to measuring signal quality, it should be done in a test fixture that matches the end environment as close as possible, or even better in the actual application if possible. Eye pattern measurements may be used to measure the amount of jitter versus the unit internal to establish the data rate versus cable length curves and therefore are a very accurate way to measure the expected signal quality in the end application. This test report assumes: maximum jitter allotment of 20%, measurements taken at 0V (differential zero) for minimum jitter, measurements taken at ±100 mV for maximum jitter, and then provides the corresponding data rate versus cable length recommendations.

WHY EYE PATTERNS?

The eye pattern is used to measure the effects of inter symbol interference on random data being transmitted through a particular media. The transition time of the signal is effected by the prior data bits, this is especially true for NRZ data which does not guarantee transitions on the line. For example in NRZ coding, a transition high after a long series of lows has a slower rise time than the rise time of a periodic (010101) waveform. This is due to the low pass filter effects that the cable causes. *Figure 1* illustrates the superposition of six different data patterns. Overlaid they form the eye pattern that is the input to the cable. The right hand side of *Figure 1*, illustrates the same pattern at the end of the cable. Note the rounding of the formerly sharp transitions. The width of the crossing point is now wider, and the opening of the eye is also now smaller (see AN-808 for an extensive discussion on eye patterns).

When line drivers (generators) are supplying symmetrical signals to clock leads, the period of the clock, rather than the unit interval of the clock waveform, should be used to determine the maximum cable lengths (e.g., though the clock rate is twice the data rate, the same maximum cable length limits apply). This is due to the fact that a periodic waveform is not prone to distortion from inter symbol distortion as is a data line.

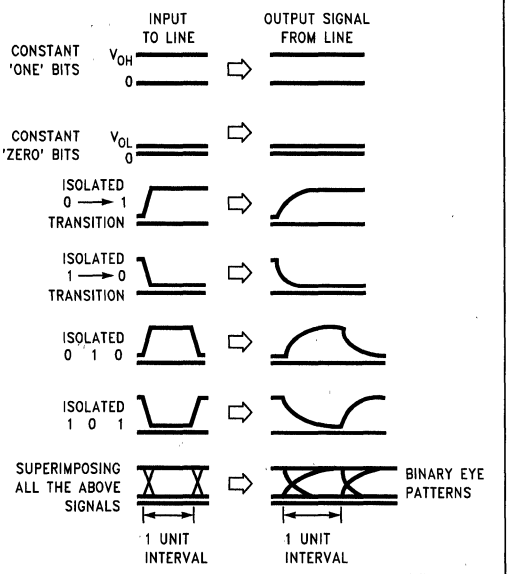

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FIGURE 1. Formation of an Eye Pattern by Superposition

Figure 2 describes the measurement locations for minimum jitter. Peak-to-Peak Jitter is the width of the signal crossing the optimal receiver thresholds. For a differential receiver, that would correspond to 0V (differential). However, the receiver is specified to switch between −100 mV and +100 mV. Therefore for a worse case jitter measurement, a box should be drawn between ±100 mV and jitter measured between the first and last crossing at ±100 mV. If the vertical axis units in *Figure 2* was 100 mV/division, the worse case jitter ±100 mV levels.

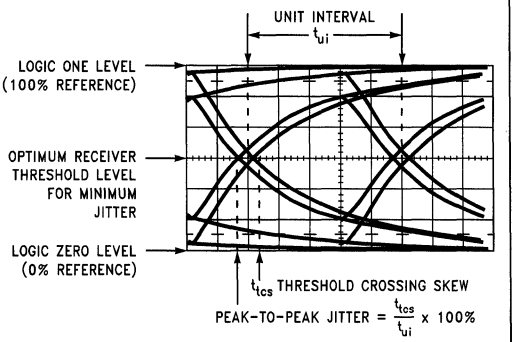

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FIGURE 2. NRZ Data Eye Pattern

EYE PATTERN TEST CIRCUIT

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 3*. This figure details the test circuit that was used to acquire the Eye pattern measurements. It includes the following components:

PCB # 1: DS90C031 LVDS Quad Driver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector.

Cable: Cable used for this testing was Berk-Tek part number 271211. This is a 105Ω (Differential Mode) 28 AWG stranded twisted pair cable (25 Pair with overall shield) commonly used on SCSI applications. This cable represents a common data interface cable. For this test report the following cable lengths were tested: 1, 2, 3, 5, and 10 meter(s). Cables longer than 10 meters were not tested, but may be employed at lower data rates.

PCB # 2: DS90C032 LVDS Quad Receiver soldered to the PCB with matched PCB traces between the device (located near the edge of the PCB) to the connector. The connector is an AMP amplite 50 series connector. A 100Ω surface mount resistor was used to terminate the cable at the receiver input pins.

TEST PROCEDURE

A pseudo-random (PRBS) generator was connected to the driver input, and the resulting eye pattern, measured differentially at TP' was observed on the oscilloscope. Different cable lengths (L) were tested, and the frequency of the input signal was increased until the measured jitter equaled 20% with respect to the unit interval for the particular cable length. The coding scheme used was NRZ. Jitter was measured twice at two different voltage points. First, jitter was measured at the 0V differential voltage (optimal receiver threshold point) for minimum jitter, and second at the maximum receiver threshold points (±100 mV) to obtain the worst case or maximum jitter at the receiver thresholds. Occasionally jitter is measured at the crossing point alone, this will result in a much lower jitter point, but ignores the fact that the receivers may not switch at that very point. For this reason this signal quality test report measured jitter at both points.

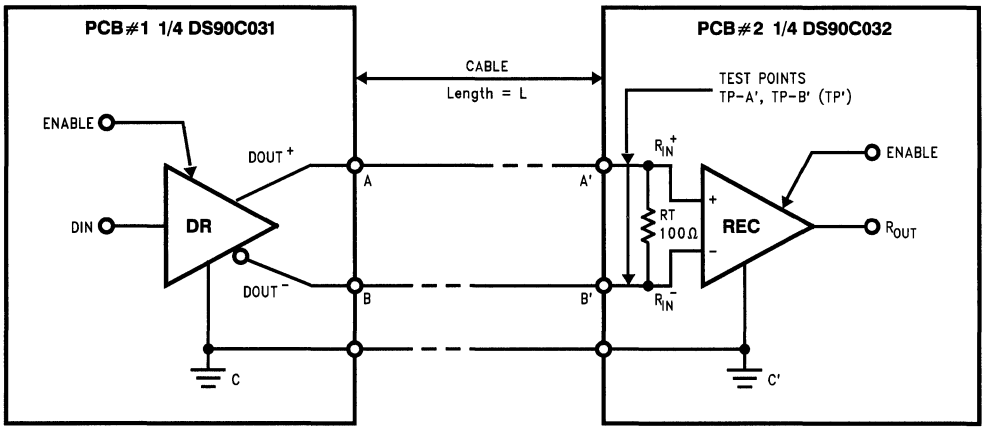

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FIGURE 3. LVDS Signal Quality Test Circuit

RESULTS AND DATA POINTS

20% Jitter Table @ 0V Differential (Minimum Jitter)

Cable Length (meter)	Data Rate (Mbps)	Unit Interval - tui (ns)	Jitter - tcs (ns)
1	400	2.500	0.490
2	391	2.555	0.520
3	370	2.703	0.524
5	295	3.390	0.680
10	180	5.550	1.160

As described above, Jitter was measured at the zero volt differential point. For the case with the 1 meter cable, 490 ps of jitter at 400 Mbps was measured, and 1.160 ns of jitter at 180 Mbps and with the 10 meter cable.

20% Jitter Table @ ±100 mV (Maximum Jitter)

Cable Length (meter)	Data Rate (Mbps)	Unit Interval - tui (ns)	Jitter - tcs (ns)
1	200	5.000	1.000
2	190	5.263	1.053
3	170	5.882	1.176
5	155.5	6.431	1.286
10	100	10.000	2.000

The second case measured jitter between ±100 mV levels. For the 1 meter cable, 1 ns of jitter was measured at 200 Mbps, and for the 10 meter cable, 2 ns of jitter occurred at 100 Mbps.

Figure 4 is the graphical representation of the relationship between data rate and cable length for the application under test. Both curves assume a maximum allotment of 20% jitter with respect to the unit interval. Basically data rates between 200–400 Mbps are possible on the shorter lengths, and data rates of 100–200 Mbps are possible at 10 meters. It should be noted that employing a different coding scheme, a different cable, a different wire gauge (AWG), etc., will create a different relationship between maximum data rate versus cable length.

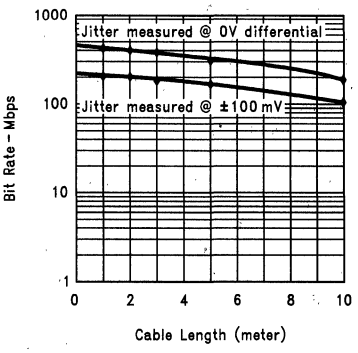

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FIGURE 4. Data Rate versus Cable Length

CONCLUSIONS

Eye patterns provide a useful tool to analyze jitter and thus the resulting signal quality as it captures the effects of a random data pattern. They provide a method to determine the maximum cable length for a given data rate or vice versa. However, different systems can tolerate different amounts of jitter, commonly 5%, 10%, or 20% is selected, with 20% being the maximum allowed. Jitter in the system that is greater than 20% tends to close down the eye opening, and error free recovery of NRZ data is increasing more difficult. This report illustrates typical maximum cable lengths for a common data interface cable at 20% jitter, for data rates between 100 Mbps and 200 Mbps. Selecting a premium cable, a category 5 cable for example, will extend the curve significantly. While selecting a lower limit for jitter, 5% for example will decrease the maximum cable length.

REFERENCES

To probe further the following National Semiconductor Application Notes are recommended which are all located in the INTERFACE: Data Transmission Databook:

AN-808 Long Transmission Lines and Data Signal Quality

AN-903 A Comparison of Differential Termination Techniques

AN-916 A Practical Guide to Cable Selection

For additional information on cables contact: Berk-Tek @ 1-800-237-5835 (USA), 1-717-354-6200.

The Practical Limits of RS-485

National Semiconductor
Application Note 979
Todd Nelson

INTRODUCTION

This application note discusses the EIA-485 standard for differential multipoint data transmission and its practical limits. It is commonly called RS-485, however its official name is EIA-485 which reflects the name of the committee at the time it was released. It is expected to be revised soon and will then become TIA/EIA-485-A.

Differential data transmission is ideal for transmitting at high data rates, over long distances and through noisy environments. It nullifies the effects of ground shifts and noise signals which appear as common mode voltages on the transmission line. TIA/EIA-422-B is a standard that defines differential data transmission from a single driver to multiple receivers. RS-485 allows multiple drivers in operation, which makes multipoint (party line) configurations possible.

This application note will discuss the specifications as defined in the RS-485 document. Interpretations of the standard and device specifications can vary among manufacturers. However, there are some guarantees required to be completely compliant with the standard.

There are many possibilities and trade-offs associated with being partially compliant—or "compatible." Some applications can tolerate the trade-offs in return for increased performance or added value. For that reason, this application note will discuss the practical application of the specifications.

A detailed explanation of each requirement of the standard will not be given as this is beyond the scope of this note. Also beyond the scope are advanced topics relating to new technology.

KEY RS-485 REQUIREMENTS

The key features are:

- Differential (Balanced) Interface
- Multipoint Operation
- Operation from a single +5V Supply
- −7V to +12V Bus Common Mode Range
- Up to 32 Unit Loads (Transceivers)
- 10 Mbps Maximum Data Rate (@40 feet)
- 4000 Foot Maximum Cable Length (@100 kbps)

A typical application is shown in *Figure 1*.

The key requirement of the driver is its guaranteed differential output voltage as measured: with no load; with a minimum configuration of two nodes; and with the full load of 32 nodes. The terms used in the specification are:

V_{OA} True output voltage with respect to ground

V_{OB} Complimentary output voltage with respect to ground

V_{OD} Differential output voltage ($V_{OA}-V_{OB}$)

V_{OS} Offset voltage, or center point of V_{OA} or V_{OA}, also called V_{OC}

V_{CM} Algebraic mean of V_{OA} and V_{OB}, including any ground potential difference or noise

The specifications are best represented by the following figures and table.

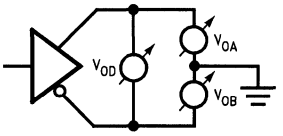

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FIGURE 2. No Load Configuration

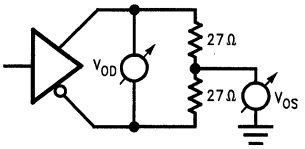

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FIGURE 3. Termination Load Configuration

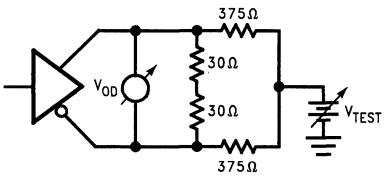

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FIGURE 4. Full Load Configuration

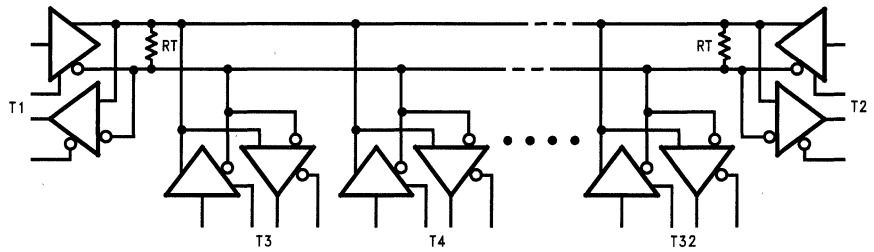

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FIGURE 1. Typical RS-485 Application

TABLE I. Driver Output Voltage Requirements

Configuration	Test	Min	Max	Units
No Load *Figure 2*	V_{OD1}	1.5	6.0	V
	V_{OA}	0	6.0	V
	V_{OB}	0	6.0	V
Termination *Figure 3*	V_{OD2}	1.5	5.0	V
	V_{OS}	−1.0	3.0	V
Full Load *Figure 4*	V_{OD3}	1.5	5.0	V
	with $-7V \le V_{CM} \le +12V$			

There is also a condition that the driver must not be damaged when the outputs are shorted to each other or any potential within the common mode range of −7V to +12V. The peak current under shorted conditions must be less than 250 mA. This point is key to multipoint operation, since contention may occur.

The data rate requirements have implications on the speed of the device. Switching characteristics must specify that the transition time (t_r, t_f) be ≤ 0.3 of the unit interval. The minimum unit interval for 10 Mbps at 40 feet is 100 ns so $t_r/t_f \le 33$ ns; for 100 kbps at 4000 feet it is 10 μs so $t_r/t_f \le 3.3$ μs.

A Unit Load is defined as a load on the bus, it is commonly a driver and a receiver. The result should be that the unit load does not load down the bus under power-on or power-off conditions. Driver leakage tends to be in micro-amps but receiver input current can be significant compared to driver leakage. Four points define the unit load, shown in *Figure 5*.

Rec. Input current (I_{IN}) at +12V	≤1 mA
I_{IN} between +5V and +12V	≥0 mA
I_{IN} at −7V	≥ −0.8 mA
I_{IN} between −3V and −7V	≤ 0 mA

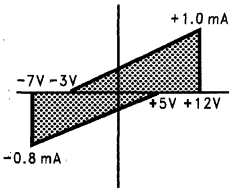

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FIGURE 5. V/I Relationship defining a Unit Load

The shaded area effectively defines the receiver input impedance (R_{IN}), ≥10.6 kΩ (19V/1.8 mA). The standard does not require a specific impedance, only that it falls within the shaded area.

The key receiver requirements are its threshold voltage levels and common mode range. The receiver output must be HIGH if the true input is more than 200 mV above the complimentary input; LOW if it is more than 200 mV below the complimentary input. This must be possible with the inputs varying from −7V to +12V. A graphic representation is shown in *Figure 6*. In this diagram, the lightly shaded region represents the range of points where RI is more than 200 mV below RI*; therefore the output is LOW.

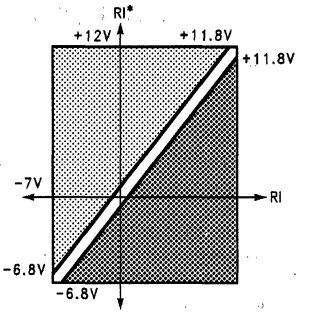

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FIGURE 6. Receiver Input Range

The 200 mV receiver threshold and the 1.5V minimum differential driver output voltage provide 1.3V of differential noise margin. Since the bus is typically a twisted pair, ground noise is canceled out by the differential operation. The result is a bus that is well suited for high data rates and noisy environments.

There are further requirements such as balance of terminated voltage, balance of offset voltage and timing which can be reviewed in the standard. Note that all of these requirements should be met over the full supply voltage and temperature range in which the device will operate.

Interpreting the standard and creating device specifications appears to be straight forward. However, the range of practices shows that there are differing opinions.

COMPATIBILITY TRADEOFFS

It is not always practical to meet all of the requirements. The devices may have limitations, the applications may not need full compliance or there may be a possible improvement in one area at the expense of another.

Commonly accepted minimum specifications for compatibility include V_{OD1}, V_{OD2}, I_{OS}, V_{CM}, V_{TH}. At times, these are specified at controlled conditions—not over the full operating range, as is required. Furthermore, "Up to 32 unit loads..." implies V_{OD3} and R_{IN} or the V/I relationship discussed above. V_{OD3} can be traded off if the application is not expected to be fully loaded.

R_{IN} can be increased and thereby allowing more than 32 nodes to be connected without exceeding the 32 unit loads. For example, a R_{IN} of 24 kΩ implies that 64 nodes equates to 32 unit loads.

In many applications, I_{CC} is the differentiating factor. Optimizing a device for low power may slow switching speed. The end user may define the acceptable speed but switching speed is quite often defined by the choice of protocol.

Many low power technologies have lower breakdown voltages, which reduces the recommended maximum voltage range for the bus pins. The recommended voltage range for the bus pins defines how much protection the device has beyond the −7V to +12V common mode range. If the environment demands that the bus survive voltages up to ±24V, then the device must guarantee this, otherwise external protection must be included.

External limitations may dictate controlled edge rates to allow greater stub lengths or reduced EMI, which may result in a device that does not meet the prescribed data rate. All of these trade-offs must be considered in the design of the system.

IMPLEMENTATION ISSUES

Topology: RS-485 is defined as a multi-point bus, *(Figure 7)* therefore multiple drivers and receivers can be connected to the bus at the same time (see discussion regarding unit load).

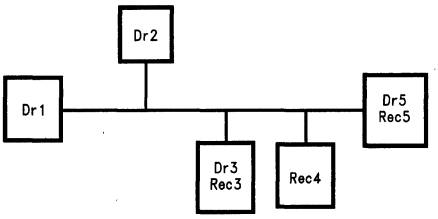

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FIGURE 7. Bus Topology

In such a configuration, only one driver has control at a time and all the active receivers receive the same signals.

A ring which is created by connecting both ends of a bus together will not work. A traditional ring uses point-to-point links between the nodes. This can be implemented using RS-485, however, there are many other point-to-point technologies available.

Star configurations are also discouraged. In a star configuration *(Figure 8)* the device is effectively at the end of a very long stub, and this causes reflection and termination problems.

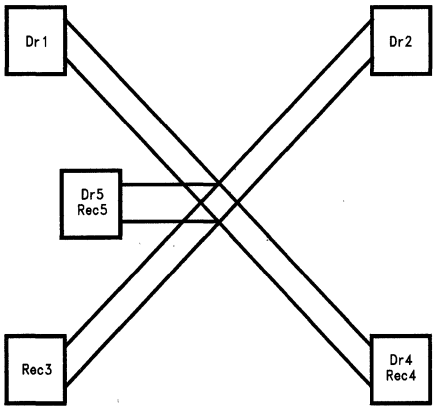

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FIGURE 8. Star Topology

Stubs: RS-485 recommends keeping the stubs as short as practical. A stub is the distance from the device to the bus, or the termination resistor (in the case at the ends of the bus), see *Figure 9*. The maximum length is not defined by the standard, but longer stubs will have a negative impact on signal quality. This affect can be reduced by controlling the transition time of the driver.

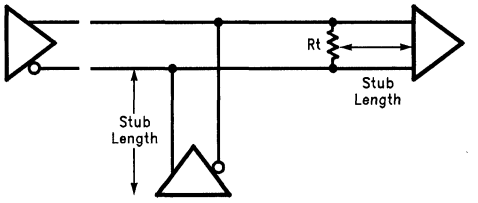

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FIGURE 9. Stub Length

The driven signal encounters a reflection at the end of the stub, if this occurs within the rising edge of the signal then it can be neglected. A general rule is that stubs should be less than $\frac{1}{3}$ of the transition time. Therefore, slowing the transition time can extend the practical stub length.

stub $\ell \leq \frac{1}{3}$ (transition time)/(velocity)

ℓ ft $\leq \frac{1}{3}$ (t_r or t_f)/(1.5 ns/ft)

Number of Nodes: The standard allows 32 unit loads, as defined by the driver leakage and receiver impedance—this was intended to mean 32 transceivers. If a number of the devices guarantee a greater impedance, then it is possible to add more than 32 transceivers to a bus.

Termination: RS-485 has defined the termination as 120Ω parallel termination at each end of the bus. This assumes a characteristic impedance in the range of Z_O = 100Ω to 120Ω for the cable. Other termination schemes could be implemented, but a thorough analysis must be done to assure adequate signal quality. For more information on termination, see AN-903.

Bus Faults: This bus is defined to be resistant to many of the faults associated with a cable environment such as noise and variations in device ground. It is built for party line applications so it can withstand driver contention. In most cases, there is enough noise margin to detect a valid HIGH or LOW. However, in the case where both lines are open or there is a short between the two lines, the state may be unknown. Such a case requires the designer to implement a "failsafe" scheme to bias the receiver to a known state. See AN-847 and AN-903 for a detailed discussion of failsafe techniques.

Data Rate: Earlier, the data rate vs distance guidelines were given as 10 Mbps at 40 feet and 100 kbps at 4000 feet. Advances in technology continue to push these limits. At long distances the practical limitation is dominated by the rise time degradation due to the cable. The approximate delay associated with 100Ω cable is 1.5 ns/foot. Therefore, 4000 feet of cable will cause 6 μs of delay—which limits the data rate to 333 kbps (166 kHz) before device delays are involved. At 100 feet only 150 ns of delay are added by the cable, so an ideal driver/receiver could switch at 10 Mbps theoretically. Further complications are added by encoding schemes (PWM, RTZ, etc.) and protocol requirements (idle time, overhead, etc.). If an off-set bias is implemented for receiver failsafe, this may induce some signal distortion or cause slight duty cycle distortion which must be factored in to the data rate considerations.

RS-485 is defined as a half-duplex bus, though many applications use multiple channels in parallel or full-duplex. In parallel bus applications, channel-to-channel skew becomes a critical issue. These and possible protocol requirements would have to be considered in the evaluation of each device.

Supply Power: I_{CC} is not always the dominant indicator of power requirements. Low power CMOS devices require little quiescent current, typically less than 1 mA. However, when switching against a heavy load, the load current can be over 60 mA! And switching at higher frequencies also requires more current. Comparing bipolar and CMOS devices should include the case when switching a heavy load at high frequencies as well as the quiescent case. The total requirement will depend on the portion of time at idle versus switching.

Signal Quality: At the extremes of distance and data rate, the signal quality will be degraded. This is a qualitative parameter that is usually judged with eye patterns or in probabilities of errors.

Eye patterns show the effects of intersymbol interference, a hypothetical example is shown in *Figure 10*. A full discussion on signal quality is given in AN-808.

Interfacing to other standards: This bus is not intended to be inter-operable with other standards such as TIA/EIA-232-E or ECL. TIA/EIA-422-B buses can accept RS-485 devices, but the opposite case is not true for the drivers. For a full discussion on this topic, see AN-972. The international standard ISO 8482.1994 has recently become compatible with RS-485.

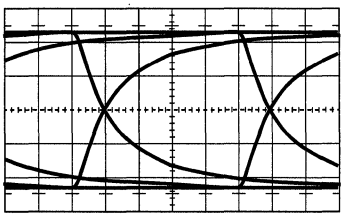
PRACTICAL LIMITS

Theoretical limits defined by the standard should not be exceeded without fully examining the trade-offs discussed above. However, there are some common practices which can extend RS-485 beyond its defined limits.

The maximum number of nodes can exceed 32. R_{IN} can be defined as ½ unit load or ¼ unit load, thus extending the number of nodes that can be attached to a single bus to 64 or 128 respectively. The leakage specifications must also support the stated unit load. Note that a bus with 128 nodes requires that the average loading be ¼ unit load—including any third-party nodes that may be attached. Not all devices need the same unit load rating, but the total cannot exceed 32 unit loads.

The common-mode voltage range requirements continue to be a factor that limits many other types of interfaces. TIA/EIA-422-B offers a common-mode range of ±7V, but does not allow multiple drivers on the bus. The process technologies and design techniques required to meet the −7V to +12V range are somewhat unique. In fact, many applications see common-mode voltages beyond this range, such as ±24V! Generally, reducing common-mode voltage in trade for any performance or integration gains has not been acceptable. Increasing common-mode beyond the RS-485 limits depends on the specific devices; wider common-mode may affect the thresholds and hysteresis of the receiver which reduces the noise margin.

Speed and power requirements are opposing trends: higher data rates tend to use more power, yet lower power (I_{CC}) technologies tend to be slower. Technologies that effectively combine both high speed and low power are becoming available, and will come down in cost. Optimizing for speed in excess of the RS-485 limits may require technologies that consume greater quiescent current. In applications that are not transmitting for extended periods, optimizing for low power is common. Such devices may not meet the 10 Mbps data rate referenced in RS-485, which is acceptable since many of these applications are specified between 9600 bps and 1 Mbps.



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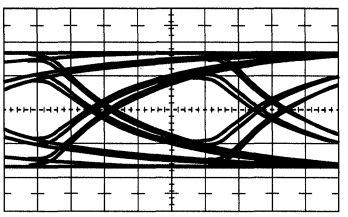

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FIGURE 10. Eye Patterns

CONCLUSION

RS-485 is a well-defined, multi-purpose electrical specification for multi-point data transmission. The standard allows manufacturers to optimize devices for speed and power. Despite the definition, there is still potential for compatibility issues if the devices are not fully specified.

Many of the limits imposed in RS-485 can be exceeded at some cost and with increased risk. But technology barriers are continuously being removed and this promises tremendous performance gains, perhaps eliminating those costs and risks.

RS-485 is a very rugged standard for multi-point applications. It has proven to be popular over a span of many years. With the breadth of devices available and new technologies being applied, RS-485 will continue for many years to come.

REFERENCES

EIA RS-485 standard for differential multi-point data transmission

TIA/EIA-422-B standard for differential multi-drop data transmission

ISO 8482.1994 Information processing systems—Data communication Twisted pair multipoint inter-connections

TIA/EIA-422-B Overview

National Semiconductor
Application Note 1031
Michael R. Wilson

ABSTRACT

This application note covers topics associated with concerns for implementing a balanced interface circuit utilizing the TIA/EIA-422-B (formerly RS-422-A) electrical interface standard. The items designated by bullets below indicate the topics covered within this application note.

- Cable Length and Data Rate
- Termination
- Failsafe
- Configuration
- ESD Protection
- Live Insertion
- By-Pass Capacitors
- Stub Lengths
- Receiver Power Off Characteristics
- Typical Cable Media

Each topic has an independent section. The sections are identified by bold all upper case titles. Subsection titles are bold only.

INTRODUCTION/OVERVIEW

TIA/EIA-422-B (RS-422) is an industry standard specifying the electrical characteristics of a balanced interface circuit. Other prefixes are commonly used with the RS-422 standard. These include EIA, EIA/TIA, and RS; although previously correct, today TIA/EIA is the correct prefix. However, for simplicity, RS-422 will be used throughout the rest of this application note. Also, a suffix letter denotes the different revisions of the standard but various prefixes with the same suffix reference the same identical standard.

RS-422 was introduced to solve the limitation problems of single-ended standards like TIA/EIA-232-E. Single-ended interfaces lack common-mode noise rejection capability; ideal for noisy environments. Also, data rates are usually limited to less than 0.5 Mbps. A RS-422 interface may be implemented to overcome these limitations.

A RS-422 driver can drive up to ten unit loads (i.e., 4 kΩ to circuit common is one unit load). The driver is capable of transmitting data across 4000 feet (recommended limit) of cable; but not at maximum data rates (see *Figure 3*). Standard RS-422 drivers are guaranteed to source and sink a minimum 20 mA across a 100Ω load. This corresponds to a minimum differential output voltage, V_{OD}, of 2V across the load (see *Figure 1*).

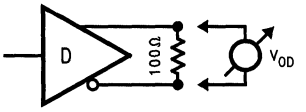

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FIGURE 1. Terminated Configuration

The complement RS-422 receiver must be equal to or less than one unit load. This is represented by the slope of the shaded region in *Figure 2*. The operating range of receiver is defined between ±10V and is represented by the shaded area in *Figure 2*.

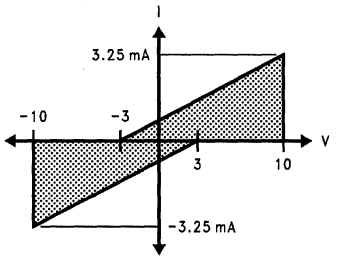

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FIGURE 2. Receiver Operating Range

Also, RS-422 receivers have a ±200 mV threshold over the entire common mode range of ±7V. A differential noise margin ≥1.8V is guaranteed between the driver's differential output swing and the receiver's threshold.

RS-422 drivers and receivers are designed for point-to-point and multi-drop configurations but not multi-point. For multi-drop configurations, a daisy chain is the recommended interface configuration.

Caution, at long distances or high data rates, termination is recommended to reduce reflections caused by a mismatch in the impedance of the cable and the impedance of the receiver's input. Refer to the section entitled "Termination" for further information.

Significantly, the RS-485 differential interface standard is very similar to RS-422. However, there are differences that distinguish the two standards from one another; which include the output stage of the driver, the common mode range of the interface, the input resistance of the receiver, and the drive capability of the driver. For more details concerning the comparison of RS-422 and RS-485, please reference National's application note AN-759.

CABLE LENGTH AND DATA RATE

Cable Length and Data Rate have an inverse affect on each other. When operating at either the recommended maximum cable length or data rate the other can not be obtained. For instance, it is not possible to operate at 4000 feet when operating at 10 Mb/s or vice-versa.

A chart displaying the recommended operational region of a typical RS-422 standard interface is shown in *Figure 3*. Other electrical interface standards operating regions are also shown for comparison. The curves were obtained from empirical data using a 24 AWG, copper, 16 pF/ft, twisted-pair cable parallel terminated with a 100Ω load.

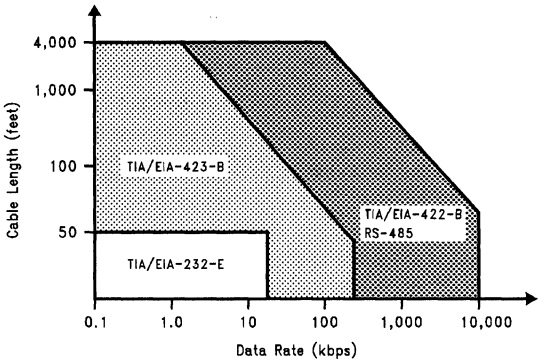

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FIGURE 3. Cable Length vs. Data Rate

TERMINATION

Termination is recommended for use when designing a RS-422 interface that is considered to be a transmission line. An interface is considered to be a transmission line if the propagation delay of the cable is greater than 1/8 the transition (rise or fall) time of the signal. This is a time-domain analysis. The same is also true in frequency-domain.

For clarification, the transition time for the time-domain analysis is measured from zero to one hundred percent of the transition. The rising or falling edge may be used for analysis, whichever edge is the fastest.

Transmission lines may restrict the use of a multi-drop configuration and limit the maximum data rate of the RS-422 interface.

Transmission line theory will not be discussed in this application note but is useful knowledge. For more details on transmission line theory, please refer to National application notes AN-806, AN-807, and AN-808.

Parallel Termination

Parallel termination, a very popular form of termination, has the advantage of allowing higher data rates and longer cable lengths than an interface using some other termination schemes because transmission line effects are minimized. This is possible because the termination resistor (Rt) is chosen to closely match the cable impedance (Z_O) (see *Figure 4*). The cable impedance can be obtained from the cable manufacturer. The cable impedance may also be measured using TDR, time domain reflectometry, techniques. Additionally, because of the minimized affect of the transmission line, multi-drop configurations with good signal quality are also possible, as long as the stubs (discussed later) are not transmission lines themselves.

A disadvantage of parallel termination is the high power dissipation associated with the heavy termination load. This also leads to a smaller differential output voltage and lower DC noise margins than with a series termination. Also, if the receiver has built-in failsafe circuitry, a known output can not be guaranteed with this type of termination scheme unless the receiver specifically says that it supports "terminated" failsafe. The cost associated with purchasing the one external component should also be considered.

Other schemes exist to choose from and each type has its advantages and disadvantages. Please refer to application note AN-903 for more detailed information on parallel and other termination schemes.

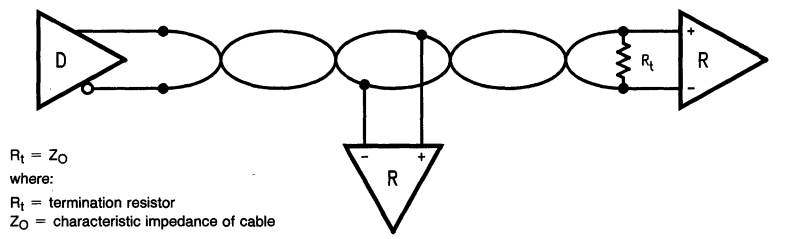
FAILSAFE

For typical RS-422 interfaces, open, terminated, and shorted input are the three types of failsafe to consider as shown in *Figure 5*. A receiver with full failsafe protection guarantees a known receiver output for all three types failsafe conditions.

Open Input Failsafe

Open input failsafe is the condition when the receiver's output is known when its inputs are left open or floating. The driver is not connected but the receiver is powered. A receiver that provides failsafe for an open input condition, may provide failsafe for idle (driver's output idle) and TRI-STATE® (driver's output disabled) conditions if the bus is not parallel terminated. Therefore, the output state of the receiver may be known for both idle and TRI-STATE bus conditions in some instances.

A receiver is able to provide open input failsafe with internal pull-up and pull-down resistors, typically >50 kΩ. Sometimes only one bias resistor is used on one input and the



$R_t = Z_O$
where:
R_t = termination resistor
Z_O = characteristic impedance of cable

TL/F/12598–4

FIGURE 4. Multi-Drop Application with Parallel Termination

other input biased to a voltage reference point. Note that any receiver that does not have built-in failsafe, may use external pull-up and pull-down resistors to provide failsafe protection.

Terminated Input Failsafe

A receiver has terminated failsafe when its output can be determined while its inputs are under terminated conditions. This must be valid for various types of termination schemes; otherwise the receiver does not have terminated failsafe. Additionally, terminated idle line and terminated TRI-STATE line conditions should also be supported. For RS-422 receivers with built-in open input failsafe, the protection circuitry does not guarantee terminated failsafe operation. If a receiver does not have this feature, external bias resistors may be used to provide terminated failsafe protection. For more information please reference application note AN-847 that is devoted to this topic.

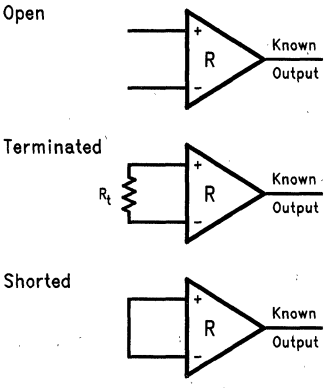


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FIGURE 5. Types of Failsafe

Shorted Input Failsafe

Shorted failsafe is when the receiver output is known when the receiver inputs are shorted together. If a receiver does not have this type of failsafe, external pull-up and pull-down resistors alone may not help. However, using an alternate-failsafe termination technique will provide protection. Please refer to application note AN-903 for details about alternate-failsafe termination.

National's DS36276 and DS36277 are interface devices that provide all three forms of failsafe protection with no external components required. To accomplish this, the threshold point of the receiver was shifted, violating the RS-422 ±200 mV threshold specification.

CONFIGURATION

For RS-422 interface devices, usually three types of configurations are commonly used.

Point-to-Point Configuration

First, point-to-point, is a one driver and one receiver system. Point-to-point applications may be thought of as using single-ended standards like TIA/EIA-232-E because this is the configuration single-ended standards are popular for. However, differential standards are not restricted from use in point-to-point applications. A typical point-to-point system is shown in *Figure 7*.

Multi-Drop Configuration

The second configuration, multi-drop, is one driver with two or more receivers normally connected in a daisy chain layout. For RS-422, the maximum number of receivers is 10 if the receiver's input impedance (R_{IN}) is equal to 4 kΩ or one unit load. If a receiver's R_{IN} is equal to 8 kΩ then that receiver is equal to ½ a unit load. Therefore a RS-422 driver that can drive 10 unit loads can drive 20 receivers with a R_{IN} = 8 kΩ. An example of a multi-drop application is shown in *Figure 4*.

Multi-Point

The last type of configuration is multi-point, which uses two or more drivers connected to one or more receivers (see *Figure 6*). RS-422 drivers are normally not designed into this type of configuration. However, a multi-point system can be accomplished if certain issues are addressed. The three issues are ground potential differences between drivers, contention between drivers, and the drive capability of the drivers. Therefore, RS-485 devices are recommended for multi-point applications.

For further details and illustrations concerning these issues please reference application note AN-759.

ESD PROTECTION

Electrostatic Discharge (ESD) is normally an event of very high potential for a short period of time. This may be damaging to some integrated circuits (IC). ESD is not limited to a one time occurence in the life of an IC, unless it is fatal the very first time. It may be an ongoing transpiration that can wear down an IC until it eventually fails fatally.

The RS-422 standard does not specify requirements for ESD protection. However, the industry has developed a defacto minimum standard of 2,000V ESD protection under human body model (HBM) conditions. However, many systems today require much higher levels of ESD protection. Possibly as high as 10 kV or 15 kV.

ESD protection may be enhanced in different ways. IC protection circuitry, TransZorbs®, and protected connectors are three possible solutions for increasing an IC's ESD

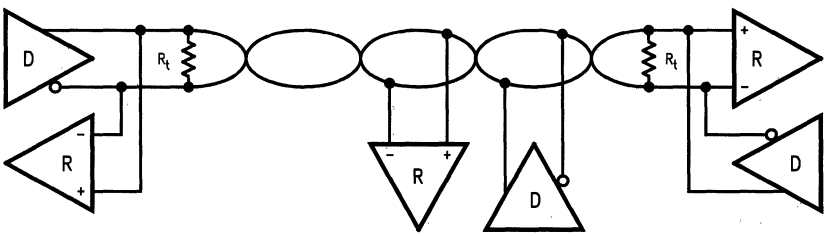

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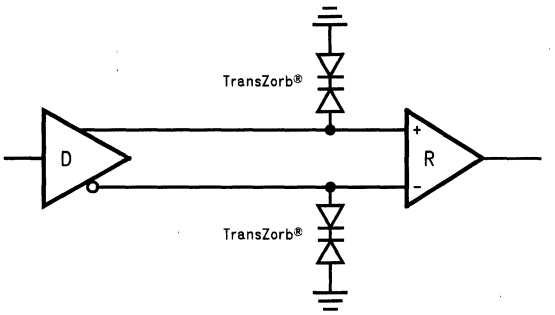
FIGURE 6. Example of Multi-Point Configuration



TL/F/12598–7

FIGURE 7. A Point-to-Point RS-422 System with TransZorbs

protection. The first method is built-in IC protection circuitry that requires no external components. This type of protection is the result of the manufacturer's IC design. In the early years of IC manufacturing, ESD was not as well publicized or standardized as it is today. Today, IC designers strive to achieve five, ten, even fifteen thousand Volts of ESD protection.

The later two solutions, TransZorbs and protected connectors, are both external to the IC and usually implemented, by the system manufacturer, to provide additional protection, if needed, beyond that which is supplied by the IC itself.

Integrated Circuits

IC protection circuitry is normally designed into the die at the input and output stages of the device. This is because these are the stages that connect to the outside world (via cables or other media). Thus, these are the locations damaged most often by ESD phenomenon. The purpose of the circuitry is to, one, be able to drain off very large amounts of current very quickly, and two, keep the high current away from sensitive areas of the IC. An analogy may be made with lightning rods that channel away large amounts of current, caused by a very large electric field (potential), from your house.

TransZorb

TransZorbs are like back-to-back diodes. They are connected between the interface line that needs protection and ground. They act like voltage clamps, clamping voltages that are above the TransZorb's specified reverse stand-off voltage (V_{rs}). Take care when selecting a TransZorb, if the V_{rs} is too high, the IC may become damaged before the TransZorb ever turns on. One TransZorb should be used per interface line. This solution could become expensive as the number of interface lines requiring protection increases. *Figure 7* shows an example of a RS-422 point-to-point system with TransZorbs.

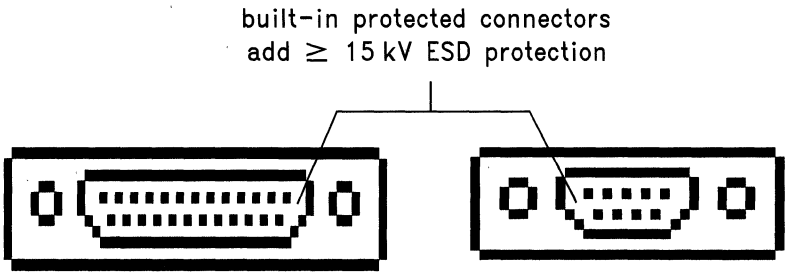
Protected Connectors

Protected connectors, another solution for increasing ESD protection of an IC, provides the same type of clamping protection that TransZorbs do. However, only one device is needed per interface connector. Therefore, if you have a DB-25 pin connector, all 25 lines receive the same increase in ESD damage resistance. Additionally, designers do not need to worry about lack of additional PC board space, since the device is built into the connector. Also, the protected connector only adds an additional 5 pF or 6 pF of capacitance to the signal load. Designers will be able to find protected connectors in a variety of connector sizes. *Figure 8* shows a diagram of two connectors with built-in ESD protection. For more information on protected connectors please refer to application note AN-878.

In the later two solutions, the system manufacturer provides additional ESD protection. Ideally, system manufacturers would like the IC manufacturers to provide all the ESD protection required for their systems, internal to the device. National Semiconductor's Interface Group recognizes the importance of ESD protection and has released the DS36276 and the DS36277 with ESD protection up to 7,500V. Future Interface products will trend toward higher ESD protection.

LIVE INSERTION

RS-422 does not specify how to insert an IC (driver or receiver) into a live interface. The same is true for removing the IC. PC board connectors, cable connectors, and sockets are likely interface points. A device may be inserted live via one of these interfaces. Live insertion is a larger concern, since removing an IC, from a live interface, normally is less damaging to an IC. For live insertion, the device may not be powered up when being inserted. Thus, the RS-422 device may receive bus potentials that exceed the power



TL/F/12598–8

FIGURE 8. Example of Protected Connectors

supply voltage (V_{CC}). First, this may cause biasing of diodes and bus clamping, or result in large current faults that damage devices. Second, the potential difference between ICs connections and the interface connector may be large enough to cause ESD strikes which may be harmful to the IC. In addition, the IC may transmit signals when the supply voltage is below minimum operating level which may result in data transfer errors. On the other hand, when removing an IC from an active interface, the V_{CC} should be within normal operating levels with no device pins higher than the supply pin. Also, the potential difference at the instance of the disconnect is minimized since the potential is the equivalent just prior.

Recommendations for implementing a live interface are, one, use an IC that supports the feature. Look for this feature in the device's datasheet. However, it will not always appear there so be sure to ask the chip manufacturer's technical support group, to be certain. These ICs usually have specially designed input and output structures that prevent damage to the device even if bus voltages exceed V_{CC}. Two, since removal is less harmful than inserting, try to create similar conditions for inserting the chip that would exist when removing the chip. In other words, it is ideal to have the device powered and referenced to the same ground potential as the interface before the inputs and outputs make physical contact.

For a PC board, a staggered connection where the ground trace is the longest, so that it makes contact first, and the V_{CC} trace is the second longest followed by the input traces then the output traces last would suffice. Live insertion via cables or sockets may require special design but should make contact in the same pattern.

BY-PASS CAPACITORS

By-pass capacitors help reduce transients on output signals. Therefore, by-pass capacitors are recommended for better signal quality. One 0.1 μF capacitor is recommended for each powered IC in the system. If a device has more than one power supply (i.e., V_{CC} and V_{EE}) then use one capacitor for each supply. The capacitor should be placed between the power supply pin and ground. Place the capacitor as close to the V_{CC} pin of the device as possible. Additionally, a 10 μF capacitor may be used near the main path where V_{CC} is delivered to the system for bulk charge storage. If a system is large, additional bulk capacitance may be distributed across the system.

STUB LENGTH

Since RS-422 is a multi-drop standard, receivers may be connected to the bus via a stub. The length of the stub is important because of the affect it may have on the signal. As the stub length is increased, its characteristics begin to act as a transmission line. When is a stub considered to be a transmission line? A typical guideline for stubs and transmission lines is stated here:

Time Domain:
If the propagation delay of the stub (one way trip) is greater than 1/8 the transition time, measured from 0% to 100% of the signal transition, then the stub may be considered a transmission line.

The boundary conditions at which a stub begins to act as a transmission line are not precise. Therefore, designers may use slightly different ratios.

Furthermore, the maximum length of the stub depends on the transition time measured at the point of the stub interconnect. This is very important to remember because if the total length of the cable is 1,000 feet, a longer stub can be hung off the cable at 750 feet away from the driver than at 75 feet away from the driver. This is because the cable capacitance slows the transition time of the driver's output as it propagates down the cable and the transition time is longer.

The length of the stub may be increased by slowing down the transition edge at the stub interconnect. This can be done using a bulk capacitance load or a RS-422 driver with output wave shape control like National's DS3691, DS3692, or DS36C280.

To implement a RS-422 interface with stubs of equal length. Apply the stub guideline rule to the stub(s) closest to the driver's output and use this length for the maximum length for all stubs on the interface bus.

If a stub is too long and causes a noticeable reflection, it will be measured positive on the stub because the voltage reflection coefficient is positive since the load impedance Z_L is larger than the stub impedance Z_O. The formula for the reflection coefficient at the load is shown in equation 1.

$$\left\{\Gamma = \frac{Z_L - Z_O}{Z_L + Z_O}\right\}$$

Eq. 1. Load Reflection Coefficient

Note, the load impedance is equivalent to the input impedance of the receiver which is equal to or greater than 4 kΩ. The stub impedance is typically about 100Ω–130Ω. The reflection created at the stub will propagate in both directions away from the stub (see *Figure 9*). Keep in mind that reflections are time dependent events.

RECEIVER POWER OFF CHARACTERISTICS

The receivers characteristics powered down are similar to those when powered up (see *Figure 10*). Therefore, the receiver, when physically connected, may be powered up or down transparent to the RS-422 driver.

Receiver Input Impedance

The receiver input impedance curve is identical for both inputs while the receiver is powered off. The characteristic curves also pass through the (0V, 0 mA) coordinate (see *Figure 10B*). While the receiver is powered on, the impedance of both inputs are the same but the input impedance curves do not pass through the (0V, 0 mA) point. Additionally, the curves may or may not cross the x and y axis at the same points (see *Figure 10A*). For receivers with built-in open input failsafe, the curves will differ by at least 200 mV over operating range.

The input impedance of a RS-422 receiver is guaranteed from −10V to +10V which is the operating range for RS-422 receivers. The 10V is equal to the 7V common mode voltage plus 3V offset voltage.

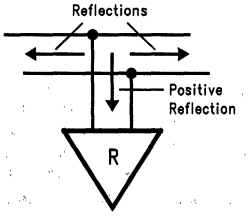


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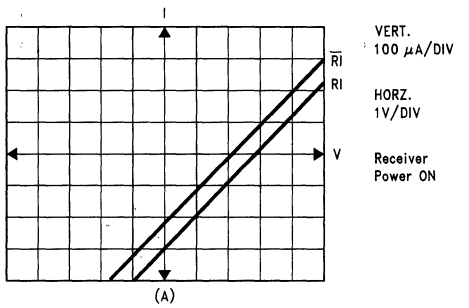
FIGURE 9. Stub Reflections



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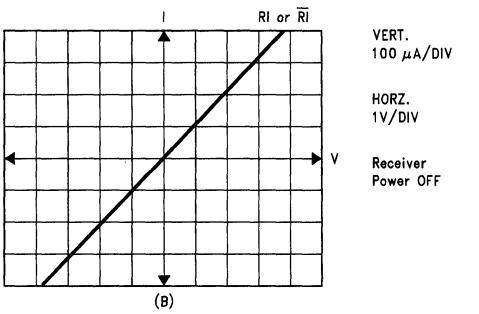

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FIGURE 10. Receiver ON/OFF Characteristics

Receiver Breakdown Voltage

The receiver breakdown voltage is guaranteed to be greater than ±10V whether the receiver is powered on or off. The breakdown point may be found by curve tracing the device out past ±10V. Breakdown voltages may be more than twice the maximum operating voltage.

TYPICAL CABLE MEDIA

Cable Type

Flat or round cables may be used when connecting a RS-422 driver and receiver(s). Twisted pair or non-twisted conductors may be used. Twisted pair cables have an advantage over non-twisted when transmitting differential signals. Twisted pair cables couple noise more symmetrically than non-twisted pair cables. This helps preserve the noise rejection limits of the RS-422 receiver (±7V).

Cable Size

The defacto standard gauge size is 24 AWG. A range of 22 AWG to 28 AWG is acceptable for most applications. For cable length see "Cable Length and Data Rate" section in this application note.

More on Cables

For more details on cable selections, including information concerning shields, insulation, and cable characteristics, refer to application note AN-916.

SUMMARY

RS-422 is a standardized differential electrical interface capable of transmitting data in point-to-point and multi-drop applications. When implementing a RS-422 interface, make sure design-in concerns are addressed at the early stages of design to eliminate problems later in the application, which may be a lot more costly. Understanding RS-422 means understanding the issue associated with the interface.

RS-422 is a well-defined standard and has many applications. However, RS-422 has been superseded by RS-485 which builds onto the existing foundation and creates an even more rugged standard. For more information on RS-485, please reference AN-979.

REFERENCES

1. TIA/EIA-422-B, *Electrical Characteristics of Balanced Digital Interface Circuits,* Electronic Industries Association Engineering Department. Washington D.C. 1994.
2. *INTERFACE: Data Transmission Databook.* National Semiconductor Corporation. Santa Clara, CA 95052. 1994.

Referenced Application Notes:

AN-759	RS-422 vs. RS-485
AN-806	Transmission Lines
AN-807	Transmission Lines
AN-808	Transmission Lines
AN-847	Failsafe
AN-878	ESD
AN-903	Termination
AN-916	Cables

An Introduction to FPD Link

National Semiconductor
Application Note 1032
Susan Poniatowski

THE FPD LINK CHIPSET

The FPD Link (Flat Panel Display Link) chipset is a family of interface devices specifically configured to support data transmission from graphics controller to LCD panels. The technology employed, LVDS (Low Voltage Differential Signaling), is ideal for high speed, low power data transfer. This enables the implementation of high end displays such as SVGA (800 x 600) and XGA (1024 x 768).

The predominant issues limiting performance in these high end displays are speed, power, and EMI considerations. The user is also concerned with the physical interface to the display; the fewer wires the better. The FPD Link chipset addresses these issues with LVDS technology and muxing TTL signals to higher speed LVDS signals which allows a substantially narrower interface between host and display. In a typical application (see *Figure 1*), TTL-level RGB and control data from the graphic controller arrives at the inputs of the FPD Link transmitter. The parallel TTL data is muxed and converted to LVDS. The outputs of the FPD Link transmitter drive the LVDS data on the cable which connects the motherboard to the display. The LVDS data traverses the cable to the FPD Link receiver at the display, The received data is then demuxed, converted back to TTL levels and sent to the inputs of the timing controller. This muxing of parallel TTL signals allows the data to travel at faster speeds across a narrow interface, addressing needs associated with high bandwidth communication.

The FPD Link chipset consists of transmitters (TTL to LVDS) and receivers (LVDS to TTL) designed to support 18-bit and 24-bit color displays. Devices are available with falling edge or rising edge data strobe for a convenient interface to a variety of graphics and LCD panel controllers. The products initially being released operate with a 5V power supply at a clock frequency range of 20 MHz–40 MHz. Additional product offerings include devices supporting a 65 MHz clock, and parts operating with a 3V power supply. See *Figure 2*.

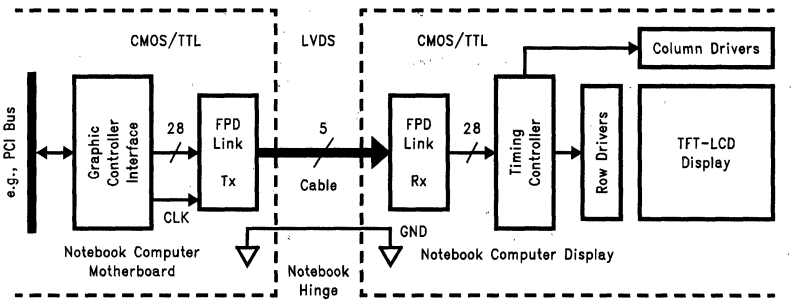

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FIGURE 1. Typical FPD Link Application (24-Bit Color)

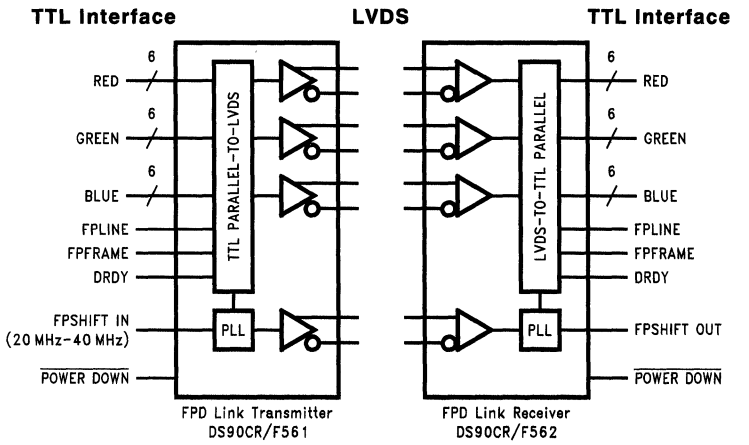

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FIGURE 2. FPD Link Chipset for 18-Bit Color

Initial product offerings are:

DS90CR561/2 — transmitter/receiver, rising edge data strobe, 21-bit TTL interface (6 Red, 6 Green, 6 Blue, 3 Control bits), 4 pairs LVDS (3 data + clock)

DS90CF561/2 — transmitter/receiver, falling edge data strobe, 21-bit TTL interface (6 Red, 6 Green, 6 Blue, 3 Control bits), 4 pairs LVDS (3 data + clock)

DS90CR581/2 — transmitter/receiver, rising edge data strobe, 28-bit TTL interface (8 Red, 8 Green, 8 Blue, 4 Control bits), 5 pairs LVDS (4 data + clock)

DS90CF581/2 — transmitter/receiver, falling edge data strobe, 28-bit TTL interface (8 Red, 8 Green, 8 Blue, 4 Control bits), 5 pairs LVDS (4 data + clock)

LVDS—THE TECHNOLOGY OF CHOICE

LVDS is a differential signaling technology designed to support applications requiring high speed data transfer, common mode noise rejection, and low power consumption. The low signal swing (345 mV) and differential nature of the signals reduces noise impact (i.e., crosstalk) and allows high operating frequencies. The constant current source is designed for low power consumption: a single LVDS driver has a static I_{CC} of 4 mA and dynamic I_{CC} of 22 mA. These attributes contribute to the low EMI of LVDS.

DESIGNING WITH FPD LINK

The FPD Link chipset provides the support needed for high speed display interfaces such as SVGA(800 x 600) and XGA(1024 x 768). Care should be taken when designing with these devices to fully realize the benefits of the technology.

Board Layout. To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer must also maintain equal length on the signal traces for a given pair. As with any high speed design, the impedance discontinuities should be limited (reduce number of vias, no 90° angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. These considerations limit reflections and crosstalk which would adversely effect high frequency performance and EMI.

Termination. Use of current mode drivers requires a terminating resistor across the receiver inputs. The FPD Link chipset uses a single 100Ω resistor between the positive and negative lines of each receiver differential pair (see *Figure 3*). No additional pull-up or pull-down resistors are necessary as with some other differential technologies (PECL). Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

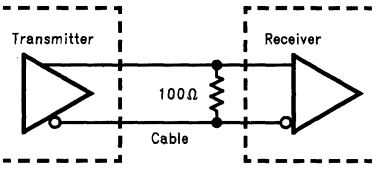

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FIGURE 3. FPD Link Termination

Decoupling Capacitors. Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. Decoupling capacitors (surface mount) between each V_{CC} and ground pin are recommended. Refer to *Figure 4* for an example of connections and capacitor values.

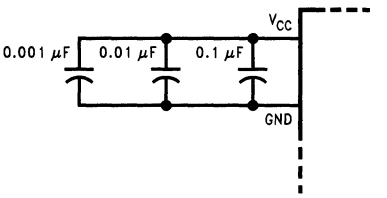

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FIGURE 4. Decoupling Configuration

Cables. A cable interface between the transmitter and receiver needs to support the differential LVDS pairs (2 wires/pair). The DS90CR581/2 and DS90CF581/2 require 10 signal wires; the DS90CR561/2 and DS90CF561/2 require 8 signal wires. This is a significant reduction in cable width as compared to the straight TTL interface which needs 28 or 21 signal wires. Shielded cables will reduce noise emissions that contribute to EMI. In addition, ground lines between each differential pair will provide further noise shielding. The grounding provides a barrier to noise coupling between adjacent pairs, thus reducing additive effects of the electrical fields. In addition to the noise shielding, the low impedance ground connection between the transmitter and receiver provides a common mode return path. A minimum of two ground conductors is recommended to provide this low impedance path.

An ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is recommended that cable skew remain below 350 ps to help maintain a sufficient data sampling window. Edge rate attenuation should also be limited to avoid signal degradation at high frequencies. Both skew and edge rate attenuation are a function of cable length. As the distance between host and display increases, a higher quality cable is needed to preserve signal integrity.

Though the interconnect between host and LCD is typically short, the FPD Link transmitters can drive cables over 5 meters long. This makes the FPD Link useful for remote display applications.

TTL TO LVDS TRANSLATION

The FPD Link transmitter translates 21 or 28 bit wide TTL data into LVDS data 3 or 4 bits wide and 7 bits deep. An additional pair of LVDS signals is used to transmit the clock. All 21/28 parallel TTL bits are transferred with a single data strobe. A single strobe also transmits all bits at the LVDS port. The clock to data relationship at the LVDS interface is shown in *Figure 5.* The clock at the LVDS ports is transmitted at the TTL clock input frequency (i.e., 40 MHz); the data is transmitted at 3.5 times the clock frequency (i.e., 140 MHz).

The TTL data bits are mapped into the 3 or 4 LVDS signal lines. *Figures 6* and *7* show the relationship of parallel TTL data bits to the LVDS link.

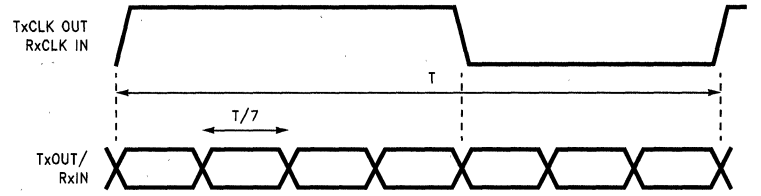

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FIGURE 5. Seven Bits of LVDS in One Clock Cycle

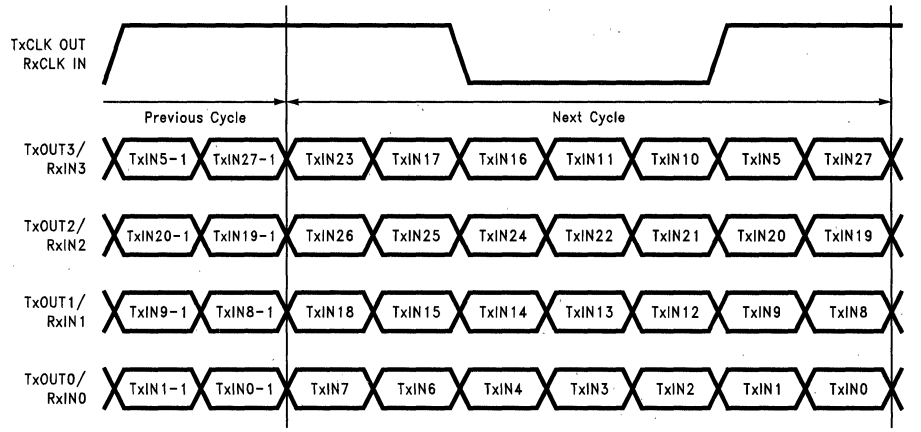

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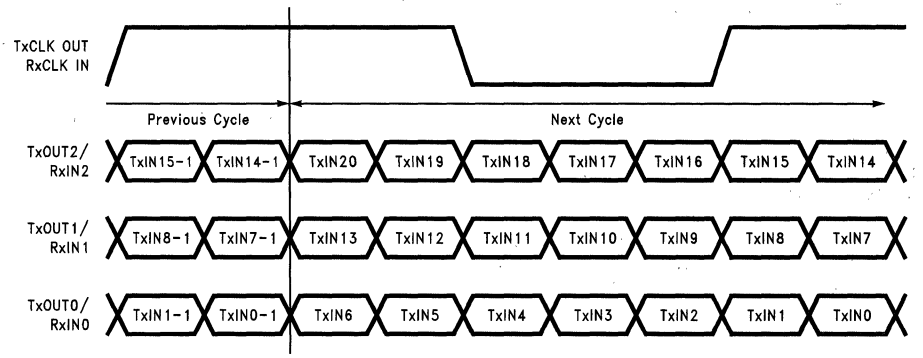
FIGURE 6. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR581)



TL/F/12599–7

FIGURE 7. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR561)

POWER SEQUENCING

Outputs of the FPD Link chip remain in TRI-STATE® until the power supply reaches 3V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 4.5V and the $\overline{\text{Powerdown}}$ pin is above 2V.

When powering down the device, the $\overline{\text{Powerdown}}$ pin may be asserted. This will TRI-STATE the outputs to prevent excess current flow (10 μA maximum). This input is typically driven by power supply control logic.

The FPD Link chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through a diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device. (Note: latchup immunity is > 300 mA) In addition, an external circuit can be used such that when the receiver board powers down, the transmit $\overline{\text{Powerdown}}$ pin is pulled low to TRI-STATE the transmitter outputs so short circuit current does not flow.

CLOCK INVERSION

The FPD Link chipset is available with rising or falling edge data strobe. A rising or falling edge strobe device should be selected based on the characteristics of the timing controller being used. If the strobe of the FPD Link device does not match that of the timing controller, a simple inverting buffer may be used at the transmitter input and receiver output to invert the signal.

CLOCK JITTER CONSIDERATIONS

The FPD Link devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. These high speed signals require an accurate, low noise clock signal. The width of the LVDS data bits is one seventh the clock period. For example, a 40 MHz clock has a period of 25 ns; the width of a data bit is 3.6 ns. Differential signal skew, interconnect skew, data and clock jitter all reduce the available window for sampling data. It is recommended to keep each component as small as possible to support the maximum operating frequency. The initial clock source should provide a clean signal to the Tx clock input. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

EMI BENEFITS

One of the benefits to using the FPD Link chips with their LVDS signaling is the relatively low EMI. LVDS has demonstrated lower spectral content (EMI) than competing technologies such as RS-422, PECL, and CMOS (often used in display interface applications). Testing was performed using DCM (direct contact method) with a 32 MHz continuous wave. Low EMI translates to less noise on a cable in a box-to-box transmission environment. The cable shielding requirements are less, thus the cost of interconnect is reduced.

CONCLUSION

The FPD Link chipset architecture in conjunction with the LVDS technology provides the high bandwidth interface necessary for leading edge display technology. The conversion from parallel TTL to serial LVDS allows for a narrow interface between graphics controller and panel. A narrower interface means lower cable cost and simplifies the physical connection through a notebook hinge. The high speed of the LVDS technology supports the high data transfer rates required. EMI problems typically associated with such high speed transmissions are addressed by the low signal swing and differential nature of LVDS. LVDS, with its high speed capabilities, will allow future products in the FPD Link chipset to support the industry's ever increasing needs for bandwidth. National's FPD Link provides the solution for the latest in display technology.

An Optimized DCE Interface for V.34 Modems Using the DS8933 and DS8934 Line Drivers and Receivers

National Semiconductor
Application Note 1034
John Goldie
Dana Kagimoto

INTRODUCTION

This application note describes the V.34 Modem Interface and the benefits obtained when the DS8933 and DS8934 Line Drivers and Receivers are employed. The following sections are covered.

- V.34 Standard
- DS8934 and DS8933
- Async Application
- Sync Application
- Driver Characteristics
- Receiver Characteristics
- RS-232 and RS-423
- Summary
- References

V.34 THE STANDARD

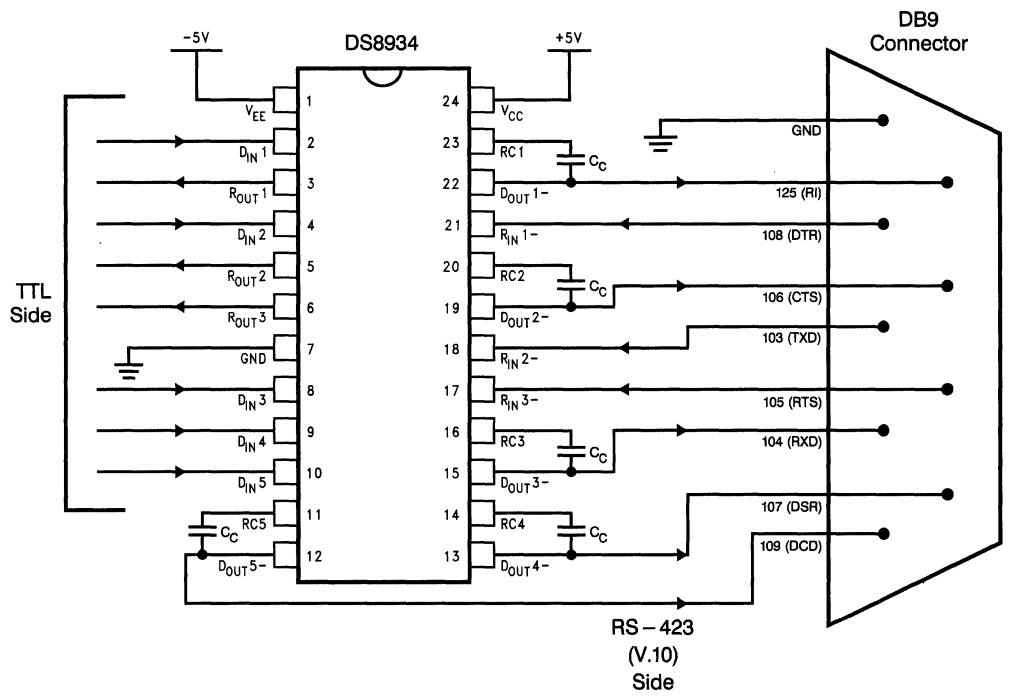
V.34 is the latest dial-up modem standard providing support at 28,800 bits per second. This standard, officially known as a recommendation was developed by the ITU (International Telecommunications Union). 28.8 kbps is only the basic rate, as this class of advanced modems uses sophisticated compression/decompression techniques along with error-correction to provide throughputs above 100,000 bits per second (115.2 kbps typical!) depending upon data patterns and compression scheme used. The impressive 115 kbps presses the de facto RS-232 interface standard to the limit, as it is officially only specified to 20 kbps maximum. For this reason, the ITU selected V.10 (RS-423) instead of V.28 (RS-232) drivers and receivers.

DS8934 AND DS8933

The DS8934 provides five V.10/RS-423 drivers and three receivers in a single 24 lead surface mount package. This configuration provides the correct number of drivers and receivers for an asynchronous interface. The DS8933 is a companion device that provides an additional two drivers and one receiver. Using the two devices together provides the correct configuration for basic synchronous communication. Prior to these devices, multiple packages were required since drivers and receivers were commonly only available in separate packages and were either quad or dual devices. For asynchronous applications, two DS1488 quad RS-232 drivers and one DS1489A quad RS-232 receiver are required, but this solution requires the placement of three devices on the PCB, is RS-232, and is not optimized (3 extra drivers and one extra receiver). Another approach is to mix RS-423 and RS-232 components to establish a hybrid interface. This would employ RS-423 drivers on the high speed lines (data, and clock if synchronous), and RS-232 on the others. This configuration has multiple packages and is not optimized for the application. The DS8934 and DS8933 are optimized parts which save precious PCB real estate, simplify assembly and procurement, and provide multiple operational (electrical) benefits over RS-232 components. The DS8934 offers a substantial cost reduction over a multi package RS-423 interface, and a comparable price against the low end RS-232 multi package solution.

ASYNCHRONOUS - APPLICATION

The DS8934 provides all the necessary drivers and receivers to implement a basic asynchronous interface and is illustrated in *Figure 1*. The five driven lines are: RI, CTS, RXD, DSR, and DCD. The three received lines are: DTR, TXD, and RTS. Driver outputs and Receiver inputs are located on one side of the device to simplify the PCB layout. Additionally the ordering of the drivers and receiver in the package allows for a non-cross over interconnect between the device and the common 9 pin D shell connector. The other side of the device provides the logic interface.



TL/F/12604–1

FIGURE 1. Asynchronous Application

SYNCHRONOUS - APPLICATION

When used together, the DS8934 and the DS8933 provides all the necessary drivers and receivers to implement a basic synchronous interface. This is illustrated in *Figure 2*. The five driven lines in the DS8934 are once again: RI, CTS, RXD, DSR, and DCD. The three received lines in the DS8934 are: DTR, TXD, and RTS. The DS8933 supports the clocking lines required in a synchronous application. The lines TXC and RXC are driven, and ETXC is received. The clock lines are isolated in the DS8933 package.

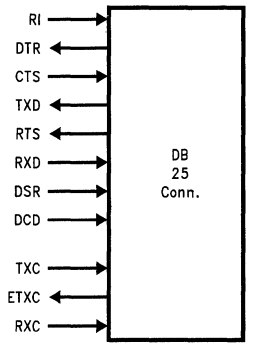


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FIGURE 2. Synchronous Application

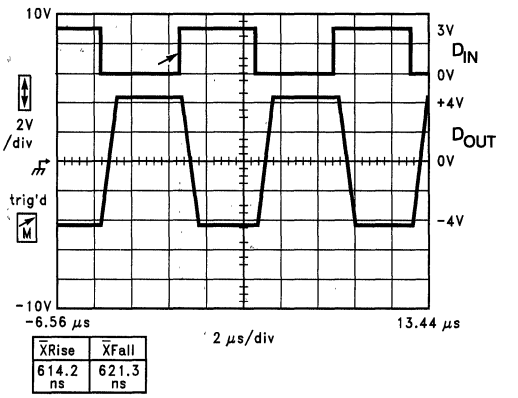
THE V.10/RS-423 DRIVER

The drivers conform to the V.10 and TIA/EIA-423-B standards. They provide an inverting logic function that translates between TTL and RS-423 levels. The driver has a typical input to output delay of 175 ns with a typical output skew of 65 ns. With an IOS of 100 mA, the driver has high drive capability (especially compared to RS-232 drivers at 5 mA IOS). The driver circuit is a low impedance single-ended voltage source producing an output from 4V to 6V in magnitude. Independent driver slew rate control is achieved by using an external capacitor on the driver response control pin. This allows for optimized control for higher speed clock and data lines, while the control lines can be slowed to minimize noise generation. Slew rates can be adjusted up to 60 V/μs. Slew rate is virtually independent of RL and CL (see Table I). In contrast an RS-232 driver's slew rate is dependent upon CL (cable length). The DS8933/34 driver rise time (tr) can be calculated by the following equation: tr = Cc x (54 ns/pF). The slew rate (sr+) can then be calculated by: sr+ = 6V/tr. When laying out the PC board, the response control capacitor should be located as close to the device (driver output) to minimize parasitic. Surface mount capacitors are advised. The driver output waveform is shown in *Figure 3*. Note that a response control capacitor of 10 pF has been used, and the driver is loaded with

2,500 pF and a 3 kΩ resistor (both to ground). Input frequency is 115 kHz (230 kbps), supplies (±5V) and operating temperature is nominal. The driver's output features a ±4V swing with smooth controlled transitions.

TABLE I. Driver Output Characteristics

Response Cap.	Load Resistor	Load Cap.	Rise Time	Slew Rate
15 pF	3 kΩ	2,500 pF	750 ns	8V/μs
15 pF	7 kΩ	50 pF	750 ns	8V/μs



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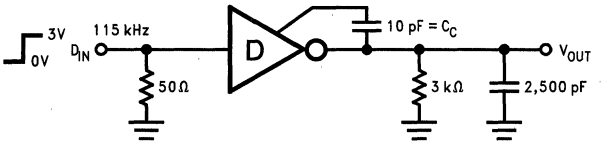

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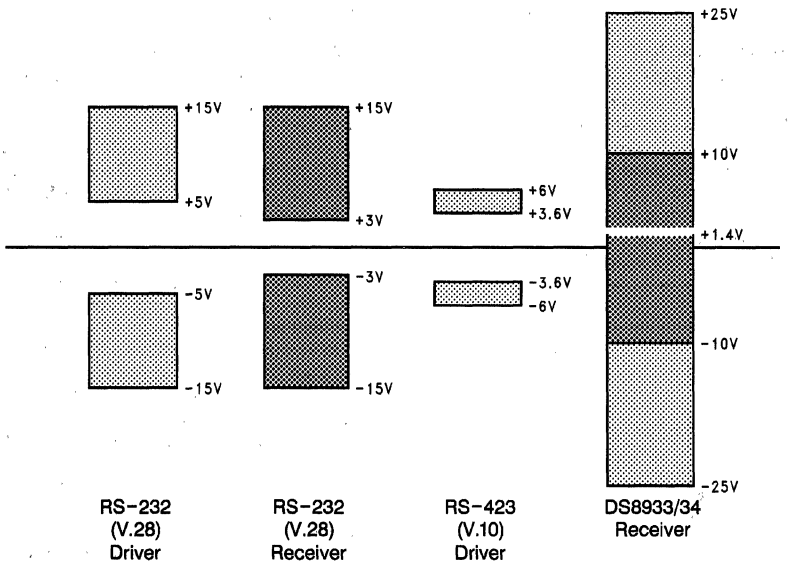
FIGURE 3. Driver Output Waveform



TL/F/12604–3

FIGURE 4. Signaling Levels

THE RECEIVER

The receivers conform to the V.10 and TIA/IEIA-423-B standards. They provide an inverting logic function that translates between RS-423 and TTL levels. The receiver has a typical input to output delay of 30 ns with a typical output skew of 3 ns. The receiver input circuitry accommodates ±25V input signals and 3 kΩ to 8 kΩ input impedance, which assures compatibility with RS-232 drivers. The receiver threshold of +1.4V guarantees a failsafe HIGH output state for an open input state (pulled low by the internal bias resistor) when the cable is unplugged. The offset threshold provides 1V of noise rejection around ground, and also a minimum 2V of noise margin between a V_{IH} of ±3.6V and the threshold at +1.36V (see *Figures 4* and *5*). 40 mV of hysteresis is incorporated to prevent oscillations.

V.28/RS-232 vs V.10/RS-423

The V.28/RS-232 Interface is without contest the most popular interface standard in the world today. The original specification was developed in the early 1960s, and even in its current revision (EIA/TIA-232-E-1991) the maximum specified data rate is still 20,000 bits per second. Unofficially some RS-232 drivers and receivers are capable of operating at higher data rates, however that maximum data rate is cable length (capacitance load) and device (slew rate) specific. With careful component selection, and limitations on capacitance load, it is possible to select a RS-232 driver that is capable of operating at 115 kbps. However, operation at the other end of the cable is not guaranteed, as the DCE manufacturer is in control over the components it selects, but is not in control over the selection of devices inside the DTE (PC). For this reason and others, the ITU recommends the use of V.10 drivers instead of the popular RS-232 components. V.10/RS-423 drivers can easily operate above 500,000 bits per second, are *not* limited by cable length (as RS-232 drivers are), and offer superior wave shaping control. Higher data rate capability is very important as the compression techniques used today double (MNP5) or quadruple (V.42bis) the basic rate of 28.8 kbps, higher ratios are being discussed and 230.4 kbps may not be too far off in the future (some high-end V.34 modems support 230 kbps today!). RS-423 drivers and receivers are however fully compatible with RS-232 drivers and receivers, as backwards compatibility was built into the RS-423 standard.

SUMMARY

The DS8934 provides an economical single chip interface optimized for a V.34 DCE modem interface. When used with the companion device, the DS8933, a basic sync interface is provided with only two small surface mount packages. Additionally, both devices offer the following performance advantages:

Less Noise—RS-423 with its typical output swing of 8V (±4V) compared to RS-232's 16V (±8V) generates less noise, and the receivers provide tight thresholds, thereby maximizing noise margins.

>230 kbps—The drivers easily operate at 115 kbps and are capable of operating above 500 kbps independent of load. This provides an easy upgrade path to high data rates that are already being discussed.

Slew Rate Control—RS-423 drivers provide independent slew rate control, allowing higher speed clock and data lines to be optimally controlled, and control lines slowed to minimize noise generation.

Single Chip—The DS8934 provides a one chip solution for an asynchronous interface saving PCB space, and costs.

Dual Chip—Together the DS8933 and DS8934 support a basic synchronous interface, again saving PCB space over multi-package solutions.

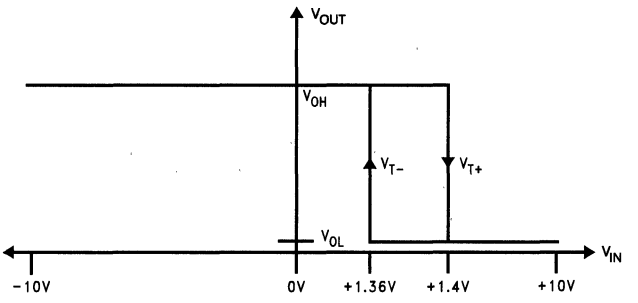
V.10 Drivers—The DS8933 and DS8934 drivers conform to the V.10/RS-423 standards as required by the V.34 standard.

REFERENCES

ITU-T Recommendations: V.10, V.24, V.28, and V.34

TIA/EIA Standards: EIA/TIA-232-E, and TIA/EIA-423-B

National Datasheets: DS8933, and DS8934



TL/F/12604–6

FIGURE 5. Receiver Voltage Transfer Curve (VTC)

PCB Design Guidelines for LVDS Technology

National Semiconductor
Application Note 1035
Syed B. Huq

INTRODUCTION

Technology advances has generated devices operating at clock speeds exceeding 100 MHz. With higher clock rates and pico seconds edge rate devices, PCB interconnects act as transmission lines and should be treated as such. Reflections due to mismatched impedance, cross-talk, die-electric loss, skin effects, dispersion loss and reduction of noise margin are some of the undesirable events seen on high-speed transmission lines. At the same time, the bandwidth limiting factors of the interconnect must be understood. It is these effects that greatly reduce the performance of Si once placed on a PCB.

Understanding controlled impedance, differential signaling layout, de-coupling, terminations, layer stack-up and stub effects, can minimize many pitfalls and reduce cycle time in designing PCB's. This application note gives the PCB designer some common guidelines to follow in designing PCB's for LVDS (Low Voltage Differential Signaling) technology.

CHOOSING THE PROPER MATERIAL FOR PCB

Proper selection of material for high-speed board is essential. As the signal propagates through the interconnect, due to the lossy nature of the interconnect, signal degradation occurs. Er (dielectric constant) of the material and loss tangent or tan delta (Tanδ) are some of the key parameters that explain the lossy nature of PCB's. Er relates to a material's capability to hold charge and Tanδ relates to how much of the energy is lost in the material due to dissipation. Ideally, materials should be selected with the lowest Er and Tanδ. Table I below shows some typical numbers:

TABLE I

Material Selection	Dielectric Constant (Er)	Loss Tangent (Tanδ)
Air	1.0	0
PTFE (Teflon)	2.1–2.5	0.0002–0.002
BT Resin	2.9–3.9	0.003–0.012
Polyimide	2.8–3.5	0.004–0.02
Silica (Quartz)	3.8–4.2	0.0006–0.005
Polyimide/Glass	3.8–4.5	0.003–0.01
Epoxy/Glass (FR-4)	4.1–5.3	0.002–0.02

(Source: DesignSuperCon '95)

As the table above shows, Er is not a constant as we know it and can vary considerably. In most applications, FR-4 material is used, FR-4 material has acceptable performance up to the 100 MHz range, beyond that Teflon should be considered. Teflon tends to be 4X more expensive than FR-4 but as Table I shows, Teflon has a lower Er thus low loss. The lower the Er, the faster the velocity of propagation (Equation 1), the faster the board. The key point to remember is to minimize signal degradation as much as possible.

$$Er = \frac{C}{V} \qquad \text{Equation (1)}$$

Where, C = 0.0118 in/ps (Speed of light)
V = Velocity of Propagation
Er = die-electric constant

PCB manufacturers publish a datasheet along with their boards. This datasheet specifies the Er and Tanδ along with other electrical parameters. Due to process variation, both the Er and Tanδ can change from board to board. Ensure that your PCB manufacturer provides this data on the fabrication material of your board.

You can think of fabricating a PCB board as laying a carpet. The glass-fiber material is held together by epoxy material. Places where the weave is not tight is where the Er can change. Within a single FR-4 PCB a 10% variation of Er is not uncommon and this can alter the propagation velocity of the signal considerably. This can lead to skew issues on signal lines.

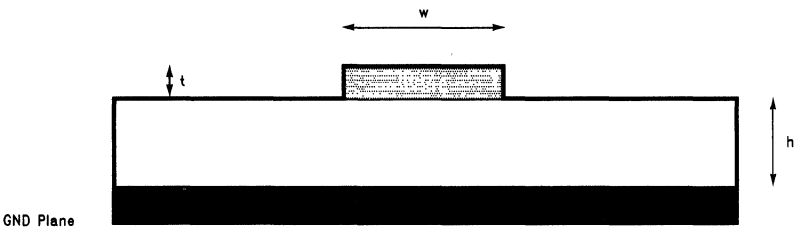
MICROSTRIP OR STRIPLINE?

Microstrip is a PCB trace above the dielectric material whereas a strip line is embedded between the substrate. The decision to use either one mainly depends on the number of layer the boards will be constructed and the complexity of signal routing. Some designs use a combination of both. Usually boards are either 4 layer or 6 and in some cases 8. Due to the high-speed nature of LVDS lines, they need to be seperated from larger swing TTL lines to avoid cross-talk. This can be done by using signals on different layers in a PCB isolated by Power/GND planes.

Delay through a stripline is longer than that of microstrip. Typically, microstrip has a delay of 147 ps/in (FR-4) and stripline has a delay of 188 ps/in (FR-4). Striplines require more via's than microstrip.

HOW TO CALCULATE FOR CONTROLLED IMPEDANCE (SINGLE-ENDED)

For a micro-strip (see *Figure 1*).



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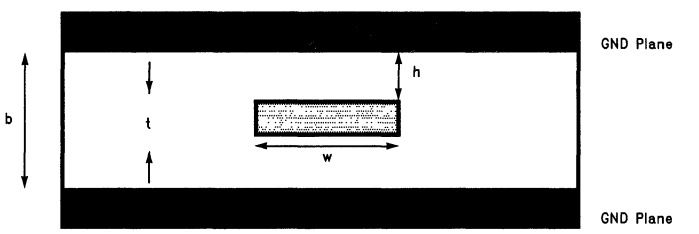
$$Z = \frac{87}{\sqrt{Er + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

Where: Z = trace impedance
Er = die-electric constant
Er = 4.5 (FR-4)
Er = 2.4 (Teflon)
w = width of trace
t = thickness of trace
h = prepeg (die-electric) height

FIGURE 1. Microstrip

Suggested typical numbers for LVDS PCB using microstrip are, t = 1.4 mils, w = 12.0 mils and h = 8.1 mils. This will give a 50Ω impedance from each trace to ground. The critical dimension that must also be taken into account is the distance between the signal pairs. This controls the differential impedance. It is recommended to hold this separation distance constant as much as possible (minor violations may occur at the device and connector connections). Next calculate the resulting differential impedance, and check that it matches the selected media (cable) differential mode characteristic impedance. If it is off substantially, the PCB trace dimensions should be adjusted to provide a match. To prevent reflections the PCB trace pair's impedance should be matched to the interconnect/media. This is also the ideal value for the termination resistor that is connected across the pair at the receiver's input. See AN-905 for more details on the calculation of differential impedance.

For a strip line (see *Figure 2*).



TL/F/12619–2

$$Z = \frac{60}{\sqrt{Er}} \ln\left(\frac{4b}{0.67\,\pi\,(0.8\,w + t)}\right)$$

Where: Z = trace impedance
Er = die-electric constant
Er = 4.5 (FR-4)
Er = 2.4 (Teflon)
w = width of trace
t = thickness of trace
b = height between GND planes
h = prepeg (die-electric) height

FIGURE 2. Stripline

ROUTING OF DIFFERENTIAL LINES

Differential lines have the characteristics of cancelling common mode noise as it appears in phase on the two lines. This cancellation of common mode noise and magnetic effects allow differential drivers and receivers to operate over longer distances. But, this will only work if the two traces are running close to each other. Care should be taken to keep the differential lines as parallel as possible. It is also critical to maintain the electrical/physical length of the two traces to be identical. This guarantees no skew on the line.

A sample layout of LVDS traces *(Figure 3)* shows the mitering effects done on the differential lines to match the electrical/physical lengths.

A sharp orthogonal turn (90°) should be avoided as it causes a sharp change in impedance. An arc should be used instead to round off the edge. This is critical in high frequency board layout.

CROSS-TALK BETWEEN TTL AND LVDS LINES

The PCB designer must note that all TTL/CMOS signal paths need to be isolated from the LVDS signal lines. Crosstalk is directly proportional to dv/dt. Since TTL/CMOS lines have a larger swing, crosstalk can easily occur if the TTL/CMOS paths are right next to the LVDS lines. Separation of the two technologies needs to be made either by increasing the distance between the two or running a ground trace between the two or isolating by using different planes.

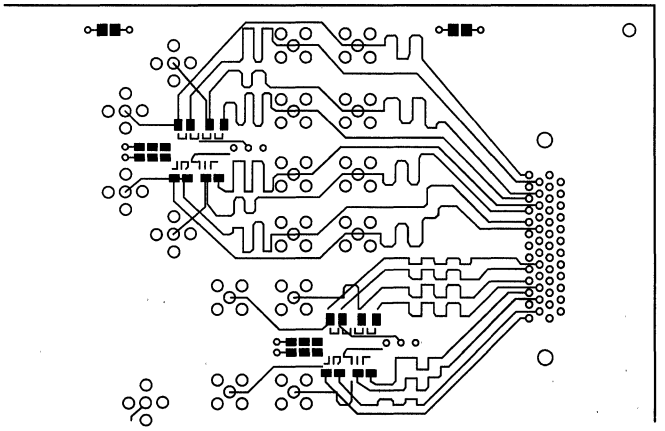


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FIGURE 3. Trace Mitering on LVDS Lines

When configuring a connector interface to a PCB and also for cable/connector interface from PCB to PCB, the designer should allow GND pins in between signal pairs on a connector as well as in a cable.

MISMATCHED IMPEDANCE

A PCB trace can be between 50Ω to 110Ω. As shown in *Figures 1* and *2,* this is dependent on the width and distance from the trace to ground. If a trace is wide and close to the ground plane, it is more capacitive and has an impedance close to 50Ω. If the trace is narrow and a good distance from a ground plane, it is more inductive and approaches 110Ω. Controlling the impedance to the desired value is very critical in avoiding reflections on the line.

Matching of impedance to reduce reflection should also be considered *(Figure 4).* Mismatch in impedance cuts into the noise margin and can ultimately render an application useless. The idea is to properly match the impedance of the media being driven with the same value of termination resistor.

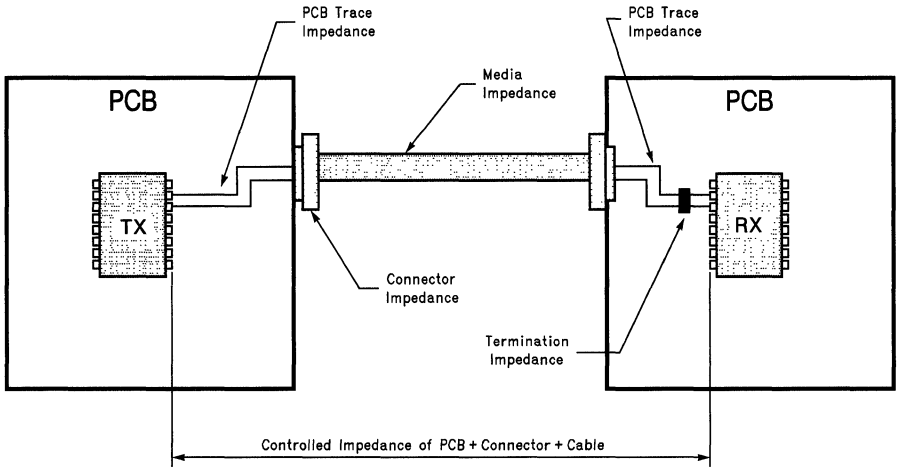

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FIGURE 4. Matching Impedance

TERMINATION RESISTOR PLACEMENT AND STUBS

LVDS Drivers are current mode and they require the termination at the far end of the cable (PCB trace) and as close to the Receiver's inputs as possible. An inch of PC trace stub (see *Figure 5*) can act as an unterminated transmission line causing reflection and this stub should be minimized. Multiple reflections causes ringing, overshoot and undershoot which reduces the noise margin.

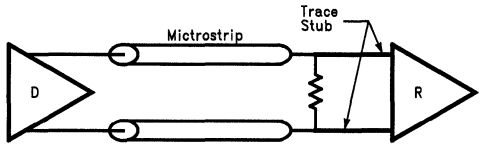

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FIGURE 5. Termination and Trace Stub

In case of probing an LVDS tranmission line, a high impedance (> 1 MΩ) scope probe should be used with a high bandwidth (BW) in the range of 3 GHz–5 GHz and low capacitance (0.25 pF–0.5 pF). Improper probing of a high speed transmission line can give deceiving results.

CHOOSING TERMINATION RESISTORS (SMT)

Various vendors offer resistors in SMT form. A terminating resistor with radial shape can have too much inductance and this should be avoided. Only SMT type chip resistors with a tight tolerance should be used. Recommended tolerance is ± 1% of the termination value (100Ω typical). The user should always use $R_t = Z_O$, termination resistor matched to the media. LVDS Drivers require a termination resistor with a range of 90Ω to 120Ω. SMT form factor also helps to reduce EMI.

DECOUPLING OF V_{CC} LINE

Both the main supply line and the device V_{CC} pins should be properly decoupled. Bulk decoupling at the supply provides a constant low amplitude longer duration current and localized decoupling at the device provides high frequency energy required during SOS (simultaneous output switching) events. Proper decoupling reduces voltage spikes when all I/O pins are simultaneously switching. When decoupling the device V_{CC} pins, the capacitors need to be placed as close to the device V_{CC} pin as possible. Inductance caused by longer lead lengths must be avoided.

MLC (Multi-Layered Ceramic) capacitors in SMT form factor are recommended. Under high frequency, a capacitor is not an ideal element and can behave more like a LCR element. The L and the R are parasitic effects that cause more problems. Since the goal is to reduce inductance in the line, short leads or SMT form factor is critical. It has been seen that a 2:1 length-width aspect ratio can have 2 nH of inductance but a 1:2 (width exceeds length) aspect ratio can cut down the inductance to 0.5 nH in MLC capacitors. For the FPD Link chip set, the recommended bypassing is as follows:

Power Supply: 10.0 μF tantalum electrolytic capacitor

V_{CC}: 0.1 μF, 0.01 μF and 0.001 μF

LVDS V_{CC}: 0.1 μF, 0.01 μF and 0.001 μF

PLL V_{CC}: 0.1 μF, 0.01 μF and 0.001 μF

A sample layout of FPD Link *(Figure 6)* with multiple decoupling per V_{CC} pin is illustrated below. Note the three MLC SMT capacitors per V_{CC} pin. V_{CC} and GND trace width should be wider to reduce inductance and multiple via's are also recommended to help reduce inductance.

In addition to low series inductance, lower effective series resistance (ESR) should be considered when choosing capacitors.

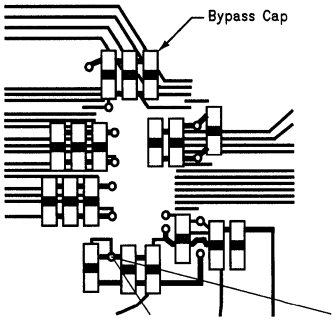


FIGURE 6. Bypass Cap Layout

SUMMARY

High frequency effects should be minimized as much as possible when designing a PCB. Effects such as cross-talk, mismatched impedance, die-electric loss, skin effects, stubs can cut into the noise margin of the design. By following the PCB design guides mentioned in this application note, a designer can ensure success in developing a PCB for LVDS technology by avoiding all the high speed pit falls that are present in PCB designs today.

REFERENCES

Designing the System from the Materials Up, Martin P. Goetz: DesignSupercon95.

LinesimPRO owners manual: Hyperlynx Inc.

LVDS Demonstration Board: National Semiconductor Corp.

AN-971: An Overview of LVDS Technology: National Semiconductor Corp.

Section 15

Bus Circuits Application Notes

Section 15 Contents

National Semiconductor

Application Note—Selection Guide
Bus Circuits

Application Note Number AN-XXXX	Title	Devices Referenced	Related Standard Area
AN-259	The Bus Optimizer	DS3662	
AN-336	Understanding Integrated Circuit Package Power Capabilities		All
AN-337	Reducing Noise on Microcomputer Buses	DS3662	
AN-450	Small Outline (SO) Package Surface Mounting Methods		All
AN-514	Timing Analysis of Synchronous and Asynchronous Buses	DS3896 DS3893	BTL
AN-725	PI-Bus	DS1776	PI-Bus
AN-738	Signals in the Futurebus+ Backplane		BTL
AN-744	Futurebus+ Wired-OR Glitch Effects and Filter	DS3884	BTL
AN-829	IEEE 1194.1 BTL Enabling Technology for High Speed Bus Applications		BTL
AN-834	Live Insertion with BTL Transceivers	DS388X	BTL
AN-835	Futurebus+ BTL Grounding Scheme	DS388X	BTL
AN-839	BTL Power Dissipation Calculation	DS388X	BTL

DS3662—The Bus Optimizer

National Semiconductor
Application Note 259
R. V. Balakrishnan

I. INTRODUCTION

A single ended Bus is an unbalanced Data Transmission medium, which is timeshared by several system elements. Like any unbalanced system, it is highly susceptible to common-mode noise, such as ground noise and crosstalk. In general, the latter determines the maximum physical length of the Bus that can be incorporated with acceptable reliability. Crosstalk is a major problem in high speed computer Buses which employ Schottky Transceivers for increased data rate capability. It is therefore highly desirable to minimize crosstalk noise in Bus circuits to allow for longer Buses and to provide higher system reliability.

This article describes the operation of the DS3662 Quad High Speed Trapezoidal Bus Transceiver, which has been specially designed to minimize crosstalk problems. The Driver generates precise Trapezoidal waveforms that reduce noise coupling to adjacent Bus channels. The Receiver uses a low pass filter, whose time constant is matched to the Driver slew rate to provide maximum noise rejection with acceptable signal delay characteristics. Precision high speed circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky Transceivers.

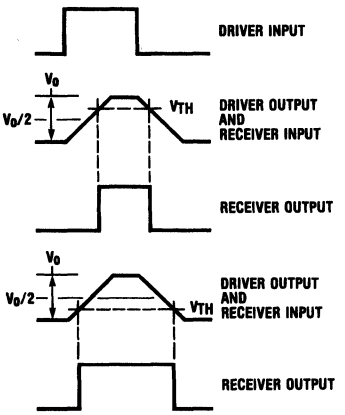
II. THE PROBLEM

Conventional Bus Drivers are designed to provide high output currents for charging and discharging relatively large Bus capacitances quickly. These high speed transitions are characterized by peak slew rates of up to 5V/ns around the mid-region of the transition. This can cause considerable noise coupling to adjacent lines, commonly referred to as crosstalk. Crosstalk also includes noise induced by sources external to the Bus. Additional noise may be generated due to reflections at imperfect terminations.

Bus Receivers are designed to respond to high speed transitions and to provide low propagation delays. Unfortunately, their fast response results in high noise sensitivity. The combined effect of the noise on the Bus and the sensitivity of the Receiver to the noise severely limits the Bus performance.

III. THE SOLUTION

The above situation can be considerably improved by employing noise reduction techniques in both the Driver and the Receiver circuits. Slew rate control can be used in the Driver to reduce crosstalk, and Receiver noise sensitivity can be reduced by using a low pass filter at its input. These techniques are commonly used in line transmission circuits where the associated data rates in general are considerably lower. However, these techniques do present some difficulties in high speed Bus circuits. Increased rise and fall times, resulting from slew rate control, can affect data rates unless care is taken to limit the maximum rise and fall times to minimum pulse width requirements. With any appreciable slew rate control, the rise and fall times of the resulting Driver output waveform will be comparable to the pulse widths at maximum data rates. This condition dictates high fidelity of the transmitted waveform and precise Receiver thresholds at the middle of the Bus voltage swing in order to minimize pulse width distortion. *Figure 1* illustrates the different sources of pulse width distortion due to the trapezoidal nature of the signal.



DISTORTION DUE TO OFF CENTERED RECEIVER THRESHOLDS (V_{TH})

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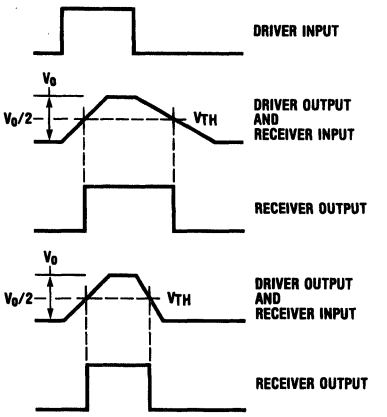

DISTORTION DUE TO NON SYMMETRICAL TRAPEZOIDAL DRIVER OUTPUT WAVEFORM

TL/F/5857–2

FIGURE 1. Pulse Width Distortion

The low pass filter in the Receiver should provide optimum noise rejection without introducing excessive delay in passing the signal waveform. In addition, the Receiver should have a symmetrical response to positive and negative going transitions in order to maintain a low level of pulse width distortion, as well as equal noise rejection to positive and negative going noise pulses. The response of an ideal low pass filter to signal and noise pulses is shown in *Figure 2.*

The DS3662 overcomes these and other problems by using high speed linear circuitry with on-chip capacitors for controlling slew rate and low pass filtering. The Driver is of open collector type intended for use with terminated 120Ω Buses. The external termination consists of a 180Ω resistor from the Bus to +5V logic supply with a 390Ω resistor from the Bus to ground. Such a termination results in a Bus logic high level of 3.4V with V_{CC} at 5V (See *Figure 2*). The Bus can be terminated at one or both ends as shown in *Figure 3.*

IV. THE DRIVER

Using a Miller integrator circuit, the Driver generates a linearly rising and falling waveform with a constant slew rate of 0.2V/ns (typical) during the entire period of transition. This corresponds to typical rise and fall times of 15 ns. *Figure 4* compares the output waveform of a typical Schottky Driver and the DS3662 under different capacitive loads. It should be noted that even under heavy loading, the regular Drivers have peak slew rates that are considerably higher than the average. In contrast, the trapezoidal waveform provides considerably lower slew rate with slightly higher rise and fall times. Such an increase in rise and fall time has very little effect on data rates. In fact, the high fidelity of the transmitted waveform allows pulse widths as low as 20 ns to be transmitted on the Bus, as shown in *Figure 5.*

The block diagram of the Driver is shown in *Figure 6* and *7.* When a high to low transition is applied to the input, switch 'S' opens and node 'A' is pulled low by the current source 'I'. This switches the amplifier output to a high state. The slew rate of the output transition is limited by the charging current through the capacitor, a constant value equal to I/C volts/sec.

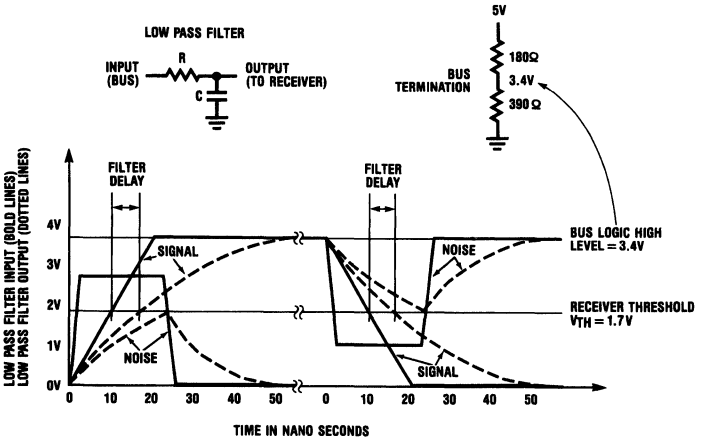

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FIGURE 2. Ideal Receiver Low Pass Filter Response

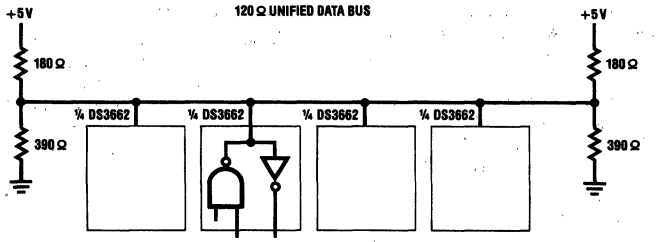

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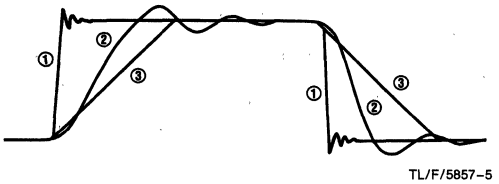
FIGURE 3. Bus Termination



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①—Typical High Speed Driver Output Unloaded

②—Typical High Speed Driver Output Loaded

③—Typical Output of Controlled Slew Rate Driver Which is Load Independent

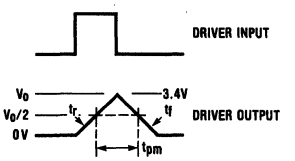
① $t_r = t_f \sim 3$ ns

② $t_r = t_f \sim 10$ ns

③ $t_r = t_f \sim 15$ ns

Note: The word "loading" here refers to capacitive loading only.

FIGURE 4. Waveform Comparison



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$t_{pm} \approx 20$ ns $\quad t_r \approx t_f \approx 15$ ns (10% to 90%)

FIGURE 5. Minimum Pulse Width Driver Output

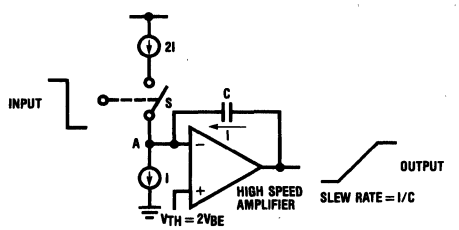

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FIGURE 6. Driver

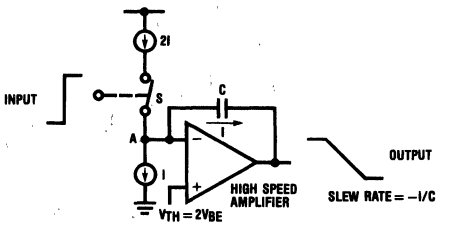

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FIGURE 7. Driver

Likewise, when a low to high transition is applied to the input, switch 'S' closes and node 'A' is pulled up by the '21' current source, switching the amplifier output to a low state. The capacitor now has an equal but opposite charging current which once again limits the slew rate to $-I/C$ volts/sec. The inherent tracking ability of I.C. current sources provide equal rise and fall times resulting in a symmetrical output waveform.

The on-chip capacitors are fabricated using back to back junction diodes. The use of junction capacitors reduces die area and the back to back connection allows operation with either polarity. The capacitor terminal, connected to the amplifier input, remains at $V_{th} \cong 1.6V$ during the output transition. This voltage, being close to the middle of the output swing, reduces the effect of the capacitor voltage sensitivity on the output waveshape.

V. THE RECEIVER

The Receiver consists of a low pass filter followed by a high speed comparator with a typical threshold of 1.7V (see *Figure 8*). This threshold value corresponds to the mid-point voltage of the 0 to 3.4V Bus swing. It is derived from a potential divider allowing the Bus logic levels to track with V_{CC} variations. If the low pass filter capacitor is voltage insensitive, this circuit will provide equal propagation delay for positive and negative going signal transitions on the Bus. In addition, it will also provide equal noise rejection to a positive and negative going pulse (see *Figure 2*). However, the junction capacitors, being voltage sensitive, will exhibit non-symmetrical response in the above circuit. This problem is overcome in the DS3662 Receiver by using a back to back junction capacitor with the ground end biased at 1.7V (see *Figure 9*). Although the capacitor still varies with the voltage at node 'A', the variation is symmetrical about 1.7V (the middle of the Bus swing) and therefore will provide an identical response to transitions of either polarity.

VI. TRANSCEIVER PERFORMANCE

The characteristics of the trapezoidal Transceiver are fully detailed in the device data sheet. Some of the more important specifications are discussed below. Both AC and DC specifications are guaranteed over a 0–70°C temperature range and a supply range of 4.75–5.25V.

The Driver typically has a propagation delay of 15 ns with a maximum of 30 ns. The Receiver propagation delays are specified at 25 ns typical and 40 ns maximum. The Driver output rise and fall times are guaranteed to be within 10 to 20 ns with a typical of 15 ns. The noise immunity of the Receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the Receiver (see *Figure 10*). The Receiver typically rejects a 20 ns pulse going positive from ground level or going negative from a 3.4V logic 1 level. Worst case rejection is specified at 10 ns.

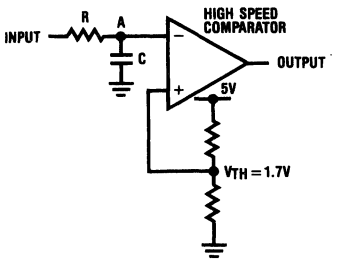

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FIGURE 8. Receiver

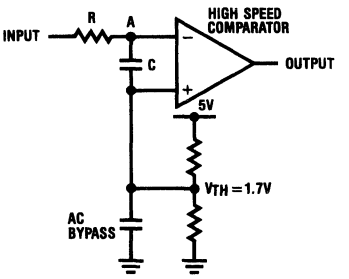

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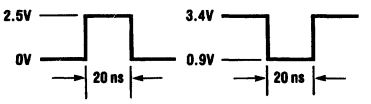
FIGURE 9. Receiver



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Rejects positive or negative going noise pulses of pulse widths up to 20 ns typical.
Detects and propagates trapezoidal signal pulses in 20 ns typical.

FIGURE 10. Receiver Noise Immunity

The AC response of the DS3662 Driver and Receiver are depicted in *Figures 11* and *12* respectively. *Figure 11* shows the typical Driver output waveform as compared to a standard high speed Transceiver output. Oscillograms in *Figure 12* demonstrate the ability of the Receiver to distinguish the trapezoidal signal from the noise. Here the Receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (= 16 ns) of the same amplitude (The signal is triangular since the pulse width is smaller than the rise and fall time of the Trapezoidal Driver output).

The performance of the Transceiver under actual operating condition is demonstrated in *Figures 13* through *15*. Oscillograms in *Figure 13* clearly show the capability of the DS3662 in real life situations. Here it is compared with the DS8834 under identical conditions. The Transceivers drive a minicomputer Bus (flat ribbon cable) 100 feet long, terminated at the far end with taps at various lengths for connecting to the Receiver input. The cable is randomly folded to generate crosstalk between the various parts. In addition a noise pulse is induced on the signal line by driving an adjacent line with a pulse generator. This corresponds to the second dominant pulse in the Bus waveforms at approximately 600 ns from the main signal pulse. As can be seen, the DS8834 with fast rise and fall times on the Driver output generates more crosstalk and its Receiver easily responds to this crosstalk and to the externally induced noise (even though it has hysteresis!), limiting the useful Bus length to less than 10 feet. In contrast, the DS3662's Driver generates much less crosstalk and its Receiver is immune to the induced noise even when the noise amplitude exceeds the signal amplitude as seen in the oscillogram at 50 feet. When the same experiment was repeated with the DS8641, it responded to the noise even at 10 feet as shown in *Figure 14*.

Figure 15 shows the plots of maximum data rate versus line length for the three Transceivers discussed above under two different conditions. The graph in *Figure 15a* is obtained with no consideration to the pulse width distortion whereas the one in *Figure 15b* is obtained for a maximum allowable pulse width distortion of ±10%. A square waveform is used so that the pulse width distortion criteria will apply to both positive and negative going pulses. These graphs clearly show that the DS3662 can be used at considerably higher data rates with lower distortion for longer distances than the other two Transceivers *(Figure 15b)* although the others have a slightly higher data rate capability at short distances with high timing distortion *(Figure 15a)*.

VII. CONCLUSION

The DS3662, with its combination of a trapezoidal Driver and a noise rejecting Receiver utilizing on chip capacitors, represents a significant improvement in high speed Bus circuits and a solution to Bus noise problems commonly encountered in Mini and Microcomputer systems.

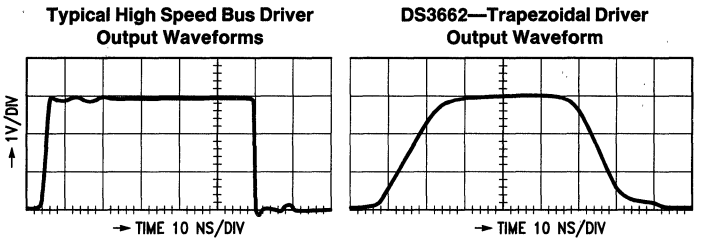

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FIGURE 11

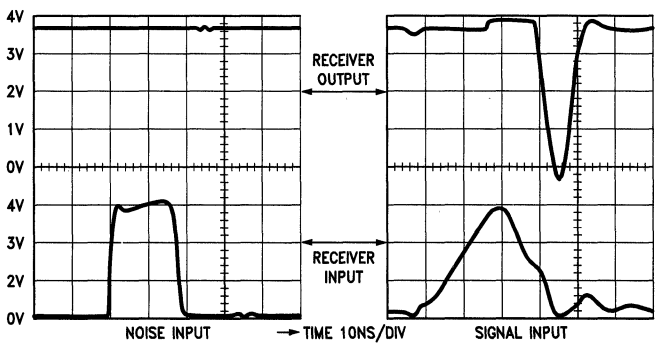

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FIGURE 12. DS3662 Receiver Response

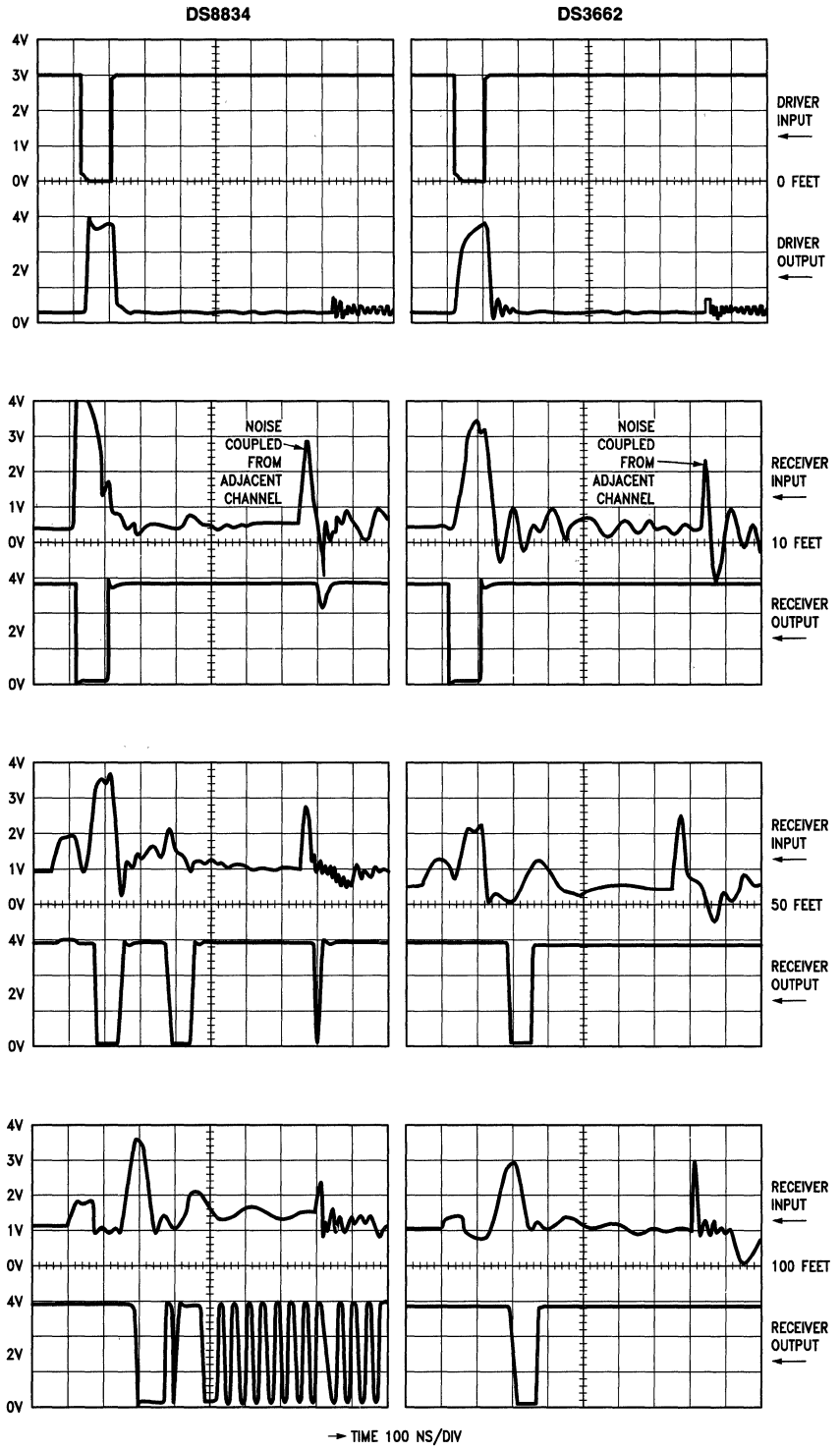
DS8834
DS3662
4V
3V
2V
1V
0V
DRIVER INPUT
0 FEET
DRIVER OUTPUT
TL/F/5857–14
NOISE COUPLED FROM ADJACENT CHANNEL
RECEIVER INPUT
10 FEET
RECEIVER OUTPUT
TL/F/5857–15
RECEIVER INPUT
50 FEET
RECEIVER OUTPUT
TL/F/5857–16
RECEIVER INPUT
100 FEET
RECEIVER OUTPUT
TIME 100 NS/DIV
TL/F/5857–17

FIGURE 13

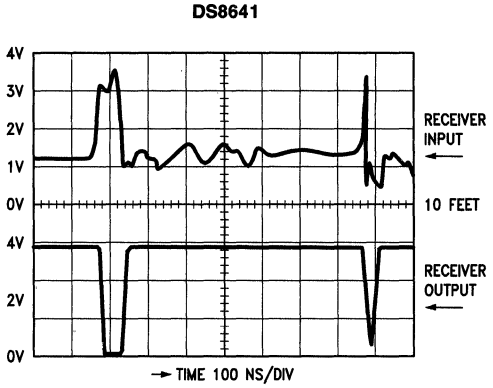

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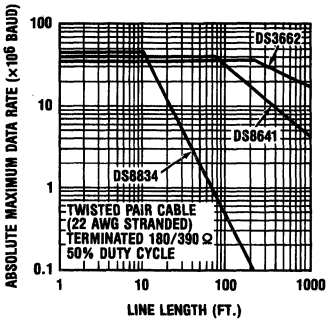
FIGURE 14



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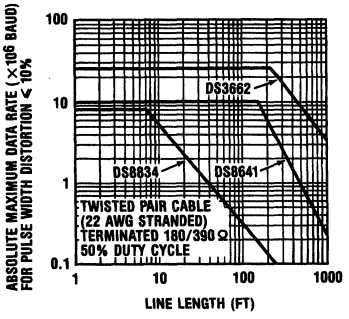

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FIGURE 15. Data Rate vs. Line Length

Reducing Noise on Microcomputer Buses

National Semiconductor
Application Note 337
R. V. Balakrishnan

Abstract: *This paper focuses on the noise components that have a significant impact on the performance of a high speed microcomputer bus. An overview of their nature is followed by ways to minimize their contribution by suitable design of the PC board backplane, the termination network and the bus transceiver. The DS3662 trapezoidal bus transceiver, which is specifically designed to minimize such noise on high speed buses, is presented along with its performance data. And to conclude, some possible new transceiver designs for further improvement of the bus performance are explored.*

INTRODUCTION

As the microcomputer bus bandwidth is extended to handle ever increasing clock rates, the noise susceptibility of a single-ended bus poses a serious threat to the overall system integrity. Thus, it is mandatory that the various noise contributions be taken into account in the design of the bus transceiver, the PC board backplane and the bus terminations to avoid intermittent or total failure of the system.

Although noise such as crosstalk and reflections are inevitable in any practical bus configuration, their impact on the system can be determined and minimized by careful design of all three components mentioned above. The combined contribution of the noise under worst-case conditions should be within the noise margin for reliable bus operation.

The design of the transceiver plays a significant role in minimizing crosstalk and reflection. The bus can be optimized for minimum noise at a given bandwidth by using a trapezoidal driver having suitable rise and fall times along with a matched low pass filtered receiver which provides a symmetrical noise margin. The DS3662 is one such transceiver, the first member in the family of trapezoidal bus transceviers available from National Semiconductor Corporation. This device represents a significant improvement in high speed bus circuit design and provides a solution to commonly encountered bus noise problems.

THE MICROCOMPUTER BUS

A typical microcomputer bus usually consists of a printed circuit board backplane with signal and ground traces on one side and a ground plane on the other. The length ranges from a few inches to several feet with as many as 32 closely spaced (0.6″ typical) card edge connectors. Each signal line interacts with the ground plane to form a transmission line with characteristic impedance 'Z' in the range of 90Ω–120Ω typical. It is desirable to have as large a 'Z' as possible in order to reduce the drive requirement of the bus driver and to reduce the power dissipated at the terminations. But much larger values of 'Z" translate to significantly larger physical dimensions and therefore are not very practical.

The bus appears like a transmission line to any signal having a transition time 't_r' less than the round trip delay '$2T_L$' of the bus. The bus delay 'T_L' is given by:

$$T_L = L\sqrt{L1\ C1} \quad (1)$$

where L = length of the bus
$L1$ = distributed inductance per unit length
$C1$ = distributed capacitance per unit length

For a typical unloaded 100Ω microstrip line, C1 ≅ 20 pF/ft and L1 ≅ 0.2 μH/ft. Therefore, T_L = 2.0 ns/ft. This corresponds to approximately half the speed of light. However, the capacitive loading at each connector on the backplane increases the delay time significantly. The loaded delay time 'T_{LL}' is given by:

$$T_{LL} = T_L\sqrt{1 + (C_L/C_1)} \quad (2)$$

where C_L = distributed load capacitance/unit length

Given a 10 pF loading at each connector (connector + transceiver capacitance) and a 0.6″ spacing between connectors, C_L = 200 pF/ft and T_{LL} = 6.6 ns/ft. So even a 6″ long bus has a $2T_{LL}$ = 6.6 ns, which is higher than the transition time (t_r) of many high speed bus drivers. When in doubt, it is always better to use the transmission line approach than the lumped circuit approach as the latter is an approximation of the former. Also, the transmission line analysis gives more pessimistic (worst-case) values of crosstalk and reflection and is, hence, safer.

CROSSTALK REDUCTION

The crosstalk is due to the distributed capacitive coupling C_C and the distributed inductive coupling L_C between two lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 1.* Their respective peak amplitudes are:

$$V_{NE} = K_{NE}(2T_L)(V_I/t_r) \quad \text{for } t_r > 2\,T_L \quad (3)$$

$$V_{NE} = K_{NE}(V_I) \quad \text{for } t_r < 2\,T_L \quad (4)$$

$$V_{FE} = K_{FE}(L)(V_I/t_r) \quad (5)$$

where V_I = signal swing on the drive line.

The coupling constants are given by the expressions:

$$K_{NE} = \frac{L(C_C Z + L_C/Z)}{4T_L} \quad (6)$$

$$K_{FE} = \frac{C_C Z - L_C/Z}{2} \text{ ns/ft} \quad (7)$$

The near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of near and far end crosstalk waveforms shown.

It should be noted from expressions 6 and 7 that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it. In microstrip backplanes the far end crosstalk pulse is usually the opposite polarity of the original signal.

Although the real world bus is far from the ideal situation depicted in *Figure 1,* several useful observations that apply to a general case can be made:

1. The crosstalk always scales with the signal amplitude.

2. Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.

3. Far end crosstalk width is always t_r.

4. For $t_r < 2T_L$, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is a function of physical layout only.

5. The higher the value of 't_r' the lower the percentage of crosstalk (relative to signal amplitude).

The corresponding design implications are:

1. The noise margin expressed as a percentage of the signal swing is what's important, not the absolute noise margin. Therefore, to improve noise immunity, the percentage noise margin has to be maximized. This is achieved by reducing the receiver threshold uncertainty region and by centering the threshold between the high and low levels.

2. Smaller signal amplitude with the same transition time reduces bus drive requirements without reducing noise immunity.

3. Far end crosstalk is eliminated if the receiver is designed to reject pulses having pulse widths less than or equal to t_r.

4. When $t_r < 2T_L$, the near end crosstalk immunity for a given percentage noise margin has to be built into the backplane PC layout. Since $(V_{NE}/V_I) = K_{NE}$ for this case, K_{NE} should be kept lower than the available worst-case noise margin. K_{NE} may be reduced by either increasing the spacing between lines or by introducing a ground line in between. The ground line, in addition to increasing the spacing between the signal lines, forces the electric field lines to converge on it, significantly reducing crosstalk.

5. For minimum crosstalk the rise and fall times of the signal waveform should be as large as possible consistent with the minimum pulse width requirements of the bus. A driver that automatically limits the slew rate of the transition can go a long way in reducing crosstalk.

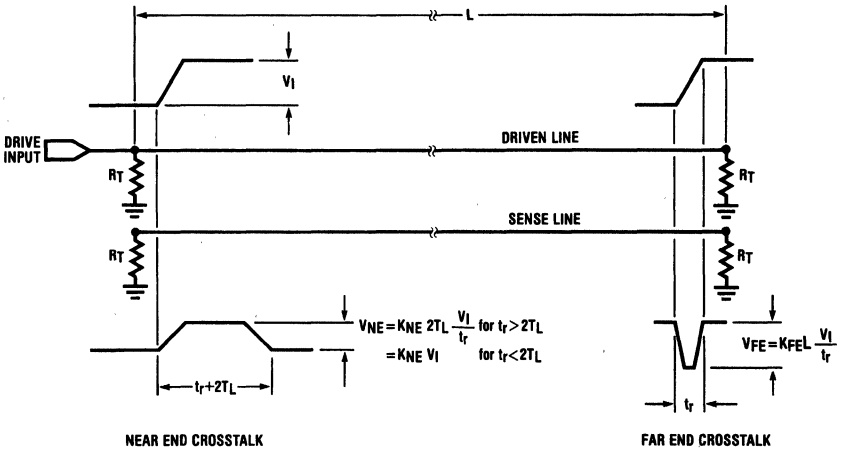

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FIGURE 1. Crosstalk under Ideal Conditions

CROSSTALK MEASUREMENT

When multiple lines on either side of the sense lines switch simultaneously the crosstalk is considerably larger, typically 3.5 times the single line switching case for microstrip backplanes. Also, the location of the drivers on the driven lines and the receiver on the sense line for worst-case crosstalk differs for the near end and far end cases as shown in *Figure 2* and *3* for a uniformly loaded bus. But if the far end crosstalk is not of the opposite polarity, then the combined effect of far end and near end crosstalk could have a larger amplitude and pulse width at a point near the middle of the sense line in *Figure 2*. So in a general case, or in the case of a non-uniformly loaded bus, it is advisable to check the sense line at several locations along the length of the bus to determine the worst-case crosstalk. The measurement should be made for both the positive and the negative transition of the drive signal.

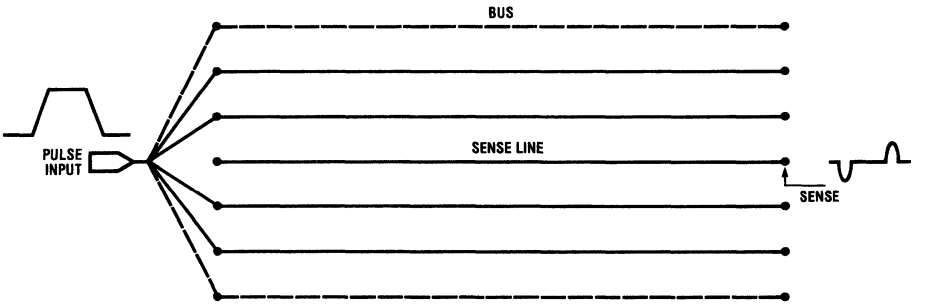
THE TERMINATION

A properly terminated transmission line has no reflections. But a practical microcomputer bus is neither a perfect transmission line nor is it properly terminated under all conditions. The capacitive loading at discrete locations, such as a used card slot, act as sources of reflection. However, in the limiting case when the bus is uniformly populated with a large number of modules, the bus behaves like a lower impedance transmission line. The loaded impedance 'Z_L' of the bus is given by the expression:

$$Z_L = \frac{Z}{\sqrt{1 + C_L/C_1}} \quad (8)$$

where Z = unloaded line impedance

Unfortunately, uniform loading of the bus is not guaranteed at all times and even if it were (by dummy loading of



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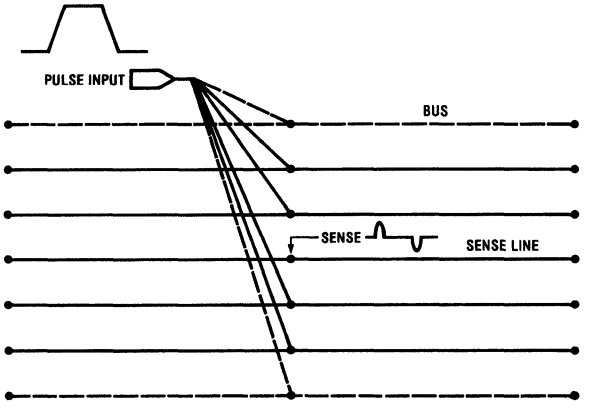
Note: All lines terminated at both ends (not shown)

FIGURE 2. Worst-Case Far End Crosstalk Measurement



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Note: All lines terminated at both ends (not shown)

FIGURE 3. Worst-Case Near End Crosstalk Measurement

the unused slots) Z_L is usually too low for proper termination of the bus. For example, a 10 pF per module loading of the 100Ω microstrip bus at 0.6" spacing results in a $Z_L = 30\Omega$. One such termination at each end will require a 200 mA drive capacity on the bus driver for a nominal 3V swing. Such large drive currents and low value terminations increase the power dissipation of the system significantly in addition to causing other problems such as increased ground drop, inductive drops in traces due to large current being switched, etc. As a compromise the bus is usually terminated at an impedance higher than Z_L but less than or equal to Z. Consequently, there is always some amount of reflection present. For a perfect transmission line the reflection coefficient 'Γ' is given by the well known expression:

$$\Gamma = \frac{Z - R_t}{Z + R_t} \quad (9)$$

where Z = impedance of the bus

R_t = termination resistance

The net effect, in the general case of a nonuniformly loaded bus, is that it may take several round trip bus delays after a bus driver output transition, before the quiescent voltage level is established. However, this delay is avoided by using a bus driver that has sufficient drive to generate a large enough voltage step during the first transition to cross well beyond the receiver threshold region under the worst-case load conditions.

Figure 4 illustrates the driver output waveform under such a condition. Here the fully loaded bus (with $Z_L = 30\Omega$), of the previous example, is driven by the DS3662 bus transceiver at the mid point. The driver is actually driving two transmission lines of $Z_L = 30\Omega$ in either direction from the middle and hence the initial step is given by:

$$V1 = \left(\frac{Z_L}{2}\right) 2I_S \quad (10)$$

where I_S = Standing current on the bus due to each termination

For the DS3662, the termination can be designed for $2I_S$ = 100 mA and therefore:

V1 = (30/2)100 = 1.5V

This value of the initial swing is large enough to cross the narrow threshold region of the receiver as shown and therefore no waiting period is required for the reflections to build up the output high level. On the negative transition the problem is less critical due to the much higher sink capability of the DS3662 during pull down.

Reflections can also be caused by resistive loading of the bus by the DC input current of the receiver. The resulting reflectoin coefficient (Γ) is given by the expression:

$$\Gamma = -\tfrac{1}{2}\left(\frac{I_R}{I_S}\right) \quad (11)$$

where I_R = receiver input current

Having a receiver with a high input impedance not only makes this component of reflection insignificant but also reduces the DC load on the driver, allowing the use of lower value termination resistors. This is particularly true when a large number of modules are connected to the bus.

The design implications of the above discussion may be summarized as follows:

1. If the driver has adequate drive to produce the necessary voltage swing under the worst-case loading ($Z_L/2$), reflections do not restrict the bus performance. This translates to a 100 mA minimum drive requirement for a typical microstrip bus.

2. If the drive is insufficient, time should be allowed for the reflections to build up the voltage level before the data is sampled.

3. For signals such as clock, strobe, etc., wherein the edge is used for triggering events, it is mandatory that the driver meet the above drive requirements if delayed or multiple triggering is to be avoided.

4. An ideal TTL bus transceiver should have at least a 100 mA drive, a high input impedance receiver with a narrow threshold uncertainty region.

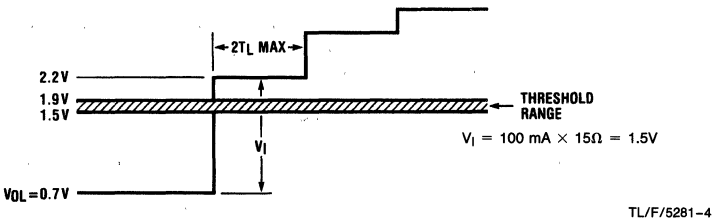


FIGURE 4. Worst-Case DS3662 Output Transition for $Z_L = 15\Omega$ and $R_T = 50\Omega$

THE DS3662 TRANSCEIVER

The DS3662 quad trapezoidal bus transceiver has been designed specifically to minimize the noise problems discussed previously. The driver generates precise trapezoidal waveforms that reduce crosstalk and the receiver uses a low pass filter to reject noise pulses having pulse widths up to the maximum driver output transition times. Precision output circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky transceivers.

Figure 5 shows the recommended configuration for microcomputer buses. The use of a 3.4V source with a single termination resistor at each end reduces the average power dissipation of the bus. However, a two resistor termination connected between the line and the power rails, having the same Thevenin's equivalent, can be substituted for lower cost.

Using a Miller integrator circuit, the driver generates a linearly rising and falling waveform with a constant slew rate of 0.2 V/ns *(Figure 6)*. This corresponds to a nominal transition time of 15 ns. *Figure 7* compares the output waveform of a typical high speed driver to that of DS3662 under different load conditions. It should be noted that even under heavy loading, the regular drivers have peak slew rates that are much higher than the average. On the other hand, the trapezoidal waveform has a much lower slew rate with only a slight increase in the transition time. Such an increase in the transition time has little or no effect on the data rates. In fact, the high fidelity of the DS3662 driver output waveform allows pulse widths as low as 20 ns to be transmitted on the bus.

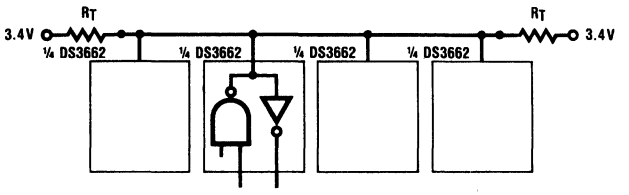


FIGURE 5. Recommended Bus Termination for Heavily Loaded Microstrip Backplanes

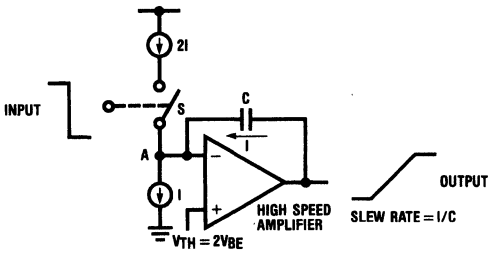
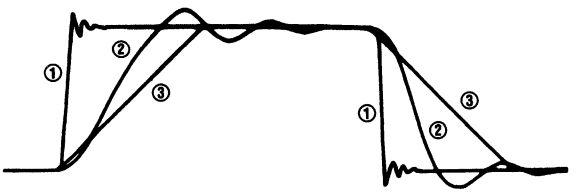


FIGURE 6. DS3662 Driver



Note 1: Typical high speed driver output unloaded; $t_r = t_f \approx 3$ ns

Note 2: Typical high speed driver output loaded; $t_r = t_f \approx 10$ ns

Note 3: Typical outupt of controlled slew rate driver which is load independent; $t_r = t_f \approx 15$ ns

FIGURE 7. Waveform Comparison

The receiver consists of a low pass filter followed by a high speed comparator, with a typical threshold of 1.7V *(Figure 8)*. The noise immunity of the receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the receiver. The receiver typically rejects a 20 ns pulse going positive from the ground level or going negative from the 3.4V logic 1 level. The receiver threshold lies within a specified 400 mV region over the supply and temperature range and is centered between the low and high levels of the bus for a symmetrical noise margin.

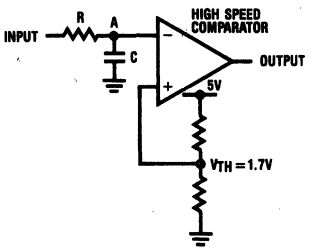


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FIGURE 8. DS3662 Receiver

Other features of the device include a 100 μA maximum DC bus loading specification under power ON or OFF condition and a glitch-free power up/down protection on the bus output.

Waveforms in *Figure 9* demonstrate the ability of the receiver to distinguish the trapezoidal signal from noise. Here the receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (16 ns) of the same peak amplitude (the signal is triangular because of the pulse width which is smaller than the transition time).

The real-world performance of the DS3662 transceiver shows an order of magnitude improvement in noise immunity over conventional transceivers under actual operating conditions (Reference #3). The controlled rise and fall times on the driver output significantly reduces both near end and the far end crosstalk. As expected, the pulse discrimination at the receiver input virtually eliminates the far end crosstalk, even on extremely long buses (over 100 feet). The near end crosstalk, which is particularly severe on the state of the art backplanes due to the tight spacing between the signal lines, is easily accommodated by the large percentage noise margin (>75%) provided by the receiver.

Field reports indicate that the DS3662 not only solves those mysterious intermittent failure problems in mini and microcomputer systems, but also helps them meet the new FCC emission requirements due to the reduced RF radiation from the bus.

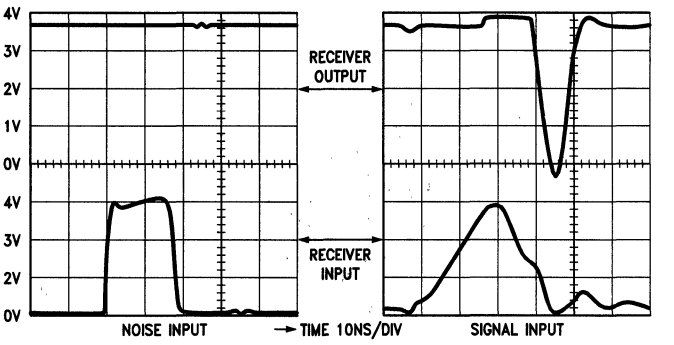

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FIGURE 9. DS3662 Receiver Response

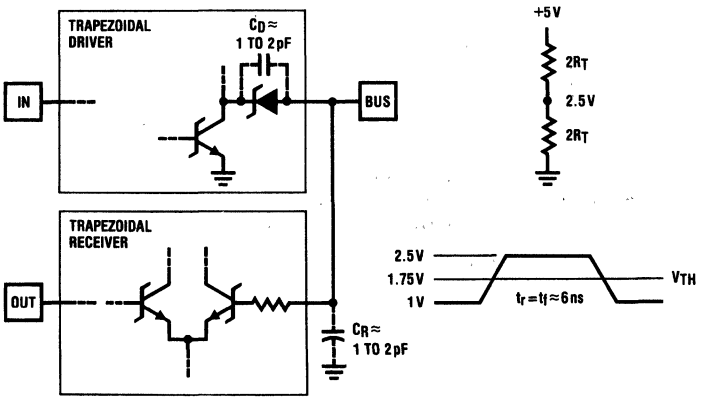

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FIGURE 10. High Speed Bus Transceiver with Low Output Loading for MicroComputer Backplanes

WHAT NEXT?

Since crosstalk scales with the signal amplitude, reducing the signal swing has not effect on the noise immunity as long as the percentage noise margin remains the same. On the other hand, there are several advantages in having lower signal swing. It reduces the drive current requirement of the driver thus reducing its output capacitance. Lower capacitive loading on the bus decreases its impedance reducing the drvie requirement even further. Having a lower current drive not only reduces the power dissipated at the terminations but also allows better matching of the termination due to the increased line impedance. In the ideal limiting case the driver has negligible loading effect on the bus and thus allows perfect termination under all load conditions.

In practice however, there are some obvious limitations. The receiver thresholds have to be maintained within tighter limits at lower signal swings to maintain the same percentage noise margin. Also, the capacitive loading is difficult to reduce beyond a certain point, due to the diminishing return in the way of lower current rating, as the loaded bus impedance approaches the unloaded impedance. However, the capacitance of an open collector driver output can be reduced significantly by using a Schottky diode as shown in *Figure 10.* The diode isolates the driver capacitance when the output is disabled. Using reduced signal swings and precise receiver thresholds, such a transceiver can provide significant improvements in microcomputer bus performance. The transceiver design presented in *Figure 10* is being considered for incorporation into the Futurebus standard by the IEEE.

CONCLUSION

A well designed bus transceiver goes a long way in improving the noise immunity of a single-ended TTL bus. Further improvements in bus performance may come from the use of reduced voltage swings and better transceiver designs for lower bus loading and tighter receiver threshold limits. Although such approaches may not be TTL compatible, the improvement in performance gained may indeed justify a new standard for bus transceivers.

REFERENCES

1) Bill Fowler, *"Transmission Line Characteristics,"* National Semiconductor—Application Note 108, May 1974.

2) A. Feller, H. P. Kaupp, and J. J. Digiacomo, *"Crosstalk And Reflections In High Speed Digital Systems,"* proceedings—Fall Joint Computer Conference, pp. 511–525, 1965

3) R. V. Balakrishnan, *"Bus Optimizer,"* National Semiconductor—Application Note 259, April 1981

4) David Montgomery, *"Borrowing RF Techniques For Digital Design,"* Computer Design, pp. 207–217, May 1982

5) R. V. Balakrishnan, *"Eliminating Crosstalk Over Long Distance Busing,"* Computer Design, pp. 155–162, March 1982

Timing Analysis of Synchronous and Asynchronous Buses

National Semiconductor
Application Note 514
David Hawley and R.V. Balakrishnan

ABSTRACT

This paper presents detailed examples of bus timing calculations for both synchronous and asynchronous busses, showing that bus throughput can be maximized by taking into account the characteristics and limitations of the transceiver technology being used. Based on these examples, a performance analysis of the currently available high speed bus interface technologies is made in terms of their maximum attainable transfer rate on both types of backplane busses. The results show that the use of a faster transceiver, as judged by its data sheet, doesn't necessarily result in a faster bus.

INTRODUCTION

In order to derive the highest possible throughput from a backplane bus, a careful analysis and optimization of timing parameters is essential. The maximum speed attainable at the physical level of the bus is a function of the transceiver technology, the electrical length of the bus, and the type of protocol, synchronous or asynchronous, being used. A clear understanding of the bus timing constraints lets the designer take best advantage of a given technology, such as TTL, ECL, or BTL (Backplane Transceiver Logic). Contrary to intuitive thinking, a faster transceiver will not always result in a faster bus. It can be shown through examples that greater bus transfer rates can be obtained by using specially designed bus transceivers, such as the BTL Trapezoidal, that at first glance may appear to be slower than the equivalent AS or FAST devices. These devices, in addition to improving bus bandwidth, also reduce crosstalk, ground noise, and system power requirements.

BUS PROPAGATION DELAY AND SETTLING TIME

Traditionally, system designers have used standard TTL devices to drive the backplane bus. Unfortunately, although TTL appears to provide fast rise and fall times, it cannot cleanly drive the capacitance of a loaded backplane or the resistance required for proper termination. BTL technology is a result of work that was done within the IEEE 896.1 Futurebus committee specifically to solve the problems of driving a backplane with transmission-line characteristics. By using a smaller voltage swing, lower capacitance drivers, and receivers with precision thresholds, BTL transceivers overcome the "bus driving problem."

Simply stated, the problem is one of driving a low impedance transmission line *(Figures 1* and *2)*. The capacitive loading of a bus due to TTL transceivers reduces its impedance from an unloaded value of 60–100Ω to a fully loaded impedance of less than 20Ω. A properly matched termination resistance would therefore require a current of over 300 mA in order to cleanly drive a 3V nominal TTL swing! Since most TTL drivers cannot supply this current, they must depend on reflections to build up the bus voltage to a DC level. This results in a settling-time penalty of one or more bus round-trip propagation delays on every signal transition, or 35 ns on a typical 20″ TTL bus.

The low output capacitance of BTL transceivers allows the total capacitive loading of a card in a backplane to be kept under 10 pF. This doubles the impedance of a loaded bus to almost 30Ω. BTL also specifies a reduced signal swing of 1V, which allows a properly terminated bus to be driven cleanly at under 75 mA. Consequently, there are no reflections, and the settling time is zero. A BTL driver can be guaranteed to cross the threshold of every receiver on the backplane with the incident edge of a signal wavefront.

The propagation delay of a bus is also a strong function of the capacitive loading. In the TTL case, the capacitive loading increases the signal propagation delay by a factor of 3 to 5 over an unloaded bus. In a 20″ bus, BTL can reduce this delay from a value of 13 ns in the TTL case to less than 9 ns, increasing the potential bus bandwidth significantly.

SYNCHRONOUS BUS TIMING

For our first example, let's consider burst data transfers on a synchronous bus. In many backplane systems, burst transfers provide the highest performance, because the overhead associated with the address cycle can be spread out over a number of data cycles. Although other types of transactions may be more complex and require more time (clock cycles), it is likely that many systems will be optimized for burst transfers.

In this example, we are making some simplifying assumptions which ignore some of the penalties associated with a general-purpose synchronous bus. One of these is that the entire interface is synchronized to the bus clock. In general, each card in a backplane will be running off of its own internal high-speed clock. This results in resynchronization metastability problems at both the master and slave interfaces, as well as a clock latency penalty of typically 50% of the clock period. We are also ignoring the return of status from the slave on each data transfer, by assuming all status can be generated before the data is clocked. This would not be true, for example, if parity had to be verified before the next data transfer could take place.

Clock Skew

In this example, the system clock is being distributed to each board through a clock line on the backplane. Since the clock line is being driven from a single point, the loaded capacitance on it is considerably less than on most other lines, and the settling time is typically zero, even in a TTL-based backplane. Due to the finite propagation delay across the bus, however, the clock edge still arrives at each board at different times, creating a relative edge inaccuracy commonly referred to as clock skew.

The worst-case skew can be cut in half by locating the clock source centrally on the backplane, rather than at one end. Additional clock skew will be introduced by the propagation delay differences in the receiver and logic gates that process the clock signal between boards. For a typical 20″

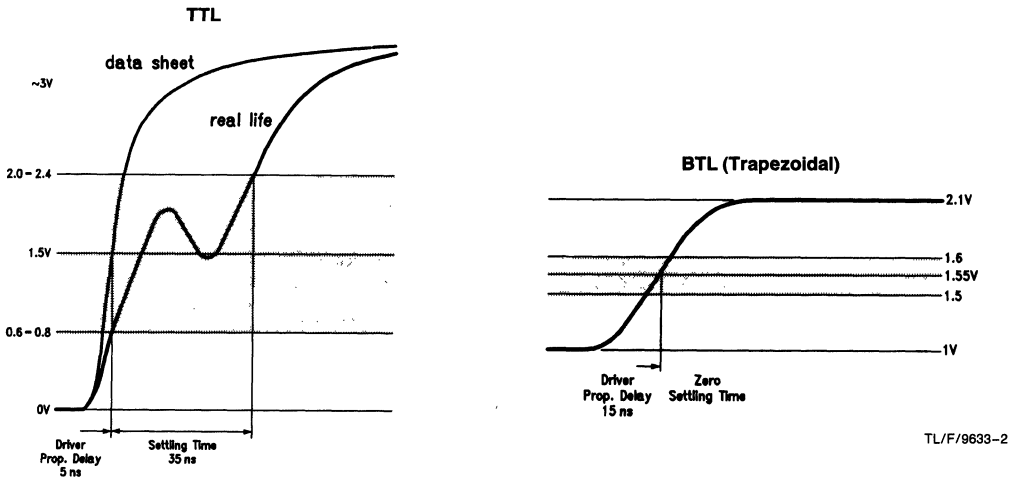


FIGURE 1. Settling Times

bus, with the clock driver located at the midpoint, total skew can easily exceed 10 ns; in our case, 5 ns for the bus, plus 7 ns for the receiver and a transparent latch used to implement bus wait states.

Synchronous Data Transfer Timing

In this example *(Figure 3),* the worst case data propagation delay from the master to the slave is simply the sum of the delays of the individual components of the data path. This path travels through the master's edge-triggered flip-flop and bus driver, across the length of the bus, and then through the slave's bus receiver and flip-flop, where the incoming data is latched. However, because this is a synchronous system, the data can be "pipelined" to some extent within the intervening logic. This means that the minimum clock cycle possible under this configuration is the sum of the logic skews, plus the maximum bus propagation delay, the set-up and hold times of the receiver, and the clock skew *(Figure 4).*

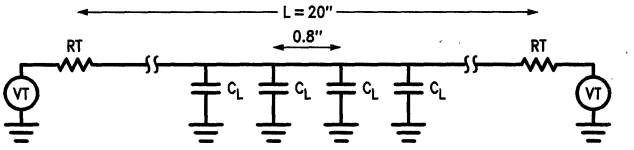
The advantage of a synchronous system is that the absolute timing requirements are set by the clock; the entire system can be optimized with this constraint in mind. This can become a disadvantage as technology advances beyond the point at which the synchronous bus was designed. A synchronous system must be continually redesigned for higher clock rates in order to take advantage of improvements in technology. Synchronous busses are therefore more suited to specific applications than to general-purpose, extended lifespan products.

Synchronous Timing Calculations

The first set of calculations assumes a TTL bus with AS transceivers and logic. As can be seen, the bus settling time overwhelms all the other skews and delays in the system. The upper limit of a discrete TTL synchronous bus implementation is roughly 15 MT (megatransfers/second). No particular advantage is gained by using FAST devices because, while the maximum propagation delays specified for that family are shorter than for AS, the maximum skews are generally greater. The effect of skew specifications is another subtlety of system performance analysis.

Two types of BTL transceivers are currently available, the BTL Trapezoidal and the BTL Turbo. The Trapezoidal transceivers have controlled rise and fall times on their drivers of 6 ns (nominal) to reduce crosstalk interference and switching noise within the backplane. In addition, the receivers incorporate crosstalk filters that practically eliminate far-end crosstalk problems on the bus. The Turbo transceivers eliminate these Trapezoidal features, but are much faster as a result. Switching noise problems are overcome by the use of individual ground return lines for each driver. Stripline backplane construction and careful layout techniques are required to minimize crosstalk.

Although the BTL Trapezoidal transceiver delays are much greater than those of the TTL devices, the absence of settling time results in a smaller overall clock cycle time. A maximum transfer rate of 18 MT becomes possible. When the Turbo devices are used, system throughput increases to 24 MT in this discrete implementation.



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C_L (TTL) ≈ 25 pF/0.8" = 375 pF/ft.
C_L (BTL) ≈ 10 pF/0.8" = 150 pF/ft.

$Z_O \approx 75\Omega$ Unloaded Bus Impedance
$C_O \approx 20$ pF/ft. Distributed Capacitance of Unloaded Bus
$T_O \approx 1.8$ ns/ft. Unloaded Bus Propagation Delay

$Z_L = Z_O/\sqrt{1 + (C_L/C_O)}$ Loaded Bus Impedance
$T_L = L \times T_O \times \sqrt{1 + (C_L/C_O)}$ Loaded Propagation Delay

T_L (TTL) ≈ 13.3 ns **TL (BTL) ≈ 8.75 ns**

FIGURE 2. Effects of Capacitive Loading

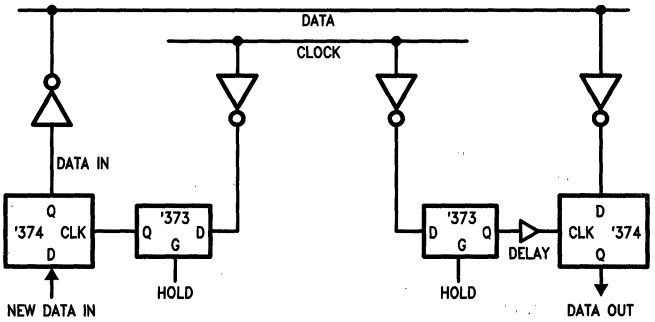

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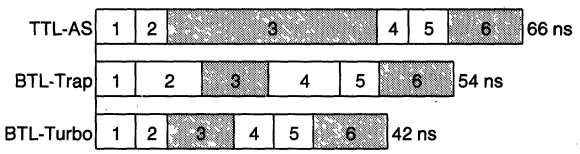
FIGURE 3. Synchronous Bus Logic for Burst Data Transfers



	TTL AS	BTL Trap	BTL Turbo
1) Max '374 Skew	5.0	5.0	5.0
2) Max Bus Driver Skew	4.5	10.0	5.0
3) Max Bus Delay	35.0	9.0	9.0
4) Max Bus Receiver Skew	4.5	13.0	6.0
5) Max '374 Setup and Hold	5.0	5.0	5.0
6) Max Clock Skew	12.0	12.0	12.0
TOTAL (ns)	66.0	54.0	42.0
MTransfers/second	18.5	18.5	23.8

FIGURE 4. Synchronous Burst Data Transfer Timing

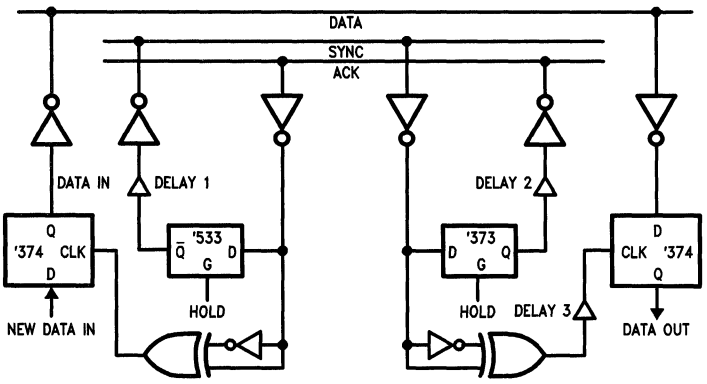


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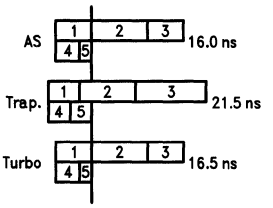
FIGURE 5. Asynchronous Bus Logic for Burst Data Transfers

DELAY 1	TTL AS	BTL Trap	BTL Turbo
1) Max XOR Delay	6.5	6.5	6.5
2) Max '374 Delay	9.0	9.0	9.0
3) Max Data Driver Delay	6.5	15.0	7.0
4) <Min '533 Delay>	−4.0	−4.0	−4.0
5) <Min Sync Driver Delay>	−2.0	−5.0	−2.0
TOTAL (ns)	16.0	21.5	16.5



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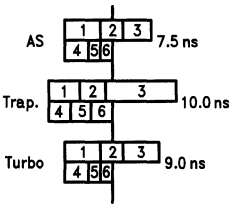
DELAY 2	TTL AS	BTL Trap	BTL Turbo
1) Max XOR Delay	6.5	6.5	6.5
2) Max '374 Hold Time	3.0	3.0	3.0
3) Delay 3	5.5	14.0	7.0
4) <Min '373 Delay>	−3.5	−3.5	−3.5
5) <Min Ack Driver Delay>	−2.0	−5.0	−2.0
5) <Min Data Receiver Delay>	−2.0	−5.0	−2.0
TOTAL (ns)	7.5	10.0	9.0



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DELAY 3	TTL AS	BTL Trap	BTL Turbo
1) Max Data Receiver Delay	6.5	18.0	8.0
2) Max '374 Setup Time	2.0	2.0	2.0
4) <Min Sync Receiver Delay>	−2.0	−5.0	−2.0
5) <Min XOR Delay>	−1.0	−1.0	−1.0
TOTAL (ns)	5.5	14.0	7.0

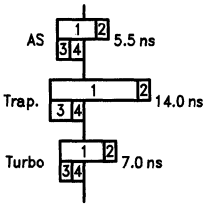

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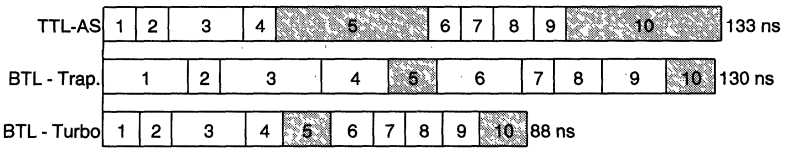
FIGURE 6. Asynchronous Bus Logic Delay Calculations



	TTL AS	BTL Trap	BTL Turbo
1) Max Ack Receiver Delay	6.5	18.0	8.0
2) Max '533 Delay	7.5	7.5	7.5
3) Delay 1	16.0	21.5	16.5
4) Max Sync Driver Delay	6.5	15.0	7.0
5) Max Bus Delay + Skew	35.0	10.0	10.0
6) Max Sync Receiver Delay	6.5	18.0	8.0
7) Max '373 Delay	6.0	6.0	6.0
8) Delay 2	7.5	10.0	9.0
9) Max Ack Driver Delay	6.5	15.0	7.0
10) Max Bus Delay	35.0	9.0	9.0
TOTAL (ns)	133.0	130.0	88.0
MTransfers/second	7.5	7.7	11.4

FIGURE 7. Asynchronous Burst Data Transfer Timing (Worst Case)

The largest cycle time delay in the final BTL Turbo example is clock skew. Bus skews can be reduced by distributing the clock to each board independently, using a dedicated trace on the backplane such that all lines are of equal length. This makes the clock propagation delay from the driver to each board the same, and thus practically eliminates the bus skew. In addition, better tolerances on driver, receiver, and logic propagation delays (smaller skews) will improve both the clock skew and the effect of transceiver delays on the cycle time.

ASYNCHRONOUS BUS TIMING

Our second example is also of a burst transfer, but this time using asynchronous bus timing. In this system, the master issues a strobe along with the data, and waits for an acknowledgement from the slave before removing the current data from the bus lines. All timing is controlled by the two participants in the data transfer. (Once again, we are assuming that new status does not have to be generated on each data transfer.)

The greatest advantage of an asynchronous bus protocol is its ability to adapt the speed of the bus to the speed of any two communicating boards. The most flexibility is achieved when no technology dependencies are introduced into the protocol. Unlike a synchronous system, where every board is designed with the same timing constraints in mind, a technology-independent module is designed with no assumptions about the timing of the rest of the system. Instead, each transmitting board simply guarantees that its data is valid on the bus at least zero nanoseconds before it issues its synchronization signal, and each receiving board is responsible for ensuring that its data has been successfully latched before issuing an acknowledge. The protocol itself imposes no artificial set-up or hold time limitations.

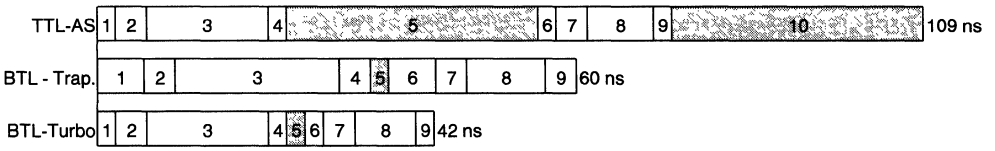
The result of this lack of timing constraints is that a board built today, using today's technology, is guaranteed to work in a system designed perhaps twenty years from now. That system will be forced to slow down whenever necessary to accommodate the greater internal delays and skews of the older module. However, if two future modules are communicating, they will transfer data at the maximum rate allowed by the future technology. The new IEEE Futurebus standard implements this type of protocol.

ASYNCHRONOUS DATA TRANSFER TIMING

The requirement that boards generate their own data synchronization and acknowledge signals, and the likelihood of zero set-up and hold times on the bus, make the timing of the asynchronous system more complicated than the previous example *(Figure 5).* Also, we are maximizing the performance of the sync/ack handshake by transferring data on each signal transition. This is known as a two-edge handshake.

On the master side, the board must guarantee that its data is valid on the bus before issuing the synchronization signal. This means that a delay must be inserted in the sync signal path (Delay 1) which includes the maximum propagation delays through the XOR clock generation circuit, edge-triggered flip-flop, and data bus driver. This is excessive, however, because the minimum delays through the sync latch and bus driver can be subtracted *(Figure 6).*

On the slave side, delays are required to guarantee that both the set-up and hold time specifications of the data latch are met. The set-up time delay (Delay 3) ensures that the sync signal, which may have minimum propagation delays through the sync bus receiver and XOR clock generator, arrives at the edge-triggered data flip-flop a set-up time after the data, which may have a maximum delay through



	TTL AS	BTL Trap	BTL Turbo
1) Min Ack Receiver Delay	2.0	5.0	2.0
2) Min '533 Delay	4.0	4.0	4.0
3) Delay 1	16.0	21.5	16.5
4) Min Sync Driver Delay	2.0	5.0	2.0
5) Min Bus Delay + Skew	35.0	1.0	1.0
6) Min Sync Receiver Delay	2.0	5.0	2.0
7) Min '373 Delay	3.5	3.5	3.5
8) Delay 2	7.5	10.0	9.0
9) Min Ack Driver Delay	2.0	5.0	2.0
10) Min Bus Delay	35.0	0.0	0.0
TOTAL (ns)	109.0	60.0	42.0
MTransfers/second	9.2	16.7	23.8

FIGURE 8. Asynchronous Burst Data Transfer Timing (Best Case)

the data bus receiver. The hold time delay (Delay 2) ensures that the data remains at the data flip-flop a hold time after the sync signal, which this time may have a maximum propagation delay through the XOR and the set-up time delay element just introduced. Since the removal of data is controlled by the ack signal, the hold time delay can be reduced by the minimum delays through the ack latch and bus driver, and the minimum propagation delay of the data bus receiver.

This is all very confusing at first, but these delay elements now in place in our circuit guarantee the receiver set-up and hold time requirements while maintaining the technology independence of the bus protocol. Now we can calculate the burst data transfer rate on this asynchronous bus.

The critical path is now the sync/ack handshake. The circuit delays are in place to make sure that data is transferred successfully. To calculate the transfer rate, simply add up all the propagation delays through the sync/ack loop *(Figures 7* and *8)*: on the master, the ack receiver, the sync latch, Delay 1, and the sync driver; a bus propagation delay; on the slave, the sync receiver, the ack latch, Delay 2, and the ack driver; and another bus propagation delay.

Should you use worst-case values throughout your evaluation? The beauty of a technology-independent asynchronous protocol is that is will adapt to the speed of the individual logic elements in the sync/ack handshake path. If all the devices happen to have worst-case characteristics, then yes. If they are all fast parts, however, then data transfer will take place under best-case conditions. Both calculations are included, providing the expected operating range of the circuit.

ASYNCHRONOUS TIMING CALCULATIONS

Once again, the TTL design is overwhelmed by the settling time of the bus. Since the sync/ack signal pair are acting as clocks in this system, glitches that may occur during the signal settling time are intolerable. This means that the 35 ns bus settling time must be hard-wired into the receiver logic, and cannot be reduced under best-case conditions. The performance of an asynchronous TTL backplane, from 7.5 to 9.2 MT, cannot approach that of a similar synchronous backplane.

The BTL Trapezoidal system has very similar performance to a TTL backplane under worst-case conditions. However, because there is no settling time penalty associated with BTL signals, the effect of improvements in device operation have a far more pronounced effect. In the best case, the performance is close to that of the equivalent synchronous system. Also, since the bus signal propagation delay is a function only of the distance between the two boards, modules placed in adjacent slots will experience almost no backplane delays.

A BTL Turbo board benefits from the same clean electrical environment that a Trapezoidal one does, except with a 40–50% overall improvement in performance. In the best case, the performance is the same as that of the equivalent synchronous system. Of course, as device parameters improve, with lower propagation delays and skews, the performance of the asynchronous system will continue to improve. The largest reductions in the transfer cycle time will come as interfaces for asynchronous busses such as Futurebus are integrated onto a single piece of silicon, where skews and delays can be more tightly controlled.

CONCLUSION

The use of transceivers designed specifically for the transmission-line environment typical in today's high-speed backplanes provides advantages in both the performance and electrical integrity of a system. The advantages of BTL only become obvious after a careful analysis of data transfer timing considerations. The Trapezoidal and Turbo options provide a designer with the opportunity to make the appropriate application-dependent cost/performance tradeoffs. A sometimes controversial issue is the appropriateness of a synchronous versus an asynchronous design. The former will usually provide an immediate performance advantage in a fully synchronized environment, but a carefully-designed general-purpose asynchronous protocol will often have a longer useful product life.

REFERENCES

1. R.V. Balakrishnan, "The Proposed IEEE 896 Futurebus—A Solution to the Bus Driving Problem," *IEEE Micro,* August 1984.
2. R.V. Balakrishnan, "Physical Layer Timing Design Considerations for High Speed Backplane Busses," Buscon/87 West, January 1987.
3. D.B. Gustavson and J. Theus, "Wire-OR Logic on Transmission Lines," IEEE Micro, June 1983, pp. 51–55.
4. *Interface Databook,* National Semiconductor Corp., Santa Clara, CA, 1986.
5. *ALS/AS Logic Databook,* National Semiconductor Corp., Santa Clara, CA, 1987.
6. *IEEE P896 D7.5a,* "Futurebus: A Bus Standard for Multiprocessing Architectures", IEEE, June 1987.

TABLE I. Device Parameters

Device	Parameter (Transition)	Minimum Prop. Delay	Maximum Prop. Delay	Maximum Skew	Setup/Hold
DM74AS374 Edge-Triggered Flip-Flop	LH HL	3.0 4.0	8.0 **9.0**	5.0 **5.0**	**2.0/3.0**
DM74AS373 Transparent Latch	LH HL	**3.5** **3.5**	**6.0** **6.0**	**2.5** **2.5**	2.0/3.0
DM74AS533 Inverting Transparent Latch	LH HL	**4.0** 4.0	**7.5** 7.0	**3.5** 3.0	2.0/3.0
DM74AS86 2-Input XOR	Other Input L Other Input H	2.0 **1.0**	**6.5** 6.0	4.5 5.0	
DM74AS240 Bus Driver/Receiver	LH HL	2.0 2.0	6.5 5.7	**4.5** 3.7	
DM74AS242 Bus Transceiver	LH HL	**2.0** 2.0	**6.5** 5.7	**4.5** 3.7	
DS3896 BTL Trapezoidal Transceiver	Rx Tx	**5.0** **5.0**	**18.0** **15.0**	**13.0** **10.0**	
DS3893 BTL Turbo Transceiver	Rx Tx	**2.0** **2.0**	**8.0** **7.0**	**6.0** **5.0**	

Note: Values in boldface are those used in the preceding calculations.

PI Bus

National Semiconductor
Application Note 725
Joe Wert

HISTORY

Throughout the 70's and early 80's the typical backplane was driven by standard TTL logic parts with tristateable outputs such as 54/74XX240 and 245. For design purposes these busses were modeled as lumped capacitances and transmission line effects were ignored because the bus data rates were generally not fast enough to require designers to be concerned with transmission line effects of the backplane. With the lower bus speeds there was sufficient bus settling time for reflections to dampen, and the signals to stabilize close enough to steady state to avoid problems. If a bus was heavily loaded and attempts were made to run the bus faster than 10 MHz, errors in data were frequently seen due to line reflections causing line voltage levels to transition through threshold more than once for a single transition of the buffer input. And as backplane densities increased, loading from the transceivers became so great that this increased the problem of driving the bus quickly and error free.

With today's higher bus data rates it has become imperative that the transmission line characteristics of the backplane be accounted for in backplane analysis. By doing so it becomes apparent that there may be better ways to drive backplanes than with traditional TTL family logic.

To solve some of the inherent problems with running densely loaded busses, the PI Bus structure was developed. PI Bus (parallel interface bus) was developed by IBM, Unisys and TRW for the VHSIC 2.2 Interoperability program. PI Bus has since been adopted by the Joint Integrated Avionics Working Group (JIAWG) section of SAE.

TRANSMISSION LINE PHYSICS

Several problems must be overcome to run a faster, more heavily loaded bus. When the bus propagation delay plus settling time decreases below about 100 ns the backplane must be considered as a transmission line. If the backplane is densely populated the problem of running it at high data rates is exacerbated.

Z_0 is the characteristic impedance of the backplane, and is calculated from the physical characteristics of the backplane. From *Figure 1*, a simple model of a transmission line, the following equation may be written:

$$Z_0 = [\,(R + jwl) / (G + jwc)\,]^{1/2}$$

For high frequency, the R and G terms become insignificant due to the increases in the w terms,

$$w = 2\pi f \text{ where f is frequency}$$

and the equation simplifies to

$$Z_0 = (L/C)^{1/2}$$

where L is in units of inductance per unit length and C is in units of capacitance per unit length

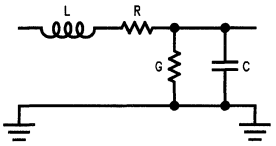


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FIGURE 1

EFFECTS OF CAPACITIVE LOADING ON BUS

Values for Z_0 can be calculated from the physics of the backplane construction. For a typical PI Bus epoxy-glass backplane the value for Z_0 is about 65Ω. The basic equation describing the impedance of a loaded bus is

$$Z_1 = Z_0 / (1 + C_1/C)^{1/2}$$

where C_1 is the additional load added to the bus by modules, connectors and connector mounting vias. So as the capacitive load of the modules increases, the impedance of the bus decreases. As the impedance of the bus decreases, the current required to drive the bus between state changes in a given time period increases (I = V/Z). The equation for the propagation delay of a signal on an unloaded transmission line is

$$T_{P0} = \ell\,(L/C)^{1/2}$$

where ℓ = length of the bus.

For a loaded bus,

$$T_{P1} = T_{P0}(1 + C_1/C)^{1/2}$$

describes the propagation delay on a transmission line. From the equation for the loaded bus, it is obvious that as the capacitive loading of the bus increases, the propagation delay for a given length of bus increases. As this time increases bus settling time increases, and hence affects how fast the bus may be operated. So a bus transceiver which had low capacitive loading would improve bus operation in several ways. A low capacitive transceiver would raise the value of Z_1, and hence the drive current requirements for a given performance would be reduced, the propagation delay for a given length of backplane would be reduced, and any bus settling time required would also be reduced.

OUTPUT V_{OH} SWING

The standard TTL swing for an output is from 0.2V to V_{CC} − two diodes (for CMOS 0V to V_{SS}). For a bipolar device, this swing could be as much as from 0.2V to 4.1V. The smaller this swing between high and low, the less charge which must be moved in any given time to effect a change of state. So from the standpoint of power usage, smaller in this case would be better.

PI Bus developed as a bus to address both these conclusions in a manner similar to Future Bus. The bus side outputs are open Schottkys, and the bus is terminated on both ends by a resistor to a voltage source with limits of 1.9V to 2.1V *(Figure 2)*. The resistors used to terminate the bus may be from 30Ω to 40Ω. By terminating the bus in this way, (Z_0 matches 40Ω termination with no loads on the bus, but including loading from raw backplane plus vias and mating connectors, and a 30Ω termination matches a fully loaded PI bus backplane) the bus is somewhat tuned to the Z_1 of the bus so that reflections can be minimized. By terminating the bus to a maximum of 2.1V, the maximum voltage swing on the bus will be from the V_{OL} minimum spec of 0.4V to the maximum 2.1V. Thus the voltage swing for the PI Bus transceiver would be 1.7V versus the 3.9V for a standard bipolar transceiver.

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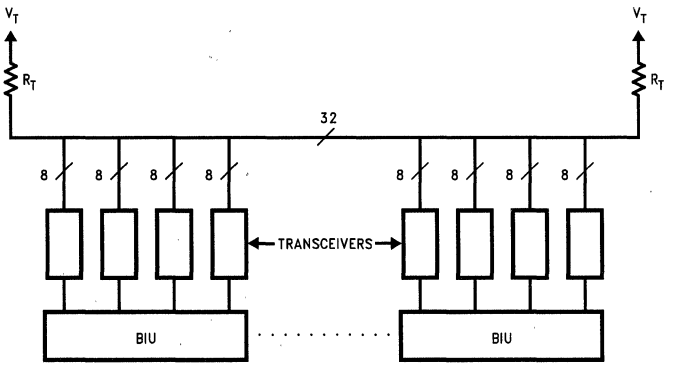

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FIGURE 2

OUTPUT CAPACITANCE OF TRANSCEIVER

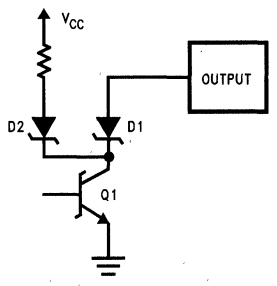
In order to decrease the capacitive loading of each transceiver, Schottky diode outputs are used, and are reverse biased when not active low. The PI Bus driver output is shown in *Figure 3a*. When the output is in a high state both the output Schottky diode and the collector-substrate diode of Q1 are reverse biased. By reverse biasing both the Schottky diode junction and the collector-substrate junction the parasitic capacitive loading of the bus driving output can be greatly decreased. The following equation gives an approximation of the impact reverse biasing has upon junction capacitance:

$$C_j = C_{j0}/(1 + V_d/V_0)^{1/2}$$

where C_{J0} equals the capacitance of the diode junction under unbiased conditions, and V_d equals the reverse biased voltage of the diode junction. V_0 is the built-in zero bias potential across a diode junction, and would be on the order of 0.7V. So, by reverse biasing the cathode of both D1 and Q1, their parasitic capacitive loading on the bus is decreased. If the bus were at 2.0V, and V_{CC} was at 5V, C_{J0} would be decreased by a factor of 2.1. Then of course, C1 and C2 are in series, so their total capacitance would be decreased according to the following equation:

$$C_T = C_P + [(C_1)(C_2 + C_3)] \div (C_1 + C_2 + C_3)$$

The capacitance of C3 (from D3) is basically negligible in comparison to C1 because it is approximately 0.5% the area Q1. The package capacitance (C_P) may vary from 0.3 pF to 1.5 pF, depending upon the package and the pin location on the package. The other capacitive loading on each bus pin would be the base-collector and base-emitter



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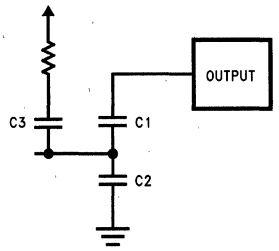
a. Simplified Circuit



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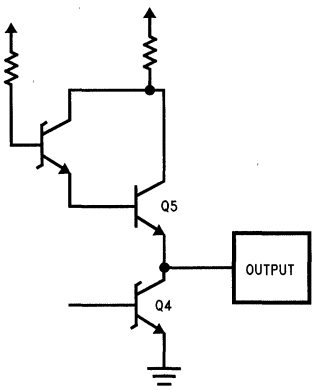
b. Parasitic Capacitance
FIGURE 3



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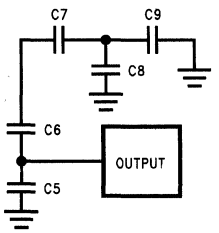
a.



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b.
FIGURE 4

capacitance of Q7 *(Figure 5b),* which connects to the anode of D1. For a typical TTL part *(Figure 4),* the capacitive loading of the output would be primarily C5 because C6 is in series with C7 and the parallel combination of C8 and C9. For Q4 and Q5 being about the same size devices, the capacitive loading of the TTL circuit would be several times larger than that of the Schottky terminated circuit.

PRECISION THRESHOLD

In order to handle the smaller output swing on the bus, it is necessary to use a more precise threshold circuit on the bus receiver input. *Figure 5a* is a typical TTL input buffer. The threshold set by this type of circuit varies considerably with temperature, and typically ranges from about 1V at high temperatures to about 1.8V at low temperatures. Such movement could not be tolerated with a bus swing which could be as small as from 1.15V to 1.9V. The circuit shown in *Figure 5b* is used on PI Bus transceivers to set a more precise threshold. A voltage reference with a very small V_{CC} and temperature dependence is placed on the chip to establish a precision threshold for the PI Bus to BIU input buffer. By using a differential pair with one of the pair controlled by the reference voltage, the threshold can be maintained within a 150 mV window centered at 1.52V.

OUTPUT RAMPS AND NOISE IMMUNITY

Ramped outputs have been touted as the solution to problems of bus reflections and crosstalk. The amount of ramp time put into rise and fall times directly related to the propagation delays of a transceiver, so longer ramps require longer delay times. An important question to ask is how much of a ramp buys what degree of decreased bus settling time. Many TTL parts have peak ramps of about 2V/ns. This rate of ramp certainly seems to increase bus settling times. The PI Bus transceiver will have a typical ramp rate of about 0.5V/ns.

Having some amount of noise rejection on the bus receiver input allows the bus buffer input to ignore small excursions above or below threshold without affecting the data being transmitted to the BIU. However the greater the amount of noise immunity, the greater the propagation delay on the path from the bus to the BIU. The PI Bus transceiver offers a compromise between noise immunity and prop delays with typically 4 ns of pulsewidth protection measured at 1.5V for a 1 to 2 volt input.

SUBMICRON BIU PROTECTION

To accommodate future submicron BIU processing, the PI Bus transceivers offer a feature for limiting the output V_{OH} excursion to the BIU. The V_X pin on the chip can be used as a clamp voltage to limit the V_{OH} of the BIU side output. The basic propagation delays on the transceiver with the exception of the BIU side low to high ramp rate are unaffected because the remainder of the transceiver is still powered by the normal V_{CC} pin. Only the BIU V_{OH} is controlled by the V_X pin. The *Figure 6* schematic shows how the V_X voltage sets the output V_{OH}.

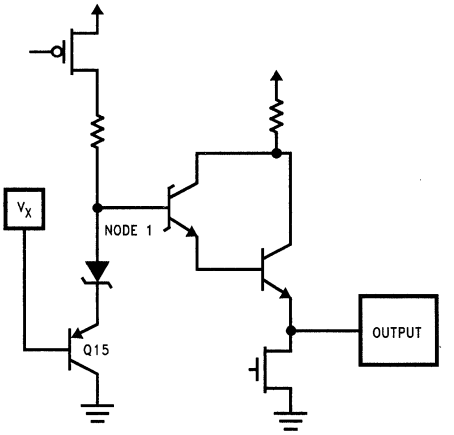

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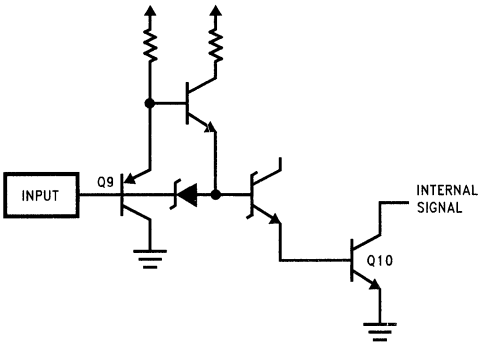
FIGURE 6



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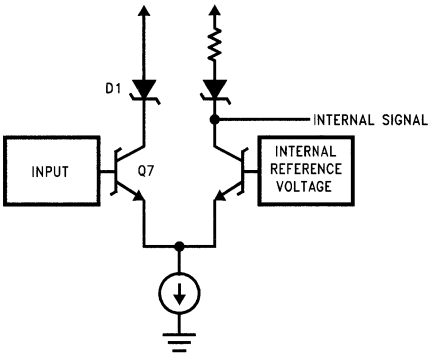
a. Typical TTL Input



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b. PI Bus Receiver Input

FIGURE 5

LOW POWER

Many applications of PI Bus are designed with a redundant bus, and as such always have a full set of transceivers in the inactive mode. And in addition, on the active bus there may be 15 inactive (for a 16 drop bus) transceivers with one active transceiver. So in order to lower the power requirements for the PI Bus backplane application the National PI Bus transceiver, the DS1776, was designed using BiCMOS in order to take advantage of the power savings possible with the use of CMOS in appropriate portions of the circuit.

A pure bipolar transceiver would have an I_{CC} inactive specification of about 100 mA. By using a BiCMOS process it was possible to design a PI Bus transceiver with an I_{CC} inactive of 35 mA.

BIPOLAR vs CMOS vs BiCMOS TECHNOLOGY

A full bipolar transceiver could be built to provide excellent performance in most areas with the exception of power consumption in both the active and inactive modes. A pure CMOS part could be designed with a much lower I_{CC}, but it would have the following drawbacks. It would be slower than a bipolar part, no Schottky diode would be available to construct a low capacitance output with limited swing, and stable CMOS voltage references which have a reasonable silicon area are non-existent, so setting a precise input voltage threshold would be difficult.

By making judicious use of bipolar and CMOS circuits where each is appropriate, it was possible to design a PI Bus transceiver with an I_{CC} inactive of typically 35 mA and yet maintain the full features which make PI Bus a clean and quiet bus to run.

REFERENCES

Chapman, Robert A. *Transmission Lines.* New York: McGraw-Hill, 1968.

Muller, Richard S., Theodore I. Kamins. *Device Electronics for Integrated Circuits.* New York: John Wiley and Sons, 1977.

Neff, Herbert P. *Basic Electromagnetic Fields.* New York: Harper and Row, 1981.

JIAWG PI-Bus Specification—J89-N1A Draft

Balakrishnan, R.V. "Eliminating Crosstalk Over Long-Distance Busing." *Computer Design,* March 1982, pp. 155–162.

Balakrishnan, R.V. "DS3662—The Bus Optimizer." National Semiconductor—Application Note 337 *Interface Databook* 1988.

"P1194.0/d2—A Guide to Backplane Electrical Performance Measurements." June 1989—Prepared by BTL Working Group from I.E.E.E.

Signals in the Futurebus+ Backplane

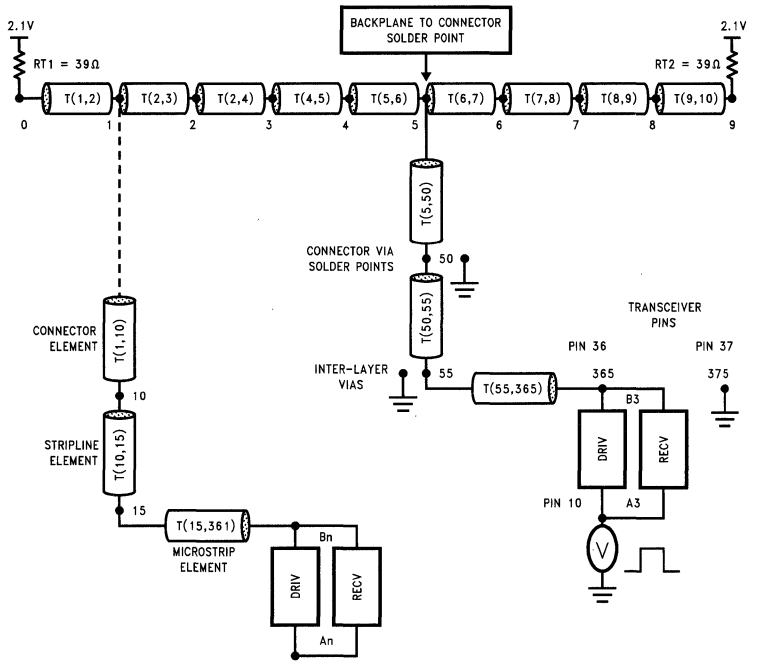
National Semiconductor
Application Note 738
Stephen Kempainen

The Futurebus+ backplane is a complex electrical environment that consists of many circuit elements. The modeling of such an environment can become time consuming and expensive. The Futurebus+ Electrical Task Group Expert Team has detailed the circuit elements in their SPICE simulation. An average Futurebus+ simulation contains over 10,880 individual elements and gobbles 8 CPU hours on a single user VAX 8650. This note is an attempt to simplify the circuit model and gain an intuitive understanding of interactive signal path elements. The elements are investigated by probing at individual impedance breaks that are considered significant. Waveforms of the signal will be correlated with the TDR signals from the same signal paths. An investigation of ground signal variations and crosstalk measurements is included because of relevance to signal measuring in this environment. The relation between the crosstalk, ground bounce and the signal path impedance will be pursued to see their combined effect on the noise margin.

The interconnect effects on the electrical signal become critical in high speed multilayer board design such as Futurebus+. PCB traces must be treated as transmission lines due to the rapid transition times of the signal. Analyzing PCB traces uncovers the impedance mismatches caused by seemingly harmless corner geometries, parasitic and crossover effects, and inter-layer vias. The impedance mismatches also affect crosstalk coupling and signal reflections which are a major concern due to the large chunk of noise margin they may consume. To demonstrate how these circuit elements affect the signal, this article will follow a signal from the transceiver as it propagates into the backplane.

FUTUREBUS+ BACKPLANE AND BOARD MODEL

Figure 1 models the signal path from a transceiver in one board, through the backplane, to a transceiver in another board. Both of the boards are mounted in a ten slot backplane. The dashed line to one module indicates it can be removed or moved around to different locations for this analysis. It is the receiver and it is seen as a load by the driver module. To first emphasize the driver module stub effects alone, the receiver is not inserted into the backplane. This focuses the driver response to only the transmission line elements. This model can be generalized to any backplane. However, it is derived from specific equipment used to obtain these waveforms. The backplane is provided by Bicc-Vero Electronics, No. 819-304105E. It uses 39Ω,



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Model of the Futurebus+ backplane with two daughter boards; one in slot 1, and one in slot 5 with an input signal at pin 10.

FIGURE 1

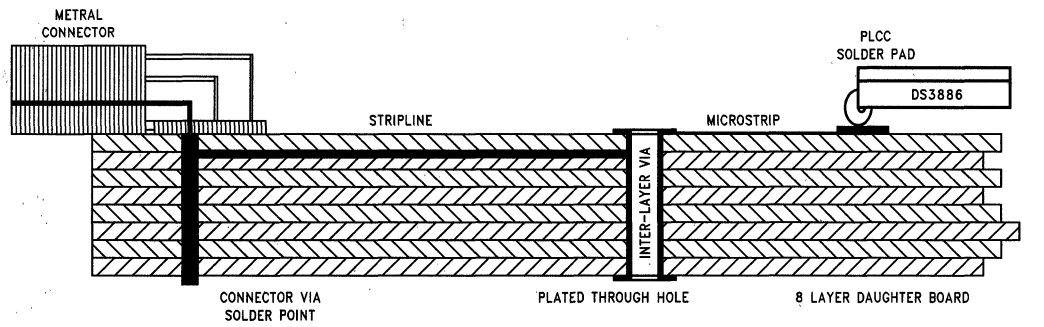

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FIGURE 2. Eight Layer Daughter Board, Side View

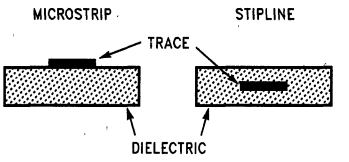

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FIGURE 2a. PCB Track Cross Section

surface mount, termination resistors and has a 1 inch spacing between the slots (soft metric). The board is provided by Hybricon. It is a Futurebus+ Wire-Wrappable Board 6U x 280mm. The part number is 031-126-10. The board is laid out (eight layers) for the National Semiconductor Futurebus+ Chip Set transceivers and can accommodate 64 data bits.

Figure 2 is a cross section of the Hybricon board showing the signal path of the DS3886 Latched Data Transceiver, pin-36. The illustration emphasizes the physical impedance differences of the transmission path elements. Examination of the Time Domain Reflection response of the signal path is a good way to "electrically see" these differences.

TIME DOMAIN REFLECTION

TDR uses a step generator to apply a positive going impulse to the signal path being investigated. The step has a very fast rise time of 35 ps and a 200 mV amplitude. The step travels down the path at the propagation velocity of the line. If there are impedance mismatches in the signal path, part of the incident wave will be reflected. The reflected wave is then algebraically added to the incident wave at the point where the mismatch occurs. The total voltage wave appears on the oscilloscope as a road map to the impedance breaks encountered by the propagating step.

A quick review of reflection coefficient (ρ) fundamentals will be helpful to intuitively understand the effects of signal path impedance breaks. Then, investigating three load impedance conditions will suffice. For all cases, the TDR generates the step from a 50Ω source and it is carried by a cable with characteristic impedance, $Z_O = 50\Omega$, to the device under test, DUT. First case is if the DUT were a 50Ω load, then ρ would be 0 and the wave on the scope would appear as a straight line after the step, no reflected wave added to the incident.

$$\rho = (Z_L - Z_O)/(Z_L + Z_O) = 0 \text{ for } Z_L = Z_O$$

Z_O = cable characteristic impedance

Z_L = load impedance

The equation for adding the reflected wave, Er, to the incident wave, Ei, is as follows.

$$E = Ei + Er, \text{ where } Er = Ei(\rho)$$

The second case is infinite load impedance as in *Figure 3a.* ρ is equal to +1 in this case and the reflected wave equals the incident wave. The total wave is then double the incident, *Figure 3b.* Now consider when the incident wave hits an inductive impedance. The current can't change instantaneously so the load momentarily appears as an open due to the increased impedance. The $\rho = +1$ at $t = 0$ in *Figure 3c.* Reflected voltage is ideally the same as the incident voltage for that moment. As the inductor current builds exponentially, the impedance drops toward zero, *Figure 3c.* The voltage a long time after $t = 0$ is determined by resistance in series with the inductor. As t goes to infinity, the reflection coefficient is $\rho = (R - Z_O)/(R + Z_O)$, where R = series resistance of the inductive load.

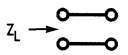

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FIGURE 3a

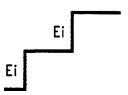

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FIGURE 3b

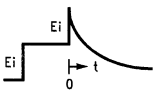

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FIGURE 3c

The third case is zero load impedance as in *Figure 4a.* $\rho = -1$ and the reflected wave is subtracted from the incident wave leaving no voltage. Expanding on this idea, when the incident wave hits a capacitive impedance, the capacitor won't accept a sudden voltage change. No change in voltage appears as a short circuit instantaneously and $\rho = -1$ at $t = 0$. The capacitor voltage builds exponentially and the impedance rises to a level determined by the shunt resistive component of the load, *Figure 4c.* The final value of ρ is again $(R - Z_O)/(R + Z_O)$, only R = shunt resistance of the capacitive load.

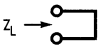

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FIGURE 4a

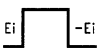

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FIGURE 4b

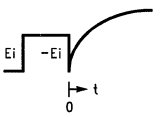

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FIGURE 4c

TDR AND IMPULSE ENERGY

Another way to look at TDR results is by considering the energy contained in the step impulse. This energy is transmitted over a non ideal medium so there are losses, but for short distances it is not unrealistic to consider the energy of the pulse to be constant. Now consider the capacitive impedance break; increasing capacitance reduces the characteristic impedance.

$$V/I = Z_O = \sqrt{(L_O/C_O)} \text{ where:}$$

L_O = inductance per unit length

C_O = capacitance per unit length

Since the energy of the pulse remains constant and the voltage and the impedance drop, the current must increase proportionally to the lowered voltage. This increased current charges the capacitor at a time constant that is determined by Z_O in parallel with the shunt R to the capacitor. As the capacitor stores the energy, the current drops off and the capacitor appears as an open circuit after a long steady state condition.

TDR SYSTEM ERRORS

The extremely fast rise time of the step impulse is important to TDR analysis. Since the leading edge of the incident step is made up almost entirely of high frequency components, it accentuates the small reactive impedance mismatches of a signal path. As the step travels down a non-ideal transmission line, the higher frequencies are attenuated by skin effect losses and dielectric losses. This distorts the step, and is called cable loss. The degraded rise time limits the accuracy of reflection measurements through a multiple discontinuity signal path. TDR measures each succeeding discontinuity with less accuracy, because the transmitted step degrades and multiple reflections occur. The stub of a daughter board qualifies as a multiple discontinuity path, so the resulting waveforms must be analyzed as such.

TDR AND FUTUREBUS+ SIGNAL STUBS

With this in mind, an analysis of the TDR waveforms of the signal path can be performed. *Figures 5a* and *5b* show the artwork for two signal path traces. The actual path length is 64mm. *Figure 5a* is the path used for all the waveforms gathered in this analysis and *Figure 5b* is a path for comparison of the TDR responses. The apparent similarity of the artwork does not show the electrical differences of the paths while the TDR waveforms do. *Figures 6* and *7* include the waveforms from these two signal paths that are similar but different enough to demonstrate some characteristics. The signal path from pin 36 of the DS3886 goes through connector B-b-16 as designated by the Futurebus+ standard, *Figure 5c.* This path is included in both figures. Also in both figures is the reflection from just the SMA connector that is used to launch the step impulse into the signal path. It is terminated with a 50Ω load. The inductance of the SMA leads can be seen by the sharp increase in impedance. The return to the 50Ω level is then illustrating the first case in the TDR review for the $\rho = 0$ situation.

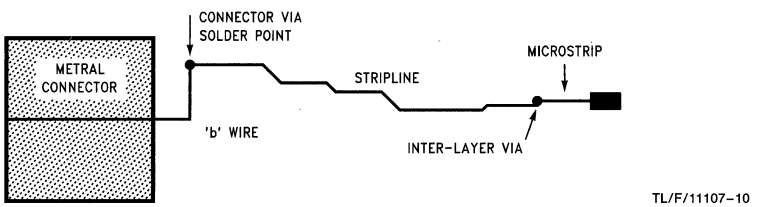

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FIGURE 5a. Signal Path B-b-16

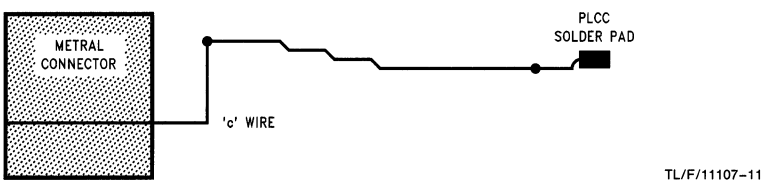

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FIGURE 5b. Signal Path B-c-16

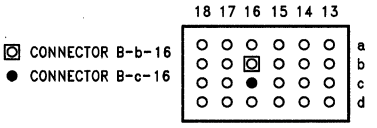

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FIGURE 5c. Signal Connector Block B, Rows 13 to 18

Figure 6 shows the effect of launching the TDR step into the solder pad. The first inductive bump is the error introduced by the SMA launching mechanism. The inductance of the microstrip follows the dip in impedance (capacitive solder pad). The path impedance is raised to 75Ω by both signal paths, *Figure 7.* Notice how the longer microstrip in *Figure 5a* adds distance to the inductive bump compared to the waveform from the shorter microstrip in *Figure 5b.* Then notice that the inter-layer via causes a capacitive drop in impedance. The stripline impedance settles in at about 60Ω for both of the paths. The next dip is the capacitance of the connector via solder point followed by the inductive increase of the connector wires. Notice that the longer "c" wire increases the impedance more than the "b" wire. Finally, the step hits the open end of the connector and the signal voltage doubles which indicates the $\rho = 1$ situation.

Figure 6a is included to show how the degradation of the incident wave through the multiple impedance mismatches of the signal path affects impedance level measurement. The TDR impulse is launched into the connector end of the path rather than the solder pad end. The difference is best seen in how the impedance of the connector is much greater when the high frequency components of the incident wave have not been attenuated by the previous impedance mismatches. The connector launch displays an impedance of 90Ω rather than the small increase that is shown in the end of the launch from the solder pad. *Figure 6a* also shows the capacitance of the transceiver mounted on the solder pad that is charging to the open state at the time constant rate.

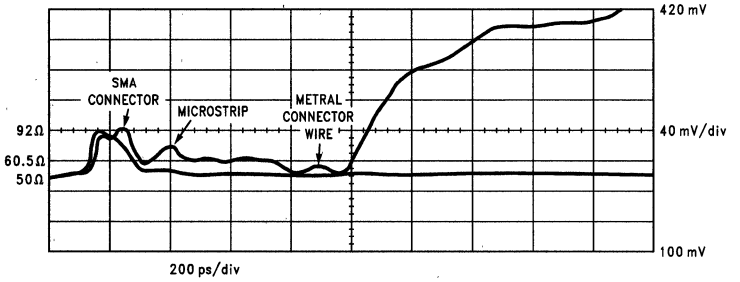

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FIGURE 6. Two TDR Waveforms, 50Ω Termination and Path B-b-16

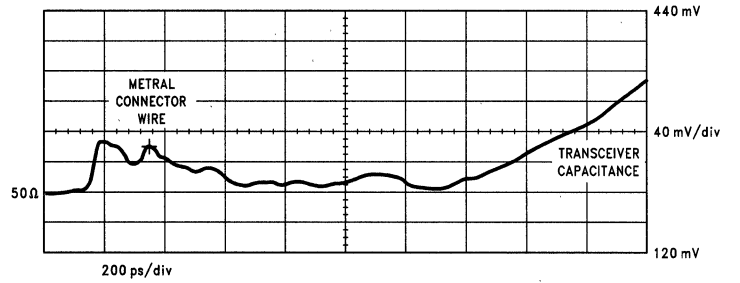

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FIGURE 6a. TDR Launch into Connector B-b-16 with DS3886 Mounted On Board

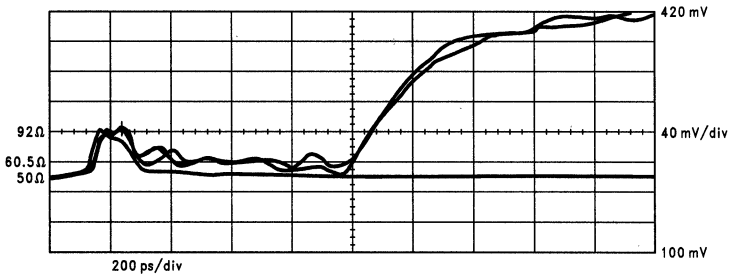

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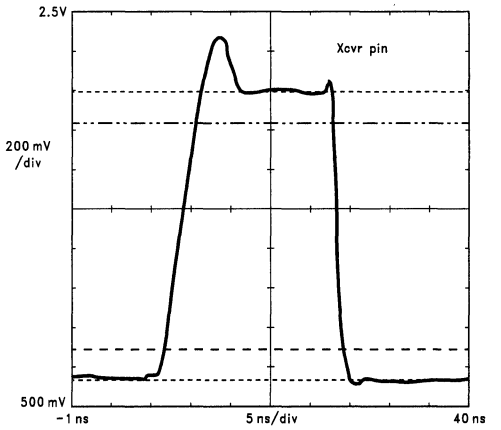
FIGURE 7. Three TDR Waveforms

THE TRANSCEIVER IN THE UNLOADED BACKPLANE

The transmitting transceiver is mounted in slot 5, *Figure 1.* Pin 36 is named B3 in both the DS3883, 9 Bit Data Transceiver, and the DS3886, the Latched Data Transceiver which is used in this application. Pin 37 is the B3 GND pin, the BTL ground for B3 (see section on BTL, QGND, and logic GND). The signal waveform in *Figure 8* is obtained by probing the circuit with a low inductance ground tip at these two pins. The signal displays a rapid fall time, large overshoot and minimal undershoot. This signal is different than that obtained from bench testing with minimal jig inductance and capacitance, *Figure 8a.* That waveform shows slower fall time and no overshoot. There are a couple of reasons for these backplane circuit responses. The first being the microstrip circuit element, T(55,365). Physically, this element is a very narrow microstrip between the solder pad and the inter-layer via. The relatively high inductance of this microstrip, shown in *Figure 6a,* inhibits the sudden change in current presented by rapid transition times. This initially appears as a large impedance mismatch which makes the reflection coefficient (ρ) approach +1 instantaneously. The effect of ρ is to speed the slew rate on the fall time and extend the overshoot on the rising edge. The different response of the two edges is due to the active pull down and the passive pull up.



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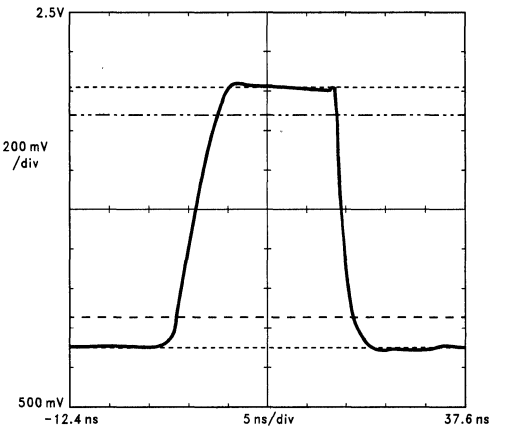
Rise 3.881 ns	Fall 1.346 ns	Max 2.37800 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 616.000 mV	Over Shoot 19.4787 %	Under Shoot 1.37174 %	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST06	Pan/ Zoom on

FIGURE 8



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Rise 5.410 ns	Fall 2.348 ns	Min 780.000 mV	Measure-ment	Distal 90% Proximal 10%
Max 2.13600 V	Over Shoot 1.52207 %	Under Shoot 1.67428 %	Statistics Comp & Def Continuous	Remove Wfm 1 ST05

FIGURE 8a. Bench Test Jig Waveform

The second reason is the path inductance and line delay of the backplane, daughter board, and the termination scheme. The transmitter pull down transistor is turned on with a very large base current needed to supply 80 mA collector current. This collector current is supplied by the termination resistor which is located at some electrical distance (backplane and daughter board paths) from the transistor. As the transistor experiences a hard turn on, it initially sees what appears to be an open circuit. The momentary open circuit causes the overshoot and fast falling edge. This is due to the inductance and delay of the signal path preventing the current from changing immediately at the collector of the transistor. This inductance limits the driver slew rate control at the transceiver pin. Bench testing of the same part shows a fall time 1 ns longer than the daughter board fall time. The difference in fall times under test conditions are due to load proximity and availability of almost instantaneous current on the test jig. The rise time is much slower because it is a passive pull up and is controlled by the exponentially decaying current due to the inductance.

Another look at the waveform will show that there is an increase in voltage just prior to the high to low transition. This is also due to the large, fast voltage change at the base to the output transistor. The voltage step is coupled through from the base to the collector by the Miller capacitance. This small spike only shows up in the backplane environment for the same reasons as already explained.

IMPEDANCE MISMATCHES

The next probe is at the inter-layer via points of the signal line and ground line. Labeled point 55 in *Figure 1.* These vias present a relatively large capacitive impedance to the signal. The capacitance of the plated through hole (PTH) via has been estimated as high as 1.1 pF by Hybricon down to 0.75 pF by the Futurebus+ Expert Team. This is also the point at which the microstrip trace changes to a stripline trace. The capacitance of a PCB track varies directly with track length and width, but inversely with the dielectric thickness. Typically, this corresponds to about a 50% increase in capacitance from outer to inner layer for an eight layer board. As seen by the TDR investigation, the path impedance drops from 75Ω to 60Ω at this point, *Figure 6.* Thus, the stripline circuit element, T(50,55), can be characterized by an increase in the capacitance per unit length.

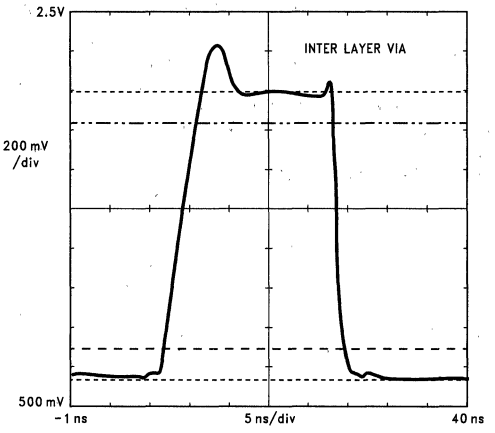
Figure 9 illustrates the damping of the overshoot and undershoot that is caused by the capacitive reactance. The fall time is increased by the capacitance. This can be intuitively understood by considering the capacitive impedance break of *Figure 4c.* This has a counter balance affect on the path inductance so the needed current is available. Initially, the load appears as a short circuit because the capacitance will not accept an immediate change in the voltage. The ρ at the impedance mismatch then initially approaches −1. The quick charging of the capacitance pulls the slew rate out of a nose dive and limits the undershoot. The rise time shows a slight increase, but the resolution of the scope comes into play for times less than 150 pico seconds.

The third major impedance mismatch of the signal path occurs at the PTH to Metral connector solder point. Point 50 in *Figure 1.* The ground reference for the low inductance tip is the solder point for an adjacent connector ground pin. The circuit element for the connector is modeled by T(5,50). A SPICE model is provided by DuPont, the connector manufacturer. The TDR waveform clearly shows the capacitance of the solder filled PTH lowering the impedance to 50Ω, *Figure 6.* The same figure then shows the connector wire presents an inductive impedance increase for the signal. *Figure 10* shows considerable overshoot damping. It also shows an increase in rise time and fall time. The multiple discontinuities to this point have degraded the initial rise time of the signal so that the overall effect is that of line loss. The passive pull up accentuates only the resistive portion of the impedance rather then the reactive.

Notice the reflection that is well defined at the bottom of the falling edge. A closer examination of *Figure 8* shows that this same reflection is present in an attenuated form. The peak of this reflection is about 2 ns from the point where the signal crosses into an undershoot state. The delay per unit length, t_{pd}, of the unloaded backplane depends on the relative magnetic permeability, μ_r, the relative dielectric permittivity, ϵ_r, and the speed of light, c.

$$t_{pd} = \frac{\sqrt{\mu_r \epsilon_r}}{c}$$

With $\epsilon_r = 4.7$ and $\mu_r = 0.99$, then $t_{pd} = 0.18$ ns/in. So a round trip of 10 in., slot 5 to slot 0 and back, will be a delay of about 1.8 ns. This is almost exactly the delay of the reflected pulse at the connector solder point in *Figure 10.* The delay is measured from the falling edge tangent line. The period of this pulse is about 1.5 ns which is a frequency of 667 MHz.



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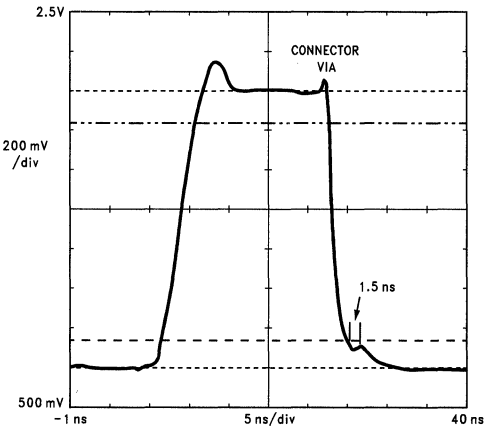
Rise 4.000 ns	Fall 1.689 ns	Max 2.34200 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 652.000 mV	Over Shoot 16.8056 %	Under Shoot 555.556 m%	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST05	Pan/ Zoom on

FIGURE 9



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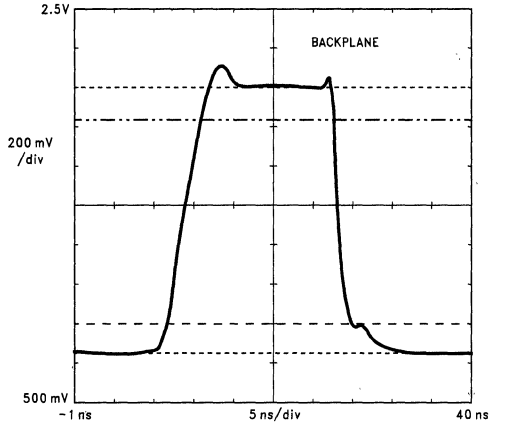
Rise 4.457 ns	Fall 2.410 ns	Max 2.26200 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 696.000 mV	Over Shoot 11.1270 %	Under Shoot 570.613 m%	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST07	Pan/ Zoom on

FIGURE 10

ENTERING THE BACKPLANE

After the connector, the signal reaches the backplane environment. The signal has been transformed by the daughter board path. Besides the impedance factors, the skin effect losses have rounded top and bottom portions of the edges.

The probe points are at the solder points of the Metral connectors to the backplane PTH. The waveform in *Figure 11* was obtained at the slot where the board is inserted, just on the backplane side of the connector from the previous figure. The connector increases the fall time by 500 ps and damps the overshoot. The increase in fall time here appears to be a result of the reflected pulse increasing in amplitude. As the incident wave propagates further down the backplane the same damping of overshoot and increase in transition times occurs. The backplane characteristics are dependent on the loading that is present in the form of inserted boards with transceivers.



TL/F/11107–19

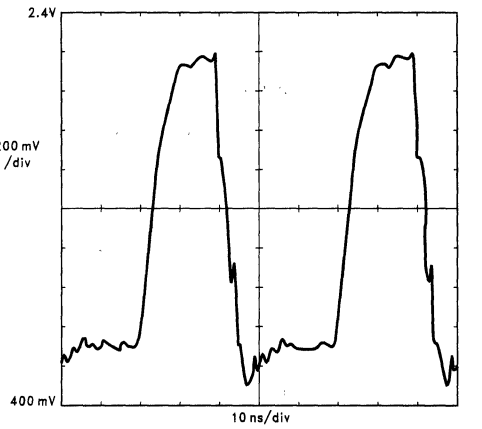
Rise 4.688 ns	Fall 2.898 ns	Max 2.21600 V	Measure-ments	Distal 90% Proximal 10%	
Min 742.000 mV	Over Shoot 8.43195 %	Under Shoot 591.716 m%	Statistics Comp & Def Sample # 100	Remove Wfm 1 ST010	

FIGURE 11

THE LOADED BACKPLANE

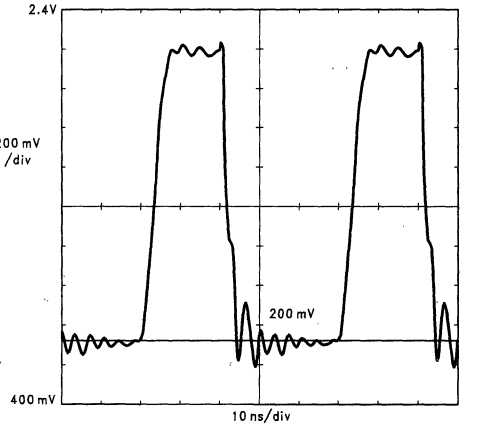
The distributed capacitive loading of the backplane has significant effects on the signal. The position of the loads with respect to the driving board will determine how the reflections add to degrade the signal. The worst case is when the reflections cut into the noise margin; i.e., the reflections that are positive going on the low output and negative going on the high output. The investigative results show that reflections in the high state never go below the 2.1V level by more than 50 mV. The problem on the high end occurs when the bus is fully loaded. At 20 MHz and fully loaded, the rising edge becomes rounded, *Figure 12.*

The worst bite into the noise margin was found in the case of 2 loads, 12 pF each, in specific slots on the backplane. The driver in slot 5 and the loads in slot 6 and 0 caused sustained ringing with a peak amplitude of 200 mV into the noise margin low. The case is shown in *Figure 13.* It should be noted that the period of the ringing in *Figure 13* is about 2 ns. This corresponds to a frequency of 500 MHz. This presents a demand on test equipment to pick up these high frequency signals.



TL/F/11107–21

FIGURE 12. Backplane Probed at Driver = Slot 5, 10 pF to 12 pF Loads in Every Slot



TL/F/11107–22

Rise 4.938 ns	Fall 3.603 ns	Max 2.21200 V	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Min 598.000 mV	Over Shoot 1.64384 %	Under Shoot 8.90411 %	Statistics Comp & Def Continuous	Remove Wfm 3 ST013	Pan/ Zoom on

FIGURE 13. Backplane Probed at Driver = Slot 5, 12 pF Loads in Slots 0 and 6

GIGA HERTZ BANDWIDTH

A 400 MHz probe and scope would not pick up all of the frequency components of this ringing. Because of the high frequency components that comprise this signal, all of the measurements done by National Semiconductor on the Futurebus+ chip set are obtained by using the Tektronix

P6204 FET probe and 11A72 amplifier mounted in the 11403 digitizing oscilloscope. This combination has a bandwidth of 1 GHz.

Figure 14 is included to show how a single load of 12 pF will cause different reflections depending on where it is inserted with relation to the driving transceiver. The line delay is evident when the reflection from the adjacent load appears before the reflection from the far end load. The different loading positions will determine the waveform shape and how it will encroach on the noise margin.

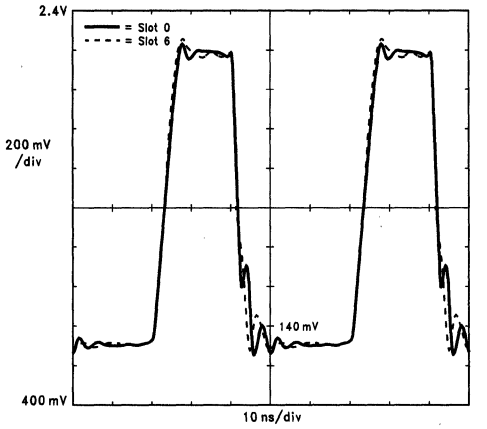


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FIGURE 14. Backplane Probed at Driver = Slot 5

WHY ALL THE DIFFERENT GROUNDS?

There are three different types of gound pins on the National Semiconductor Futurebus+ Chip Set. They are the logic ground (GND), the BTL grounds (B0GND–B8GND) and the bandgap reference ground for receiver threshold (QGND). All of these ground reference pins are isolated inside of the chip to limit the interference from high current switching transients. Outside the chip, the bandgap reference ground should be connected to the backplane ground through a quiet channel. The isolation purpose is so the receiver input threshold will follow the same reference as the signals coming off the backplane. The other grounds should be tied to the board ground plane to prevent ground loop currents inside the chip.

FUTUREBUS+ TRANSCEIVER GROUND BOUNCE

A single transceiver can have up to 9 BTL channels switching at the same time. If each channel sinks 80 mA, there is substantial current switching taking place. The combination of the ground lead inductance and finite resistance of the current return paths cause voltage drops and rises to occur along this path that are proportional to the changing current.

$$V = L\,(di/dt)$$

where V = amplitude of the ground bounce

L = inherent inductance of signal and ground trace

The DS3886 Latched Data Transceiver mounted in the Hybricon proto board was used to investigate the amount of ground shift that is experienced in the Futurebus+ environment.

Eight channels are connected to the same input so that they are switching simultaneously. The ninth channel, B3 (located between the other eight), is driven to the asserted state and used as a reference. Six other data transceivers were also on the board and allowed to switch at random (open driver inputs). The Futurebus+ connector pin layout uses 1 of every 3 pins as a ground pin. The Hybricon board links all these pins to the board ground plane as they enter through the Metral connector. The transceiver BTL ground pins are mounted to the solder pad and then traverse a microstrip track to a PTH via to make ground plane contact. The microstrip adds inductance to the ground path but is necessary for even heating to solder the chip package to the thermally isolated pad.

PROBING THE GROUND

The backplane ground plane is used as a reference to investigate all of the ground differences in the circuit. It is accessed through a ground tab connector on the Metral power connector module. *Figure 15* shows the idle backplane noise at the top of the picture. The GHz probe with a short, low inductance alligator clip ground was used to probe two of the empty slot ground tabs. There was no transceiver activity for this situation. The second from the top waveform is the same probe position only eight transceiver channels are now switching. Large disturbances in the signal occur at the time that eight channels are all going from high to low, the time of substantial active current change. Notice how the low to high transition does not create the same sort of voltage spike on the ground signal. This is because the collapsing current doesn't have a large *di/dt.*

The same backplane ground reference was used for all of the measurements in *Figure 15.* The third pattern was obtained probing the daughter board ground plane close to the Metral connector between the switching transceiver and the backplane. The disturbances are muted in this case by the bypass capacitors of the board. The board is decoupled by 4–180 μF and 14–0.1 μF capacitors. The next waveform is from the same ground plane but it is probed at the via that connects the microstrip from the transceiver BTL ground pin to the board ground plane. This waveform is a slightly attenuated version of the waveform seen on the non switching ground pin. This is because the waveform seen at the B3GND pin is coming from the board ground plane! The inductance of the microstrip and the lead frame inside the package increase the overshoot and the undershoot of the ground bounce. The worst ground disturbance is measured at one of the switching channel BTL ground pins. This is as expected from interior transceiver noise caused by the hard turn on of the output transistor creating very rapid build and collapse of current.

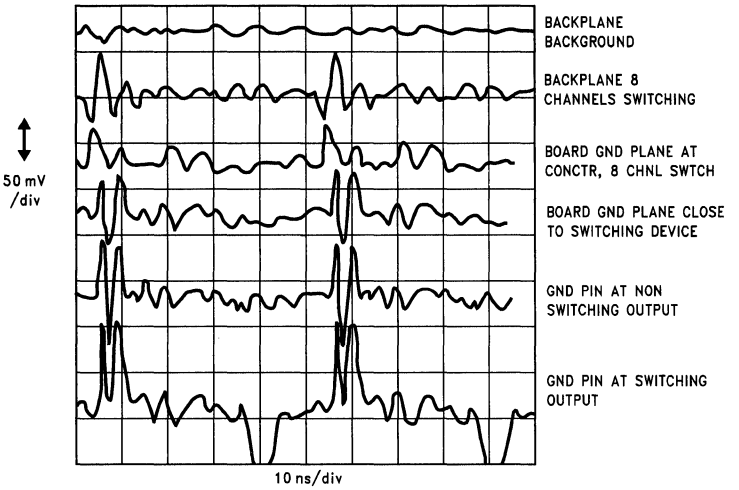

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FIGURE 15

CROSSTALK IN THE FUTUREBUS+ ENVIRONMENT

The crosstalk problem has received a lot of attention. There is the potential for significant forward and backward crosstalk due to the high speed signals, multiple transmission path media, and the density of the signal lines. These are the simplified equations relating the contributing factors.

$V_{bkwd} = (V_a/t_r)\,(\ell/2t_\ell)\,(C_CZ + L_C/Z)$
= backward coupled voltage to victim line

$V_{frwd} = (V_a/t_r)\,(\ell/2)\,(C_CZ - L_C/Z)$
= forward coupled voltage to victim line

V_a = aggressor signal amplitude
t_r = aggressor signal transition time
ℓ = line length
t_ℓ = line delay
Z = line impedance
C_C = capacitive coupling due to electric field
L_C = inductive coupling due to magnetic field

Both types of crosstalk are directly proportional to the amplitude, and inversely proportional to the transition times of the aggressor signal. The capacitive and inductive coupling affect both types of crosstalk. In backward crosstalk they add together and are multiplied by the aggressor amplitude to give a same polarity pulse to the victim. In forward crosstalk, the quantity $(C_CZ - L_C/Z)$ is multiplied by the aggressor amplitude to give a pulse of either polarity depending on the relative size of the coupled reactances. The connector does present a special problem due to the open wire configuration. The inherent inductance of the open wires and the proximity in the Metral connector are favorable situations for crosstalk. Not modeled in the above equations but still a factor is the signal wave velocity differences. Forward crosstalk also results from velocity differences of an aggressor signal due to the conductive medium contacting substances of different dielectric constants. The microstrip line is such a medium that contacts both air and epoxy glass. This creates an energy pulse that will couple electrostatically to the victim. For these reasons, crosstalk was investigated in two different ways.

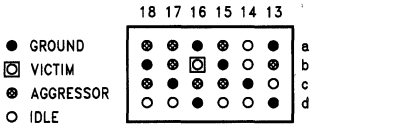

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FIGURE 16. Module B, Section 3, Used in Crosstalk Measurements. The Victim Line is Labeled B-b-16

Futurebus+ standards committees set up the pin designations on the Metral connector so that there is one ground pin for every 2 signal carrying pins. The worst case then is the situation where 1 signal pin can be surrounded by 5 signal pins and 3 ground pins as in *Figure 16*. The Expert Team tested crosstalk using a switching line as victim and measured the difference between 0 and 5 aggressors at a receiving module. *Figure 17* shows these same tests for DS3886.

The driver module is located in slot 7 and two receiver modules are in slots 0 and 9. As mentioned in the section on reflections, this is the worst configuration for cutting into

the noise margin. It is also a long length for the parallel backplane tracks to cross couple. The signal line ST2 was used as the victim and ST0–ST7 as the aggressors. *Figure 17* shows the falling edges at the driver and receiver pins for the two conditions, only the victim switching and then all aggressors and the victim switching. The largest amount of induced voltage onto the victim line is 50 mV. This is the same result as the Expert Team.

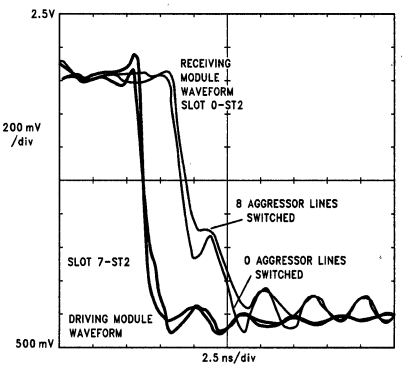

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FIGURE 17

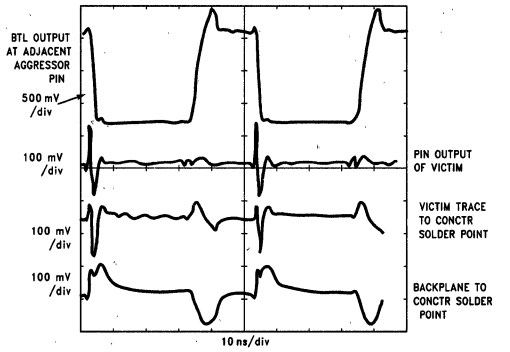

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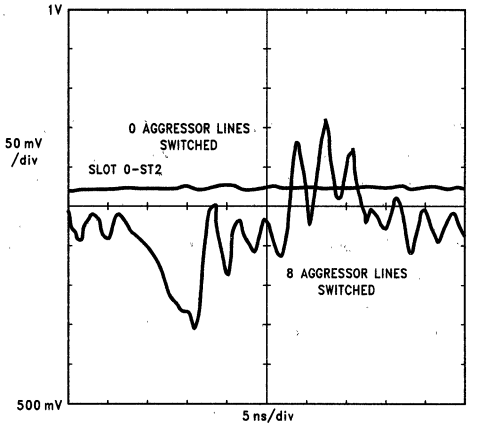
FIGURE 18. Victim Is Only Asserted, 8 Aggressor Channels Switching

Figure 18 shows results of a different way of investigating the crosstalk than the Futurebus+ Expert Team method. The victim line was held in the asserted state while 8 aggressor lines were switching. The top waveform is the aggressor signal. The three lower waveforms are the victim signal probed at daughter board impedance points. The figure shows that the victim experiences a 100 mV pulse into the noise margin at the high to low transition of all the aggressors. This case is measured on the backplane at the same slot as the driver. A demonstration of the high inductance of the Metral connector is the inversion of the induced signal through the connector. The inductance of the connector is large enough to give the forward crosstalk an inverted pulse at this point. In an actual data transmission, the crosstalk concern would be at the input to the receiving transceiver. The slowing of the edge rates by the time they reach a receiver on another board will further reduce the magnitude of the crosstalk. *Figure 19* shows the signal at the same receiver input pin with no aggressors and with 8. The coupled voltage intrusion to the noise margin is 85 mV.



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Rise 466.7 ps	Fall 435.0 ps	Min 590.000 mV	Measure-ments	Horz Mag 1 x Horz Pos Gr Opts	
Max 862.000 mV	Frequency 274.3 MHz		Statistics Comp & Def Continuous	Remove Wfm 2 ST014	Pan/ Zoom On

FIGURE 19. Crosstalk Voltage at Receiver with 8 Aggressor Lines Compared to 0 Aggressors

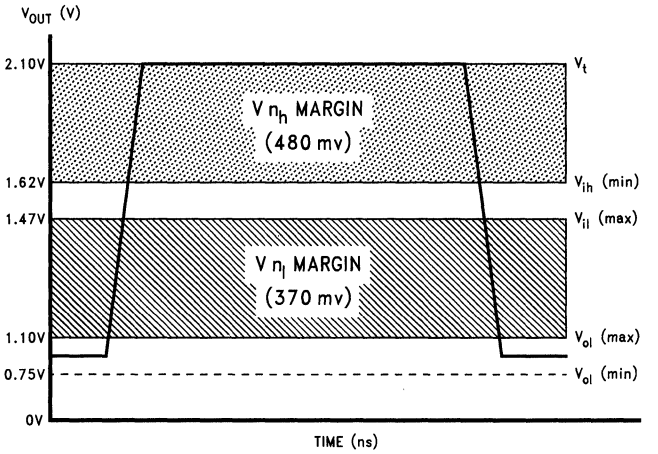

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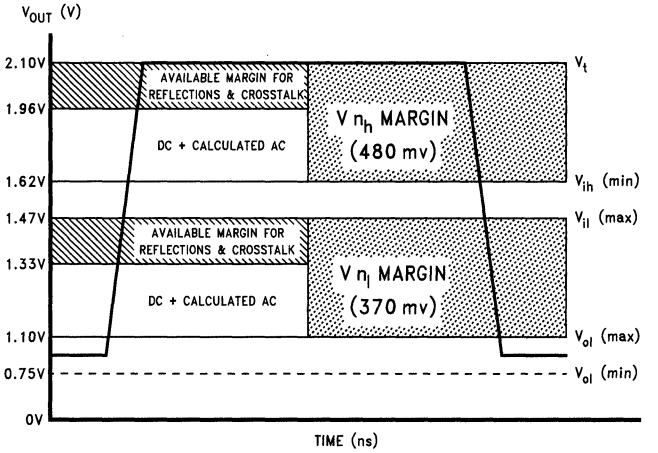
FIGURE 20a.



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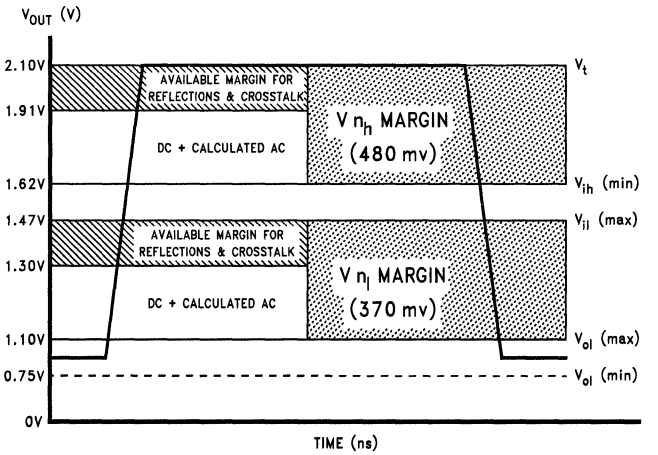
(all slots loaded)
FIGURE 20b.



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slots 0 to 6 loaded
FIGURE 20c.

CONCLUSION

The Futurebus+ environment presents impedance mismatches to the high speed data signals. These circumstances make the measurement of the signals dependent on where they are measured. The fast edge rates of the signals have high frequency components that compose a large part of the waveform and can not be ignored. For these reasons, National Semiconductor uses 1000 MHz bandwidth test equipment, and specially designed low impedance test jigs for all of the data sheet specifications.

The placement of modules in a partially loaded backplane is crucial to the magnitude of the ringing. The equal distribution of the modules in the backplane appears to be the best condition for the lowest magnitude ringing.

Figure 20a shows the noise margins for BTL. *Figure 20b* shows the allocation of the noise margin for a fully loaded backplane and partially loaded in *Figure 20c* according to the Futurebus+ Expert Team. They have done extensive simulations that are reported in the Interim Report presented on September 14, 1990. This investigation of the reflections and crosstalk will be compared to their findings.

Figure 17 shows the combination of worst case crosstalk and reflections that were found in this investigation. The crosstalk added to the reflections to cut into the noise margin low by 100 mV. The 100 mV intrusion is deduced from the fact that the incident edge has a distinct edge at the 1.2V level. This is within the allowed 170 mV range in the Expert Team analysis of the partially loaded backplane, *Figure 20c*. This investigation also showed that the fully loaded backplane produced lower magnitude reflections than the partially loaded backplane. The measurements collected here support the Expert Teams allowance of only 140 mV for reflections and crosstalk in the fully loaded backplane, *Figure 20b*.

The National Semiconductor DS3886 Latched Data Transceiver maintained signal integrity in the Futurebus+ Backplane environment under severe operating conditions. Worst case situations of crosstalk, stub length and ground bounce combined with a transmission speed of 40 MBaud were used to test the DS3886 in real backplane operating conditions. The incident edge of the BTL signal consistently crossed the receiver threshold without a problem.

REFERENCES

1. *The Multilayer Printed Circuit Board Handbook,* J.A. Scarlett, Electromechanical Publications, Ayer, Scotland, 1985.
2. *TDR Fundamentals,* Application Note 62, Hewlett Packard, April, 1988.
3. *FAST Applications Handbook,* National Semiconductor Corporation, 1987.
4. *Handbook of Printed Circuit Design, Manufacture, Components and Assembly,* Giovanni Leonida, Electromechanical Publications, Ayer, Scotland, 1981.
5. Interim Report of the Electrical Task Group Expert Team ... Futurebus+ Modeling and Noise Margin Results, Raytheon and DEC, Sept. 14, 1990.

Futurebus+ Wired-OR Glitch Effects and Filter

National Semiconductor
Application Note 744
Joel Martinez/Stephen Kempainen

INTRODUCTION

Futurebus+ addresses the needs of the high-end user who requires more bus performance than what has previously existed. In order to optimize bus performance, the backplane bandwidth has been increased to where the backplane line delays are in the same order of magnitude as the transfer periods. At this level, the backplane can no longer be treated as lumped loads but must be modeled as distributed loads which is in the realm of transmission lines. Designers must now deal with transmission line effects and be aware of glitches that occur when performing wired-OR functions. As the name implies, the wired-OR glitch occurs on lines that perform wired-OR logic. Wired-OR logic is implemented by connecting open-collector drivers in parallel and tying their collectors to a resistor pull-up (*Figure 1*). National Semiconductor's Futurebus+ Handshake Transceiver addresses this concern by incorporating a programmable low pass filter into the receiver. It provides optimum noise rejection while maintaining high bus through-put.

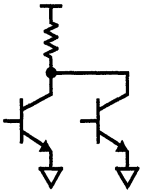

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FIGURE 1

BTL (Backplane Transceiver Logic) is the driving technology behind the Futurebus+ physical layer. Driver outputs are open-collector with a series Schottky diode. The additional diode on BTL drivers isolates the normally large collector capacitance associated with the output transistor from the bus thus reducing bus loading. BTL is used on all the bus lines in a Futurebus+ backplane. Termination of the bus is done at both ends as shown in *Figure 2*. All Futurebus+ lines are connected in a wired-OR fashion, however, only a subset of these lines actually perform the wired-OR logic. These lines are the handshake, status, capability and arbitration lines. The critical timing lines used in handshaking must have wired-OR glitch filters to maintain signal integrity. The lines requiring glitch filtering are AK*, AI*, DK*, DI*, AP*, AQ*, AR*, and RE*.

In the wired-OR configuration, the glitch observed on the backplane is caused by the release of one or more drivers on the bus while others remain asserted. The resulting positive voltage pulse is the glitch characteristic that could cross the receiver threshold and degrade signal integrity. The transmission line effect, enhanced by the fast transition times and transmission line propagation delay, dictates how the wave reflections will affect the data signal. If the rise and fall times were longer than the line delays, the reflections would be included (shadowed) in these transition portions of the signal. Then the bus would not exhibit transmission line effects. However, the Futurebus+ transition times on the backplane can be one fourth to one fifth of the line delay. A transition at one end of the backplane takes some time before it reaches the other end and voltage levels will vary significantly, due to reflections, before equilibrium.

Low to High Transition of Open Collector Bus Driver

First the low to high transition of a single driver releasing the bus will be studied. The same characteristics are involved for the wired-OR glitch as will be seen later. Referring to *Figure 3*, what happens when Q1 releases?

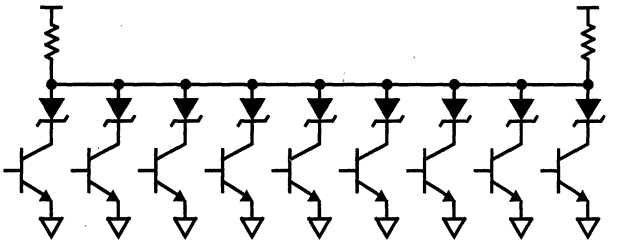

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FIGURE 2

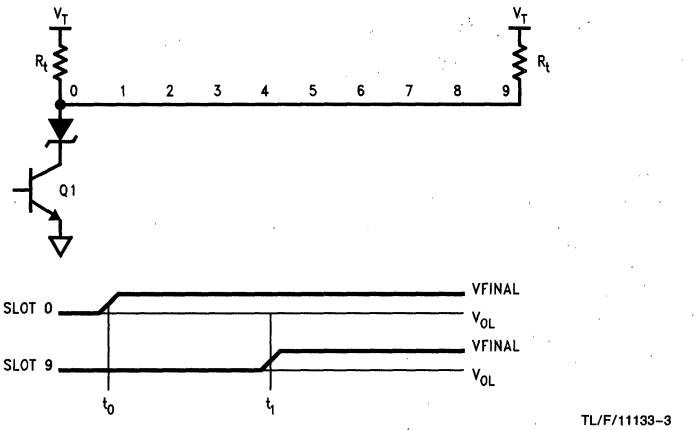

FIGURE 3

$t < t_0$; Q1 is on (asserted) and maintains a V_{OL} level on the bus.

$$V_{OL} = V_T * \frac{Zdriver}{Zdriver + (R_t/2)}$$

where Zdriver = driver output impedance

$t = t_0$; Q1 releases and a low to high wave front propagates from slot 0 towards slot 1. The current which was previously sunk by Q1 now gets injected back into the line. The driver sees an impedance of the termination resistance in parallel with the line impedance. The amplitude of the signal propagating down the line is described by the following equation:

$$VFINAL = V_{OL} + [I_{OL} * (R_t // Z_0')]$$

$$= V_{OL} + \frac{V_T - V_{OL}}{R_t/2} * (R_t // Z_0') \quad (1.a)$$

For $R_t = Z_0'$, where Z_0' is the unloaded line impedance.

$$VFINAL = V_{OL} + V_T - V_{OL}$$
$$= V_T$$

If the driver was located in slots 1 to 8 then the equation would be;

$$VFINAL = V_{OL} + \frac{V_T - V_{OL}}{R_t/2} * (Z_0' // Z_0') \quad (1.b)$$

$t = t_1$; The signal reaches slot 9. For $R_t = Z_0'$, all the energy is absorbed at slot 9 by the termination and the bus will be at equilibrium. For $R_t \neq Z_0'$ then secondary reflections will occur until the reflections settle.

Figure 4 shows the actual waveform from a 10 slot backplane with 1 in. pitch and 39Ω termination resistors. The 3 waveforms were obtained by probing the backplane at the solder points of the board connectors. In this case there were two boards inserted into the backplane, slots 0 and 9. The driver in slot 0 is switching while the other in slot 9 is off. The propagation delay of the line, tpd, is then defined as $t_1 - t_0$. This is plainly illustrated by the delay in the waveform probed at slot 0 and at slot 9. The tpd = 3 ns in this arrangement.

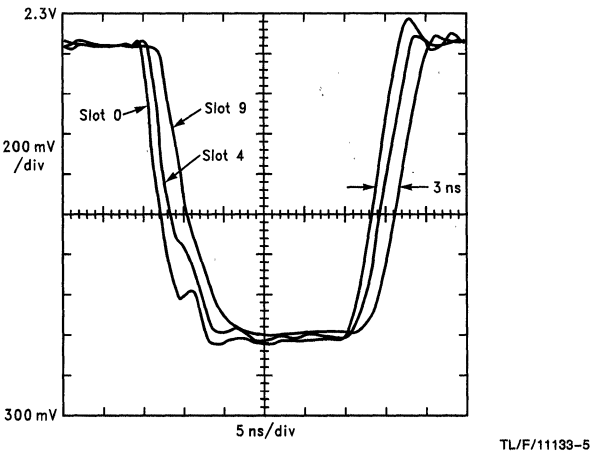

FIGURE 4

Wired-OR Glitch

As shown in *Figure 5*, things become more complicated by adding another driver at the opposite end of the bus. Initially, both drivers are asserted. Assuming they share the current from the termination equally, the V0 will be less than V_{OL} for a single driver. V0 is also influenced by the fact that the driver impedance increases with reduced current through the transistor. When Q1 releases, a glitch occurs at the drivers bus slot with a pulse-width equal to 2 times the line delay. The glitch amplitude is dependent on the amount of current that was sunk by the driver prior to releasing the line. So the more drivers that release the line simultaneously, the greater the amplitude of the glitch.

$t < t_0$ Both Q1 and Q9 are on keeping the bus voltage low. Note that V0 results from the resistor divider between the parallel driver output impedance and the parallel termination resistance. V2 is slightly higher because only one driver is on and the bus voltage is then just the resistor divider between a single driver output impedance and the two termination resistors in parallel.

$t = t_0$ Q1 turns off and transitions into a high impedance state, a low to high wave front propagates down the bus towards slot 9.

$$V1 = V0 + \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0' \qquad (2.1)$$

For $R_t = Z_0'$

$$V1 = V0 + \frac{1}{2}(V_T - V0)$$

$$= \frac{1}{2}(V_T + V0) \qquad (2.2)$$

$t = t_1$ The glitch reaches slot 9 and the reflection at slot 9 is negative because the output impedance of the driver is small compared to the termination resistor and backplane impedance.

$$V2 = V1 + \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0' * \rho$$

where $\rho = \dfrac{R_t//Zdriver - Z_0'}{R_t//Zdriver + Z_0'}$ (negative number)

$t = t_2$ The reflected wave reaches slot 0. It is important to point out that the output of Q1 is in a high impedance state when turned off. Therefore, the mismatch at slot 0 is only due to the backplane impedance and termination. For $R_t = Z_0'$, all the energy is absorbed at slot 0 by the termination and the bus will be at equilibrium. When $R_t \neq Z_0'$, then secondary reflections will occur and will continue until the reflections settle to the termination voltage.

The pulse width at the end of the backplane where the driver is still asserted is as wide as the propagation delay of the bus. Since the reflection must return to the released driver end, the pulse width there will be 2 tpd, where tpd = $(t_1 - t_0) = (t_2 - t_1)$.

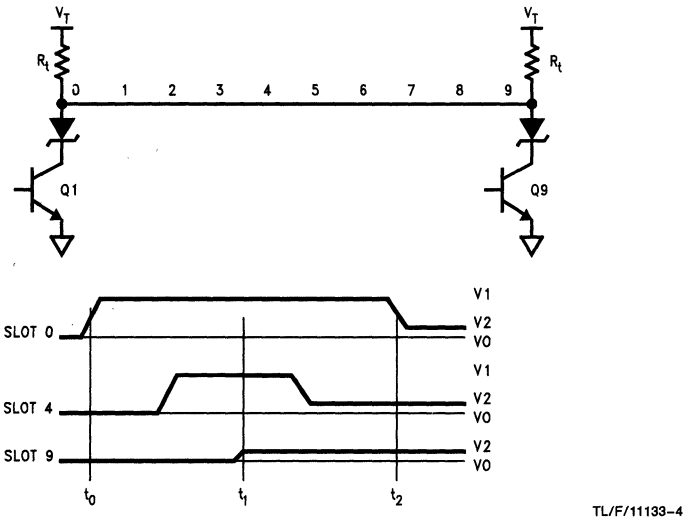

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FIGURE 5

Wired-OR Glitch Calculation for Futurebus+

To simplify the wired-OR glitch calculation for a Futurebus+ backplane, the following assumptions are used;

Z_0'	60Ω	Unloaded Backplane with Connector and Vias
Z_0''	31Ω	Fully Loaded Backplane
R_t	33Ω	Termination Resistor
$R_t//Z_0'$	21Ω	
$R_t//Z_0''$	16.0Ω	
$R_t//Zdriver$	4.3Ω	
Zdriver	5Ω	Driver Series Resistance
Vdriver	0.7V	Driver on Voltage in Series with the Resistance
V_T	2.1V	Termination Voltage
V_{TH}	1.47V to 1.62V	Receiver Input Threshold
tpd	1.8 ns	Unloaded, 10 Slot by 1 in. Pitch Backplane
	4.4 ns	Same Backplane Fully Loaded

For drivers at each end *(Figure 5)* and assuming an Unloaded condition we have;

$$V0 = Vdriver - (V_T - Vdriver) * \frac{\frac{1}{2}Zdriver}{\frac{1}{2}Zdriver + \frac{1}{2}R_t}$$

$$V0 = 0.52V$$

From equation (2.1)

$$V1 = V0 + \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0$$

$$V1 = 1.3V$$

When the reflected wave hits the mismatch at slot 9, a negative reflection adds to V1.

$$V2 = V1 + \rho^1 * V_x^1 \qquad \rho^1 = \frac{R_t//Zdriver - Z_0'}{R_t//Zdriver + Z_0'}$$

$$= 0.62V \qquad Vx^1 = \frac{1}{2} * \frac{(V_T - V0)}{R_t/2} * R_t//Z_0'$$

When this wave front reaches slot 0, another negative reflection adds to V2.

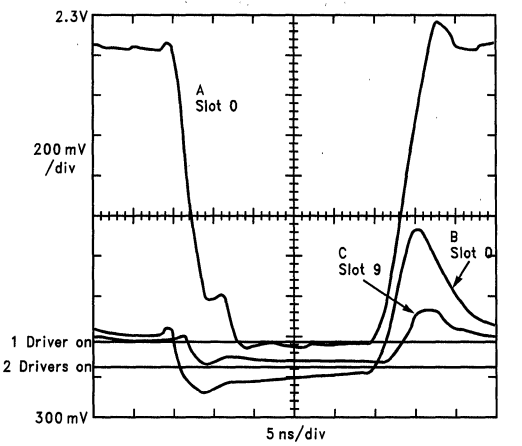
$$V3 = V2 + \rho^2 * Vx^2 \qquad \rho^2 = \frac{R_t - Z_0'}{R_t + Z_0'}$$

$$= 0.78V \qquad Vx^2 = Vx^1 * \rho^2$$

Subsequent reflections will be smaller and smaller until equilibrium is reached on the line.

The glitch has a maximum amplitude of 1.3V for two drivers sharing the bus current equally, which is below the receiver threshold of 1.47V. This isn't enough amplitude to false trigger the receiver and thus data corruption will not occur. The glitch also has a maximum pulse width equal to 2 tpd or 3.6 ns. If Q1 was sinking most of the current, then the resulting glitch will have a greater amplitude than that calculated, but the pulse width will remain the same. The greater amplitude may cross the receiver threshold and cause false triggering. The purpose of the glitch filter on the DS3884 is to filter any glitch that crosses the receiver threshold and thereby prevent false triggering. Since the glitch width is independent of amplitude, a filter can be set to reject certain duration glitches.

Figure 6 shows actual waveforms from the 10 slot backplane. The drivers are mounted in the end slots and R_t = 39Ω. The Vdriver (1 driver on) level is 685 mV and VO (2 drivers on) is 545 mV. The switching driver is shown without the other driver asserted, waveform A in *Figure 6*. Then the wired-OR glitch is shown at the end slots with one driver switching and the other holding the asserted level, waveforms B and C. As predicted by the model, the amplitude and pulse width of the glitch is greatest at the driver slot that is releasing the line. The maximum amplitude of the glitch is 1.25V. The propagation delay of the backplane with 2 boards inserted was shown in *Figure 4* to be 3 ns. The model predicted the pulse width to be twice this delay, but it is shown to be 2.33 times the delay at 50% of the amplitude. This is because the model does not take into account the



TL/F/11133–6

FIGURE 6

wave dispersion effects of the backplane which filter the high frequency components and round the signal corners. Since the glitch amplitude will never equal V_T as indicated by equation (2.1), the glitch pulse width at the receiver threshold will always be less than the 50% amplitude pulse width. Two times the measured backplane propagation delay is the worst case width that will be seen at the receiver threshold.

Theory states that glitch width is only dependent on the bus propagation delay. *Figure 7* and *8* are included to demonstrate this theory in the backplane application. *Figure 7* shows the glitch for a 1 MHz signal. The pulse width is the same as that in *Figure 6* which has a 20 MHz signal. *Figure 8* is the same situation as *Figure 6* except that the backplane slots between 0 and 9 are loaded with 10 pF to 12 pF each. This increases the propagation delay of the backplane. The width of the pulse is 10.7 ns. Using the fully loaded backplane tpd of 4.4 ns, this pulse width is 2.43 times the propagation delay. This figure correlates well with the previous partially loaded glitch width. The amplitude is noticeably less when the backplane is fully loaded due to the decreased impedance seen by the driver.

The simultaneous release of the bus line by more than one driver at a time will increase the amplitude of the glitch but the width still depends on the propagation delay of the bus. The current of more than one driver injected into the line directly affects the amplitude of the pulse. *Figure 9* shows the glitch when 2 drivers release the line simultaneously and 1 holds the line asserted. The releasing drivers are in slots 0 and 3, and the hold driver is in slot 9. The glitch amplitude of 1.81V will cause a false trigger of receivers on the line. The pulse width of the glitch at the receiver threshold low is 6 ns, about 2 tpd. The 50% of amplitude pulse width is slightly larger than the case of 2 drivers on the bus, but this is explained by the additional load capacitance of the third driver which increases the line delay.

WIRED-OR FILTER

The worst case glitch that can occur on the bus will have a pulse width equal to the round trip delay of the backplane. The filter must reject glitch pulses which are equal to and less than the worst case round trip bus delay, 2 tpd. Since the line delay is dependent on the length and the loading of the backplane, the simplest way to determine the worst case delay is by measuring the line delay of a fully populated backplane. Once the worst case delay is determined, the receivers should provide a filter that will reject the glitch and allow signals to pass through with minimum delay.

The DS3884A Handshake Transceiver which is part of National's Futurebus+ chip set has a built in glitch filter. The filter can be tailored to a specific backplane delay to minimize timing delays. Four different settings—(5 ns, 10 ns, 14 ns and 24 ns) are available via the pulse select pins—PS1 and PS2. For example, if the round trip delay of the backplane is 8 ns, then the filter setting should be rounded-off to the higher setting which is 10 ns.

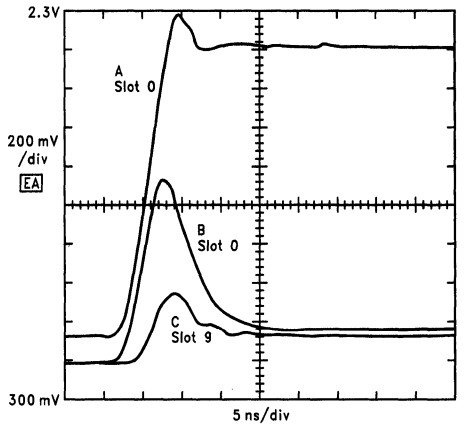


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FIGURE 7

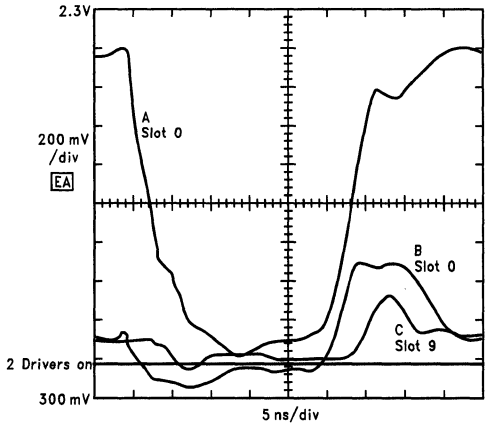

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FIGURE 8

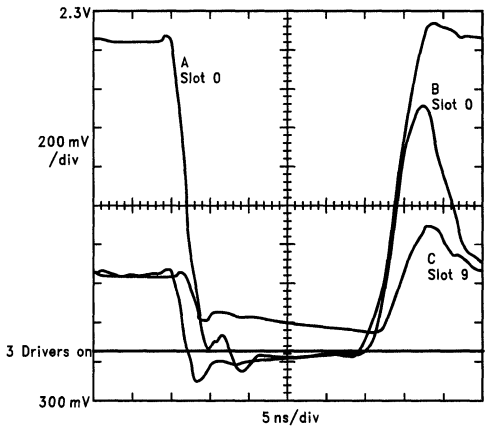

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FIGURE 9

This setting will reject glitches with pulse widths of 10 ns and less. The maximum propagation delay from the transceiver bus input, Bn, to the filtered receiver output, FRn, for the receiver high to low transition will be 21 ns at this setting. *Figure 10* shows three waveforms from the DS3884A operating in slot 0 of the same backplane configuration as *Figure 9*. Waveform B1 results from the same 2 drivers releasing the line simultaneously as Waveform B slot 0 in *Figure 9*. The lower signal amplitude is due to probing directly at the receiver input pin rather than the backplane solder point as in *Figure 9*. R1 and FR1 are the waveforms from DS3884A, channel 1, for the receiver and filtered receiver outputs respectively. PS1 and PS2 are both set to 0V to obtain a glitch rejection of 5 ns and less. Waveform FR1 clearly rejects the false triggering of the glitch, which is about 3 ns wide at the 1.5V receiver threshold. *Figure 11* shows the propagation delays for B1 to R1 and FR1 for both the high to low and low to high transitions at the 5 ns glitch rejection setting. The t_{PHL} is extended from 5 ns to 10 ns for the filtered output. The ringing on the receiver output signals results from wire wrap board frequency response limits.

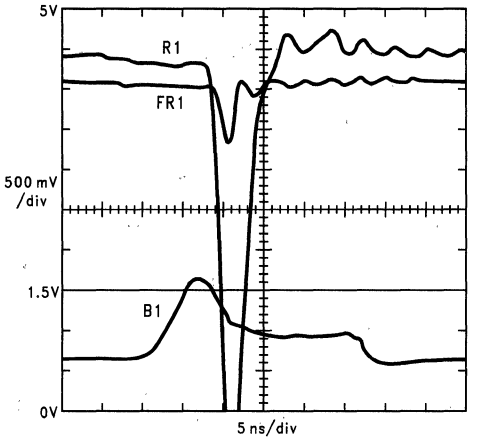

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FIGURE 10

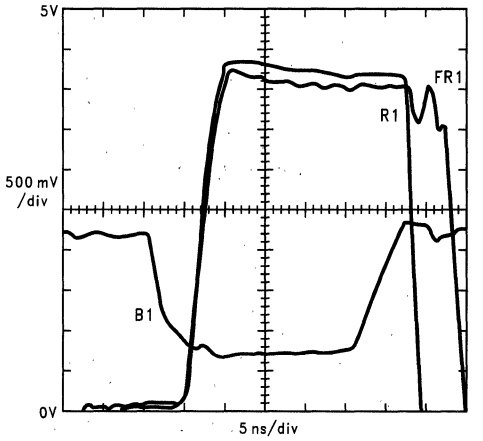

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FIGURE 11

The wired-OR glitch is inherent in wired-OR busses and will exist in a high speed transmission line environment. However, it is comforting to know that it is a well understood phenomena and there are ways of maintaining signal integrity through the use of filters.

IEEE 1194.1 BTL-Enabling Technology for High Speed Bus Applications

National Semiconductor
Application Note 829
Joel Martinez
Application Engineer

INTRODUCTION

IEEE 1194.1 Standard for Electrical Characteristics of Backplane Transceiver Logic Interface Circuits validates BTL as the enabling technology for high speed busses. Driving backplanes with BTL means higher data rates and better noise margins than previously available.

BTL solves, for the first time, the fundamental problem associated with driving a densely populated backplane. As a result, it provides significant improvements in both speed and data integrity. BTL evolved from many years of work within the IEEE committee, leading to a deeper understanding of the physics of the backplane bus and an ingenious solution to the bus driving problem.

Speed is probably the most important feature for any bus standard. In many cases the backplane becomes the bottleneck in systems where increasing processor speed and shared resources are common. In asynchronous systems, the maximum data transfer rate between any two plug-in cards is determined simply by the sum of the response times of the two cards and the bus delay. Ultimately, as logic devices get faster, bus delay will be the dominating factor limiting bus speed. In synchronous systems, the maximum achievable clock rate on the bus will also depend on the bus delay.

There are two components to the bus delay in a typical system, namely, the settling time and the propagation delay. The settling time is the time needed for reflections and crosstalk to subside before data are sampled; it is usually several times longer than the backplane propagation delay. As will be shown later, the settling time is the price the user pays for not driving the bus properly.

By using BTL, backplane busses not only eliminate the settling time delay but also reduce the propagation delay of the loaded backplane to provide maximum possible bus throughput.

THE PHYSICS OF THE BACKPLANE BUS

For high-speed bus signals where the signal rise and fall times are less than the round-trip delay, the bus acts as a transmission line with an associated characteristic impedance and propagation delay whose unloaded values, Z_o and tp_o are given by

$$Z_o = \sqrt{\frac{L_o}{C_o}} \qquad \text{(EQ 1)}$$

$$tp_o = \sqrt{L_o C_o} \qquad \text{(EQ 2)}$$

where,
L_o = Distributed intrinsic inductance per unit length
C_o = Distributed intrinsic capacitance per unit length (1)

These values can be calculated for a typical stripline backplane *(Figure 1)* by means of the following equations;

$$Z_o = \frac{60}{\sqrt{\epsilon_e}} \ln\left[\frac{4h}{0.67\pi\,(0.8w + t)}\right] \qquad \text{(EQ 3)}$$

$$tp_o = 1.017\sqrt{\epsilon_r} \qquad \text{(EQ 4)}$$

where,
ϵ_r = relative dielectric constant of the board material
h = height between ground planes
w = width of signal trace
t = thickness of signal trace (5)

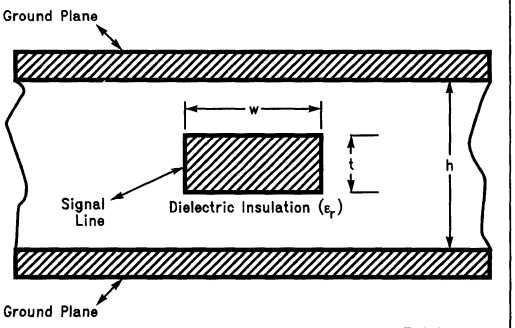

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FIGURE 1. Stripline

For a typical backplane, h = 52 mils, w = 12 mils, t = 1.4 mils (1 oz. Copper), ϵ_r = 3.5 (epoxy-glass). By substituting these values we get Z_o = 70Ω and tp_o = 1.9 ns/ft.

These values correspond to an unloaded backplane. When the backplane is uniformly loaded with the capacitance of plug-in cards and connectors at frequent intervals, the loaded values of the impedance, Z_L, and the propagation delay, tp_L, are given by

$$Z_L = \frac{Z_o}{\sqrt{1 + \frac{C_L}{C_o}}} \qquad \text{(EQ 5)}$$

$$tp_L = tp_o\sqrt{1 + \frac{C_L}{C_o}} \qquad \text{(EQ 6)}$$

where,
C_L = distributed load capacitance per unit length(1)

The distributed capacitance, C_o, of the unloaded backplane can be derived from equations 1 and 2.

$$C_o = \frac{tp_o}{Z_o} \qquad \text{(EQ 7)}$$

For our stripline,

$$C_o = \frac{1.9\,\frac{ns}{ft}}{70\Omega} = 27\,\frac{pF}{ft}$$

This does not include, however, the capacitance of the connectors mounted on the backplane and the associated plated-through holes, which can amount to 5 pF per card slot.

The loading capacitance of the plug-in card, however, is dominated by the loading capacitance of the transceiver, which may be 12–20 pF for TTL devices. Allowing another 3–5 pF for printed-circuit traces and the connector, the total loading per card slot may add up to 25 pF. For a backplane where the spacing between adjacent slots is 0.8 inch, the capacitance per unit length is given as

$$C_L = \frac{1}{d_{slot}}\left(\frac{12\text{ in}}{1\text{ ft}}\right)(C_{slot})$$

where,

d_{slot} = slot to slot spacing

C_{slot} = capacitance per slot

For the example above,

$$C_L = \frac{1}{0.8\text{ in}}\left(12\,\frac{\text{in}}{\text{ft}}\right)(25\text{ pF}) = 375\,\frac{pF}{ft}$$

Therefore,

$$Z_L = \frac{70\Omega}{\sqrt{1+\frac{375\,\frac{pF}{ft}}{27\,\frac{pF}{ft}}}} = 18\Omega \qquad \text{From (EQ 5)}$$

$$tp_L = 1.9\,\frac{ns}{ft} \times \sqrt{1+\frac{375\,\frac{pF}{ft}}{27\,\frac{pF}{ft}}} = 7.3\,\frac{ns}{ft} \qquad \text{From (EQ 6)}$$

As can be seen above, the capacitive loading drastically alters both the impedance and the propagation delay of the bus. This reduces the bus throughput in two ways. One obvious impact is the increased propagation delay. But the not so obvious and even more serious problem is the reduced bus impedance, which is much harder to drive.

For example, to drive the loaded bus properly with a TTL driver which has a 3V nominal swing, the required drive current, I_D, must be

$$I_D = \frac{3V}{\left(\frac{Z_L}{2}\right)}$$

The impedance seen by the driver is half of Z_L, since from a given board two transmission lines are being driven in parallel towards each terminator *(Figure 2)*. Therefore,

$$I_D = \frac{3V}{\left(\frac{18\Omega}{2}\right)} = 333\text{ mA}$$

This is much higher than the standard TTL's drive capability of 50 mA to 100 mA. *Figure 3* shows the effect of using a 50 mA driver, in this situation, on the bus waveform. The voltage swing on the bus has its first transition at 0.45V, the product of the drive current and the $Z_L/2$ (loaded impedance in parallel). This value falls well below the upper threshold limit of the TTL receiver. Therefore, several round-trip delays to the nearest termination are required for the waveform to cross the receiver threshold region. In our example, one round-trip delay for a 19 inch backplane is given by

$$t_{(2\,d)} = 2\,(tp_L)\,(\text{length})$$

$$t_{(2\,d)} = 2\left(7.3\,\frac{ns}{ft}\right)(19\text{ in})\left(\frac{1\text{ ft}}{12\text{ in}}\right) = 23\text{ ns}$$

Therefore, settling times can exceed 100 ns even for relatively short buses. This long settling time drastically affects bus throughput at high speeds. Even worse, the voltage steps in the threshold region may cause multiple triggering in the clock and strobe cases.

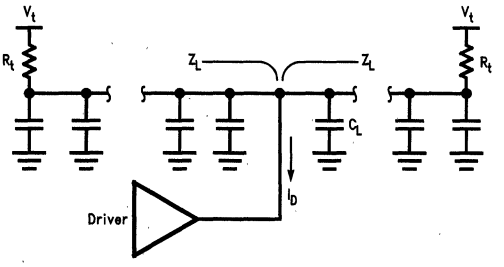

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FIGURE 2. Driver Sees Two lines in Parallel ($Z_L \parallel Z_L = Z_L/2$)

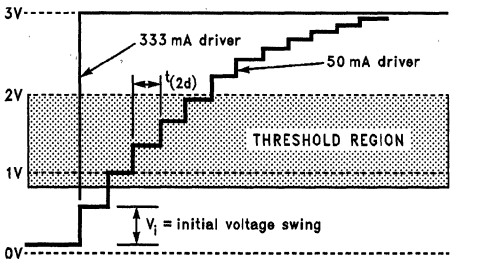

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FIGURE 3. TTL Bus Waveforms (50 mA vs 333 mA Driver)

One way to solve these problems is to use high current drivers with precision receivers that have a narrow threshold region such that the first transition crosses well over the threshold. This technique is widely used for clock lines to avoid multiple triggering. Its use on data/address lines is limited because of the significantly higher power requirements arising from the large number of lines involved (32 or 64 address/data lines).

Even if power is not a limitation, switching to higher current drivers provides only a marginal improvement. The reason for this is quite simple. A high current driver unfortunately has a higher output capacitance, which reduces the bus impedance further. This in turn requires an even higher current drive for proper operation.

IEEE 1194.1—BTL

A more elegant solution—one that is now IEEE 1194.1 Backplane Transceiver Logic—directly attacks the root of the problem, namely, the large output capacitance of the driver. IEEE 1194.1 specifies the maximum input/output capacitance to less then 5 pF. One BTL implementation is to add a Schottky diode in series with an open-collector driver output. The capacitance of the drive transistor is isolated by the small reverse-biased capacitance of the diode in the non-transmitting state *(Figure 4)*. The Schottky diode capacitance is typically less than 2 pF and is relatively independent of the drive current. Allowing for a receiver capacitance of another 2 pF, the total loading of a BTL transceiver is kept under 5 pF.

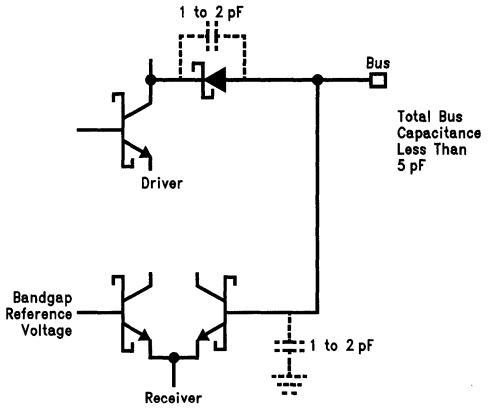

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FIGURE 4. Typical BTL Input/Output Structure

In addition to reducing the loading on the bus, BTL features several other enhancements over a conventional TTL transceiver that drastically reduce power consumption and improve system reliability.

A major portion of the power saving comes from a reduced voltage swing (1V) on the bus. Contrary to popular belief, the lower swing does not reduce crosstalk immunity (provided the receiver threshold is tightly controlled). The induced crosstalk from other lines on the bus scales down with the amplitude of the signal transition causing it. Consequently, if a line receiver has a precision threshold, the noise margin, expressed as the percentage of signal amplitude, remains the same, as does the crosstalk immunity. However, the absolute noise margin, with reference to a noise source external to the bus, does shrink linearly with amplitude. Fortunately, the low impedance and the relatively short length of the bus make this externally generated noise component insignificant in high-speed backplanes. Nevertheless, it is recommended that the backplane be shielded from strong noise sources external to the bus. Strip-line construction for backplanes provide excellent shielding from the environment but also aids in reducing crosstalk.

NOISE IMMUNITY AND EMI

IEEE 1194.1-BTL specifies a precision receiver threshold centered between the low and high bus levels of 1V and 2.1V, respectively *(Figure 5)*. Confined to a narrow region of 1.55V ±75 mV (1.47V to 1.62V), the threshold voltage is independent of V_{CC} and temperature. This tight threshold control is achieved by using an internal bandgap reference at the receiver input *(Figure 4)*. And with a smaller 1V swing, EMI is also reduced threefold compared with TTL.

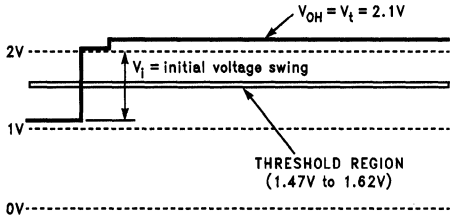

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FIGURE 5. BTL Bus Waveforms—IEEE 896 Electrical Environment

IEEE 896—Futurebus+ ELECTRICAL

The bus termination, backplane impedance and module capacitance tolerance are found within IEEE 896.2 Physical Layer and Profile Specifications. The electrical specification for Profiles A, B and F are found in chapters 6, 7 and 8, respectively. The nominal backplane impedance for the profiles listed above is specified as 60Ω for an unloaded backplane with vias. Without the vias, the backplane impedance Z_O is 67Ω with C_O = 29 pF/ft. The load capacitance per slot is the sum of the backplane via and backplane connector capacitance plus the board capacitance. C_{slot} is calculated below,

$$C_{slot} = C_{via} + C_{connector} + C_{board}$$
$$C_{slot} = 0.75\ pF + 0.45\ pF + 10\ pF$$
$$C_{slot} = 11.2\ pF$$

The load capacitance C_L is

$$C_L = 11.2\ pF \left(\frac{1}{1.2\ in}\right)\left(\frac{12\ in}{1\ ft}\right) = 112\frac{pF}{ft}$$

Note: d_{slot} = 30mm (about 1.2 inches)

The fully loaded Futurebus+ backplane therefore, has an impedance value given by

$$Z_L = \frac{67\Omega}{\sqrt{1 + \dfrac{112\frac{pF}{ft}}{29\frac{pF}{ft}}}} = 30\Omega$$

From (EQ 6)

The drive current required for a 1V swing is

$$I_D = \frac{1V}{\left(\frac{30\Omega}{2}\right)} = 67\ mA$$

The current drive capability for BTL with $V_t = 2.1V$, $R_t = 33\Omega$ as specified in IEEE 896.2, is

$$I_D = \frac{2.1V - 1.1V}{\left(\frac{33\Omega}{2}\right)} = 61\ mA$$

The current drive capability of BTL is finely tuned to accomplish incident wave switching even for worse case loading situations. On the first transition, the signal passes threshold with a very comfortable noise margin as shown on *Figure 5.*

OTHER HIGHLIGHTS

As a result of reducing capacitive loading, the propagation delay decreased which further improves the bus speed.

Recalculating the loaded propagation delay for the Futurebus+ example yields

$$tp_L = 1.9\frac{ns}{ft} \times \sqrt{1 + \frac{112\frac{pF}{ft}}{29\frac{pF}{ft}}} = 4.2\frac{ns}{ft} \qquad \text{From (EQ 7)}$$

This is a 40-percent improvement over the TTL example given earlier.

It should be noted that this is the worst-case delay per foot and that the asynchronous nature of the Futurebus+ protocol will take full advantage of lower propagation delays in a typical system, either due to lower loading levels or the closer spacing of two plug-in boards that are in communication.

TERMINATION AND DRIVE CURRENT

IEEE 1194.1 specifies that BTL drivers shall be capable of sinking 80 mA (I_{OL}) at V_{OL} levels within 0.75V to 1.1V. In practice, the backplane is terminated such that the driver I_{OL} is less than 80 mA.

The drive current and the signal swing requirements determine the termination resistor value. If the drive current is derived properly, the termination will match the bus impedance under the given loading. For IEEE 896.2, the value of each of the two termination resistors (R_t) is derived below

$$R_t = \left(\frac{1V}{67\ mA}\right) 2 = 30\Omega \approx 33\Omega$$

The value chosen by the Futurebus+ electrical task group was 33Ω. The Futurebus+ Electrical Task Group performed many hours of simulation and deduced 33Ω to be the optimum value for the range of loaded and unloaded impedance of the backplane. Their thorough analysis included the effects of crosstalk, reflections, ground shift, ground bounce, termination shift, termination tolerance and multiple switching.

IEEE 896.2 requires the resistor tolerance to be within plus or minus 1% and the termination voltage (V_t) be within plus or minus 2%. Both ends of the backplane are terminated with active terminations as shown in *Figure 6.* This arrangement has significantly lower power dissipation than a "Thevenin-equivalent" two-resistor termination connected to ground and the 5V rail. The source may be shared among bus lines as long as it is properly bypassed for alternating current close to each resistor. Bypass networks should be capable of maintaining V_t within the specified tolerance during multiple switching where each bus line will source and sink at least 61 mA. Finite resistance, although small, should be taken into account when designing the termination network to compensate for voltage drops on terminations farthest from the source.

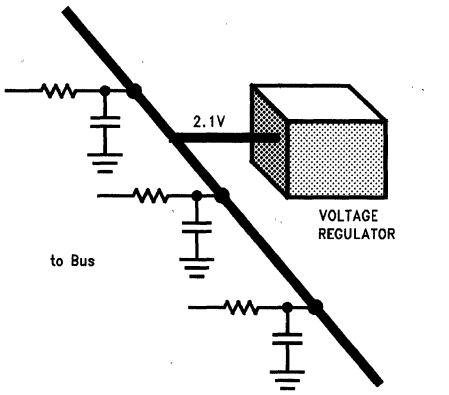

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FIGURE 6. BTL Termination

WIRED-OR GLITCH

One of the advantages of an open-collector type bus is a wired-OR capability. This feature is fully exploited in Futurebus+, particularly in its sophisticated arbitration protocol, broadcast and handshake mechanism. Unfortunately, due to the fundamental nature of transmission lines, Wired-ORing on the bus may cause erroneous glitches having pulse widths of up to the round-trip delay of the bus. The analysis of the wired-OR glitch is covered well in Application Note 744, "Futurebus+ Wired-OR and Glitch Effects and Filter".(2)

TRANSITION TIME

The rise and fall times affect the amount of unwanted noise and reflection present in a system. When it comes to transition times, faster is not always better. Drivers with fast rise and fall times induce more noise and reflections in a system than do drivers with slower rise and fall times. Some of the noise will come from voltage spikes caused by parasitic inductance in the system described by

$$V = L\frac{di}{dt}$$

where,
V = Amplitude of voltage spike
L = Inductance
di = Current through the inductor
dt = rise time

Slower rise times will reduce the amplitude of voltage spike from inductance in the current paths. Futurebus+ minimizes this problem by specifying a maximum slew rate, slew rate is the inverse of rise time. IEEE 896.2 specifies that BTL drivers shall have a maximum slew rate of 0.5V/ns or a minimum rise and fall time of 1 ns measured between 1.3V and 1.8V.

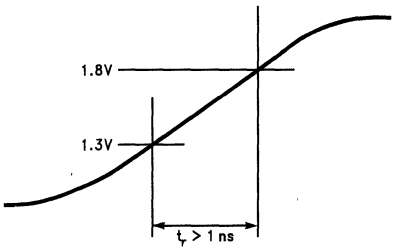

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FIGURE 7. IEEE 896.2 Rise and Fall Time Specification

MORE ON FUTUREBUS+

Geographic addressing, live insertion and withdrawal capability are some of the other highlights of Futurebus+.

The use of BTL within the Futurebus+ Electrical environment is based on a thorough knowledge of backplane operation and transmission line physics. A combination of theoretical analysis, extensive simulations and bench measurements has been used to create an electrically clean bus environment. Significant improvements have been made in favor of higher performance—at the expense of only a slight increase in today's cost and complexity—to assure a long design lifetime for the standard. The result is a robust standard that has the performance, in terms of both speed and reliability, to justify the name "Futurebus+".

PROPRIETARY BACKPLANES

The examples given above were based on the use of BTL in a Futurebus+ electrical environment. BTL is also found in many proprietary backplanes which have different requirements than those of Futurebus+. The termination resistor should be optimized to specific backplane parameters such as slot-to-slot spacing, backplane length, bus configuration, module capacitance and backplane impedance.

National also offers BTL transceivers that are similar to IEEE 1194.1 and offer other important features, such as trapezoidal drivers. The output waveform from BTL trapezoidal drivers have controlled rise and fall times which resemble a trapezoid as shown in *Figure 8*. The 6 ns transition times lead to reduced crosstalk, ground bounce and reflections. The drawback is a slower propagation delay compared to non-trapezoidal BTL drivers.

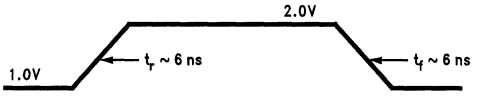

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FIGURE 8. Trapezoidal Drivers Output Waveform

ACKNOWLEDGEMENT

Special thanks to R.V. Balakrishnan for his earlier article "IEEE 896 Futurebus—A Solution to the Bus Driving Problem" of which much of this is based upon.(1)

REFERENCES

1. R.V. Balakrishnan, "IEEE 896 Futurebus—A Solution to the Bus Driving Problem", National Semiconductor Interface Data Book, 1988.
2. Joel Martinez/Stephen Kempainen, "Futurebus+ Wired-OR Glitch Effects and Filter", National Semiconductor High Performance Bus Interface Designer's Guide, 1991.
3. IEEE 1194.1—Electrical Characteristics of Backplane Transceiver Logic BTL Interface Circuits, 1990.
4. IEEE 896.2—Futurebus+ Physical Layer and Profile Specifications, 1992.
5. Michael Hayward, "Backplanes for Bus Systems", Hybricon Corporation, 1989.
6. Standard Logic Incorporated, "High-Speed Printed Circuit Backplane Electrical Design Considerations and Signal Integrity.", Technical Bulletin No. 0188.

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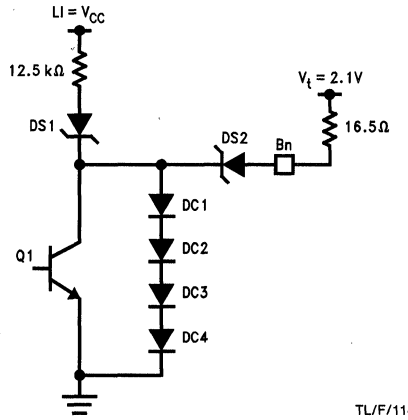
Live Insertion with BTL Transceivers

National Semiconductor
Application Note 834
Joel Martinez
Stephen Kempainen

This paper investigates the possible glitches caused by inserting a board or module into a powered Futurebus+ backplane. The signal lines on the backplane will be in one of three states; high—when the bus is released, low—when the bus is asserted, and the transition state. In the transition state the bus will be going from a high to a low state or vice versa. The bus will spend the majority of the time in the high or low state. The glitch during live insertion will be investigated for the high and low state.

The LI (live insertion) pin on the Futurebus+ Transceivers helps minimize the loading on the bus during live insertion and after the board has been plugged into the backplane.



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When LI is connected to V_{CC} and the output is in the released state, the output Schottky diode (DS2) remains reversed biased thereby minimizing the output capacitance as shown below. Reducing the capacitance at the output will minimize bus loading.

The measurements were taken from a 10 slot backplane with 1″ slot to slot spacing. The lines were terminated with 39Ω resistors to 2.1V at each end. This is not a Profile A/B/F compliant Futurebus+ backplane. A standard backplane will have 30 mm (1¼″) slot to slot spacing, 14 slots and 33Ω terminations. The board was provided by Hybricon and uses the DS3884A Futurebus+ 6-bit transceiver offered by National Semiconductor. The live insertion glitch taken on this backplane will be similar if taken on a standard Futurebus+ backplane. The measurements were taken directly on the backplane (the rear side of the backplane was probed using a high impedance 2 GHz scope) unless otherwise specified.

The Futurebus+ backplane has two stages of contact. Stage one is when the power pins between the board and the backplane mate. Stage two is when the rest of the signal pins make contact. These two stages are implemented by having short signal pins and long power pins on the backplane. As the board is inserted into the backplane the backplane power pins (VBP and ground) make contact with the board sooner than the signal pins as shown on *Figure 1*. Stage two, when the signal pins make contact with the backplane, will be the subject of this paper.

Live insertion was tested using this basic set-up. Some of the testing done included a 1 MΩ pull-up or pull-down resistor to V_{CC} or ground, respectively.

Test done with device and connector excluding the board differs in that QV_{CC}, V_{CC} and $\overline{DE}$ were not connected to 5V.

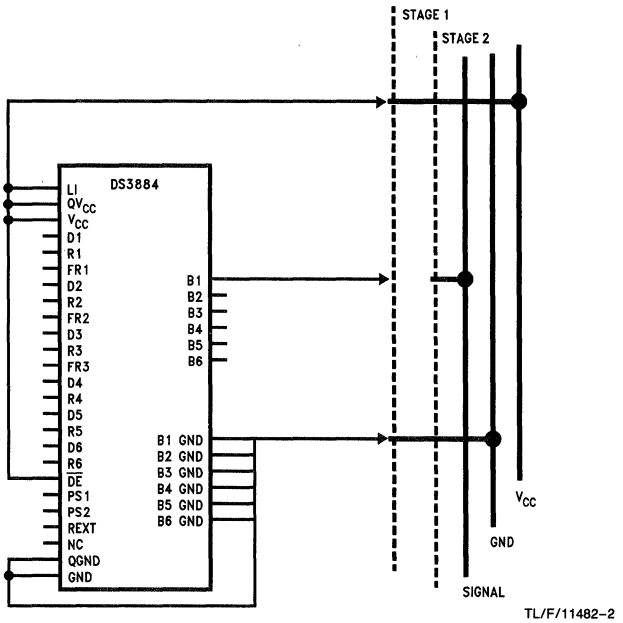

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FIGURE 1. Live Insertion Diagram

The waveforms shown on *Figures 2* to *7* are based on multiple board insertions. In each figure several waveforms are superimposed to show the various glitches observed. The waveforms shown were chosen from at least thirty that were taken for each case.

Case 1: All power pins connected—Prior to insertion all the power pins including LI and $\overline{DE}$ are connected together as shown on *Figure 1*. When the board was inserted into a backplane that was in a high state, the glitch had a maximum negative amplitude of 150 mV, as shown in *Figure 2*. The glitch reached an absolute minimum level of 1.94V. The noise margin below the glitch is about 320 mV. The noise margin is equal to the absolute minimum level minus V_{IH} min of the receiver which is 1.62V.

When the board was inserted into a backplane that was in a low state, no glitch was observed on the backplane as shown on *Figure 3*. The low state on the backplane is accomplished by having another board pull the bus low.

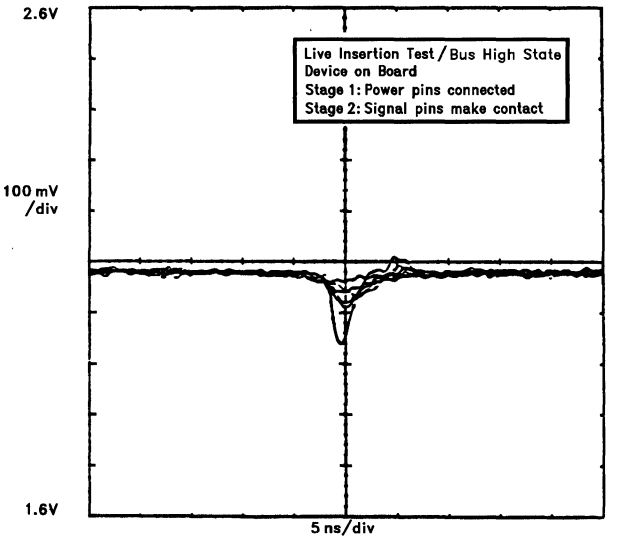

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FIGURE 2

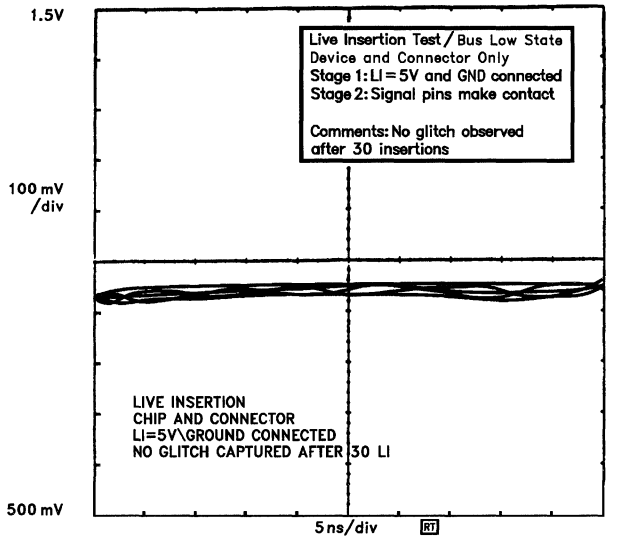

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FIGURE 3

Case 2: Live insertion pin connected—Prior to insertion. LI is connected to the power pins. LV_{CC}, QV_{CC} and $\overline{DE}$ are left floating. The device was directly soldered on a connector since the board was not re-configurable for this set-up. As shown on *Figures 4* and *5*, no glitch was observed when the backplane was high or low prior to insertion.

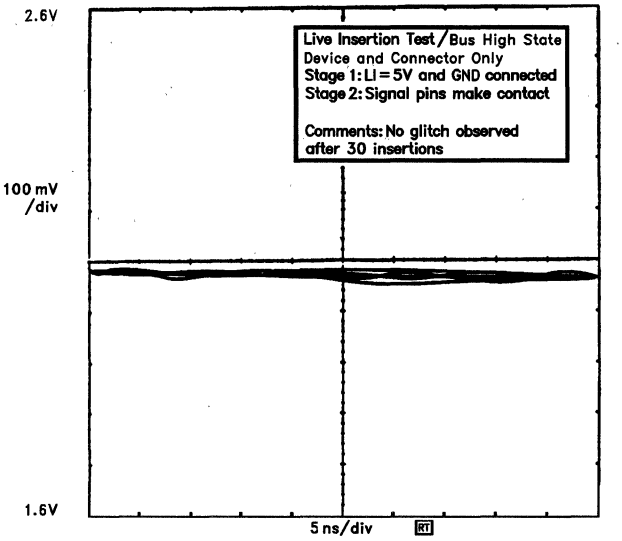

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FIGURE 4

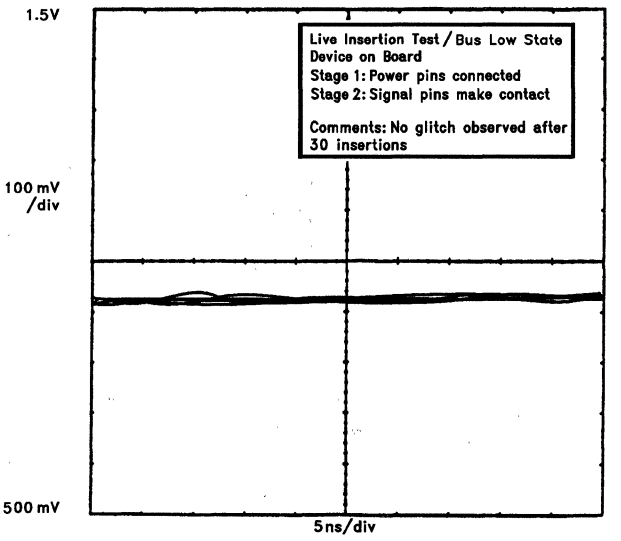

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FIGURE 5

Case 3: Live insertion pin connected to V_{CC} and B port has a 1 MΩ pull-up to V_{CC}. Case three was performed to insure that the test methodology in case two was correct. To intentionally cause a glitch during insertion, a 1 MΩ pull-up resistor was used to bias the output to V_{CC} before inserting the device into a backplane. The backplane was in a low state prior to insertion. The maximum amplitude of the glitch was 1240 mV as shown in *Figure 6*. The noise margin above the glitch was 230 mV where noise margin is equal to V_{IL} of the receiver (V_{IL} max = 1.47V) minus maximum amplitude.

Case 4: Live insertion pin connected to V_{CC} and B port has a 1 MΩ pull-down to ground. Case four was performed to insure that the test methodology in case two was correct. To intentionally cause a glitch during insertion, a 1 MΩ resistor was used to bias the output to ground before inserting the device into a backplane. The backplane was in a high state prior to insertion. The glitch reached a minimum level of 1.925V which was 325 mV away from V_{IH} of the receiver (V_{IH} min = 1.62V) as shown on *Figure 7*.

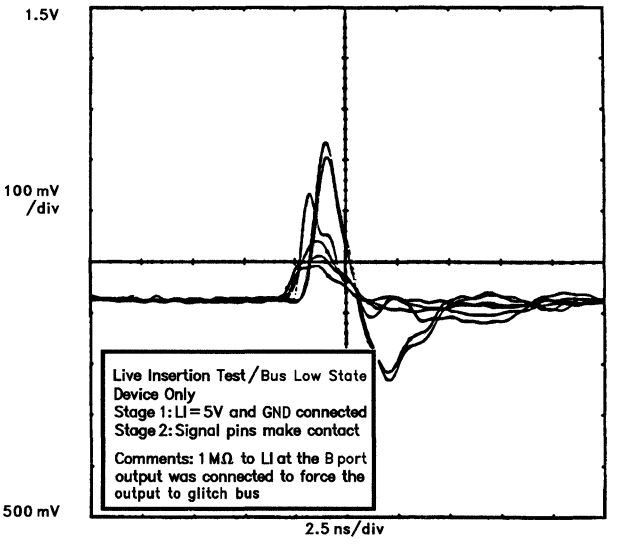

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FIGURE 6

SUMMARY

The live insertion pin LI for the Futurebus+ transceiver was designed so that the outputs could be reverse biased during live insertion prior to powering up the whole board. Reverse biasing the outputs will present minimum loading to the bus. Results showed that when LI was pulled up to V_{CC}, with QV_{CC} and LV_{CC} floating, prior to insertion no glitch was observed on the backplane. When all power pins (V_{CC}, LI, QV_{CC}) and driver enable ($\overline{DE}$) were connected to V_{CC} prior to insertion, the glitch never crossed threshold. This does not prove that there is no chance of a Live insertion glitch that may cross the threshold, but it does indicate the nature of that possible glitch. The investigations show that the glitch peak amplitude will be of short duration if it should cross the receiver threshold from either direction. If that should be the case, then National's BTL/Futurebus+ transceivers have a natural glitch rejection specified at 1 ns typical, in case a live insertion signal does cross threshold.

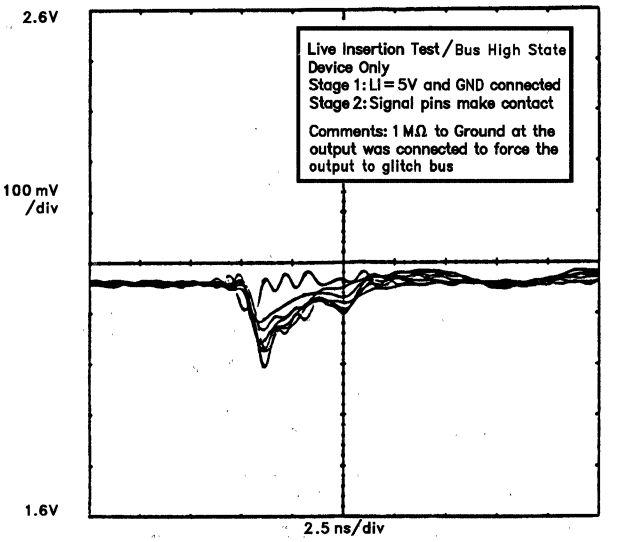

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FIGURE 7

Futurebus+ BTL Grounding Scheme

National Semiconductor
Application Note 835
Joel Martinez

Due to the high current and very high speed capability of the Futurebus+ driver output stage, device ground pin allocation, circuit board layout and bus grounding are critical factors that affect the system performance. The series inductance on any ground path should be minimized to improve ground noise and ringing. The voltage spike generated by an inductor is described by the equation;

$$V = L\,di/dt$$

where, V Voltage
L Inductance
di Change in Current
dt Change in Time

Ground bounce is dependent on the rate at which current changes with respect to time. Reducing the current passing through the inductor and minimizing the inductance will reduce the noise.

It is desirable to have multiple ground pins to distribute the current among several ground paths, thereby reducing the ground bounce. There are many ground pins on the transceivers which can be categorized into three types, Bn GND, GND and QGND. These grounds are electrically isolated within the device to reduce noise coupling between them. Externally the grounds should be connected to a common point. The driver is capable of sinking up to 80 mA with a rise and fall time of 3 ns typical. Assuming that L = 10 nH, the noise spike will be (10 nH) (80 mA/3 ns) = 266 mV per output which is acceptable. Improper ground pin allocation can have devastating consequences. In the following example, we will assume a 9-bit device with a single ground return. The noise spike from this will be (10 nH) (80 mA/3 ns) (9 output) = 2.4V which is unacceptable. For this reason, each driver output has a dedicated ground return, Bn GND. QGND, quiet ground, is used for DC circuits such as bandgaps, and current sources. QGND, the most critical of the ground pins, is a reference point to the bandgap circuit which sets the receiver threshold and other non-switching circuits. The purpose of isolating QGND is to keep the receiver threshold at the same reference as signals coming off the backplane. Noise coupled to this ground, which should be avoided, will have a direct effect on the receiver threshold. GND is used for other logic circuits.

The goal is to isolate QGND from high current switching signals. The principles above can be applied to printed circuit board design using Futurebus+ transceivers. *Figure 1* and *2* illustrate these principles. The board shown on *Figure 1* has two ground planes. Both ground palnes are connected to each other and to the backplane ground at the connector. In a Futurebus+ board, a third of the connector pin array is allocated to ground along with the power ground pins which are not shown. QGND is isolated from Bn GND on separate ground planes. GND should be connected on the same plane as Bn GND, as shown on *Figure 1*. In *Figure 2*, there is a single ground plane which connects GND and Bn GND. QGND is connected to the connector ground pin via a PCB trace. These traces should not carry any switching currents and should be kept as short as possible. There are many ways to layout and construct the grounding scheme for a board as long as you adhere to these principles.

1. Reduce the ground path inductance from the transceiver to the backplane.
   a. Short traces.
   b. Ground planes and wide traces.
   c. Use vias to connect ground pins to ground planes.
   d. Use as many connector pins for ground as possible.
   e. Place transceivers as close to the connector as possible.
2. Isolate Bn GND's from QGND's.
   a. Separate ground paths common at connector only.

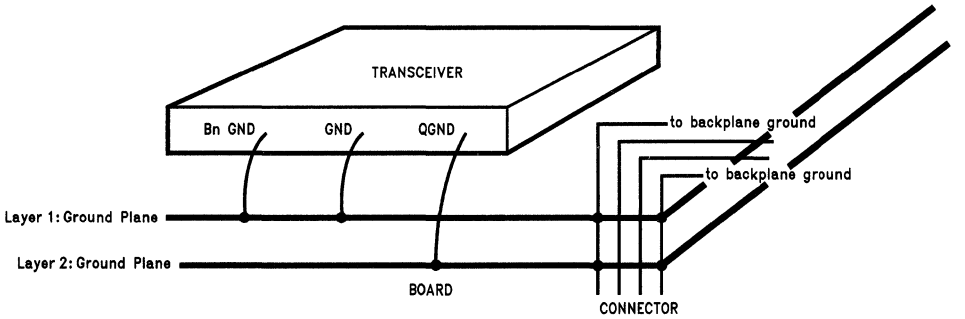

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FIGURE 1. Ground Structure with Two Ground Planes

15

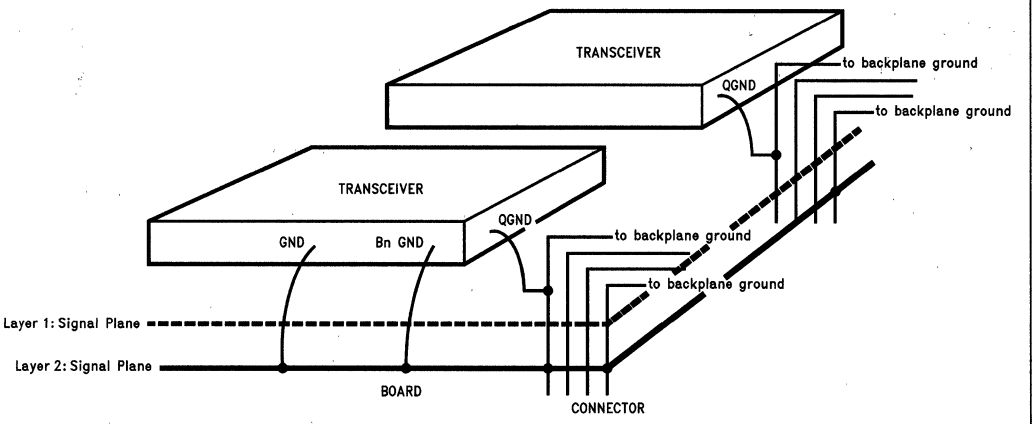

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FIGURE 2. Ground Structure with One Ground Plane

BTL Power Dissipation Calculation

National Semiconductor
Application Note 839
Joel Martinez,
Stephen Kempainen

INTRODUCTION

Futurebus+ systems designed today have bus widths of 32 or 64. To support higher bandwidths in the future, Futurebus+ provides a data width extension of up to 256 bits. BTL (Backplane Transceiver Logic) is the electrical signaling environment for Futurebus+. The number of BTL transceivers in a system will increase as the bus width is extended to accommodate higher bandwidths. A total of 16 transceivers is required to implement a 64-bit data bus. Four 6-bit Handshake Transceivers (DS3884A) are used for the handshake, central arbitration, capability and serial bus lines. One 9-bit Arbitration Transceiver (DS3885) is used for the arbitration competition lines. Three 9-bit Data Transceivers (DS3883A or DS3886A) are used for the command, status and tag lines. A 64 wide bus with byte parity requires 8 data transceivers for the multiplexed address and data lines alone. A 256 wide bus requires 32 data transceivers. Including the other lines, the total number of transceivers on single board for a 256-bit data bus is 40. The power required and dissipated by these transceivers must be fully understood to design an efficient cooling and power supply system for the backplane. Power calculations differ depending on the assumptions made concerning supply and output power. This application note illustrates how to use graphs provided by manufacturers to obtain accurate power calculations. Power is calculated for these conditions; worst case, driver outputs high, driver outputs low and outputs switching.

POWER CALCULATION EQUATIONS AND DEFINITIONS

Table I summarizes the equations and terms used in following discussions.

CALCULATING BTL POWER USING THE STANDARD METHOD

The power equation may be divided into two parts. One part is the supply power (P_S) which is derived from the quiescent current flowing into the power pins. The other is output power (P_O) derived from current flowing into or out of the input and output pins. The standard method to calculate P_S and P_O is to use specifications available in the DC Electrical Characteristics of datasheets. I_{CC}(typ) and I_{CC}(max) are typical and maximum supply current which may be found directly within the DC Electrical Characteristics. Typical power dissipation (P_{S_Typ}) is equal to I_{CC}(typ) × V_{CC}(typ). Maximum power dissipation (P_{S_max}) is equal to I_{CC}(max) × V_{CC}(max). Output power is different when the output is low and when it is high. With the output high (the device is in high impedance) essentially zero current flows in or out of the device and P_O equals zero. With the output low, P_O is equal to V_{OL}(max) × I_{OL}(max). P_O is worst case when the output is low or asserted. Typical and Maximum power calculations are shown in Table II for DS3886A. V_{OL} and I_{OL} will differ depending on the termination resistor and voltage used on the backplane which is not taken into account. Actual P_O for Futurebus+ is less and an accurate calculation of power dissipation is presented later.

TABLE I. Power Calculation Equations and Terms

Parameter	Equation	Description
V_{CC}	$4.5V < V_{CC} < 5.5V$	Supply Voltage
I_{CC}	See DC Electrical Characteristics, Typical I_{CC} vs Temperature Curves or Typical I_{CC} vs Frequency	Supply Current
V_{OL}	See Typical I_{OL} vs V_{OL} Curves	Output Low Voltage For the BTL Driver V_{OL} will Depend on the Termination Resistance Used
I_{OL}	See Typical I_{OL} vs V_{OL} Curves	Output Low Current For the BTL Driver I_{OL} will Depend on the Termination Resistance Used
V_t	2.1V	Termination Voltage
P_S	$I_{CC} \times V_{CC}$	Supply Power Power Dissipated Due to Quiescent Current Flowing into Power Pins
P_O	$V_{OL} \times I_{OL}$	Output Power Power Dissipated per Channel at the Driver or Receiver Output when the Output is Low
	$(V_{CC} - V_{OH}) \times I_{OH}$	Power Dissipated per Channel at the Driver or Receiver Output when the Output is High; For BTL I_{OH} is Zero

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TABLE II. Standard Power Calculations for the DS3886A

Typical	Max
$P_S = 5.0V \times 55\ mA = 275\ mW$	$P_S = 5.5V \times 62\ mA = 341\ mW$
$P_O = 1.0V \times 65\ mA = 65\ mW$	$P_O = 1.1V \times 80\ mA = 88\ mW$
$P_{total} = 275\ mW + (65\ mW \times 9) = 860\ mW$	$P_{total} = 341\ mW + (88\ mW \times 9) = 1.13W$

REVIEW OF BTL—BACKPLANE TRANSCEIVER LOGIC

A brief review of BTL is given to help the reader understand how the driver operates. A schematic of the BTL output stage is shown in *Figure 1*. The driver output is composed of a Schottky diode—DS2 in series with the collector of transistor Q1. DS2 shields the capacitance of Q1 from the bus to reduce capacitive loading. When the driver is asserted Q1 is "on", node a is approximately 0.4V, and node b is approximately 1V. Current flows from the 2.1V termination voltage through Rt/2, through DS2 and into the collector of Q1. When the driver is released Q1 is "off", a 12.5 kΩ resistor pulls node a which is clamped to 3V by four diode clamps (DC1 to DC4) in series. DS2 is reversed biased (node a is at a higher potential than node b), with node b at 2.1V which is equal to the termination voltage. Essentially zero current flows into or out of the driver output.

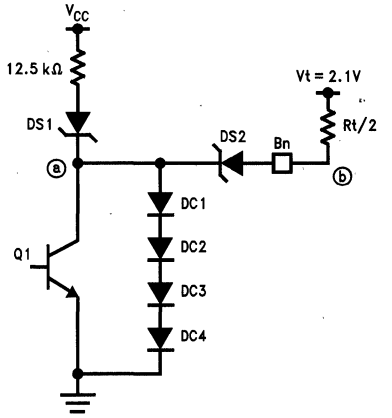

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FIGURE 1. Futurebus+ BTL Driver Output Schematic

CALCULATION OF OUTPUT POWER USING LOAD LINES

IEEE 1194.1 BTL Electrical Characteristics define I_{OL} and V_{OL}. BTL devices are required to sink 80 mA (I_{OL}) within a specified V_{OL} range of 0.75V to 1.1V. This requirement was established to maintain compatibility between vendors offering BTL devices. The BTL devices offered by National conform to this specification. The actual I_{OL} flowing into the output is dependent on the termination resistor and voltage on the backplane. National's datasheets specify 12.5Ω in series with 2.1V to test AC and DC requirements which conform to an I_{OL} of 80 mA. The equivalent representation of a 12.5Ω load in a backplane environment is 25Ω at opposite ends. The Thevenin equivalent of two 25Ω resistors is 12.5Ω. Futurebus+ requires 33Ω termination resistors in series with 2.1V at each end of the backplane as shown on *Figure 2*. The Thevenin equivalent for the Futurebus+ termination of 33Ω is 16.5Ω in series with 2.1V which is shown in *Figure 3*. I_{OL} for a Futurebus+ termination will be less than 80 mA.

I_{OL} for a Futurebus+ termination is equal to the intersection point between the output V_{OL} vs I_{OL} curve and the resistor load line as shown on *Figure 4*. The intersection point for a Futurebus+ load line of 16.5Ω in series with 2.1V at 25°C, is 65 mA and 1.025V. The intersection point for 12.5Ω in series with 2.1V is 83 mA and 1.075V. The intersection point for 9Ω in series with 2.1V is 110 mA and 1.125V. I_{OL} and V_{OL} may be obtained for any termination resistor and voltage using the load line intersection point.

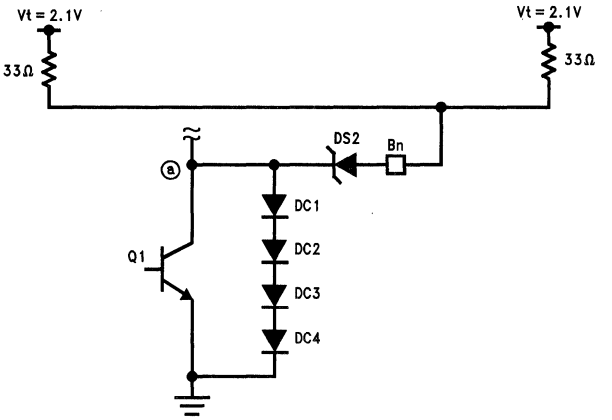

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FIGURE 2. Futurebus+ Backplane Termination

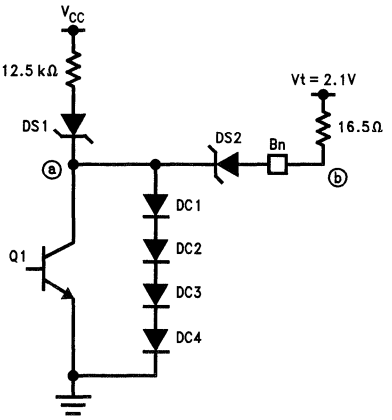

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FIGURE 3. Thevenin Equivalent of Futurebus+ Backplane

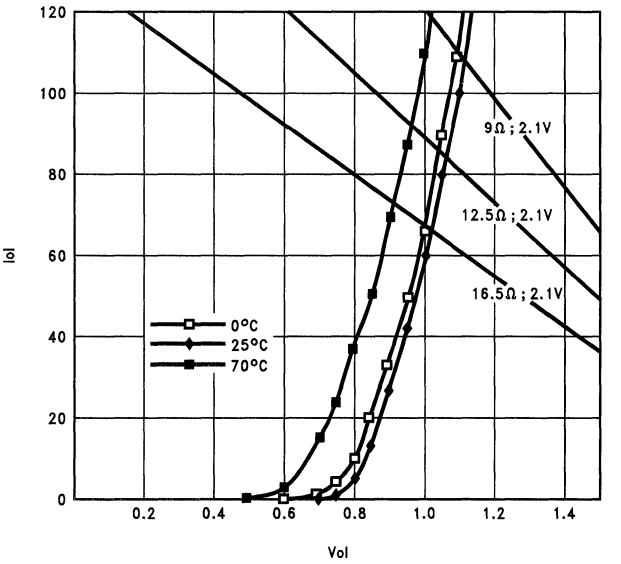

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FIGURE 4. I_{OL} vs V_{OL} and Load Line

Output power (P_O) per channel is equal to the product of I_{OL} vs V_{OL} at the intersection point. For Futurebus+ with the driver asserted, the point of intersection is 65 mA and 1.025V which yields 66.6 mW for output power. Output power for a transceiver is directly proportional to the number of bits. A 9-bit transceiver (like the DS3886A, DS3883A or DS3885) with all outputs low will need to dissipate 599 mW, which is 66 mW times 9 bits. In addition to P_O, P_S must also be included for the total power. Calculations for P_S will be given later. Output power for different loads is shown on Table III. Output power almost doubles when the resistor is reduced from 16.5Ω to 9Ω. When all drivers are released, the outputs are in a high impedance state and pulled high by the termination. At this state, essentially zero power is dissipated at the outputs.

Output power is also dependent on the duty cycle. The power dissipated at the output will equal the average power between the asserted and the released state. Assume that in a normal operation the drivers are high half of the time and low half of the time. This condition may be approximated to a 50% duty cycle. Power is calculated for a 50% duty cycle in Table III. To calculate power for other duty cycles the equation below may be used:

$$P_{O(k)} = P_O \text{ (asserted)} \times k$$

where k is equal to the duty cycle.

For example, P_O is calculated for a 9-bit device terminated according to Futurebus+ specification with a 60% duty cycle.

$$P_{O(60\%)} = 600 \text{ mW} \times 0.60 = 360 \text{ mW}$$

CALCULATION OF TOTAL BTL TRANSCEIVER POWER

Total Power is equal to the sum of P_O and P_S. Using P_O from Table III and P_S derived from *Figures 5–7*, Table IV shows total typical power for different conditions; all outputs high, all outputs low, 10 MHz and 20 MHz with 50% duty cycles. Supply power is equal to $I_{CC} \times V_{CC}$, where V_{CC} and I_{CC} were taken from *Figures 5–7*. Table V shows Maximum power using $I_{CC}(max) \times V_{CC}(max)$ from the datasheet.

TABLE III. Calculation of BTL Output Power (T = 25°C)

Termination Voltage (V)	Termination In Parallel (Ω)	Output Low Current—I_{OL} (mA)	Output Low Voltage—V_{OL} (V)	Output Power (mW)	Output Power 6-Bits (mW)	Output Power 9-Bits (mW)
BTL OUTPUT POWER PER CHANNEL WHEN DRIVERS ARE ASSERTED						
2.1	16.5	65	1.025	66.6	400	600
2.1	12.5	83	1.050	87.2	523	784
2.1	9	110	1.125	123.8	743	1,114
BTL OUTPUT POWER PER CHANNEL WHEN DRIVERS ARE RELEASED						
2.1	16.5, 12.5 or 9	0	2.1V	0	0	0
BTL OUTPUT POWER PER CHANNEL WHEN DRIVERS @ 50% DUTY CYCLE						
2.1	16.5	65	1.025	66.6/2	200	300
2.1	12.5	83	1.050	87.2/2	262	392
2.1	9	110	1.125	123.8/2	372	557

TABLE IV. DS3886 Typical Power with Futurebus+ Termination

Parameter	Supply Power	Output Power	Total Power
All Outputs Low (25°C and 5V)	210 mW	600 mW	810 mW
All Outputs High (25°C and 5V)	140 mW	0 mW	140 mW
Switching at 10 MHz (25°C and 5V)	230 mW	300 mW	530 mW
Switching at 20 MHz (25°C and 5V)	235 mW	300 mW	535 mW

TABLE V. DS3886 Maximum Power with Futurebus+ Termination

Parameter	Supply Power	Output Power	Total Power
All Outputs Low	341 mW	600 mW	941 mW

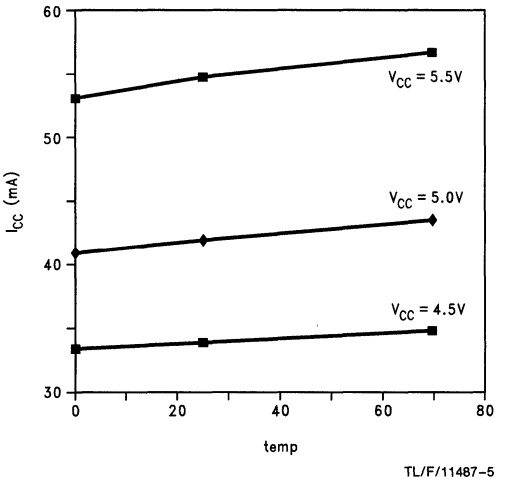


FIGURE 5. DS3886A I_{CC} vs Temperature (All Bn Outputs Low)

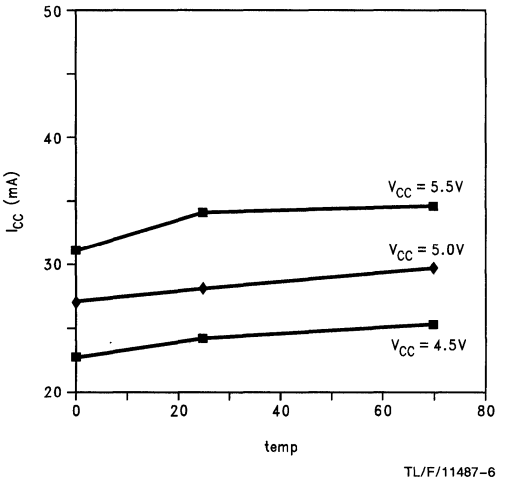


FIGURE 6. DS3886A I_{CC} vs Temperature (All Bn Outputs High)

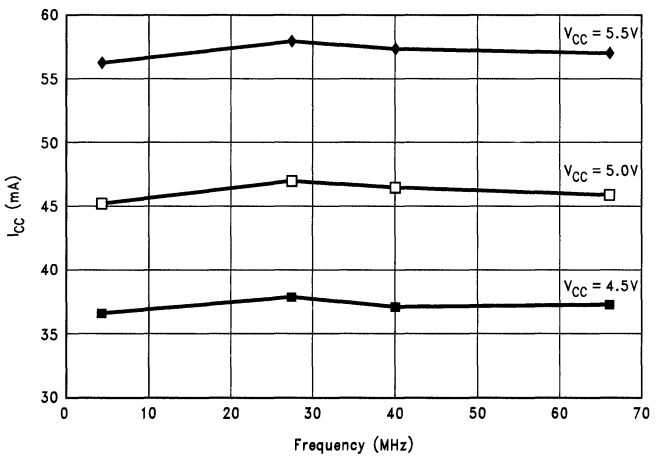


FIGURE 7. DS3886A I_{CC} vs Switching Frequency (A_n to B_n) (All Channels Switching at Room Temperature)

The maximum power dissipation result shown in Table V is 1.315W compared to 1.51W in Table II derived from the standard method. Power calculated using the standard method is 15% higher than actual maximum of 1.315W. I_{OL} of 80 mA and V_{OL} of 1.1V was used in the standard method yielding the higher P_O. The results derived in Table V take into account the Futurebus+ termination specification in the calculation of P_O. There are four typical power calculations in Table IV reflecting different conditions. Typical power varied from 325 mW when all outputs are high to 990 mW when all outputs are low. The typical power calculated in Table II is 1.08W which is 10% higher than that calculated in Table IV. These different power calculations are important when determining the total power of a system. A Futurebus+ backplane may contain several modules. Only one module may transmit data on the bus while others receive. It is important to know how to calculate power dissipation for modules in the transmit mode as well as modules in the receive mode to derive accurate system power.

CALCULATION OF SYSTEM POWER REQUIREMENTS

In a backplane, one board will normally be active and driving the bus while other modules are receiving or in standby. If all lines were asserted, the termination voltage must be able to supply enough current to all the lines. To determine the current requirement from the termination voltage, use this equation;

$$I_{OL} \times \text{Number of Lines} = \text{Termination Current}$$

In a 32-bit Futurebus+ backplane the total number of lines will be 89 which includes all the required lines in addition to the 32-bit address/data lines. The current requirement from the termination supply will be;

$$65\ \text{mA} \times 89\ \text{Lines} = 5.79\text{A}$$

A 64-bit Futurebus+ backplane requires;

$$65\ \text{mA} \times (89 + 32 + 4) = 8.13\text{A}$$

Calculation of typical system power is shown below. Two assumptions are made for the given equation. First, one module transmits while others receive. Second, the transmitting module will have an average duty cycle equal to 50% and running at 20 MHz. Power per bit allows easy calculation of total power for different number of lines. Dividing the total transceiver power by the number of bits on the transceiver will yield power/bit. The total number of modules on the backplane minus one gives the number of receiving modules. The receiving modules will have their outputs in a high state.

(Power/bit with 50% Duty Cycle @ 20 MHz × # of Lines) + (# Boards − 1) (Power/Bit with all Outputs High × # of Lines) = Transceiver System Power

For a 32-bit Futurebus+ Interface with 14 boards the transceiver system power required will be;

$$(725\ \text{mW}/9 \times 89) + (14 - 1)(325\ \text{mW}/9 \times 89) = 49\text{W}$$

CONCLUSION

There are several ways of calculating power dissipation. The results of these calculations will greatly vary depending on the assumptions. An error in calculating output power will be multiplied when extending the results to determine overall system power. A thorough understanding of how to calculate power will yield accurate power calculations. A preferred method of calculating output power is to use the load line intersection point. Typical power dissipation calculation should use duty cycle approximation. Typical device curves are provided with datasheets. Refer to individual datasheets for most up to date information. With this background, the designer will be able to make accurate thermal and power analysis of the interface which may ultimately reduce cost.

Section 16

Mil/Aero

Section 16 Contents

National Semiconductor

Line Drivers and Receivers*
Military Products—Selection Guide

Device No.	Pin Count	Description	Process Flows	Desc SMD/ Slash Sheet*	Package Types
TIA/EIA-232					
DS14C232	16	Dual Line Driver and Receiver	883		CDIP, LCC
DS9616HM	14	Triple Line Driver	883		CDIP, LCC
DS9627M	16	Dual Line Driver	883	5692-8978701MxA	CDIP,LCC
TIA/EIA-422/423					
DS1691A		Single Line Driver	883		CDIP
DS26C31M	16	Quad Line Driver	883, MLS	5962-9163901MxA	CDIP, LCC, FP
DS26C32AM	16	Quad Line Receiver	883, MLS	5962-9164001MxA	CDIP, LCC, FP
DS26F31M	16	Quad Line Driver	883, MLS	5962-7802302MxA	CDIP, LCC, FP
DS26F32M	16	Quad Line Receiver	883, MLS	5962-7802005MxA	CDIP, LCC, FP
DS26LS31M	16	Quad Line Driver	883, MLS	5962-7802301MxA	CDIP, LCC, FP
DS26LS32M	16	Quad Line Receiver	883, MLS		CDIP, LCC, FP
DS26LS33M	16	Quad Line Receiver	883, MLS		CDIP, LCC, FP
DS78C20	14	Dual Line Receiver	883		CDIP
DS78C120	16	Dual Line Receiver	883, MLS		CDIP, FP
DS78LS120	16	Dual Line Receiver	883, MLS		CDIP, FP
DS9636AM	8	Dual Line Driver	883	5962-8752301xA	CDIP
DS9637AM	8	Dual Line Receiver	883	5962-8752401xA	CDIP
DS9638M	8	Dual Line Driver	883, MLS	5962-8754601xA	CDIP
TIA/EIA-485					
DS16F95	8	Single Transceiver	883, MLS	5962-8961501xA	CDIP, LCC, FP
DS96F172M	16	Quad Line Driver	MIL	5962-9076501MxA	CDIP, LCC, FP
DS96F173M	16	Quad Line Receiver	883	5962-9076602MxA	CDIP, LCC, FP
DS96F174M	16	Quad Line Driver	883, MLS	5962-907502MxA	CDIP, LCC, FP
DS96F175M	16	Quad Line Receiver	883, MLS	5962-9076601MxA	CDIP, LCC, FP
GENERAL PURPOSE					
DS1603	14	Dual TRI-STATE Line Receiver	883		CDIP
DS7820	14	Dual Line Receiver	883, MLS		CDIP, FP
DS7820A	14	Dual Line Receiver	883, MLS		CDIP, FP
DS7830	16	Dual Differential Line Driver	883, MLS		CDIP, FP
DS7831	16	Dual Differential TRI-STATE Line Driver	883	8004101xX	CDIP, FP
DS7832	16	Dual Differential TRI-STATE Line Driver	883	8004102xA	CDIP, FP
DS9615M	16	Dual Differential Line Receiver	883, MLS	10404*	CDIP, FP
DS9622M	16	Triple Line Receiver	883	5962-8752201xA	CDIP, LCC, FP
DS55107A	14	Dual Line Receiver	883	10401*	CDIP
DS55113	16	Dual Differential TRI-STATE Line Driver	883		CDIP
DS55122	16	Triple Line Receiver	883		CDIP
MM78C29	14	Quad Single-Ended Line Driver	883		CDIP, FP
MM78C30	14	Dual Differential Line Driver	883		CDIP

* See Datasheets

PACKAGING KEY:

Code	Suffix	Description
CDIP	J, D	Ceramic Dual-in-Line
LCC	E	Leadless Chip Carrier (Ceramic)
FP	W	Flatpak (Dual-in-Line, Ceramic)

National Semiconductor

Bus Circuits*
Military Products—Selection Guide

Device No.	Pin Count	Description	Process Flows	Desc SMD/ Slash Sheet*	Package Types
PI-BUS CIRCUITS					
DS1776	28	8-Bit Transceiver	883		CDIP, LCC
BTL BUS CIRCUITS					
DS3875	68	Arbitration Controller	883		FP
DS3884A	40/44	Handshake Transceiver	883		FP
DS3885	44	Arbitration Transceiver	883		FP
DS3886A	40/44	9-Bit Transceiver	883		FP
GENERAL PURPOSE BUS CIRCUITS					
DP7304B	20	8-Bit Transceiver	MIL		CDIP
DS7633	16	Quad Bus Transceiver	883		CDIP
DS7834	16	Quad Bus Transceiver	883		CDIP
DS7835	16	Quad Bus Transceiver	883		CDIP
DS7836	14	Quad Bus Transceiver	883		CDIP
DS7837	16	Hex Bus Receiver	883		CDIP
DS7838	16	Quad Bus Transceiver	883		CDIP

* See Datasheets

PACKAGING KEY:

Code	Suffix	Description
CDIP	J	Ceramic Dual-in-Line
LCC	E	Leadless Chip Carrier (Ceramic)
FP	W	Flatpak (Dual-in-Line, Ceramic)

Military/Aerospace Programs from National Semiconductor

The following is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *Reliability Handbook.*

MIL-I-38535

National Semiconductor's Mil/Aero Division has received QML approval for the FAB and Assembly sites manufacturing Military Aerospace devices. The following section regarding MIL-M-38510 is undergoing revision and is expected to eventually merge into the MIL-I-38535 QML program. Please contact your local sales office for further details regarding this qualification timeline and status.

TABLE A. QML Marking Code

NS JM38510/33001
BCA 27014QS
Δ ZSSXXYYA

		Legend
NS	=	Corporate Logo
27014	=	Cage Code
Δ	=	ESD Indicator (as applicable)*
Z	=	Assembly Code Location
SS	=	Wafer Fab/Sort Data Code**
XXYY	=	Calendar Year/Seal Week***
Q	=	QML Processing
S	=	Test Location

***ESD Indicator Codes**

Mark	Class	Voltage
Δ	1	0-1999V
ΔΔ	2	2000–3999V
——	3	≥ 4000V

****Assembly Code Locations**

Country	Code
Bangkok	B
Combined Country of Origin	C
Cebu Philippines	D
Hong Kong	K
Indy Electronics	W
Japan	J
Korea	E
Malacca	M
Mountain View	V
Pantronix	A
Penang	P
Philippines	H
Puyallup	G
Salt Lake	L
Santa Clara	F
Singapore	S
South Portland	Z
Taiwan	T
Tucson	Y
United Kingdom	U
Outside Vendor	N

*****Calendar/Seal Week Codes**

2nd digit: Last digit of the year wafer sort was performed

3rd digit: Alpha character indicating the calendar quarter in which wafer sort was performed.

Character	Months	Weeks
A	Jan–Mar	13
B	April–June	14–26
C	July–Sept	27–39
D	Oct–Dec	40–53
GF	Prior to 1988	

4th & 5th digits: Calendar Year

6th & 7th digits: Sealweek

8th digit: Alphacharacter indicating the lot is a sublot (when applicable).

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

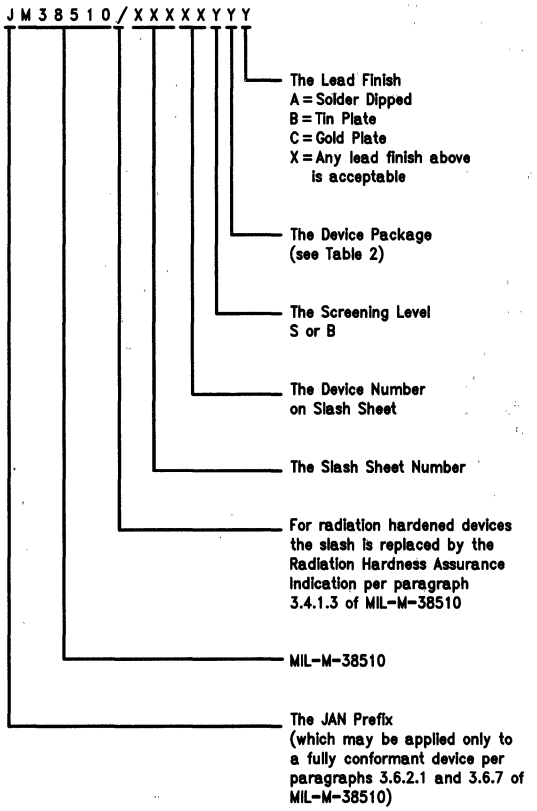
There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table 3.

Tables 1 and 2 explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

TABLE I. The MIL-M-38510 Part Marking



TL/XX/0113-1

MIL-M-38510 (Continued)

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4" x 1/4" (Metal) Flatpack
B	14-Pin 3/16" x 1/4" (Metal) Flatpack
C	14-Pin 1/4" x 3/4" Dual-In-Line
D	14-Pin 1/4" x 3/8" (Ceramic) Flatpack
E	16-Pin 1/4" x 7/8" Dual-In-Line
F	16-Pin 1/4" x 3/8" (Metal or Ceramic) Flatpack
G	8-Pin TO-99 Can or Header
H	10-Pin 1/4" x 1/4" (Metal) Flatpack
I	10-Pin TO-100 Can or Header
J	24-Pin 1/2" x 1 1/4" Dual-In-Line
K	24-Pin 3/8" x 5/8" Flatpack
L	24-Pin 1/4" x 1 1/4" Dual-In-Line
M	12-Pin TO-101 Can or Header
N	(Note 1)
P	8-Pin 1/4" x 3/8" Dual-In-Line
Q	40-Pin 3/16" x 2 1/16" Dual-In-Line
R	20-Pin 1/4" x 1 1/16" Dual-In-Line
S	20-Pin 1/4" x 1/2" Flatpack
T	(Note 1)
U	(Note 1)
V	18-Pin 3/8" x 15/16" Dual-In-Line
W	22-Pin 3/8" x 1 1/8" Dual-In-Line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-Terminal 0.350" x 0.350" Chip Carrier
3	28-Terminal 0.450" x 0.450" Chip Carrier

Note 1: These letters are assigned to packages by individuals MIL-M-38510 detail specifications and may be assigned to different packages in different specifications.

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales representatives, of DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision D of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883, but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product, but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

Reliability Electrical Test Specifications (RETS)

National has implemented the first realtime, electronic catalog of military test specifications called RETS.

Included in this computerized directory is a detailed listing of the electrical tests performed on all military devices qualified by National, including forcing functions, test limits and temperature ranges.

Call your local National sales office for essential up-to-the-minute information on device testing.

TABLE III. Classes S and B Screening*

Screen	Class S		Class B	
	Method	Reqt	Method	Reqt
3.1.1 Wafer Lot Acceptance (Note 1)	5007	All Lots		
3.1.2 Nondestructive Bond Pull	2023	100%		
3.1.3 Internal Visual (Note 2)	2010, Test Condition A	100%	2010, Test Condition B	100%
3.1.4 Temperature Cycling (Note 3)	1010, Test Condition C	100%	1010, Test Condition C	100%
3.1.5 Constant Acceleration	2001, Test Condition E (Min) Y_1 Orientation Only	100%	2001, Test Condition E (Min) Y_1 Orientation Only	100%
3.1.6 Visual Inspection (Note 4)		100%		100%
3.1.7 Particle Impact Noise Detection (PIND)	2020, Test Condition A	100% (Note 5)		
3.1.8 Serialization		100% (Note 6)		
3.1.9 Pre Burn-In Electrical Parameters	In accordance with Applicable Device Specification	100% (Note 7)	In accordance with Applicable Device Specification	100% (Note 8)
3.1.10 Burn-In Test	1015 (Note 9) 240 Hours at 125°C Minimum	100%	1015 160 Hours at 125°C Minimum	100%
3.1.11 Interim (Post-Burn-In) Electrical Parameters	In accordance with Applicable Device Specification	100% (Note 7)		
3.1.12 Reverse Bias Burn-In (Note 10)	1015; Test Condition A or C, 72 Hours at 150°C Minimum	100%		
3.1.13 Interim (Post Burn-In) Electrical Parameters	In accordance with Applicable Device Specification	100% (Note 7)	In accordance with Applicable Device Specification	100% (Note 8)
3.1.14 Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters at 25°C	All Lots	5%	All Lots
3.1.15 Final Electrical Test	In accordance with Applicable Device Specification		In accordance with Applicable Device Specification	
a. Static Tests				
1. 25°C (Subgroup 1, Table I, 5005)		100%		100%
2. Maximum and Minimum Rated Operating Temperature (Subgroups 2, 3, Table I, 5005)		100%		100%
b. Dynamic or Functional Tests (Note 11)				
1. 25°C (Subgroup 4 or 7, Table I Method 5005)		100%		100%
2. Minimum and Maximum Rated Operating Temperature (Subgroups 5 and 6, or 8, Table I Method 5005)		100%		100%
c. Switching Tests 25°C (Subgroup 9, Table I, Method 5005)		100%		100%

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

TABLE III. Classes S and B Screening* (Continued)

Screen	Class S		Class B	
	Method	Reqt	Method	Reqt
3.1.16 Seal a. Fine b. Gross	1014	100% (Note 12)	1014	100% (Note 12)
3.1.17 Radiographic (Note 13)	2012 Two Views (Note 14)	100%		
3.1.18 Qualification or Quality Conformance Inspection Test Sample Selection		(Note 15)		(Note 15)
3.1.19 External Visual (Note 16)	2009	100%	2009	100%
3.1.20 Radiation Latch-Up (Note 17)	1020	100%	1020	100%

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: All lots shall be selected for testing in accordance with the requirements of Method 5007 herein.

Note 2: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam).

Note 3: For Class B devices, this test may be replaced with thermal shock Method 1011, test condition A, minimum.

Note 4: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 5: See MIL-I-38535, 40.6.3. The PIND test may be performed in any sequence after 3.1.4 and prior to 3.1.13.

Note 6: Class S devices shall be serialized prior to initial electrical parameter measurements.

Note 7: Post burn-in electrical parameters shall be read and recorded (see 3.1.13, subgroup 1). Pre burn-in or interim electrical parameters (see 3.1.9 and 3.1.11) shall be read and recorded only when delta measurements have been specified as part of post burn-in electrical measurements.

Note 8: When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delta calculations.

Note 9: Dynamic burn-in only. Test condition F of Method 1015 shall not apply.

Note 10: Reverse bias burn-in (see 3.1.12) is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim electrical parameter measurements 3.1.11 are omitted. The order of performing the burn-in (see 3.1.10) and the reverse bias burn-in may be inverted.

Note 11: Functional tests shall be conducted at input test conditions as follows:
$V_{IH} = V_{IH}(min) + 20\%, -0\%$; $V_{IL} = V_{IL}(max) + 0\%, -50\%$; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.
CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(min)$ and $V_{IL}(max)$ requirements are not violated at the device terminals.

Note 12: For Class B devices, the fine and gross seal tests (3.1.16) shall be performed separately or together, between constant acceleration (3.1.5) and external visual (3.1.19). For class S devices, the fine and gross seal tests (3.1.16) shall be performed separately or together, between final electrical testing (3.1.15) and external visual (3.1.19). In addition, for classes S and B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal (3.1.16) or external visual (3.1.19) shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (Method 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (Method 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal (3.1.16), but before external visual (3.1.19) if the devices are installed in individual carriers during electrical test.

Note 13: The radiographic (see 3.1.17) screen may be performed in any sequence after 3.1.8.

Note 14: Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides.

Note 15: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005. See 3.5 of Method 5005.

Note 16: External visual shall be performed on the lot any time after 3.1.17 and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing. Exposed underplate or base metal on leads of hard glass seals, bead seals, or individual feedthrough seals due to acceptable glass meniscus chipouts shall not be considered rejectable provided salt atmosphere test requirements (Method 1009) are met in accordance with applicable group D requirements. Acceptable glass meniscus chipouts are defined as chipouts in the glass meniscus that are located within the region one-half the distance from the lead to the case.

Note 17: Radiation latch-up screen shall be conducted when specified in purchase order or contract. Latch-up screen is note required for SOS, SIO, and DI technology when latch-up is physically not possible. At the manufacturer's option, latch-up screen may be conducted at any screening operation step after seal.

TABLE IV. Group A Electrical Tests for Classes S and B Devices* (Note 1)

Subgroups (Note 2) Quality/Accept No. = 116/0 (Notes 3 to 5)
Subgroup 1 Static Tests at 25°C
Subgroup 2 Static Tests at Maximum Rated Operating Temperature
Subgroup 3 Static Tests at Minimum Rated Operating Temperature
Subgroup 4 Dynamic Tests at 25°C
Subgroup 5 Dynamic Tests at Maximum Rated Operating Temperature
Subgroup 6 Dynamic Tests at Minimum Rated Operating Temperature
Subgroup 7 Functional Tests at 25°C
Subgroup 8A Functional Tests at Maximum Rated Operating Temperatures
Subgroup 8B Functional Tests at Minimum Rated Operating Temperatures
Subgroup 9 Switching Tests at 25°C
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

Note 2: At the manufacturer's option, the applicable tests required for Group A testing (see Note 1) may be conducted individually or combined into sets of tests, subgroups (as defined in Table I), or sets of subgroups. However, the munufacturer shall predesignate these groupings prior to Group A testing. Unless otherwise specified, the individual tets, subgroups, or sets of tests/subgroups may be performed in any sequence.

Note 3: The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as predesignated in Note 2, shall be 116/0.

Note 4: A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

Note 5: If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class S only, if this testing results in a percent defective greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

TABLE V. Group B Tests for Class S Devices* (Note 1)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1			
a. Physical Dimensions (Note 2)	2016		2(0)
b. Internal Water-Vapor Content (Notes 2 and 3)	1018	5,000 ppm Maximum Water Content at 100°C	3(0) or 5(1) (Note 4)
Subgroup 2 (Note 5)			
a. Resistance to Solvents	2015		3(0)
b. Internal Visual and Mechanical	2013, 2014	Failure Criteria from Design and Construction Requirements of Applicable Acquisition Document	2(0)
c. Bond Strength	2011		LTPD = 10 (Note 6)
1. Thermocompression		1. Test Condition C or D	
2. Ultrasonic		2. Test Condition C or D	
3. Flip-Chip		3. Test Condition F	
4. Beam Lead		4. Test Condition H	
d. Die Shear Test or Substrate Attach Strength Test		In accordance with Method 2019 or 2027 for the Applicable Die Size	3(0)
Subgroup 3			
Solderability (Note 7)	2003 or 2022	Soldering Temperature of 245°C ±5°C	LTPD = 10
Subgroup 4 (Note 2)			LTPD = 5
a. Lead Integrity (Note 8)	2004	Test Condition B_2, Lead Fatigue	
b. Seal	1014	As applicable	
1. Fine			
2. Gross			
c. Lid Torque (Note 9)	2024	As applicable	
Subgroup 5 (Note 10)			LTPD = 5
a. End-Point Electrical Parameters (Note 11)		As Specified in the Applicable Device Specification	
b. Steady State Life (Note 12)	1005	Test Condition C, D, or E	
c. End-Point Electrical Parameter (Note 11)		As specified in the applicable device specification	
Subgroup 6			LTPD = 15
a. End-Point Electrical Parameters		As specified in the Applicable Device Specification	
b. Temperature Cycling	1010	Condition C, 100 Cycles Minimum	
c. Constant Acceleration	2001	Test Condition E: Y1 Orientation Only	
d. Seal	1014		
1. Fine			
2. Gross			
e. End-Point Electrical Parameters		As Specified in the Applicable Device Specification	
Subgroup 7 (Note 13)			

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Electrical reject devices from that same inspection lot may be used for all subgroups when end-point measurements are not required, provided that the rejects are processed identically to the inspection lot through pre burn-in electricals and provided the rejects are exposed to the full temperature/time exposure of burn-in.

Note 2: Not required for qualification or quality conformance inspections where Group D inspection is being performed on samples from the same inspection lot.

Note 3: This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed Method 1018, procedure 3 shall be used. See Note 6 of Table IV.

Note 4: Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., three or five devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

Note 5: Resistance to solvents testing required only on devices using inks or paints as a marking medium.

Note 6: Unless otherwise specified, the LTPD sample size for conditions C and D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds).

Note 7: All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

TABLE V. Group B Tests for Class S Devices* (Note 1) (Continued)

Note 8: The LTPD of 5 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of three devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable (see Note 9), in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use Method 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a LTPD of 15 based on the number of pads tested taken from three devices minimum. Seal test (subgroup 4b) need be performed only on packages having leads exiting through a glass seal.

Note 9: Lid torque test shall apply only to glass-frit-sealed packages.

Note 10: The alternate removal-of-bias provisions of 3.3.1 of Method 1005 shall not apply for test temperature above +125°C.

Note 11: Read and record group A subgroups 1, 2, and 3.

Note 12: The same test temperature that was used for burn-in shall be used for the steady-state life test.

Note 13: Subgroup 7 has been deleted from Table V. The requirements for ESD testing are specified in MIL-M-38510.

TABLE VI. Group B Tests for Class B* (Notes 1 and 2)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 2 (Note 3) a. Resistance to Solvents	2015		3 (0)
Subgroup 3 a. Solderability (Note 4)	2003 or 2022	Soldering Temperature of 245°C ±5°C	10
Subgroup 5 a. Bond Strength (Note 5) 1. Thermocompression 2. Ultrasonic or Wedge 3. Flip-Chip 4. Beam Lead	2011	 1. Test Condition C or D 2. Test Condition C or D 3. Test Condition F 4. Test Condition H	15

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electricals and provided the rejects are exposed to the full temperature/time exposure of burn-in.

Note 2: Subgroups 1, 4, 6, 7, and 8 have been deleted from this table. For convenience, the remaining subgroups will not be renumbered.

Note 3: Resistance to solvents testing required only on devices using inks or paints as the marking or contrast medium.

Note 4: All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin fusing after burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

Note 5: Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in Method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of four devices, and for condition F or H is the number of dice (not bonds) (see Method 2011).

TABLE VII. Group C (Die-Related Tests) (For Class B Only)*

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1			
a. Steady-State Life Test	1005	Test Condition to be Specified (1,000 Hours at 125°C or Equivalent in Accordance with Table I)	5
b. End-Point Electrical Parameters		As specified in the Applicable Device Specification	

TABLE VIII. Group D (Package-Related Tests for All Classes)*

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (Note 2)			
a. Physical Dimensions	2016		15
Subgroup 2 (Note 2)			
a. Lead Integrity (Note 3)	2004	Test Condition B_2 (Lead Fatigue)	5
b. Seal (Note 4)			
1. Fine	1014	As Applicable	
2. Gross			
Subgroup 3 (Note 5)			
a. Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum	15
b. Temperature Cycling	1010	Test Condition C, 100 Cycles Minimum	
c. Moisture Resistance (Note 6)	1004		
d. Visual Examination		In accordance with visual criteria of Method 1004 and 1010	
e. Seal	1014	As Applicable	
1. Fine			
2. Gross (Note 7)			
f. End-point Electrical Parameters (Note 8)		As specified in the Applicable Device Specification	
Subgroup 4 (Note 5)			
a. Mechanical Shock	2002	Test Condition B Minimum	15
b. Vibration, Variable Frequency	2007	Test Condition A Minimum	
c. Constant Acceleration	2001	Test Condition E Minimum (See Note 3), Y_1 Orientation Only	
d. Seal	1014	As Applicable	
1. Fine			
2. Gross			
e. Visual Examination	(Note 9)		
f. End-Point Electrical Parameters		As Specified in the Applicable Device Specification	
Subgroup 5 (Note 2)			
a. Salt Atmosphere (Note 6)	1009	Test Condition A Minimum	15
b. Visual Examination		In accordance with visual criteria of Method 1009	
c. Seal	1014	As Applicable	
1. Fine			
2. Gross (Note 7)			
Subgroup 6 (Note 2)			
a. Internal Water-Vapor Content	1018	5,000 ppm Maximum Water Content at 100°C	3(0) or 5(1) (Note 10)
Subgroup 7 (Note 2)			
a. Adhesion of Lead Finish (Notes 11 and 12)	2025		15
Subgroup 8			
a. Lid Torque (Notes 2 and 13)	2024		5 (0)

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: In-line monitor data may be substituted for subgroups D1, D2, D6, D7 and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. This in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

Note 2: Electrical reject devices from that same inspection lot may be used for samples.

TABLE VIII. Group D (Package-Related Tests for All Classes) (Continued)

Note 3: The LTPD of 5 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of three devices. All devices required for the lead integrity test shall pass the seal test if applicable (see Note 4) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use Method 2028. For leadless chip carrier packages only, use test condition D and an LTPD of 15 based on the number of pads tested taken from three devices minimum.

Note 4: Seal test (Subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

Note 5: Devices used in Subgroup 3, "Thermal and Moisture Resistance" may be used in Subgroup 4, "Mechanical".

Note 6: Lead bend stress initial conditioning is not required for leadless chip carrier packages.

Note 7: After completion of the required visual examinations and prior to submittal to Method 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

Note 8: At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

Note 9: Visual examination shall be in accordance with Method 1010 or 1011.

Note 10: Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., three or five devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

Note 11: The adhesion of lead finish test shall not apply for leadless chip carrier packages.

Note 12: LTPD based on number of leads.

Note 13: Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

TABLE IX. Group E (Radiation Hardness Assurance Tests)* (Note 1)

Test	MIL-STD-883		Class S		Class B	
	Method	Condition	Quantity/Accept Number	Notes	Quantity/Accept Number	Notes
Subgroup 1 (Note 2)						
Neutron Irradiation	1017	25°C				
a. Qualification			a. 11(0)	(Note 3)	a. 11(0)	(Note 4)
b. QCI			b. 11(0)	(Note 3)	b. 11(0)	(Note 4)
Endpoint Electrical Parameters		As specified in accordance with detail specification				
Subgroup 2 (Note 5)						
Steady-State Total Dose Irradiation	1019	25°C, Maximum Supply Voltage				
a. Qualification			a. 4(0) 2(0)	a. (Note 6) (Note 8)	a. 22(0)	(Note 7)
b. QCI			b. 4(0) 2(0)	b. (Note 6) (Note 8)	b. 22(0)	(Note 7)
Endpoint Electrical Parameters		As specified in accordance with detail specification				
Subgroup 3 (Note 9)						
Transient						
Ionizing	1021	25°C	11(0)	(Note 3)	11(0)	(Note 4)
Irradiation	1023	25°C				
Endpoint Electrical Parameters		As specified in accordance with detail specification				

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. Total exposure shall not be considered cumulative unless testing is performed within the time limits of the test method. Group E tests may be performed prior to device screening.

Note 2: Waive neutron tests for MOS devices where neutron susceptability is less than 10^{13} neutrons/cm^2 (e.g. charge coupled devices, BICMOS, etc.). When testing is required, the limit for neutron fluence shall be 2×10^{12} neutrons/cm^2.

Note 3: In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

Note 4: In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

Note 5: Class B devices shall be inspected using either the class B quantity/accept number criteria as specified, or by using the class S criteria on each wafer.

Note 6: In accordance with wafer for device types with less than or equal to 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius, and spaced uniformly around this radius.

Note 7: In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

Note 8: In accordance with wafer for device types with greater than 4,000 equivalent transistors/chip selected from the wafer at a radius approximately equal to two-thirds of the wafer radius and spaced uniformly around this radius.

Note 9: Upset testing during qualification on first QCI shall be conducted when specified in purchase order or contract. When specified, the same microcircuits may be tested in more than one subgroup.

TABLE X. Wafer Lot Acceptance Tests*

Test	Conditions (Note 1)	Limits (Note 3)	Sampling Plan
1. Wafer Thickness	MIL-STD-977 Method 1580. Measurement shall be performed after final lap or polish. All readings shall be recorded. (Note 2)	Maximum deviation of ±2 mil from approved design nominal 6 mil minimum.	Two wafers per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
2. Metallization Thickness	MIL-STD-977 Method 5500. All readings shall be recorded.	a. Conductor: 8 kÅ minimum for single level metal and for the top level of multi-level metal; 5 kÅ minimum for lower levels, with a maximum deviation of ±20% from the approved design nominal. b. Barrier: Maximum deviation of ±30% from the approved design nominal.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.
3. Thermal stability (applicable to: All linear; all MOS; all bipolar digital operating at 10V or more)	MIL-STD-977, Method 2500. Record V_{FB} or V_T.	a. ΔV_{FB} or $\Delta V_T \leq 0.75$, normalized to an oxide thickness of 1000Å for bipolar digital devices operating at 10V or greater and all bipolar linear devices not containing MOS transistor(s). The monitor shall have an oxide and shall be metallized with the lot. b. ΔV_{FB} or $\Delta V_T \leq 1.0V$, normalized to an oxide thickness of 1,000Å for bipolar linear devices that operate above 5V and containing MOS transistor(s), and digital devices that operate above 10V and containing MOS structures. The V_{FB} limit shall not be exceeded by the sum of the absolute values of the MOS oxide transistors and the metallization Δ. The monitor(s) shall be oxidized and metallized with the lot. Separate monitors may be used for this test. c. ΔV_{FB} or $V_T \leq 0.4V$, normalized to an oxide thickness of 1,000Å for MOS devices. A monitor consisting of a gate oxide metallized with the lot shall be used.	One wafer (or monitor) per lot. Reject lot if measurement exceeds limits or revert to test of each wafer.

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Approved equivalent test methods may be used in lieu of the MIL-STD-977 reference method.

Note 2: This test is not required when the finished wafer design thickness is greater than 10 mil.

Note 3: Approved design nominal values or tolerances shall be submitted for line certification in accordance with DESC-EQM-42.

TABLE X. Wafer Lot Acceptance Tests* (Continued)

Test	Conditions (Note 1)	Limits (Note 3)	Sampling Plan
4. SEM	MIL-STD-883, Method 2018.	MIL-STD-883, Method 2018.	MIL-STD-883, Method 2018. Lot acceptance basis.
5. Glassivation thickness	MIL-STD-977, Method 5500. All readings shall be recorded.	6 kÅ minimum for SiO_2 and 2 kÅ for Si_3N_4 with maximum deviation of $\pm 20\%$ from approved design nominal.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.
6. Gold backing thickness (When applicable)	MIL-STD-977, Method 5500. All readings shall be recorded.	In accordance with approved design nominal thickness and tolerance.	One wafer (or monitor) per lot. Reject lot if any measurement exceeds limits or revert to test of each wafer.

***Note:** These requirements are per MIL-STD-883 Revision D, notice 1 dated June 1, 1993. All requirements are subject to change of the latest revision of MIL-STD-883.

Note 1: Approved equivalent test methods may be used in lieu of the MIL-STD-977 reference method.

Note 2: This test is not required when the finished wafer design thickness is greater than 10 mil.

Note 3: Approved design nominal values or tolerances shall be submitted for line certification in accordance with DESC-EQM-42.

Section 17

Appendices and Physical Dimensions

Section 17 Contents

National Semiconductor

Interface
Tape and Reel Availability

Line Drivers and Receivers

DS1488MX	DS26C32ATMX
DS14C88MX	DS3486MX
DS14C88TMX	DS34C86TMX
DS1489MX	DS3487MX
DS1489AMX	DS34C87TMX
DS14C89AMX	DS3650MX
DS14C89ATMX	DS3691MX
DS14185WMX	DS3691VX
DS14C232CMX	DS3695AMX
DS14C232CWMX	DS3695ATMX
DS14C232TMX	DS36F95MX
DS14C232TWMX	DS3696AMX
DS14C237WMX	DS36276MX
DS14C237TWMX	DS36277TMX
DS14C238WMX	DS36C278MX
DS14C238TWMX	DS36C278TMX
DS14C239WMX	DS36C279MX
DS14C239TWMX	DS36C279TMX
DS14C241WMX	DS36C280MX
DS14C241TWMX	DS36C280TMX
DS14C335MSAX	DS36950VX
DS14C535MSAX	DS36954MX
DS26LS31CMX	DS36954VX
DS26C31TMX	DS75107AMX
DS26LS32ACMX	DS75107MX
DS26LS32CMX	DS75108MX
DS26LS33ACMX	DS75110AMX

DS75113MX	DS90CR281MTDX
DS75150MX	DS90CR282MTDX
DS75154MX	DS90CR561MTDX
DS75176BMX	DS90CR562MTDX
DS75176BTMX	DS90CF561MTDX
DS8921MX	DS90CF562MTDX
DS8921AMX	DS90CR581MTDX
DS8921ATMX	DS90CR582MTDX
DS89C21TMX	DS90CF581MTDX
DS89LV21TMX	DS90CF582MTDX
DS8922MX	**Bus Circuits**
DS8922AMX	
DS8923MX	DS3662WMX
DS8923AMX	DS3862WMX
DS8925MX	DS3883AVX
DS8933MX	DS3884AVX
DS8934WMX	DS3886AVX
DS8935WMX	DS3892MX
DS9637ACMX	DS3893AVX
DS9638CMX	DS3896MX
DS90C031TMX	DS3897MX
DS90LV031TMX	DS75160AWMX
DS90C032TMX	DS75162AWMX
DS90LV032TMX	DS26S10CVX
DS90CR211MTDX	DS8837MX
DS90CR212MTDX	DS8838MX

Note: "X" suffix designates tape and reel.

Tube/Tape and Reel Quantities

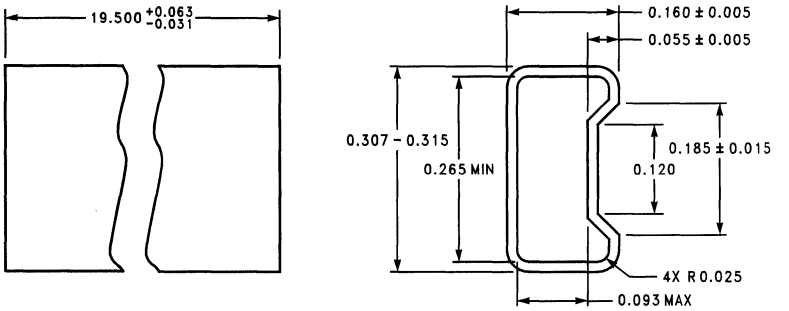
Package Code	Package Description	Package Number	Immediate Container Quantity	
			Tube/Rail	Tape and Reel
M	Small Outline Package, JEDEC (SOIC)	M14A	55	2500
M		M16A	48	2500
WM		M20B	36	1000
WM		M24B	30	1000
SJ	Small Outline Package, EIAJ (SOP)	M14D	47	2000
SJ		M16D	47	2000
SJ		M20D	38	2000
QSC	Shrink Small Outline Package, JEDEC (QSOP or JEDEC SSOP)	MQA20	54	2500
QSC		MQA24	54	2500
MSA	Shrink Small Outline Package, EIAJ, Type II (SSOP II)	MSA20	66	2000
MSA		MSA24	58	2000
MSC	Shrink Small Outline Package, EIAJ, Type I (SSOPI)	MSC14	Not Available	2000
MSC		MSC16	Not Available	2000
MSC		MSC20	Not Available	2000
MTC	Thin Shrink Small Outline Package, JEDEC, 4.4mm (TSSOP)	MTC14	94	2500
MTC		MTC16	94	2500
MTC		MTC20	73	2500
MTC		MTC24	61	2500
MEA	Shrink Small Outline Package (SSOP)	MS48A	29	1000
MEA		MS56A	25	1000
MTD	Thin Shrink Small Outline Package, 6.1mm (TSSOP)	MTD48	39*	1000
MTD		MTD56	35*	1000

*FPD-Link and Channel-Link Devices.

Tube Specifications and Drawings

14/16 Lead SOIC, JEDEC and QSOP

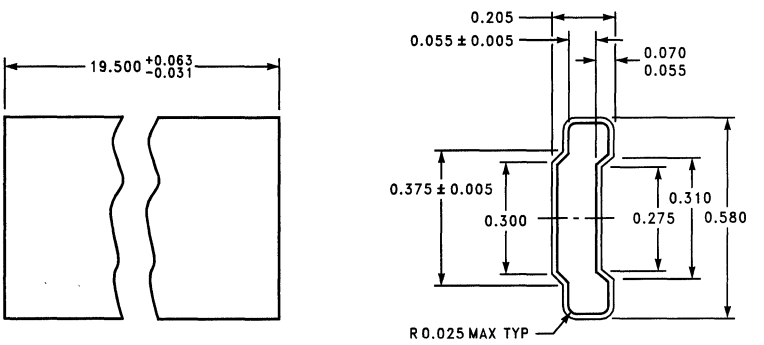
Package Number: M14A, M16A, MQA20, MQA24



TL/F/12657–1

20/24 Lead SOIC, JEDEC

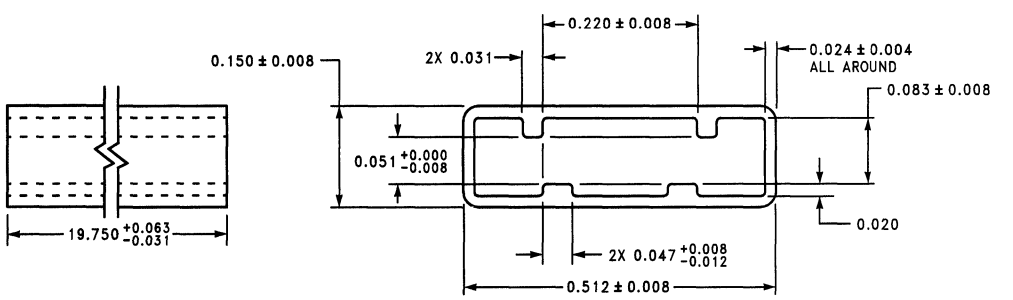
Package Number: M20B, M24B



TL/F/12657–2

SOP, EIAJ and SSOP II, EIAJ

Package Number: M14D, M16D, M20D, MSA20, MSA24



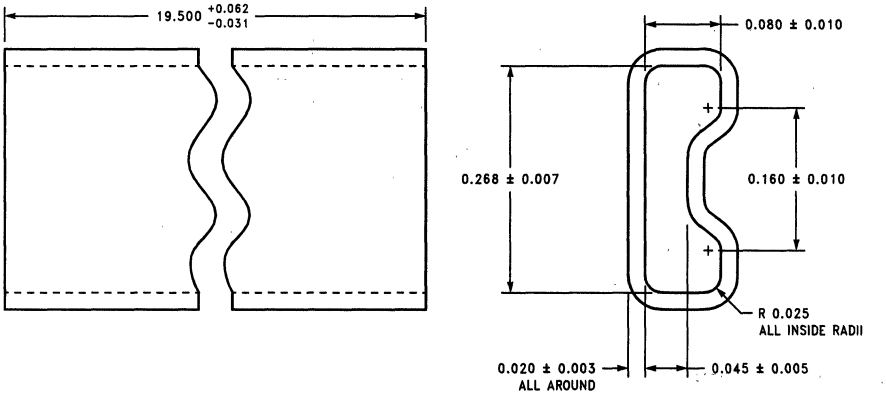
TL/F/12657–3

17

Tube Specifications and Drawings (Continued)

TSSOP, JEDEC, 4.4 mm Body Width

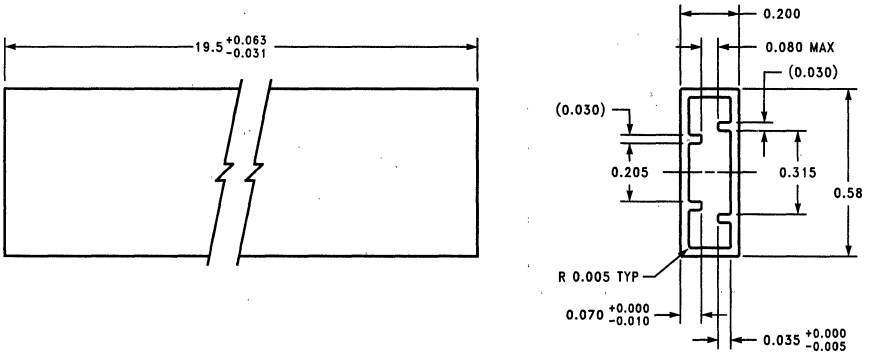
Package Number: MTC14, MTC16, MTC20 and MTC24



TL/F/12657–4

SSOP

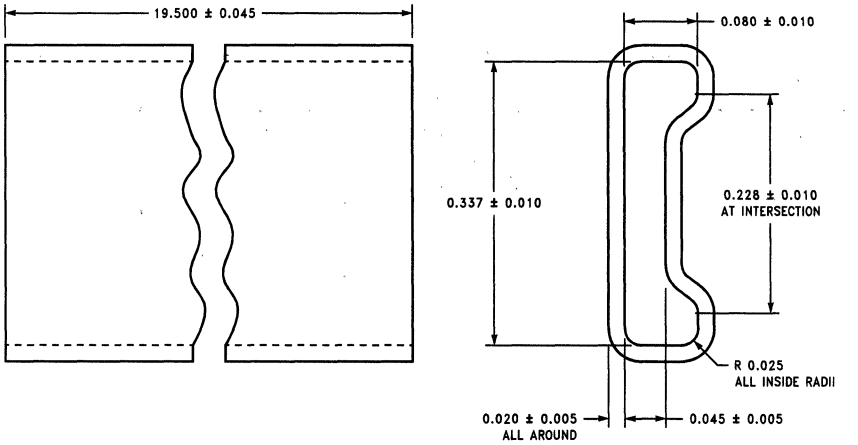
Package Number: MS48A, MS56A



TL/F/12657–5

TSSOP

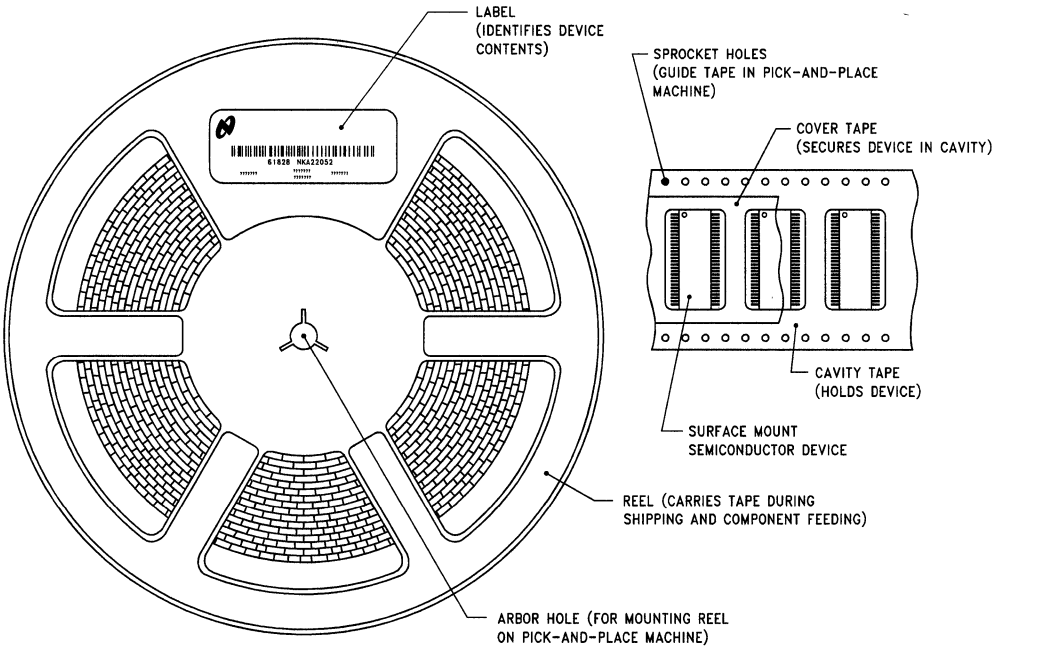
Package Number: MTD48, MTD56



TL/F/12657–6

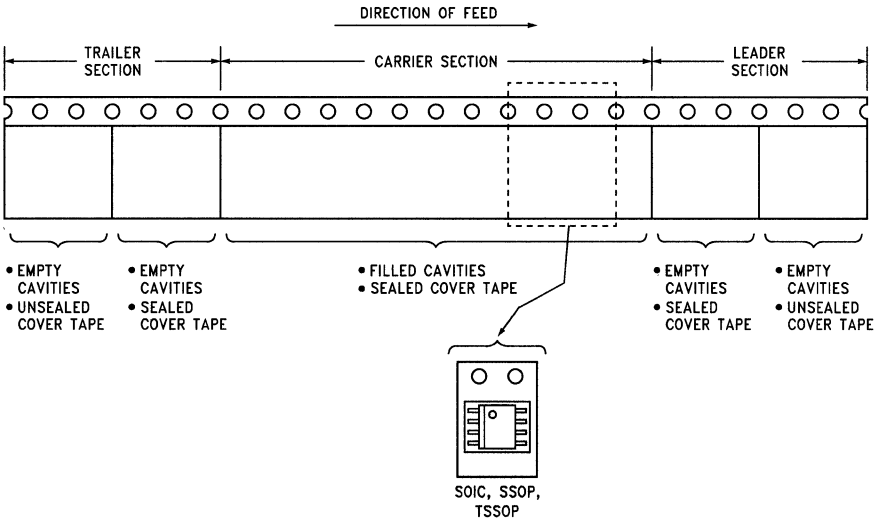
Tape and Reel Overview and Technical Information

Tape and Reel Diagram



TL/F/12657–7

Tape Format and Device Orientation



TL/F/12657–8

Tape and Reel Overview and Technical Information (Continued)

MATERIALS

- Cavity Tape: Static Dissipative PVC or Polystyrene
- Cover Tape: Static Dissipative Polyester or Polyethylene
- Reel: Static Dissipative PVC or Polystyrene
- Surface Resistivity: 10^5 Ω/□ to less than 10^{12} Ω/□ all materials.

COVER TAPE PEEL STRENGTH

- The force required to peel off the cover tape from the carrier tape will fall within the range of 0.1 Newton to 1.3 Newton (10 grams to 130 grams) at a peeling speed of 300 mm per minute. This complies with the EIA standard.

TAPE STORAGE

- It is recommended that the sealed tape be stored in conditions where the environment does not exceed:
  - → Temperature: 40°C maximum
  - → Relative humidity: 90% maximum
  - → No direct exposure to sunlight.

ELECTROSTATIC CHARGES

National Semiconductor uses only static dissipative tape and reel materials (surface resistivity of $10^5\Omega$ to 10^{12} Ω/□) to avoid damaging static charges building up during the peeling off of the cover tape prior to pick and place. National Semiconductor ran extensive evaluations on cover tape materials and found that static charge build up was very low (less than 200V) on static dissipative cover tapes. In comparison, commonly used insulative cover tapes had readings consistently in excess of 3000V.

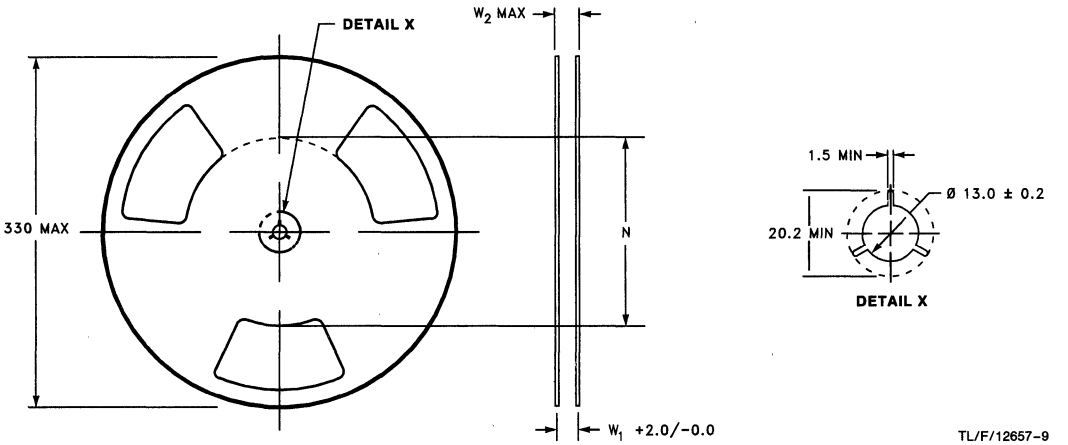
DRYPACK (also applies to tube shipments)

Packages susceptible to package cracking during the surface mount reflow process are drypacked to minimize moisture absorption during shipping and storage. Once dry bags have been opened, packages must be surface mounted within the specified time printed on the bags. If this time limit is exceeded, the parts must be baked prior to reflow. The baking requirement is also printed on the bag.

Currently, the packages that are drypacked are:

- SSOP-48
- SSOP-56
- TSSOP-48
- TSSOP-56

REEL Specifications and Drawings (All dimensions in millimeters)



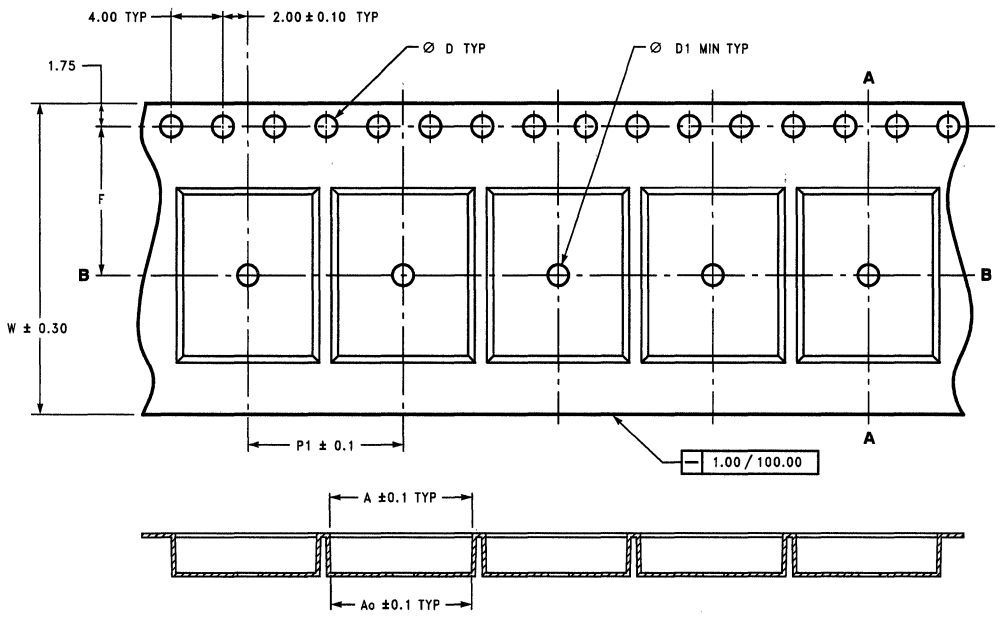
TL/F/12657–9

Plastic 330mm (13") Reel Dimensions for 12mm, 16mm, 24mm and 32mm Tape

Tape Size	Package Drawing	N (Typical)	W1	W2 (Max)
12mm	MTC14 MTC16	178	12.4	18.4
16mm	M14A M16A MQA20 MQA24 MSA20 MSA24 MTC20 MTC24	178	12.4	22.4
16mm	MSC14 MSC16 MSC20	80	12.4	22.4
16mm	M14D M16D	100	12.4	22.4
24mm	M20B M24B M20D MTD48 MTD56	178	12.4	30.4
32mm	MS48A MS56A	100	12.4	38.4

Tape Specifications and Drawings

SOIC, SOP, QSOP, SSOP II, SSOP I



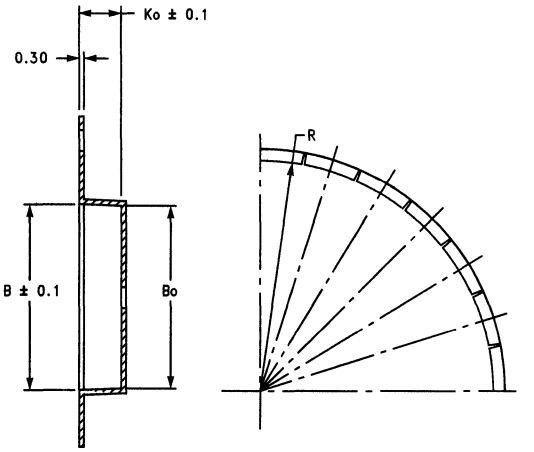
SECTION B – B

TL/F/12657–10

Package Code	Package Description	Package Number	W	F	D	D1	P1	A	A0
M	Small Outline Package, JEDEC (SOIC)	M14A	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
M		M16A	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
WM		M20B	24.0	11.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	12.0	11.08	10.9
WM		M24B	24.0	11.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	12.0	11.10	10.9
SJ	Small Outline Package, EIAJ (SOP)	M14D	16.0	7.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.5	12.0	8.70	8.4
SJ		M16D	16.0	7.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.5	12.0	8.80	8.4
SJ		M20D	24.0	11.5 ± 0.05	ϕ1.55 ± 0.05	ϕ1.5	12.0	8.70	8.4
QSC	Shrink Small Outline Package, JEDEC (QSOP or JEDEC SSOP)	MQA20	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
QSC		MQA24	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0	6.65	6.5
MSA	Shrink Small Outline Package, EIAJ, Type II (SSOP II)	MSA20	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0		8.6
MSA		MSA24	16.0	7.5 ± 0.1	ϕ1.55 ± 0.05	ϕ1.5	8.0		8.6
MSC	Shrink Small Outline Package, EIAJ, Type I (SSOP I)	MSC14	16.0	7.5 ± 0.1	ϕ1.50 + 1/-0	ϕ1.6	8.0		6.8
MSC		MSC16	16.0	7.5 ± 0.1	ϕ1.50 + 1/-0	ϕ1.6	8.0		6.8
MSC		MSC20	16.0	7.5 ± 0.1	ϕ1.50 + 1/-0	ϕ1.6	8.0		6.8

Tape Specifications and Drawings (Continued)

SOIC, SOP, QSOP, SSOP II, SSOP I (Continued)



SECTION A–A **BEND RADIUS**

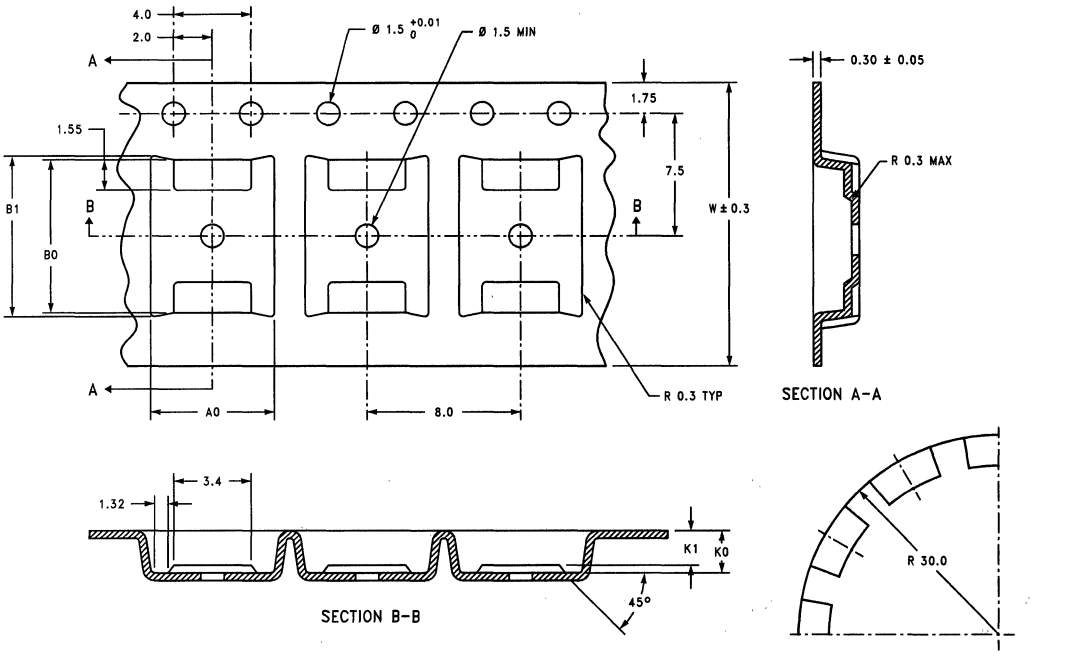
SMALLEST ALLOWABLE BENDING RADIUS.

TL/F/12657–11

Package Code	Package Description	Package Number	B0	B	K0	R
M	Small Outline Package, JEDEC (SOIC)	M14A	9.5	9.65	2.1	30.00
M		M16A	10.3	10.45	2.1	30.00
WM		M20B	13.3	13.45	3.0	30.00
WM		M24B	15.9	16	3.0	30.00
SJ	Small Outline Package, EIAJ (SOP)	M14D	10.7	11	2.4	50.00
SJ		M16D	10.7	11	2.4	50.00
SJ		M20D	13.2	13.5	2.4	50.00
QSC	Shrink Small Outline Package, JEDEC (QSOP or JEDEC SSOP)	MQA20	9.5	9.65	2.1	30.00
QSC		MQA24	9.5	9.65	2.1	30.00
MSA	Shrink Small Outline Package, EIAJ, Type II (SSOP II)	MSA20	7.6		2.5	30.00
MSA		MSA24	8.9		2.5	30.00
MSC	Shrink Small Outline Package, EIAJ, Type I (SSOP I)	MSC14	5.5		1.9	
MSC		MSC16	5.5		1.9	
MSC		MSC20	7.0		1.9	

Tape Specifications and Drawings (Continued)

TSSOP 14, 16, 20 and 24-Lead

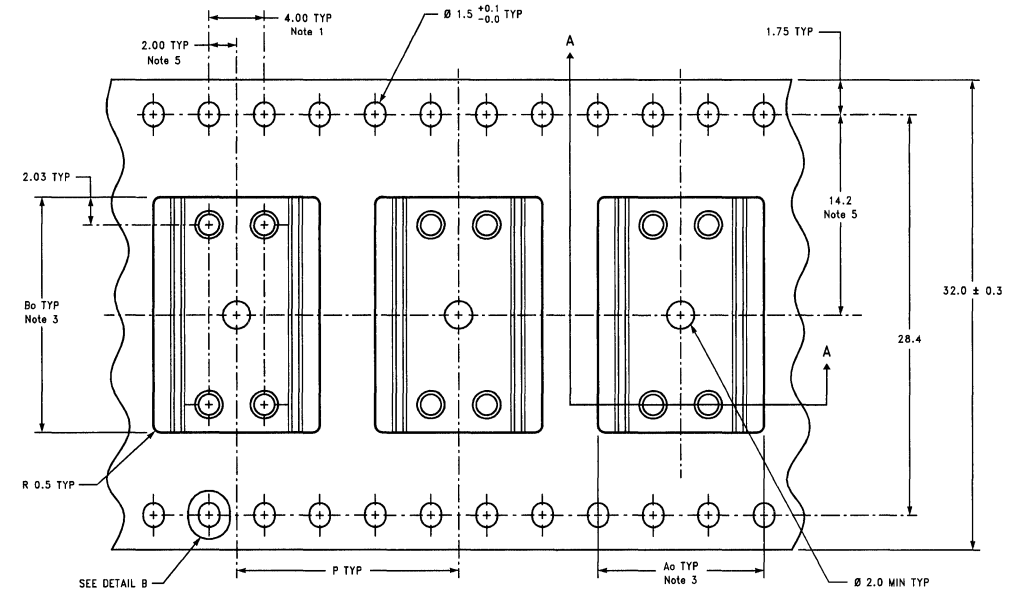


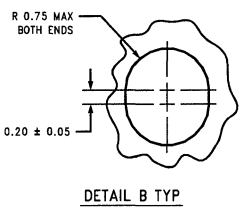
TL/F/12657–12

Package Code	Package Description	Package Number	W	A0	B0	B1	K0	K1
MTC	Thin Shrink Small Outline Package, JEDEC, 4.4mm (TSSOP)	MTC14	12.0	6.95 ± 0.1	5.6 ± 0.1	6.3	1.6	1.2
MTC		MTC16	12.0	6.95 ± 0.1	5.6 ± 0.1	6.3	1.6	1.2
MTC		MTC20	16.0	6.95 ± 0.1	7.1 ± 0.1	7.8	1.6	1.3
MTC		MTC24	16.0	6.95 ± 0.1	8.3 ± 0.1	9.0	1.6	1.3

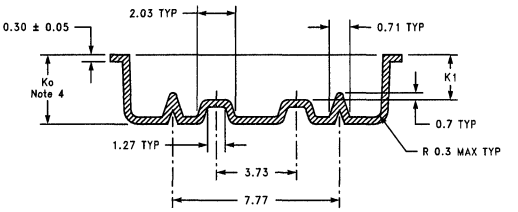
Tape Specifications and Drawings (Continued)

SSOP 48 and 56-Lead

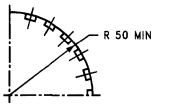




DETAIL B TYP



SECTION A-A



BEND RADIUS

Tape with components shall pass around mandril radius R without damage. (NOT TO SCALE)

TL/F/12657–13

Notes: Unless otherwise specified.

Note 1: 10 sprocket hole pitch cumulative tolerance ±0.2.

Note 2: Camber not to exceed 1mm in 100 mm.

Note 3: A_0 and B_0 measured on a plane 0.3 mm above the bottom of the pocket.

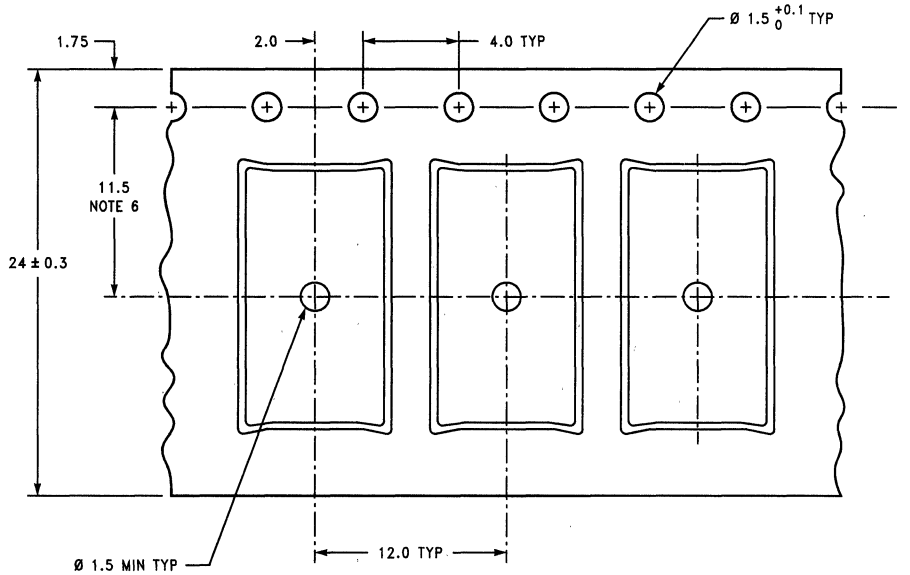
Note 4: K_0 measured from a plane on the inside bottom of the pocket to the top surface of the carrier.

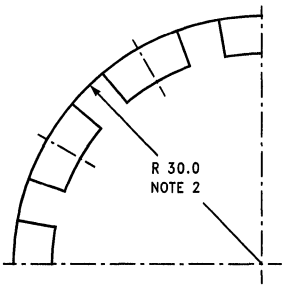
Note 5: Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Package Code	Package Description	Package Number	A0	B0	K0	K1	P
MEA	Shrink Small Outline Package, JEDEC (SSOP)	MS48A	12.0	16.2	3.2	2.4	16.0
MEA		MS56A	12.0	18.7	3.2	2.4	16.0

Tape Specifications and Drawings (Continued)

TSSOP 48 and 56-Lead





BEND RADIUS
(NOT TO SCALE)

TL/F/12657–14

Notes: Unless otherwise specified.

Note 1: Cumulative pitch tolerance for feeding holes and cavities (chip pockets) not to exceed 0.2 mm over 10 pitch span.

Note 2: Smallest allowable bending radius.

Note 3: Camber not to exceed 1 mm in 100 mm.

Note 4: Dimensions A_0 and B_0 measured on a plane 0.3 mm above the bottom of the pocket.

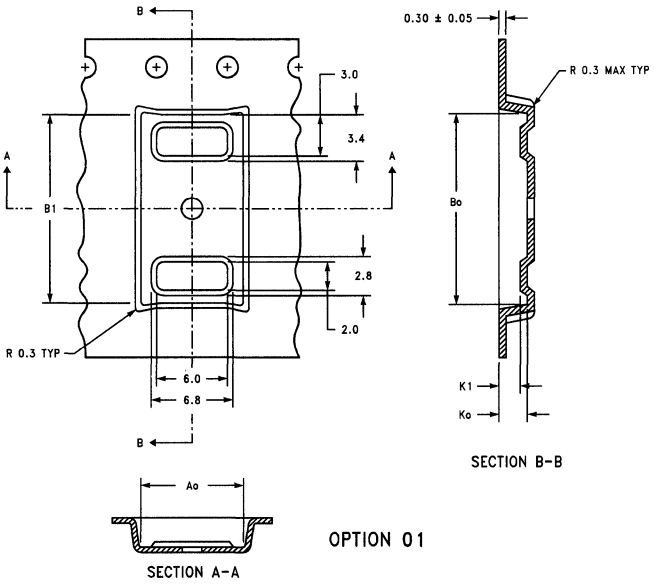
Note 5: Dimension K_0 measured from a plane on the inside bottom of the pocket to the top of the carrier.

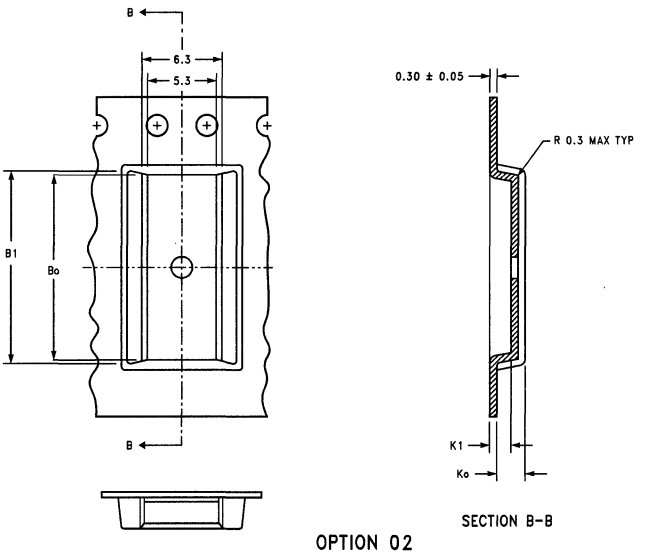
Note 6: Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Note 7: Both Option A and Option B pocket designs are acceptable.

Tape Specifications and Drawings (Continued)

TSSOP 48 and 56-Lead (Continued)

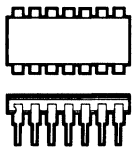
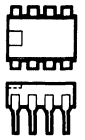
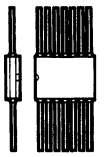
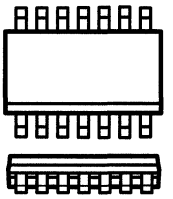
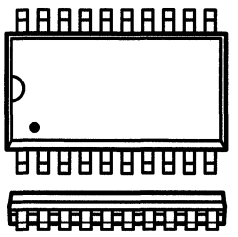


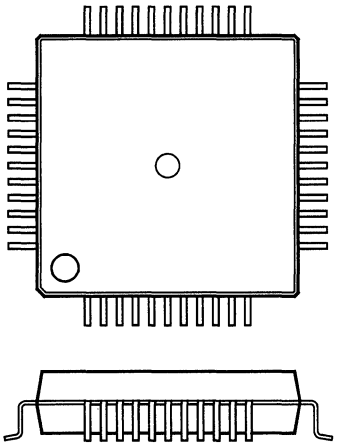
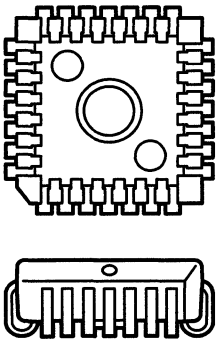
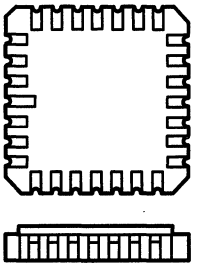


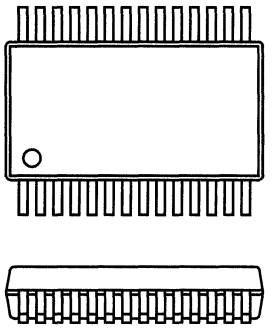
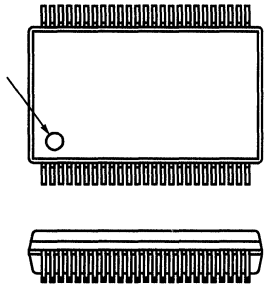
TL/F/12657–15

Package Code	Package Description	Package Number	A0	B0	B1	K0	K1
MTD	Thin Shrink Small Outline Package, JEDEC, 6.1mm (TSSOP)	MTD48	8.6	13.2	13.9	1.6	1.2
MTD		MTD56	8.6	14.5	17	1.8	1.3

Interface Package Cross-Reference Guide and Comparison Summary

		NSC	Motorola	TI	AMD
	8-, 14- and 16-Lead Low Temperature Ceramic DIP	J	U	J	D
	8-, 14- and 16-Lead Plastic DIP	N	P	P, N	P
	Low Temperature Glass Hermetic Flat Pack	W	F	W	F
	SO (Narrow Body)	M	D	D	
	SO (Wide Body)	WM		DW	

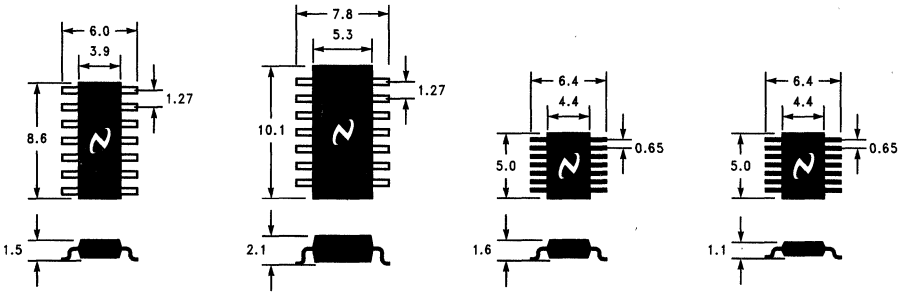
	NSC	Motorola	TI	AMD
 PQFP Plastic Quad Flat Package Top View Side View	VF			
 PCC	V	FN	FN	L
 LCC Leadless Ceramic Chip Carrier	E	U	FK/ FD	

	NSC	Motorola	TI	AMD
 SSOP Shrink Small Outline Package (EIAJ, Type II)	MSA		DB	
 SSOP Shrink Small Outline Package (JEDEC)	MEA		DL	

Selected Small Outline Package Comparison Summary

Dimensions in millimeters to scale but not actual size

14-Lead Package Options



SOIC (JEDEC)
(M, MX)
Area = 52 sq mm

SOP (EIAJ)
(SJ, SJX)
Area = 79 sq mm

SSOPI
(MSCX)
Area = 32 sq mm

TSSOP
(MTC, MTCX)
Area = 32 sq mm

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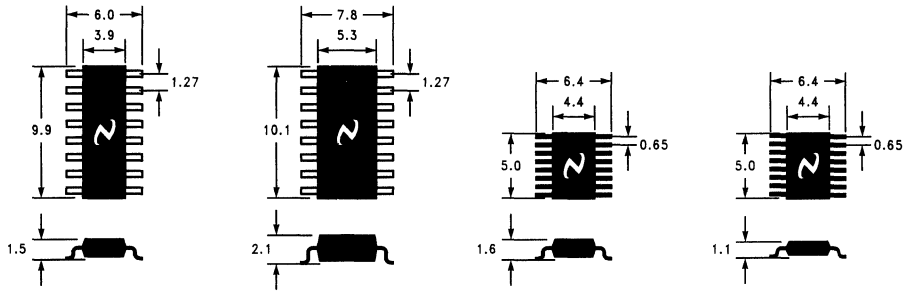
Selected Small Outline Package Comparison Summary

Dimensions in millimeters to scale but not actual size (Continued)

16-Lead Package Options



SOIC (JEDEC) (M, MX) Area = 59 sq mm

SOP (EIAJ) (SJ, SJX) Area = 79 sq mm

SSOPI (MSCX) Area = 32 sq mm

TSSOP (MTC, MTCX) Area = 32 sq mm

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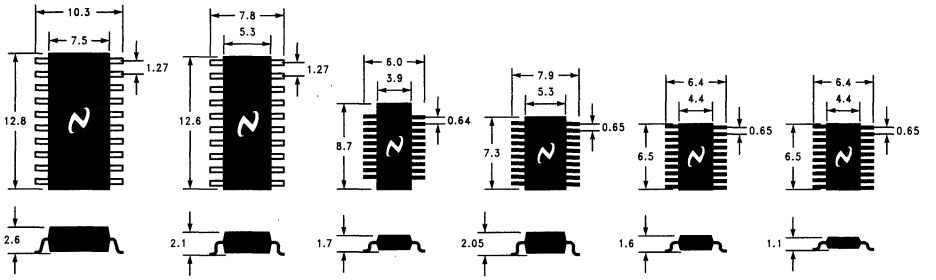
20-Lead Package Options



SOIC (JEDEC) (WM, WMX) Area = 132 sq mm

SOP (EIAJ) (SJ, SJX) Area = 98 sq mm

QSOP (QSC, QSCX) Area = 52 sq mm

SSOPII (MSA, MSAX) Area = 58 sq mm

SSOPI (MSCX) Area = 42 sq mm

TSSOP (MTC, MTCX) Area = 42 sq mm

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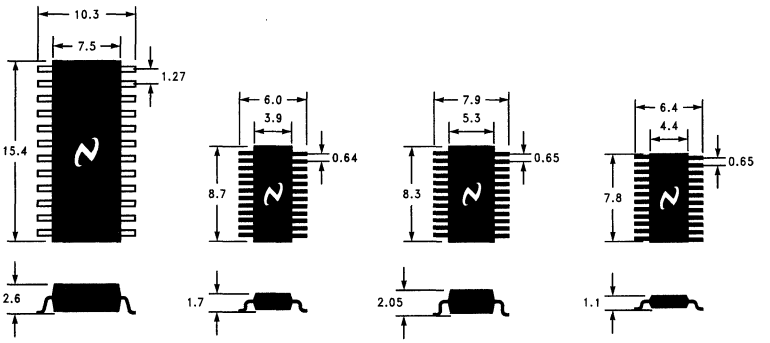
24-Lead Package Options



SOIC (JEDEC) (WM, WMX) Area = 159 sq mm

QSOP (QSC, QSCX) Area = 52 sq mm

SSOPII (MSA, MSAX) Area = 66 sq mm

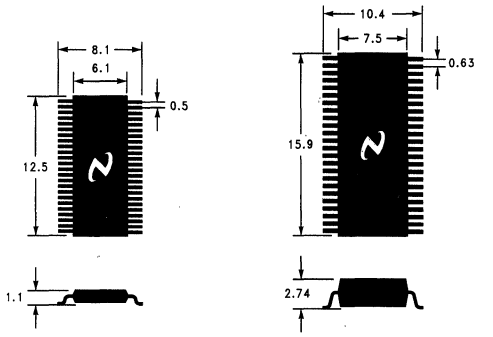
TSSOP (MTC, MTCX) Area = 50 sq mm

TL/XX/0093-4

Selected Small Outline Package Comparison Summary

Dimensions in millimeters to scale but not actual size (Continued)

48-Lead Package Options

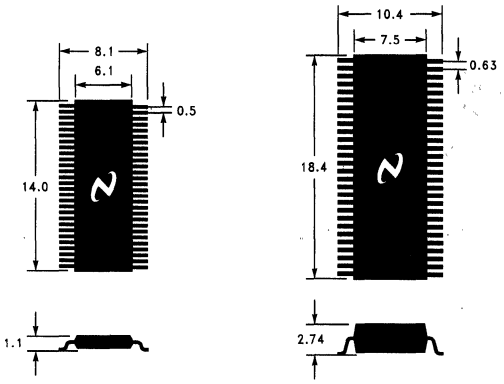


TSSOP
(MTD, MTDX)
Area = 101 sq mm

SSOP
(MEA, MEAX)
Area = 165 sq mm

TL/XX/0093-5

56-Lead Package Options



TSSOP
(MTD, MTDX)
Area = 113 sq mm

SSOP
(MEA, MEAX)
Area = 191 sq mm

TL/XX/0093-6

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

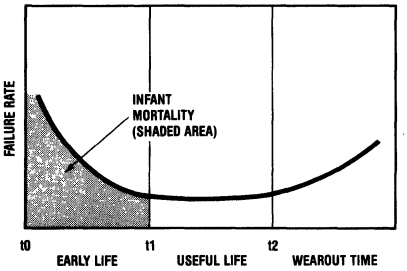


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2.* This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

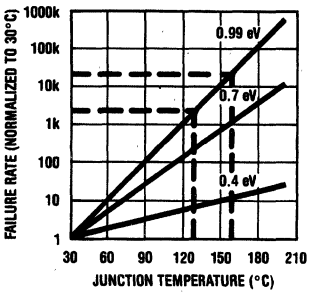

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4.*

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

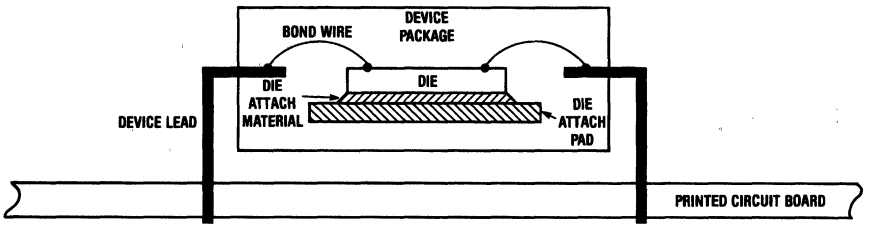

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

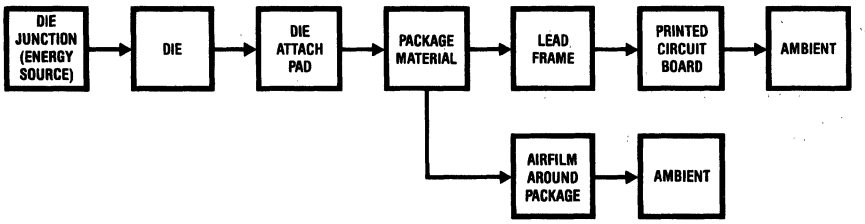

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

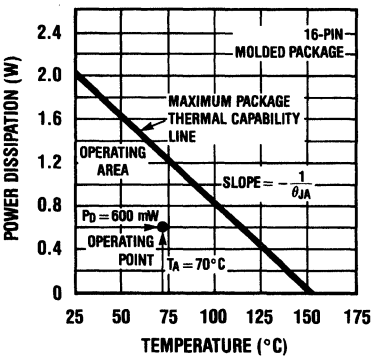

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

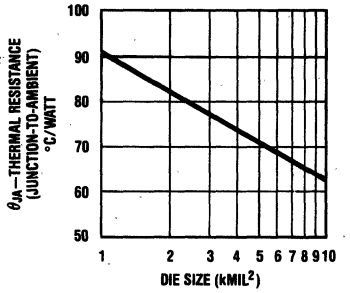

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

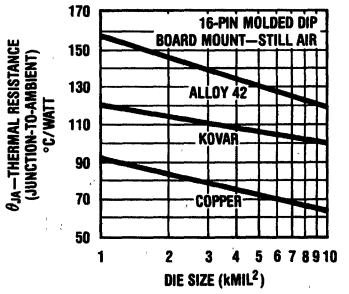

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

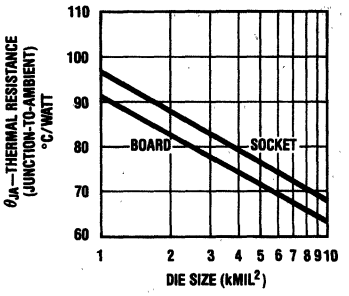

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

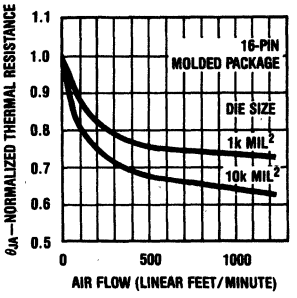

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

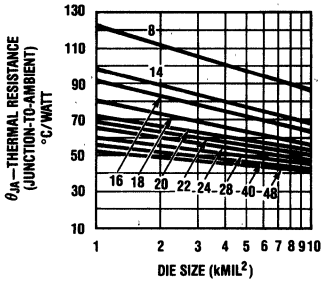
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

P_D @ 70°C = 1476 mW − (11.8 mW/°C) × (70°C − 25°C)
= 945 mW

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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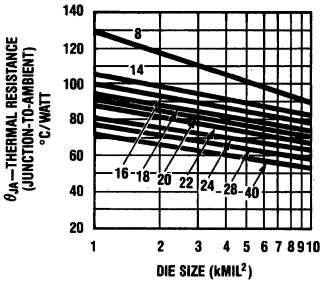
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

TL/F/5280–11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

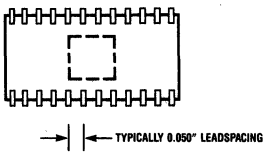
Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

S.O. Package



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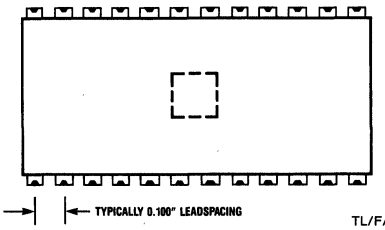
Standard DIP Package



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Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelerated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

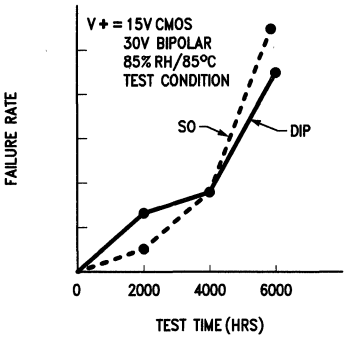

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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

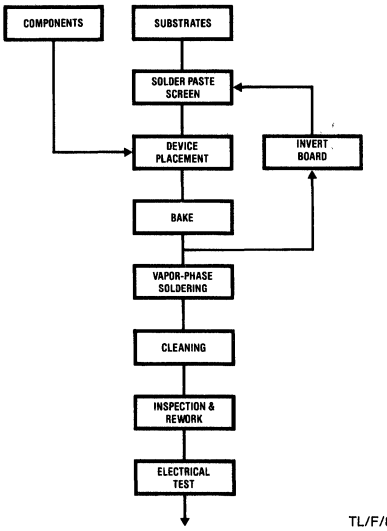
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

PRODUCTION FLOW

Basic Surface-Mount Production Flow



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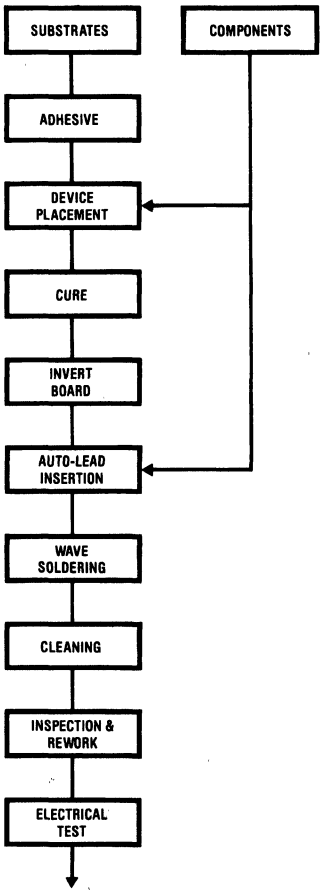
Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



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Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

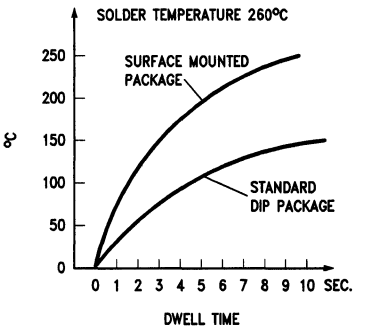

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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C*. At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

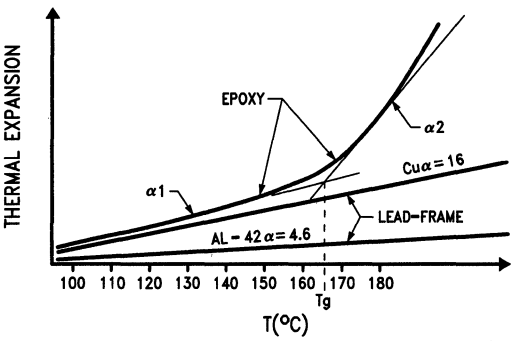

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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

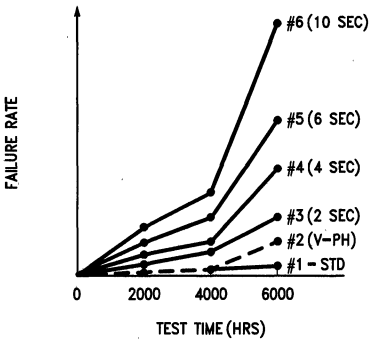
Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds



TL/F/8766–7

FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

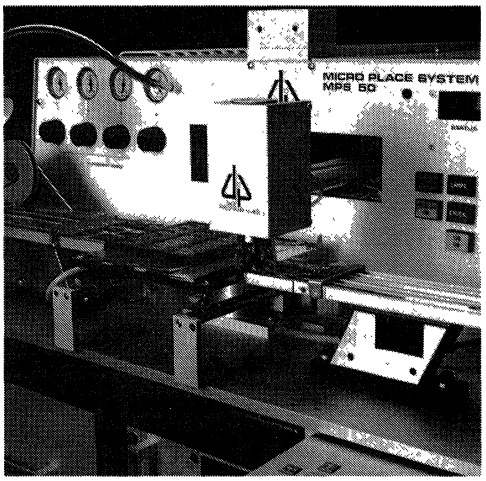
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



TL/F/8766–8

BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

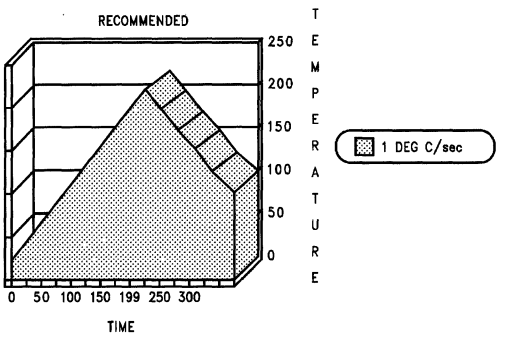
A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

INFRARED REFLOW SOLDERING

Use of an infrared furnace is currently the most popular method to automate mass reflow, the heating is promoted by use of IR lamps or panels. Early objections to this method were that certain materials may heat up at different rates under IR radiation and could result in damage to those components (usually sockets and connectors). This has been minimized by using far-infrared (non-focused) systems and convected air.

Infrared Profile



TL/F/8766–27

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

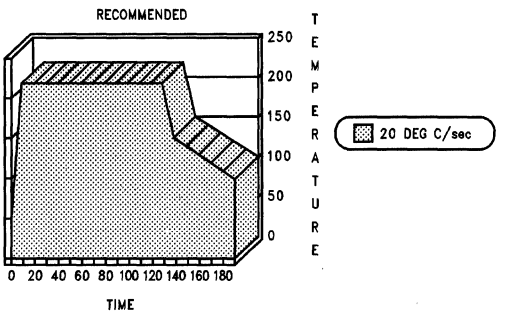
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

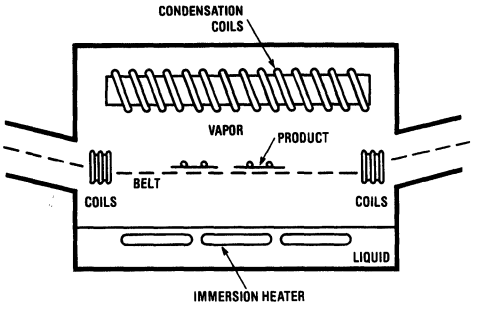
Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

Vapor-Phase Profile



TL/F/8766–28

In-Line Conveyorized Vapor-Phase Soldering



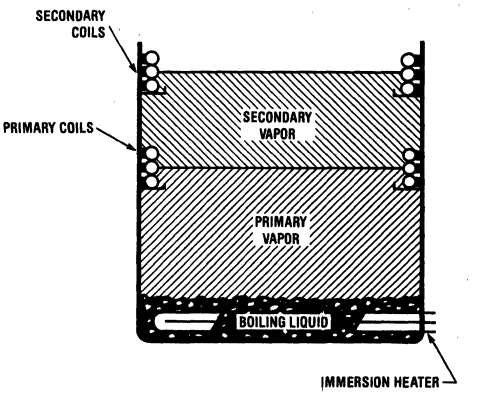
TL/F/8766–9

The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace

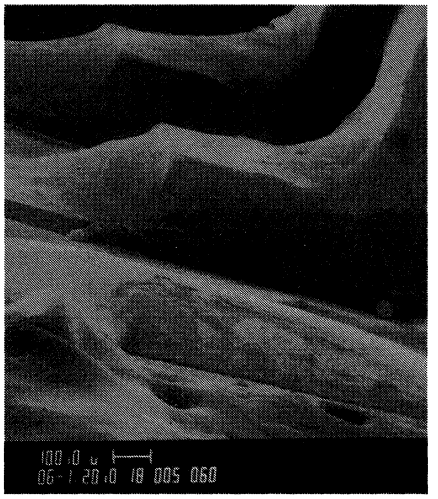
TL/F/8766–10

Batch-Fed Production Vapor-Phase Soldering Unit



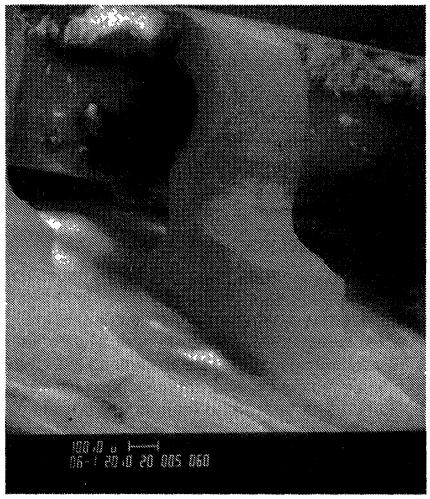
TL/F/8766–11

Solder Joints on a SO-14 Package on PCB



TL/F/8766–12

Solder Joints on a SO-14 Package on PCB



TL/F/8766–13

PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed 1/8", to avoid damage to screens and minimize distortion.

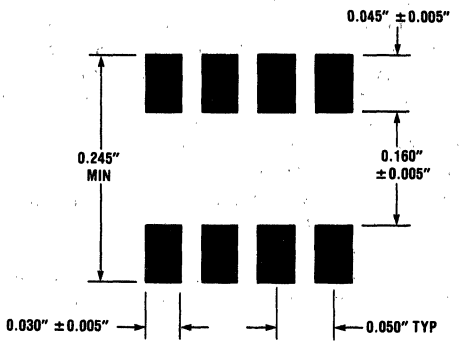
SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see following photographs). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.
- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 × magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

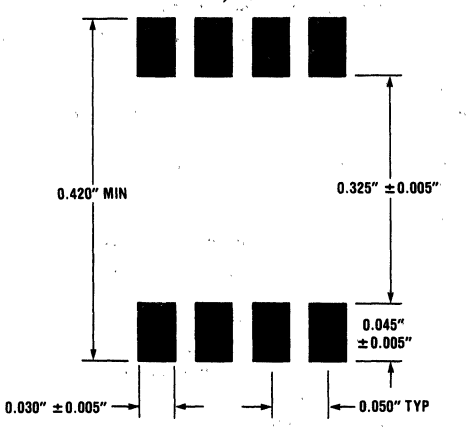
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



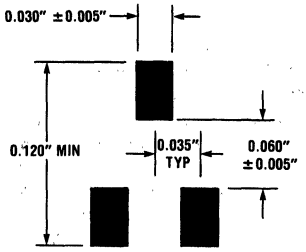
TL/F/8766–14

SO-16L, SO-20



TL/F/8766–15

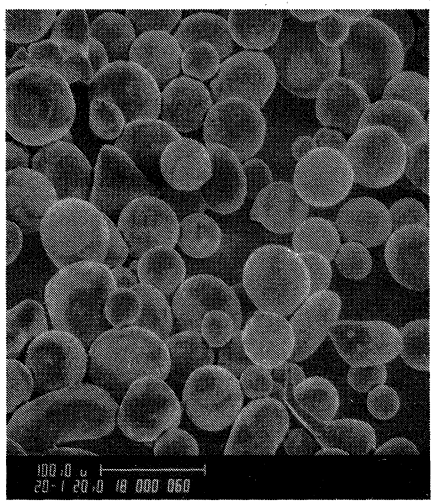
SOT-23



TL/F/8766–16

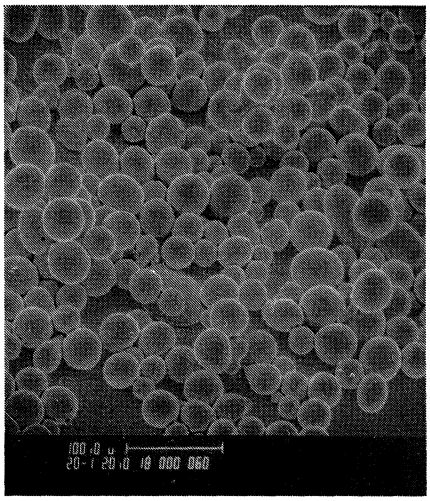
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



TL/F/8766–17

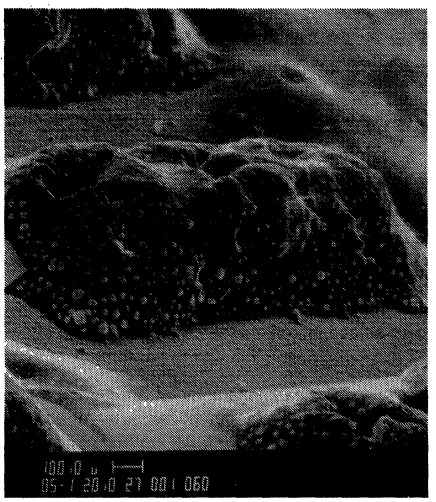
200 × Kester (63/37)



TL/F/8766–18

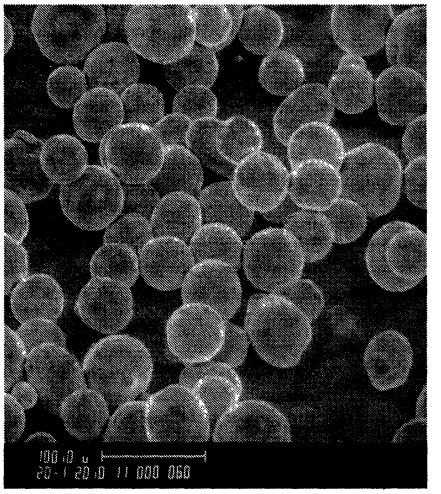
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



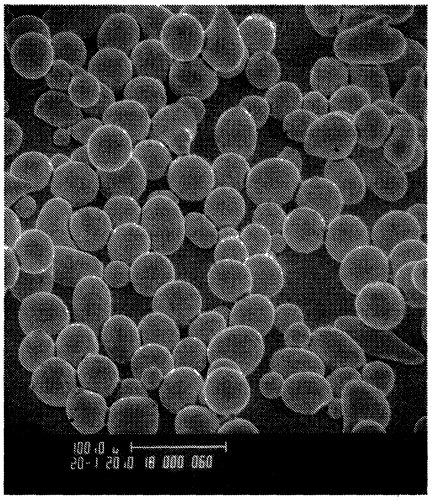
TL/F/8766–19

200 × Fry Metal (63/37)



TL/F/8766–20

200 ESL (63/37)



TL/F/8766–21

CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. CFC solvents are being phased out as they are hazardous to the environment. Other approaches to cleaning are commercially available and should be investigated on an individual basis considering local and government environmental rules.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

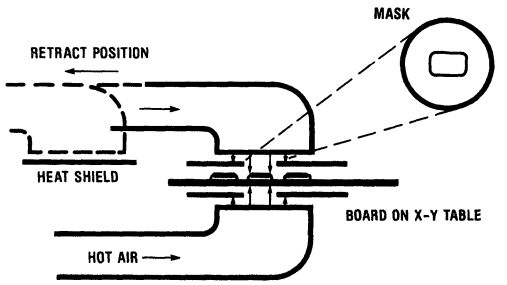
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

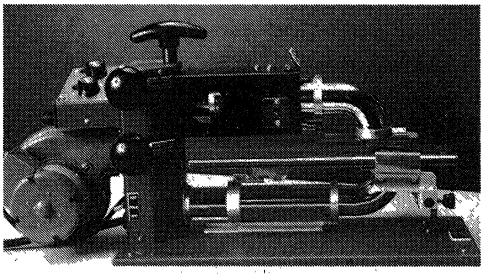
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



TL/F/8766–22

Hot-Air Rework Machine



TL/F/8766–23

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

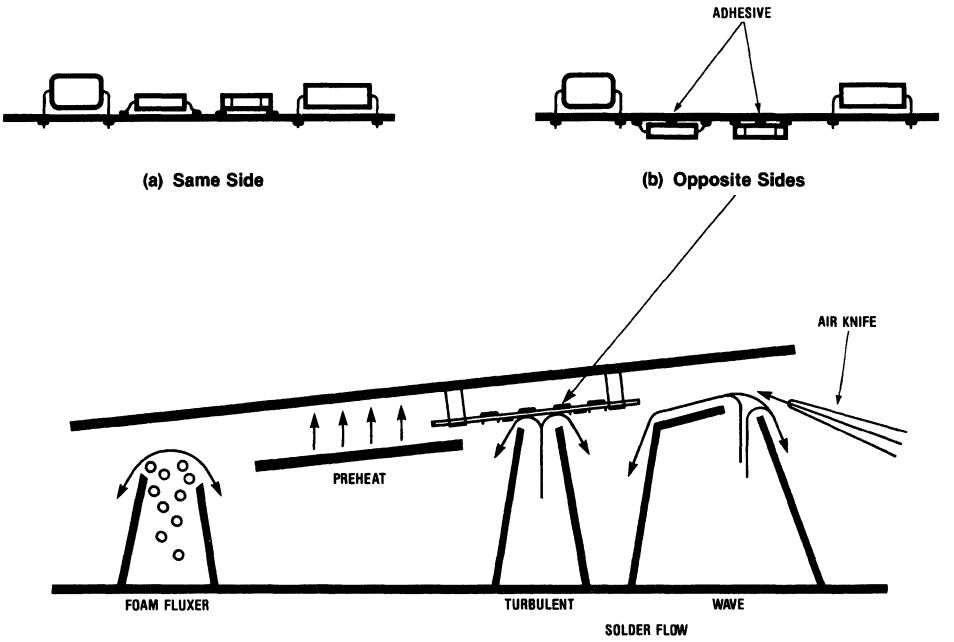
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



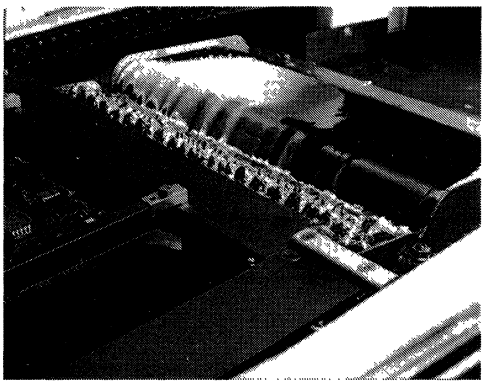
TL/F/8766–24

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766–25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.

National Semiconductor

Interface Products
Nomenclature Revisions and Obsolescence Cross Reference Guide

The Data Transmission Products Nomenclature Revision and Obsolescence Cross Reference Guide is provided as an aid in identifying part numbers of products that have been revised or obsoleted.

The Nomenclature Table provides a list of old device designations vs new device designations for devices that have been revised or encountered name changes along with a respective comment.

The Obsolescence Cross Reference Guide provides a list of parts that have been discontinued recently. This includes device types, temperature grades, and or package options. Whenever possible a cross reference to a similar part is provided.

Before replacing a specific part, it is recommended to compare electrical, functional, and mechanical specifications as interchangeability for all applications is not guaranteed.

Nomenclature Revisions

Old Device Designation	New Device Designation	Comments
DS26C31C	DS26C31T	ESD Enhancement
DS26C32C	DS26C32AT	Name Change
DS26C32AC	DS26C32AT	ESD Enhancement
DS34C86	DS34C86T	ESD Enhancement
DS34C87	DS34C87T	ESD Enhancement
DS75176A	DS75176B	Name Change
DS75176AT	DS75176BT	Name Change
DS96F172	DS96F172C/M	Temp. Range Suffix Added
DS96F173	DS96F173C/M	Temp. Range Suffix Added
DS96F174	DS96F174C/M	Temp. Range Suffix Added
DS96F175	DS96F175C/M	Temp. Range Suffix Added
μA	DS	FSC to NSC Prefix Change

Obsolescence Cross Reference Guide

Obsolete NSID	Similar Device	Comments
DS1650		
DS3587	DS35F87	Different Process
DS3696AT	DS3696A	Com. Temp. Range Only
DS3696AT	DS3696T	DIP Package Only
DS3898		
DS55107	DS55107	883 Part Available
DS55108	DS75108	Com. Temp. Range Only
DS55110A	DS75110A	Com. Temp. Range Only
DS55114	DS75114	Com. Temp. Range Only
DS55121	DS75121	Com. Temp. Range Only
DS75125		
DS75127		
DS75128		
DS7641		
DS8924		
DS8921T	DS8921AT	Enhanced AC Specs.
DS9614	DS75114	Com. Temp. Range Only
DS96F177	DS96177	
DS96F178		

National/Fairchild Consolidation and Nomenclature Changes

Device Designation	Device Designation
Fairchild	National
μA1488DC	DS1488J
μA1488PC	DS1488N
μA1488SC	DS1488M
μA1489DC	DS1489J
μA1489PC	DS1489N
μA1489SC	DS1489M
μA1489APC	DS1489AN
μA26LS31DC	DS26LS31CJ
μA26LS31PC	DS26LS31CN
μA26LS32PC	DS26LS32ACN
μA3486DC	DS3486J
μA3486PC	DS3486N
μA3487PC	DS3487N
μA55107ADM	DS55107AJ
μA75107ADC	DS75107AJ
μA75107APC	DS75107AN
μA75107ASC	DS75107AM
μA75107BDC	DS75107J
μA75107BPC	DS75107N
μA75107BSC	DS75107M
μA75108BPC	DS75108N
μA75108BSC	DS75108M
μA75110APC	DS75110AN
μA75110ASC	DS75110AM
μA75150TC	DS75150N
μA75150SC	DS75150M
μA75154PC	DS75154N

Device Designation	Device Designation
Fairchild	National
μA9614DM	*
μA9614PC	DS75114N
μA9615DM	*
μA9615PC	DS75115N
μA96172DC	DS96172CJ
μA96172PC	DS96172CN
μA96174DC	DS96174CJ
μA96174PC	DS96174CN
μA96173DC	DS96173CJ
μA96173PC	DS96173CN
μA96175DC	DS96175CJ
μA96175PC	DS96175CN
μA96176RC	DS96176CJ
μA96176TC	DS96176CN
μA96177TC	DS96177CN
μA9636ARM	DS9636AMJ
μA9636ARC	DS9636ACJ
μA9636ATC	DS9636ACN
μA9637ARM	DS9637AMJ
μA9637ARC	DS9637ACJ
μA9637ATC	DS9637ACN
μA9637ASC	DS9637ACM
μA9638RM	DS9638MJ
μA9638RC	DS9638CJ
μA9638TC	DS9638CN
μA9639ATC	DS9639ACN

*Contact Product Marketing

National Semiconductor

National/Fairchild Consolidation and Nomenclature Changes

Device Designation	Device Designation
MIL/AREO FSC	**MIL/AREO NSC**
μA55107ADMQB	DS55107AJ/883
μA55110ADMQB	DS55110AJ/883
μA9614DMQB	DS9614MJ/883
μA9614FMQB	DS9614MW/883
μA9614LMQB	DS9614ME/883
μA9615DMQB	DS9615MJ/883
μA9615FMQB	DS9615MW/883
μA9615LMQB	DS9615ME/883
μA9616HDMQB	DS9616HMJ/883
μA9616HLMQB	DS9616HME/883
μA9622DMQB	DS9622MJ/883
μA9622LMQB	DS9622ME/883
μA9622FMQB	DS9622MW/883
μA9627DMQB	DS9627MJ/883
μA9636ARMQB	DS9636AJ/883
μA9637ARMQB	DS9637AMJ/883
μA9638RMQB	DS9638MJ/883
μA55110ADMQM	SMD-8754701CA
μA9622DMQM	SMD-8752201CA
μA9622FMQM	SMD-8752201AA
μA9638RMQM	SMD-8754601PA

National Semiconductor

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who need better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connote identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population of faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction; the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

National's A+ Program (Continued)

Five Temperature Cycles (0°C to 100°C)

Exercising each device over a 100°C temperature range provides an additional die and package stress.

High Temperature (100°C) Functional Electrical Test

A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C—15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-In Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96 eV activation energy (i.e., 23 hours at +155°C). All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-Than-Normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

Backplane Reference

Backplane Manufacturers

Augat
33 Perry Avenue/P.O. Box 779
Attleboro, MA 02703
(508) 222-2202

BICC-VERO Electronics, Inc.
1000 Sherman Avenue
Hamden, CT 06514-1336
(203) 288-8001

Hybricon Corporation
12 Willow Road/P.O. Box 149
Ayer, MA 01432
(508) 772-5422

Mupac Corporation
10 Mupac Drive
Brockton, MA 02401
(508) 588-6110

Schroff, Inc.
170 Commerce Drive
Warwick, RI 02866
(401) 732-3770

2mm Connector Manufacturers

DuPont Electronics
Barley Mill Plaza
P.O. Box 80019
Bloomington, DE 19880-0019
(800) 237-2374

ITT ElectroMechanical Components Worldwide
1851 East Deere Avenue
Santa Ana, CA 92705-6500
(714) 261-5300

ATT Microelectronics
555 Union Blvd
Allentown, PA 18103
(800) 372-2447

Molex Incorporated
Corporate Headquarters
Lisle, IL 60532
(708) 969-4550

Futurebus+ and Related Standards

896.1	Futurebus+ Logical Layer Specifications
896.2	Futurebus+ Physical Layer Specifications Includes: Profiles A, B, F
P896.3	Futurebus+ Systems Configuration Guide
P896.4	Futurebus+ Conformance Test
P896.X	Additional Profile Documents including C, D, M, T
P1014.1	VME/Futurebus+ Bridge
1101.2	2mm Connector Specification
P1101.3	Conduction Cooling Specification
1156	Environmental and Power Supply Specification
1194.1	Backplane Transceiver Logic (BTL) Specification
1212	CSR Architecture
P1296.2	Multibus II/Futurebus+ Bridge
1301	Metric Equipment Practice
1301.1	Futurebus+ Hard Metric Boards + 2mm Connector
P1394	High Speed Serial Bus
1596	SCI (Scalable Coherent Interface)

All specifications/standards for Futurebus+ are available from either the IEEE or VITA. Please see user groups for information on how to contact these associations.

Futurebus+ Users Groups and Standards Associations

VFEA International Trade Association (VITA)
10229 North Scottsdale Road
Suite B
Scottsdale, AZ 85253-1437 USA
(602) 951-8866

Futurebus Manufacturers and Users Group (FMUG)
P.O. Box 130
Fleet, Hampshire GU13 8XU England
0252-629937

Standards Department
IEEE Computer Society
1730 Massachusetts Avenue, N.W.,
Washington, D.C. 20036-1903
(202) 371-0101

National Semiconductor

Glossary of Terms for Futurebus+ (Listed Alphabetically)

ADDRESS ONLY TRANSACTION: A bus transaction that does not include a data phase. The only information transferred is contained within the connection phase and, in some cases, the disconnection phase.

APPLICATION ENVIRONMENT PROFILE (AEP): An application environment profile is a document that describes functional requirements and points to existing standards, selecting and binding options within those standards. An implementor who then designs a specific board and/or system SHOULD be reasonably assured that another designer's (manufacturer or supplier) boards will properly function within the same system. This includes all aspects of definition: mechanical, electrical, protocol environmental, and system considerations.

ARBITRATION: The process of selecting the next bus master.

ARBITRATION MESSAGE: An event number broadcast on the arbitration bus to all modules on the bus.

BACKPLANE: An electronic circuit board and connectors used to connect other boards together electrically. The backplane connects selected pins of the connectors, thus providing the medium for the transfer of signals needed for the operation of the bus.

BACKPLANE BUS: A means to connect circuit modules using common signal traces on a backplane and a standard set of rules.

BEAT: An event that begins with the transition on a synchronization line by the master followed by the release of an acknowledge line by one or more slaves. Command and data information may be transferred from the master to one or more slaves in the first half of the beat. During the second half of the beat the slaves may transfer capability, status, and data information back to the master.

BIU: The BIU (Bus Interface Unit) refers to the logic on a module that converts bus signals and the protocols to and from signals which are compatible with the functional logic of the module.

BLOCK READ TRANSACTION: An address beat followed by a block of one or more data read transfers from a set of contiguous addresses beginning with the address in the address beat. This is terminated by the appropriate style of end beat.

BLOCK WRITE TRANSACTION: An address beat followed by a block of one or more data write transfers to a set of contiguous addresses beginning with the address in the address beat. This is terminated by the appropriate style of end beat.

BRIDGE: A bridge is a protocol converter and Control and Status Register Architecture (CSRA) unit which interfaces between two or more buses. The buses may adhere to different bus standards for mechanical, electrical and logical operation (such as a bridge from Futurebus+ to VMEbus or to Multibus II).

BUS TENURE: The duration of a master's control of the bus; i.e., the total time that a module has the right to initiate bus transactions.

BUS TRANSACTION: An event initiated with a connection phase and terminated with a disconnection phase. Data may or may not be transferred during a bus transaction.

BUSY: If a slave cannot or should not accept a bus transaction at that time it, or any other module, may issue a Busy status to the master of the transaction. The master must then release the bus. The master must relinquish the bus and may re-acquire and re-try the transaction after a suitable time interval.

BYTE LANE: A data path formed by eight data lines and one parity line used to carry a single byte among the system modules.

CACHE COHERENCE: A system of caches is said to be coherent with respect to a cache line if each cache and main memory in the coherence domain observes all modifications of that same cache line. A modification is said to be observed by a cache when any subsequent read would return the newly written value.

CACHE MEMORY: A buffer memory inserted between one or more processors and the bus, used to hold currently active copies of blocks from main memory. Cache memories exploit spatial locality by what is brought into a cache. Temporal locality is exploited by what is removed from the cache.

COHERENCE DOMAIN: A coherence domain is a region in a multiple-cache system inside which cache consistency measures are enforced. In a system which contains bus bridges, a coherence domain may or may not be extensible beyond the local bus through a bus bridge to remote buses.

COHERENCE LINE: A data block for which cache consistency attributes are maintained.

COMPETITOR: A module actively participating in the current control acquisition cycle of the arbitration process.

CONNECTED SLAVE: A slave that is permitted to participate actively in the data transfer handshake. A selected slave that is not disabled (including a diverted slave), a reflecting slave, and an intervening slave are connected slaves. A disabled slave or, an unselected slave that is not intervening or reflecting, is not a connected slave.

CONNECTED TRANSACTION: A transaction in which both the request and response are performed within the same bus transaction.

CONNECTION PHASE: A beat that begins with the assertion of the address synchronization line followed by the release of an address acknowledge line. It is used to broadcast the address and command information. Modules determine whether they wish to take part in the transaction based on this information.

CONTROL ACQUISITION: The total of all bus activity associated with acquiring exclusive control of the bus.

COPYBACK CACHE: A cache memory scheme with the attribute that data written from the processor is normally written to the cache rather than the main memory. Modified data in the cache is written to the main memory when a cache line flush or replacement forces it to be written to main memory to avoid loss of the data.

CSR: Control and Status Register.

CSRA: Control and Status Register Architecture.

DATA PHASE: A period within a transaction used to transfer data.

DEADLOCK: Deadlock occurs when actors are waiting on actions that can only be performed by those waiting.

DISABLED SLAVE: A selected slave that detects that an intervening slave is participating in the data transfer in its place. A disabled slave treats the transaction as an address-only transaction and does not participate in the data transfer phase. A slave may be disabled only during single-slave mode transactions.

DISCONNECTION PHASE: A period within a transaction used to return the bus signals to their quiescent state. In addition, this phase might be used to transfer additional information required to perform or abort the requested operation.

DIVERTED SLAVE: A selected slave that detects that a reflecting slave is participating in the data transfer in its place. A diverted slave participates in the transfer by reading the data being transferred between the master and the reflecting slave. A slave may be diverted only during single-slave mode transactions.

DMA: A direct memory access architecture is an option capability of an I/O controller. After being started by the processor, the I/O controller with DMA capabilities can access their commands, fetch data, and report status by accessing memory directly.

DOUBLET: A set of two adjacent bytes.

EMERGENCY MESSAGE: An arbitration cycle with a special high arbitration number, which is selected from a set of numbers assigned to emergency messages.

ENTRANT: A live inserted module in the process of aligning itself with the arbitration protocol.

FAIRNESS: A bus request protocol in which a module refrains from acquiring the bus in order to allow other modules of the fairness class to use the bus.

FORWARD PROGRESS: A module which is not blocked from performing the tasks necessary to achieve its goal is said to be making forward progress. Forward progress is guaranteed only in the absence of deadlock or starvation.

FREE BYSTANDER: A free bystander can be a participating slave that is no longer an entrant, or a potential master that has no current need to acquire the bus and is not fairness inhibited.

GEOGRAPHICAL ADDRESS: A unique identifier statically assigned to each logical module slot on the bus and assumed by any module connected to that slot.

INACTIVE MODULES: This category contains all the modules that have no need to participate in the control acquisition process in any way.

INHIBITED BYSTANDER: An inhibited bystander is a potential master that has no current need to acquire the bus and is fairness inhibited.

INTERVENING SLAVE: An unselected slave that disables the selected slave and replaces that selected slave with itself. Intervening slaves can operate only during single-slave mode transactions.

LIVE INSERTION: Insertion of boards into a backplane can be performed when power is OFF or when power is ON. The process of inserting or withdrawing boards into and from a backplane when power is ON is referred to as "Live Insertion".

LIVELOCK: Livelock is a metastable situation in which some modules acquire and release resources in a way that none of them make progress.

LOCKING: A facility whereby a module is requested to guarantee exclusive access to addressed data, blocking other modules from accessing that data. This allows indivisible operations to be performed on addressed resources.

MASTER: A module which has acquired control of the bus through the control acquisition procedure.

MASTER ELECT: A master elect is the module that has won the arbitration process and is waiting for the master to transfer control to it.

MIXED TRANSACTION: An address beat followed by any number or combination of data write and data read transfers to a single location using the single address transfer mode. This is terminated by the appropriate style of end beat.

MODULE: A collection of circuitry designed to perform Futurebus+ operations.

MONARCH PROCESSOR: A monarch processor, or simply the monarch, is the processor selected to manage the configuration and initialization of all modules on that logical bus. A grand monarch is a processor selected to direct the configuration and initialization of an entire system with multiple interconnected logical buses.

NODE: A node is a set of control registers addresses (including identification-ROM and reset command register), which are initially defined in a 4k-byte (minimum) initial node address space. Each node can be reset independently.

OCTLET: A set of eight adjacent bytes.

PACKET DATA TRANSFER PROTOCOL: A very fast but technology dependent non-compelled transfer mechanism which uses a compelled protocol over the entire packet to provide flow control.

PARALLEL CONTENTION ARBITRATION: A process whereby modules assert their unique arbitration number of a parallel bus and release signals according to an algorithm such that after a period of time the winner's number appears on the bus.

PARKING: The process whereby the master retains control of the bus without actively using in. Parking typically occurs when no other module has requested the bus. The idle bus arbitration mechanism may be used when the bus is parked.

PARTICIPATING SLAVE: A participating slave may be in any of these states; 1) entrant, 2) bystander.

PORT: A port is the interconnection of a bus bridge to a bus. From the point of view of a particular node on a bus, the node connects to the local port of a bus bridge, while ports to other buses connected to the same bus bridge are called remote ports.

POTENTIAL MASTER: A potential master is a module that is capable of participating in the control acquisition process and taking full control of the bus. A potential master may be in any of these states; 1) entrant, 2) free bystander, 3) inhibited bystander, 4) competitor, 5) withholder, 6) master elect, 7) master, 8) recompeting master.

POTENTIAL SLAVE: A module that is capable of being addressed by and is able to carry out transactions with the master.

PRIORITY: A bus request protocol in which the module with the highest arbitration number acquires the bus.

PREEMPTION: Preemption occurs when the arbitration process is restarted after a master elect has been chosen in order to allow a high priority module to jump the queue.

QUADLET: A set of four adjacent bytes.

RECOMPETING MASTER: The module that is in control of the bus and has initiated a control acquisition procedure in order to unlock slave interfaces.

REFLECTING SLAVE: An unselected slave that forces the selected slave into a write only mode. In read transfers the reflecting slave substitutes itself for the selected slave in providing data while causing the selected slave to store the data that appears on the bus. In write transfers the reflecting slave copies the data into itself as well as the selected slave. Reflecting slaves can operate only during single-slave mode transactions.

REPOSITORY OF LAST RESORT: In a cache-based environment, the repository of last resort of shared data is a physical storage location that is the ultimate source and destination of the datum that is shared.

REQUEST: A request is a command generated by a requester, to initiate an action on a responder. For a processor-to-memory read transaction, for example, the request transfers the memory address and command from the processor to memory. In the case of a split transaction the request would be a separate bus transaction. In the case of a connected transaction the request would be the connection phase of a bus transaction.

REQUESTER: A transaction initiated by a module sending a request (containing address, command, and sometimes data). This module is referred to as the requester.

RESPONDER: A transaction is completed by a module sending a response (containing the completion status and sometimes data).

RESPONSE: A reply generated by a responder, to complete a transaction initiated by a requester. For a processor-to-memory read transaction, for example, the response returns the data and status from the memory to the processor. In the case of a split transaction the response would be a separate bus transaction. In the case of a connected transaction the response would be the data and disconnection phases of a bus transaction.

ROUND ROBIN: An arbitration mode where, after a module acquires and uses the bus, it must then wait until all other modules currently requesting the bus at the same priority level have had a chance to use the bus.

SELECTED SLAVE: A potential slave that has been selected by the master because it recognized its address on the bus lines during an address transfer, and will become a connected slave, unless an intervening slave prevents it from becoming so.

SHARED MEMORY: The address space in the system accessible to all caching modules.

SKEW: The difference between the propagation delays of two or more signals passing through multiple paths in a device or along a set of signal lines in parallel.

SLAVE: A module that can be addressed and is capable of participating in bus transactions.

SNARF: A module is said to snarf a transaction if it takes a copy of data passing by on the bus even though it did not request it.

SNOOP: A module is said to snoop a transaction if it is not the master that originated the transaction or the repository of last resort for the data, but it still monitors the transaction. Cache memories snoop transactions to maintain coherence.

SPATIAL LOCALITY: The tendency for a program to reference closely related clusters of memory addresses over short time intervals.

SPLIT TRANSACTION: An operation in which the request is transmitted in one bus transaction and the response is transmitted in a separate subsequent bus transaction.

STARVATION: A system condition which occurs when one or more modules perform no useful work for an indefinite period of time due to lack of access to the bus or other system resources.

STRONG SEQUENTIAL CONSISTENCY: A system is strong sequentially consistent if each cache in the system observes all modifications to all cache lines in the same order.

TEMPORAL LOCALITY: The tendency for a program to reference the same memory locations over short time intervals.

TRANSFER LINE SIZE: The size of the block of data transferred to or from main memory in a caching environment.

UNSELECTED SLAVE: A potential slave module that does not recognize its address on the bus during an address transfer.

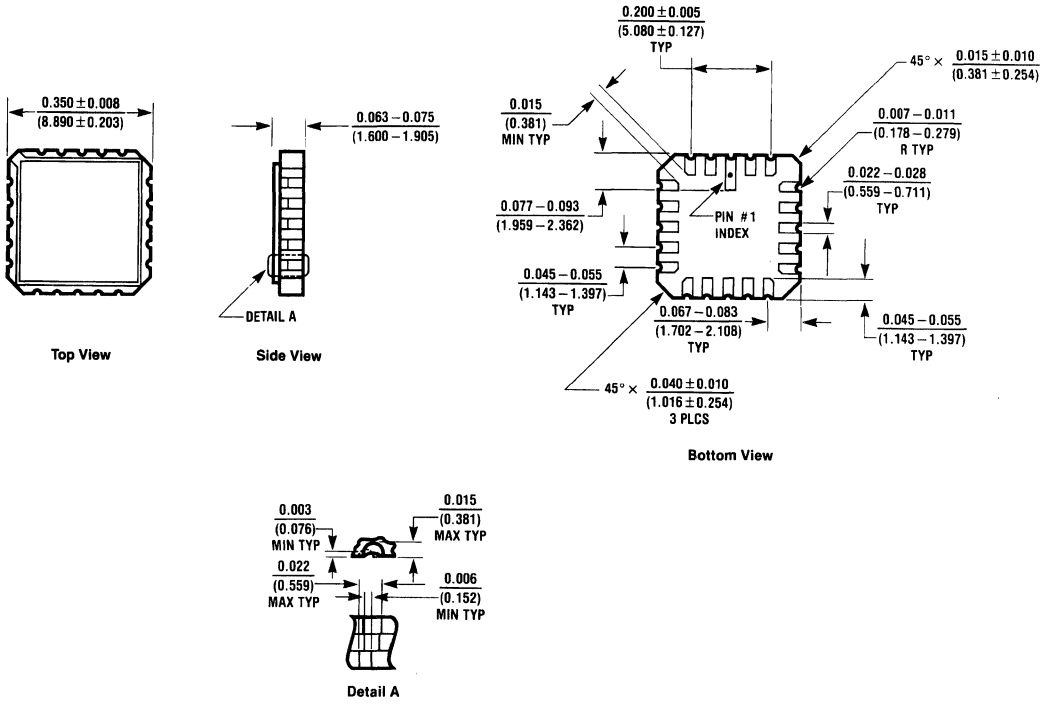
WEAK SEQUENTIAL CONSISTENCY: A system exhibits weak sequential consistency if references to global synchronizing variables are strong sequential consistency, and if no reference to a synchronizing variable is issued by any processor until all previous modifications to global data have been observed by all caches, and if no reference to global data is issued by any processor until all previous modifications to synchronizing variables have been observed by all caches.

WITHHOLDER: A withholder is a potential master that requires control of the bus module and is fairness inhibited.

National Semiconductor

20 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E20A

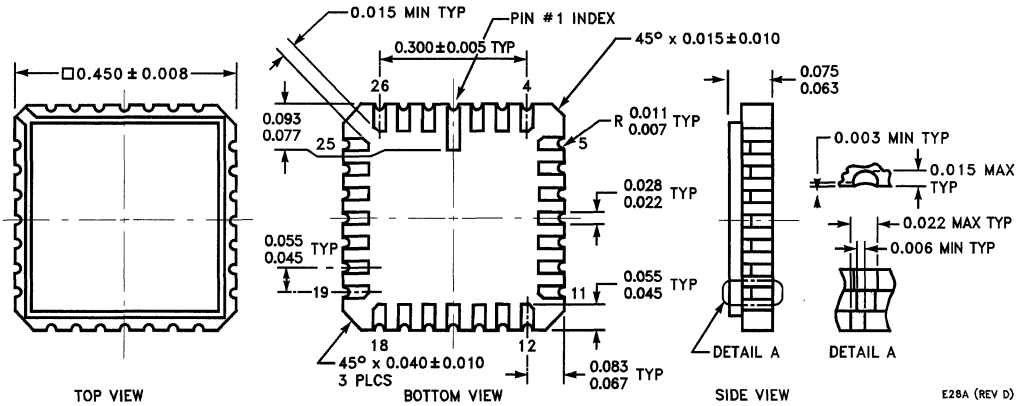
All dimensions are in inches (millimeters)



E20A (REV D)

28 Lead Ceramic Leadless Chip Carrier, Type C
NS Package Number E28A

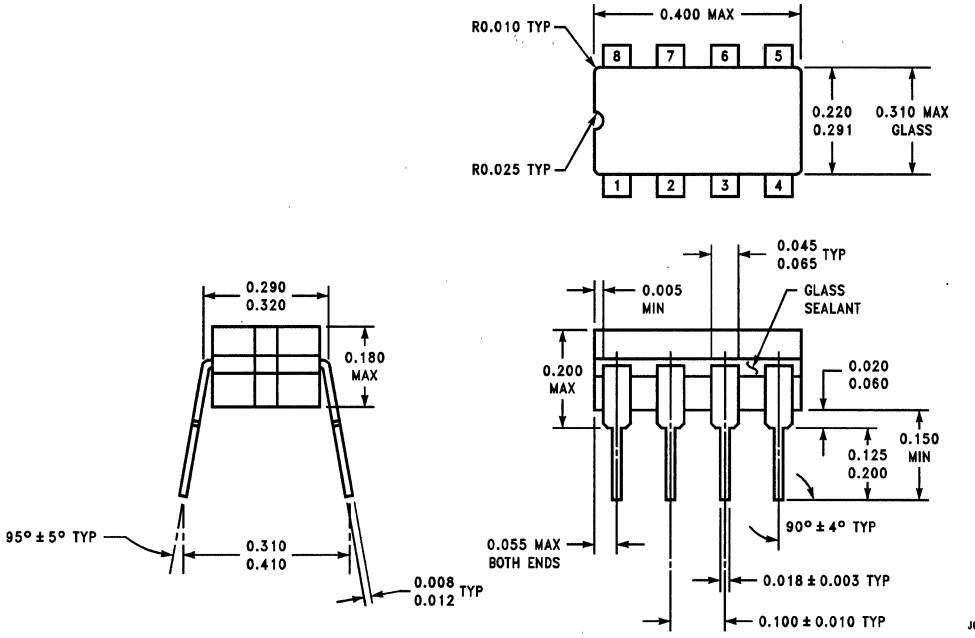
All dimensions are in inches



E28A (REV D)

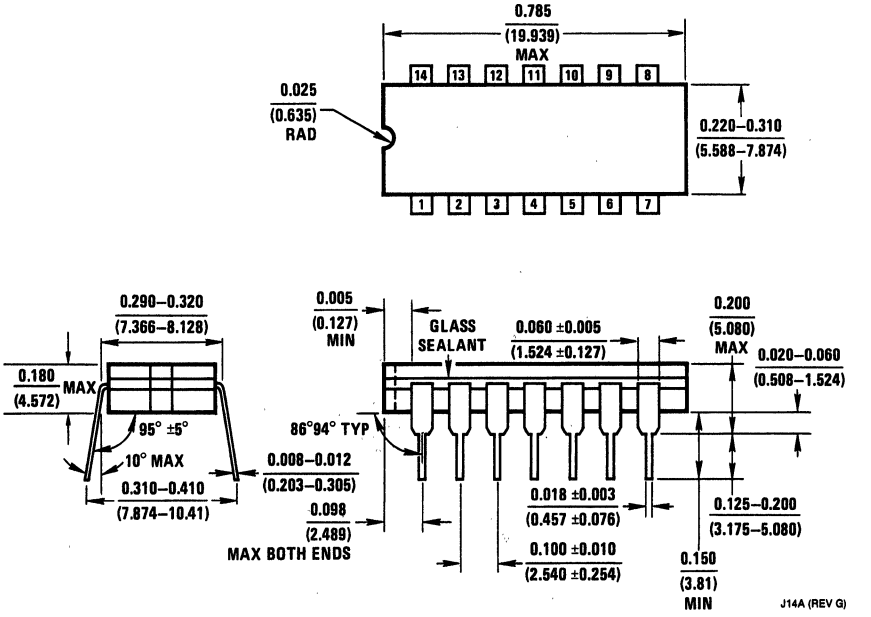
8 Lead Ceramic Dual-in-Line Package
NS Package Number J08A

All dimensions are in inches



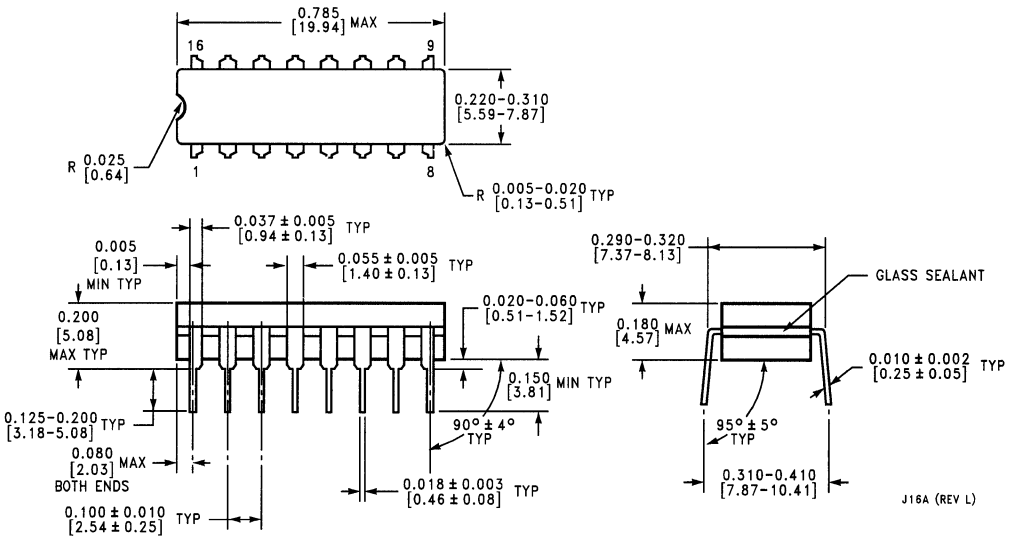
14 Lead Ceramic Dual-in-Line Package
NS Package Number J14A

All dimensions are in inches (millimeters)



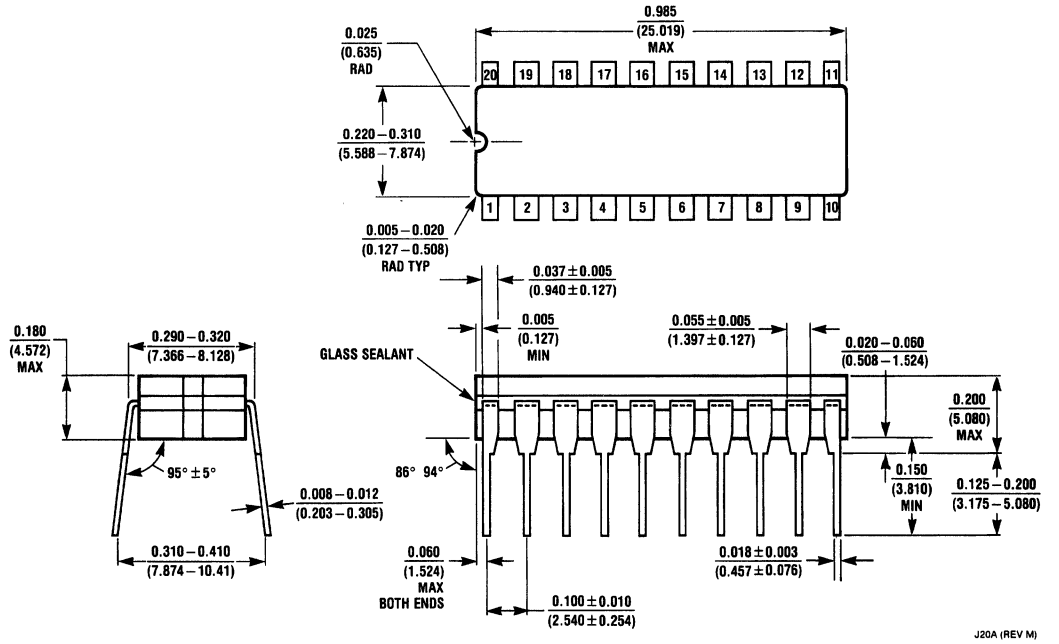
16 Lead Ceramic Dual-in-Line Package
NS Package Number J16A

All dimensions are in inches [millimeters]



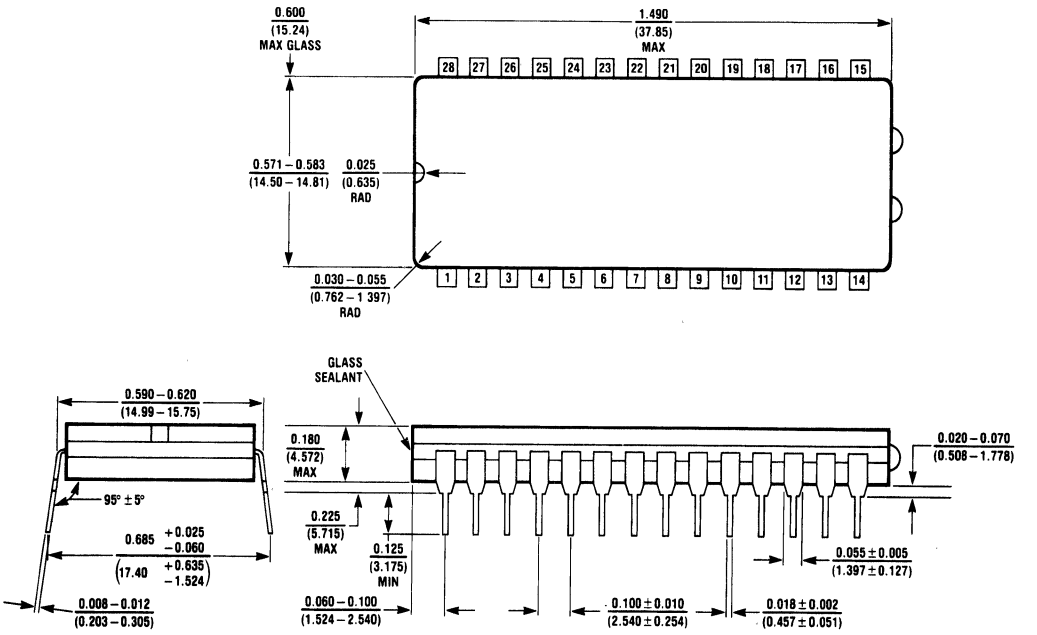
20 Lead Ceramic Dual-in-Line Package
NS Package Number J20A

All dimensions are in inches (millimeters)



28 Lead Ceramic Dual-in-Line Package
NS Package Number J28B

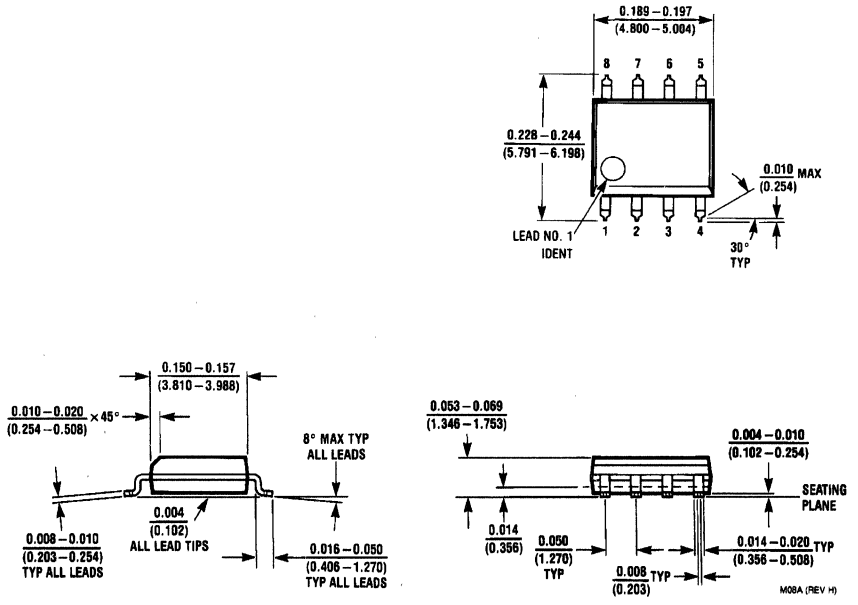
All dimensions are in inches (millimeters)



J28B (REV C)

8 Lead (0.150″ Wide) Molded Small Outline Package, JEDEC
NS Package Number M08A

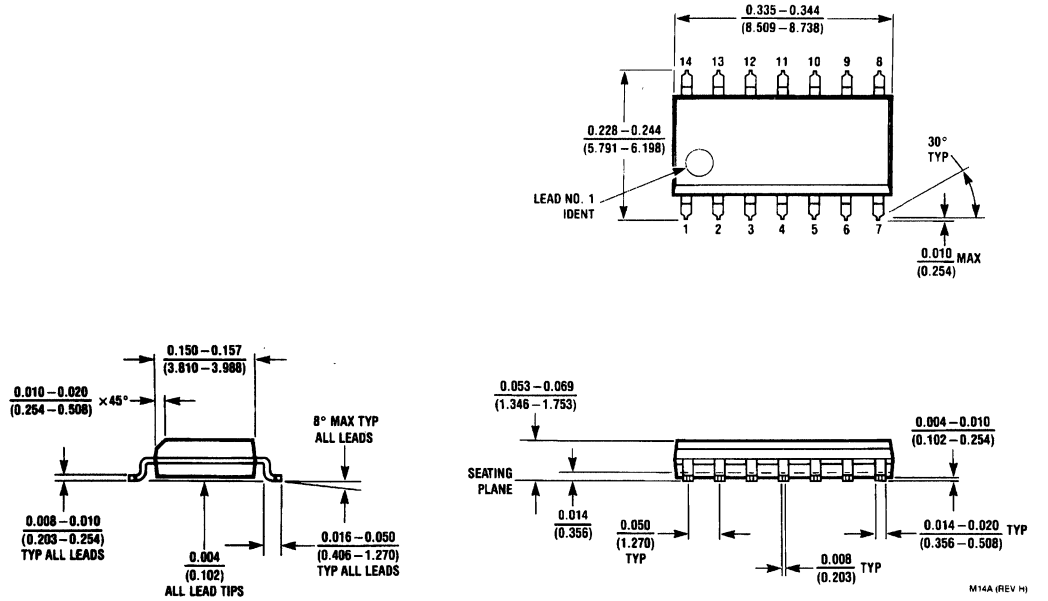
All dimensions are in inches (millimeters)



M08A (REV H)

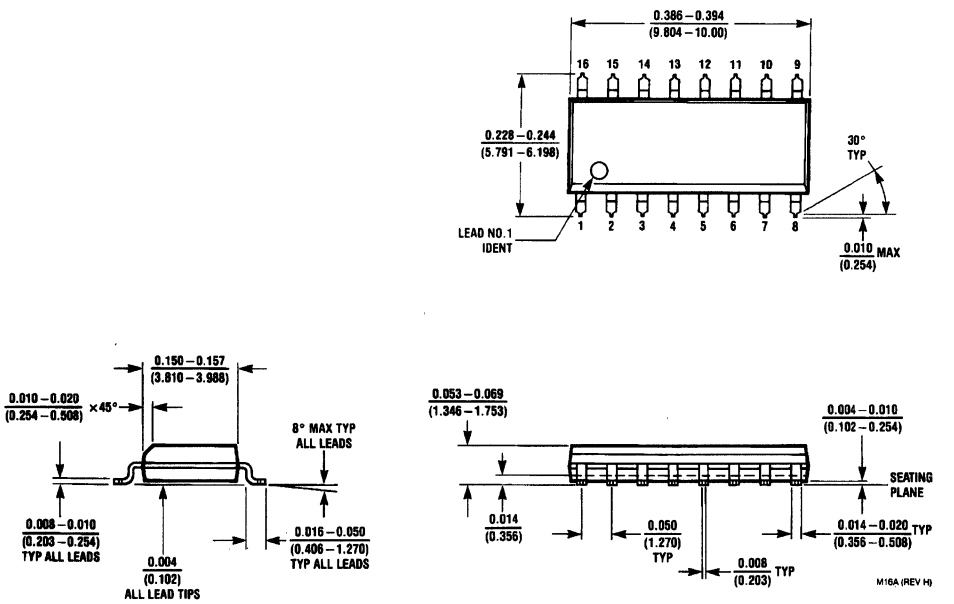
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M14A

All dimensions are in inches (millimeters)



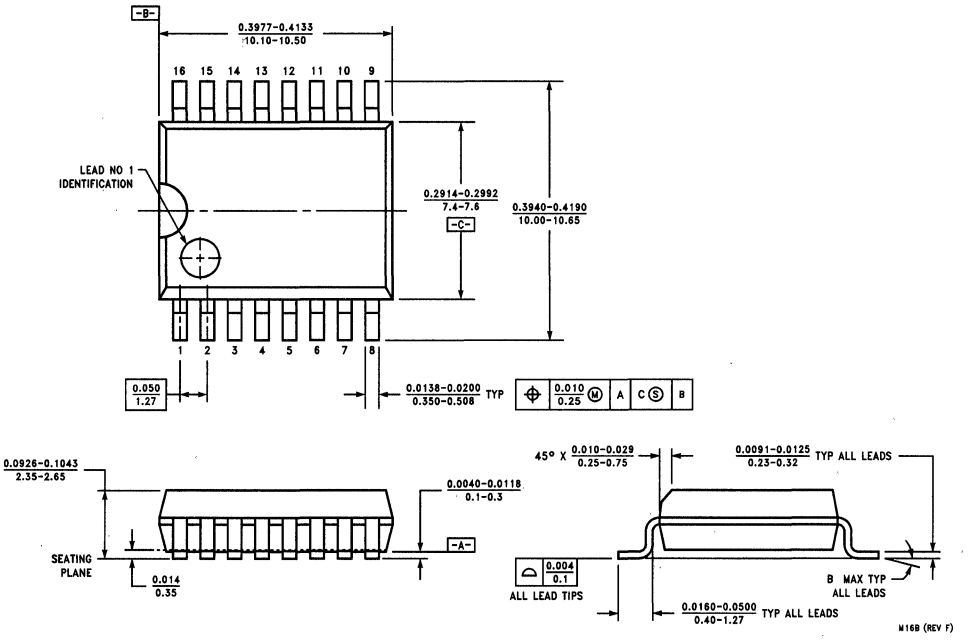
16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A

All dimensions are in inches (millimeters)



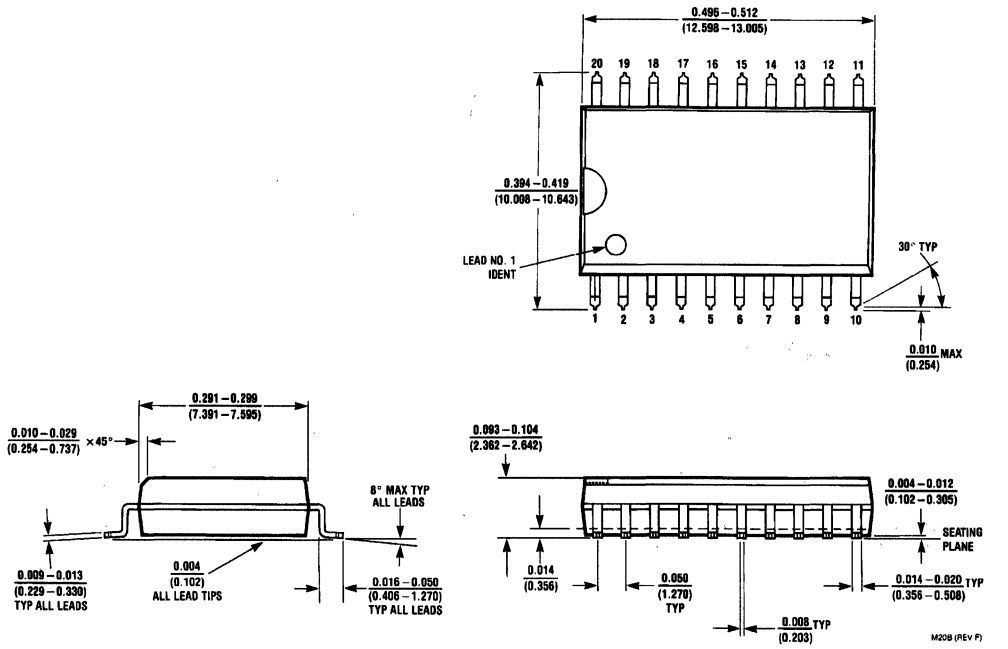
16 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16B

All dimensions are in inches / millimeters



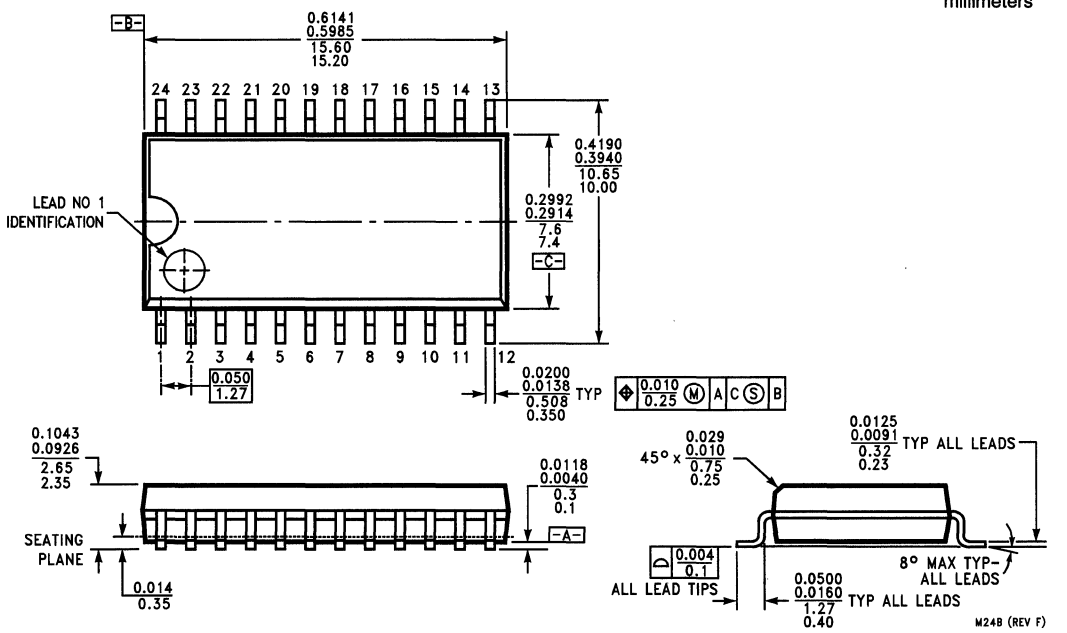
20 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M20B

All dimensions are in inches (millimeters)



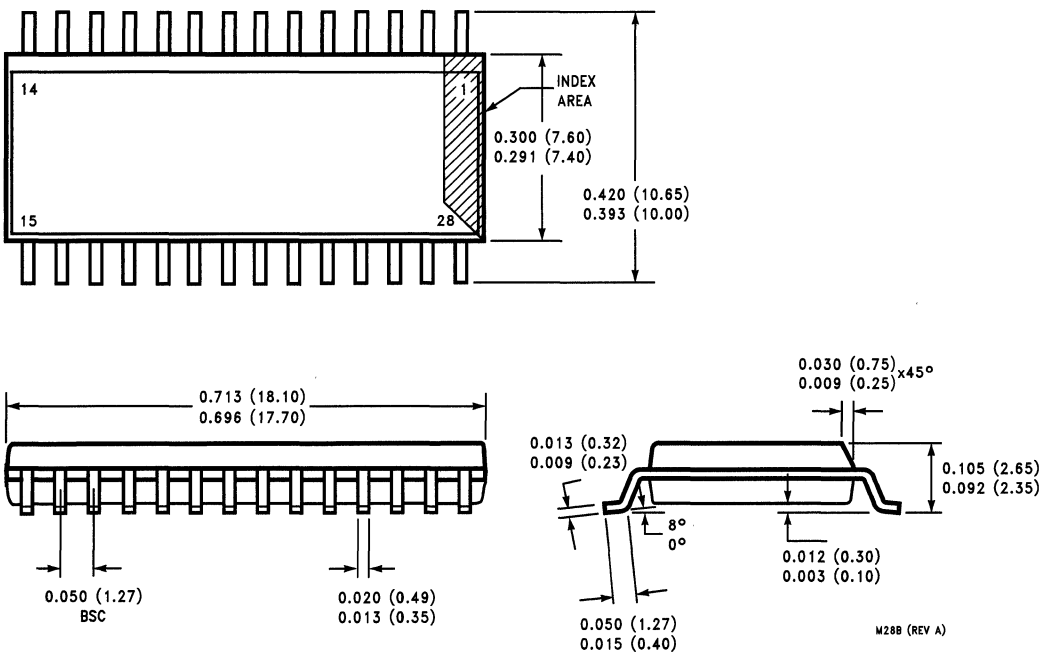
24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



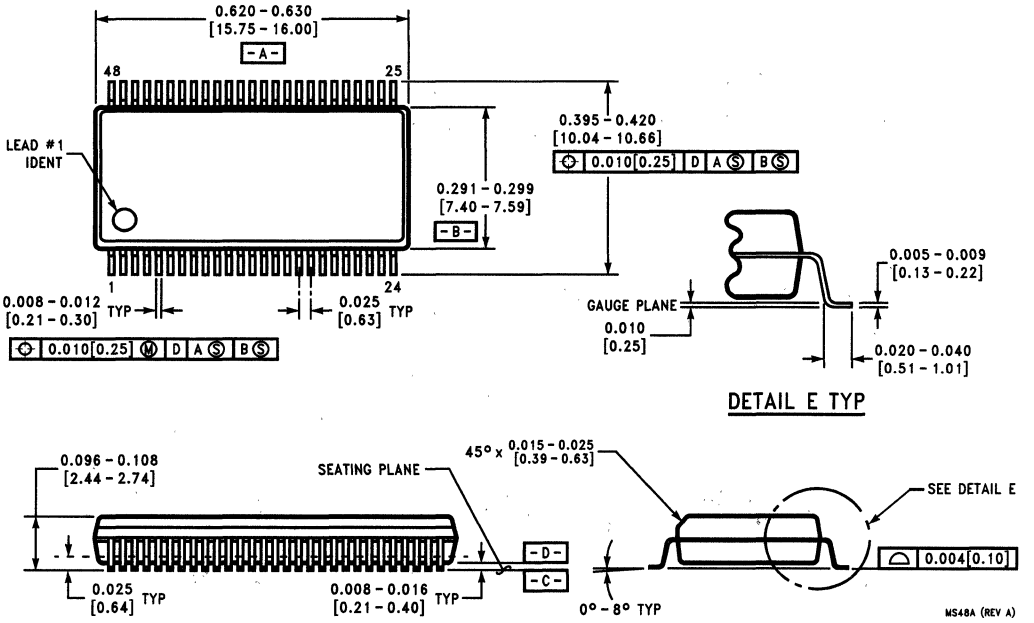
28 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M28B

All dimensions are in inches (millimeters)



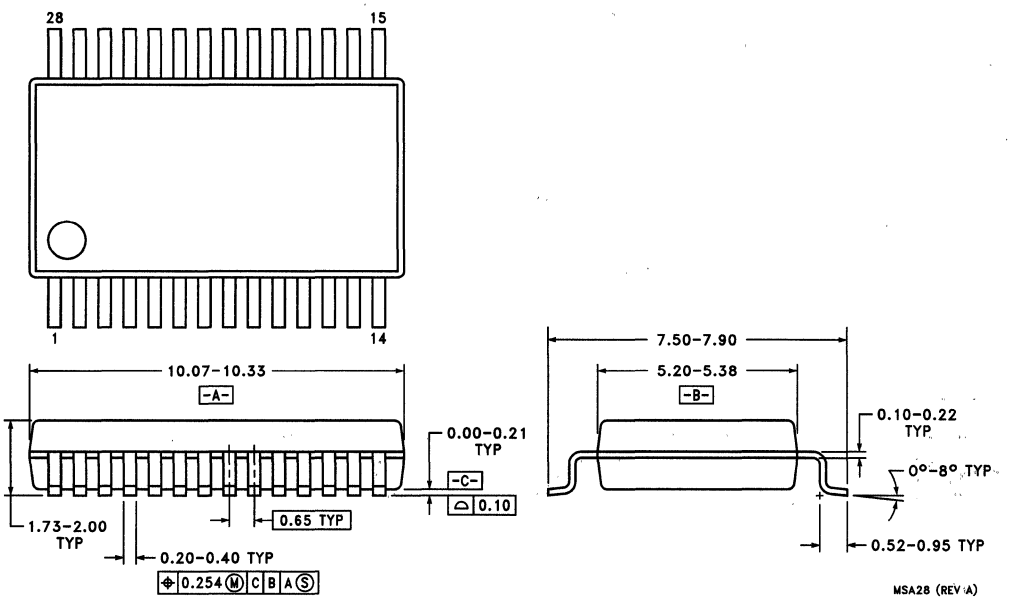
48 Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
NS Package Number MS48A

All dimensions are in inches [millimeters]



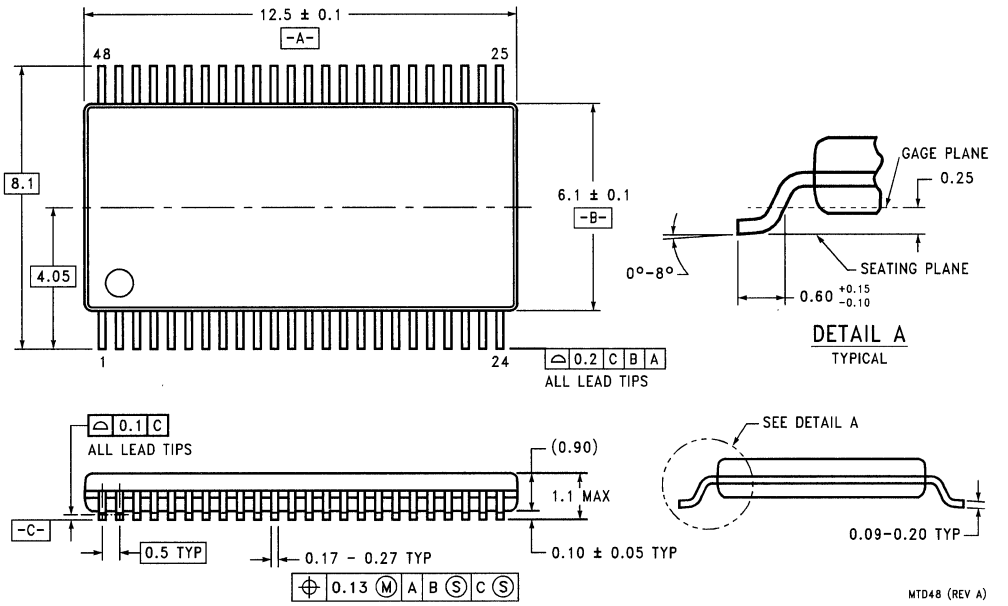
28 Lead Molded Shrink Small Outline Package, EIAJ, Type II
NS Package Number MSA28

All dimensions are in millimeters



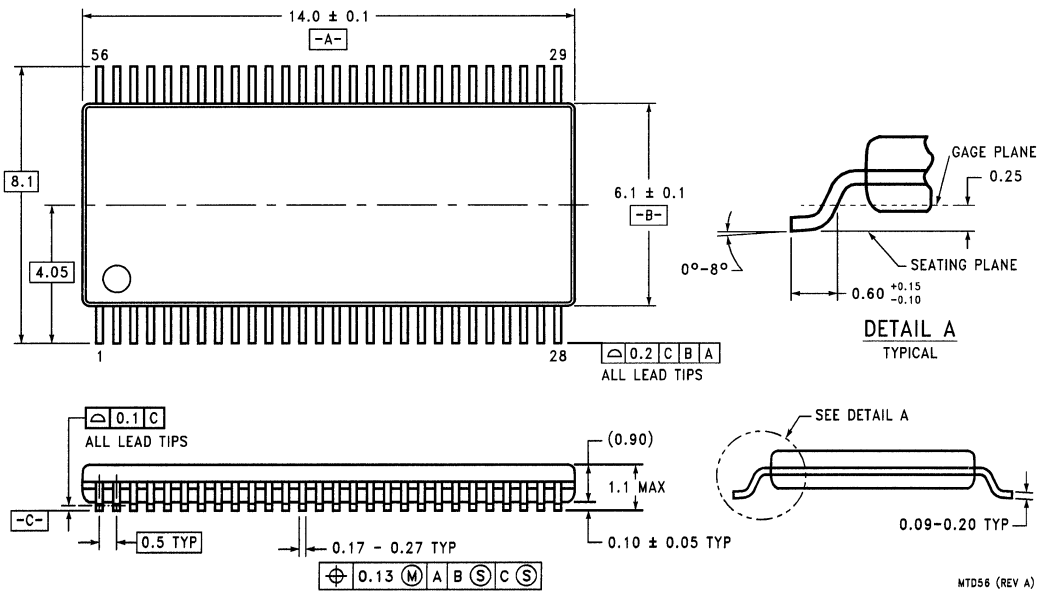
48 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48

All dimensions are in millimeters



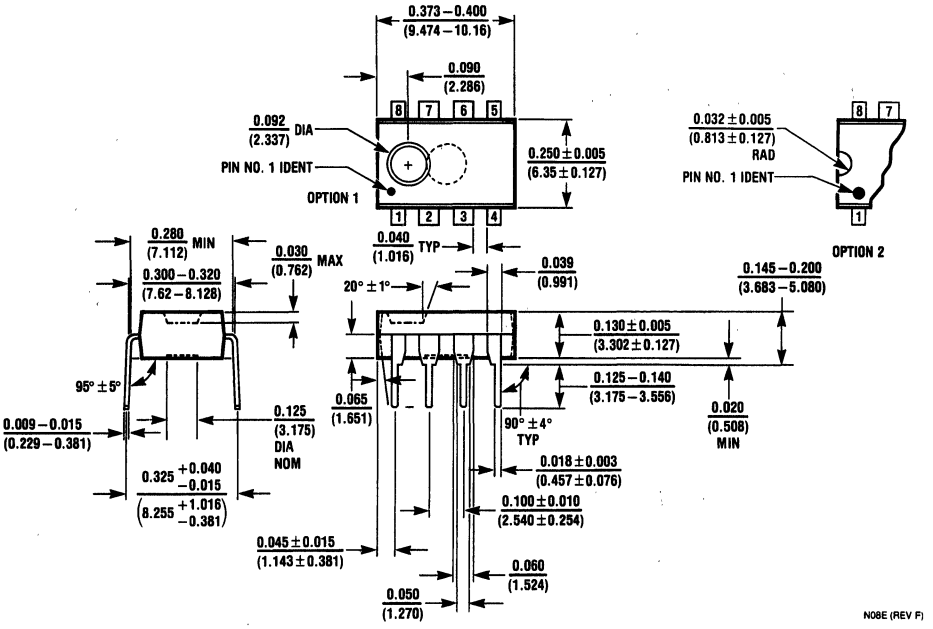
56 Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD56

All dimensions are in millimeters



8 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N08E

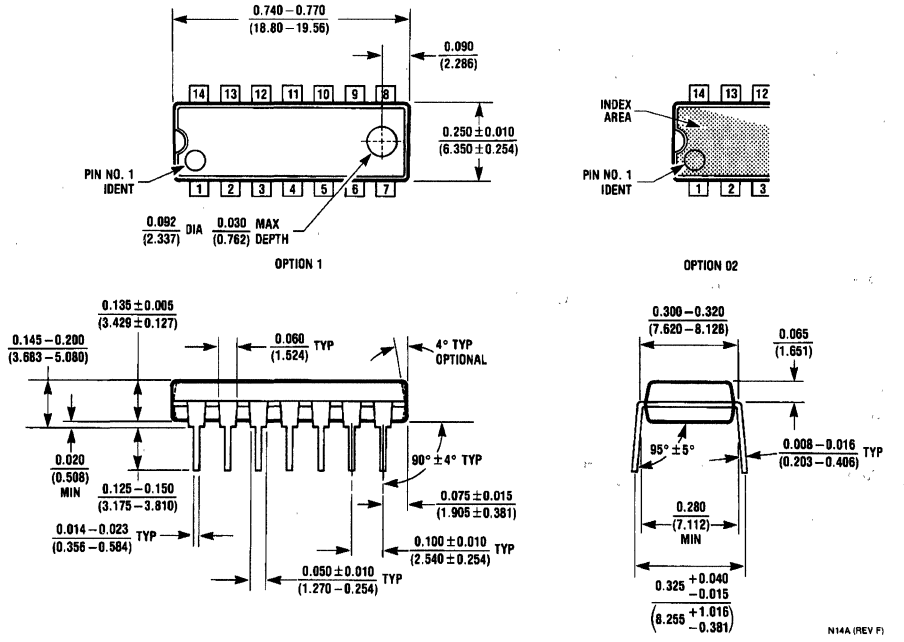
All dimensions are in inches (millimeters)



N08E (REV F)

14 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N14A

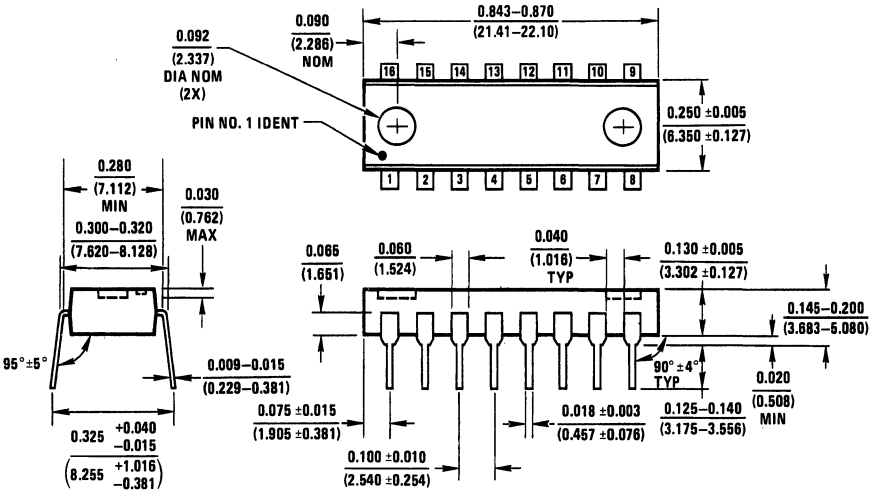
All dimensions are in inches (millimeters)



N14A (REV F)

16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16A

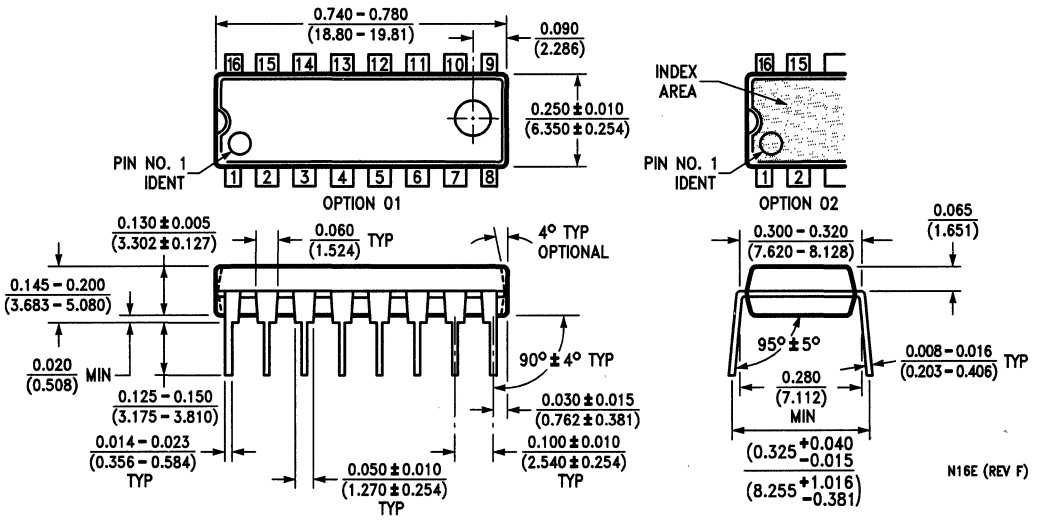
All dimensions are in inches (millimeters)



N16A (REV E)

16 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N16E

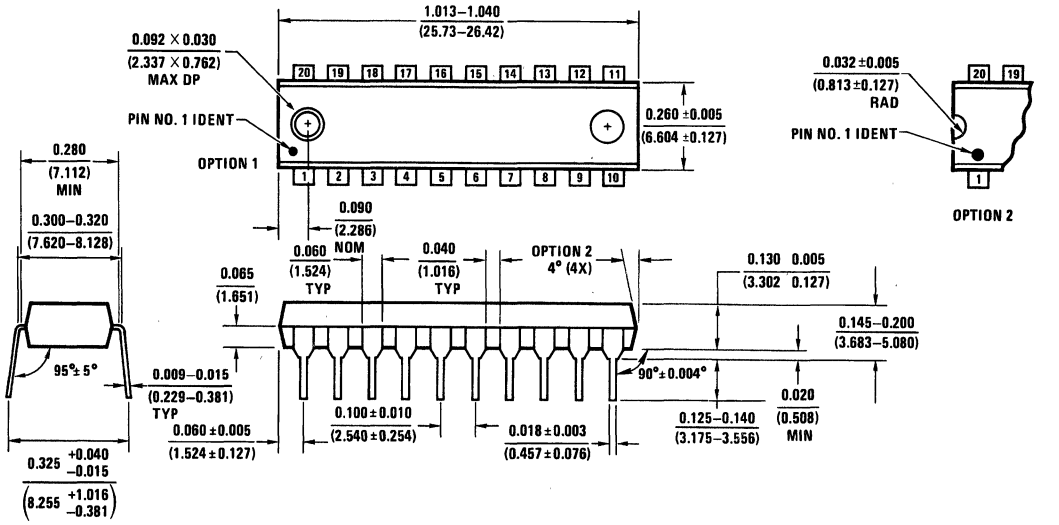
All dimensions are in inches (millimeters)



N16E (REV F)

20 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N20A

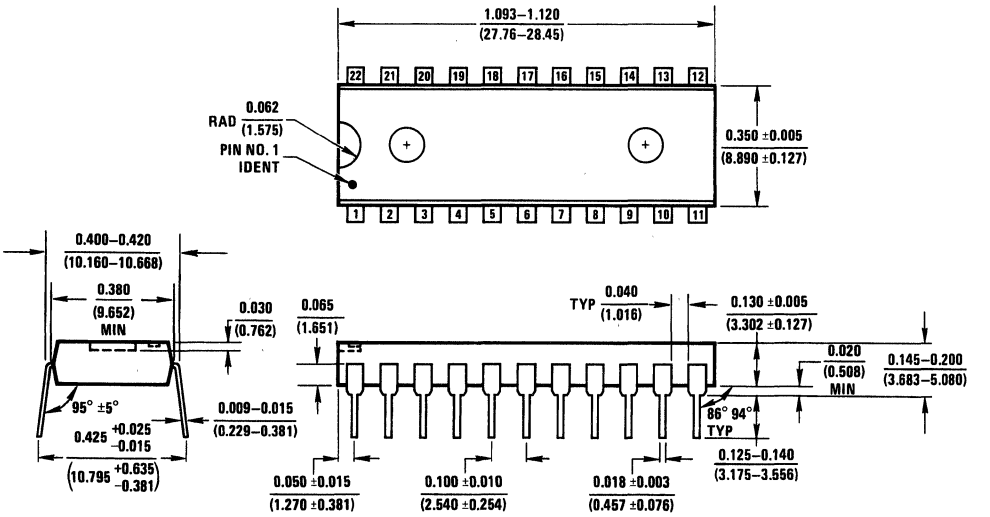
All dimensions are in inches (millimeters)



N20A (REV G)

22 Lead (0.300" Wide) Molded Dual-in-Line Package
NS Package Number N22A

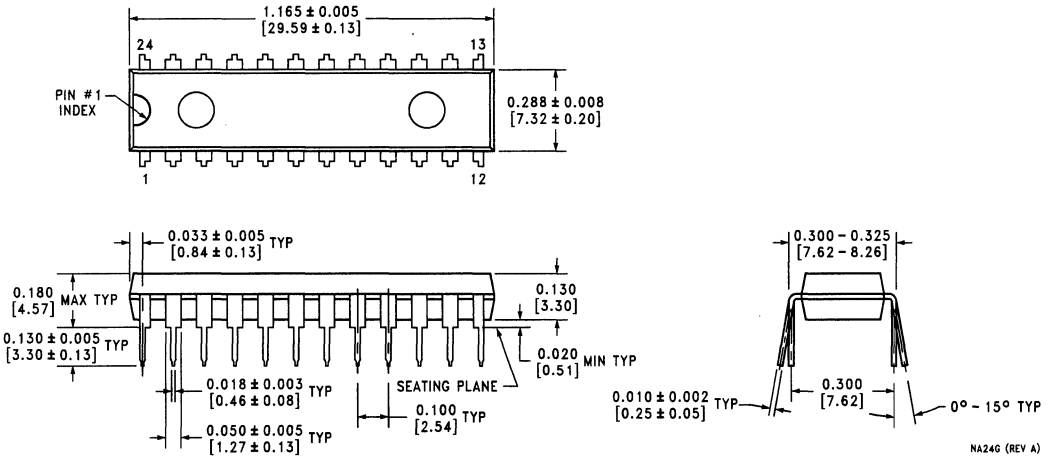
All dimensions are in inches (millimeters)



N22A (REV D)

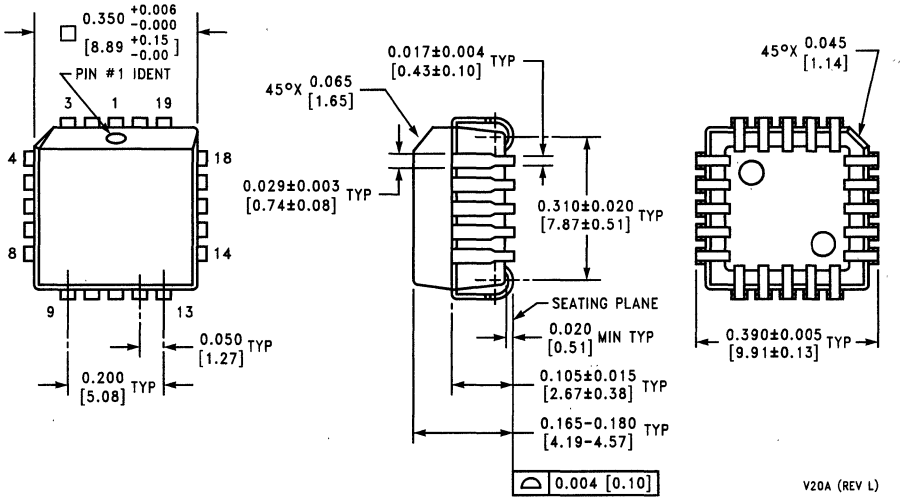
24 Lead Molded Dual-in-Line Package
NS Package Number NA24G

All dimensions are in inches [millimeters]



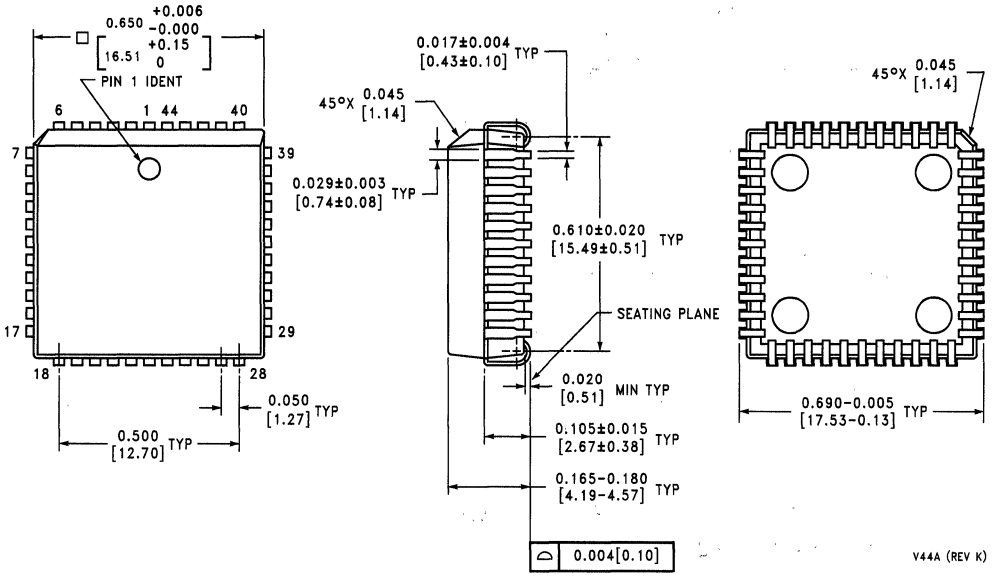
20 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V20A

All dimensions are in inches [millimeters]



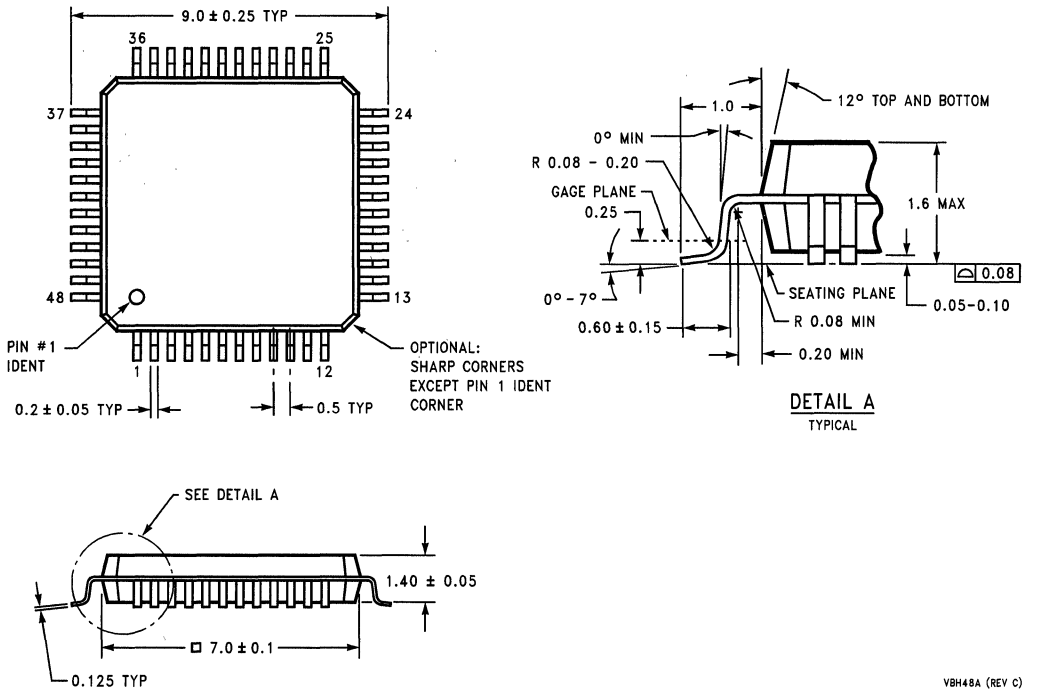
44 Lead Molded Plastic Leaded Chip Carrier
NS Package Number V44A

All dimensions are in inches [millimeters]



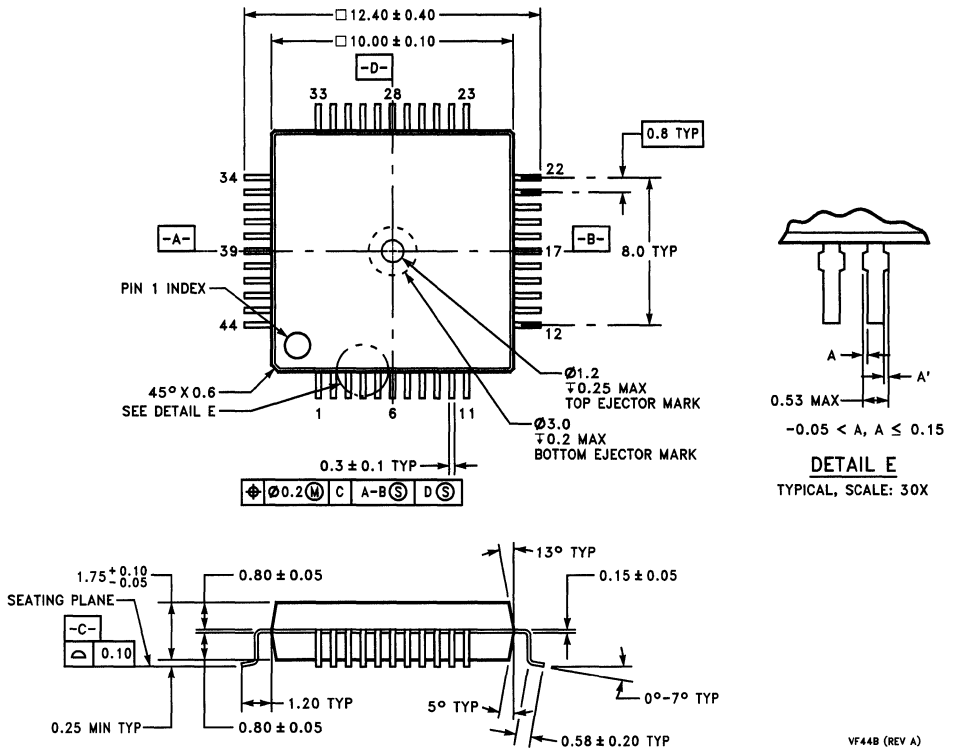
48 Lead (7mm x 7mm) Molded Plastic Quad Flat Package, JEDEC
NS Package Number VBH48A

All dimensions are in millimeters



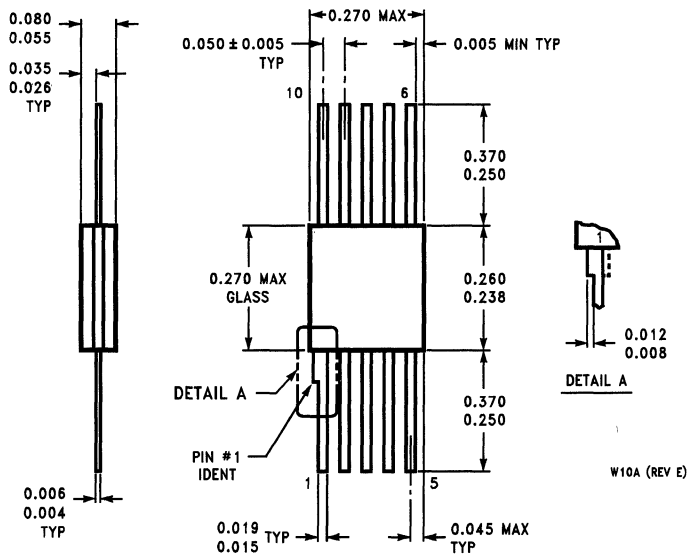
44 Lead Molded Plastic Quad Flat Package, EIAJ
NS Package Number VF44B

All dimensions are in millimeters



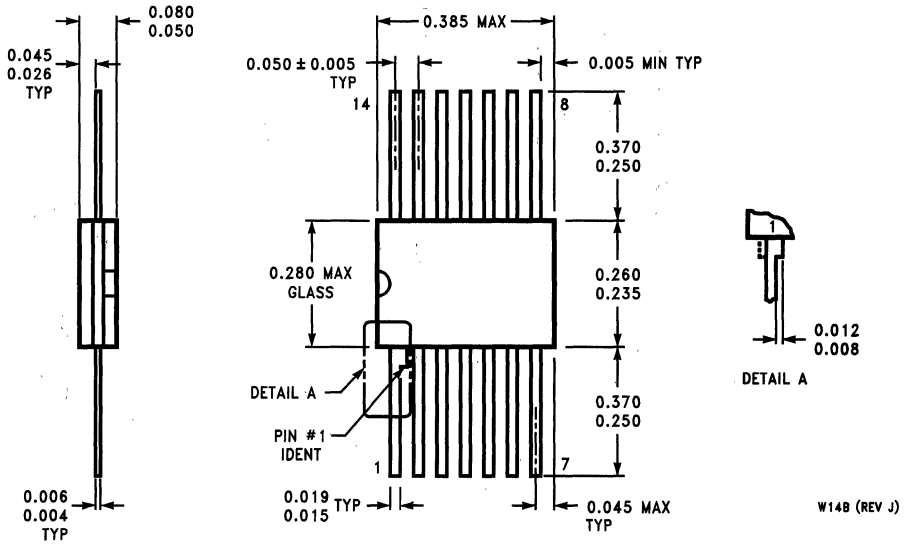
10 Lead Cerpack
NS Package Number W10A

All dimensions are in inches



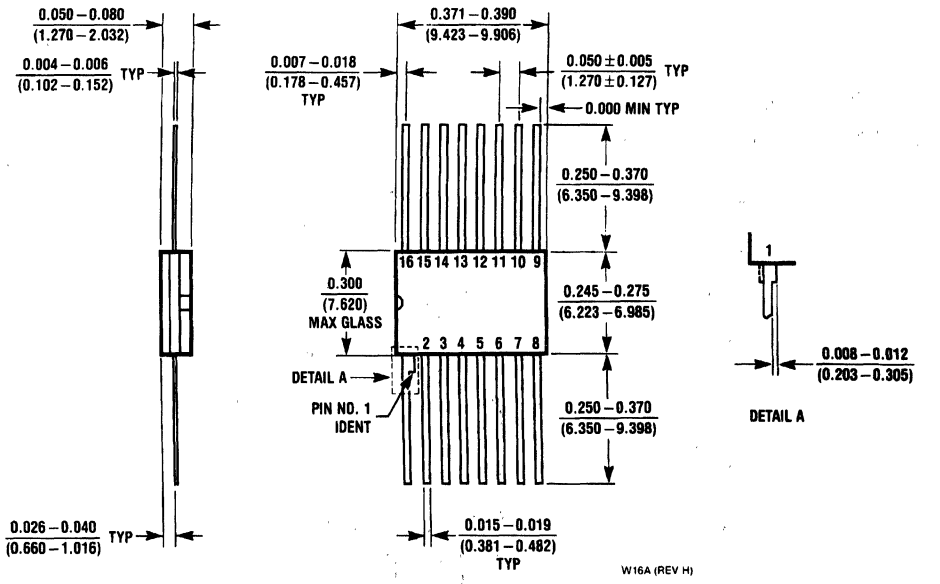
14 Lead Ceramic Flatpack
NS Package Number W14B

All dimensions are in inches



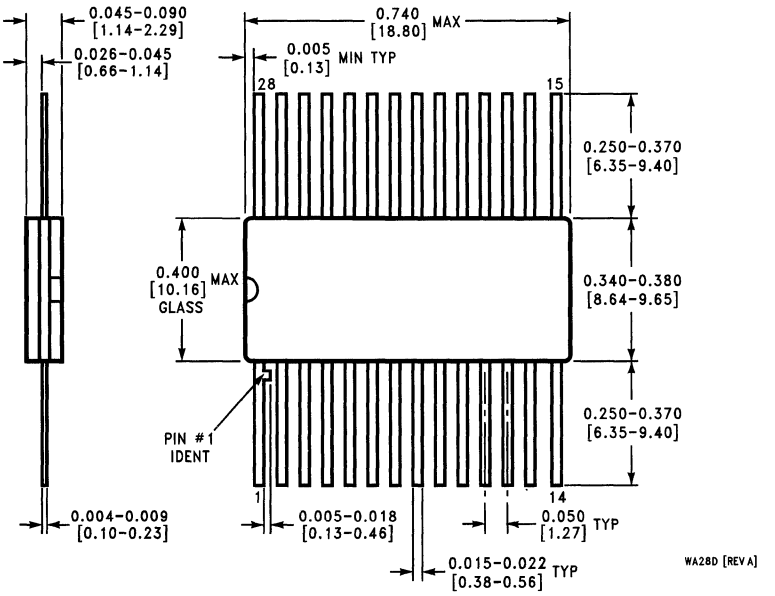
16 Lead Ceramic Flatpack
NS Package Number W16A

All dimensions are in inches (millimeters)



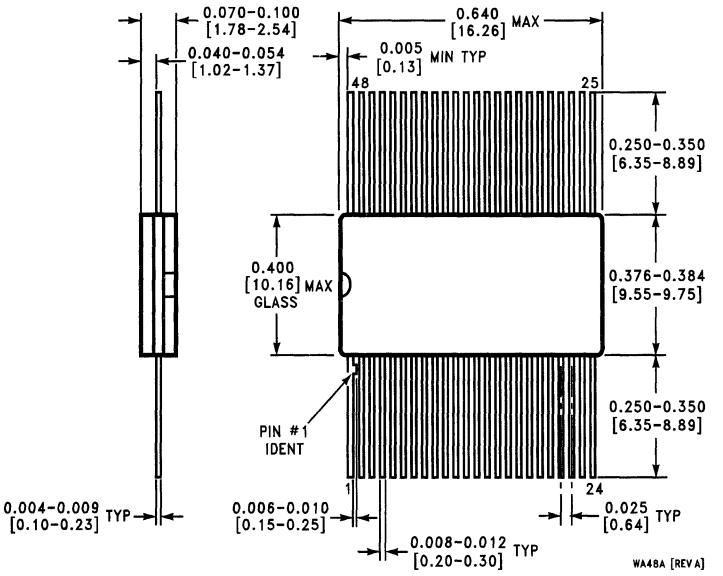
28 Lead Cerpack
NS Package Number WA28D

All dimensions are in inches [millimeters]



48 Lead Cerpack
NS Package Number WA48A

All dimensions are in inches [millimeters]



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