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Edge Index by Product Family

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*TV Game Kit #SK1115 includes this circuit

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SECTION 1
CLOCKS

Clocks

For additional application information, see AN-143 at the end of this section.

MM5309, MM5311, MM5312, MM5313, MM5314, MM5315 digital clocks

general description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion implanted. depletion mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (4 or 6-digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11V to 19V and do not require a regulated supply. These clocks are packaged in dual-in-line packages.

features

- 50 or 60 Hz operation
- 12 or 24-hour display format
- Leading-zero blanking (12-hour format)
- 7-segment outputs
- Single power supply
- Fast and slow set controls
- Internal multiplex oscillator
- For features of individual clocks, see Table I

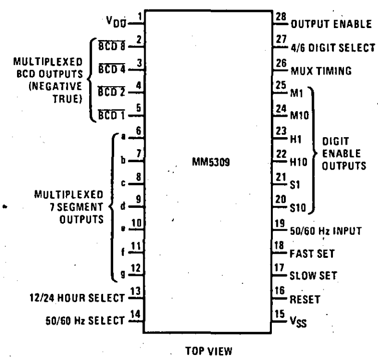
applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Interval Timers

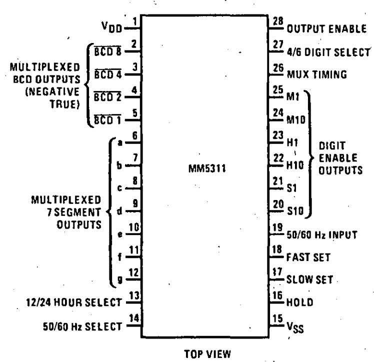
TABLE I.

FEATURES	MM5309	MM5311	MM5312	MM5313	MM5314	MM5315
$\overline{BCD}$ Outputs	X	X	X	X		X
4/6-Digit Display Mode	X	X		X	X	X
Hold Count Control		X		X	X	X
1 Hz Output			X	X		
Output Enable Control	X	X			X	
Reset	X					X

connection diagrams (Dual-In-Line Packages)



Order Number MM5309N
See Package 23



Order Number MM5311N
See Package 23

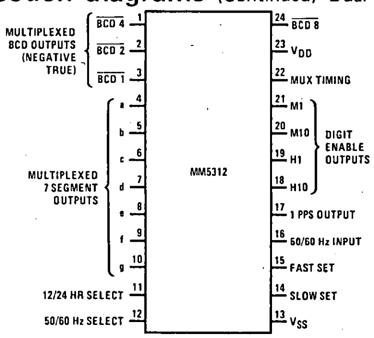
absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} – 20V
Operating Temperature	–25°C to +70°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

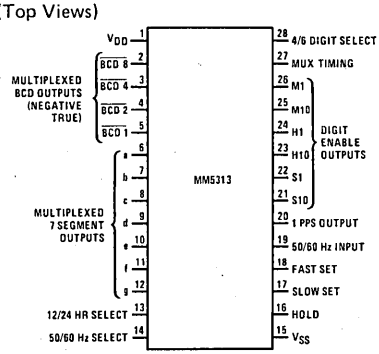
electrical characteristics T_A within operating range, V_{SS} = 11V to 19V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11		19	V
Power Supply Current	V_{SS} = 14V, (No Output Loads)			10	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS}–1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}–10	V
Multiplex Frequency	Determined by External R & C	0.100	1.0	60	kHz
All Logic Inputs	Driven by External Timebase	dc		60	kHz
Logical High Level	Internal Depletion Device to V_{SS}	V_{SS}–1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}–10	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2 kΩ to V_{DD}	2.0		20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100 Ω to V_{SS}	5.0		25	mA sink

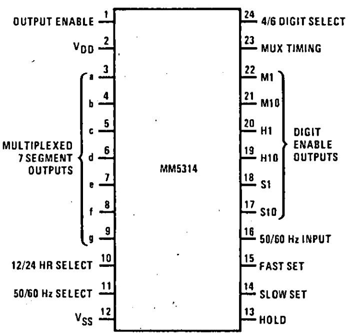
connection diagrams (Continued) Dual-In-Line Packages (Top Views)



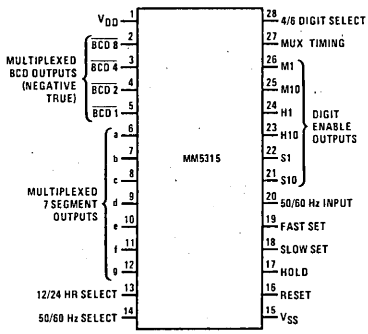
Order Number MM5312N
See Package 22



Order Number MM5313N
See Package 23



Order Number MM5314N
See Package 22



Order Number MM5315N
See Package 23

functional description

A block diagram of the MM5309 digital clock is shown in *Figure 1*. MM5311, MM5312, MM5313, MM5314 and MM5315 clocks are bonding options of MM5309 clock. Table I shows the pin-outs for these clocks.

50 or 60 Hz Input: This input is applied to a Schmitt Trigger shaping circuit which provides approximately 5V of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 10* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 Hz timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal depletion device is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation. As shown in *Figure 1*, the prescale counter provides both 1 Hz and 10 Hz signals, which can be brought out as bonding options.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal depletion devices provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function.

The three gates in the counter chain *(Figure 1)* are used for setting time. During normal operation, gate A connects the shaper output to a prescale counter (÷50 or ÷60); gates B and C cascade the remaining counters. Gate A is used to inhibit the input to the counters for the duration of slow, fast or hold time-setting input activity. Gate B is used to connect the shaper output directly to a seconds counter (÷60), the condition for slow advance. Likewise, gate C connects the shaper output directly to a minutes counter (÷60) for fast advance.

Fast set then, advances hours information at one hour per second and slow set advances minutes information at one minute per second.

12 or 24-Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format. The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal depletion device) selects the 24-hour format.

Output Multiplexer Operation: The seconds, minutes, and hours counters continuously reflect the time of day. Outputs from each counter (indicative of both units and tens of seconds, minutes, and hours) are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 42 leads to interconnect a 6-digit clock and its display (7 segments per digit), only 13 output leads are required. The multiplexer is addressed by a multiplex divider decoder, which is driven by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function and, as controlled by the 4 or 6-digit select input, the divider determines whether data will be output for 4 or 6 digits. A zero-blanking circuit suppresses the zero that would otherwise sometimes appear in the tens-of-hours display; blanking is effective only in the 12-hour format. The multiplexer addresses also become the display digit-enable outputs. The multiplexer outputs are applied to a decoder which is used to address a programmable (code converting) ROM. This ROM generates the final output codes, i.e., $\overline{BCD}$ and 7-segment. The sequential output order is from digit 6 (unit seconds) through digit 1 (tens of hours).

Multiplex Timing Input: The multiplex oscillator is shown in *Figure 2*. Adding an external resistor and capacitor to this circuit via the multiplex timing input (as shown in *Figure 4a*) produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt Trigger in *Figure 2*. *Figure 3* provides guidelines for selecting the external components relative to desired multiplex frequency.

Figure 4 also illustrates two methods of synchronizing the multiplex oscillator to an external timebase. The external RC timing components may be omitted and this input may be driven by an external timebase; the required logic levels are the same as 50 or 60 Hz input.

Reset: Applying V_{DD} to this input resets the counters to 0:00:00.00 in 12-hour format and 00:00:00.00 in 24-hour formats leaving the input unconnected (internal depletion pull-up) selects normal operation.

4 or 6-Digit Select Input: Like the other control inputs, this input is provided with an internal depletion pull-up device. With no input connection the clock outputs data for a 4-digit display. Applying V_{DD} to this input provides a 6-digit display.

Output Enable Input: With this pin unconnected the $\overline{BCD}$ and 7-segment outputs are enabled (via an internal depletion pull-up). Switching V_{DD} to this input inhibits these outputs. (Not applicable to MM5312, MM5313, and MM5315 clocks.)

Output Circuits: *Figure 5a* illustrates the circuit used for the $\overline{BCD}$ and 7-segment outputs. *Figure 5b* shows the digit enable output circuit. *Figure 6* illustrates interfacing these outputs to standard and low power TTL. *Figures 7 and 8* illustrate methods of interfacing these outputs to common anode and common cathode LED displays, respectively. A method of interfacing these clocks to gas discharge display tubes is shown in *Figure 9*. When driving gas discharge displays which enclose more than one digit in a common gas envelope, it is necessary to inhibit the segment drive voltage(s) during inter-digit transitions. *Figure 9* also illustrates a method of generating a voltage for application to the output enable input to accomplish the required inter-digit blanking.

functional description (Continued)

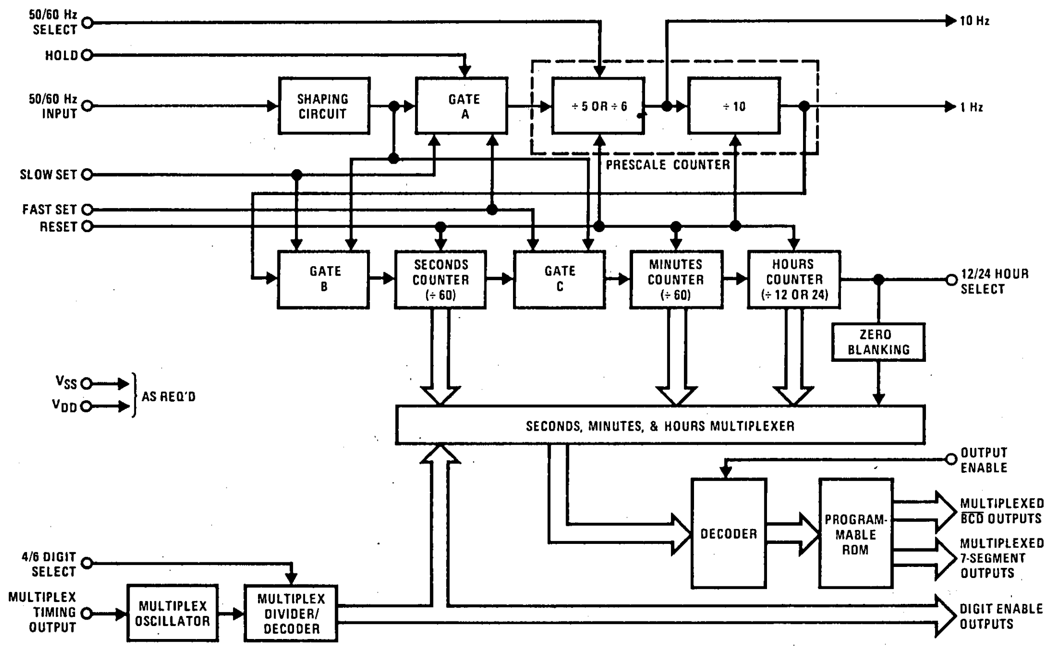


FIGURE 1. MM5309 Digital Clock Block Diagram

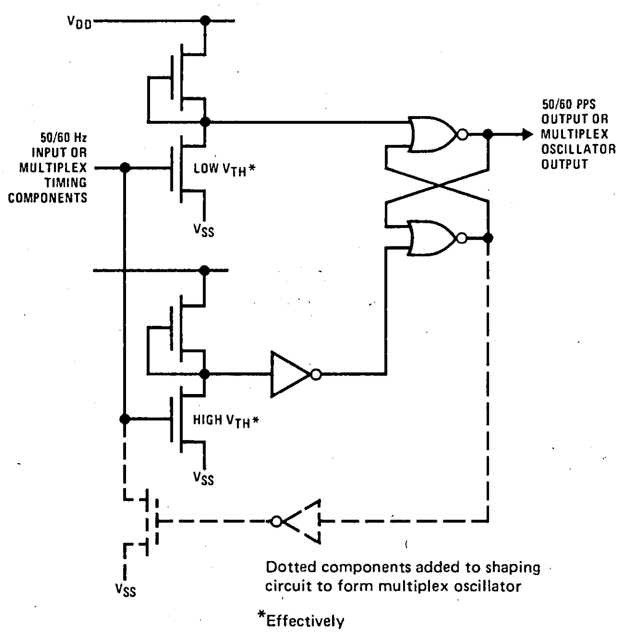


FIGURE 2. 50/60 Hz Shaping Circuit/Multiplex Oscillator

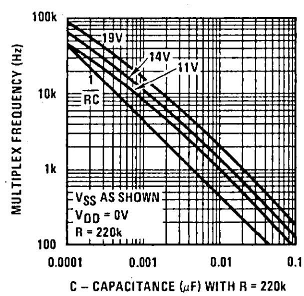


FIGURE 3. Multiplex Timing Component Selection Guide

functional description (Continued)

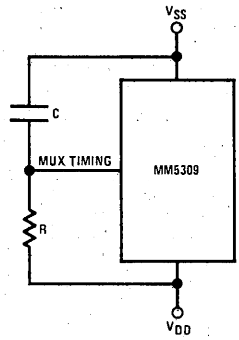


FIGURE 4a. Relaxation Oscillator

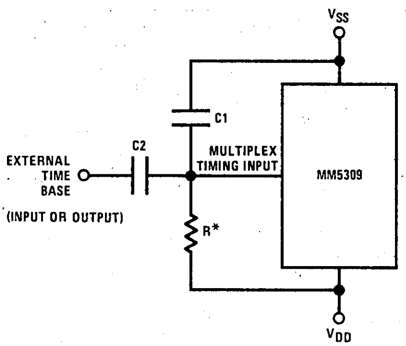


FIGURE 4b. External Time Base

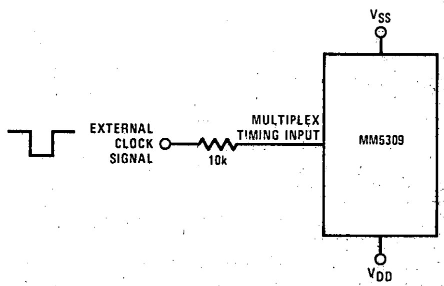


FIGURE 4c. External Clock

Note. Free running frequency should be set to run slightly lower than system frequency over temperature. External time base may be input or output.
* R=100k.

FIGURE 4. Synchronizing or Triggering Multiplex Oscillators

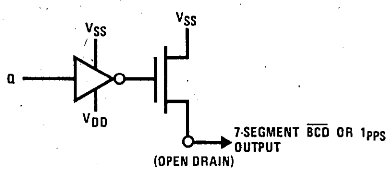


FIGURE 5a

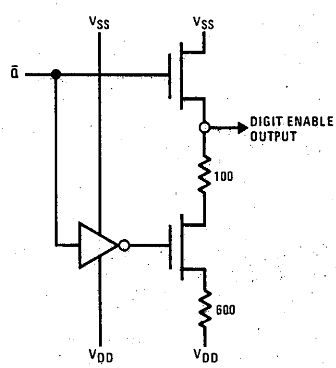
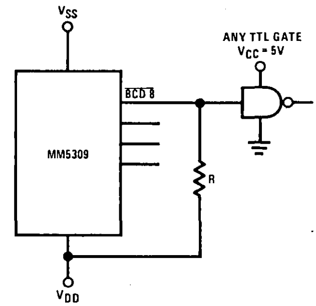


FIGURE 5b

FIGURE 5. Output Circuits

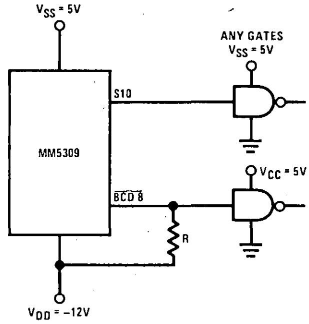
functional description (Continued)

MOS to Low Power TTL Interface



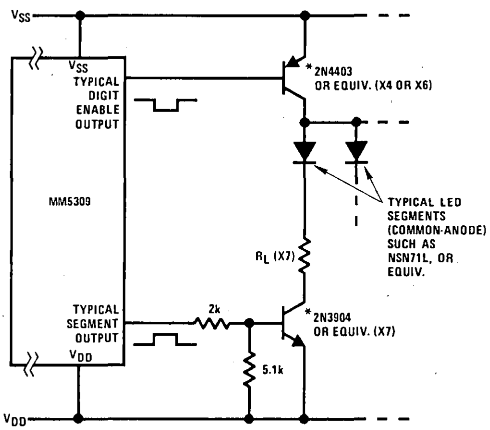
For $V_{SS} = 5$, $V_{DD} = 12$, $R = 10k$
For $V_{SS} = 10$ to $17V$, V_{DD} = Gnd, $R = 3k$

MOS to TTL Interface



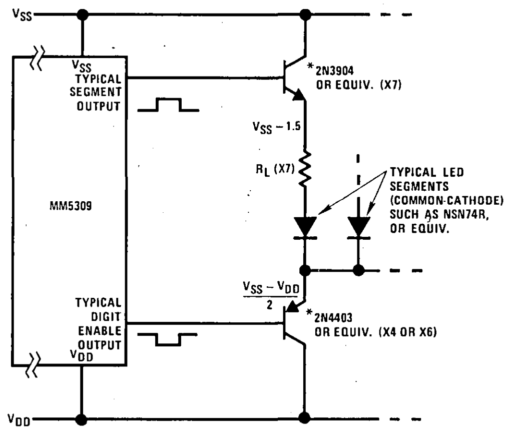
For $V_{SS} = 5$, $V_{DD} = -12$, $R = 7.5k$
Note. Digit select will drive TTL directly when 5, −12 supplies are used.

FIGURE 6. Interfacing TTL



$$R_L = \frac{V_{SS} - V_{DD} \quad V_F \quad 0.6V}{N(I_F)}$$

Where R_L as in kΩ
And V_F = forward drop of LED
0.6V ≈ voltage drop of transistors
N = number of digits in display
I_F = required average LED current



$$R_L = \frac{(V_{SS} \, V_{DD})/2 \; V_F \; 1.5V}{N(I_F)}$$

Where R_L is in kΩ
And V_F = forward drop of LED
0.9V = voltage drop of transistors
N = number of digits in display
I_F = required average LED current

*Transistors may be replaced by DM75491, DM75492, DM8861, DM8863 or equivalent segment/digit drivers.

FIGURE 7. Interfacing Common Anode LED Displays

FIGURE 8. Interfacing Common Cathode LED Displays

functional description (Continued)

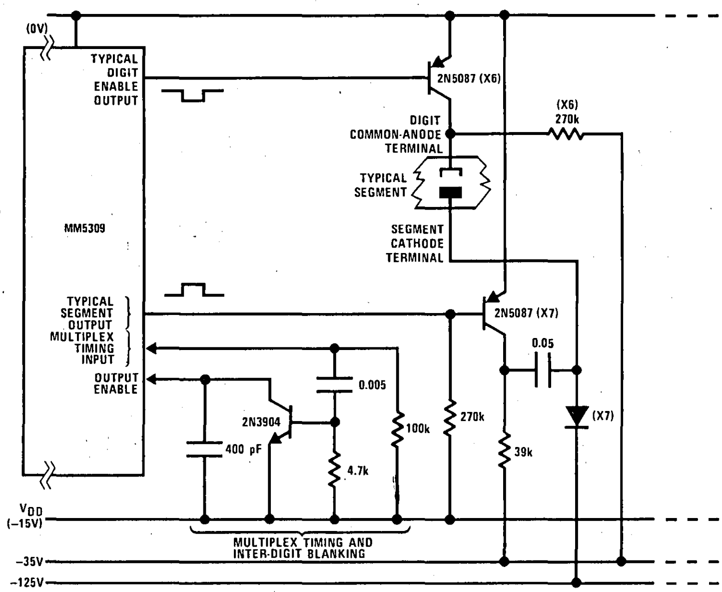


FIGURE 9. Interface Panaplex II* Neon Display Tube

*TM of Burroughs Corp.

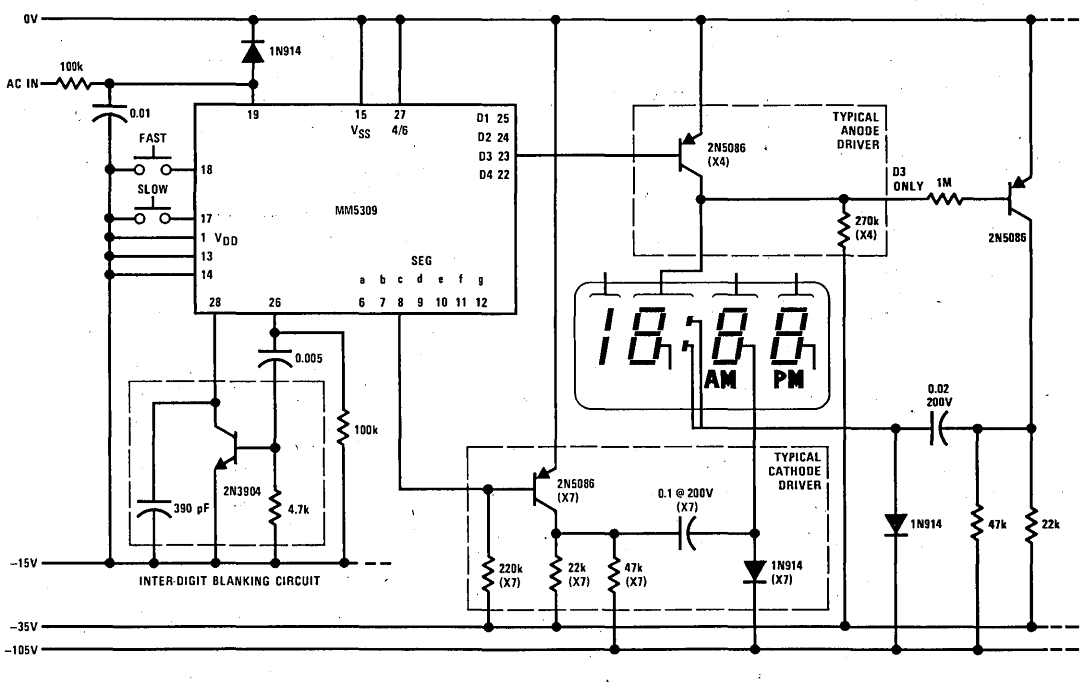


FIGURE 10. MM5309 Driving Gas Discharge Display, Typical Applications

MM5316 digital alarm clock

general description

The MM5316 digital alarm clock is a monolithic MOS integrated circuit utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic required to build several types of clocks and timers. Four display modes (time, seconds, alarm and sleep) are provided to optimize circuit utility. The circuit interfaces directly with 7-segment fluorescent tubes, and requires only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, sleep (e.g., timed radio turn off), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The device operates over a power supply range of 8–29V and does not require a regulated supply. The MM5316 is packaged in a 40-lead dual-in-line package.

features

- 50 or 60 Hz operation
- Single power supply
- Low power dissipation (36 mW at 9V)
- 12 or 24-hour display format
- AM/PM outputs, Leading-zero blanking } 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Blanking/brightness control capability
- Elimination of illegal time display at turn on
- Direct interface to fluorescent tubes
- 9-minute snooze alarm
- Presettable 59-minute sleep timer

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block and connection diagrams

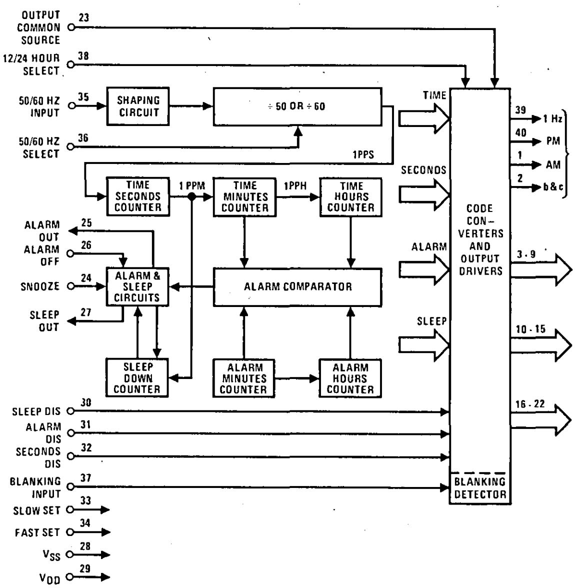
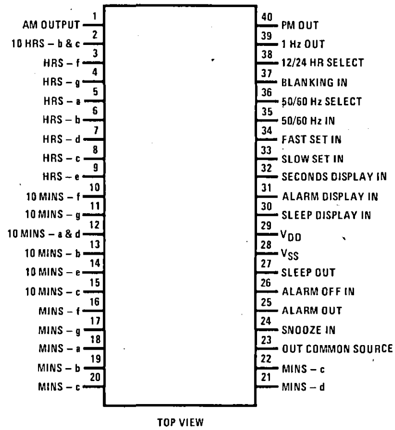


FIGURE 1.

Dual-In-Line Package



Order Number MM5316N
See Package 24

FIGURE 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 30V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 21V to +29V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	21		29	V
Power Supply Current	No Output Loads				
	V_{SS} = 8V			4	mA
	V_{SS} = 29V			5	mA
Counter Operation Voltage		8		29	V
50/60 Hz Input Frequency Voltage		dc	50 or 60	10k	Hz
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+1	V
Blanking Input Voltage					
Logical High Level		V_{SS}−1.5	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−4	V
All Other Input Voltages					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Device to V_{DD}	V_{DD}	V_{DD}	V_{DD}+2	V
Power Failure Detect Voltage	(V_{SS} Voltage)	10		20	V
Output Currents, 1 Hz Display	V_{SS} = 21V to 29V, Output Common = V_{SS}				
Logical High Level	V_{OH} = V_{SS} − 2V	1500			μA
Logical Low Level, Leakage	V_{OL} = V_{DD}			1	μA
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level	V_{OH} = V_{SS} − 2V	1000			μA
Logical Low Level, Leakage	V_{OL} = V_{DD}			1	μA
All Other Display, Alarm and Sleep Outputs					
Logical High Level	V_{OH} = V_{SS} − 2V	500			μA
Logical Low Level, Leakage	V_{OL} = V_{DD}			1	μA

functional description

A block diagram of the MM5316 digital alarm clock is shown in *Figure 1*. The various display modes provided by this clock are listed in Table I. The functions of the setting controls are listed in Table II. *Figure 2* is a connection diagram. The following discussions are based on *Figure 1*.

50 or 60 Hz Input (pin 35): A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt Trigger that is designed to provide about 6V of hysteresis. A simple RC filter, such as shown in *Figure 6*, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input (pin 36): A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving pin 36 unconnected; pull-down to V_{DD} is provided by an internal depletion device. Operation at 50 Hz is programmed by connecting pin 36 to V_{SS}.

Display Mode Select Inputs (pins 30–32): In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal pull-down depletion devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs (pins 33 and 34): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal pull-down depletion devices are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, in the 12-hour format (00:00:00 in the 24-hour format), by selecting seconds display and actuating both slow and fast set inputs.

Blanking Control Input (pin 37): Connecting this Schmitt Trigger input to V_{DD} places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display, (see *Figures 3 and 4*). Conversely, V_{SS} applied to this input enables the display.

Output Common Source Connection (pin 23): All display output drivers are open-drain devices with all sources common to pin 23 *(Figure 4)*. When using fluorescent tube displays, V_{SS} or a display brightness control voltage is permanently connected to this pin. Since the brightness of a fluorescent tube display is dependent on the anode (segment) voltage, applying a variable voltage to pin 23 results in a display brightness control. This control is shown in *Figure 6*.

12 or 24-Hour Select Input (pin 38): By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal depletion pull down device is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Segment connections for 10's of hours in 24-hour mode are shown in *Figure 5b*.

Power Fail Indication: If the power to the integrated circuit drops indicating a momentary ac power failure and possible loss of clock, the power fail latch is set. The power failure indication consists of a flashing of the AM or PM indicator at a 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. In the 24-hour format, the power failure indication consists of flashing segments "c" and "f" for times less than 10 hours, and of a flashing segment "c" for times equal to or greater than 10 hours but less than 20 hours; and a flashing segment "g" for times equal to or greater than 20 hours.

Alarm Operation and Output (pin 25): The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver *(Figure 4)*, the MM5316 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input (pin 24) or reset by the alarm "OFF" input (pin 26). If power fail occurs and power comes back up, the alarm output will be in high impedance state.

Snooze Alarm Input (pin 24): Momentarily connecting pin 24 to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm "OFF" Input (pin 26): Momentarily connecting pin 26 to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion device. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at V_{SS}.

Sleep Timer and Output (pin 27): The sleep output at pin 27 can be used to turn off a radio after a

functional description (Continued)

desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output via pin 27, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. The turn off may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the snooze input (pin 24). The output circuitry is the same as the other outputs *(Figure 4)*.

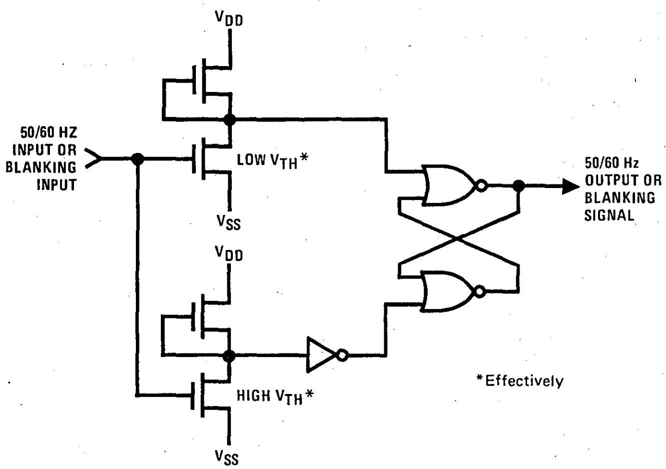
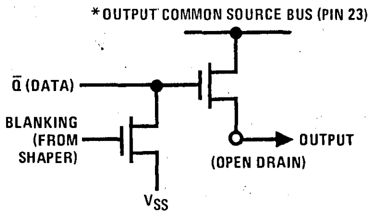
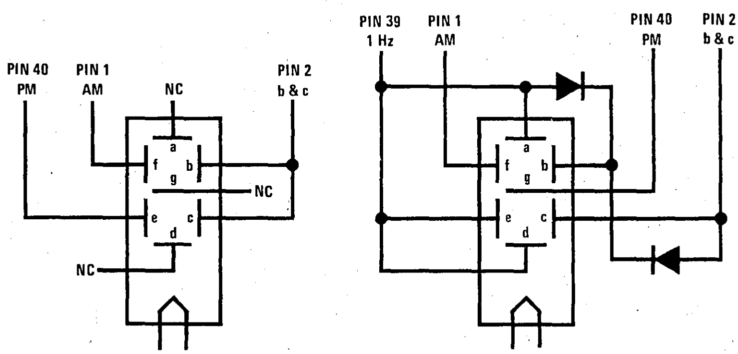


FIGURE 3. 50/60 Hz or Blanking Input Shaping Circuit



*Alarm and sleep output sources are connected to V_{SS}: blanking is not applied to these outputs.

FIGURE 4. Output Circuit



(a) 12-Hour Display Format (b) 24-Hour Display Format

FIGURE 5. Wiring Ten's-of-Hours Digit

functional description (Continued)

TABLE I. MM5316 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE II. MM5316 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 00:00:00 (24-hour format)
Sleep	Slow	Substracts Count at 2 Hz
	Fast	Substracts Count at 60 Hz
	Both	Substracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

typical application

Figure 6 is a schematic diagram of a general purpose alarm clock using the MM5316 and a fluorescent tube display.

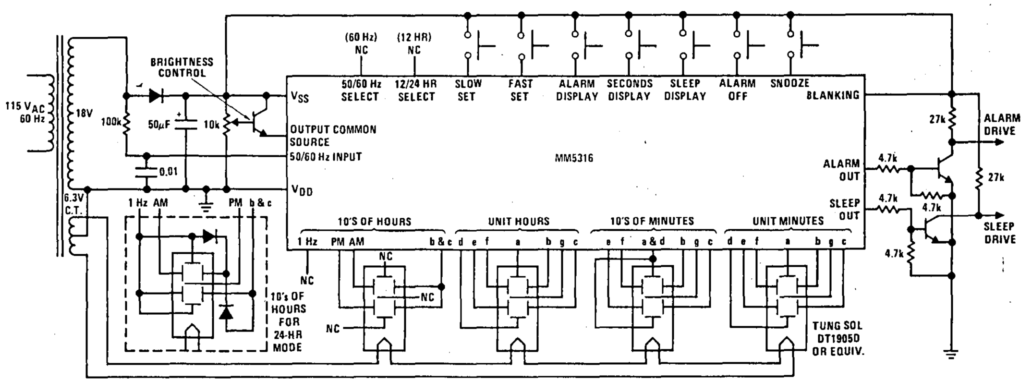


FIGURE 6. Schematic

MM5370, MM5371 digital alarm clocks

general description

The MM5370 and MM5371 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers. Three display modes (time, alarm and sleep) are provided to optimize circuit utility. The circuits interface simply with 7-segment gas discharge displays. The timekeeping function operates from either a 60 Hz (MM5370) or 50 Hz (MM5371) input, and the display format may be either 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drives, alarm enable and sleep (e.g., timed radio turn off). Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. These clocks are packaged in 28-pin dual-in-line packages.

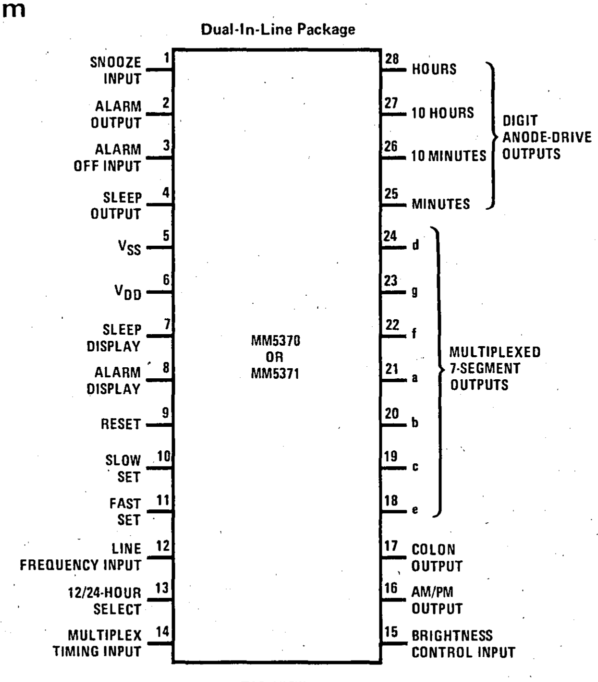
features

- Single power supply
- Low power dissipation
- 12 or 24-hour display format
- Colon drive output
- AM/PM drive output in 12-hour format
- Leading-zero blanking in 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power fail indication
  - Blinking colon—12-hour or 24-hour mode
  - Blinking AM/PM indicators—12-hour only
- Brightness control capability
- Simple interface to gas discharge display
- Presettable 59-minute sleep timer
- 9-minute snooze timer

applications

- Alarm clocks
- Desk clocks
- Clock/radios
- Automobile clocks
- Industrial clocks
- Appliance timers

connection diagram



Order Number MM5370N or MM5371N
See Package 23

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 29V
Voltage at Any Display Output Pin	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −21V to −29V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage					
Functioning Clock	No Output Loads	−8.0	−25	−29	V
Outputs Driving Display		−21		−29	V
Power Supply Current	No Output Loads, (See "Power Supply" Section)			5.0	mA
60 Hz (or 50 Hz) Input Frequency					
MM5370		dc		30k	Hz
MM5371		dc		30k	Hz
60 Hz (or 50 Hz) Input Voltage					
Logical High Level		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+1	V
Brightness Control Voltage					
Logical High Level		V_{SS}−2.0	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−4.0	V
All Other Input Voltages					
Logical High Level		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Load to V_{DD}	V_{DD}	V_{DD}	V_{DD}+2.0	V
Multiplex Frequency	Determined by Ext. RC	500		60k	Hz
	Driven by Ext. Time Base	dc		60k	Hz
Power Failure Detect Voltage	(V_{DD} Voltage)	−3.0		−8.0	V
Output Currents	V_{DD} = −21V to −29V, V_{SS} = 0V				
Digit Anode Outputs					
Logica High Level, ("ON")	V_{OH} = V_{SS} − 5V	8.0			mA
Logical Low Level, ("OFF")	V_{OL} = V_{SS} − 45V			40	μA
Segment Cathode Outputs					
Logical High Level, ("OFF")	V_{OH} = V_{SS} − 5V	2.0			mA
Logical Low Level, ("ON")	V_{OL} = V_{SS} − 45V			10	μA
Alarm and Sleep Outputs					
Logical High Level, ("ON")	V_{OH} = V_{SS} − 2V	1.5			mA
Logical Low Level, ("OFF")	V_{OL} = V_{DD} + 2V	−10			μA

functional description

A block diagram of the MM5370 and MM5371 clocks is shown in *Figure 1*. The various display modes provided by these clocks are listed in Table I. The functions of the controls are listed in Table II. A connection diagram for these devices is shown on page 1. Unless indicated otherwise, the following discussions are based on *Figure 1*.

Power Supply: Even though these clocks do not require a regulated supply, and operate over a wide voltage range, certain factors should be remembered. Power supply voltages between −8V and −21V will provide all functions of the clocks (proper counting, etc.) except output drive capabilities. In order to ensure proper output levels and breakdown voltages it is necessary to provide supply voltages between −21V and −29V. At some point between −7V and −3V, the power fail latch becomes "set". All counters will then hold their count at least 0.5V below this point. This ensures power failure indication before any count is lost. For proper power failure indication, power supply rise time should not exceed 10 V/ms, since faster rise times may be faster than propagation delays within the latch circuitry.

functional description (Continued)

Line Frequency Input (pin 12): A shaping circuit is provided to square the 60 Hz (MM5370) or 50 Hz (MM5371) input. This circuit allows use of a sinewave input. The Schmitt Trigger shaper *(Figure 2)* is designed to provide approximately 6V of hysteresis. A simple RC filter, such as shown in *Figure 8*, should be used to remove possible line-voltage transients that could cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the time-keeping function. A prescale counter divides the line input frequency to obtain a 1 pps timebase.

Display Mode Select Inputs (pins 7 and 8): In the absence of either of these inputs, the display drivers output time-of-day information to the display. Internal pull-down (to V_{DD}) depletion loads allow use of simple SPST switches for connecting these inputs to V_{SS}, thereby selecting alternate display modes. If more than one mode is simultaneously selected, the priorities are are noted in Table I. As shown in *Figure 1* the multiplexed code converter receives time, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the multiplexed code converter inputs and ultimately (via output drivers) to the display.

Time Setting Inputs (pins 10 and 11): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal pull-down depletion loads are provided; application of V_{SS} to these pins effects the control functions. Note that the control functions proper are determined by the selected display mode. An optional hold-time control function can be obtained as shown in *Figure 8.*

Reset Input (pin 9): Applying V_{SS} to this input results in resetting the timekeeping function of the clock; a pull-down depletion load is provided at this input. Time is reset to 12:00 AM in the 12-hour format, or 00:00 in the 24-hour format. See Table II.

12 or 24-Hour Select Input (pin 13): By leaving this pin unconnected, the clock is programmed to provide a 12-hour display format. This format provides for zero-blanking the most significant display digit (ten's of hours). An internal pull-down depletion load is again provided; connecting this pin to V_{SS} programs the 24-hour display format. (See *Figure 8*).

Output Multiplexer Operation: Depending upon the selected display mode (see Table I), outputs from the appropriate internal counter are time division multiplexed to provide digit-sequential access to the data. Thus, instead of requiring 28 leads to interconnect a 4-digit clock and its display (7-segments per digit), only 11 output leads are required. Note that the MM5370 and MM5371 actually provide 13 outputs (4-digit anode drive outputs plus 9 "segment" cathode drive outputs). The two additional "segment" drives are provided to accommodate displays which feature a colon and/or AM/PM indication. (See sections on pin 16 and pin 17). The multiplexed code converter and output drivers are controlled by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function. Each digit anode is sequentially enabled for a time equal to the period of one cycle of the multiplex oscillator frequency.

When driving gas discharge displays which enclose more than one digit in a common gas envelope, it is necessary to either (1) inhibit the segment drive voltage(s) for a short time during inter-digit transitions, or (2) avoid physically adjacent inter-digit transitions. The MM5370 and MM5371 clocks utilize an interlaced output sequence to eliminate the need for inter-digit blanking circuitry and to prevent display arcing problems. The digit sequence is: (1) digit no. 1 (ten's of hours), (2) digit no. 3 (ten's of minutes), (3) blank for one digit time, (4) digit no. 2 (unit hours), (5) digit no. 4 (unit minutes), (6) blank for one digit time, etc. The two blanking intervals are provided to recharge level-translating capacitors located in the display segment drive lines (see *Figure 8*). Both segment data and digit enables are blanked. *Figure 3* is a timing diagram which illustrates output timing.

Multiplex Timing Input (pin 14): The multiplex oscillator is shown in *Figure 4*. Adding an external resistor and capacitor to this circuit via the multiplex timing input produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt Trigger in *Figure 4. Figure 5* provides guidelines for selecting the external components relative to the desired multiplex frequency. *Figure 6* illustrates a method of synchronizing or driving the multiplex oscillator with an external timebase. The external RC timing components may be omitted and this input driven by an external timebase; the required logic levels are the same as the 60 Hz or 50 Hz input.

Output Circuits: All display output drivers are open-drain devices with sources common to V_{SS} (pin 5), see *Figure 7. Figure 8* illustrates interfacing the clock outputs and a gas discharge display.

Brightness Control Input (pin 15): Since display brightness is a function of cathode segment current, a capability of interrupting this current for a variable percentage of the digit interval results in a brightness control. Connecting this Schmitt Trigger input (see *Figure 2*) to V_{DD} places all cathode segment drive voltages at the high level, thereby inhibiting the display. Conversely, V_{SS} applied to this input enables the cathode segment drives. The Schmitt Trigger shaper provides approximately 1V of hysteresis, which facilitates using a waveform such as a sawtooth with a variable slope (or variable dc component) to effect the shaper output duty cycle and, therefore, the display brightness. The control waveform should be derived from the multiplex frequency; a circuit is included in *Figure 8*.

Alarm Operation and Output (pin 2): An alarm comparator (see *Figure 1*) senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. This latch enables the alarm output driver (see *Figure 7*), the output of which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will sound if the latch output is not

functional description (Continued)

temporarily inhibited by another latch set by the snooze input (pin 1) or reset by the alarm "OFF" input (pin 3). Alarm time setting and resetting are outlined in Table II. When initially powered, alarm is in "OFF" state.

Alarm "OFF" Input (pin 3): Momentarily connecting this pin to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion load. The momentary alarm "OFF" input also readies the alarm latch for the next alarm comparator output; the alarm will sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm input should remain at V_{SS}.

Snooze Timer Input (pin 1): Momentarily connecting this pin to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled to V_{DD} by an internal depletion load. The snooze feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Sleep Timer and Output (pin 4): The sleep output at pin 4 can be used to turn off a radio (or other appliance) after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (see Table I) and setting the desired time interval (see Table II). This automatically results in a current-source output via pin 4 which can be used to turn on a radio. When the sleep counter, which counts downwards, reaches 00 minutes a latch is reset and the sleep output drive current is removed, thereby turning off the radio. This turn off also may be manually controlled (at any time in the count-down) by a momentary V_{SS} connection to the snooze input (pin 1). This input is also returned to V_{DD} by a depletion load. The output circuitry is the same as the alarm output (see *Figure 7*).

AM/PM Cathode Output (pin 16): Current with this writing, gas-discharge clock displays are available with two types of AM/PM indications, (1) AM and PM indicators common to digits 3 and 4 respectively; and (2) a PM only indication common to digit 1. *Figure 3* illustrates an AM/PM cathode drive output that is compatible with both display types. Note that this same output also provides a non-blinking (steady) colon drive common to digit two. Power failure is shown by turning off this output at a 1 Hz rate.

Colon Cathode Output (pin 17): As an optional indication of clock operation, some users may prefer to display a 1 Hz activity. As shown in *Figure 3*, a cathode drive output is provided to facilitate a blinking colon.

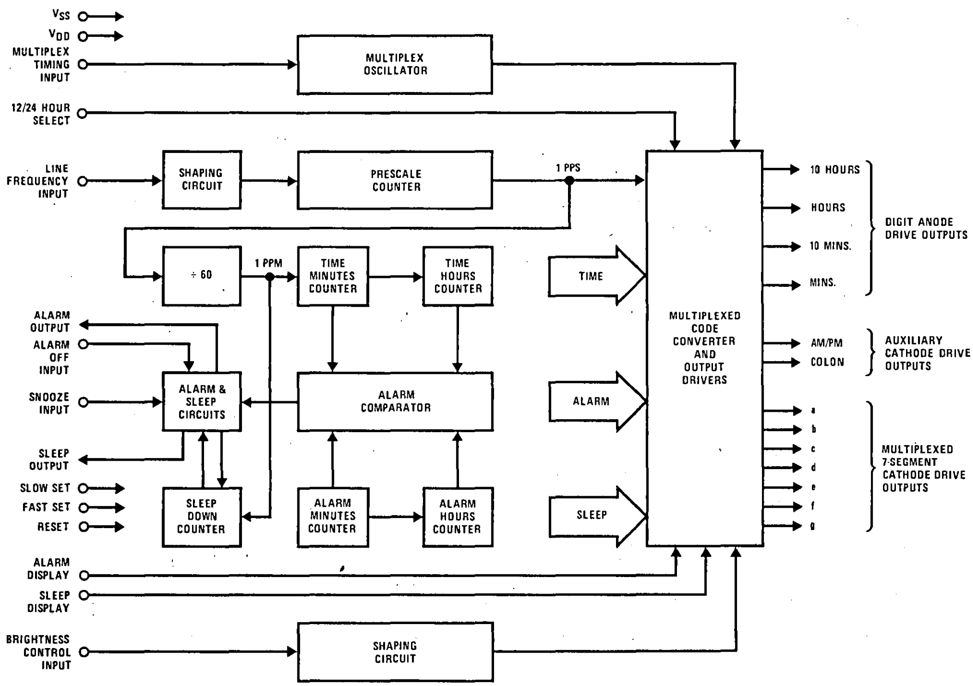


FIGURE 1. MM5370 and MM5371 Digital Alarm Clock, Block Diagram

functional description (Continued)

TABLE I. MM5370 and MM5371 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time	10's of Hours	Unit Hours	10's of Minutes	Unit Minutes
Alarm	10's of Hours	Unit Hours	10's of Minutes	Unit Minutes
Sleep	Blanked**	Blanked	10's of Minutes	Unit Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

**F segment is lit in 12-hour display mode. This may be eliminated by using circuit shown in *Figure 9.*

Table II. MM5370 and MM5371 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
Time*	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
	Reset	Time Resets to 12:00 AM (12-hour format)
	Reset	Time Resets to 00:00 (24-hour format)
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Sleep	Slow	Subtracts Count at 2 Hz Rate
	Fast	Subtracts Count at 60 Hz Rate
	Both	Subtracts Count at 60 Hz Rate

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

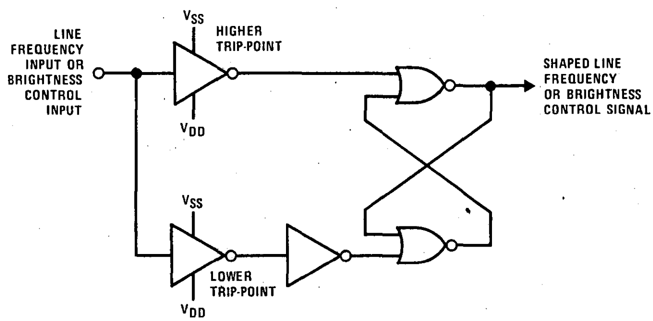


FIGURE 2. 60 Hz (or 50 Hz) Input (or Brightness Control Input) Shaping Circuit

functional description (Continued)

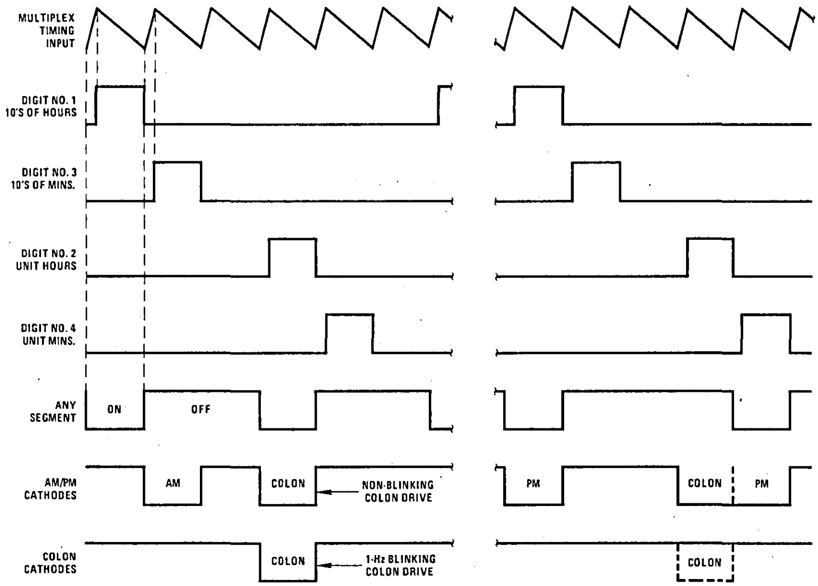


FIGURE 3. Output Timing Diagram

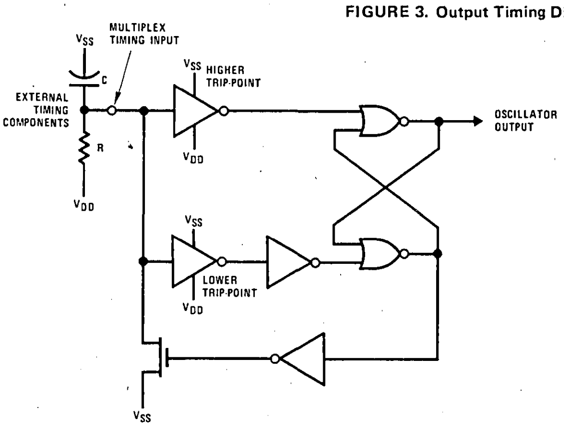


FIGURE 4. Multiplex Oscillator Circuit

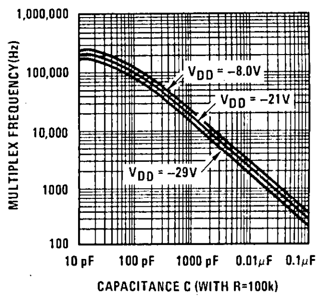
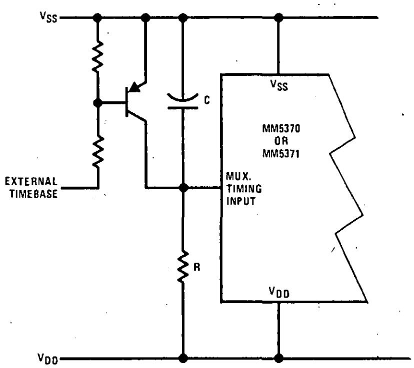


FIGURE 5. Multiplex Timing Component Selection Guide (Typical Only)



Note 1: For synchronizing, free running period should be set to run slightly longer than external timebase over temperature.

Note 2: For driving, timing capacitor should be deleted.

FIGURE 6. Synchronizing or Driving Multiplex Oscillator

functional description (Continued)

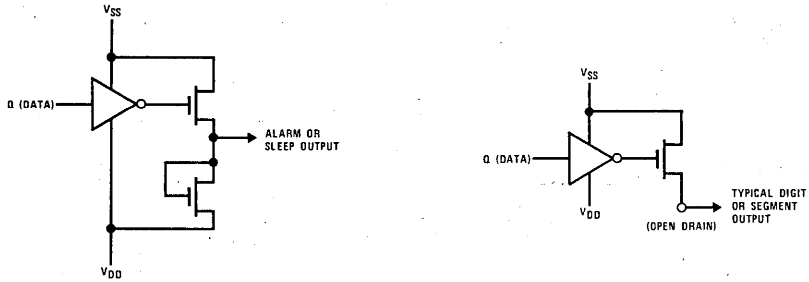


FIGURE 7. Output Circuits

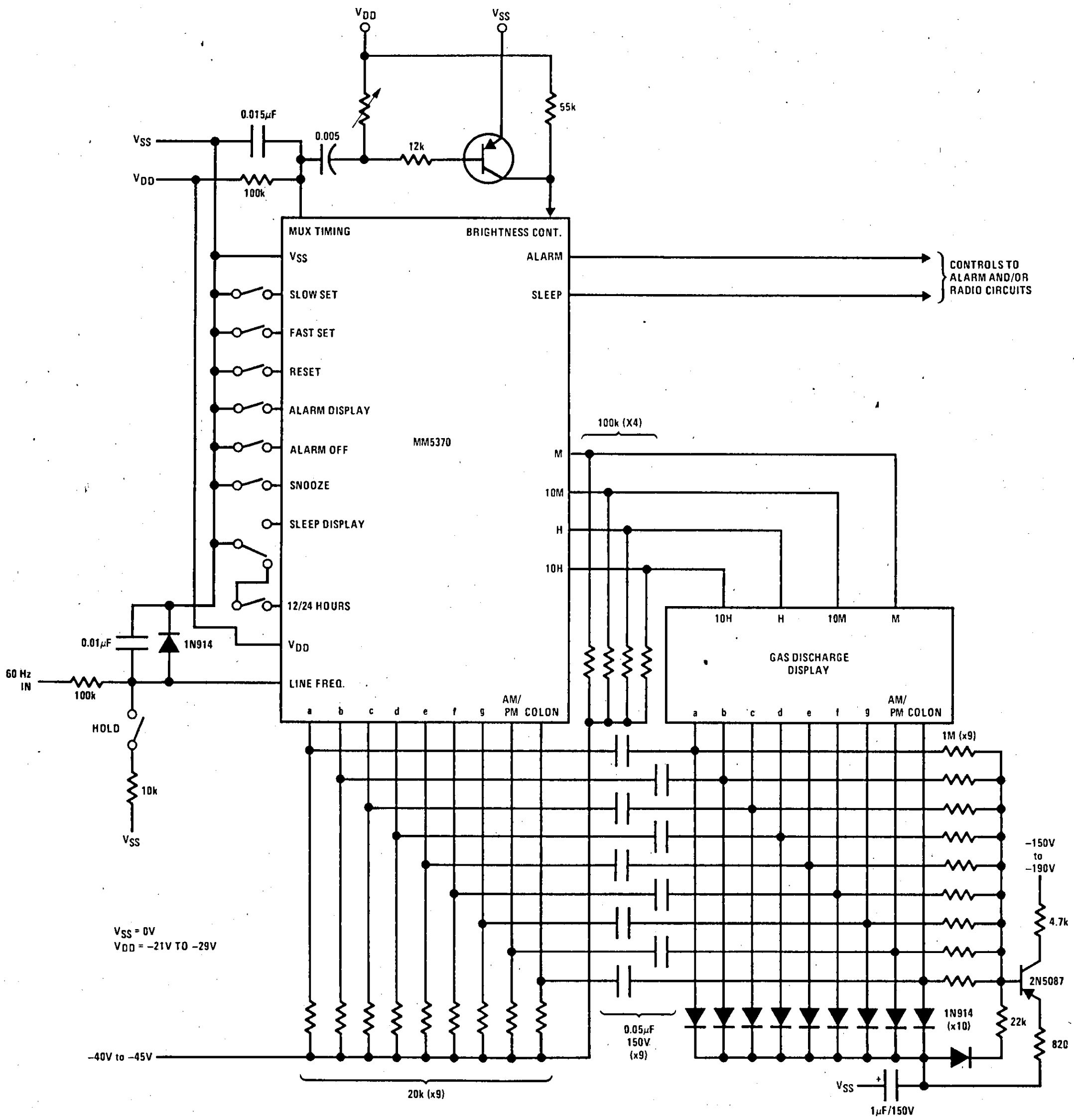


FIGURE 8. Recommended Application

MM5375XX series clocks

general description

MM5375XX series clock is a monolithic MOS integrated circuit utilizing P-channel low threshold enhancement-mode and ion-implanted depletion-mode devices. It provides all the logic required to give a 4 or 6-digit 12-hour or 24-hour display from a 50 or 60 Hz input. An auxiliary counter allows various options. Available options have been listed under features. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting time cancels this indication. MM5375XX is available in a 24-lead dual-in-line epoxy package.

features

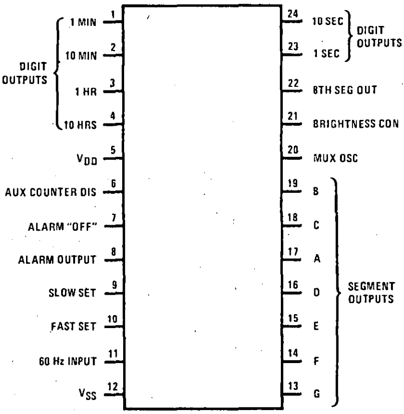
- Single power supply
- Low power dissipation
- All counters resettable
- Fast and slow set controls
- Power failure indication
- Brightness control capability
- No illegal time display at turn-on
- Simple interface to gas discharge displays and LED's
- Internal digit multiplex oscillator
- Leading zero blanking
- Activity indicator
- 4 to 6-digit operation
- Available options†

application

- Alarm clocks
- Desk clocks
- Automobile clocks
- Industrial clocks
- Date clocks
- Minute timer clocks
- Seconds timer clocks

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5375XXN
See Package 22

available options table†

FEATURE	FUNCTION	OPTION NAME								
		AA	AB	AC	AD	AE	AG	AH	AI	AJ
Input Frequency	60 Hz	•	•		•	•	•	•		
	50 Hz			•					•	•
Time Display	12-Hour	•	•		•		•	•		
	24-Hour			•		•			•	•
Auxiliary Counter	Alarm Counter	•	•				•		•	•
	Date Counter			•				•		
	Minute Timer				•					
	Second Timer					•				
Alarm Signal	Tone *	•	•	N/A	N/A	N/A	•	N/A	•	•
	DC Level			N/A	N/A	N/A		N/A		
Alarm Output	Modulated at 2 Hz	•	•	N/A	N/A	N/A	•	N/A	•	•
	Not Modulated			N/A	N/A	N/A		N/A		
Alarm at Power Failure	"ON"	•	•	N/A	N/A	N/A	•	N/A	•	•
	"OFF"			N/A	N/A	N/A		N/A		
Segment Output Polarity	V_{SS} for Display		•		•		•	•	•	•
	V_{DD} for Display	•		•		•				
AM or PM Indication	"OFF" During Time Display	•	•	N/A		N/A			N/A	N/A
	Displayed at All Times			N/A	•	N/A	•	•	N/A	N/A
8th Segment Blanked During Alarm Display	Yes			N/A	N/A	N/A		N/A		
	No	•	•	N/A	N/A	N/A	•	N/A	•	•

*Tone is 1/6 multiplex frequency

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 30V
Voltage at Any Display Output Pin	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −21V to −29V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{DD})	Excluding Outputs	−8.0		−29	V
	Outputs Driving Displays	−21		−29	V
Power Supply Current	Excluding Outputs			8.0	mA
60 Hz Input					
Frequency		DC	50/60	30k	Hz
Logical High		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logical Low		V_{DD}	V_{DD}	V_{DD}+1.0	V
Brightness Control Range % of Digit Time	Determined by External R and C, *(Figure 2)*	0		95	%
Multiplex Oscillator Frequency Input	Determined by External R and C, *(Figure 2)*	DC		30	kHz
All Other Input Voltages					
Logical High Level		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+2.0	V
Power Failure Detect Voltage	(V_{DD} Voltage)	−1.0		−8.0	V
Output Current	V_{DD} = −21V to −29V				
Digit Select Outputs	V_{SS} = 0V				
Logical High, Source	V_{OH} = V_{SS} − 5V	8.0			mA
Logical Low, Leakage	V_{OL} = V_{SS} − 45V			40	μA
Segment Outputs					
Logical High, Source	V_{OH} = V_{SS} − 5V	2.0			mA
Logical Low, Leakage	V_{OL} = V_{SS} − 45V			10	μA
Alarm Output					
Logical High, Source	V_{OH} = V_{SS} − 2V	1.5			mA
Logical Low, Sink	V_{OL} = V_{DD} + 2V	1			μA

functional description

A block diagram of the MM5375XX series of clocks is shown in *Figure 1*. The display modes are listed in Table I. The functions of the setting controls are listed in Table II. The following discussions are based on *Figure 1*.

60 Hz Input (Pin 11): A shaping circuit is provided to square the 60 Hz input (50 Hz optional). This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 3V of hysteresis. The shaper output drives a counter chain which performs the timekeeping function.

Time Setting Inputs (Pins 9 and 10): The time setting control functions are affected by the application of V_{SS} to these 2 pins, which are internally pulled to the power supply. Activating Fast Set (pin 10) causes the minutes counter to advance at a 60 Hz rate, thus clocking the hours counter at a rate of 1 hour per second. Slow Set (pin 9) advances the minutes counter at a rate of 2 minutes per second. Activating either Fast Set or Slow Set resets the seconds counter to zero. When Fast Set and Slow Set are activated simultaneously, all counters are reset to 12:00 p.m. and remain in that count until Slow Set is deactivated. The 2 time setting inputs affect only the counters that are displayed (either the timekeeping counters or the alarm counters).

8-Segment Test (Pin 24): For testing purposes, all 8-segment output lines may be activated by connecting pin 24 (S10 digit output) to V_{SS}.

functional description (Continued)

Brightness Control (Pin 21): In LED applications, brightness of the display may be varied by use of an external time constant. This time constant is used in the integrated circuit to control the pulse width or duty cycle of the 6-digit enable outputs, *(Figure 2)*. In gas discharge applications, connect as shown in *Figure 3*.

Activity Indication (Pin 23): When all 6 digits are being used, it is not necessary to blink the colon to indicate operation of the clock, because the seconds digits provide this information. When only 4 digits are in use, the S1 digit (pin 23) may be connected to V_{SS}. In this case, the colon flashes at a 1 Hz rate.

Multiplex Frequency (Pin 20): Applying an external time constant to this pin allows the multiplex frequency to be adjusted, *(Figure 2)*.

Power Failure Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, the AM or PM and colon indicator will flash at a 2 Hz rate. If power drops completely, the clock will reset itself (on resumption of power) to a legal state, and the AM or PM and colon indicators will flash at a 2 Hz rate. In addition to the flashing AM or PM and colon indicator, if a power failure occurs when alarm "OFF" (pin 7) is at V_{DD} (logical "0"), the alarm output will be activated (non-activated optional). A logical "1" (V_{SS}) on pin 7 will deactivate the alarm signal.

8-Segment Outputs (Pins 13–19 and 22): These outputs contain multiplexed information for the display of 7-segment numerical readouts. The 8th segment is for the activation of AM/PM and colon(s) as included in the gas discharge displays for which these outputs are designed.

4-Digit Operation: Connect pin 23 to V_{SS}.

Digit Enable Outputs (Pin 1–4, 23 and 24): These outputs are used to select the 6 digits and are synchronized with the segment outputs. If pin 23 is grounded, segment outputs will be blanked during the scanning of the seconds digits.

Auxiliary Counter: Alarm Counter Option: In this option, the auxiliary counter is programmed and used as an alarm counter. Pin 6 serves as both alarm display and snooze input pin. Alarm counter is displayed when pin 6 is held at V_{SS}. Alarm setting (Table II) is done using alarm display, Fast Set (pin 10) and Slow Set (pin 9). If the alarm "OFF" input (pin 7) is open and whenever the real time matches with the alarm time, the alarm comparator sets the alarm latch. This latch activates the alarm output (pin 8). The alarm will remain activated until the alarm "OFF" input is connected to V_{SS} temporarily. This readies the alarm latch for next comparison. To deactivate the alarm output for more than 24 hours, the alarm "OFF" input is held at V_{SS} for that long. When the alarm output is active, connecting pin 6 to V_{SS} will interrupt the alarm signal for 6 to 8 minutes (snooze function).

Auxiliary Counter: Date Counter Option: In this option, the auxiliary counter is programmed and used as a month and day counter. The day counter counts up to 31 days and increments the month counter. The day counter rolls over from 31 to 1. The month counter counts up to 12 and rolls over to 1. The date counter can be displayed by connecting date display (pin 6) to V_{SS}. The effects of Fast and Slow Set controls are shown in Table II. In this option, do not use the alarm output (pin 8).

Auxiliary Counter: Timer Option: In this option, the auxiliary counter is programmed and used as a timer counter. When the display pin 6 is connected to V_{SS}, the elapsed time from the previous setting is displayed. The following sequence describes the use of the product as a minute (or seconds) timer.

1. Hold display pin 6 at V_{SS}.
2. Hold both Fast and Slow Set controls at V_{SS}.
   Note: This will reset the timer counter to 12:00 in 12-hour mode and 00:00 in 24-hour mode.
3. Release both the Fast and Slow Set controls simultaneously.
   Note: The timer counter starts counting minutes (or seconds).
4. If it is required to monitor elapsed time continuously, retain the display pin 6 at V_{SS}. Otherwise, release pin 6.
5. Elapsed time can be displayed any time by holding pin 6 at V_{SS}.

In this option, the clock can be used for up to 12 hours (12 minutes in seconds timer) of elapsed time in 12-hour mode and 24 hours (24 minutes in seconds timer) of elapsed time in 24-hour mode. The effect of Fast and Slow Set controls are listed in Table II. In these options, do not use the alarm output (pin 8).

Accuracy of Elapsed Time: Elapsed time = displayed time ± 1 minute (or second).

TABLE I. Display Modes

SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4	DIGIT NO. 5	DIGIT NO. 6
Time Display	10's of Hours	Units Hours	10's of Minutes	Units Minutes	10's of Seconds	Units Seconds
Alarm Display	10's of Hours	Units Hours	10's of Minutes	Units Minutes	ϕ	ϕ
Date Display	Month	Month	Date	Date	ϕ	ϕ
Minute Timer Display	10's of Hours	Units Hours	10's of Minutes	Units Minutes	ϕ	ϕ
Second Timer Display	10's of Minutes	Units Minutes	10's of Seconds	Units Seconds	ϕ	ϕ

functional description (Continued)

TABLE II. Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
Time Display	Slow	Minutes advance at 2.0 Hz rate and seconds are held at a reset (00) condition
	Fast	Minutes advance at 60 Hz rate and seconds are held at a reset (00) condition
	Both	Time resets to 12:00:00 p.m. (12-hour mode) or 00:00:00 (24-hour mode)
Alarm Display	Slow	Alarm minutes advance at a 2.0 Hz rate
	Fast	Alarm minutes advance at a 60 Hz rate
	Both	Alarm resets to 12:00 p.m. (12-hour mode) or 00:00 (24-hour mode)
Date Display	Slow	Date advances at a 2.0 Hz rate
	Fast	Date advances at a 60 Hz rate
	Both	Date counter resets to 12:00
Minute Timer Display	Slow	Minutes (auxiliary counter) advance at a 2.0 Hz rate
	Fast	Minutes (auxiliary counter) advance at a 60 Hz rate
	Both	Timer counter resets to 12:00 (12-Hour mode) or 00:00 (24-hour mode)
Second Timer Display	Slow	Seconds (auxiliary counter) advance at a 2.0 Hz rate
	Fast	Seconds (auxiliary counter) advance at a 60 Hz rate
	Both	Timer counter resets to 12:00 (12-hour mode) or 00:00 (24-hour mode)

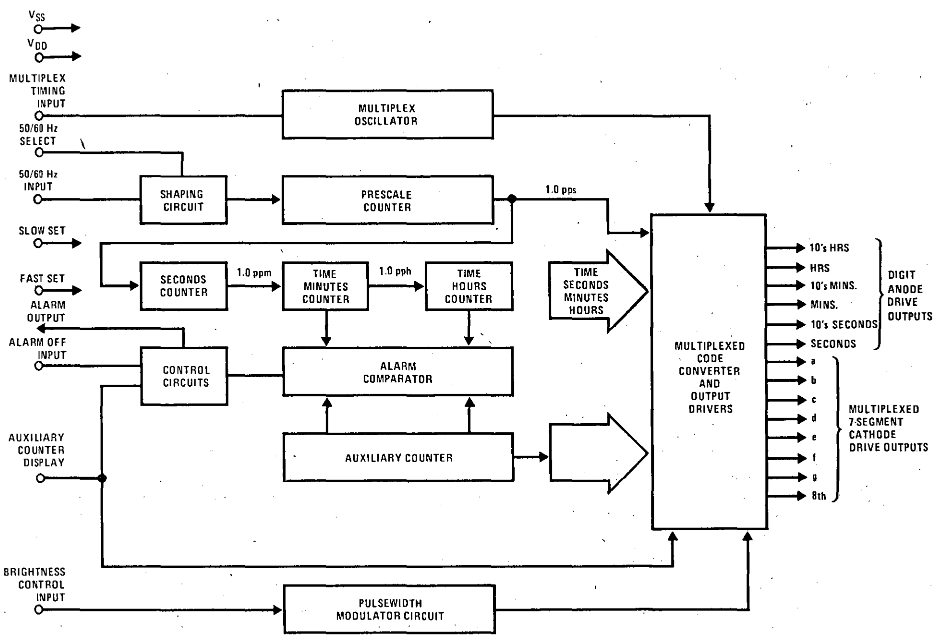


FIGURE 1. Block Diagram

functional description (Continued)

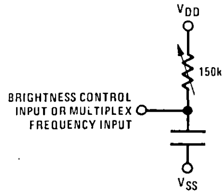
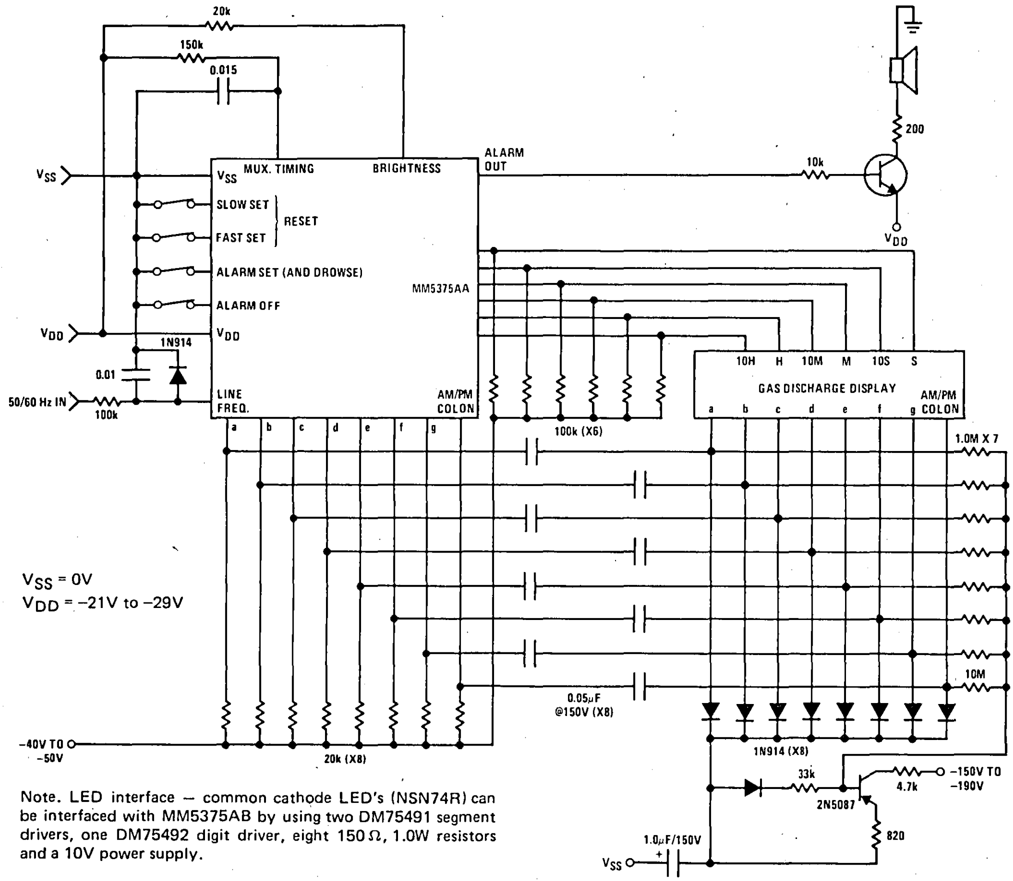


FIGURE 2



Note. LED interface – common cathode LED's (NSN74R) can be interfaced with MM5375AB by using two DM75491 segment drivers, one DM75492 digit driver, eight 150 Ω, 1.0W resistors and a 10V power supply.

FIGURE 3. Typical Application

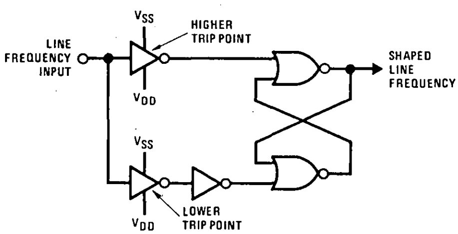


FIGURE 4. 50 or 60 Hz Shaping Circuit

functional description (Continued)

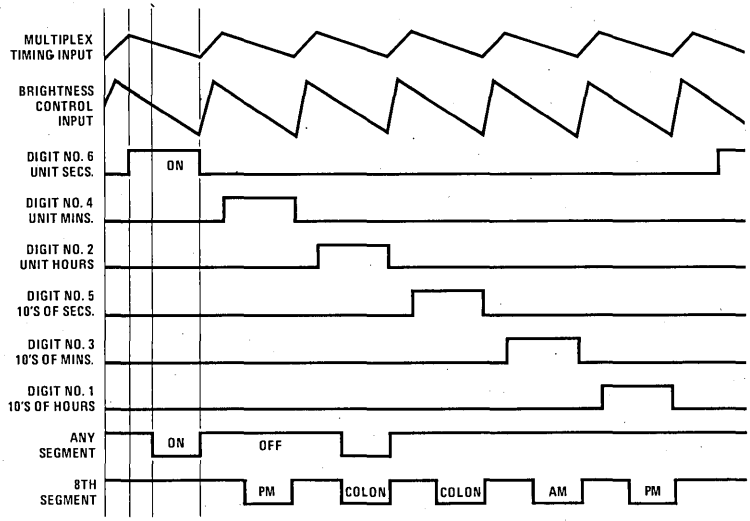


FIGURE 5. Output Timing Diagram

MM5376XX series clocks

general description

MM5376XX series clock is a monolithic MOS integrated circuit utilizing P-channel, low threshold, enhancement-mode and ion-implanted depletion-mode devices. It provides all the logic required to give a 4 or 6-digit 12-hour or 24-hour display from a 50 or 60 Hz input. An auxiliary counter allows various options. Available options have been listed under features. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting time cancels this indication. MM5376XX is available in a 24-lead dual-in-line epoxy package.

features

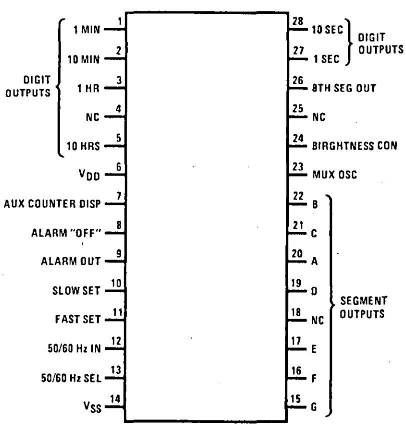
- 50 or 60 Hz operation
- Single power supply
- Low power dissipation
- All counters resettable
- Fast and slow set controls
- Power failure indication
- Brightness control capability
- No illegal time display at turn-on
- Simple interface to gas discharge displays and LED's
- Internal digit multiplex oscillator
- Leading zero blanking
- Activity indicator
- 4 to 6-digit operation
- Available options†

application

- Alarm clocks
- Desk clocks
- Automobile clocks
- Industrial clocks
- Two time zone clocks
- Date clocks
- Minute timer clocks
- Seconds timer clocks

connection diagram

Dual-In-Line Package



TOP VIEW

Note 1: 50 Hz input at pin 12 connect pin 13 to V_{DD}.
Note 2: 60 Hz input at pin 12 connect pin 13 to V_{SS}.

Order Number MM5376XXN
See Package 23

available options table†

FEATURE	FUNCTION	OPTION NAME					
		AA	AB	AD	AE	AG	AH
Input Frequency	60 Hz	•	•	•	•	•	•
	50 Hz	•	•	•	•	•	•
Time Display	12-Hour	•	•	•		•	•
	24-Hour				•		
Auxiliary Counter	Alarm Counter	•	•			•	
	Date Counter						•
	Minute Timer			•			
	Second Timer				•		
Alarm Signal	Tone*	•	•	N/A	N/A	•	N/A
	DC Level			N/A	N/A		N/A
Alarm Output	Modulated at 2 Hz	•	•	N/A	N/A	•	N/A
	Not Modulated			N/A	N/A		N/A
Alarm at Power Failure	"ON"	•	•	N/A	N/A	•	N/A
	"OFF"			N/A	N/A		N/A
Segment Output Polarity	V_{SS} for Display		•	•		•	•
	V_{DD} for Display	•			•		
AM or PM Indication	"OFF" During Time Display	•	•		N/A		
	Displayed at All Times			•	N/A	•	•
8th Segment Blanked During Alarm Display	Yes			N/A	N/A		N/A
	No	•	•	N/A	N/A	•	N/A

*Tone is '16 multiplex frequency

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 30V
Voltage at Any Display Output Pin	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −8V to −29V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	Excluding Outputs			8.0	mA
50/60 Hz Input Frequency		DC	60/50	10k	Hz
Logic High		V_{SS}−1.0		V_{SS}	V
Logic Low			V_{DD}	V_{SS}−15.0	V
Brightness Control Range % of Digit Time	Determined by External R and C *(Figure 2)*	0		95	%
Multiplex Oscillator Frequency Input	Determined by External R and C *(Figure 2)*	DC		10	kHz
All Other Input Voltages					
Logic High Level		V_{SS}−1.0	V_{SS}	V_{SS}	V
Logic Low Level			V_{DD}	V_{SS}−15.0	V
Power Failure Detect Voltage	(V_{DD} Voltage)	−1.0		−8.0	V
Output Current Levels	V_{DD} = −21V to −29V				
Digit Select Outputs	V_{SS} = 0V				
Logic High, Source	V_{OH} = V_{SS} − 5.0V	8.0			mA
Logic Low, Leakage	V_{OL} = V_{SS} − 45V			40	μA
Segment Outputs					
Logic High, Source	V_{OH} = V_{SS} − 5.0V	2.0			mA
Logic Low, Leakage	V_{OL} = V_{SS} − 45V			10	μA
Alarm Output					
Logic High, Source	V_{OH} = V_{SS} − 2.0V	1.5			mA
Logic Low, Sink	V_{OL} = V_{DD} + 2.0V	1.0			μA

functional description

A block diagram of the MM5376XX series of alarm clocks is shown in *Figure 1*. The two display modes are listed in Table I. The functions of the setting controls are listed in Table II. The following discussions are based on *Figure 1*.

50 or 60 Hz Input (Pin 12): A shaping circuit is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 3.0V of hysteresis. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select (Pin 13): 50 or 60 Hz input at pin 12 is selected by pin 13. 50 Hz operation is selected by connecting pin 13 to V_{DD} (pin 6) and 60 Hz operation is selected by connecting pin 13 to V_{SS} (pin 14).

functional description (Continued)

Time Setting Inputs (Pins 10 and 11): The time setting control functions are affected by the application of V_{SS} to these two pins, which are internally pulled to the power supply. Activating Fast Set (pin 11) causes the minutes counter to advance at 50 or 60 Hz rate, thus clocking the hours counter at a rate of one hour per second. Slow Set (pin 10) advances the minutes counter at a rate of 2 minutes per second. Activating either Fast Set or Slow Set resets the seconds counter to zero. When Fast Set and Slow Set are activated simultaneously, all counters are reset to 12:00 p.m. and remain in that count until Slow Set is deactivated. The two time setting inputs affect only the counters that are displayed (either the timekeeping counters or the alarm counters).

8-Segment Test (Pin 28): For testing purposes, all 8-segment output lines may be activated by connecting pin 24 (S10 digit output) to V_{SS}.

Brightness Control (Pin 24): In LED applications, brightness of the display may be varied by use of an external time constant. This time constant is used in the integrated circuit to control the pulse width or duty cycle of the 6-digit enable outputs *(Figure 2)*. In gas discharge applications, connect as shown in *Figure 3*.

Activity Indication (Pin 27): When all 6 digits are being used, it is not necessary to blink the colon to indicate operation of the clock, because the seconds digits provide this information. When only 4 digits are in use, the S1 digit (pin 27) may be connected to V_{SS}. In this case, the colon flashes at a 1.0 Hz rate.

Multiplex Frequency (Pin 23): Applying an external time constant to this pin allows the multiplex frequency to be adjusted. See *Figure 2*.

Power Failure Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, the AM or PM and colon indicator will flash at a 2.0 Hz rate. If power drops completely, the clock will reset itself (on resumption of power) to a legal state, and the AM or PM and colon indicators will flash at a 2.0 Hz rate. In addition to the flashing AM or PM and colon indicator, if a power failure occurs when alarm "OFF" (pin 8) is at V_{DD} (logic "0"), the alarm output will be activated (non-activated optional). A logic "1" (V_{SS}) on pin 8 will deactivate the alarm signal.

8-Segment Outputs (Pins 15–17, 19–22 and 26): These outputs contain multiplexed information for the display of 7-segment numerical readouts. The eighth segment is for the activation of AM/PM and colon(s) as included in the gas discharge displays for which these outputs are designed.

4-Digit Operation: Connect pin 23 to V_{SS}.

Digit Enable Outputs (Pins 1–3, 5, 27 and 28): These outputs are used to select the 6 digits and are synchronized with the segment outputs. If pin 27 is grounded, segment outputs will be blanked during the scanning of the seconds digits.

Auxiliary Counter, Alarm Counter Option: In this option, the auxiliary counter is programmed and used as an alarm counter. Pin 7 serves as both alarm display and snooze input pin. Alarm counter is displayed when pin 7 is held at V_{SS}. Alarm setting (Table II) is done using Alarm Display, Fast Set (pin 11) and Slow Set (pin 10). If the alarm "OFF" input (pin 8) is open and whenever the real time matches with the alarm time, the alarm comparator sets the alarm latch. This latch activates the alarm output (pin 9). The alarm will remain activated until the alarm "OFF" input is connected to V_{SS} temporarily. This readies the alarm latch for next comparison. To deactivate the alarm output for more than 24 hours, the alarm "OFF" input is held at V_{SS} for that long. When the alarm output is active, connecting pin 7 to V_{SS} will interrupt the alarm signal for 6 to 8 minutes (snooze function).

TABLE I. Display Modes

SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4	DIGIT NO. 5	DIGIT NO. 6
Time Display	10's of Hours	Units Hours	10's of Minutes	Units Minutes	10's of Seconds	Units Seconds
Alarm Display	10's of Hours	Units Hours	10's of Minutes	Units Minutes	ϕ	ϕ
Date Display	Month	Month	Date	Date	ϕ	ϕ
Minute Timer Display	10's of Hours	Units Hours	10's of Minutes	Units Minutes	ϕ	ϕ
Second Timer Display	10's of Minutes	Units Minutes	10's of Seconds	Units Seconds	ϕ	ϕ

functional description (Continued)

TABLE II. Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
Time Display	Slow	Minutes advance at 2.0 Hz rate and seconds are held at a reset (00) condition
	Fast	Minutes advance at 60 Hz rate and seconds are held at a reset (00) condition
	Both	Time resets to 12:00:00 p.m. (12-hour mode) or 00:00:00 (24-hour mode)
Alarm Display	Slow	Alarm minutes advance at a 2.0 Hz rate
	Fast	Alarm minutes advance at a 60 Hz rate
	Both	Alarm resets to 12:00 p.m. (12-hour mode) or 00:00 (24-hour mode)
Date Display	Slow	Date advances at a 2.0 Hz rate
	Fast	Date advances at a 60 Hz rate
	Both	Date counter resets to 12:00
Minute Timer Display	Slow	Minutes (auxiliary counter) advance at a 2.0 Hz rate
	Fast	Minutes (auxiliary counter) advance at a 60 Hz rate
	Both	Timer counter resets to 12:00 (12-Hour mode) or 00:00 (24-hour mode)
Second Timer Display	Slow	Seconds (auxiliary counter) advance at a 2.0 Hz rate
	Fast	Seconds (auxiliary counter) advance at a 60 Hz rate
	Both	Timer counter resets to 12:00 (12-hour mode) or 00:00 (24-hour mode)

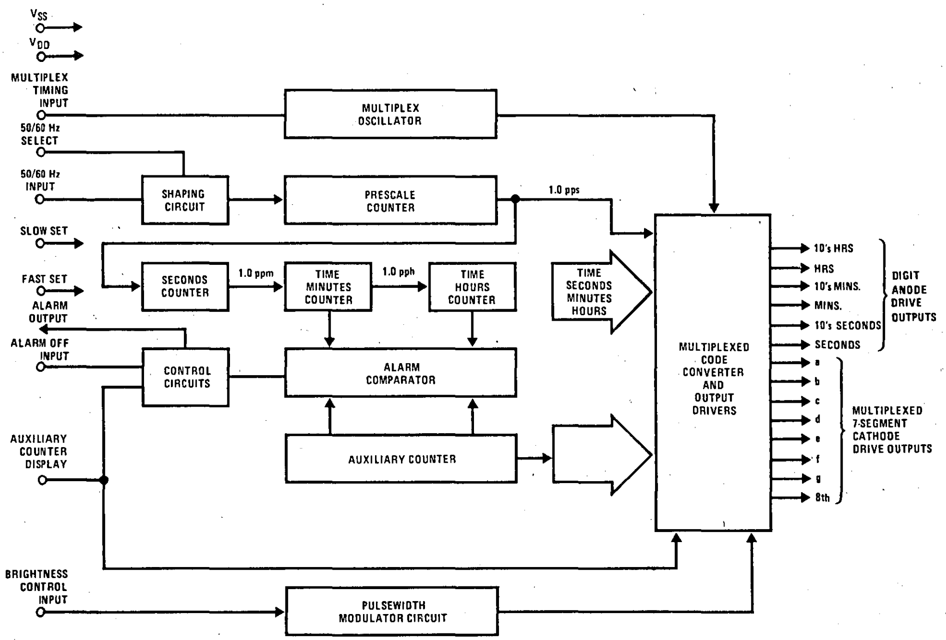


FIGURE 1. Block Diagram

functional description (Continued)

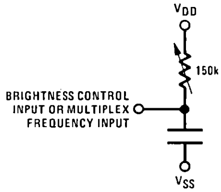
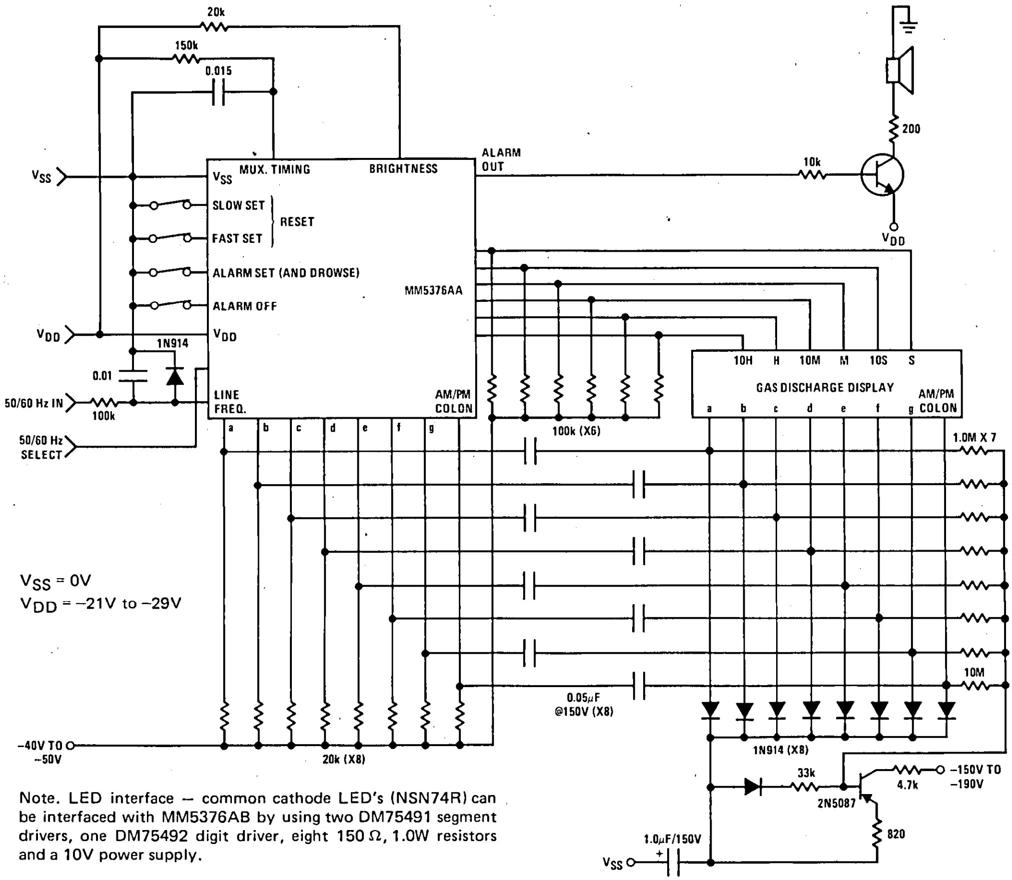


FIGURE 2



$V_{SS} = 0V$

$V_{DD} = -21V$ to $-29V$

Note. LED interface – common cathode LED's (NSN74R) can be interfaced with MM5376AB by using two DM75491 segment drivers, one DM75492 digit driver, eight 150 Ω, 1.0W resistors and a 10V power supply.

FIGURE 3. Typical Application

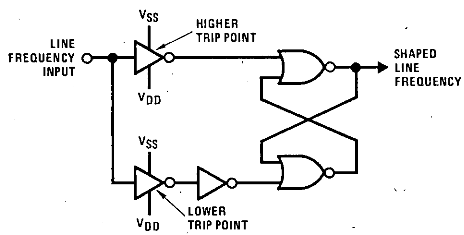


FIGURE 4. 50 or 60 Hz Shaping Circuit

functional description (Continued)

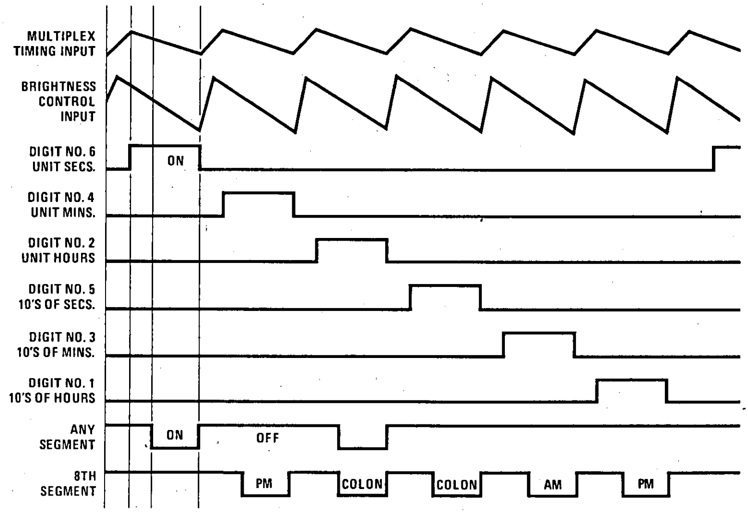


FIGURE 5. Output Timing Diagram

MM5377 auto clock

general description

The MM5377 Auto Clock is a monolithic MOS integrated circuit utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. The circuit interfaces directly with liquid crystal 4 digit displays and fluorescent tubes. The display format is 12 hours with leading-zero blanking and colon indication. A voltage sensitive output is provided that drives an energy storage network which performs as a voltage doubler/regulator. The circuit uses a 2 MHz crystal oscillator as the reference time base and is packaged in a 40 lead dual-in-line package.

features

- Crystal controlled oscillator (2.097152 MHz)
- 12 hour display format
- Colon output
- Leading zero blanking
- Hours and minutes set controls
- Crystal tuner output
- Voltage doubler control output
- Elimination of illegal time display at turn-on
- Direct interface to liquid crystal display
- Direct interface to fluorescent tubes
- Low standby power dissipation

applications

- Automobile clocks
- Desk clocks
- Portable clocks
- High accuracy clocks

block and connection diagrams

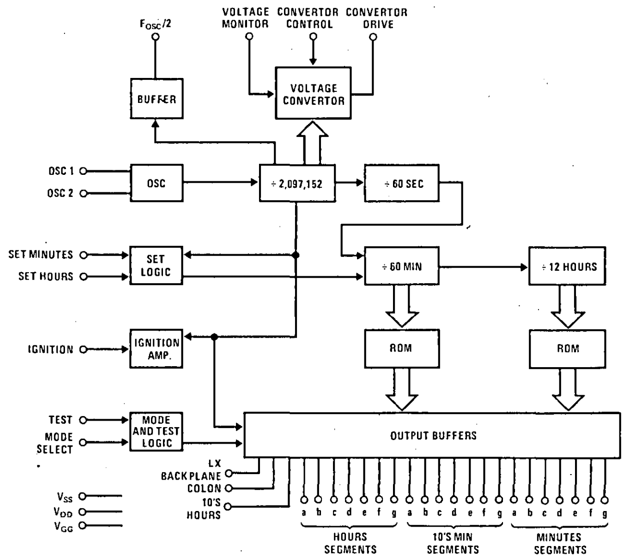
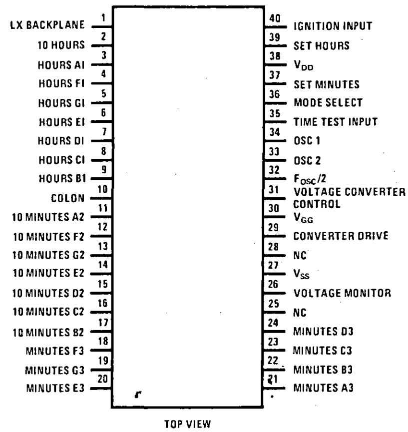


FIGURE 1.

Dual-In-Line Package



Order Number 5377N
See Package 24

FIGURE 2.

absolute maximum ratings

Voltage at V_{GG} Pin	V_{SS} + 0.3V to V_{SS} − 30V
Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 24V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = +9V to +20V, V_{DD} = 0V, V_{GG} = −10V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})	Outputs and OSC Operational	8	18	20	V
Power Supply Voltage (V_{GG})	Outputs and OSC Operational	−6	−8	−10	V
Power Supply Voltage (V_{SS})	No Loss of Time Memory	5	18	20	V
Power Supply Voltage (V_{SS})	Ignition Open	7	9	20	V
Power Supply Voltage (V_{GG})	Ignition Open		0		V
Power Supply Current (I_{SS})	Ignition Open	1	3	5	mA
Input Frequency	OSC 1	DC	2.097152	2.1	MHz
Frequency of Outputs	Liquid Crystal Display f_{IN} = 2.097152 MHz		32		Hz
OUTPUT CURRENTS					
Display Segments	V_{SS} = +18V				
Source Current	V_{OUT} = V_{SS} − 1V	200			μA
Sink Current	V_{OUT} = V_{SS} − 17V	200			μA
Display Colon and 10's Hours	V_{SS} = +18V				
Source Current	V_{OUT} = V_{SS} − 1V	400			μA
Sink Current	V_{OUT} = V_{SS} − 17V	400			μA
Display Backplane	V_{SS} = +18V				
Source Current	V_{OUT} = V_{SS} − 1.2V	4			mA
Sink Current	V_{OUT} = V_{SS} − 16.8V	4			mA
Convertor Drive Output	V_{SS} = +10V				
Source Current	V_{OUT} = V_{SS} − 6V	500			μA
Sink Current	V_{OUT} = V_{SS} − 8V	100			μA
FOSC/2 Source Current	V_{SS} = +18V V_{OUT} = V_{SS} − 2V	200			μA
Voltage Monitor	Zener = 16V				
Source Current			100		μA
Trip Point		17	18	19	V

functional description

A block diagram of the MM5377 auto clock is shown in *Figure 1.* A connection diagram is shown in *Figure 2.* Unless otherwise indicated, the following discussions are based on *Figure 1.*

Oscillator 1 (Pin 34) and Oscillator 2 (Pin 33)

A quartz crystal, resonant at 2.019752 MHz, two capacitors and one resistor, together with the internal MOS circuits form a crystal controlled oscillator as shown in *Figure 3.* Varying one of the capacitors allows precise frequency setting. For test purposes, OSC 1 is the input and OSC 2 is the output of an inverting amplifier.

FOSC/2 (Pin 32)

FOSC/2 is the output of the first divide-by-two stage. This output allows frequency tuning of the crystal oscillator without adding any additional capacitance to the oscillator circuit.

Set Hours (Pin 39) and Set Minutes (Pin 37)

Set Hours will advance the hours at a 1 Hz rate when the input is held at V_{DD}. While setting hours, the minute's counter may also advance the hours count. Set Minutes will advance the minutes at a 1 Hz rate, hold the internal seconds counter reset and cause the colon to blink at 1 Hz rate when the input is held at V_{DD}. Depressing both switches at the same time shall cause the clock to initiate a hold and not advance until the switches are released.

Mode Select (Pin 36)

Mode Select determines the shape of the output wave form as shown in *Figure 4.* With the input open or at V_{DD}, the output wave form is a 32 Hz square wave. Segments to be energized have the 32 Hz square wave 180° out of phase with respect to the backplane 32 Hz square wave. Segments not to be energized have their outputs in phase with the backplane output. With the mode select input at V_{SS}, the outputs are at a constant level. Segments to be energized are at V_{SS}, and segments not to be energized are at V_{DD}.

Time Test Input (Pin 35)

Time Test Input causes the circuit to cycle through a 12 hour period using an internal clock of 65536 Hz instead of 1 Hz to increment the seconds counter when the input is at V_{SS}. The input also causes the mode of the outputs to change from 32 Hz square wave to constant levels.

Ignition Input (Pin 40)

The Ignition Input enables setting of the clock using the set hour or set minute inputs, and enables the drive to the display and the voltage doubler. When the input is at a voltage greater than 50 percent of the V_{SS} supply the time set, display and voltage doubler are enabled. When the input is open circuited or at V_{DD}, the time set, display and voltage doubler are disabled. The display outputs and backplane drive are held to V_{DD} when the display is disabled. This input does not affect the accuracy of the time keeping logic in any manner.

Voltage Converter Control (Pin 31)

The Voltage Converter Control input enables the voltage doubler to operate regardless of the state of the ignition input when it is at V_{DD}. When the input is open circuited or at V_{SS}, the voltage doubler is controlled by the ignition input.

Output Circuits

The Converter Drive output and all display outputs are push-pull stages with sources common to V_{SS} (Pin 27) and drains common to V_{DD} (Pin 38) as shown in *Figure 5.* FOSC/2 output is a open-drain stage with the source common to V_{SS} as shown in *Figure 6. Figure 8* illustrates the interfacing between the clock and a liquid crystal display and the clock and fluorescent tubes. When driving fluorescent tubes, V_{GG} can be connected to V_{DD}.

Converter Drive (Pin 29) and Voltage Monitor (Pin 26)

The Converter Drive output oscillates at 65.636 kHz. The duty cycle of the wave depends on the state of the Voltage Monitor input pin as shown in *Figure 7.* With V_{SS} on the input pin, the duty cycle of the output wave is 50%, which enables the voltage doubler. Once the input pin is a few volts above the zener breakdown voltage of its' zener diode *(Figure 8)*, the duty cycle of the output is 0% or held at V_{DD}, which disables the voltage doubler. Therefore, the duty cycle of the output wave form varies from 50% to 0% as the voltage at the voltage monitor input pin varies. Therefore, the voltage to the chip is regulated about 2V above the zener breakdown voltage.

Colon Output (Pin 10)

The colon output indicates the clock is counting by blinking at a 1/2 Hz rate. When setting minutes, the colon blinks at 1 Hz rate.

typical applications

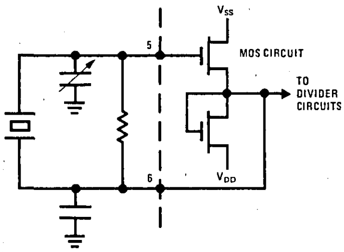


FIGURE 3. Crystal Oscillator

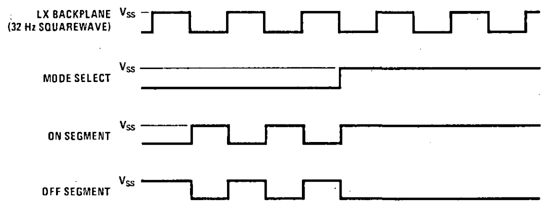


FIGURE 4. Output Timing Diagram

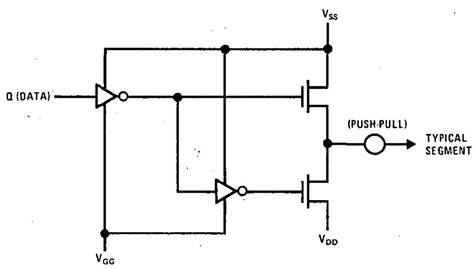


FIGURE 5. Push-Pull Output Circuit

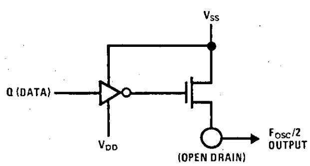


FIGURE 6. Open Drain Output Circuit

typical applications (con't)

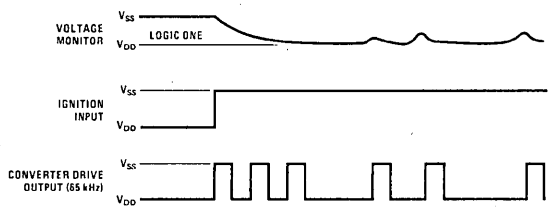


FIGURE 7. Operation of Converter Drive

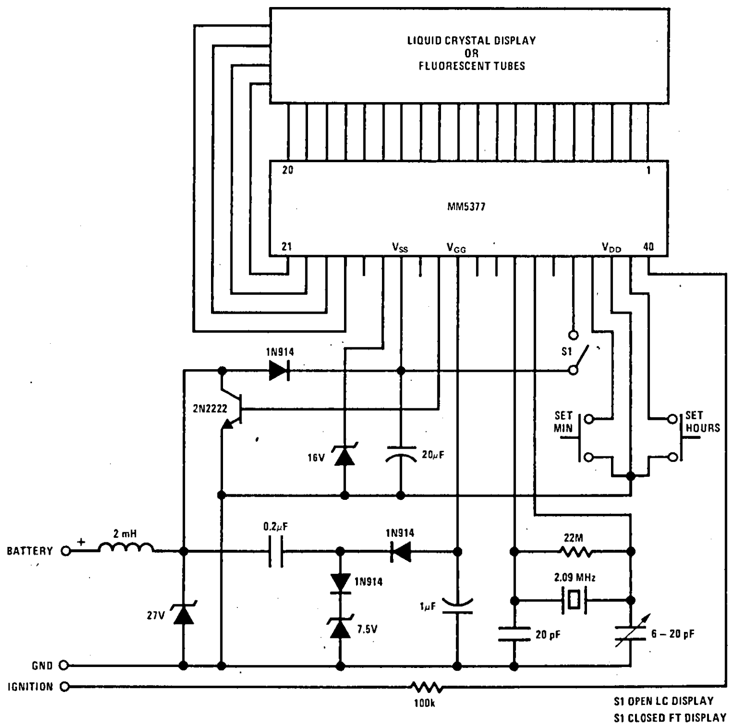


FIGURE 8. Typical Application

MM5378, MM5379 auto clocks

general description

The MM5378 and the MM5379 auto clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. The MM5378 circuit interfaces with vacuum fluorescent 4-digit displays. The MM5379 circuit interfaces with gas-discharge 4-digit displays. The display format is 12 hours with leading-zero blanking and colon indication. The time keeping function operates from a 2 MHz crystal controlled or externally applied source.

features

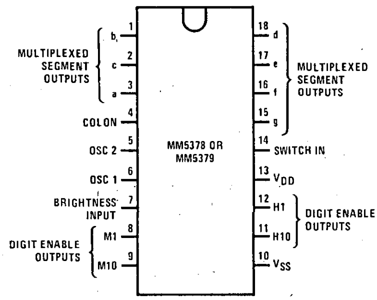
- Crystal-controlled oscillator (2.097152 MHz)
- 12-hour display format
- Blinking colon output
- Leading-zero blanking
- Hours and minutes set controls
- Brightness control capability
- No illegal time display at turn-on
- Simple interface to vacuum fluorescent and gas discharge displays
- Low standby power dissipation

applications

- Automobile clocks
- Desk clocks
- Portable clocks
- High accuracy clocks

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5378N or MM5379N
See Package 20

block diagram

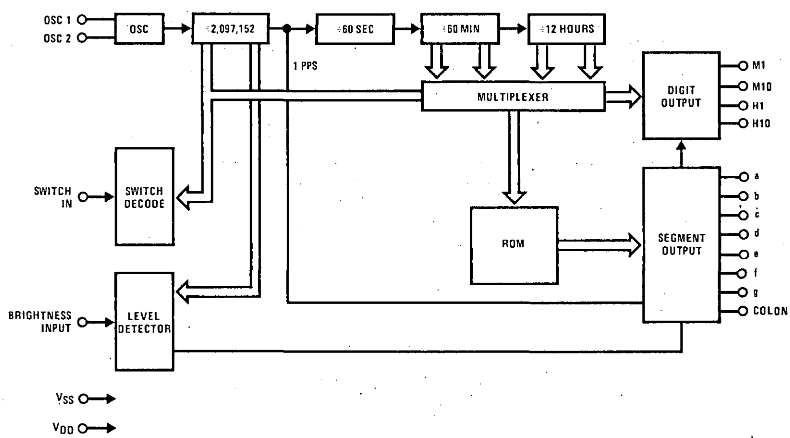


FIGURE 1.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 25V
Voltage at Any Display Output or Switch Input Pin (MM5379 Only)	V_{SS} + 0.3V to V_{SS} − 55V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics T_A within operating range, V_{SS} = 9V to 20V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})	Outputs and Osc. Operational	9		20	V
Power Supply Voltage (V_{SS})	No Loss of Time Memory	5		25	V
Power Supply Current (I_{SS})	No Output Loads	1		5	mA
Input Frequency (Osc. 1 or Osc. 2)		dc	2.097152	2.1	MHz
Oscillator Input Voltage	(Note 1)				
Logical High Level		V_{SS}−1.5		V_{SS}	V
Logical Low Level				V_{SS}−5.5	V
Switch In Voltage (MM5378)					
Logical High Level	Internal Depletion Device to	V_{SS}−1.5	V_{SS}	V_{SS}	V
Logical Low Level	V_{SS}		V_{DD}	V_{SS}−5	V
Switch In Voltage (MM5379)					
Logical High Level	Internal Depletion Device to	V_{SS}−5	V_{SS}		V
Logical Low Level	V_{SS}			V_{SS}−25	V
Output Currents (MM5378)					
Digit Outputs					
Logical High Level	$V_{OH} = V_{SS} - 1V$	8.0			mA
Logical Low Level	$V_{OL} = V_{DD}$			40	μA
Segment Outputs					
Logical High Level	$V_{OH} = V_{SS} - 1V$	2.0			mA
Logical Low Level	$V_{OL} = V_{DD}$			10	μA
Output Currents (MM5379)					
Digit Anode Outputs					
Logical High Level	$V_{OH} = V_{SS} - 5V$	8.0			mA
Logical Low Level	$V_{OL} = V_{SS} - 45V$			40	μA
Segment Cathode Outputs					
Logical High Level	$V_{OH} = V_{SS} - 5V$	2.0			mA
Logical Low Level	$V_{OL} = V_{SS} - 45V$			10	μA

Note 1: These are the input levels required if an external oscillator input is preferred, using Osc. 2 (pin 5) as the input while holding Osc. 1 (pin 6) to V_{SS}.

functional description

A block diagram of the MM5378 and the MM5379 auto clocks is shown in *Figure 1*. Connection diagrams for these devices are shown on the front page. Unless otherwise indicated, the following discussions are based on *Figure 1*.

Crystal Oscillator: A quartz crystal, resonant at 2.097152 MHz, two capacitors and one resistor, together with the internal MOS circuits form a crystal-controlled oscillator as shown in *Figure 2*. Varying one of the capacitors allows precise frequency setting. For test purposes, Osc. 1 is the input and Osc. 2 is the output of an inverting amplifier.

Time Setting: Time setting is accomplished via the switch input pin. If this input is a logic high during the M1 digit time, the minutes counter will advance at a 2 Hz rate with no carry to hours counter and will also cause seconds counter to reset. If the switch input is a logic high during the M10 digit time, the hours counter will advance at a 2 Hz rate, minutes and seconds counter will continue in real time. If the switch input is a logic high during H1 digit time, seconds, minutes, and hours counters will reset to 12:00:00. If this input is a logic high during H10 digit time, a test mode will exist in which the minutes counter will advance at a 65.536 kHz rate with carry to hours counter (see *Figure 3*). An

functional description (Continued)

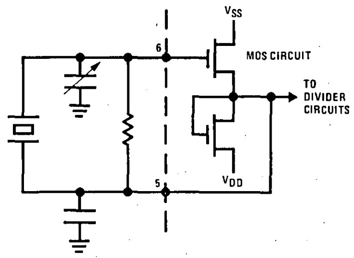


FIGURE 2. Crystal Oscillator

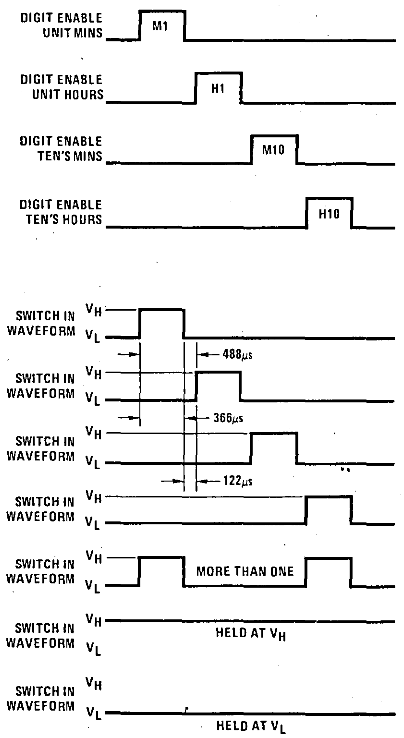
internal pull-up resistor to V_{SS} provides normal time-keeping.

Output Multiplex Operation: Outputs from the appropriate internal counter are time division multiplexed at a 2048 Hz rate. The MM5378 and MM5379 provide 12 outputs (4 digit-anode drive outputs plus 8 segment-cathode drive outputs). The additional "segment" drive is provided to accommodate displays which feature a colon. The colon output is switched at a 1/2 Hz rate to provide a blinking colon as a short-time indication that the clock is operating.

When driving vacuum fluorescent displays which enclose more than one digit in a common gas envelope, it is necessary to either (1) inhibit the segment drive voltage(s) for a short time during inter-digit transitions, or (2) avoid physical adjacent inter-digit transitions. The MM5379 auto clock utilizes an interlaced output sequence and inter-digit blanking circuitry to prevent display arcing problems. The digit sequence is: (1) digit no. 4 (unit minutes), (2) digit no. 2 (unit hours), (3) digit no. 3 (ten's of minutes), (4) digit no. 1 (ten's of hours), etc. Blanking intervals are provided to recharge level-translating capacitors located in the display segment drive lines (*Figure 6*). Both segment data and digit enables are blanked. *Figure 4* is a timing diagram which illustrates output timing for the MM5379. *Figure 5* is a timing diagram which illustrates output timing for the MM5378.

Brightness Control: Since display brightness is a function of cathode segment current, a capability of interrupting this current for a variable percentage of the digit interval results in a brightness control. Depending on the magnitude of the voltage applied, the digit "ON" time will vary from 0% to 100% of its possible period in 8 1/3% increments. This is illustrated in *Figures 4 and 5.*

Output Circuits: All display output drivers, both digit and segment outputs, are open-drain enhancement devices (*Figure 6*). Thus, all outputs are capable of sourcing currents while external pull-downs are required to sink currents. *Figure 7* illustrates method of interfacing these outputs to gas discharge displays.



SELECTED MODE	FUNCTION
SET MINUTES	MINUTES COUNTER ADVANCES AT 2 Hz RATE. HOURS COUNTER UNAFFECTED. COLON HELD "ON".
RESET	TIME SET AND HELD AT 12:00:00. COLON HELD "ON".
SET HOURS	HOURS COUNTER ADVANCES AT 2 Hz RATE. MINUTES COUNTER UNAFFECTED. COLON BLINKING.
TEST	MINUTES COUNTER ADVANCES AT 65.536 kHz RATE WITH COMPLETE CARRY. COLON HELD "ON" AT 65.536 kHz RATE.
REAL TIME	NORMAL TIME KEEPING. COLON BLINKING.
REAL TIME	NORMAL TIME KEEPING. COLON BLINKING.
RESET	TIME SET AND HELD AT 12:00:00. COLON HELD "ON".

FIGURE 3. MM5378, MM5379 Setting Control Functions

functional description (Continued)

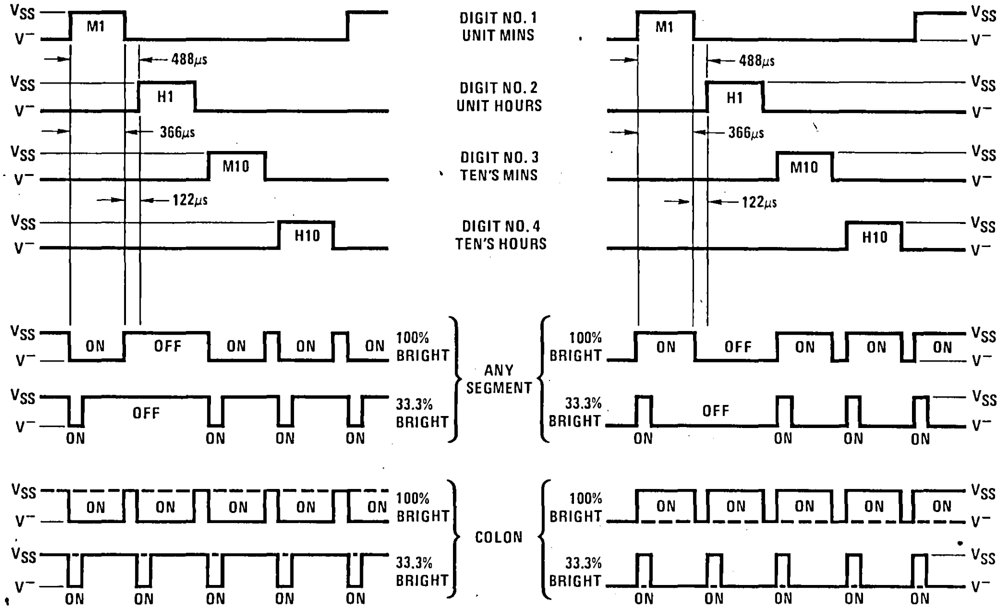


FIGURE 4. MM5379 Output Timing Diagram

FIGURE 5. MM5378 Output Timing Diagram

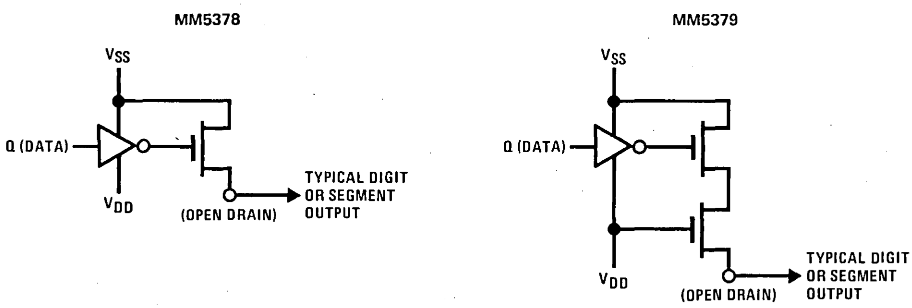


FIGURE 6. Output Circuits

functional description (Continued)

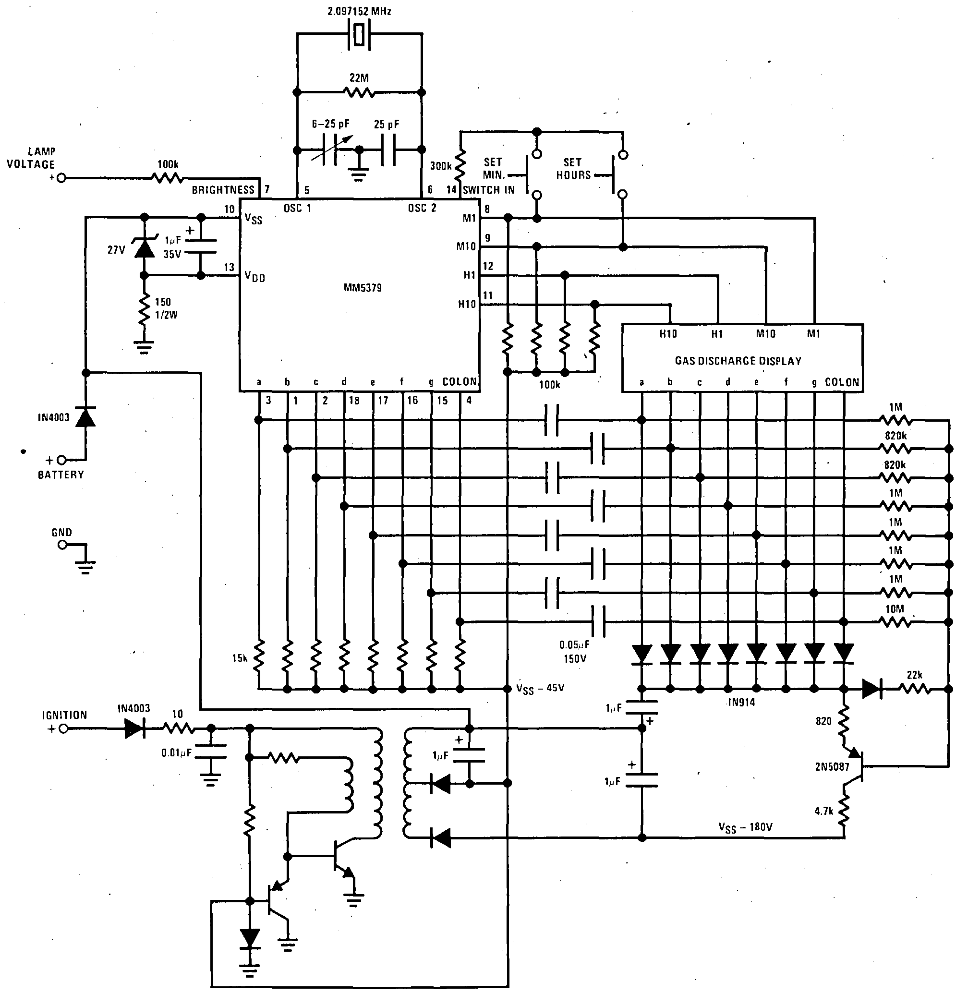


FIGURE 7. Typical Application for MM5379

MM5382, MM5383 digital calendar clock radio circuits

general description

The MM5382 and MM5383 digital calendar clock circuits provide the timing, control, and interface circuitry for a minimum-cost, solid state, digital clock radio.

The timekeeping function operates in either a 12-hour or a 24-hour mode. The MM5382 is the 12-hour version, and has a month-date format; the MM5383 is the 24-hour version, and has a date-month format.

Outputs consist of a presettable 59-minute sleep timer (e.g., a timed radio turn-off) and an alarm tone. A power failure indication warns the user that the time displayed may be in error.

Other features include: alarm display; brightness control; 24-hour alarm set; PM indication; fast and slow set controls; and a 9-minute snooze alarm. (The MM5383 has an alarm "ON" indicator.) Both circuits provide open drain outputs for the direct drive of LED displays to 15 mA.

features

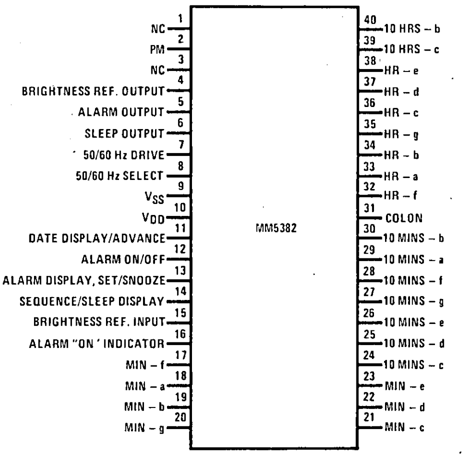
- 50 or 60 Hz operation
- 12 hour, month-date (MM5382) or 24 hour, date-month (MM5383) display
- PM indication (MM5382)
- Leading zero blanking
- 24-hour alarm setting
- Power failure indication (the word "OFF" is displayed in MM5382 and all "ON" digits blink in MM5383
- Brightness control
- Date display (4 year calendar)
- Presettable 59-minute sleep timer
- Alarm display
- Fast and slow set sleep and alarm
- 9 minute snooze alarm
- Blinking colon
- Alarm "ON" indication (MM5382 only)
- Alarm tone output
- No illegal time or date display at turn-on

applications

- Alarm clock
- Desk clock
- Clock radios
- Stop watch
- Industrial clock
- Portable clock
- Timer
- Sequential controllers

connection diagrams

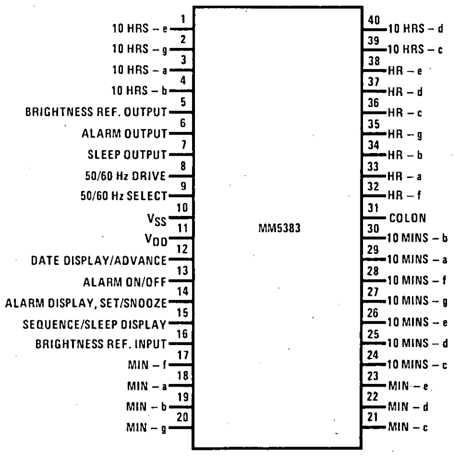
Dual-In-Line Package



TOP VIEW

Order Number MM5382N
See Package 24

Dual-In-Line Package



TOP VIEW

Order Number MM5383N
See Package 24

FIGURE 1

absolute maximum ratings

Voltage at Any Pin except Segment, Colon, and PM	V_{SS} +0.3V to V_{SS} −28V
Voltage at Segment, Colon, and PM	V_{SS} +0.3V to V_{SS} −10V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation	1 Watt
Electrical Characteristics	
T_A within Operating Range	V_{SS} = +18V to +26V, V_{DD} = 0V, with specified output drive unless otherwise specified
Functional Clock Voltage	V_{SS} = +8V to +26V, V_{DD} = 0 (No output drive spec)

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	No output levels				
	V_{SS} = 8V			4	mA
	V_{SS} = 26V			5	mA
50/60 Hz Input					
Frequency		DC	50 or 60	30k	Hz
Voltage	V_{SS} = 18V				
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+1	
Switch Input Voltages (Date, Sequence, Alarm Enable, Alarm Display)					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	
Logical Low Level (1)	Nominal Floating Level	V_{SS}−3	Float	V_{SS}−6	V
Logical Low Level (2)		V_{DD}	V_{DD}	V_{DD}+2	V
All Other Input Voltages					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	
Logical Low Level	Internal Depletion Load to V_{DD}			V_{SS}−15	
Power Failure Detect Voltages	(V_{SS} Voltage)	1.0		8.0	V
Output Currents:	V_{SS} = 18V to 26V, V_{DD} = 0V				
All Segments and Colon					
Logical High Level, Source	V_{OH} = V_{SS} −2V	15			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} −10V			10	μA
PM Indicator and Alarm Indicator					
Logical High Level, Source	V_{OH} = V_{SS} −2V	15			mA
Logical Low Level, Leakage	V_{OH} = V_{SS} −10V			10	μA
Alarm and Sleep Outputs					
Logical High Level, Source	V_{OH} = V_{SS} −2V	2			mA
Logical Low Level, Sink	V_{OH} = V_{SS} −15V	500			μA
Alarm Output Tone Frequency Modulated with 2 Hz	V_{SS} = 18V to 26V	400		2000	Hz
Total Power Dissipation	V_{SS} = 26V, V_{DD} = 0V I_{OUT} (25 Segments) = 15 mA T = 70°C V_{OUT} = V_{SS} −2V			830	mW

block diagram

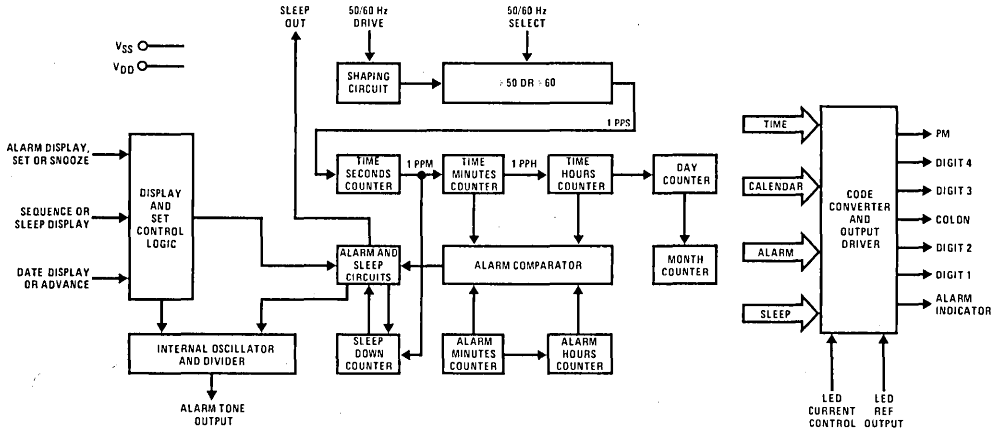


FIGURE 2.

TABLE I. Display Modes and Setting Control Functions

FUNCTION	STEP	DATE DISPLAY/ ADVANCE	ALARM DISPLAY – SET/SNOOZE	SEQUENCE/SLEEP DISPLAY
Display Time	1	Float	Float	Float
Set Time	1	Float	Float	Momentary connect to V_{DD} for each step of setting time and calendar
	2	V_{DD}	Float	Float
Display Alarm	1	Float	Connect to V_{DD} for < 2 seconds	Float
Set Alarm:				
2 Hz Rate	1	Float	Connect to V_{DD} for > 2 seconds	Float
60 Hz Rate	2	V_{DD}	V_{DD}	Float
Display Sleep	1	Float	Float	Connect to V_{SS} for < 2 seconds
Set Sleep:				
2 Hz Rate	1	Float	Float	Hold V_{SS} for > 2 seconds (Advances at 2 Hz Rate)
60 Hz Rate	2	V_{DD} (Advances at 60 Hz Rate)	Float	V_{SS}

functional description

Connection diagrams for the MM5382 and the MM5383 Digital Clock Radio Circuits are shown in *Figure 1.* A block diagram of these devices is shown in *Figure 2.* Unless otherwise indicated, the following discussions are based on *Figure 2. Figure 3* shows the general purpose alarm clock and procedure to set the time, month, day, alarm and sleep counters. Table I shows the display modes and setting control functions.

50 or 60 Hz Drive: A shaping circuit is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 4V of hysteresis. A simple RC filter should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz base. This counter is programmed to divide by 60 simply by leaving the pin unconnected; a pull-down to V_{DD} is provided by an internal resistor. Operation at 50 Hz is programmed by connecting this input to V_{SS}.

Alarm Operation: The internal alarm comparator senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The alarm latch remains set for 59 minutes during which time the alarm or radio will sound if the latch outputs are not temporarily inhibited by another latch set by the snooze input or reset by the alarm "OFF" input.

functional description (Continued)

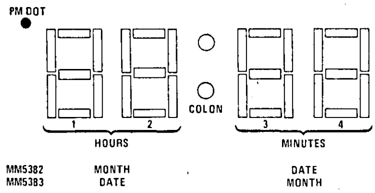
Alarm ON/OFF/RADIO Input: Momentarily leaving this input unconnected resets the alarm latch and thereby silences the alarm. This input is also used to determine if the alarm or the sleep output will be enabled when the alarm latch is set. By connecting the input pin to V_{DD}, both the alarm output and the sleep output (radio) are enabled when the alarm latch is set. If the input pin is connected to V_{SS}, only the sleep output (radio) is enabled when the alarm latch is set. Momentarily leaving this pin unconnected also readies the alarm latch for the next comparator output, hence, the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the Alarm ON/OFF Radio input pin should remain unconnected.

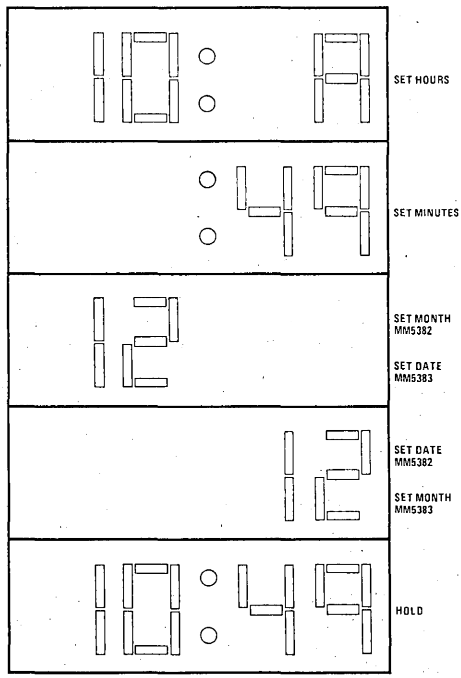
Alarm Output: The alarm output signal is a tone of from 400 Hz to 2000 Hz, which is gated on and off at a 2 Hz rate.

Alarm Display, Set/Snooze: Momentarily connecting this pin to V_{DD} when the alarm and sleep outputs are disabled displays the alarm setting for 1.5 to 2 seconds. The display shows the hours and minutes of the alarm setting, a constant colon and a PM indication if the clock is in the 12 hour mode. If the input pin is held to V_{DD} for longer than 2 seconds, the minutes of the alarm counter start to advance at a 2 Hz rate. To increase the rate that the alarm counter is set at, also connect the Date/Advance input pin to V_{DD}. The minutes of the alarm counter will now advance at a 60 Hz rate. By momentarily connecting the input pin to V_{DD} when the alarm or sleep output is enabled, snooze is enabled for 8 or 9 minutes. Snooze inhibits the alarm output for between 8 and 9 minutes, after which the alarm output is enabled again. Snooze has no effect on the sleep output. The snooze feature may be repeatedly used during the 59 minutes in which the alarm latch remains set. Momentarily connecting this input pin to V_{DD} when the clock is in the power failure mode stops all power failure indications and displays alarm. If this pin is connected to V_{SS} and date advance pin is connected to V_{SS}, the clock is in a test mode. All outputs are enabled and time and alarm are set to 12:00 AM, the date is set to the 12th month and the 1st day, and the sleep counter is set to 00 minutes. If the Alarm Display, Set/Snooze is at V_{SS}, all outputs and inputs are disabled except 50/60 Hz Select and 50/60 Hz Drive.

Sleep Timer and Output: The sleep output can be used to turn off a radio after a desired interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode and setting the desired time interval. This automatically results in a current-source output, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momentary V_{DD} connection to the Alarm Display, Set/Snooze input.

Sequence/Sleep Display and Set: If left open, time or the counter to be set is displayed. Momentarily connecting this pin to V_{SS} displays the sleep counter for 1.5 to 2 seconds. If after 2 seconds the pin is still at V_{SS}, the sleep counter will decrement at a 2 Hz rate. To increase the rate at which the sleep counter is decremented, also connect the Date/Advance pin to VDD. The sleep counter will now decrement at a 60 Hz rate. Momentarily connecting the Sequence pin to V_{DD} steps the clock through its set modes. There are 6 states; they are real time, set hours, set minutes, set month (12 hour mode), set day (12 hour mode), and the holding state. When real time is displayed, a momentary connection to V_{DD} advances the clock to the set hours state. In this state, hours are displayed, minutes are blanked, the colon is constant, and an A or P is displayed in the unit minutes position if the clock is in the 12 hour mode. To set hours, the Date/Advance pin is connected to V_{DD}. The next time the Sequence pin is connected to V_{DD}, the clock is advanced to the set minutes state. In this state, the minutes are displayed, the hours are blank, the colon is constant and the PM indication is displayed if the clock is in the 12 hour mode and set for PM. The next state the clock advances to is the set left state. In the 12 hour mode, this is a month set state. For the 24 hour mode, this is a day set state. In this state, the left two digits of the display are shown, the colon and the right two digits of the display are blank. The next state the clock advances to is the set right state. In this state, the day in the 12 hour mode or month in the 24 hour mode is displayed in the right two digits of the display.





Time and Date Display Format in 'Set' Mode

functional description (Continued)

The left two digits and colon are blank. The next transition on the Sequence input displays real time if the minutes were not set. If the minutes counter was set, the next state the clock advances to is the holding state. In this state the time and the colon are blinking at a 2 Hz rate and held to the set time. To leave the holding state, the Sequence Input is connected to V_{DD} momentarily. If the clock remains in any state except the holding state for more than 10 seconds without being set, the clock will automatically advance to real time or the holding state if minutes were set.

Note: Time set mode should not be initiated while in alarm or sleep display 2 second time out. Time set mode should be sequenced only when the clock displays real time.

Date/Advance Input: If left open, this input has no effect on the clock. Momentarily connecting this pin to V_{DD} displays the date for 1.5 to 2 seconds if the clock was not in a set state. If after 2 seconds the input pin is still at V_{DD}, the date remains displayed until the input pin is released. If the Date/Advance pin is connected to V_{DD} when the clock is in a set mode, the counter displayed will advance at a 2 Hz rate until the pin is released. Connecting this input pin to V_{DD} when the sleep counter or the alarm counter is displayed advances the displayed counter at a 60 Hz rate. If the Date/Advance pin is connected to V_{SS}, the seconds counter is bypassed and minutes counter advances at a 1 Hz rate.

Colon: The colon output blinks at a 1 Hz rate in the run mode. It is constant during set hours and minutes, and alarm display. The colon is blank for date display. The colon blinks at a 2 Hz rate in the holding state.

Alarm Indication Output: Whenever the alarm is enabled, the Alarm Indicator output is turned on. It is used to indicate to the user that the alarm has been set.

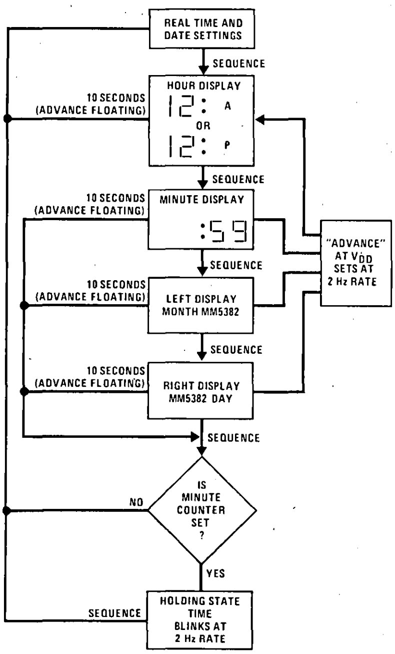
PM Output: The PM Output is available only in the MM5382. This output is enabled only when time or alarm are displayed.

Power Failure Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of the correct time, in the MM5382 the word 'OFF' is displayed blinking at a 2 Hz rate, in the MM5383 all the 'ON' segments blink at 2 Hz rate and the colon is blank. Momentarily connecting the Alarm Display Set/Snooze input to V_{DD} displays first the alarm for 1.5 to 2 seconds and then real time. In addition, if the alarm was "ON" the Alarm "ON/OFF" input should also be momentarily connected to V_{DD}.

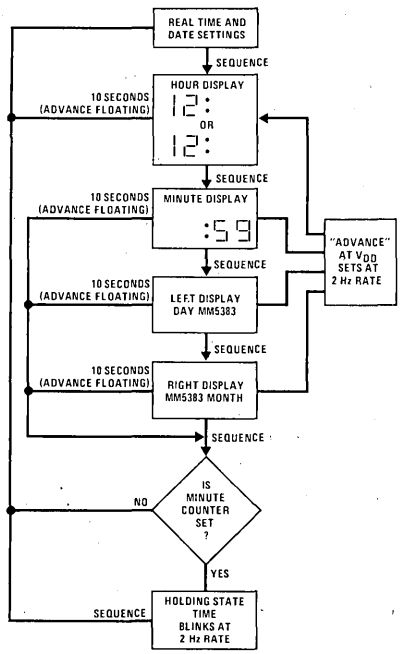
LED CURRENT CONTROL INPUT AND REFERENCE OUTPUT

Pin (15) MM5382, pin (16) MM5383 controls the gate voltage at all the display outputs and the reference device. The output drives can be disabled by connecting pin 15 MM5382, 16 MM5383 to V_{SS}. This wire-OR capability allows the display to be used for other functions (e.g., temperature). The output current can be controlled two ways; 1) driving the output in saturated mode; 2) driving the output in linear mode. (Refer to *Figures 4* and *5.*)

1. The reference device pins (4, 15) MM5382 (5, 16) MM5383 are connected as diodes and an external resistor is used to set the desired current in these diodes (see *Figure 4*). The segment drivers of all digits are connected as current mirrors. The drain



Time and Date Set Flow Chart MM5382, 12-Hour Mode



Time and Date Set Flow Chart MM5383, 24-Hour Mode

functional description (Continued)

voltage V1 of the segment drivers is selected such that these devices operate in saturation mode. Since the drain current variation in saturation mode operation of the MOS device is relatively constant, the segment drive current does not vary significantly, even though V1 is increased considerably. However, as the voltage across the output buffers increases, average power dissipation also increases linearly. This technique of current control is recommended to be used only with low current LEDs (1–7 mA).

2. The high current drive requirement of large LED displays can be accomplished by operating the segment drivers in the linear mode. The circuit for high current LED drivers is shown in *Figure 5.* The reference output device is used in series with a reference LED, diode and current setting resistor. A high beta PNP transistor provides the current drive for all the segments. A reference voltage V3 is developed which compensates for variations in MOS process parameters and the variations in the voltage drop across the LED. The resistor sets the current in the reference LED which sets the reference voltage V3 which in turn sets the current in the LEDs equal to resistor current minus the base current of the transistor. Variation in second supply voltage does not vary the LED currents so long as the PNP transistor is kept operating in the linear mode. Full wave rectified power supply without any filtering can be used as a second supply voltage V2. The LED brightness can be varied by using a variable resistor.

Figure 6 shows a LED drive circuit which uses a single resistor. The resistor controls the total current flowing through all the segments. Brightness shall vary depending on number of segments that are "ON" at that time.

Radio Frequency Interference: All display outputs include circuitry to slow up the switching transition time to minimize radio frequency interference.

Clock Set Up Procedure: (MM5382)

1. Connect 110V supply.
2. Blinking 'OFF' displayed.
3. Momentarily connect alarm display set/snooze pin (13) to V_{DD} which removes "OFF" and displays first the alarm for 1.5 to 2 seconds, then real time.
4. Momentarily connect alarm "ON/OFF" to V_{SS}.
5. *Wait till the colon starts blinking.* (Approximately 2 seconds.)
6. Time setting
   a. Momentarily connect sequence pin (14) to V_{DD} display shows hour and AM or PM. Connect advance pin (11) to V_{DD} to advance hour.
   b. Connect pin (14) momentarily to V_{DD} display shows minutes, connect pin (11) to V_{DD} and set minutes.
   c. Connect pin (14) momentarily to V_{DD} display shows month, connect pin (11) to V_{DD} and set month.
   d. Connect pin (14) momentarily to V_{DD} display shows date, connect pin (11) to V_{DD} and set date.
   e. Connect pin (14) momentarily to V_{DD} and the real time is displayed at 2 Hz rate.
   f. Connect pin (14) momentarily to V_{DD} again and real time is displayed continuously.
7. Alarm setting
   a. Connect alarm display pin (13) to V_{DD} and hold it for more than 2 seconds. Alarm minutes will advance at slow rate.
   b. Connecting pin (11) and pin (13) to V_{DD} simultaneously will advance the alarm time at a fast rate.
   c. Set the desired alarm time.
8. Sleep time setting
   a. Connect, sleep display, pin (14) to V_{SS} and hold it for more than 2 seconds. Sleep time will decrement at slow rate.
   b. Connecting pin (11) and pin (14) to V_{DD} simultaneously will decrement the sleep time at a fast rate.
   c. Set the desired sleep time.
9. Connect pin 12 to V_{DD} to activate alarm.

Note: Time and date setting must be done only in the real time display mode.

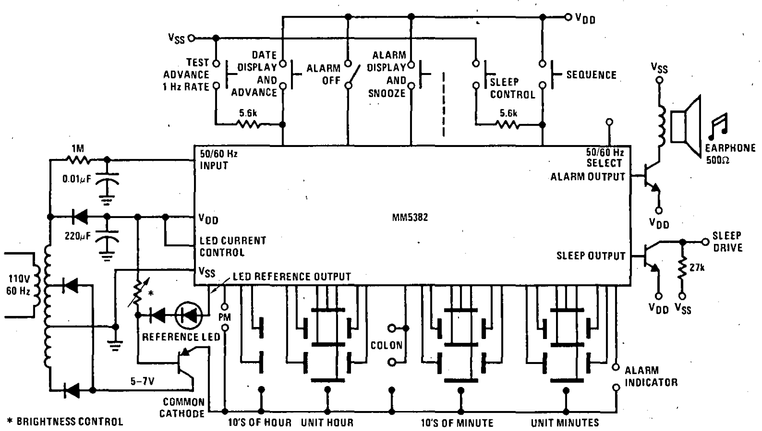


FIGURE 3. Calendar Alarm Clock Using the MM5382 and a LED Display

functional description (Continued)

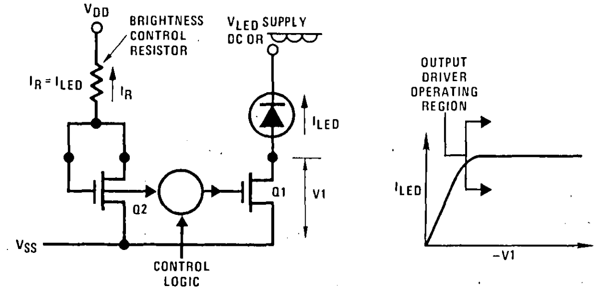


FIGURE 4(a). Low Current LED Drive Control Circuit (1–7 mA)

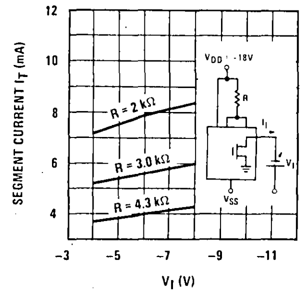


FIGURE 4(b). Segment Current vs V_I (V_{DD} at −18V) (Typical Output Characteristics)

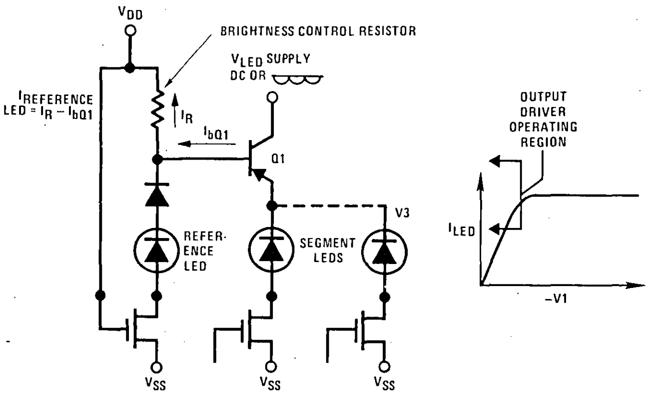


FIGURE 5(a). High Current LED Drive Current Circuits (7–15 mA)

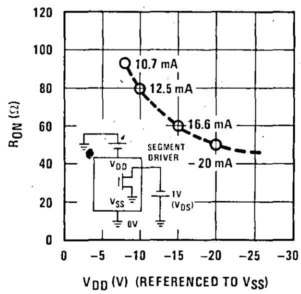


FIGURE 5(b). R_{ON} vs V_{DD} (V_{DS} at −1V) (Typical Output Characteristics)

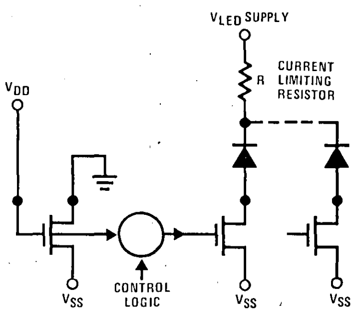


FIGURE 6. Simple LED Drive Circuit

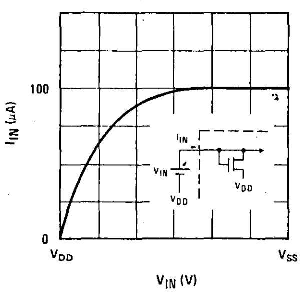


FIGURE 7. I_{IN} vs V_{IN} (Typical Input Depletion Load Characteristics)

Clocks

MM5384 LED display digital clock radio circuit

general description

The MM5384 digital clock radio circuit is a monolithic MOS integrated circuit utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. It provides all the logic required to build several types of clocks and timers. Four display modes (time, seconds, alarm and sleep) are provided to optimize circuit utility. The circuit interfaces directly with 3 1/2 digit 7-segment LED displays. The timekeeping function operates from either a 50 or 60 Hz input, and the display format is 12 hours (with leading-zero blanking and AM/PM indication) or 24 hours. Outputs consist of display drivers, sleep (e.g., timed radio turn-off), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. Setting the time cancels this indication. The device operates over a power supply range of 8–26V and does not require a regulated supply. The MM5384 is packaged in a 40 lead dual-in-line package.

features

- 50 or 60 Hz operation
- Single power supply
- 12 or 24 hour display format
- AM/PM outputs } 12-hour format
- Leading-zero blanking } 12-hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Blanking/brightness control capability
- Elimination of illegal time display at turn-on
- Direct interface to 0.5" LED displays
- 9-minute snooze alarm
- Presettable 59-minute sleep timer

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block and connection diagrams

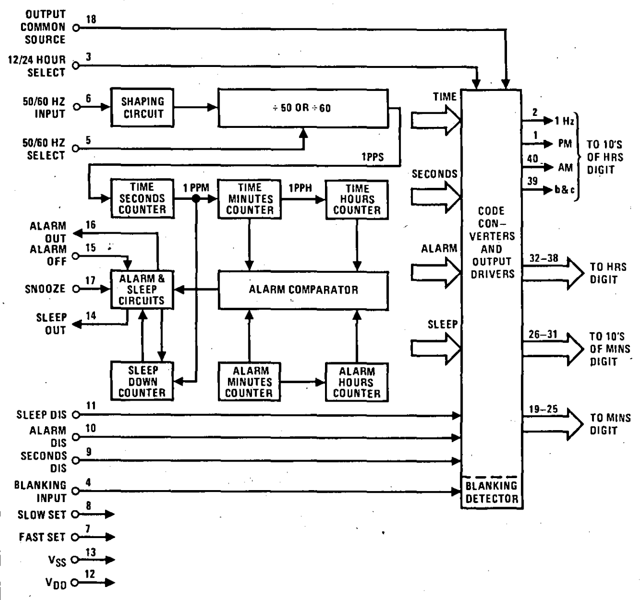
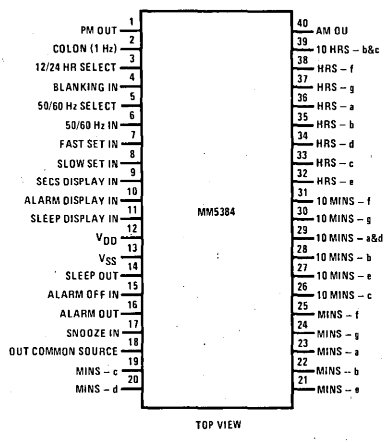


FIGURE 1.

Dual-In-Line Package



Order Number MM5384N
See Package 24

FIGURE 2

absolute maximum ratings

Voltage at Any Pin Except Segment Outputs	V_{SS} + 0.3 to V_{SS} − 30V
Voltage at Segment Outputs	V_{SS} + 0.3 to V_{SS} − 15V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 24V to 26V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	Output Driving Display	24		26	V
	Functional Clock	8		26	V
Power Supply Current	No Output Loads				
	V_{SS} = 8V			4	mA
	V_{SS} = 26V			5	mA
50/60 Hz Input Frequency Voltage	V_{SS} = 8V to 26V	dc	50 or 60	10k	Hz
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+2	V
50/60 Hz Input Leakage				10	μA
Blanking Input Voltage					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−5	V
Blanking Input Leakage				10	μA
All Other Input Voltages					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Device to V_{DD}	V_{DD}	V_{DD}	V_{SS}−6	V
Power Failure Detect Voltage	(V_{SS} Voltage), (Note 2)	1		8	V
Count Operating Voltage		8		26	V
Hold Count Voltage	(Note 2)			26	V
Output Current Levels	V_{SS} = 24V to 26V, Output Common = V_{SS}				
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level, Source	V_{OH} = V_{SS} − 7V	10			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} − 14V			10	μA
1 Hz Display					
Logical High Level, Source	V_{OH} = V_{SS} − 7	15			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} − 14			10	μA
All Other Displays					
Logical High Level, Source	V_{OH} = V_{SS} − 7V	5			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} − 14V			10	μA
Alarm and Sleep Outputs	V_{SS} = 24V				
Logical High, Source	V_{OH} = V_{SS} − 2	500			μA
Logical Low, Sink	V_{OL} = V_{DD} + 2	1			μA

Note 1: Segment Output Current must be limited to 6 mA maximum by user; power dissipation must be limited to 900 mW at 70°C and 1.2W at 25°C.

Note 2: Power fail detect voltage is 0.25V or more above the hold count voltage. The power fail latch trips into power fail mode at least 0.25V above the voltage at which data stored in the time latch is lost.

functional description

A block diagram of the MM5384 digital clock radio circuit is shown in *Figure 1*. The various display modes provided by this clock are listed in Table I. The functions of the setting controls are listed in Table II. *Figure 2* is a connection diagram. The following discussions are based on *Figure 1*.

50 or 60 Hz Input: A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 6V of hysteresis. A simple RC filter such as shown in *Figure 5*, is recommended in order to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Inputs: A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving 50/60 Hz select unconnected; pull-down to V_{DD} is provided by an internal depletion device. Operation at 50 Hz is programmed by connecting 50/60 Hz select to V_{SS}.

Display Mode Select Inputs: In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal pull-down depletion devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs: Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal pull-down depletion devices are provided; application of V_{SS} to these pins affects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, by selecting seconds display and actuating both slow and fast set inputs.

Blanking Control Inputs: Connecting this Schmitt Trigger input to V_{DD} places all display drivers in a non-conducting, high-impedance state, thereby inhibiting the display. See *Figures 3 and 4*. Conversely V_{SS} applied to this input enables the display. This input does not have internal pull-down device.

Output Common Source Connection: All display output drivers are open-drain devices with all sources common *(Figure 4)*. Common source pin should be connected to V_{SS}.

12 or 24-Hour Select Input: By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal pull-down depletion device is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. See *Figure 6* for 24-hour application.

Power Fail Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, the AM or PM indicator will flash at 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal.

Alarm Operation and Output: The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver *(Figure 4)*, the MM5384 output that is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input or reset by the alarm off input.

Snooze Alarm Input: Momentarily connecting snooze to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm Off Input : Momentarily connecting alarm off to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion device. The momentary alarm off input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm off input should remain at V_{SS}.

Sleep Timer and Output: The sleep output at pin 14 can be used to turn off a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode. (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output via pin 14, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning off the radio. This turn-off may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the Snooze input. The output circuitry is the same as the other outputs *(Figure 4)*.

functional description (Continued)

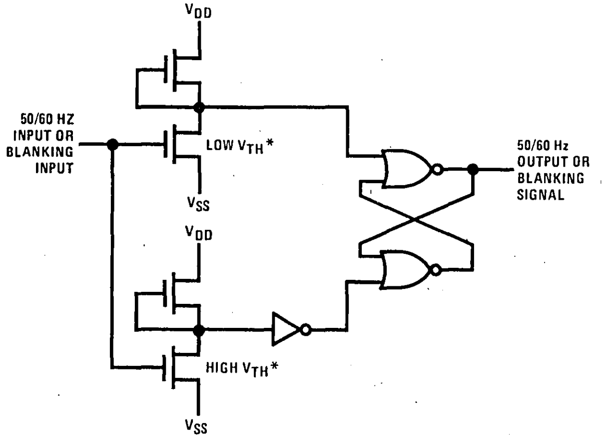


FIGURE 3. 50/60 or Blanking Input Shaping Circuits

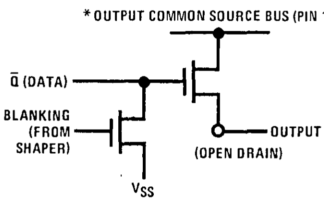


FIGURE 4a. Segment Outputs

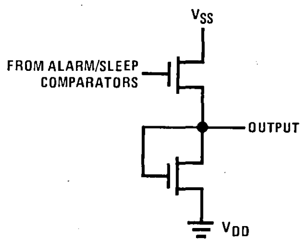


FIGURE 4b. Alarm and Sleep Outputs

TABLE I. MM5384 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

functional description (Continued)

TABLE II. MM5384 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (12-hour format)
	Both	Alarm Resets to 00:00 (24-hour format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (12-hour format)
	Both	Time Resets to 00:00:00 (24-hour format)
Sleep	Slow	Substracts Count at 2 Hz
	Fast	Substracts Count at 60 Hz
	Both	Substracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

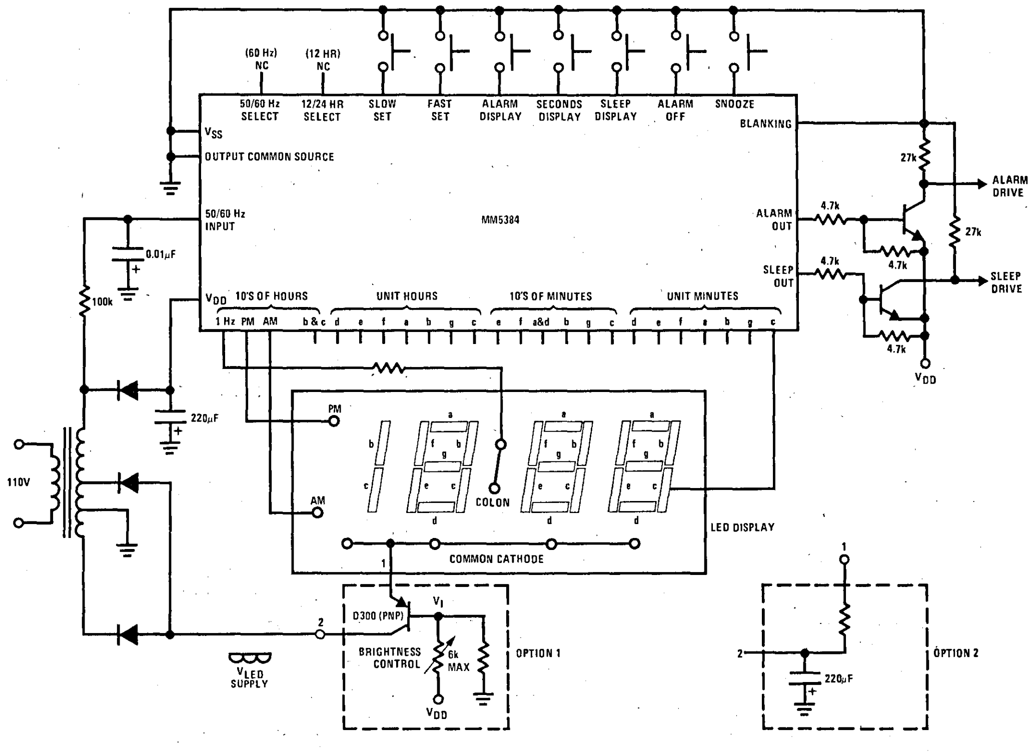
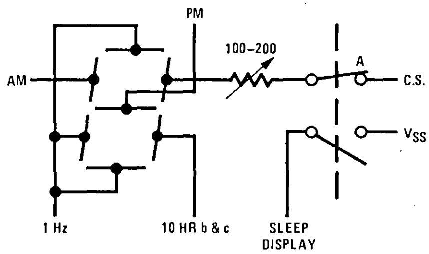


FIGURE 5. A Schematic Diagram of a General Purpose Alarm Clock (12-Hour Mode) using the MM5384 and a 3 1/2-Digit LED Display

functional description (Continued)



Switch A must be ganged with Sleep display switch as shown.

FIGURE 6. 24-Hour Operation: 10's of Hours Digit Connections

MM5385, MM5386, MM5396, MM5397 digital alarm clocks

general description

The MM5385, MM5386, MM5396 and MM5397 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. MM5385 or MM5396 and MM5386 or MM5397 have display formats of 12 hours and 24 hours respectively, with 24-hour alarm display capability. They provide all the logic required to build several types of clocks and timers. Four display modes (time, seconds, alarm and sleep) are provided to optimize circuit utility. The circuit interfaces directly with 7-segment light emitting diodes and requires two power supplies. The timekeeping function operates from either a 50 or 60 Hz input. MM5385 or MM5396 displays 12 hours with colon flashing at a one second rate and a PM indication. MM5386 or MM5397 displays 24 hours with leading zero blanking. Outputs consist of display drives, sleep (e.g., timed radio turn off), and alarm enable. Power failure indication is provided to inform the user that incorrect time is being displayed. The power failure indication consists of flashing of all the "ON" digits at a 1 Hz rate. Setting the time cancels this indication. The device operates over a power supply range of 18–26V and LED supply voltage of 4–7V.

The MM5396 and MM5397 are reverse lead-bend versions (mirror image) of the MM5385, MM5386 (respectively) ideally suited to facilitate PC board layouts when designing an "L" shaped clock "module" (vertical display, horizontal component board); the MM5385, MM5386 are better suited for applications where the display and IC are mounted on a PC board in the same plane. All four versions are supplied in a 40-lead dual-in-line package.

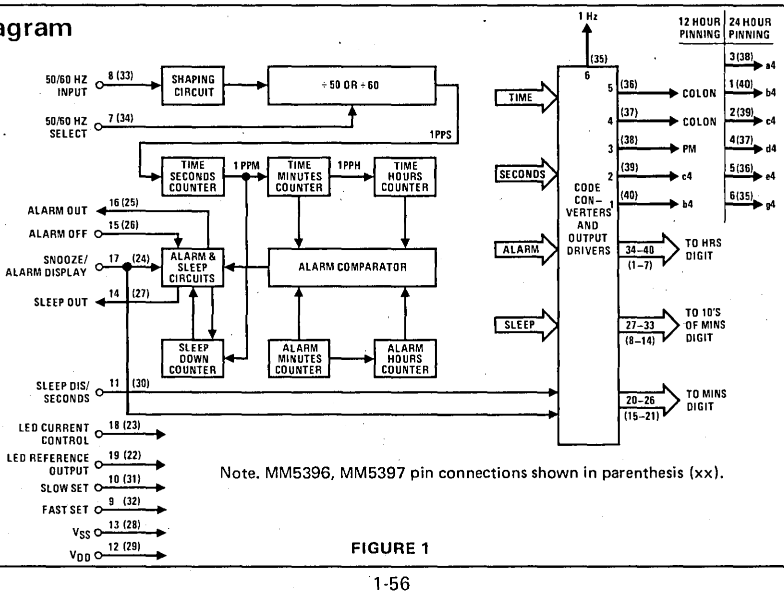
features

- 50 or 60 Hz operation
- Low power dissipation
- PM outputs in 12-hour format with a colon flashing at a one second rate ((MM5385 and MM5396 only)
- Leading zero blanking
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Blanking/brightness control capability
- Direct interface to light emitting diode (LED) with forward current of 3–15 mA
- Individual drivers for each segment of each digit
- 9-minute snooze alarm
- Presettable 59-minute sleep timer
- Radio frequency interference eliminating slow up circuitry at the outputs
- Available in standard (MM5385, MM5386) or reverse lead-bend version (MM5396, MM5397)

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block diagram



Note. MM5396, MM5397 pin connections shown in parenthesis (xx).

FIGURE 1

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 28V
Voltage at Any Output Pin	V_{SS} + 0.3 to V_{SS} − 7.5V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 18V to 26V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})	Output Driving Display	18		26	V
	Functional Clock	8		26	V
Power Supply Current	No Output Loads, V_{SS} = 26V			5	mA
50/60 Hz Input Frequency Voltage		dc	50 or 60	10k	Hz
Logical High Level		V_{SS}−1		V_{SS}	V
Logical Low Level		V_{DD}		V_{DD}+1	V
All Other Input Voltages Except Sleep/Seconds Display	(Note 2)				
Logical High Level		V_{SS}−1		V_{SS}	V
Logical Low Level	Internal Depletion Device to V_{DD}	V_{DD}		V_{DD}+7	V
Power Failure Detect Voltage	(V_{SS} Voltage) (Note 1)	1		7.5	V
Output Currents	V_{SS} = 18V to 26V, V_{DD} = 0V. Current Measured in Individual Segment Driver with 0 Current in Remaining Segment Driver. LED Current Control Connected to V_{DD}				
All Segment Drivers					
Logical High Level	$V_{OH} = V_{SS} - 2$	15			mA
Logical Low Level	$V_{OL} = V_{SS} - 6$			10	µA
Alarm and Sleep Outputs					
Logical High Level	$V_{OH} = V_{SS} - 2V$	500			µA
Logical Low Level	$V_{OL} = V_{DD} + 2$			1	µA
LED Reference Output	LED Current Control Connected to V_{DD}, V_{SS} = 18V, All Segment Driver 0 Current				
Logical High Level	$V_{OH} = V_{SS} - 2$	15			mA
Logical Low Level	$V_{OL} = V_{SS} - 6$			10	µA

Note 1: The power-fail detect voltage is 0.5V or more above the hold count voltage. The power-fail latch trips into the power-fail mode at least 0.5V above the voltage at which data stored in the time latch is lost.

Note 2: Sleep/seconds display (pin 11 on MM5385 and MM5386, pin 30 on MM5396 and MM5397). Connect pin to V_{SS} for Sleep display. Connect pin to V_{DD} for Seconds display. Leave pin open for normal time display.

functional description

A block diagram of the MM5385, MM5386, MM5396 and MM5397 digital alarm clock is shown in *Figure 1*. The various display/setting modes are listed in Table I and Table II shows the setting control functions. The following description is based on *Figure 1*; for simplification, pin numbers in the text are shown only for the MM5385 and MM5386, but pin connections for the MM5396 and MM5397 may be cross-referenced from the diagrams in *Figure 2*.

50 or 60 Hz Input (pin 8): A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt Trigger that is designed to provide about 6V of hysteresis. A simple RC filter, such as shown in *Figure 7*, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

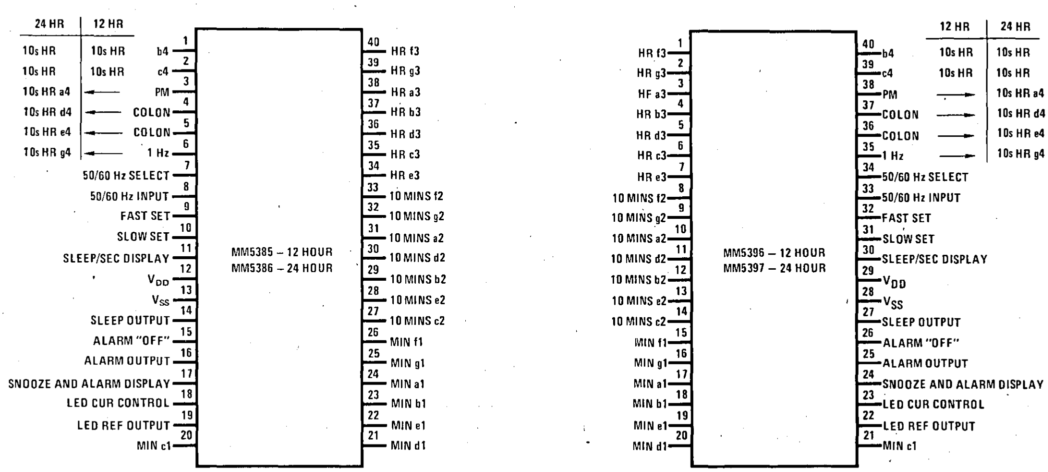
50 or 60 Hz Select Input (pin 7): A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 pps time base. This counter is programmed to divide by 60 simply by leaving pin 7 unconnected; pull-down to V_{DD} is provided by an internal depletion load. Operation at 50 Hz is programmed by connecting pin 7 to V_{SS}.

Display Mode Select Inputs (pins 11 and 17): In the absence of any of these two inputs (i.e., pin open), the display drivers present time-of-day information to the appropriate display digits. Snooze/alarm display input has an internal pull-down depletion load to V_{DD}. Sleep/seconds display input has an internal voltage control which allows this input to assume three input states. The sleep time can be displayed by connecting pin 11 to V_{SS} and seconds can be displayed by connecting pin 11 to V_{DD}, and if pin 11 is left open, normal time is displayed. If more than one mode is selected, the priorities are as noted in Table I. As shown in *Figure 1* the code converters receive time, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs (pins 9 and 10): Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal depletion loads to V_{DD} are provided, application of V_{SS} to these pins affects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM (midnight), in the 12-hour format (0:00:00 in the 24-hour format), by selecting seconds display and actuating both slow and fast set inputs.

Alarm Operation and Output (pin 16): The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the open drain alarm output driver to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input (pin 17) or reset by the alarm "OFF" input (pin 15).

Snooze/Alarm Display (pin 17): Momentarily connecting pin 17 to V_{SS} inhibits the alarm output for between 8 and 9 minutes after which the alarm will again be sounded and display alarm time. This input is pulled-down to V_{DD} by an internal depletion load. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains are set; connecting pin 17 to V_{SS} displays alarm time.



TOP VIEW

Order Number MM5385N or MM5386N
See Package 24

TOP VIEW

Order Number MM5396N or MM5397N
See Package 24

FIGURE 2

functional description (Continued)

Alarm "OFF" Input (pin 15): Momentarily connecting pin 15 to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion load. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at V_{SS}.

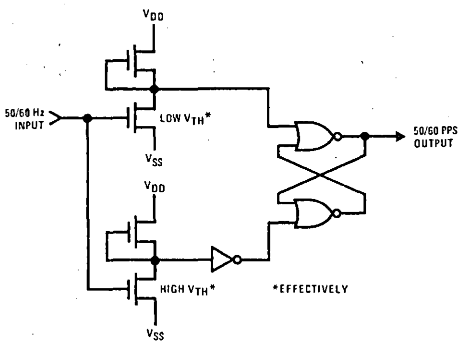


FIGURE 3. 50/60 Hz Input Shaping Circuits

Sleep Timer and Output (pin 14): The sleep output at pin 14 can be used to turn off a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output via pin 14, which can be used to turn on a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output drive is removed, thereby turning off the radio. This turn off may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the snooze input (pin 17).

Segment Outputs (pins 1–6 and 20–40): All segment outputs are open drain devices with all sources connected to V_{SS}. Each segment output may source direct current of 15 mA at 2V on the output device. *Figure 5(b)* shows the output resistance (R_{ON}) of segment driver with respect to V_{DD}.

Power Failure Indications: Power failure indication is shown by the flashing of all "ON" digits at 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal. The power failure latch trips into the power failure mode prior to the loss of data stored in the time latches. When powered up, alarm and sleep outputs will be in the "OFF" state. In order to assure guaranteed power fail indication, power supply rise time should not exceed 10 V/ms.

LED CURRENT CONTROL INPUT AND REFERENCE OUTPUT (PINS 19 AND 18)

Pin 18 controls the gate voltage at all the display outputs and the reference device. The output drivers can be disabled by connecting pin 18 to V_{SS}. This wire-OR capability allows the display to be used for other functions (e.g., temperature, radio frequency wavelength).

TABLE I. MM5385, MM5386, MM5396, MM5397 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

*If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE II. MM5385, MM5386, MM5396, MM5397 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (Midnight) (MM5385, MM5396)
	Both	Alarm Resets to 0:00 (MM5386, MM5397)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (Midnight) (MM5385, MM5396)
	Both	Time Resets to 0:00:00 (MM5386, MM5397)
Sleep	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 60 Hz
	Both	Subtracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

functional description (Continued)

The output current can be controlled two ways: 1) driving the output in saturated mode; 2) driving the output in linear mode. (Refer to *Figures 4 and 5)*.

1) The reference device (pins 18 and 19) is connected as a diode, and an external resistor is used to set the desired current in this diode (see *Figure 4*). The segment drivers of all digits are connected as current mirrors. The drain voltage V1 of the segment drivers is selected such that these devices operate in saturation mode. Since the drain current variation in saturation mode operation of the MOS device is relatively constant, the segment drive current does not vary significantly, even though V1 is increased considerably. However, as the voltage across the output buffers increases, average power dissipation also increases linearly. This technique of current control is recommended to be used only with low current LEDs (1–7 mA).

2) The high current drive requirement of large LED displays can be accomplished by operating the segment drivers in the linear mode. The circuit for high current LED drivers is shown in *Figure 5*. The reference output device is used in series with a reference LED, diode and current setting resistor. A high beta PNP transistor provides the current drive for all the segments. A reference voltage V3 is developed which compensates for variations in MOS process parameter and the variations in the voltage drop across the LED. The resistor sets the current in the reference LED which sets the reference voltage V3. This in turn sets the current in the LEDs equal to resistor current less the base current of the transistor. Variation in second supply voltage does not vary the LED currents so long as the PNP transistor is kept operating in the linear mode. Full wave rectified power supply without any filtering can be used as a second supply voltage V2. The LED brightness can be varied by using a variable resistor.

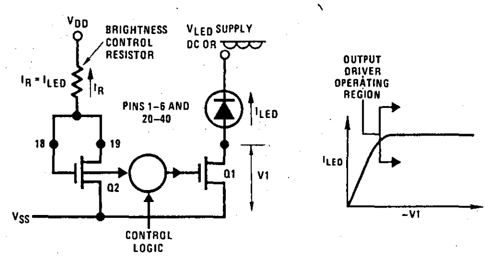


FIGURE 4(a). Low Current LED Drive Control Circuit (1–7 mA)

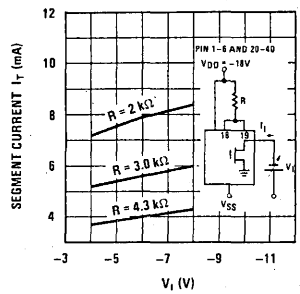


FIGURE 4(b). Segment Current vs V_I (V_{DD} at −18V) (Typical Output Characteristics)

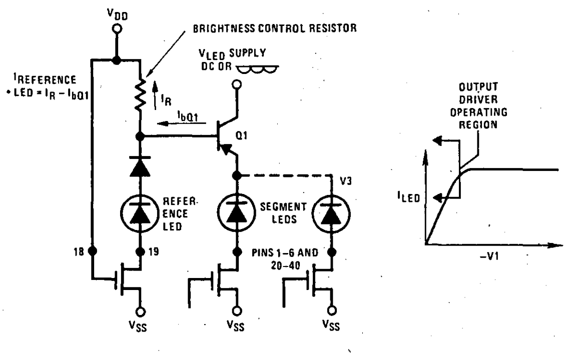


FIGURE 5(a). High Current LED Drive Control Circuit (7–15 mA)

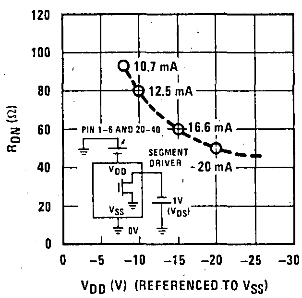


FIGURE 5(b). R_{ON} vs V_{DD} (V_{DS} at −1V) (Typical Output Characteristics)

functional description (Continued)

Figure 6 shows a LED drive circuit which uses a single resistor. The resistor controls the total current flowing through all the segments. Brightness shall vary depending on number of segments that are on at that time.

Radio Frequency Interference: All display outputs include circuitry to slow up the switching transition time to minimize radio frequency interference.

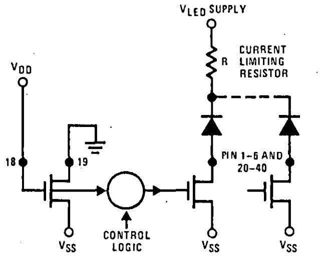


FIGURE 6. Simple LED Drive Circuit

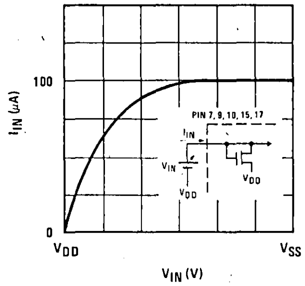


FIGURE 7. I_{IN} vs V_{IN} (Typical Input Depletion Load Characteristics)

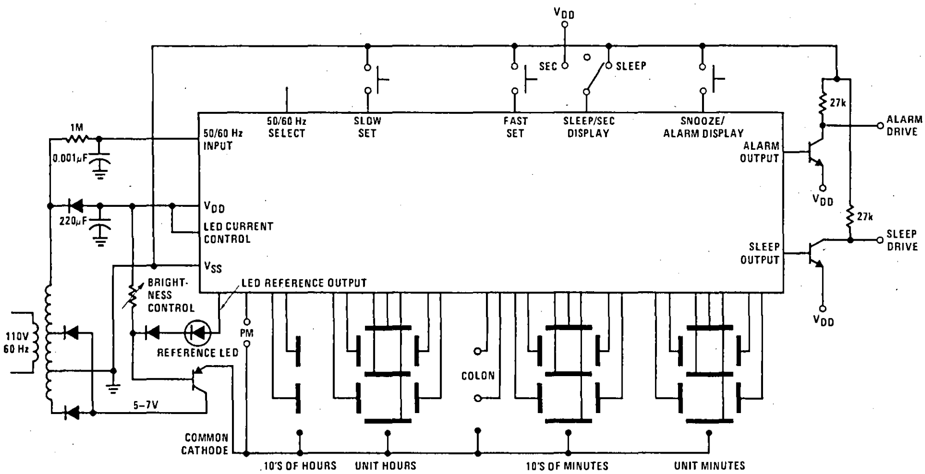


FIGURE 8. General Purpose Alarm Clock Using the MM5385 or MM5396 and LED Display

Clocks

MM5387AA, MM53108 digital alarm clocks

general description

The MM5387AA, MM53108 digital alarm clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers with up to four display modes (time, seconds, alarm and sleep) to maximize circuit utility, but are specifically intended for clock-radio applications. Both devices will directly-drive 7-segment LED displays in either a 12 hour format (3½ digits) with lead-zero blanking, AM/PM indication and flashing colon, or 24 hour format (4 digits) through hard-wire pin selection; the timekeeping function operates from either a 50 or 60 Hz input, also through pin selection. Outputs consist of display drivers, sleep (e.g., timed radio turn-off), and alarm enable. A power-fail indication mode is provided to inform the user of incorrect time display by flashing all "ON" digits at a 1 Hz rate, and is cancelled by simply resetting time. The device operates over a supply range of 24–26V which does not require regulation.

The MM53108 is electrically identical to the MM5387AA, but with mirror-image pin-out to facilitate PC board layout when designing a "module" where the LED display and MOS chip are mounted on the same side; the MM5387AA is more suited for "L" shaped module designs (vertical LED display, horizontal component board). Both devices are supplied in a 40-lead dual-in-line package.

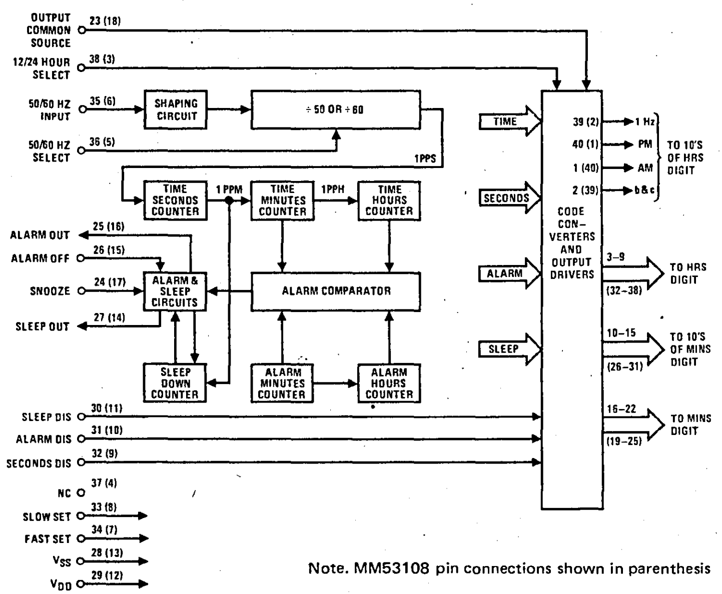
features

- 50 or 60 Hz operation
- Single power supply
- 12 or 24 hour display format
- AM/PM outputs } 12 hour format
- Leading-zero blanking } 12 hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Elimination of illegal time display at turn "ON"
- Direct interface to LED displays
- 9-minute snooze alarm
- Presettable 59-minute sleep timer
- Available in standard (MM5387AA) or mirror image (MM53108) pin-out

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block diagram



Note. MM53108 pin connections shown in parenthesis

FIGURE 1

absolute maximum ratings

Voltage at Any Pin Except Segment Outputs	V_{SS} + 0.3 to V_{SS} − 30V
Voltage at Segment Outputs	V_{SS} + 0.3 to V_{SS} − 15V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 24V–26V, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	Output Driving Display	24		26	V
	Functional Clock	8		26	V
Power Supply Current	No Output Loads				
	V_{SS} = 8V			4	mA
	V_{SS} = 26V			5	mA
50/60 Hz Input					
Frequency Voltage	V_{SS} = 8V to 26V	dc	50 or 60	10k	Hz
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{DD}+2	V
Input Leakage				100	μA
All Other Input Voltages					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level	Internal Depletion Load to V_{DD}	V_{DD}	V_{DD}	V_{SS}−6	V
Power Failure Detect Voltage	(V_{SS} Voltage), (Note 2)	1		7.5	V
Count Operating Voltage		8		26	V
Hold Count Voltage		(Note 2)		26	V
Output Current Levels	V_{SS} = 24V to 26V, Output Common = V_{SS}				
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level, Source	V_{OH} = V_{SS} − 4V	16			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} − 14V			10	μA
1 Hz Display					
Logical High Level, Source	V_{OH} = V_{SS} − 4	24			mA
Logical Low Level, Leakage	V_{OL} = V_{SS} − 14			10	μA
All Other Displays					
Logical High Level, Source	V_{OH} = V_{SS} − 4V	8		(Note 1)	mA
Logical Low Level, Leakage	V_{OL} = V_{SS} − 14V			10	μA
Alarm and Sleep Outputs	V_{SS} = 24V				
Logical High , Source	V_{OH} = V_{SS} − 2	500			μA
Logical Low, Sink	V_{OL} = V_{SS} − 2	1			μA

Note 1: Segment output current must be limited to 11 mA maximum by user; power dissipation must be limited to 900 mW at 70°C and 1.2W at 25°C.

Note 2: The power-fail detect voltage is 0.5V or more above the hold count voltage. The power-fail latch trips into power-fail mode at least 0.5V above the voltage at which data stored in the time latch is lost.

functional description

A block diagram of the MM5387AA, MM53108 digital clock radio circuit is shown in *Figure 1*. The various display setting modes are listed in Table I, and Table II shows the setting control functions. The following description is based on *Figure 1* and refers to both devices as they are electrically identical.

50 or 60 Hz Input: A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 6V of hysteresis. A simple RC filter such as shown in *Figure 7*, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving 50/60 Hz select unconnected; pull-down to V_{DD} is provided by an internal depletion load. Operation at 50 Hz is programmed by connecting 50/60 Hz select to V_{SS}.

Display Mode Select Inputs: In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal depletion pull-down devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs: Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal depletion pull-down devices are provided; application of V_{SS} to these pins affects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, by selecting seconds display and actuating both slow and fast set inputs.

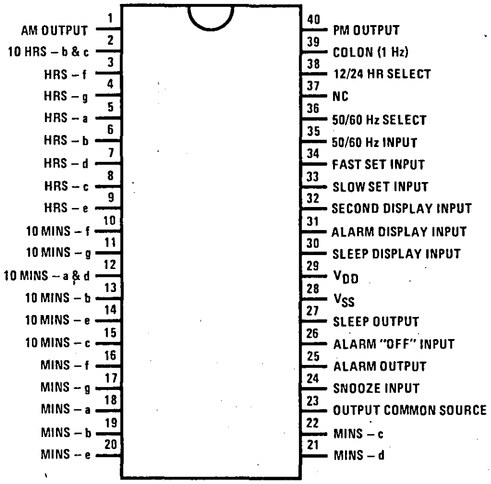
Output Common Source Connection: All display output drivers are open-drain devices with all sources common *(Figure 4a)*. The common source pin should be connected to V_{SS}.

12 or 24 Hour Select Input: By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal depletion pull-down device is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Segment connections for 10's of Hours in 24-hour mode are shown in *Figure 6*.

Power Fail Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, all "ON" segments will flash at 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal.

connection diagrams

Dual-In-Line Package

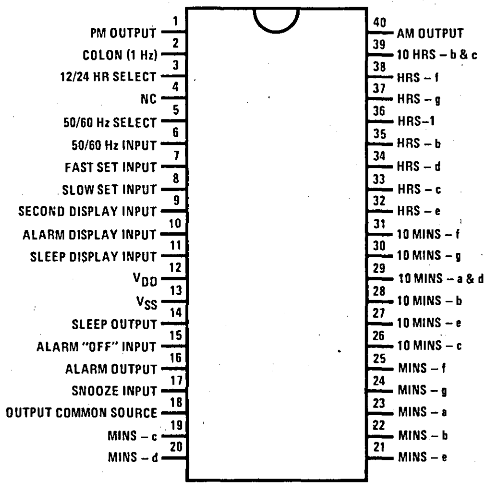


TOP VIEW

Order Number MM5387AAN
See Package 24

FIGURE 2(a). MM5387AA

Dual-In-Line Package



TOP VIEW

Order Number MM53108N
See Package 24

FIGURE 2(b). MM53108 (Mirror Image Pin-Out)

functional description (Continued)

Alarm Operation and Output: The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver *(Figure 4b)* which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input or reset by the alarm "OFF" input.

Snooze Alarm Input: Momentarily connecting snooze to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-down to V_{DD} by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm "OFF" Input: Momentarily connecting alarm "OFF" to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion device. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at V_{SS}.

Sleep Timer and Output: The sleep output can be used to turn "OFF" a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode, (Table I) and setting the desired time interval (Table II). This automatically results in a current-source output which can be used to turn "ON" a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning "OFF" the radio. This turn "OFF" may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the Snooze input. The output circuitry is the same as the other outputs *(Figure 4b)*.

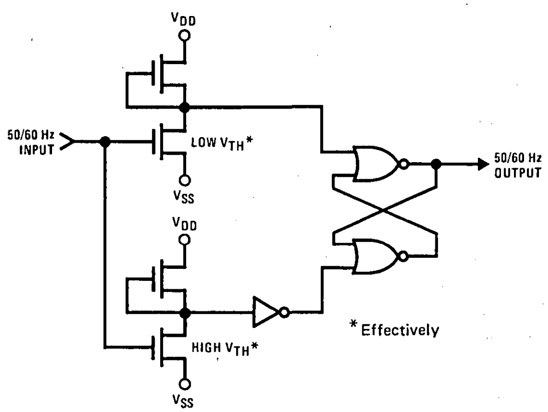


FIGURE 3. 50/60 Hz Input Shaping Circuit

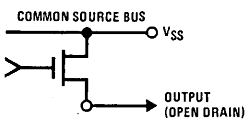


FIGURE 4(a). Segment Outputs

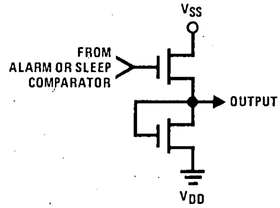


FIGURE 4(b). Alarm and Sleep Outputs

functional description (Continued)

TABLE I. MM5387AA, MM53108 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

* If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE II. MM5387AA, MM53108 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (Midnight) (12-Hour Format)
	Both	Alarm Resets to 00:00 (24-Hour Format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (Midnight) (12-Hour Format)
	Both	Time Resets to 00:00:00 (24-Hour Format)
Sleep	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 60 Hz
	Both	Subtracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

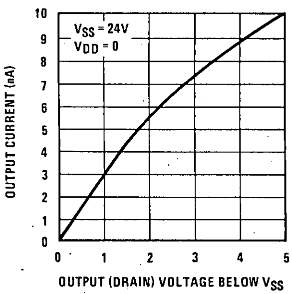
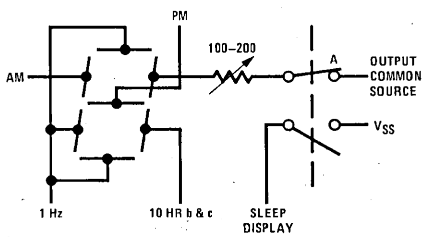


FIGURE 5. Typical Output Current Characteristics of MM5387AA, MM53108



Switch A must be ganged with Sleep display as shown.

FIGURE 6. 24-Hour Operation: 10's of Hours Digit Connections

typical applications

Figure 7 is a schematic diagram of a general purpose alarm clock circuit (12-hour mode) using the MM5387AA or MM53108 and a 3 1/2-digit LED display.

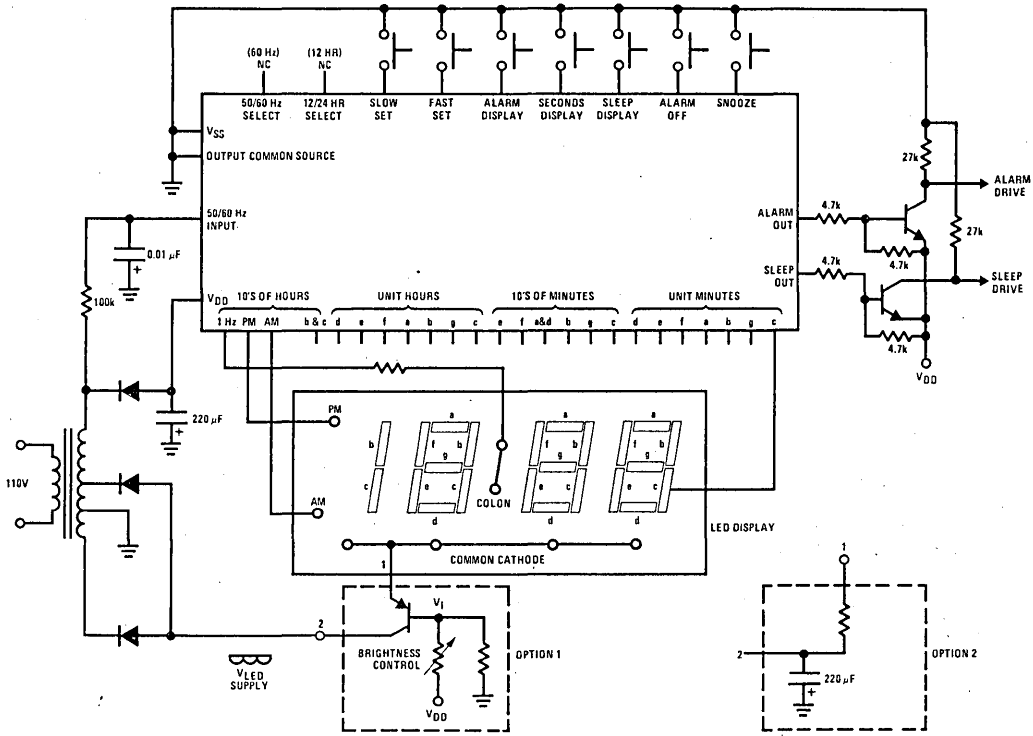


FIGURE 7

MM5402, MM5405 digital alarm clocks

general description

The MM5402, MM5405 digital alarm clocks are monolithic MOS integrated circuits utilizing N-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. They provide all the logic required to build several types of clocks and timers with up to four display modes (time, seconds, alarm and sleep) to maximize circuit utility, but are specifically intended for clock-radio applications. Both devices will directly-drive 7-segment LED displays in either a 12-hour format (3 1/2 digits) with lead-zero blanking, AM/PM indication and flashing colon, or 24-hour format (4 digits) through hard-wire pin selection; the timekeeping function operates from either a 50 or 60 Hz input, also through pin selection. Outputs consist of display drivers, sleep (e.g., timed radio turn-off), and alarm enable. A power-fail indication mode is provided to inform the user of incorrect time display by flashing all "ON" digits at a 1 Hz rate, and is cancelled by simply resetting time. The device operates over a supply range of 7V—11V which does not require regulation.

The MM5405 is electrically identical to the MM5402, but with mirror-image pin-out to facilitate PC board layout when designing a "module" where the LED display and MOS chip are mounted on the same side; the MM5402 is more suited for "L" shaped module designs (vertical LED display, horizontal component board). Both devices are supplied in a 40-lead dual-in-line package.

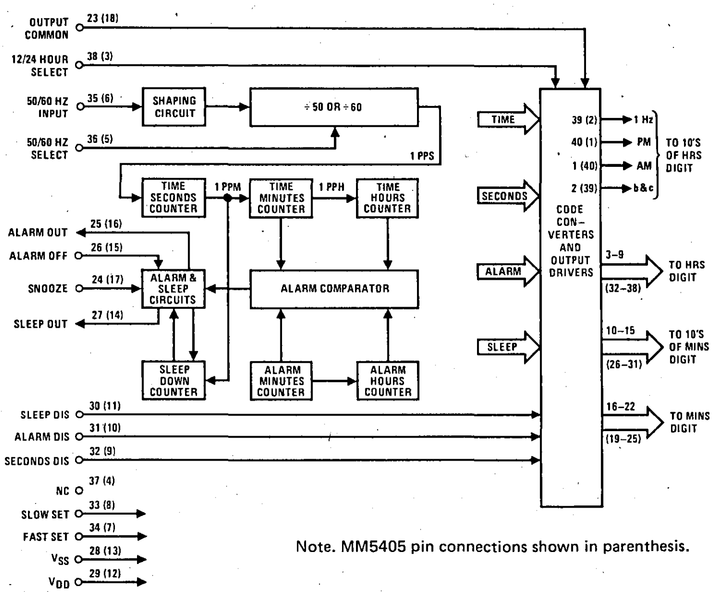
features

- 50 or 60 Hz operation
- Single power supply
- 12 or 24 hour display format
- AM/PM outputs } 12 hour format
- Leading-zero blanking } 12 hour format
- 24-hour alarm setting
- All counters are resettable
- Fast and slow set controls
- Power failure indication
- Elimination of illegal time display at turn "ON"
- Direct interface to LED displays
- 9-minute snooze alarm
- Presettable 59-minute sleep timer
- Available in standard (MM5402) or mirror-image (MM5405) pin-out

applications

- Alarm clocks
- Desk clocks
- Clock radios
- Automobile clocks
- Stopwatches
- Industrial clocks
- Portable clocks
- Photography timers
- Industrial timers
- Appliance timers
- Sequential controllers

block diagram



Note. MM5405 pin connections shown in parenthesis.

FIGURE 1

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} to V_{SS} +12V	Lead Temperature (Soldering, 10 seconds)	300°C
Operating Temperature	−25°C to +70°C	Segment Output Current	Note 1
Storage Temperature	−65°C to +150°C		

electrical characteristics T_A within operating range, V_{DD} = 7V to 11V, V_{SS} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	Output Driving Display	9		11	V
	Functional Clock	7		11	V
Power Supply Current	No Output Loads				
	V_{DD} = 7V			4	mA
	V_{DD} = 11V			5	mA
50/60 Hz Input					
Frequency	V_{DD} = 7V to 11V	dc	50 or 60	10k	Hz
Logical Low Level		V_{SS}	V_{SS}	V_{SS}+0.5	V
Logical High Level		V_{DD}−3	V_{DD}	V_{DD}	V
Input Leakage				100	μA
All Other Input Voltages					
Logical Low Level		V_{SS}	V_{SS}	V_{SS}+0.5	V
Logical High Level	Internal Depletion Load to V_{DD}	V_{DD}−3	V_{DD}	V_{DD}	V
Power Failure Detect Voltage	(V_{DD} Voltage), (Note 2)	1		5	V
Count Operating Voltage		7		11	V
Hold Count Voltage		(Note 2)		11	V
Alarm and Sleep Outputs	V_{DD} = 11V				
Logical High, Source	V_{OH} = V_{SS} + 2	1			μA
Logical Low, Sink	V_{OL} = V_{SS} + 2	5			mA
Output Current Levels	V_{DD} = 9V to 11V				
	Output Common = V_{SS}				
Common Anode	*(Figure 5a)*				
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level, Leakage	V_{OH} = V_{DD}			10	μA
Logical Low Level, Sink	V_{OL} = V_{SS} + 2V	24			mA
1 Hz Display					
Logical High Level, Leakage	V_{OH} = V_{DD}			10	μA
Logical Low Level, Sink	V_{OL} = V_{SS} + 2V	36			mA
All Other Segment Displays					
Logical High Level, Leakage	V_{OH} = V_{DD}			10	μA
Logical Low Level, Sink	V_{OL} = V_{SS} + 2V	12			mA
Output Current Levels	V_{DD} = 9V to 11V			(Note 1)	
	Output Common = V_{SS} + 4				
Common Cathode	*(Figure 5b)*				
10's of Hours (b & c), 10's of Minutes (a & d)					
Logical High Level, Source	V_{OH} = V_{SS} + 1.5V	20			mA
Logical Low Level, Leakage	V_{OL} = V_{SS}			10	μA
1 Hz Display					
Logical High Level, Source	V_{OH} = V_{SS} + 1.5V	30			mA
Logical Low Level, Leakage	V_{OL} = V_{SS}			10	μA
All Other Segment Displays					
Logical High Level, Source	V_{OH} = V_{SS} + 1.5V	10			mA
Logical Low Level, Leakage	V_{OL} = V_{SS}			10	μA

Note 1: Segment output current must be limited to 15 mA maximum by user; power dissipation must be limited to 900 mW at 70°C and 1.2W at 25°C.

Note 2: The power-fail detect voltage is 0.25V or more above the hold count voltage. The power-fail latch trips into power-fail mode at least 0.25V above the voltage at which data stored in the time latch is lost.

Note 3: Power supply voltage should not exceed a maximum voltage of 12V under any circumstances, such as during plug in, power up, display "ON"/"OFF", or power supply ripple. Doing so runs the risk of permanently damaging the device.

functional description

A block diagram of the MM5402, MM5405 digital clock radio circuit is shown in *Figure 1*. The various display setting modes are listed in Table I, and Table II shows the setting control functions. The following description is based on *Figure 1* and refers to both devices as they are electrically identical.

50 or 60 Hz Input: A shaping circuit *(Figure 3)* is provided to square the 50 or 60 Hz input. This circuit allows use of a filtered sinewave input. The circuit is a Schmitt trigger that is designed to provide about 0.8V hysteresis. A simple RC filter such as shown in *Figure 7*, should be used to remove possible line-voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: A programmable prescale counter divides the input line frequency by either 50 or 60 to obtain a 1 Hz time base. This counter is programmed to divide by 60 simply by leaving 50/60 Hz select unconnected; pull-up to V_{DD} is provided by an internal depletion load. Operation at 50 Hz is programmed by connecting 50/60 Hz select to V_{SS}.

Display Mode Select Inputs: In the absence of any of these three inputs, the display drivers present time-of-day information to the appropriate display digits. Internal depletion pull-up devices allow use of simple SPST switches to select the display mode. If more than one mode is selected, the priorities are as noted in Table I. Alternate display modes are selected by applying V_{SS} to the appropriate pin. As shown in *Figure 1* the code converters receive time, seconds, alarm and sleep information from appropriate points in the clock circuitry. The display mode select inputs control the gating of the desired data to the code converter inputs and ultimately (via output drivers) to the display digits.

Time Setting Inputs: Both fast and slow setting inputs are provided. These inputs are applied either singly or in combination to obtain the control functions listed in Table II. Again, internal depletion pull-up devices are provided; application of V_{SS} to these pins affects the control functions. Note that the control functions proper are dependent on the selected display mode. For example, a hold-time control function is obtained by selecting seconds display and actuating the slow set input. As another example, the clock time may be reset to 12:00:00 AM, by selecting seconds display and actuating both slow and fast set inputs.

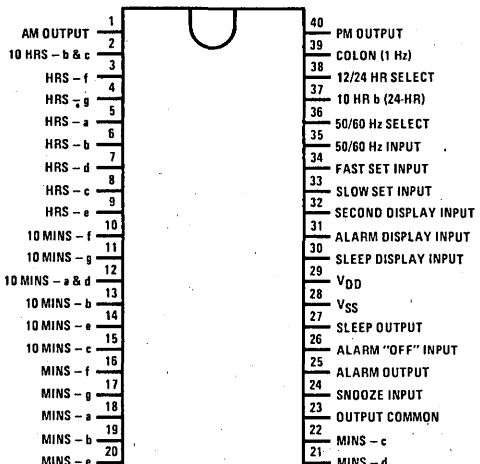
Output Common: All display output drivers are open drain devices with all the sources connected to output common pin. This pin can be used as a common source or a common drain. When used as a common source, this pin is connected to V_{SS} and when used as a common drain, this pin is connected to V_{DD}. This allows the use of either common anode or common cathode LED's for displays. *Figure 5* shows these connections.

12 or 24 Hour Select Input: By leaving this pin unconnected, the outputs for the most-significant display digit (10's of hours) are programmed to provide a 12-hour display format. An internal depletion pull-up device is again provided. Connecting this pin to V_{SS} programs the 24-hour display format. Segment connections for 10's of hours in 24-hour mode are shown in *Figure 6*.

Power Fail Indication: If the power to the integrated circuit drops, indicating a momentary ac power failure and possible loss of clock, all "ON" segments will flash at 1 Hz rate. A fast or slow set input resets an internal power failure latch and returns the display to normal.

connection diagrams (Top Views)

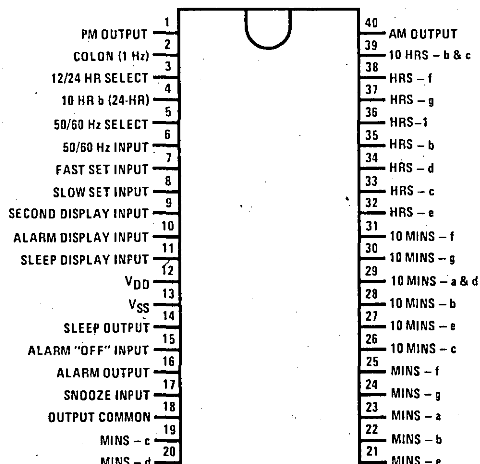
Dual-In-Line Package



Order Number MM5402N
See Package 24

FIGURE 2(a). MM5402

Dual-In-Line Package



Order Number MM5405N
See Package 24

FIGURE 2(b). MM5405 (Mirror-Image Pin-Out)

functional description (Continued)

Alarm Operation and Output: The alarm comparator *(Figure 1)* senses coincidence between the alarm counters (the alarm setting) and the time counters (real time). The comparator output is used to set a latch in the alarm and sleep circuits. The latch output enables the alarm output driver *(Figure 4b)* which is used to control the external alarm sound generator. The alarm latch remains set for 59 minutes, during which the alarm will therefore sound if the latch output is not temporarily inhibited by another latch set by the snooze alarm input or reset by the alarm "OFF" input.

Snooze Alarm Input: Momentarily connecting snooze to V_{SS} inhibits the alarm output for between 8 and 9 minutes, after which the alarm will again be sounded. This input is pulled-up to V_{DD} by an internal depletion device. The snooze alarm feature may be repeatedly used during the 59 minutes in which the alarm latch remains set.

Alarm "OFF" Input: Momentarily connecting alarm "OFF" to V_{SS} resets the alarm latch and thereby silences the alarm. This input is also returned to V_{DD} by an internal depletion device. The momentary alarm "OFF" input also readies the alarm latch for the next comparator output, and the alarm will automatically sound again in 24 hours (or at a new alarm setting). If it is desired to silence the alarm for a day or more, the alarm "OFF" input should remain at V_{SS}.

Sleep Timer and Output: The sleep output can be used to turn "OFF" a radio after a desired time interval of up to 59 minutes. The time interval is chosen by selecting the sleep display mode, (Table I) and setting the desired time interval (Table II). This automatically results in a current sink output which can be used to turn "ON" a radio (or other appliance). When the sleep counter, which counts downwards, reaches 00 minutes, a latch is reset and the sleep output current drive is removed, thereby turning "OFF" the radio. This turn "OFF" may also be manually controlled (at any time in the countdown) by a momentary V_{SS} connection to the Snooze input. The output circuitry is the same as the other outputs *(Figure 4b)*.

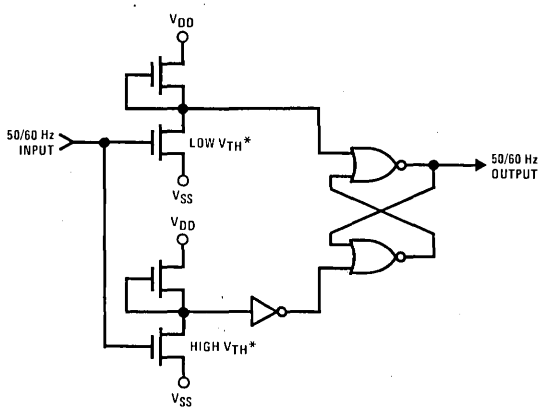


FIGURE 3. 50/60 Hz Input Shaping Circuit

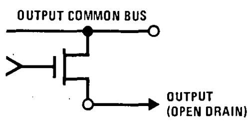


FIGURE 4(a). Segment Outputs

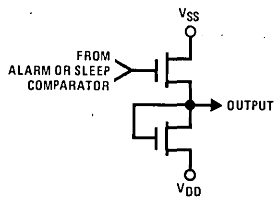


FIGURE 4(b). Alarm and Sleep Outputs

1

functional description (Continued)

TABLE I. MM5402, MM5405 Display Modes

*SELECTED DISPLAY MODE	DIGIT NO. 1	DIGIT NO. 2	DIGIT NO. 3	DIGIT NO. 4
Time Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Seconds Display	Blanked	Minutes	10's of Seconds	Seconds
Alarm Display	10's of Hours & AM/PM	Hours	10's of Minutes	Minutes
Sleep Display	Blanked	Blanked	10's of Minutes	Minutes

* If more than one display mode input is applied, the display priorities are in the order of Sleep (overrides all others), Alarm, Seconds, Time (no other mode selected).

TABLE II. MM5402, MM5405 Setting Control Functions

SELECTED DISPLAY MODE	CONTROL INPUT	CONTROL FUNCTION
*Time	Slow	Minutes Advance at 2 Hz Rate
	Fast	Minutes Advance at 60 Hz Rate
	Both	Minutes Advance at 60 Hz Rate
Alarm	Slow	Alarm Minutes Advance at 2 Hz Rate
	Fast	Alarm Minutes Advance at 60 Hz Rate
	Both	Alarm Resets to 12:00 AM (Midnight) (12-Hour Format)
	Both	Alarm Resets to 00:00 (24-Hour Format)
Seconds	Slow	Input to Entire Time Counter is Inhibited (Hold)
	Fast	Seconds and 10's of Seconds Reset to Zero Without a Carry to Minutes
	Both	Time Resets to 12:00:00 AM (Midnight) (12-Hour Format)
	Both	Time Resets to 00:00:00 (24-Hour Format)
Sleep	Slow	Subtracts Count at 2 Hz
	Fast	Subtracts Count at 60 Hz
	Both	Subtracts Count at 60 Hz

*When setting time sleep minutes will decrement at rate of time counter, until the sleep counter reaches 00 minutes (sleep counter will not recycle).

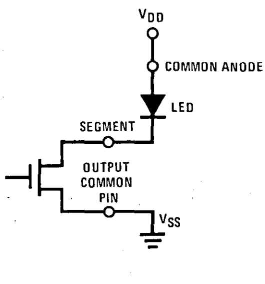


FIGURE 5(a). Common Anode Application

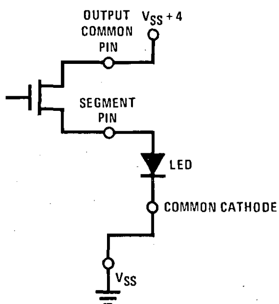


FIGURE 5(b). Common Cathode Application

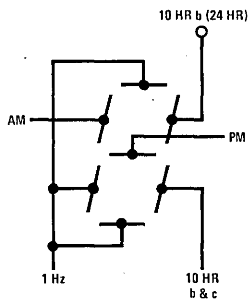


FIGURE 6. 24-Hour Operation: 10's of Hours Digit Connections

typical applications

Figure 7 is a schematic diagram of a general purpose alarm clock circuit (12-hour mode) using the MM5402 or MM5405 and a 3 1/2-digit LED display.

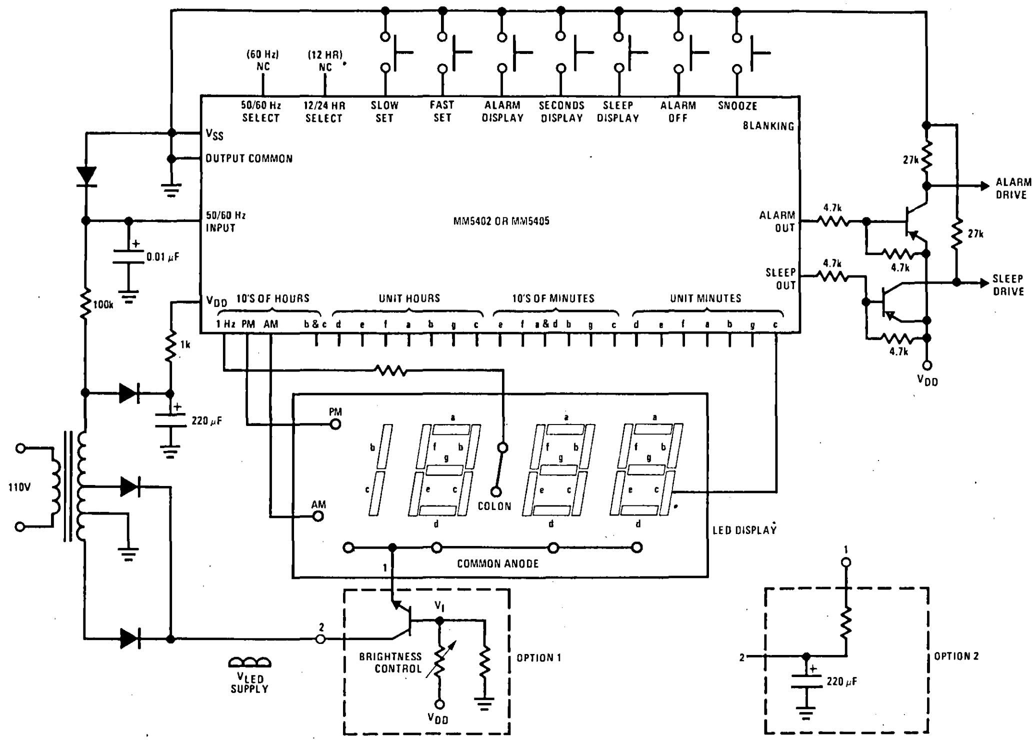


FIGURE 7

USING NATIONAL CLOCK INTEGRATED CIRCUITS IN TIMER APPLICATIONS

INTRODUCTION

The following is a description of a technique which allows the use of the National MM5309, MM5311, MM5312 and MM5315 clock integrated circuits as timers in industrial and consumer applications. What will be presented is the basic technique along with some simple circuitry and applications.

BASIC TECHNIQUE

When first approaching the problem of using clock chips for timers, the most obvious technique is to attempt to compare the display data with preset BCD numbers. Because of the multiplexing and number of data bits this technique, while possible, is unwieldy and requires a large number of components.

An easier method is to use one or more demultiplexed BCD lines as control waveforms whose edges determine timer data. In *Figure 1* we examine the 1-bit of the BCD data of the units second time.

From this waveform we observe a one second wide pulse every two seconds. If we look at the 4-bit of the 10 minutes digit we find a pulse which is 20 minutes wide and occurs once each hour.

Figure 3 is a chart showing the various pulses and their widths for all digits and the useful BCD lines.

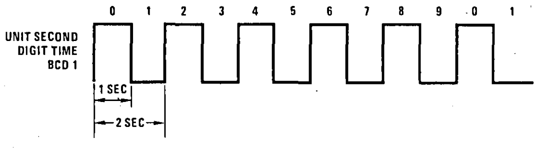


FIGURE 1. 1 Second Pulse Every 2 Seconds

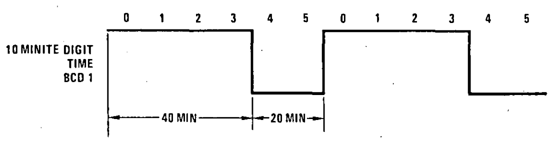


FIGURE 2. 20 Minute Pulse Every Hour

BCD	PULSE RATE	PULSE WIDTH	BCD	PULSE RATE	PULSE WIDTH
	1 Sec Digit			**10 Sec Digit**	
1	1 every 2 sec	1 sec*	1	1 every 20 sec	10 sec*
2			2	1 every min	20 sec
4	1 every 10 sec	4 sec	4	1 every min	20 sec
8	1 every 10 sec	2 sec	8		
	1 Min Digit			**10 Min Digit**	
1	1 every 2 min	1 min*	1	1 every 20 min	10 min*
2			2	1 every hr	20 min
4	1 every 10 min	4 min	4	1 every hr	20 min
8	1 every 10 min	2 min	8		
	Units Hrs Digit (12 Hr Mode)			**Units Hrs Digit (24 Hr Mode)**	
1	1 every 2 hrs	1 hr*	1	1 every 2 hrs	1 hr*
2			2		
4	1 every 12 hrs	4 hrs	4		
8	1 every 12 hrs	4 hrs	8		
	10 Hrs Digit (12 Hr Mode)			**10 Hrs Digit (24 Hr Mode)**	
1			1	1 every 24 hrs	10 hrs
2	1 every 12 hrs	9 hrs	2	1 every 24 hrs	4 hrs
4	1 every 12 hrs	9 hrs			
8	1 every 12 hrs	9 hrs			

*Square waves

FIGURE 3

SIMPLE DEMULTIPLEXING

In the simple case where, for example, a four hour wide pulse each day is desired, perhaps to turn on lights in the evening, a simple demultiplexing scheme using one diode is shown in *Figure 4.* When power is applied, the internal multiplex circuitry will strobe each digit until the digit with the diode connected is accessed. This digit will sink the multiplex charging current and stop the multiplex scanning. Thus, the BCD outputs now present the data from the selected digit. The waveforms as previously discussed are presented at the BCD lines. Note that these pulses are negative true for all BCD outputs.

An advantage of this type of timer over mechanical types is the elimination of line power drop outs. The circuit shown in *Figure 5* will maintain timing to within a few percent during periods of power line failure, but automatically return to the 60 Hz line for timing as soon as power is restored.

MORE COMPLEX APPLICATIONS

Where it is desired to maintain the display, or in more complex timing of the "10 seconds every two hours" variety, external demultiplexing shown in *Figure 6* can be used. In this figure the BCD lines are demultiplexed with MM74C74 flip-flops. Examining the waveforms of these circuits we see two edges which allow the 10 second each two hours timing. These are differentiated by the NAND and INVERTERS and the first edge sets and the second resets the S-R flip-flop. The output of the flip-flop is ten seconds wide every two hours. By examining the edges of the *Figure 3* entries any combination of timings can be obtained with the circuit of *Figure 6.*

LOW FREQUENCY WAVEFORM GENERATION

The asterisked BCD lines in *Figure 3* are those waveforms which are symmetric. By the use of the simple diode demultiplexing scheme previously discussed we

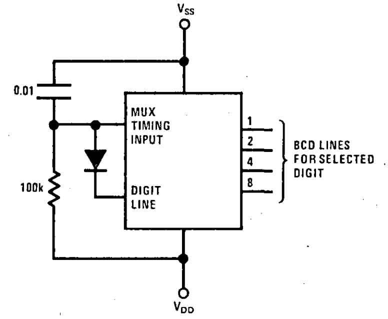


FIGURE 4

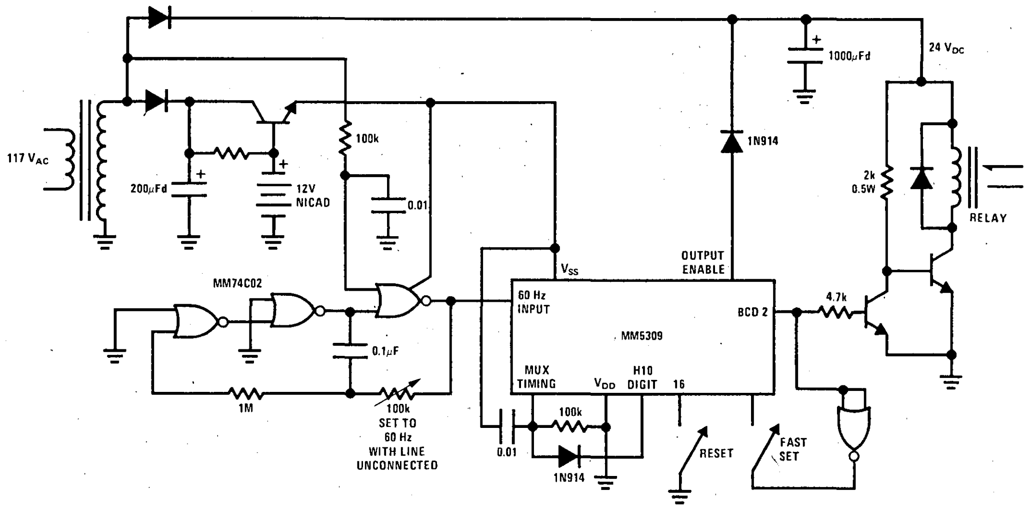


FIGURE 5. Fail-Safe Automatic Lights Timer. Four Hours Each 24 Hours

easily obtain square waves with periods of two seconds, two minutes, twenty minutes and two hours. In other cases, where the waveforms are asymmetric, a simple flip-flop can square, while dividing by two, these waveforms producing other low frequency square waves as long as one per two days.

SUMMARY

We have shown some simple low cost timer and waveform generating examples using National clock integrated circuits. Because of the vast number of timing applications possible, this can in no way be looked at as the limit of clock-timer circuits. Use of the Reset on the MM5309 and MM5315 or the use of clocks in conjunction with programmable counters such as the MM74C161 allows other possibilities to meet specific applications. Also the clock chips themselves can run on frequencies other than 50 or 60 Hz (actually from dc to 10 kHz) which can allow scaling of the waveforms presented in *Figure 3* to different timing rates.

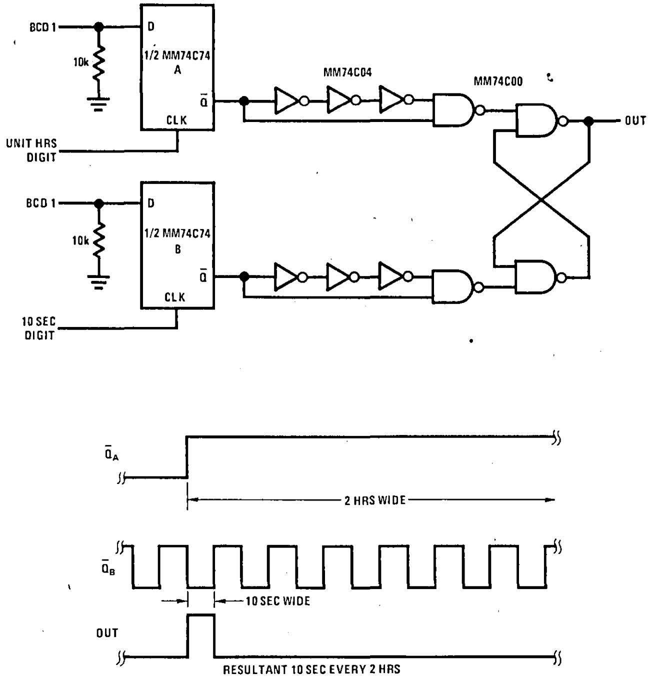


FIGURE 6. More Universal Demultiplexing Technique

SECTION 2
COUNTERS/TIMERS

Counters/Timers

MM5307 baud rate generator/programmable divider

general description

The National Semiconductor MM5307 baud rate generator/programmable divider is a MOS/LSI P-channel enhancement mode device. A master clock for the device is generated either externally or by an on-chip crystal oscillator (Note 4). An internal ROM controls a divider circuit which produces the output frequency. Logic levels on the four control pins select between sixteen output frequencies. The frequencies are chosen from the following possible divisors: 2N, for $3 \leq N \leq 2048$; 2N + 1 and 2N + 0.5 for $4 \leq N \leq 2048$. Also one of the sixteen frequencies may be gated from the external frequency input. The MM5307AA is supplied with the divisors shown in Table I.

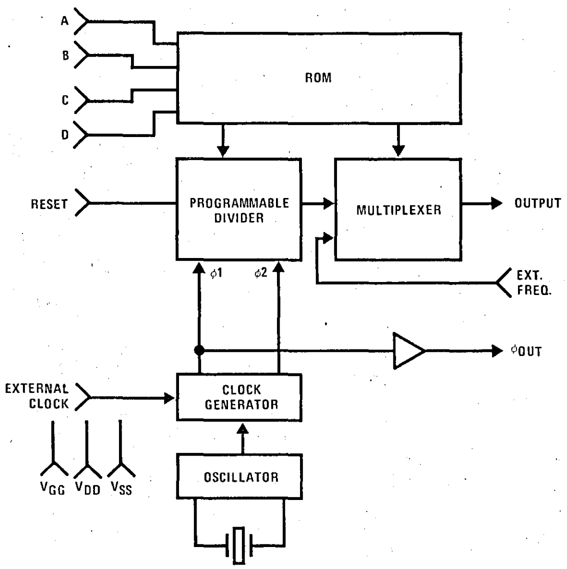
features

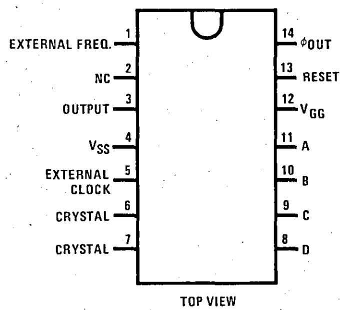
- On-chip crystal oscillator
- Choice of 16 output frequencies from 1 crystal
- External frequency input pin
- Internal ROM allows generation of other frequencies on order
- Bipolar compatibility
- 0.01% accuracy (typ) exclusive of crystal
- 1 MHz master clock frequency

applications

- DAR/T clocks
- System clocks
- Electrically programmable counters

schematic and connection diagrams





Order Number MM5307N
See Package 18

absolute maximum ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3V to V_{SS} – 20V
Power Dissipation	700 mW
Storage Temperature Range	–65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating range, V_{SS} = 5V ±5%, V_{GG} = –12V ±5%, unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	All Inputs (Except Crystal Pins)					
V_{IH}	Logical High Level		V_{SS}–1.5		V_{SS}+0.3	V
V_{IL}	Logical Low Level		V_{SS}–18		V_{SS}–4.2	V
	Leakage	V_{IN} = –10V, T_A = 25°C, All Other Pins GND			0.5	μA
	Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND, (Note 1)			7.0	pF
	External Clock Duty Cycle		40%		60%	
	Capacitance Measured Across Crystal Pins	f = 1 MHz, (Note 3)			5.0	pF
	Output Levels					
V_{OH}	Logical High Level	I_{SOURCE} = –0.5 mA	V_{SS}–2.6	V_{SS}		V
V_{OL}	Logical Low Level	I_{SINK} = 1.6 mA			V_{SS}–4.6	V
I_{GG}	Power Supply Current	f = 1 MHz			35	mA

ac electrical characteristics

T_A within operating range V_{SS} = 5V ±5%, V_{GG} = –12V ±5%, unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Master Frequency		0.01		1.0	MHz
t_A	Access Time	C_L = 50 pF, (Note 2)			16	μs
t_{RD}	Reset Delay Time	f = Master Clock Frequency			500 + 4/f	ns
R_{PW}	Reset Pulse Width		500 + 4/f			ns
t_{OD}	Output Delay From Reset				500 + 4/f	ns
	Output Duty Cycle = 0.5T ± 1/f	T = Output Period f = Master Frequency	0.5T–1/f		0.5T+1/f	

Note 1: Capacitance is guaranteed by periodic measurement.

Note 2: Access time is defined as the time from a change in control inputs (A, B, C, D) to a stable output frequency. Access time is a function of frequency. The following formula may be used to calculate maximum access time for any master frequency: T_A = 2.8μs + 1/f x 13, f is in MHz.

Note 3: The MM5307 is designed to operate with a 1 MHz parallel resonant crystal. When ordering the crystal a value of load capacitance (C_L) must be specified. This is the capacitance "seen" by the crystal when it is operating in the circuit. The value of C_L should match the capacitance measured at the crystal frequency across the crystal input pins on the MM5307. Any mismatch will be reflected as a very small error in the operating frequency. To achieve maximum accuracy, it may be necessary to add a small trimmer capacitor across the terminals.

Note 4: If the crystal oscillator is used Pin 5 (external clock) is connected to V_{SS}. If an external clock is used Pin 7 is connected to V_{SS}.

control table

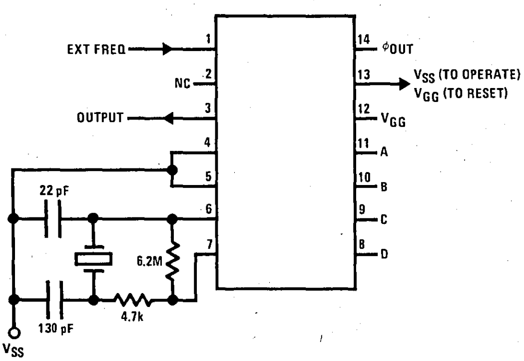
Input Freq: 921.6 kHz Master Clock

CONTROL PINS				NOMINAL BAUD RATES (OUTPUT FREQUENCY/16)			DIVISOR FOR AA
A	B	C	D	AA	AB	FAG	
0	0	0	1	50	50	50	1152
0	0	1	0	75	200	75	768
0	0	1	1	110	110	110	524
0	1	0	0	134.5	134.5	134.5	428.5
0	1	0	1	150	150	150	384
0	1	1	0	300	300	300	192
0	1	1	1	600	600	600	96
1	0	0	0	900	900	1050	64
1	0	0	1	1200	1200	1200	48
1	0	1	0	1800	1800	45.5	32
1	0	1	1	2400	2400	2400	24
1	1	0	0	3600	3600	56.9	16
1	1	0	1	4800	4800	4800	12
1	1	1	0	7200	75	66.7	8
1	1	1	1	9600	9600	9600	6
0	0	0	0	EXTERNAL FREQ			

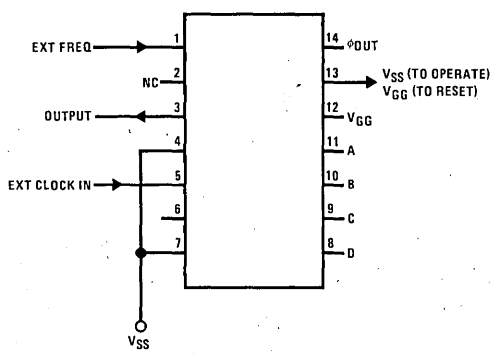
Positive Logic: $1 = V_H$
$0 \equiv V_L$

typical applications

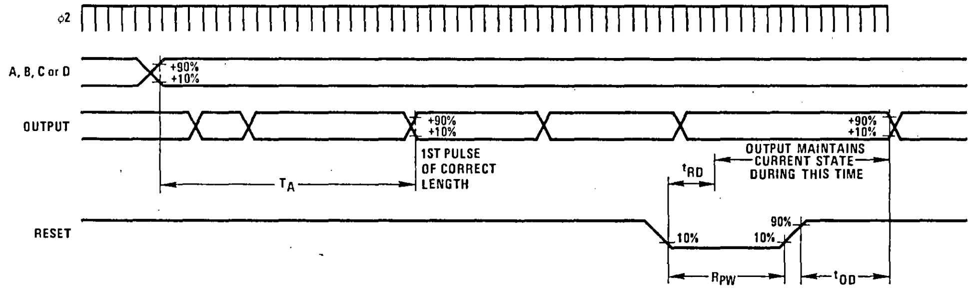
Internal Oscillator



External Clock



timing diagram

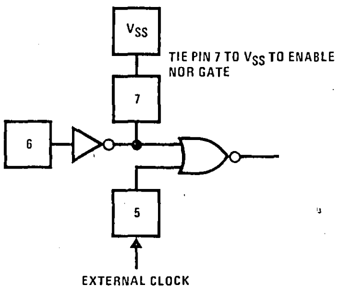


application hints

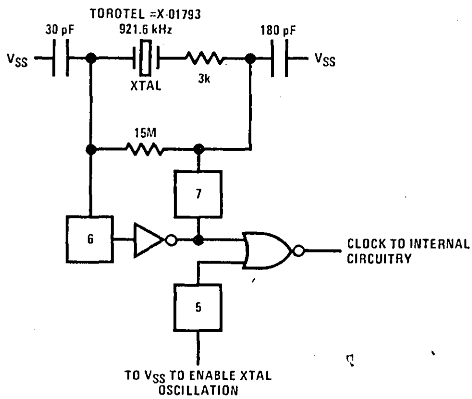
APPLICATION NOTES

The external clock is brought in on pin 5 and pin 7 is tied to V_{SS} to enable the external clock input. Pin 6 can be left open.

1) To use the MM5307 with an external clock, hook it up as follows:



2) To use a crystal directly:



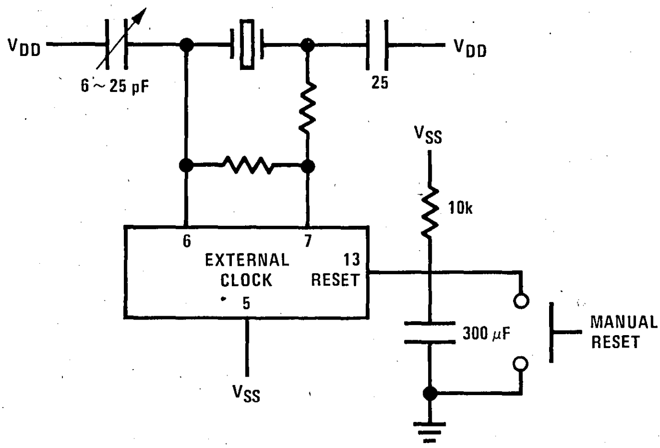
3) Reset (pin 13) must be at V_{SS} to operate. It may be necessary to take this to GND or V_{GG} to reset the ROM select circuit. An option is to tie ϕ out (pin 14) to external Freq In (pin 1), if not otherwise used.

4) An interesting application might use two MM5307's in series to generate additional frequencies, i.e., with one programmed from the 921.6 kHz to 800 Hz out, a second could divide that by 16 to give a 50 Hz crystal controlled signal.

5) MM307AA divisors are on the data sheet. AB divisors are the same as the AA except: 1) Code 0010 is divided by 288 → 32 kHz out, 200 baud; 2) Code 1110 is divided by 768 → 1.2 kHz, 75 baud.

The MM5307 does not always generate an output when the power is up, even though the oscillator seems to be operating properly. In order to eliminate this problem, it is necessary to reset the chip at power "ON". This can be done manually, with a reset signal by a host system, or automatically by using R/C timing elements. The reset is done internally, when program inputs change. When using an R/C combination for auto resetting, the time constant must be several times larger than that of the power supply. For example, most lab power supplies take at least 0.5 sec for the voltage to reach 90% of full level. A 10 kΩ resistor and 300 μF capacitor combination should be adequate for most applications.

application hints (Continued)



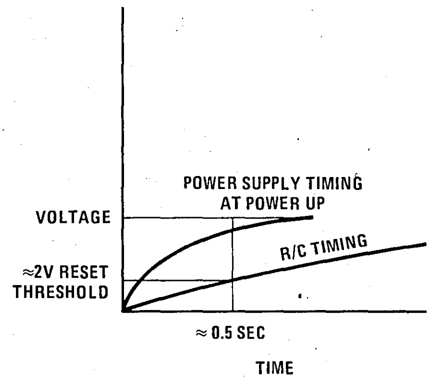


FIGURE 1

MM5369 17-stage programmable oscillator/divider

general description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise 60 Hz reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The programmable number the circuit will divide by can vary from 10000 to 98000. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the crystal frequency for tuning purposes and the 17th stage 60 Hz output. Mask options are available for use with commonly available, low cost, high frequency crystals. Therefore, this design can be "customized" by special order to design specific programmable divider limits whereby the maximum divide-by can be 98,000 and the minimum divide-by can be 10,000. The MM5369 is available in an 8-lead dual-in-line epoxy package.

features

- Crystal Oscillator
- Two buffered outputs
  - Output 1 cyrstal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10)
- Wide supply range 3–15V
- Low Power
- Fully static operation
- 8 lead dual-in-line package
- Low current

Standard MM5369N Only

- 3.58 MHz (color TV oscillator) input frequency
- 60 Hz output frequency

connection diagram

Dual-In-Line Package

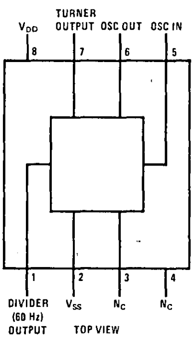


FIGURE 1.

Order Number MM5369N
See Package 17

block diagram

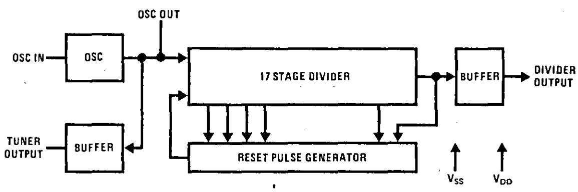


FIGURE 2.

absolute maximum ratings

Voltage at Any Pin	$-0.3V$ to V_{CC} +0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	16V
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = GND, $3V \leq V_{DD} \leq 15V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 15V			10	µA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V	DC		4.5	MHz
	V_{DD} = 6V	DC		2	MHz
Output Current Levels	V_{DD} = 10V V_{OUT} = 5V				
Logical "1" Source		500			µA
Logical "0" Sink		500			µA
Output Voltage Levels	V_{DD} = 10V I_O = 10 µA				
Logical "1"		9.0			V
Logical "0"				1.0	V

functional description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2*.

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

A pulse is generated when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter, thus varying the modulus of the counter from 10000 to 98000. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs. A typical application of the MM5369 is shown in *Figure 5*.

functional description (cont.)

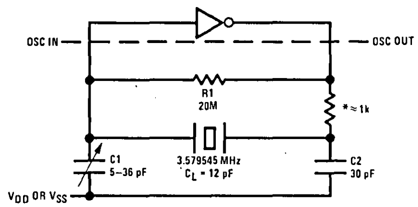


FIGURE 3. Crystal Oscillator Network

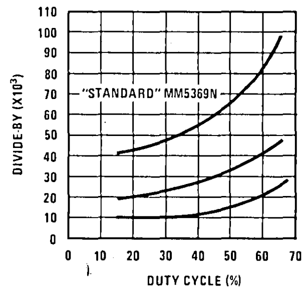


FIGURE 4. Plot of Divide-By Vs Duty Cycle

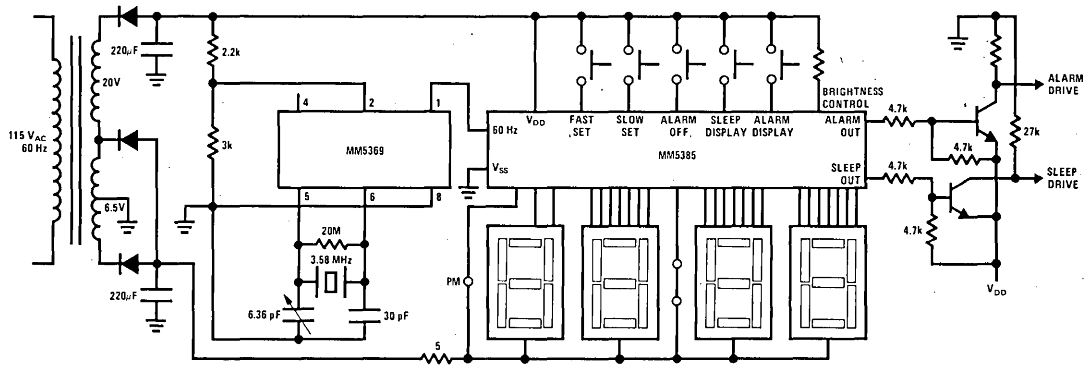


FIGURE 5. Clock Radio Circuit with Battery Back-Up

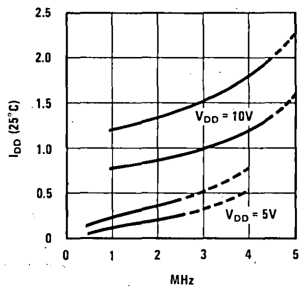


FIGURE 6. Typical Current Drain Vs Oscillator Frequency

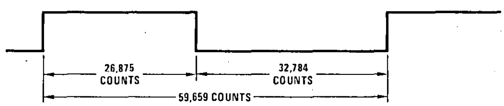


FIGURE 7. Output Waveform for Standard MM5369

*To be selected based on xtal used

Counters/Timers

For additional application information, see AN-168 and AN-169 at the end of this section.

MM5865 universal timer general description

The MM5865 Universal Timer is a monolithic MOS integrated circuit utilizing P-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. The chip contains all the logic required to control the two 4-digit counters, blank leading zeros, compare the two counters and to cascade with another MM5865. Input pins start, stop, reset and set the counters, determine which of the 7 functions is performed, the resolution of the display (0.01 sec, 0.1 sec, 1 sec, or external clock) and what modulo the counters divide by. Outputs include the comparator output, multiplexed BCD outputs and digit enables. The BCD outputs interface directly with MM14511, a BCD to 7-segment decoder, which interfaces with a LED display. The digit enable outputs of 2 cascaded MM5865's interface directly with a DM8863 LED 8-digit driver. A DS8877 or DS75492 Hex Digit Driver may be used with a single MM5865. The digit enable outputs interface directly with a DM8863, a LED digit driver. The 7 functions include start-stop with total elapsed time, start-stop with accumulative event time, split, sequential with total elapsed time, rally with total elapsed time, program up count and program down count. The circuit uses a 32.8 kHz crystal or an external clock and is packaged in a 40-lead dual-in-line package.

applications

- Stop watch
- Kitchen timer
- Oven timer
- Event timer/counter
- Rally timer
- Navigational timer
- Industrial timer/counter

features

- Function 1: Standard Start-Stop with total elapsed time memory
- Function 2: Standard Start-Stop with total accumulative event time
- Function 3: Sequential with total elapsed time memory
- Function 4: Standard split
- Function 5: Rally with total elapsed time memory
- Function 6: Programmable up count. Repeatable upon command
- Function 7: Programmable down count
- Comparator output
- Crystal controlled oscillator (32.8 kHz)
- External clock input (option)
- Provides external clock
- Select resolution
- Select count up or down
- Select modulo 6 or 10 for digits 2, 3 and 4
- Blanking between digits
- Leading-zero blanking
- Multiplex rate output
- External multiplex rate input (option)
- Can be cascaded
- Waiting state indicator
- Simple interface to LED display
- Elimination of illegal time display at turn-on
- Wide power supply range 7V–20V

block and connection diagrams

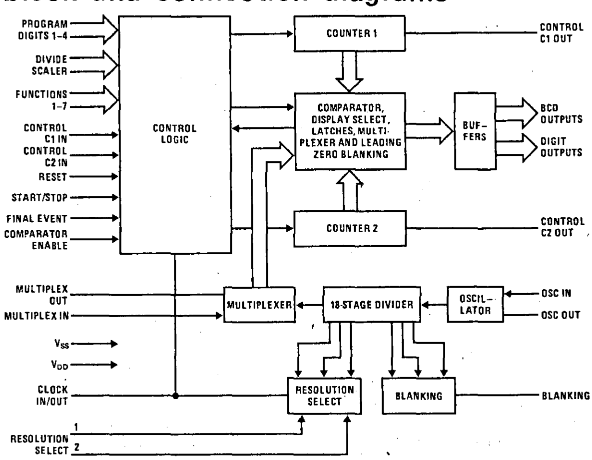
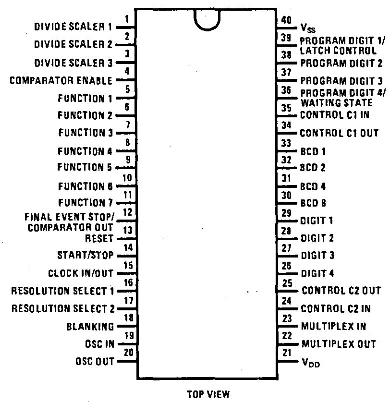


FIGURE 1.

Dual-In-Line Package



Order Number MM5865N
See Package 24

FIGURE 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 25V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, $7V \le V_{SS} \le 20V$, V_{DD} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD} Power Supply Current			7	15	mA
Input Frequency at OSC IN	$V_{SS} \ge 10V$	dc	32.8	80	kHz
Multiplex Frequency	$V_{SS} \ge 10V$	dc	0.4	80	kHz
Blanking Frequency	$V_{SS} \ge 10V$	dc	0.8	10	kHz
Clock Frequency	V_{SS} = 7V	dc	0.1	10	kHz
	V_{SS} = 10V	dc		100	kHz
Input Levels					
Input Logic Low	Internal Resistor	V_{DD}		V_{DD}+1	V
Input Logic High	~100k to V_{DD}	V_{SS}− 1		V_{SS}	V
OUTPUT CURRENTS					
Digit and BCD Outputs	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ −2V	1			mA
Sink Current	$V_{OUT} = V_{SS}$ − 6.3V	1			μA
Blanking Output	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ − 2V	1			mA
Sink Current	$V_{OUT} = V_{SS}$ − 6.3V	1			μA
Multiplex Output	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ − 2.5V	500			μA
Sink Current	$V_{OUT} = V_{SS}$ − 6.3V	8			μA
Clock Output	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ − 4V	10			μA
Sink Current	$V_{OUT} = V_{SS}$ − 6.3V	5			μA
Control C1, C2 Outputs	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ − 2.5V	500			μA
Control C1, C2 Inputs	V_{SS} = 7V				
Sink Current	$V_{IN} = V_{SS}$ − 6.3V	8			μA
Comparator Output	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ − 2V	1			mA
Sink Current	$V_{OUT} = V_{SS}$ − 6.3V	1			μA
Waiting State Indicator	V_{SS} = 7V				
Source Current	$V_{OUT} = V_{SS}$ − 2V	1			mA
Sink Current	$V_{OUT} = V_{SS}$ − 6.3V	1			μA

functional description

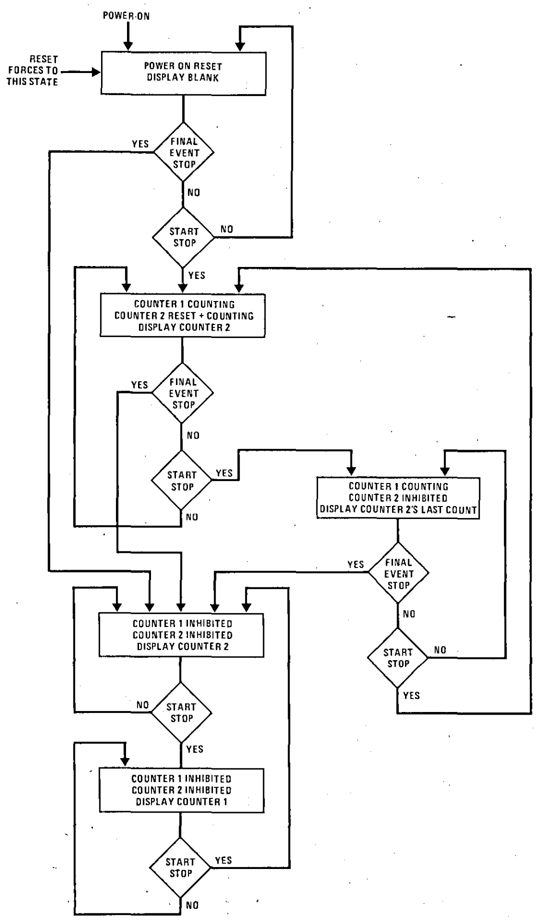
A block diagram of the MM5865 Universal Timer is shown in *Figure 1.* A connection diagram is shown in *Figure 2.* Unless otherwise indicated, the following discussions are based on *Figure 1.*

Function 1

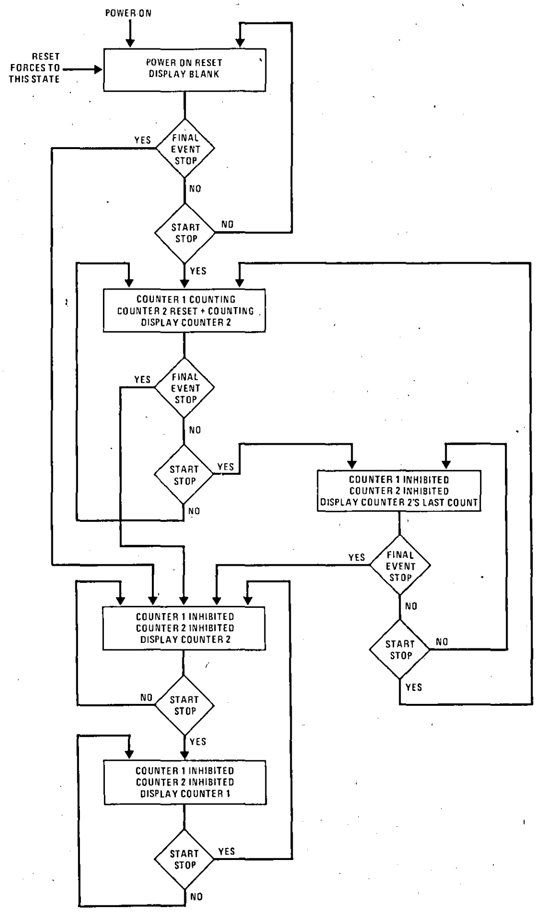
In Function 1, counters 1 and 2 count up beginning with a transition on the Start-Stop pin from V_{DD} to V_{SS}. Counter 2 is shown counting. A second transition from V_{DD} to V_{SS} on the Start-Stop pin inhibits the clock pulses to counter 2, stores and displays the contents of counter 2. Counter 1 continues to count. The third transition from V_{DD} to V_{SS} on the Start-Stop pin resets counter 2, enables clock pulses to counter 2 and displays counter 2 counting. Subsequent Start-Stop transitions repeat this sequence, all this time counter 1 continues to count. At the conclusion of the last event to be timed, a Final Event Stop transition from V_{DD} to V_{SS} inhibits the clock to both counters and displays counter 2. A Start-Stop transition from V_{DD} to V_{SS} switches the display from counter 2 to counter 1. Repetitive Start-Stop transitions switch the display between counter 2 and counter 1.

Function 2

In Function 2, counter 1 and 2 count up beginning with a transition on the Start-Stop pin. Counter 2 is displayed counting. A second transition on the Start-Stop pin inhibits the clock pulses to both counter 1 and counter 2, stores and displays the contents of counter 2. The third transition on the Start-Stop pin resets counter 2, enables the clock to both counters and displays counter 2 counting. Subsequent Start-Stop transitions repeat this sequence. At the conclusion of the last event to be timed, a Final Event Stop transition inhibits the clock to both counters and displays counter 2. A Start-Stop transition switches the display from counter 2 to counter 1. Repetitive Start-Stop transitions switch the display between counter 2 and counter 1.



Flow Chart for Function 1



Flow Chart for Function 2

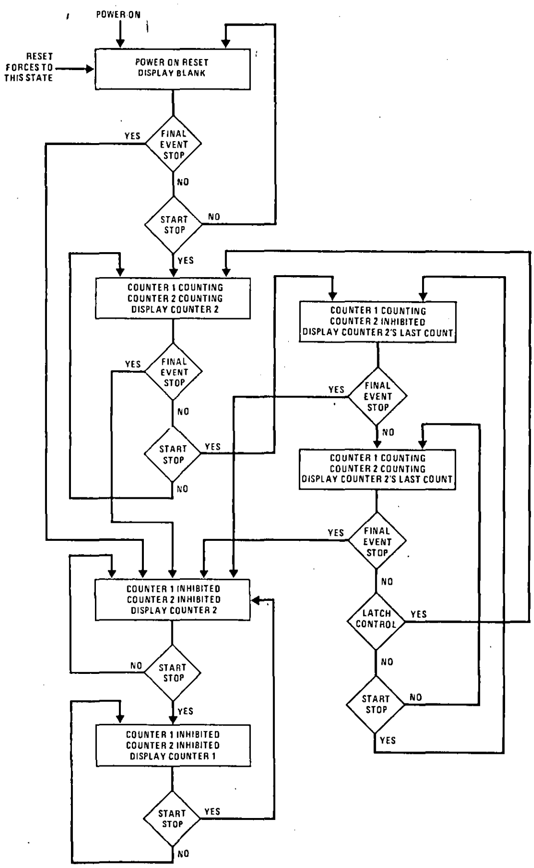
functional description (con't)

Function 3

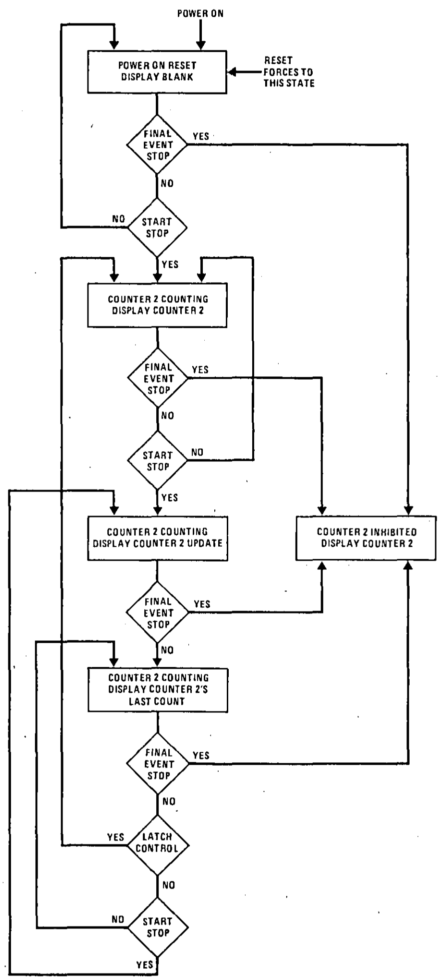
In Function 3, counter 1 and 2 count up beginning with a transition on the Start-Stop pin. Counter 2 is displayed counting. A second transition on the Start-Stop pin stores and displays the contents of counter 2, resets counter 2, and initiates a new up-count in counter 2; however, the new up-count is not displayed. Counter 1 continues to count. A transition on the Latch Control pin will display counter 2 counting until another transition on the Start-Stop pin. A Final Event Stop transition inhibits the clock pulses to both counters 1 and 2 and displays the contents of counter 2. A Start-Stop transition after the Final Event transition switches the display from counter 2 to counter 1. Repetitive Start-Stop transitions switch the display between counter 2 and counter 1.

Function 4

In Function 4, counter 2 counts up beginning with a transition on the Start-Stop pin. Counter 2 is displayed counting. A second transition on the Start-Stop pin stores and displays the contents of counter 2. Subsequent Start-Stop transitions update the display of counter 2. A transition on the Latch Control pin will display counter 2 counting until a transition on the Start-Stop pin. A Final Event Stop transition inhibits the clock pulses to counter 2 and displays the contents of counter 2.



Flow Chart for Function 3



Flow Chart for Function 4

functional description (con't)

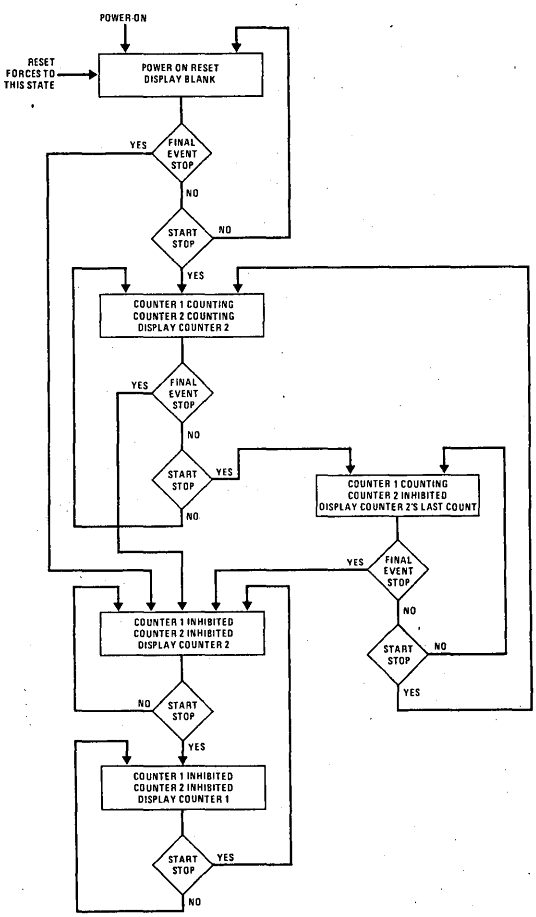
Function 5

In Function 5, counter 1 and 2 count up beginning with a transition on the Start-Stop pin. Counter 2 is displayed counting. A second transition on the Start-Stop pin inhibits the clock pulses to counter 2, and the contents of counter 2 are displayed. Counter 1 continues counting. The third Start-Stop transition enables the clock pulses to counter 2 and counter 2 is displayed counting. Subsequent Start-Stop transitions repeat this sequence, all the time counter 1 continues counting. At the conclusion of the last event to be timed, a Final Event Stop inhibits the clock pulses to both counters 1 and 2, and displays counter 2. A Start-Stop transition switches the display from counter 2 to counter 1. Repetitive Start-Stop transitions switch the display between counter 2 and counter 1.

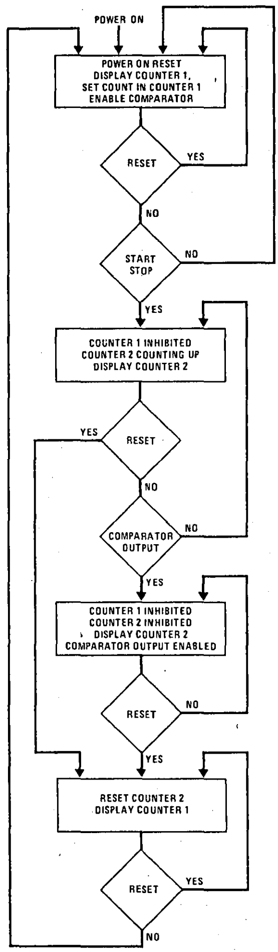
Function 6

In Function 6, counter 1 is displayed at power-on or reset. Counter 1 is set to a specific count by Program Digit 1–4 pins. Then the comparator is enabled. Counter 2 is displayed counting up beginning with a transition on the Start-Stop pin. When counter 2 is coincident with counter 1, the clock pulses to counter 2 are inhibited, the contents of counter 2 are displayed and the Comparator Output is enabled. Upon the transition of Reset, counter 1 is again displayed with the time that was set, and the Comparator Output is disabled. Counter 1 can be reprogrammed by the Program Digit 1–4 pins if desired. A Start-Stop transition repeats the sequence.

If the Comparator Output pin is connected to the Reset pin, Automatic Reset will occur; however, this connection must be broken during digit programming.



Flow Chart for Function 5

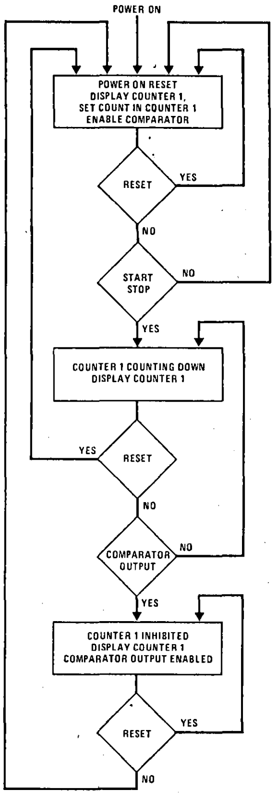


Flow Chart for Function 6

functional description (con't)

Function 7

In Function 7, counter 1 is displayed all the time. Counter 1 is set to a specific count by Program Digit 1–4 pins. Then the comparator and Control C1 In are enabled. Pin 4 and pin 35 must be floating or connected to V_{DD} during digit programming. Counter 1 counts down from the set count beginning with a transition on the Start-Stop pin. When counter 1 counts down to zero, the clock pulses to counter 1 are inhibited and the comparator Output is enabled. This is not repeatable without setting a new count into counter 1. The comparator and Control C1 In must be inhibited and a reset pulse must occur before the new count may be entered.



Flow Chart for Function 7

Reset

This input will reset all logic and counters in Functions 1–5 and Function 7. In Function 6, Reset will reset logic but not counter 1. Reset is internally pulled to V_{DD}, or a logic zero. For a reset to occur, the Reset pin must be held to V_{SS}, a logic one.

Start-Stop

This input is used to control the counters. How it affects the counters is explained in each function. For Start-Stop to affect the counters, it must be held to V_{SS}, a logic one. Logic zero results when the pin is tied to V_{DD} or left floating (internal pull-up to V_{DD}).

Final Event Stop/Comparator Output

This pin is used to indicate to the circuit that no more events will be timed or counted. Final Event Stop affects the circuit when it is held to V_{SS}. There is an internal pull-up to V_{DD}. This pin is also an output pin, V_{SS} indicates comparison between the two counters.

Divide Scale Inputs

These three inputs are used to determine whether the counters will count in Modulo 6 or Modulo 10. Table I shows the code for which digit will count in Modulo 6 or Modulo 10. A logic one is when the pin is held to V_{SS}. When the pin is tied to V_{DD} or left floating (internal pull-up to V_{DD}), a logic zero results.

TABLE I. Divide Scaler Code

DIVIDE SCALER			COUNTER 1				COUNTER 2			
1	2	3	D4	D3	D2	D1	D4	D3	D2	D1
0	0	0	10	10	10	10	10	10	10	10
1	0	0	6	10	10	10	6	10	10	10
0	1	0	10	6	10	10	10	6	10	10
1	1	0	10	10	6	10	10	10	6	10
0	0	1	10	10	10	10	10	10	10	10
1	0	1	10	10	10	10	6	10	10	10
0	1	1	10	10	10	10	10	6	10	10
1	1	1	10	10	10	10	10	10	6	10

Comparator Enable

This input enables the comparator. To enable the comparator, the pin is held to V_{SS} or logic one. To disable the comparator, the pin is tied to V_{DD} or left floating (internal pull-up to V_{DD}).

Resolution Select Inputs

These two inputs are used to select the frequency of the clock pulses to the counters, Table II shows the code for each frequency. A logic one is when the pin is held to V_{SS}. A logic zero results when the pin is tied to V_{DD} or left floating (internal pull-up to V_{DD}).

TABLE II. Resolution Select Code

RESOLUTION SELECT		FREQUENCY OF CLOCK TO COUNTERS	DISPLAY RESOLUTION
1	2		
0	0	100 Hz	0.01 sec
0	1	10 Hz	0.1 sec
1	0	1 Hz	1 sec
1	1	External	

functional description (con't)

Clock In/Out

This pin is either an input or output depending on the code at the Resolution Select inputs. If the pin is used as an output pin, it will output the clock frequency the Resolution Select inputs have selected. When used as an input, an external clock is used to clock the counters.

Blanking Output

This output is used to blank the display at the beginning and end of each digit time to allow for internal delay between two cascaded chips, see *Figure 3.* The display is blanked when the Blanking Output is at V_{DD}.

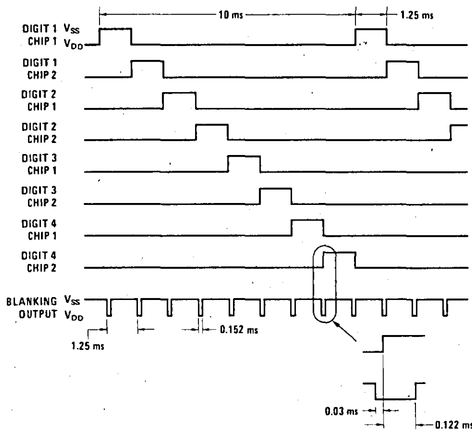


FIGURE 3. Blanking Output

Oscillator In and Out

A quartz crystal, resonant at 32.8 kHz, two capacitors and one resistor, together with the internal MOS circuits form a crystal controlled oscillator as shown in *Figure 4.* Varying one of the capacitors allows precise frequency settings. For test purposes, OSC IN is the input and OSC OUT is the output of an inverting amplifier.

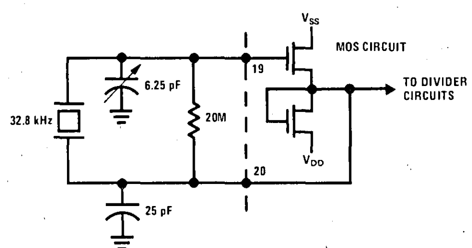


FIGURE 4. Crystal Oscillator

Multiplex Input and Output

The Multiplex Input pin allows an external multiplex rate to be used in the chip. The multiplex rate inside the chip is one fourth the Multiplex Input and Multiplex Output rate. When using the Multiplex Input pin, the Multiplex Output pin must be tied to V_{SS}. The Multiplex Output pin is four times the internal multiplex rate. To use the Multiplex Output pin, the Multiplex Input pin must be tied to V_{DD}. The Multiplex Input must be used if the oscillator pins are not used. If the Multiplex Input pin is used, OSC IN, OSC OUT and the blanking output are not used.

Control C1, C2 In and Control C1, C2 Out

These four input pins are used to cascade two chips together. When the Control C1 In pin is floating (internal pull-up to V_{DD}) or tied to V_{DD}, the clock pulses to counter 1 are inhibited. When Control C1 In is at V_{SS}, counter 1 is enabled. Control C1 Out is at V_{SS} when counter 1 is at it s maximum count, and it is floating at all other times. The Control C1 In pin must be floating (or connected to V_{DD}) while digit programming in Function 7. Control C2 pins operate on counter 2 in a similar manner.

Program Digits 1–4

These four input pins are used to program or set any count desired in counter 1 in Functions 6 and 7. When Program Digit 1 is at V_{SS}, the least significant digit of counter 1 advances at a 2.5 Hz rate. There is no carry-over from digit to digit. Program Digit 1 has no effect if tied to V_{DD} or left floating (internal pull-up to V_{DD}). Only one Program Digit input may be held to V_{SS} at a time.

Program Digit 1/Latch Control

This input has two functions; besides setting a count in digit 1 of counter 1 in Functions 6 or 7, it also affects Functions 3 and 4. In Functions 3 and 4, this input allows the display to show counter 2 counting as described in Functions 3 and 4.

Program Digit 4/Waiting State Indicator

This input besides setting a count in digit 4 of counter 1 in Functions 6 and 7, also indicates that the chip has been reset and is in the stand-by mode at power-on. In Functions 1–5, the Waiting State Indicator is at V_{SS} until a Start-Stop transition has occured. Once a Start-Stop transition has occured, the output remains at V_{DD}.

Leading Zero Blanking

In Functions 1–5, leading zeros are blanked for both counters 1 and 2. In Functions 6 and 7, counter 2 has leading zero blanking. At power-on, the display is blank in Functions 1–5, and all zeros are displayed in Functions 6 and 7.

Output Circuits

For BCD and Digit Outputs, V_{SS} is a logic one. *Figure 5* illustrates the circuit used for all outputs except for Control C1, C2 Out. The Control C1, C2 Out circuit is illustrated in *Figure 6. Figure 7* illustrates the simple interface needed for an 8-digit stop-watch. *Figure 8* illustrates the MM5865 being used to count how many events occur in a specified time. *Figure 9* shows the MM5865 as a simple industrial counter when the input clock is a constant frequency above 400 Hz.

functional description (con't)

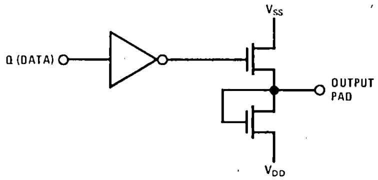


FIGURE 5. Output Circuit

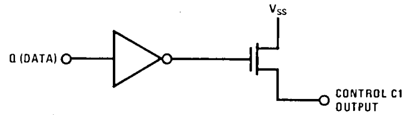


FIGURE 6. Control C1 Out Circuit

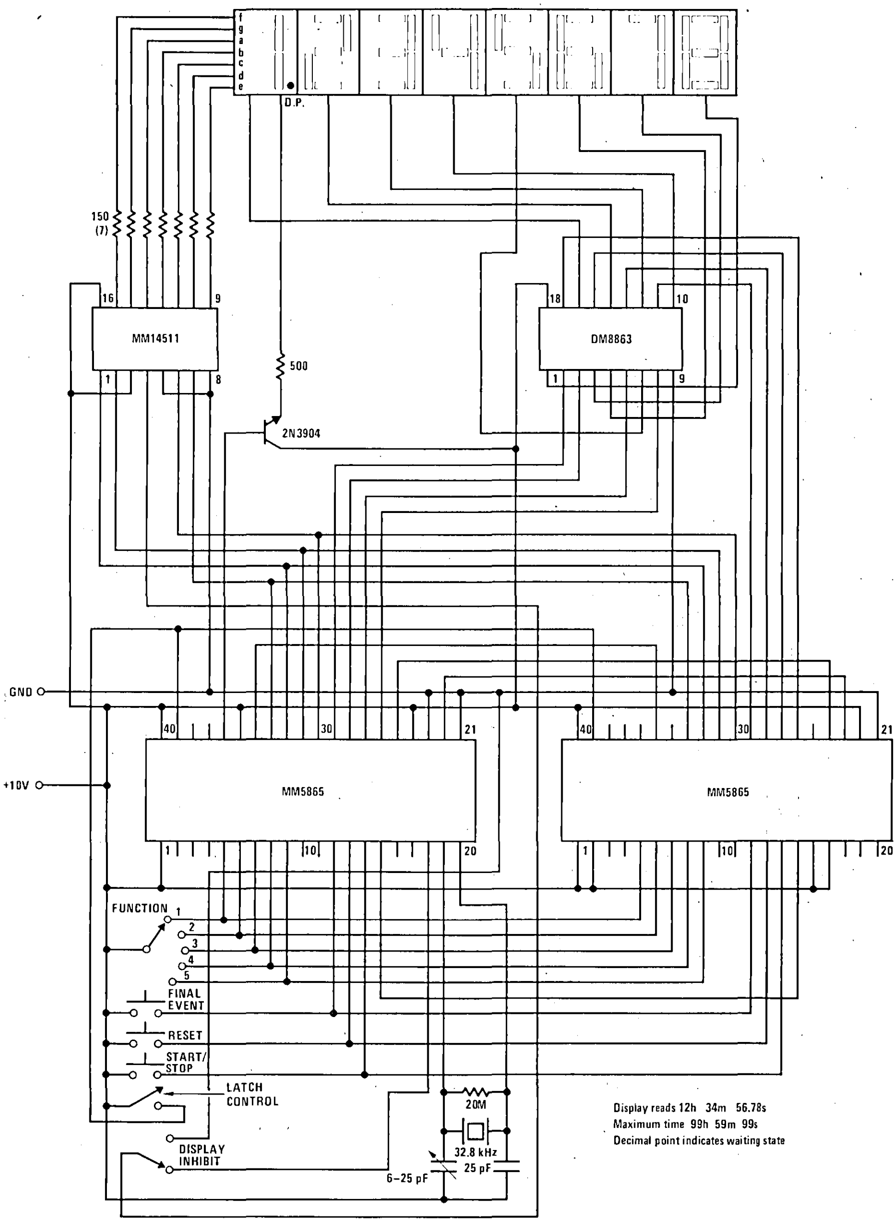


FIGURE 7. Stop Watch Application

functional description (con't)

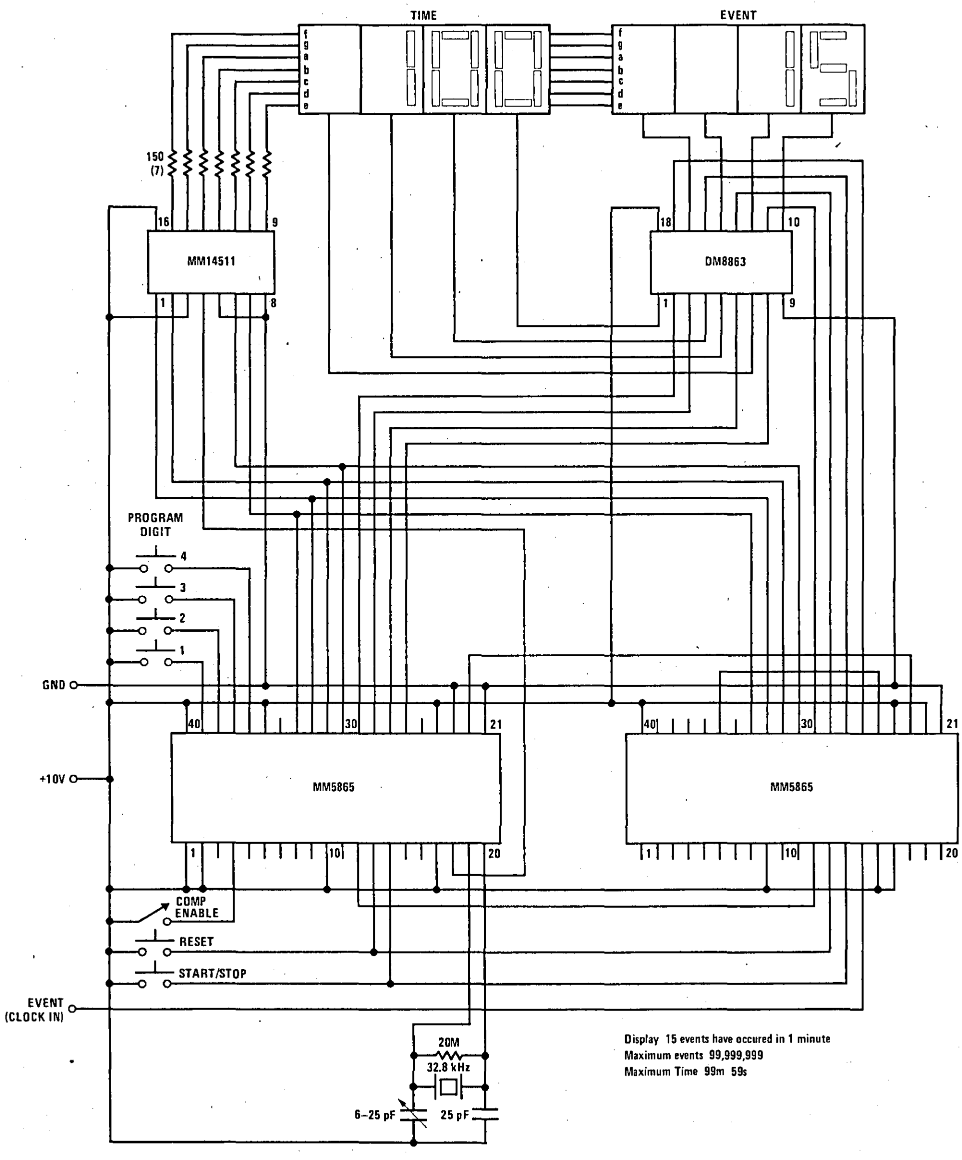


FIGURE 8. Application of MM5865 to Count Events in a Specified Time

functional description (con't)

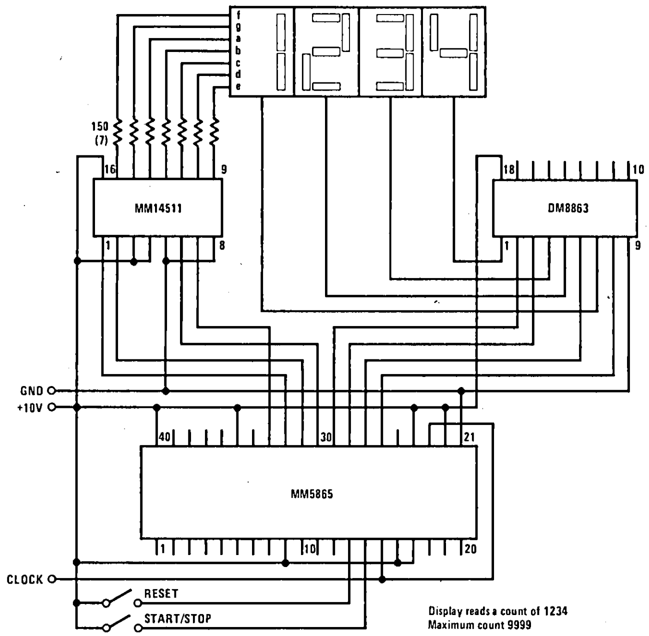


FIGURE 9. Industrial Counter

Counters/Timers

MM53107 17-stage oscillator/divider

general description

The MM53107 is a low threshold voltage CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise 60 Hz reference from a 2.097152 MHz quartz crystal. An internal pulse is generated by the combinations of stages 1–4, 16 and 17 to set or reset the individual stages. The number the circuit will divide by is 34,952. The MM53107 is advanced one count on the positive transition of each clock pulse. One buffered output is available: the 17th stage 60 Hz output. The MM53107 is available in an 8-lead dual-in-line epoxy package.

features

- Divides by 34,952
- Input frequency—2.097152 MHz
- Output frequency—60 Hz
- Crystal oscillator
- High speed (2 MHz at V_{DD} = 2.5V)
- Wide supply range 2–6V
- Low power (0.5 mW @ 2 MHz/2.5V)
- Fully static operation
- 8-lead dual-in-line package

block and connection diagrams

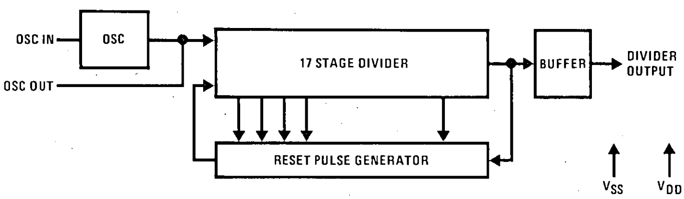
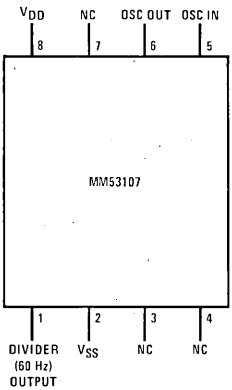


FIGURE 1

Dual-In-Line Package



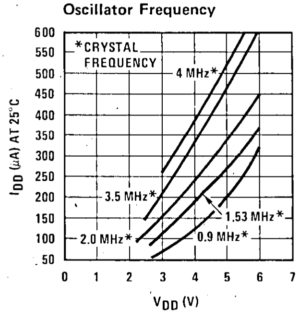
TOP VIEW

FIGURE 2

Order Number MM53107N
See Package 17

typical performance characteristics

Typical Current Drain vs Oscillator Frequency



absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Package Dissipation	500 mW
Maximum V_{CC} Voltage	6V
Operating V_{CC} Range	2.5V to 6V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = Gnd, 2.5V $\leq V_{DD} \leq$ 6V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 6V			10	μA
Operating Current Drain	V_{DD} = 2.5V, f_{IN} = 2.1 MHz			200	μA
Frequency of Oscillation	V_{DD} = 2.4V	dc		2.1	MHz
	V_{DD} = 6V	dc		4.0	MHz
Output Current Levels					
Logical "1" Source	V_{DD} = 4V,	100			μA
Logical "0" Sink	V_{OUT} = 2V	100			μA
Output Voltage Levels					
Logical "1"	V_{DD} = 6V	5.0			V
Logical "0"	I_O = 10 μA			1.0	V

functional description

A connection diagram for the MM53107 is shown in *Figure 2* and a block diagram is shown in *Figure 1.*

TIME BASE

A precision time base is provided by the interconnection of a 2,097,152 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the Osc In and the Osc Out terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

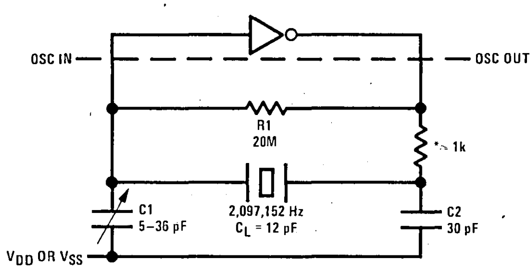
The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

A pulse is generated when divider stages 1–4, 16 and 17 are in the correct state. This pulse is used to set or reset individual stages of the counter, the modulus of the counter is 34,952.

OUTPUT

The Divide Output is the input frequency divided by 34,952. The output is a push-pull output. A typical application of the MM53107 is shown in *Figure 5.*



*To be selected based on the crystal used

FIGURE 3. Crystal Oscillator Network

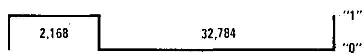
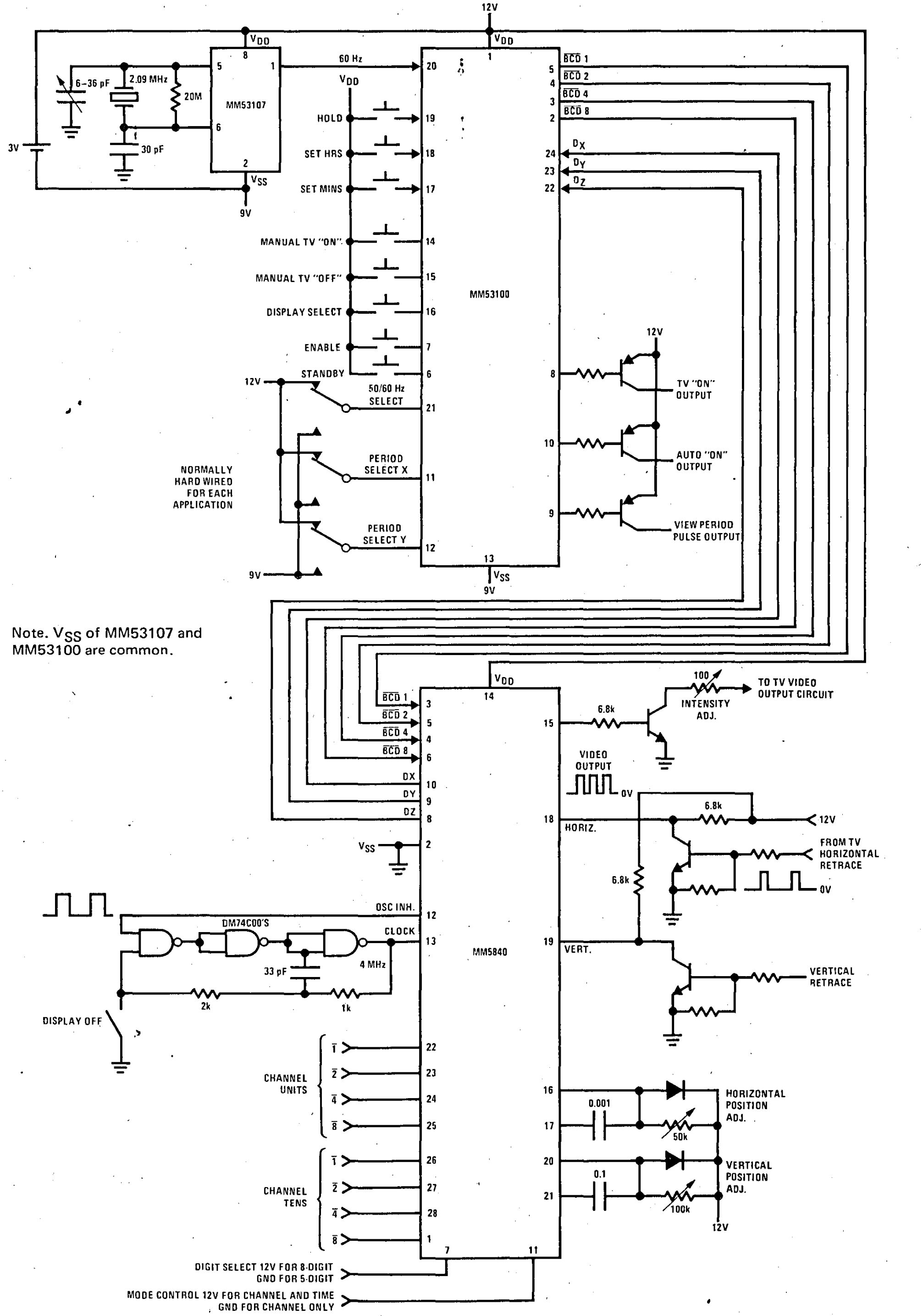


FIGURE 4. Duty Cycle

functional description (Continued)



Note. V_{SS} of MM53107 and MM53100 are common.

FIGURE 5. Typical Application TV Channel and Time Display

MM5865 Universal Timer Applications

introduction

A single chip universal counter and timer is now available from National Semiconductor Corporation through distributors of their products.

The MM5865 universal timer contains, in one 40-pin package, two 4-digit counters, oscillator, 18-stage divider, multiplexer, and all the logic required to control the counters, blank leading zeros, compare the two counters, program one of the counters, and cascade two MM5865 integrated circuits.

The MM5865 provides input pins for seven modes of timing and/or counting operations. When the chip is used as a timer, two input pins may be programmed to provide a display resolution of 0.01 second, 0.1 second, 1 second, or external clock. In addition, the modulo by which the counters divide may be programmed using three divide scaler input pins.

The outputs include the comparator output, multiplexed BCD segment outputs, and digit enable. The BCD segment outputs interface directly with the MM14511 (CD4511), a BCD to 7-segment latch/decoder/driver which interfaces with an LED display. The digit enable outputs of cascaded MM5865s interface directly with a DS8863 (DM8863), an MOS to LED 8-digit driver. A single MM5865 interfaces directly with a DS8877 or DS75492 6-digit driver.

When a suitable crystal is used with the MM5865 oscillator, the counters of a single chip (or those of two chips cascaded) may be used as timers with the following functions:

1. Counter 2: Start-Stop timing
   Counter 1: Total elapsed time
2. Counter 2: Start-Stop timing
   Counter 1: Total accumulated time
3. Counter 2: Sequential event timing
   Counter 1: Total elapsed time
4. Counter 2: Split-timing with total elapsed time
   Counter 1: Not actively used
5. Counter 2: Total accumulated time
   Counter 1: Total elapsed time
6. Counter 2: Up counter
   Counter 1: Programmable counter
7. Counter 2: Programmable down counter
   Counter 1: Not actively used

Therefore, one or two MM5865s along with two other integrated circuits and a 4- or 8-digit display may be used in the following applications:

1. Photographic enlarger timer, with each digit individually programmable
2. Stopwatch
3. General purpose timer
4. Event timer/counter
5. Rally timer
6. Navigational timer
7. Industrial timer/counter

The MM5865 may also be used as a frequency counter, or it may be used as the time reference of a larger frequency counter. The maximum oscillator frequency of the MM5865 is 80kHz; the maximum clock input frequency is 100kHz.

how the MM5865 operates

As can be assumed from the brief description above, the MM5865 is a very powerful integrated circuit, capable of many applications. Therefore, in order to fully stimulate the imagination of readers, its repertoire will be presented in detail.

A block diagram of the MM5865 universal timer is shown in *Figure 1*, and the connection diagram is shown in *Figure 2*. As nearly as possible, all technical terms in the following discussion conform to definitions presented in the *Radio Shack Dictionary of Electronics*, edited by Rudolf F. Graf.

Multiplexer

Because of the internal multiplexer, only one BCD to 7-segment latch/decoder/driver need be used to interface one or two MM5865s to a suitable display. The multiplexer may be controlled in three ways.

An externally generated multiplex frequency may be applied to the Multiplex Input pin of the MM5865. An external clock is then applied to the Clock Input pin. (For example, an LM555C may be used as a square-wave oscillator to provide the necessary input to pin 23.)

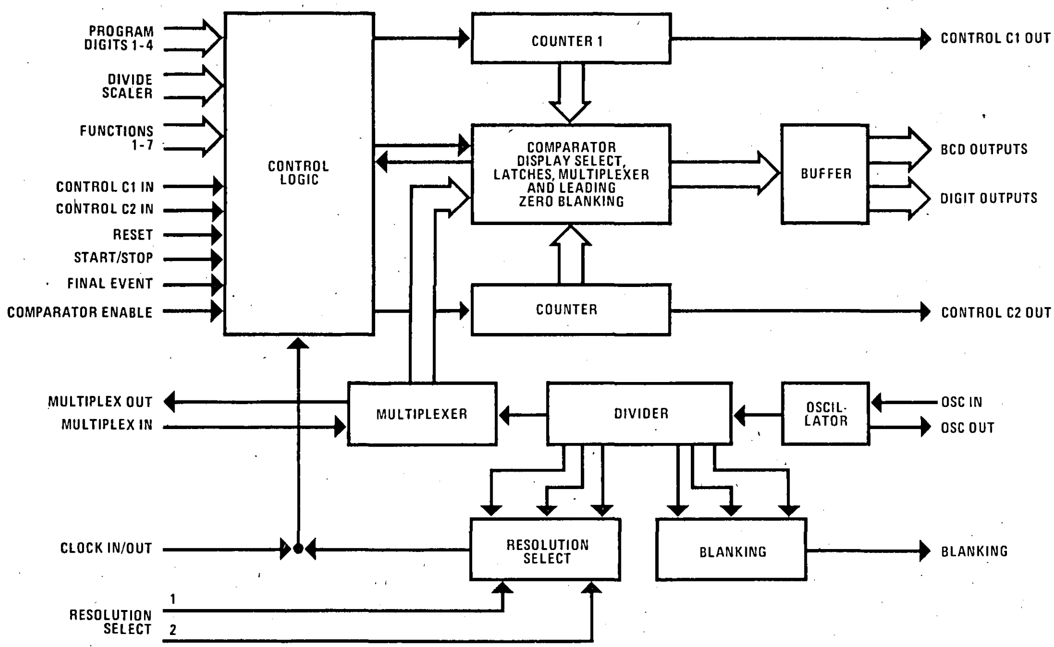


Figure 1. Internal block diagram of the MM5865 Universal Timer.

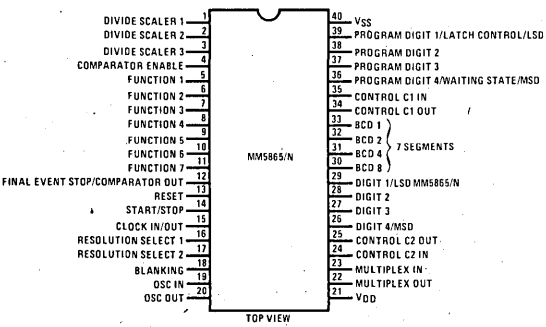


Figure 2. MM5865 connection diagram.

When an external multiplex rate is applied to the Multiplex Input pin, the Multiplex Output pin must be connected to V_{SS}, and the Oscillator In, Oscillator Out, and Blanking pins should be floating. The multiplex rate inside the chip is one fourth the frequency applied to the Multiplex Input pin. In this mode of operation two MM5865s may not be cascaded. In fact, to make use of the Multiplex Output pin, the Multiplex Input pin must be connected to V_{DD}. The frequency at the Multiplex Output pin is the same as that applied to the Multiplex Input pin.

The multiplexer may also be controlled by using internal MOS circuits to form a crystal controlled oscillator. To form the oscillator a crystal, two capacitors, and one resistor must be added externally. One of the capacitors should be variable to allow precise frequency settings. When these external components are connected to the Oscillator Input and Oscillator Output pins, the Multiplex input pin must be connected to V_{DD}.

When the input clock is at a constant frequency above 400Hz the Multiplex Input pin may be connected to the Clock Input pin. In this mode of operation the input clock which is being counted is also used as the externally generated multiplex frequency. The multiplex rate inside the chip will be one fourth the clock input frequency as described above.

Oscillator

Figure 3 shows how external components may be connected to the Oscillator Input and Output pins. A frequency counter used to adjust the frequency of the oscillator may be connected to the Oscillator Output pin through a 50pF capacitor.

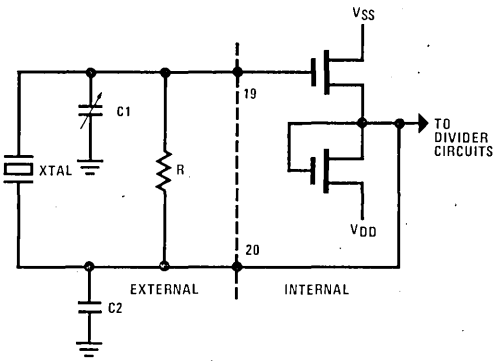


Figure 3. Crystal oscillator connections.

Divider

The divider stages produce the blanking output by dividing the oscillator input frequency by 41. This output is used to blank the display at the beginning and end of each digit time to allow for internal delay between two cascaded chips. The display is blanked when the Blanking Output is at V_{DD}.

The divider stages then divide the blanking output by 2 to generate the Multiplex Output. The frequency which appears at the Multiplex Output pin is further reduced in frequency by the divider stages so that the Resolution Select pins may be used to program the resolution of the display. *Table I* shows how these two inputs are used to select the frequency of the internal clock pulses to be applied to the two counters. The frequencies and display resolutions for an oscillator frequency of 32.8kHz are given.

Table I. Resolution Select Code. A zero indicates that the pin is left floating (or connected to V_{DD}); a one indicates that the pin is connected to V_{SS}. Note that when an external clock is applied to pin 15, pins 16 and 17 must be connected to V_{SS}.

Resolution Select		Frequency of Clock to Counters	Display Resolution
Pin 16	Pin 17		
0	0	100Hz	0.01sec
0	1	10Hz	0.1 sec
1	0	1Hz	1 sec
1	1	External	–

The Clock Input/Output pin is either an input or an output depending on the code at the Resolution Select input pins. If the pin is used as an output it will output the clock frequency selected by the program applied to pins 16 and 17. When it is used as an input an external clock must be used to clock the counters.

Control Logic

The block labeled "Control Logic" contains the logic required to select one of the seven functions, reset all logic and counters, start and stop the counters, indicate that a final event has occurred, and display counter 2 in Functions 3 and 4.

The selection of a function is accomplished by connecting one of the seven function pins to V_{SS}; the other six function pins are left floating.

The Reset Input will reset all logic and counters in Functions 1 - 5 and Function 7. In Function 6, Reset will reset logic and counter 2, but not counter 1. For reset to occur the Reset pin must be momentarily connected to V_{SS}. Internal control logic provides power-on reset, however, to insure proper power-on resetting of all logic and the counters a 10μF, 35V Solid Tantalum Capacitor (Allied #852-5680) should be used across the V_{SS} - V_{DD} power busses.

In Function 6, the Reset Input pin may be connected to the Comparator Output pin in order to automatically reset logic and counter 2. When this connection is made, a Start/Stop transition is all that is needed to repeat the up count of counter 2.

The Start/Stop Input is used to control the counters by momentarily connecting pin 14 to V_{SS}. The manner in which this input affects the counters during the execution of each function will be explained as the descriptions of the functions are given.

The Final Event Stop/Comparator Output pin is used to indicate to the circuit that no more events will be timed or counted. Final Event Stop affects the circuit when it is momentarily connected to V_{SS}. When this pin is used as the comparator output, a V_{SS} level at the pin indicates comparison between the two counters.

Additional Control Logic

The three Divide Scaler inputs permit the counters to be programmed to count in Modulo 6 or Modulo 10. *Table II* shows the possible codes which may be applied to the Divide Scaler pins. A zero indicates that the pin is left floating (or connected to V_{DD}); a one indicates that the pin is connected to V_{SS}.

Table II. Divide Scaler Code

Divide Scalers			Modulo							
			Counter 1				Counter 2			
Pin			Digit				Digit			
1	2	3	4	3	2	1	4	3	2	1
0	0	0	10	10	10	10	10	10	10	10
1	0	0	6	10	10	10	6	10	10	10
0	1	0	10	6	10	10	10	6	10	10
1	1	0	10	10	6	10	10	10	6	10
0	0	1	10	10	10	10	10	10	10	10
1	0	1	10	10	10	10	6	10	10	10
0	1	1	10	10	10	10	10	6	10	10
1	1	1	10	10	10	10	10	10	6	10

A zero indicates that the pin is left floating (or connected to V_{DD}); a one indicates that the pin is connected to V_{SS}.

2

For example, if the Resolution Select pins are programmed to give a 1 second display resolution (code "10") in a stopwatch application, and if the Divide Scaler code is "110," then the maximum possible count for both counters 1 and 2 would be 9959 (99 min, 59 sec). This means that the unit minutes display will advance by one digit every 60 seconds.

Connecting pin 4 to V_{SS} enables the comparator. In functions 1-5 the Comparator Enable pin must be left floating (or connected to V_{DD}). In function 6 the Comparator Enable pin must be connected to V_{SS} after digit programming; if the Comparator Enable pin is connected to V_{SS} (comparator enabled) at power on, the Reset pin must be momentarily connected to V_{SS} before a Start/Stop transition will begin the counter 2 count-up.

In function 7, if the Comparator Enable pin is floating (or connected to V_{DD}) when power is applied to the chip, or when the function switch is switched to function 7, the Comparator Enable pin must be connected to V_{SS} after digit programming as in function 6; however, in function 7, if the Comparator Enable pin is connected to V_{SS} (comparator enabled) at power on (or when the function switch is switched to function 7), the comparator must be disabled by 1) disconnecting the Comparator Enable pin from V_{SS}, and 2) momentarily connecting the Reset pin to V_{SS}; this must be done before the digits are programmed. This is necessary, of course, because connecting the Reset pin to V_{SS} after digit programming will simply reset counter 1 to "0000." In function 6, a Reset transition after digit programming does not reset counter 1 to "0000."

In addition, the Control C1 In pin (pin 35) must be floating (or connected to V_{DD}) during digit programming in function 7. After digit programming, the Control C1 In pin must be connected to V_{SS} before the count-down begins. A DPDT, Center "OFF" switch connected as shown in *Figure 4*, may be used to control both the Comparator Enable pin and the Control C1 In pin. In one position the DPDT switch connects the Control C1 In pin to V_{SS} for functions 1-5. Digit programming may be accomplished in function 7 by placing the switch in the Center "OFF" position. In the third position both the Comparator Enable and the Control C1 In pins are connected to V_{SS} for functions 6 and 7.

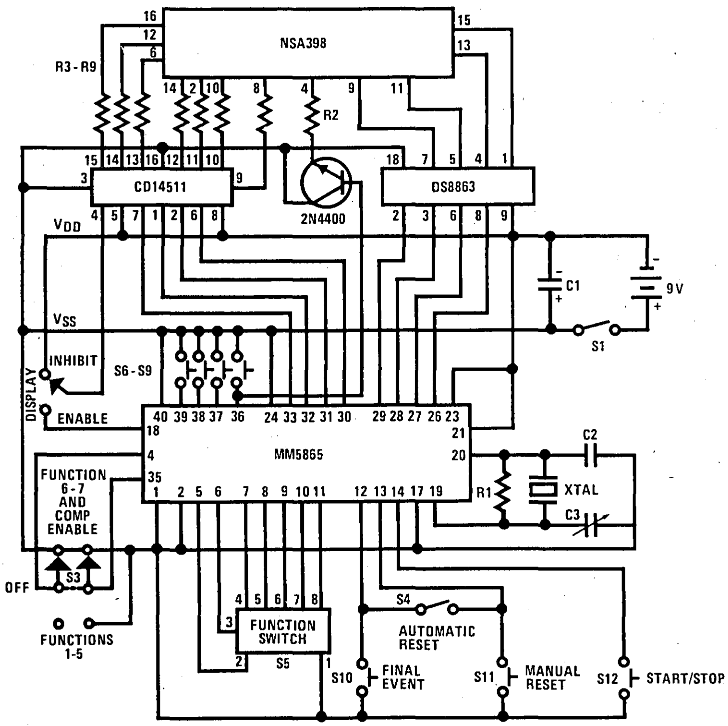


Figure 4. Stopwatch/Timer application showing the connections for a single MM5865. Two cascaded MM5865s may also be used, as described in the text.

Pins 36 - 39, the Program Digit 1 - 4 pins, are used to program a desired count into counter 1 when using functions 6 and 7. When any of the four Program Digit pins are connected to V_{SS}, the display digit of counter 1 associated with that pin advances at a 2.5 Hz rate (assuming the oscillator frequency is 32.8kHz). The Program Digit 1 pin advances the least significant digit of counter 1; the Program Digit 4 pin advances the most significant digit. There is no carry over from digit to digit, and only one Program Digit Input may be connected to V_{SS} at a time.

The Program Digit 1 pin also functions as a counter 2 latch control in functions 3 and 4. In functions 3 and 4, momentarily connecting the Program Digit 1/Latch Control pin to V_{SS} permits the display to show counter 2 counting.

The Program Digit 4 pin also serves two purposes; in functions 1 - 5 this pin indicates that the chip has been reset and is in the standby mode at power-on. Visual indication of this condition may be accomplished by connecting a transistor between the Program Digit 4/ Waiting State Indicator pin and the Segment DP Anode of a multiplexed display. With the transistor connected as shown in *Figure 4*, the Waiting State Indicator pin will be at V_{SS} at power-on until a Start/Stop transition occurs. After a Start/Stop transition occurs, the Waiting State Indicator pin will remain at V_{DD} until power is removed from the chip.

Leading Zero Blanking

In functions 1 - 5, leading zeros are blanked for both counters. In functions 6 and 7, counter 2 has leading zero blanking but counter 1 does not. At power-on the display is blank (or all decimal points if the Waiting State Indicator pin is used) in functions 1 - 5; all zeros are displayed in functions 6 and 7.

Control C1, C2 In and Control C1, C2 Out

These four pins are used to cascade two chips together. In this mode of operation the primary MM5865, which is directly controlled by the crystal oscillator, connects to another MM5865 in the following manner: the Control C1 In pin of the primary chip is connected to V_{SS} except during digit programming in function 7; the Control C1 Out pin connects to the Control C1 In pin of the other MM5865; the Control C2 In pin of the primary chip is connected to V_{SS}; the Control C2 Out pin connects to the Control C2 In pin of the other MM5865; the Control C1 Out and the Control C2 Out pins of the second chip are left floating.

When the Control C1 In pin is floating (or connected to V_{DD}), the clock pulses to counter 1 are inhibited. When the Control C1 In pin is connected to V_{SS}, counter 1 is enabled. Control C1 Out is at V_{SS} when counter 1 is at its maximum count, and it is floating at all other times. The Control C2 pins affect counter 2 in a similar manner.

Other possible connections between the two chips are: 1) all function pins connected together, 2) pins 12, 13, 14, and 15 connected together, 3) all BCD pins connected together, and 4) pins 39 connected together in functions 1 - 5 only.

When two MM5865s are cascaded as described above, eight momentary switches or individual electrical signals must be provided if every digit of the display is to be programmable. In addition, another switch would have to be provided to break the pin 39 connection between the two chips in functions 6 and 7. Of course, all of the switching action could be provided by one ganged rotary switch if desired; even the function 6 Reset to Comparator Out connection could be accomplished if the proper switch were used.

Electrical Characteristics

The maximum supply voltage which may be connected between V_{SS} and V_{DD} (V_{DD} = 0V) is 20V. National specifies that the minimum voltage at which the chip will operate is 7V; however, some chips will operate well down to V_{SS} = 5V. With a 9V transistor battery used as the power supply, and display inhibited, the power supply current will be approximately 7mA to 15mA for a one-chip stopwatch.

The maximum input frequency at the oscillator is 80kHz; however, the oscillator and dividers are designed for stopwatch applications using a 32.8kHz crystal. (A 32.768kHz crystal, available from Quest Electronics, P.O. Box 4430 E, Santa Clara, CA 95054, may be used without much loss in accuracy.)

Drivers must be provided for the Digit and BCD Outputs. Two MM5865s interface directly with the MM14511 Segment Driver and the DS8863 Digit Driver. A DS8877 or DS75492 Hex Digit Driver may be used with a single MM5865.

The Seven Functions

The one-chip circuit shown in *Figure 4* indicates all connections necessary to employ the MM5865 as a 4-digit stopwatch/timer. The seven available functions will be described using this figure, in which the desired function is selected by switching S5. When necessary, refer also to *Figures 1* through *3*.

Function 1

In function 1, at power-on (S1 closed) four decimal points are visible on the display, indicating that the counters have been reset, but not necessarily all logic. If the Comparator Enable pin is connected to V_{SS} (S3 in Function 6 - 7 position) at power-on, a Start/Stop transition (obtained by momentarily closing S12) will cause the decimal points to disappear from the display; however, the chip will not begin counting. First it is necessary to place S3 in the Functions 1 - 5 position, then to reset the logic (by momentarily closing S11).

Once all logic is reset (either by applying power with S3 in the Functions 1 - 5 position or by the method discussed above), a Start/Stop transition will cause both counters to begin counting up. The up-count of counter 2 is displayed, the least significant digit advancing at a 1 Hz rate. A second Start/Stop transition inhibits the clock pulses to counter 2 and stores and displays the contents of counter 2; however, counter 1 continues to count. A third Start/Stop transition resets counter 2, enables clock pulses to counter 2 and, again, displays counter 2 counting up. Subsequent Start/Stop transitions repeat this sequence. Counter 1 continues to count, from the time of the first Start/Stop transition, until the occurrence of a Final Event Stop transition (obtained by momentarily closing S10). A Final Event

2

Stop transition inhibits the clock pulses to both counters and displays counter 2. After this Final Event Stop transition has occurred, a Start/Stop transition switches the display from counter 2 to counter 1. Each subsequent Start/Stop transition alternately displays one of the counters.

To summarize, in function 1 both counters start counting up with an initial Start/Stop transition. Counter 1 continues to count (recording total elapsed time) until a Final Event Stop transition. Counter 2 (alternately) starts, then stops counting with each Start/Stop transition (timing as many intervals as desired), until a Final Event Stop transition. Any time a Reset transition occurs both counters are reset to "0000" and the display blanks.

Function 2

The only difference between functions 1 and 2 is that in function 2, whenever a Start/Stop transition inhibits the clock pulses to counter 2, the clock pulses to counter 1 are also inhibited. Start/Stop transitions which reset counter 2 and enable clock pulses to counter 2 also enable clock pulses to counter 1; counter 1 does not reset, however. The up-count in counter 1 resumes at the stored count; therefore, counter 1 records total accumulated time.

Function 3

In function 3 the power-on conditions are the same as those in functions 1 and 2. Once all logic is reset a Start/Stop transition causes both counters to begin counting up Counter 2 is displayed counting. A second Start/Stop transition stores and displays the contents of counter 2, resets counter 2, and initiates a new up-count. However, the new up-count is not displayed. Counter 1 continues to count. The initial count remains displayed until a third Start/Stop transition. This third Start/Stop transition and subsequent Start/Stop transitions repeat the sequence described above, indicating the length of time between successive Start/Stop transitions.

The occurrence of a Latch Control transition (obtained by momentarily closing S5) any time after the second Start/Stop transition will cause counter 2 to be displayed while counting. The count will continue to be displayed until a Start/Stop transition. This Start/Stop transition also stores and displays the contents of counter 2 and then resets counter 2. As before, counter 1 continues to count, but counter 2 begins a new count.

A Final Event Stop transition inhibits the clock pulses to both counters and displays the contents of counter 2. A Start/Stop transition occurring after the Final Event Stop transition switches the display from counter 2 to counter 1. Repetitive Start/Stop transitions switch the display between counter 2 and counter 1. Any time a Reset transition occurs, both counters are reset to "0000" and the display blanks.

Function 4

In function 4 the power-on conditions are the same as those in functions 1 - 3. Once all logic is reset a Start/Stop transition causes counter 2 to begin up-counting. Counter 2 is displayed counting. A second Start/Stop transition stores and displays the contents of counter 2. Subsequent Start/Stop transitions update the display of counter 2. A Latch Control transition will display counting until the occurrence of a Start/Stop transition. This Start/Stop transition, following the Latch Control transition, does not reset counter 2 as it does in function 3. Rather, counter 2 continues to count up. A Final Event Stop transition inhibits the clock pulses to counter 2 and displays the contents of counter 2. A Reset transition at any time resets counter 2 to "0000."

Function 5

Again, in function 5 the power-on conditions are the same as those in functions 1 - 4. Once all logic is reset a Start/Stop transition causes both counters to begin counting up. Counter 2 is displayed counting. A second transition on the Start/Stop pin inhibits the clock pulses to counter 2, and the contents of counter 2 are displayed. Counter 1 continues to count. A third Start/Stop transition enables the clock pulses to counter 2; counter 2 resumes counting where it left off, and counter 2 is displayed counting.

Subsequent Start/Stop transitions repeat this sequence with counter 1 counting continuously. A Final Event Stop transition inhibits the clock pulses to both counters and displays counter 2. A Start/Stop transition switches the display from counter 2 to counter 1. Repetitive Start/Stop transitions switch the display between counter 2 and counter 1. A Reset transition at any time resets both counters to "0000."

Function 6

At power-on in function 6, counter 1 is displayed with "0000." If the comparator is enabled (S3 in the Function 6 - 7 position) at power on, a Reset transition (obtained by momentarily closing S11) is necessary before a Start/Stop transition can begin the counter 2 count-up.

Counter 1 is programmed to the desired count by holding each of the four Digit Programming Switches Closed in turn. The comparator must then be enabled by placing S3 in the Function 6 - 7 position (unless it was already enabled at power-on). Counter 2 is displayed counting up beginning with a Start/Stop transition. When counter 2 is coincident with counter 1, the clock pulses to counter 2 are inhibited, the contents of counter 2 are displayed, and the Comparator Output is enabled. A Reset transition after the counter 2/counter 1 coincidence disables the Comparator Output and displays counter 1 with the programmed time. The Reset transition can be obtained either by momentarily closing S11 or by connecting the reset Input pin to the Comparator Output pin after Digit Programming so that logic and counter 2 are reset automatically whenever counter 2 is coincident with counter 1.

After each Reset transition, subsequent Start/Stop transitions repeat the sequence. Counter 1 may be reprogrammed after any Reset transition, if desired. If a Reset transition occurs while counter 2 is counting up, the clock pulses to counter 2 are inhibited, counter 2 is reset, and counter 1 is displayed with the programmed time.

If a Start/Stop transition occurs while counter 2 is counting up, the clock pulses to counter 2 are inhibited and counter 1 is displayed with the programmed time. With the next Start/Stop transition, counter 2 resumes counting where it was stopped.

If the Reset Input pin is not connected to the Comparator Output pin and if a Final Event Stop transition occurs while counter 2 is counting up, the clock pulses to counter 2 are inhibited and the contents of counter 2 are displayed. The next Start/Stop transition displays counter 1 with the programmed time. Repetitive Start/Stop transitions switch the display between counter 2 and counter 1. A Reset transition followed by a Start/Stop transition starts the counter 2 up-count sequence again.

In function 6, and also in function 7, the digit which is preprogrammed to count in Modulo 6 cannot, of course, be programmed to a digit greater than 5.

Function 7

In function 7 counter 1 is displayed with "0000" at power-on. If S3 is in the Function 6 - 7 position at power-on, it must be placed in the "OFF" position; then S11 must be momentarily closed. Counter 1 is set to a specific count by holding each of the four Digit Programming Switches closed in turn; then the Comparator must be enabled by placing S3 in the Function 6 - 7 position.

Counter 1 counts down from the set count beginning with a Start/Stop transition. When counter 1 counts down to zero the clock pulses to counter 1 are inhibited and the Comparator Output is enabled. This is not repeatable without a new count being entered into counter 1. A Final Event transition halts the counter 1 down-count, and subsequent Start/Stop transitions have no effect on counter 1 or counter 2. A Reset transition resets counter 1 to "0000."

Peripheral

The other components shown in *Figure 4* consist of input/output interfaces between the user and the MM5865. The crystal used in this stopwatch/timer circuit is a watch crystal cut to oscillate at 32.768kHz. (A 32.8kHz crystal would be best.) This means that the blanking frequency is 799.2Hz, the multiplex frequency is 399.6Hz, and the clock frequency to the counters is 0.99902Hz.

The oscillator frequency may be adjusted by connecting a counter to pin 20 of the MM5865 through a 50pF capacitor and then varying the capacitance of C3. Any attempt to alter the values of R1, C2, or C3 will probably fail; that is, the oscillator will probably not oscillate.

Most of the switches which control the MM5865 are momentary push-buttons which are available from many sources. The function switch, however, is a very small 8-position switch in a TO-5 package; it is available from James Electronics, P.O. Box 822, Belmont, CA 94002.

The 2N4400 (a 2N3904 can also be used) drives the decimal point anode of the display and is itself driven by the Waiting State output of the MM5865.

The MM14511 provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability of 25mA. The DS8863 is an 8-digit driver; each driver is capable of sinking up to 75mA. The MM14511 may be operated at supply voltages up to 15V; however, the DS8863 cannot be operated with supply voltage greater than 10V. For operation with supplies up to 18V, the DS8963 is a direct replacement for the DS8863.

The NSA398 is a 9-digit common cathode LED numeric display with a 1/8-inch character height. Eight inputs are provided for selection of the appropriate segments and decimals (anodes) and nine inputs for digit (cathodes) selection. The anodes are internally interconnected for multiplexing. The NSA398 has a red faceplate which provides excellent visual contrast and ease of visibility over a wide angle. *Figure 5* shows the physical dimensions and pin connections of the NSA398.

practical applications of the stopwatch/timer

Now that the basic operation of the MM5865 has been presented, it is possible to examine practical applications of the seven function universal timer shown in *Figure 4*. This timer, as shown, has a maximum timing capability of 99 minutes, 59 seconds. If another MM5865 is added to the circuit, this timing capability may be extended to 99 hours, 59 minutes, 99.99 seconds. For very accurate timing, the crystal should be cut to oscillate at 32.8kHz, and the oscillator frequency should be precisely tuned to 32.8kHz.

When the stopwatch/timer is being used to time any event, the display should be disabled with S2 as much as possible so that battery power will be conserved.

Function 1 may be used to time two events occurring simultaneously in the following manner. A driver often travels from his home to a city some hours away. On the way he passes a small town about halfway between his home and the city. He wishes to know how long it takes him to travel from his home to the small town, how long it takes to travel from the town to the city, and finally, how long it takes him to travel from his home to the city.

At the beginning of the trip the driver presses the Start/Stop switch. The display begins to record the time accumulating in counter 2. As he passes through the small town he presses the Start/Stop switch again and records the traveling time from his home to the town. Then he presses the Start/Stop switch again. As he arrives at the city he presses the Final Event Stop switch and records the time shown in the display as being the traveling time from the town to the city. He then presses the Start/Stop switch and sees in the display the traveling time from his home to the city.

Function 2 may be used to record the total accumulated time of several events while each event is being timed individually. For example, a television repairman spends his day ordering parts, talking to customers, and repairing televisions on the bench. He wants to record the time he spends repairing each set so that customers may be properly billed, and he wishes to record his total bench time for the day.

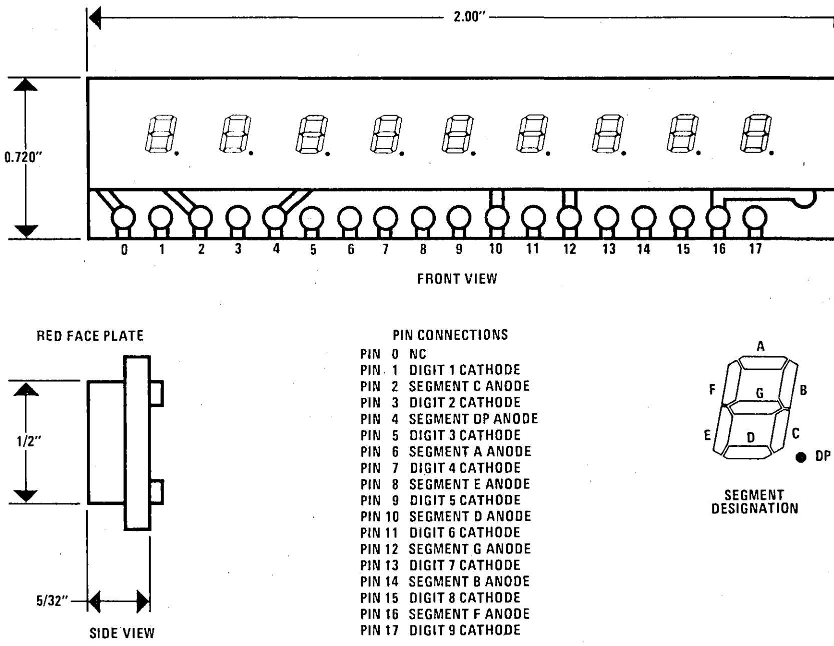


Figure 5. Physical dimensions and pin connections of the NSA398.

At the beginning and end of every bench job he presses the Start/Stop switch to record the time for each job. At the end of his day he presses the Final Event Stop switch, then the Start/Stop switch to record his total bench time.

As an example of a function 3 application, consider an assembly line position at which a worker must fasten three parts to a piece of equipment. A supervisor wishes to record the time it takes the worker to fasten each part and the amount of time the equipment spends at this position.

As the worker receives the piece of equipment, the supervisor presses the Start/Stop switch. The display begins counting up. As the worker finishes with the first part, the supervisor presses the Start/Stop switch. This time will remain in the display until the next Start/Stop transition; the supervisor therefore has a chance to record the first event time.

As the worker finishes with the second part, the supervisor presses the Start/Stop switch again and records the time of the second event. After the worker finishes with the third part the supervisor presses the Final Event Stop switch. The display will show the third event time. The supervisor can then press the Start/Stop switch to record the total time this worker handled the equipment.

With function 4, the total time of an event may be accumulated, and the display may be updated while counter 2 is accumulating the total time. For example, a long distance runner desires to pace himself over a 5-mile run. As he starts out he presses the Start/Stop switch. Then, as he passes known checkpoints, he presses the Start/Stop switch to update the display and note the time of arrival at each check point. At the end of the 5-mile run he presses the Final Event Stop switch to record the total time for the run.

Function 5 may be used to record both total accumulated time and total elapsed time. As an example of an application of function 5, consider a pilot who wants to record total flying time as well as total trip time.

As the pilot starts out he presses the Start/Stop switch. He then presses the Start/Stop switch each time he lands and each time he resumes flying. At the end of his trip he presses the Final Event Stop switch and records total flying time. He then presses the Start/Stop switch to record total trip time.

With proper interfacing, function 6 can be used as an enlarger timer. A photographer programs the desired printing time into the display with the Digit Programming switches, closes the Comparator Enable switch, and closes the Automatic Reset switch. For each print he

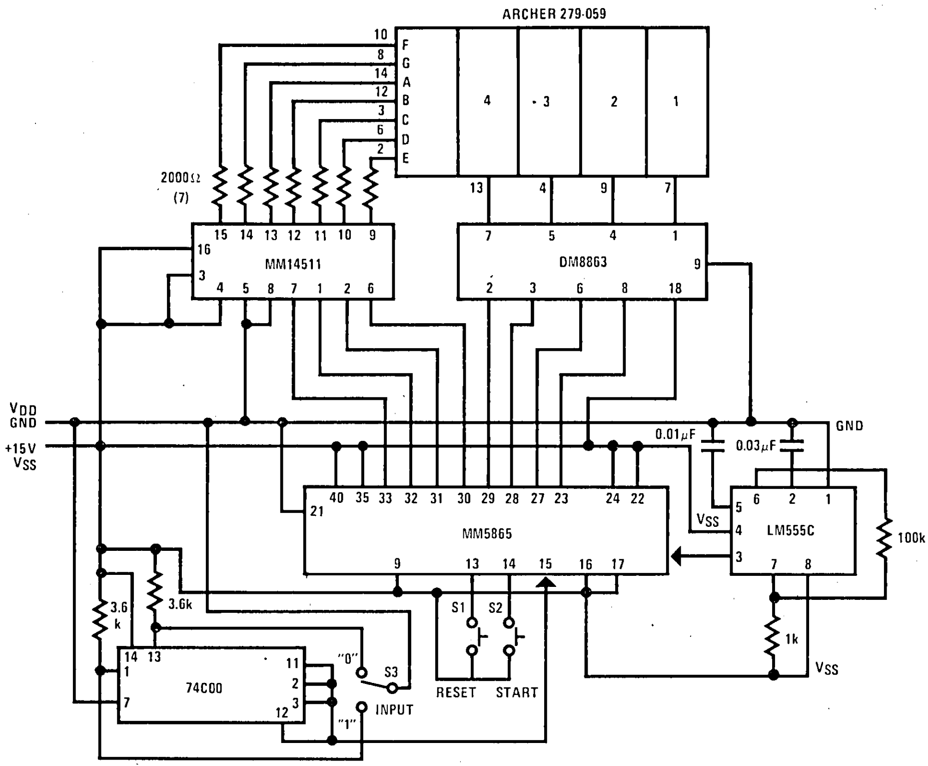


Figure 6. The MM5865 used in a simple counting circuit.

simply presses the Start/Stop switch to turn on the enlarger for the desired length of time.

It is not necessary to enable the display while operating the timer. The display must be enabled only to program counter 1. The Reset switch may be pressed at any time to turn off the enlarger. The enlarger may be turned on for adjusting negatives by pressing the Start/Stop switch without enabling the comparator.

With proper interfacing, function 7 may be used as a down-count timer for many applications, including cooking and washing. The desired time is simply programmed into counter 2, the comparator is enabled, and then the Start/Stop switch is pressed. Counter 2 will count down to zero and turn off the appliance.

A few applications (some for which two MM5865s are required) have been presented to illustrate the utility of the MM5865. The Stopwatch/Timer discussed above is but one general application for which the MM5865 may be used.

Figure 6 shows a simple manual counting circuit in which the MM5865 is used to count the closures of a manual switch. Of course, the manual clock could be replaced by electrical pulses.

The 74C00 in this circuit debounces the switch used as a clock, S3. An LM555 is used to provide a multiplexer input frequency of 233 Hz.

The MM5865 is operating in function 5, and displays the up-count of counter 2. After an initial Start/Stop transition, each closure of the manual switch advances the displayed digits by one count. A Reset transition resets counter 2 to "0000."

conclusion

The emphasis of this presentation has been on the general timing and programmable capabilities of the MM5865 rather than on specific applications. Because so many functions are available in one package, it is possible to use the MM5865 as a general purpose chip, adding another MM5865 when it is necessary. In most applications only one or several of the seven functions need be used; however, because of its general purpose nature, the MM5865 lends itself well to the concept of quantity purchasing.

A final note: Unless the start pulse is externally synchronized to the clock (available at pin 15 of the MM5865, if the internal oscillator is used), the amount of time which will elapse between the arrival of the start pulse at pin 14 of the MM5865 and the appearance of the first digit in the display will not be equal to the programmed display resolution. It is possible to develop a start pulse that is synchronized to the clock using an MM74C221 Dual Monostable Multivibrator as shown in *Figure 20*. The time constant of R1 - C1 should be equal to the display resolution, the time constant of R2 - C2 should be less than the programmed display resolution, and the time constant of R3 - C3 should be less than the time constant of R2 - C2.

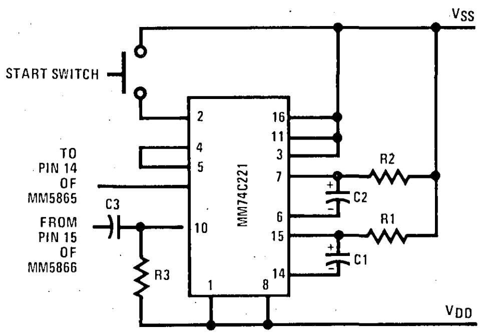


Figure 21. Start-Pulse Synchronizer. Time constant of R1 - C1 = display resolution. Time constant of R2 - C2 < display resolution. Time constant of R3 - C3 < time constant of R2 - C2.

A 4-Digit, 7-Function Stopwatch/Timer

introduction

This construction article is the second of a series which is to concentrate on applications of the MM5865 universal timer. The first article, "MM5865 Universal Timer Applications," presented in detail the programmable and functional characteristics of the MM5865.

This second article illustrates the construction and use of a 4-digit, 7-function stopwatch/timer in which the display resolution and counter modulo may be programmed with printed circuit board jumper wires.

Other than switches, all components of the stopwatch/timer are mounted on a glass-epoxy or glass-polyester board which is laminated with 1-ounce copper foil on one side. The board is mounted in the attractive instrument/clock case available from James Electronics.

This instrument/clock case has provisions for the display, precut holes for four calculator-type switches, and a precut line cord hole. In addition, the case is sold with a red display bezel, four rubber feet, and a flip-top to conceal the four switches which may be assembled in the precut holes.

A display resolution of 1 second, 0.1 second, or 0.01 second may be programmed by on-board jumpers or a suitable switch. Furthermore, the counters may be programmed to count in modulo 6 or modulo 10.

When used as a photographic enlarger timer or as an appliance timer, each digit is individually programmable with one of four pushbutton switches. The comparator output of the timer may be coupled to an enlarger/appliance control circuit that can be permanently mounted to the enlarger or appliance.

Applications for the stopwatch/timer include, but are not limited to, the following:

- Laboratory reaction and interval timer
- Photographic enlarger and chemical processing timer
- Stopwatch
- Event timer
- Appliance timer

A simple listing of possible applications for the timer does not adequately describe the enormous power of the instrument. A tabulation of the seven functions which includes a break-out of the functions performed simultaneously by counters 1 and 2 of the MM5865 is much more revealing, and is presented below:

1. Counter 2: Start-stop timing
   Counter 1: Total elapsed time
2. Counter 2: Start-stop timing
   Counter 1: Total accumulated time
3. Counter 2: Sequential event timing
   Counter 1: Total elapsed time
4. Counter 2: Split-timing with total elapsed time
   Counter 1: Not actively used
5. Counter 2: Total accumulated time
   Counter 1: Total elapsed time
6. Counter 2: Up counter
   Counter 1: Programmable counter
7. Counter 2: Programmable down counter
   Counter 1: Not actively used

operation

The switches which control the operation of the stopwatch/timer are visible on top of the case shown in the photographs of *Figures 1a* and *1b*. Each switch is indicated in the schematic drawing of *Figure 2*.

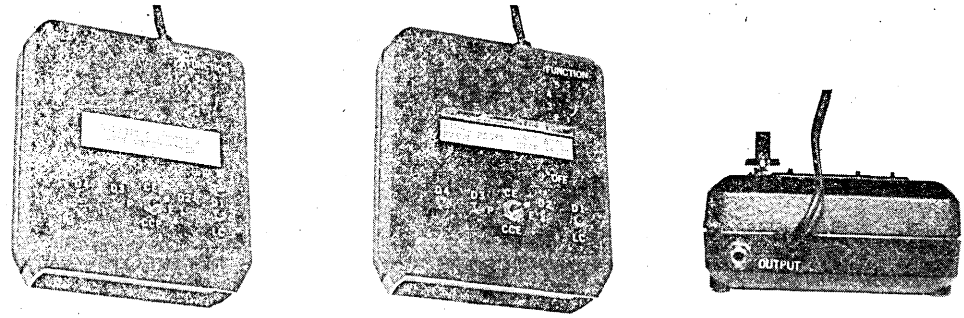
In *Figure 1a*, the switch in the rear right hand corner of the case is a 7-position rotary Function Switch (F). At the front of the case the switches are, from left to right, Digit 4 Programming Switch (D4), Digit 3 Programming Switch (D3), Comparator Switch (C), Digit 2 Programming Switch (D2), and Digit 1 Programming (D1)/Latch Control (LC) Switch. Digit 1 is the least significant digit (LSD); Digit 4 is the most significant digit (MSD).

There are four switches under a center flip-cover. These are shown in *Figure 1b*. From left to right they are Final Event Switch (FE), Reset Switch (R), Start/Stop Switch (SS), and Automatic Reset Enable Switch (ARE).

The ARE switch is used only in function 6; it must be OFF for all other functions. The C switch has three positions: Comparator/Count Enable (CCE), used for functions 6 and 7; Program Enable (PE), used for function 7; and Count Enable (CE), used for functions 1 through 5. The D1/LC switch is a dual purpose switch; for functions 3 and 4 it serves as the latch control switch, and for functions 6 and 7 it serves as the Digit 1 programming switch. There is no ON-OFF switch. Power is applied to the stopwatch/timer by plugging the line cord into a 120VAC/60Hz outlet.

Table I is a tabulation of the abbreviations used for the switches and the functions to which they apply. If the F switch is set to any of the stop watch functions (1 through 5) when power is initially applied to the stopwatch/timer, the display will remain blank. See "MM5865 Universal Timer Applications" for information on using pin 39 as a power on indicator.

To operate the stopwatch/timer in any of the stopwatch functions, rotate the F switch to one of the stopwatch function positions, place the ARE switch in the OFF position, place the C switch in the CE position, and press the R switch.



(a) (b) (c)

Figure 1. External Photographs of Stopwatch/Timer. a) View of Function Switch, Comparator Switch, and Digit Programming Switches. b) With flip-cover raised, four additional switches are seen. The flip-cover is designed so that a press of the closed cover closes the Start/Stop Switch. c) A miniature jack is mounted at the rear of the case so that a cable may be run to the appliance control box.

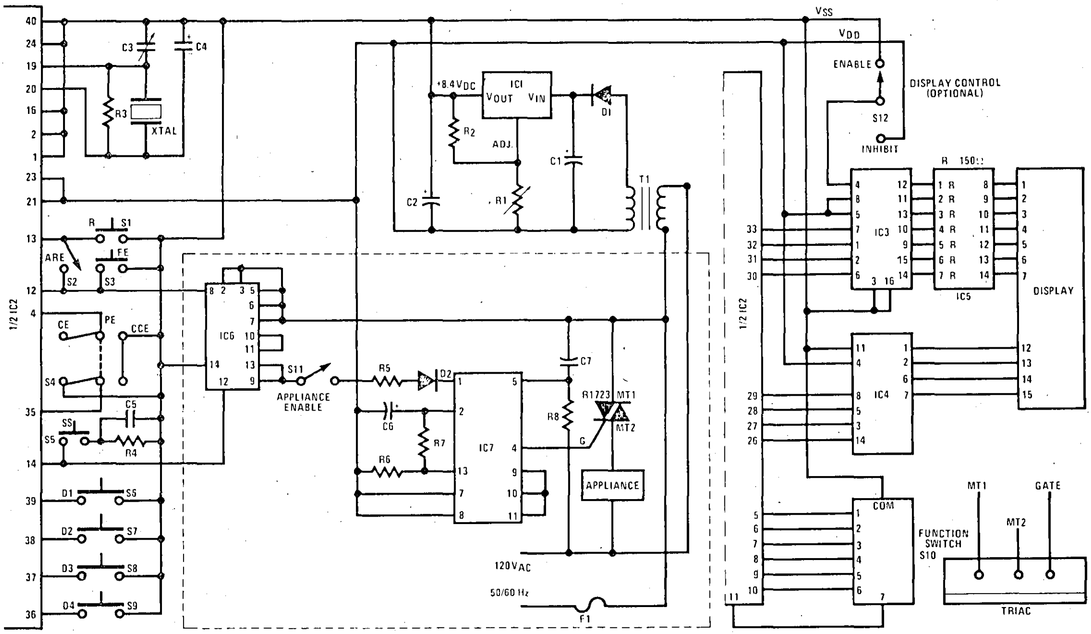


Figure 2. Schematic Diagram of the 4-Digit, 7-Function Stopwatch/Timer. As drawn, the display resolution is 1 second. A SPST switch may be included between pin 16 of IC2 and V_{SS} to provide a display resolution of 0.01 second or 1 second. Another option, shown in the figure, is the Display Control Switch, which may be used to inhibit the display.

Table I. Switch Abbreviations

Abbreviation	Switch	Functions
ARE	Automatic Reset Enable	6
C	Comparator	1-7
D1	LSD Programming	6, 7
D2	Digit 2 Programming	6, 7
D3	Digit 3 Programming	6, 7
D4	MSD Programming	6, 7
F	Function	1-7
FE	Final Event	1-5
LC	Latch Control	3, 4
R	Reset	1-7
SS	Start/Stop	1-7

Table II. Resolution Select Code. A zero indicates that the pin is left floating (or connected to V_{DD}); a one indicates that the pin is connected to V_{SS}. Note that when an external clock is applied to pin 15, pins 16 and 17 must be connected to V_{SS}.

Resolution Select		Frequency of Clock to Counters	Display Resolution
Pin 16	Pin 17		
0	0	100Hz	0.01sec
0	1	10Hz	0.1 sec
1	0	1Hz	1 sec
1	1	External	—

Table III. Divide Scaler Code

Divide Scalers			Modulo							
			Counter 1				Counter 2			
Pin			Digit				Digit			
1	2	3	4	3	2	1	4	3	2	1
0	0	0	10	10	10	10	10	10	10	10
1	0	0	6	10	10	10	6	10	10	10
0	1	0	10	6	10	10	10	6	10	10
1	1	0	10	10	6	10	10	10	6	10
0	0	1	10	10	10	10	10	10	10	10
1	0	1	10	10	10	10	6	10	10	10
0	1	1	10	10	10	10	10	6	10	10
1	1	1	10	10	10	10	10	10	6	10

A zero indicates that the pin is left floating (or connected to V_{DD}); a one indicates that the pin is connected to V_{SS}.

Press the SS switch to initiate a sequence of timing series. Press the SS switch again to end a serial (functions 1, 2, 3, 5) and simultaneously initiate a new serial while freezing the display (function 3), or to freeze the display during a continuous count sequence (function 4).

Press the SS switch a third time to initiate a new timing serial (functions 1, 2, 3, 5) or to update the display during a continuous count sequence (function 4). Subsequent presses of the SS switch will repeat the action described above.

Press the LC switch to display a continuing, undisplayed count (functions 3 and 4). Press the FE switch to end a sequence. A final press of the SS switch at the end of a sequence is required to display total elapsed time (functions 1, 3, 5) or total accumulated time (function 2). Subsequent presses of the SS switch after the end of a sequence simply repeat the display of the final serial time, then the total elapsed or total accumulated time.

The operations which may be performed in each function are shown in the flow charts of *Figures 3* through *8*. The first line of type in each PROCESS rectangle indicates a switch or the display upon which an action may be performed. The second line of type indicates the position in which the switch must be placed or the action to be performed. The parallelograms in the flow charts indicate points at which a DECISION must be made. The operation of each function is detailed in the first article of this series.

To operate the timer in function 6, rotate the F switch to function 6, place the C switch in the CCE position, and press the R switch. The display will show four zeros when the R switch is pressed.

The count-up time is programmed into the timer by pressing D1 through D4, one switch at a time, until the desired count-up time appears in the display.

After digit programming, place the ARE switch in the ON position if automatic resetting is desired. The initial press of the SS switch will cause the display to blank, then to indicate the count-up to the programmed time. During the up-count the CA3059 will be enabled, allowing the appliance to be turned on. When the count-up reaches the programmed time, the comparator output will go from 0 volts to 8.4 volts. At this time the CA3059 will be inhibited, and the appliance will turn off. Pressing the R switch any time after the digits have been programmed causes the comparator and counter 2 to reset. Switching the C switch to OFF causes the comparator output pin to go to V_{DD} as long as it is OFF. If the C switch is again placed in the CCE position (before the R switch is pressed), the comparator output pin will go back to V_{SS}. Of course, any time the FE switch is pressed the comparator output will go to V_{SS}.

If the ARE switch is ON, the count-up sequence may be repeated by pressing the SS switch again. Nothing need be changed until it is necessary to reprogram the digits. When reprogramming is necessary, simply change the time shown in the display to the new time, with the ARE switch in the OFF position, using the digit programming switches. Then press the SS switch to start the up-count. If the ARE switch is OFF, it is necessary to press the reset before starting a new count-up.

To operate the timer in function 7, rotate the F switch to function 7, place the ARE switch in the OFF position, place the C switch in the PE position, and press the R switch. The count-down time is programmed into the timer by pressing D1 through D4, one switch at a time, until the desired count-down time appears in the display. The C switch must then be placed in the CCE position.

Pressing the SS switch will cause counter 1 to begin its down-count from the programmed time to "0000" and will cause the CA3059 to be enabled, turning on the appliance as in function 6. When counter 1 reaches "0000" the CA3059 will be inhibited, turning the appliance off. The down-count is displayed, and may be halted at any time by pressing the FE switch; the down-count may not be resumed. Pressing the R switch any time after digit programming will reset counter 1.

When using function 7, the comparator must be disabled and the R switch must be pressed before digit programming. Then the comparator must be enabled. This is unlike function 6, in which digit programming is allowed at any time, regardless of the state of the comparator. In addition, the ARE switch must not be used in function 7.

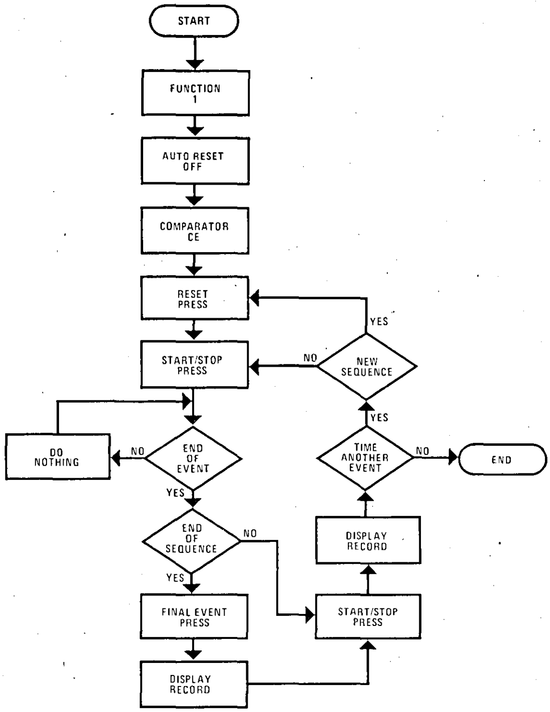


Figure 3. Functions 1 and 2. Pressing START/STOP after FINAL EVENT has been pressed gives Total Elapsed Time in Function 1, Total Accumulated Time in Function 2.

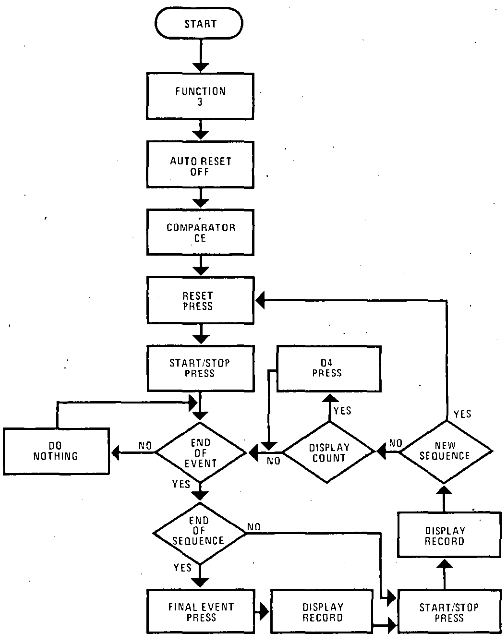


Figure 4. Function 3. Pressing START/STOP after FINAL EVENT has been pressed gives Total Accumulated Time.

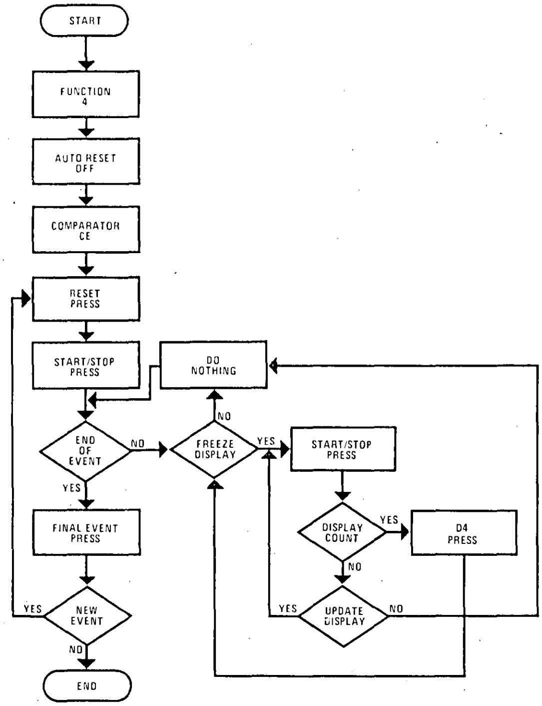


Figure 5. Function 4.

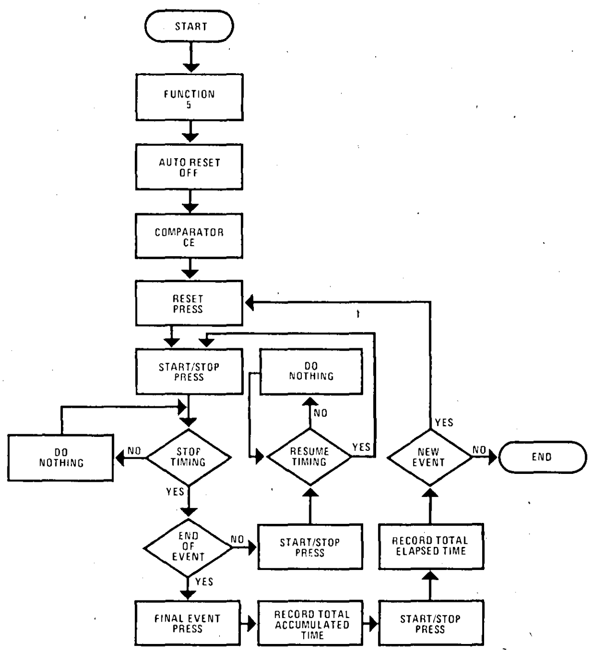


Figure 6. Function 5.

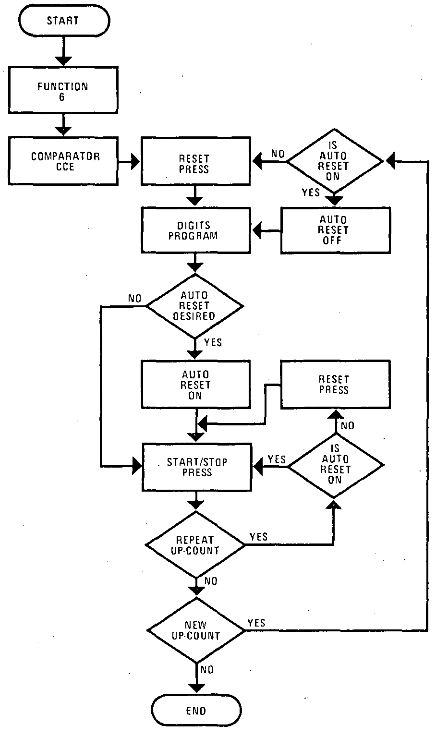


Figure 7. Function 6.

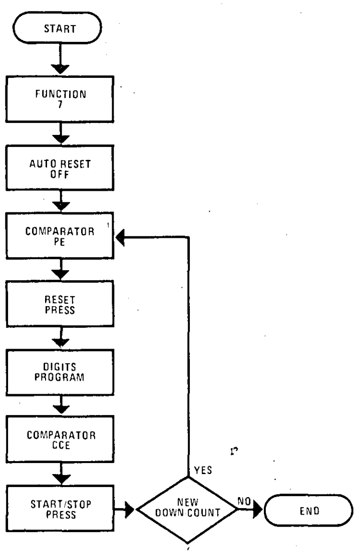


Figure 8. Function 7.

interfacing the stopwatch/timer with an appliance circuit

There are many ways to interface the comparator output with an appliance control circuit. One method of interfacing the MM5865 with an appliance control circuit is shown enclosed in dotted lines in *Figure 2*. *Figure 2* is the schematic diagram of the stopwatch/timer.

The 74C02 has been included as the interfacing element between the comparator output pin and the trigger circuit of a triac. *Figure 9* is a detailed schematic of the 74C02 connections which form a NOR latch.

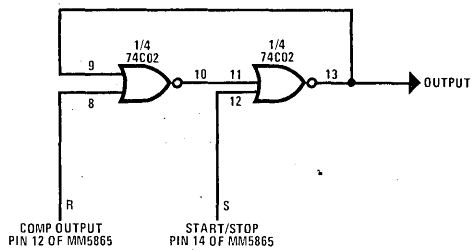


Figure 9. Detail of the 74C02 NOR Latch. The latch interfaces the MM5865 to the CA3059.

The appliance control circuit does not cause RFI because the triac is triggered by a zero-voltage switch. Triac firing can be inhibited by the application of a positive (up to 10V) voltage to pin 1 of the CA3059.

When power is initially applied to the stopwatch/timer the S and R inputs of the latch are both "0." When the R switch is pressed, the output of the latch will go to V_{SS}, inhibiting the CA3059 pulses to the triac.

When the SS switch is pressed (after digit programming) the output of the latch will go to V_{DD} and the CA3059 will be enabled, turning on the appliance. As the programmed time is reached by counter 2 of the MM5865 (function 6), or as counter 1 reaches "0000" (function 7), the comparator output will go to V_{SS}, the output of the latch will go to V_{SS}, and the CA3059 will be inhibited, turning off the appliance.

The inhibit level provided by the latch may be removed from the CA3059 by opening the Appliance Enable Switch. This allows the appliance to be turned on for adjustments. For example, when the timer is used with an enlarger, the Appliance Enable Switch permits enabling of the enlarger lamp for focusing and magnification adjustments.

The output of the latch is connected to the appliance control circuit via a tape recorder cable which plugs into a jack mounted at the rear of the stopwatch/timer case and a jack mounted on the appliance control circuit housing. The housing for the appliance control circuit should also have a socket into which the appliance may be plugged, unless a direct connection is desired.

As shown in *Figure 2*, the appliance control circuit consists of a triac and its trigger circuit. When the CA3059 zero voltage switch is enabled, the trigger circuit applies a brief gate signal to the triac for every alternation of the AC line voltage. After the triac is turned on by the gate signal, it remains on for the complete half cycle until the zero-crossing point is reached at the end of the alternation. The appliance receives the full AC line voltage under these conditions.

If the NOR latch inhibits the trigger circuit while the triac is conducting, the triac cuts off when the line voltage approaches zero. It remains off until another gate signal is applied. Therefore, the NOR latch controls the AC input to the appliance.

With the heat sink specified the triac can safely handle appliances rated up to 100 watts (0.83 Amp). For greater appliance loads a larger heat sink should be used. The specified triac is able to handle appliance loads up to 10 Amps. Of course, the fuse must be large enough to handle the current drawn by the appliance. Use a fast blow fuse if possible.

construction

The printed circuit board was designed specifically for the James Electronics' instrument/clock case only after assurance that the company has a permanent source for the cases; however, the board may be mounted in any case of sufficient size.

Because the layout of the PC board requires that some traces be proximate, the board must be inspected while it is being etched. During these inspections proper resolution of the traces is maintained, if necessary, by rinsing the board in water and carefully scraping the photoresist from any copper which forms a short circuit between adjacent traces. The scraping is done best with an X-Acto blade. Etching should be continued with frequent inspections.

If the exposure time, the amount of light, and the development time are exactly correct, trace resolution is usually not a problem. However, it is difficult to compute and control these variables without performing many experiments. The inspection method described above can save many boards which otherwise would be lost because of trace resolution defects.

In addition to the care which must be given to the PC board during the etching process, excessive solder should be avoided when soldering to the pads. In case of difficulty with timer operation during the checkout procedure, suspect the board immediately.

Furthermore, no thought should be given to the idea of not using sockets for the integrated circuits. James Electronics has four socket styles. All are adequate except the wire wrap sockets. (The diameter of the wire wrap leads is too large.) However, it is easier to insert and remove ICs from the standard tin and gold sockets.

The drilling guides shown in *Figure 10* indicate all drill sizes for the parts shown in the parts list. Every effort has been made to allow the board to accommodate a variety of components. For this reason, there are extra pads and punch guides on the drilling guides. Refer also to the component layouts shown in *Figure 11*. The boards may be prepared using the X1 positives shown in *Figure 12*.

The bottom half of the James case should be prepared for the board by removing the 6 plastic pegs at the front of the case if they are present. The pegs may be removed by grasping them in the jaws of a long-nose pliers and shaking them from side to side while pulling on the pliers.

The earphone socket should be drilled out from the outside of the bottom half of the case with a 31/64-inch drill bit. This will allow a 7-function rotary switch to be mounted in the right hand (facing the display) corner of the rear section of the top half of the case. When doing this, first press the bit to the 3/8-inch hole in the bottom half of the case, *then* turn on the drill. The bit should slice the earphone socket off with 4 or 5 turns of the chuck.

FIG. 10A

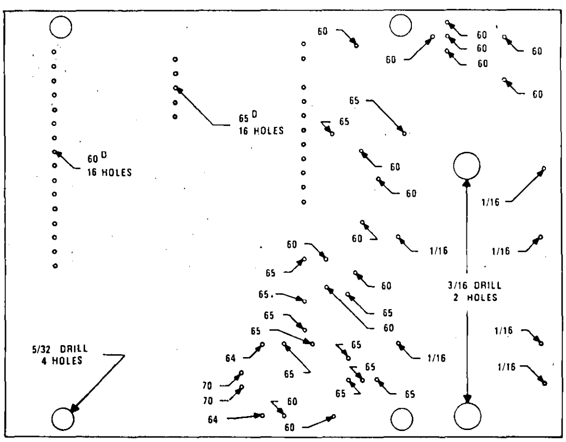


FIG. 10B

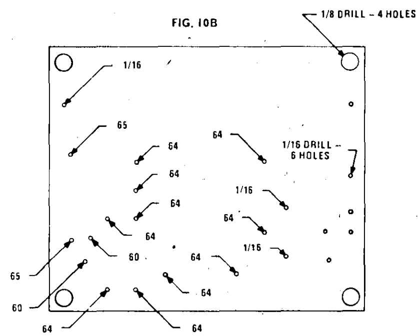


Figure 10. Drilling Guides for the Printed Circuit Boards. a) Drill sizes and hole locations for the Stopwatch/Timer PC board. b) Drill sizes and hole locations for the appliance control circuit. Dimensions are in inches.

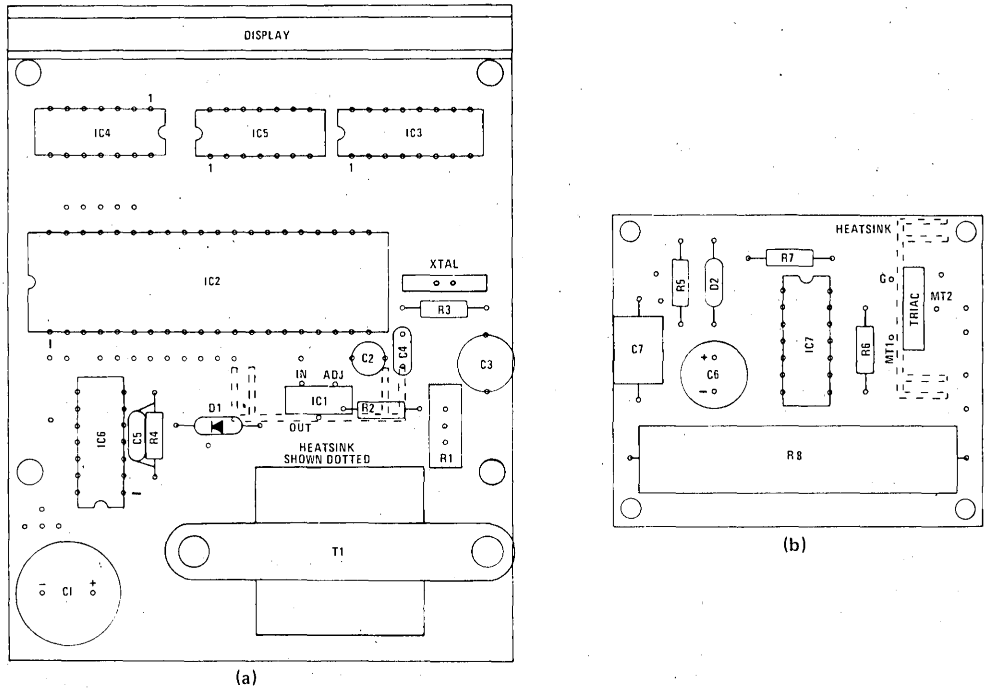


Figure 11. Printed Circuit Board Component Layouts. a) Layout for the Stopwatch/Timer PC board. b) Layout for the Appliance Control PC board. (Approximately 4/5 size shown).

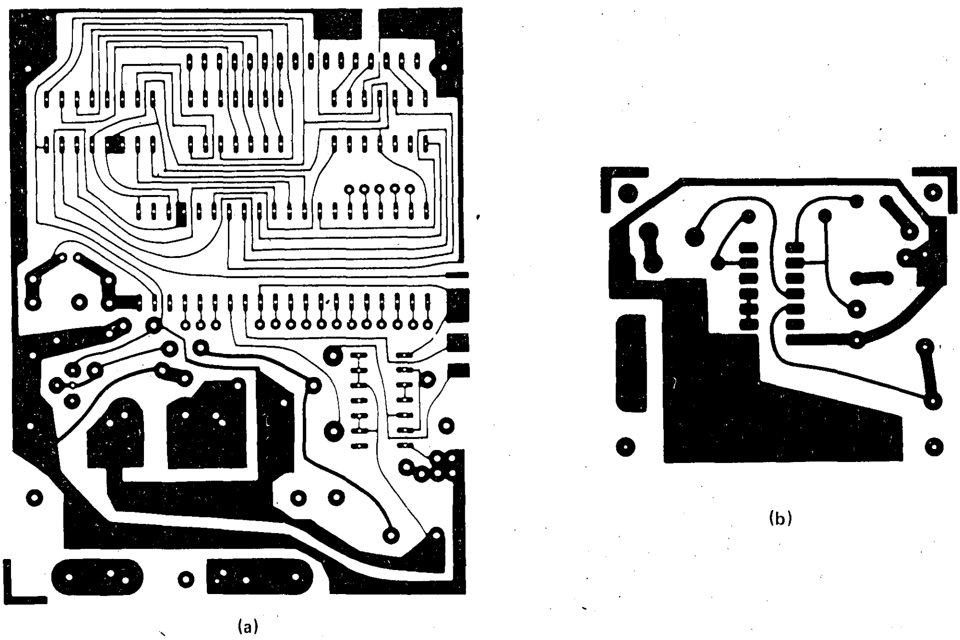


Figure 12. Positives for the Printed Circuit Boards. a) Positive for the Stopwatch/Timer. b) Positive for the Appliance Control circuit. (Approximately 4/5 size shown).

The center portion of the top half of the case has been designed for a switch assembly composed of three push-button switches and one slide switch. The assembly is made of calculator-type switches and a flex-circuit; however, James Electronics provides neither the switches nor the flex-circuit.

Figure 13a shows the layout of the flex-circuit; *Figure 13b* is a view of the flex-circuit after it has been folded over the thin plastic insulator which is shown in *Figure 13c*. The insulator must be oriented so that the circular cutouts are between the two sets of four copper hexagons. The copper trace through each hexagon forms one contact of a SPST switch.

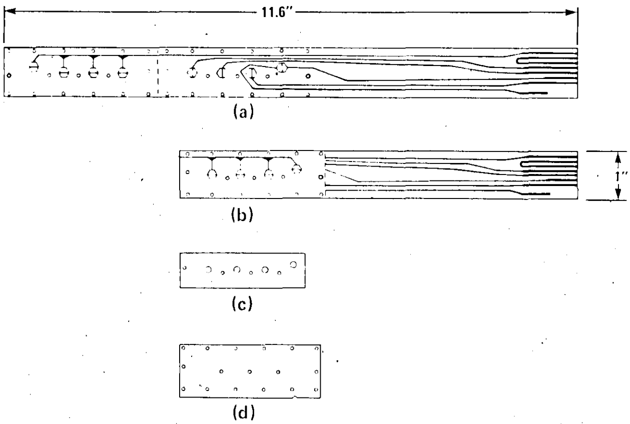


Figure 13. Flex-Circuit Assembly. a) Layout of the flex-circuit. b) Layout of the flex-circuit after it has been folded to form the contacts of three SPST momentary pushbutton switches and one SPST slide switch. c) Thin plastic insulator which must be inserted between the folded portions of the flex-circuit. d) Plastic cover which fits over the flex-circuit assembly to hold it in place in the top of the case.

If the automatic reset feature for function 6 is to be included, cut the slide switch hexagon connection to V_{SS} as shown in *Figure 14* and cut a little square piece from the thin insulator. This small square should be just large enough to allow a solder connection to be made between the trace going to the slide switch hexagon and the trace going to the FE switch hexagon. To solder the traces together, pretin both traces slightly, fold the flex-circuit as shown in *Figure 13b*, and apply a small soldering iron tip to the trace going to the slide switch hexagon at a point above the insulator cutout.

The switches should then be placed in the top of the box in the spaces provided. The flex-circuit is then placed over the switches. Finally, the plastic cover fits over the entire assembly as shown in *Figure 15*. Holding the plastic cover firmly in place, touch a clean soldering iron tip to each of the plastic pegs protruding through the holes in the plastic switch assembly cover until the assembly cover is sealed to the top of the case. Cut the single tall plastic peg to the rear of the switch assembly cutout if there is one.

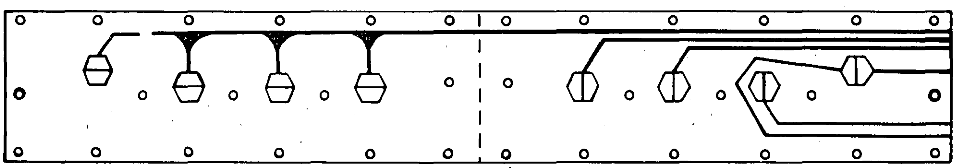


Figure 14. Full-Size Partial Drawing of the Flex-Circuit Layout Showing the Trace which Must be Cut if the Auto Reset Option is Desired.

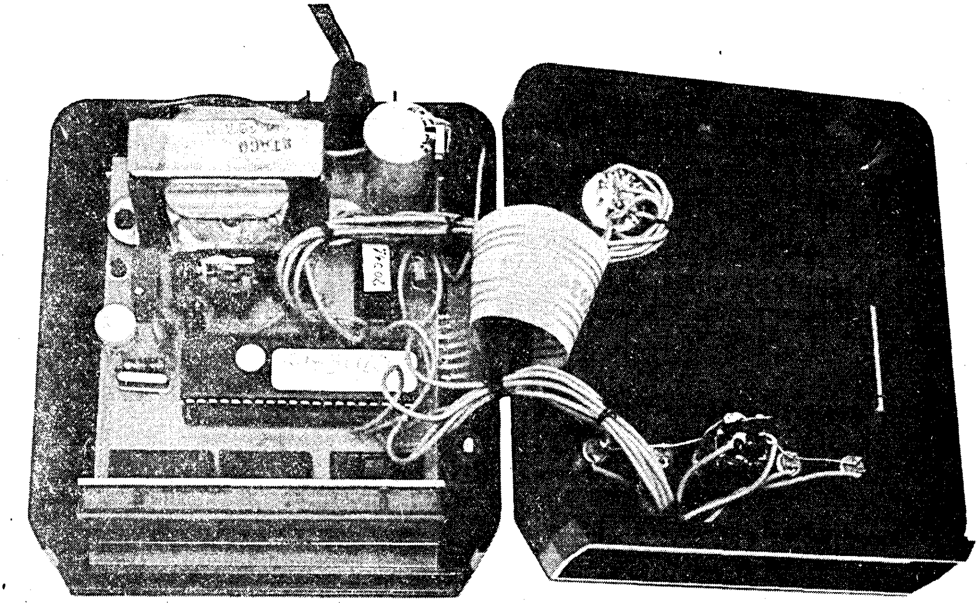


Figure 15. Photograph Showing the Internal Construction of the Stopwatch/Timer. Note how flex-circuit runs from the top of the case to the trace-side of the printed circuit board.

Drill the holes for the rotary function switch, the comparator switch, and the four programming switches as shown in the drilling guide of *Figure 16*. The drilling guide must be modified as shown in *Figure 17* if the Centralab PS-101 switch is used. The holes for the rotary switch must be marked and drilled precisely. In addition, if the Centralab PS-101 switch is used the filter capacitor, C1, must lie on its side to make room for the function switch. Mounting the top of the case to the bottom is easier if the Centralab PS-101 switch is used. If desired, a jack may be mounted in the bottom half of the case in the right hand rear corner, behind C1, to provide a quick connection to an enlarger or appliance control circuit. The fit will be tight, but a miniature jack can be mounted without much difficulty. This completes the case preparations.

Before parts are mounted to the PC board, the fit of the board to the case should be checked. It may be necessary to adjust the mounting holes slightly with a small round file. Try not to completely break the traces surrounding the mounting holes. There are six mounting holes in the PC board. These holes match six plastic pegs in the bottom of the case. Two of the pegs are to be inserted through the transformer mounting flanges if a transformer of the correct size is used. If the Radio Shack, or some other transformer which does not fit precisely, is used, it may not be possible to fit the pegs through the transformer mounting flanges.

After the IC sockets are mounted, the transformer and C1 should be mounted. If the Centralab PS-101 switch is used, the filter capacitor should be attached to the board

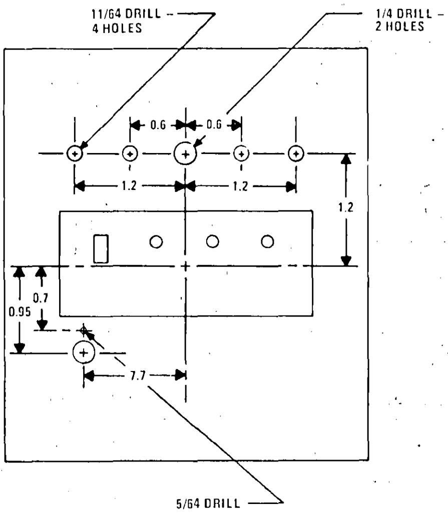


Figure 16. Drilling Guide for the Case Top if the MRC-1-10 Rotary Function Switch is Used. (Dimensions in inches.)

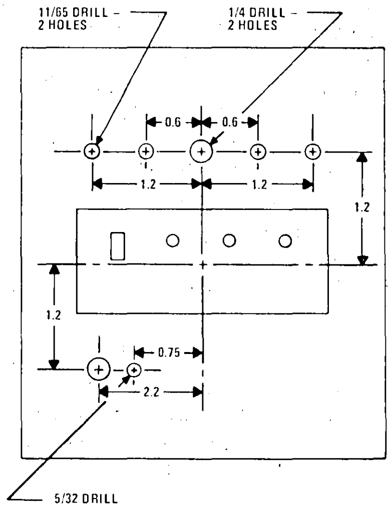


Figure 17. Drilling Guide for the Case Top if the PS-101 Rotary Function Switch is Used. (Dimensions in inches.)

with leads that are long enough to permit the capacitor to lie on its side. The diameter of C1 must not be greater than 0.7 inch and its length must not be greater than 1.2 inch.

The display mounting pins should be soldered to the display before the display is mounted to the board. Be careful not to lift the display pin pads when soldering.

Wires must be soldered to the board and connected to the switches mounted to the top of the case. Refer to the wiring diagram shown in *Figure 18*.

Wire jumpers may be used to program the display resolution and the modulo of the counters using the charts shown in *Tables I* and *II*. The connections shown in *Figure 2* cause the display to read in tens of minutes, minutes, tens of seconds, and seconds; maximum time is 99 min 59 sec. A pad which allows a connection to an external clock is available at pin 15 of the MM5865.

After all components have been mounted and all wire connections have been made, proceed to the preliminary checkout and adjustments section before applying power to the board.

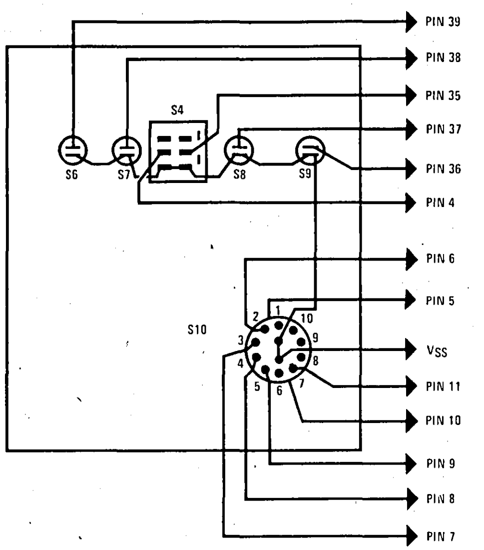


Figure 18. Wiring Diagram for the Switches Mounted in the Case Top.

preliminary checkout and adjustments

The following tests and adjustments should be carefully completed before power is applied to the stopwatch/timer or the appliance control circuit.

Rotate the F switch to function 7, place the ARE switch in the OFF position, place the C switch in the CCE position, and disconnect the tape recorder plug from the jack at the rear of the stopwatch/timer case. Adjust R1 for minimum resistance. Do not connect any appliance to the appliance control circuit, but do place a fuse in the fuse holder.

Measure the following points for the indicated amount of resistance:

1. Across the stopwatch/timer line cord plug > 50 ohms
2. Across C1, with VOM on X1K scale and common probe to V_{DD}, > 5k ohms, after C1 charges
3. Across R1 < 15 ohms
4. Across C2 > 100 ohms
5. Across the appliance control circuit line plug > 10k ohms

If these values of resistance cannot be found at the points indicated, check the PC boards for opens or shorts as necessary. Then, with a VOM connected across C2, apply power to the stopwatch/timer; the VOM should read slightly more than 1 volt. Increase the resistance of R1 until the VOM reads 8.4 volts. Slightly under 8.4 volts is better than slightly over. Pressing the reset switch should cause "0000" to appear on the display, unless the display already reads "0000."

If the display is blank or indicates only one or two zeroes, the oscillator is probably not oscillating. Rotate C3, 360 degrees if necessary, while observing the display. If the display still fails to respond properly, check the voltage at pin 20 of the MM5865; it is very close to 6 volts when the oscillator is functioning.

After oscillation has been confirmed the display should be examined for segment and digit defects. If any segment or digit does not appear in the display (The g segment does not appear when the display reads all zeroes.), the board and the display mounting pin connections must be checked.

When handling the stopwatch/timer before it is mounted in its case, extreme care must be used to not break the connections between the flex-circuit and the printed circuit board. However, these connections need not be made until the oscillator and display have been checked out.

After the oscillator and display checkout, the frequency of the oscillator should be adjusted to the crystal frequency using C3. Then the board may be placed in the bottom of the case. The balance of the preliminary checkout consists of stepping through the operational flow diagrams in *Figures 3-8*; a VOM should be connected to the output jack during the functions 6 and 7 checkout. If any of the switches under the flip cover fail to respond, check to see if the flex-circuit is broken at the point where it connects to the board.

final assembly and checkout

The board may be fastened to the bottom of the case by forcing #6 tinnerman nuts over the plastic pegs which appear through the holes indicated in *Figure 11*. This may be done easily with a 5/16-inch nutdriver. Then force the line cord in the cutout provided.

The top of the case may then be carefully fitted to the bottom, with the red plastic filter partially in place.

A slot in each half of the case retains the filter when the case halves are fastened. If the MRC-1-10 switch is used, the fit will be tight because of its proximity to C1. The cutout for the line cord in the top half of the case must be forced over the line cord.

Once the two halves are fitted properly, fasten them together using the four screws provided with the case. Install the rubber feet and proceed with the final checkout.

The final checkout is a repetition of the operational checks using the flow diagrams. Each option at each decision point in every flow diagram should be exercised.

resolution and accuracy

If a crystal is used for the time base of the stopwatch/timer, the accuracy of the displayed count will, of course, depend upon the particular crystal used. In addition, because the MM5865 begins to count on the leading edge of the start/stop pulse, the width of this pulse becomes important when the event time is very short.

For example, when coupling the timer to an appliance, if the width of the start/stop pulse is longer than the event time, the appliance will not turn off at the end of the programmed time.

This is why C5 and R4 have been included. Together they insure that the start/stop pulse will not be longer than 0.01 second. This pulse width should be adequate for most users. C5 and R4 may be omitted if the length of time the start/stop switch is to be held closed will always be less than any timed event. When C5 and R4 are omitted, the SS switch simply connects to V_{SS}.

As to crystal accuracy, the stopwatch/timer will lose 0.001 sec/sec if a 32.768kHz crystal is used instead of a 32.8kHz crystal. This should be insignificant for most users.

Also, the display resolutions which may be programmed by on board jumper wires will be adequate for most users. *Figure 2* illustrates the connections to the MM5865 which will cause the display to read in tens of minutes, minutes, tens of seconds, and seconds.

When it becomes desirable to achieve a display resolution which allows the timing of events that are hours in length, it is necessary to provide the MM5865 with an external time base. This may be done by cascading two MM5865s or by using a simple timing circuit built around an LM555 timer or a digital clock. *Figure 19* shows how an MM5315 digital clock may be used as a time base for the MM5865. The MM5315 itself uses the line frequency as a time base. The MM5315 is shown as it would be connected for a 60Hz line frequency.

When an external time base is provided for the MM5865 in this manner, an external multiplexer must also be provided. The oscillator formed with the 74C14 supplies the desired multiplex frequency as shown in *Figure 19.*

A final note: Unless the start pulse is externally synchronized to the clock (available at pin 15 of the MM5865, if the internal oscillator is used), the amount of time which will elapse between the arrival of the start pulse at pin 14 of the MM5865 and the appearance of the first digit in the display will not be equal to the programmed display resolution. It is possible to develop a start pulse that is synchronized to the clock using an MM74C221 Dual Monostable Multivibrator as shown in *Figure 20.* The time constant of R1 - C1 should be equal to the display resolution, the time constant of R2 - C2 should be less than the programmed display resolution, and the time constant of R3 - C3 should be less than the time constant of R2 - C2.

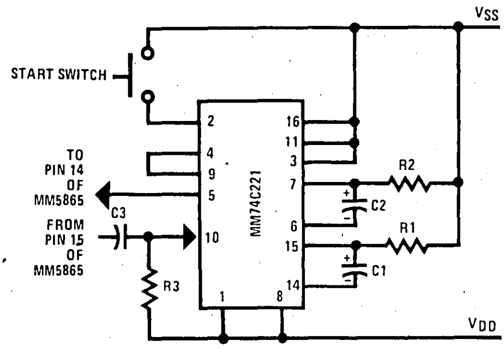


Figure 20. Start-Pulse Synchronizer. Time constant of R1 - C1 = display resolution. Time constant of R2 - C2 < display resolution. Time constant of R3 - C3 < time constant of R2 - C2.

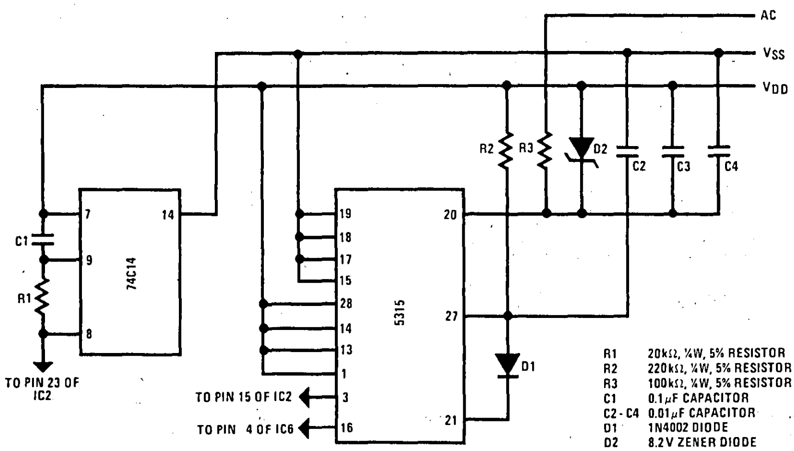


Figure 19. Using an MM5315 Digital Clock and an External Multiplexer to Provide an External Time Base for the MM5865 to Generate a Display Resolution of 1 Minute.

PARTS LIST

R1	5kΩ trimpot
R2	240Ω, ¼W, 5% resistor
R3	20MΩ, ¼W, 5% resistor
R4	1MΩ, ¼W, 5% resistor
R5	100kΩ, ¼W, 5% resistor
R6	5.1kΩ, ¼W, 5% resistor
R7	4.7kΩ, ¼W, 5% resistor
R8	10kΩ, 1W, 5% resistor
C1	470 - 1000mF, 25V capacitor
C2	10mF, 25WV$_{DC}$ solid tantalum capacitor
C3	6 - 25pF variable capacitor. Sprague QT1-18 4 - 30pF may be used.
C4	25 - 27pF, disc ceramic capacitor
C5	0.01mF disc ceramic capacitor
C6	100mF, 25WV$_{DC}$ capacitor
C7	0.05mF, 200WV$_{DC}$ capacitor
D_1, D_2	IN4003
T1	10 - 16.5V$_{AC}$ @ 300mA transformer
IC1	LM317T voltage regulator
IC2	MM5865 universal timer
IC3	CD14511 decoder/driver/latch
IC4	DS8877 or DS75492 digit driver
IC5	RA07 - 150 resistor array
IC6	74C02 quad 2-input NOR gate
IC7	CA3059 zero voltage switch
Triac	HEP R1723
F1	1A fast or normal blow fuse
XTAL	32.8kHz crystal (32.768kHz can be substituted. Timer will lose about 35 sec in 11 hr 20 min of use.)
S1, S3, S5	SPST, NO, momentary pushbutton switches; part of flex-circuit switch assembly.
S2	SPST slide switch; part of flex-circuit switch assembly.
S4	DPDT, center OFF toggle switch
S6 - S9	SPST, NO, momentary pushbutton switches
S10	7 - 12 position rotary switch – Centralab PS-101 or Alcoswitch MRC-1-10.
S11	SPST toggle switch
S12	SPDT toggle switch (optional)
Display	National Semiconductor NSB5411 4-digit multiplexed display.
Heat Sink	TO-220 heat sink. Two needed.
Misc.	16 display mounting pins (strip of 16 pins); 1 case; Clock/Instrument (available from James Electronics); 1 flex-circuit; 1 flex-circuit insulator; 2 Tinnerman nuts, #6; fuseholder; appliance control box, #LMB C.R.-234; 115V$_{AC}$ chassis mounting socket; miniature jacks; phone cable (shielded); IC sockets.

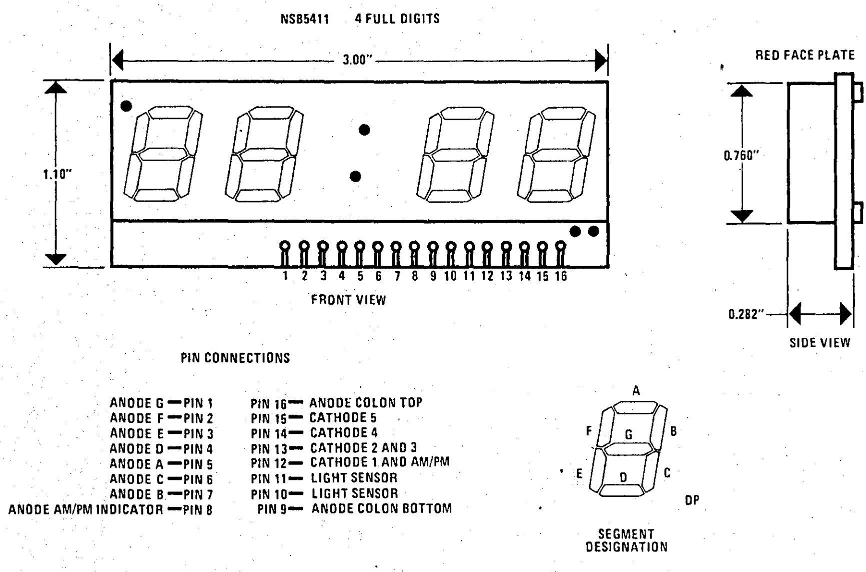


Figure 21. Dimensions and Pin Connections for the National Semiconductor Corp. NSB5411 4-Digit, Multiplexed Display. Mounting holes for a photocell are included on the display board.

SECTION 3
ELECTRONIC ORGAN CIRCUITS

Electronic Organ Circuits

MM5554 frequency divider

general description

The MM5554 frequency divider provides six stages of binary division to produce six octave-related outputs of an electronic musical instrument tone generator. Each divider stage consists of an asynchronous, DC-coupled flip-flop. The six stages are internally connected in cascades of one, two, and three flip-flops. Each flip-flop drives a push-pull output buffer, which provides low output impedance in both logic states. Two of the internal cascades also provide trigger outputs for use in cascading the divider stages. The timing diagram shown results from connecting the same input trigger to all three inputs.

The MM5554 complements the MM5555/MM5556 chromatic frequency generator; output characteristics and power supply requirements are compatible. The MM5554 is packaged in a 14-lead dual-in-line package.

features

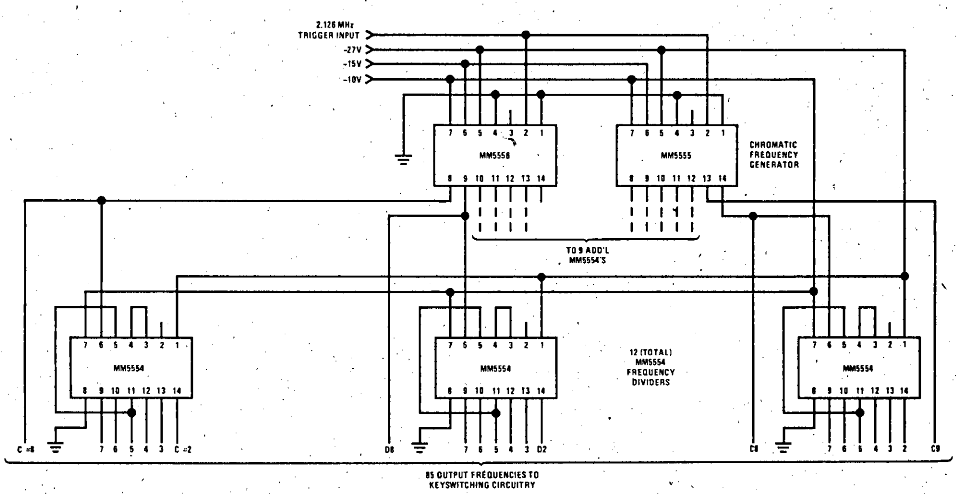
- 0 to 500 kHz toggle frequency
- 1–, 2–, 3–stage partitioning

applications

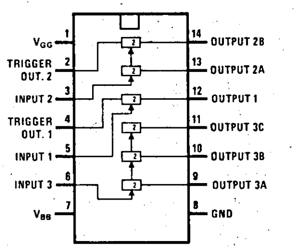
- Electronic organs
- Electronic music synthesizers
- Musical instrument tuners

logic and connection diagrams

Typical Organ Tone Generator



Dual-In-Line Package



TOP VIEW

Order Number MM5554N
See Package 18

absolute maximum ratings

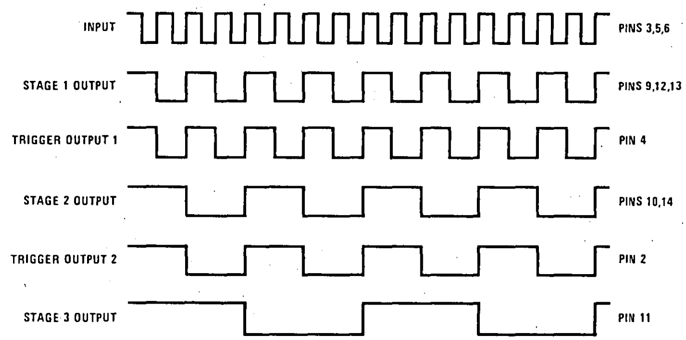
Logic Supply Voltage (V_{GG})	V_{SS} + 0.3V to V_{SS} − 33V
Buffer Supply Voltage (V_{BB})	V_{SS} + 0.3V to V_{SS} − 18V
Trigger Input Voltage (V_{IT})	V_{SS} + 0.3V to V_{SS} − 18V
Power Dissipation (P_D)	250 mW
Storage Temperature (T_S)	−55°C to +100°C
Operating Temperature (T_A)	0°C to +70°C

electrical characteristics

T_A within operating range (V_{GG} = −27 ±2V, V_{BB} = −10 ± .5V), unless otherwise noted.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Trigger Inputs:					
Frequency	f_{IT}	DC		500	kHz
Rise and Fall Times (10% to 90%)	t_r, t_f			25	ns
Pulse Width (at 90%)	pw	1			µs
Logical High Level	V_{ITH}	−2.5		V_{SS}	V
Logical Low Level	V_{ITL}	−18.0		−7.0	V
Leakage Current	I_{ITL}			1.0	µA
Trigger Outputs: (loaded 10M ohm to ground, T_A = 25°C)					
Logical High Level	V_{OTH}	−1.5		0	V
Logical Low Level	V_{OTL}			−10	V
Buffer Outputs: (loaded 20K ohm to ground and 20K ohm to V_{BB}, T_A = 25°C)					
Logical High Level	V_{OH}	−1.0		0	V
Logical Low Level	V_{OL}	V_{BB}		−8.0	V
Supply Currents: (no output loads, T_A = 25°C)					
Logic Supply	I_{GG}			4	mA
Buffer Supply	I_{BB}			20	µA

timing diagram



3

Electronic Organ Circuits

MM5555, MM5556 chromatic frequency generators

general description

The National Semiconductor MM5555, MM5556 chromatic frequency generators are MOS/LSI frequency synthesizers designed to generate musical frequencies. The circuits provide thirteen semitone outputs, fully spanning the equal tempered octave. The divisors have been carefully selected to offer excellent tuning accuracy and to eliminate any "locked" (just-intoned) fifths. Output characteristics are fully compatible with the MM5554 Frequency Divider. The MM5555 or MM5556 is packaged in a 14-lead dual-in-line package.

features

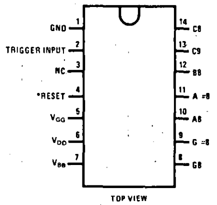
- Single-phase squarewave input
- 7 kHz to 2.2 MHz input frequency
- Accuracy of 0.5129 cent

applications

- Electronic organs
- Electronic music synthesizers
- Musical instrument tuners

connection and logic diagrams

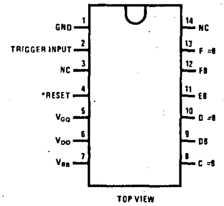
Dual-In-Line Package



Order Number MM5555N
See Package 18

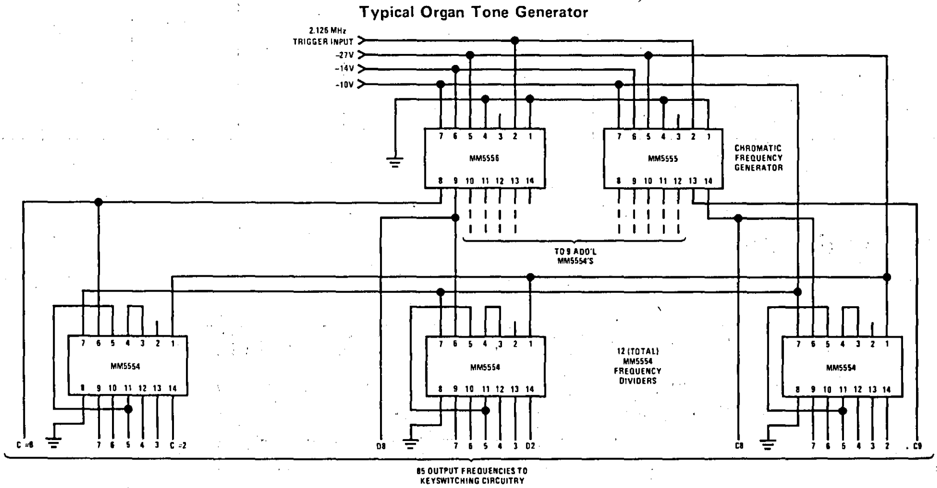
*Used only for testing. Pin 4 is normally grounded.

Dual-In-Line Package



Order Number MM5556N
See Package 18

Typical Organ Tone Generator



output details (2.12608–MHz input)

MM5555

NOTE	DIVISOR	OUTPUT FREQUENCY	E.T.S. FREQUENCY	CENT ERROR
C8	508	4185.20	4186.01	-0.326
C9	254	8370.39	8372.02	-0.326
B8	269	7903.64	7902.13	+0.321
A ♯8	285	7459.93	7458.62	+0.295
A8	302	7040.00	7040.00	0
G ♯8	320	6644.00	6644.88	-0.221
G8	339	6271.62	6271.93	-0.082

MM5556

NOTE	DIVISOR	OUTPUT FREQUENCY	E.T.S. FREQUENCY	CENT ERROR
F ♯8	359	5922.23	5919.91	+0.658
F8	380.5	5587.60	5587.65	-0.017
E8	403	5275.63	5274.04	+0.507
D ♯8	427	4979.11	4978.03	+0.364
D8	452.5	4698.52	4698.64	-0.042
C ♯8	479.5	4433.95	4434.92	-0.368

absolute maximum ratings

Clock Generator Voltage (V_{GG})	0.3V to −33V
Logic Supply Voltage (V_{DD})	0.3V to −25V
Buffer Supply Voltage (V_{BB})	0.3V to −18V
Trigger Input Voltage (V_{IT})	0.3V to −18V
Power Dissipation (P_D)	800 mW
Storage Temperature (T_S)	−55°C to +100°C
Operating Temperature (T_A)	0°C to +70°C

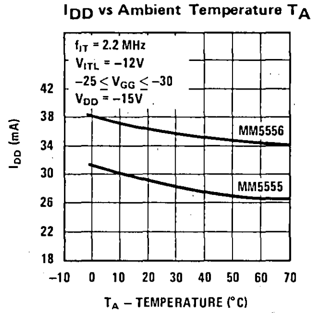
electrical characteristics

T_A within operating range (V_{GG} = −27V ±2V, V_{DD} = −14V ±1V, V_{BB} = −10V ±0.5V), unless otherwise noted.

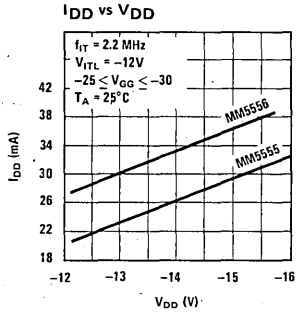
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Trigger Input					
Frequency	f_{IT}	7.0	2126.08	2200	kHz
Capacitance	C_{IT}			7.0	pF/pkg
Rise and Fall Times (10% to 90% at 2.2 MHz)	t_r, t_f			30	ns
Pulse Width (at −5.0V)	pw	0.4T		0.6T	$(T = \frac{1}{f_{IT}})$
Logical High Level	V_{ITH}	−2.0	0	0.3	V
Logical Low Level	V_{ITL}	−16	−10	−8.0	V
Leakage Current	I_{ITL}			1.0	μA
Buffer Outputs: (loaded 20 kΩ to ground and 20 kΩ to V_{BB}, T_A = 25°C)					
Logical High Level	V_{OH}	−1.0		0	V
Logical Low Level	V_{OL}	V_{BB}		−8.0	V
C8 Duty Cycle			50		%
C #8 thru C9 Duty Cycle			30		%
Supply Currents: (no output loads, T_A = 25°C)					
Clock Generator Supply	I_{GG}	1.5		3.5	mA
Logic Supply MM5555	I_{DD}	16		34	mA
Logic Supply MM5556	I_{DD}	22		40	mA
Buffer Supply	I_{BB}			25	μA

typical performance characteristics

I_{DD} vs Ambient Temperature T_A



I_{DD} vs V_{DD}



Electronic Organ Circuits

MM5559 serial-to-parallel converter

general description

The MM5559 serial-to-parallel converter provides 33 bits of conversion in a single package. A serial output facilitates cascading these devices to provide larger conversions.

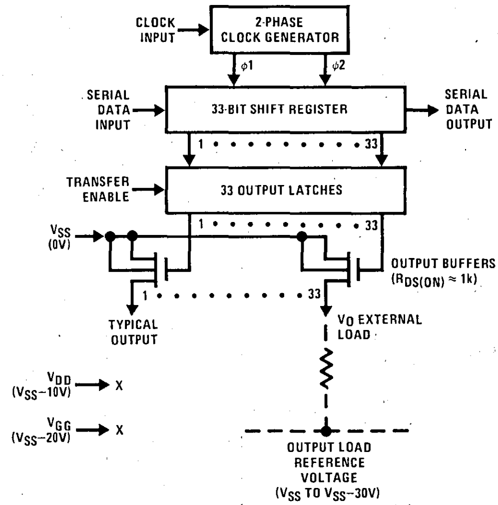
applications

- Matrix displays and printers
- Musical instrument keyboard/tone generator interface controllers

features

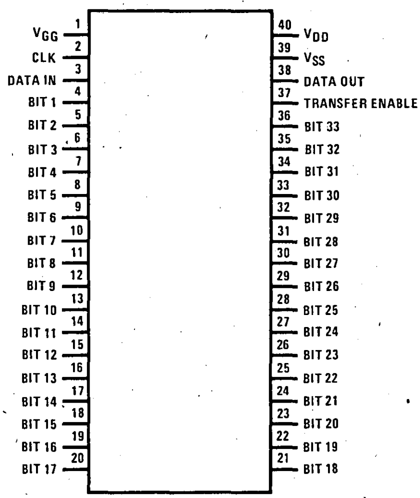
- 33 Parallel outputs
- Serial output
- DC-to-250 kHz operation

logic and connection diagrams



33-Bit Serial-to-Parallel Converter

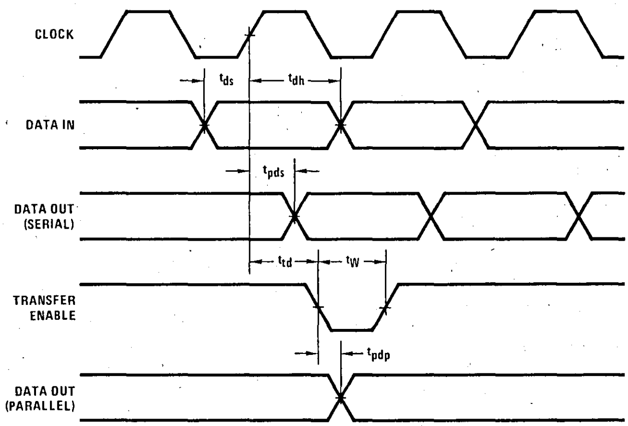
Dual-In-Line Package



TOP VIEW

Order Number MM5559N
See Package 24

timing diagram



absolute maximum ratings

Voltage At Any Pin	V_{SS} + 0.3 to V_{SS} − 25V
Voltage At Any Output Pin	V_{SS} + 0.3 to V_{SS} − 33V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −10V, ±10%, V_{GG} = −20V ±10%, output load reference voltage = 0V to −30V (via external load resistor)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Voltages					
Logic High Level		V_{SS}−2.2		V_{SS}	V
Logic Low Level		V_{SS}−11		V_{SS}−7	V
Clock and Transfer Enable Input Voltages					
Logic High Level		V_{SS}−1.0		V_{SS}	V
Logic Low Level		V_{SS}−11		V_{SS}−8.6	V
Input Capacitance				7	pF
Input Leakage Current	T_A = 25°C, V_{IN} = V_{SS}−11			10	μA
Clock Input Frequency	Duty Cycle = 50%	0		250	kHz
Rise and Fall Times	V_{SS}−2.2 through V_{SS}−8.6			0.2	μs
Transfer Enable Input					
Pulse Width	Time at V_{SS}−8.6	1.6			μs
Rise and Fall Times				0.2	μs
Parallel Outputs					
Output Voltage	I_O = 2 mA	V_{SS}−2			V
Leakage Current	T_A = 25°C, V_O = V_{SS}−30			10	μA
Serial Output Voltages					
Logical High Level	Loaded 56 kΩ to V_{DD}	V_{SS}−2		V_{SS}	V
Logical Low Level	Loaded 560 kΩ to V_{SS}	V_{DD}		V_{SS}−8	V
Power Supply Currents					
Drain Supply, I_{DD}				10	mA
Gate Supply, I_{GG}	(Note 1)		7.5	20	mA

Note 1: The magnitude of I_{GG} is modulated by the parallel output data; the current is inversely proportional to the number of outputs that are high (sourcing current). The typical value of 7.5 mA is representative of an alternating 1's and 0's output pattern.

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ds} Data Setup Time	Referenced from V_{SS} − 7 on Data In to V_{SS} − 8.6 on Clock In	0.4			μs
t_{dh} Data Hold Time		0.2			μs
t_{td} Transfer Delay	Referenced from V_{SS} − 8.6	0.6			μs
t_W Transfer Strobe Width		1.6			μs
Propagation Delay					
t_{pds} Serial	High-to-Low (V_{SS} to V_{DD})	3.0			μs
	Low-to-High	1.2			μs
t_{pdp} Parallel	Low-to-High with 10 kΩ Load	1.2			μs

Electronic Organ Circuits

MM5823, MM5824 frequency dividers

general description

These frequency dividers provide six stages of binary division to produce six octave-related outputs of an electronic musical instrument tone generator. Each divider stage consists of an asynchronous, dc-coupled flip-flop.

The six stages of the MM5823 are internally connected in cascades of two, one, one, and two flip-flops. Each flip-flop drives a push-pull output buffer which provides very low output impedance in both logic states.

The six stages of the MM5824 are internally connected in cascades of one, two and three flip-flops. Each flip-flop drives a push-pull output buffer which provides very low output impedance in both logic states. Two of the internal cascades also provide trigger outputs for use in cascading the divider stages.

The timing diagram shown results from connecting the same input trigger to all three inputs.

The MM5823 and MM5824 complement the MM5832, MM5833 and MM5555, MM5556 chromatic frequency generators; output characteristics and power supply requirements are compatible. The MM5823 and MM5824 are packaged in a 14-lead dual-in-line package.

features

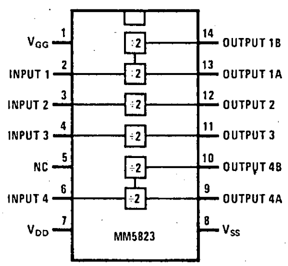
- 0 to 100 kHz toggle frequency
- 1, 2, 3 or 2, 1, 1, 2 stage partitioning

applications

- Electronic organs
- Electronic music synthesizers
- Musical instrument tuners

connection diagrams

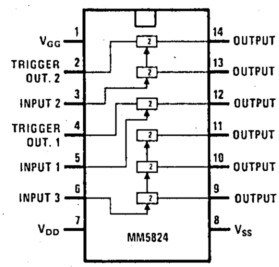
Dual-In-Line Package



TOP VIEW

Order Number MM5823N
See Package 18

Dual-In-Line Package



TOP VIEW

Order Number MM5824N
See Package 18

absolute maximum ratings

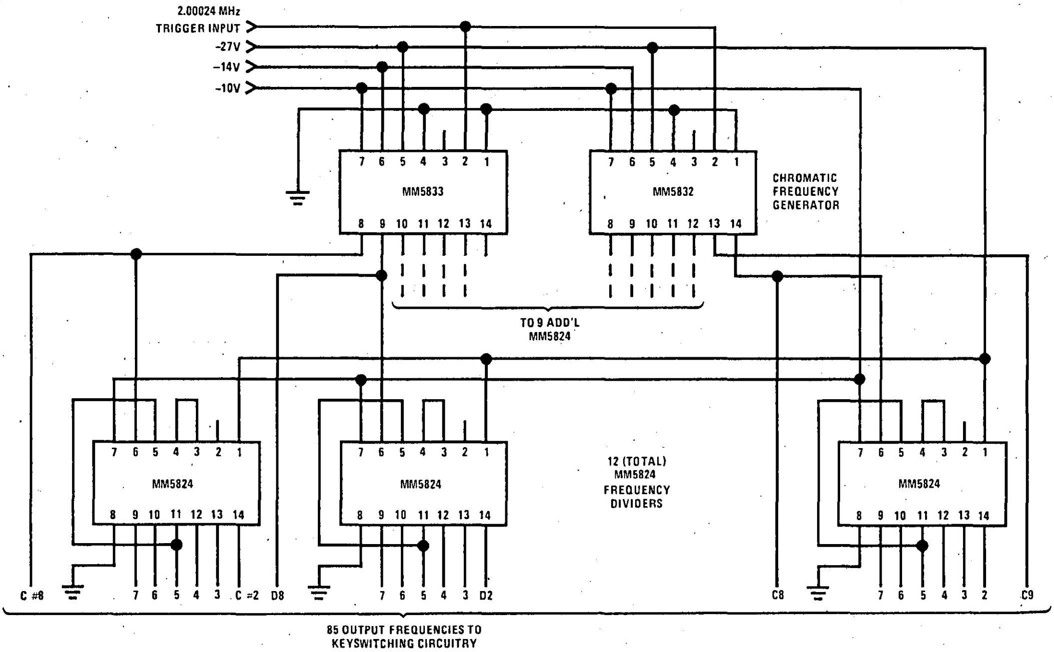
Logic Supply Voltage (V_{GG})	0.3V to −30V
Buffer Supply Voltage (V_{DD})	0.3V to −18V
Trigger Input Voltage (V_{IT})	0.3V to −25V
Power Dissipation (P_D)	250 mW
Storage Temperature (T_S)	−55°C to +150°C
Operating Temperature (T_A)	0°C to +70°C

electrical characteristics

T_A within operating range (V_{GG} = −27 ±1V, V_{DD} = −11.5 ±0.5V, V_{SS} = 0V), unless otherwise noted.

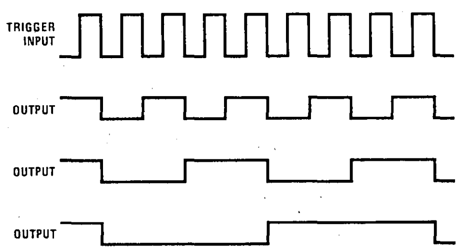
PARAMETER	MIN	TYP	MAX	UNITS
Inputs:				
Frequency (f_{IT})	DC		100	kHz
Rise and Fall Times (10% to 90%) (t_r, t_f)			25	μs
Pulse Width (at 90%) (pw)	2			μs
Logical High Level (V_{ITH})	−2.0	V_{SS}	0.3	V
Logical Low Level (V_{ITL})	−18	−10	−8.0	V
Leakage Current @ V_{ITL} = −18V (I_{ITL})			1.0	μA
Trigger Outputs: (loaded 10M ohm to ground, T_A = 25°C)				
Logical High Level (V_{OTH})	V_{SS}−1.5		V_{SS}	V
Logical Low Level (V_{OTL})	−18		−10	V
Outputs: (loaded 10k ohm to ground and 10k ohm to V_{DD}, T_A = 25°C)				
Logical High Level (V_{OH})	−0.5		−0.3	V
Logical Low Level (V_{OL})	V_{DD}+0.3		V_{DD}+0.5	V
Supply Currents: (No output loads, T_A = 25°C)				
Logic Supply (I_{GG})		2.0	8.0	mA
Buffer Supply (I_{DD})			20	μA

typical application



Typical Organ Tone Generator

timing diagram



Electronic Organ Circuits

MM5832, MM5833 chromatic frequency generator

general description

The National Semiconductor MM5832, MM5833 chromatic frequency generator is an MOS/LSI frequency synthesizer designed to generate musical frequencies. The circuits provide thirteen semi-tone outputs, fully spanning the equal tempered octave. The divisors have been carefully selected to offer excellent tuning accuracy. Output characteristics are fully compatible with the MM5554, MM5823 and MM5824 Frequency Dividers. The MM5832 or MM5833 is packaged in a 14-lead dual-in-line package.

features

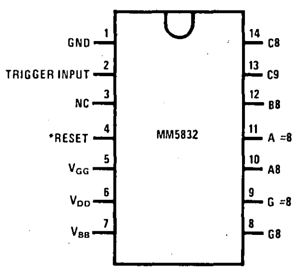
- Single-phase squarewave input
- 7 kHz to 2.1 MHz input frequency
- Maximum error of 1.16 cent

applications

- Celeste tone generator
- Electronic music synthesizers
- Organ tone generators
- Chorus tone generators

connection diagrams

Dual-In-Line Package

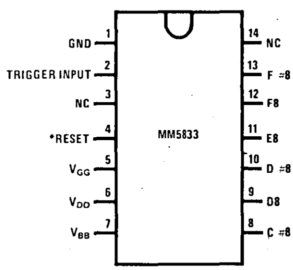


TOP VIEW

Order Number MM5832N
See Package 18

*Used only for testing. Pin 4 is normally grounded.

Dual-In-Line Package



TOP VIEW

Order Number MM5833N
See Package 18

absolute maximum ratings

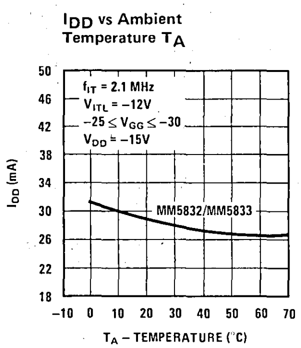
Clock Generator Voltage (V_{GG})	V_{SS} + 0.3V to V_{SS} − 33V
Logic Supply Voltage (V_{DD})	V_{SS} + 0.3V to V_{SS} − 25V
Buffer Supply Voltage (V_{BB})	V_{SS} + 0.3V to V_{SS} − 18V
Trigger Input Voltage (V_{IT})	V_{SS} + 0.3V to V_{SS} − 18V
Power Dissipation (P_D)	800 mW
Storage Temperature (T_S)	−55°C to +100°C
Operating Temperature (T_A)	0°C to +70°C

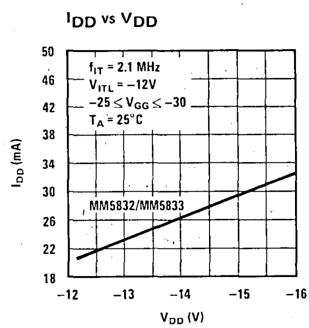
electrical characteristics

T_A within operating range (V_{GG} = −27V ±2V, V_{DD} = −14V ±1V, V_{BB} = −10V ±0.5V, V_{SS} = 0V), unless otherwise noted.

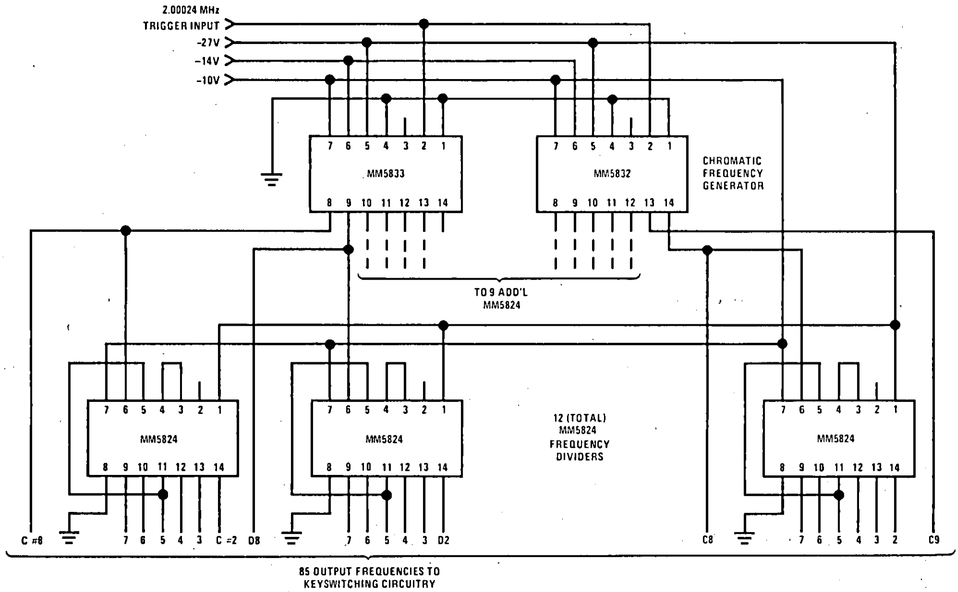
PARAMETER	MIN	TYP	MAX	UNITS
Trigger Input				
Frequency (f_{IT})	7.0	2000.24	2100	kHz
Capacitance (C_{IT})			7.0	pF/pkg
Rise and Fall Times (t_r, t_f) (10% to 90% at 2.1 MHz)			30	ns
Pulse Width (at −5.0V) (pw)	0.4T		0.6T	(T = $1/f_{IT}$)
Logical High Level (V_{ITH})	+0.3	0	−2.0	V
Logical Low Level (V_{ITL})	−16		−8.0	V
Leakage Current (I_{ITL})			1.0	μA
Buffer Outputs: (loaded 20 kΩ to ground and 20 kΩ to V_{BB}, T_A = 25°C)				
Logical High Level (V_{OH})	−2.0		0	V
Logical Low Level (V_{OL})	V_{BB}		−8.0	V
C8 Duty Cycle		50		%
C ≠8 thru C9 Duty Cycle		30		%
Supply Currents: (no output loads, T_A = 25°C)				
Clock Generator Supply (I_{GG})	1.5		3.5	mA
Logic Supply (I_{DD})	16		34	mA
Buffer Supply (I_{BB})			25	μA

typical performance characteristics





typical application



Typical Organ Tone Generator

output details (2.00024 MHz input)

MM5832

NOTE	DIVISOR	OUTPUT FREQUENCY	E.T.S. FREQUENCY	CENT. ERROR
C8	478	4184.61	4186.01	−0.565
C9	239	8369.21	8372.02	−0.565
B8	253	7906.09	7902.13	0.842
A #8	268	7463.58	7458.62	1.119
A8	284	7043.10	7040.00	0.740
G #8	301	6645.32	6644.88	0.112
G8	319	6270.34	6271.93	−0.424

MM5833

NOTE	DIVISOR	OUTPUT FREQUENCY	E.T.S. FREQUENCY	CENT. ERROR
F #8	338	5917.87	5919.91	−0.580
F8	358	5587.26	5587.65	−0.117
E8	379	5277.68	5274.04	1.160
D #8	402	4975.72	4978.03	−0.780
D8	426	4695.40	4698.64	−1.159
C #8	451	4435.12	4434.92	0.076

Electronic Organ Circuits

MM5837 digital noise source

general description

The MM5837 digital noise source is an MOS/MSI pseudo-random sequence generator, designed to produce a broadband white noise signal for audio applications. Unlike traditional semiconductor junction noise sources, the MM5837 provides very uniform noise quality and output amplitude. The shift register starts at a random non-zero state when power is applied. The circuit is packaged in an 8-lead Epoxy-B mini-DIP.

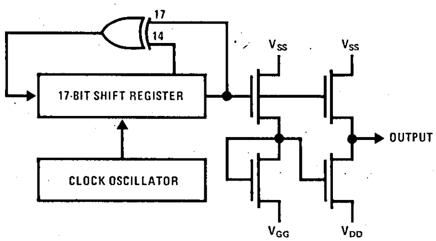
features

- Uniform noise quality
- Uniform noise amplitude
- Eliminates noise preamps
- Self-contained oscillator
- Single component insertion

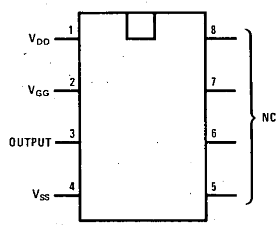
applications

- Electronic musical rhythm instrument sound generators
- Music synthesizer white and pink noise generators
- Room acoustics testing/equalization

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5837N
See Package 17

absolute maximum ratings

Optional Gate Supply Voltage, V_{GG}	V_{SS} − 33V to V_{SS} + 0.3V
Logic Supply Voltage, V_{DD}	V_{SS} − 25V to V_{SS} + 0.3V
Storage Temperature, T_S	−55°C to +100°C
Operating Temperature, T_A	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −14V ±1.0V, V_{GG} = −27V ±2V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output (Loaded 20 kΩ to V_{SS} and 20 kΩ to V_{DD}	T_A = 25°C				
Logical "1" Level		V_{SS}−1.5		V_{SS}	V
Logical "0" Level		V_{DD}		V_{DD}+1.5	V
Logical "0" Level	V_{GG} = −14V ±1V	V_{DD}		V_{DD}+3.5	V
Supply Currents					
I_{DD}	No Output Load	3		8	mA
I_{GG}				7	mA
Half Power Point		24		56	kHz
Cycle Time		1.1		2.4	Sec

3

Electronic Organ Circuits

MM5871 rhythm pattern generator

general description

The MM5871 rhythm pattern generator is an MOS/LSI circuit, fabricated with P-channel enhancement-mode and ion-implanted, depletion-mode devices. The PLA implementation is programmed to produce 6 rhythm patterns which may be combined in any manner and provide 5 instrument-trigger outputs. Trigger output pulse width is determined by an external RC network, *(Figure 1)*. A similar network, including a potentiometer, determines tempo of the on-chip oscillator. This circuit is packaged in a 16-pin Epoxy-B DIP, *(Figure 2)*. *Figure 3* illustrates the standard pattern coding. *Figure 4* is a programming worksheet for ordering custom patterns.

features

- On-chip tempo oscillator
- Variable output pulse width
- 6 rhythm patterns
- 5 trigger outputs
- Flexible supply voltages
- Low power dissipation

standard patterns

- Waltz (3/4)
- Swing (3/4)
- Country/Western (3/4)
- March (4/4)
- Latin (4/4)
- Rock (4/4)

applications

- Electronic organs
- Portable rhythm boxes

block and connection diagrams

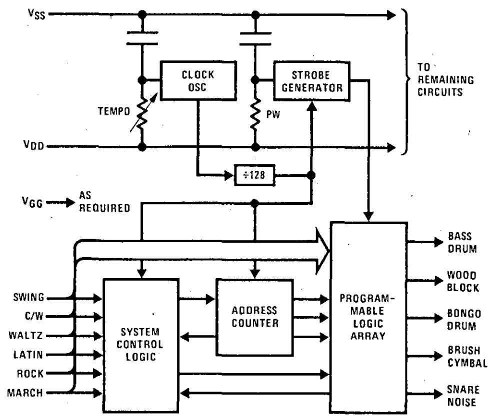
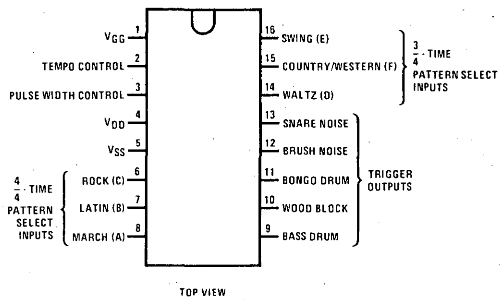


FIGURE 1.

Dual-In-Line Package



Order Number MM5871N
See Package 19

FIGURE 2.

absolute maximum ratings

		MIN	MAX	UNITS
Supply Voltages	V_{GG}	−33	0.3	V
	V_{DD}	−22	0.3	V
Input Voltage		−18	0.3	V
Storage Temperature	T_S	−55	100	°C
Operating Temperature	T_A	0	70	°C
Lead Temperature (Soldering, 10 seconds)			300	°C

electrical characteristics

T_A within operating range, V_{SS} = 0V, V_{DD} = −14V ±2V, V_{GG} = −27V ±2V, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tempo Control Input	C to V_{SS} = 0.0056 μF				
Minimum Tempo	R to V_{DD} = 1.1 MΩ	≤2.7			bps
Maximum Tempo	R to V_{DD} = 120 kΩ (Note 1)			≥27	bps
Pulse Width Control Input	C to V_{SS} = 0.0056 μF				
	R to V_{DD} = 100 kΩ, (Note 1)	2	3	4	ms
Select Inputs					
Logic High Level	(Active Level)	V_{SS}−0.75	V_{SS}	V_{SS}+0.3	V
Input Current	V_{IH} = V_{SS}			0.2	mA
Logic Low Level		V_{DD}	V_{DD}	V_{DD}+0.75	V
Trigger Outputs					
Logic High Level	(Active Level) (w/20k to V_{DD})	V_{SS}−0.37		V_{SS}+0.3	V
Leakage Current	V_{OL} = V_{DD}, (Note 2)			−10	μA
Supply Currents	(No Output Loads)				
	I_{DD}			20	mA
	I_{GG}			5	mA

Note 1: Both the Tempo Control and Pulse Width Control inputs utilize external RC networks to determine tempo and strobe pulse width. Additionally, these parameters are affected by the $V_{SS} - V_{DD}$ voltage. Therefore, for these tests the RC values apply to $V_{SS} - V_{DD}$ = −14 ±0.5 volts.

Note 2: All trigger outputs are open-drain transistors. The active output level is therefore high, and the off condition is high impedance as indicated by the specified leakage current.

3

Device: MM5871

Customer:

Pattern: AA (Standard).

	DEVICE PIN		16									15									14								
	Rhythm Name		Swing									Country/Western									Waltz								
	Rhythm Space		E									F									D								
	Time		3/4									3/4									3/4								
	Instrument Trigger Outputs:																												
			Counts									Counts									Counts								
Device Pin	Instrument Name	Card Address	0	1	2	3	4	5	5	5	5	0	1	2	3	4	5	5	5	5	0	1	2	3	4	5	5	5	5
9	Bass Drum	A0	X									X					X				X								
10	Block	A1																											
11	Bongo	A2				X									X								X		X				
12	Brush	A3	X					X				X	X	X		X	X				X								
13	Snare	A4				X									X								X		X				
		A5																											
		A6																											
	“1” Totals		2	0	0	2	0	1	0	0	0	2	1	1	2	1	2	0	0	0	2	0	2	0	2	0	0	0	0

	DEVICE PIN		7								6								8								
	Rhythm Name		Latin								Rock								March								
	Rhythm Space		B								C								A								
	Time		4/4								4/4								4/4								
	Instrument Trigger Outputs:																										
			Counts								Counts								Counts								“1”
Device Pin	Instrument Name	Card Address	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	Totals
9	Bass Drum	A0	X				X			X	X			X	X				X				X				12
10	Block	A1	X			X			X																		3
11	Bongo	A2							X	X			X				X	X			X				X	X	12
12	Brush	A3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X				X				26
13	Snare	A4											X				X	X			X				X	X	10
		A5																									0
		A6																									0
	“1” Totals		3	1	1	2	2	1	3	3	2	1	3	2	2	1	3	3	2	0	2	0	2	0	2	2	63

Note 1: In this chart, “X” represents the presence of a gate in the spot.

Note 2: “X” = 1; negative logic.

FIGURE 3. Standard Pattern Coding

Device: MM5871

Customer:

Pattern:

	DEVICE PIN		16									15									14								
	Rhythm Name																												
	Rhythm Space		E									F									D								
	Time		3/4									3/4									3/4								
	Instrument Trigger Outputs:																												
			Counts									Counts									Counts								
Device Pin	Instrument Name	Card Address	0	1	2	3	4	5	5	5	5	0	1	2	3	4	5	5	5	5	0	1	2	3	4	5	5	5	5
9	Bass Drum	A0																											
10	Block	A1																											
11	Bongo	A2																											
12	Brush	A3																											
13	Snare	A4																											
		A5																											
		A6																											
	“1” Totals								0	0	0							0	0	0							0	0	0

	DEVICE PIN		7								6								8								
	Rhythm Name																										
	Rhythm Space		B								C								A								
	Time		4/4								4/4								4/4								
	Instrument Trigger Outputs:																										
			Counts								Counts								Counts								“1”
Device Pin	Instrument Name	Card Address	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	Totals
9	Bass Drum	A0																									
10	Block	A1																									
11	Bongo	A2																									
12	Brush	A3																									
13	Snare	A4																									
		A5																									0
		A6																									0
	“1” Totals																										

Note 1: Combination counts of 5 on 3/4 time are not programmable, i.e., no gates in “555” section.

Note 2: In this chart, “X” represents the presence of a gate in the spot.

Note 3: “X” = 1; negative logic.

FIGURE 4. Programming Worksheet For Ordering Custom Patterns

Electronic Organ Circuits

MM5891 MOS top octave frequency generator

general description

The MM5891 top octave frequency generator is an MOS/LSI frequency synthesizer designed to generate musical frequencies. The circuit provides 13 semitone outputs, which encompass the equal tempered octave. The divisor set approximates the $\sqrt[12]{2}$ semitone interval to an accuracy of ±1.16 cent.

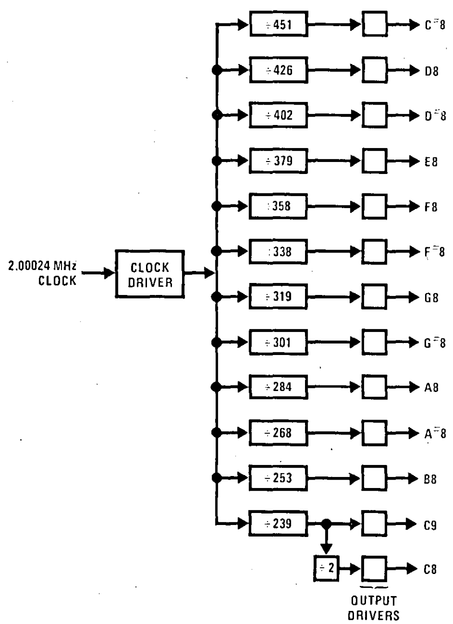
Low threshold voltage enhancement-mode and depletion-mode devices are utilized; the MM5891 therefore operates from a single, wide range power supply. Power dissipation is less than 600 mW. The circuit is packaged in the 16-pin Epoxy B dual-in-line package.

Potential RFI emission of the input clock is minimized by positioning the clock input between the V_{SS} and V_{DD} pins. Chip layout also isolates the clock and output buffer areas. Additionally, the outputs are slew-limited to reduce RF spectral content of the output signals.

features

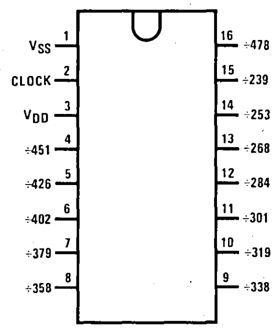
- Single power supply
- Broad supply voltage operating range
- Low power dissipation
- High output drive capability
  - MM5891AA–50% output duty cycle
  - MM5891AB–30% output duty cycle

block diagram



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5891N
See Package 19

absolute maximum ratings

Voltage on Any Pin Relative to V_{SS}	+0.3V to −20V
Operating Temperature (Ambient)	0°C to +50°C
Storage Temperature (Ambient)	−40°C to +100°C

recommended operating conditions

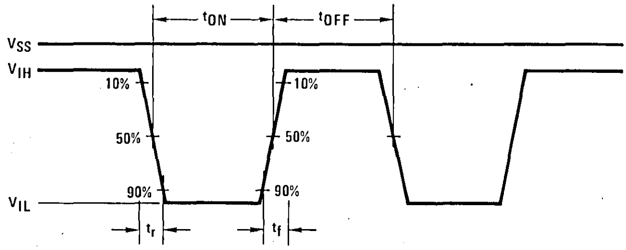
($0°C \leq T_A \leq 50°C$)

	MIN	MAX	UNITS
Supply Voltage (V_{SS})	0	0	V
Supply Voltage (V_{DD})	−11.0	−16.0	V

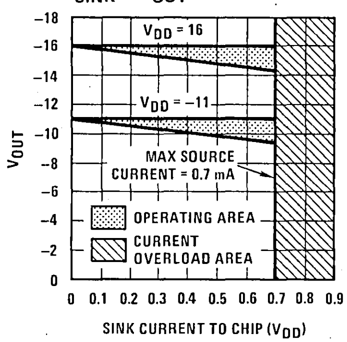
electrical characteristics $0°C \leq T_A \leq 50°C$; $V_{SS} = 0$, $V_{DD} = -11$ to $-16V$ unless otherwise specified

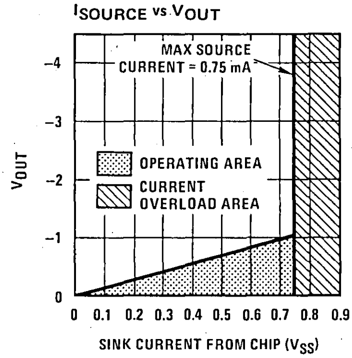
	PARAMETER	MIN	TYP	MAX	UNITS
V_{IH}	Input Clock, High	0		−1.0	V
V_{IL}	Input Clock, Low	V_{DD}+1.0		V_{DD}	V
f_I	Input Clock Frequency	100	2000.240	2500	kHz
t_r, t_f	Input Clock Rise and Fall Times, 10% to 90% at 2.5 MHz			30	ns
t_{ON}, t_{OFF}	Input Clock "ON" and "OFF" Times at 2.5 MHz		200		ns
C_I	Input Capacitance		5	10	pF
V_{OL}	Output, Low at 0.70 mA	V_{DD}+1.5		V_{DD}	V
V_{OH}	Output, High at 0.75 mA	V_{SS}−1.0		V_{SS}	V
t_{ro}, t_{fo}	Output Rise and Fall Times, 500 pF Load	250		2500	ns
t_{ON}	Output Duty Cycle				
	MM5891AA		50		%
	MM5891AB– (Pin 16, 50%)		30		%
I_{DD}	Supply Current		24	37	mA

switching time waveform



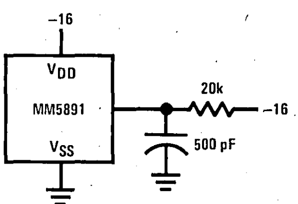
typical performance characteristics



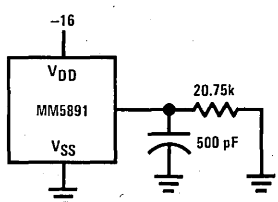


output loading

Output Loading t_{fo} Test



Output Loading t_{ro} Test



3

SECTION 4
TV CIRCUITS

MM5318 TV digital clock

general description

The MM5318 digital clock is a monolithic MOS integrated circuit utilizing P-channel low-threshold, enhancement mode devices. The circuit contains all the logic required to give a 4 or 6-digit, 12 or 24-hour display from a 50 or 60 Hz input. The digit select inputs enable an external digital system to select which digit will be available at the BCD and 7-segment outputs. An example of this is a television receiver. By using the MM5318 with a MM5841 in a television receiver, the time of day can be displayed with the TV channel selected on the TV screen. The MM5841 determines what digit it requires from the MM5318, where on the screen it will be displayed and presents the information to the TV receiver. The MM5318 is packaged in a 28-lead dual-in-line package.

features

- 12 or 24 hour operation
- 50 or 60 Hz input
- 4 or 6-digit display
- BCD outputs
- Digit select inputs
- Leading zero blanking in 12-hour mode
- High output currents for simplified display interfacing
- Single power supply

applications

- TV time display
- Computer real time clock

block and connection diagrams

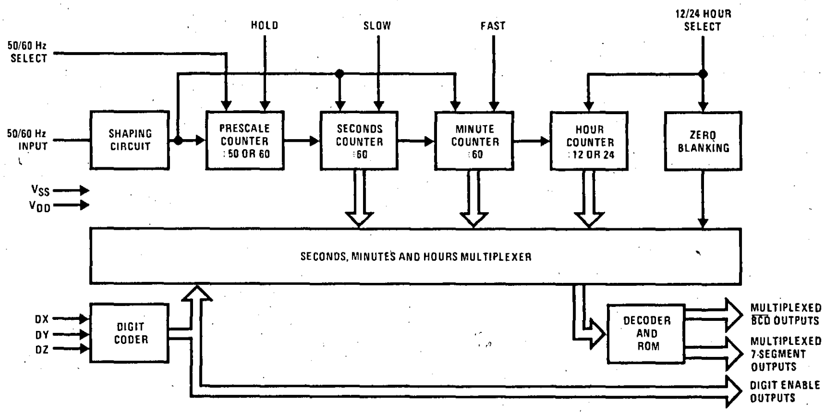
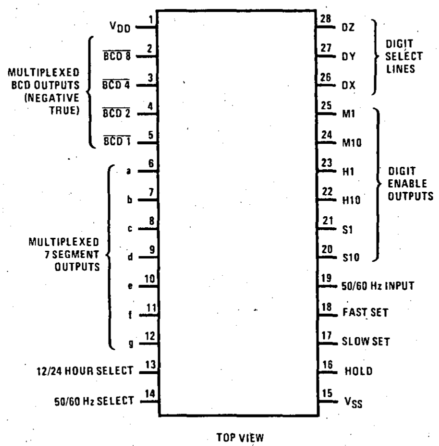


FIGURE 1. Block Diagram

Dual-In-Line Package



Order Number MM5318N
See Package 23

FIGURE 2. Connection Diagram

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 20V
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{DD} = 0V, V_{SS} = 14V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	V_{SS} = 14V (No External Output Loads All $\overline{BCD}$ Outputs at Logical "1")	4		30	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logic "1"		V_{SS}−2	V_{SS}	V_{SS}	V
Logic "0"		−2	V_{DD}	4	V
Digit Select Input Delay		400		2000	ns
All Logic Inputs	Internal 20k, Resistor to V_{SS}				
Logic "1"	(Except Digit Select Inputs)	V_{SS}−1	V_{SS}	V_{SS}	V
Logic "0"		−2	V_{DD}	4	V
$\overline{BCD}$ Outputs					
Logic "1"	Output Voltage at V_{SS} − 2	2		10	mA source
Logic "0"	0.01 mA Sink	V_{DD}		0.3	V
7-Segment Outputs	Output Voltage at V_{SS} − 2				
Logic "1"		2		20	mA source
Logic "0"				0.01	mA leakage
Digit Enable Outputs					
Logic "1"	0.1 mA Source	V_{SS}−0.3		V_{SS}	V
Logic "0"	Output Voltage at V_{SS} − 2	5		15	mA sink

functional description

A block diagram of the MM5318 digital clock is shown in *Figure 1*. A connection diagram is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 1*.

50 or 60 Hz Drive: This input is applied to a Schmitt Trigger shaping circuit which provides approximately 5V of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 6* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 Hz timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal 20k pull-up resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal 20 kΩ pull-up resistors provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function. Fast set advances hours information at one hour per second and slow set advances minutes information at one minute per second. The Hold Input stops the clock to the prescale counter.

12 or 24 Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format. The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal 20 kΩ pull-up) selects the 24-hour format.

Digital Select Inputs (DX, DY, DZ): These three inputs are used to determine what digit will be displayed, Table I shows the code for each digit. A logic "1" is when the pin is held to V_{SS}. When the pin is tied to V_{DD}, a logic "0" results.

Output Circuits: *Figure 3* illustrates the circuit used for the $\overline{BCD}$ outputs. *Figure 4* shows the circuit used for the 7-segment outputs. The digit enables output circuit is shown in *Figure 5*. *Figures 6 and 7* illustrate typical applications for the MM5318.

functional description (Continued)

TABLE I. Digit Select Code

DIGIT SELECT LINES	DIGIT DISPLAYED							
	S1	S10	*	M1	M10	*	H1	H10
DX	1	0	0	1	1	0	0	1
DY	1	1	0	0	0	0	1	1
DZ	0	0	0	0	1	1	1	1

*Output blanked

output circuits

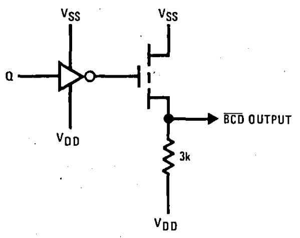


FIGURE 3. $\overline{BCD}$ Output Circuit

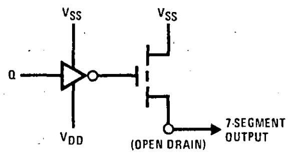


FIGURE 4. 7-Segment Output Circuit

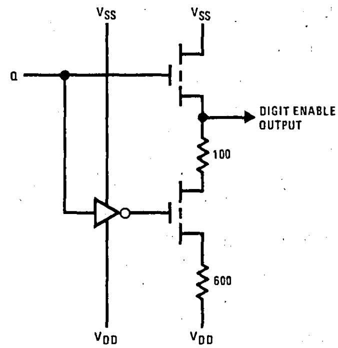


FIGURE 5. Digit Enable Output Circuit

typical applications

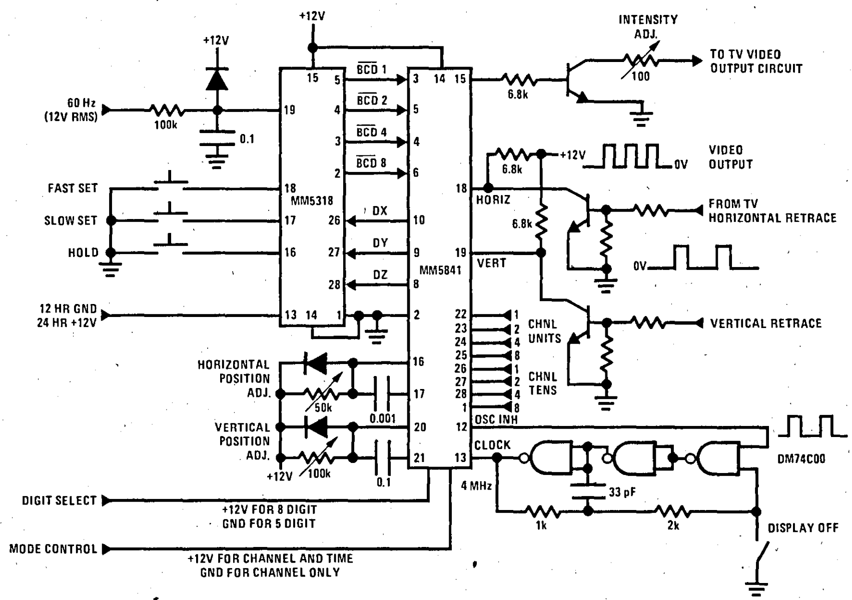


FIGURE 6. TV Channel and Time Display

typical applications (Continued)

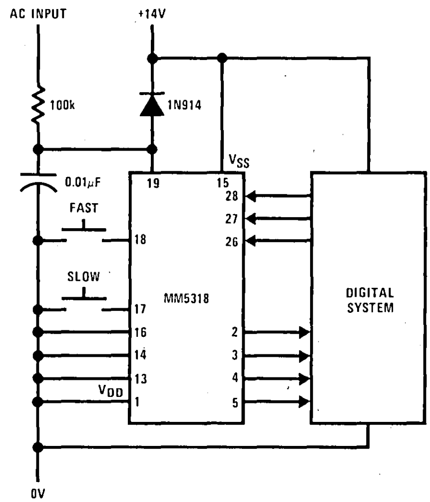


FIGURE 7. Typical Application

TV Circuits

MM5320 TV camera sync generator

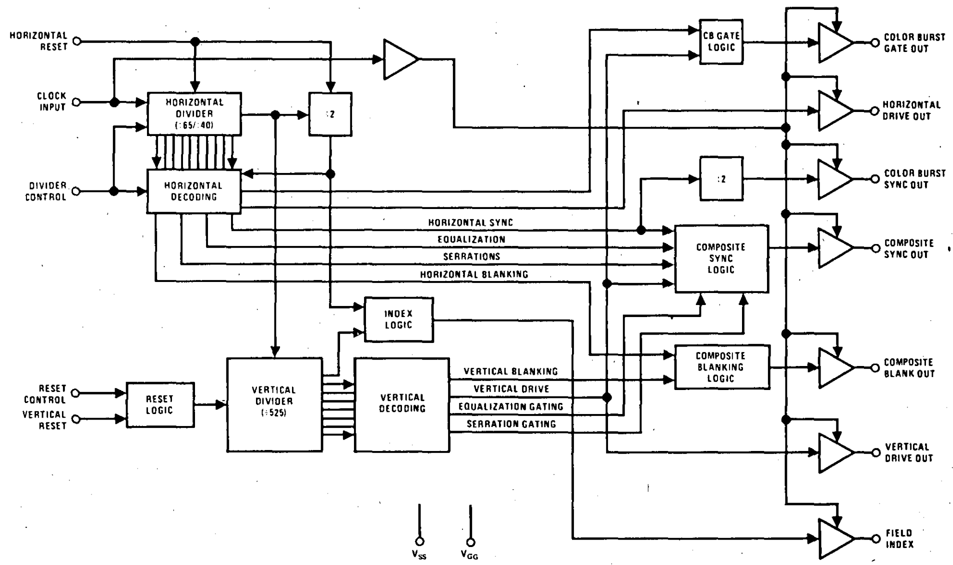
general description

The MM5320 TV camera sync generator is an MOS, P-channel enhancement mode, LSI chip designed to supply the basic sync functions for either color or monochrome 525 line/60 Hz interlaced camera and video recorder applications. Required power supplies are +5V and −12V, or any other combination resulting in V_{SS} − 17V. All inputs and outputs are TTL compatible without the use of external components.

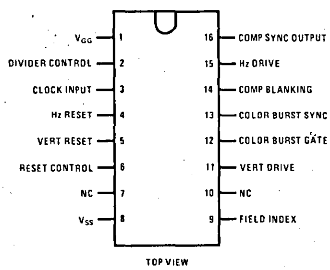
features

- Multi-function gen lock input provides flexible control of multiple camera installations
- 16 lead dual-in-line package
- Conventional +5V, −12V power supplies
- Uses 2.04545 MHz or 1.260 MHz input reference
- Field indexing provided for VTR applications
- Color burst gate and sync allow stable color operation

logic and connection diagrams



Dual-In-Line Package



Order Number MM5320N
See Package 19

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} − 22
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Levels					
Logical High Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} − 18		V_{SS} − 4.2	V
Input Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Input Capacitance	V_{IN} = 0V, f = 1.0 MHz, All Other Pins GND (Note 1)		3.5	6.0	pF
Clock Input Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND			0.5	μA
Clock Input Capacitance	V_{IN} = 0V, f = 1.0 MHz, All Other Pins GND (Note 1)		3.5	6.0	pF
Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Logical Low Level (V_{OL})	MOS Load	V_{SS} − 12.5	V_{SS} − 11	V_{SS} − 9.0	V
Power Supply Current (I_{GG})	T_A = +25°C, V_{GG} = −12V, ϕ_{PW} = 235 ns, V_{SS} = +5.0V, Input Clock Frequency = 2.04545 MHz		24	36	mA

ac electrical characteristics

T_A within operating temperature range V_{SS} = +5.0V ±5%, V_{GG} = −12V ±5%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Pulse Width (ϕ_{PW})	Input Clock Frequency = 2.04545 MHz, ϕt_r, ϕt_f = 20 ns	190	235	280	
Input Clock Pulse Width (ϕ_{PW})	Input Clock Frequency = 1.26 MHz, ϕt_r = ϕt_f = 20 ns (Note 3)	520	545	570	
Horizontal Reset Pulse Width	Within 400 ns after the Falling Edge of Master Clock (Figure 5), Rise and Fall Time = 20 ns	500	600	800	ns
Output Propagation Delay (t_{pd})					
Logical High Level (V_{OH})	Capacitance at the Output = 15 pF		500	750	ns
Logical Low Level (V_{OL})	(Figure 5)		500	750	ns
Field Index Pulse Width	Within 400 ns after the Falling Edge of Master Clock (Figure 5) (Note 2), Rise and Fall Time = 20 ns	500	600	700	ns

Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Field index output available only for master clock of 1.26 MHz.

Note 3: If field index is not required the clock pulse width is 300 ns ≤ ϕ_{PW} ≤ 570 ns

functional description

EXTERNAL CONTROL LEVELS

Horizontal Reset occurs for Logic "0," this resets the horizontal counter to a state shown in Figures 2 and 3.

Vertical Reset occurs for Logic "0," this resets the vertical counter to a state determined by reset control input as shown below:

RESET CONTROL INPUT	PERMITS THE VERTICAL COUNTER TO RESET TO THE:
V_{IH}, (V_{SS})	0 th count
V_{IL}, (V_{GG})	11 th count

Logic "0" = V_{IL}

Logic "1" = V_{IH}

Divide select input = V_{IL}, (V_{GG}) for master clock frequency of 1.26 MHz.

Divide select input = V_{IH}, (V_{SS}) for master clock frequency of 2.04545 MHz.

INPUTS

The user may select either of two input clock frequencies by properly programming the Divider Control pin. In one case the input frequency is 2.04545 MHz; which is 14.318180 MHz divided by seven. The other is eighty times the horizontal frequency, or 1.260 MHz. The divider control will be programmed by connecting it to V_{IH} (V_{SS}) and V_{IL}, (V_{GG}) respectively.

There are separate *Vertical* and *Horizontal Reset* inputs which allow directly resetting the appropriate divider(s) by a control pulse generated by external means. Both horizontal and vertical dividers may be reset simultaneously by connecting the *Vertical* and *Horizontal Reset* pins together and driving them with the same reset signal. Actual resetting of the vertical divider is to either of two states, depending upon the state of, the *Reset Control* input; to zero, or to the fifth vertical serration pulse (eleven 0.5H time intervals from leading edge of *Vertical Blanking*). Refer to the reset table above. The horizontal divider will always be reset to a position which is 8 input clock pulses from the leading edge of the serration gate in the horizontal timing scheme (Figure 2 and 3). The generator is reset to the odd field (field one). The *Field Index* output pulse occurs once each odd field at the leading edge of *Vertical Blanking.* It can be used to reset, or "gen-lock," similar sync generator chips by connecting it to their *Vertical* and *Horizontal Reset* inputs.

OUTPUTS

The generator supplies the following standard output functions: *Horizontal Drive Out, Vertical Drive Out, Composite Blanking Out, Composite Sync Out* and the *Color Burst Gate.*

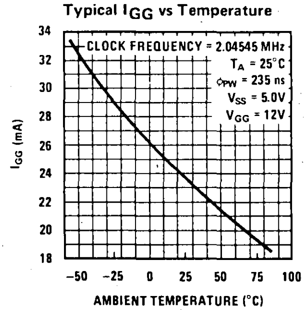
In addition, *Field Index* and *Color Burst Sync* outputs are provided. The *Field Index* identifies the odd field, or field one, by occurring for two clock periods at the leading edge of Vertical Blanking in that field. Thus, its rate is 30 Hz. As described above, it can also be used to "gen-lock" other sync generator chips.

The *Color Burst Sync* output signal occurs at half the horizontal rate with the same timing as the *Color Burst Gate* output. It may be used to sync the color burst as it will have the same delay characteristics as the other outputs (including, of course, the *Color Burst Gate*) — the color burst sync is present during the vertical interval.

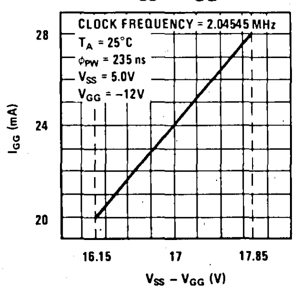
Differences in phasing between outputs are minimized by the use of identical push-pull output buffers clocked by the internal clock.

typical performance characteristics

Typical I_{GG} vs Temperature



Typical I_{GG} vs Power Supply Voltage ($V_{SS} - V_{GG}$)



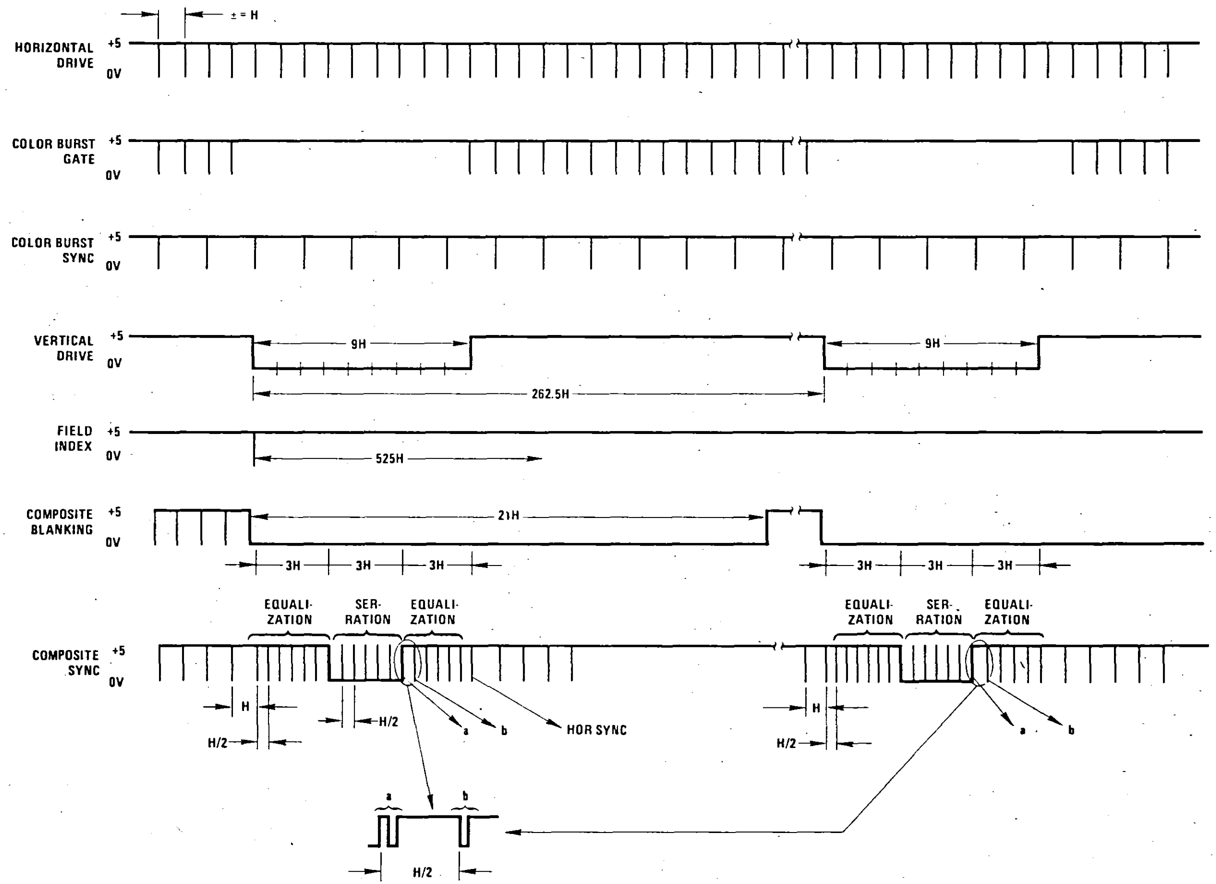

t = H
HORIZONTAL DRIVE
+5
0V
COLOR BURST GATE
+5
0V
COLOR BURST SYNC
+5
0V
VERTICAL DRIVE
+5
0V
9H
9H
262.5H
FIELD INDEX
+5
0V
525H
COMPOSITE BLANKING
+5
0V
21H
3H
3H
3H
3H
3H
3H
EQUALI-ZATION
SER-RATION
EQUALI-ZATION
EQUALI-ZATION
SER-RATION
EQUALI-ZATION
COMPOSITE SYNC
+5
0V
H
H/2
H/2
a
b
HOR SYNC
H
H/2
a
b
a
b
H/2

FIGURE 1.

switching time waveforms (con't)

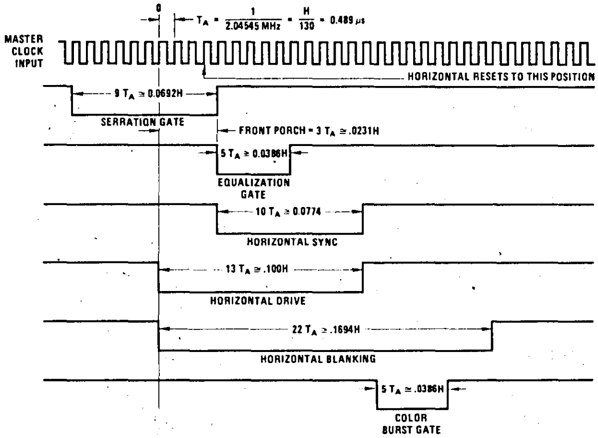


FIGURE 2. Horizontal Timing Master Clock = 2.04545 MHz

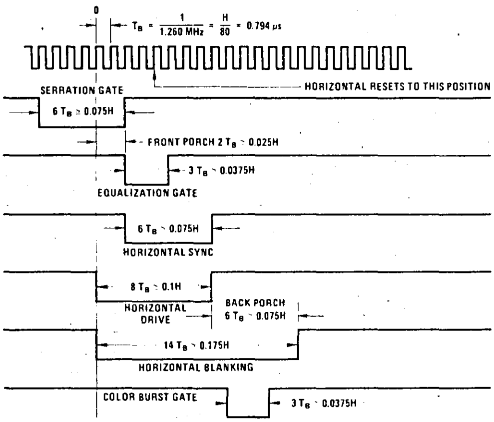


FIGURE 3. Horizontal Timing Master Clock = 1.26 MHz

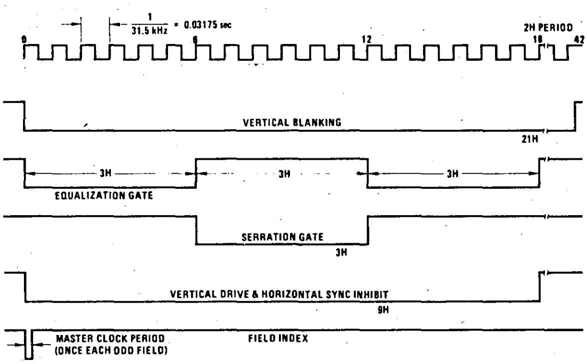


FIGURE 4. Vertical Timing

switching time waveforms (con't)

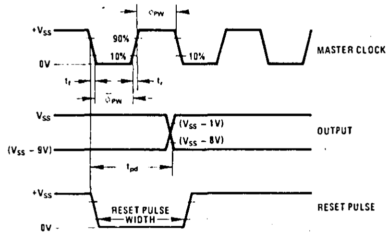
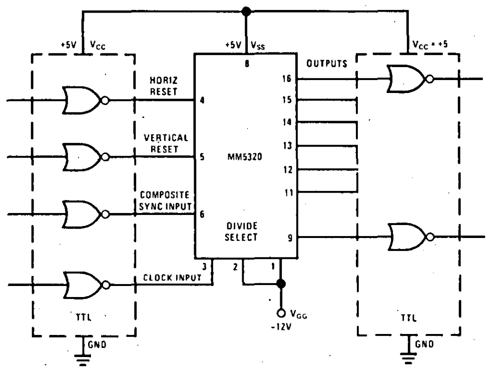


FIGURE 5.

typical application



TTL Interface

TV Circuits

MM5321 TV camera sync generator

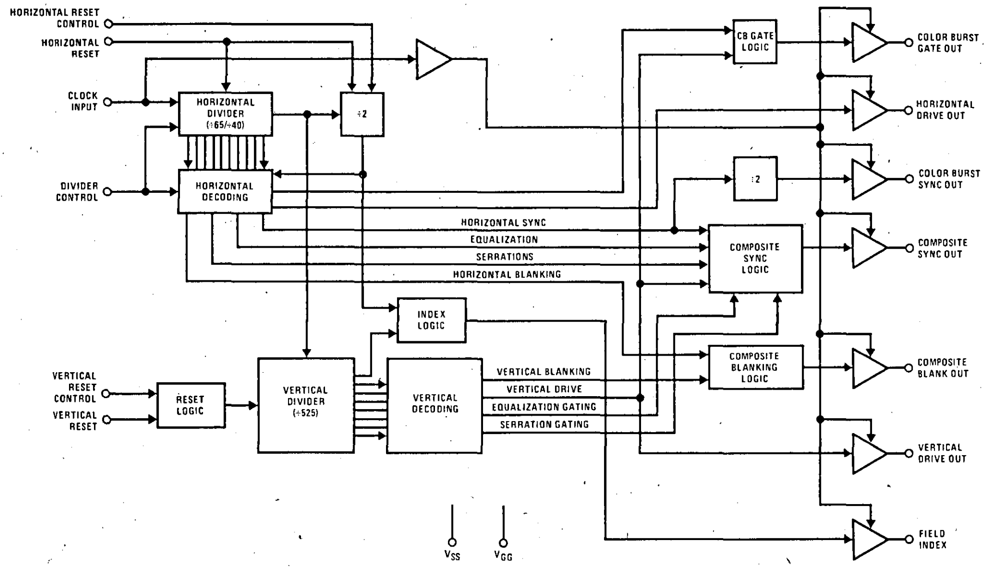
general description

The MM5321 TV camera sync generator is a MOS, P-channel enhancement mode, LSI chip designed to supply the basic sync functions for either color or monochrome 525 line/60 Hz interlaced camera and video recorder applications. Required power supplies are +5V and −12V, or any other combination resulting in V_{SS} − 17V. All inputs and outputs are TTL compatible without the use of external components. Military and commercial temperature ranges are available.

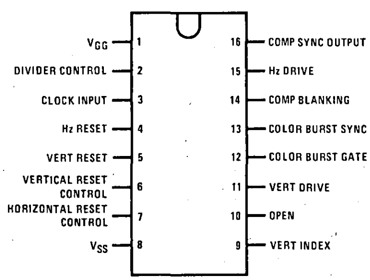
features

- Multi-function gen lock input provides flexible control of multiple camera installations
- 16-lead dual-in-line package
- Conventional +5V, −12V power supplies
- Uses 2.04545 MHz or 1.260 MHz input reference
- Field indexing provided for VTR applications
- Color burst gate and sync allow stable color operation

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5321N
See Package 19

absolute maximum ratings

Voltage at Any Pin	$V_{SS}+0.3$ to $V_{SS}-22$
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

T_A within operating temperature range $V_{SS} = 5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, unless otherwise stated.

	PARAMETER	CONDITIONS	MIN	MAX	UNITS
	Input Levels				
V_{IH}	Logical High Level		$V_{SS}-1.5$	$V_{SS}+0.3$	V
V_{IL}	Logical Low Level		$V_{SS}-18$	$V_{SS}-4.2$	V
	Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$, All Other Pins GND		0.5	μA
	Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND, (Note 1)		6	pF
	Clock Input Leakage	$V_{IN} = -10V$, $T_A = 25°C$, All Other Pins GND		0.5	μA
	Clock Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND, (Note 1)		6	pF
	Output Levels				
V_{OH}	Logical High Level	$I_{SOURCE} = -0.5$ mA	2.4	V_{SS}	V
V_{OL}	Logical Low Level	$I_{SINK} = 1.6$ mA		0.4	V
		MOS Load	$V_{SS}-12.5$	$V_{SS}-9$	V
I_{GG}	Power Supply Current	$T_A = 25°C$, $V_{GG} = -12V$, $\phi_{PW} = 235$ ns, $V_{SS} = 5V$, Input Clock Frequency = 2.04545 MHz		36	mA

ac electrical characteristics

T_A within operating temperature range $V_{SS} = 5V \pm 5\%$, $V_{GG} = -12V \pm 5\%$, unless otherwise stated.

	PARAMETER	CONDITIONS	MIN	MAX	UNITS
ϕ_{PW}	Input Clock Pulse Width	Input Clock Frequency = 2.04545 MHz, ϕt_r, ϕt_f = 20 ns	190	280	ns
		Input Clock Frequency = 1.26 MHz, $\phi t_r = \phi t_f$ = 20 ns	300	570	ns
	Horizontal Reset Pulse Width	Within 400 ns after the Falling Edge of Master Clock, *(Figure 5)* Rise and Fall Time = 20 ns	500	800	ns
t_{pd}	Output Propagation Delay				
V_{OH}	Logical High Level	Capacitance at the Output = 15 pF		750	ns
V_{OL}	Logical Low Level	*(Figure 5)*		750	ns

Note 1: Capacitance is guaranteed by periodic testing.

functional description

EXTERNAL CONTROL LEVELS

Horizontal Reset occurs for Logic "0." This resets the horizontal counter to a state shown in *Figures 2 and 3*.

Vertical Reset occurs for Logic "0." This resets the vertical counter to a state determined by reset control input as shown below:

VERTICAL RESET CONTROL INPUT	PERMITS THE VERTICAL COUNTER TO RESET TO THE:
V_{IH}, (V_{SS})	0th count
V_{IL}, (V_{GG})	11th count

HORIZONTAL RESET CONTROL INPUT	RESETS THE HORIZONTAL DIVIDER TO:
V_{IH}	Beginning of line
V_{IL}	Center of line

Logic "0" = V_{IL}

Logic "1' = V_{IH}

Divide select input = V_{IL}, (V_{GG}) for master clock frequency of 1.26 MHz.

Divide select input = V_{IH}, (V_{SS}) for master clock frequency of 2.04545 MHz.

INPUTS

The user may select either of two input clock frequencies by properly programming the Divider Control pin. In one case the input frequency is 2.04545 MHz, which is 14.31818 MHz divided by seven. The other is eighty times the horizontal frequency, or 1.26 MHz. The divider control will be programmed by connecting it to V_{IH} (V_{SS}) and V_{IL}, (V_{GG}) respectively.

There are separate Vertical and Horizontal Reset inputs which allow directly resetting the appropriate divider(s) by a control pulse generated by external means. Both horizontal and vertical dividers may be reset simultaneously by connecting the Vertical and Horizontal Reset pins together and driving them with the same reset signal. Actual resetting of the vertical divider is to either of two states, depending upon the state of the Vertical Reset Control input; to zero, or to the fifth vertical serration pulse (eleven 0.5H time intervals from leading edge of Vertical Blanking). Refer to the reset table. The horizontal divider will always be reset to a position which is 8 input clock pulses from the leading edge of the serration gate in the horizontal timing scheme *(Figures 2 and 3)*. The generator is reset to the odd field (field one). The Field Index output pulse occurs once each odd field at the leading edge of Vertical Blanking. It can be used to reset, or "gen-lock," similar sync generator chips by connecting it to their Vertical and Horizontal Reset inputs. The Horizontal Reset Control selects Horizontal Reset to the start or center of a line.

OUTPUTS

The generator supplies the following standard output functions: Horizontal Drive Out, Vertical Drive Out, Composite Blanking Out, Composite Sync Out and the Color Burst Gate.

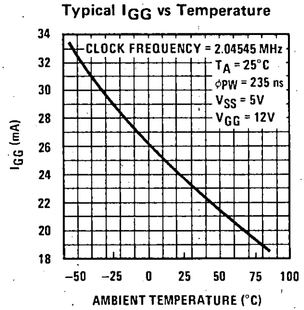
In addition, Field Index and Color Burst Sync outputs are provided. The Field Index identifies the odd field, or field one, by occurring for two clock periods at the leading edge of Vertical Blanking in that field. Thus, its rate is 30 Hz. As described above, it can also be used to "gen-lock" other sync generator chips.

The Color Burst Sync output signal occurs at half the horizontal rate with the same timing as the Color Burst Gate output. It may be used to sync the color burst as it will have the same delay characteristics as the other outputs (including, of course, the Color Burst Gate) — the color burst sync is present during the vertical interval.

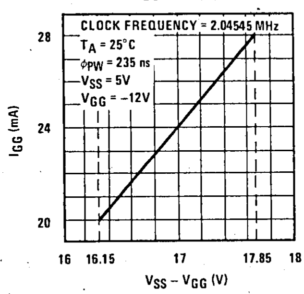
Differences in phasing between outputs are minimized by the use of identical push-pull output buffers clocked by the internal clock.

typical performance characteristics

Typical I_{GG} vs Temperature



Typical I_{GG} vs Power Supply Voltage ($V_{SS} - V_{GG}$)



switching time waveforms

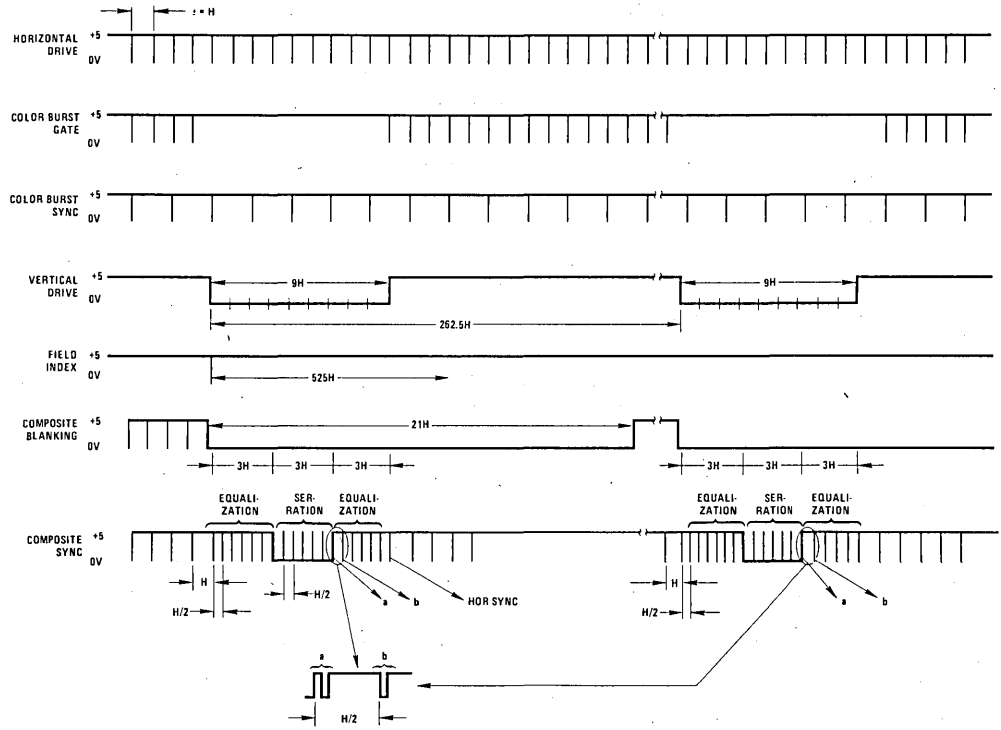


FIGURE 1.

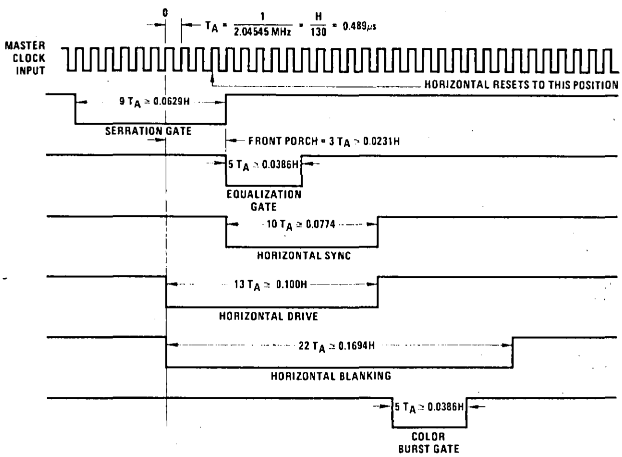


FIGURE 2. Horizontal Timing Master Clock = 2.04545 MHz

switching time waveforms (Continued)

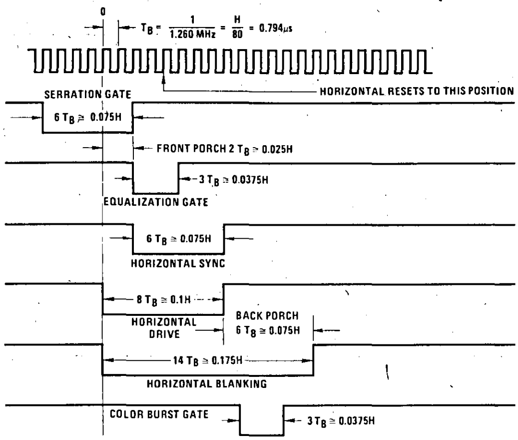


FIGURE 3. Horizontal Timing Master Clock = 1.26 MHz

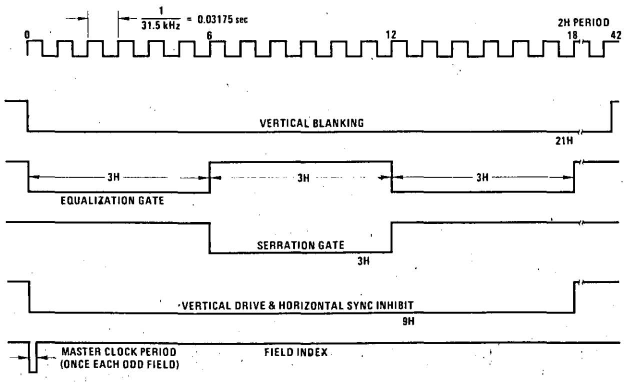


FIGURE 4. Vertical Timing

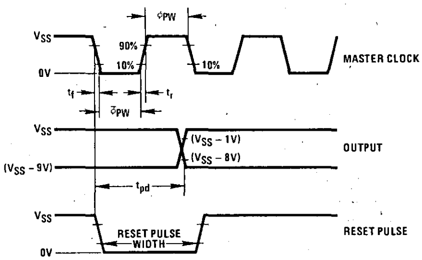


FIGURE 5.

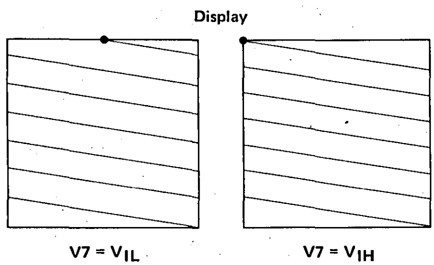
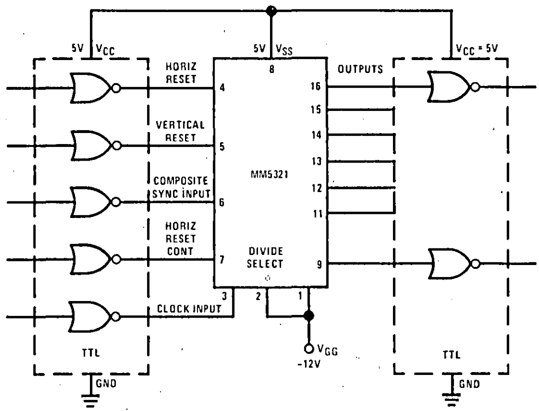


FIGURE 6. Horizontal Reset Characteristics

typical application



TTL Interface

MM5322 color bar generator chip

general description

The MM5322 Color Bar Generator Chip is a complete dot-bar and color hue generation system in a single monolithic P-channel MOS integrated circuit. The chip divides an internal oscillator (crystal controlled) frequency to provide the various timing, synchronization, and video information required in the alignment of color television receivers. A composite video output is provided for complete black and white dot-bar operation. It consists of all synchronization, blanking, and video information required for a fairly standard set of dot, bar, and cross hatch screen patterns. In addition a separate output for precise gating of 3.56 MHz color bursts is provided. For servicing ease an oscilloscope trigger is provided on either the horizontal blanking or vertical synchronization time slots.

features

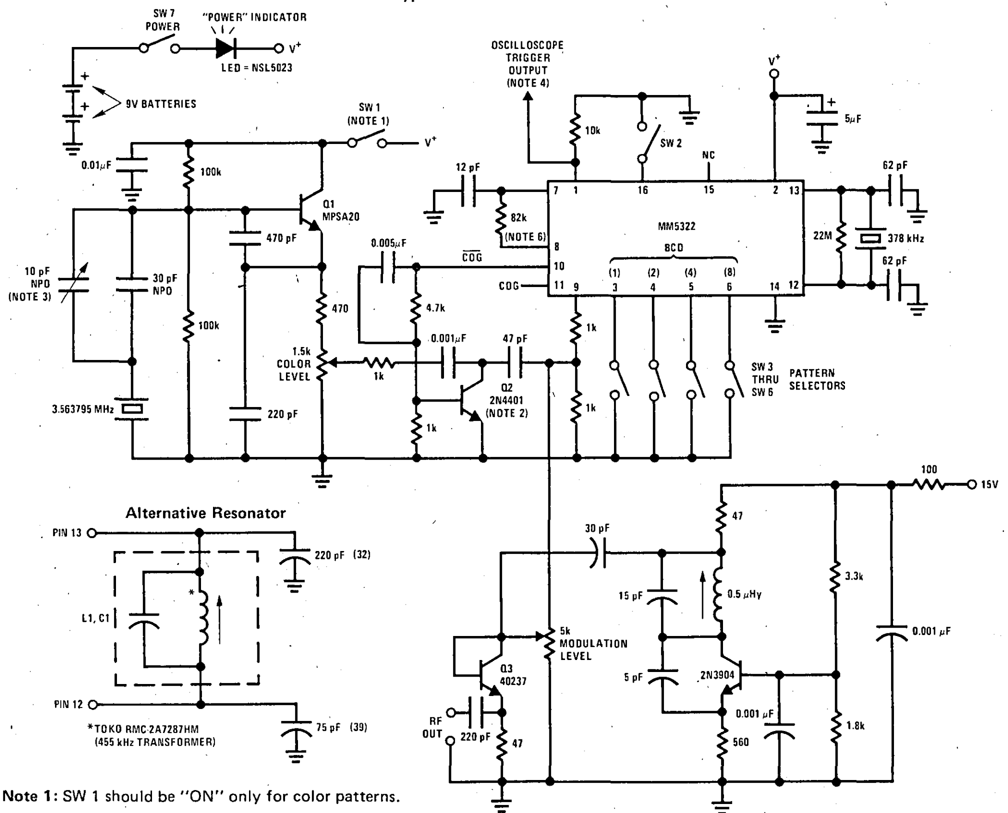
- Battery operation
- Oscilloscope trigger
- Composite video output signal
- Crystal controlled oscillator
- Multiple screen patterns
- Variable dot size

applications

- Battery or bench powered test instruments
- Manufacturing test sets
- Built in test capability

typical application

Typical Color Bar Generator Circuit



Note 1: SW 1 should be "ON" only for color patterns.

Note 2: Do not substitute Q2.

Note 3: Variable cap may be used to trim color crystal to exact frequency.

Note 4: SW 2 and 10k resistor on pins 16 and 1 are needed only if scope trigger pulse is desired.

Note 5: SW 2 selects "H" or "V" trigger output pulses.

Note 6: A 27k resistor in series with a 100k trimpot may be used in place of 82k resistor for variable vertical line width.

Note 7: Modulation level adjusted for best patterns as viewed on TV screen.

absolute maximum ratings

Voltage at Any Pin	V_{SS}+0.3V to V_{SS}−25V
Operating Temperatures	−25°C to +75°C
Storage Temperature	−65°C to +150°C
Lead Temperatures (Soldering, 10 seconds)	300°C

electrical characteristics T_A within operating range, V_{SS} = +12 to +19V, V_{GG} = 0V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		12		19	V
Clock Input Frequency OSC 1 and 2	Crystal or External Drive (Note 1)		378		kHz
Clock Input Levels	For External Drive (Note 1)				
Logical High		V_{SS}−2		V_{SS}+0.3	V
Logical Low		V_{GG}		V_{GG}+2	V
Control Inputs BCD and Trigger	Internal Resistor To V_{SS}, 1M Ω Min.				
Logical High	(Note 2)	V_{SS}−2		V_{SS}+0.3	V
Logical Low		V_{GG}		V_{GG}+2	V
Control Output Currents Cog and $\overline{\text{Cog}}$					
Logical High	V_{SS} − 2.0V	2.5			mA
Logical Low	V_{GG} − V_{GG}/2 (Note 3)	0.25			mA
Trigger and Z					
Logical High	With 10k to V_{GG}, V_{GG} + 5.0V (Note 4)	0.5			mA
Logical High	With 1k to V_{GG}, V_{GG} + 1 (Note 4)	1.0			mA
Video Output					
Analog Highs	With 2k to V_{GG} (Note 5)		2.0 to 4.0		mA
Power Supply Current	T_A = 25°C, Freq = 378 kHz, V_{GG} = 0V, V_{SS} = +19V			30	mA

Note 1: The oscillator may be operated with external components to oscillate at 378 kHz or it may be driven by an external pulse source using OSC 2 (Pin 13) as an input.

Note 2: These inputs are driven by switches.

Note 3: The color gate outputs are push-pull buffers.

Note 4: The trigger output and Z output are open drain outputs and require a resistor to V_{GG} for operation. Two possible resistor values are shown with their associated voltage and current levels.

Note 5: The video output requires a resistor to V_{GG} for operation. This resistor must be trimmed externally to achieve the desired output levels. The minimum voltage swing is 4.0 volts with a 10% change with temperature and from unit to unit. The percentage magnitude change with supply voltage can approach one.

composite video output

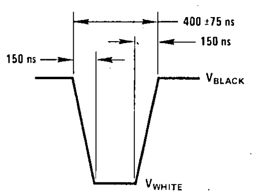


FIGURE 1. White Dot Video Information Pulse Width

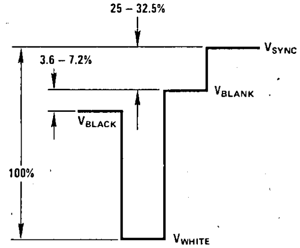


FIGURE 2. Composite Video Voltage Percentages

composite video output (con't)

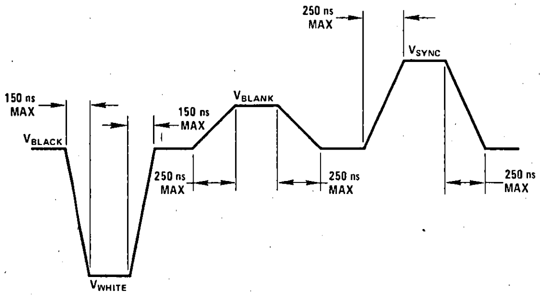


FIGURE 3. Composite Video Rise and Fall Times

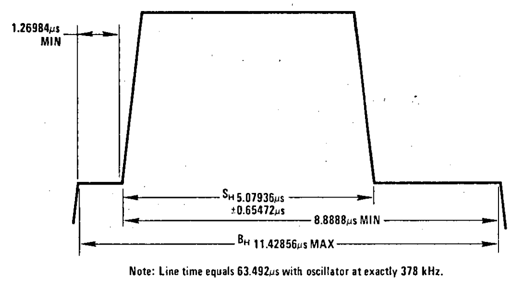


FIGURE 4. Composite Video Pulse Timing, Horizontal Sync

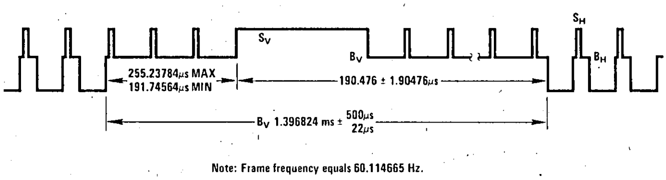


FIGURE 5. Composite Video Pulse Timing, Vertical Sync

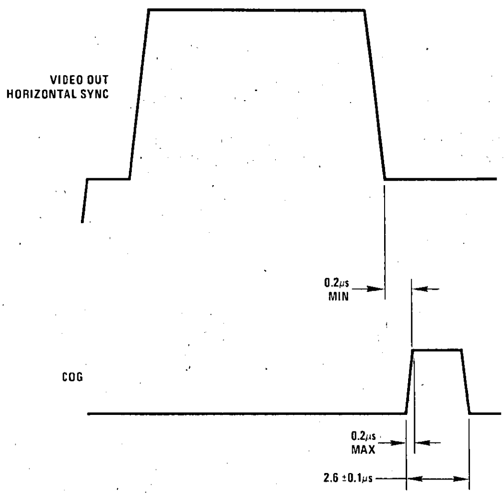


FIGURE 6. Color Gate Signal Timing

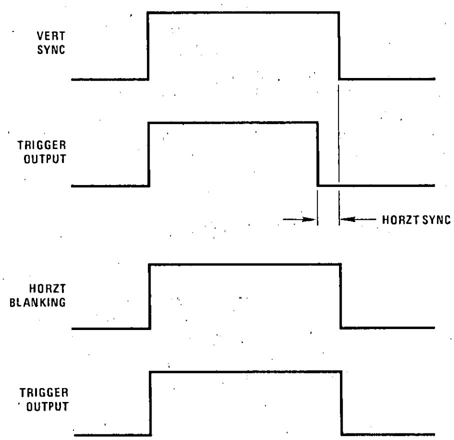
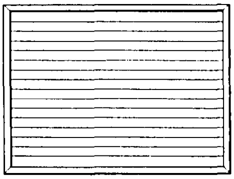
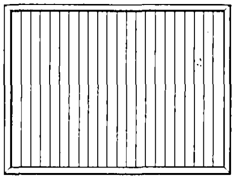


FIGURE 7. Trigger Output Timing Relationship

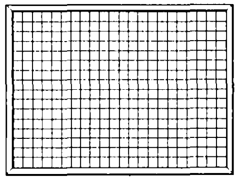
video output patterns



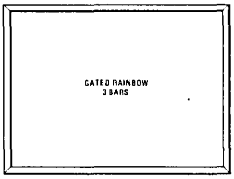
15 Horizontal Lines
0000



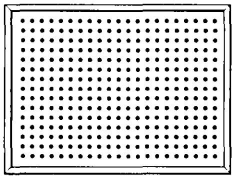
21 Vertical Lines
0001



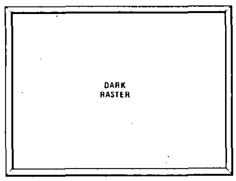
15 x 21 Cross Hatch
0010



Gated Rainbow
0011

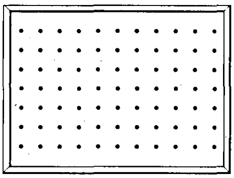


Dots 15 x 21
0100

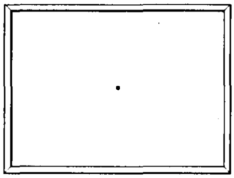


Note: Pattern switch codes are BCD 1248 positive logic.

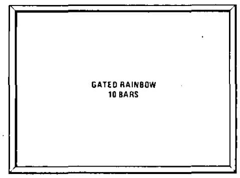
Purity
0101



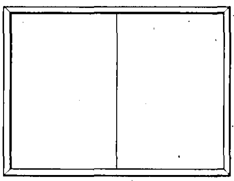
Dots 7 x 11
0110



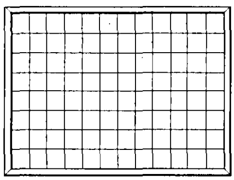
Single Dot
0111



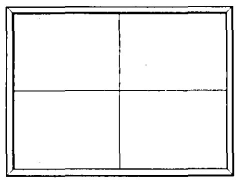
Gated Rainbow
1000



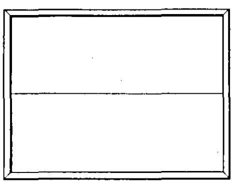
Single Vertical Line
1001



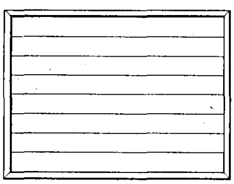
7 x 11 Cross Hatch
1010



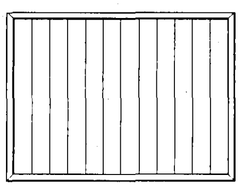
Single Crosshair
1011



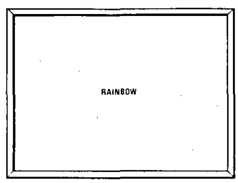
Single Horizontal Line
1100



7 Horizontal Lines
1101



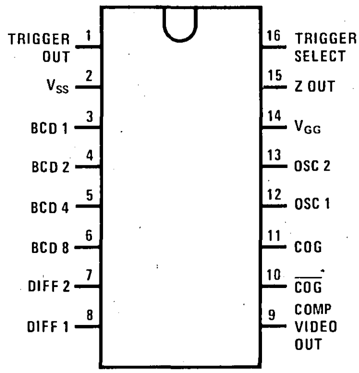
11 Vertical Lines
1110



Ungated Rainbow
1111

connection diagram

Dual-In-Line Package



TOP VIEW

Note. Z_{OUT} is an internal counter test point.

Order Number MM5322N
See Package 19

MM5840 TV channel number (16 channels) and time display circuit

general description

The MM5840 TV Channel Number and Time Display Chip is a monolithic metal gate CMOS integrated circuit which generates a display of channel numbers (up to 16 channels) and time readouts on the television screen.

By external connection, it has the option of displaying the channel number only while switching channels with a period controlled by the external RC time constant of a timeout monostable.

This chip includes all the logic required to provide two modes of operation, namely channel number, or channel number and time display.

In addition, it can have a five (hour tens, hour units, colon, minute tens, and minute units) or eight digit (hour tens, hour units, colon, minute tens, minute units, colon, second tens, and second units) display, depending on the digit select input logic level.

By employing the video gating input together with the video output, a symmetrical blanked rectangular frame around the display may be generated on the TV screen.

This chip serves as a display generator with BCD channel inputs, as provided from the clock chips MM5318, MM53100 or MM53105. The position of the display on the TV screen can be controlled by adjusting external RC time constants.

functional description

The channel number and time readout circuit operates with a 2 to 4.5 MHz input clock. Counters are incorporated in the chip, operated by the input clock to keep track of the time slots of the display.

The position of the display is controlled by adjusting the external RC time constants of the horizontal and vertical monostable multivibrators.

A 7-segment decoder is used to decode either channel inputs or time which is stored temporarily in the channel number buffers or 4-bit latches, respectively, depending on the time slot of the display. Each digit of time is stored in a 4-bit latch while it is being decoded and displayed, and the next digit enters the latch while the horizontal sweep is between digits.

A time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that modulates the sweep of the television tube for the display on the screen.

features

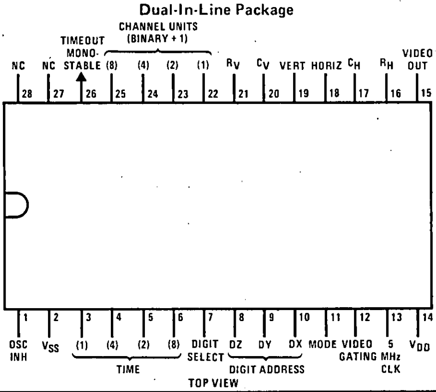
- 12 or 24-hour operation (controlled by clock chip)
- 5 or 8-digit display
- Channel number leading zero blanking
- Single power supply
- Channel number only or channel number and time display
- Video gating output for generating a symmetrical blanked rectangular frame around the display
- Oscillator inhibit output
- Channel number display only while switching channels
- 4-bit binary plus one code for channel numbers

functions

- 8-digit mode is selected by a logic "1" at digit select input
- Channel number and time mode is selected by a logic "1" at mode input
- Permanent channel number display is selected by a logic "1" at timeout monostable input

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5840N
See Package 23

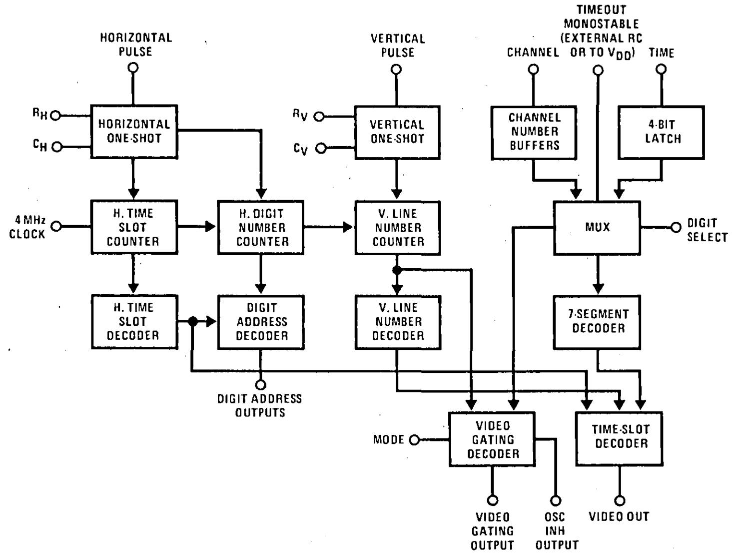
absolute maximum ratings

Supply Voltage ($V_{DD} - V_{SS}$)	−0.3V to +15V
Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics V_{DD} = 12V, V_{SS} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage					
V_{DD}	V_{SS} = 0	11	12	14	V
Power Supply Current				800	μA
Input Voltage Levels					
Time, Oscillator, Digit					
Select, and Mode Inputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Channel Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Input Frequency	Interfacing with MM53100, MM53105	2		4.5	MHz
Oscillator	Interfacing with MM5318	2		4.5	MHz
Horizontal	Pulse Width = 14 μs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Video Gating, Osc. Inhibit					
Digit Address and Video Outputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal		15		50	μs
Vertical		1.5		13	ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1V	|−1|			mA
Logical High	V_{DD} − 1V	1			mA
Video Gating and Osc.					
Inhibit Outputs					
Logical Low	Output Forced Up to V_{DD} − 4.5V	|−2|			mA
Logical High	V_{DD} − 1V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		μF
$C_{HORIZONTAL}$			0.001		μF
$R_{VERTICAL}$			50		kΩ
$R_{HORIZONTAL}$			100		kΩ
$C_{TIMEOUT}$			5		μF
$R_{TIMEOUT}$				1	MΩ
Propagation Delay					
Video Gating and Osc.	From Input Clock to Oscillator			2	clock
Inhibit Outputs	Inhibit or Video Gating Outputs				pulses
Input Leakage				1	μA
Input Capacitance				5	pF

block diagram



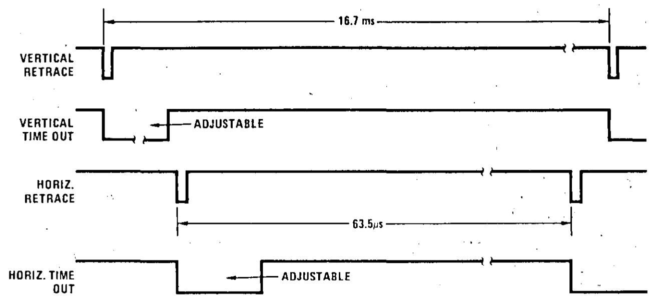
truth table

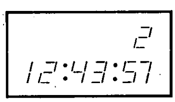
Digit Address (DX, DY, DZ) Codes

CODES	DURING RESET	DIGITS 1	2	3	4	5	6	7	8
DX	1	0	0	1	1	0	0	1	1
DY	1	1	0	0	0	0	1	1	1
DZ	1	1	1	1	0	0	0	0	1

timing diagram

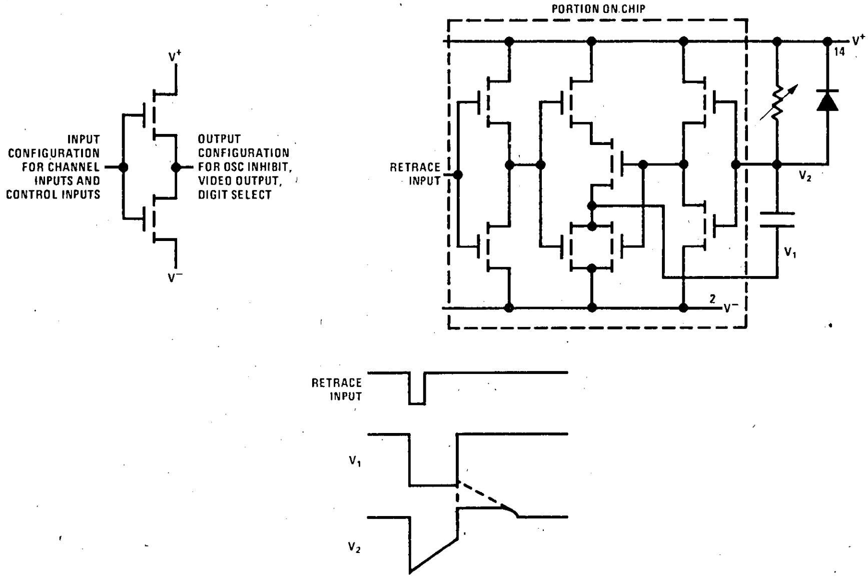
With Video Gating, Output Gated with Video Output



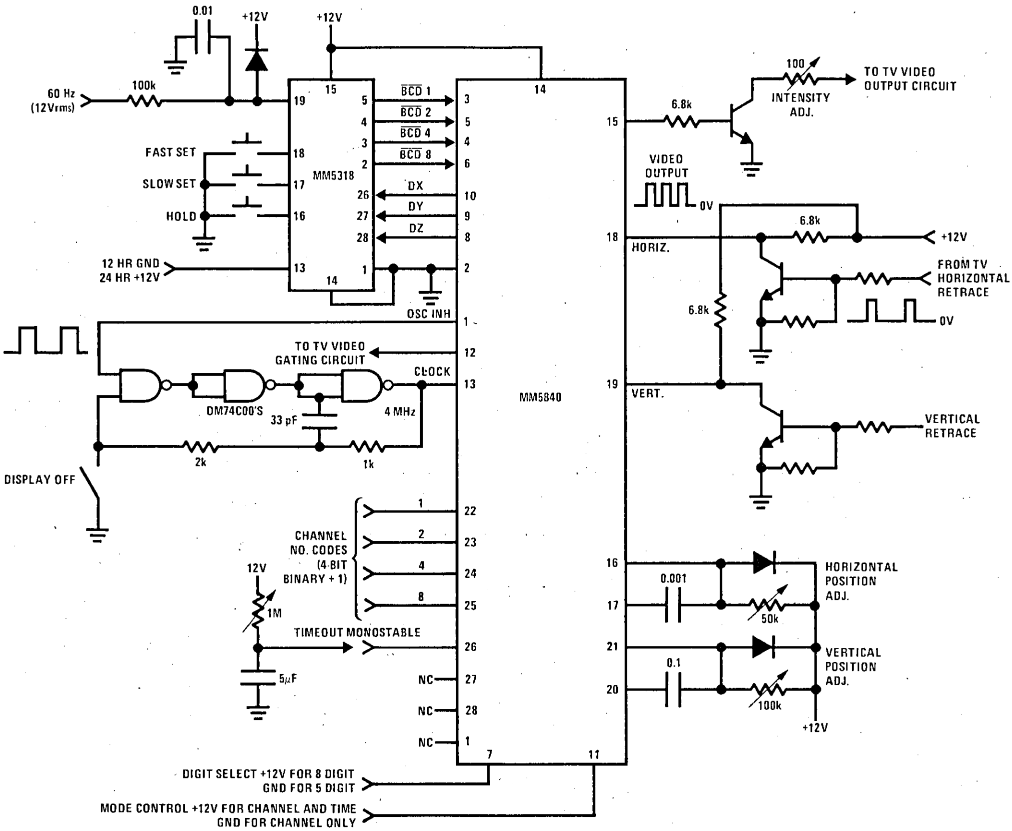


typical applications

Horizontal and Vertical One-Shot Circuit

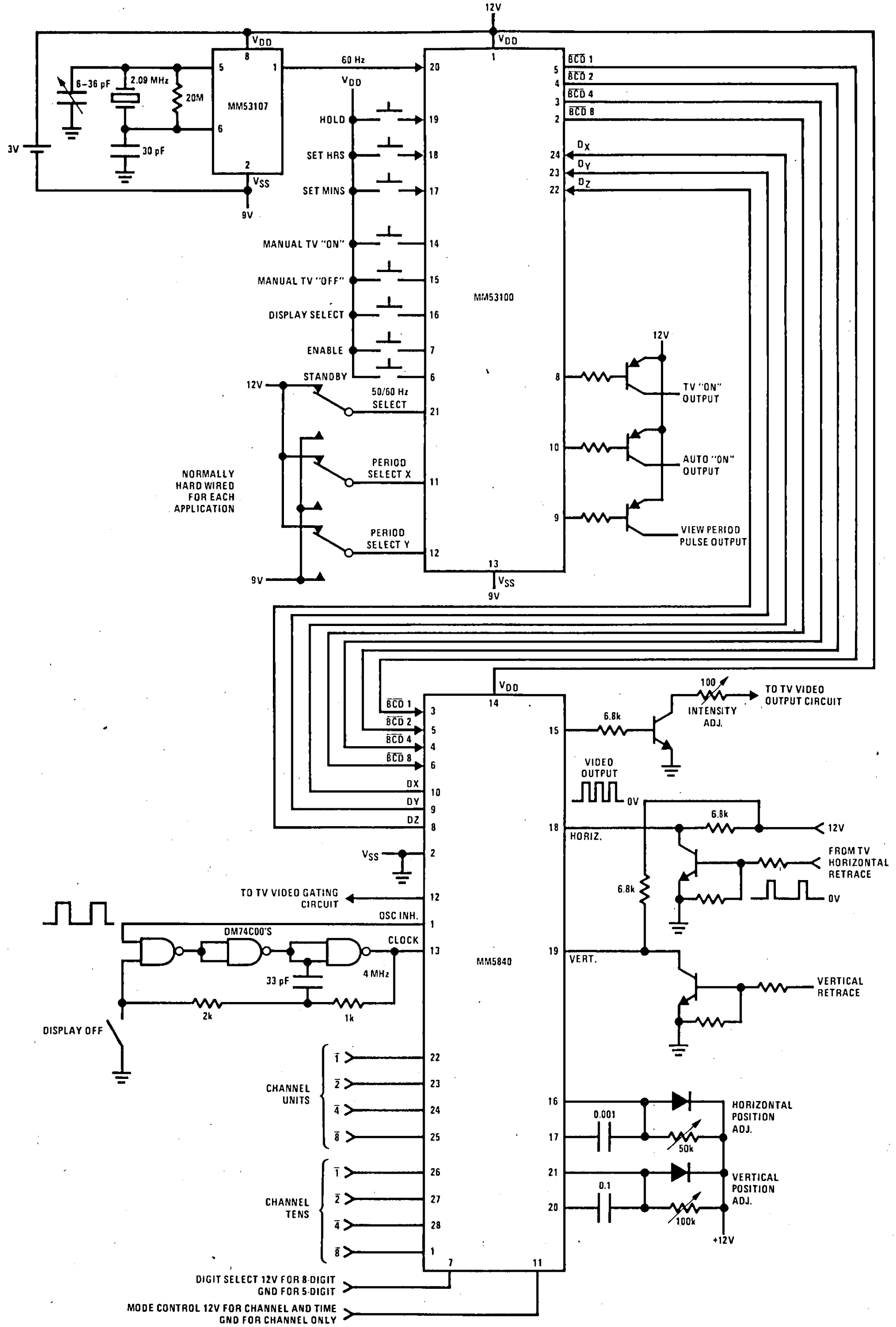


TV Channel and Time Display Interfacing MM5318



typical applications (Continued)

TV Channel and Time Display Interfacing MM53100



Note. For interfacing with MM53105, refer to MM53105 specifications.

MM5841 TV channel number and time readout circuit

general description

The MM5841 TV Channel Number and Time Readout Circuit is a monolithic metal gate CMOS integrated circuit, which generates a display of channel number and time readouts on the television screen.

This chip includes all the logic required to provide two modes of operation, namely channel number, or channel number and time displays.

In addition, it can have a five (hour tens, hour units, colon, minute tens, and minute units) or eight digit (hour tens, hour units, colon, minute tens, minute units, colon, second tens, and second units) display, depending on the digit select input logic level.

This chip serves as a display generator between the BCD channel inputs, the clock chip (MM5318) and the television set. The position of the display on the TV screen can be controlled by adjusting the external RC time constants.

functional description

The channel number and time readout circuit operates with a 4 MHz input clock. Counters are incorporated in the chip, operated by the input clock to keep track of the time slots of the display.

The position of the display is controlled by adjusting the external RC time constants of the horizontal and vertical monostable multivibrators.

A 7-segment decoder is used to decode either channel inputs or time which is stored temporarily in the channel number buffers or 4 bit latches, respectively, depending on the time slot of the display. Each digit of time is stored in a 4-bit latch while it is being decoded and displayed, and the next digit enters the latch while the horizontal sweep is between digits.

A time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that modulates the sweep of the television tube for the display on the screen.

features

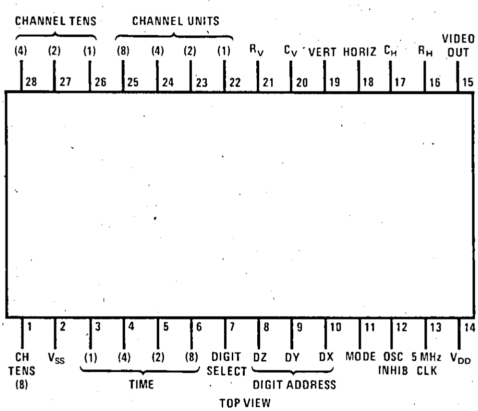
- 12 or 24 hour operation (controlled by clock chip)
- 5 or 8 digit display
- Channel number leading zero blanking
- Single power supply
- Channel number only or channel number and time display

functions

- 8 digit mode is selected by a logic "1" at digit select input
- Channel number and time mode is selected by a logic "1" at mode input

connection diagram

Dual-In-Line Package



Order Number MM5841N
See Package 23

absolute maximum ratings

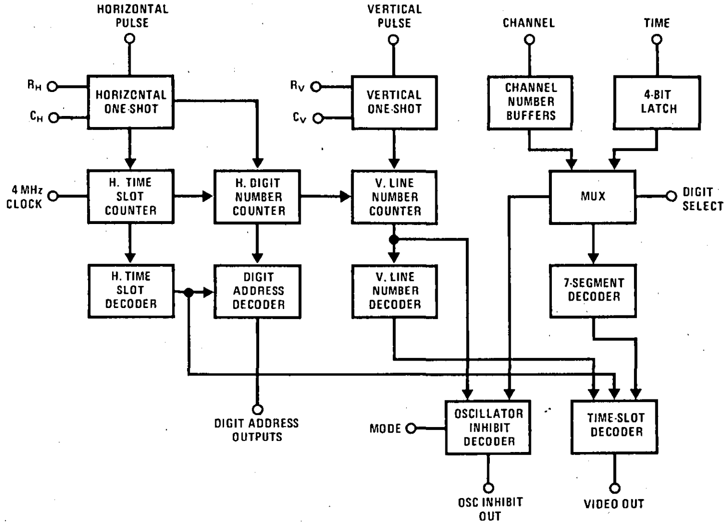
Supply Voltage ($V_{DD} - V_{SS}$)	−0.3V to +15V
Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

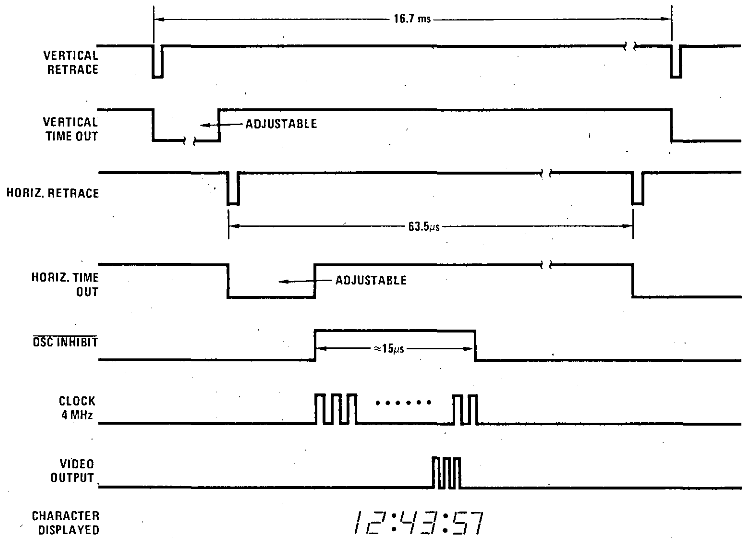
V_{DD} = 12V, V_{SS} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage					
V_{DD}	V_{SS} = 0	11	12	14	V
Power Supply Current				800	µA
Input Voltage Levels					
Time, Oscillator, Digit Select, and Mode Inputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Channel Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Input Frequency					
Oscillator		1	4	4.5	MHz
Horizontal	Pulse Width = 14µs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Oscillator Inhibit, Digit Address and Video Outputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal		15		50	µs
Vertical		1.5		13	ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1.0V	−1			mA
Logical High	V_{DD} − 1.0V	1			mA
Oscillator Inhibit Output					
Logical Low	Output Forced Up to V_{DD} − 4.5V	−2			mA
Logical High	V_{DD} − 1.0V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		µF
$C_{HORIZONTAL}$			0.001		µF
$R_{VERTICAL}$			50		kΩ pot
$R_{HORIZONTAL}$			100		kΩ pot
Propagation Delay					
Oscillator Inhibit Output	From Input Clock to Oscillator Inhibit Output			2	clock pulses
Input Leakage				1	µA
Input Capacitance				5	pF

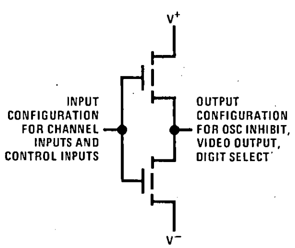
block diagram

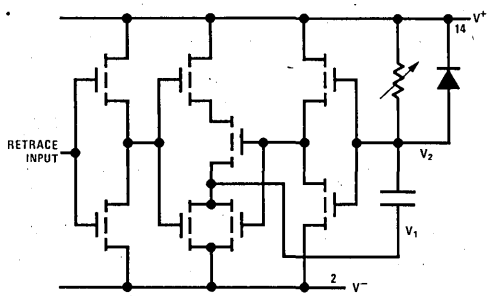


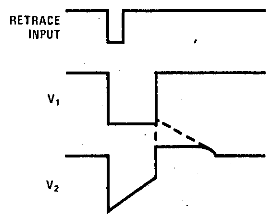
timing diagram



typical applications

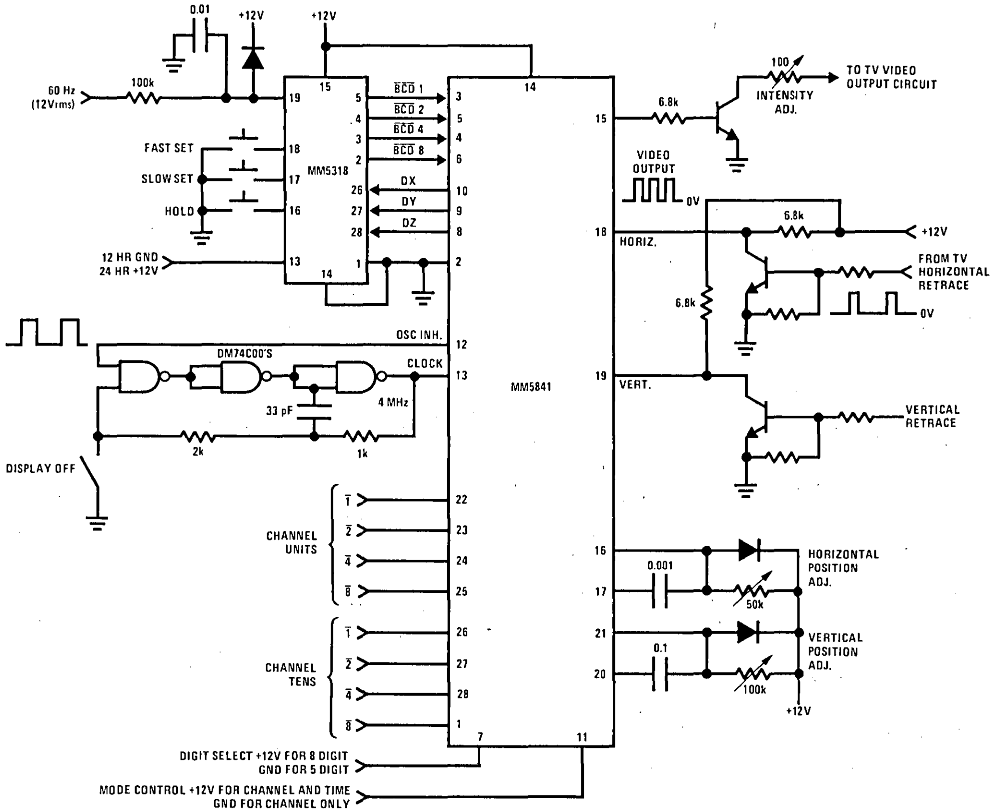






Horizontal and Vertical One-Shot Circuit

typical applications (con't)



TV Channel and Time Display

4

MM53100, MM53105 programmable TV timers

general description

The MM53100 and MM53105 programmable TV timers are monolithic CMOS integrated circuits utilizing P and N-channel low threshold enhancement devices. These circuits contain all the logic to give a 4 or 6-digit, 24-hour display from a 50 or 60 Hz input, and control the "ON" time of the TV. The duration of the viewing period is 5, 10, 20 or 30 mins, selected by 2 input pins. Manual "ON" and "OFF" inputs are also provided. The MM53100 and MM53105 have ultra-low power dissipation in the stand-by mode and are ideally suited to crystal controlled battery-operated systems. The MM53100 is designed for an optimum interface in TVs with a positive common reference voltage (e.g., +18V). The MM53105 is designed for an optimum interface for TVs with a 0V reference voltage. Both are packaged in a 24-lead dual-in-line epoxy package.

features

- 50 or 60 Hz operation
- 24-hour display format
- Programmable TV on time
- Selectable view time
- Ultra-low power dissipation
- All counters resettable
- Low voltage operation
- Elimination of illegal time display at turn-on
- Daily repeat or non-repeating operating
- Fool-proof safety features
- Compatible with MM5840 or MM5841 display circuits

applications

- TV time display
- Remote TV "ON"/"OFF" switch
- Computer clock
- Time data—logging systems

block diagram

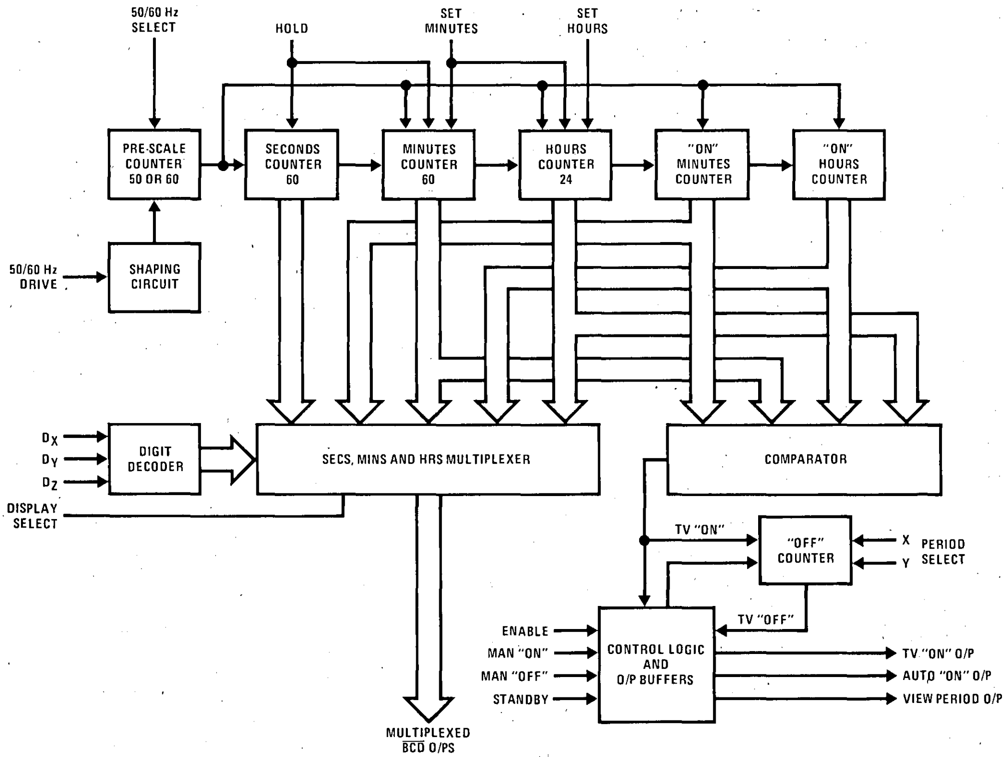


FIGURE 1. MM53100, MM53105 Block Diagram

absolute maximum ratings (MM53100) (V_{DD} common voltage reference)

Supply Voltage ($V_{DD} - V_{SS}$)	6V
Voltage at 50/60 Hz Select and Period Select Inputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Current Into or Out of Any Other Input	100 μA max

electrical characteristics (MM53100) $T_A = 25°C$, $V_{DD} = 4.5V$, $V_{SS} = 0V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.8		5.0	V
Supply Current	$V_{DD} = 4.5V$		10	25	μA
Input Logic Levels					
50/60 Hz Input, Digit Select Inputs, Display Select, "ON", "OFF", Time Setting Control, Standby Control					
Logic "1"		$V_{DD}-0.5$		V_{DD}	V
Logic "0"	(Note 1)			$V_{SS}+0.5$	V
50/60 Hz Select, Period Select (X, Y)					
Logic "1"		$V_{DD}-0.5$		V_{DD}	V
Logic "0"		V_{SS}		$V_{SS}+0.5$	V
Display Select Input Delay		0.5		2.0	μs
Output Logic Levels					
BCD Outputs	External Resistor, 15 kΩ to $V_{DD} - 12V$, $C_L = 15$ pF				
Logic "1"		$V_{DD}-0.8$			V
Logic "0"				$V_{DD}-11.2$	V

Note 1: If input voltages go more negative than V_{SS}, the input current must be limited to a maximum of 100 μA by the use of external series resistors. No resistors are required on the D_X, D_Y, D_Z inputs when interfacing with the MM5840.

absolute maximum ratings (MM53105) (V_{SS} common voltage reference)

Supply Voltage ($V_{DD} - V_{SS}$)	6V
Voltage at 50/60 Hz Select and Period Select Inputs	$V_{SS} + 6V$
Voltage at Any Other Pin	$V_{SS} + 13V$

electrical characteristics (MM53105) $T_A = 25°C$, $V_{DD} = 4.5V$, $V_{SS} = 0V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.8		5.0	V
Supply Current	$V_{DD} = 4.5V$		10	25	μA
Input Logic Levels					
50/60 Hz Input, Digit Select Inputs, "ON", "OFF", Display Select, Time Setting Controls, Standby Control					
Logic "1"		$V_{DD}-0.5$		13	V
Logic "0"		V_{SS}		$V_{SS}+0.5$	V
50/60 Hz Select, Period Select (X, Y)					
Logic "1"		$V_{DD}-0.5$		V_{DD}	V
Logic "0"		V_{SS}		$V_{SS}+0.5$	V
Display Select Input Delay		0.5		2.0	μs

electrical characteristics (Continued) (MM53105) $T_A = 25°C$, $V_{DD} = 4.5V$, $V_{SS} = 0V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Levels					
BCD Outputs	External Resistor 15 kΩ to 12V, C_L = 15 pF				
Logic "1"		11.2			V
Logic "0"				0.8	V
TV "ON" Output, Auto "ON" Output, View Period Output					
Logic "1"	Loaded 2.7 kΩ to V_{SS}	0.5			mA
Logic "0"	Loaded 2.7 kΩ to V_{DD}	1.0			mA

Note 1: Input voltages to go more positive than V_{DD}.

functional description

A block diagram of the MM53100, MM53105 TV timers is shown in *Figure 1*. A connection diagram is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 1. Figures 5a and 5b* illustrate the system configuration for a crystal controlled TV display system using both circuits.

Dual-In-Line Package, Top View

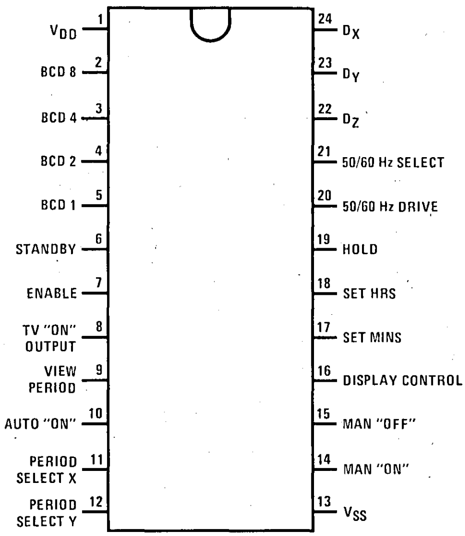


FIGURE 2.

Order Number MM53100N or MM53105N
See Package 22

50 or 60 Hz Drive: This input is applied to a Schmitt trigger shaping circuit which allows use of a filtered sinewave input. A simple RC filter should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the time-keeping function.

Alternatively, in a crystal controlled battery operated system, an oscillator and prescaler such as the MM53107 could be used as a time base.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 pps time base. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal 1 MΩ pull-down resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation.

Time Setting Inputs: Inputs to set hours and set minutes as well as hold input, are provided. Internal 1 MΩ pull-down resistors provide the normal timekeeping function. Switching any 1 of these inputs (1 at a time) to "1" results in the desired time setting function. Set Hours advances hours information at 1 hour/second and Set Minutes advances minutes information at 1 minute/second, without roll over into the hours counter. Set Minutes also resets the seconds counter to 0. The hold input stops the clock to the minutes counter and resets the seconds counter. Activating Set Minutes and Set Hours simultaneously resets the displayed counters to all 0's.

Display: This input controls the display and time-setting operation. It has an internal 1 MΩ pull-down resistor to V_{SS}. When taken to Logic "0" or in open circuit condition, the real time is displayed and the Set Hours and Set Minutes inputs operate the real time counters. When taken to logic "1", the "ON" time is displayed and the time-setting inputs operate on the "ON" counters.

Digital Select Inputs (D_X, D_Y, D_Z): These 3 inputs are used to determine which digit will be displayed. Table IA shows the code for each digit. Seconds will be displayed as "00" when the "ON" time is being displayed.

Enable: This input has an internal resistor to V_{SS}. When taken to logic "1", this input disables the programmed "ON" time for the TV output.

Period Select Inputs (X, Y): These inputs have pull-down resistors to V_{SS}. They determine the view period, i.e., 5, 10, 20 or 30 mins. Table IB shows the Period Select Code.

functional description (Continued)

Standby Control Input: This input has an internal resistor to V_{SS}. Its function is to sense when the line generated 12V supply is turned off and to then disable the outputs. In the TV, this input should be connected to the 12V supply.

Manual "ON" Input: This input has an internal resistor to V_{SS}. When taken to logic "1", this input turns the TV output to the "0" state. It is designed to have typically 0.75 second debounce time to prevent mal-operation.

Manual "OFF" Input: This input has an internal resistor to V_{SS}. When taken to logic "1", this input turns the TV output to the "1" state. It is designed to have typically 0.75 second debounce time to prevent mal-operation.

TV "ON" Output: *Figure 3* illustrates the CMOS inverter output circuit used.

In the manual mode of operation, the manual "ON" input sets this output to "0", the manual "OFF" input resets this output to "1". The manual "ON" input inhibits the auto "ON" output.

In the programmable mode, this output goes to "0" when the programmed "ON" time coincides with the real time (unless enable = 1). The output will then stay at "0" for the selected period of 5, 10, 20 or 30 minutes before returning to "1" state. During this period, a signal on the manual "ON" input will prevent the automatic switch-off.

Manual "OFF" input will always reset the output to a logic "1" state.

Auto "ON" TV Output: An additional output is provided to indicate that the TV is "ON" in the automatic mode of operation. This output goes to a logic "0" for the duration of the auto "ON" time. Manual "ON" switches this output back to a logic "1".

View Period Indicator: This output normally is a logic "1". When the TV switches on at the programmed time, this output transmits a 1 Hz waveform for the duration of the selected view period. Hence, it can be used to indicate that the TV is switched on for a limited period only by means of a flashing on-screen and/or off-screen display. The output will permanently return to "1" at the end of the viewing period or when a valid manual "ON" or "OFF" input signal is received during the view period.

BCD Outputs: *Figure 4* illustrates the open drain output circuits used, a) MM53100, b) MM53105.

With the use of the external respective pull-up and pull-down resistors, these outputs are designed to be compatible with the MM5840 and MM5841 TV display circuits.

Note. Case (a) for common V_{DD}, case (b) for common V_{SS} when used with the MM5840.

TABLE IA. Digit Select Code

DIGIT SELECT LINES	DIGIT DISPLAYED							
	S1	S10	*	M1	M10	*	H1	H10
D_X	1	0	0	1	1	0	0	1
D_Y	1	1	0	0	0	0	1	1
D_Z	0	0	0	0	1	1	1	1

TABLE IB. Period Select Code

PERIOD SELECT INPUTS		VIEW PERIOD PROGRAMMED
X	Y	
0	0	5 mins
0	1	10 mins
1	0	20 mins
1	1	30 mins

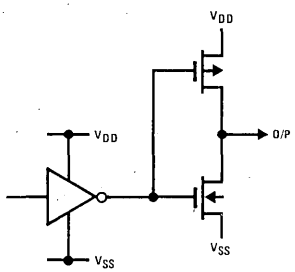


FIGURE 3. CMOS Output (TV "ON", Auto "ON", Indicator)

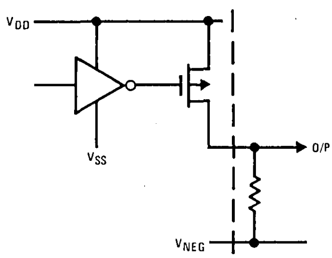


FIGURE 4a. BCD Outputs, MM53100

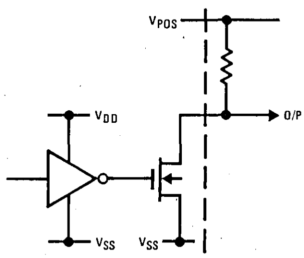


FIGURE 4b. BCD Outputs, MM53105

functional description (Continued)

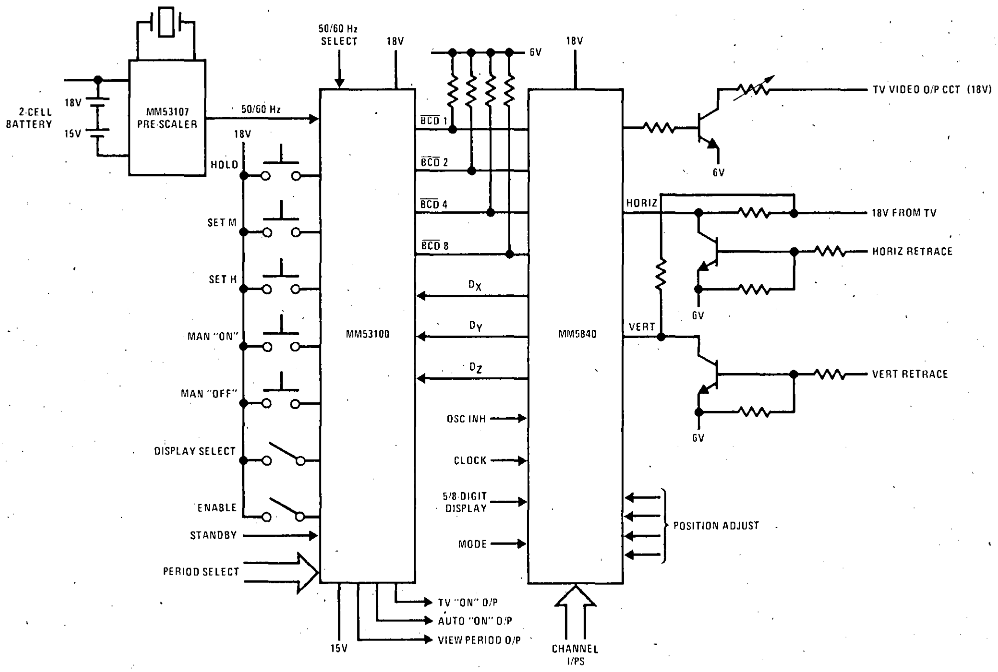


FIGURE 5a. Typical System Diagram, MM53100

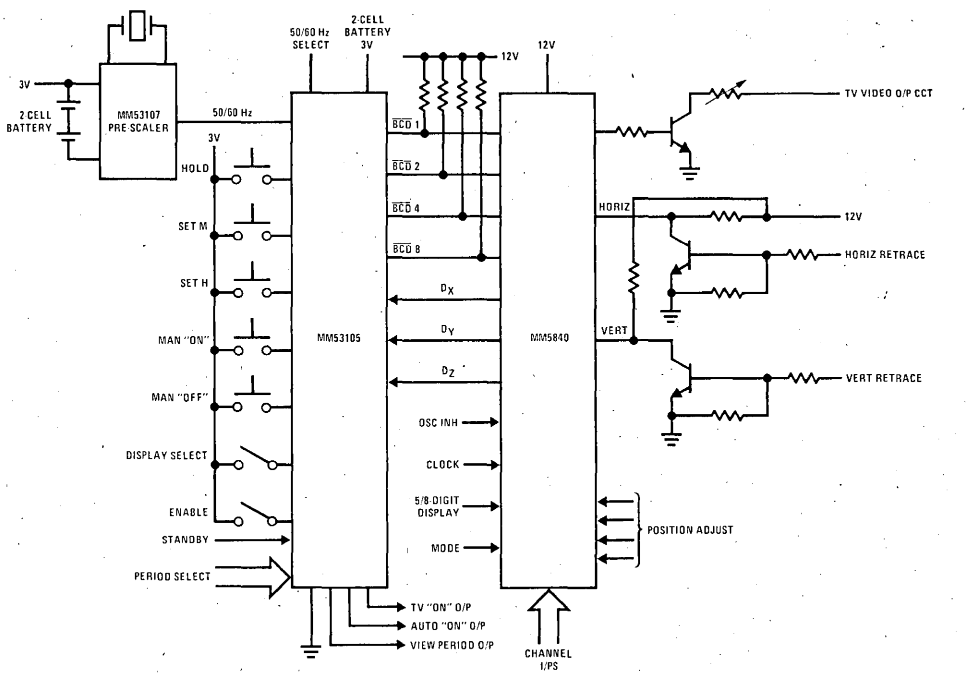


FIGURE 5b. Typical System Diagram, MM53105

TV Circuits

Note. SK1115 kit includes: MM57100N, MM53104N and LM1889N

MM57100 TV game circuit general description

The MM57100 TV Game Chip provides all of the logic necessary to generate backgrounds, paddles, ball and digital scoring for three games: Hockey, Tennis and Handball. All games are in color and have sound. The MM57100 was designed for low system cost and is aimed at the high volume consumer marketplace. It generates all the necessary timing (sync, blanking and burst) to interface to a standard TV receiver, and interfaces directly to the antenna terminals of a TV with the addition of a chroma, audio and RF modulator. If mounted directly into a receiver, much of this circuitry can be eliminated. The chip requires the true and complement clocks of 1.0227 MHz (3.579545 MHz ÷ 3.5). *Figure 1* shows a block diagram of a complete TV Game System.

The paddles for the games are controlled by two external RC networks. R and C provides for full screen movement by developing a time delay of about 16.5 ms. For Hockey and Tennis, each of the player paddles can be made to be either large, medium or small in size, thus allowing for handicapping. The size of a player paddle is modified by moving the paddle to either the top or bottom boundary and depressing the game reset button. In Handball, the players can modify the paddles as described above, but both players must use the same size paddle.

Single player "practice," can be created by connecting the two player paddle input lines on the MM57100 to a single external RC network. Single player operation can be achieved for all three games. Thus the MM57100 can actually play six games—three single player games and three dual player games.

The player paddles are divided into nine different areas that define eight angles at which the ball will reflect upon incidence. The top-most area of the player paddle will reflect the ball with the most upward direction, the areas towards the bottom will reflect the ball with the most downward direction. And the very bottom of the paddle will cause the ball to go up at a sharp angle, simulating a "wood" or handle shot. The areas in between will give reflections with less of an angle. There are two areas in the center of the player paddle which will make the ball have zero vertical velocity. The player paddles are transparent in one direction so that in Hockey the ball can rebound off the back wall and pass through the defensive player paddle. The machine paddles in Hockey are also transparent in one direction.

The ball is always served by the player who won the last point. The serve comes about 1.6 seconds from the time of the score and it is served from the paddle. This allows for a more realistic situation: the server can "place" his shot. After four player paddle hits, the ball speeds up to twice the initial velocity. Each time the ball strikes an object, a signal is generated at the audio output for the duration of the frame and one more full frame. When the ball strikes the boundaries or a machine paddle, it bounces off the object under the rule that the angle of incidence is equal to the angle of reflection. Regardless of the angle that the ball is traveling as it hits the front of the player paddles, it will reflect as a function of which segment it hits.

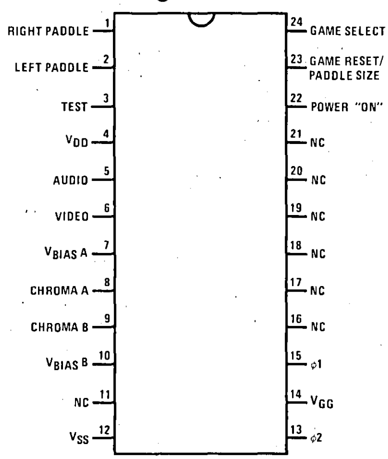
The score is automatically blanked when the ball is put into play. It remains blanked until a miss is recorded and it is then properly incremented and displayed. The game is completed when one of the players reaches 15 points. At this time, the score remains on and the serve is inhibited until the Game Reset is depressed. Both the Game Reset and Game Select inputs are debounced for 16.5 ms.

The video output signal contains horizontal and vertical blanking, horizontal and vertical sync and the black and white information necessary to generate the picture on a TV receiver through the antenna input. The picture is not interlaced. Chroma outputs provide the color and burst information and are properly timed with the video.

features

- Three games: Hockey, Tennis and Handball
- All games in full color
- Ball speed doubles after fourth hit
- Segmented paddles for automatic ball spin
- Adjustable paddle size/handicapped play
- Automatic digital scoring
- Sound
- Serve from paddles
- Designed to interface with a minimum effort to a standard television receiver

connection diagram (DIP Top View)



Order Number MM57100N
See Package 22

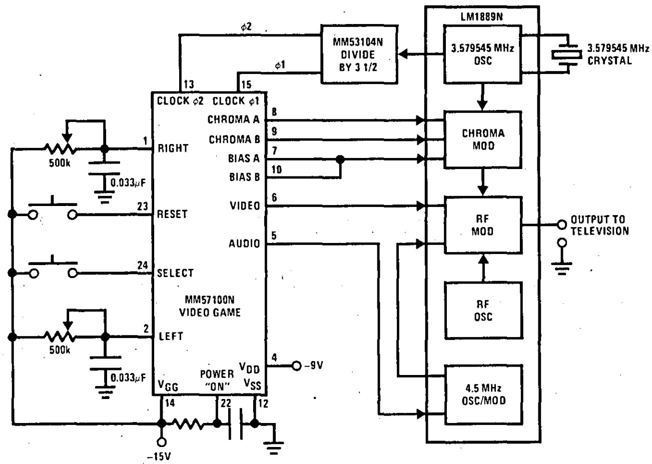


FIGURE 1. Video Game System Diagram

GAME DESCRIPTION

Tennis

Tennis consists of a green court with a blue border, a yellow net, orange paddles and a light green ball. It is played by two players who, through the use of their individual controllers, can vertically raise or lower their paddles. Play starts when the machine automatically serves the ball cross court. This can be from either the left or the right. The player who is served must hit the ball back to his opponent, who must then return it.

As the volley begins, the speed of the ball increases once, making it more difficult to return. The speed change occurs on the fourth hit. When either player misses the ball, a point is scored for his opponent and the next serve comes to him after a wait of 1.6 seconds. To increase the play value, the ball can bounce off both the top and bottom walls. In addition, before the play begins, each player can choose a large, medium or small paddle, depending on his playing skill. The paddles are sectioned, giving a "spin" effect to the ball.

The score, which is yellow, is automatically displayed in large, easy-to-read numerals. The score appears when the ball is missed and remains on until the ball is served. Play ends when the first player reaches 15 points. At the end of the game, the score remains on until the game is reset.

Hockey

Hockey consists of a blue playing field which is surrounded by yellow walls, two yellow player-controlled goalies, six light yellow machine-controlled forwards and a light blue hockey puck.

Hockey, while similar to tennis, is a much faster and more exciting game. Each player controls only his goalie, who moves in a vertical motion. In addition, each player has three forward men who also move vertically. These men are not under player control but move up and down, as a group, automatically. As in tennis, the opening serve comes cross court and can come to either player. Further serves are to the player who has just lost a point.

Since each player has four men who can return the puck, the play is very fast. To make it even more difficult, a point can only be made when the puck slips through either player's goal — a small opening located directly in the middle of the side walls. Since only a small portion of the left and right walls is used for scoring, the puck can essentially rebound off all four walls. Scoring is the same as in tennis — first player to reach 15 is the winner. The score is yellow.

Handball

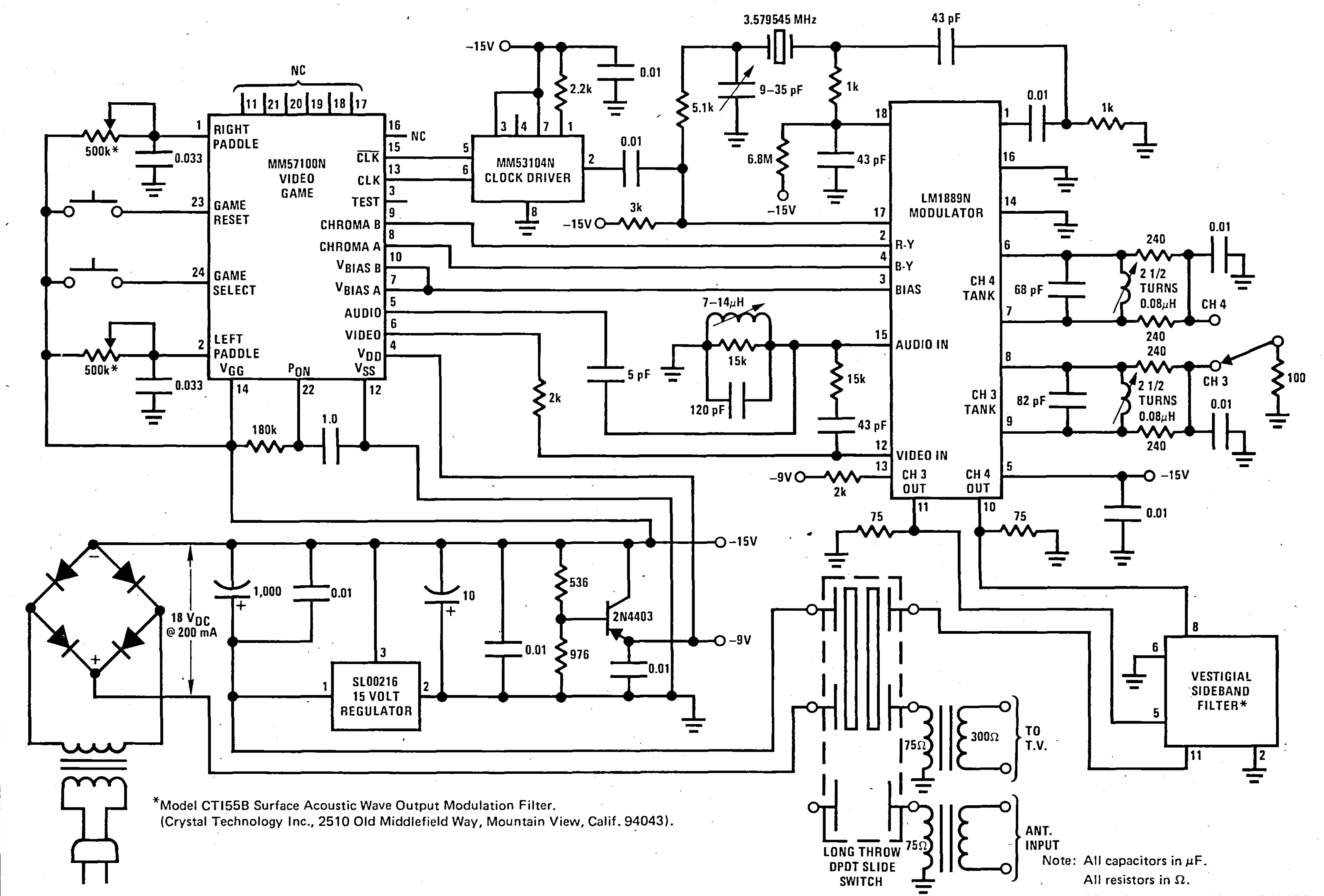
Handball consists of a brown court, two paddles — one blue and one orange, and a yellow ball. It plays identical to tennis except only one player plays at a time and both are on the same side of the court, playing against the opposite wall. After the ball is served, the serving player disappears from the screen and the other player's paddle appears. He must hit it, or he loses the point and the other player serves again. If he hits it, his paddle disappears and the other paddle comes on the screen. The other player must return it to the wall. The object of the game is to keep the ball in play by continuously hitting it to the back court wall. The ball can be reflected off three sides — the top, bottom and right wall. The first player to score 15 is the winner. The score colors match the paddle colors — one blue and one orange.

SUMMARY

Table 1 describes how the game will appear on a standard 25" TV. The actual appearance will vary somewhat from set to set as a function of color control settings, fine tuning, overscan, etc. Table 2 and *Figure 10* define the Chroma Outputs and the approximate color they generate.

SYSTEM CONFIGURATION

Figure 2 is a detailed schematic of how the MM57100 TV Game Chip would appear in a completed system, including the MM53104 clock generator and the LM1889 channel modulator.



*Model CTI55B Surface Acoustic Wave Output Modulation Filter. (Crystal Technology Inc., 2510 Old Middlefield Way, Mountain View, Calif. 94043).

Note: All capacitors in μF.
All resistors in Ω.

*CENTRALAB Model 2 ULTRALIFE potentiometer or equivalent.

FIGURE 2. Schematic Diagram

dc electrical characteristics $0°C \leq T_A \leq 75°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltages					
$V_{SS} - V_{DD}$	$14.25 \leq V_{SS} - V_{GG} \leq 15.75$	8.5	9	9.5	V
$V_{SS} - V_{GG}$	$8.5 \leq V_{SS} - V_{DD} \leq 9.5$	14.25	15	15.75	V
Operating Supply Current					
I_{DD}	$V_{DD} = V_{SS} - 9.5V$		35		mA
I_{GG}	$V_{GG} = V_{SS} - 15.75V$		15		mA
Osc. Input Levels, $\phi1$, $\phi2$ *(Figure 3)*					
V_{IH} Logical High Level		$V_{SS}-0.5$		V_{SS}	V
V_{IL} Logical Low Level		V_{GG}		$V_{GG}+0.5$	V
Chroma A Output Levels *(Figure 4)*	$C_L = 50$ pF, $I_{DC} = 0$, $8.5 \leq V_{SS} - V_{DD} \leq 9.5$, (Typical values are for $V_{SS} - V_{DD} = 9V$). All voltages specified with respect to V_{DD}				
V_{A1} $A1 = 0.465 \times (V_{SS} - V_{DD})$		3.95	4.18	4.42	V
Ro_{A1} Output Impedance		900		2060	Ω
V_{A0} $A0 = 0.298 \times (V_{SS} - V_{DD})$		2.53	2.68	2.83	V
Ro_{A0} Output Impedance		790		2060	Ω
V_{ABURST} $A_{BURST} = 0.238 \times (V_{SS} - V_{DD})$		1.82	1.93	2.04	V
Ro_{ABURST} Output Impedance		710.0		2030	Ω
V_{A3} $A3 = 0.134 \times (V_{SS} - V_{DD})$		1.13	1.2	1.27	V
Ro_{A3} Output Impedance		520.0		2100	Ω
Chroma B Output Levels *(Figure 4)*	$C_L = 50$ pF, $I_{DC} = 0$, $8.5 \leq V_{SS} - V_{DD} \leq 9.5$. (Typical values are for $V_{SS} - V_{DD} = 9V$). All voltages specified with respect to V_{DD}				
V_{B1} $B1 = 0.465 \times (V_{SS} - V_{DD})$		3.95	4.18	4.42	V
Ro_{B1} Output Impedance		900		2060	Ω
V_{B0} $B0 = 0.298 \times (V_{SS} - V_{DD})$		2.53	2.68	2.83	V
Ro_{B0} Output Impedance		790		2060	Ω
V_{B3} $B3 = 0.134 \times (V_{SS} - V_{DD})$		1.13	1.2	1.27	V
Ro_{B3} Output Impedance		520		2100	Ω
Chroma A Bias and Chroma B Bias Output Levels	$C_L = 50$ pF, $I_{DC} = 0$, $8.5 \leq V_{SS} - V_{DD} \leq 9.5$. (Typical values are for $V_{SS} - V_{DD} = 9V$). All voltages specified with respect to V_{DD}				
V_{BIASA}, $V_{BIASB} = 0.298 (V_{SS} - V_{DD})$		2.53	2.68	2.83	V
Ro_{BIASA}, Ro_{BIASB}		790		2060	Ω
Chroma and Chroma Bias Output Offset Voltages	$C_L = 50$ pF, $\lvert I_{DC}\rvert \leq 50\mu A$, $\lvert I_{CHROMA} - I_{BIAS}\rvert \leq 5\mu A$, $\lvert I_{CHROMAA} - I_{CHROMAB}\rvert \leq 5\mu A$				
V_{OS}			10	50	mV

dc electrical characteristics (con't) $0°C \leq T_A \leq 75°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Video Output Levels *(Figure 5)*	C_L = 50 pF, I_{DC} = 0, 8.5 = $V_{SS} - V_{DD} \leq 9.5$. All voltages specified with respect to V_{DD}.(Typical values are for $V_{SS} - V_{DD}$ = 9V)				
V_{SYNC}	V_{SYNC} = 0.444 x ($V_{SS} - V_{DD}$)		3.77	4	4.22	V
Ro_{SYNC}	Output Resistance		906		2080	Ω
V_{BLANK}	V_{BLANK} = 0.333 x ($V_{SS} - V_{DD}$) = 0.75 x V_{SYNC}		2.83	3	3.18	V
Ro_{BLANK}	Output Resistance		835		2080	Ω
V_{DARK}	V_{DARK} = 0.242 x ($V_{SS} - V_{DD}$) = 0.545 x V_{SYNC}		2.06	2.18	2.30	V
Ro_{DARK}	Output Resistance		726		2030	Ω
V_{LIGHT}	V_{LIGHT} = 0.148 x ($V_{SS} - V_{DD}$) = 0.383 x V_{SYNC}		1.26	1.33	1.41	V
Ro_{LIGHT}	Output Resistance		556		2040	Ω
	Audio Output Level *(Figure 6)*	R_{LOAD} = 100k, C_{LOAD} = 20 pF				
V_{OUT}				V_{DD}		V
	Output Resistance to V_{DD}					
Ro"ON"	"ON" Resistance	$V_{OL} \leq V_{DD}$ +0.5		1.0	5	kΩ
Ro"OFF"	"OFF" Resistance	$V_{OH} \geq V_{DD}$ + 3.0	50	500		kΩ
C_{OUT}				5		pF
	Reset, Test and Game Select Input Levels					
V_{IH}	Logical High Level		V_{SS}−1.5		V_{SS}	V
V_{IL}	Logical Low Level		V_{DD}		V_{DD}+2.5	V
	Paddle 1 and Paddle 2 Input Levels *(Figure 7)*	$8.5 \leq V_{SS} - V_{DD} \leq 9.5$				
V_{PI}	Input Trip Level		V_{DD}−0.4	V_{DD}	V_{DD}+0.4	V
V_{OH}	Logical High Output Reset Level	R_{LOAD} = 15 kΩ to V_{GG}, C_{LOAD} = 0.1μF, 10%	V_{SS}−2.5		V_{SS}	V
	Power "ON" Clear Input Levels *(Figure 8)* See Note 6					
V_{CLR}	Input Trip Level	R_{LOAD} = 180k, 10%, C_{LOAD} = 1μF, 10%	V_{DD} −0.5	V_{DD}	V_{DD}+0.5	V
V_{OH}	Logical High Output Reset Level		V_{SS}−2.5		V_{SS}	V
e_n	**Noise Levels on Chroma A, Chroma B, and Video Outputs**	$8.5 \leq V_{SS} - V_{DD} \leq 9.5$, $14.25 \leq V_{SS} - V_{GG} \leq 15.75$, C_{LOAD} = 50 pF, $\lvert I \rvert \leq 50\mu A$	−200		200	mV

Note 1: Chroma A, Chroma B and the Chroma bias output levels are specified for dc current = 0. Typical dc loading conditions are 30μA or less. The resistor network in *Figure 9(a)* can be used to determine the shift and interaction in outputs for dc load conditions.

Note 2: Video output levels are specified for dc current = 0. Any other loading conditions will influence the output levels and the resistor network in *Figure 9(b)* can be used to calculate output levels. Typical dc currents are 30μA or less.

Note 3: All diffused resistors have a ±30% tolerance, and tracking of tolerance can be assumed.

Note 4: All MOS switch impedances include all variations, i.e., due to process, and supply variations, tracking of MOS switch impedances can be assumed.

Note 5: Tracking of diffused resistor tolerances and MOS device tolerances *cannot* be assumed.

Note 6: Power On Clear input pin is reset by the MM57100 to the V_{OH} level near the end of the internal Power On Clear cycle, as shown in *Figure 8.*

ac electrical characteristics (0°C to +70°C, except where otherwise noted)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Osc Inputs, $\phi 1$ and $\phi 2$ Input Frequency *(Figure 3)*			1.0227		MHz
	Rise and Fall Times					
t_r, t_f					40	ns
t_{dL1}					10	ns
t_ϕ				0.9778		µs
t_{pw1}			0.405			µs
t_{pw2}			0.380			µs
V_{OL1}			$V_{SS}-1.0$	$V_{SS}-0.5$	V_{SS}	V
V_{OL2}			$V_{SS}-2.0$	$V_{SS}-1.0$	V_{SS}	V
	Chroma A and Chroma B Output Timing *(Figure 4)*	$C_L = 50$ pF, $I_{DC} \leq 50\mu A$				
t_{rA}				175	225	ns
t_{fA}				175	225	ns
t_{rB}				175	225	ns
t_{fB}				175	225	ns
t_{SCB}				450		ns
t_{rCB}				175		ns
t_{fCB}				175		ns
t_{CL1}				0		ns
t_{CL2}				0		ns
t_{BURST}				2900		ns
	Video Output Timing *(Figure 5)*	$C_{LOAD} = 50$ pF, $\lvert I_{DC} \rvert \leq 50\mu A$				
t_{rv}				250	500	ns
t_{fv}				250	500	ns
t_{rS}				250	500	ns
t_{fS}				250	500	ns
t_{rL}				150	225	ns
t_{fL}				150	225	ns
t_{bp}				5		µs
t_{SYNC}				4.5	4.9	µs
t_{fp}				1	1.25	µs
t_{VIDEO}				0.97		µs
t_{BLANK}			10.5	11	11.9	µs
	Audio Output Timing *(Figure 6)*	$\phi 1$, $\phi 2$ inputs = 1.0227 MHz, $C_{LOAD} = 20$ pF				
f_a	Output Frequency	$\lvert I_{DC} \rvert \leq 50\mu A$		491		Hz
	Audio Tone Duration					
t_{ON}			18.55		30.25	ms
t_{OFF}				15		µs
t_{ra}, t_{fa}		$C_{LOAD} = 20$ pF, $R_{EXT} = 120k$ to V_{SS}		10		µs
t_{ha}				1		ms
t_{pwa}				2.037		ms
	Player Paddle Timing *(Figure 7)*	$C_{LOAD} = 0.1\mu F + 10\%$, $R_{LOAD} \geq 15\ k\Omega$ (to V_{GG})				
t_{PH}	Paddle High (25H)		1.58			ms
t_{PL}	Paddle Low (215H)				13.7	ms
t_{RP}					1.2	ms
	Power "ON" Clear Timing *(Figure 8)*	RC > 138 ms, R = 180k, 10%; C = 1µF, 10%				
t_{dcl}			60			ms
t_{POWER}					30	ms

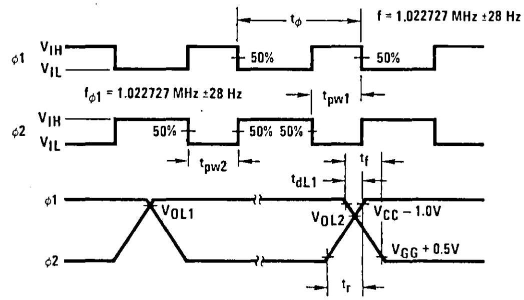


FIGURE 3. Input Clock Waveforms

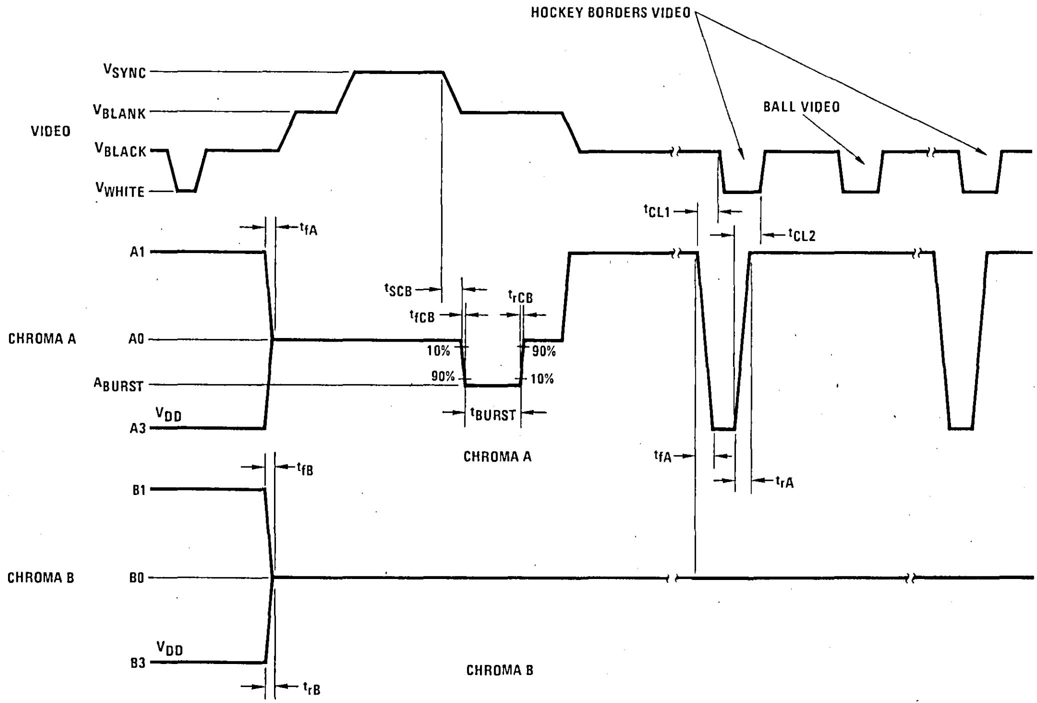
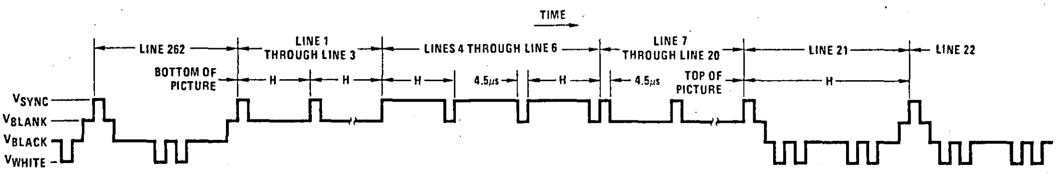


FIGURE 4. Video-Chroma Timing



H ≅ 63.557μs

Note: Interlaced scan and equalization pulses are not used.

FIGURE 5(a). Video Output Waveform

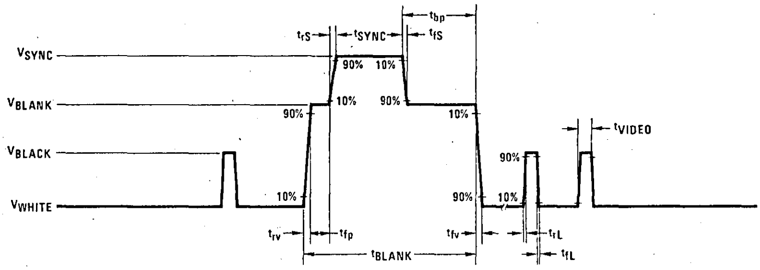


FIGURE 5(b). Composite Video Timing and Levels

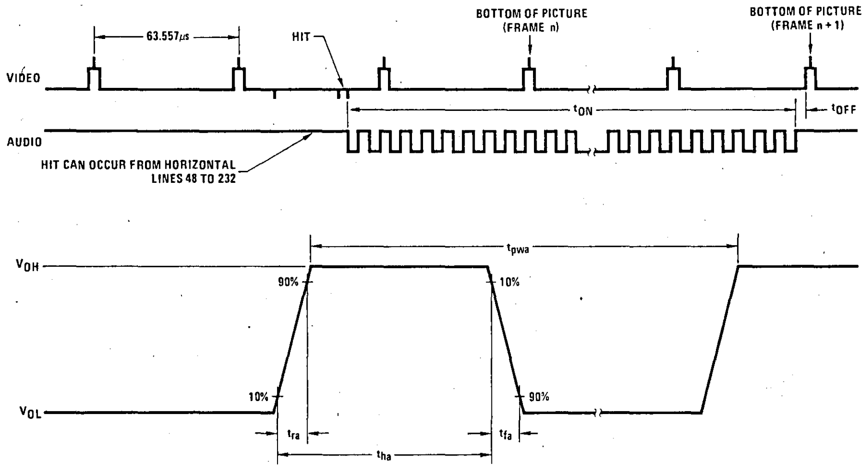


FIGURE 6. Audio Output Timing

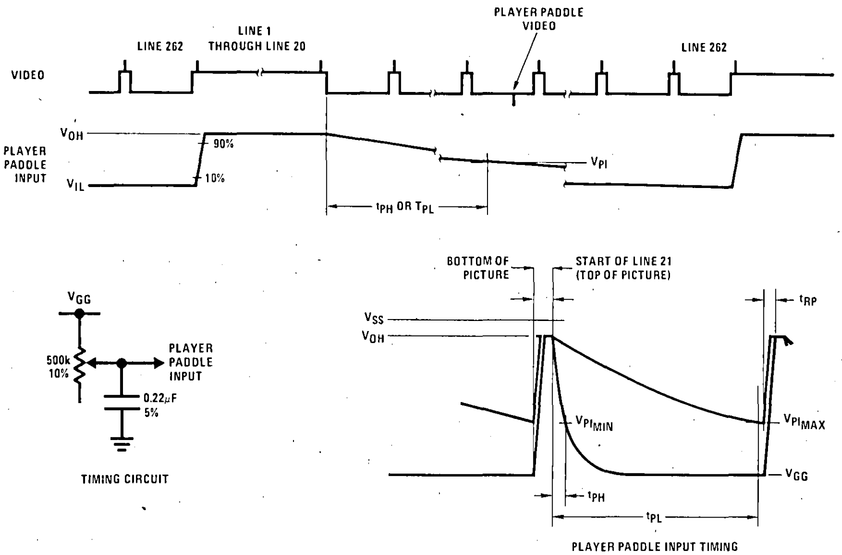
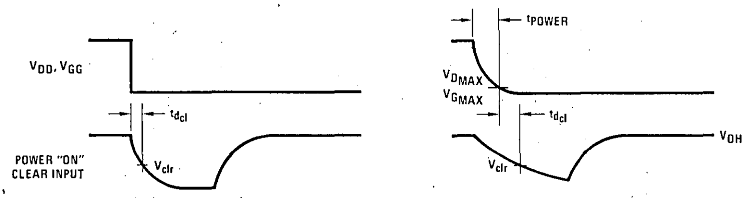


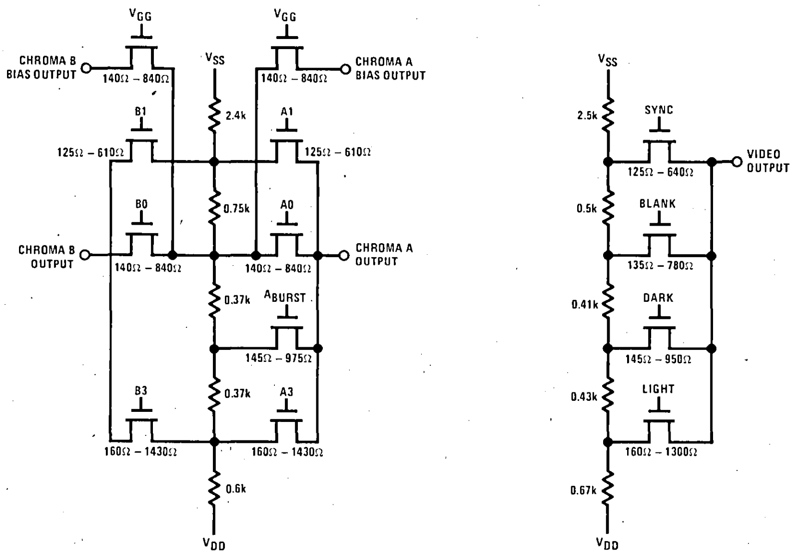
FIGURE 7. Player Paddle Inputs



(a) Fast Power Supply Edges

(b) Slow Power Supply Edges

FIGURE 8. Power "ON" Clear Input Timing



(a)

(b)

FIGURE 9. Chroma and Video Output Networks (See Notes on Page 4-41)

TABLE I. Game Colors and Size on a 25" TV

ELEMENT	CHROMA OUTPUT	VIDEO OUTPUT	APPR. COLOR	APPR. SIZE	COMMENTS
Tennis Background	A1B0	Light	Blue		
Tennis Field	A0B3	Dark	Cyan	13.2 x 16.8 inches^2	
Tennis Ball	A0B3	Light	Cyan	0.5 x 0.5 inches^2	
Tennis Score	A3B0	Light	Yellow	4 x 5 inches^2	Blanked during play
Tennis Net	A3B0	Light	Yellow	0.5 x 13.2 inches^2	
Tennis Left Player	A3B1	Light	Orange	3 sizes	2.4, 1.2 or 0.6 inches x 0.5 inches independent of other paddle
Tennis Right Player	A3B1	Light	Orange	3 sizes	2.4, 1.2 or 0.6 inches x 0.5 inches independent of other paddle
Handball Background	A3B0	Light	Yellow		
Handball Field	A3B0	Dark	Yellow	13.2 x 16.8 inches^2	
Handball Ball	A3B0	Light	Yellow	0.5 x 0.5 inches^2	
Handball Left Score	A3B1	Light	Orange	4 x 5 inches^2	Blanked during play
Handball Right Score	A1B0	Light	Blue	4 x 5 inches^2	Blanked during play
Handball Left Player	A3B1	Light	Orange	3 sizes	2.4, 1.2 or 0.6 x 0.5 inches, same as other paddle
Handball Right Player	A1B0	Light	Blue	3 sizes	2.4, 1.2 or 0.6 x 0.5 inches, same as other paddle
Hockey Background	A1B0	Dark	Blue		
Hockey Field	A1B0	Dark	Blue	13.2 x 16.8 inches^2	
Hockey Border	A3B0	Light	Yellow		
Hockey Puck	A1B0	Light	Blue	0.5 x 0.5 inches^2	
Hockey Score	A3B0	Light	Yellow	4 x 5 inches^2	Blanked during play
Hockey Left Player	A3B0	Light	Yellow	3 sizes	2.4, 1.2 or 0.6 x 0.5 inches independent of other paddle
Hockey Right Player	A3B0	Light	Yellow	3 sizes	2.4, 1.2 or 0.6 x 0.5 inches independent of other paddle
Hockey Machine Forwards	A3B0	Light	Yellow	0.5 x 0.6 inches^2	
Hockey Goals	A1B0	Light	Blue	4.6 x 0.5 inches^2	Hole in the Border

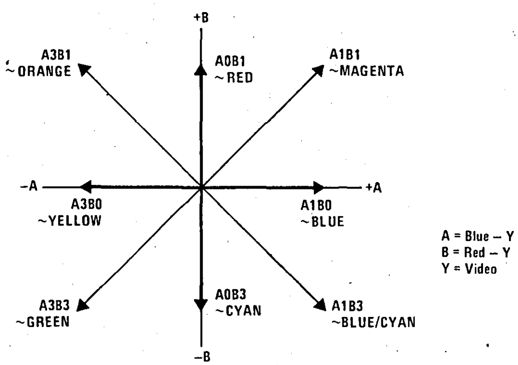


FIGURE 10. Chroma Outputs/Color Phase Diagram

TABLE II. Chroma Outputs vs Approximate Color

CHROMA A AND CHROMA B OUTPUTS	APPROXIMATE COLOR
A0, B0	Light Gray
A0, B1	Red
A0, B3	Cyan
A1, B0	Blue
A1, B1	Magenta
A1, B3	Blue Cyan
A3, B0	Yellow
A3, B1	Orange
A3, B3	Green
A_{BURST}, B0	Color Burst

DESIGN CONSIDERATION FOR THE PLAYER PADDLE INPUTS

Calculations are based on an input waveform at the "PLAYER PADDLE" input:

$$V_{IN} = V_{IH} + (1 - e^{-t/RC})(V_{GG} - V_{IH})$$

A solution for t = RC is done, at the input trip point where $V_{IN} = V_{TRIP} = V_{DD} \pm 0.4V$, and $t = t_d$.

$$RC = \frac{-t_d}{\ln\left[\frac{V_{GG} - V_{DD} \pm 0.4V}{V_{GG} - V_{IH}}\right]}$$

Over the design range of V_{DD}, V_{GG} and V_{IH}, the denominator has a range

$$-1.187 \leq \ln(x) \leq -0.5864 \text{ where } x = \frac{V_{GG} - V_{DD} \pm 0.4V}{V_{GG} - V_{IH}}$$

The time delays required vary from a minimum of t_{dT} = 1.58 ms for the player paddle positioned at the top of the screen, to a delay of t_{dB} = 13.7 ms for the player paddle positioned at the bottom of the screen. For these time delays, the ranges of RC are:

$$(RC)_{T_{MIN}} = 1.33\text{ ms} \leq \frac{t_{dT}}{\ln\left[\frac{V_{GG} - V_{DD} \pm 0.4V}{V_{GG} - V_{IH}}\right]} \leq (RC)_{T_{MAX}} = 2.69\text{ ms}$$

for the upper paddle position and

$$(RC)_{B_{MIN}} = 11.54\text{ ms};\ (RC)_{B_{MAX}} = 23.36\text{ ms}$$

for the lower paddle position.

Thus, the external RC network must guarantee a minimum RC of 1.33 ms or less and a maximum RC of 23.36 ms or greater.

Calculations of potentiometer resistance based on a linear pot use the formula:

$$R_\theta = \frac{\theta \times R_p}{\theta_{fs}} \pm R_p \cdot L$$

where: R_θ is the potentiometer tap resistance
θ is the angle of pot rotation beyond 0
θ_{fs} is the full scale rotation of the pot, ± tolerance
R_p is the full scale resistance of the pot, ± tolerance
L is the linearity of the pot

Using RC = t_d, values of θ can be calculated for the required extremes using the expression:

$$\theta = \frac{\left(\frac{t_d}{C} \pm R_p \cdot L\right)\theta_{fs}}{R_p}$$

This expression assumes prior selection of R_p, L, θ_{fs}, and C. This expression can be modified to calculate R_p or C if there is any restriction on the upper limit of θ.

Mechanical variations, either in the potentiometer or the control housing which affect pot rotation should also be considered.

TIMING AND LEVEL DEFINITIONS

t_r, t_f	Rise and fall times of $\phi 1$ and $\phi 2$ clock inputs.
t_{dL1}	Delay from the V_{SS} − 1V point of the $\phi 2$ positive transition to the V_{SS} − 1V point of the $\phi 1$ negative transition.
t_ϕ	Clock cycle time.
t_{PW1}	Time from 50% point on negative edge of $\phi 2$ to the 50% point on the negative edge of $\phi 1$.
t_{PW2}	Pulse width of the $\phi 2$ input, at the 50% point.
V_{OL1}	Crossover point where $\phi 1 = \phi 2$ and $\phi 1$ is on a negative transition.
V_{OL2}	Crossover point where $\phi 1 = \phi 2$ and $\phi 1$ is on a positive transition.
t_{rA}, t_{rB}, t_{fA}, t_{fB}	Rise and fall times of the chroma A and chroma B outputs.
t_{SCB}	Delay from start of sync pulse trailing edge to the start of the chroma A output color burst leading edge.
t_{rCB}, t_{fCB}	Rise and fall times of the chroma A output color burst pulse.
t_{BURST}	Chroma A output color burst pulse width.
t_{CL1}	Delay from the start of a chroma output negative transition to the start of the VIDEO output (luminance) transition.
t_{CL2}	Delay from the start of a chroma output positive transition to the start of the VIDEO output (luminance) transition.
t_{rv}, t_{fv}	Rise and fall times of the VIDEO output blanking pulse.
t_{rS}, t_{fS}	Rise and fall times of the VIDEO output SYNC pulse.
t_{rL}, t_{fL}	Rise and fall times of the VIDEO output luminance pulses.
t_{fp}, t_{bp}	Duration of the VIDEO output front porch and back porch.
t_{SYNC}	Duration of the VIDEO output SYNC pulse.
t_{VIDEO}	Duration of the VIDEO output luminance pulses.
t_{BLANK}	Duration of the VIDEO output blanking pulse.
t_{ON}	Duration of the AUDIO output "HIT" tone burst.
t_{OFF}	Delay from the end of the AUDIO output "HIT" tone burst to the start of the VIDEO output blanking pulse.
t_{ra}, t_{fa}	Rise and fall times of the AUDIO output.
tha	Width of the AUDIO output tone pulse positive level.
t_{pwa}	AUDIO output tone cycle time ($t = 1/f_{AUDIO}$)
t_{RP}	Rise time of the PLAYER PADDLE input.
t_{PH}	Delay time from the top of the picture to the highest player paddle position.
t_{PL}	Delay time from the top of the picture to the lowest player paddle position.
t_{dcl}	Delay from point where the power supplies are within the operating spec to the point where the power-on clear input level is less than V_{CLRI}.
t_{POWER}	Fall time of the power supply at turn-on, to 95% point.
H	One horizontal scan line.

4

TV Circuits

Note. SK1115 kit includes: MM57100N, MM53104N and LM1889N

LM1889 TV video modulator

general description

The LM1889 is designed to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, and R.F. oscillators and modulators for two low-VHF channels.

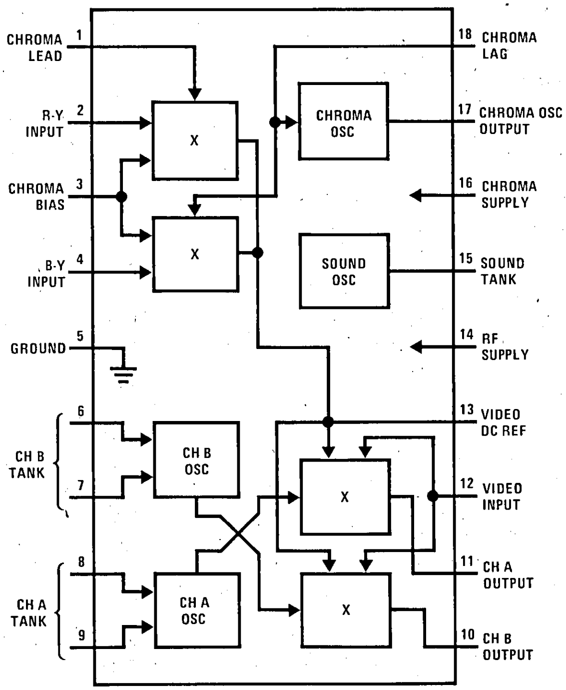
The LM1889 allows video information from VTR's, games, test equipment, or similar sources to be displayed on black and white or color TV receivers. When used with the MM57100 and MM53104, a complete TV game is formed.

features

- DC channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video

block diagram

Dual-In-Line Package

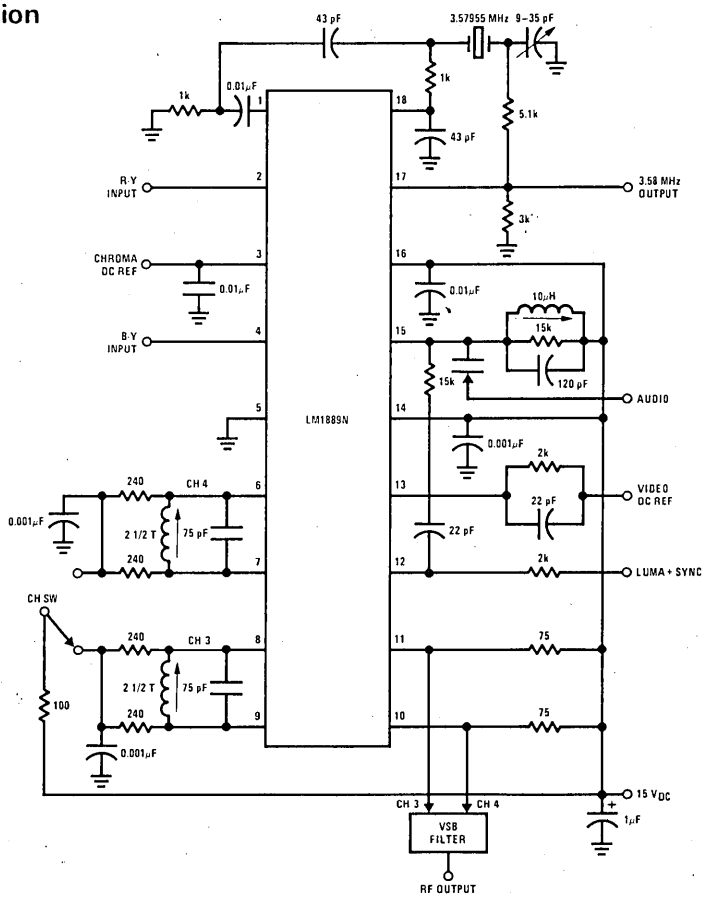


Order Number LM1889N
See Package 20

tentative electrical characteristics (Applications circuit, V = 15V)

	TYP
Supply Voltage Range V14, V16	12–18 V_{DC}
Total Supply Current $I_{14} + I_{16}$	35 mA_{DC}
Common-Mode Input Range	
Chroma Mod. V2, V3, V4	4–10.5 V_{DC}
RF Mod. V12, V13	3.5–11 V_{DC}
Oscillator Levels	
Sound Osc V15	3.5 Vp-p
Chroma Osc V17	5 Vp-p
RF Osc V6, V7 or V8, V9	300 mVp-p
Chroma Modulator Conversion Gain	
V13 Out/V4–V3	0.6 Vp-p/V_{DC}
V13 Out/V2 – V3	0.6 Vp-p/V_{DC}
Residual Chroma Output, V13 V2 = V3 = V4	50 mVp-p
RF Modulator Conversion Gain V10 or V11/V12-V13	10 mVrms/V_{DC}

typical application



TV Circuits

Note. SK1115 kit includes: MM57100N, MM53104N and LM1889N

MM53104 TV game clock generator

general description

The MM53104 is a monolithic CMOS clock generator designed to generate the 2-phase non-overlapping clocks, ϕ_1 and ϕ_2, for the MM57100 TV game chip.

The MM53104 contains two independent oscillator circuits that can either be driven by an external input or be used as a Colpitts-type oscillator (e.g., crystal oscillator). The first oscillator (X1, X2) is designed to operate at 3.58 MHz and the output (X2) is fed internally to a divide-by-3 1/2 counter to generate the 1.0227 MHz ϕ_1 and ϕ_2 outputs required by the MM57100. The second oscillator (Y1, Y2) is a completely independent oscillator and is designed for a 4.5 MHz operation.

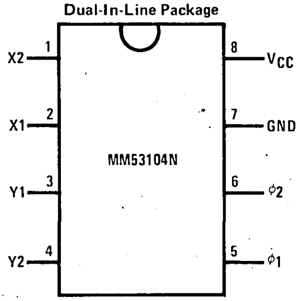
All pins are protected against static damages by diode clamps to both V_{CC} and ground.

features

- Directly drives MM57100
- Two on-chip oscillator circuits
- Low power consumption 250 mW typ @ 15V

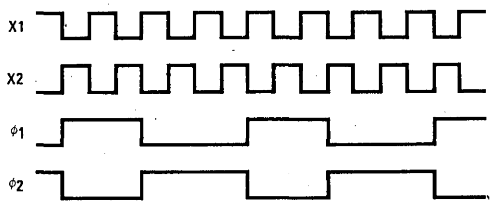
connection diagram

Dual-In-Line Package

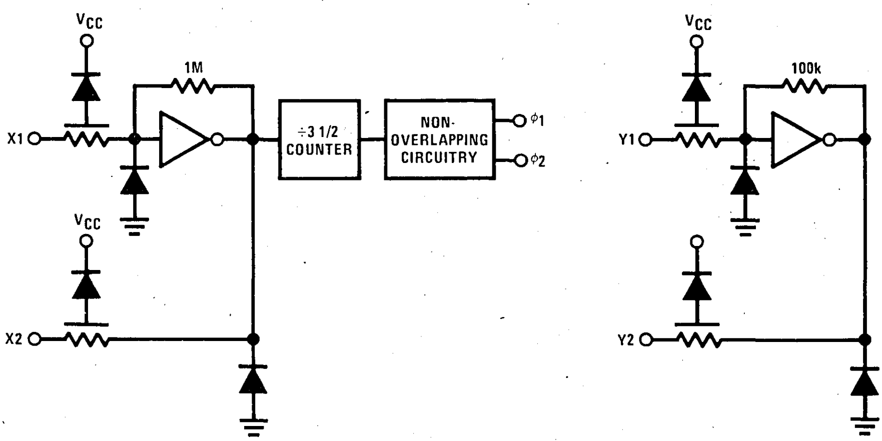


TOP VIEW
Order Number MM53104N
See Package 17

timing diagram



logic diagrams



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
V_{CC}	−0.3V to 16V
Recommended V_{CC}	15V ±5%
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics $14.25V \leq V_{CC} \leq 15.75V$

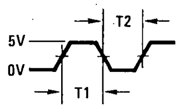
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	X1 = Y1 = V_{CC}			600	µA
	Operating Current	Y1 = GND		15		mA
V_{OH}	Output High Level, ϕ_1 or ϕ_2	V_{CC} = 15V	14.95			V
V_{OL}	Output Low Level, ϕ_1 or ϕ_2	V_{CC} = 15V			0.05	V
I_{OH}	Output Source Current, ϕ_1 or ϕ_2	V_{CC} = 15V, V_O = 13.5V	−7.0			mA
I_{OL}	Output Sink Current, ϕ_1 or ϕ_2	V_{CC} = 15V, V_O = 1.5V	11.0			mA

ac electrical characteristics V_{CC} = 15V, C_L = 15 pF, all limits apply across temperature.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
T_R	Rise Time of ϕ_1 or ϕ_2			15	30	ns
T_F	Fall Time of ϕ_1 or ϕ_2			15	30	ns
T_{PW,ϕ_1+}	Positive Pulse Width of ϕ_1		410	455	510	ns
T_{PW,ϕ_1-}	Negative Pulse Width of ϕ_1		470	520	570	ns
T_{PW,ϕ_2+}	Positive Pulse Width of ϕ_2		510	570	600	ns
T_{PW,ϕ_2-}	Negative Pulse Width of ϕ_2		380	410	470	ns
T_{W,ϕ_2-}	Effective Negative Pulse Width of ϕ_2		405	440		ns
T_{dL1}	ϕ_1 Overlapping ϕ_2 Time			−13	5	ns
T_{dL2}	ϕ_2 Overlapping ϕ_1 Time			−2	10	ns
V_{OL1}	ϕ_1 Cross-Over ϕ_2 Voltage		V_{CC}−1.0	V_{CC}		V
V_{OL2}	ϕ_2 Cross-Over ϕ_1 Voltage		V_{CC}−2.0	V_{CC}−0.8		V

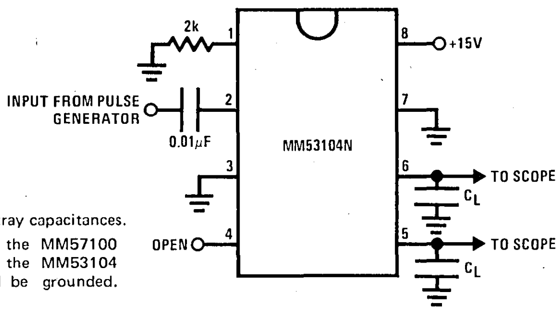
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

ac test circuit

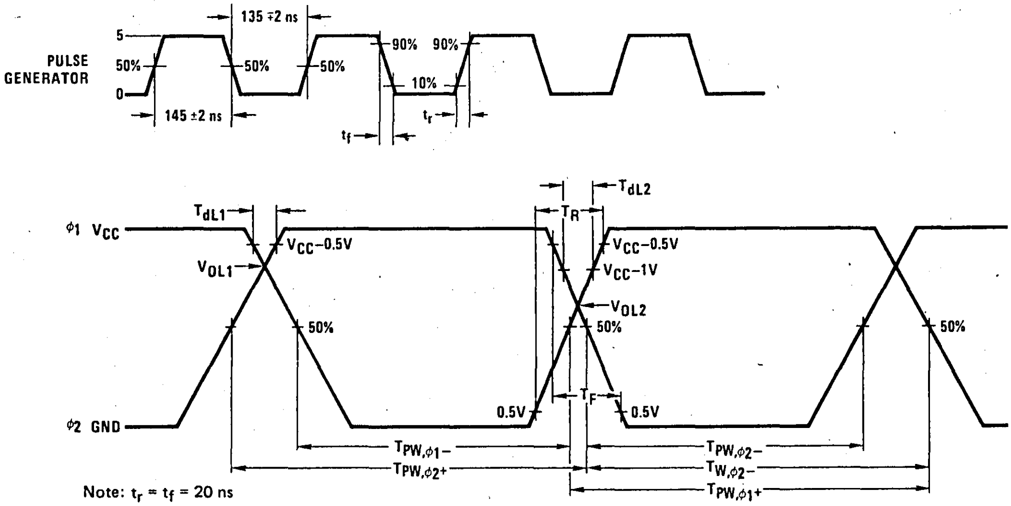


T1 = 145 ns
T2 = 135 ns
$t_r = t_f$ = 20 ns
C_L = 15 pF including scope probe and all stray capacitances.

Note: When the MM53104 is used with the MM57100 and LM1889, the 4.5 MHz oscillator in the MM53104 is not needed and thus pin 3 should be grounded.



switching time waveforms



Note: $t_r = t_f = 20$ ns

MM58106 digital clock and TV display circuit

general description

The MM58106 is a monolithic CMOS integrated circuit which generates a display of channel number and time on the television screen. The circuit can either display channel number (2–83) or program number (1–16). Time display can be 4 or 6-digit, in either 12 or 24-hour mode. Timekeeping is controlled from a 50 Hz or 60 Hz input. The position of the display on the TV screen is controlled by adjusting the external RC time constants.

The circuit is packaged in a 28-lead dual-in-line epoxy package.

features

- Single chip clock and display
- 12 or 24-hour operation
- 5 or 8-digit time display
- Channel or program number display
- 50/60 Hz operation
- Channel and time display on channel change

block diagram

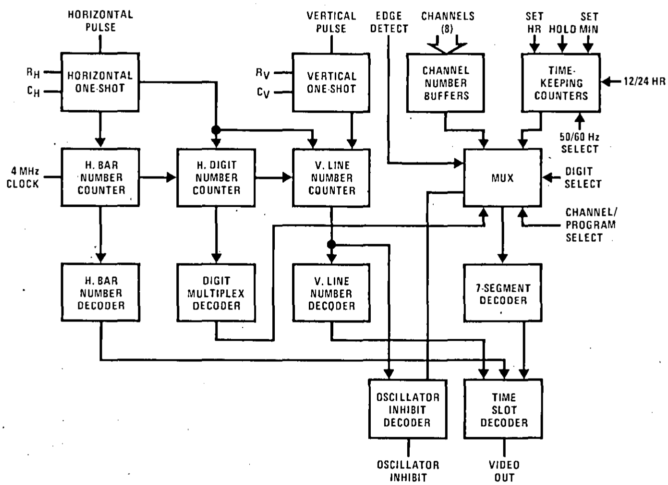


FIGURE 1

connection diagram

Dual-In-Line Package

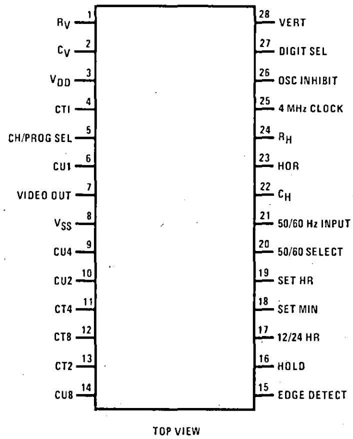


FIGURE 2

Order Number MM58106N
See Package 23

absolute maximum ratings

Supply Voltage ($V_{DD} - V_{SS}$)	5.5V
Voltage at Any Pin	V_{SS} – 0.3V to +5.5V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage, V_{DD}	V_{SS} = 0	4.75	5	5.25	V
Power Supply Current				800	μA
Input Voltage Levels					
Channel Inputs					
Logical Low		V_{SS}–0.3	V_{DD}–5	V_{DD}–4.5	V
Logical High		V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}–0.3	V_{DD}–5	V_{DD}–4.5	V
Logical High		V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Set Mins, Set Hours, Hold, 12/24-Hour Select, 50/60 Hz Select, Channel/ Program Select	Internal Pull-Up Resistor to V_{DD} (600k Min)				
Logical Low		V_{SS}–0.3	V_{SS}	V_{SS}+0.3	V
Logical High			Open		
All Others					
Logical Low		V_{SS}–0.3	V_{SS}	V_{SS}+0.3	V
Logical High		V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Input Frequency					
4 MHz Clock		1	4	4.5	MHz
Horizontal	Pulse Width = 14 μs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Oscillator Inhibit and Video Output					
Logical Low		V_{SS}–0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}–0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal			50		μs
Vertical			13		ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1V	(–1)			mA
Logical High	V_{DD} – 1V	1			mA
Oscillator Inhibit Output					
Logical Low	Output Forced Up to V_{DD}–4.5V	(–2)			mA
Logical High	V_{DD} – 1V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		μF
$C_{HORIZONTAL}$			0.001		μF
$R_{VERTICAL}$			100		kΩ pot
$R_{HORIZONTAL}$			100		kΩ pot
Propagation Delay Oscillator Inhibit Output	From Input Clock to Oscillator Inhibit Output			2	clock pulses
Input Leakage				1	μA
Input Capacitance				5	pF
Edge Detect Pulse Duration	C = 2 μF, R = 1 MΩ		2		sec

functional description

A block diagram of the MM58106 TV timer is shown in *Figure 1*. A connection diagram is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 1*.

50 or 60 Hz Input: This input has a shaping circuit which allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 4* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

Alternatively, in a crystal controlled battery operated system, an oscillator and prescaler circuit such as the MM5369 could be used as a timebase.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 pps timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{SS}. An internal 1 MΩ pull-up resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation.

Time Setting Inputs: Inputs to set hours and set minutes as well as a hold input, are provided. Internal 1 MΩ pull-up resistors provide the normal timekeeping function. Switching any one of these inputs (one at a time) to "0" results in the desired time setting function. Set Hours advances hours information at 1 hour per second, and Set Minutes advances minutes information at one minute per second, without roll over into the hours counter. The hold input stops the clock to the minutes counter and resets the seconds counter.

Display Control: The channel number and time display circuits operate from the 4 MHz input clock frequency. The horizontal and vertical position of the display is controlled by adjusting the external RC time constants (R_H, C_H, R_V, C_V).

These monostables are triggered by the horizontal and vertical retrace signals as shown in the timing diagram in *Figure 3*.

A 7-segment decoder is used to decode either channel inputs or time. Also a time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that can modulate the sweep of the television tube for the on-screen display.

Channel/Program Number Select: This control pin has a pull-up resistor to V_{DD} and, with the input open, the chip will accept a binary plus 1 code on the CU1 to CU8 inputs and display the program number. For example, an input code of 0000 will indicate channel 1 and 1111 will indicate channel 16.

With this input at "0", inputs CU1 to CU8 and CT1 to CT8 will accept BCD inputs for channel units and channel tens respectively, and display channels 2–83.

Edge Detect: On program change, the time and number will be displayed for a period depending on the external capacitor and resistor connected to the Edge Detect pin *(Figure 4)*.

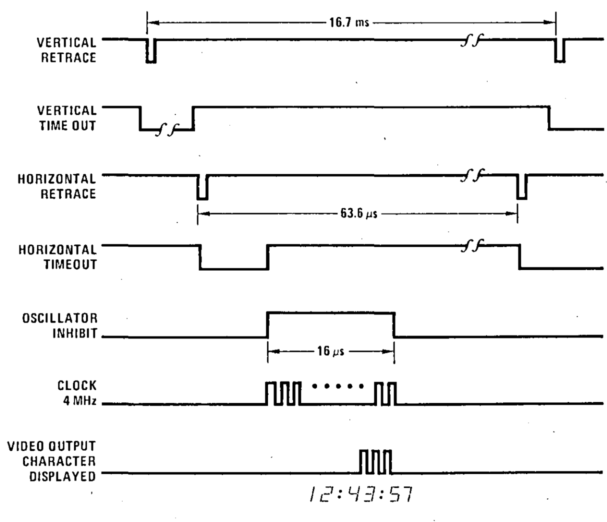


FIGURE 3. Timing Diagram

typical applications

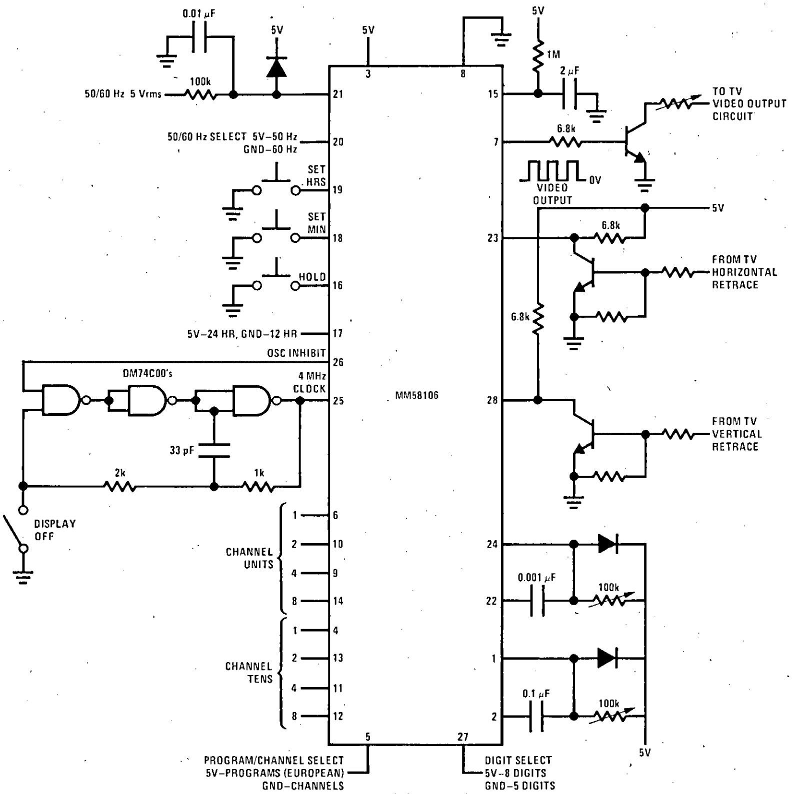


FIGURE 4.

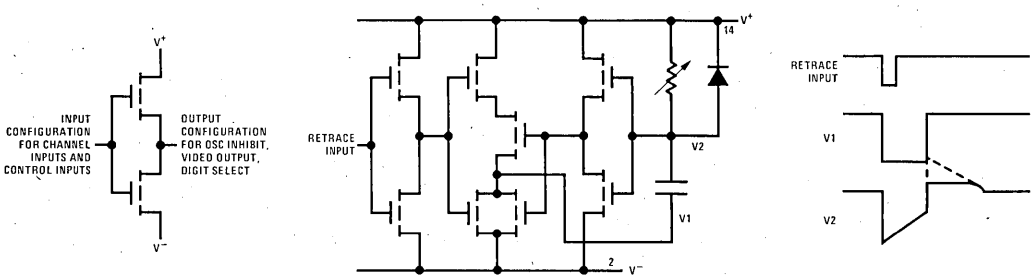
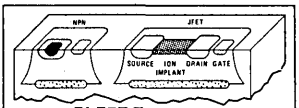


FIGURE 5. Horizontal and Vertical One-Shot Circuit

SECTION 5
ANALOG TO DIGITAL (A/D) CONVERTERS

Analog to Digital (A/D) Converters



BI-FET Technology

LF13300 integrating A/D analog building block

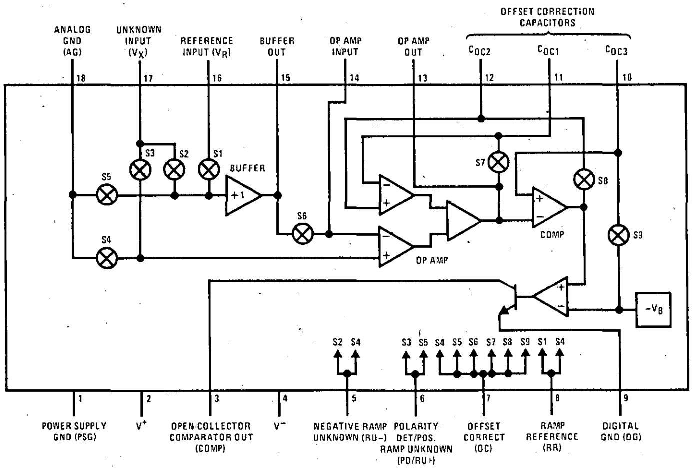
general description

The LF13300 is the analog section of a precision integrating analog to digital (A/D) system. JFET and bipolar transistors (BI-FET) are combined on the same chip to provide a high input impedance unity gain buffer, comparator and integrator, along with 9 JFET analog switches. The LF13300 has sufficient accuracy to construct up to a 4 1/2-digit Digital Panel Meter (DPM) or up to 14-bit (plus sign) Data Acquisition System and is specifically designed for use with either the MM5330 BCD digital building block or the MM5863 12-bit binary building block.

features

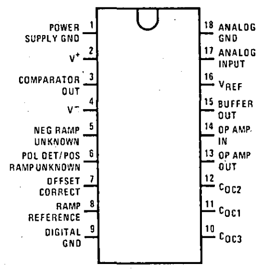
- Rugged JFETs allow blow-out free handling
- High input impedance > 1000 MΩ
- Automatic offset correction
- Analog circuitry can be physically and electrically isolated from high noise digital circuits
- Analog input range of ±11V with ±15V supplies
- Wide power supply voltage range ±5V to ±18V
- TTL and CMOS compatible logic
- Can interface directly with microprocessors
- Versatile: can be used as a 12-bit plus sign binary A/D, 4 1/2-digit, 3 3/4-digit and 3 1/2-digit Digital Panel Meter (DPM)
- Low cost

block and connection diagrams



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Number LF13300N
See Package 20

absolute maximum ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	570 mW
Operating Temperature Range	0°C to +70°C
Junction Temperature	110°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (V_S = ±15V, T_A = 25°C, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Current, I_{IN}	V_X = 0, Currents into Pins 17 and 18, Test Circuits 1 and 2		50	500	pA
Analog Input Voltage Range	V_X adjusted until $\|I_{IN}\| \geq$ 10 nA, Test Circuits 1 and 2	±11	±12		V
Analog Input Resistance	V_X = 0V, Test Circuits 1 and 2		1000		MΩ
Reference Input Currents, I_R	V_R = 10V, Current into Pin 16, Test Circuit 3		100	1000	pA
Reference Input Voltage Range	V_R Adjusted until $\|I_R\| \geq$ 10 nA, Test Circuit 3	0		11	V
Reference Input Resistance	V_R = 10V, Test Circuit 3		500		MΩ
Offset Correction Voltage, $-V_B$	Test Circuit 4		−12		V
Offset Correction Input Current, I_{OC}	Test Circuit 5		200	2000	pA
Op Amp Slew Rate	Test Circuit 6		10		V/μs
Op Amp Bandwidth	Test Circuit 7		3		MHz
Buffer Slew Rate	Test Circuit 9		25		V/μs
Comparator Response Time	200 μV Input Step, 100 μV Overdrive, Test Circuit 11		2.5		μs
Comparator Output Saturation Voltage	V_{CC} = 5V, R_L = 2k, 0°C $\leq T_A \leq$ +70°C, Test Circuit 11		0.2	0.4	V
Logic "1" Input Voltage		2.0		6	V
Logic "0" Input Voltage	All Switching Input Pins 5, 6, 7 and 8, 0 $\leq T_A \leq$ +70°C	−5		0.8	V
Logic Input Current			2	20	μA
Power Supply Voltage Range, $\pm V_S$	$V_R \leq V^+ - 3V$, V_{IN} = 0V, $\pm V_S$ is Variable	±4.75		±18	V
Power Supply Currents, $\pm I_S$			±4	±11	mA

Note 1: For operating at elevated temperatures, the LF13300 in the DIP package must be derated based on the thermal resistance of 100°C/W junction to ambient.

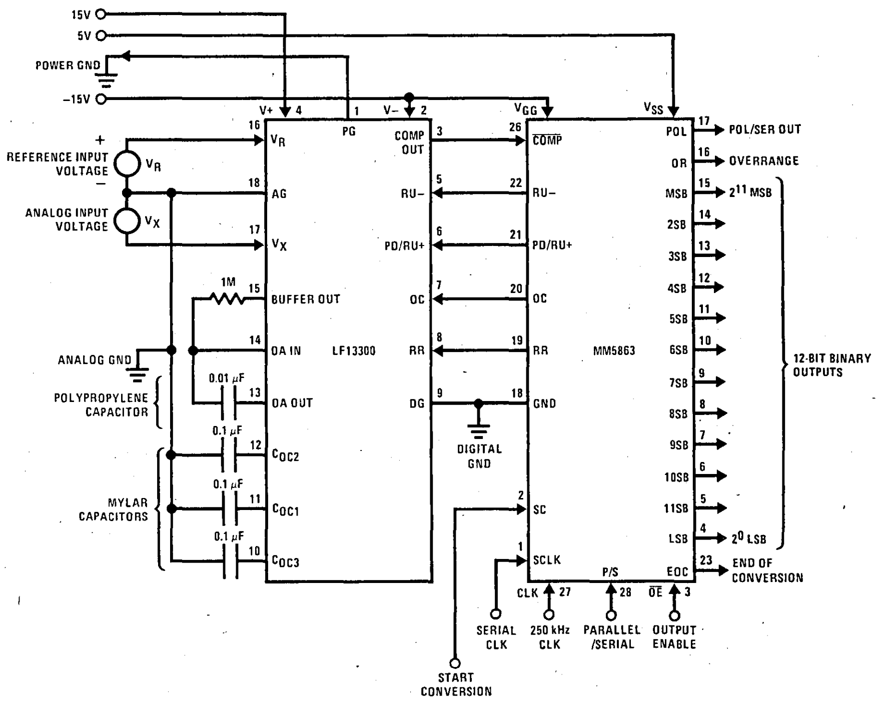
electrical characteristics

12-bit plus sign A/D converter system characteristics. (LF13300 with MM5863). (Circuit configured as in *Figure 1,* V_R = 10.000V, 0°C ≤ T_A ≤ +70°C unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	V_R = 5.000V, −10V ≤ V_X ≤ +10V	14			Bits
Nonlinearity			±1/8	±1/2	LSB
Differential Nonlinearity			±1/8	±1/2	LSB
Ratiometric Gain Error	V_X = ±10.000V, T_A = 25°C		±1/2	±2	LSB
Gain Error Drift	V_X = 10.000V		±1		ppm/°C
Zero Reading Drift	V_X = 0V		±0.5		ppm/°C
Analog Input Voltage Range		±11	±12		V
Analog Input Leakage Current	T_A = 25°C, V_X = 0V		50	500	pA
Analog Input Resistance	T_A = 25°C, V_X = 0V		1000		MΩ
Reference Input Voltage Range	T_A = 25°C, V_R Varied	0		12	V
Reference Input Leakage Current			100	1000	pA
Reference Input Resistance	T_A = 25°C, V_R = 10.000V		500		MΩ
Conversion Time	V_{IN} = 10.000V, F_C = 250 kHz			36	ms
15V Supply Currents	LF13300, V^+ Current		4	11	mA
−15V Supply Currents	LF13300, V^- Current, MM5863 V_{GG} Current		27	44.8	mA
5V Supply Currents	V_{IN} = 0V, MM5863, V_{SS} Current		23	38.5	mA

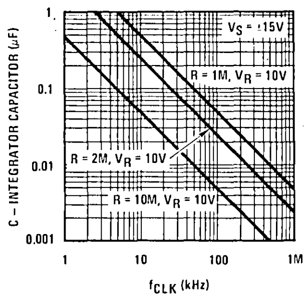
ac test circuits

Test Circuit 12
12-Bit A/D Converter

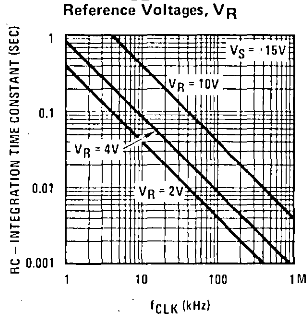


typical performance characteristics

Integrator Capacitance, C vs f_{CLK} for Different Integrator Resistances, R



Integration Time Constant (RC) vs f_{CLK} for Different Reference Voltages, V_R



functional description

The LF13300 goes through the following 5 states during normal cycle: 1) Offset Correction; 2) Polarity Determination; 3) Initialization; 4) Ramp Unknown; 5) Ramp Reference.

Offset Correction Description *(Figure 1)*

The Offset Correction scheme will drive the input of the comparator to its switching threshold when the analog input is zero and the timing components, RC, are bypassed.

The Offset Correction input (OC) is driven high, closing switches S4–S9.

The offset voltages are assigned as follows: V_{OS1} – the input offset voltage of the buffer; V_{OS2} – the input offset voltage of A1; V_{OS3} – the input offset voltage of A2; V_{OS4} – the input offset voltage of the comparator.

S5 grounds the input of the buffer so that its output voltage is simply V_{OS1}. S6 bypasses R to keep the integration time constant, RC, from affecting the circuit operation. S4 makes the total equivalent input voltage to A1 be $-V_{OS1} - V_{OS2}$. S7 puts the op amp in a unity gain configuration with respect to the input of A2. S8 keeps the output voltage of the op amp at $-V_B + V_{OS4} = -V_B'$ (the Offset Correction potential) since the comparator is placed inside the loop. C3 samples the output of the $-V_B$ generator. The voltage at the non-inverting input of A2 is $-V_B + V_{OS1} + V_{OS2} + V_{OS3} + V_{OS4} = V1$. Thus, the sum of the offsets is stored on C1, and the differential voltage across the comparator is zero.

Polarity Determination *(Figure 2)*

The simplified diagram of the LF13300 in the Polarity Determination state is shown in *Figure 3*. S5 and S3 are closed during this period. S5 grounds the buffer input and V_X (the unknown voltage) is applied through S3 to the non-inverting input of A1. The equation that describes the op amp output voltage is given in *Figure 3*. When V_X is applied to A1 at t_1, the output of the op amp slews to V_X and is integrated until t_2, when S3 opens and S4 closes. This causes V_{OUT} to slew down by $-V_X$ leaving $\frac{1}{RC}\int_{t_1}^{t_2} V_X dt - V_B'$ on the output of the op amp. The comparator output goes high if $V_X > 0$ and remains low if $V_X \leq 0$.

Initialization *(Figure 1)*

During initialization, the LF13300 is configured the same way as it is in the Offset Correction state and the op amp output is brought back to the Offset Correction potential $-V_B'$.

Ramp Unknown *(Figures 2 and 3)*

In the Ramp Unknown state, if $V_X \geq 0$, S3 and S5 are closed, as shown in *Figure 2*, and V_X is applied to the + input of the integrator. If $V_X \leq 0$ and the LF13300 is connected as in *Figure 3* with S2 and S4 closed. V_X is now applied through the buffer to the – input of the integrator. In either Ramp Unknown case, the op amp output ramps in the positive direction and V_X is applied to a high impedance JFET input.

functional description (Continued)

Ramp Reference *(Figure 4)*

In this state, the LF13300 is configured with switches S1 and S4 closed. The reference voltage, V_R, a positive voltage, is applied to the buffer input and the op amp output ramps down until $V_{OUT} = -V_B'$ where the comparator will trip.

If V_X and V_R are assumed to be constant over their respective integration periods, the integrals of *Figure 7* are reduced to,

$$\frac{V_X\,(t_4 - t_3)}{RC} = \frac{V_R\,(t_5 - t_4)}{RC}$$

or

$$\frac{V_X}{V_R} = \frac{t_5 - t_4}{t_4 - t_3}.$$

Since $t_4 - t_3$ = 4096 clock periods and $t_5 - t_4$ can be measured in clock periods, $V_X/V_R = X/2^{12}$, where X is a digital binary output representing an analog input V_X with respect to V_R.

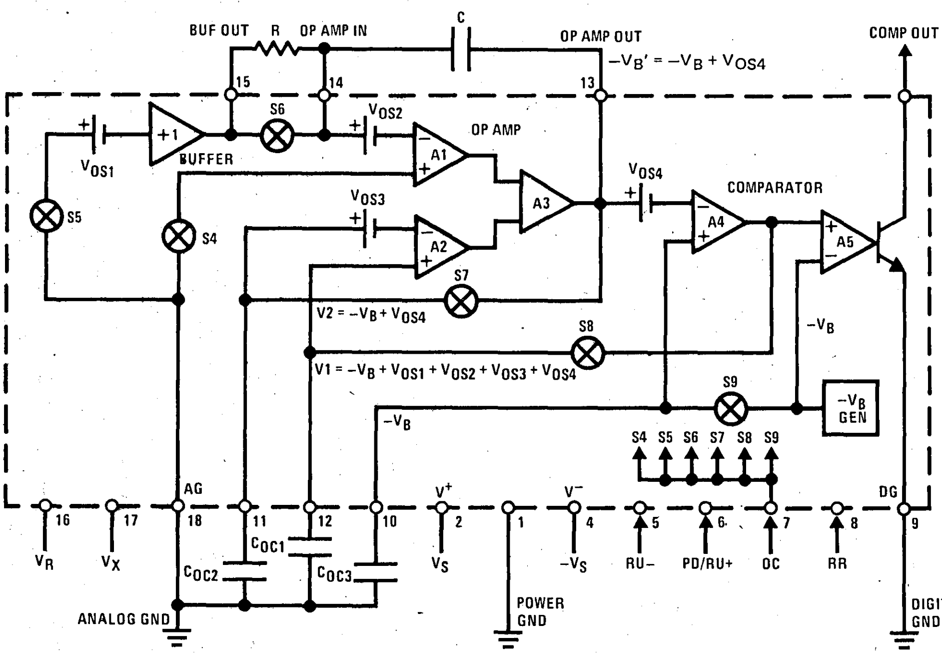


FIGURE 1. Offset Correction Circuit

functional description (Continued)

$$V_{OUT} = \begin{cases} -V_B' + V_X + \dfrac{1}{RC}\displaystyle\int_{t_3}^{t_4} V_X\,dt\text{: Ramp Unknown for } V_{IN} \geq 0 \\ -V_B' + V_X + \dfrac{1}{RC}\displaystyle\int_{t_1}^{t_2} V_X\,dt\text{: Polarity Determination} \end{cases}$$

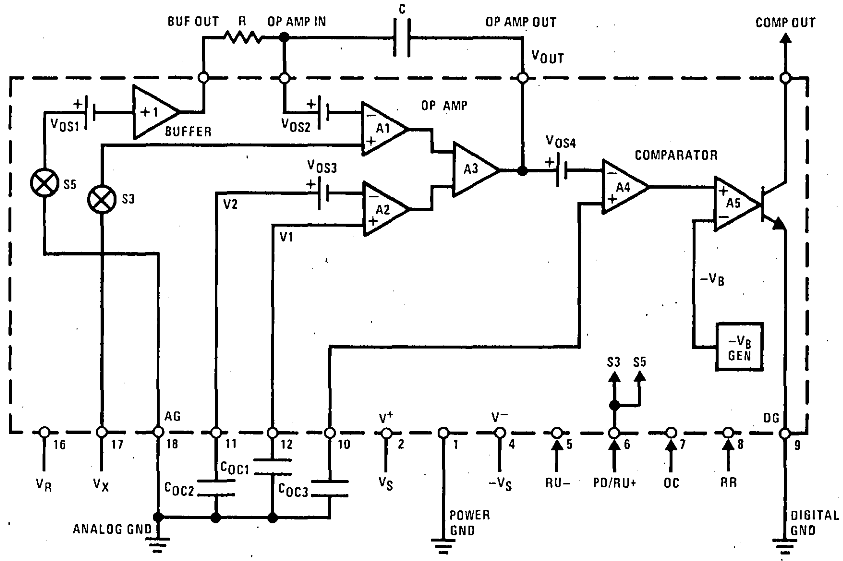


FIGURE 2. Polarity Determination Circuit or Ramp Unknown Circuit for $V_X \geq 0$

$$V_{OUT} = -V_B' + \frac{1}{RC}\int_{t_3}^{t_4} V_X\,dt$$

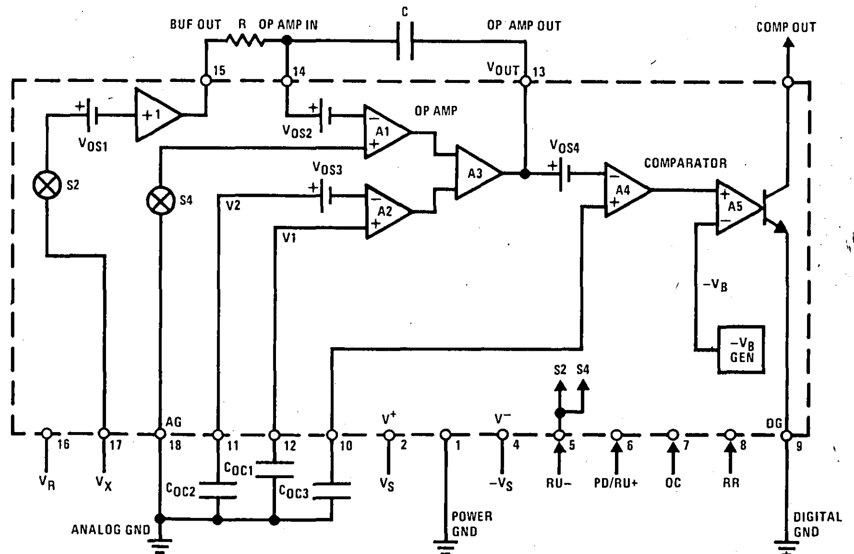
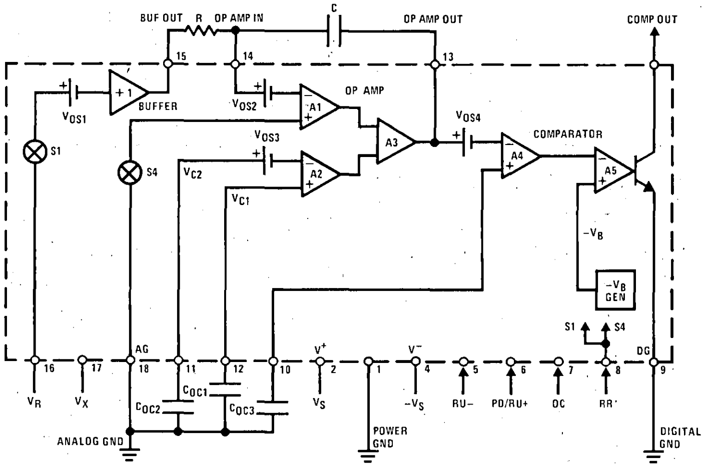


FIGURE 3. Ramp Unknown for $V_X < 0$

functional description (Continued)

$$V_{OUT}^{*} = -V_B' + \frac{1}{RC}\left(\int_{t_3}^{t_4} V_X\,dt - \int_{t_4}^{t_5} V_R\,dt\right)$$



*More accurately

$$V_O = -V_B' + \frac{1}{RC}\left(\int_{t_4}^{t_S+\Delta} V_R\,dt + \int_{t_3}^{t_4} V_X\,dt\right) + \delta$$

Where δ is the incremental voltage overdrive needed to fully switch the comparator and Δ is the sum of the additional time required to develop δ and the comparator propagation delay.

FIGURE 4. Ramp Reference Circuit

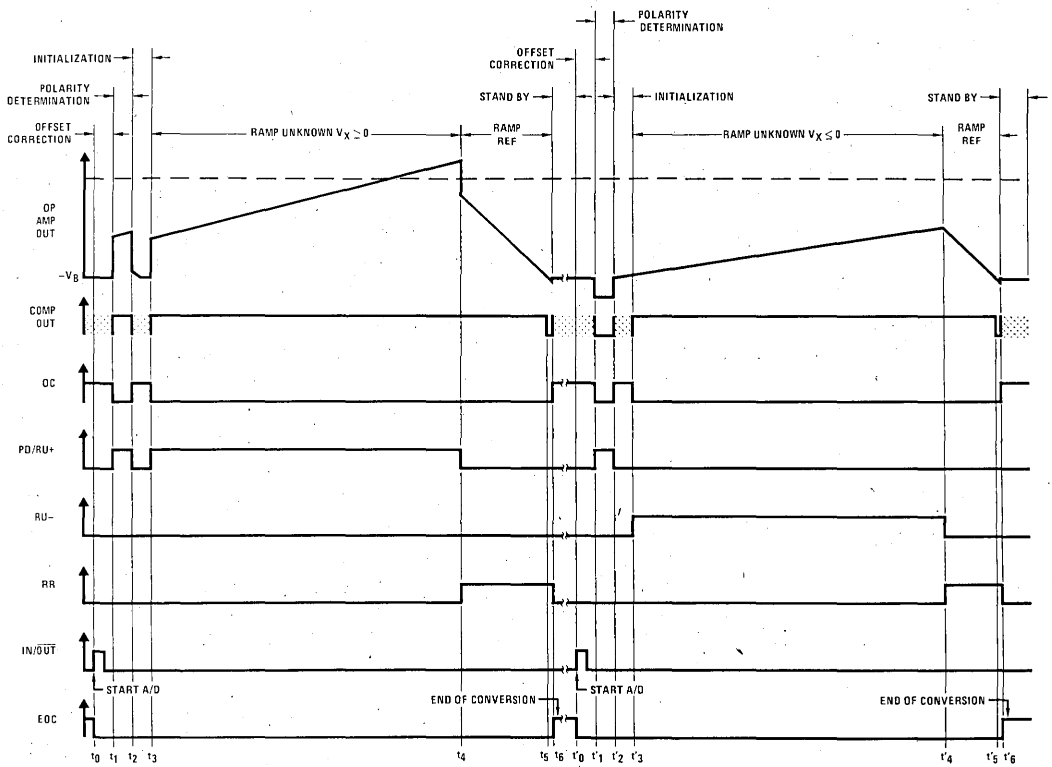


FIGURE 5. Timing Diagram

application hints

Increasing the Input Impedance of the LF13300, MM5863 12-Bit A/D Converter

The input impedance of the LF13300, MM5863 A/D converter can be increased 1 to 2 orders of magnitude over the typical 1000 MΩ cited in the specifications by insuring that the signals that switch the LF13300 do not overlap. A circuit that eliminates switching overlap by introducing a Delay (t_d) ≈ 3.3k x 100 pF ≈ 300 ns to the rising edge of the signals from the MM5863A is shown in *Figure 6. Figure 8* shows the operation of this circuit. The total delay time t_r' of the output will be equal to the inherent gate rise time, t_r, plus the RC delay, t_d. The fall time, t_f will be the basic gate delay.

Nulling the Residual Offset in the LF13300

The residual offset of the LF13300 is < 200 μV which is negligible for most applications. This can be reduced to < 40 μV by lowering the clock frequency from 250 kHz to about 75 kHz. If a residual offset of < 40 μV is required, we may trim out the remainder as shown in *Figure 9.* This circuit applies a negative step to the Offset Correction capacitor, C_{OC2}, by means of a variable capacitor which is adjusted until charge injection imbalance of the Offset Correction switches are cancelled.

Eliminating Errors Due to Power Supply Noise

For many applications, power supply noise (f ≥ 10 Hz) causes errors which reduces the accuracy of the system. In most applications, noise can be adequately eliminated by putting a series resistor (100Ω) in the power supply line with a 10 μF tantalum capacitor connected at the power supply pins *(Figure 8)*. The 10 μF capacitor is, in addition to the normal 0.1 μF ceramic disc capacitors, used as supply bypass capacitors.

Errors caused by noise on the negative supply, $-V_S$, can be further reduced by replacing, C_{OC3} with a 10 μF low leakage tantalum capacitor. Since $-V_B$ is 3V above $-V_S$, any noise appearing at $-V_S$ appears at $-V_B$; the 10 μF capacitor eliminates the noise at $-V_B$.

Miscellaneous

Since none of the output pins of the LF13300 employ short-circuit protection, extreme care should be taken when breadboarding or troubleshooting with the power "ON".

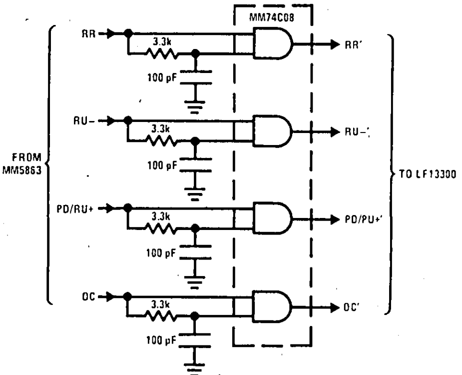


FIGURE 6. Overlap Elimination Circuit

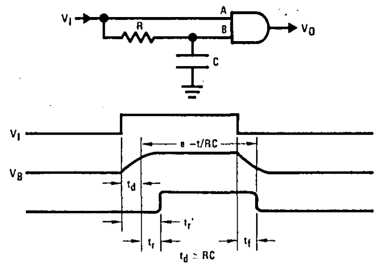


FIGURE 7. Rise Time Delay Circuit

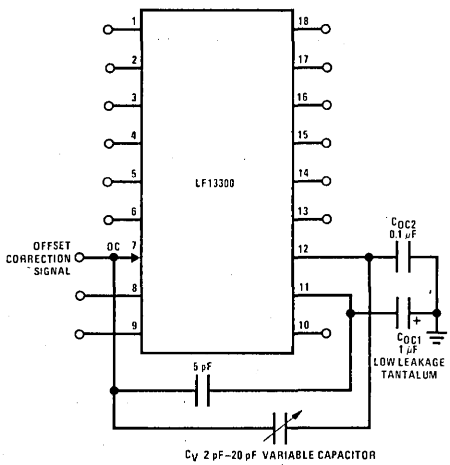


FIGURE 8

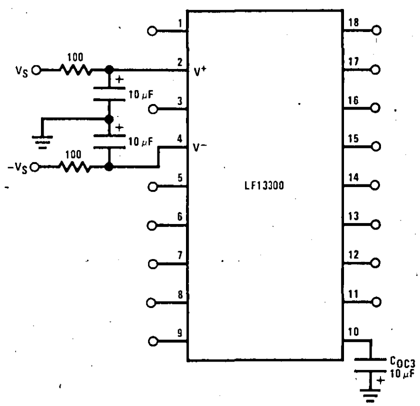


FIGURE 9. Residual Offset Nulling Circuit

typical applications

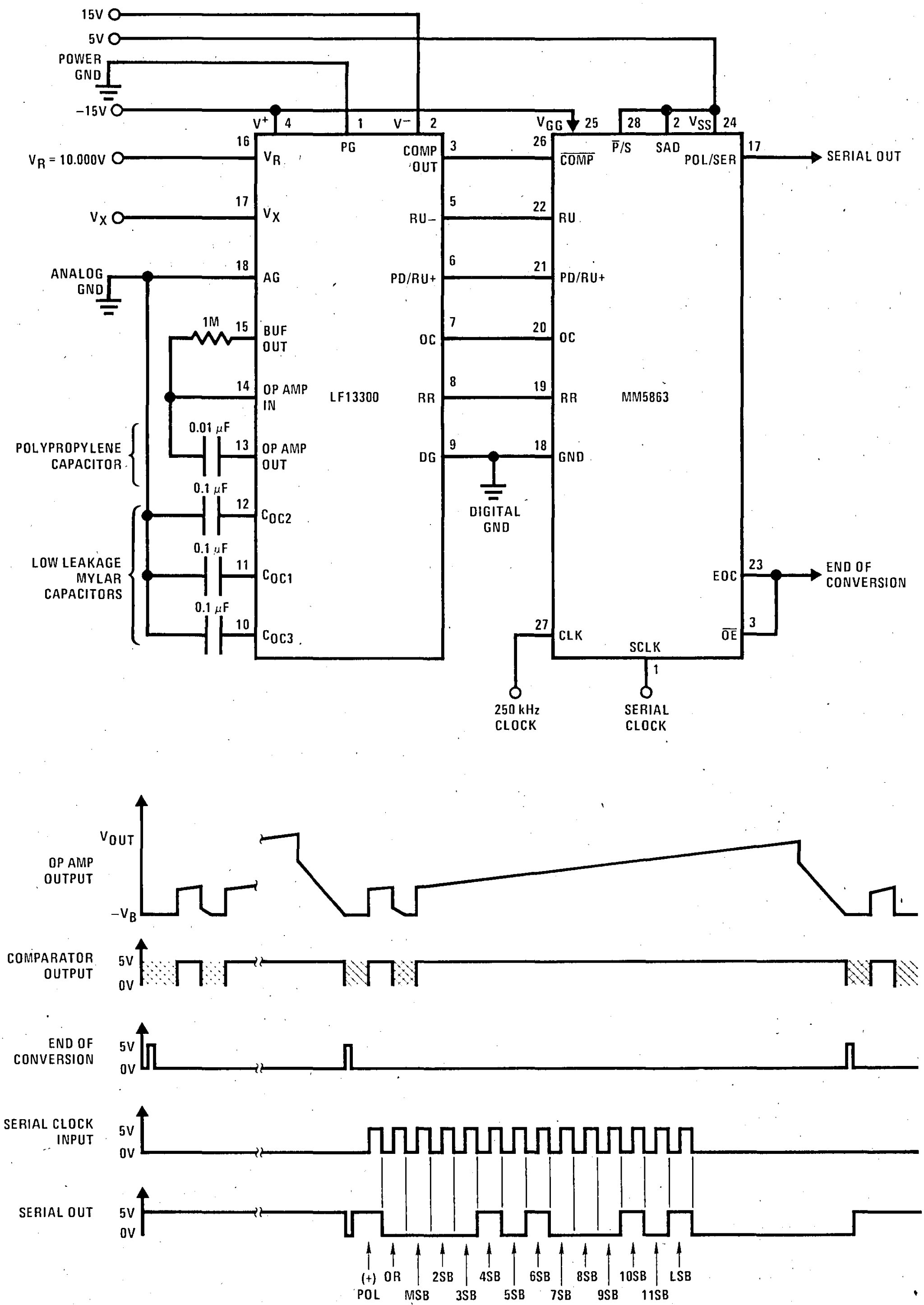


FIGURE 10. 12-Bit Plus Sign Serial Output A/D Using the LF13300 and the MM5863

typical applications (Continued)

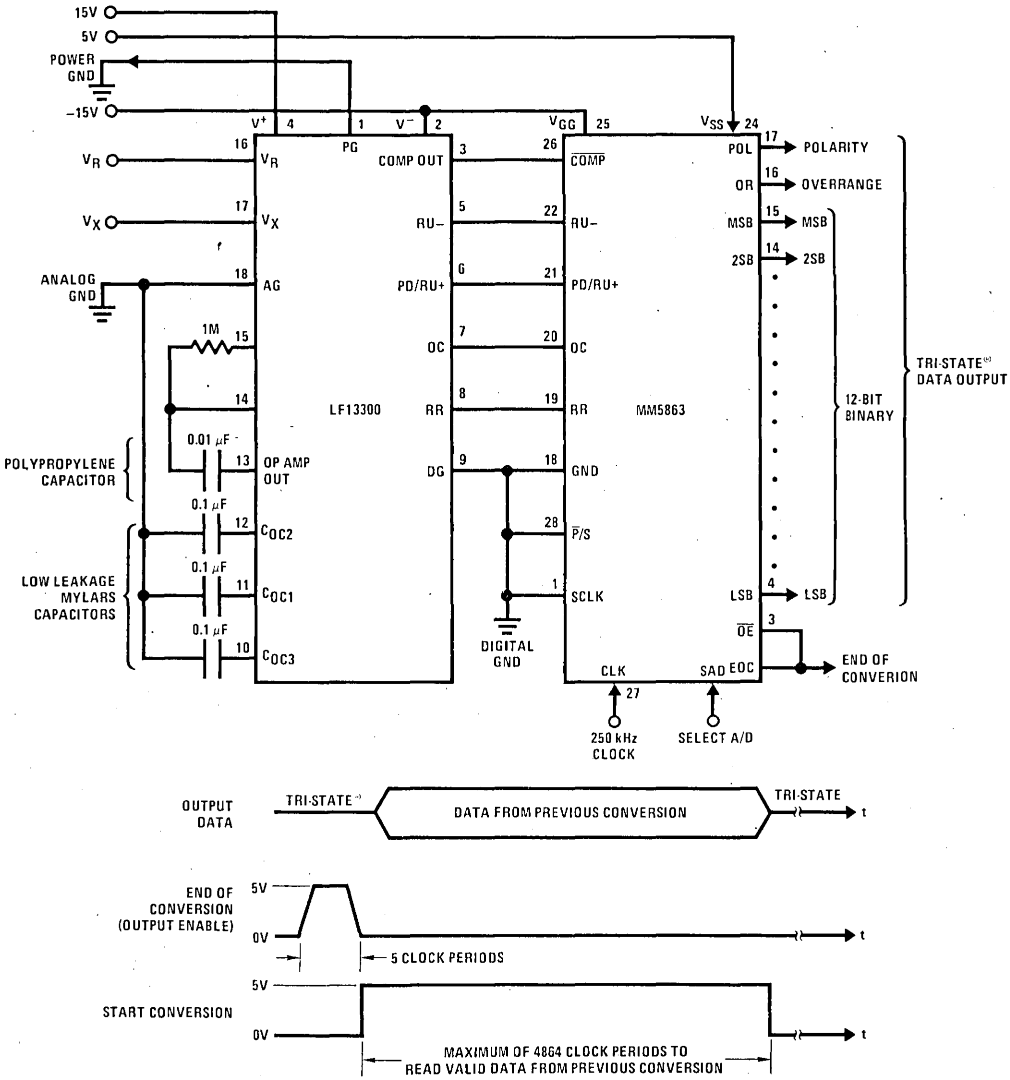


FIGURE 11. 12-Bit Plus Sign A/D in Intermittent Conversion Mode

4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

Figure 12 shows a low speed, high accuracy, data acquisition unit where the analog input signal is acquired differentially and preconditioned through an LF352 monolithic instrumentation amplifier. To eliminate amplifier offset errors, autozeroing circuitry is added around the LF352 and is timed through the MM5863 and flip-flop C. Flip-flops A and B form a 2-bit up counter for channel select.

The instrumentation amplifier is zeroed at power-up and after each conversion as shown in the timing diagram; during this cycle the multiplexer is disabled. When the system does polarity detection and then A/D conversion, the LF352 is active and the multiplexer is enabled. The zeroing cycle for the LF13300 and the LF352 lasts for 256 clock periods, so the maximum clock frequency will depend upon the required accuracy and the minimum zeroing time of the instrumentation amplifier. Notice here that the system accuracy will be less than 12 bits since it will be affected by the gain linearity of the instrumentation amplifier.

For more details concerning data acquisition, see AN-156 and LF11508, LF11509 data sheet. For details on the instrumentation amplifier, see LF352 data sheet.

typical applications (Continued)

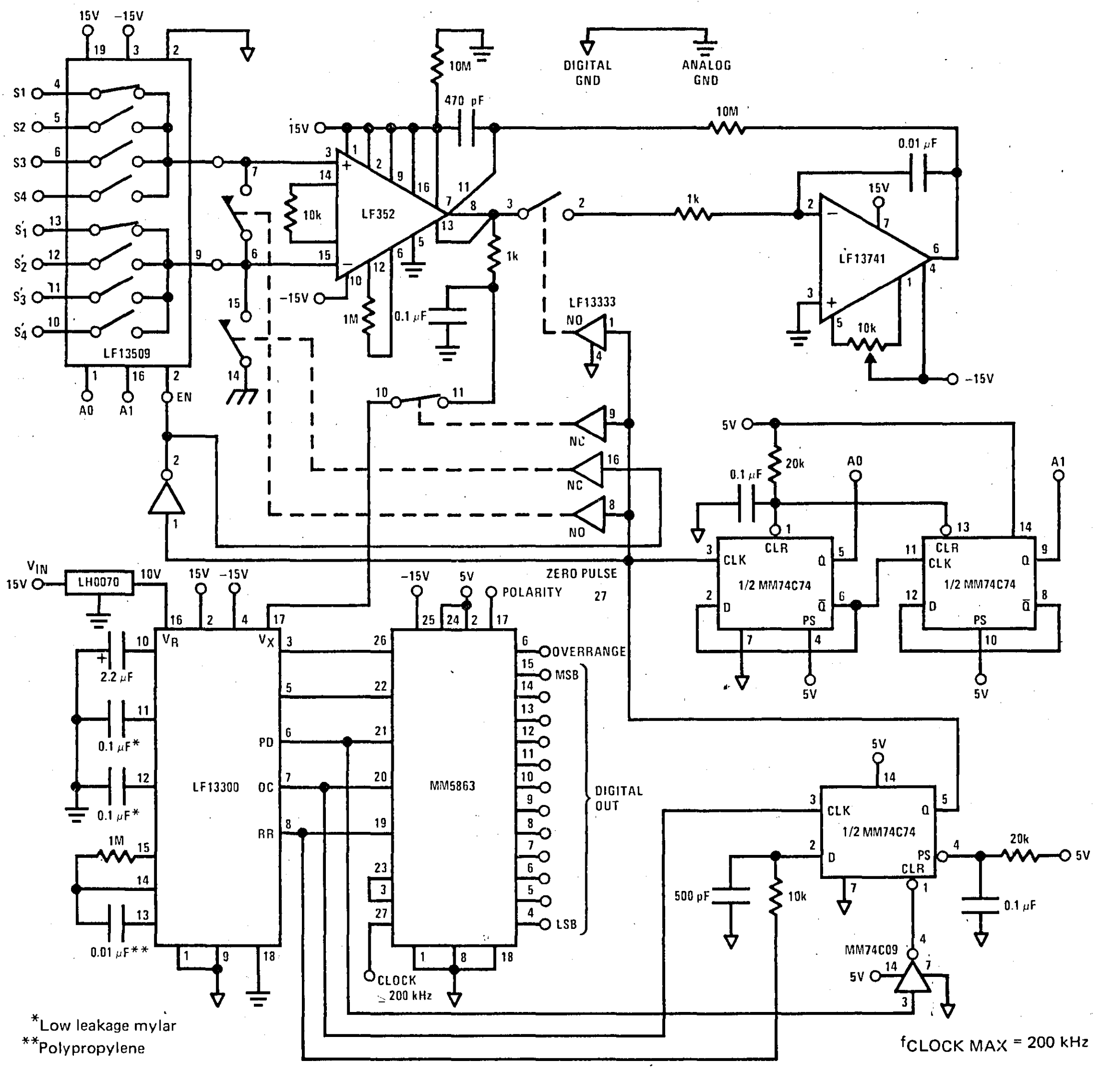


FIGURE 12. 4-Channel Differential Multiplexer with Autozeroed Instrumentation Amplifier and 12-Bit A/D Converter

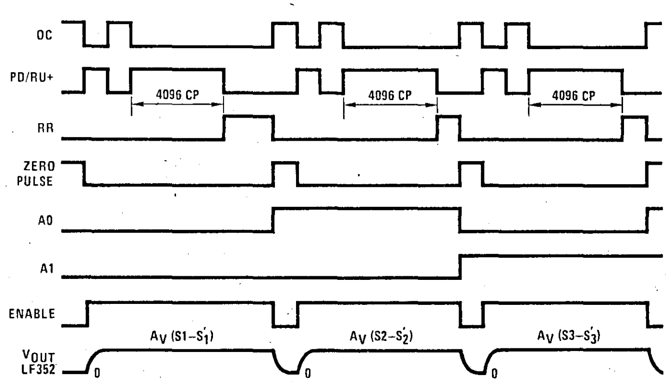
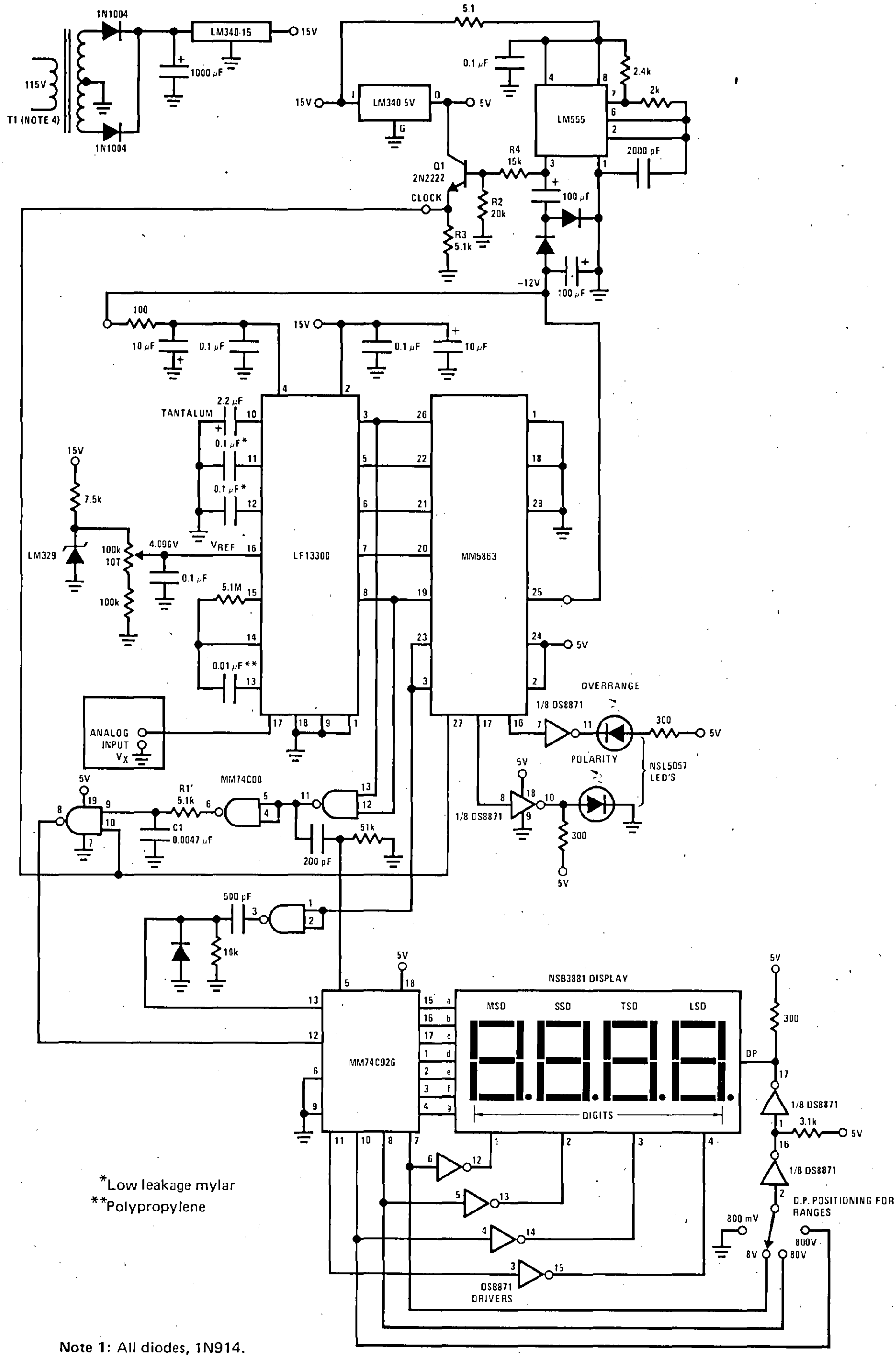


FIGURE 13. Timing Diagram for *Figure 12*

typical applications (Continued)



*Low leakage mylar
**Polypropylene

Note 1: All diodes, 1N914.
Note 2: All resistors 1/4W, 5% tolerance.
Note 3: Circuit drawn for 8V full scale operation input scaling not shown.

FIGURE 14. 3 3/4 and 3 1/2-Digit DPM Schematic Diagram

typical applications (Continued)

3 3/4-Digit (±8191 Counts)/3 1/2-Digit (±1999 Counts) DPM

In this circuit of *Figure 14*, the LF13300 and MM5863 interact as previously described. The CMOS counter (MM74C926, MM74C928) is connected to count clock pulses during the ramp reference cycle of the LF13300. The counts are latched into the display when the comparator output trips, (goes low), as shown in the timing diagram *Figure 15.*

The RC network consisting of R1 and C1 is a low pass filter that prohibits the fast transients that occur on the comparator output during Offset Correction from loading any erroneous counts into the counter.

The DPM is able to operate from a single 15V power supply with the aid of a dc-dc converter. The LM555 generates the negative voltages required in the circuit and also doubles as the clock. The combination of Q1, R2, R3 and R4 forms a level shift to convert the output swing of the LM555 to a 0V–5V swing that is compatible with the logic. The LM340–5 drops the incoming 15V to 5V for use by the logic circuits and the LED display.

This circuit can be a 3 3/4-digit DPM if the MM74C926 is used or a 3 1/2-digit DPM if the MM74C928 is used. These counters are pin compatible and physically interchangeable.

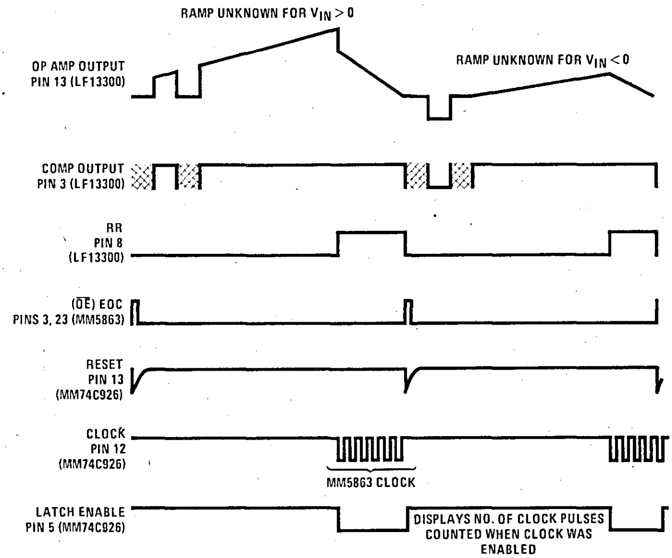


FIGURE 15. Timing Diagram for 3 3/4-Digit DVM

electrical characteristics

3 3/4-digits plus sign (±8191 counts) DPM system characteristics.
(Circuit as in *Figure 18*, V_S = ±15V, V_R = 4.096V, T_A = 25°C, unless otherwise noted).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution	$-8.2V \leq V_X \leq +8.2V$	16,382			Counts
Nonlinearity	V_{IN} = 4.000V		±1/8	±1/2	Counts
Ratiometric Gain Error	V_{IN} = 4.000V		±1/2	±2	Counts
Gain Error Drift	V_{IN} = 4.000V, $0°C \leq T_A \leq +70°C$		±1		ppm/°C
Zero Reading Drift	V_{IN} = 0V		±1		ppm/°C
Analog Input Voltage Range		±11	±12		V
Reference Input Voltage Range	Reference Varied	0		+12	V
Analog Input Leakage Current	V_{IN} = 0V		50	500	pA
Reference Input Leakage Current			100	1000	pA
Analog Input Resistance	V_{IN} = 0V		1000		MΩ
Conversion Time	V_{IN} = 4.000V, f_C = 125 kHz			74	ms

typical applications (Continued)

Component Side Foil

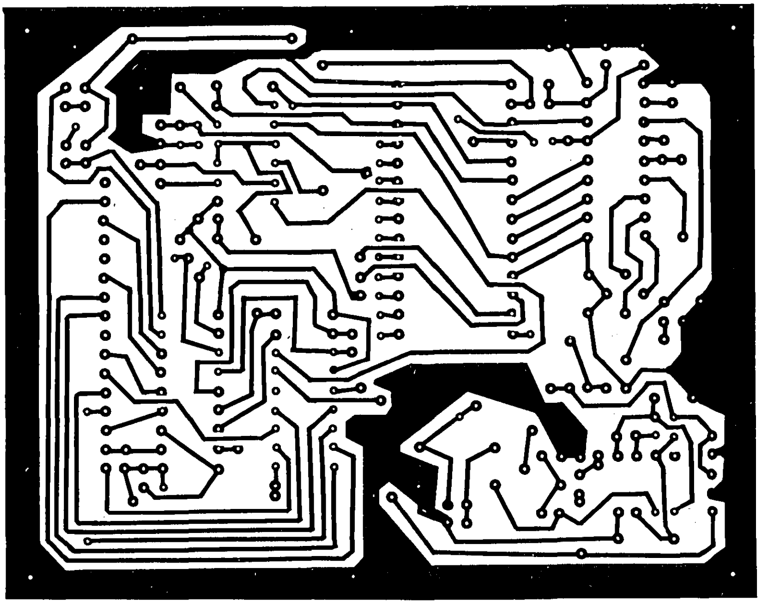


FIGURE 16. PC Board for 3 3/4 and 3 1/2-Digit DPM (Shown 1/2 Size)

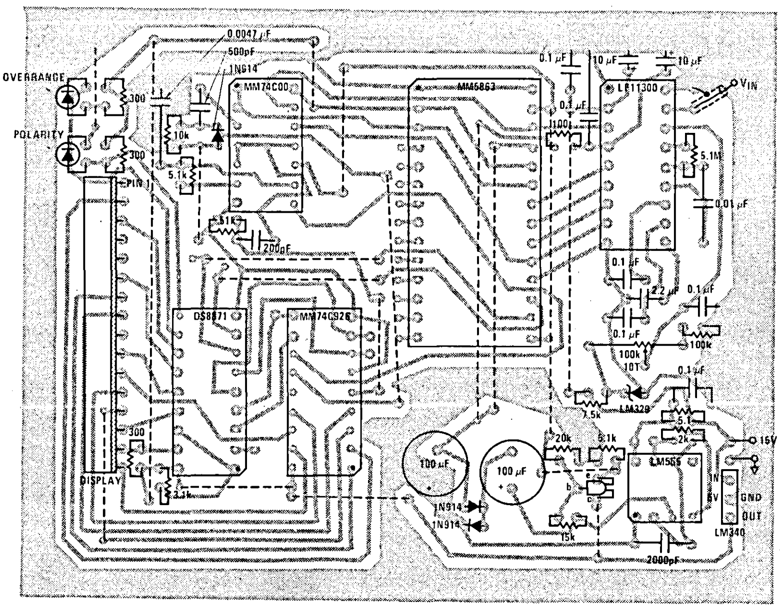


FIGURE 17. Stuffing Diagram for 3 3/4 and 3 1/2-Digit DPM (Shown 1/2 Size)

typical applications (Continued)

4 1/2-Digit (±19,999 Counts) DPM

The following circuit illustrates how a 4 1/2-digit DPM can be realized using the LF13300 and the MM5330. The MM5330 is the display and control for this integrating system.

It contains the counters and latches together with a multiplexing system to provide 4 digits of display with one decoder/driver. It also provides a sign bit that is valid during overrange and a ten thousand count digit for a full display of ±19,999 counts. By eliminating the right-most digits it may also be used as a 2 1/2 or 3 1/2-digit DPM.

The LF13300 features automatic zeroing of all offset voltages in its integrator, comparator and buffer amplifiers and, unlike conventional dual slope techniques, provides an input impedance > 1000 MΩ.

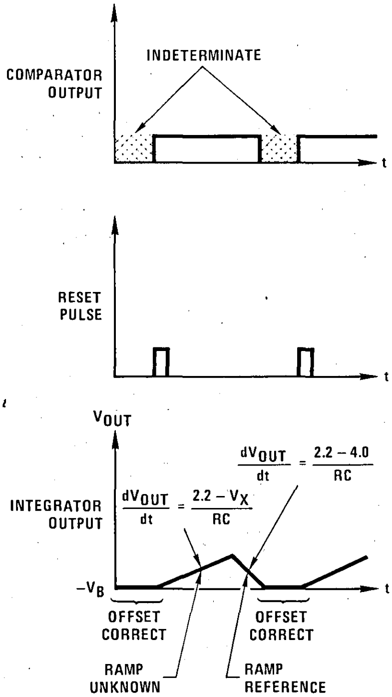
The waveform at the integrator output is shown in *Figure 18*. At the rising edge of the reset pulse the unknown input voltage is applied to the integrator for a reference period of 18,000 clock periods. After this reference period, the 4.0000V reference is applied to the integrator and the counter is started. The reference voltage is integrated until the comparator switches.

At this point, the accumulated counts are transferred from the counters to the latches and zeroing begins until the next reset pulse.

It may be obvious, however, that while we have eliminated several of the basic dual slope circuits disadvantages, we have created another—the number of counts are no longer proportional to V_{IN} but rather to $(V_{MAX}-V_{IN})$. In fact, when we short V_{IN} to ground we are actually measuring our own 2.2000 V_{MAX}.

What is done in the MM5330 is to code convert the number of counts as shown in the count diagram. This chart shows a code conversion starting at the time of a reset. The first 18,000 counts are the reference period after which time the integrator changes slope. If a comparator crossing is detected within the next 2000 counts, a plus overrange condition will occur at the display. This condition results in a lit "+" sign, a lit "1" and 4 blanked right-most digits. A transfer at 20,000, however, will create a reading of +1.9999, at 20,001 a reading of 19.998 and so on, until at 39,999 a reading of +0000 would be displayed. A transfer occuring at 40,000 would cause a −0000 display and so on until 60,000 counts were entered, at which time a −1 with 4 blanked digits would be displayed, indicating a minus overrange condition.

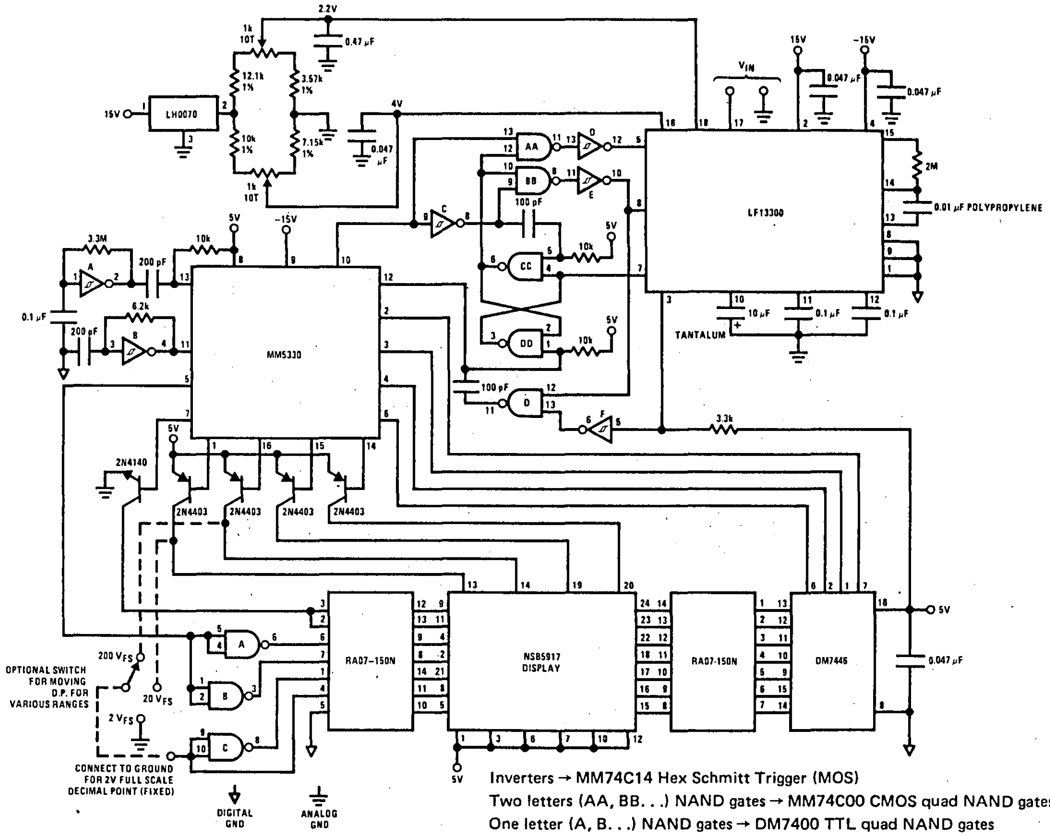
The display interface used is a TTL, 7-segment decoder/driver and 4 2N4403 transistors. The ±1 digit is driven directly by TTL. The clock-synchronous reset and transfer functions prevent any cyclic digit variations and present a blink-free, flicker-free display.



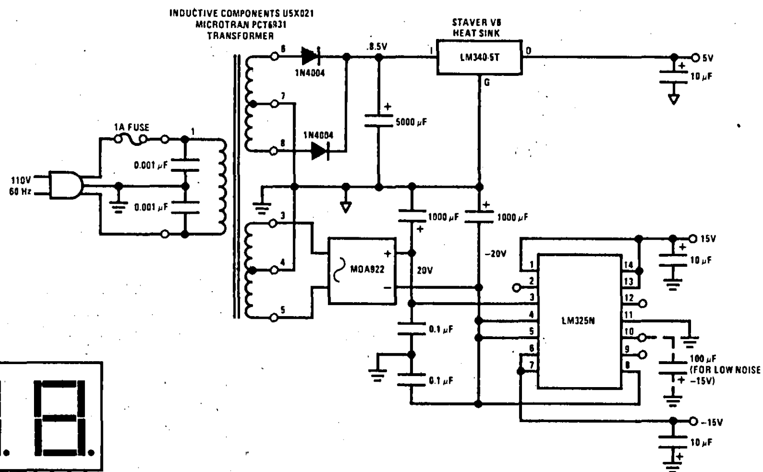
Note. Here the LF13300 always operates as an autozeroed, high input impedance inverting integrator; bipolar input voltages are handled by offsetting the analog ground by 2.2V.

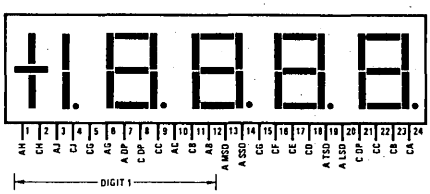
FIGURE 18. Timing Diagram for 4 1/2-Digit DPM

typical applications (Continued)



Inverters → MM74C14 Hex Schmitt Trigger (MOS)
Two letters (AA, BB. . .) NAND gates → MM74C00 CMOS quad NAND gates
One letter (A, B. . .) NAND gates → DM7400 TTL quad NAND gates
All resistors 1/4W, 5% unless otherwise noted.
All capacitor values in μF unless otherwise noted.





NSB5917 Display (Front View)

First letter code:
A → anode
C → cathode

MSD → digit 2
SSD → digit 3
TSD → digit 4
LSD → digit 5

(Second letter code)

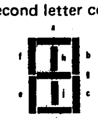
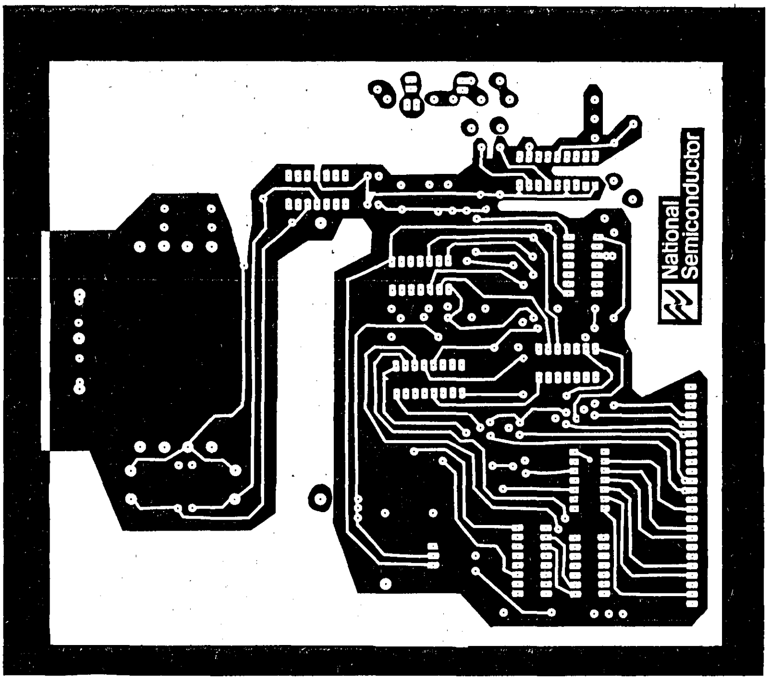


FIGURE 19. Schematic Diagram for 4 1/2-Digit DVM

typical applications (Continued)

Component Side Foil



Bottom Side Foil

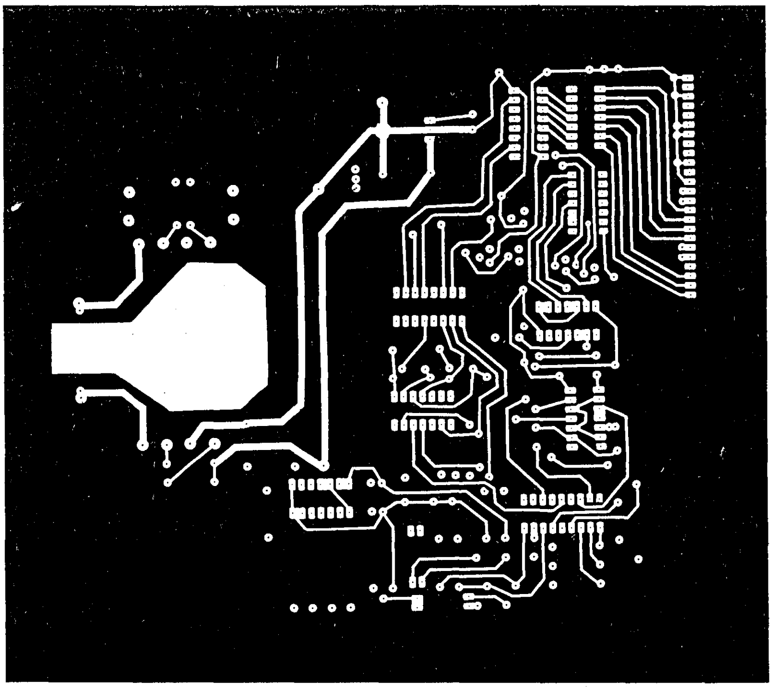


FIGURE 20. PC Board for 4 1/2-Digit DVM (Shown 1/2 Size)

typical applications (Continued)

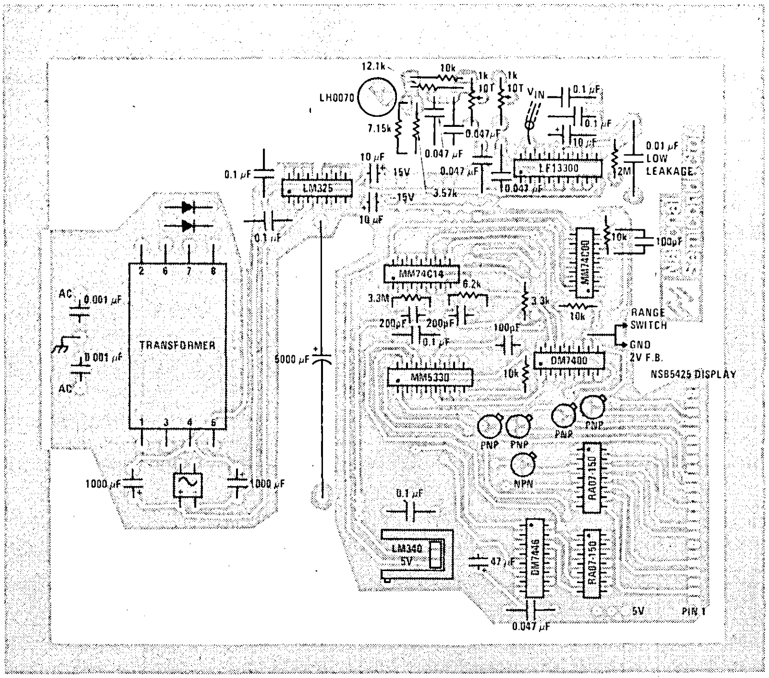
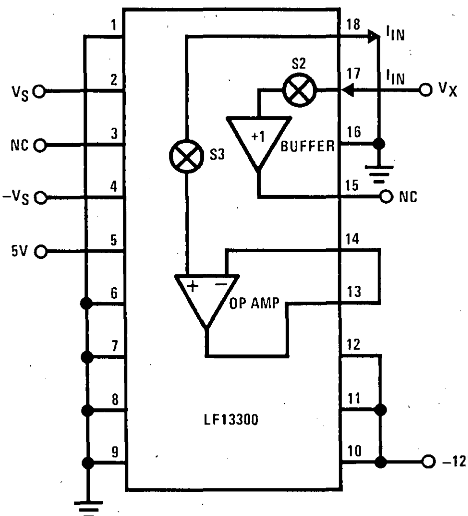


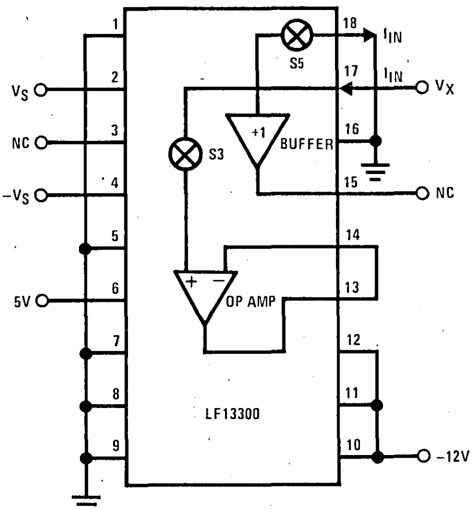
FIGURE 21. Stuffing Diagram for 4 1/2-Digit DVM (Shown 1/2 Size)

ac test circuits (Continued)

Test Circuit 1
Analog Input Characteristics Test with RU − High

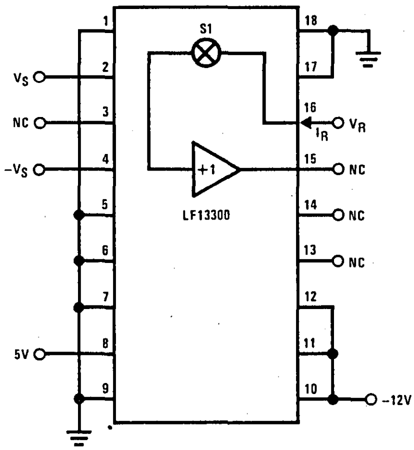


Test Circuit 2
Analog Input Characteristics Test with PD/RU+ High

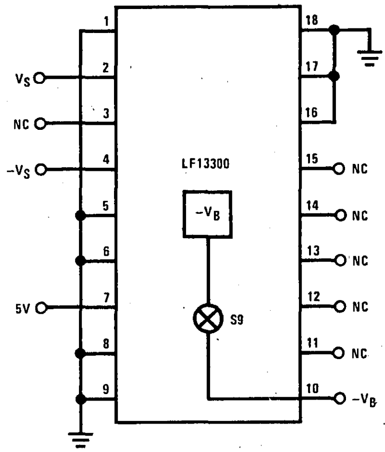


ac test circuits (Continued)

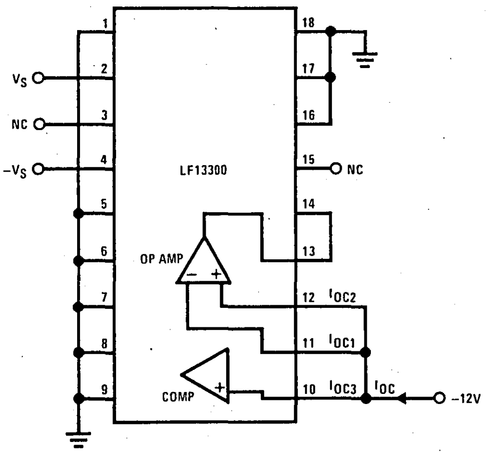
Test Circuit 3
Reference Input Characteristic Test with RR High



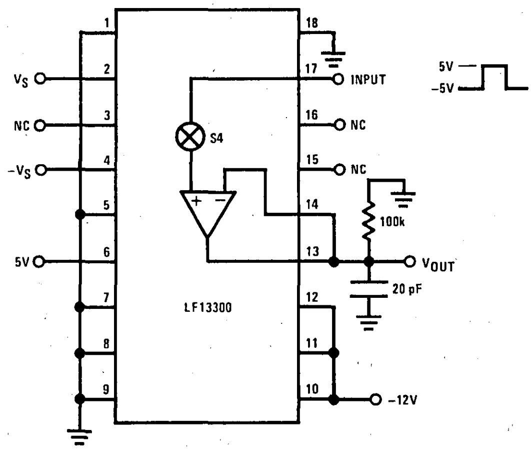
Test Circuit 4
−VB Voltage Measurement Test



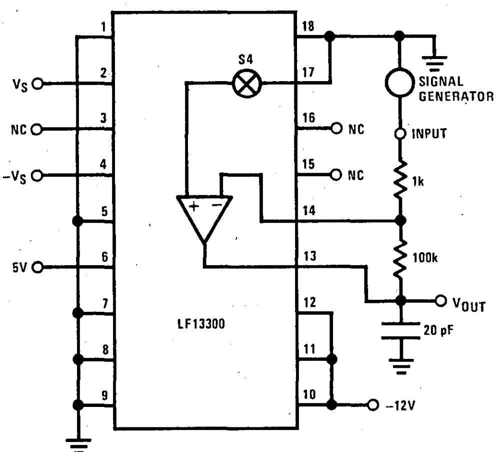
Test Circuit 5
Offset Correction Input Current, I_{OL} Test



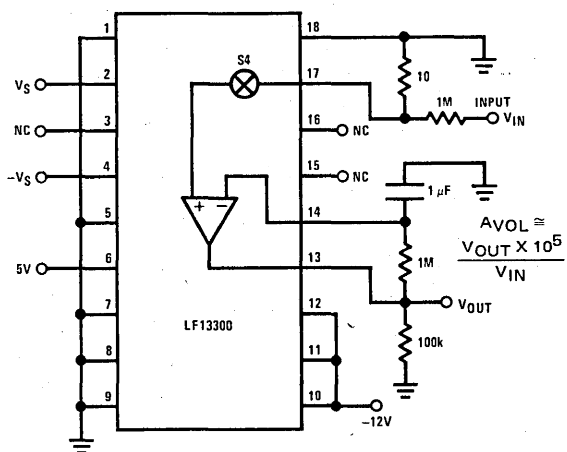
Test Circuit 6
Op Amp Slew Rate Test



Test Circuit 7
Frequency Response Test

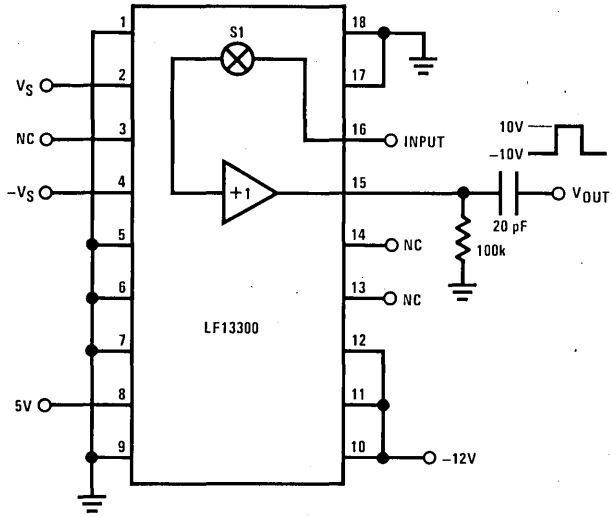


Test Circuit 8
Open Loop Gain Test

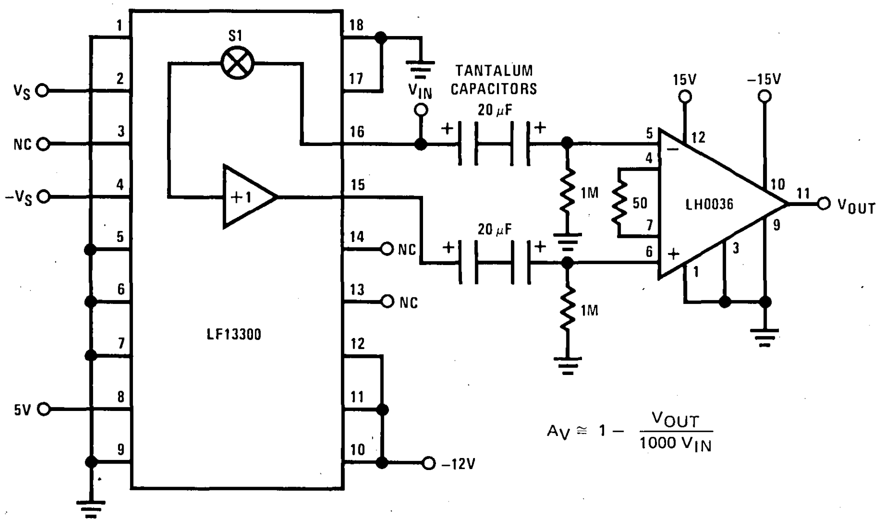


ac test circuits (Continued)

Test Circuit 9
Buffer Slew Rate Test



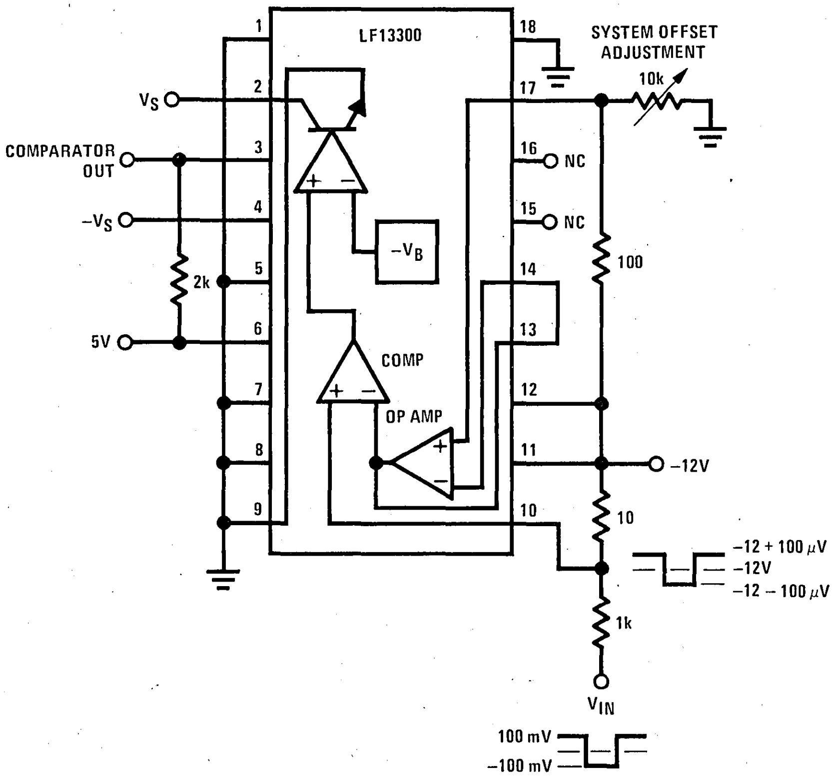
Test Circuit 10
Buffer Voltage Gain Test



$$A_V \cong 1 - \frac{V_{OUT}}{1000\ V_{IN}}$$

ac test circuits (Continued)

Test Circuit 11
Comparator Response Time Test



Analog to Digital (A/D) Converters

For additional application information, see AN-155 at the end of this section.

MM5330 4 1/2-digit panel meter logic block

general description

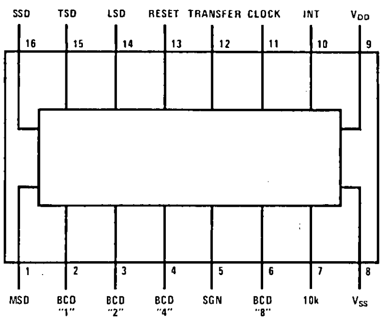
The MM5330 is a monolithic integrated circuit which provides the logic circuitry to implement a 4-1/2 digit panel meter. The MM5330 utilizes P-channel low threshold enhancement mode devices and ion-implanted depletion mode devices. All inputs and outputs are TTL compatible with BCD output for direct interface with various display drivers.

features

- dc to 400 kHz operation
- TTL compatible inputs and outputs
- BCD output code
- Overrange blanking
- Valid sign bit during overrange
- Standard supply voltages; +5, −15V

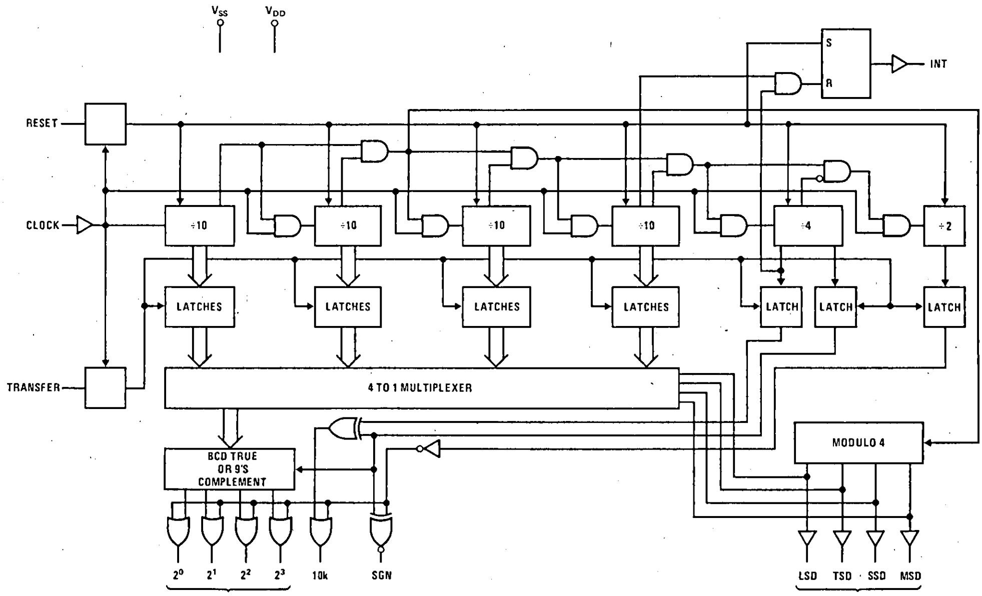
connection and block diagrams

Dual-In-Line Package



TOP VIEW

Order Number MM5330N
See Package 19



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 25V
Operating Temperature	0°C to +75°C
Storage Temperature	−40°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, V_{SS} = 4.75V to 5.25V, V_{DD} = −16.5V to −13.5V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5	5.25	V
Power Supply Voltage (V_{DD})		−16.5	−15	−13.5	V
Power Supply Current (I_{SS})	No Load			30	mA
Input Frequency		dc		400	kHz
Reset or Transfer Pulse Width		200			ns
Input Voltage Levels	V_{SS} = 5V, V_{DD} = −15V				
Logic "1"	Inputs Driven by TTL or Square Waves	3		5	V
Logic "0"	Inputs Driven by TTL or Square Waves	−15		0.8	V
Clock Input Voltage Levels					
Logic "1"	Driven by Sinewave	V_{SS}−0.5		V_{SS}+0.3	V
Logic "0"	Driven by Sinewave	V_{SS}−25		V_{SS}−4.5	V
Output Current Levels	V_{SS} = 5V, V_{DD} = −15V				
Digit Output State					
Logic "1"	V_O Forced To 4.75V	100			μA
Logic "0"	V_O Forced To 4.5V	−5		−20	mA
All Other Outputs					
Logic "1"	V_O Forced To 3V	100			μA
Logic "0"	V_O Forced To 0.4V	−2			mA
Delay From Digit Output to BCD Output		0.1		5	μs

FUNCTIONAL DESCRIPTION

Counters: The MM5330 has four ÷10 counters, one ÷4 counter, and one ÷2 for a count of 80,000 clock pulses. A ripple carry is provided and all counter flip-flops are synchronous with the negative transition of the input clock. The last flip-flop in the divider chain (÷2 in the block diagram) triggers with the "0" to "1" transition of the previous flip-flop. The count sequence is shown in the first column of the count diagram.

Reset: All counter stages are reset to "0" and the INT flip-flop (driving the INT output) is set to "1" on the first negative clock transition after a "0" is applied to the Reset input. The internal reset is removed on the first negative clock transition after the internal reset has occured and a "1" has been applied to the Reset input. This timing provides an on-chip reset at least one clock cycle wide and a one cycle delay to remove reset before counting begins.

Transfer: Data in the counters is transferred to the latches when the Transfer input is at "0." If the Transfer input is held low the state of the counters is continuously displayed (see count diagram). Data will cease to transfer to the latches on the first positive clock transition after the first negative clock transition after a "1" is applied to the Transfer input. This provides a transfer pulse at least one half clock cycle wide and a half clock cycle delay to remove the transfer signal before the counters change state.

INT: The integrate output is used to set the charge time on a dual slope integrator. INT is "1" from reset to the 18,000th clock pulse, then "0" until the next reset. The dual slope integrator is the voltage monitoring part of the external circuitry needed for a DPM. It charges a capacitor at a rate proportional to the measured voltage while INT is "1," then discharges at a rate proportional to a fixed reference as shown in the dual slope diagram. When the output of the integrator reaches 0V a pulse is generated and fed into the Transfer input of the chip. As the dual slope diagram indicates, the number in the latches is proportional to the measured voltage.

Multiplexing: The modulo 4 multiplex counter is triggered by the carry from the second decade counter, making the multiplex rate one hundredth the counting rate (4 kHz for a 400 kHz clock). The LSD, TSD, SSD and MSD (least significant, third significant, second significant and most significant digits) outputs indicate by a low level which decade latch is displayed at the BCD outputs.

FUNCTIONAL DESCRIPTION (Continued)

Overrange Blanking and Sign: The data in the latch for the ÷2 counter is used to detect an out-of-range voltage. If this latch is "0" the BCD and 10k outputs are forced to all "1's" and the SGN output is inverted. When the data in the overrange latch and the sign bit latch are "1" the sign bit generates the 9's complement of the decade latches and the complement of the 10k latch at the respective outputs. When the overrange bit is "1" and the sign bit is "0" true BCD of the decade latches and the uncomplemented 10k latch appear at the outputs.

APPLICATIONS INFORMATION

The MM5330 is the display and control for a modified dual slope system. It contains the counters and latches, together with a multiplexing system to provide 4 digits of display with one decoder driver. It also provides a sign digit, either plus or minus, and a ten-thousand counts digit for full display of ±19999. By eliminating the right-most digits it may also be used as a 2-1/2 or 3-1/2 digit DVM chip.

The basic modified dual slope system for which the MM5330 is designed, is shown in *Figure 1.* The integrator is now used in a non-inverting mode and is biased to integrate negatively for all voltages below V_{MAX}. Thus if the maximum positive voltage at V_{IN} is 1.9999V, then V_{MAX} would be set at 2.200V. In this way, all voltages measured are below V_{MAX}. This eliminates the need for reference switching and provides automatic polarity with no additional components. Also, it can be shown that the amplifier input bias currents which cause errors in conventional dual slope systems are eliminated by merely zeroing the display. Thus low bias current op amps are not necessarily required unless a high input impedance is desired at V_{IN}.

count diagram

INTERNAL STATES / OUTPUTS WITH TRANSFER LOW (CONTINUOUS COUNT)

Internal zone	OVERRANGE BIT COMPLEMENT	SIGN BIT	10k BIT	DECADE COUNTERS				Output zone	INT (AFTER RESET)	SGN	10k	BCD DECADE OUTPUTS			
BLANKING ZONE	0	0	0	0	0	0	0	OUTPUT BLANKED	1	1	1				
	0	0	0	0	0	0	1		1	1	1				
	0	0	0	0	0	0	2		1	1	1				
				•								•			
	0	0	0	9	9	9	9		1	1	1				
	0	0	1	0	0	0	0		1	1	1				
				•								•			
	0	0	1	7	9	9	9		1	1	1				
	0	0	1	8	0	0	0	POSITIVE OVERRANGE	0	1	1				
				•								•			
	0	0	1	9	9	9	9		0	1	1				
COMPLEMENT OUTPUT INTERVAL (DISPLAY ZONE)	1	1	0	0	0	0	0	POSITIVE VALUE	0	1	1	9	9	9	9
				•								•			
	1	1	0	9	9	9	9		0	1	1	0	0	0	0
	1	1	1	0	0	0	0		0	1	0	9	9	9	9
				•								•			
	1	1	1	9	9	9	9		0	1	0	0	0	0	0
TRUE OUTPUT INTERVAL (DISPLAY ZONE)	1	0	0	0	0	0	0	NEGATIVE VALUE	0	0	0	0	0	0	0
				•								•			
	1	0	0	9	9	9	9		0	0	0	9	9	9	9
	1	0	1	0	0	0	0		0	0	1	0	0	0	0
				•								•			
	1	0	1	9	9	9	9		0	0	1	9	9	9	9
BLANKING ZONE	0	1	0	0	0	0	0	NEGATIVE OVERRANGE	0	0	1				
				•								•			

APPLICATIONS INFORMATION (Continued)

Secondly, the use of a conventional op amp for a comparator allows zeroing of all voltage offsets in both the op amp and comparator. This is achieved by zeroing the voltage on the capacitor through the use of the comparator as part of a negative feedback loop. During the zeroing period, the non-inverting input of the integrator is at V_{REF}. As this voltage is within the active common-mode range of the integrator the loop will respond by placing the integrator and comparator in the active region. The voltage on the capacitor is no longer equal to zero, but rather to a voltage which is the sum of both the op amp and comparator offset voltages. Because of the intrinsic nature of an integrator, this constant voltage remains throughout the integrating cycle and serves to eliminate even large offset voltages.

The waveforms at the output of the integrator are as shown. The voltage at A is the comparator threshold just discussed. Simultaneously, with the opening of switch A, V_{IN} is connected to the input of the integrator via switch B. The output then slews to V_{IN}. Integration then begins for the reference period, after which time the reference voltage is again applied to the input. The output again slews the difference between V_{REF} and V_{IN} and integrates for the unknown period until the comparator threshold is crossed. At this point, the accumulated counts are transferred from the counters to the latches and zeroing begins until the next conversion interval.

It may be obvious, however, that while we have eliminated several of the basic dual slope circuits disadvantages, we have created another—the number of counts are no longer proportional to V_{IN} but rather to ($V_{MAX}-V_{IN}$). In fact, when we short V_{IN} to ground we are actually measuring our own 2.2000 V_{MAX}.

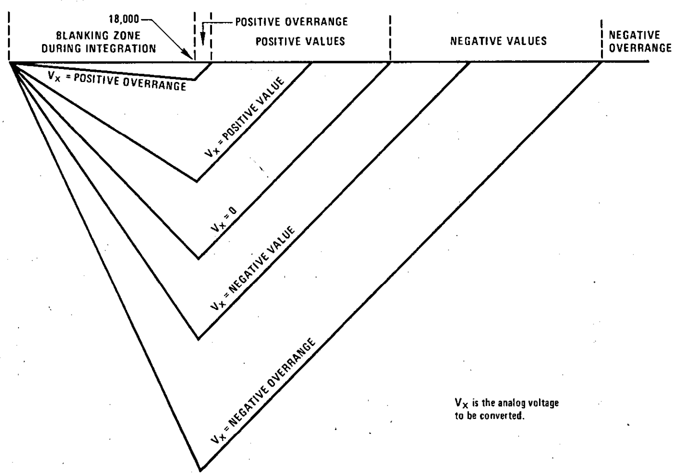
What is done in the MM5330 is to code convert the number of counts as shown in the count diagram. This chart shows a code conversion starting at the time of a reset. The first 18,000 counts are the reference period after which time the integrator changes slope. If a comparator crossing is detected within the next 2000 counts, a plus overrange condition will occur at the display. This condition results in a lit "+" sign, a lit "1" and four blanked rightmost digits. A transfer at 20,000 however, will create a reading of +1.9999, at 20,001 a reading of 19.998 and so on, until at 39,999 a reading of +0000 would be displayed. A transfer occuring at 40,000 would cause a −0000 display and so on until 60,000 counts were entered at which time a −1 with four blanked digits would be displayed indicating a minus overrange condition.

A typical circuit for a low cost 4 1/2 digit DPM is shown in *Figure 2.* The display interface used is a TTL, 7-segment decoder driver and four P-type transistors. The ±1 digit is driven directly by CMOS. The clock-synchronous reset and transfer functions prevent any cyclic digit variations and present a blink-free, flicker-free display. CMOS analog switches are used as reference, zero, and input switches and used also in the comparator slew rate circuit.

A problem with all dual slope systems occurs when short integrating times and high clock frequencies are used. Because of the very slow rise time of the ramp into the comparator, the output of the comparator will normally ramp at approximately 1/10 of its actual slew rate. Thus, a significant number of extra counts are displayed due to the slow rate of rise of the comparator. A technique to improve this consists of capacitor C_S and analog switch four. An unstable positive loop is created by this capacitor when the comparator comes out of saturation. This causes the output to rise at its slew rate to the comparator threshold. As soon as this threshold is reached the analog switch opens and zeroing is initiated as previously discussed.

A simplified approach to performing the modified dual slope function combines the MM5330 and the LF11300 dual slope analog block as in *Figure 3.* The LF11300 provides the front analog circuitry required. This includes a FET input amplifier, analog switches, integrator and comparator. The LF11300 provides auto zero, > 1000 MΩ input impedance, and a ±10V analog range.

dual slope diagram



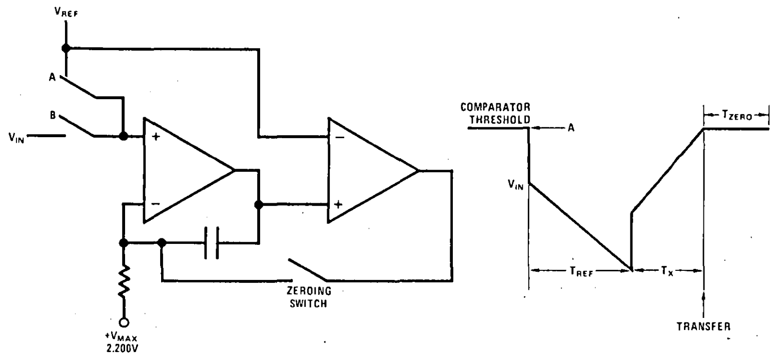


FIGURE 1. Modified Dual Slope

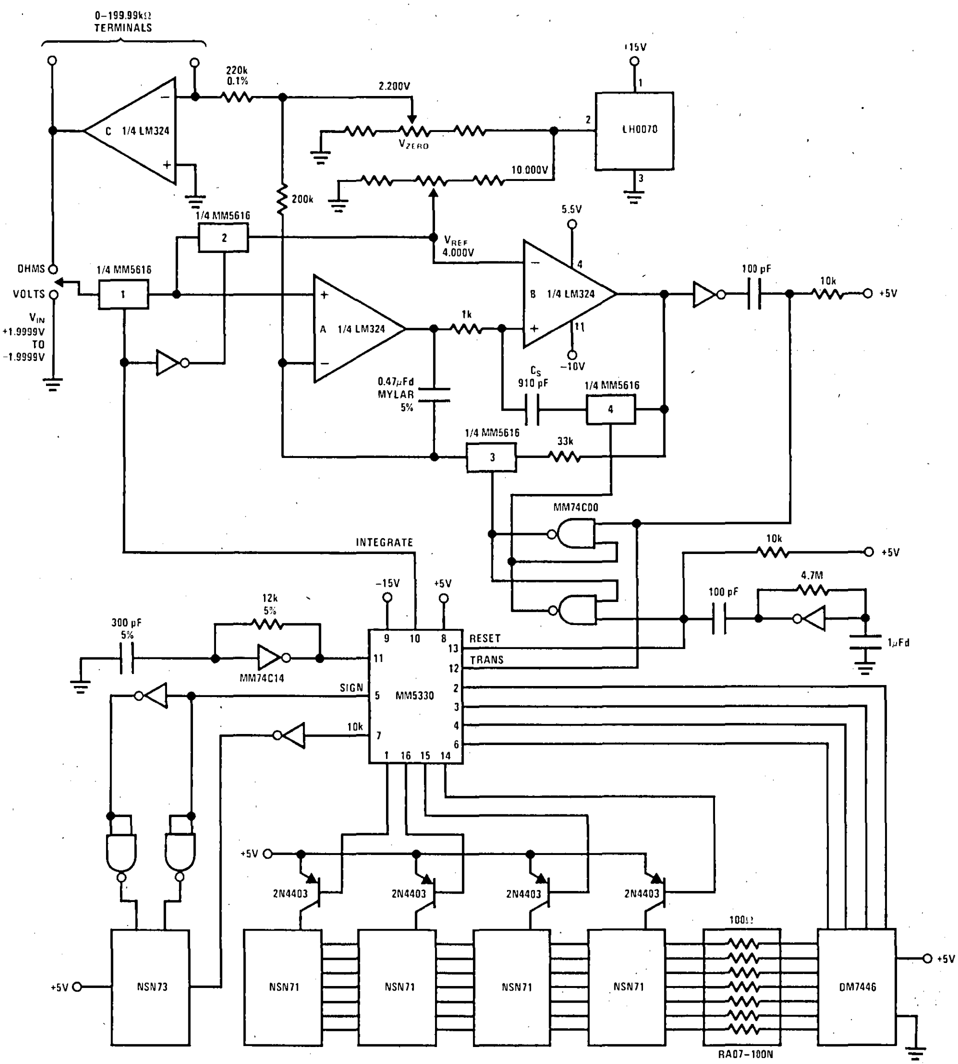
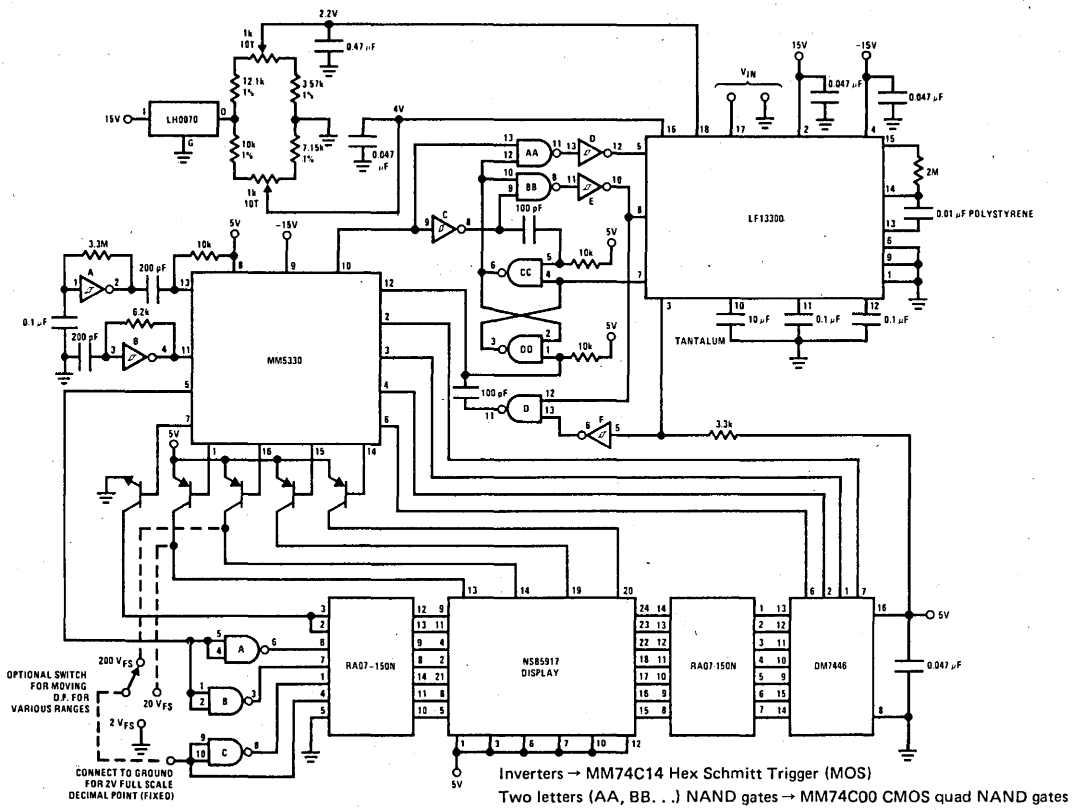


FIGURE 2. Typical Application Low Cost 4 1/2 Digit Volt-Ohm Meter

typical applications (Continued)



Inverters → MM74C14 Hex Schmitt Trigger (MOS)

Two letters (AA, BB. . .) NAND gates → MM74C00 CMOS quad NAND gates

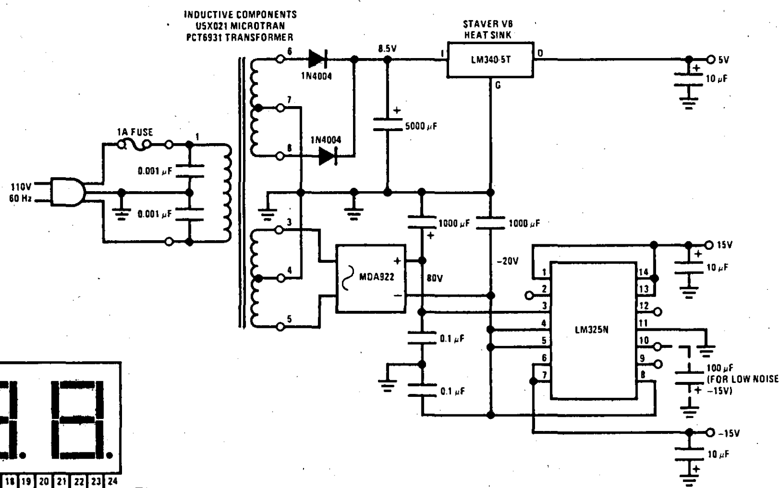
One letter (A, B. . .) NAND gates → DM7400 TTL quad NAND gates

↓→ analog ground

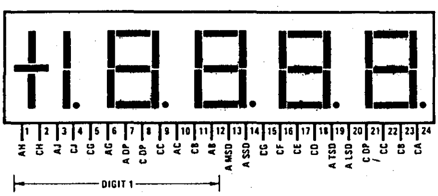
→ digital ground

All resistors 1/4W, 5% unless otherwise noted.

All capacitor values in μF unless otherwise noted.



(Second letter code)



NSB5917 Display (Front View)

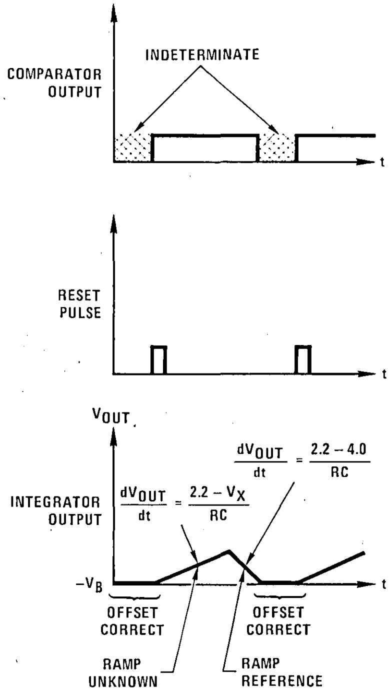
First letter code:

A → anode	MSD → digit 2
C → cathode	SSD → digit 3
	TSD → digit 4
	LSD → digit 5

FIGURE 3. 4 1/2-Digit DVM

timing diagrams

4 1/2-Digit DPM



Note. Here the LF13300 always operates as an autozeroed, high input impedance inverting integrator; bipolar input voltages are handled by offsetting the analog ground by 2.2V.

Analog to Digital (A/D) Converters

MM5863 12-bit binary A/D building block

general description

The MM5863 is the digital controller for the LF13300D* analog building block. Together they form an integrating 12-bit A/D converter. The MM5863 provides all the necessary control functions, plus features like auto zeroing, polarity and overrange indication, as well as continuous conversion. The 12-bit plus sign parallel and serial outputs are TRI-STATE® TTL level compatible. The device also includes output latches to simplify data bus interfacing.

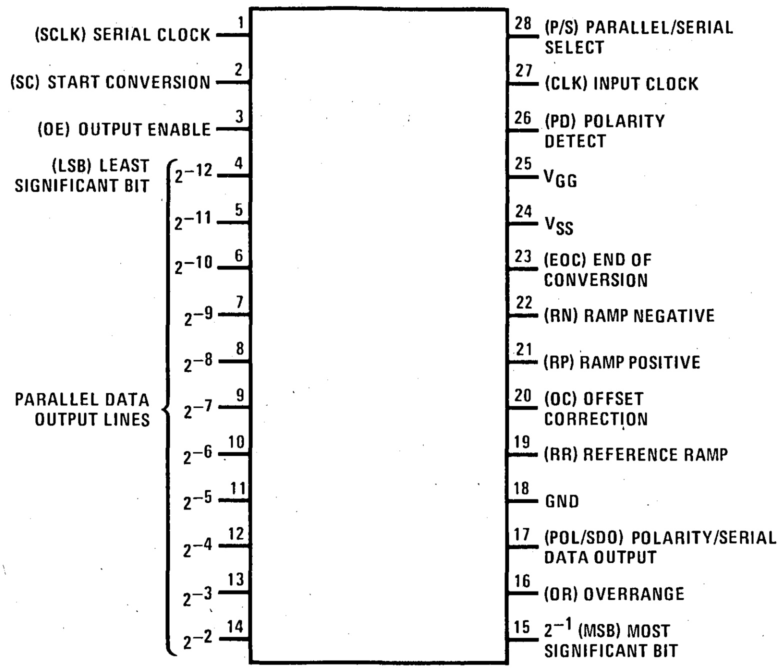
*See LF13300D data sheet for more information

features

- 12-bit binary output
- Parallel or serial output
- Parallel TRI-STATE output
- Polarity indication
- Overrange indication
- Continuous conversion capability
- 100% overrange capability
- 5V, −15V power requirements
- TTL compatible
- Clock frequency to 500 kHz

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5863N
See Package 23

absolute maximum ratings

Supply Voltage (V_{SS})	5.25V
Supply Voltage (V_{GG})	−16.5V
Voltage at Any Input	5.25V
Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +150°C
Clock Frequency	500 kHz
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

V_{SS} = 5V, V_{GG} = −15V, 0°C to +70°C, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage (V_{SS})		4.75	5.00	5.25	V
Power Supply Voltage (V_{GG})		−13.5	−15.00	−16.5	V
Power Supply Current (I_{SS})				28	mA
Power Supply Current (I_{GG})				34	mA
Logic "1" Input Voltage		3.4			V
Logic "0" Input Voltage				0.8	V
Logic "1" Output Voltage	V_{SS} = 4.75, I_{OH} = 100 μA	3.8			V
Logic "0" Output Voltage	V_{SS} = 5.25, I_{OL} = −1.6 mA			0.4	V
Width of EOC	Auto Cycle	5/f			Sec
Prop. Delay PD to EOC		4/f		5/f+1 μs	Sec
Output Enable Time	OE to Any Data Output, SC = 1, P/S = 0			1.0	μs
Output Disable Time	OE to Any Data Output, SC = 1, P/S = 0			2.4	μs
Output Enable Time	P/S to Any Data Output Except Polarity, SC = 1, OE = 0			0.9	μs
Output Disable Time	P/S to Any Data Output Except Polarity, SC = 1, OE = 0			2.2	μs
Output Enable Time	SC to Any Data Output, OE = 0, P/S = 0			1.0	μs
Output Disable Time	SC to Any Data Output, OE = 0, P/S = 0			2.4	μs
Prop. Delay Serial Clock	SCLK to POL/SDO			0.6	μs
Conversion Time	Full Scale			8966/f	Sec
Conversion Time	100% Overrange			13062/f	Sec

functional description

OPERATION

The MM5863 is designed for use with the LF13300 analog front end. Four control signals are supplied to the LF13300 and 1 control signal is required from the LF13300. The conversion cycle is composed of 5 distinct phases. They are: Phase I – Offset Correct; Phase II – Polarity Detect; Phase III – Offset Correct; Phase IV – Ramp Unknown; Phase V – Ramp Reference.

Phase I – Offset Correct (256 Clock Periods)

This phase is initiated by taking the Start Conversion (SC) and the Output Enable (OE) lines to a logic "1". At this time, Offset Correct (OC) will be a logic "1". The LF13300 requires this phase to correct any intrinsic offset voltage errors prior to the polarity detect phase.

Phase II – Polarity Detect (256 Clock Periods)

This phase is used to determine polarity of the analog input. At the midpoint of this phase, PD from the LF13300 is examined for polarity. If PD = logic "1", then the input voltage is positive. If PD = logic "0", then the input is negative. The Ramp Positive signal (RP) will be a logic "1", and Offset Correct will be logic "0" for the entire phase of 256 clock periods. The above operation is also necessary to determine which integrator input (positive or negative) of the LF13300 should be used for proper A/D conversion (see LF13300 data sheet).

Phase III – Offset Correct (256 Clock Periods)

This phase is identical to Phase I and is used by the LF13300 to eliminate any offsets induced as a result of the Polarity Detect Phase. Offset Correct (OC) will be at a logic "1".

Phase IV – Ramp Unknown (4096 Clock Periods)

The unknown input voltage is integrated for a fixed time during this phase. The result of the Phase II Polarity Detect Cycle determines whether RP or RN will be at logic "1". If Phase II indicates a positive input, the RP signal will be a logic "1". If phase II indicates a negative input, Ramp Negative (RN) will be a logic "1". These 2 signals will never be at logic "1" simultaneously.

Phase V – Ramp Reference

This phase is a variable length phase depending on the magnitude of the analog input voltage. During this time, Ramp Reference (RR) will be in the logic "1" state. When PD goes to a logic "0" state, or when the internal counter reaches 100% of full scale (8192 clock periods), the Ramp Reference (RR) signal goes to the logic "0" state, the counter output is loaded into the output register, and the End of Conversion, (EOC) signal goes to a logic "1". The Polarity Bit will reflect whatever value was determined during Phase II. The output register will hold the data until a new conversion is completed and new data is loaded into the register. The OE line must be low in the logic "0" state and SC must be high in the logic "1" state to enable the outputs.

DATA OUTPUTS

Both serial and parallel outputs are available. In either case, OE must be low and SC must be high to enable the outputs. For parallel output, the P/S line must be low in the logic "0" state. For serial outputs, the P/S line must be high. In the serial mode, the data is shifted out of the Polarity/Serial Output POL/SDO line and all other data outputs are in the high impedance state. Each Serial Clock (SCLK) will right shift the output register one bit. Thus, 13 clock pulses are required to fully shift out the data. The data will be shifted out in the following order: Polarity, Overrange, MSB, 2SB, 3SB, . . ., LSB. If OE and P/S are in the logic "0" state and SC in the logic "1" state, all outputs will momentarily go to the logic "1" state for 1 clock period immediately preceding EOC.

CONTINUOUS CONVERT MODE

In this mode, the End of Conversion (EOC) output is connected to the OE input. As long as SC is in the logic "1" state, then each EOC will initiate a new conversion. The data outputs will be disabled for the first 5 clock cycles after EOC goes high.

truth table

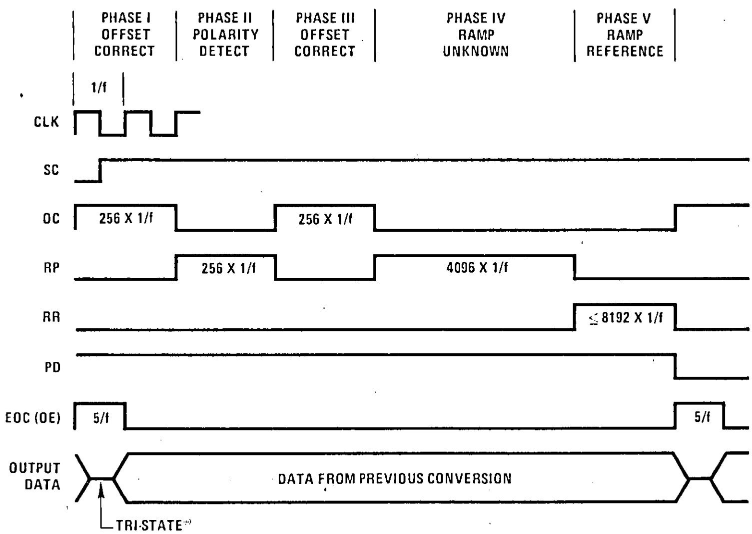
INPUT	SC	OE	P/S	LSB											MSB	OVER-RANGE	POLARITY
100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Zero	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
−Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
−100% Full Scale	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
Any	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Any	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Serial Output
Any	0	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

1 = High
0 = Low
Z = High Impedance
X = Don't Care

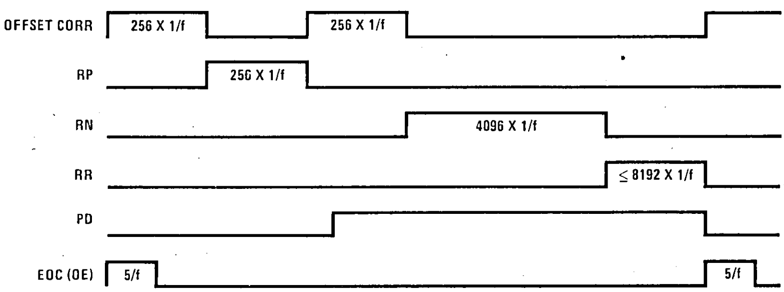
timing diagrams

The following timing diagrams are shown for the MM5863 connected in the auto-cycle mode.

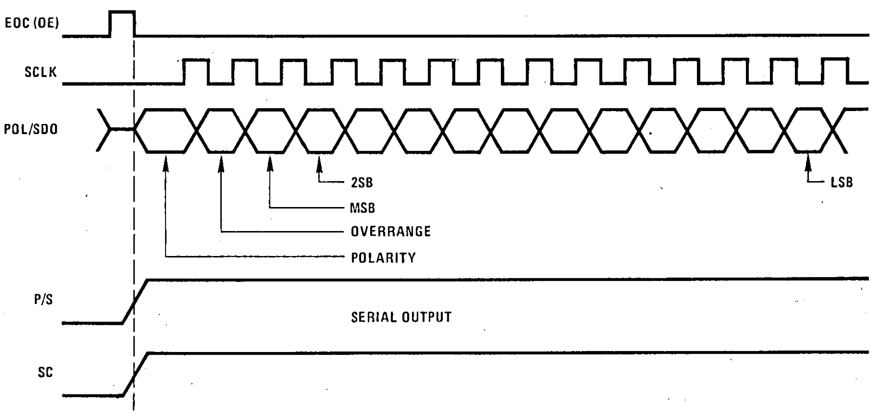
Positive Input



Negative Input



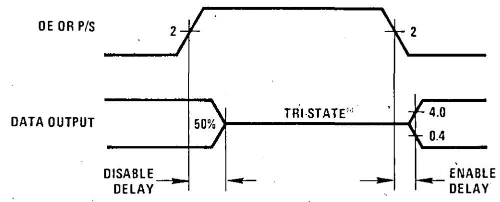
Serial Output



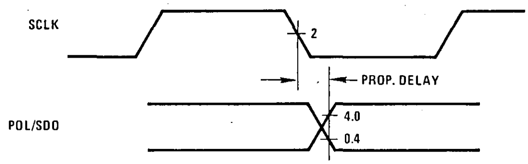
5

timing diagrams (Continued)

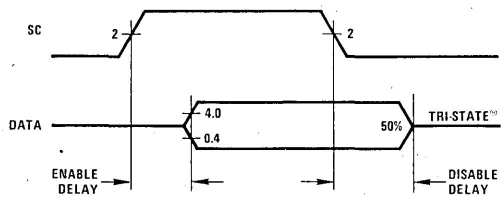
Output Enable/Disable Time



Serial Clock Delay

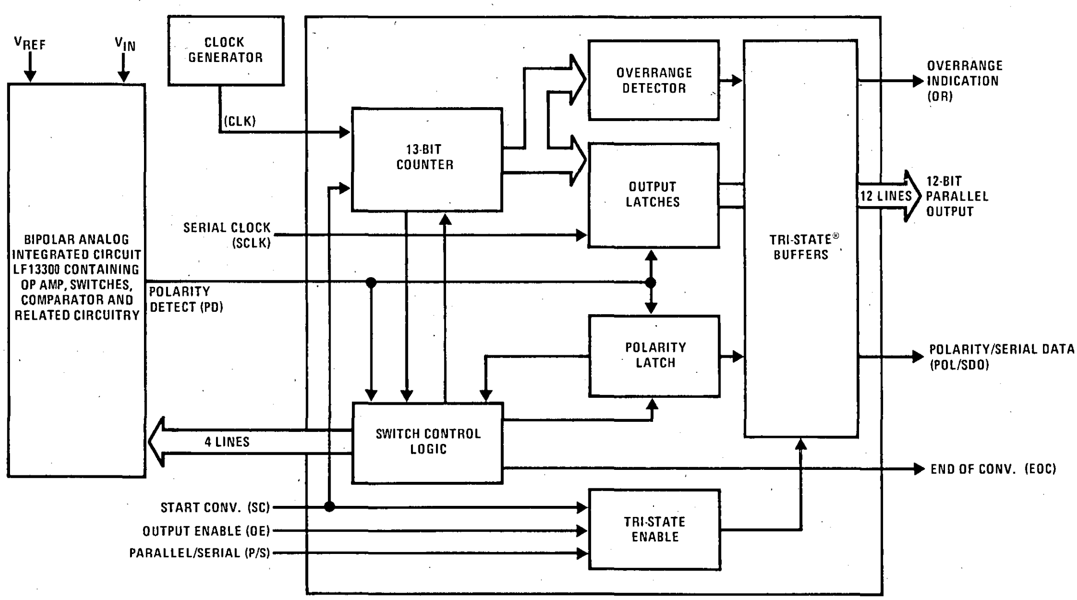


Output Enable/Disable Time



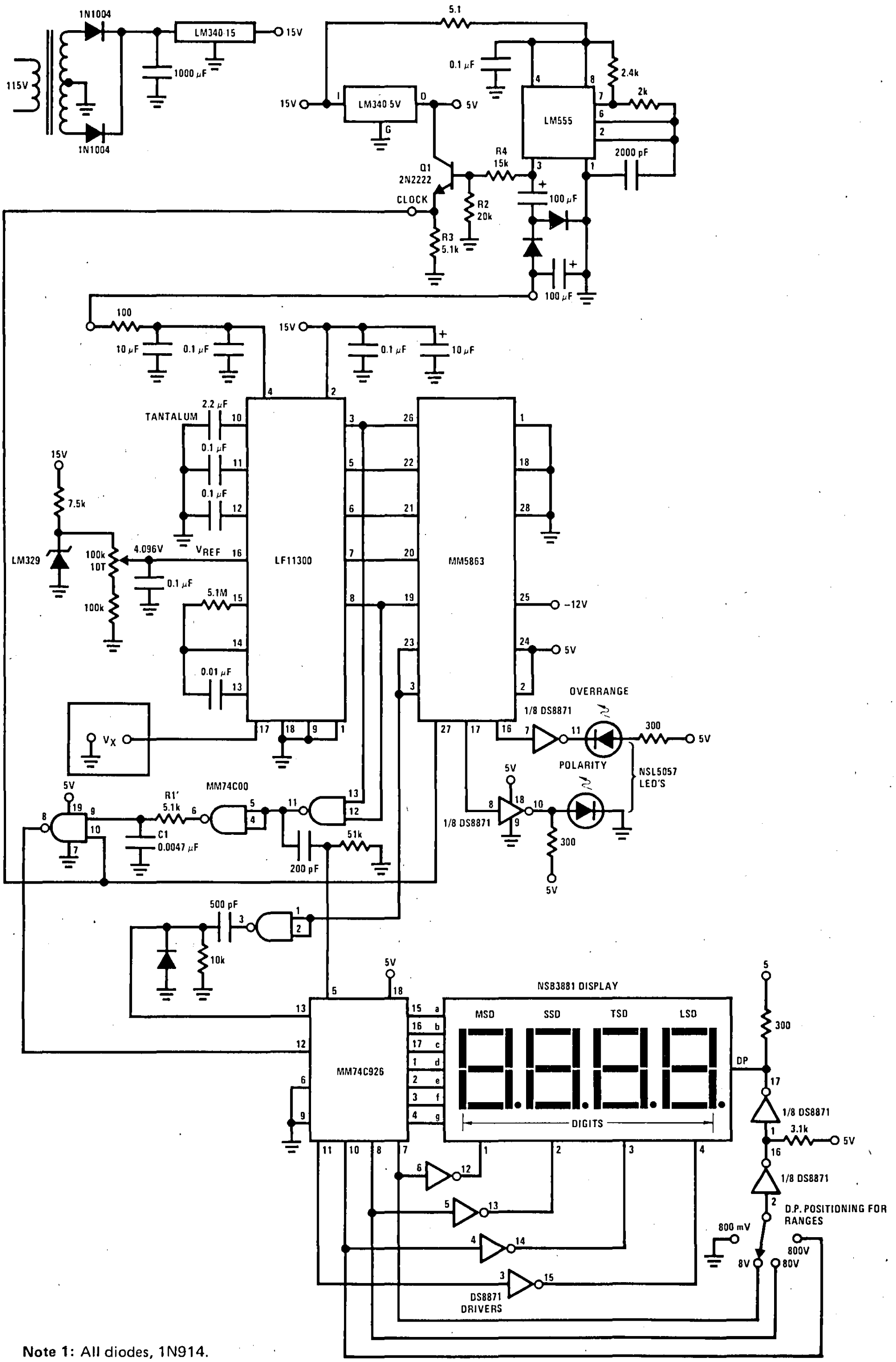
block diagram

Digital Control Integrated Circuit



typical applications

3 3/4–3 1/2-Digit DPM



Note 1: All diodes, 1N914.

Note 2: All resistors 1/4W, 5% tolerance.

Note 3: Circuit drawn for 8V full scale operation input scaling not shown.

Analog to Digital (A/D) Converters

DIGITAL VOLTMETERS AND THE MM5330

INTRODUCTION

The first of what could be called the modern digital voltmeter began to appear in the early sixties. Prior to that time a few laboratory types were available, but they were plagued by inaccuracy, temperature drifts, and other problems inherent in vacuum tube technology.

One of the first successful, relatively low cost DMVS was a gated voltage-controlled oscillator configuration. The components of this technique consist of a high gain amplifier, a dc-to-frequency converter, and a linear, accurate frequency to-dc-converter developed from the reference voltage, which supplies the summing voltage at the input node. The amplifiers used were of the chopper stabilized type, that is, the error voltage is chopped to from an ac component which is amplified by ac coupled amplifiers then reconverted to dc. The choppers were made with light sensitive resistors, neon bulbs and light pipes.

They were built as the only method possible to avoid the drifts and offsets which were unavoidable in early transistor technology. Obviously the low current op amps so readily available today, are a significant advantange over these old systems.

The gate voltage was developed from the 60 Hz line. A problem which occurs when the gate is asynchronous with the frequency fed to the display counter, is also shown in *Figure 1*. A beat frequency effect is developed between the gate and the dc to frequency converter and produces a cyclic one digit error. These early voltmeters allowed this phenomenon to occur, today cyclic display errors are unacceptable.

A second display characteristic of these early voltmeters, was to use the ripple counters as the display storage, that is, the rippled counts would move through the display until the gate closed and the final value would be displayed. This was done primarily because of the number of discrete devices required to perform counting and latching. With the coming of integrated circuits, displays were improved, latches were employed, and blink-free displays were adopted.

Polarity selection was made by a front panel switch which internally rearranged references and other circuitry.

An example of today's use of the VCO technique is shown in *Figure 2.* This is a low cost digital thermometer, which, while not a DVM, still employs the basic components of the voltage-controlled oscillator system. These are the high gain amplifiers contained in the LM5700, the dc-to-frequency converter consisting of the transistor source and LM555 timer, and the frequency-to-dc converter consisting of the CMOS inverters and reference voltage. This brings up a characteristic of CMOS most useful in DVM's and other analog-to-digital converters, the ability to switch directly to the supply and ground without offsets. In this case the fixed width negative-going pulses, when filtered, produce a feedback voltage directly proportional to the number of pulses—frequency-to-dc conversion.

The early counter storage display system previously mentioned, is shown in *Figure 3.* Because the best display available was the gaseous tube, no attempt was made to blank displays during the counting period. When the gate closed, the counters had reached a certain count and these counts were displayed.

After the development of the integrated circuit, displays took on a configuration as in *Figure 4.* Between the counters and display, latches were placed to display previous data while new counts were accumulated. The cost and pack count of this scheme made another display technique popular, that of multiplexing.

Briefly, this technique consists of connecting, sequentially, each of the latches to a single decoder driver which drove the display digit which corresponded to that latch. When sequenced at a 50 Hz rate or greater, a flicker-free display results. For this type of display system, TRI-STATE® counter-latches were developed *(Figure 5).* This technique is still used today in many DVM's.

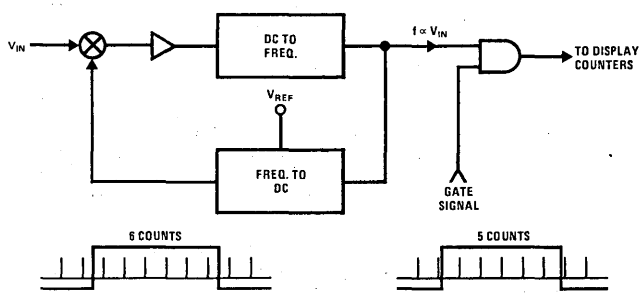


FIGURE 1. Basic VCO Scheme

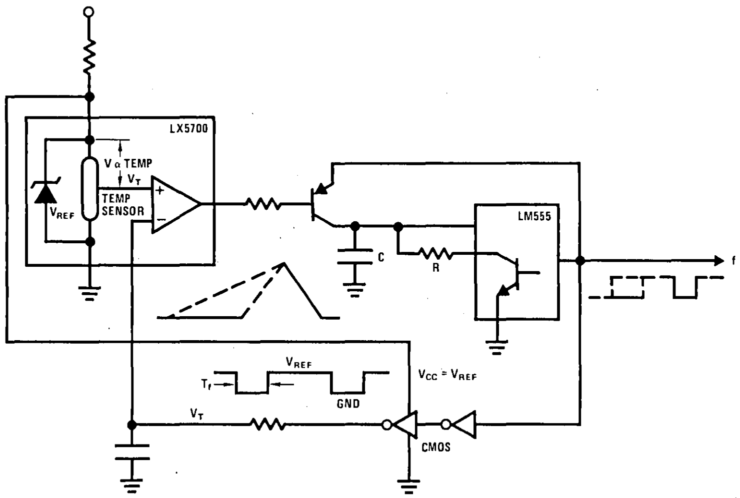


FIGURE 2. Typical VCO Circuit

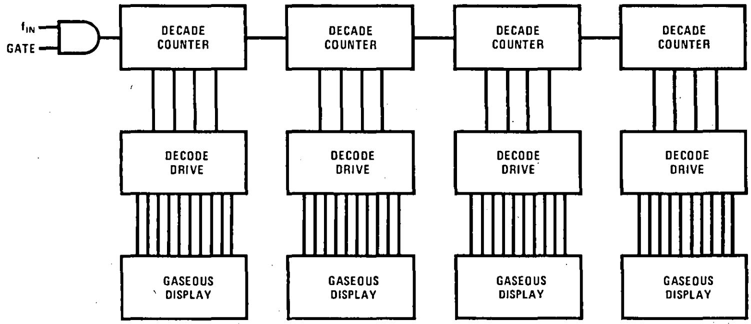


FIGURE 3. Early Display Configuration

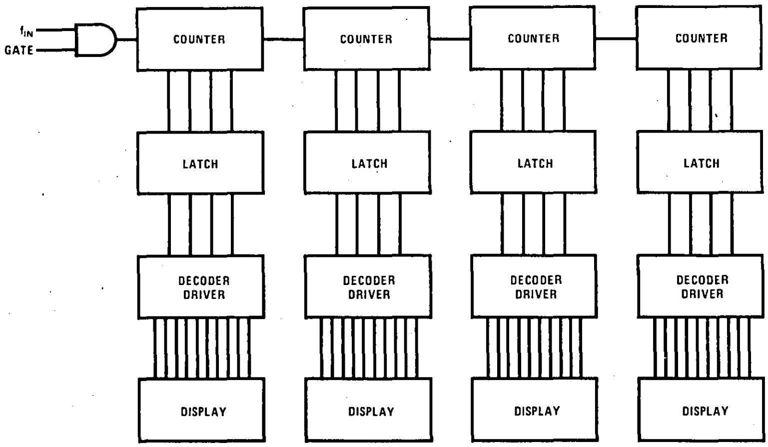


FIGURE 4. Integrated Circuit Display

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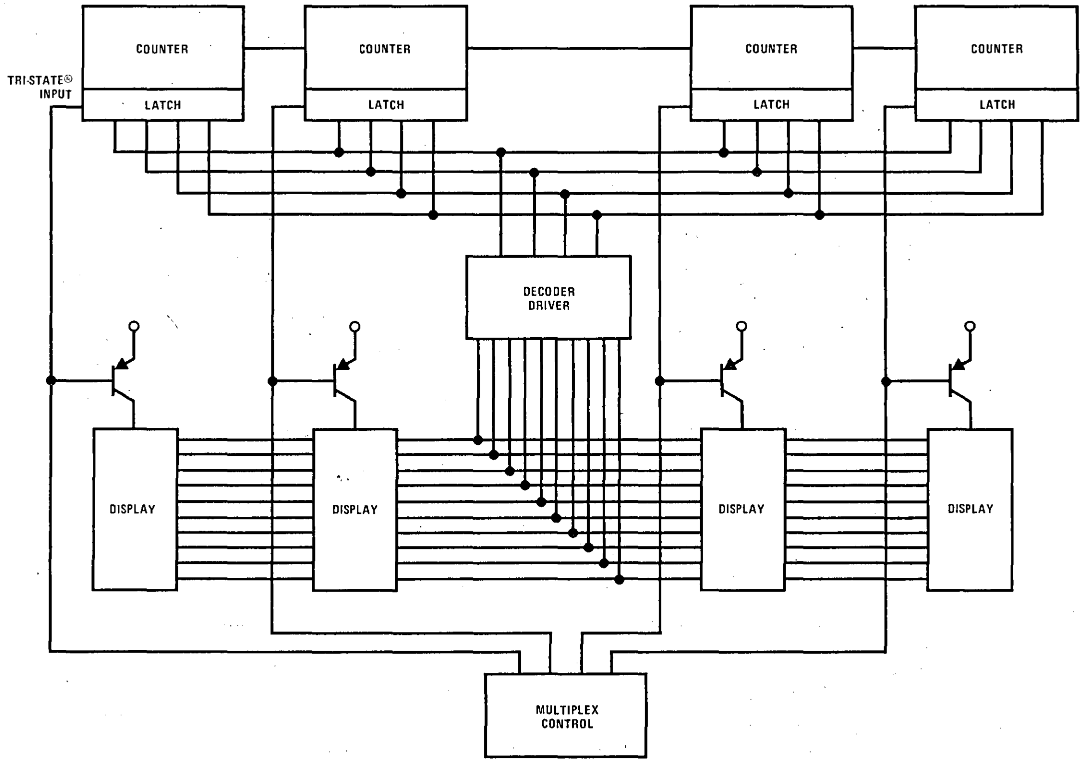


FIGURE 5. Multiplexed Display

While multiplexing cuts display costs considerably, the series connection of counters required to accumulate the counts proportional to voltage, could not be multiplexed to do the very nature of VCO or dual slope voltmeter schemes.

The recirculating remainder circuitry to be discussed next is unique in that the data is both derived and displayed on multiplexed, that is sequential digit basis (as seen in *Figure 6*.)

The technique used in the recirculating remainder circuit is to subtract digit valued voltage steps from the input voltage, until ten times the difference between these two voltages is less than ten times the digit valued steps. The number of voltage steps required is the display data and the ten times the difference voltage becomes the new voltage input for the next digit conversion. An example is shown in *Figure 7.*

An analog input of 6.903V is applied to the $[(V_{IN}-V_{STEP}) \times 10]$ amplifier. The $\div 12$ and decade counters are clocked simultaneously until a (difference x 10) less than V_{REF} is detected by the comparator. At this time, the decade counter stops counting. In this example, the decade counter ceases counting on a six during the digit one period, thus a six is latched in the display. When the digit period ends, both counters are reset and the (difference x 10) voltage is recirculated via the CMOS switch and sample and hold capacitor to become the digit two input voltage (9.03V). The process is then repeated for the next digit. At a repetition rate of 50 Hz or greater, this produces a flicker-free, blink-free display. As such the recirculating remainder system has but one counter, one latch, and one decoder driver for as many digits as are desired. Once again CMOS is used for its capability to swing directly to the supply rail and controls the R-2R ladder directly from the reference voltage.

Some disadvantages of the system are the difficulties in reading voltages of both polarities and an unusual sort of error characteristic when slight ladder or reference drifts occur. While both VCO and dual slope techniques have gradual slope or linearity errors, the recirculating remainder errors are step-like in response to gradual input voltage changes. Lastly, the update rate is fixed by display flicker requirements and thus measurements of noisy voltages cause an annoying inability to read the last digits. It was however, an accurate low-cost technique used successfully in pre-LSI digital voltmeters.

The most widely used system for analog-to-digital conversion is the dual slope circuit. The basic dual slope system appears in *Figure 8.* Assuming the integrator output at zero when V_x is applied, the integrator begins to ramp with an output voltage $V = I_x\ t/C$ where $I_x = -V_x/R$. Simultaneously with the beginning of this ramping, counts from an oscillator are fed into the display counters. At some fixed time, usually counter overflow, V_x would be disconnected and the reference voltage connected to the resistor. The integrator now ramps at $V = I_{REF}\ t/C$ where $I_{REF} = V_{REF}/R$.

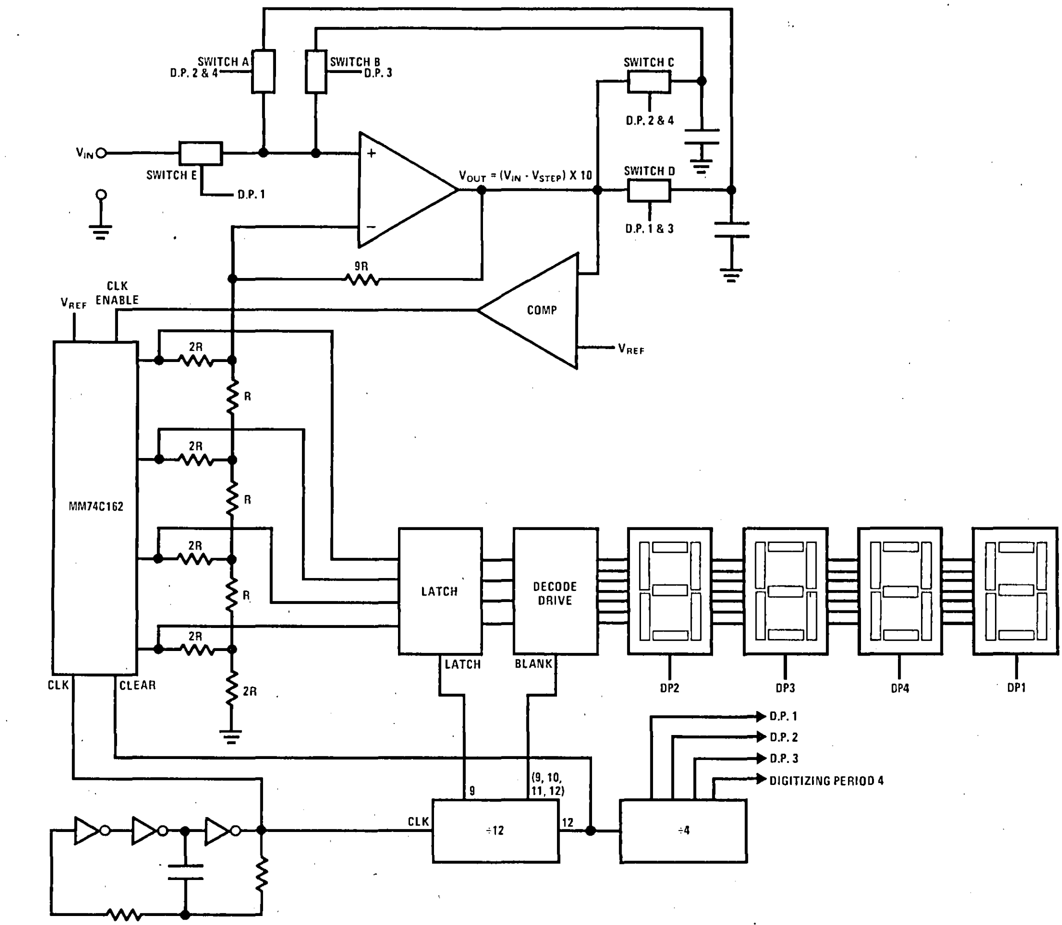
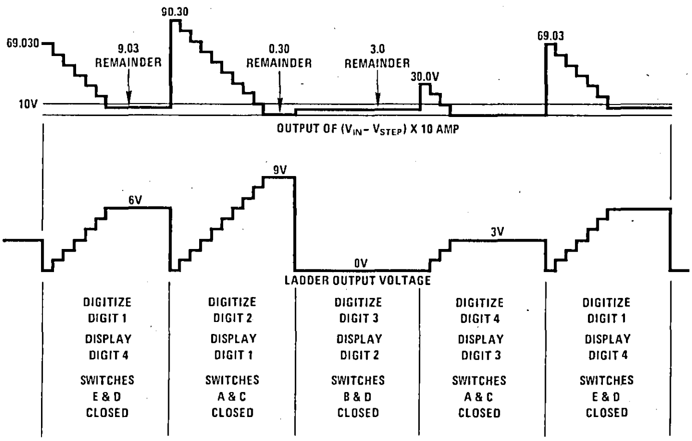


FIGURE 6. Basic Recirculating Remainder System



Example: (Voltage in = 6.903V)

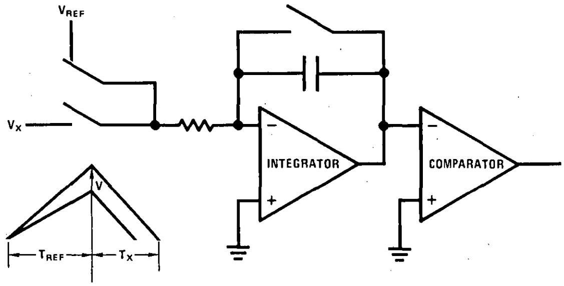
6.903
<u>−6.000</u> 6 1.000V steps—display 6
0.903 x 10 = 9.03

9.030
<u>−9.000</u> 9 1.000V steps—display 9
0.03 x 10 = 0.3

0.300
<u>−0.000</u> 0 1.000V steps—display 0
0.3 x 10 = 3

3.000
<u>−3.000</u> = 3 1.000V steps—display 3

FIGURE 7. Recirculating Remainder Waveforms



$$V = \frac{I_x t_{REF}}{C} \qquad I_x = -\frac{V_x}{R}$$

$$-V = \frac{I_{REF} T_x}{C} \qquad I_{REF} = \frac{V_{REF}}{R}$$

$$\frac{I_x T_{REF}}{C} = -\frac{I_{REF} T_x}{C}$$

$$\therefore V_x T_{REF} = V_{REF} T_x$$

FIGURE 8. Basic Dual Slope

When the integrator crosses the comparator threshold, the counters are latched to the number of counts accumulated from T to T_x. Clearly the voltage at T_{REF} was I_x T_{REF}/C and the voltage integrated from T_{REF} to T_x was $-I_{REF}$ T_x/C and these two voltages are equal. Therefore,

$$\frac{I_x \; T_{REF}}{C} = \frac{-I_{REF} \; T_x}{C} \text{ or}$$

$$V_x \; T_{REF} = V_{REF} \; T_x$$

Thus, the number of counts accumulated in the display from T_{REF} to T_x is proportional to the unknown voltage. Thus, the basic dual slope system has no gate, and requires stability of the R, C and count frequency only over one conversion period.

The technique for insuring that the ramp begins at zero on each conversion cycle, is to short the capacitor with a switch after each conversion is made. This, of course, forces the integrator output to zero until the next conversion period begins. It is also necessary to start each conversion cycle synchronously with the counter input frequency, or cyclic display errors like that of the gated VCO will appear in the display.

To measure both polarities in conventional dual slope systems, V_{REF} must change in polarity. A problem which can occur is that bias currents which will add to the slope in one polarity, will subtract from the slope in the other. The usual solution, is to use op amps of very low input bias current. Also offset voltages in either the op amps or comparator can cause significant error unless carefully controlled.

Hence, while conventional dual slope has many advantages, its use requires considerable care in op amp, and comparator selection. Also, the measurement of either polarity requires two reference voltages which are, in accurate systems, quite expensive.

The MM5330 is the display and control for a modified dual slope system. It contains, as shown in *Figure 9*, the counters and latches, together with a multiplexing system to provide four digits of display with one decoder driver. It also provides a sign digit, either plus or minus, and a ten-thousand counts digit for a full display of ±19999. By eliminating the right-most digits it may also be used as a 2 1/2 or 3 1/2 digit DVM chip.

The basic modified dual slope system for which the MM5330 is designed, is shown in *Figure 10*. The integrator is now used in a non-inverting mode and is biased to integrate negatively for all voltages below V_{MAX}. Thus, if the maximum positive voltage at V_{IN} is 1.9999V, the V_{MAX} would be set at 2.2000V. In this way, all voltages measured are below V_{MAX}. This eliminates the need for reference switching and makes the system automatic polarity, with no additional components. Also, it can be shown that the amplifier input bias currents which cause the aforementioned errors in conventional dual slope systems, are eliminated by merely zeroing the display. Thus, low bias current op amps are not necessarily required unless a high input impedance is desired at V_{IN}.

Secondly, the use of a conventional op amp for a comparator, allows zeroing of all voltage offsets in both the op amp and comparator. This is achieved by zeroing the voltage on the capacitor through the use of the comparator as part of a negative feedback loop. During the zeroing period, the non-inverting input of the integrator is at V_{REF}. As this voltage is within the active common-mode range of the integrator the loop will respond by placing the integrator and comparator in the active region. The voltage on the capacitor is no longer equal to zero, but rather to a voltage which is the sum of both the op amp and comparator offset voltages. Because of the intrinsic nature of an integrator, this constant voltage remains throughout the integrating cycle and serves to eliminate even large offset voltages.

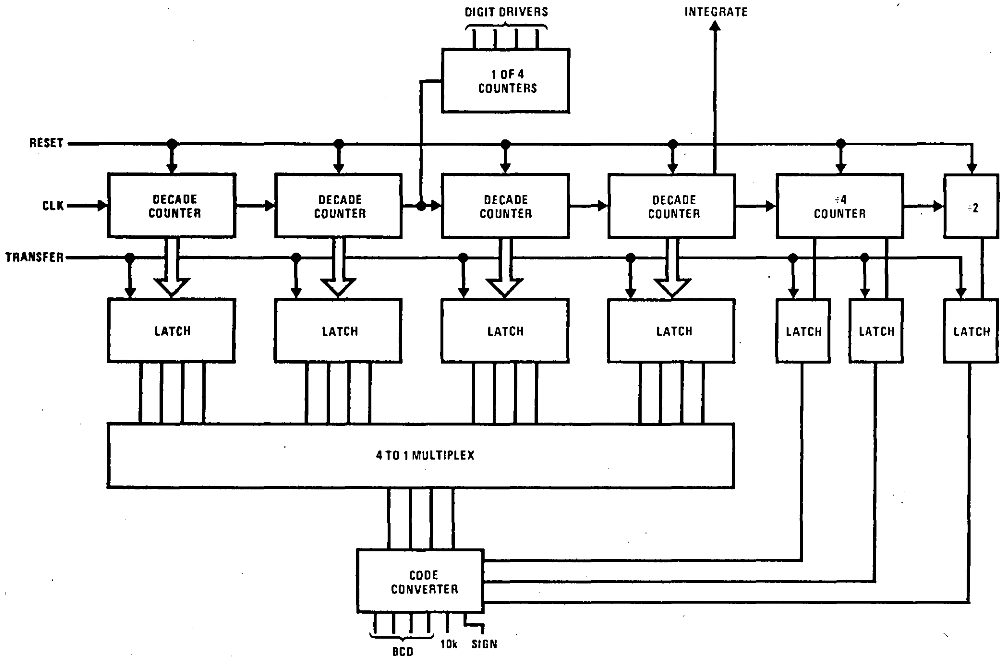


FIGURE 9. Block Diagram MM5330

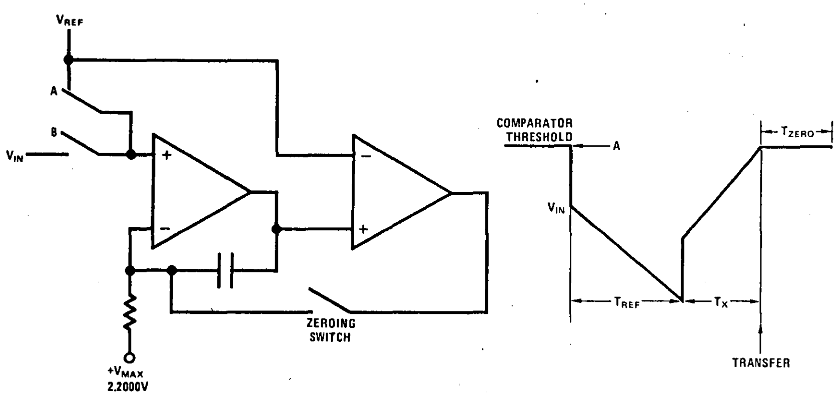


FIGURE 10. Modified Dual Slope

The waveforms at the output of the integrator are as shown. The voltage at A is the comparator threshold just discussed. Simultaneously, with the opening of switch A, V_{IN} is connected to the input of the integrator via switch B. The output then slews to V_{IN}. Integration then begins for the reference period, after which time, the reference voltage is again applied to the input. The output again slews the difference between V_{REF} and V_{IN} then integrates for the unknown period until the comparator threshold is crossed. At this point, the accumulated counts are transferred from the counters to the latches and zeroing begins until the next conversion interval.

It may be obvious, however, that while we have eliminated several of the basic dual slope circuits disadvantages, we have created another—the number of counts are no longer proportional to V_{IN} but rather to $(V_{MAX}-V_{IN})$. In fact, when we short V_{IN} to ground we are actually measuring our own 2.2000V V_{MAX}.

What is done in the MM5330 is to code convert the number of counts as shown in *Figure 11*. This chart shows a code conversion starting at the time of a reset. The first 18,000 counts are the reference period after which time the integrator changes slope. If a comparator crossing is detected within the next 2000 counts, a plus overrange condition will occur at the display. This condition results in a lit plus sign, a lit one and four blanked right-most digits. A transfer at 20,000, however, will create a reading of +1.9999, at 20,001 a reading of 19,998 and so on, until at 40,000 a reading of +0000 would be displayed. A transfer occuring at 40,001 would cause a −0001 display and so on until 60,000 counts were entered at which time a −1 with four blanked zeros would be displayed indicating a minus overrange condition.

A typical circuit for a low cost 4 1/2 digit circuit is shown in *Figure 12.* The display interface used is a TTL, seven-segment decoder driver and four PNP transistors. The ±1 digit is driven directly by CMOS. The clock-synchronous reset and transfer functions prevent any cyclic digit variations and present a blink-free flicker-free display. CMOS analog switches are used as reference, zero, and input switches and used also in a comparator slew rate circuit.

A problem with all dual slope systems occurs when short integrating times and high clock frequencies are used. Because of the very slow rise time of the ramp into the comparator, the output of the comparator will normally ramp at approximately 1/10 of its actual slew rate. Thus a significant number of extra counts are displayed due to the slow rate of rise of the comparator. A technique to improve this consists of capacitor C_S and analog switch section four. An unstable positive loop is created by this capacitor when the comparator comes out of saturation. This causes the output to rise at its slew rate to the comparator threshold. As soon as this threshold is reached the analog switch opens and zeroing is initiated as previously discussed.

The rapid improvement in display and LSI technology has allowed considerable improvement in digital voltmeters. The modified dual slope technique together with the simplified display interface of the MM5330 are felt to be a much improved technique when compared to circuits of just a short time ago. While DVM chips do not by themselves solve all inherent problems, their careful use allows low cost, high accuracy units, with excellent display characteristics.

COUNTS AFTER RESET	DISPLAY
0 . . . 18,000	+1- - - -
. . . 19,999	+1- - - -
20,000 20,001 . . . 40,000	+19999 +19998 + 0000
40,001 . . . 59,999 60,000	− 0001 −19999 −1- - - -

FIGURE 11. Code Conversion Table MM5330

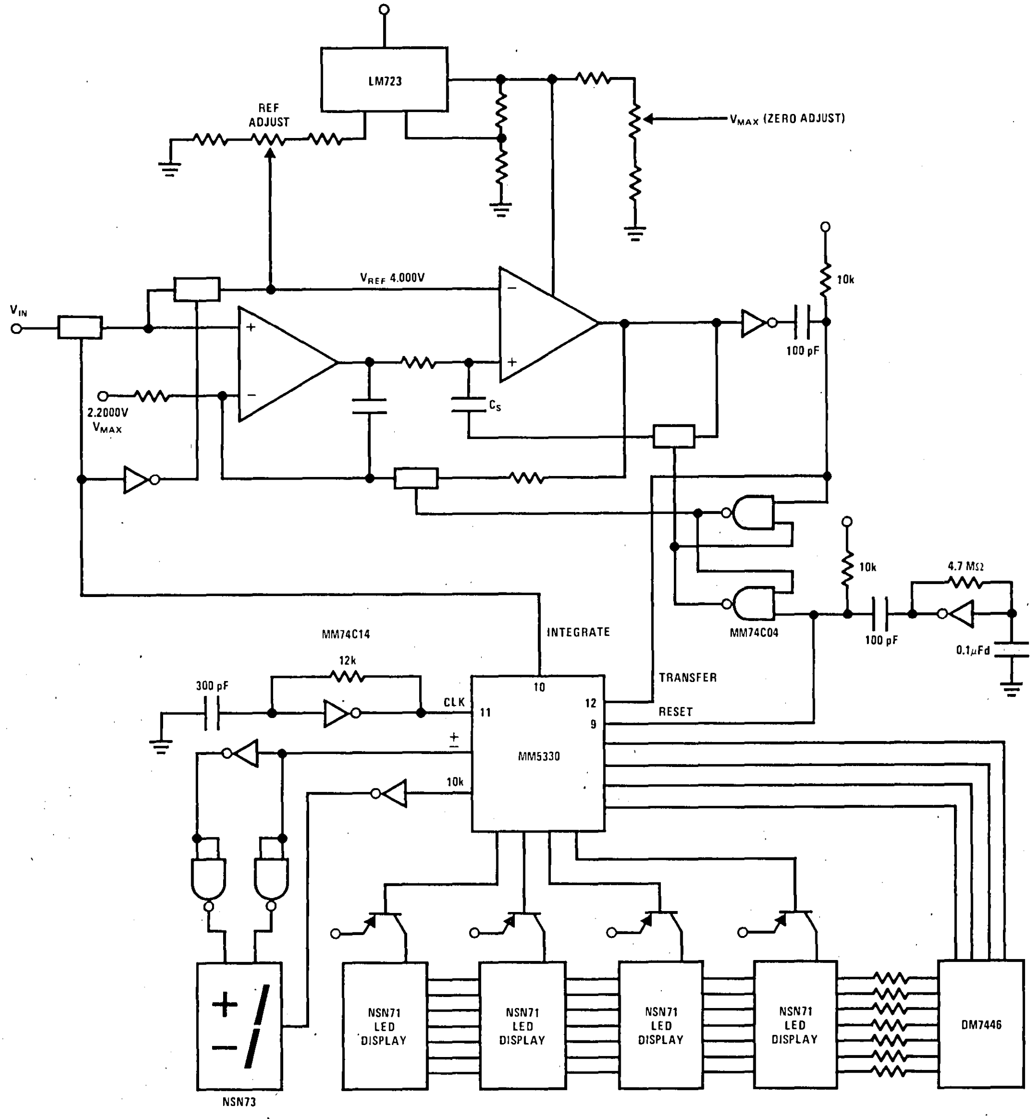


FIGURE 12. Typical Application MM5330

Analog to Digital (A/D) Converters

SPECIFYING A/D AND D/A CONVERTERS

The specification or selection of analog-to-digital (A/D) or digital-to-analog (D/A) converters can be a chancey thing unless the specifications are understood by the person making the selection. Of course, you know you want an accurate converter of specific resolution; but how do you insure that you get what you want? For example, 12 switches, 12 arbitrarily valued resistors, and a reference will produce a 12-bit DAC exhibiting 12 quantum steps of output voltage. In all probability, the user wants something better than the expected performance of such a DAC. Specifying a 12-bit DAC or an ADC must be made with a full understanding of accuracy, linearity, differential linearity, monotonicity, scale, gain, offset, and hysteresis errors.

This note explains the meanings of and the relationships between the various specifications encountered in A/D and D/A converter descriptions. It is intended that the meanings be presented in the simplest and clearest practical terms. Included are transfer curves showing the several types of errors discussed. Timing and control signals and several binary codes are described as they relate to A/D and D/A converters.

MEANING OF PERFORMANCE SPECS

Resolution describes the smallest standard incremental change in output voltage of a DAC or the amount of input voltage change required to increment the output of an ADC between one code change and the next adjacent code change. A converter with n switches can resolve 1 part in 2^n. The least significant increment is then 2^{-n}, or one least significant bit (LSB). In contrast, the most significant bit (MSB) carries a weight of 2^{-1}. Resolution applies to DACs and ADCs, and may be expressed in percent of full scale or in binary bits. For example, an ADC with 12-bit resolution could resolve 1 part in 2^{12} (1 part in 4096) or 0.0245% of full scale. A converter with 10V full scale could resolve a 2.45mV input change. Likewise, a 12-bit DAC would exhibit an output voltage change of 0.0245% of full scale when the binary input code is incremented one binary bit (1 LSB). Resolution is a design parameter rather than a performance specification; it says nothing about accuracy or linearity.

Accuracy is sometimes considered to be a non-specific term when applied to D/A or A/D converters. A linearity spec is generally considered as more descriptive. An accuracy specification describes the worst case deviation of the DAC output voltage from a straight line drawn between zero and full scale; it includes all errors. A 12-bit DAC could not have a conversion accuracy better than ±½ LSB or ±1 part in 2^{12+1} (±0.0122% of full scale due to finite resolution). This would be the case in figure 1 if there were no errors. Actually, ±0.0122% FS represents a deviation from 100% accuracy; therefore accuracy should be specified as 99.9878%. However, convention would dictate 0.0122% as being an accuracy spec rather than an inaccuracy (tolerance or error) spec.

Accuracy as applied to an ADC would describe the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. If a 12-bit ADC is stated to be ±1 LSB accurate, this is equivalent to ±0.0245% or twice the minimum possible quantizing error of 0.0122%. An accuracy spec describes the maximum sum of all errors including quantizing error, but is rarely provided on data sheets as the several errors are listed separately.

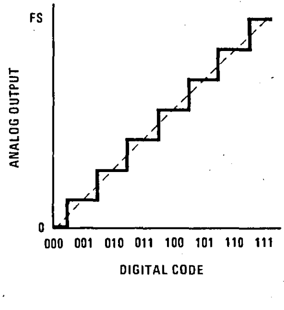


FIGURE 1. Linear DAC Transfer Curve Showing Minimum Resolution Error and Best Possible Accuracy

Quantizing Error is the maximum deviation from a straight line transfer function of a perfect ADC. As, by its very nature, an ADC quantizes the analog input into a finite number of output codes, only an infinite resolution ADC would exhibit zero quantizing error. A perfect ADC, suitably offset ½ LSB at zero scale as shown in figure 2, exhibits only ±½ LSB maximum output error. If not offset, the error will be $^{+1}_{-0}$ LSB as shown in figure 3. For example, a perfect 12-bit ADC will show a ±½ LSB error of ±0.0122% while the quantizing error of an 8-bit ADC is ±½ part in 2^8 or ±0.195% of full scale. Quantizing error is not strictly applicable to a DAC; the equivalent effect is more properly a resolution error.

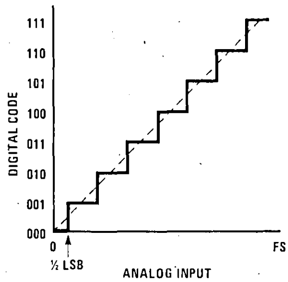


FIGURE 2. ADC Transfer Curve, ½ LSB Offset at Zero

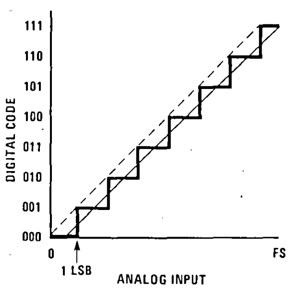


FIGURE 3. ADC Transfer Curve, No Offset

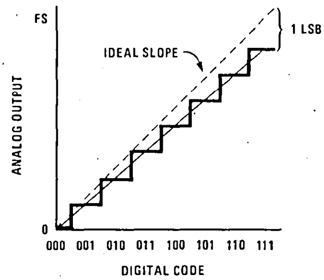


FIGURE 4. Linear, 1 LSB Scale Error

Gain Error is essentially the same as scale error for an ADC. In the case of a DAC with current and voltage mode outputs, the current output could be to scale while the voltage output could exhibit a gain error. The amplifier feedback resistors would be trimmed to correct the gain error.

Offset Error (zero error) is the output voltage of a DAC with zero code input, or it is the required mean value of input voltage of an ADC to set zero code out. (See figure 5.) Offset error is usually caused by amplifier or comparator input offset voltage or current; it can usually be trimmed to zero with an offset zero adjust potentiometer external to the DAC or ADC. Offset error may be expressed in % FS or in fractional LSB.

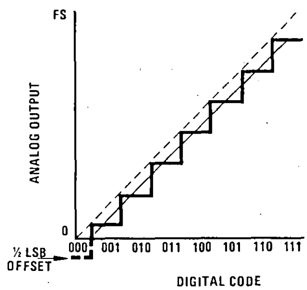


FIGURE 5. Linear, ½ LSB Offset Error

Scale Error (full scale error) is the departure from design output voltage of a DAC for a given input code, usually full-scale code. (See figure 4.) In an ADC it is the departure of actual input voltage from design input voltage for a full-scale output code. Scale errors can be caused by errors in reference voltage, ladder resistor values, or amplifier gain, *et. al.* (See **Temperature Coefficient.**) Scale errors may be corrected by adjusting output amplifier gain or reference voltage. If the transfer curve resembles that of figure 7, a scale adjustment at ¾ scale could improve the overall ± accuracy compared to an adjustment at full scale.

Hysteresis Error in an ADC causes the voltage at which a code transition occurs to be dependent upon the direction from which the transition is approached. This is usually caused by hysteresis in the comparator inside an ADC. Excessive hysteresis may be reduced by design; however, some slight hysteresis is inevitable and may be objectionable in converters if hysteresis approaches ½ LSB.

Linearity, or, more accurately, non-linearity specifications describe the departure from a linear transfer curve for either an ADC or a DAC. Linearity error does not include quantizing, zero, or scale errors. Thus, a specification of ±½ LSB linearity implies error in addition to the inherent ±½ LSB quantizing or resolution error. In reference to figure 2, showing no errors other than quantizing error, a linearity error allows for one or more of the steps being greater or less than the ideal shown.

Figure 6 shows a 3-bit DAC transfer curve with no more than ±½ LSB non-linearity, yet one step shown is of zero amplitude. This is within the specification, as the maximum deviation from the ideal straight line is ±1 LSB (½ LSB resolution error plus ½ LSB non-linearity). With any linearity error, there is a differential non-linearity (see below). A ±½ LSB linearity spec guarantees monotonicity (see below) and ≤ ±1 LSB differential non-linearity (see below). In the example of figure 6, the code transition from 100 to 101 is the worst possible non-linearity, being the transition from 1 LSB high at code 100 to 1 LSB low at 110. Any fractional non-linearity beyond ±½ LSB will allow for a non-monotonic transfer curve. Figure 7 shows a typical non-linear curve; non-linearity is 1¼ LSB yet the curve is smooth and monotonic.

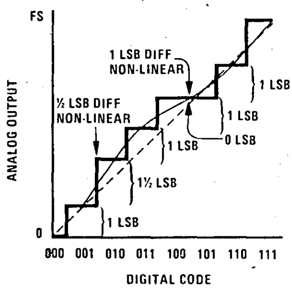


FIGURE 6. ±½ LSB Non-Linearity (Implies 1 LSB Possible Error), 1 LSB Differential Non-Linearity (Implies Monotonicity)

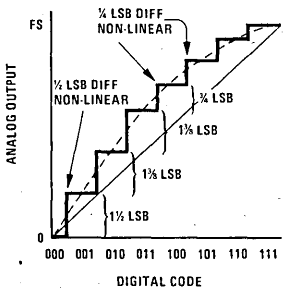


FIGURE 7. 1¼ LSB Non-Linear, ½ LSB Differential Non-Linearity

Linearity specs refer to either ADCs or to DACs, and do not include quantizing, gain, offset, or scale errors. Linearity errors are of prime importance along with differential linearity in either ADC or DAC specs, as all other errors (except quantizing, and temperature and long-term drifts) may be adjusted to zero. Linearity errors may be expressed in % FS or fractional LSB.

Differential Non-Linearity indicates the difference between actual analog voltage change and the ideal (1 LSB) voltage change at any code change of a DAC. For example, a DAC with a 1.5 LSB step at a code change would be said to exhibit ½ LSB differential non-linearity (see figures 6 and 7). Differential non-linearity may be expressed in fractional bits or in % FS.

Differential linearity specs are just as important as linearity specs because the apparent quality of a converter curve can be significantly affected by differential non-linearity even though the linearity spec is good. Figure 6 shows a curve with a ±½ LSB linearity and ±1 LSB differential non-linearity while figure 7 shows a curve with +1¼ LSB linearity and ±½ LSB differential non-linearity. In many user applications, the curve of figure 7 would be preferred over that of figure 6 because the curve is smoother. The differential non-linearity spec describes the smoothness of a curve; therefore it is of great importance to the user. A gross example of differential non-linearity is shown in figure 8 where the linearity spec is ±1 LSB and the differential linearity spec is ±2 LSB. The effect is to allow a transfer curve with grossly degraded resolution; the normal 8-step curve is reduced to 3 steps in figure 8. Similarly, a 16-step curve (4-bit converter) with only 2 LSB differential non-linearity could be reduced to 6 steps (a 2.6-bit converter?). The real message is, "Beware of the specs." Do not ignore or omit differential linearity characteristics on a converter unless the linearity spec is tight enough to guarantee the desired differential linearity. As this characteristic is impractical to measure on a production basis, it is rarely, if ever, specified, and linearity is the primary specified parameter. Differential non-linearity can always be as much as twice the non-linearity, but no more.

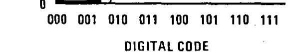


FIGURE 8. ±1 LSB Linear, ±2 LSB Differential Non-Linear

Monotonicity. A monotonic curve has no change in sign of the slope; thus all incremental elements of a monotonically increasing curve will have positive or zero, but never negative slope. The converse is true for decreasing curves. The transfer curve of a monotonic DAC will contain steps of only positive or zero height, and no negative steps. Thus a smooth line connecting all output voltage points will contain no peaks or dips. The transfer function of a monotonic ADC will provide no decreasing output code for increasing input voltage.

Figure 9 shows a non-monotonic DAC transfer curve. For the curve to be non-monotonic, the linearity error must exceed ±½ LSB no matter by how little. The greater the linearity error, the more significant the negative step might be. A non-monotonic curve may not be a special disadvantage in some systems; however, it is a disaster in closed-loop servo systems of any type (including a DAC-controlled ADC). A ±½ LSB maximum linearity spec on an n-bit converter guarantees monotonicity to n bits. A converter exhibiting more than ±½ LSB non-linearity may be monotonic, but is not necessarily monotonic. For example, a 12-bit DAC with ±½ bit linearity to 10 bits (not ±½ LSB) will be monotonic at 10 bits but may or may not be monotonic at 12 bits unless tested and guaranteed to be 12-bit monotonic.

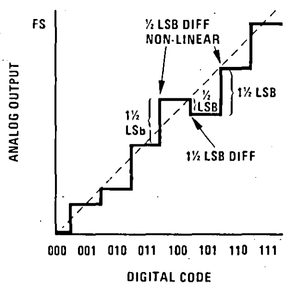
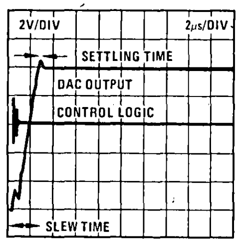
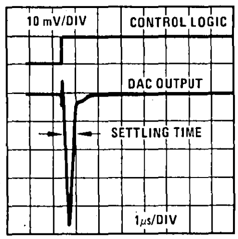


FIGURE 9. Non-Monotonic (Must be > ±½ LSB Non-Linear)



(a) Full-Scale Step



(b) 1 LSB Step

FIGURE 10. DAC Slew and Settling Time

Settling Time is the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±½ LSB. (See also **Conversion Rate** below.) Settling time is often listed along with a slew rate specification; if so, it may not include slew time. If no slew rate spec is included, the settling time spec must be expected to include slew time. Settling time is usually summed with slew time to obtain total elapsed time for the output to settle to final value. Figure 10 delineates that part of the total elapsed time which is considered to be slew and that part which is settling time. It is apparent from this figure that the total time is greater for a major than for a minor code change due to amplifier slew limitations, but settling time may also be different depending upon amplifier overload recovery characteristics.

Slew Rate is an inherent limitation of the output amplifier in a DAC which limits the rate of change of output voltage after code transitions. Slew rate is usually anywhere from 0.2 to several hundred volts/μs. Delay in reaching final value of DAC output voltage is the sum of slew time and settling time as shown in figure 10.

Overshoot and Glitches occur whenever a code transition occurs in a DAC. There are two causes. The current output of a DAC contains switching glitches due to possible asynchronous switching of the bit currents (expected to be worst at half-scale transition when all bits are switched). These glitches are normally of extremely short duration but could be of ½ scale amplitude. The current switching glitches are generally somewhat attenuated at the voltage output of the DAC because the output amplifier is unable to slew at a very high rate; they are, however, partially coupled around the amplifier via the amplifier feedback network and seen at the output. The output amplifier introduces overshoot and some non-critically damped ringing which may be minimized but not entirely eliminated except at the expense of slew rate and settling time.

Temperature Coefficient of the various components of a DAC or ADC can produce or increase any of the several errors as the operating temperature varies. Zero scale offset error can change due to the TC of the amplifier and comparator input offset voltages and currents. Scale error can occur due to shifts in the reference, changes in ladder resistance or non-compensating RC product shifts in dual-slope ADCs, changes in beta or reference current in current switches, changes in amplifier bias current, or drift in amplifier gain-set resistors. Linearity and monotonicity of the DAC can be affected by differential temperature drifts of the ladder resistors and switches. Overshoot, settling time, and slew rate can be affected by temperature due to internal change in amplifier gain and bandwidth. In short, every specification except resolution and quantizing error can be affected by temperature changes.

Long-Term Drift, due mainly to resistor and semiconductor aging can affect all those characteristics which temperature change can affect. Characteristics most commonly affected are linearity, monotonicity, scale, and offset. Scale change due to reference aging is usually the most important change.

Supply Rejection relates to the ability of a DAC or ADC to maintain scale, offset, TC, slew rate, and linearity when the supply voltage is varied. The reference must, of course, remain constant unless considering a multiplying DAC. Most affected are current sources (affecting linearity and scale) and amplifiers or comparators (affecting offset and slew rate). Supply rejection is usually specified only as a % FS change at or near full scale at 25°C.

Conversion Rate is the speed at which an ADC or DAC can make repetitive data conversions. It is affected by propagation delay in counting circuits, ladder switches and comparators; ladder RC and amplifier settling times; amplifier and comparator slew rates; and integrating time of dual-slope converters. Conversion rate is specified as a number of conversions per second, or conversion time is specified as a number of microseconds to complete one conversion (including the effects of settling time). Sometimes, conversion rate is specified for less than full resolution, thus showing a misleading (high) rate.

Clock Rate is the minimum or maximum pulse rate at which ADC counters may be driven. There is a fixed relationship between the minimum conversion rate and the clock rate depending upon the converter accuracy and type. All factors which affect conversion rate of an ADC limit the clock rate.

Input Impedance of an ADC describes the load placed on the analog source.

Output Drive Capability describes the digital load driving capability of an ADC or the analog load driving capacity of a DAC; it is usually given as a current level or a voltage output into a given load.

CODES

Several types of DAC input or ADC output codes are in common use. Each has its advantages depending upon the system interfacing the converter. Most codes are binary in form; each is described and compared below.

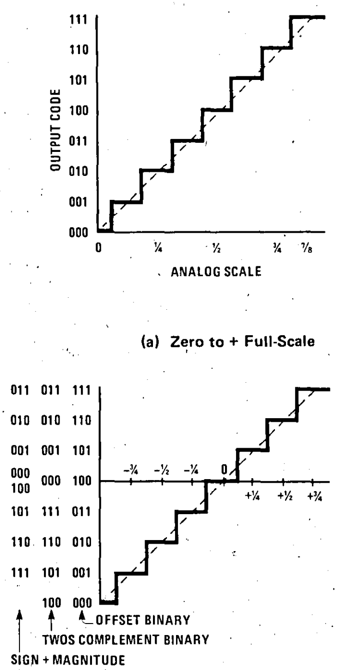
Natural Binary (or simply Binary) is the usual 2^n code with 2, 4, 8, 16, . . . , 2^n progression. An input or output high or "1" is considered a signal, whereas a "0" is considered an absence of signal. This is a positive true binary signal. Zero scale is then all "zeros" while full scale is all "ones."

Complementary Binary, (or Inverted Binary) is the negative true binary system. It is identical to the binary code except that all binary bits are inverted. Thus, zero scale is all "ones" while full scale is all "zeros."

Binary Coded Decimal (BCD) is the representation of decimal numbers in binary form. It is useful in ADC systems intended to drive decimal displays. Its advantage over decimal is that only 4 lines are needed to represent 10 digits. The disadvantage of coding DACs or ADCs in BCD is that a full 4 bits could represent 16 digits while only 10 are represented in BCD. The full-scale resolution of a BCD coded system is less than that of a binary coded system. For example, a 12-bit BCD system has a resolution of only 1 part in 1000 compared to 1 part in 4096 for a binary system. This represents a loss in resolution of over 4:1.

Offset Binary is a natural binary code except that it is offset (usually ½ scale) in order to represent negative and positive values. Maximum negative scale is represented to be all "zeros" while maximum positive scale is represented as all "ones." Zero scale (actually center scale) is then represented as a leading "one" and all remaining "zeros." The comparison with binary is shown in figure 11.

Twos Complement Binary is an alternate and more widely used code to represent negative values. With this code, zero and positive values are represented as in natural binary while all negative values are represented in a twos complement form. That is, the twos complement of a number represents a negative value so that interface to a computer or microprocessor is simplified. The twos complement is formed by complementing each bit and then adding a 1; any overflow is neglected. The decimal number −8 is represented in twos complement as follows: start with binary code of decimal 8 (off scale for ± representation in 4 bits so not a valid code in the ± scale of 4 bits) which is 1000; complement it to 0111; add 0001 to get 1000. The comparison with offset binary is shown in figure 11. Note that the offset binary representation of the ± scale differs from the twos complement representation only in that the MSB is complemented. The conversion from offset binary to twos complement only requires that the MSB be inverted.



(b) ± Full-Scale

FIGURE 11. ADC Codes

Sign Plus Magnitude coding contains polarity information in the MSB (MSB = 1 indicates a negative sign); all other bits represent magnitude only. This code is compared to offset binary and twos complement in figure 11. Note that one code is used up in providing a double code for zero. Sign plus magnitude code is used in certain instrument and audio systems; its advantage is that only one bit need be changed for small scale changes in the vicinity of zero, and plus and minus scales are symmetrical. A DVM might be an example of its use.

CONTROL

Each ADC must accept and/or provide digital control signals telling it and/or the external system what to do and when to do it. Control signals should be compatible with one or more types of logic in common use. Control signal timing must be such that the converter or connected system will accept the signals. Common control signals are listed below.

Start Conversion (SC) is a digital signal to an ADC which initiates a single conversion cycle. Typically, an SC signal must be present at the fall (or rise) of the clock waveform to initiate the cycle. A DAC needs no SC signal; however, such could be provided to gate digital inputs to a DAC.

End of Conversion (EOC) is a digital signal from an ADC which informs the external system that the digital output data is valid. Typically, an EOC output can be connected to an SC input to cause the ADC to operate in continuous conversion mode. In non-continuous conversion systems, the SC signal is a command from the system to the ADC. A DAC does not supply an EOC signal.

Clock signals are required or must be generated within an ADC to control counting or successive approximation registers. The clock controls the conversion speed within the limitations of the ADC. DACs do not require clock signals.

CONCLUSION

Once the user has a working knowledge of DAC or ADC characteristics and specifications, he should be able to select a converter to suit a specific system need. The likelihood of overspecification, and therefore an unnecessarily high cost, is likewise reduced. The user will also be aware that specific parameters, test conditions, test circuits, and even definitions may vary from manufacturer to manufacturer. For practical production reasons, parameters may not be tested in the same manner for all converter types, even those supplied by the same manufacturer. Using information in this note, the user should, however, be able to sort out and understand those specifications (from any manufacturer) pertinent to his needs.

SECTION 6
COMMUNICATIONS/CB RADIO CIRCUITS

Communications/CB Radio Circuits

MM5303 universal fully asynchronous receiver/transmitter

general description

The MM5303 is a fully asynchronous receiver/transmitter, fabricated with National's metal-gate, depletion load, PMOS technology. All inputs and outputs are fully TTL compatible, requiring no external resistors or level shifting.

This device is a programmable interface between an asynchronous serial data channel and a parallel data channel. The transmitter section converts parallel data into a serial word which includes: start bit, data, parity bit (if selected), and stop bit(s). The receiver converts a serial word of the same format into a parallel one and automatically checks start bit, parity (if selected), and stop bit(s).

Both transmitter and receiver are doubly buffered; in addition, received data out and status words may be TRI-STATED, facilitating bus configurations.

Status conditions are: transmission complete, Tx buffer register empty, Rx data available, parity error, framing error, and over-run error.

The MM5303 is fully programmable. It can operate full or half duplex, transmitting and receiving simultaneously at different baud rates; word length may be 5, 6, 7 or 8 bits; parity generation/checking may be even, odd or inhibited; the number of stop bits may be either 1 or 2, with 1 1/2 bits when transmitting a 5 bit code.

features

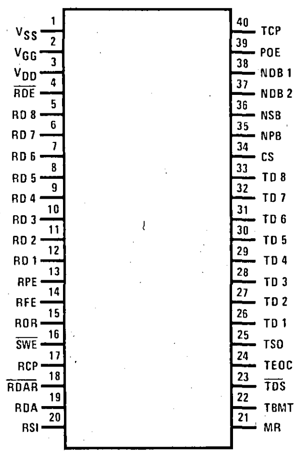
- Low power
- High speed
- Fully externally programmable:
  - Word length
  - Parity mode
  - Number of stop bits
- Fully double buffered eliminating need for precise synchronization
- Full or half duplex operation
- Direct TTL/DTL compatibility
- Automatic data received/transmitted status generation
- TRI-STATE outputs
- Automatic start bit generation/verification
- Internal pull-ups on all inputs

applications

- Peripherals
- Terminals
- Mini computers
- Facsimile transmission
- Modems
- Concentrators
- Asynchronous data multiplexers
- Card and tape readers
- Printers
- Data sets
- Controllers
- Keyboard encoders
- Remote data acquisition systems
- Asynchronous data cassettes

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5303N
See Package 24

absolute maximum ratings (Note 1)

Voltage at Any Pin	$V_{SS} - 25V/V_{SS} + 0.3V$*
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Outputs should not have more than $V_{SS} - 15V$

dc electrical characteristics

T_A within operating temperature range, V_{SS} = 5V ±5%, V_{DD} = 0V, V_{GG} = −12V ±5% unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Input Voltage Levels	(Note 3)	$V_{SS}-1.5$		$V_{SS}+0.3$	V
V_{IL}	Low Input Voltage Levels		V_{DD}		0.8	V
V_{OH}	High Output Voltage Levels	I_{OH} = −100µA	2.4			V
V_{OL}	Low Output Voltage Levels	I_{OL} = 1.6 mA			0.4	V
I_{IH}	High Level Input Current Levels	$V_{IN} = V_{SS}$			10	µA
I_{IL}	Low Level Input Current Levels	V_{IN} = 0.4V, V_{SS} = 5.25V			1.6	mA
I_{OL}	Output Leakage Current Level	$\overline{SWE} = \overline{RDE} = V_{IH}$, $0 \leq V_{OUT} \leq 5V$			−1	µA
I_{OS}	Output Short Circuit Current Level	V_{OUT} = 0V, (Note 4)			25	mA
C_{IN}	Input Capacitance	(Note 2)				
	All Inputs	$V_{IN} = V_{SS}$, f = 1 MHz		5	10	pF
C_{OUT}	Output Capacitance					
	All Outputs	$\overline{SWE} = \overline{RDE} = V_{IH}$, f = 1 MHz		10	20	pF
I_{SS}	Power Supply Current	All Inputs at V_{SS}		13	25	mA
I_{GG}	Power Supply Current	All Inputs at V_{SS}		6	15	mA

ac electrical characteristics at 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Clock Frequency	RCP, TCP	dc		500	kHz
t_{PW}	Pulse Width					
	Clock	RCP, TCP	1			µs
	Master Reset	MR	5			µs
	Control Strobe	CS	1			µs
	Tx Data Strobe	$\overline{TDS}$	300			ns
	Rx Data Available Reset	$\overline{RDAR}$, (Note 5)	200			ns
t_C	Coincidence Time	$\overline{TDS}$	300			ns
		CS	1			µs
t_{SET}	Input Set-Up Time	TD1−TD8	0			ns
		NPB, NSB, NDB, POE	0			ns
t_{HOLD}	Input Hold Time	TD1−TD8	300			ns
		NPB, NSB, NDB, POE	0			ns
t_{pd0}	Output Propagation Delay to Low State	$\overline{RDE}$, $\overline{SWE}$ Enable to Outputs Low			500	ns
t_{pd1}	Output Propagation Delay to High State	$\overline{RDE}$, $\overline{SWE}$ Enable to Outputs High			500	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

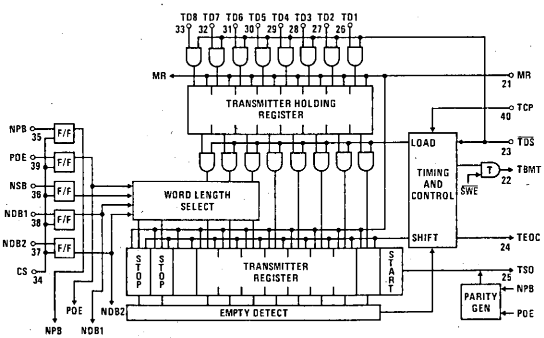
Note 2: Capacitance is guaranteed by periodic testing.

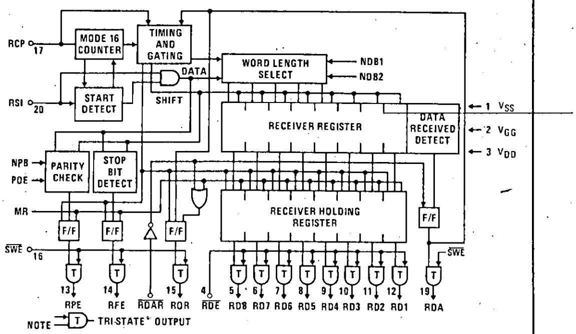
Note 3: Positive true logic notation is used:
Logic "1" = most positive voltage level
Logic "0" = most negative voltage level

Note 4: Only one output should be shorted at a time.

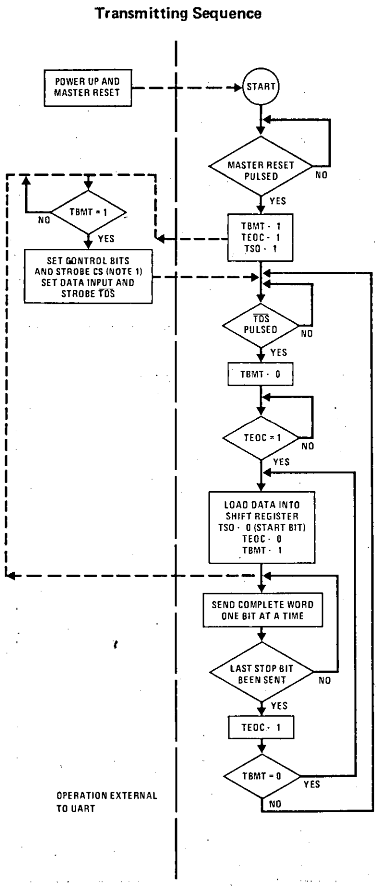
Note 5: Refer to Receiver Timing diagram for detail.

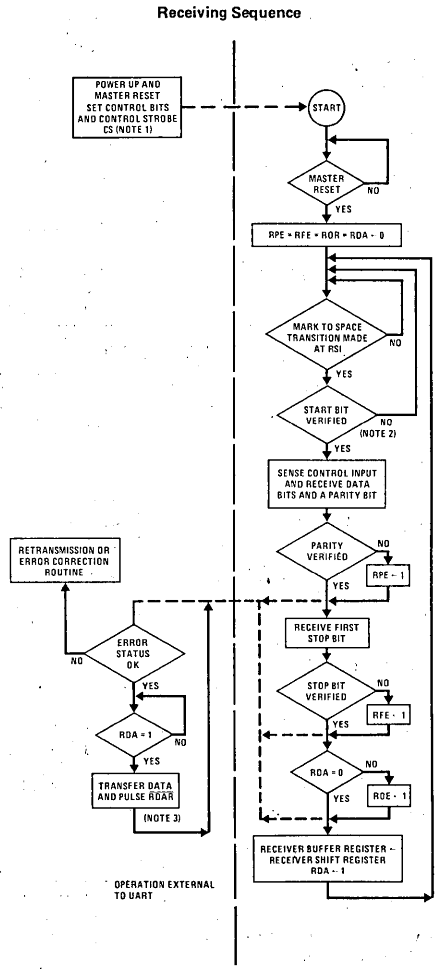
functional block diagrams





flow charts





Note 1: Control Strobe should be made only at the beginning of transmission and remain inactive during transmission. It may be tied high if no change is necessary.

Note 2: The line must stay low for 8 RCP pulses to be verified.

Note 3: $\overline{\text{RDAR}} \leftarrow 0$ will cause RDA $\leftarrow 0$, refer to receiver timing for detail.

pin functions

PIN NO.	SYMBOL	NAME	FUNCTION
1	V_{SS}	Power Supply	+5V supply
2	V_{GG}	Power Supply	−12V supply
3	V_{DD}	Ground	Ground
4	$\overline{RDE}$	Received Data Enable	A low-level input enables the outputs (RD8–RD1) of the receiver buffer register.
5–12	RD8–RD1	Receiver Data Outputs	These are the 8 TRI-STATE data outputs enabled by $\overline{RDE}$. Unused data output lines, as selected by NDB1 and NDB2, have a low-level output, and received characters are right justified, i.e., the LSB always appears on the RD1 output.
13	RPE	Receiver Parity Error Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level if the received character parity bit does not agree with the selected parity.
14	RFE	Receiver Framing Error Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level if the received character has no valid stop bit.
15	ROR	Receiver Over Run Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level if the previously received character is not read (RDA output not reset) before the present character is transferred into the receiver buffer register.
16	$\overline{SWE}$	Status Word Enable Input	A low-level input enables the outputs (RPE, RFE, ROR, RDA, and TBMT) of the status word buffer register.
17	RCP	Receiver Clock	This input is a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	$\overline{RDAR}$	Receiver Data Available Reset Input	A low-level input resets the RDA output to a low-level.
19	RDA	Receiver Data Available Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level when an entire character has been received and transferred into the receiver buffer register.
20	RSI	Receiver Serial Input	This input accepts the serial bit input stream. A high-level (mark) to low-level (space) transition is required to initiate data reception.
21	MR	Master Reset	This input should be pulsed to a high-level after power turn-on. This sets TSO, TEOC, and TBMT to a high-level and resets RDA, RPE, RFE and ROR to a low-level.
22	TBMT	Transmitter Buffer Empty Output	This TRI-STATE output (enabled by $\overline{SWE}$) is at a high-level when the transmitter buffer register is empty and may be loaded with new data.
23	$\overline{TDS}$	Transmitter Data Strobe Input	A low-level input strobe enters the data bits into the transmitter buffer register.
24	TEOC	Transmitter End of Character Output	This output appears as a high-level each time a full character is transmitted. It remains at this level until the start of transmission of the next character or for one full TCP period in the case of continuous transmission.
25	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. TSO remains at a high-level when no data is being transmitted.
26–33	TD1–TD8	Transmitter Data Inputs	There are 8 data input lines (strobed by $\overline{TDS}$) available. Unused data input lines,as selected by NDB1 and NDB2, may be in either logic state. The LSB should always be placed on TD1.
34	CS	Control Strobe Input	A high-level input enters the control bits (NDB1, NDB2, NSB, POE and NPB) into the control bits holding register. This line may be strobed or hard wired to a high-level.
35	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted; the stop bit(s) immediately follow the last data bit. In addition, the receiver requires the stop bit(s) to follow immediately after the last data bit. Also, the RPE output is forced to a low-level. See pin 39, POE .
36	NSB	Number of Stop Bits	This input selects the number of stop bits, 1, 1 1/2, or 2 to be transmitted. A low-level input selects 1 stop bit; a high-level input selects 2 stop bits, except when 5-bit data is selected, then 1 1/2 stop bits will occur.

pin functions (con't)

PIN NO.	SYMBOL	NAME	FUNCTION
37–38	NDB2, NDB1	Number of Data Bits/ Character	These 2 inputs are internally decoded to select either 5, 6, 7 or 8 data bits/ character as per the following truth table:

NDB2	NDB1	data bits/character
L	L	5
L	H	6
H	L	7
H	H	8

PIN NO.	SYMBOL	NAME	FUNCTION
39	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following truth table:

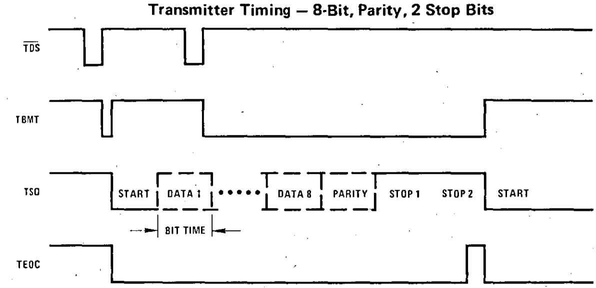
NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity

X = don't care

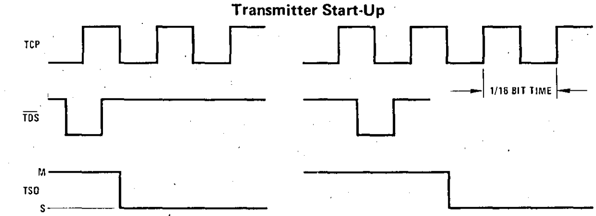
PIN NO.	SYMBOL	NAME	FUNCTION
40	TCP	Transmitter Clock	This input is a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

timing diagrams

Transmitter Timing — 8-Bit, Parity, 2 Stop Bits

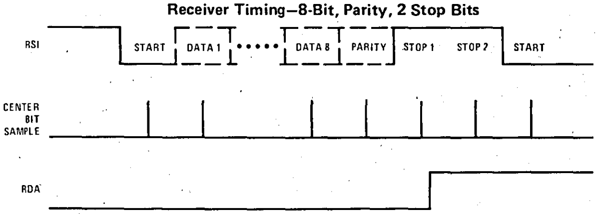


Transmitter Start-Up

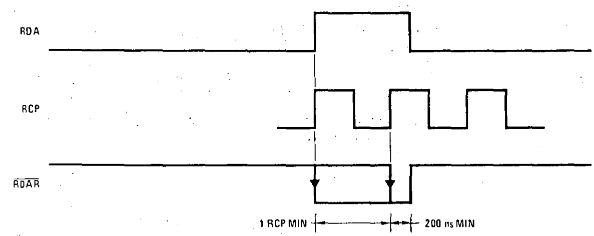


Upon data transmission initiation, or when not transmitting at 100% line utilization, the start bit will be placed on the TSO line at the high to low transition of the TCP clock following the trailing edge of $\overline{TDS}$.

Receiver Timing–8-Bit, Parity, 2 Stop Bits



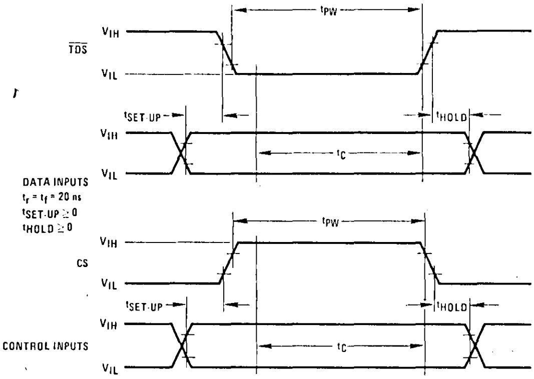
Resetting RDA



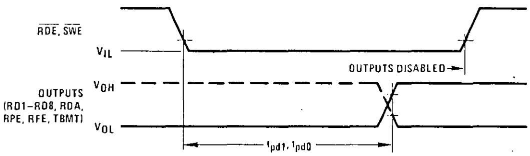
$\overline{RDAR}$ may go low any time after the RDA comes up but must stay low for at least 200 ns after the first clock pulse period. $\overline{RDAR}$ may be hard wired low, in which case RDA will go high and remain high for the duration of the positive clock pulse.

timing diagrams (con't)

Data/Control Timing Diagram

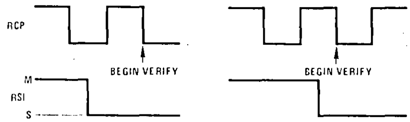


Output Timing Diagram



Note: Waveform drawings not to scale for clarity.

Start Bit Detect/Verify



If the RSI line remains spacing for 1/2 a bit time, a genuine start bit is verified. Should the line return to a marking condition prior to 1/2 a bit time, the start bit verification process begins again.

Communications/CB Radio Circuits

MM5393 push button telephone dialer

general description

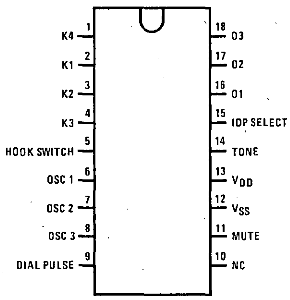
The MM5393 is a monolithic metal gate CMOS integrated circuit which provides all logic required to convert a push button input to a series of pulses suitable for simulating a telephone dial. Storage is provided for 21 digits, therefore, the information is retained after the call is completed and the number is available for redial. Entering a new number simply overrides the previous one. An interdigital pause can be externally selected as either 415 ms or 830 ms. A muting output is supplied to mute receiver noise during outpulsing, and a 600 Hz tone is activated every time a key is depressed.

features

- 21-digit storage
- Selectable interdigital pause
- Redial of last number
- 600 Hz tone
- Line powered operation

connection diagram

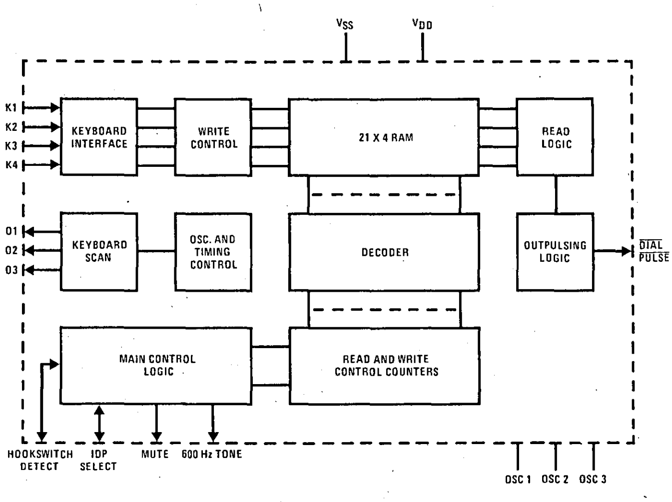
Dual-In-Line Package



TOP VIEW

Order Number MM5393N
See Package 20

block diagram



absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	−30°C to +65°C
Storage Temperature Range	−40°C to +70°C
$V_{DD} - V_{SS}$	6V max
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics T_A within operating temperature range, V_{SS} = Gnd, $2V \leq V_{DD} \leq 5.5V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Levels					
Logical "1"		V_{DD}−0.25		V_{DD}	V
Logical "0"		V_{SS}		V_{SS}+0.25	V
Output Current Levels					
Dial Pulse					
Logical "1"	$V_{DD} = 3V, V_{OUT} = V_{DD} - 0.5$	150			μA
Logical "0"	$V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5$	150			μA
Mute					
Logical "1"	$V_{DD} = 3V, V_{OUT} = V_{DD} - 0.5$	100			μA
Logical "0"	$V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5$	100			μA
Tone					
Logical "1"	$V_{DD} = 3V, V_{OUT} = V_{DD} - 0.5$	10			μA
Logical "0"	$V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5$	10			μA
01, 02, 03					
Logical "1"	$V_{DD} = 3V, V_{OUT} = V_{DD} - 0.5$	20			μA
Logical "0"	$V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5$	150			μA

functional description

The time base for the MM5393 is an RC controlled oscillator nominally tuned to 20 kHz. This is successively divided to provide timing signals for the various counters. The keyboard inputs, K1–K4, in conjunction with the scan counter outputs, 01–03, indicate the presence of a particular key depression. If only one key is detected for 5 ms, the decoded key will be loaded into the RAM. The push button inputs are accepted at an asynchronous rate, loaded into a first-in-first-out memory, and outpulsing of the correct number of pulses begins immediately after the first digit is entered. After the first digit has been completed, outpulsing will cease unless another key has been entered. This allows use in a PBX system to ensure receipt of a dial tone before entering the remainder of the number. If the call was not successful, it can be redialed at a later time by pressing the redial key (#). If an access code is required as in a PBX system, it can be entered, the dial tone can be established, then the redial key can be pushed. Only one key can be entered before pushing the redial key because after the second key entry, the memory is erased. A block diagram of the MM5393 is shown in *Figure 1*.

KEYPAD DATA INPUTS

Keypad closures cause the connection of 2 of 7 switch contacts arranged as a matrix (shown in *Figure 2*). Key closures are protected from contact bounce for 5 ms.

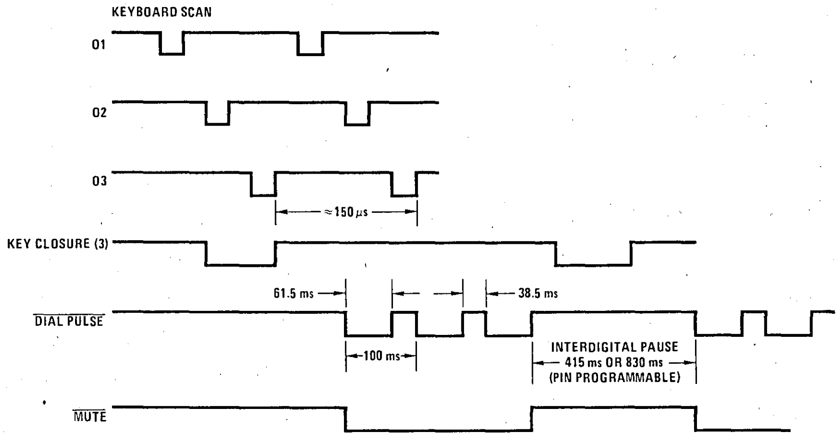
IMPULSING MARK-TO-SPACE RATIO

The mark-to-space ratio is 1.6:1 (61.5% to 38.5%).

IMPULSING OUTPUT

The number of pulses will correspond to the input digit. For example, key 5 will generate 5 pulses. The outpulsing rate is 10 Hz, and it can be varied by adjusting the frequency of the oscillator. Because it is intended to drive a transistor buffer, the outpulsing data is inverted. Digits are separated by an interdigital pause which is pin programmable for either 415 ms or 830 ms.

switching time waveforms



Note. All times are based on a 20 kHz oscillator.

FIGURE 1

keypad matrix

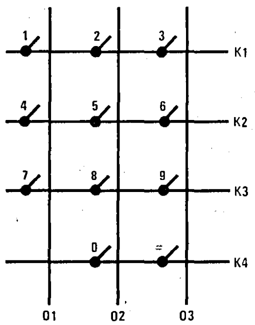


FIGURE 2

typical application

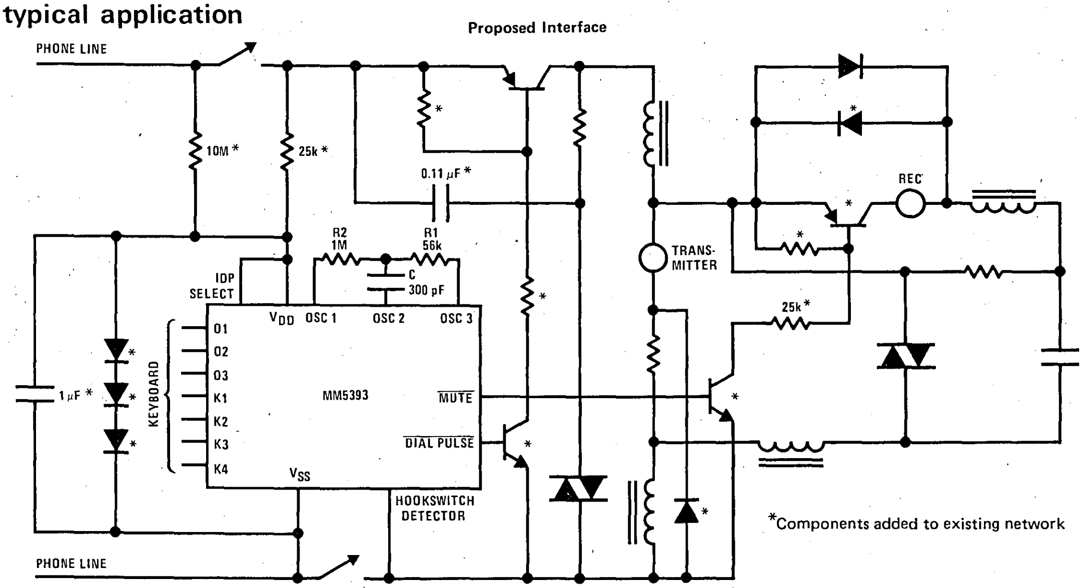


FIGURE 3

MM5395 TOUCH TONE® generator

general description

The MM5395 is an integrated circuit that can provide all tone frequency pairs required for the TOUCH TONE® telephone dialing system. The output frequencies are generated by programmably dividing the frequency of the on-chip crystal-controlled oscillator; thus, accurate output frequencies can be obtained without tuning. The only external component needed for the oscillator is an inexpensive 3.579545 MHz crystal.

The device has four row and four column inputs. Inputs to the device can either be in a 2-out-of-8 code format from a keyboard, or by BCD signals to the row inputs.

The device is fabricated using our low voltage CMOS process so that it may be powered directly from the telephone line.

The MM5395 is designed to be used in a wide variety of tone signaling and data transmission applications.

features

- 3V to 5V supply
- On-chip 3.579545 MHz crystal-controlled oscillator
- Interface with standard telephone keypad
- Interface with single contact low-cost keypad option
- Multi-key lockout with single tone capability
- On-chip high band and low band tone generators and mixer
- High band pre-emphasis
- Low harmonic distortion
- Accurate tone frequencies
- Open emitter, emitter follower output
- Mute switch output
- Can be powered directly from the telephone line

functional description

The functional block diagram of MM5395 is shown in *Figure 1*. The device can be operated in Keypad Interface Mode or Signal Interface Mode (BCD into row input) depending on the logical level at "Control" input. In either mode, the MM5395 will digitally synthesize the high and/or low band sine waves when valid signals are applied to row or column inputs. The sum of the two sine waves is then provided at the "Tone Output." The base of the output NPN transistor is brought out ("FILTER") for easy filtering. Operational functional features are summarized in tables.

block diagram

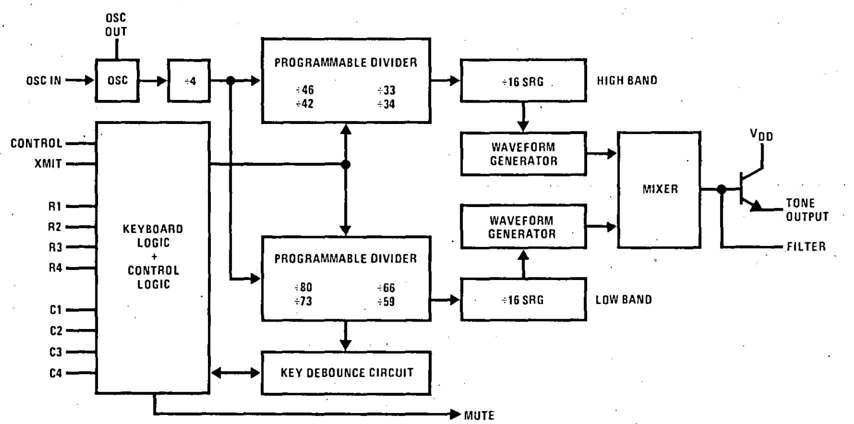


FIGURE 1

absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−65°C to +150°C
$V_{DD} - V_{SS}$	6V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature, $3V \leq V_{DD} - V_{SS} \leq 5V$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pull-Up Resistor @ Column Inputs	$V_{IN} = V_{SS}$	100		400	kΩ
Input Pull-Down Resistor @ "Xmit"	$V_{IN} = V_{DD}$	100		400	kΩ
Internal Resistor @ Row Inputs					
To V_{DD} (Option A)	$V_{IN} = V_{SS}$	100		400	kΩ
To V_{SS} (Option B)	$V_{IN} = V_{DD}$	100		400	kΩ
Input Voltage Levels					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Output Voltage Swings @ "TONE OUTPUT"	$V_{DD} - V_{SS} = 3.0V$, $R_L > 500\Omega$				
Low Band Only			820		mVp-p
High Band Only			1000		mVp-p
Harmonic Distortion	$R_L \geq 500\Omega$, No External Filtering			−20	dB
Tone Frequency Deviation				1.0	%
Operating Frequency			3.579545		MHz
Key-Down Debounce Time			7	11.35	ms
Key-Up Debounce Time			4	7.15	ms
Power Dissipation	$V_{DD} - V_{SS} = 6V$, $R_L = 500\Omega$			30	mW
Output Current Level @ "MUTE"	$V_{DD} - V_{SS} = 3.0V$				
Logical "1"	$V_{OUT} = V_{DD} - 0.2V$	20			µA
Logical "0"	$V_{OUT} = V_{SS} + 0.5V$	2.0			mA

functional description (Continued)

TABLE I. Interface Mode Control

CONTROL	XMIT	INTERFACE MODE	
0	Open	Keypad	
1	0	Idle	BCD Signal
1	1	Send tones	e.g. MM5393

functional description (Continued)

TABLE II. Keypad Interface
(a). Functional Truth Table

ROW	COLUMN	LOW BAND	HIGH BAND
None	None	DC	DC
One	One	f_L	f_H
None	One	DC	f_H
One	None	f_L	DC
Two or more	None	DC	DC
Two or more	One	DC	f_H
None	Two or more	DC	DC
One	Two or more	f_L	DC

(b). Output Frequencies

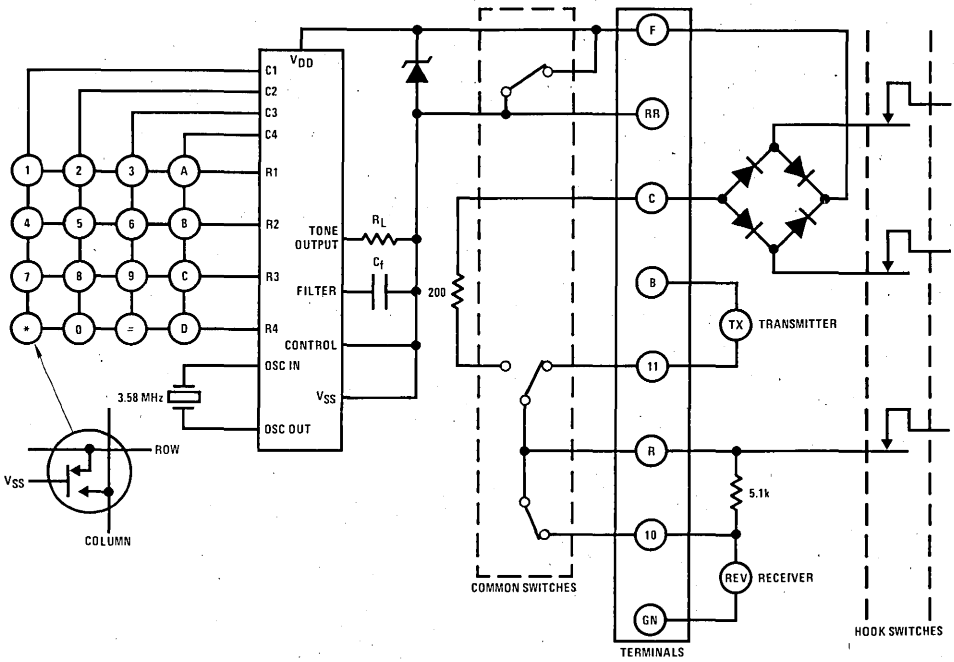
INPUTS	DESIRED FREQUENCIES		ACTUAL FREQUENCY (Hz)	PERCENT DEVIATION
	f_L (Hz)	f_H (Hz)		
R1	697	–	699.1	0.306
R2	770	–	766.2	−0.497
R3	852	–	847.4	−0.536
R4	941	–	948.0	0.741
C1	–	1209	1215.9	0.569
C2	–	1336	1331.7	−0.324
C3	–	1477	1471.9	−0.35
C4	–	1633	1645.0	0.736

TABLE III. Functional Truth Table for Signal Interface

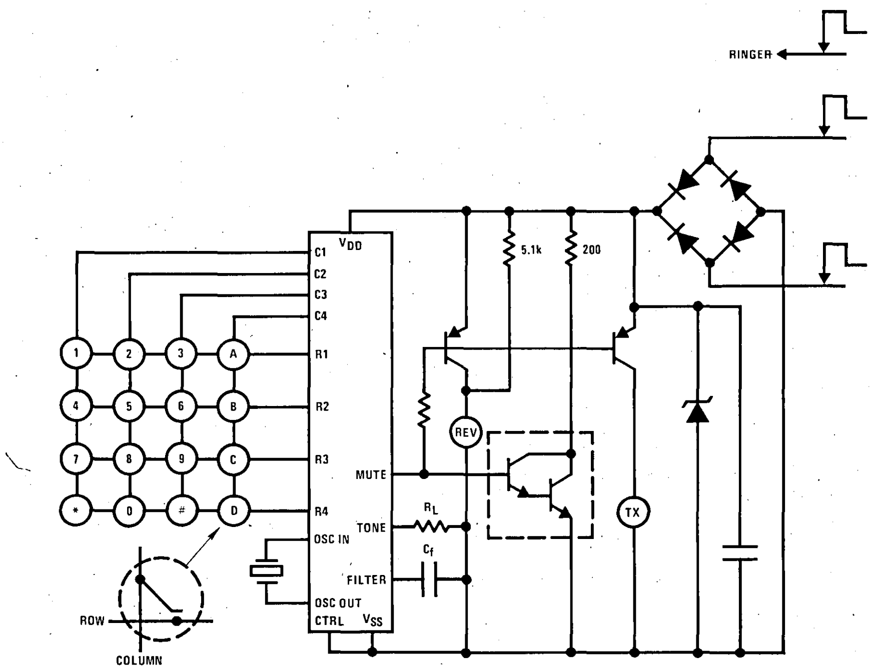
XMIT	C1	C2	R1	R2	R3	R4	FREQUENCIES GENERATED	
							f_L (Hz)	f_H (Hz)
0	X	X	X	X	X	X	DC	DC
1	Open	Open	0	0	0	0	941	1336
1	Open	Open	0	0	0	1	697	1209
1	Open	Open	0	0	1	0	697	1336
1	Open	Open	0	0	1	1	697	1477
1	Open	Open	0	1	0	0	770	1209
1	Open	Open	0	1	0	1	770	1336
1	Open	Open	0	1	1	0	770	1477
1	Open	Open	0	1	1	1	852	1209
1	Open	Open	1	0	0	0	852	1336
1	Open	Open	1	0	0	1	852	1477
1	0	Open	Valid BCD Inputs				f_L	DC
1	Open	0					DC	f_H
1	0	0					DC	DC

typical applications

Standard Telephone Keypad

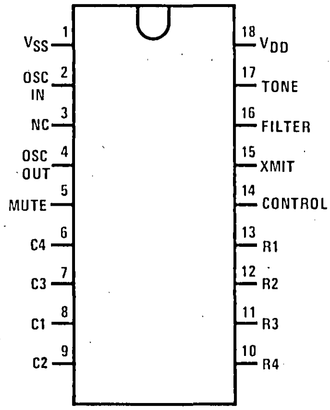


Single Contact Keypad



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5395N
See Package 20

Communications/CB Radio Circuits

MM55104, MM55106, MM55114, MM55116 PLL frequency synthesizer

general description

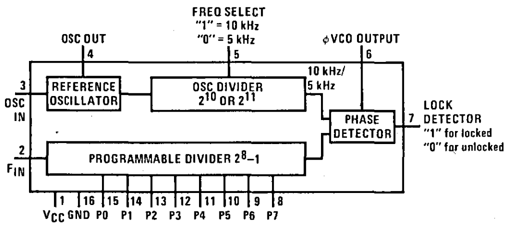
The MM55104 and MM55106 devices contain phase locked loop circuits useful for frequency synthesizer applications in C.B. transceivers. The devices operate off a single power supply and contain an oscillator, a 2^{10} or 2^{11} divider chain, a binary input programmable divider, and phase detector circuitry. The devices may be used in double I.F. or single I.F. systems. The MM55104, MM55114, MM55106 and MM55116, use a 10.24 MHz or 5.12 MHz quartz crystal to determine the reference frequency. The MM55106 and MM55116 have an output pin which provides a 5.12 MHz signal, which may be tripled for use as a reference oscillator frequency in two crystal systems. Also, the MM55106 provides an additional input to the programmable divider which allows $2^9 - 1$ division of the input frequency (F_{IN}). The inputs to the programmable divider are standard binary signals. Selection of a channel is accomplished by mechanical switches or by external electronic programming of the programmable divider.

The ϕVCO output provides a high level voltage (sources current) when the VCO frequency is lower than the lock frequency, and ϕVCO provides a low level voltage (sinks current) when the VCO frequency is higher than the lock frequency. The ϕVCO output goes to a high impedance (TRI-STATE®) condition under lock conditions, and the lock detector output LD goes to a high state under lock conditions.

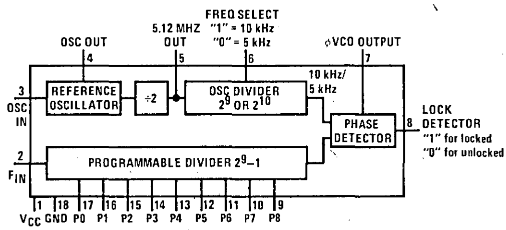
features

- Single power supply
- Low power CMOS technology
- Binary input channel select code
- 5 kHz or 10 kHz output from oscillator divide
- 5.12 MHz output (MM55106 and MM55116 only)
- On-chip oscillator
- Pull-down resistors on programmable divider inputs
- Low voltage operation—5V (MM55104, MM55106)
- High voltage operation—8V (MM55114, MM55116)

block diagrams



MM55104, MM55114



MM55106, MM55116

pin descriptions

P0–P8	Programmable divider inputs
F_{IN}	Frequency input from VCO (mixed down)
OSC IN	Oscillator amplifier input terminal
OSC OUT	Oscillator amplifier output terminal
LD	Lock detector
ϕVCO	Output of phase detector for control of the VCO
FS	Frequency division select 10 kHz or 5 kHz – "1" is 10 kHz; "0" is 5 kHz
5.12 MHz OUT	OSC Frequency divided by 2 output

truth table

Truth table for binary inputs to programmable divider.

N	P8	P7	P6	P5	P4	P3	P2	P1	P0
1	0	0	0	0	0	0	0	0	X
2	0	0	0	0	0	0	0	1	0
	.			.					
	.								
511	1	1	1	1	1	1	1	1	1

$F_{OUT} = F_{IN}/N$

1 = High voltage level, V_{OH}

0 = Low voltage level, V_{OL}

X = Don't care

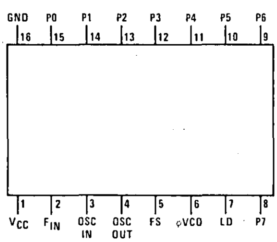
absolute maximum ratings

Voltage at Any Pin	V_{CC} + 0.3V to Gnd − 0.3V
Operating Temperature Range	−30°C to +75°C
Storage Temperature Range	−40°C to +125°C
V_{CC} Max	
MM55104, MM55106	7V
MM55114, MM55116	12V
Lead Temperature (Soldering, 10 seconds)	300°C

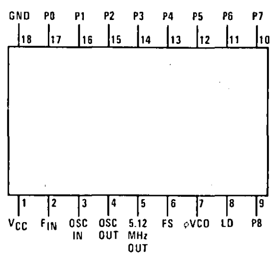
electrical characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})					
MM55104, MM55106		4.5	5.0	5.5	V
MM55114, MM55116		7.0	8.0	10.0	V
Supply Current (I_{CC})	Freq @ Osc In = 10 MHz, @ F_{IN} = 2.5 MHz, All Other I/O Pins Open, (Note 1)				
MM55104, MM55106	V_{CC} = 5V		3	10	mA
MM55114, MM55116	V_{CC} = 8V		8	16	mA
Logical "1" Input Voltage ($V_{IN(1)}$)					
P0–P8, FS, F_{IN}		(V_{CC}–0.4V)			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
P0–P8, FS, F_{IN}				0.4	V
Logical "1" Output Voltage					
5.12 MHz Out, LD	I_O = 0.5 mA				
φVCO	I_O = 0.4mA	(V_{CC}–0.5V)			V
Osc Out	I_O = 0.25mA				
Logical "0" Output Voltage					
φVCO, 5.12 MHz Out, LD	I_O = −0.5mA			0.5	V
Osc Out	I_O = −0.25mA				
Logical "1" Input Current					
FS (Pull-Up)				1.0	μA
MM55104, MM55106 } P0–P8 (Pull-Down)	V_{CC} = 5V	5	20	50	μA
MM55114, MM55116 } P0–P8 (Pull-Down)	V_{CC} = 8V	10	40	100	μA
Logical "0" Input Current					
P0–P8 (Pull-Down)				1.0	μA
MM55104, MM55106 } FS (Pull-Up)	V_{CC} = 5V	−10	−35	−100	μA
MM55114, MM55116 } FS (Pull-Up)	V_{CC} = 8V	−30	−120	−300	μA
Toggle Frequency @ F_{IN}		3			MHz
Oscillator Frequency @ Osc In		10.24			MHz
TRI-STATE Leakage @ φVCO				1.0	μA

connection diagrams (Dual-In-Line Packages, Top View)



Order Number MM55104N or MM55114N
See Package 19



Order Number MM55106N or MM55116N
See Package 20

typical applications

INTRODUCTION TO FREQUENCY SYNTHESIS

The components of a frequency synthesizer are shown in *Figure 1*. The voltage controlled oscillator produces the desired output frequencies spaced f_V Hz apart according to the relation:

$$f_V = f_r N$$

The reference frequency, fr, must be equal to or less than the (channel) spacing between the frequencies being synthesized.

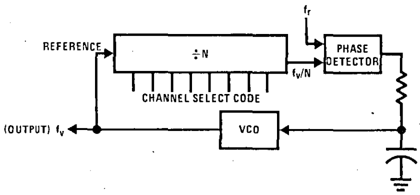


FIGURE 1. Basic Frequency Synthesizer

Although simple in concept, the circuit of *Figure 1* has certain difficulties. In CB, we are synthesizing the following frequencies:

Ch 1	26.965
Ch 2	26.975
.	.
.	.
.	.
Ch 23	27.225

Although the channel spacing is 10 kHz, a reference frequency of 5 kHz would be necessary due to the odd 5 kHz in the assigned channel. This in itself poses no problem; however, present technology limits the counting speed of programmable dividers to something less than 5 MHz, ruling out the approach shown in *Figure 1*.

Two solutions to this problem are shown in *Figure 2*.

Frequency prescaling shown in *Figure 2(a)* reduces the VCO frequency by M (a fixed number) to a frequency that can be divided by the programmable counter. The reference frequency f_r must also be reduced by M. In the case of CB, if M = 10, f_V = 26.965 MHz, the input to the programmable divider will be 2.6965 MHz, and the 5 kHz reference frequency will be reduced to 500 Hz. This poses problems in speed of response of the phase locked loop.

The second technique mixes the output frequency of the VCO with a stable fixed frequency to obtain a related reference frequency.

$$f_V = Nf_r + f_o$$

This technique has the advantage of allowing a 10 kHz reference frequency in the loop instead of 5 kHz.

Further complexity arises when one considers that the synthesizer must also generate a local oscillator signal as well as a transmitter input signal for the radio *(Figure 3)*. A system which provides these frequencies, as well as the proper offset to allow the programmable divider to operate within its limits is shown in the typical applications diagrams *(Figure 4)*. The only departure from the ideal situation shown in *Figure 3* is that the first IF frequency of 10.7 MHz must be changed to 10.695 MHz (a change of 5 kHz).

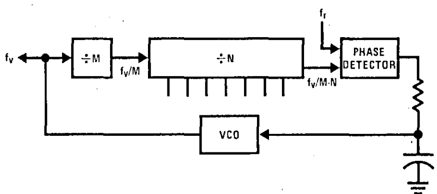


FIGURE 2(a). Frequency Prescaling

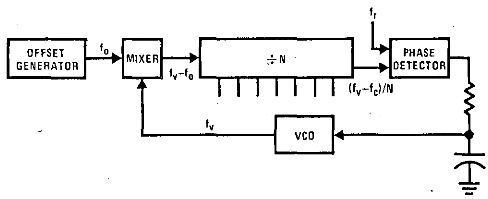


FIGURE 2(b). Frequency Offset

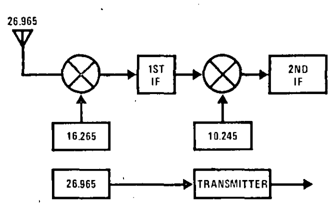


FIGURE 3. Signals Needed to Transmit and Receive Ch 1

typical applications (con't)

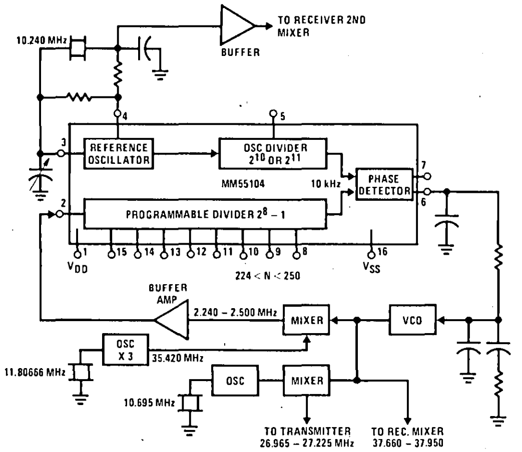


FIGURE 4(a). MM55104 or MM55114 3-Crystal Application

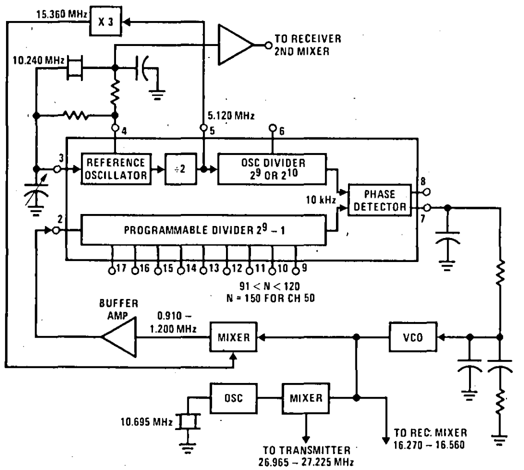


FIGURE 4(b). MM55106 or MM55116 2-Crystal, 23-Channel Application

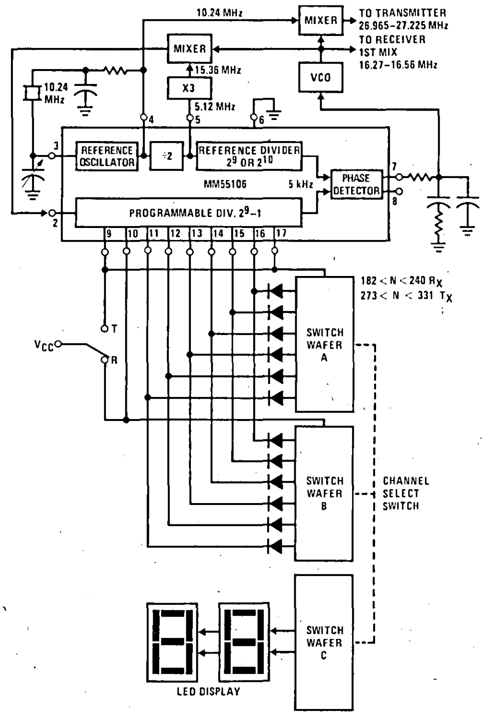


FIGURE 4(c). MM55106 or MM55116 Single Crystal, 23-Channel Application

Communications/CB Radio Circuits

MM55108, MM55110 PLL frequency synthesizer with receive/transmit mode

general description

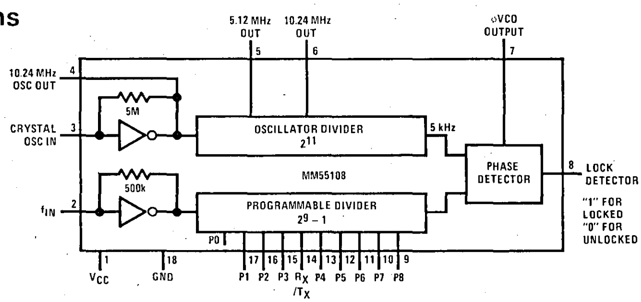
The MM55108 and MM55110 PLL frequency synthesizers are monolithic metal gate CMOS integrated circuits which contain phase lock loop circuits useful for frequency synthesis applications in CB transceivers. The devices operate from a single power supply and contain an oscillator with feedback resistor, divider chain, a binary input programmable divider with control logic for the transmit mode (÷ by (N + 91)), and the necessary phase detector logic. The devices may be used in double IF or single IF systems.

Both the MM55108 and the MM55110 use a 10.24 MHz quartz crystal to determine the reference frequency. The MM55108 has a 2^{11} divider chain which generates a 5 kHz reference frequency. The MM55110 has a selectable 2^{10} or 2^{11} divider chain which gives either a 10 kHz or 5 kHz reference frequency. The selection of reference frequency is made by use of the FS pin. In addition, the MM55110 contains an amplifier for filter applications and an additional input to the programmable divider which allows $2^{10} - 1$ division of the input frequency (f_{IN}) for FM applications. Due to the internal amplifier stage at input frequency input (f_{IN}), the MM55108 and MM55110 may take a 1 Vp-p signal at f_{IN} as the input frequency for the programmable divider. Inputs to the programmable divider are standard binary signals. Selection of a channel is accomplished by mechanical switches or by external electronic programming of the programmable divider. The ϕVCO output provides a high level voltage (sources current) when the ϕVCO frequency is lower than the lock frequency, and ϕVCO provides a low level voltage (sinks current) when the ϕVCO frequency is higher than the lock frequency. The ϕVCO output goes to a high impedance state (TRI-STATE®) while in lock mode, and the lock detector output LD also goes to a high state under lock condition.

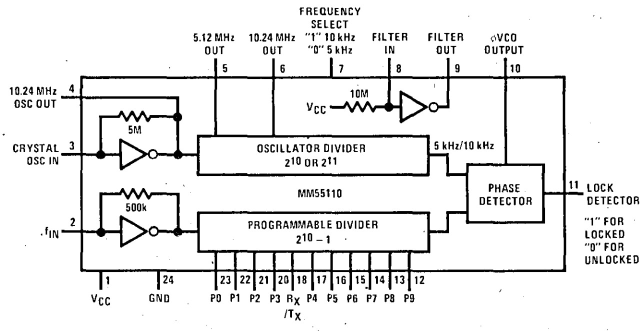
features

- Single crystal operation
- Single power supply
- Low power CMOS technology
- Binary input channel select code
- 2^{10} or 2^{11} divider chain from oscillator input (MM55110), 2^{11} divider chain (MM55108)
- Buffered 5.12 MHz and buffered 10.24 MHz outputs
- On-chip oscillator with bias resistor
- Pull-down resistors on programmable divider inputs
- Receive/transmit input for ÷ by (N+91) while in transmit mode
- Amplifier for filter applications (MM55110)
- Programmable $2^9 - 1$ division of f_{IN}
- Additional programmable input for $2^{10} - 1$ division of f_{IN} (MM55110)
- Amplifier stage on f_{IN} input to accept 1Vp-p signal

block diagrams



MM55108



MM55110

absolute maximum ratings

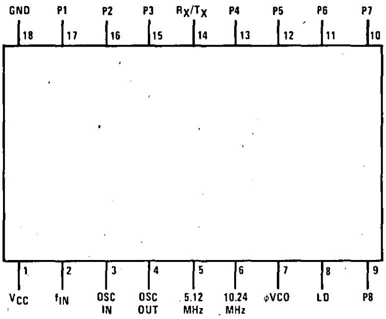
Voltage at Any Pin	V_{CC} + 0.3V to Gnd – 0.3V
Operating Temperature Range	–30°C to +75°C
Storage Temperature	–40°C to +125°C
Operating V_{CC}	12V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics T_A = 25°C, V_{CC} = 8V unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		4.5		10	V
Supply Current (I_{CC})	Freq. at Osc. In = 10.24 MHz at f_{IN} = 2.5 MHz, All Other I/O Pins Open		4	10	mA
Logical "1" Input Voltage ($V_{IN(1)}$) P0–P9, I_S		(V_{CC}–0.4)			V
Logical "0" Input Voltage ($V_{IN(0)}$) P0–P9, I_S				0.4	V
Logical "1" Output Voltage ϕVCO, 10.24 MHz Out, 5.12 MHz Out, Osc. Out, LD	I_O = –0.5 mA	(V_{CC}–0.5)			V
Logical "0" Output Voltage ϕVCO, 10.24 MHz Out, 5.12 MHz Out, Osc. Out, LD	I_O = 0.5 mA			0.5	V
Logical "1" Input Current					
Filter In (Pull-Up)				1	μA
R_X/T_X (Pull-Up)				1	μA
FS, P0–P9 (Pull-Down)		20	40	60	μA
Logical "0" Input Current					
Filter In (Pull-Up)				–1	μA
R_S/T_X (Pull-Up)		–60	–120	–180	μA
FS, P0–P9 (Pull-Down)				1	μA
Toggle Frequency at f_{IN}		3			MHz
Input Signal at f_{IN} (Maximum 3 MHz)	For ac Signal or	1			Vp-p
	($V_{IN(1)}$)	(V_{CC}–0.4)			V
	($V_{IN(0)}$)			0.4	V
Oscillator Frequency at Osc. In				10.24	MHz
TRI-STATE Leakage at ϕVCO	V_{OUT} = V_{CC} or Gnd			|1|	μA

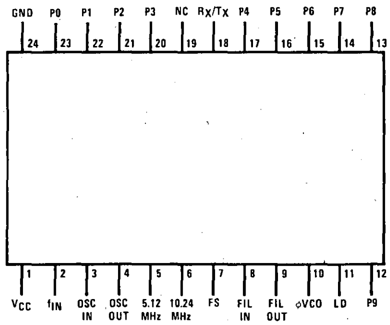
connection diagrams

Dual-In-Line Package



Order Number MM55108N
See Package 20

Dual-In-Line Package



Order Number MM55110N
See Package 22

pin descriptions

P0–P9	Programmable Divider Inputs
f_{IN}	Frequency Input From VCO (Mixed down)
OSC IN	Oscillator Amplifier Input
OSC OUT	Oscillator Amplifier Output
LD	Lock Detector
φVCO	Output of Phase Detector for Control of VCO
FS	Frequency Division Select "1" for 2^{10} Division "0" for 2^{11} Division
5.12 MHz OUT	Buffered 5.12 MHz Output (Oscillator Frequency ÷ By 2)
10.24 MHz OUT	Buffered 10.24 MHz Output (Oscillator Frequency)
FILTER IN	Filter Amplifier Input
FILTER OUT	Filter Amplifier Output
R_X/T_X	Receive/Transmit Input "0" for Transmit Mode (÷ by (N+91))

typical applications

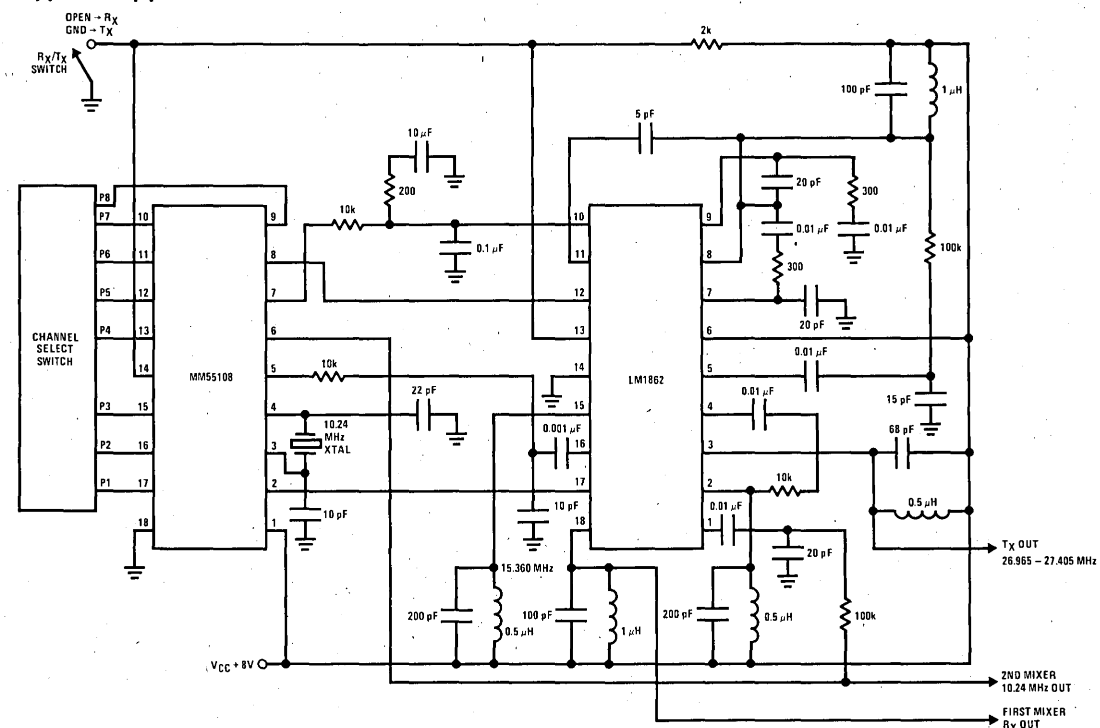


FIGURE 1. Single Crystal 40-Channel Low Side Injection with MM55108 and LM1862

typical applications (Continued)

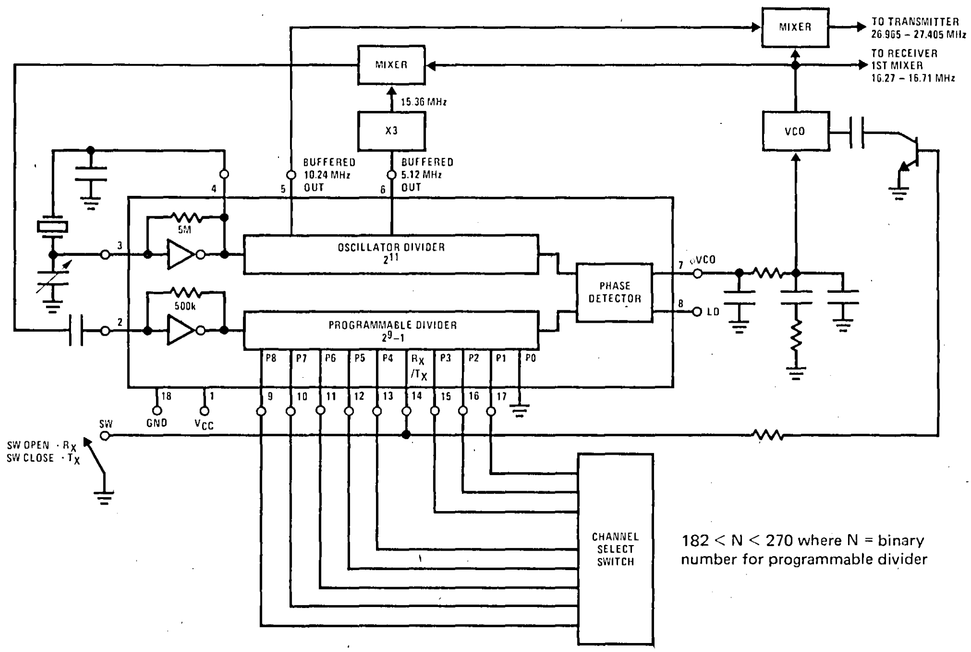


FIGURE 2. MM55108 Single Crystal 40-Channel Low Side Injection

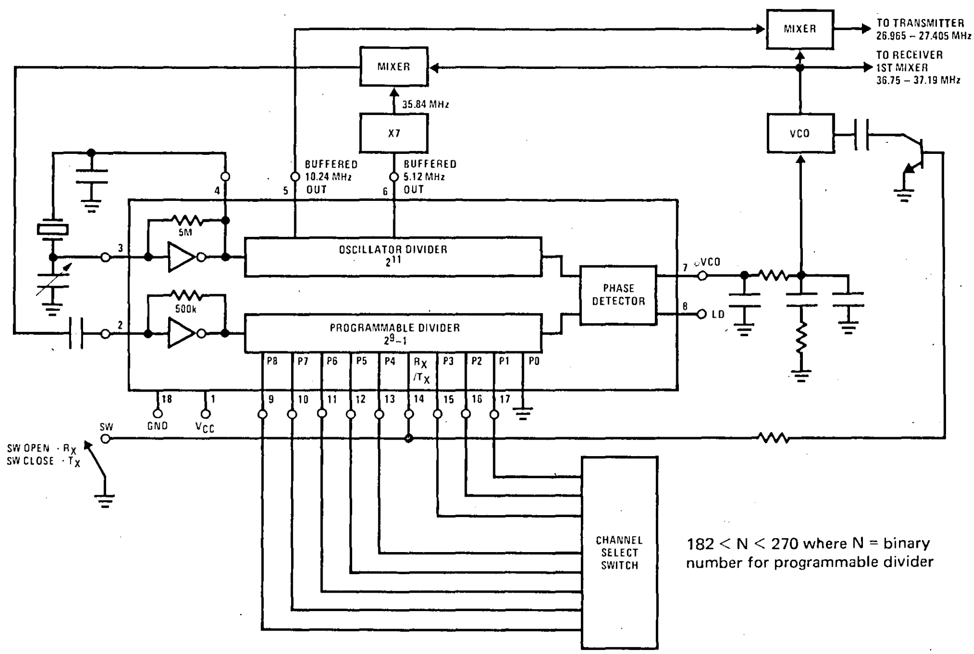


FIGURE 3. MM55108 Single Crystal 40-Channel High Side Injection

6

truth tables

TABLE I. Binary Inputs to Programmable Divider for MM55108

	R_X/T_X "1" OR "OPEN" N	R_X/T_X "0" OR "CLOSED" N	INPUTS 2^8 P8	2^7 P7	2^6 P6	2^5 P5	2^4 P4	2^3 P3	2^2 P2	2^1 P1
	1	92	0	0	0	0	0	0	0	0
	2	93	0	0	0	0	0	0	0	1
	4	95	0	0	0	0	0	0	1	0
	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
Channel 1 →	182	273	0	1	0	1	1	0	1	1
	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
Channel 40 →	270	361	1	0	0	0	0	1	1	1
	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.
	510	601	1	1	1	1	1	1	1	1

1 = logical "1"
0 = logical "0"

TABLE II. Binary Inputs to Programmable Divider for MM55110

	R_X/T_X "1" OR "OPEN" N	R_X/T_X "0" OR "CLOSED" N	INPUTS 2^9 P9	2^8 P8	2^7 P7	2^6 P6	2^5 P5	2^4 P4	2^3 P3	2^2 P2	2^1 P1	2^0 P0
	1	92	0	0	0	0	0	0	0	0	0	X
	2	93	0	0	0	0	0	0	0	0	1	0
	3	94	0	0	0	0	0	0	0	0	1	1
	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.
Channel 1 →	182	273	0	0	1	0	1	1	0	1	1	0
	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.
Channel 40 →	270	361	0	1	0	0	0	0	1	1	1	0
	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.
	1023	1114	1	1	1	1	1	1	1	1	1	1

X = don't care
1 = logical "1"
0 = logical "0"

SECTION 7
WATCHES

MM5829 LED watch circuit

general description

The MM5829 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that provides or controls all signals needed for a 3 1/2 digit LED watch. The display format is 12 hours. The circuit time base is a 32768 Hz crystal controlled oscillator. This time base frequency is successively divided to provide drive signals for a multiplexed 7 segment LED display of either HOURS-MINUTES or SECONDS upon demand. Outputs interface with currently available standard bipolar segment and digit driver integrated circuits. The device operates from a single 2.4V to 5.0V supply. A STOP MODE is provided such that an entire watch may be placed in a powered down state with the oscillator stopped when still connected to the battery. The MM5829 is available in a 30-lead ceramic flat package or as unpackaged die suitable for hybrid assembly.

features

- 32768 Hz crystal controlled operation
- Single 3V supply
- Low power dissipation (15μW typ)
- Seconds, minutes and hours operation
- 3 1/2 digit, 12 hour display format
- Simple display/set controls
- Power-down mode
- Easy interface to standard bipolar IC's for display drive

block diagram

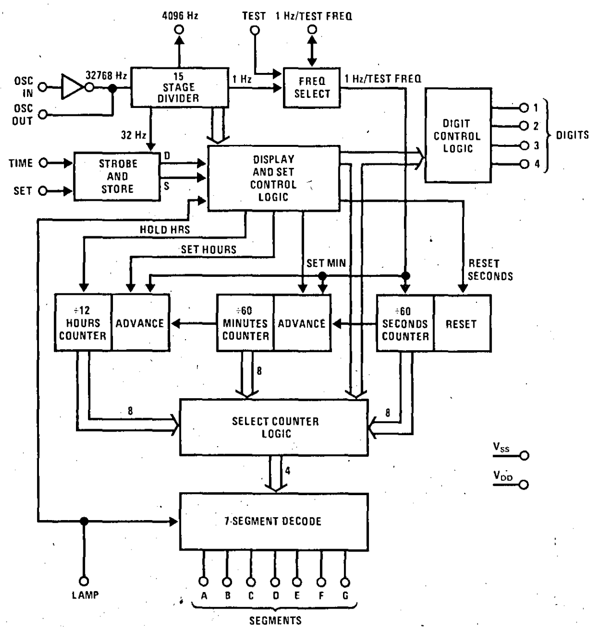


FIGURE 1.

chip pad layout

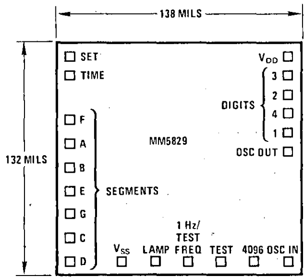


FIGURE 2.

connection diagram

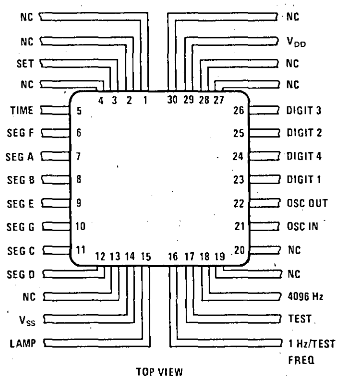


FIGURE 3.

absolute maximum ratings

Voltage at Any Pin	V_{SS}–0.3V to V_{DD}+0.3V
Operating Temperature Range	–5°C to +70°C
Storage Temperature Range	
Dice	–25°C to +85°C
Packages	–55°C to +125°C
$V_{DD} - V_{SS}$	5V max
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = GND, $2.4 \leq V_{DD} \leq 4.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	T_A = 25°C	2.7			V
Input Voltage Level @ Time, Set	V_{DD} = 3.0V				
Logical "1"		1/2 V_{DD}		V_{DD}	V
Logical "0"	300 kΩ Pull-Down to V_{SS}		Open		V
Input Voltage Level @ Test Frequency	V_{DD} = 3.0V				
Logical "1"		V_{DD}–0.25		V_{DD}	V
Logical "0"		V_{SS}		V_{SS}+0.25	V
Input Voltage Level @ Lamp, Test	V_{DD} = 3.0V				
Logical "1"	1 MΩ Pull-Up to V_{DD}		Open		V
Logical "0"		V_{SS}		V_{SS}+0.25	V
Input Current @ Time and Set	$V_{IN} = V_{DD}$, Sink Only, V_{DD} = 3.0V			10	μA
Input Current @ Lamp and Test	$V_{IN} = V_{SS}$, Source Only, V_{DD} = 3.0V			3	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0.0V All other pads GND			5	pF
Output Voltage Level @ Segment Drivers					V
Logical "1"	V_{DD} = 2.4V, $I_{SOURCE} \geq 10\mu A$	V_{DD}–0.2		V_{DD}	V
Logical "0"	V_{DD} = 2.4V, $I_{SINK} \geq 300\mu A$	V_{SS}		V_{SS}+0.5	V
Output Voltage Level @ Digit Drivers					
Logical "1"	V_{DD} = 2.4V, $I_{SOURCE} \geq 840\mu A$	V_{DD}–1.3		V_{DD}	V
Logical "0"	V_{DD} = 2.4V, $I_{SINK} \geq 20\mu A$	V_{SS}		V_{SS}+0.2	V
Output Voltage Level @ 4096, 1 Hz	V_{DD} = 3.0V				
Logical "1"	$I_{SOURCE} \geq 10\mu A$	V_{DD}–0.2		V_{DD}	V
Logical "0"	$I_{SINK} \geq 10\mu A$	V_{SS}		V_{SS}+0.2	V
Supply Current (I_{DD})	f = 32768 Hz, T_A = 25°C V_{DD} = 3.0V, Unused Inputs Open, Outputs Open		5	10	μA
Supply Current (I_{DD})	Stop Mode, T_A = 25°C, V_{DD} = 3.0V, Unused Inputs Open, Outputs Open			1	μA

functional description

A block diagram of the MM5829 digital watch chip is shown in *Figure 1*. A chip pad layout is shown in *Figure 2* and a package connection diagram in *Figure 3*.

Time Base

The precision time base of the watch is provided by the interconnection of a 32768 Hz quartz crystal and the RC network shown in *Figure 4* together with the CMOS inverter/amplifier provided between the oscillator in and oscillator out terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Resistor R2 is required in order to (a) reduce the voltage sensitivity of the network, (b) limit the power dissipation in the quartz crystal, and (c) provide added phase shift for good start-up and low voltage circuit performance. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides >100 ppm tuning range when used with standard X-Y flexure crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

The 4096 Hz output or 1 Hz output can be used to monitor the oscillator frequency during initial tuning without disturbing the network itself.

functional description (con't)

Time Display

The HOURS-MINUTES/SECONDS Display feature is controlled by a normally open switch connected to the Time input as shown in *Figure 6.* A logic "1" applied to the Time input will cause HOURS-MINUTES to be displayed for not less than 1.5 seconds or more than 2.0 seconds. The hours digits can display values 1–12 while the minutes digits can display values 00–59. All zero values are displayed for minutes and leading zero values of hours are blanked. The character display font is shown in *Figure 5.* Holding a logic "1" on the Time input after the time-out of HOURS-MINUTES will cause SECONDS to be displayed in digit positions 3 and 4 until the Time input is opened. SECONDS will blink while displayed. Each value is visible for 0.5 seconds and blanked for 0.5 seconds. The SECONDS digits can display values 00–59. All zero values are displayed.

Display Multiplexing

Outputs from each counter are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 28 leads to interconnect a four digit (7 segments/digit) watch, only 11 output leads are required. *Figure 6* shows the interconnection of an LED watch system. The four digit outputs of the MM5829 are designed to interface with the bipolar DM8650 digit driver chip. The seven segment outputs are designed to interface with the bipolar DM8651 segment driver chip. The four digits of the LED Display are multiplexed with a 25% duty cycle, 1024 Hz signal during Display. The digit drivers are turned off for 15μs during change of digits to allow the seven segments to change without "ghosting" of the Display. When the MM5829, DM8650, and DM8651 are used as shown in the typical application of *Figure 6* the peak segment on currents are typically 9 mA. The 0101 LED Display gives excellent brightness under these drive conditions.

Time Setting

A normally open switch connected to the Set input is used in conjunction with the Time switch to set hours, minutes, and synchronize seconds.

HOURS: A logic "1" applied to the Set input will cause HOURS-MINUTES to be displayed and will advance HOURS at a 1 Hz rate. The Seconds and Minutes counters continue normal counting during this condition.

SECONDS: With a logic "1" on the Time input, the application of a logic "1" to the Set input will immediately reset the Seconds counter to 00 and allow a normal seconds count from there.

MINUTES: A logic "1" applied to both the Time and Set inputs will allow HOURS-MINUTES to be displayed and will advance the MINUTES at a 1 Hz rate. A transition from 59 to 00 will not advance the Hours counter in this condition.

CONTACT BOUNCE: Debounce circuitry is provided on the Time and Set inputs to remove any logic uncertainty upon either closure or release of switches providing switch bounce settles within 20 ms.

Oscillator Stop

The oscillator can be stopped in order to conserve battery life during shipment of the watch. The oscillator will stop if a logic "1" is momentarily applied to the Time input and while HOURS-MINUTES are displayed a logic "1" is momentarily applied to the Set input. The Display is inactive during this mode. The oscillator will start again when a logic "1" is applied to the Set input.

Test Points

Four pins are provided for test purposes. A 4096 Hz symmetrical signal is brought out for oscillator tuning. The pin 1 Hz/Test Frequency is an input/output under control of Test. With Test open, a 1 Hz output will appear on the 1 Hz/Test Frequency pin. If Test is connected to a logic "0," the 1 Hz/Test Frequency becomes an input and any frequency connected to it will be divided by the Seconds counter in place of the normal 1 Hz signal. This feature is provided to allow high speed functional testing of the watch system. If lamp is connected to a logic "0," all segments will be forced to an on condition under control of the normal 25% duty cycle of the digit drivers. An internal pull-up resistor will normally hold the lamp input to logic "1."

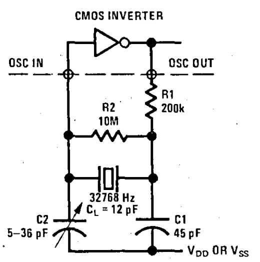


FIGURE 4. Crystal Oscillator Network

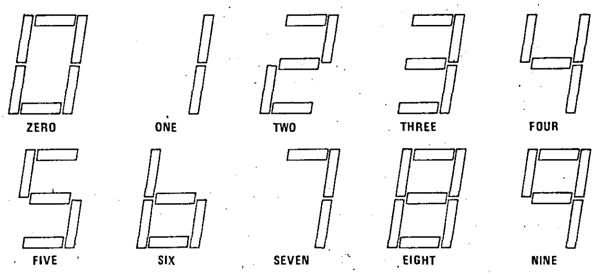


FIGURE 5. Character Display Font

functional description (con't)

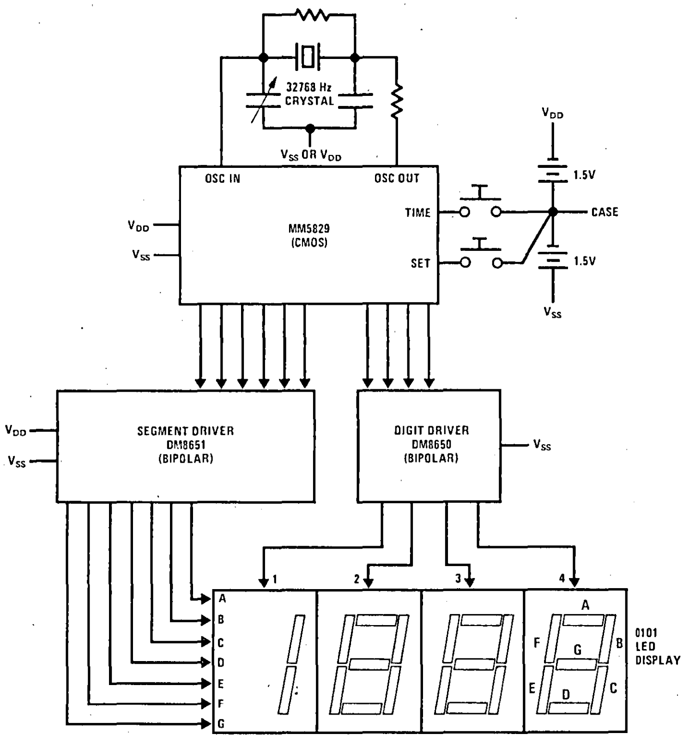


FIGURE 6. Typical Application

MM5860, MM58601, MM5880, MM58801
two time zone LED watch circuits

general description

The MM5860/MM5880 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that provides or controls all signals needed for a 4-digit LED watch. The display format is either 12 or 24 hours. The circuit time base is a 32,768 Hz crystal controlled oscillator. This time base is successively divided to provide drive signals for a multiplexed 7-segment LED display of Date-Month, Local Hours-Minutes, Zone Hours-Minutes, or Seconds upon demand for the MM5860 version. The MM5880 version will vary only in the date display by displaying Month-Date. The MM58X01 versions will blink the Month during the date display. Outputs interface with currently available standard bipolar segment and digit driver integrated circuits. The device operates from a single 2.4–4.0V supply. All versions are available as unpackaged die suitable for hybrid assembly or in 40-lead dual-in-line packages for evaluation purposes.

features

- 32,768 Hz crystal controlled operation
- Single 3V supply
- Low power dissipation (15μW typical)
- Seconds, Minutes, Local and Zone Hours, Date, and Month display
- 4 year calendar
- 4-digit, 12/24 hour display format
- AM indication in 12-hour format
- Simple display/set controls
- Auto return from Set and Display mode
- Easy interface to standard bipolar IC's for display drive
- Display brightness control

block and connection diagrams

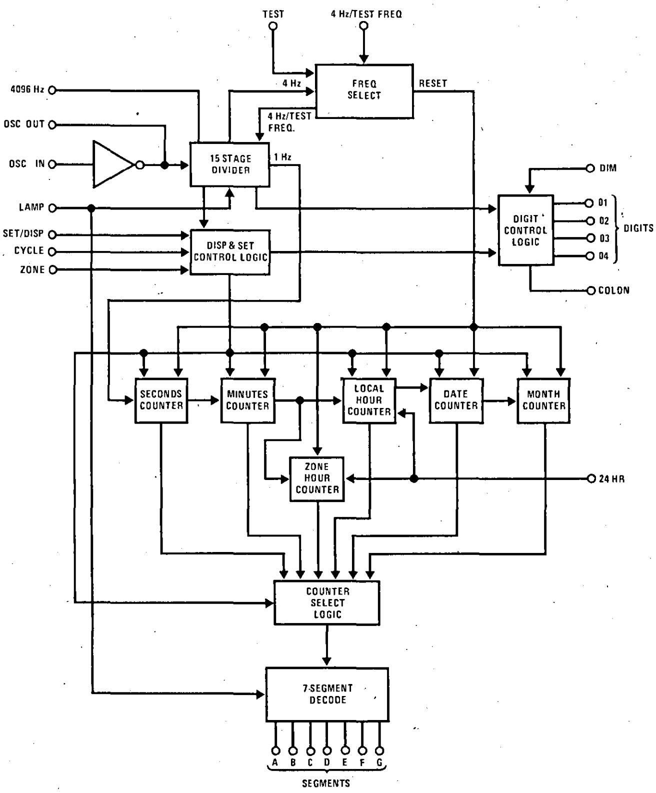


FIGURE 1.

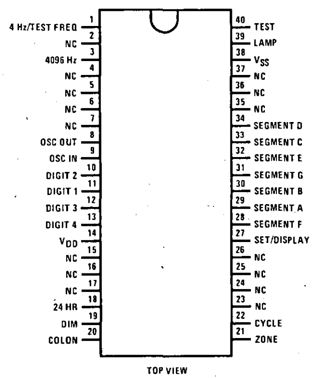


FIGURE 2.

absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	$-5°C$ to $+70°C$
Storage Temperature Range	$-25°C$ to $+85°C$
$V_{DD} - V_{SS}$	5V max
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = Gnd, $2.4V \leq V_{DD} \leq 4V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	$T_A = 25°C$, Circuit of *Figure 4*	2.7			V
Input Voltage Levels at Cycle, Set/Display and Zone	$V_{DD} = 3V$				
Logical "1"		1/2 V_{DD}		V_{DD}	V
Logical "0"	300kΩ Internal Pull-Down to V_{SS}		Open		
Input Voltage Levels at 4 Hz/Test Freq, 24 Hr.					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels at Lamp, Test	$V_{DD} = 3V$				
Logical "1"	1 MΩ Internal Pull-Up to V_{DD}		Open		
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels at Dim					
Display Duty Cycle = 21.875%	5 MΩ Pull-Down to V_{SS}	Open	or	$V_{SS}+0.3$	V
Display Duty Cycle = 9.125%		$V_{SS}+0.9$		$V_{DD}-1.1$	V
Display Duty Cycle = 3.125%		$V_{DD}-0.5$			V
Input Current at Cycle, Set/Display and Zone	$V_{IN} = V_{DD}$, Sink Only, $V_{DD} = 3V$	0.2		10	μA
Input Current at Lamp and Test	$V_{IN} = V_{SS}$, Source Only, $V_{DD} = 3V$	0.2		5	μA
Input Current of Dim	$V_{IN} = V_{DD}$, Sink Only, $V_{DD} = 3V$	0.1		2	μA
Input Capacitance	f = 1 MHz, V_{IN} = 0V, All Other Pads Gnd			5	pF
Output Current Levels at Segment Drivers					
Logical "1," Source	$V_{DD} = 2.4V$, $V_{OUT} = V_{DD} - 0.2V$	10	30		μA
Logical "0," Sink	$V_{DD} = 2.4V$, $V_{OUT} = V_{SS} + 0.5V$	300	600		μA
Output Current Levels at Digit Drivers					
Logical "1," Source	$V_{DD} = 2.4V$, $V_{OUT} = V_{DD} - 1.3V$	840	1500		μA
Logical "0," Sink	$V_{DD} = 2.4V$, $V_{OUT} = V_{SS} + 0.2V$	10	30		μA
Output Current Levels at 4 Hz/Test Freq, 4096 Hz	$V_{DD} = 3V$				
Logical "1," Source	$V_{OUT} = V_{DD} - 0.2V$	10			μA
Logical "0," Sink	$V_{OUT} = V_{SS} + 0.2V$	10			μA
Output Current Levels at Colon					
Logical "0," Sink	$V_{DD} = 2.4V$, $V_{OUT} = 1V$	0.8			mA
Supply Current (I_{DD})	f = 32,768 Hz, $T_A = 25°C$, $V_{DD} = 3V$, Unused Inputs Open, Outputs Open		5	10	μA
Supply Current (I_{DD})	Oscillator Stopped, $T_A = 25°C$, $V_{DD} = 3V$, Unused Inputs Open, Outputs Open		0.05	1	μA

functional description

Unless otherwise specified, all references to the MM58X0 will also refer to the MM58X01. A block diagram of the MM5860/MM5880 is shown in *Figure 1.* The connection diagram is shown in *Figure 2* and the chip pad layout in *Figure 3.*

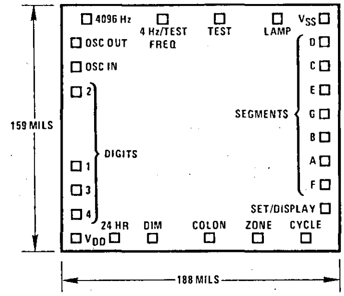


FIGURE 3. Pad Layout

Time Base: The precision time base of the watch is provided by connecting a crystal-controlled RC network to the on-chip CMOS inverter/amplifier as shown in *Figure 4.* For proper operation, the network should be tuned to 32,768 Hz. Resistor R1 is used to bias the on-chip inverter for class A amplifier operation. Resistor R2 is used to (a) reduce the voltage sensitivity of the network; (b) limit the power dissipation in the quartz crystal; and (c) provide added phase shift for good start-up and low voltage circuit performance. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. The network shown in *Figure 4* provides greater than 100 ppm tuning range when used with standard X-Y flexure quartz crystals trimmed for C_L = 12 pF. Tuning to better than 2 ppm is easily obtainable.

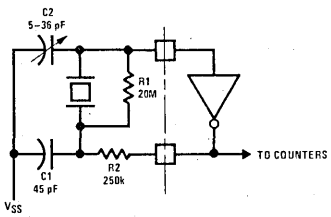


FIGURE 4. Oscillator RC Network

The 4096 Hz output or the 4 Hz output can be used to monitor the oscillator frequency during initial tuning without disturbing the network itself.

Display Multiplexing: The counter data selected to be displayed is time-division multiplexed to provide digit-sequential presentation to the LED display. This reduces the number of outputs required to drive the 4-digit display to 11 (7 segment drivers and four digit drivers). The display font is shown in *Figure 5. Figure 6* is a schematic diagram of a typical LED watch using the MM5860/MM5880 watch chip. The digit outputs of the MM5860/MM5880 are designed to interface with the bipolar DS8658 digit driver chip and the segment driver outputs will interface with the bipolar DS8659 segment driver chip. The four digits of the LED display are multiplexed with a 25% duty cycle, 1024 Hz signal during the display period. The digit drivers are disabled for 32μs at the beginning of each digit enable time to allow the segment decoding circuitry adequate time to switch to the next digit's information. This eliminates the possibility of "ghosting" information between digits. When the MM5860/MM5880, DS8658 and DS8659 are used in a typical application as shown in *Figure 6* the peak segment "ON" currents are typically 11 mA. The NSCO101 LED display gives excellent brightness under these drive conditions.

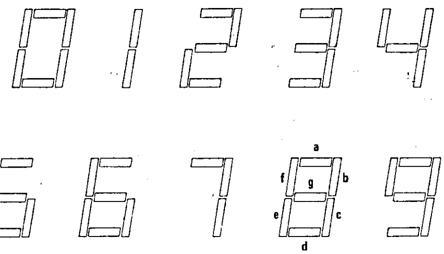


FIGURE 5. Character Display Font

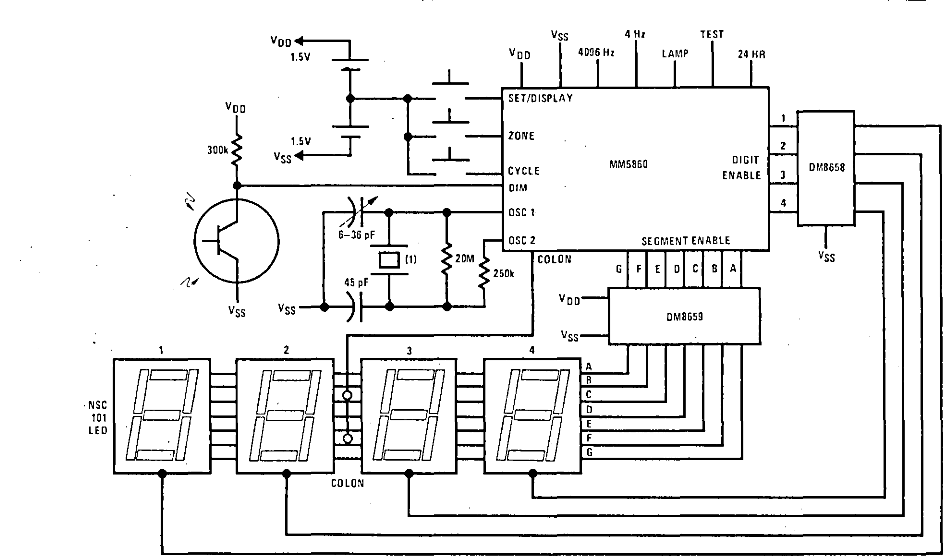
DISPLAY CONTROL

The Time and Date display sequence is controlled by a normally open switch connected to the Set/Display input. With the display off, depressing the Set/Display switch will activate the Local Hour: Minute display. This display will remain on for 1.25 seconds ±0.125 seconds. If the switch is still held in at the end of this time out, Seconds will be displayed, blinking on for 0.25 seconds and off for 0.75 seconds, until the Set/Display switch is released. If, during the Hour:Minute display, the Set/Display switch is released and depressed a second time the date will be displayed as Date Month in the MM5860 version and as Month Date in the MM5880 version. The Month will blink on for 0.25 seconds and off for 0.75 seconds in the MM58601 and the MM58801 versions and not blink in the MM5860 and the MM5880 versions. The display will remain on for 1.25 seconds and turn off automatically if the Set Display switch has been released. Holding the Set/ Display switch in past the display time out will maintain the display until the Set/Display switch is released. Zone Hour:Minute can be displayed by depressing the Zone switch. This display will also remain on for 1.25 seconds ±0.125 seconds. Holding the Zone switch depressed beyond this period will cause Seconds to be displayed until the switch is released. The date information can not be displayed using the Zone switch. Leading zeros are blanked on the Month, Date and Hour displays.

TIME SETTING

The setting sequence is controlled by a normally open switch connected to the Cycle input. Depressing the Cycle switch will advance the watch to the next set mode.

Set Hour Mode: With the watch in normal Run mode and the display off, depressing the Cycle switch will advance the watch to the Set Local Hour mode. In this mode local hours will be displayed in digit positions 1 and 2 followed by the colon. The AM dot will be on during AM time display. Depressing the Set/Display switch will advance the Local Hour counter at a 2 Hz rate. Depressing the Zone switch while in the Set Local Hour mode will cause zone hours information to replace the local hours information in digit positions 1 and 2.



(1) Anti-resonant quartz crystal, C_L = 12 pF

FIGURE 6. System Schematic

The colon and the AM dot will still be presented as in the Local Hours display. The Zone Hour counter can now be advanced at a 2 Hz rate by depressing the Set/Display switch.

In either of the above Set Hour modes if no switches are depressed for 5.25 seconds ±0.125 seconds consecutively, the watch will automatically return to the Run mode. Depressing the Cycle switch while in the Set Zone Hour mode will return the watch to the Run mode. Depressing it while in the Set Local Hour mode will place the watch in the Set Minutes mode.

Set Minutes Mode: The Set Minutes mode will display minutes in digit positions 3 and 4 preceded by the colon. Depressing the Set/Display switch while still holding the Cycle switch in will enable the Hold flag but will not allow advancement of the Minutes Counter. Depressing the Set/Display switch after the Cycle switch has been released will do the following:

a. Reset and hold the Seconds Counter
b. Enable the Hold flag, and
c. Advance the Minutes Counter at a 2 Hz rate

If none of the switches are depressed for 5.25 seconds ±0.125 seconds consecutively while in the Set Minutes mode, the watch will automatically return to the Run Mode if minutes have not been set or will jump to the Hold mode if minutes have been set. Depressing the Cycle switch while in the Set Minutes mode will advance the watch to the Set Date mode for the MM5860 version or the Set Month mode for the MM5880 version.

Set Date Mode: The Set Date mode will display the Day of Month in digit positions 1 and 2 in the MM5860 version, or in digit positions 3 and 4 in the MM5880 version, with no colon displayed. Depressing the Set/Display switch while in the Set Date mode will advance the Date Counter at a 2 Hz rate.

If none of the switches are depressed for 5.25 seconds ±0.125 seconds consecutively while in the Set Date mode, the watch will automatically return to the Run mode if the Minutes Counter was not set or will jump to the Hold mode if the Minutes Counter was set. Depressing the Cycle switch while in the Set Date mode will advance the watch to the Run mode if the Minutes Counter was not set or will advance it to the Hold mode if the Minutes Counter was set for the MM5880 version. Depressing the Cycle switch while in the Set Date mode of the MM5860 version will advance the watch to the Set Month mode.

Set Month Mode: The Set Month mode will display the month in digit positions 3 and 4 in the MM5860 version, or in digit positions 1 and 2 in the MM5880 version, with no colon displayed. Depressing the Set/Display switch while in the Set Month mode will advance the Month Counter at a 2 Hz rate.

If none of the switches are depressed for 5.25 seconds ±0.125 seconds consecutively while in the Set Month mode, the watch will automatically return to the Run mode if the Minutes Counter was not set or will jump to the Hold mode if the Minutes Counter was set. Depressing the Cycle switch while in the Set Month mode will advance the watch to the Run mode if the Minutes Counter was not set or will advance it to the Hold mode if the Minutes Counter was set for the MM5860 version. Depressing the Cycle switch in the Set Month mode of the MM5880 version will advance the watch to the Set Date mode.

Hold Mode: In the Hold mode the Seconds Counter is held at 00. Local Hour:Minute will blink on for 0.25 seconds and off for 0.75 seconds. Depressing the Cycle switch while in the Hold mode will put the watch back into the Set Hour mode and then the counters can be set as described previously. With the Hold mode still activated, the watch will return to the Hold mode only. Depressing the Set/Display switch while in the Hold mode will place the watch into the display Local Hour: Minute mode and allow the Seconds Counter to begin normal operation.

There is no roll-over of the next higher counter while a counter is being set. For example, while the Minutes Counter is set from 59 to 00 neither the Local Hour nor the Zone Hour Counter will be advanced.

Figure 7 is a state diagram showing the display and set functions for both the MM5860 and the MM5880.

COLON OUTPUT

This output provides direct drive of the colon in the LED display unit. Colon will sink current when activated. The colon output will be activated during the display of either one of the hour counters or the minute counter or both.

CONTACT BOUNCE

Debounce circuitry is provided on the "Set/Display" and "Cycle" inputs to remove any logic uncertainty upon either closure or release of switches provided switch bounce settles within 100 ms.

12/24 HOUR OPTION

12/24 hour mode operation of the watch is controlled by the logical state of the "24 Hr" input. If the "24 Hr" input is a logical "1" the watch will operate in the 24 hour mode. When the "24 Hr" input is a logical "0" the watch operates in 12 hour mode.

DIM INPUT

The Dim input is a three level input used to control the display intensity of the watch. This input has a pull-down to V_{SS} to hold it normally at a logical "0."

In this condition the display will normally be at maximum intensity. With the Dim input at 1/2 V_{DD}, the display will be at approximately 1/2 of full intensity. Placing the input at V_{DD} will reduce the display intensity to approximately 1/8 of full intensity. *Figure 8* shows the switching threshold ranges for the three level DIM input.

TEST POINTS

Four pads are provided for test purposes.

4096 Hz: This pad outputs a 4096 Hz signal that can be used for oscillator tuning.

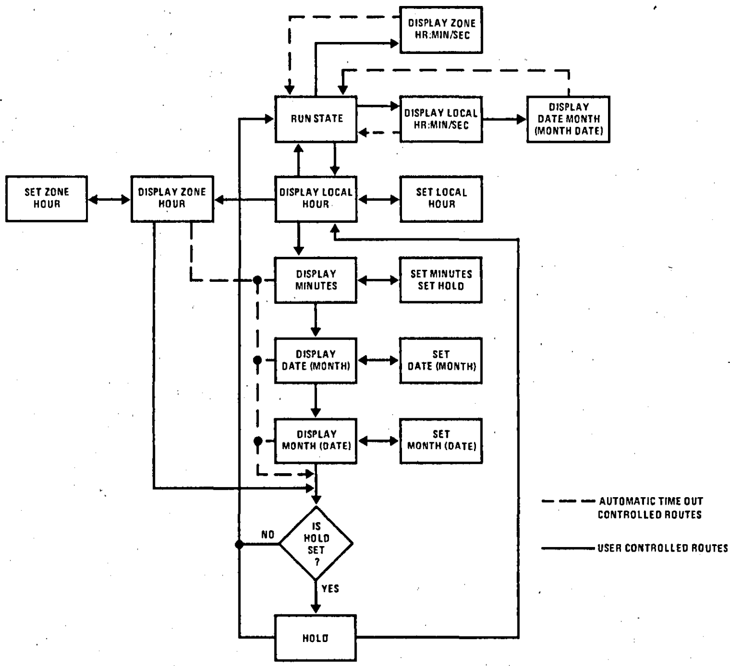


FIGURE 7. Control State Diagram MM5860 (MM5880)

	DISPLAY TIME/DIGIT	DISPLAY CONDITION
$V_{IN} = V_{DD}$	3.125%	Low Ambient Light Levels
$V_{IN} = V_{DD} - 0.5V$	Threshold Region	
$V_{IN} = V_{DD} - 1.1V$	9.125%	Moderate Ambient Light Levels
$V_{IN} = V_{SS} + 0.9V$	Threshold Region	
$V_{IN} = V_{SS} + 0.3V$	21.875%	High Ambient Light Levels
$V_{IN} = V_{SS}$		

FIGURE 8. Counter Voltage Levels at Dim Input

TEST POINTS (CON'T)

4 Hz/Test Freq: This is an input/output pad under the control of the "Test" input. When "Test" is at a logical "0," the "4 Hz/Test Freq" pad becomes an input and any frequency connected to it will replace the normal internal 4 Hz signal. This feature is provided to allow high speed functional testing of the watch system. When "test" is open or at a logical "1", a 4 Hz output will appear on the "4 Hz/Test Freq" pad.

Test: This pad is used as an input to control "4 Hz/ Test Freq." An internal pull-up resistor will normally hold "Test" at a logical "1."

Changing the Test input from a logical "1" to a logical "0" will generate a reset pulse which will Set the internal counters to 1 PM on January the first. The watch is now in a known state for testing purposes.

Lamp: When the "Lamp" input is at a logical "0," all segments of the display will be forced to an "ON" condition under control of the normal 25% duty cycle of the digit drivers. An internal pull-up resistor will normally hold the "Lamp" input at a logical "1."

Watches

MM5879, MM5889, MM5899 RC circuits

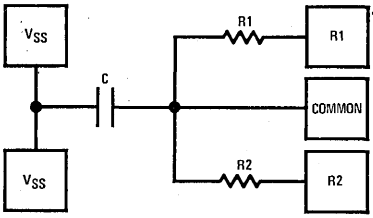
general description

The MM5879, MM5889, MM5899 are RC circuits which may be used in watch modules and other similar applications. They are available in die form. All die are pad-for-pad interchangeable, offering a range of capacitance and resistance values.

absolute maximum ratings

Voltage at Any Pad	V_{SS} + 0.3V to V_{SS} − 20V
Operating Temperature	−5°C to +70°C
Storage Temperature	−65°C to +150°C

schematic diagram



PART NUMBER	R1		R2		CAP (Note 1)	
	MIN	MAX	MIN	MAX	MIN	MAX
MM5879	125k	235k	15M	30M	9 pF	13 pF
MM5889	250k	470k	15M	30M	45 pF	55 pF
MM5889AB	250k	470k	15M	30M	24 pF	36 pF
MM5899	250k	470k	15M	30M	14 pF	20 pF

Note 1: Capacitances are measured periodically only. Capacitance measured from V_{SS} to common.

chip pad layout

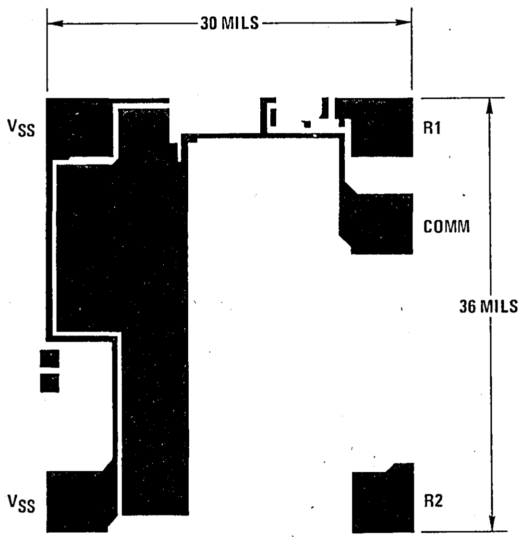


FIGURE 1.

MM5885, MM5886 direct drive LED watch

general description

The MM5885, MM5886 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that provides or controls all signals needed for a 4-digit LED watch. The display format is 12 hours. The circuit time base is a 32,768 Hz crystal controlled oscillator. This time base frequency is successively divided to provide drive signals for a multiplexed 9-segment, alphanumeric LED display of DAY-DATE, HOURS-MINUTES or SECONDS upon demand. A Month counter is provided to control the count sequence of the Date counter. The MM5885 uses one button to display while the MM5886 uses two buttons for display purposes. Outputs interface directly with an alphanumeric LED display. The device operates from a single 2.4V to 4.0V supply. Both the MM5885 and MM5886 are available as unpackaged die suitable for hybrid assembly or in a 40-lead dual-in-line package for evaluation purposes.

features

- No external parts except the battery, LEDs and crystal
- 32,768 Hz crystal controlled operation
- Single 3V supply
- Low power dissipation (15μW typ)
- Seconds, Minutes, Hours, Day-of-Week, Date and Month operation
- 4 year calendar
- 4-digit, 12 hour display format
- Simple display/set controls
- Inertial switch input
- Alphanumeric display
- Direct drive outputs
- Display brightness control
- AM/PM indication during set hours
- Month indication during set month
- Test features
- Single button display control (MM5885)

block diagram

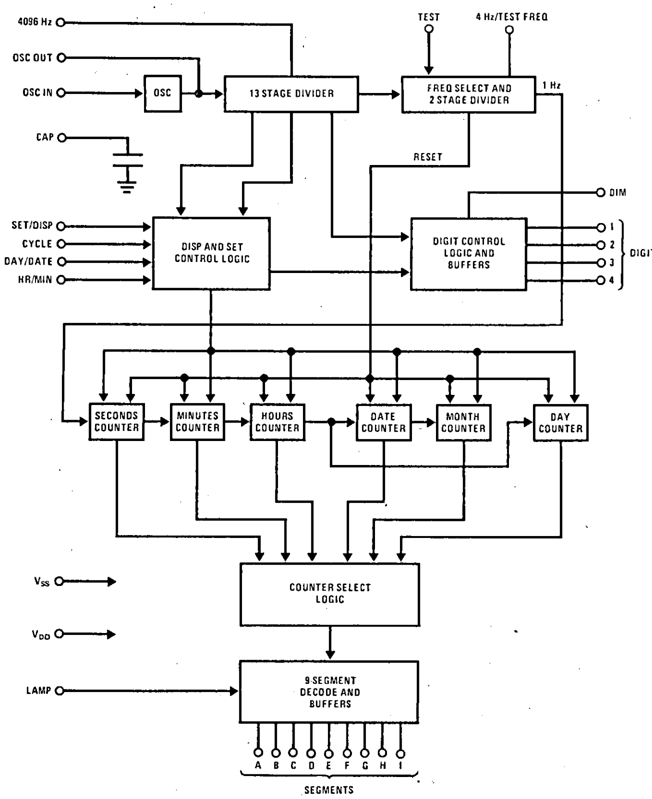


FIGURE 1.

absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	$-5^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-25^{\circ}C$ to $+85^{\circ}C$
$V_{DD} - V_{SS}$	5V max
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, V_{SS} = GND, $2.4 \leq V_{DD} \leq 4.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	$T_A = 25^{\circ}C$	2.7			V
Input Voltage Levels at Cycle, Set/Display, Day/Date, Hour/Min					
Logical "1"	300 kΩ Internal Pull-Down to V_{SS}	1/2 V_{DD}		V_{DD}	V
Logical "0"			Open		
Input Voltage Levels at 4 Hz/Test Freq.					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels at Lamp, Test					
Logical "1"	100 kΩ Internal Pull-Up to V_{DD}		Open		
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels at Dim, Display Duty Cycle = 21.875%	5 MΩ Pull-Down to V_{SS}	Open		$V_{SS}+0.3$	V
Display Duty Cycle = 9.125%		$V_{SS}+0.9$		$V_{DD}-1.1$	V
Display Duty Cycle = 3.125%		$V_{DD}-0.5$		V_{DD}	V
Input Current at Cycle, Set/Display, Day/Date, Hour/Min	$V_{DD} = 3.0V$, $V_{IN} = V_{DD}$, Sink Only		30	50	μA
Input Current at Lamp, Test	$V_{DD} = 3.0V$, $V_{IN} = V_{SS}$, Source Only		30	50	μA
Input Capacitance	f = 1 MHz, V_{IN} = 0V, All Other Pads GND			5	pF
Output Current Levels at Segment Drivers	$V_{DD} = 2.7V$				
"ON" Source	$V_{OUT} = V_{DD} - 0.5V$	7	10	15	mA
"OFF" Source	$V_{OUT} = V_{DD} - 1.1V$			50	μA
Output Current Levels at Digit Drivers	$V_{DD} = 2.7V$				
"ON" Sink	$V_{OUT} = V_{SS} + 0.6V$	50	70	2	mA
"OFF" Sink	V_{OUT} = 2.0V, All Digit Drivers Tied in Parallel			1	μA
Output Current Levels at 4 Hz/Test Freq., 4096 Hz					
Logical "1" Source	$V_{OUT} = V_{DD} - 0.2V$	10			μA
Logical "0" Sink	$V_{OUT} = V_{SS} + 0.2V$	10			μA
Operating Supply Current (I_{DD})	f = 32,768 Hz, $T_A = 25^{\circ}C$, V_{DD} = 3V, Unused Inputs Open, Outputs Open		5	10	μA
Quiescent Supply Current (I_{DD})	Osc In @ Gnd, V_{DD} = 3V, $T_A = 25^{\circ}C$, Other Inputs and Outputs Open		0.05	1	μA

functional description

A block diagram of the MM5885/MM5886 direct drive digital watch is shown in *Figure 1*. The chip pad layout is shown in *Figure 2* and a package connection diagram in *Figure 3*.

Time Base: The precision time base of the watch is provided by the 32,768 Hz crystal controlled oscillator, which consists of the quartz crystal, the CMOS inverter/amplifier and the RC network shown in *Figure 4*. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Resistor R2 is required in order to (a) reduce the voltage sensitivity of the network; (b) limit the power dissipation in the quartz crystal; and (c) provide added phase shift for good start-up and low voltage circuit performance. Capacitors C1 and C_{eff} in series provide the parallel load capacitance required for precise tuning of the quartz crystal. The network shown in *Figure 4* provides greater than 100 ppm tuning range when used with standard X-Y flexure quartz crystal trimmed for C_L = 12 pF. Tuning to better than 2 ppm is easily obtainable.

Cap: This pin is used with Oscillator Out to add more capacitance to the oscillator RC network shown in *Figure 4*.

Display Control: The "Time" and "Date" display sequence is controlled by normally open switches connected to SET/DISPLAY, DAY/DATE (MM5886), and HOUR/MINUTE (inertial switch) inputs. With the display "OFF," depressing the SET/DISPLAY switch will activate the HOUR-MINUTE display. This display will remain "ON" for 1.25 seconds ±0.125 seconds. If the switch is still held in at the end of this time out, SECONDS will be displayed blinking "ON" for 0.25 seconds and "OFF" for 0.75 seconds until the SET/DISPLAY switch is released. If, during the HOUR-MINUTE display, the SET/DISPLAY switch is released and depressed a second time, the date will be displayed as DAY-DATE in the MM5885. The DAY-DATE display will remain "ON" for 1.25 seconds ±0.125 seconds and turn "OFF" automatically if the SET/DISPLAY switch has been released. Holding the SET/DISPLAY switch past the display time out will maintain the DAY-DATE display until the SET/DISPLAY switch is released. In the MM5886, depressing the SET/DISPLAY a second time has no effect. To display DAY-DATE information in the MM5886, depress the DAY/DATE switch. The DAY-DATE display will remain "ON" for 1.25 seconds ±0.125 seconds. If the switch is still held in at the end of this time out, the display will remain until the DAY/DATE switch is released. "Time" may also be displayed in both the MM5885 and

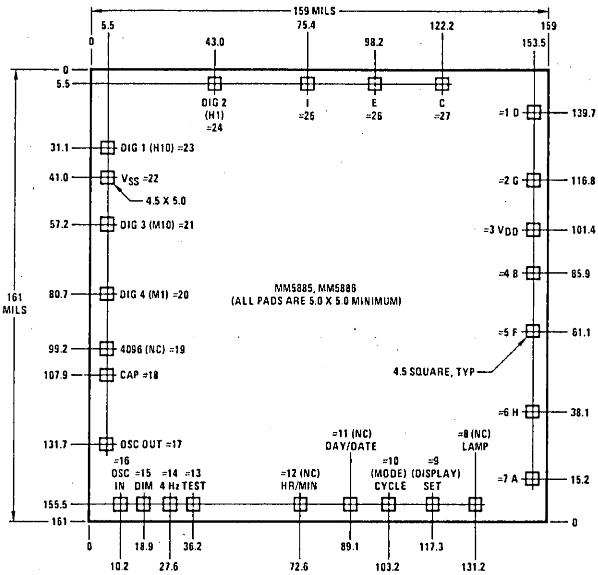


FIGURE 2. Pad Layout

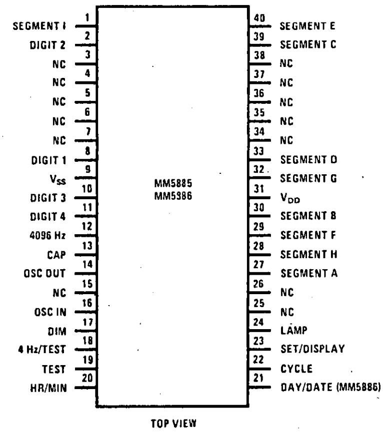


FIGURE 3. Connection Diagram

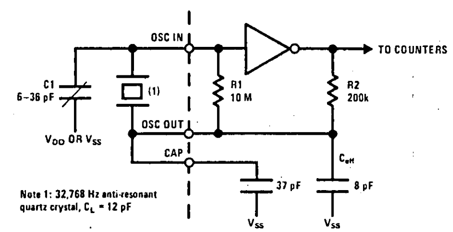


FIGURE 4(a). Oscillator RC Network for Anti-Resonant Quartz Crystals

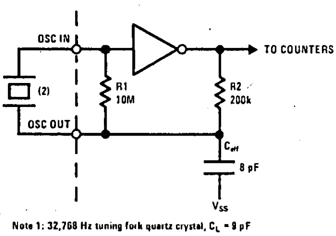


FIGURE 4(b). Oscillator RC Network for Tuning Fork Quartz Crystals

functional description (con't)

MM5886 by activating the HOUR/MINUTE input. The HOUR/MINUTE input is used with an inertial switch that is normally open. Closing the switch activates the HOUR/MINUTE display. This display will remain "ON" for 1.25 seconds ±0.125 seconds and then turn "OFF" automatically.

Time Setting: The setting sequence is controlled by a normally open switch connected to the Cycle input. Depressing the Cycle switch will advance the watch to the next set mode. *Figure 5* is a flow diagram showing the display and set functions for both the MM5885 and the MM5886.

Set Hour Mode: With the watch in the normal Run mode and the display "OFF," depressing the Cycle switch will put the watch into the Set Hour mode. In this mode, HOURS will be displayed in digit positions 1 and 2 followed by the colon. An A or a P will be displayed in digit position 4 to indicate AM or PM, respectively. Depressing the SET/DISPLAY switch will advance the Hours counter at a 2 Hz rate. If neither the SET/DISPLAY switch nor the Cycle switch are depressed for 5.25 seconds ±0.125 seconds, the watch will automatically return to the Run mode. Depressing the Cycle switch while in the Set Hours mode will advance the watch to the Set Minutes mode.

Set Minutes Mode: The Set Minutes mode will display minutes in digit positions 3 and 4 preceded by the colon. Depressing the SET/DISPLAY switch while still holding in the Cycle switch will enable the hold flag but will not allow advancement of the MINUTE counter. Depressing the SET/DISPLAY switch after the Cycle switch has been released resets and holds the SECOND counter, enables the hold flag, and advances the MINUTE counter at a 2 Hz rate. If neither switch is depressed for 5.25 seconds ±0.125 seconds while the watch is in the Set Minutes mode, the watch will automatically return to the Run mode if minutes have not been set or will jump to the Hold mode if minutes have been set. Depressing the Cycle switch while in the Set Minutes mode will advance the watch to the Set Day mode.

Set Day Mode: The Set Day mode will display DAY-OF-THE-WEEK in digit positions 1 and 2. Depressing the SET/DISPLAY switch while in the Set Day mode will advance the DAY counter at a 2 Hz rate. If neither switch has been depressed for 5.25 seconds ±0.125 seconds while in the Set Day mode, the watch will automatically return to the Run mode if the hold flag was not set or will jump to the Hold mode if the hold flag was set. Depressing the Cycle switch while in the Set Day mode will advance the watch to the Set Date mode.

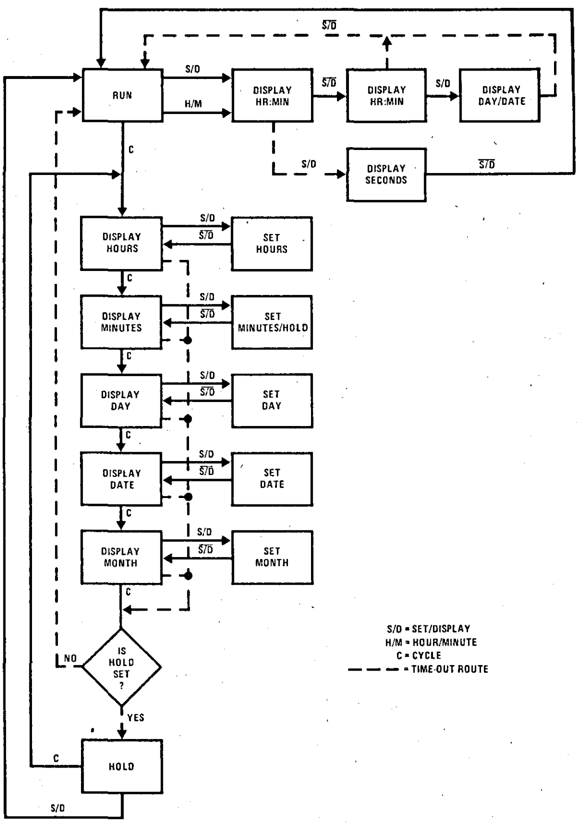


FIGURE 5(a). MM5885 Flow Diagram

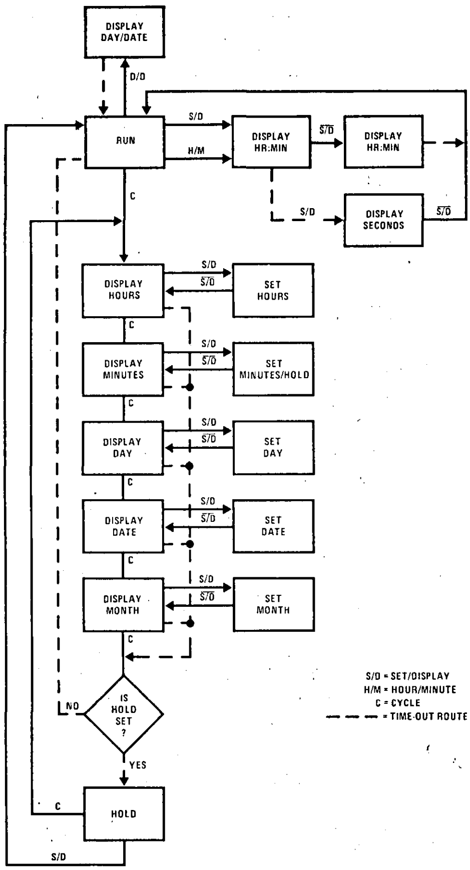


FIGURE 5(b). MM5886 Flow Diagram

functional description (con't)

Set Date Mode: The Set Date mode will display DATE in digit positions 3 and 4. Depressing the SET/DISPLAY switch while in the Set Date mode will advance the DATE counter at a 2 Hz rate. If neither the SET/DISPLAY nor the Cycle switches have been depressed for 5.25 seconds ±0.125 seconds while in the Set Date mode, the watch will automatically return to the Run Mode if the hold flag was not set or will jump to the Hold mode if the hold flag was set. Depressing the Cycle switch while in the Set Date mode will advance the watch to the Set Month mode.

Set Month Mode: The Set Month mode will display MONTH in digit positions 3 and 4 and an "M" in digit position 1. Depressing the SET/DISPLAY switch while in the Set Month mode will advance the MONTH counter at a 2 Hz rate. If neither the SET/DISPLAY nor the Cycle switches have been depressed for 5.25 seconds ±0.125 seconds while in the Set Month mode, the watch will automatically return to the Run mode if the hold flag was not set, or will advance to the Hold mode if the hold flag was set. Depressing the Cycle switch while in the Set Month mode will advance the watch to the Hold mode if the hold flag was set; otherwise, the watch will advance to the Run mode.

Hold Mode: In the Hold mode the SECOND counter is held at 00, and the HOUR-MINUTE display will blink "ON" for 0.25 seconds and "OFF" for 0.75 seconds. Depresssing the SET/DISPLAY switch will place the watch in the display HOUR/MINUTE mode for 1.25 seconds ±0.125 seconds. Depressing the Cycle switch while in the Hold mode will advance the watch to the Set Hour mode. There is no roll-over of the next higher counter while a counter is being set at a 2 Hz rate.

Month Counter: The MONTH counter provides "smart Date" but is only displayed during the Set Month mode. The DATE counter will count 28 days in February, 30 in April, June, September and November, and 31 in the remaining months.

Contact Bounce: Debounce circuitry is provided on the SET/DISPLAY, CYCLE, DAY/DATE and HOUR/MINUTE inputs to remove any logic uncertainty upon either closure or release of the switches. 20 ms debounce protection is provided for SET/DISPLAY, CYCLE and DAY/DATE inputs and 200 ms protection is provided for the HOUR/MINUTE input.

Display Multiplexing: The counter data selected to be displayed is time-division multiplexed to provide digit-sequential presentation to the LED display. This reduces

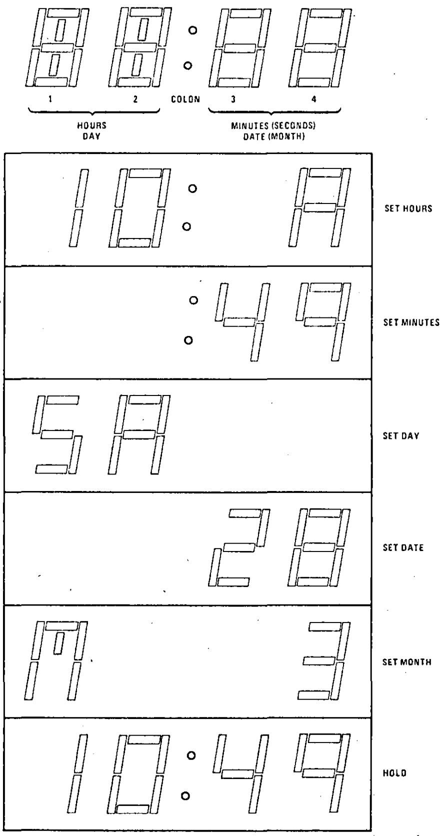


FIGURE 5(c). Set Display Font

functional description (con't)

the number of outputs required to drive the 4-digit display to thirteen (9-segment drivers and 4-digit drivers). The display font is shown in *Figure 6*. *Figure 8* is a schematic diagram of a typical LED watch using the MM5885 watch chip. The segment and digit drivers are designed to interface directly with the LED display. The four digits of the LED display are multiplexed with a 23% duty cycle, 1024 Hz signal during the display period. The digit drivers are disabled for 32μsec at the beginning of each digit enable time to allow the segment decoding circuitry adequate time to switch to the next digit's information. This eliminates the possibility of "ghosting" information between digits.

Dim Input: The Dim input is a 3-level input used to control the display intensity of the watch. This input has a pull-down to V_{SS} to hold it normally at a logical "0." In this condition, the display will normally be at maximum intensity. With the Dim input at 1/2 V_{DD} the display will be at approximately 1/2 of full intensity. Placing the input at V_{DD} will reduce the display intensity to approximately 1/8 of full intensity. *Figure 7* shows the switching threshold ranges for the 3-level Dim input.

Colon Output: Colon information is present on the "h" and "i" segment outputs during digit position 4.

Test Points: Four pads are provided for test purposes.

4096 Hz: This pad outputs a 4096 Hz signal that can be used for oscillator tuning.

4 Hz/Test Freq: This is an input/output pad under the control of the Test input pad. When "Test" is at a logical "0," the 4 Hz/Test Freq pad becomes an input and any frequency connected to it will replace the normal internal 4 Hz signal. This feature is provided to allow high speed functional testing of the watch system. When "Test" is open or at a logical "1," a 4 Hz output will appear on the 4 Hz/Test Freq pad.

Test: This pad is used as an input to control the 4 Hz/Test Freq pad. An internal pull-up resistor will normally hold "Test" at a logical "1." Changing the Test input from a logical "1" to a logical "0" will generate a reset pulse which will set the internal counters to 1 AM on Sunday, January the first. The watch is now in a known state for testing.

Lamp: When the Lamp input is at a logical "0," all segments of the display will be forced to an "ON" condition under control of the normal 23% duty cycle of the digit drivers. An internal pull-up resistor will normally hold the Lamp input at a logical "1."

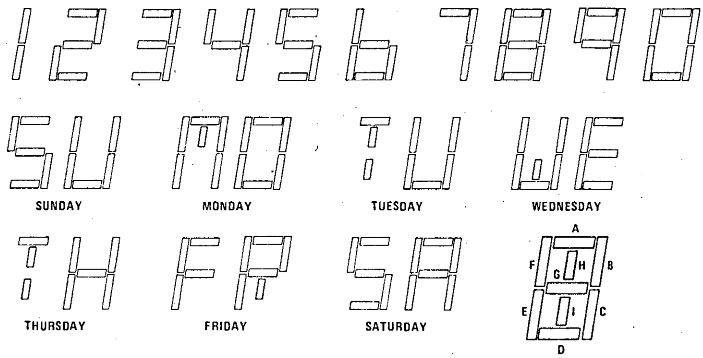
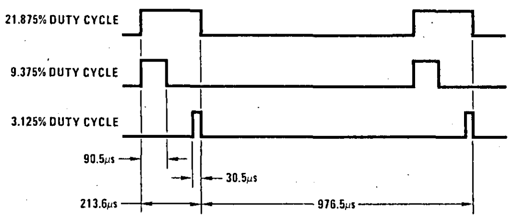


FIGURE 6. Display Font



V_{IN}	DISPLAY TIME/DIGIT	DISPLAY CONDITION
V_{DD}	3.125%	Low Ambient Light
$V_{DD} - 0.5V$	Threshold Region	
$V_{DD} - 1.1V$	9.375%	Moderate Ambient Light
$V_{SS} + 0.9V$	Threshold Region	
$V_{SS} + 0.3V$	21.875%	High Ambient Light
V_{SS}		

FIGURE 7. Dim Input Levels

functional description (con't)

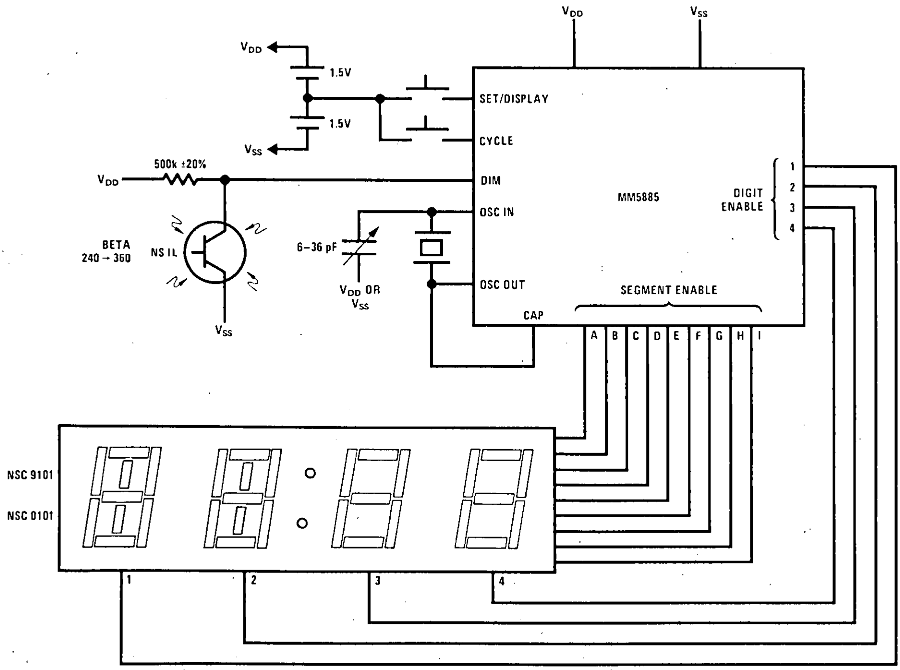


FIGURE 8(a). System Schematic for MM5885 LED Watch (Anti-Resonant Crystal)

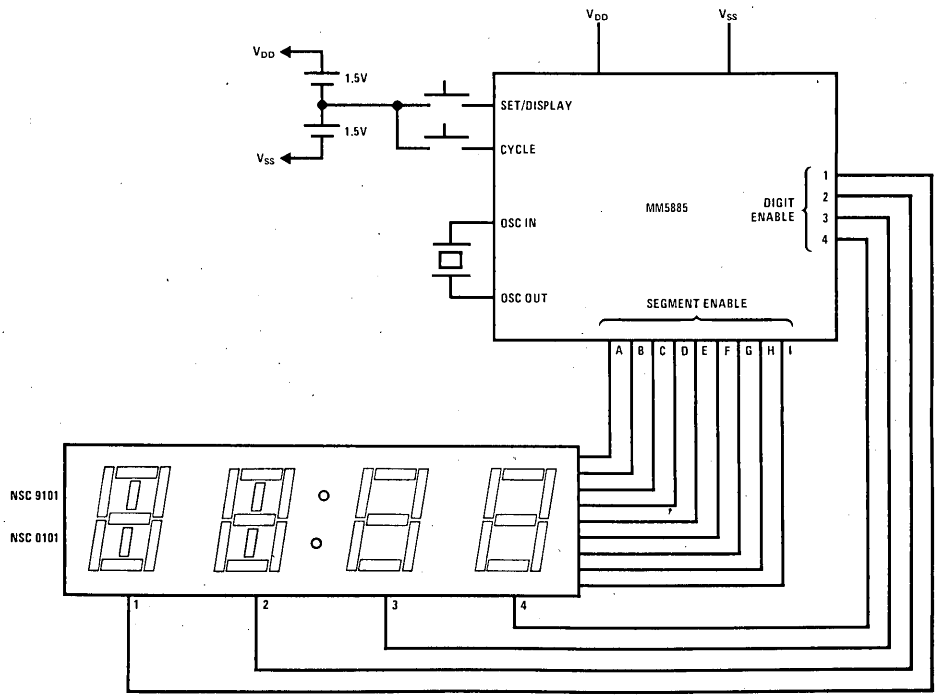


FIGURE 8(b). System Schematic for MM5885 LED Watch (Tuning Fork Crystal)

MM5890 LCD chronograph circuit

general description

The MM5890 is a low threshold voltage, ion implanted, metal-gate CMOS integrated circuit that provides all signals needed to drive an LCD watch of six digits plus nine information segments. The circuit time base is a 32.768 kHz crystal controlled oscillator. This base frequency is divided down to provide SECONDS, MINUTES, HOURS, DAY-OF-THE-WEEK, DATE and MONTH information in the normal watch mode with separate minutes, seconds, and hundredths of a second available in the stopwatch mode. Time display can be bonded to either 12 or 24 hour format. 51 phase controlled outputs are provided for direct drive of the display. The 32 Hz output is used as the backplane drive for normal operation and as a test frequency input during testing. The MM5890 operates on a single 1.4V to 1.6V supply. An on-chip voltage multiplier is used to provide 2 or 3 times the battery voltage to drive the display. The MM5890 is available in die form suitable for hybrid assembly or mounted on a 68-lead dual-in-line PCB assembly for test and evaluation purposes.

features

- Direct continuous LCD drive capability
- 32.768 kHz crystal controlled operation
- Single 1.5V battery operation
- Voltage multiplier
- Low power dissipation
- 6-digit plus 9 information segment display
- Colon display
- 12 or 24 hour format
- 4 year calendar
- Stopwatch with split operation
- 6-function watch
- 4 button sequential operation

block diagram

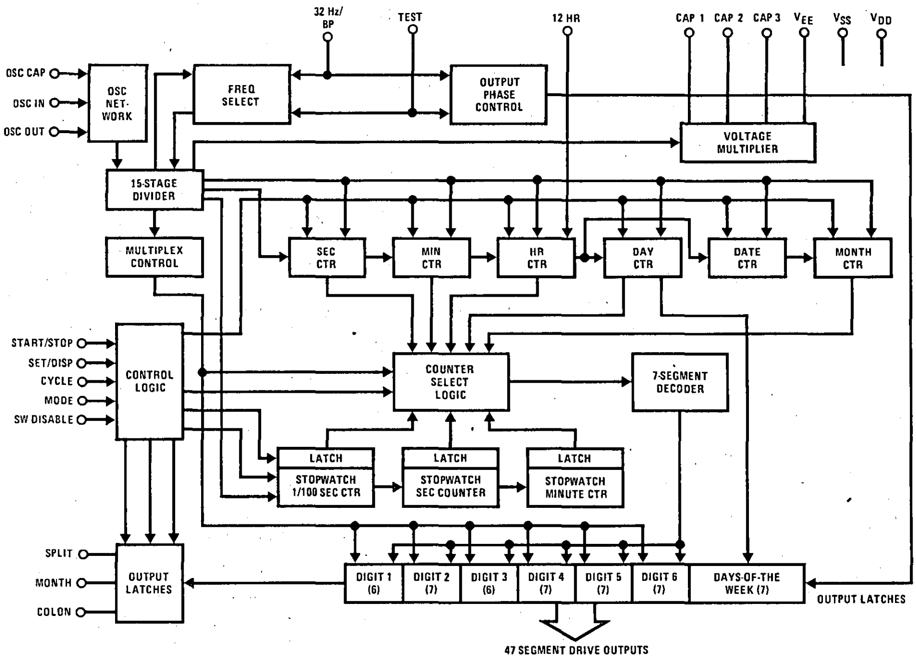


FIGURE 1.

absolute maximum ratings

Voltage at OSC IN, OSC OUT, 12 HR. SW Disable, Double, Triple Set/Display, Cycle, Mode, Start/Stop	V_{DD} + 0.3V to V_{SS} – 0.3V
Voltage at Any Other Pin	V_{DD} + 0.3V to V_{EE} – 0.3V
Operating Temperature Range	–5°C to +70°C
Storage Temperature Range	–25°C to +85°C
$V_{DD} - V_{EE}$	6.5V
$V_{DD} - V_{SS}$	3.0V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, $V_{DD} - V_{SS}$ = 1.5V, $V_{DD} - V_{EE}$ = 4.5V, V_{DD} @ Ground unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	T_A = 25°C, (Note 1)	1.40			V
Oscillator Sustaining Voltage	T_A = –5°C, (Note 1)	1.30			V
Input Voltage Levels					
Set/Display, Cycle					
Start/Stop, Mode					
Logical "1"		V_{DD}–0.25			V
Logical "0"	Internal Pull-Down to V_{SS}		Open		V
Test					
Logical "1"		V_{DD}–0.25			V
Logical "0"	Internal Pull-Down to V_{EE}		Open		V
32 Hz/Backplane	Test Input = V_{DD}				
Logical "1"		V_{DD}–0.25			V
Logical "0"				V_{EE}+0.25	V
12 HR, SW Disable					
Logical "1"		V_{DD}–0.25			V
Logical "0"				V_{SS}+0.25	V
Input Current Levels					
Set/Display, Cycle, Start/Stop, Mode, Test	V_{IN} = V_{DD}		30	50	μA
Input Capacitance	f = 1 MHz, V_{IN} = 0V, All Other Pads Gnd				
OSC OUT		8			pF
OSC Cap		37			pF
All Others				5	pF
Output Current Levels					
Segment Drivers					
Logical "1" Source	V_{OUT} = V_{DD} – 0.2V, ($V_{DD} - V_{EE}$ = 3V)	2.0			μA
Logical "0" Sink	V_{OUT} = V_{EE} + 0.2V, ($V_{DD} - V_{EE}$ = 3V)	2.0			μA
BP/32 Hz Output					
Logical "1" Source	V_{OUT} = V_{DD} – 0.2V, ($V_{DD} - V_{EE}$ = 3V)	200			μA
Logical "0" Sink	V_{OUT} = V_{EE} + 0.2V, ($V_{DD} - V_{EE}$ = 3V)	200			μA
Output Current Levels					
Double, Triple					
Logical "1," Source	V_{OUT} = V_{DD} – 0.25V, Phase 2 < 1 ms	7.5			μA
Logical "0," Sink	V_{OUT} = V_{SS} + 0.25V, Phase 3	35.0			μA

electrical characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Cap 1					
Logical "1," Source	$V_{OUT} = V_{DD} - 0.25V$, Phase 1	7.5			µA
Logical "0," Sink	$V_{OUT} = V_{SS} + 0.25V$, Phase 2	20.0			µA
Leakage	$V_{OUT} = V_{DD} - 3.0V$, Phase 3			0.6	µA
Cap 2					
Logical "0," Sink	$V_{OUT} = V_{SS} + 0.25V$, Phase 1	35.0			µA
Leakage	$V_{OUT} = V_{EE} + 1.5V$, Phase 2			0.6	µA
V_{EE}					
Logical "0," Sink	Cap 2 = $V_{DD} - 4.2V$, Phase 3 $V_{OUT} = V_{DD} - 3.95V$	250.0			µA
Input Debounce	Test Input Open				
Cycle, Mode	Osc. In Freq = 32.768 kHz	120		260	ms
Set ("0" to "1" Transition)		120		260	ms
Set ("1" to "0" Transition)		60		130	ms
Start/Stop		60		130	ms
Supply Current (I_{DD})	$T_A = 25°C$, $I_{EE} = 1\ \mu A$,				
Doubler Operation	f = 32,768 Hz, $V_{DD} - V_{SS}$ =		3.0	6.0	µA
Tripler Operation	1.6V, (Note 1)		6.0	8.0	µA
Supply Voltage (V_{EE})	$T_A = 25°C$, C = 0.047 µF,				
Doubler Operation	$I_{EE} = 1\ \mu A$, f = 32,768 Hz,	2.5			V
Tripler Operation	$V_{DD} - V_{SS} = 1.5V$, *(Figure 9)*, (Note 2)	3.8			V

Note 1: In oscillator network shown in *Figure 4*.
Note 2: External capacitors connected as shown in *Figure 9*.

functional description

A block diagram of the MM5890 chronograph chip is shown in *Figure 1* with the chip pad layout shown in *Figure 2*.

Time Base: The precision time base of the chronograph is provided by connecting a crystal controlled RC network to the on-chip CMOS inverter/amplifier as shown in *Figure 3*. For proper operation the network should be tuned to 32.768 kHz. Resistor R1 is used to bias the on-chip inverter for class A amplifier operation. Resistor R2 is used to: a) reduce the voltage sensitivity of the network; b) limit the power dissipation in the quartz crystal; and c) provide added phase shift for good start-up and low voltage operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. The network shown in *Figure 4* provides greater than 100 ppm tuning range when used with standard X-Y flexure quartz crystals trimmed for C_L = 13 pF. Tuning to better than 2 ppm is easily obtainable. The 32 Hz output can be used to monitor the oscillator frequency during initial trimming without disturbing the network itself.

DISPLAY CONTROL

Watch Mode: When used as a watch, the MM5890 has two display modes. The first mode displays the HOUR in digit positions 1 and 2, the MINUTE in digit positions 3 and 4, the DATE in digit positions 5 and 6 and the DAY-OF-THE-WEEK *(Figure 5)*. The second mode will display SECONDS in digit positions 5 and 6 instead of the DATE. Depressing the Set/Display switch will change the watch from one mode to the other.

Leading zero values of the DATE and HOUR are blanked. The circuit contains a 4 year calendar which will automatically reset the Date Counter to 1 and advance the Month Counter at the end of each month (except for February in Leap Year). The character display font is shown in *Figure 6*.

functional description (Continued)

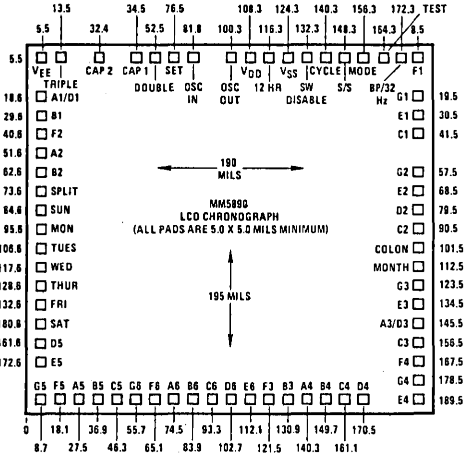


FIGURE 2. Chip Pad Layout

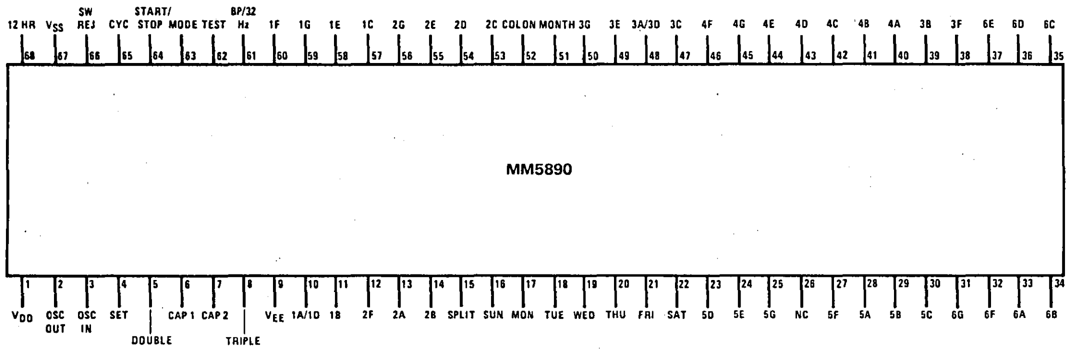


FIGURE 3. Connection Diagram

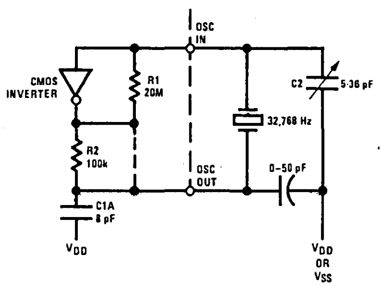


FIGURE 4. Crystal Oscillator Network

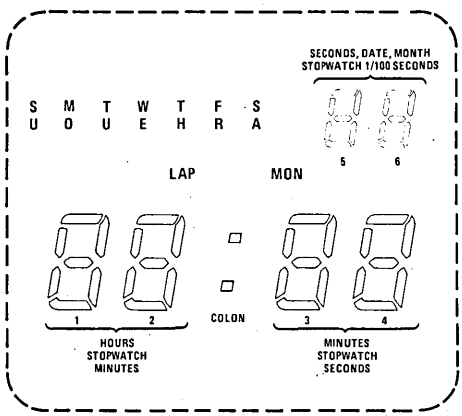


FIGURE 5. Display Format

functional description (Continued)

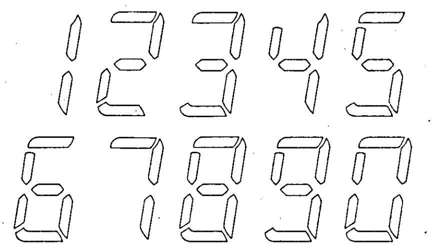


FIGURE 6. Display Font

Stopwatch Mode: Depressing the Mode Switch will switch the watch from the normal watch mode to the stopwatch mode. When used as a stopwatch, the MM5890 displays the stopwatch MINUTE in digit positions 1 and 2, the stopwatch SECOND in digit positions 3 and 4, and the stopwatch 1/100 SECOND in digit positions 5 and 6. Depressing the Start/Stop Switch will either start the stopwatch if it is not counting or stop it if it is counting.

Depressing the Set switch will activate the Split Time mode. In this mode the watch will freeze the time showing on the display at the instant the Set switch is depressed. The stopwatch continues counting and the colon will begin blinking at a 1 Hz rate to indicate the continuing count. Depressing the Start/Stop switch will stop or start the stopwatch counters. The colon will remain "ON" in the Split Time mode if the stopwatch is not counting. The Split indicator (refer to *Figure 5*) will be "ON" during the Split Time mode. Depressing the Set switch while the watch is in the Split Time mode will return the accumulated time in the stopwatch to the display and the Split indicator will turn "OFF."

Depressing the Set switch while the stopwatch is not running and is not in the Split Time mode will clear the stopwatch counters to a zero count. Depressing the Mode switch while the stopwatch mode is active will transfer the watch to the normal watch mode. This transfer will not affect the stopwatch function and the stopwatch will continue performing the same function until the stopwatch mode is again activated with the mode switch.

Setting Control: A normally open switch connected to the Cycle input is used in conjunction with the Set/Display input to set the MONTH, DATE, DAY-OF-THE-WEEK, HOUR, MINUTE and synchronize the SECOND information.

HOUR: With the watch in the watch mode depressing the Cycle switch will put the watch in the Set Hour mode. The HOUR information will be in digit positions 1 and 2 with either an A or a P in digit position 4 indicating AM or PM. While in this mode, depressing the Set/Display switch will cause the HOUR counter to advance at a 1 Hz rate until the switch is released.

MINUTE: Depressing the Cycle switch while the watch is in the Set Hour mode will put the watch in the Set Minute mode with the MINUTE information displayed in digit positions 3 and 4. Depressing the Set/Display switch will advance the MINUTE counter at a 1 Hz rate and activate the Hold mode.

DAY-OF-THE-WEEK: Depressing the Cycle switch while the watch is in the Set Minute mode will place it in the Set Day mode with the DAY-OF-THE-WEEK displayed. Depressing the Set/Display switch will change the DAY-OF-THE-WEEK at a 1 Hz rate until the switch is released.

DATE: Depressing the Cycle switch while the watch is in the Set Day mode will advance it to the Set Date mode with the DATE (day of the month) displayed in digit positions 5 and 6. Depressing the Set/Display switch while the watch is in the Set Date mode will advance the DATE at a 1 Hz rate until the switch is released.

Month: Depressing the Cycle switch while the watch is in the Set Date mode will advance it to the Set Month mode with the Month displayed in digit positions 5 and 6 and the Month indicator "ON." Depressing the Set/Display switch while in this mode will advance the Month counter at a 1 Hz rate until the switch is released.

Depressing the Cycle switch while the watch is in the Set Month Mode will place the watch in the normal display mode with HOUR, MINUTE, DATE, and DAY-OF-THE-WEEK information displayed.

Hold: If the Hold mode was activated while in the Set Minute mode the colon will not blink in the normal time display but remain on continuously. The SECOND counter is held at 00, forcing the watch to remain at the displayed time. Depressing the Set/Display switch will switch the watch to the alternate time display mode (HOUR, MINUTE, SECOND, and DAY-OF-THE-WEEK) and release the SECOND counter allowing normal operation to begin. While in any of the Set modes, advancing the selected counter will not cause a roll-over of higher state counters. For example, advancing the HOUR counter from 11 PM to 12 AM will not cause the DATE or DAY-OF-THE-WEEK counters to advance.

A control state diagram for the MM5890 is provided in *Figure 7*.

Contact Bounce: Debounce circuitry is provided on the Set/Display, Cycle, Start/Stop, and Mode inputs to remove any logic uncertainty upon either closure or release of switches provided switch bounce settles within 120 ms (Set/Display release bounce must settle within 60 ms.)

12/24 Hour Option: 12/24 hour operation is controlled by the logical state of the 12 HR pad. Connecting the 12 HR pad to a logical "1" will cause the watch to operate in the 12 hour mode while connecting the 12 HR pad to a logical "0" will cause the watch to operate in the 24 hour mode.

functional description (Continued)

Segment Outputs: The Segment outputs are designed to drive field-effect liquid crystal displays. Each display segment has its own output which supplies the proper 32 Hz drive signal. By definition, the segment is "OFF" when its drive signal is in phase with the Back Plane drive signal (BP/32 Hz) and the segment is "ON" when the drive signal is 180° out of phase with the Back Plane drive signal (refer to *Figure 8*).

BP/32 Hz: This input/output pad is under control of the Test input. When Test is open or at a logical "0," a 32 Hz signal is provided at BP/32 Hz which is used to drive the backplane of the LCD unit or to monitor the oscillator frequency. If Test is at a logical "1," the BP/32 Hz pad is converted into an input and any frequency connected to it will replace the normal internal 32 Hz signal. This feature allows high speed testing of all timekeeping and stopwatch counters.

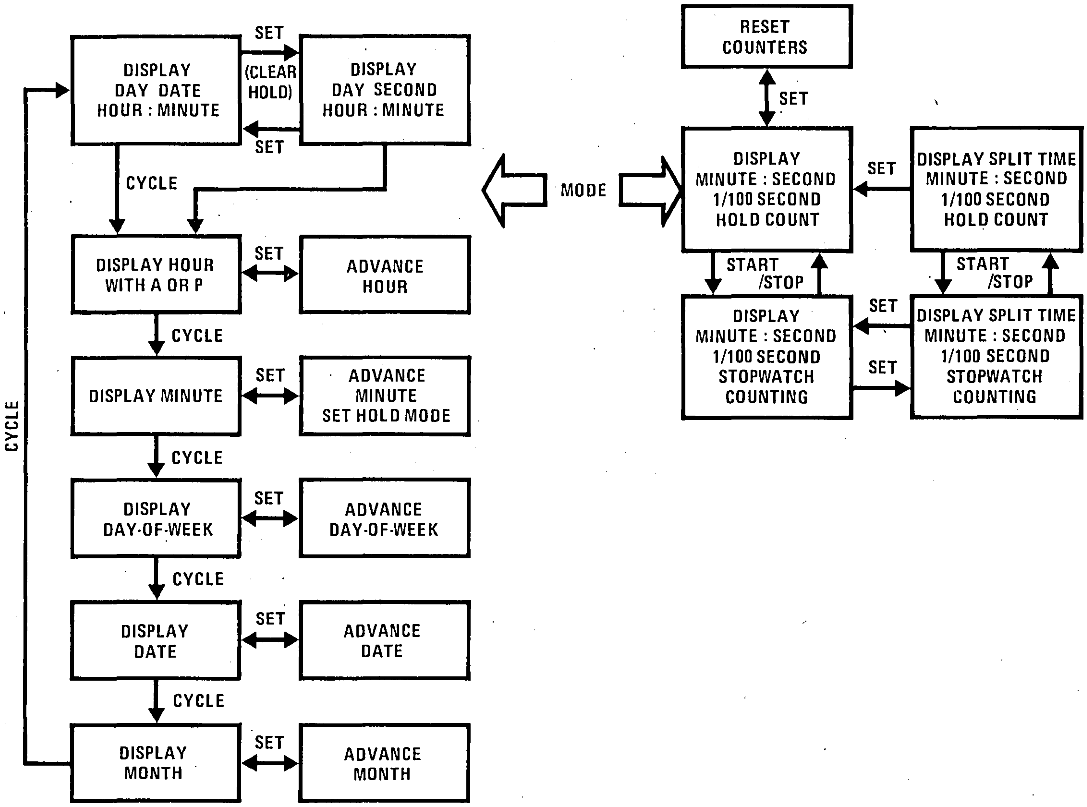


FIGURE 7. Control State Diagram

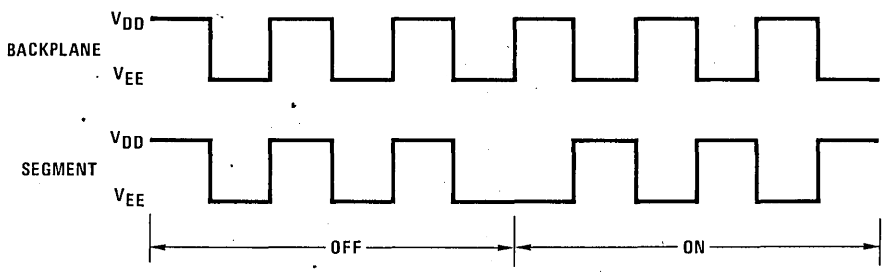


FIGURE 8. Phase Drive Signals

functional description (Continued)

Test: This input is used to control the BP/32 Hz pad as described above. When Test is at a logical "1" the phase-control is disconnected from the segment drive outputs and the segment information is referenced to a logical "0" backplane. Switching the Test input from a logical "0" to a logical "1" generates a reset pulse that will reset the counters to Sunday, 1 AM on January the first. All stopwatch counters will be set to 00 and the watch will be placed in the normal time display mode.

SW Disable: This input is used to control accessability to the stopwatch functions. If SW Disable is at a logical "0" the Mode switch can be used to activate the stopwatch functions. If SW Disable is at a logical "1" the Mode switch is inoperative and the stopwatch functions are locked out.

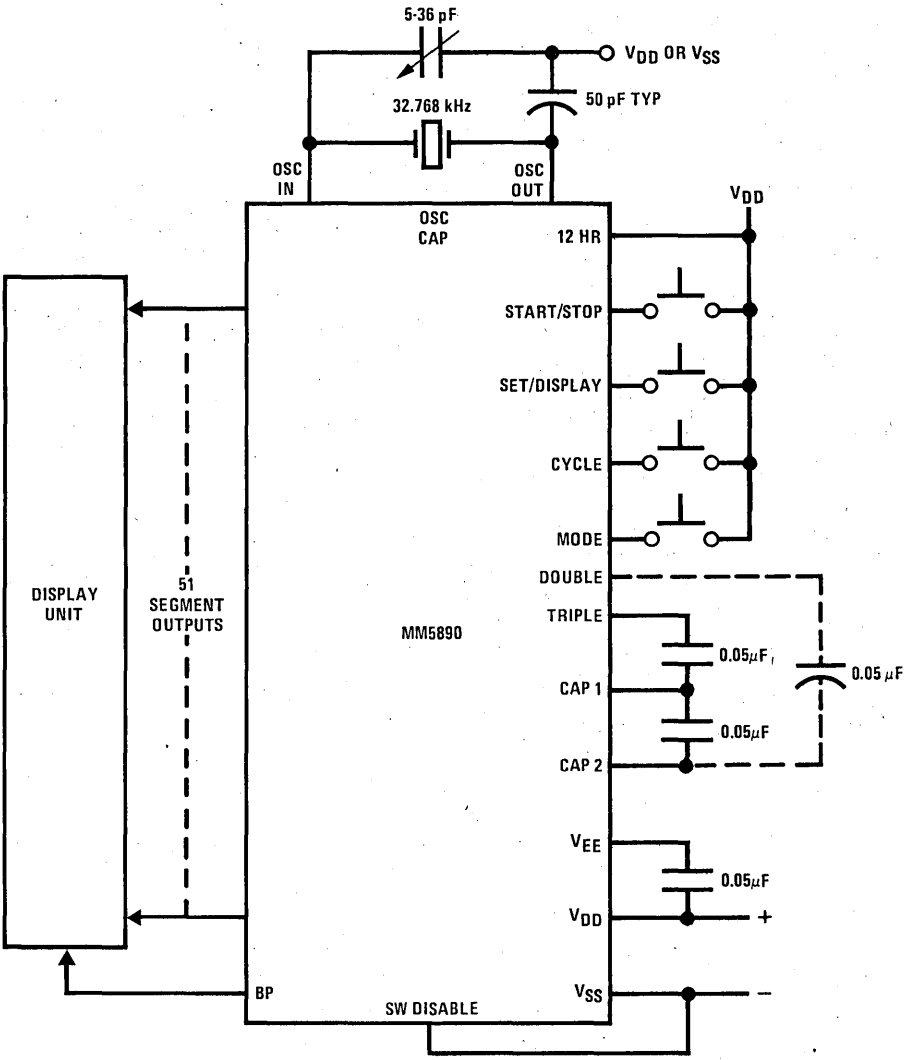


FIGURE 9. Typical Application

MM58104 direct drive LED watch

general description

The MM58104 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that provides or controls all signals needed for a 3 1/2 digit 3-function or a 4-digit 4-function LED watch. The display format is 12 hours. The circuit time base is a 32,768 Hz crystal controlled oscillator. This time base frequency is successively divided to provide drive signals for a multiplexed 7-segment LED display. Upon demand MM58104 will display HOURS-MINUTES or SECONDS when it is used as a 3-function watch and will also display DATE when it is used as a 4-function watch. The outputs will directly drive a 7-segment LED display. The device operates from a single 2.4V to 4.0V supply. The MM58104 is available as unpackaged die suitable for hybrid assembly or in 40-lead dual-in-line packages for evaluation purposes.

features

- 32,768 Hz crystal control oscillator
- Single 3V supply
- Low power dissipation (15μW typical)
- 3 1/2 digit (3-function) or 4-digit (4-function) option
- 12 hour display format
- Simple display/set controls
- Direct drive outputs for LED's
- Display brightness control
- On-chip oscillator bias network

functional description

A block diagram of the MM58104 digital watch chip is shown in *Figure 1.* A chip pad layout is shown in *Figure 2* and package connection diagram in *Figure 3.*

block diagram

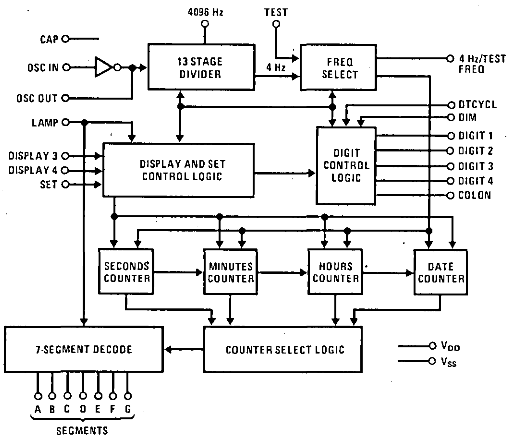


FIGURE 1.

chip pad layout

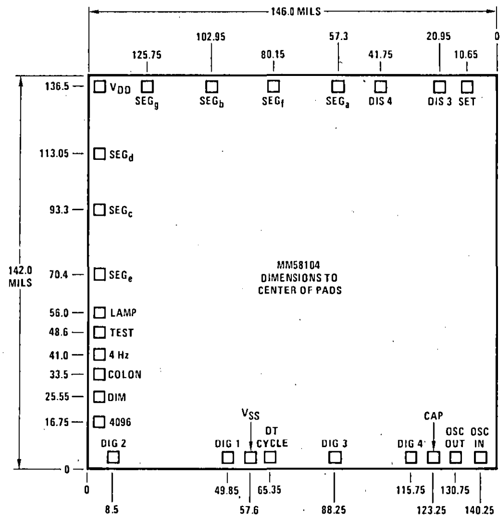


FIGURE 2.

connection diagram (Top View)

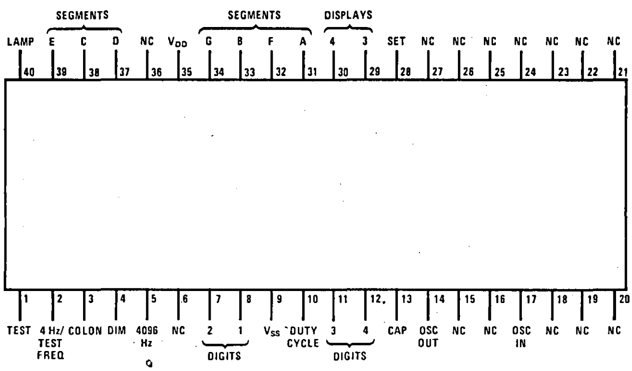


FIGURE 3.

7

absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	−5°C to +70°C
Storage Temperature Range	−25°C to +85°C
$V_{DD} - V_{SS}$	5V max
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = GND, $2.4 \le V_{DD} \le 4.0V$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	$T_A = 25°C$	2.7			V
Input Voltage Levels @ Display 3, Display 4, Set	$V_{DD} = 3.0V$				
Logical "1"		$1/2\ V_{DD}$		V_{DD}	V
Logical "0"	300 kΩ Internal Pull-Down to V_{SS}		Open		
Input Voltage Levels @ 4 Hz/ Test Freq, Dtcycl	$V_{DD} = 3.0V$				
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels @ Lamp, Test	$V_{DD} = 3.0V$				
Logical "1"	1 MΩ Internal Pull-Up to V_{DD}		Open		
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Current @ Display 3, Display 4, Set	$V_{IN} = V_{DD}$, Sink Only, $V_{DD} = 3.0V$		30	50	μA
Input Current @ Lamp and Test	$V_{IN} = V_{SS}$, Source Only, $V_{DD} = 3.0V$		30	50	μA
Output Current Levels @ Segment Drivers	$V_{DD} = 2.7V$				
"ON" Source	$V_{OUT} = V_{DD} - 0.5V$	7	10	15	mA
"OFF"	$V_{OUT} = V_{SS} + 1.1V$			50	μA
Output Current Levels @ Digit Drivers	$V_{DD} = 2.7V$				
"ON" Sink	$V_{OUT} = V_{SS} + 0.6V$	50	70		mA
"OFF"	$V_{OUT} = 2.0V$, All Digit Drivers Tied in Parallel			2	μA
Output Current Level @ COLON	$V_{DD} = 2.7V$				
"ON" Sink	$V_{OUT} = V_{SS} + 0.7V$		6		mA
"OFF"	$V_{OUT} = V_{DD} - 1.6V$			0.5	μA
Output Current Levels @ 4096 Hz, 4 Hz/Test Freq.	$V_{DD} = 3.0V$				
Logical "1," Source	$V_{OUT} = V_{DD} - 0.5V$	10			μA
Logical "0," Sink	$V_{OUT} = V_{SS} + 0.5V$	10			μA
Supply Current (I_{DD})	f = 32,768 Hz, $T_A = 25°C$, $V_{DD} = 3.0V$, Unused Inputs Open, Outputs Open		5	10	μA
Supply Current (I_{DD})	$T_A = 25°C$, V_{SS}, OSC IN & Dtcycl @ GND, $V_{DD} = 3.0V$, Unused Inputs Open, Outputs Open		0.05	1	μA
Input Capacitance	f = 1.0 MHz				
OSC OUT	$V_{IN} = 0.0V$		8		pF
CAP	All Other Pads GND		37		pF
All Others				5	pF
Input Voltage Level @ DIM	$V_{DD} = 3.0V$				
Positive-Going Threshold (V_{T+})			1.5		V
Negative-Going Threshold (V_{T-})			1.0		V
$V_{T+} - V_{T-}$ Hysteresis			0.5		V
Input Current @ DIM	$V_{IN} = V_{SS}$, $V_{DD} = 3.0V$, Source Only			0.3	μA

functional description (con't)

Time Base: The precision time base of the watch is provided by the interconnection of a 32,768 Hz quartz crystal and the RC network shown in *Figure 4* together with the CMOS inverter/amplifier provided between the oscillator in and oscillator out terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Resistor R2 is required in order to (a) reduce the voltage sensitivity of the network; (b) limit the power dissipation in the quartz crystal; and (c) provide added phase shift for good start-up and low voltage circuit performance. Capacitors C1, C2 and C3 provide the parallel load capacitance required for precise tuning of the quartz crystal. The RC network except the trim capacitor C3 is integrated on-chip.

The network shown provides > 100 ppm tuning range when used with standard X-Y flexure quartz crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

The 4096 Hz output or 4 Hz output can be used to monitor the oscillator frequency during initial tuning without disturbing the network itself.

Display Multiplexing: Outputs from each counter are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 28 leads to interconnect a four digit (7 segments/digit) watch, only 11 output leads are required. The character display font and segment identification is shown in *Figure 5*. *Figure 6* shows the interconnection of a LED watch system. The 4-digit outputs, colon output and the 7-segment outputs of the MM58104 are designed to interface directly with the NSC0101 LED display. The four digits of the LED display are multiplexed with a 25% duty cycle, 1024 Hz signal during Display. The digit drivers are turned off by the internally generated inter-digit blanking signal during the change of digits to allow the segments to change without "ghosting" of the Display. When MM58104 is used as shown in the typical application of *Figure 6,* the segment on currents are typically 9 mA. The NSC0101 LED Display gives excellent brightness under these drive conditions.

The switch inputs "Display 3" and "Display 4" of the MM58104 are to be used for 3 and 4-function LED watches, respectively. However, "Display 3" can be connected to an inertial switch for HOURS-MINUTES Display in a 4-function watch. In subsequent paragraphs, the term "Display" will take the place of "Display 3" and/or "Display 4," unless otherwise specified.

Time Display: The DATE and HOUR-MINUTES/SECONDS displays are controlled by a normally open switch connected to "Display" input as shown in *Figure 6.* DATE or HOUR is displayed in digit positions 1 and 2. MINUTE or SECOND is displayed in digit positions 3 and 4. Colon output will be "ON" except when the Display involves DATE. The two colon dots are to be connected in parallel with their anodes to V_{DD} and cathodes to the "COLON" output.

Closure of the "Display" switch will cause HOUR-MINUTES to be displayed for 1.25 ±0.125 seconds.

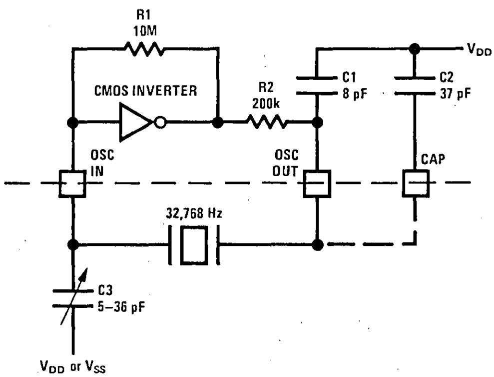


FIGURE 4. Crystal Oscillator Network

functional description (con't)

Holding the "Display" switch closed after the time-out of HOUR-MINUTES display will cause SECONDS to be displayed until the "Display" switch is open. SECONDS will blink while displayed. Each value is visible for, 0.25 second and blank for 0.75 second. HOURS digits can display values 1–12 with an AM indicator, which is the F segment of digit 1. Leading zero values of hours are blanked. MINUTES or SECONDS digits can display values from 00 to 59. All zero values of minutes or seconds are displayed.

Closure of the "Display 4" switch twice before the time-out of HOURS-MINUTES display will cause DATE to be displayed for 1.25 ±0.125 seconds. Holding the "Display" switch closed will continue DATE display until the switch is open. Date digits can display values from 1 to 31. Leading zero values of Date are blanked.

Time Setting: A normally open switch connected to the "Set" input is used in conjunction with the "Display" switch to set date, hours, minutes and synchronize seconds.

DATE: Closure of the "Display 4" switch twice and holding it closed will cause DATE to be displayed continuously. Closure of the "Set" switch will then advance DATE at a 2 Hz rate until the "Set" or both switches are opened. Seconds, Minutes and Hours counters continue normal counting during this condition.

HOURS: Closure of the "Set" switch will cause HOURS-MINUTES to be displayed and will advance HOURS at a 2 Hz rate until the "Set" switch is opened. Seconds and Minutes counters continue normal counting during this condition.

MINUTES: Closure of both "Display" and "Set" switches will cause HOURS-MINUTES to be displayed and will advance MINUTES at a 2 Hz rate after both switches have been closed for 0.75 to 1.0 seconds. When the minutes count is correct, opening the "Set" switch while keeping the "Display" switch closed will cause HOURS-MINUTES to be displayed and Hold the watch. HOURS-MINUTES will blink while displayed, visible for 0.25 second and blank for 0.75 second. The seconds counter is reset and held at 00 during Minutes setting or during the Hold Mode. All counters resume their normal counting when both "Set" and "Display" switches are opened. With the "Display" switch closed,

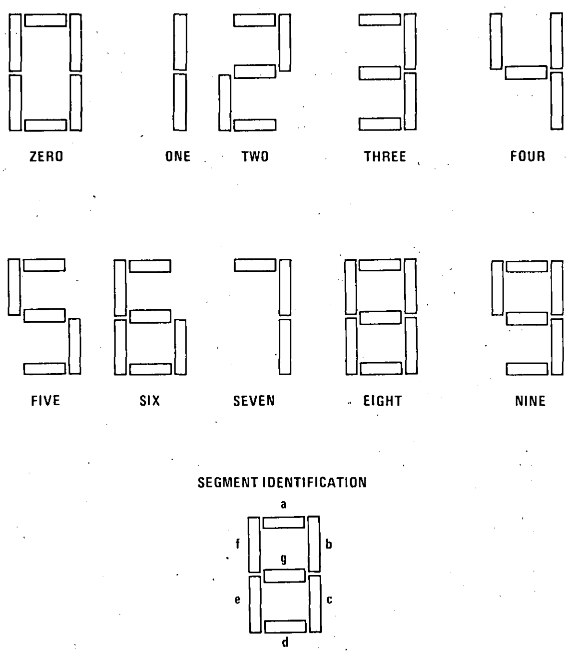


FIGURE 5. Character Display Font

functional description (con't)

a closure of the "Set" switch for less than 0.75 second will reset the seconds counter to 00 without advancing the minutes.

There is no roll-over of the higher counters while the lower time counters are being set. For example, while setting Minutes a 59 to 00 transition will not advance the Hours counter.

Contact Bounce: Debounce circuitry is provided on the "Display" and "Set" inputs to remove any logic uncertainty upon either closure or release of switches provided switch bounce settles within 20 ms.

Display Brightness Control: The display brightness is a function of digit on-time which is a fraction of the digit multiplexers. The digit on-time varies from 1/8 to 7/8 of the digit multiplexer in steps depending on the logical levels of both "DIM" and "DTCYCL" inputs as shown in Table I. The "DIM" input has an internal pull-up resistor which will hold the open input at a logical "1." The logical levels at the "DIM" input can be established by a network as shown in *Figure 6.*

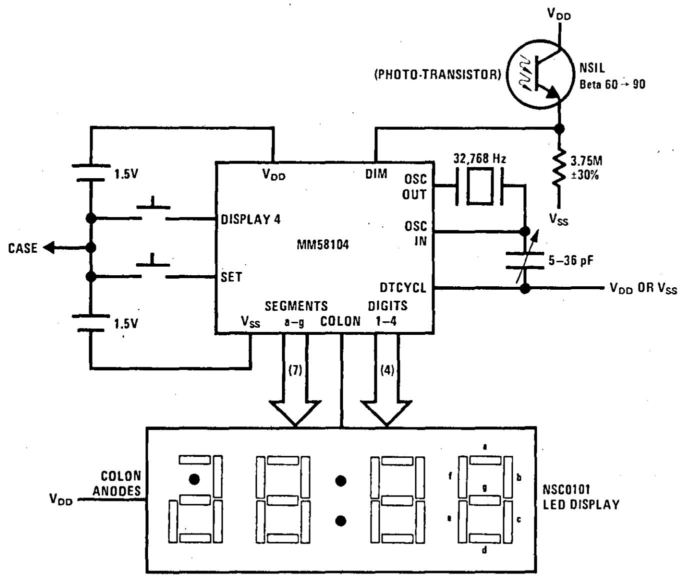
Test Points: Four pads are provided for test purposes.

4096 Hz: is an output. A 4096 Hz symmetrical signal is brought out for oscillator tuning.

4 Hz/TEST FREQ: is an input/output under the control of "TEST." When "TEST" is open or at a logical "1," a 4 Hz signal will appear on the "4 Hz/TEST FREQ pad." If "TEST" is at a logical "0," the "4 Hz/TEST FREQ pad" becomes an input and any frequency connected to it will replace the normal internal 4 Hz signal. This feature is provided to allow high speed functional testing of the watch system.

TEST: is an input. It is used to control "4 Hz/TEST FREQ" as described above. An internal pull-up resistor will normally hold the "TEST" input to a logical "1."

LAMP: is an input. When "LAMP" is at logical "0," all segments will be forced to an "ON" condition under control of the normal 25% duty cycle of the digit drivers. An internal pull-up resistor will normally hold the "LAMP" input to a logical "1."



The DOT in the first digit is tied to segment bus "F."
It is used as the AM indicator.

FIGURE 6. Typical Application of MM58104 in LED Digital Watch System

TABLE I. Display Brightness Control

DTCYCL	DIM	DIGIT ON-TIME (Fraction of Digit Multiplexer)
1	1	7/8
1	0	2/8
0	1	4/8
0	0	1/8

Watches

MM58115 digitally tuned direct drive 6-function LED watch

general description

The MM58115 is a low threshold voltage, ion-implanted, metal-gate CMOS integrated circuit that provides or controls all signals needed for a 4-digit, 6-function LED watch. The display format is 12 hours. The circuit time base is a 32,768 Hz crystal controlled oscillator. This time base frequency is successively divided to provide drive signals for a multiplexed 9-segment, alphanumeric LED display of HOURS-MINUTES, DAY-DATE, MONTH-DATE or SECONDS upon demand. A month counter is provided to control the count sequence of the Date counter. Inputs are also provided to digitally tune the time base (i.e., no tuner capacitor is required). The MM58115 uses one button for display purposes. Both segment and digit outputs can be directly interfaced with 100 mil LED displays of the NSC9101 type. Special circuitry is included to provide uniform digit-to-digit brightness. The device operates from a single 2.4V to 4V supply. The MM58115 is available as unpackaged die suitable for hybrid assembly or in a 40-lead dual-in-line package for evaluation purposes.

features

- No external parts except the battery, LED display and crystal
- Single button display control
- Direct drive outputs
- Digital tune network
- Uniform display brightness
- 32,768 Hz crystal controlled operation
- Single 3V supply
- Low power dissipation (10μW typ)
- Seconds, Minutes, Hours, Day-of-Week, Date and Month operation
- 4 year calendar
- 4-digit, 6-function, 12-hour display format
- Simple display/set controls
- Alphanumeric display
- Display brightness control
- AM/PM indication during set hours
- Month indication during set month
- Test features

block diagram

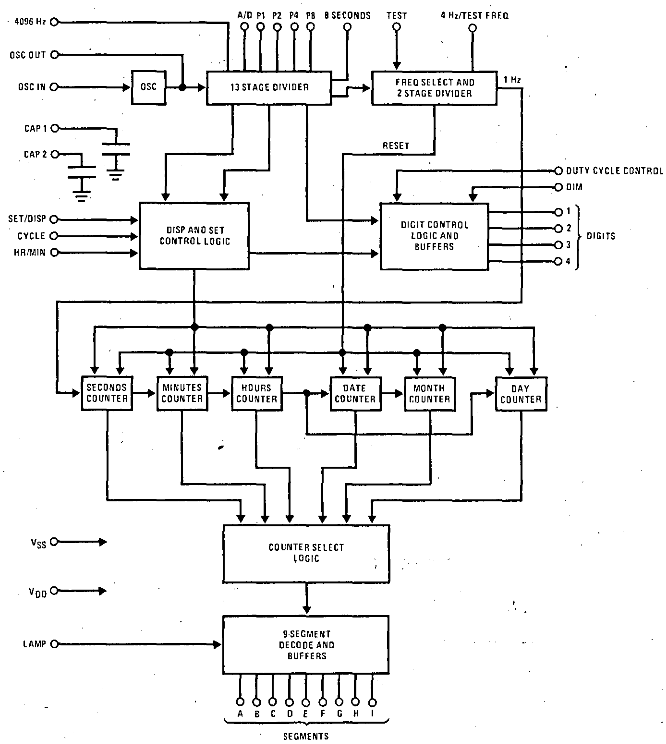


FIGURE 1.

absolute maximum ratings

Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range	−5°C to +70°C
Storage Temperature Range	−25°C to +85°C
$V_{DD} - V_{SS}$	5V max
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = Gnd, $2.4 \leq V_{DD} \leq 4V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	$T_A = 25°C$	2.7			V
Input Voltage Levels at Cycle, Set/Display, Hour/Min					
Logical "1"	100 kΩ Internal Pull-Down	$1/2V_{DD}$		V_{DD}	V
Logical "0"	to V_{SS}		Open		
Input Voltage Levels at 4 Hz/ Test Frequency					
Logical "1"		$V_{DD}-0.25$		V_{DD}	V
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels at Lamp, Test					
Logical "1"	100 kΩ Internal Pull-Up to V_{DD}		Open		
Logical "0"		V_{SS}		$V_{SS}+0.25$	V
Input Voltage Levels at Duty Cycle					
Logical "1"	No Pull-Up (Must Be Bonded)		V_{DD}		V
Logical "0"			V_{SS}		V
Input Voltage Levels at Dim	Duty Cycle = V_{SS}				
display duty cycle = 21.875%	5 MΩ Pull-Down to V_{SS}	Open		$V_{SS}+0.3$	V
display duty cycle = 9.375%		$V_{DD}-0.5$		V_{DD}	V
Input Voltage Levels @ A/D, P1–P8	10 MΩ Internal Pull-Down to				
Logical "1"	V_{SS}	$V_{DD}-0.25V$		V_{DD}	V
Logical "0"			Open		
Input Current at Cycle, Set/Display, Hour/Min	$V_{DD} = 3V$, $V_{IN} = V_{DD}$, Sink Only		30	50	μA
Input Current at Lamp, Test	$V_{DD} = 3V$, $V_{IN} = V_{SS}$, Source Only		30	50	μA
Input Current @ A/D, P1, P2, P4, P8	$V_{DD} = 3V$, $V_{IN} = V_{DD}$				
Logical "1"				350	nA
Logical "0"					
Input Capacitance	f = 1 MHz, V_{IN} = 0V, All Other Pads Gnd				
Osc. Out			8		pF
CAP 1			37		pF
CAP 2			15		pF
All Others				5	pF
Output Current Levels at Segment Drivers	$V_{DD} = 2.7V$				
"ON," Source	$V_{OUT} = V_{DD} - 0.5V$	7	10	15	mA
"OFF," Leakage	$V_{OUT} = V_{DD} - 1.1V$			50	μA

electrical characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current Levels at Digit Drivers	V_{DD} = 2.7V				
"ON," Sink (6 or 7-segment display)	$V_{OUT} = V_{SS} + 0.6V$	50	70		mA
(5 or 4-segment display)	If Colon is "ON," Add 2 mA		60% of 6 or 7-segment current		
(1, 2 or 3-segment display)	to Digit 4 Sink Current		46% of 6 or 7-segment current		
"OFF," Leakage	V_{OUT} = 2V, All Digit Drivers Tied in Parallel			2	µA
Output Current Levels at 4 Hz/Test Freq, 4096 Hz, 8 Sec.					
Logical "1," Source	$V_{OUT} = V_{DD} - 0.6V$	10			µA
Logical "0," Sink	$V_{OUT} = V_{SS} + 0.6V$	10			µA
Supply Current (I_{DD})	T_A = 25°C, f = 32,768 Hz, Unused Inputs Open, Outputs Open		3.5	7	µA
Supply Current (I_{DD})	T_A = 25°C, V_{SS}, Osc. In, Duty Cycle Control at Gnd, V_{DD} = 3V, Unused Inputs Open, Outputs Open		0.05	1.5	µA

functional description

A block diagram of the MM58115 direct drive digital watch is shown in *Figure 1*. The chip pad layout is shown in *Figure 2* and package connection diagram in *Figure 3*.

Time Base: The precision time base of the watch is provided by the 32,768 Hz crystal controlled oscillator, which consists of quartz crystal, a CMOS inverter/amplifier and the RC network shown in *Figure 4*. Resistor R1 biases the inverter for class A amplifier operation. Resistor R2 (a) reduces the voltage sensitivity of the network; (b) limits the power dissipation in the quartz crystal; and (c) provides added phase shift for good start-up and low voltage circuit performance. Capacitors C1 and C_{EFF} in series provide the parallel load capacitance required for precise tuning of the quartz crystal. The network shown in *Figure 4* provides greater than 100 ppm tuning range when used with standard X-Y flexure quartz crystals trimmed for C_L = 12 pF and a 5–36 pF trim capacitor. If digital tuning is used, the tuning range is ±114 ppm and no trim capacitor is required.

Cap 1: This pin is used with Oscillator Out to add more capacitance to the oscillator RC network shown in *Figure 4*.

Cap 2: This pin is used with Oscillator In to form the RC network shown in *Figure 4* if the digital tuning is to be used.

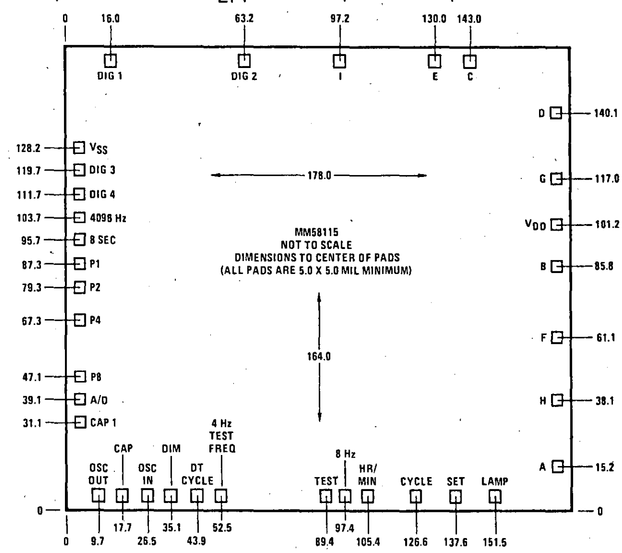


FIGURE 2. Pad Layout

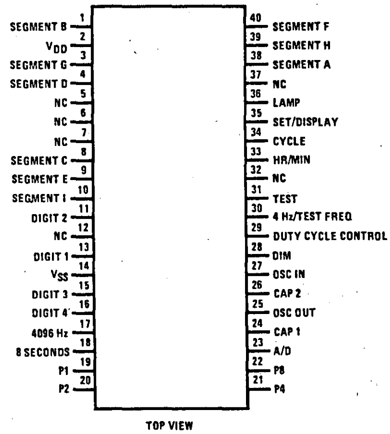


FIGURE 3. Connection Diagram

functional description (Continued)

Display Control: The TIME and DATE display sequence is controlled by normally open switches connected to SET/DISPLAY, and HOUR/MINUTE (inertial switch) inputs. With the display "OFF," depressing the SET/DISPLAY switch will activate the HOUR-MINUTE display. This display will remain "ON" for 1.25 seconds ±0.125 seconds. If the switch is still held in at the end of this time out, SECONDS will be displayed blinking "ON" for 0.25 seconds and "OFF" for 0.75 seconds until the SET/DISPLAY switch is released. If during the HOUR-MINUTE display, the SET/DISPLAY switch is released and depressed a second time, the date will be displayed as DAY-DATE. The DAY-DATE display will remain "ON" for 1.25 seconds ±0.125 seconds and turn "OFF" automatically if the SET/DISPLAY switch has been released. Holding the SET/DISPLAY switch past the display time out will cause the watch to display MONTH-DATE information until the SET/DISPLAY switch is released or until the SET/DISPLAY switch has been depressed longer than 2.0 seconds ±0.125 seconds. If held longer than 2 seconds, the MONTH-DATE display will return to DAY-DATE display. MONTH-DATE and DAY-DATE display will continue to alternate until the SET/DISPLAY switch is released. DAY-DATE will be displayed for 1.25 seconds and MONTH-DATE will be displayed for 0.75 seconds before the sequence starts to repeat. TIME may also be displayed in the MM58115 by activating the HOUR/MINUTE input. The HOUR/MINUTE input is used with an inertial switch that is normally open. Closing the switch activates the HOUR/MINUTE display. This display will remain "ON" for 1.25 seconds ±0.125 seconds and then turn "OFF" automatically.

Time Setting: The setting sequence is controlled by a normally open switch connected to the Cycle Input. Depressing the CYCLE switch will advance the watch to the next set mode. *Figure 5* is a flow diagram showing the display and set functions for the MM58115.

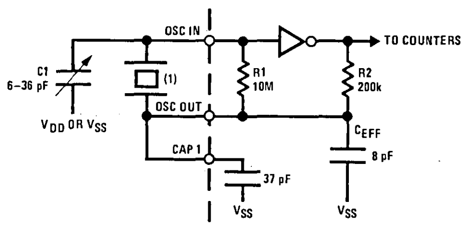
Set Hour Mode: With the watch in the normal Run mode and the display "OFF," depressing the CYCLE switch will put the watch into the Set Hour Mode. In this mode, HOURS will be displayed in digit positions 1 and 2 followed by the colon. An A or a P will be displayed in digit position 4 to indicate AM or PM, respectively. Depressing the SET/DISPLAY switch will advance the HOURS counter at a 2 Hz rate. If neither the SET/DISPLAY switch nor the CYCLE switch are depressed for 5.25 seconds ±0.125 seconds, the watch will automatically return to the Run mode. Depressing the CYCLE switch while in the Set Hours mode will advance the watch to the Set Minutes mode.

Set Minutes Mode: The Set Minutes mode will display minutes in digit positions 3 and 4 preceded by the colon. Depressing the SET/DISPLAY switch while still holding in the CYCLE switch will enable the hold flag but will not allow advancement of the MINUTE counter. Depressing the SET/DISPLAY switch after the CYCLE switch has been released resets and holds the SECOND counter, enables the hold flag, and advances the MINUTE counter at a 2 Hz rate. If neither switch is depressed for 5.25 seconds ±0.125 seconds while the watch is in the Set Minutes mode, the watch will automatically return to the Run mode if minutes have not been set. Depressing the CYCLE switch while in Set Minutes mode will advance the watch to the Set Day Mode.

Set Day Mode: The Set Day mode will display DAY-OF-THE-WEEK in digit positions 1 and 2. Depressing the SET/DISPLAY switch while in the Set Day mode will advance the DAY counter at a 2 Hz rate. If neither switch has been depressed for 5.25 seconds ±0.125 seconds while in the Set Day mode, the watch will automatically return to the Run mode if the hold flag was not set or will jump to the Hold mode if the hold flag was set. Depressing the CYCLE switch while in the Set Day mode will advance the watch to the Set Date mode.

Set Date Mode: The Set Date mode will display DATE in digit positions 3 and 4. Depressing the SET/DISPLAY switch while in the Set Date mode will advance the DATE counter at a 2 Hz rate. If neither the SET/DISPLAY nor the CYCLE switches have been depressed for 5.25 seconds ±0.125 seconds while in the Set Date mode, the watch will automatically return to the Run Mode if the hold flag was not set. Depressing the CYCLE switch while in the Set Date mode will advance the watch to the Set Month mode.

Set Month Mode: The Set Month mode will display MONTH in digit positions 3 and 4 and an M in digit position 1. Depressing the SET/DISPLAY switch while in the Set Month mode will advance the MONTH counter at a 2 Hz rate. If neither the SET/DISPLAY nor the cycle switches have been depressed for 5.25 seconds ±0.125 seconds while in the Set Month mode, the watch



Note 1. 32,768 Hz anti-resonant quartz crystal, C_L = 12 pF

FIGURE 4(a). Oscillator RC Network

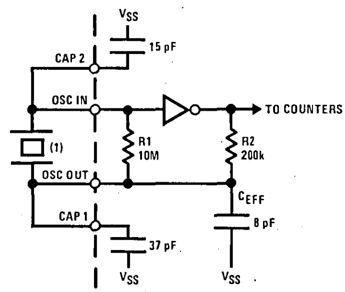


FIGURE 4(b). Oscillator RC Network If Digital Tuning is Used.

7

functional description (Continued)

will automatically return to the Run mode if the hold flag was not set, or will advance to the Hold mode if the hold flag was set. Depressing the Cycle switch while in the Set Month mode will advance the watch to the Hold mode if the hold flag was set; otherwise, the watch will advance to the Run mode.

Hold Mode: In the Hold mode the SECOND counter is held at 00, and the HOUR-MINUTE display will blink "ON" for 0.25 seconds and "OFF" for 0.75 seconds. Depressing the SET/DISPLAY switch will place the watch in the display HOUR/MINUTE mode for 1.25 seconds ±0.125 seconds. Depressing the Cycle switch while in the Hold mode will advance the watch to the Set Hour mode. There is no roll-over of the next higher counter while a counter is being set at a 2 Hz rate.

Month Counter: The MONTH counter provides "smart Date." The DATE counter will count 28 days in February, 30 in April, June, September and November, and 31 in the remaining months.

Contact Bounce: Debounce circuitry is provided on the SET/DISPLAY, CYCLE, and HOUR/MINUTE inputs to remove any logic uncertainty upon either closure or release of the switches. 100 ms debounce protection is provided for SET/DISPLAY and CYCLE inputs and 200 ms protection is provided for the HOUR/MINUTE input.

Display Multiplexing: The counter data selected to be displayed is time-division multiplexed to provide digit-sequential presentation to the LED display. This reduces the number of outputs required to drive the 4-digit display to thirteen (9-segment drivers and 4-digit drivers). The display font is shown in *Figure 6. Figure 8* is a schematic diagram of a typical LED watch using the MM58115 watch chip. The segment and digit drivers are designed to interface directly with the LED display. The four digits of the LED display are multiplexed with a 23% duty cycle, 1024 Hz signal during the display period. The digit drivers are disabled for 32µs at the beginning of each digit enable time to allow the segment

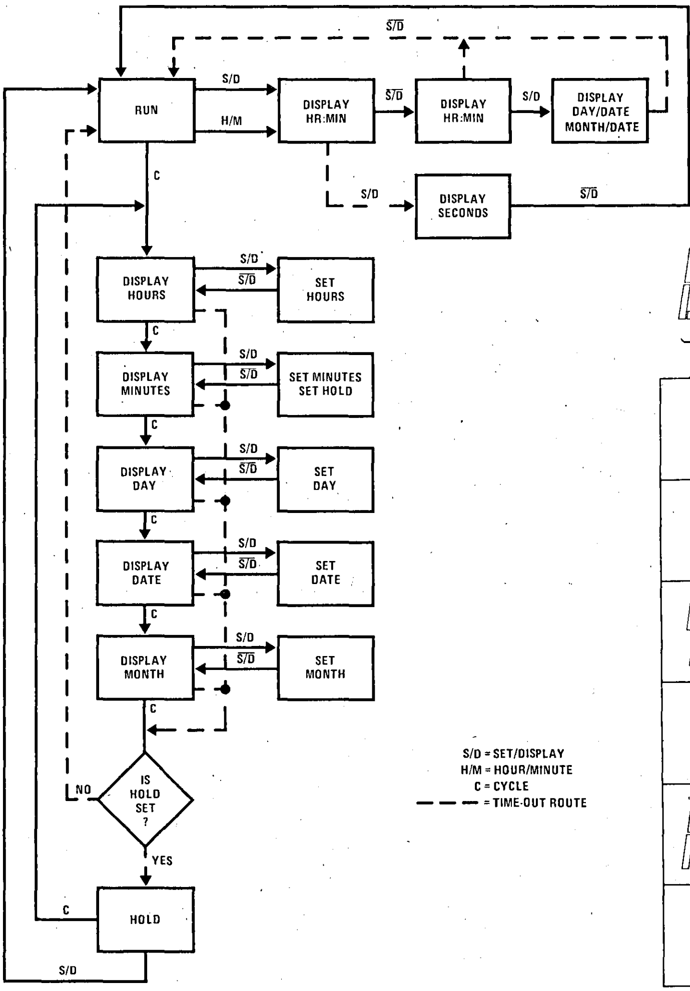


FIGURE 5(a). MM58115 Flow Diagram

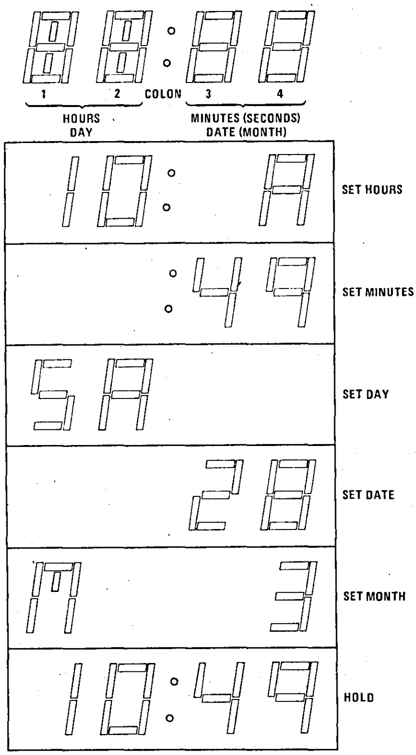


FIGURE 5(b). Set Display Font

functional description (Continued)

decoding circuitry adequate time to switch to the next digit's information. This eliminates the possibility of "ghosting" information between digits.

Colon Output: Colon information is present on the "h" and "i" segment outputs during digit position 4.

Dim Input: The Dim Input is a 2-level input. This input has a pull-down to V_{SS} to hold it normally at a logical "0." In this condition with Duty Cycle Control at V_{SS} the display will normally be at maximum intensity. With the Dim input at V_{DD}, the display will be at 3/7 of the full intensity. If the Dim input is at V_{DD} and the Duty Cycle Control input is at V_{SS}; maximum intensity will be 3/7 of full intensity. With the Dim input at V_{DD}, the display intensity will be reduced to 1/7 of full intensity. *Figure 7* shows the switching threshold ranges for the Dim Input.

Duty Cycle Control: The Duty Cycle Control Input is used with the Dim Input to determine the intensity of display. The duty cycle range is shown in *Figure 7*.

Digital Tuning: To digitally tune the time base, A/D, P1, P2 P4 and P8 inputs are used. A/D input either adds or deletes pulses into the counter chain. P1, P2, P4 and P8 inputs determine the number of pulses to be added or deleted from the counter chain in a specific time period. Each pulse added or deleted "tunes" the time base by 7.6 ppm. An 8-second output pad is provided to easily check the time base frequency. When A/D is open (internal pull-down to V_{SS}) or at V_{SS}, pulses are deleted. If A/D is tied to V_{DD}, pulses are added into the counter chain. P1, P2, P4 and P8 inputs have internal pull-downs to V_{SS}, which is a logical "0." When these inputs are tied to V_{DD}, they are at a logical "1." Table I shows the tuning range for each input code. If the Digital Tuning scheme is not used, leave all inputs open.

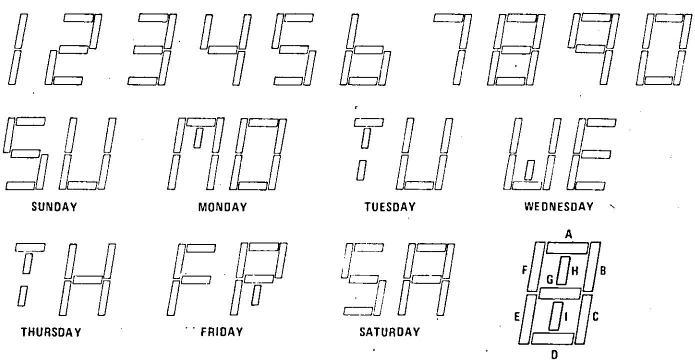
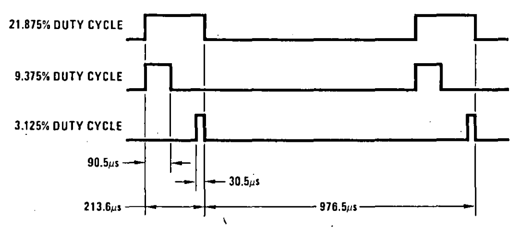


FIGURE 6. Display Font



DUTY CYCLE CONTROL	DIM INPUT	DISPLAY TIME/DIGIT	DISPLAY CONDITION
V_{SS}	$> V_{DD} - 0.5V$	9.375%	Low Ambient Light
	$< V_{SS} + 0.3V$	21.875%	High Ambient Light
V_{DD}	$> V_{DD} - 0.5V$	3.125%	Low Ambient Light
	$< V_{SS} + 0.3V$	9.375%	High Ambient Light

FIGURE 7. Dim Input Levels

functional description (Continued)

Test Points: Five pads are provided for test purposes.

8 Seconds: This output is used with A/D, P1, P2, P4 and P8 to digitally tune the time base frequency.

4096 Hz: This pad outputs a 4096 Hz signal that can be used for oscillator tuning.

4 Hz/Test Frequency: This is an input/output pad under the control of the Test input pad. When "Test" is at a logical "0," the 4 Hz/Test Freq pad becomes an input and any frequency connected to it will replace the normal internal 4 Hz signal. This feature is provided to allow high speed functional testing of the watch system. When "Test" is open or at a logical "1," a 4 Hz output will appear on the 4 Hz/Test Freq pad.

Test: This pad is used as an input to control the 4 Hz/ Test Freq pad. An internal pull-up resistor will normally hold "Test" at a logical "1." Changing the Test input from a logical "1" to a logical "0" will generate a reset pulse which will set the internal counters to 1 AM on Sunday, January the first. The watch is now in a known state for testing.

Lamp: When the Lamp input is at a logical "0," all segments of the display will be forced to an "ON" condition under control of the normal 23% duty cycle of the digit drivers. An internal pull-up resistor will normally hold the Lamp input at a logical "1."

TABLE I. Digital Tuning Table

P1	P2	P4	P8	Δf (ppm)
0	0	0	0	0
1	0	0	0	7.63
0	1	0	0	15.26
1	1	0	0	22.89
0	0	1	0	30.52
1	0	1	0	38.15
0	1	1	0	45.78
1	1	1	0	53.41
0	0	0	1	61.04
1	0	0	1	68.57
0	1	0	1	76.29
1	1	0	1	83.92
0	0	1	1	91.55
1	0	1	1	99.18
0	1	1	1	106.81
1	1	1	1	114.44

A/D is 1 to add to frequency
A/D is 0 to slow down frequency
Procedure: Monitor 4096 Hz output, determine frequency shift desired, bond A/D, P1, P2, P4, P8 to the correct code. 8 second pad will be at the correct frequency.

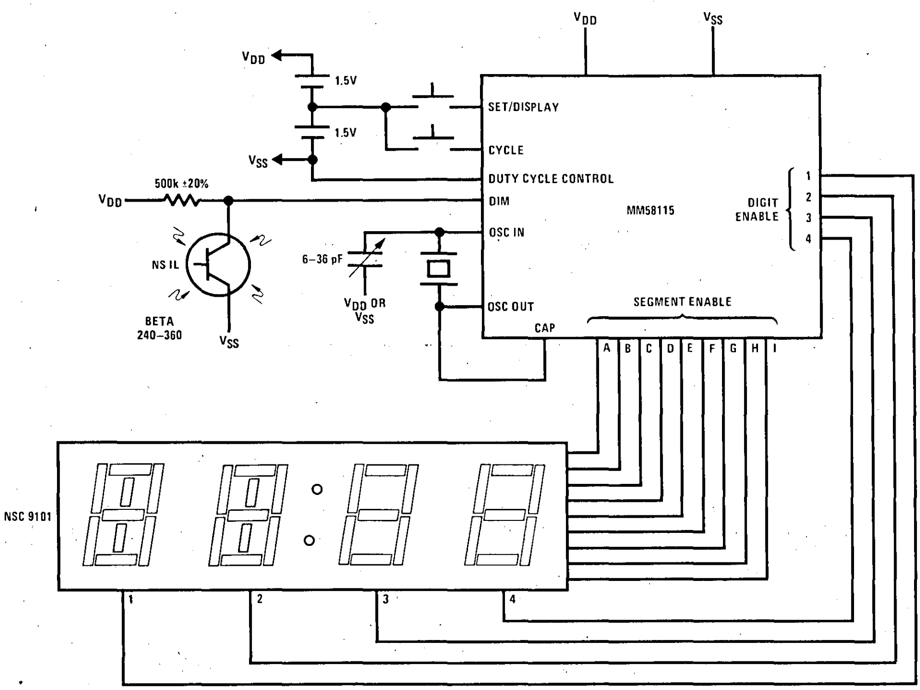


FIGURE 8(a). System Schematic for MM58115 LED Watch

functional description (Continued)

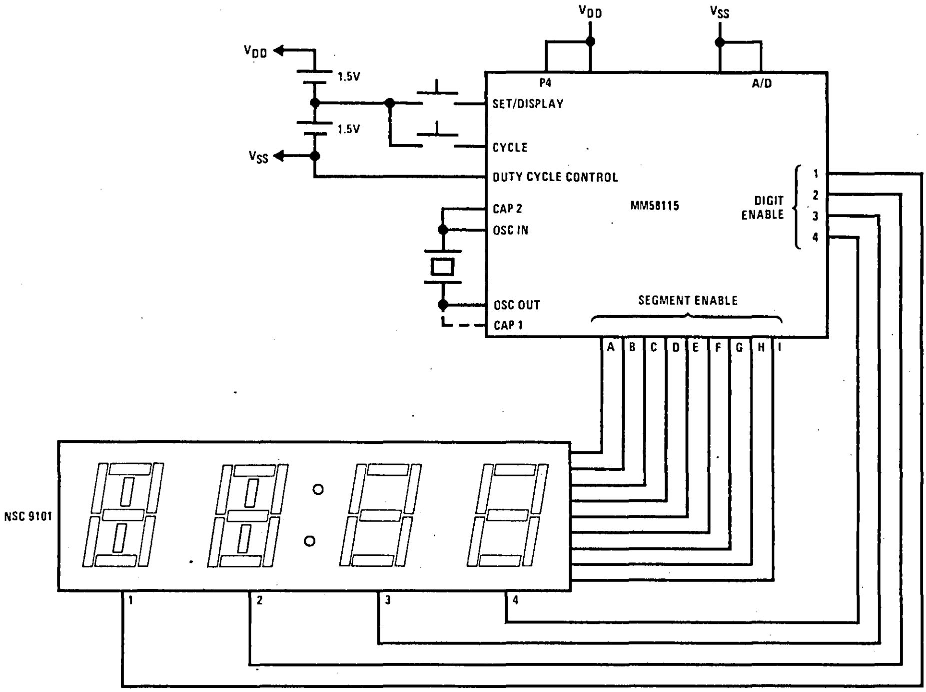


FIGURE 8(b). System Schematic for MM58115 Digitally Tuned LED Watch

MM58117, MM58118, MM58119, MM58120 LCD watch circuits

general description

The MM58117, MM58118, MM58119, and MM58120 are low threshold voltage, ion implanted, metal-gate CMOS integrated circuits that provide or control all signals needed for a 3-1/2 digit LCD watch. The circuit time base is a 32,768 Hz crystal controlled oscillator. This time base frequency is counted down to provide proper signals to display Hours-Minutes information continuously with Month-Date or Seconds information available upon demand. Time is displayed in 12 hour format. 23 phase controlled outputs are available for direct drive of a 3-1/2 digit liquid output display (LCD). The 32 Hz output serves as the backplane drive for the LCD. All four parts operate on a single 1.3—1.7V supply. An on-chip voltage multiplier using external capacitors is used to provide the drive voltage for the display. The MM58117 and MM58118 have on-chip voltage doublers which provide 2.5V minimum at 1μA load current. The MM58119 and MM58120 have on-chip voltage triplers which provide 3.8V minimum at 1μA load current. Alternatively, the MM58117 and MM58119 provide a 256 Hz output pulse and the MM58118 and MM58120 provide a 1024 Hz output pulse that can be used to drive an inductive up-converter off chip. The Regulate input can be used to suppress this output pulse to regulate the voltage generated. The Regulate pad is not present on the MM58117, MM58119 versions. A Test input can be used to convert the 32 Hz output into an input for testing the divider circuitry at a higher frequency. All four parts are available as unpackaged die suitable for hybrid assembly or in 40-lead dual-in-line packages for evaluation purposes.

features

- Direct continuous LCD drive capability
- 32,768 Hz crystal controlled operation
- Single 1.5V battery operation
- Low power dissipation
- 3-1/2 digit, 12 hour display
- 4 year calendar
- Seconds, Month, and Date display upon demand
- Colon display
- Simple 2 button sequential setting
- Auto reset feature (MM58118 and MM58120)
- On-chip capacitive voltage multiplier
- Regulated bipolar drive also available (MM58118, MM58120)

block diagram

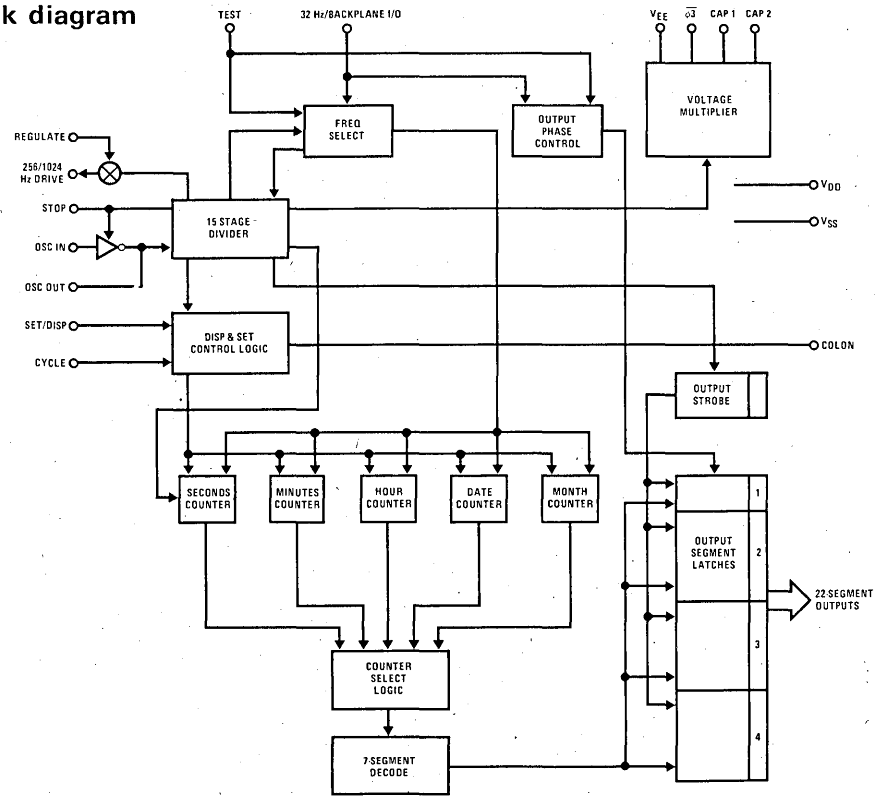


FIGURE 1

absolute maximum ratings

Voltage at OSC IN, OSC OUT, 256/1024 Hz Regulator, Set/Display, Cycle, Stop, $\overline{\text{Phase 3}}$	V_{DD}+0.3V to V_{SS}−0.3V
Voltage at Any Other Pin	V_{DD}+0.3V to V_{EE}−0.3V
Operating Temperature Range	−5°C to +70°C
Storage Temperature Range	−25°C to +85°C
$V_{DD} - V_{EE}$	8.0V
$V_{DD} - V_{SS}$	3.0V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, $V_{DD} - V_{SS}$ = 1.5V, $V_{DD} - V_{EE}$ = 4.5V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	T_A = 25°C, (Note 1)	1.4			V
Oscillator Sustaining Voltage	T_A = −5°C, (Note 1)	1.3			V
Input Voltage Levels					
Set/Display, Cycle					
Logical "1"		V_{DD}−0.25		V_{DD}	V
Logical "0"	Internal Pull Down to V_{SS}		Open		V
BP/32 Hz Input					
Logical "1"		V_{DD}−0.25		V_{DD}	V
Logical "0"		V_{EE}		V_{EE}+0.25	V
Test, Stop					
Logical "1"	Internal Pull Down to V_{EE}	V_{DD}−0.25		V_{DD}	V
Logical "0"			Open		V
Input Current Levels					
Set/Display, Cycle	$V_{IN} = V_{DD}$	0.2		10.0	μA
Test	$V_{IN} = V_{DD}$			15	μA
Stop	$V_{IN} = V_{DD}$, $V_{EE} = V_{SS}$ + 0.3V			0.5	μA
Input Capacitance OSC IN,	f = 1 MHz, V_{IN} = 0V All Other Pads GND			5	pF
Output Voltage Levels					
Segment Drivers					
Logical "1"	$V_{OUT} = V_{DD}$ − 0.2V, $V_{DD} - V_{EE}$ = 3V	4			μA
Logical "0"	$V_{OUT} = V_{EE}$ + 0.2V, $V_{DD} - V_{EE}$ = 3V	4			μA
BP/32 Hz Output					
Logical "1"	$V_{OUT} = V_{DD}$ − 0.2V, $V_{DD} - V_{EE}$ = 3V	40			μA
Logical "0"	$V_{OUT} = V_{EE}$ + 0.2V, $V_{DD} - V_{EE}$ = 3V	40			μA
256/1024 Hz					
Logical "1"	$V_{OUT} = V_{DD}$ − 0.2V, $V_{DD} - V_{SS}$ = 1.5V	30			μA
Logical "0"	$V_{OUT} = V_{SS}$ + 0.3V, $V_{DD} - V_{SS}$ = 1.5V	300			μA
Output Current Levels	$V_{DD} - V_{SS}$ = 1.4V, $V_{DD} - V_{EE}$ = 4.2V				
$\overline{\text{Phase 3}}$					
Logical "1," Source	$V_{OUT} = V_{DD}$ − 0.25V, Phase 2 < 1.5 ms	7.5			μA
Logical "0," Sink	$V_{OUT} = V_{SS}$ + 0.25V	35.0			μA
CAP 1					
Phase 1, Source	$V_{OUT} = V_{DD}$ − 0.25V	7.5			μA
Phase 2, Sink	$V_{OUT} = V_{SS}$ + 0.25V	20.0			μA
Phase 3, Leakage	$V_{OUT} = V_{DD}$ − 3.0V			0.6	μA
CAP 2					
Phase 1, Sink	$V_{OUT} = V_{SS}$ + 0.25V	35.0			μA
Phase 2, Leakage	$V_{OUT} = V_{EE}$ + 1.5V			0.6	μA
V_{EE}					
Phase 3, Sink	CAP 2 = V_{DD} − 4.2V, $V_{OUT} = V_{DD}$ − 3.95V	250			μA

7

electrical characteristics (Continued) T_A within operating range, $V_{DD} - V_{SS} = 1.5V$, $V_{DD} - V_{EE} = 4.5V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_{DD})	$T_A = 25°C$, $I_{EE} = 1\mu A$, f = 32,768 Hz, $V_{DD} = 1.5V$				
Doubler Operation			3.0	5.0	μA
Tripler Operation			6.0	8.0	μA
Voltage Regulator Input Current	$V_{IN} = V_{DD} - 0.75$, $T_A = 25°C$ MM58118, MM58120 Only		0.2	1.0	μA
Voltage Regulator Switching Threshold		V_{DD}−0.4		V_{DD}−1.1	V
256/1024 Hz Pulse Width		13		17	μs
Supply Voltage (V_{EE})	$T_A = 25°C$, $C = 0.047\mu F$, $I_{EE} = 1\mu A$, f = 32,768 Hz, $V_{DD} - V_{SS} = 1.5V$, *(Figure 9)*, (Note 1)				
Doubler Operation		2.5			V
Tripler Operation		3.8			V

Note 1: In oscillator network shown in *Figure 4*.

functional description

A block diagram of the Watch Chip is shown in *Figure 1*. A chip pad layout is shown in *Figure 2* and a package connection diagram in *Figure 3*.

The MM58117 and MM58118 contain an on-chip voltage doubler for display drive and the MM48119 and MM48120 contain an on-chip voltage tripler.

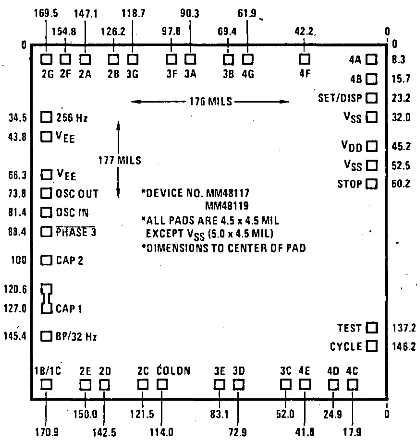


FIGURE 2(a)

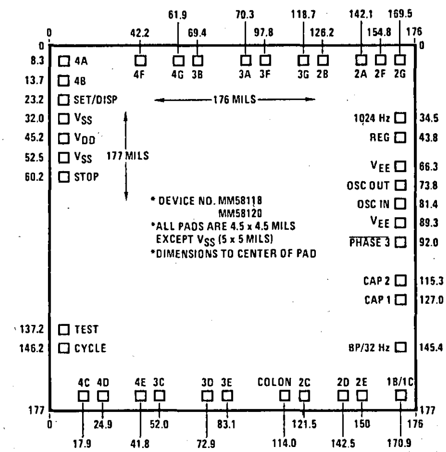


FIGURE 2(b)

MM58117N, MM58119N

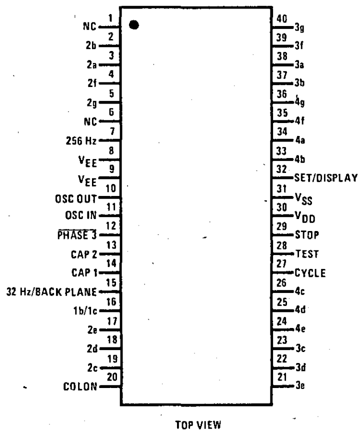


FIGURE 3(a)

MM58118N, MM58120N

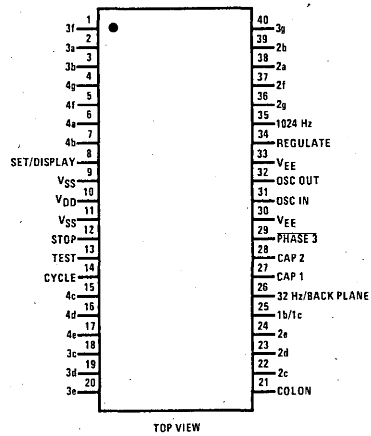


FIGURE 3(b)

functional description (Continued)

Time Base: The precision time base of the watch is provided by connecting a crystal controlled RC network to the on-chip CMOS inverter/amplifier as shown in *Figure 4*. For proper operation, the network should be tuned to 32,768 Hz. Resistor R1 is used to bias the on-chip inverter for class A amplifier operation. Resistor R2 is used to (a) reduce the voltage sensitivity of the network; (b) limit the power dissipation in the quartz crystal; and (c) provide added phase shift for good start-up and low voltage circuit performance. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. The network shown in *Figure 4* provides greater than 100 ppm tuning range when used with standard X-Y flexure quartz crystals trimmed for C_L = 13 pF. Tuning to better than 2 ppm is easily obtainable.

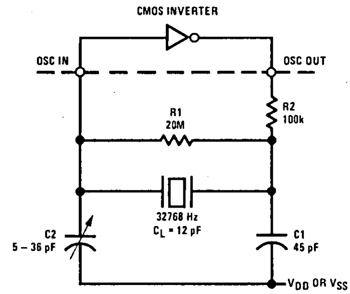


FIGURE 4. Crystal Oscillator Network

The 256/1024 Hz output or the 32 Hz output can be used to monitor the oscillator frequency during initial tuning without disturbing the network itself.

DISPLAY CONTROL

The Hour:Minute, Month Date, and Second displays are controlled by a normally open switch connected to the Set/Display input. Month and Hour are displayed in digit positions 1 and 2. Date, Minute, and Second are displayed in digit positions 3 and 4.

The circuit will normally display Hour and Minute with the colon flashing at a 1 Hz rate (*Figure 5*). Depressing the Set/Display switch will cause Month and Date to be displayed with no colon. The display will automatically return to Hour and Minute display 2.25 ±0.25 seconds after the Set/Display switch has been released. Depressing the Set/Display switch a second time while the Month and Date are being displayed will cause the Second to be displayed until the Set/Display switch is again depressed, returning the display to Hour and Minute.

The MM58117 and MM58119 have an additional display mode that can be used by depressing the Cycle switch while the watch is in the first display mode described above. The second display mode will alternately display Hour:Minute and Month Date for a period of 2 seconds each. Depressing the Set/Display switch will cause the Second to be displayed. Depressing the Set/Display switch again will return the watch to the second display mode.

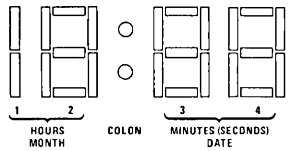


FIGURE 5. Time Display

Leading zero values of month, date, and hours are blanked. The circuit contains a 4 year calendar which will automatically reset the Date Counter to 1 and advance the Month Counter at the end of each month (except for February in Leap Year). The character display font is shown in *Figure 6*.

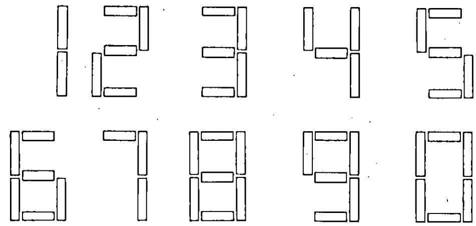


FIGURE 6. Character Display Font

SETTING CONTROL

A normally open switch connected to the Cycle input is used in conjunction with the Set/Display switch to set Month, Date, Hour, Minute, and synchronize Second information.

MM58118, MM58120

Hour: With the watch in the display mode, depressing the Cycle switch will put the watch in the Set Hour mode. In this mode the Hour will be displayed in digit positions 1 and 2 followed by the colon and either an A or a P (for AM or PM) displayed in digit position 4. While in this mode depressing the Set/Display switch will advance the Hour Counter at a 1 Hz rate until the Set/Display switch is released.

Minute: Depressing the Cycle switch while the watch is in the Set Hour mode will advance it to the Set Minute mode. In this mode the Minute will be displayed in digit positions 3 and 4 preceeded by the colon. Depressing the Set/Display switch while still holding the Cycle switch in will cause the Hold mode to be activated but will not advance the Minute counter. Depressing the Set/Display switch after the Cycle switch has been released will cause the Hold mode to be activated and will advance the Minute counter at a 1 Hz rate as long as the switch is held in.

Month: Depressing the Cycle switch while the watch is in the Set Minute mode will advance it to the Set Month mode. In this mode the Month will be displayed in digit positions 1 and 2 with no colon. Depressing the Set/Display switch will cause the Month counter to be advanced at a 1 Hz rate as long as the switch is held in.

functional description (Continued)

Date: Depressing the Cycle switch while the watch is in the Set Month mode will advance it to the Set Date mode. In this mode the Date will be displayed in digit positions 3 and 4 with no colon. Depressing the Set/Display switch will cause the Date counter to be advanced at a 1 Hz rate as long as the switch is held in.

Hold: If the Hold mode was activated while in the Set Minute mode, depressing the Cycle switch while in the Set Day mode will advance the watch to the Hold mode. In this mode Hour:Minute will be displayed flashing at a 1 Hz rate. The Second counter will be held at 00. Depressing the Set/Display switch will advance the watch to the normal run mode with Month:Date displayed and release the Second counter to begin normal operation. Depressing the Cycle switch will place the watch in the Set Hour mode with the Hold mode still activated. If the Hold mode was not activated while in the Set Minute mode, depressing the Cycle switch while in the Set Date mode will advance the watch to the Run mode with Hour:Minute displayed.

While in any of the above set modes if no switches are activated for 5.25 ± 0.25 continuous seconds the watch will automatically jump to the Hold mode if it was activated in the Set Minutes mode or to the Run mode if the Hold mode was not activated. There is no roll over of the next higher counter while a counter is being set. For example, while in the Set Minute mode, advancing the Minute counter from 59 to 00 will not advance the Hour counter.

MM58117, MM58119

The MM58117 and MM58119 setting procedure is similar to that of the MM58118, except that the setting sequence is as follows:

1. Set Month
2. Set Date
3. Set Hour
4. Set Minute/Hold

There is no 5.25 second time-out while in the setting mode and the watch will stay in each set mode until it is advanced to the next mode. The Cycle switch is used to advance from the Set Minute state to the first display state. The colon will blink on and off while time is being displayed unless the Hold mode is activated, forcing the colon to remain on continuously. During the second display mode, the colon will remain on during time display. Depressing the Set/Display switch while in either one of the two display states will cause the Hold mode to be cleared, allowing the watch to begin normal operation.

Control state diagrams for the MM58117, MM58118, MM58119 and the MM58120 are provided in *Figure 7.*

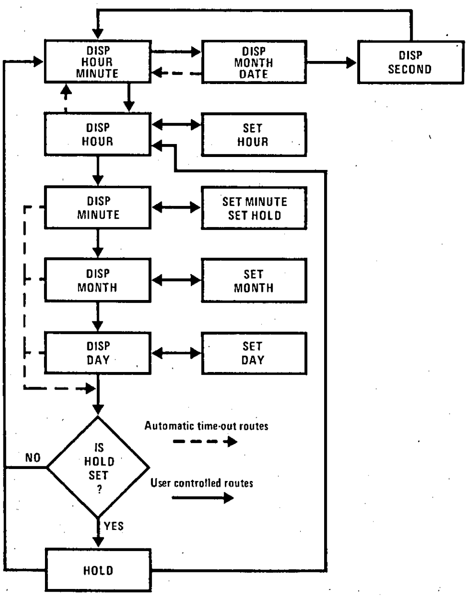


FIGURE 7(a). MM58118, MM58120 Control State Diagram

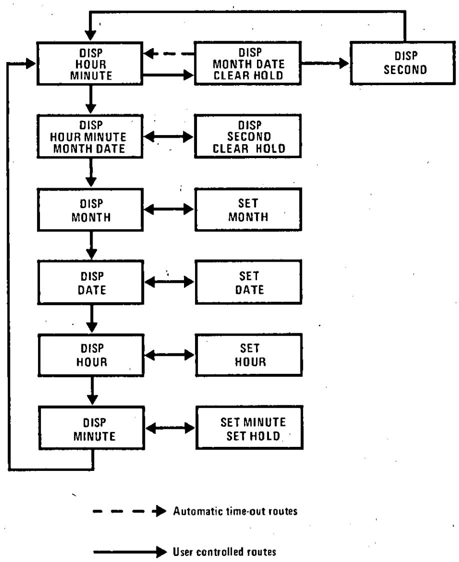


FIGURE 7(b). MM58117, MM58119 Control State Diagram

functional description (Continued)

Stop Input: This input pad has an internal resistor to V_{EE} holding it normally at a logical "0." A logical "1" at stop will force all of the display segments "OFF" and stop the oscillator, placing the watch in a static mode to decrease power dissipation during extended periods of storage.

Contact Bounce: Debounce circuitry is provided on the Set/Display and Cycle inputs to remove any logic uncertainty upon either closure or release of switches provided switch bounce settles within 20 ms.

Segment Outputs: The Segment outputs are designed to drive field-effect liquid crystal displays. Each display segment has its own output which furnishes the proper 32 Hz drive signal. By definition, the segment is "OFF" when its drive signal is in phase with the display backplane signal (BP/32 Hz). The segment is "ON" when its drive signal is 180° out of phase with the display backplane signal. Typical output waveforms are shown in *Figure 8.*

Colon Output: The Colon output provides a 32 Hz phase controlled signal identical to the segment outputs. The colon will blink at a 1 Hz rate during time display mode (except for display mode one with the Hold mode activated, and display mode two in the MM58117, MM58119) and remain on continuous while displaying time (Hours or Minutes) during the setting operation.

VOLTAGE MULTIPLIER OUTPUTS:

256/1024 Hz: The 256/1024 Hz pad is provided to drive a bipolar transistor which, in conjunction with a coil or transformer, generates the higher voltage needed for the display. A typical circuit is shown in *Figure 9.* The output waveform is shown in *Figure 10.* The MM58118, MM58120 provides a 1024 Hz output pulse while the MM58117, MM58119 provides the 256 Hz output pulse.

Voltage Regulator: The Regulator input is used in conjunction with a zener diode to shut-off the 1024 Hz output to regulate the level of the V_{EE} supply voltage. The Regulator input is provided on the MM58118 and MM58120 only.

Test Pads: Two pads are provided for test purposes.

BP/32 Hz: This input/output pad is under the control of Test. When Test is open or at a logical "0," a 32 Hz signal is provided on BP/32 Hz which can be used to drive the backplane of the LCD unit or to monitor the oscillator frequency without affecting the oscillator circuitry. If Test is at a logical "1," the BP/32 Hz pad is converted into an input and any frequency connected to it will replace the normal internal 32 Hz signal. This feature is provided to allow high speed advancement of the internal counters for testing purposes.

Test: This input pad is used to control the BP/32 Hz pad as described above. When the Test pad is at a logical "1," the phase-control is disconnected from the segment drive outputs and the segment information will be referenced to a logical "0" backplane. Switching the Test pad from a logical "0" to a logical "1" generates a reset pulse that will reset the watch counters to 1 AM on January the first. This places the watch into a known state for testing purpose.

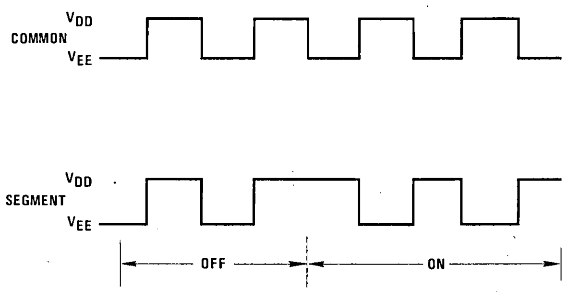
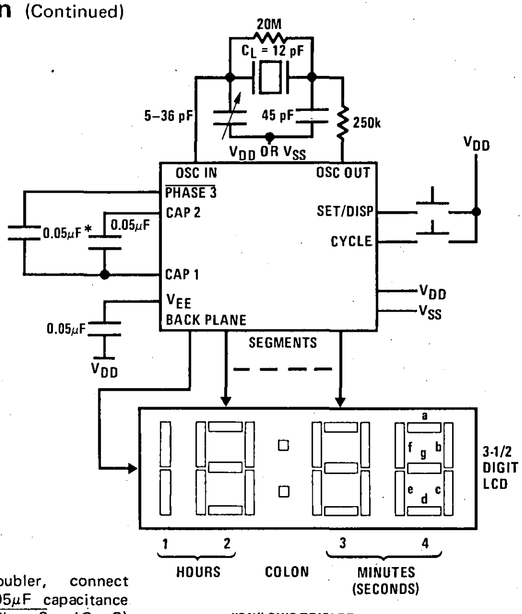


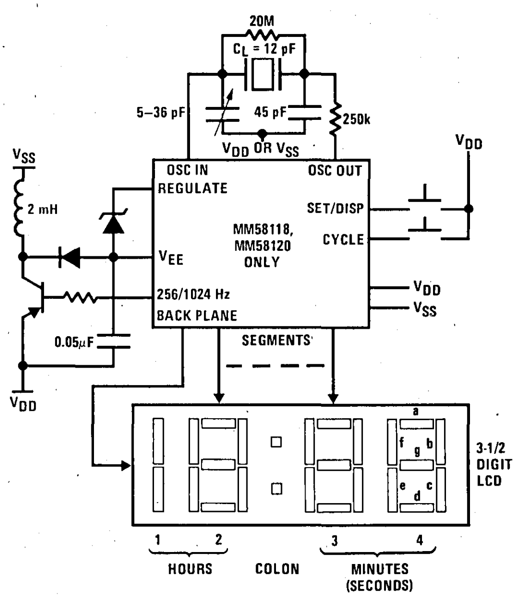
FIGURE 8. Common and Segment Output Signals

functional description (Continued)



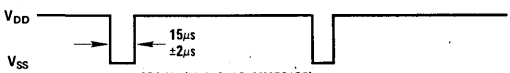
*(For doubler, connect single 0.05μF capacitance between $\overline{\text{Phase 3}}$ and Cap 2)

"ON" CHIP TRIPLER



"OFF" CHIP MULTIPLIER

FIGURE 9. Typical Application of MM58117, MM58118, MM58119 and MM58120 in LCD Watch System



1024 Hz (MM58118, MM58120)
256 Hz (MM58117, MM58119)

FIGURE 10. 1024 Hz Output

Watches

MM58127, MM58128, MM58129, MM58130 LCD watch circuits

general description

The MM58127, MM58128, MM58129, and MM58130 are low threshold voltage, ion implanted, metal-gate CMOS integrated circuits that provide or control all signals needed for a 3 1/2-digit LCD watch. The circuit time base is a 32,768 Hz crystal controlled oscillator. Oscillator RC network components are included on the circuits. The time base frequency is counted down to provide proper signals to display Hours-Minutes information continuously with Month-Date or Seconds information available upon demand. Time is displayed in 12-hour format. 23 phase controlled outputs are available for direct drive of a 3 1/2-digit liquid output display (LCD). The 32 Hz output serves as the backplane drive for the LCD. All 4 parts operate on a single 1.3–1.7V supply. An on-chip voltage multiplier using external capacitors is used to provide the drive voltage for the display. All circuits have an on-chip voltage doublers which provide 2.5V minimum at 1 μA load current or voltage triplers which provide 3.8V minimum at 1 μA load current. A Test input can be used to convert the 32 Hz output into an input for testing the divider circuitry at a higher frequency. All 4 parts are available as unpackaged die suitable for hybrid assembly or in 40-lead dual-in-line packages for evaluation purposes.

features

- Direct continuous LCD drive capability
- 32,768 Hz crystal controlled operation
- Single 1.5V battery operation
- Low power dissipation
- 3 1/2-digit, 12 hour display
- 4 year calendar
- Seconds, Month and Date display upon demand
- Colon display
- Simple 2 button sequential setting
- On-chip oscillator RC network
- On-chip capacitive voltage multiplier

block diagram

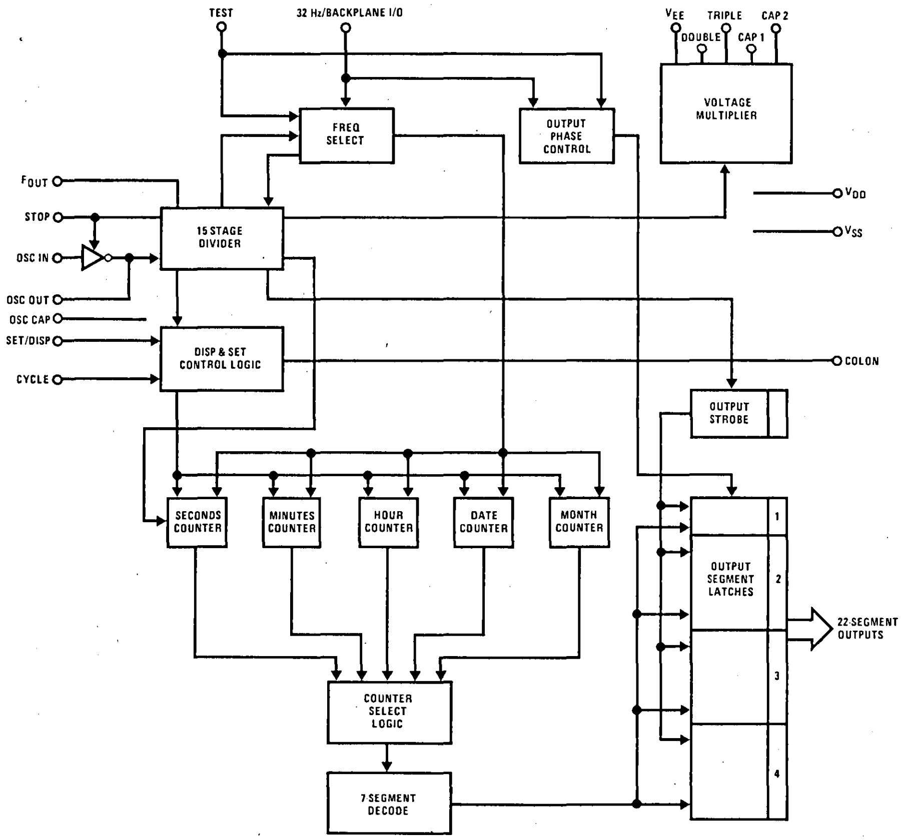


FIGURE 1

absolute maximum ratings

Voltage at Osc. In, Osc. Out, F_{OUT} Regulator, Set/Display, Cycle, Stop, Double, Triple	V_{DD}+0.3V to V_{SS}–0.3V
Voltage at Any Other Pin	V_{DD}+0.3V to V_{EE}–0.3V
Operating Temperature Range	–5°C to +70°C
Storage Temperature Range	–25°C to +85°C
$V_{DD} - V_{EE}$	8.0V
$V_{DD} - V_{SS}$	3.0V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating range, $V_{DD} - V_{SS}$ = 1.5V, $V_{DD} - V_{EE}$ = 4.5V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Start Voltage	T_A = 25°C, (Note 1)	1.4			V
Oscillator Sustaining Voltage	T_A = –5°C, (Note 1)	1.3			V
Input Voltage Levels					
Set/Display, Cycle					
Logical "1"		V_{DD}–0.25		V_{DD}	V
Logical "0"	Internal Pull Down to V_{SS}		Open		V
BP/32 Hz Input					
Logical "1"		V_{DD}–0.25		V_{DD}	V
Logical "0"		V_{EE}		V_{EE}+0.25	V
Test, Stop					
Logical "1"	Internal Pull Down to V_{EE}	V_{DD}–0.25		V_{DD}	V
Logical "0"			Open		V
Input Current Levels					
Set/Display, Cycle	$V_{IN} = V_{DD}$	0.2		10.0	µA
Test	$V_{IN} = V_{DD}$			15	µA
Stop	$V_{IN} = V_{DD}$, $V_{EE} = V_{SS}$ + 0.3V			0.5	µA
Input Capacitance Osc. In,	f = 1 MHz, V_{IN} = 0V All Other Pads Gnd			5	pF
Output Voltage Levels					
Segment Drivers					
Logical "1"	$V_{OUT} = V_{DD}$ – 0.2V, $V_{DD} - V_{EE}$ = 3V	4			µA
Logical "0"	$V_{OUT} = V_{EE}$ + 0.2V, $V_{DD} - V_{EE}$ = 3V	4			µA
BP/32 Hz Output					
Logical "1"	$V_{OUT} = V_{DD}$ – 0.2V, $V_{DD} - V_{EE}$ = 3V	40			µA
Logical "0"	$V_{OUT} = V_{EE}$ + 0.2V, $V_{DD} - V_{EE}$ = 3V	40			µA
F_{OUT}					
Logical "1"	$V_{OUT} = V_{DD}$ – 0.2V, $V_{DD} - V_{SS}$ = 1.5V	30			µA
Logical "0"	$V_{OUT} = V_{SS}$ + 0.3V, $V_{DD} - V_{SS}$ = 1.5V	300			µA
Output Current Levels	$V_{DD} - V_{SS}$ = 1.4V, $V_{DD} - V_{EE}$ = 4.2V				
Double, Triple					
Logical "1," Source	$V_{OUT} = V_{DD}$ – 0.25V, Phase 2 < 1.5 ms	7.5			µA
Logical "0," Sink	$V_{OUT} = V_{SS}$ + 0.25V	35.0			µA
Cap. 1					
Phase 1, Source	$V_{OUT} = V_{DD}$ – 0.25V	7.5			µA
Phase 2, Sink	$V_{OUT} = V_{SS}$ + 0.25V	20.0			µA
Phase 3, Leakage	$V_{OUT} = V_{DD}$ – 3.0V			0.6	µA
Cap. 2					
Phase 1, Sink	$V_{OUT} = V_{SS}$ + 0.25V	35.0			µA
Phase 2, Leakage	$V_{OUT} = V_{EE}$ + 1.5V			0.6	µA
V_{EE}					
Phase 3, Sink	Cap. 2 = V_{DD} – 4.2V, $V_{OUT} = V_{DD}$ – 3.95V	250			µA

electrical characteristics (Continued)

T_A within operating range, $V_{DD} - V_{SS} = 1.5V$, $V_{DD} - V_{EE} = 4.5V$ unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_{DD})	$T_A = 25°C$, $I_{EE} = 1\mu A$, f = 32,768 Hz, $V_{DD} = 1.5V$				
Doubler Operation			3.0	5.0	μA
Tripler Operation			4.0	7.0	μA
256/1024 Hz Pulse Width		13		17	μs
Supply Voltage (V_{EE})	$T_A = 25°C$, $C = 0.047\mu F$, $I_{EE} = 1\mu A$, f = 32,768 Hz, $V_{DD} - V_{SS} = 1.5V$, *(Figure 9)*, (Note 1)				
Doubler Operation		2.5			V
Tripler Operation		3.8			V

Note 1: In oscillator network shown in *Figure 4*.

functional description

A block diagram of the Watch Chip is shown in *Figure 1*. A chip pad layout is shown in *Figure 2* and a package connection diagram in *Figure 3*.

The MM58127 and MM58128 contain an on-chip voltage doubler for display drive and the MM58129 and MM58130 contain an on-chip voltage tripler.

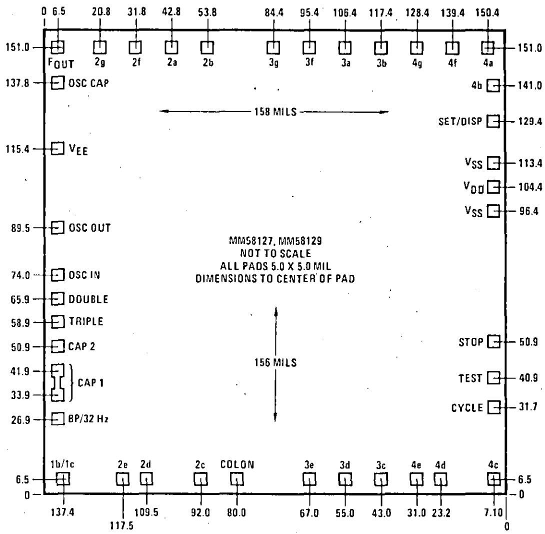


FIGURE 2(a)

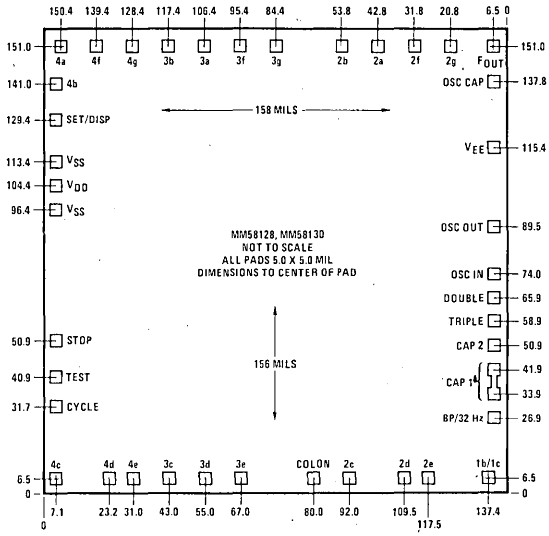


FIGURE 2(b)

MM58127N, MM58129N

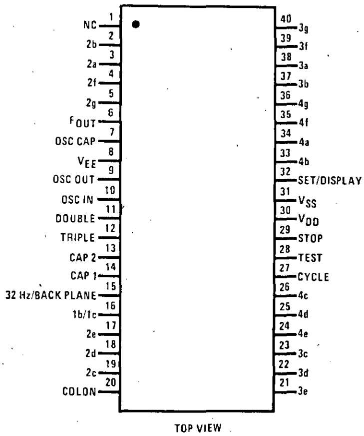


FIGURE 3(a)

MM58128N, MM58130N

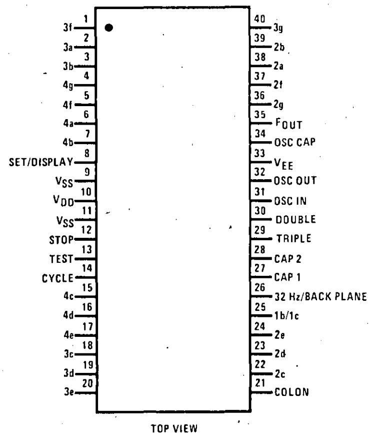


FIGURE 3(b)

functional description (Continued)

Time Base: The precision time base of the watch is provided by connecting a crystal controlled RC network to the on-chip CMOS inverter/amplifier as shown in *Figure 4*. For proper operation, the network should be tuned to 32,768 Hz. Resistor R1 is used to bias the on-chip inverter for class A amplifier operation. Resistor R2 is used to (a) reduce the voltage sensitivity of the network; (b) limit the power dissipation in the quartz crystal; and (c) provide added phase shift for good start-up and low voltage circuit performance. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. The network shown in *Figure 4* provides greater than 100 ppm tuning range when used with standard X-Y flexure quartz crystals trimmed for C_L = 13 pF. Tuning to better than 2 ppm is easily obtainable.

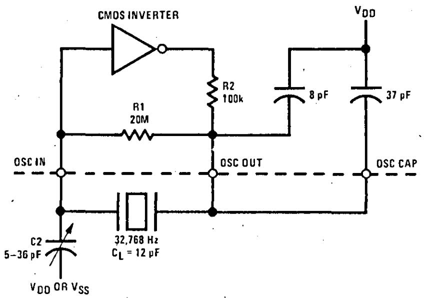


FIGURE 4. Crystal Oscillator Network

The 256/1024 Hz output or the 32 Hz output can be used to monitor the oscillator frequency during initial tuning without disturbing the network itself.

DISPLAY CONTROL

The Hour:Minute, Month Date, and Second displays are controlled by a normally open switch connected to the Set/Display input. Month and Hour are displayed in digit positions 1 and 2. Date, Minute, and Second are displayed in digit positions 3 and 4.

The circuit will normally display Hour and Minute with the colon flashing at a 1 Hz rate (*Figure 5*). Depressing the Set/Display switch will cause Month and Date to be displayed with no colon. The display will automatically return to Hour and Minute display 2.25 ±0.25 seconds after the Set/Display switch has been released. Depressing the Set/Display switch a second time while the Month and Date are being displayed will cause the Second to be displayed until the Set/Display switch is again depressed, returning the display to Hour and Minute. An option is available to display Minutes unit and Seconds in this mode.

All versions have an additional display mode that can be used by depressing the Cycle switch while the watch is in the first display mode described above. The second display mode will alternately display Hour:Minute and Month Date for a period of 2 seconds each. Depressing the Set/Display switch will cause the Second to be displayed. Depressing the Set/Display switch again will return the watch to the second display mode.

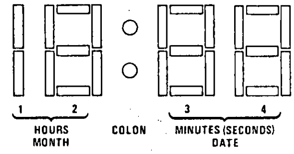


FIGURE 5. Time Display

Leading zero values of month, date, and hours are blanked. The circuit contains a 4 year calendar which will automatically reset the Date Counter to 1 and advance the Month Counter at the end of each month (except for February in Leap Year). The character display font is shown in *Figure 6*.

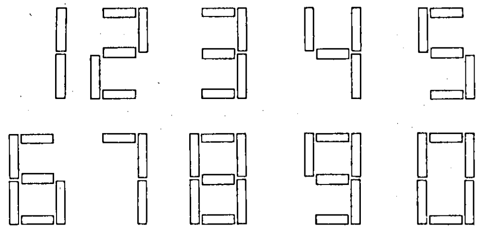


FIGURE 6. Character Display Font

SETTING CONTROL

A normally open switch connected to the Cycle input is used in conjunction with the Set/Display switch to set Month, Date, Hour, Minute, and synchronize Second information.

Month: Depressing the Cycle switch while the watch is in the Alternating Display mode will advance it to the Set Month mode. In this mode the Month will be displayed in digit positions 1 and 2 with no colon. Depressing the Set/Display switch will cause the Month counter to be advanced at a 1 Hz rate as long as the switch is held in.

Date: Depressing the Cycle switch while the watch is in the Set Month mode will advance it to the Set Date mode. In this mode the Date will be displayed in digit positions 3 and 4 with no colon. Depressing the Set/Display switch will cause the Date counter to be advanced at a 1 Hz rate as long as the switch is held in.

Hour: With the watch in the Set Date mode, depressing the Cycle switch will put the watch in the Set Hour mode. In this mode the Hour will be displayed in digit positions 1 and 2 followed by the colon and either an A or a P (for AM or PM) displayed in digit position 4. While in this mode, depressing the Set/Display switch will advance the Hour Counter at a 1 Hz rate until the Set/Display switch is released.

Minute: Depressing the cycle switch while the watch is in the Set Hour mode will advance it to the Set Minute mode. In this mode the Minute will be displayed in digit positions 3 and 4 preceeded by the colon. Depressing the Set/Display switch while still holding the Cycle switch in will cause the Hold mode to be activated but will not advance the Minute counter. Depressing the Set/Display switch after the Cycle switch has been released will cause the Hold mode to be activated and will advance the Minute counter at a 1 Hz rate as long as the switch is held in.

functional description (Continued)

Hold: The Cycle switch is used to advance from the Set Minute state to the first display state. The colon will blink on and off while time is being displayed unless the Hold mode is activated, forcing the colon to remain on continuously. During the second display mode, the colon will remain on during time display. Depressing the Set/Display switch while in either one of the two display states will cause the Hold mode to be cleared, allowing the watch to begin normal operation.

Control state diagrams for the watch are provided in *Figure 7*.

Options are available for 1 or 2 Hz setting rate. In addition, a further option allows a fast set at 4 times the normal rate by pushing both Set/Display and then the cycle switch.

Stop Input: This input pad has an internal resistor to V_{EE} holding it normally at a logical "0." A logical "1" at stop will force all of the display segments "OFF" and stop the oscillator, placing the watch in a static mode to decrease power dissipation during extended periods of storage.

Contact Bounce: Debounce circuitry is provided on the Set/Display and Cycle inputs to remove any logic uncertainty upon either closure or release of switches.

Segment Outputs: The Segment outputs are designed to drive field-effect liquid crystal displays. Each display segment has its own output which furnishes the proper 32 Hz drive signal. By definition, the segment is "OFF" when its drive signal is in phase with the display backplane signal (BP/32 Hz). The segment is "ON" when its drive signal is 180° out of phase with the display backplane signal. Typical output waveforms are shown in *Figure 8*.

Colon Output: The Colon output provides a 32 Hz phase controlled signal identical to the segment outputs. The colon will blink at a 1 Hz rate during time display mode (except for display mode one with the Hold mode activated, and display mode two in the MM58117, MM58119) and remain on continuous while displaying time (Hours or Minutes) during the setting operation.

TEST PADS

Three pads are provided for test purposes.

F_{OUT}: The 256/1024 Hz pad is provided for oscillator tuning.

BP/32 Hz: This input/output pad is under the control of Test. When Test is open or at a logical "0," a 32 Hz signal is provided on BP/32 Hz which can be used to drive the backplane of the LCD unit or to monitor the oscillator frequency without affecting the oscillator circuitry. If Test is at a logical "1," the BP/32 Hz pad is converted into an input and any frequency connected to it will replace the normal internal 32 Hz signal. This feature is provided to allow high speed advancement of the internal counters for testing purposes.

Test: This input pad is used to control the BP/32 Hz pad as described above. When the Test pad is at a logical "1," the phase-control is disconnected from the segment drive outputs and the segment information will be referenced to a logical "0" backplane. Switching the Test pad from a logical "0" to a logical "1" generates a reset pulse that will reset the watch counters to 1 AM on January the first. This places the watch into a known state for testing purpose.

Options: Various mask options of the basic part type are available as standard parts. These are described in Table I. Other combinations of these options can also be made upon special request.

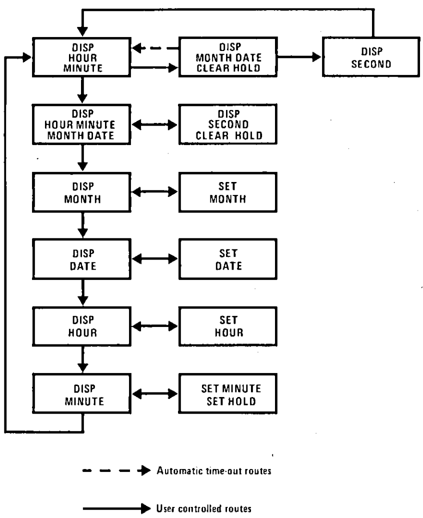


FIGURE 7. Control State Diagram

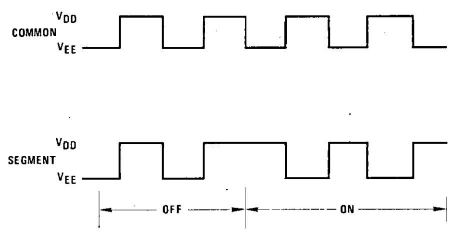
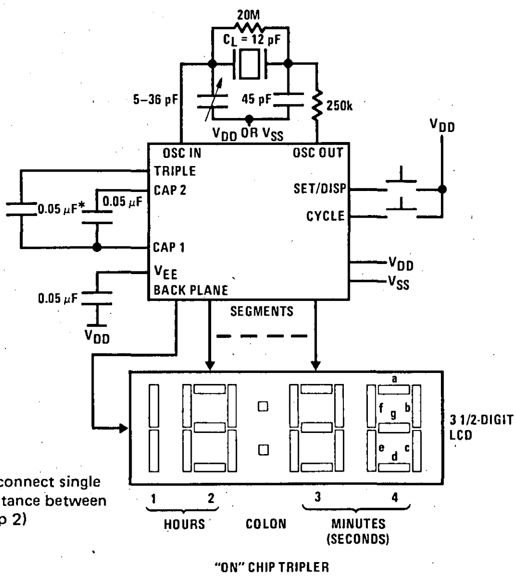


FIGURE 8. Common and Segment Output Signals

functional description (Continued)

TABLE I. Standard Available Options

PART NO.	MOUNTING	F_{OUT}	DEBOUNCE FREQUENCY	SETTING RATE	RUN 2 RATE	MIN/SEC
MM48127	Front	1024	8 Hz	2 Hz/8 Hz	1/4 Hz	Yes
MM48128	Back	TO BE DETERMINED				
MM48129	Front	256	16 Hz	1 Hz	1/4 Hz	No
MM48130	Back	1024	8 Hz	2 Hz/8 Hz	1/4 Hz	Yes



*(For doubler, connect single 0.05 µF capacitance between double and Cap 2)

FIGURE 9. Typical Application in LCD Watch System

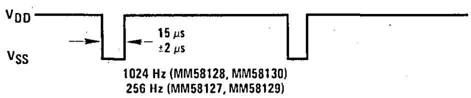


FIGURE 10. 1024 Hz Output

SECTION 8
CALCULATORS

Calculators

MM5734 8-function accumulating memory calculator

general description

The single-chip MM5734 calculator was developed using a metal-gate P-channel enhancement and depletion mode MOS/LSI technology with a primary object of low end-product cost. A complete calculator as shown in *Figure 1* requires only the MM5734 calculator chip, an X-Y matrix keyboard, an NSA1198 or NSA1298 LED display and a 9V battery.

Keyboard decoding and key debounce circuitry, all clocks and timing generators, power-on clear, and 7-segment output display decoding are included on-chip, and require no external components. Segments and digits can usually be driven directly from the MM5734, as the segments typically source 8 mA of peak current and the digit drivers sink 20 mA min.

Leading zero suppression and a floating negative sign allow convenient reading of the display and conserve power. The MM5734 is capable of sensing a low battery voltage and indicates this by displaying a decimal point in digit eight. Up to 8-digits for positive numbers and 7 for negative numbers can be displayed, with the negative sign displayed in the 8th position. Typical current drain of a complete calculator displaying five "5's" is 25 mA.

The MM5734 is capable of decoding a keyboard matrix as shown in *Figure 1.* Three possible models are shown in *Figure 2. Figure 2(c)* illustrates a keyboard scheme which includes all 8 functions with only 23 keys by using a function key (F).

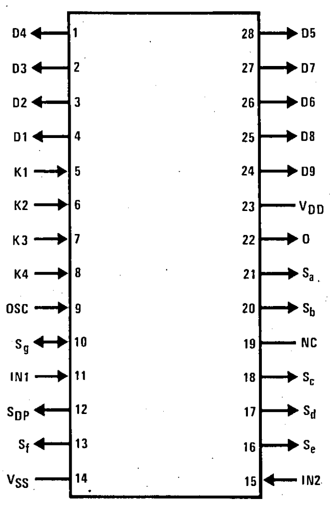
features

- 8-digit, (7-negative), capacity
- 8 functions (+, −, X, ÷, X^2, $\sqrt{X}$, 1/X, %)
- Convenient algebraic notation
- Fully protected accumulating memory (M+, M−)
- Automatic constant independent of memory
- Floating input/floating output
- Power-on clear*
- On-chip oscillator*
- Direct 9V battery compatibility
- Low system cost
- Direct digit drive of LED display
- Low cost X-Y keyboard matrix

*Requires no external components

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5734N
See Package 23

Pin Description

K1–K4	Keyboard Inputs
IN1, IN2	General Purpose Inputs
OSC	Programmable as External Oscillator
D1–D9	Digit Outputs
S_a–S_g	Segment Outputs
SDP	Decimal Point Segment Output
O	General Purpose Output
V_{DD}	−9 Volts
V_{SS}	0 Volts

keyboard outline

	F*	CS*	%*	D9
	F*	X^2*	EX*	D8
√*	M+*	M−*	÷*	D7
1/X*	MR*	MC*	%*	D6
1/X	√	x^2	÷	D5
7	8	9	×	D4
4	5	6	−	D3
1	2	3	+	D2
C CF	0	•	=	D1
K4	K3	K2	K1	

*Double Function Key

absolute maximum ratings

Volume at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Time	0°C to +70°C
Ambient Storage Time	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \le V_{SS} - V_{DD} \le 9.5V$

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD} Operating Supply Current	$V_{DD} = V_{SS} -9.5V$, $T_A = 25°C$		8	15	mA
Keyboard Scan Input Levels CK1 K4					
V_{IH} Logical High Level	$V_{DD} = V_{SS} -6.5V$	V_{SS}−4.0		V_{SS}	V
	$V_{DD} = V_{SS} -9.5V$	V_{SS}−4.0		V_{SS}	V
V_{IL} Logical Low Level	$V_{DD} = V_{SS} -6.5V$, $I_{IL} \le -80\mu A$	V_{DD}		V_{SS}−6.0	V
	$V_{DD} = V_{SS} -9.5V$, $I_{IL} \le -80\mu A$	V_{DD}		V_{SS}−6.3	V
Segment Output Current	$V_{OUT} = V_{SS} -1.0V$, $V_{DD} = V_{SS} -6.5V$	−2.5			mA
	$V_{OUT} = V_{SS} -5.0V$, $V_{DD} = V_{SS} -8.0V$		−8		mA
	$V_{OUT} = V_{SS} -6.5V$, $V_{DD} = V_{SS} -9.5V$			−12	mA
Digit Output Current					
I_{OH} Logical High Level	$V_{OUT} = V_{SS} -2.0V$, $V_{DD} = V_{SS} -6.5V$	−300			µA
I_{OL} Logical Low Level	$V_{OUT} = V_{SS} -3.0V$	20			mA
Ready Output	$V_{DD} = V_{SS} -6.5V$				
V_{OH} Logical High Level	$I_{OUT} = -550\mu A$	V_{SS}−1.0			V
V_{OL} Logical Low Level	$I_{OUT} = 5\mu A$			V_{DD}+6.0	V
Keyboard Resistance K1, K4				5	K

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Display Word Time	*(Figure 3)*	2.9		15.4	ms
Display Digit Time	*(Figure 3)*	0.32		1.71	ms
Interdigit Blanking Time (Segment Outputs)	*(Figure 3)*		175		µs
Ready Transition Times					
High-to-Low	$V_{DD} = V_{SS} -6.5V$			20	µs
Low-to-High	C_L = 50 pF			1	µs
Digit Output Transition Times					
High-to-Low	C_L = 100 pF		8		µs
Low-to-High			3		µs
Keyboard Inputs High-to-Low Transition Time After Key Release	C_L = 25 pF		6		µs
Key Bounce-Out Stability Time (The time a keyboard input must be continuously lower than the maximum logical low level to be accepted as a key closure, or higher than the minimum logical high level to be accepted as a key release.)		11.7		61.7	ms
Worst-Case Calculation Time				0.56	s

functional description

The MM5734 is a calculator chip which contains five data registers: (1) entry, (2) accumulator, (3) 2 working and (4) memory, each consisting of 8 digits, sign, and decimal point. The entry register is always displayed. It contains digit entries from the keyboard, and results of all functions except M+ and M–. The accumulator is used in all arithmetic functions and stores a copy of the entry register on all results. This allows another number to be entered without losing an intermediate result. Multiply and divide requires three registers to perform the function and save the divisor, or multiplier. The working register is provided to perform these functions in conjunction with the entry and accumulator registers. A second working register is used to store the constant in chain operations while performing X^2 or 1/X. This allows chain operation using X^2, 1/X and $\sqrt{X}$.

The memory register is used only to store a number to be used later. It is fully protected during all operations, and is only modified by depressing a "MS," "M+," or "M–" key. Power-on clears all of the registers including the memory register.

The MM5734 performs the "+," "–," "X" and "÷" functions using algebraic notation. This requires the use of a mode register and a terminate flag. The mode register directs the machine to the proper function (add, subtract, multiply or divide) with each new key entry. After the function has been performed, the key entered is used to modify the mode register.

The terminate flag is set on "=" and sometimes on "%" and "C." This signifies the end of the problem. The MM5734 allows for full floating entries and intermediate results.

If the terminate flag is set, a "+," "–," "X" or "÷" key signals the beginning of a new problem. The number being displayed is copied into the accumulator register and the mode register assumes the mode of the key entered. The terminate flag is always reset by the "+," "–," "X" and "÷" keys.

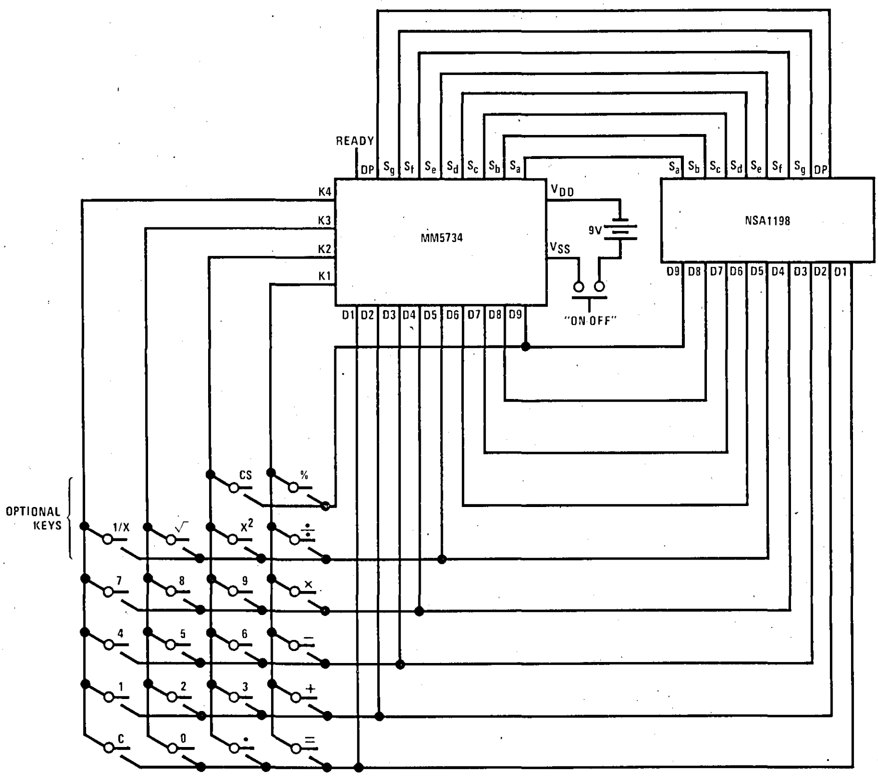


FIGURE 1A. Complete Calculator Schematic

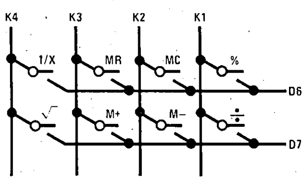


FIGURE 1(b). Optional Keys

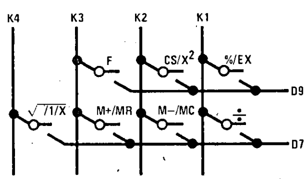


FIGURE 1(c). Optional Keys

OPERATION IN THE ADD AND SUBTRACT MODE

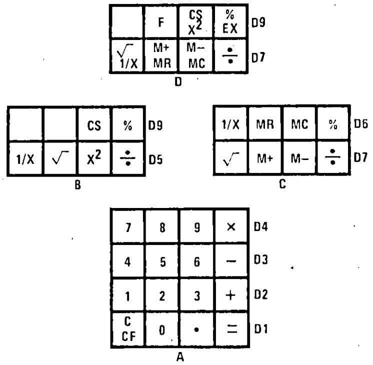


FIGURE 2

If the terminate flag is set, an "=" key will result in a constant add/subtract. The number in the accumulator will be added to (or subtracted from) the number being displayed. The result is right-justified and displayed in the entry register. Accumulator and mode registers are not altered, allowing for constant operations.

If the terminate flag is not set and a number has been entered from the keyboard, or memory register, a "+," "−," "X" or "÷" key will result in an addition or subtraction. The entry register will be added to or subtracted from the accumulator and the new running total will be displayed in the entry register and copied into the accumulator register. The mode will be altered according to which key is entered.

If the terminate flag is not set, and a number has not been entered from the keyboard, or memory, a "+," "−," "X," "÷" key will only change the mode register to the new key entry.

If the terminate flag is not set, an "=" key will add/subtract the number being displayed to/from the number in the accumulator register. The number being displayed is transferred to the accumulator, and the result of the operation is displayed in the entry register. The terminate flag is set, conditioning the calculator for constant, add/subtract operation. The number being displayed previous to the "=" key is stored in the accumulator as the constant.

Operation of the "%" key in add/subtract mode, with the terminate flag reset, will multiply the accumulator by the last entry, divide the result by 100, and display it in the entry register. The mode register remains as it was in the add/subtract mode. All of the above is required to perform the percent add on or discount problems. Depression of an "=" key after the "%" key will either tax or discount the original number as a function of the mode register and the last entry.

Operation of the "%" key in add/subtract mode, with the terminate flag set, will shift the decimal point of the number being displayed two places to the left and copy it into the accumulator register. The mode is set to multiply and the terminate flag remains set.

Operation in the Multiply Mode

If the terminate flag is set, an "=" key will result in a constant multiply operation. The number being displayed is multiplied by the constant stored in the accumulator register. The result is displayed in the entry register and the accumulator and mode registers are not altered, allowing for constant operation. Repeated depressions of the "=" key can be used to raise a number to an integer power, i.e., "C," "C," "5.2," "X," "=," "=," "=," computes 5.2^4.

The constant in multiplication, as well as in addition, subtraction and division is the last number entered. For the sequence: "C," "C," "3," "÷," "4," "X," "2," "=" the constant multiplier for future problems is 2.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the display will be multiplied by the contents of the accumulator, and the results will be displayed in the entry register. The number previously in the entry register is stored in the accumulator register and the terminate flag is set.

If the terminate flag is not set, and a number has been entered from the keyboard or memory register, a "+," "−," "X" or "÷" key will result in a multiplication. The number being displayed will be multiplied by the number residing in the accumulator register. The result will be copied into the accumulator and displayed in the entry register. The mode register is updated as a function of the key depressed.

Operation of the "%" key while in multiply mode looks exactly the same as an "=" key except the decimal point of the display is shifted two positions to the left before the multiplication takes place.

Operation in the Divide Mode

If the terminate flag is set, an "=" key will result in constant divide operation. The number being displayed is divided by the constant stored in the accumulator register. The accumulator and mode registers are not altered allowing for constant operations. Repeated depressions of the "=" key will result in repeated divisions by the constant. Thus, it is possible to raise a number to a negative power using the sequence "C," "C," "1," "÷," "No.," "=," "=," etc.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the accumulator register will be divided by the number being displayed. The result is transferred to the entry register and displayed. The terminate flag is set and the divisor is stored in the accumulator register.

If the terminate flag is not set, a "+," "−," "X" or "÷" key will result in a division. The number in the accumulator register will be divided by the number being displayed. The results are displayed in the entry register, and a copy of the result is stored in the accumulator. The mode register is modified to reflect the latest key entry.

Operation of the "%" key while in divide mode looks exactly the same as the "=" key except the decimal point of the display is shifted two positions to the left before division takes place.

Error Conditions

If any of the operations mentioned above generates a number larger than 99999999, an error will occur. An error is indicated by displaying the 8 most significant digits and sign with all 9 decimal points. The first depression of the "C" key will clear the error condition, and all registers except the memory register.

It is not possible to generate an error during number entry. The ninth and subsequent digits entered are ignored.

Leading Zero Suppression and Negative Sign

In order to conserve battery power, the MM5734 blanks leading zeros on all numbers displayed. No more than 7 decimal digits are permitted. The MM5734 displays 8 digits for positive numbers, and 7 digits negative, allowing the 8-digit position for a negative sign. The negative sign floats to the left of the most significant digit on numbers containing less than 7 digits.

Power-On Condition

The MM5734 has an internal power-on clear circuit which clears all registers to zero, places the mode to add and sets the terminate flag. A zero and decimal point are displayed.

Keyboard Bounce and Noise Rejection

The MM5734 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint. A simple X-Y keyboard matrix can be used with all the necessary decoding accomplished within this MM5734.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3, K4, is forced more negative than the logical low level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after 11 word times if the key input is still at a logical low level. As long as the key is held down (and the key input remains low) no further entry is allowed. When the key input changes to a logical high level, the internal counter starts an 11 word timeout for key release. During both, entry and release timeouts, the key inputs are sampled during every display period for valid levels. If they are found invalid, the counter is reset and the calculator resumes scanning the keyboard.

The "Ready" signal indicates calculator status. When the calculator is in an "idle" state, the output is at a logical high level (near V_{SS}). When a key is closed, the internal key entry timer is started. "Ready" remains high until the timeout is completed and the key entry is accepted as valid, then goes low. It remains at a logical low level until the function initiated by the key is completed and the key is released. The low-to-high transition indicates the calculator has returned to an idle state and a new key can be entered.

Function of Keys

Some of the keys operate differently when in the data or number entry condition. The MM5734 switches to entry condition when entering numbers and leaves this condition after most function keys. The following paragraphs which discussed the action of "+," "–," "X," "÷" and "%" keys and the examples given in later sections will act in further explaining these actions.

Clear Key, "CE/C"

While in the number entry condition, one depression will clear the entry register to zero. The machine then leaves the number entry state.

If the error condition is displayed, one depression will clear the error, and all registers except the memory register. The machine could not be in the number entry condition with the error flag set.

If the error flag is not set and the machine is not in the number entry condition, one depression of "CE/C" key will clear the entry and accumulator registers. It also places the machine in the add mode and sets the terminate flag. The memory register remains unchanged.

Number Keys 0–9

If not in the number entry condition, a number key will clear the display and then enter the value of the key into the LSD. The digits are displayed as they are entered and the machine assumes the number entry condition.

If in the number entry condition, the entry register is shifted left one position and the key depressed is entered into the LSD. Digits entered after 8 digits positive, or 7 digits negative, will be ignored. Digits entered after 7 decimal digits are displayed will also be ignored.

Square Root Key "$\sqrt{X}$"

The square root key extracts the square root of the absolute value of the number being displayed in the entry register.

The mode of the calculator remains unchanged. This enables square root operations in the middle of chain calculations. For example:

KEY	DISPLAY	KEY	DISPLAY	KEY	DISPLAY
A	A	A	A	11	11
$\sqrt{\ }$	$\sqrt{A}$	X	A	+	11
+	$\sqrt{A}$	B	B	5	5
B	B	$\sqrt{\ }$	$\sqrt{B}$	=	16
$\sqrt{\ }$	$\sqrt{B}$	=	$A\sqrt{B}$	$\sqrt{\ }$	4
=	$\sqrt{A}+\sqrt{B}$			6	6
				=	11
				9	9
				$\sqrt{\ }$	3
				=	8

Square

Depression of the "X^2" key squares the number in the display register, and displays the results. The mode of the calculator remains unchanged. This enables square operations in the middle of chain calculations.

Inverse

Depression of the "1/X" key takes the inverse of the number in the display register and displays the results. The mode of the calculator remains unchanged. This enables inverse operations in the middle of chain calculations.

F Key (Function Key)

The "F" key translates the following key depressed to this code of the key below it, *Figure 2*, if it is a DOUBLE FUNCTION KEY. If the CLEAR KEY is the following key, the FUNCTION CONDITION is removed leaving the calculator in its previous mode.

SQUARE PROBLEMS

KEYS	DISPLAY	COMMENTS
72	72.	
X^2	5184.	Squares display
7	7.	
CS	−7.	
X^2	49.	Squares minus numbers
+	49.	Chain capabilities
8	8.	
X^2	64.	Squares display (mode unchanged)
=	113.	Completes addition, terminates problems

INVERSE PROBLEMS

KEY	DISPLAY	COMMENTS
5	5.	
1/X	0.2	Takes inverse of display
4	4.	
1/X	0.25	Takes inverse
+		
8	8	
1/X	0.125	Takes inverse (mode unchanged)
=	0.375	Completes addition, terminates problem

MM5737 calculator—8-digit, 4-function, floating decimal point

general description

The MM5737 single-chip calculator was developed using a metal gate, P-channel, enhancement and depletion mode MOS process with low end-product cost as the primary objective. A complete calculator, as shown in *Figure 1*, requires only a keyboard, DM8864 digit driver, nine digit LED display and a 9V battery with appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and output 7-segment display decoding are all included on-chip and require no external discrete components. LED segments can be driven directly from the MM5737 as it typically sources 8.0 mA of peak current. [Note: The typical duty cycle of each digit is 0.111; average LED segment current is therefore approximately 0.111 (8.0 mA), or 0.89 mA. Correspondingly, the worst-case average segment current is 0.111 (5.0 mA), or 0.555 mA.] The ninth digit is used for the negative sign of an eight digit number, and as an error indicator. Negative results less than eight digits will have the negative sign displayed one digit to the left of the most-significant-digit (MSD). The DM8864 digit driver is capable of indicating a low battery voltage condition by turning on the ninth digit decimal point—which does not hinder the actual calculator operation.

Leading and trailing zero suppression allows convenient reading of the right justified display and conserves power. Battery life is estimated to be 10 to 20 hours, depending on battery quality, operating schedule and the average number of digits displayed.

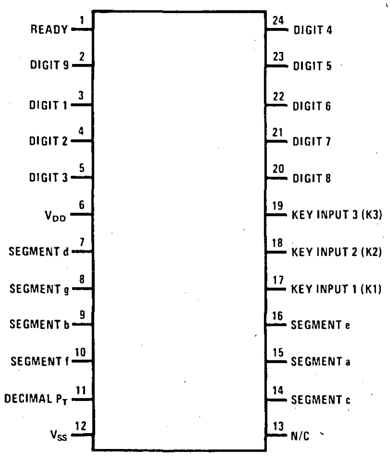
The Ready output signal is used to indicate when the calculator is performing an operation (Table I). It is useful in testing of the device or when the MM5737 is used as part of a larger system and is required to interface with other logic. (Another feature that is important in such applications is the ability to reduce the key debounce time from seven word times to four word times by forcing the Digit 7 output high during Digit 9 time.)

features

- Full 8-digit entry and display capacity
- Four functions (+, −, x, ÷)
- Floating negative sign indicator is always displayed one digit to left of MSD
- Convenient algebraic key entry notation
- Floating point input and output
- Chain operations
- Direct 9V battery compatibility; low power
- Direct interface to LED segments
- No external components are required other than display digit driver, keyboard and LED display for complete calculator
- Overflow and divide-by-zero error indication
- Right justified entry and results, with leading and trailing zero suppression

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5737N
See Package 22

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}. (All other pins connected to V_{SS}).	V_{SS} + 0.3V to V_{SS} − 12.0
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$
(V_{SS} always defined as most positive supply voltage.)

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS} -9.5V$ $T_A = 25°C$		8.0	14.0	mA
Keyboard Scan Input Levels (K1, K2 and K3)					
Logical High Level (V_{IH})	$V_{SS} -6.5V \leq V_{DD} \leq V_{SS} -9.5V$	V_{SS}−2.5			V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS} -6.5V$			V_{SS}−5.0	V
	$V_{DD} = V_{SS} -9.5V$			V_{SS}−6.0	V
Digit Output Levels (Note 1)					
Logical High Level (V_{OH})	$V_{SS} -6.5V \leq V_{DD} \leq V_{SS} -9.5V$	V_{SS}−1.5			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS} -6.5V$			V_{SS}−6.0	V
	$V_{DD} = V_{SS} -9.5V$			V_{SS}−7.0	V
Segment Output Current (Sa through Sg and Decimal Point)	$T_A = 25°C$				
	$V_{OUT} = V_{SS} -3.8V$, $V_{DD} = V_{SS} -6.5V$	−5.0	−8.0		mA
	$V_{OUT} = V_{SS} -5.0V$, $V_{DD} = V_{SS} -8.0V$		−10.0		mA
	$V_{OUT} = V_{SS} -6.5V$, $V_{DD} = V_{SS} -9.5V$			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	$I_{OUT} = -0.4$ mA	V_{SS}−1.0			V
Logical Low Level (V_{OL})	$I_{OUT} = 10\mu A$			V_{DD}+1.0	V

Note 1: With digit connected through key to K-line and to DM8864.

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time *(Figure 2)*		0.63	1.5	5.2	ms
Digit Time *(Figure 2)*		70	170	580	µs
Interdigit Blanking Time *(Figure 2)*			4		µs
Digit Output Transition Times (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF		2		µs
Keyboard Inputs High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		µs
Ready Output Propagation Time *(Figure 3)*					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	60	140	480	µs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF	0.06	0.5	1.5	ms
Key Bounce-out Stability Time (The time a keyboard input must be continuously higher than the minimum logical high level to be accepted as a key closure, or continuously lower than the maximum logical low level to be accepted as a key release.)		4.2	10.5	35	ms
Calculation Time for 99999999 ÷ 1 = 99999999		90	220	760	ms

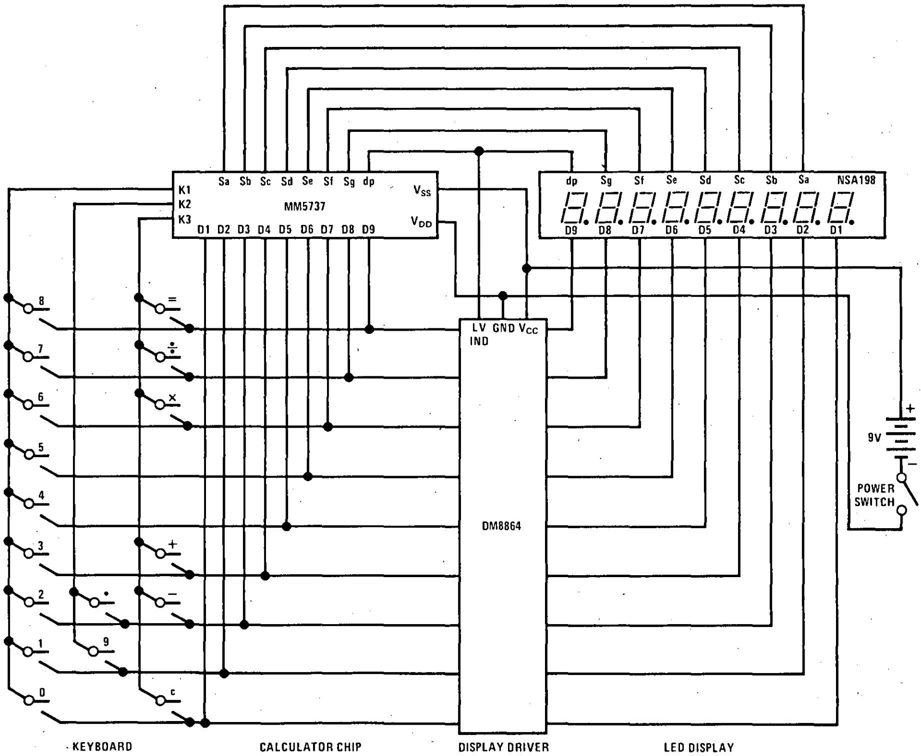


FIGURE 1. Complete Calculator Schematic

TABLE I. Ready Signal Description

CALCULATOR FUNCTION	READY SIGNAL
Idle	*READY* is quiescently at a Logical High Level ($\sim V_{SS}$).
Key Entry and Functional Operation	When a key is depressed, the bounce-out stability timer is initiated. *READY* remains high until the bounce-out time is completed and the key is entered, at which time it changes to a Logical Low Level ($\sim V_{DD}$).
Key Release and Return to Idle	*READY* remains low until key release is debounced and the calculator returns to the idle state. The low to high transition signals the return to idle. (The display may lag the *READY* by up to eight word times.)

KEY INPUT BOUNCE AND NOISE REJECTION

The MM5737 calculator chip is designed to interface with low cost keyboards, which are often the least desirable from a noise and false entry standpoint.

A key closure is sensed by the calculator chip when one of the Key Input Lines, K1, K2 or K3 is forced more positive than the Logical High Level specified in the Electrical Specifications. At the instant of closure, an internal "Key Bounce-out Stability Time" counter is started. Any significant voltage perturbation occurring on the switched key input during timeout will reset the timer. Hence, a key is not accepted as a valid entry until noise or ringing has stopped and the stability time counter has timed out. Noise that persists will inhibit key entry indefinitely. Key release is timed in the same manner.

One of the popular types of low cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5737 defines a series contact resistance up to 50 kΩ as a valid key closure, providing an optimum interface to that type of keyboard as well as more conventional types.

ERROR CONDITIONS

In the event of an overflow, the MM5737 will display an "E" in the leftmost digit and at least seven of the significant digits of the answer. Division by zero results in an "E" with eight trailing zeroes. Once in an error condition, all keys except the clear key are ignored.

KEY OPERATIONS

Clear Key

Operation after a number entry clears the entry and displays a previous result. Second depression clears all registers and displays a zero without decimal point in the LSD. Operation after a function key (+, −, x, ÷ or =) clears all registers and displays a zero without decimal point. Two depressions are always required after power is applied.

Number Entries

First entry clears the display register and enters the number into the least significant digit (LSD) of the display register. Second through eighth entry shifts the display register left one digit and enters the number into the LSD. The ninth, and subsequent entries, are ignored and no error condition is generated. Because only seven positions are allowed to follow the decimal point, the eighth and subsequent entries after a decimal point entry are ignored.

Decimal Point

First depression of this key in a number entry will enter a decimal point in the LSD position of the display register. Subsequent depressions of the decimal point key before any function key will be ignored.

Add, Subtract, Multiply or Divide Keys

First depression after a number entry will terminate the entry, perform the previously recorded operation, if any, and record the function key depressed as the next operation to be performed after another number entry. Subsequent depressions of any function key, without an interceding number or decimal point entry will supersede the previous function as the next to be performed. After an equal key, the displayed result of the equal operation will be re-entered and the function key depressed will become the next operation to be performed after a number entry is followed by another function key (including equal).

Equal

First depression after a number entry will terminate the entry, perform the previously recorded operation and record the fact that an equal key has been depressed. Depression after the add, subtract or divide keys, without an interceding number or decimal point entry, will be ignored. After a multiply key, the number being displayed will be squared.

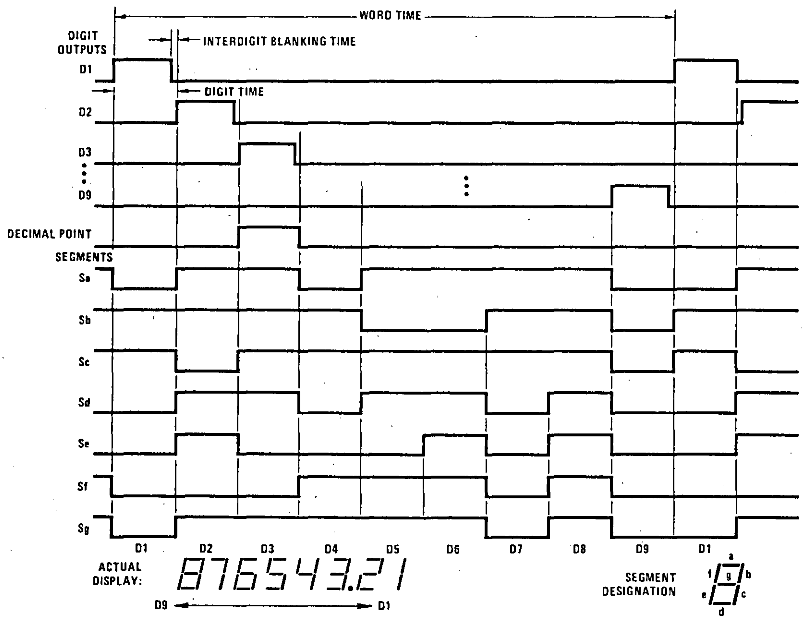


FIGURE 2. Display Timing Diagram

8

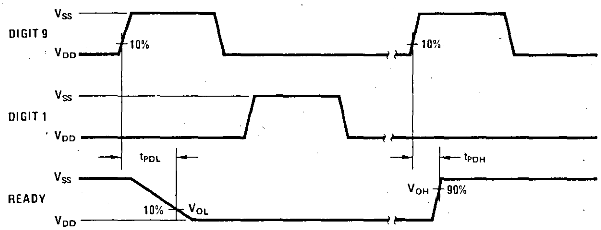


FIGURE 3. Ready Output Timing

sample problems

I. Single Calculations

5 x 3.14 = 15.7

Key	Display	Comments
C		Two clears are required after power-up.
C	0	
5	5	
x	5	
3	3	
.	3.	
1	3.1	
4	3.14	
=	15.7	

II. Chain Calculations

A. 23.37 + 243.00 − 489.16 = −222.79

Key	Display	Comments
C		
C	0	
23.37	23.37	
+	23.37	
243	243	
x (Wrong Function Key)	266.37	Function key completes previously recorded "+" operation.
−	266.37	Wrong "X" function key is updated to "−."
489.17	489.17	
C	266.37	
489.16	489.16	Number entry error is cleared and corrected. Note the floating negative sign.
=	−222.79	

B. Find square root of 169 using a modified Newton approximation method. Let N represent the squared number and X_0 the initial estimate. The first approximation, X_1, is

$X_1 = (N/X_0 + X_0)/2$
If X_0 is 15,
$X_1 = (169/15 + 15)/2$
$X_2 = (169/X_1 + X_1)/2$
$X_3 = (169/X_2 + X_2)/2$, etc.

Key	Display	Comments
C		
C	0	
169	169	
÷	169	
15	15	
+	11.266666	
15	15	
÷	26.266666	
2	2	
=	13.133333	Result is X_1
169	169	
÷	169	
13.13	13.13	Four digits are conveniently remembered

sample problems (con't)

II. Chain Calculations (continued)

Key	Display	Comments
+	12.871287	
13.13	13.13	
÷	26.001287	
2	2	
=	13.000643	Result is X_2, which is usually adequate. If more accuracy is required, continue the iteration.

III. Auto Squaring.

A. $5.25^2 = 27.5625$

Key	Display	Comments
C		
C	0	
5.25	5.25	
x	5.25	
=	27.5625	Number in display register is squared.

B. $5.25^5 = 3988.3798$

Key	Display	Comments
C		
C	0	
5.25	5.25	
x	5.25	
=	27.5625	Auto square = 5.25^2
x	27.5625	
=	759.6914	Auto square = 5.25^4
x	759.6914	
5.25	5.25	
=	3988.3798	Result is 5.25^5

MM5758 scientific calculator

general description

The single-chip MM5758 Scientific Calculator is another MOS/LSI product from National Semiconductor using a metal-gate, P-channel enhancement/depletion mode technology to achieve low system cost. A complete calculator performs a wide range of complex scientific problems, yet consists of only the MM5758, two display driver ICs, the NSA5101 LED display, a keyboard and power supply *(Figure 1)*. No discrete components are required.

An internal power-on clear circuit automatically clears all registers, including the storage memory and four-register operational stack, when power is initially applied to the chip.

The MM5758 performs trigonometric, logarithmic, exponentiation, power and square root functions simply by pressing a key. It computes and displays numbers over a range of $\pm 9.9999999 \times 10^{\pm 99}$. A four-register operational stack simplifies computation of problems with multi-nested terms and reverse polish entry notation provides a logical and consistent method of keying in even the most complex problems.

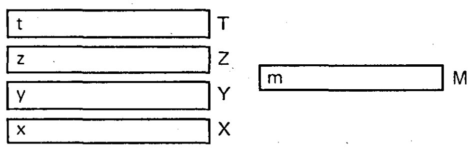
The displayed output has an eight digit mantissa with a two digit exponent; both the mantissa and exponent display an additional sign digit. Sign information is presented to the display by the calculator chip during a single digit time, but the NSA5101 display physically separates the two as shown in *Figure 2*.

All computed results greater than 99999999. or less than 0.1 are automatically converted to scientific notation. Trailing zero suppression of the mantissa allows convenient reading of the left justified display and conserves power. The exponent digits are blanked if no exponent is displayed. The most-significant-digit of the exponent is not blanked, even if it is a zero, when an exponent is being displayed. A low battery indication, activated by sensing circuitry in the DS8868, is included in the mantissa sign digit.

A Ready output signal is used to indicate calculator status. It is useful in providing synchronization information during testing and when the MM5758 is used with other logic; e.g., with the MM5766 Programmer.

Thirty-six keys are arranged within a four-by-eleven matrix (Table 1 and *Figure 2*). Dual function keys are not required.

The user has access to five registers designated X, Y, Z, T and M. X is the display and entry register and the bottom of a "push-up" operational stack that includes registers Y, Z and T.

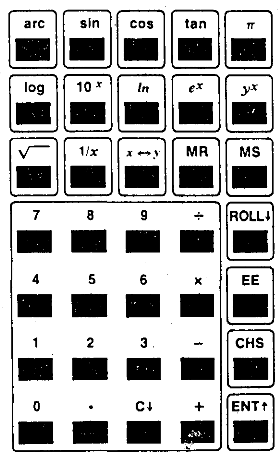


The contents of the storage register M are replaced with the contents of the X-register by using the "STO" key. The memory recall key, "RCL," copies M into register X without disturbing the value of M. M is cleared automatically at power-on or by storing a zero. All registers contain eight mantissa digits, two exponent digits and the sign information for each.

features

- Enters, computes and displays numbers as large as $\pm 9.9999999 \times 10^{99}$ and as small as $\pm 1 \times 10^{-99}$
- Complete slide-rule capability
  - Arithmetic functions: $+, -, \times, \div, 1/x, \sqrt{x}$
  - Logarithmic functions: $\ln x$, $\log x$, e^x, 10^x
  - Power function: Y^x
  - Trigonometric functions: sin x, cos x, tan x, arc sin x, arc cos x, arc tan x
  - Other functions: π, exchange, change sign
- Reverse polish notation
- Four-register operational stack with roll capability
- Independent two key storage register
- Floating point input and output
- Power-on clear
- Designed-in low system cost
- Automatic display cutoff

sample keyboard



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All other pins connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$7.2\text{ V} \leq V_{SS} - V_{DD} \leq 8.8\text{V}$

V_{SS} is always the most positive supply voltage.

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}$ −8.8V, T_A = 25°C		12.0	20.0	mA
Keyboard Scan Input Levels (K1 through K4)					
Logical High Level		V_{SS}−2.5			V
Logical Low Level				V_{DD}+1.5	V
Display Reset Input Levels					
Logical High Level		V_{SS}−1.5			V
Logical Low Level				V_{DD}+1.5	V
Encoded Digits Output Current (D_A through D_D)					
Logical High Level (I_{OH})	$V_{OUT} = V_{DD}$ + 1.0V	−0.5		−2.50	mA
Logical Low Level (I_{OL})	$V_{OUT} = V_{DD}$			−50	µA
Low Voltage Indicator Level (V_{IH}) (Digit D_A must be forced to a V_{IH} voltage level during the IDLE digit time to cause Segment S_b to be turned "ON" at digit time D1.		V_{DD}+2.8		V_{SS}	V
Segment and Decimal Point Output Current (Sa through Sg, DP)					
Logical High Level (I_{OH})	$V_{OUT} = V_{DD}$ + 5.4V	−550			µA
Logical Low Level (I_{OL})	$V_{OUT} = V_{DD}$ + 1.5V			−10	µA
Ready Output Levels					
Logical High Level (V_{OH})	I_{OUT} = −0.4 mA	V_{SS}−1.0			V
Logical Low Level (V_{OL})	I_{OUT} = 10µA			V_{DD}+1.0	V

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time *(Figure 3)*		0.5	1.3	2.2	ms
Digit Time *(Figure 3)*		42	108	183	µs
Interdigit Blanking Time *(Figure 3)*		3.5	8.0	14.0	µs
Keyboard Scan Inputs (K1 through K4) Low to High Transition Time (during Interdigit Blanking Time), (t_{PDH})	C_{LOAD} = 100 pF			14.0	µs
Ready Output Propagation Time *(Figure 4)*					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	30		115	µs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF	30		120	µs
Key Bounce-out Stability Time. (The time a keyboard scan input, K1, K2, K3 or K4, must be continuously connected to a digit to be accepted as a key closure, or lower than the maximum Logical Low Level to be accepted as a key release.) *(Figure 5)*		3.5	9.1	15.4	ms
Display Cutoff Time (The time after the last valid key closure at which all digits except the most-significant-digit of the mantissa will be blanked.)			50		second
Calculation Times					
Square Root			0.50	0.90	second
LOG X or LN X			0.85	1.50	second
10^x or e^x			1.00	1.75	second
Y^x			1.80	3.10	second
SIN X, COS X or TAN X			1.30	2.20	second
ARC SIN X or ARC COS X			1.40	2.40	second
ARC TAN X			0.85	1.50	second

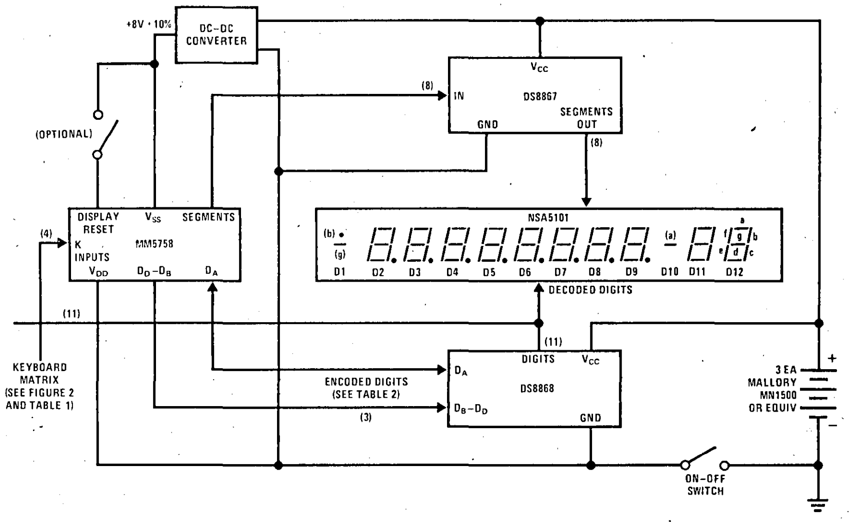


FIGURE 1. Block Diagram of Complete Handheld Scientific Calculator Using MM5758.

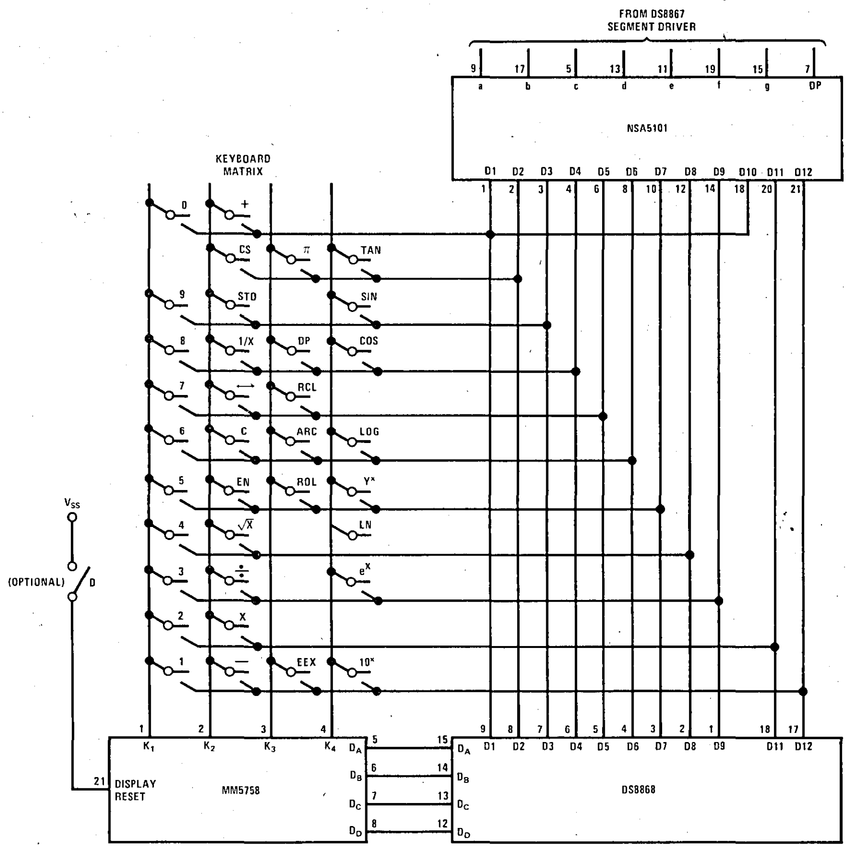


FIGURE 2. Digits Interconnection Detail For Scientific Calculator.

SCALING OF DISPLAYED NUMBERS

Computed results are displayed in either floating point or scientific notation. Answers in the range between 0.1 and 99999999. are displayed in floating point format; otherwise scientific notation is used. For example: 123.4 is displayed as written; whereas, 123.4 million would appear as 1.234×10^8. The smallest magnitude displayed is $\pm 1.0 \times 10^{-99}$, and the largest $\pm 9.9999999 \times 10^{99}$. Number entries are always displayed in the manner entered until "ENT" is depressed, after which they appear scaled.

KEYBOUNCE AND NOISE REJECTION

The MM5758 is designed to interface with most low-cost keyboards, which are often the least desireable from a false or multiple entry standpoint.

When a key closure is sensed by the calculator, an internal timeout is started. Any voltage perturbations of significant magnitude which occur on the Key Input Lines (K1, K2, K3 or K4) during the timeout will reset the timer to zero. A key is accepted as valid after a noise-free timeout period; noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

The internal timeout period (Key Bounceout Stability Time) is normally seven word times. By forcing digit D_B to a Logical High State during Digit Timing State D12 time (Table II), the Stability Time is reduced to four word times.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately 50 seconds, an internal automatic display cutoff circuit will modify the encoded digit output sequence sent to the DS8868 Decoder/Driver to be the blanking input code (Table II) during all digit times except the most-significant of the mantissa (D2). Thus, in the cutoff power saving mode, only one digit is displayed. The blanking code has been selected to also be the minimum power case for the DS8868.

Any of the D11 ("CS," "π" or "TAN") keys will restore the display; to restore the display without modifying the status of the calculator use the "CS" key twice, or momentarily force the Display Reset high. The automatic display cutoff feature can be disabled by hardwiring the Display Reset pin to V_{SS}.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 4 and 5*. It remains at a Logical Low Level until the function initiated by the key is completed and the key is released and timed out. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

TABLE I. Keyboard Matrix

SWITCH INPUTS	DIGIT TIMING STATES									
	D1	D2	D3	D4	D5	D6	D7	D8	D9	D11	D12
K1	0		9	8	7	6	5	4	3	2	1
K2	+	CS	STO	1/X	↔	C	EN	$\sqrt{X}$	÷	X	–
K3		π		•	RCL	ARC	ROL				EEX
K4		TAN	SIN	COS		LOG	Y^x	LN	e^x		10^x

TABLE II. Digits Timing State Truth Table

ENCODED DIGITS				DECODED DIGIT STATES (DS8868)											
D_D	D_C	D_B	D_A	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12
H	H	L	L	ON											
H	H	H	H		ON										
L	H	H	H			ON									
H	L	H	H				ON								
L	H	L	H					ON							
H	L	H	L						ON						
H	H	L	H							ON					
L	H	H	L								ON				
L	L	H	H									ON			
H	H	H	L										ON		
L	L	L	H											ON	
H	L	L	L												ON
L	L	L	L												

ON = DS8868 output buffer will sink $\geq$ 110 mA @ $V_{OUT} \leq 0.4V$

H = Logical High State ($\sim V_{SS}$)

L = Logical Low State ($\sim V_{DD}$)

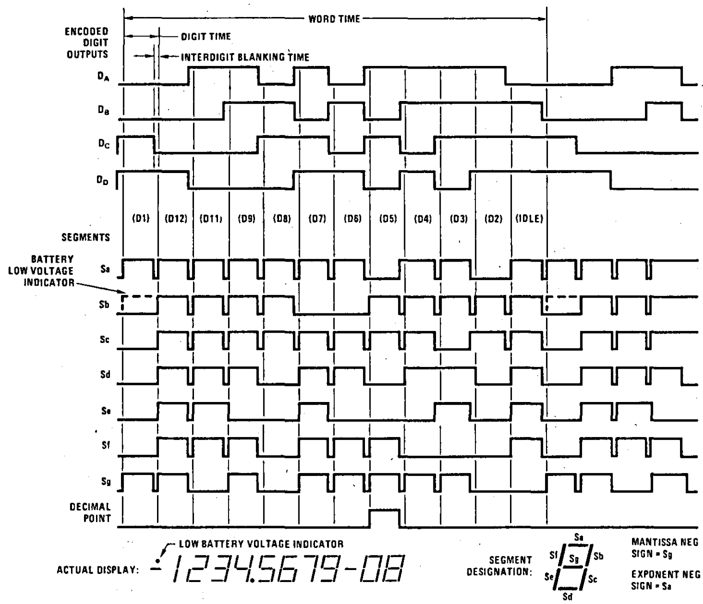


FIGURE 3. Display Timing Diagram

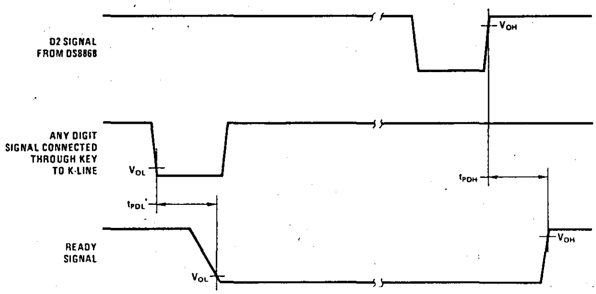


FIGURE 4. Ready Timing

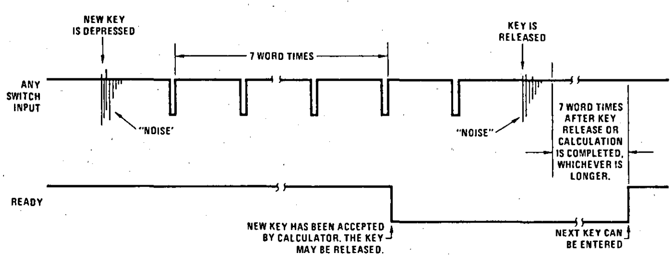


FIGURE 5. Functional Description of Ready Signal and Key Entry.

ERROR INDICATION

In the event of an operating error, the MM5758 will display all zeros and decimal points. Improper operations or calculations are summarized in Table III. All square root computations are of the absolute value of X; therefore, the square root of a negative number is not considered an invalid operation.

An error condition is reset by pressing "C." All registers in the stack are lost and replaced with zeros. M is saved.

TABLE III. Conditions for Error Indication

FUNCTION	CONDITION (REGISTER X ≡ X)
÷ or 1/X	$\|X\| = 0$
Y^x	$Y < 0$, $X \text{ LOG } Y > 99$
e^x	$\|X\| > 230$
10^x	$\|X\| > 99$
LOG X or LN X	$X \leq 0$
SIN X, COS X, TAN X	$X < 0$ or $X > 90$
ARC SIN X or ARC COS X	$X < 0$ or $X > 1$
ARC TAN X	$X < 0$

KEY OPERATIONS

Clear Key, "C"

Clears X, pushes Y down to X, Z to Y, T to Z and places a zero in T. Subsequent depressions perform the same operation; thus, four "C" depressions will clear a completely full stack. If the display indicates an error condition exists, the "C" key clears X, Y, Z and T. Storage memory M is not affected by any "C" operation.

Number Entries

The first numeral of a number entry following any function, other than "EN," raises the stack and T is lost. Numerals are entered and displayed from left to right. Following "EN" the first number entry is placed in X without affecting the rest of the stack. Ninth and subsequent entries of the mantissa are ignored; third and subsequent entries of the exponent are entered as a new least-significant-digit, and the previous most-significant-digit is lost.

Decimal Point, "."

Places a decimal point on the right side of the least-significant-digit being displayed during entry of the mantissa. It is invalid during exponent entry and clears the X-register to zero (starting a new number entry).

Change Sign Key, "CS"

Changes the sign of X. In the exponent entry mode, it changes the exponent sign. It does not terminate entry and therefore can be depressed at any time during the entry mode. Multiple depressions are allowed.

Enter Key, "EN"

Register T is lost, Y and Z are pushed up and X is copied into Y.

THE FOUR FUNCTION KEYS, "+," "–," "x," and "÷"

$$
\begin{array}{lcl}
\text{Add key, "+"} & : & Y + X \rightarrow X \\
\text{Subtract key, "–"} & : & Y - X \rightarrow X \\
\text{Multiply key, "x"} & : & Y \cdot X \rightarrow X \\
\text{Divide key, "÷"} & : & Y \div X \rightarrow X
\end{array}
\left.\vphantom{\begin{array}{l}a\\a\\a\\a\end{array}}\right\}
\begin{array}{l}
Z \rightarrow Y \\
T \rightarrow Z \\
0 \rightarrow T
\end{array}
$$

Pi Key, "π"

Register T is lost; X, Y and Z are pushed up in the stack and the constant 3.1415927 is placed in X.

Exchange Key, "⟷"

Registers X and Y are exchanged; other registers are not affected.

Inverse Trigonometric Key, "ARC"

Preceding one of the three trigonometric keys, "SIN," "COS" or "TAN," it conditions the calculator to determine the angle in degrees of the value in register X. "ARC" followed by any key other than one of the trigonometric keys will be ignored.

Enter Exponent Key, "EEX"

Puts calculator in exponential entry mode. "EEX" must be preceded by a number (mantissa), or it will be ignored. A decimal point is an invalid entry that changes X to zero.

Trigonometric Keys, "SIN," "COS," and "TAN"

Assumes the value of X is an angle in degrees and computes the indicated trigonometric function, replacing X with the result. Register T is replaced by a zero; M, Z and Y are not affected. Following "ARC," the trigonometric keys determine the angle represented by the function in X, and replace X with that value in degrees. T is replaced by a zero; M, Z and Y are unchanged.

Reciprocal Key, "1/X"

A non-zero value of X is replaced by its reciprocal. Registers Y, Z, T and M are unaltered.

Square Root Key, "$\sqrt{X}$"

The absolute value of X is replaced by its square root. Registers Y, Z, T and M are not altered.

Logarithmic Keys, "LN" and "LOG"

These keys replace the value of X by its natural or common logarithm, respectively. Registers Z and T become zero. Registers Y and M are not affected.

Power Key, "Y^X"

Determines the value of Y raised to the power of X and replaces X with that result. Registers Y, Z and T become zero. M is not affected.

Exponential Keys, "e^x" and "10^x"

The constants 2.7182812 or 10.0 are raised to the power of X, respectively, and placed in X. Register T becomes zero; Y, Z and M are not affected.

Memory Keys, "STO" and "RCL"

The memory store key, "STO," copies the value of X (including sign) into storage register M, without altering the stack. The recall key, "RCL," transfers Z to T, Y to Z and X to Y, then copies M into X. Storage register M is not changed and T is lost. Both "STO" and "RCL" terminate an entry mode.

Roll Stack Key, "ROL"

Repositions the data within the operational stack by transferring X to T, Y to X, Z to Y and T to Z. After four successive depressions each of the four data positions has been viewed and returned to its original location.

Range and Accuracy of Functions

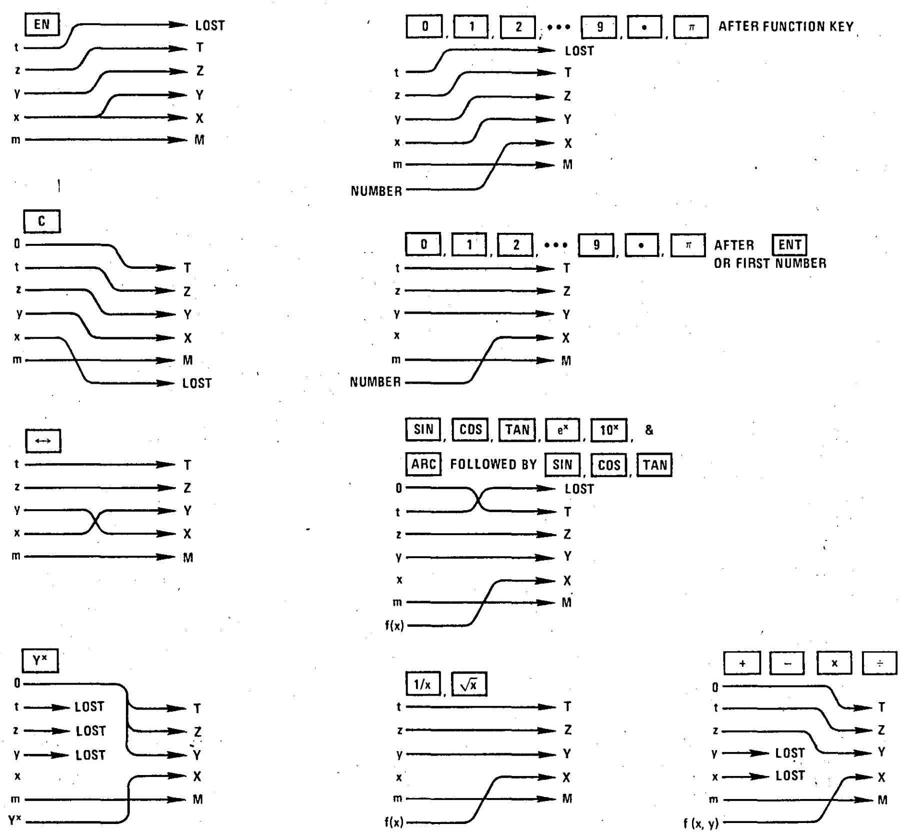
The smallest magnitude that can be displayed is $\pm 10^{-99}$ and the total range is $\pm 9.9999999 \times 10^{99}$. Table IV summarizes range and accuracy of the MM5758 functions.

TABLE IV.

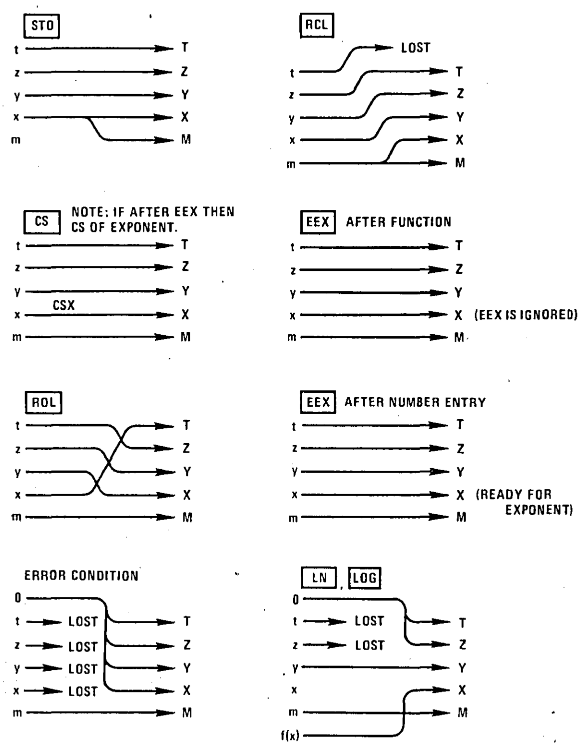
FUNCTION	RANGE	ACCURACY
+, −, x, ÷, 1/X	$\pm 1 \times 10^{-99} \leq X \leq \pm 9.9999999 \times 10^{99}$	±1 in first non-zero digit from LSD
$\sqrt{X}$	$\lvert \pm 1 \times 10^{-99} \rvert \leq X \leq \lvert \pm 9.9999999 \times 10^{99} \rvert$	±2 in first non-zero digit from LSD
LOG X	$0 < X \leq +9.9999999 \times 10^{99}$	7 digits
LN X	$0 < X \leq +9.9999999 \times 10^{99}$	7 digits
10^x	$\pm 1 \times 10^{-99} \leq X \leq +99$	5 digits
e^x	$\pm 1 \times 10^{-99} \leq X \leq +230$	5 digits
Y^x	Y > 0, with X and Y values such that the results will be $+1 \times 10^{-99} \leq X \leq +9.9999999 \times 10^{99}$	5 digits
SIN, COS, TAN	$0 \leq X \leq +90$	7 digits
ARC SIN, ARC COS	$0 \leq X \leq +1$	5 digits
ARC TAN	$0 \leq X \leq 9.9999999 \times 10^{99}$	5 digits

*Error in last useable digit is less than 5

Summary of Stack Operations



Summary of Stack Operations (con't)



SAMPLE PROBLEMS

Problem No. 1 1.345 + 7120 − 14251 = ?

STACK REGISTERS

KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
POWER ON	0.	0	0	0	0	Power on clears all registers and memory
1	1					
.	1.					
3	1.3					
4	1.34					
5	1.345					
ENTER	1.345	1.345				Copy X in Y
7	7					
1	71					
2	712					
0	7120					
+	7121.345	0				Add X and Y
1	1	7121.345				
7	17					
CLR	7121.345	0				Clear entry, pushes down stack
1	1	7121.345				
4	14					
2	142					
5	1425					
1	14251	7121.345	0	0	0	
−	−7129.655	0	0	0	0	Subtract X from Y Note: It is not necessary to clear calculator for the next problem.

Problem No. 2 $(3.73 \times 10^{-7}) \times (-15 \times 10^{24}) \div 27357.3 = ?$

STACK REGISTERS

KEY ENTRY	DISPLAY X		Y		Z	T	MEMORY M	COMMENTS
3	3		−7129.655		0	0	0	The new number entry pushes the answer of the last problem up in the stack
.	3.							
7	3.7							
3	3.73							
EEX	3.73							Prepare for exponent entry
7	3.73	07						
CHS	3.73	−07						Change sign of exponent
ENTER	3.73	−07	3.73	−07	−7129.655			
1	1							
5	15							
CHS	−15							Change sign of mantissa
EEX	−15							
2	−15	02						
4	−15	24						
x	−5.595	18	−7129.655		0	0	0	Multiply X and Y
2	2		−5.595	18	−7129.655	0	0	
7	27							
3	273							
5	2735							
7	27357							
.	27357.							
3	27357.3							
÷	−2.0451579	14	−7129.655		0			Divide Y by X
CLR	−7129.655		0					Clear Answer
CLR	0.		0		0	0	0	Clear answer from problem 1 Note: This is not necessary. It is done here to avoid confusion of stack operation in the next problem.

Problem No. 3 $\sqrt{10.3\ (3^2+4^2)\ (5^2+6^2)}$

STACK REGISTERS

KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
10.3	10.3	0	0	0	0	
ENTER	10.3	10.3				The "Roll" key can be used to examine the stack. It is not necessary for the solution.
3	3	10.3				
ENTER	3.	3	10.3			Register contents displayed:
ROLL	3.	10.3	0	3		Y
ROLL	10.3	0	3	3		Z
ROLL	0.	3	3	10.3		T
ROLL	3.	3	10.3	0		X
x	9.	10.3	0	0		3^2
4	4	9	10.3	0		
ENTER	4.	4	9	10.3		
x	16.	9	10.3	0		4^2
+	25.	10.3	0	0		(3^2+4^2)
x	257.5	0	0	0	0	$10.3\ (3^2+4^2)$
5	5	257.5	0	0	0	
ENTER	5.	5	257.5			
x	25.	257.5	0			5^2
6	6	25.	257.5			
ENTER	6.	6	25	257.5		
x	36.	25	257.5	0		6^2
+	61.	257.5	0			(5^2+6^2)
x	15707.5	0				$10.3\ (3^2+4^2)\ .5^2+6^2)$
$\sqrt{X}$	125.32956	0	0	0	0	$\sqrt{10.3\ (3^2+4^2)\ (5^2+6^2)}$

Problem No. 4 $1 + \frac{1}{2!} X + \frac{1}{3!} X^2 = ?, \quad X = -0.15$

		STACK REGISTERS				
KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
1	1	125.32956	0	0	0	
ENTER	1.	1	125.32956			
2	2					2!
$\frac{1}{X}$	0.5					$\frac{1}{2!}$
0.15 CHS	−0.15	0.5	1	125.32956		X
STO	−0.15				−0.15	Store X for use later in the problem
X	−7.5 −02	1	125.32956	0		$\frac{1}{2!}$ X
+	0.925	125.32956	0			$1 + \frac{1}{2!}X$
3	3	0.925	125.32956			
ENTER	3.	3	0.925	125.32956		
2	2					
X	6.	0.925	125.32956	0		3!
$\frac{1}{X}$	0.1666666	0.925	125.32956	0	−0.15	$\frac{1}{3!}$
RCL	−0.15	0.1666666	0.925	125.32956	−0.15	X
ENTER	−0.15	−0.15	0.1666666	0.925		Answer to last problem is lost here
X	2.25 −02	0.1666666	0.925	0		X^2
X	3.7499985 −03	0.925	0			$\frac{1}{3!}X^2$
+	0.9287499	0				$1 + \frac{1}{2!}X + \frac{1}{3!}X^2$
CLR	0					
RCL	−0.15	0	0	0	−0.15	Notice that the clear does not affect the memory register. Memory is changed only by storing another value or by power off.

Problem No. 5 $\pi(21) = ? \quad 21^2 (\pi) = ?$

		STACK REGISTERS				
KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
π	3.1415927	−0.15	0	0	−0.15	
21	21	3.1415927	−0.15			
X	65.973446	−0.15	0			$\pi(21)$
21	21	65.973446	−0.15			
ENTER	21.	21	65.973446	−0.15		
X	441.	65.973446	−0.15	0		21^2
π	3.1415927	441	65.973446	−0.15		
X	1385.4423	65.973446	−0.15	0	−0.15	$21^2(\pi)$

Problem No. 6 Example using Exchange and Reciprocal keys.

		STACK REGISTERS				
KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
5	5	1385.4423	65.973446	−0.15	−0.15	
ENTER	5.	5	1385.4423	65.973446		
1	1					
EXCH	5.	1				
÷	0.2	1385.4423	65.973446	0		
5	5	0.2	1385.4423	65.973446		
$\frac{1}{X}$	0.2	0.2	1385.4423	65.973446		Compare the answers obtained by exchanging X and Y. In this case, they are identical.
EXCH	0.2	0.2	1385.4423	65.973446		
EXCH	0.2	0.2	1385.4423	65.973446		
−	0.	1385.4423	65.973446	0		Compare by subtracting zero error
$\frac{1}{X}$	0.0.0.0.0.0.0.0.	0	0	0		Divide by zero. Error clears all registers.
CLR	0.	0	0	0	−0.15	After clearing an error, all registers are zero. Memory is not disturbed.

Problem No. 7 Example using "10^x" and "LOG" keys

KEY ENTRY	DISPLAY X	STACK REGISTERS Y	Z	T	MEMORY M	COMMENTS
1.2345678	1.2345678	0	0	0	−0.15	
STO	1.2345678				1.2345678	Store original value
10^x	17.161995					
LOG	1.2345678					
RCL	1.2345678	1.2345678				
EXCH	1.2345678					Compare answer to original value
EXCH	1.2345678					
4	4		1.2345678			Fill the stack
ENTER	4.	4		1.2345678		
3	3					
ENTER	3.	3	4			
2	2					
ENTER	2.	2	3	4		
1	1	2	3	4	1.2345678	
10^x	10.	2	3	0	1.2345678	Notice that "T" is lost (same for 10^x, e^x)
4	4	10.	2	3		
ENTER	4.	4	10.	2		
3	3					
ENTER	3.	3	4	10		
2	2					
ENTER	2.	2	3	4		
1	1					
LOG	2.2 −07	2	0	0	1.2345678	Notice that "Z" and "T" are lost (same for LOG, LN)

Problem No. 8 Example using "e^x" and "LN" keys

KEY ENTRY	DISPLAY X	STACK REGISTERS Y	Z	T	MEMORY M	COMMENTS
8.7654321	8.7654321	2.2 −07	2	0	1.2345678	
STO	8.7654321				8.7654321	Store original value
e^x	6408.8309					
LN	8.7654321		0			
RCL	8.7654321	8.7654321	2.2 −07			
−	0.0	2.2 −07	0	0	8.7654321	Compare answer to original. Error is 0.0

Problem No. 9 2^{10}

KEY ENTRY	DISPLAY X	STACK REGISTERS Y	Z	T	MEMORY M	COMMENTS
2	2	8.7654321	8.7654321	2.2 −07	8.7654321	
ENTER	2.	2		8.7654321		
10	10					
Y^x	1024.0037	0	0	0	8.7654321	Notice that "Y," "Z" and "T" are lost

Problem No. 10 Trigonometric computations

KEY ENTRY	DISPLAY X	STACK REGISTERS Y	Z	T	MEMORY M	COMMENTS
30	30	1024.0037	0	0	8.7654321	Enter X in degrees
SIN	0.5000002					Sine of 30° is computed
ARC	0.5000002					ARC sine is computed
SIN	29.999556					
4	4	29.999556	1024.0037			
ENTER	4.	4	29.999556	1024.0037		
3	3					
ENTER	3.	3	4	29.999556		
2	2					
ENTER	2.	2	3	4		
1	1					
SIN	1.7452415 −02	2	3	0	8.7654321	Notice that "T" is lost (same for SIN, COS, TAN)
4	4	1.7452415 −02	2	3	8.7654321	
ENTER	4.	4	1.7452415 −02	2		

Problem No. 10 (con't)

KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
			STACK REGISTERS			
3	3					
ENTER	3.	3	4	1.7452415 −02		
2	2					
ENTER	2.	2	3	4		
1	1					
ARC	1.					
SIN	89.999997	2	3	0	8.7654321	Notice that "T" is lost (same for ASIN, ACOS, ATAN)

Problem No. 11

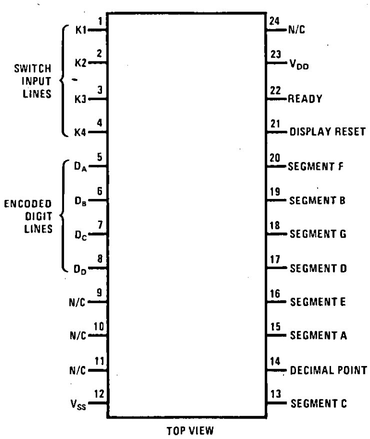
KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
			STACK REGISTERS			
30	30	89.999997	2	3	8.7654321	
COS	0.8660252			0		
ARC	0.8660252					
COS	29.999569	89.999997	2	0	8.7654321	

Problem No. 12

KEY ENTRY	DISPLAY X	Y	Z	T	MEMORY M	COMMENTS
			STACK REGISTERS			
45	45	29.999569	89.999997	2	8.7654321	
TAN	0.9999991			0		
ARC						
TAN	45.000629	29.999569	89.999997	0	8.7654321	

connection diagram

Dual-In-Line Package



Order Number MM5758N
See Package 22

Calculators

MM5760 slide rule calculator general description

The single-chip MM5760 Slide Rule Calculator was developed using a metal-gate, P-channel enhancement and depletion mode MOS/LSI technology with the primary objective of low end-product cost. A complete calculator as shown in *Figure 1* requires only the MM5760, a keyboard, DM8864 digit driver, NSA298 LED display and a 9V battery with appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and 7-segment output display encoding are included on-chip and require no external components. Segments can usually be driven directly from the MM5760, as it typically sources about 8.5 mA of peak current. (Note: the typical duty cycle of each digit is 0.104; average LED segment current is therefore approximately 0.89 mA.) The left-most digit is used for the negative sign or the decimal point of a number less than unity.

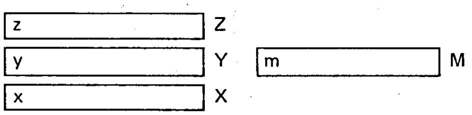
An internal power-on clear circuit clears all registers, including the memory, when V_{DD} and V_{SS} are initially applied to the chip.

Trailing zero suppression allows convenient reading of the left justified display, and conserves power. The DM8864 digit driver is capable of sensing a low battery voltage and providing a signal during Digit 9 time that can be used to turn on one of the segments as an indicator. Typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff is included. If no key closure occurs for approximately 35 seconds, all numbers are blanked and all decimal points displayed.

The Ready output signal is used to indicate calculator status. It is useful in providing synchronization information during testing and when the MM5760 is used with other logic or integrated circuits; e.g., with the MM5765 Programmer (*Figure 3*).

Thirty-two keys are arranged in a four-by-nine matrix (*Figure 1*). In addition to seven arithmetic functions plus logarithmic, trigonometric and accumulating memory functions, the calculator is capable of calculating Y^x, adding the square of X to memory, automatically entering π and providing degrees/radian conversions.

The user has access to four registers designated X, Y, Z and M. X is the display and entry register, and is the bottom of a "push-up" stack that also includes registers Y and Z:



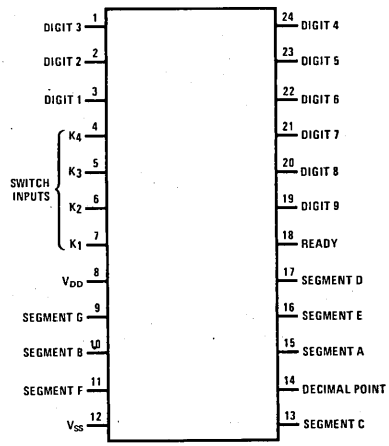
Note: Lower case letters designate the data in the register identified by a capital letter.

features

- Full 8-digit entry and display capacity
- Complete electronic slide rule capability
  - Arithmetic functions: +, −, x, ÷, $\sqrt{x}$, 1/x, x^2
  - Logarithmic functions: ln x, log x, e^x
  - Trigonometric functions: sin x, cos x, tan x, arc sin x, arc cos x, arc tan x
  - Other functions: Y^x, π, change sign, exchange, x^2 + memory → memory, radians to degrees, degrees to radians
- Three-register operational stack
- Independent accumulating storage register with store, recall, memory plus and memory minus functions
- Floating point input and output
- Direct 9V battery compatibility; low power
- Power-on clear
- No external components required other than display digit driver, keyboard and LED display for complete calculator
- Error indication for over range, overflow and invalid operations
- Left justified entry and results with trailing zero suppression
- Automatic display cutoff
- Reverse polish notation

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5760N
See Package 22

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All other pins connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

V_{SS} is always defined as the most positive supply voltage.

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}$−9.5V, T_A = 25°C			16.0	mA
Keyboard Scan Input Levels (K1, K2, K3 and K4)					
Logical High Level	V_{SS}−6.5V ≤ V_{DD} ≤ V_{SS}−9.5V	V_{SS}−2.5			V
Logical Low Level	$V_{DD} = V_{SS}$−6.5V			V_{SS}−5.0	V
	$V_{DD} = V_{SS}$−9.5V			V_{SS}−6.0	V
Digit Output Levels					
Logical High Level (V_{OH})	R_{LOAD} = 3.2 kΩ to V_{DD}				
	V_{SS}−6.5V ≤ V_{DD} ≤ V_{SS}−9.5V	V_{SS}−1.5			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS}$−6.5V			V_{SS}−6.0	V
	$V_{DD} = V_{SS}$−9.5V			V_{SS}−7.0	V
Segment Output Current	T_A = 25°C				
(Sa through Sg and Decimal Point)	$V_{OUT} = V_{SS}$−3.6V, $V_{DD} = V_{SS}$−6.5V	−5.0	−8.5		mA
	$V_{OUT} = V_{SS}$−5V, $V_{DD} = V_{SS}$−8V		−10.0		mA
	$V_{OUT} = V_{SS}$−6.5V, $V_{DD} = V_{SS}$−9.5V			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	I_{OUT} = −0.4 mA	V_{SS}−1.0			V
Logical Low Level (V_{OL})	I_{OUT} = 10µA			V_{DD}+1.0	V

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (*Figure 2*)		0.32	0.65	1.3	ms
Digit Time (*Figure 2*)		36	70	145	µs
Segment Blanking Time (*Figure 2*)		2	4.5	9	µs
Digit Output Transition Times (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF, R_{LOAD} = 9.6 kΩ		2		µs
Keyboard Inputs High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		µs
Ready Output Propagation Time (*Figure 3*)					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	10		50	µs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF			1	ms
Key Input Time-out					
Key Entry		2.8	6.0	11.7	ms
Key Release		5.1	10.4	20.5	ms
Display Cutoff Time (The time after the last valid key closure that all numbers will be blanked and all decimal points displayed.)		10	22	44	second

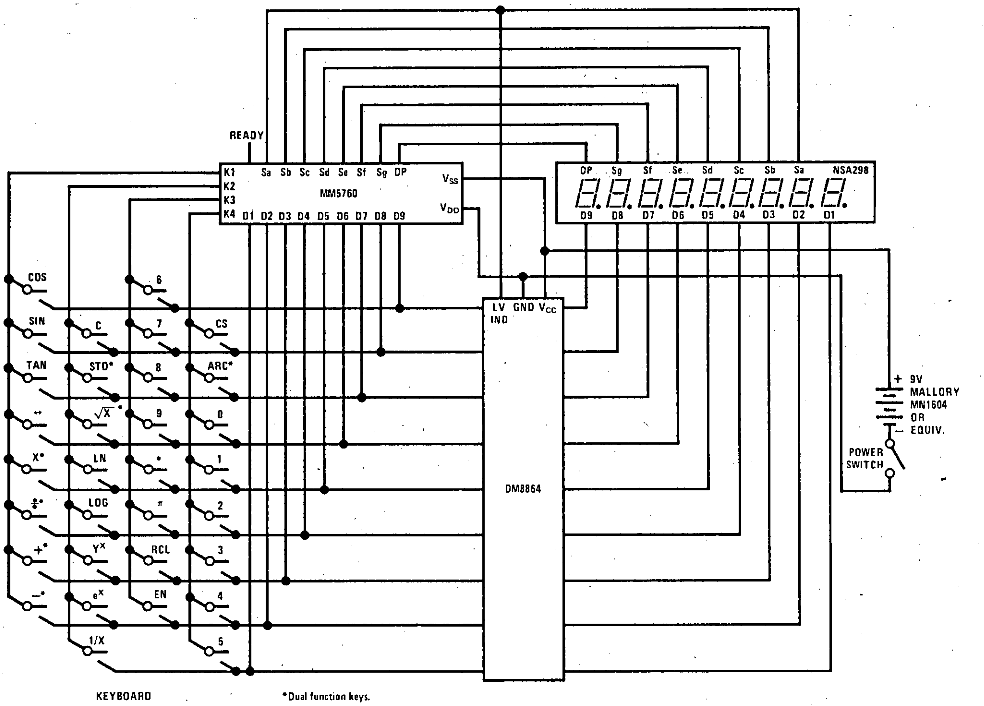


FIGURE 1. Complete Calculator Schematic

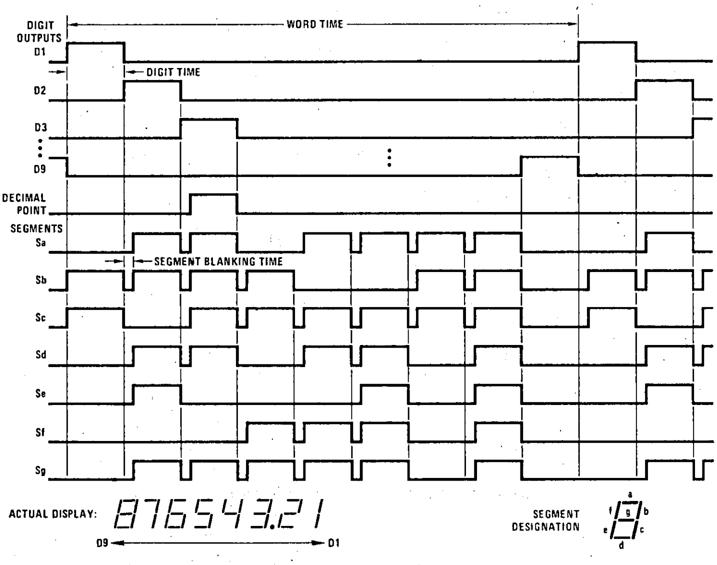


FIGURE 2. Display Timing Diagram

The contents of the accumulating storage register M are replaced with the contents of the X register by using the "STO" key. Preceding "+" or "–" with the "ARC" key sums X into M, or subtracts X from M. "ARC" followed by "STO" squares X and sums it into the memory without changing the value of X. The memory recall key, "RCL," copies M into X without disturbing the value of M. Storage register M is cleared automatically at power-on or by storing a zero. All registers contain eight digits and sign information.

Inputs are entered and outputs displayed in floating point. The output results are truncated. Data entry always precedes the operation keys that operate on them; this is referred to as Reverse Polish notation. (See examples.)

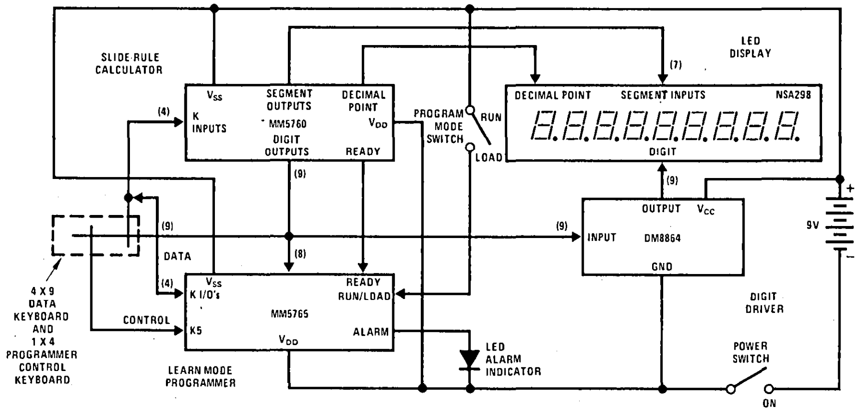


FIGURE 3. Low Cost Hand Held Programmable Electronic Slide Rule Using the MM5760 Calculator and MM5765 Programmer

KEY SEQUENCE EXAMPLES

KEY	DISPLAY	COMMENTS
	0.	Power-On Clear
1	1	
0	1 0	
0	1 0 0	
LOG	2.	
EN	2.	Copy X into Y
10	1 0	
C	2.	Clear X, stack pushes down
C	0.	Stack cleared
10	1 0	
EN	1 0.	
2	2	
Y^x	9 9.9 9 9 9 3	6 digit accuracy. Typical calculation time = 1.7 seconds
50	5 0	
+	1 4 9.9 9 9 9 3	
4	4	
$\sqrt{X}$	2.	Typical calculation time = 90 ms
EN	2.	
7	7	
−	−5.	
2	2	
X	−1 0.	
÷	−1 4.9 9 9 9 9 3	
9	9	
STO	9.	"STO" terminates data entry
3	3	
ARC	3	
SIN	.0.0.0.0.0.0.0.0	Error indication ($X > 1$)
.	.	No clear needed
1	.1	
LN	−2.3 0 2 5 8 5	Typical calculation time = 260 ms
RCL	9.	
1/X	.1 1 1 1 1 1 1 1	
9	9	Exchange X and Y
↔	.1 1 1 1 1 1 1 1	
Y^x	1.2 7 6 5 1 7	$1^9\sqrt{9} = 9^{1/9}$
.8	.8	
ARC	.8	
ARC	.8	Second "ARC" ignored
SIN	5 3.1 3 0 1	SIN^{-1} in degrees
SIN	.8	SIN of 53.1301°

KEY SEQUENCE EXAMPLES (Con't)

KEY	DISPLAY	COMMENTS
ARC	.8	
COS	3 6.8 6 9 9	COS^{-1} in degrees
COS	.8	COS of 36.8699
ARC	.8	
TAN	3 8.6 5 9 8 1	TAN^{-1} in degrees
TAN	.8	TAN of 38.65981
LOG	−.0 9 6 9 1	
LN	.0.0.0.0.0.0.0.0	
e^x	1.	e^x for X = 0
π	3.1 4 1 5 9 2 6	
C	1.	
C	1.2 7 6 5 1 7	
C	0.	
LN	.0.0.0.0.0.0.0.0	
1	1	
CS	−1	
STO	−1.	
ARC	−1.	
COS	1 8 0	
ARC	1 8 0	
TAN	8 9.6 8 1 6 9	
RCL	−1.	
e^x	.3 6 7 8 7 9 6	
RCL	−1.	
ARC	−1.	
SIN	−9 0.	
ARC	−9 0.	
÷	−1.5 7 0 7 9 6 3	90° in radians
ARC	−1.5 7 0 7 9 6 3	
+	−1.5 7 0 7 9 6 3	Accumulate X· in M
RCL	−2.5 7 0 7 9 6 3	Recall M

EXAMPLE DEMONSTRATING STACK OPERATIONS

$$\text{Evaluate: } \frac{\text{LOG}\left(\frac{14+26}{6-\sqrt{4}}\right)}{\text{SIN }(25+5)}$$

STACK REGISTERS

KEY	X	Y	Z	COMMENTS
14	14	?	?	Y and Z are unknown
EN	14.	14	?	
26	26	14	?	
+	40.	?	0	14 + 26 = 40
6	6	40	?	
EN	6.	6	40	
4	4	6	40	
$\sqrt{X}$	2.	6	40	$\sqrt{4} = 2$
−	4.	40	0	$6 - \sqrt{4} = 4$
÷	10.	0	0	$(14 + 26)/6 - \sqrt{4} = 10$
LOG	1.	0	0	$\text{LOG}[(14 + 26)/(6 - \sqrt{4})] = 1$
25	25	1	0	
EN	25.	25	1	
5	5	25	1	
+	30.	1	0	
SIN	.5	1	0	SIN (25 + 5) = 0.5
÷	2.	0	0	$\frac{\text{LOG }[(14 - 26)/(6 - \sqrt{4})]}{\text{SIN}(25 + 5)} = 2$
C	0.	0	0	

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5760 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip.when one of the key inputs, K1, K2, K3 or K4 is forced more positive than the Logical High Level specified in the Electrical Specifications. An internal counter is started as a result of the closure. The key operation begins after nine word times if the key input is still at a Logical High Level. As long as the key is held down (and the key input remains high) no further entry is allowed. When the key input changes to a Logical Low Level, the internal counter starts a sixteen word time-out for key release. During both entry and release time-outs the key inputs are sampled approximately every other word time for valid levels. If they are found invalid, the counter is reset and the calculator assumes the last valid key input state.

One of the popular types of low-cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5760 recognizes a series contact resistance up to 50 kΩ as a valid key closure, assuring a reliable interface for that type of keyboard.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately 35 seconds, an internal automatic display cutoff circuit will blank all segments and display nine decimal points. Any key depression will restore the display; to restore the display without modifying the status of the calculator, use two change sign, "CS," depressions.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 4* and *5.* It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

ERROR INDICATION

In the event of an operating error, the MM5760 will display all zeros and all decimal points. In addition to normal calculator overflow situations which occur as a result of adding, subtracting, multiplying or dividing and including division by zero, the error indication is displayed for the conditions of Table I.

The Z-register is automatically cleared and the Y- and M-registers are saved. An error condition is cleared by depressing any key except "1/X," "÷," "LOG X" or "LN X." Operation on the X register with an error displayed will be performed as if X contained a zero.

KEY OPERATIONS

(Note: Register X is always displayed.)

Clear Key, "C"

After any key except "ARC," it clears X, pushes Y down to X, Z to Y and places a zero in Z. Subsequent depressions perform the same function; thus, three "C" depressions after a number entry will clear a completely

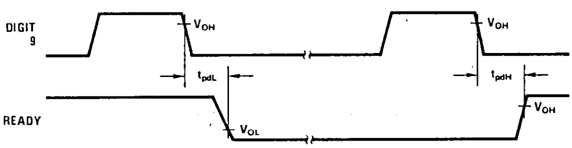


FIGURE 4. Ready Timing

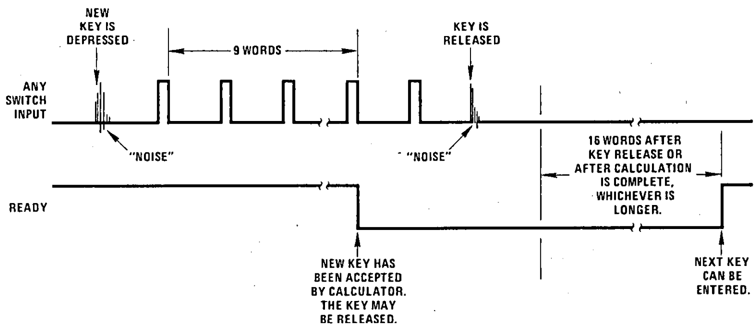


FIGURE 5. Functional Description of Ready Signal and Key Entry

TABLE I. Conditions for Error Indication

FUNCTION	CONDITIONS (REGISTER $X \equiv X$)
$+, -, x, \div$	Result $> 99999999.$
$\div$ or $1/X$	$\lvert X \rvert \leq 0.00000001$
$\sqrt{X}$	$X < 0$
Y^X	$Y \leq 0$ $\ell n\ 99999999 < X\ \ell n\ Y < -28$
log X or ln X	$X \leq 0.00000001$
e^X	$\ell n\ 99999999 < X < -28$
Sin X or Cos X	$X \geq 7$ radians or $\sim 401°$
ARC Sin X or ARC Cos X	$X > 1$
Tan X	$X = \pm 90°$, or $X \geq 7$ radians

Note: $\ell n\ 99999999 = 18.420680$

full stack. This is also the method used to gain access to the Z register. Memory register M is not affected by "C." Pressing "C" after "ARC" resets the ARC function without affecting any of the data registers.

Number Entries

First entry after "EN" clears X and enters the number into Digit 8 (the second digit from the left of the display) of X. Second through eighth entry (excluding a decimal point) enters the number one digit to the right of the last number entered. The ninth, and subsequent entries, are ignored. The first number key after any key other than "EN" loses Z, pushes Y up to Z, X to Y, clears X and enters the number in Digit 8 of X.

Decimal Point, "."

After an ENTER key, it clears X and displays a decimal point in the left-most digit position. Following a number entry, it places a decimal point to the right of the last number entered. Subsequent depressions without an interceding number entry are ignored; subsequent depressions after interceding number entries will replace the previous point with one to the right of the last entered number.

Change Sign Key, "CS"

Changes the sign of X.

Enter Key, "EN"

Register Z is lost; Y is pushed up to Z and X is copied into Y.

Addition Key, "+"

X is added to Y and the result is placed in X. Z is transferred to Y and cleared. Following an "ARC" key, "+" adds the contents of X to M without changing X, Y or Z.

Subtraction Key, "–"

X is subtracted from Y and the result is placed in X. Z is copied into Y, then cleared. Following an "ARC" key, "–" subtracts the contents of X from M without changing X, Y or Z.

Multiplication Key, "X"

X is multiplied by Y and the result is placed in X. Z is transferred to Y and cleared. Following an "ARC" key, "X" converts the value of X from radians to degrees without changing M, Y or Z.

Division Key, "÷"

X is divided into Y and the result is placed in X. Z is transferred to Y and cleared. Following an "ARC" key, "÷" converts the value of X from degrees to radians without changing M, Y or Z.

Pi Key, "π"

Register Z is lost; Y is pushed up to Z and X to Y. The constant 3.1415926 is placed in X.

Exchange Key, "←→"

Registers X and Y are exchanged. Z and M are not affected.

Inverse Trigonometric and Multifunction Key, "ARC"

When used as a prefix to one of the trigonometric keys it conditions the calculator to determine the inverse function of the value in X. For example "ARC" followed by "SIN" computes the angle that has a sine equal to the value of X, replacing X with that angle in degrees. See key descriptions of "+," "–," "X," "÷," "$\sqrt{X}$," "STO" and "C" for secondary functions assigned to those keys by preceding them with "ARC." "ARC" followed by any key other than one of the above or one of the trig functions will be ignored.

Reciprocal Key, "1/X"

A non-zero value of X is replaced by its reciprocal. Registers M, Y and Z are not altered.

Square Root Key, "$\sqrt{X}$"

A positive value of X is replaced by its square root. Registers Y and Z are not altered. Following an "ARC" key, "$\sqrt{X}$" replaces the value of X with its square. Registers M, Y and Z are not affected.

Logarithmic Keys, "LN" and "LOG"

These keys replace the value of X by its natural or common logarithm, respectively; register Z is lost. M is not altered.

Exponential Key, "e^X"

Determines the value of 2.7182818 raised to the power contained in register X, and places that value in X. The contents of Z are lost and Z is cleared. M is not altered.

Power Key, "Y^X"

Determines the value of Y raised to the power of X and replaces X with the result. The contents of Z are lost, Y retains the exponent and Z is cleared. M is not affected.

Memory Keys, "STO" and "RCL"

The memory store key, "STO" copies the value of X (including sign) into storage register M without altering the stack. "STO" following "ARC" squares the value of X and accumulates the result into M. Registers X, Y and Z are not affected. The recall key, "RCL," transfers Y to Z and X to Y, then copies M into X. Storage register M is not changed and Z is lost. Both "STO" and "RCL" terminate the entry mode.

MEMORY OPERATIONS RESULTING IN ERROR CONDITIONS

Any operation in which the storage register M is involved that results in an error condition, will not affect the previous contents of M. For example, if by accumulating X into M("ARC," "+") the contents of M will become greater than 99999999., an error indication will occur and the original contents of M are protected. As a result of the overflow, registers X and Z will be lost an shown in Table II.

TABLE II. Summary of Stack Operations

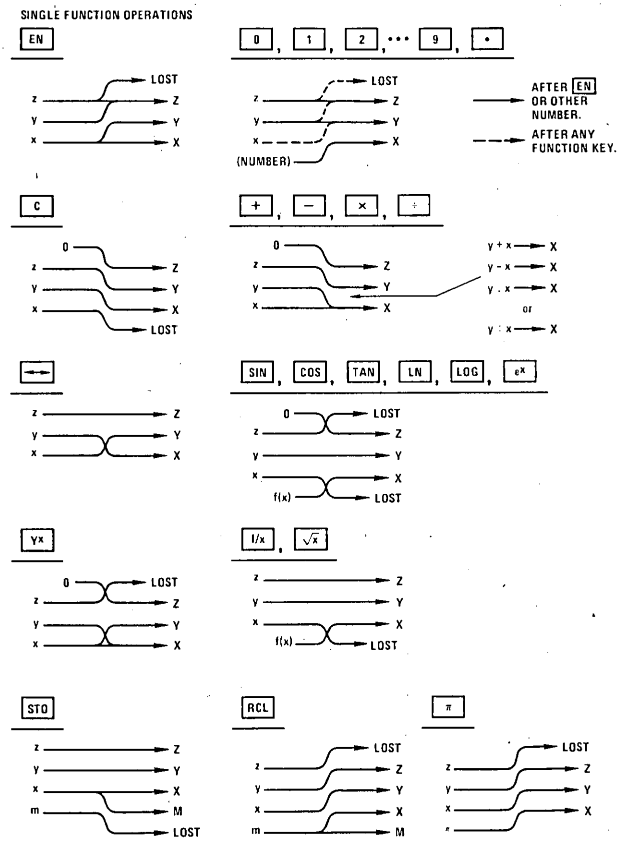
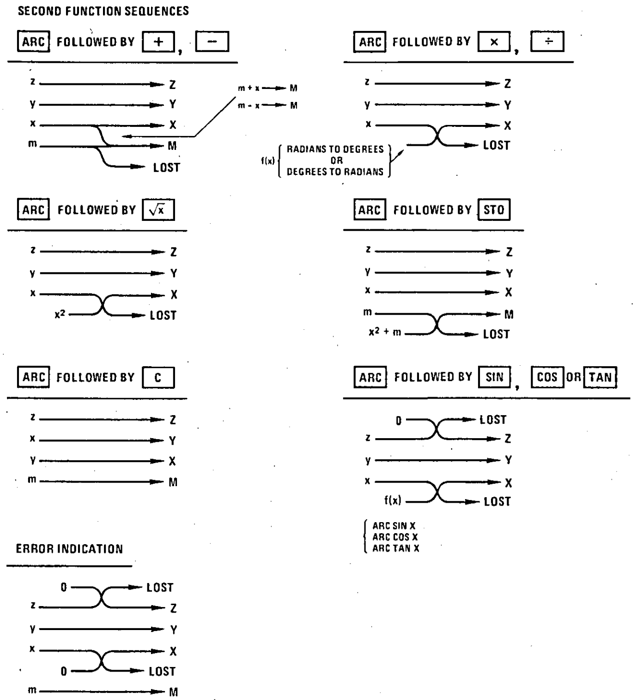


TABLE II. Summary of Stack Operations (Cont'd)



RANGE AND ACCURACY OF FUNCTIONS

The smallest magnitude that can be displayed is ±0.00000001 and the total range is from −99999999 to +99999999. The arithmetic functions (+, −, x, ÷, 1/X, $\sqrt{X}$, X^2) have eight digit accuracy. All results are truncated. Table III summarizes range and accuracy of the other functions. Arithmetic calculations will be completed in less than 0.5 second; all others except Y^x in less than 2.5 seconds and Y^x in less than 5 seconds.

TABLE III. Digit Accuracy for Various Functions

FUNCTION	RANGE	APPROXIMATE ACCURACY (Note 1)
SIN, COS, TAN	∿ −90° to ∿ 90° ∿ −360° to ∿ 360°	7 Digits 6 Digits
ARC SIN and ARC COS	∿ −1 to ∿ +1	6 Digits
ARC TAN	−99999999 to 99999999	6 Digits
LOG	$X \geq 0$	6 Digits
e^X	$-28 \leq X \leq \ell n\ 99999999$	6 Digits
LN	$X \geq 0$	6 Digits
$\sqrt{X}$	$X \geq 0$	8 Digits
Y^X	$Y > 0$ $X\ \ell n\ Y \leq \ell n\ 99999999$	5 Digits

Note 1: Six digit accuracy, as an example, would be:

1 2 3 4 5 6 X X

±1

n digit accuracy has the n^{th} digit from the MSD being displayed accurate within ±1.

MM5762 financial calculator

general description

The single-chip MM5762 Business and Financial Calculator was developed using a metal-gate, P-channel enhancement and depletion mode MOS/LSI technology with low end-product cost as a primary objective. A complete calculator as shown in *Figure 1* requires only the MM5762, a keyboard, DS8864 digit driver, NSA1298 LED display, 9V battery and appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and 7-segment output display encoding are included on-chip and require no external components. Segments can usually be driven directly from the MM5762, as it typically sources about 8.5 mA of peak current. [Note: The typical duty cycle of each digit is 0.104; average LED segment current is therefore approximately 0.104 (8.5 mA), or 0.9 mA average. Correspondingly, the worse-case average segment current is 0.104 (5.0 mA), or 0.52 mA.] The ninth digit (left-most) is used for the negative sign, or the decimal point of a number less than unity.

An internal power-on clear circuit is included that clears all registers, including the memory, when V_{DD} and V_{SS} are initially applied to the chip.

Trailing zero suppression allows convenient reading of the left justified display, and conserves power. The DS8864 digit driver is capable of sensing a low battery voltage and providing a signal during Digit 9 time that can be used to turn on one of the segments as an indicator. Typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff is included. If no key closure occurs for approximately 35 seconds, all numbers are blanked and all decimal points are displayed.

The Ready output signal is used to indicate calculator status. It is useful in providing synchronization information for testing or applications where the MM5762 is used with other logic or integrated circuits; e.g., with the MM5765 Programmer *(Figure 3)*.

Thirty-two keys are arranged in a four-by-nine matrix as shown in *Figure 1*. There are the standard four function keys (+, −, ÷, x), Change Sign, Exchange, three accumulating memory control keys plus ten unique business or financially oriented computation keys: three keys for entering interest rate per period, number of periods and amount, three keys for computing present and future values, sinking funds, saving and loan payments and other time/money factors, two keys for computing per cent and delta per cent, a sum-of-digits key and a power key. There is an automatic constant feature.

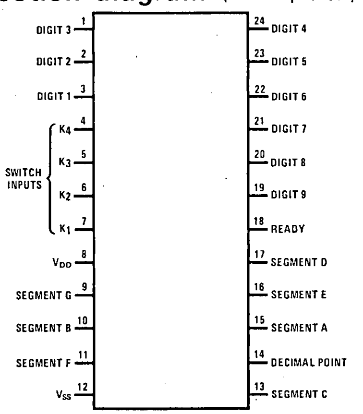
The user has access to six registers designated X, Y, A, I, N and M. The X-register is used for keyboard entry and display. The Y and A-registers are used in multiply/divide and add/subtract calculations, respectively. Interest values are held in the I-register and the N-register stores the number of time periods in financial calculations. M is an accumulating storage memory and is completely independent of the others.

Data is entered into the calculator in floating point business notation. All entries and results are displayed left justified with insignificant zeros to the right of the decimal point suppressed. All intermediate results of a chain calculation are floating point. Terminating keys (such as equal, per cent, etc.) round the displayed result to two decimal positions.

features

- Complete business and financial capability
  - Arithmetic functions: +, −, x, ÷
  - Power function: Y^X
  - Percent: both live percent *and* delta percent keys
  - Sum-of-digits capability for computing depreciation or "Rule of 78's" loan costs
  - Financial functions:
    - ▲ "n" key, enters number of periods
    - ▲ "i" key, enters interest rate per period
    - ▲ "AMT" key, enters given amount
    - ▲ "VAL" key, computes PV or FV
    - ▲ "SAV" key, computes deposit or sinking fund amounts
    - ▲ "LOAN" key, computes payment or loan amounts
- Accumulating memory
- Automatic constant
- Convenient business (adding machine) entry notation
- Eight full digits
- Power-on clear
- Automatic display cutoff
- Low system cost

connection diagram (DIP Top View)



Order Number MM5762N
See Package 22

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}. (All other pins connected to V_{SS}.)	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

V_{SS} is always defined as the most positive supply voltage.

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}$–9.5V, T_A = 25°C		8.0	16.0	mA
Keyboard Scan Input Levels (K1, K2, K3 and K4)					
Logical High Level	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	V_{SS}–2.5			V
Logical Low Level	$V_{DD} = V_{SS}$–6.5V			V_{SS}–5.0	V
	$V_{DD} = V_{SS}$–9.5V			V_{SS}–6.0	V
Digit Output Levels					
Logical High Level (V_{OH})	R_{LOAD} = 3.2 kΩ to V_{DD}				
	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	V_{SS}–1.5			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS}$–6.5V			V_{SS}–6.0	V
	$V_{DD} = V_{SS}$–9.5V			V_{SS}–7.0	V
Segment Output Current (Sa through Sg and Decimal Point)	T_A = 25°C				
	$V_{OUT} = V_{SS}$–3.6V, $V_{DD} = V_{SS}$–6.5V	−5.0	−8.5		mA
	$V_{OUT} = V_{SS}$–5V, $V_{DD} = V_{SS}$–8V		−10.0		mA
	$V_{OUT} = V_{SS}$–6.5V, $V_{DD} = V_{SS}$–9.5V			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	I_{OUT} = −0.4 mA	V_{SS}–1.0			V
Logical Low Level (V_{OL})	I_{OUT} = 10μA			V_{DD}+1.0	V

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (*Figure 2*)		0.32	0.75	2.0	ms
Digit Time (*Figure 2*)		36	83	220	μs
Segment Blanking Time (*Figure 2*)		2	4.5	14	μs
Digit Output Transition Times (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF, R_{LOAD} = 9.6 kΩ		2		μs
Keyboard Inputs High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		μs
Ready Output Propagation Time (*Figure 4)*					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	10		50	μs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF			1	ms
Key Input Time-out *(Figure 5)*					
Key Entry		2.8	7.0	18	ms
Key Release		5.1	12	32	ms
Display Cutoff Time (The time after the last valid key closure that all numbers will be blanked and all decimal points displayed.)		15	35	92	sec

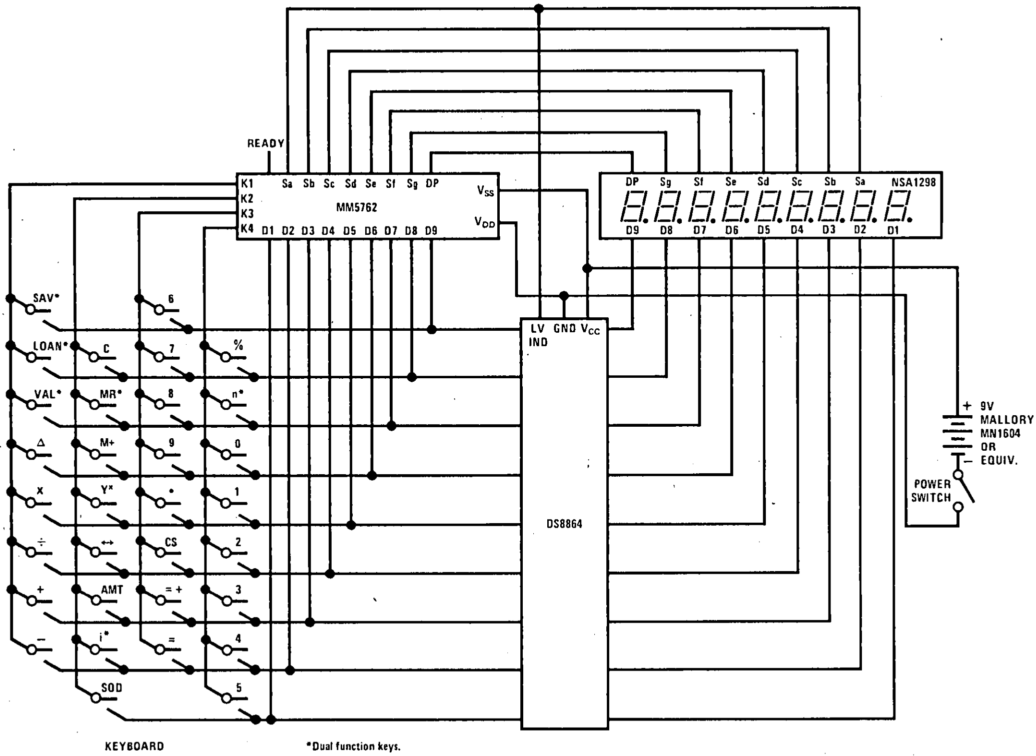


FIGURE 1. Complete Calculator Schematic

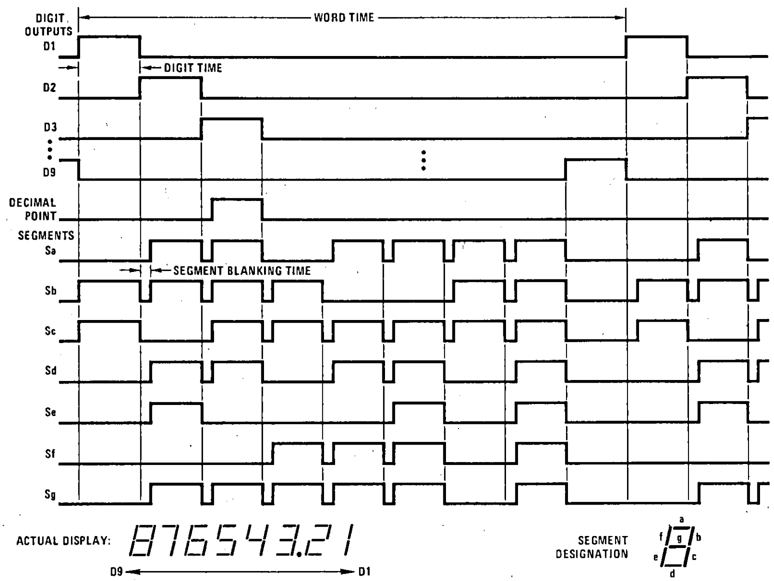


FIGURE 2. Display Timing Diagram

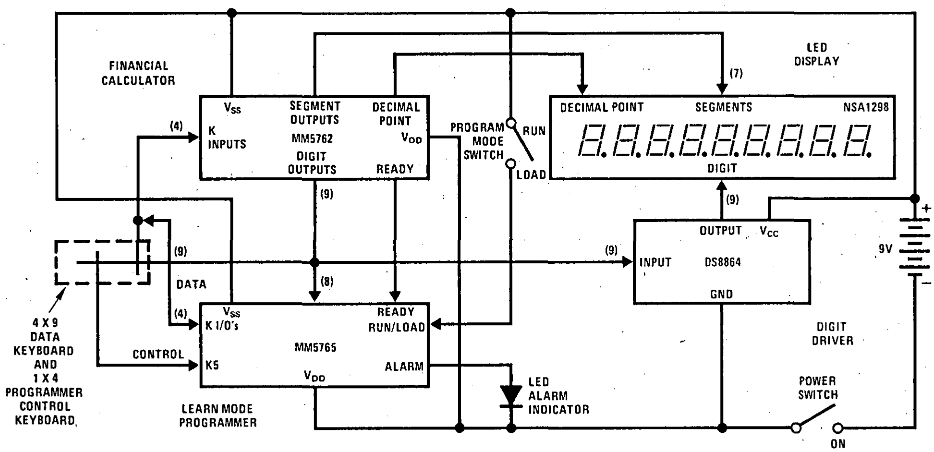


FIGURE 3. Low Cost Hand Held Programmable Financial Computer using the MM5762 Calculator and MM5765 Programmer

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5762 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3 or K4 are forced more positive than the Logical High Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after nine word times if the key input is still at a Logical High Level. As long as the key is held down (and the key input remains high) no further entry is allowed. When the key input changes to a Logical Low Level, the internal counter starts a sixteen word time-out for key release. During both entry and release time-outs the key inputs are sampled approximately every other word time for valid levels. If they are found invalid, the counter is reset and the calculator assumes the last valid key input state.

One of the popular types of low-cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristics that can generate continuous noise during "teasing" or low pressure key depressions. The MM5762 defines a series contact resistance up to 50 kΩ as a valid key closure, assuring a reliable interface for that type of keyboard.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately thirty-five seconds, an internal automatic display cutoff circuit will blank all segments and display nine decimal points. Any key depression will restore the display; to restore the display without modifying the status of the calculator, use two Change Sign key depressions.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 4 and 5.* It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

ERROR INDICATION

In the event of an operating error, the MM5762 will display all zeros and all decimal points. The error indication occurs if division by zero is attempted or either a result or intermediate value exceeds 99999999.

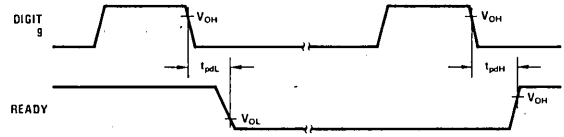


FIGURE 4. Ready Timing

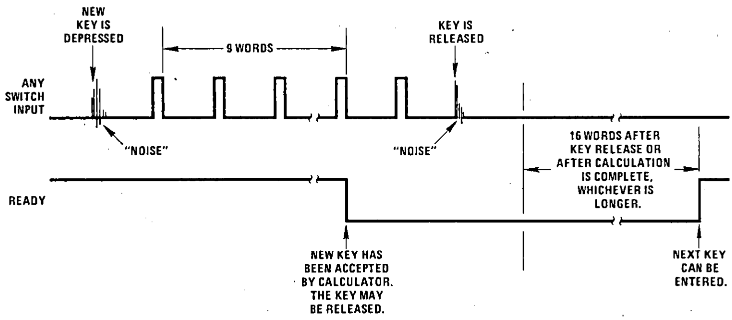


FIGURE 5. Functional Description of Ready Signal and Key Entry

The indication is cleared by depressing any key.

If an error results from a "+" or "–" key, the X-register is cleared and the last entry is saved in the A-register; all other registers are not effected. An error condition during "x" or "÷" operations clears X without changing any of the other registers.

Overflow as a result of the "Y^x," "VAL," "SAV" or "LOAN" keys clears the X-register and destroys the values in N, I and A. Y is not changed.

An attempt to raise a negative number to a power will cause the error indication to appear, the X-register will be cleared and the exponent will be stored in Y. The other registers are not changed.

Overflow as a result of "M+" destroys the value stored in M, clears X and displays the error indication. Calculations are immediately stopped and other registers are not cleared.

AUTOMATIC CONSTANT

The MM5762 retains as a constant the first factor of a multiplication calculation or the second factor of a division calculation, when that calculation is terminated by an "=" key, "%" key or "= +" key. Subsequent calculations using the stored constant are made by entering a number and operating upon it with the appropriate terminator ("=," "%" or "= +" key). The Y-register is used to store the constant in the constant mode of operation.

The calculator automatically changes to the chain mode when an "x" or "÷" key occurs in the calculation. In the chain mode, the result of each "x" or "÷" key is stored in both X and Y-registers. A new entry replaces X without altering Y. At the completion of a chain calculation, the Y-register will contain the value used as first factor of the last multiply, or the latest entry if the last operation was a divide.

Table I summarizes the four modes.

KEY OPERATIONS

(Note: Register X is always displayed.)

Clear Key, "C"

Following a number entry or a "MR" key, it clears the X-register only (clear entry). Following any other key it clears registers X, Y and A.

Number Entries

The first entry clears the X-register and enters the number into the LSD of X. Second through eighth entries (excluding a decimal point) are entered one digit to the right of the last number. The ninth, and subsequent entries are ignored. First entry after a "+," "–," or "M+" following a "+" or "–" key causes the number in the X-register to be transferred to the A-register before clearing and placing the new entry in X.

Decimal Point, "."

As the first depression of a number entry, it clears the X-register and places a point in the leftmost digit. If the previous key was a number, it enters a decimal point to the right of the last number entered. Following a "+," "–," or those keys preceding a "M+" key, the X-register is transferred to A, cleared and a decimal point entered in the leftmost digit. The last decimal point depression in a single number entry is accepted as the valid point.

Change Sign Key, "CS"

Changes sign of register X.

Addition Key, "+"

If the previous key was not a "+" or "–" key, the number in the A-register is added to the X-register, X is transferred to A, and the sum is stored in X. When the last key was a "+" or "–" key, the number in A is added to the number in X without destroying the value of A. The sum is stored in X.

Subtraction Key, "–"

If the previous key was not a "+" or "–" key, the number in the X-register is subtracted from the number in the A-register, X is transferred to A, and the difference is stored in X. When the last key was a "+" or "–" key, the number in A is subtracted from X without destroying the value of A. The result is stored in X.

Multiplication Key, "x"

If there has not been a "x" or "÷" key since the last terminator key ("=," "= +" or "%"), the value of the X-register is copied into the Y-register and the calculator is set to the chain multiply mode. In a chain calculation in which there has been a "x" key since the last terminator or "÷" key, X is multiplied by Y and the resulting product is stored in both X and Y; if a "÷" key has occured since the last terminator or "x" key, depression of "x" will divide the Y-register by the X-register, with the quotient stored in both X and Y.

Division Key, "÷"

If there has not been an "x" or "÷" key since the last terminator key ("=," "= +" or "%"), the value of the X-register is copied into the Y-register and the calculator is set to the chain divide mode. In a chain calculation if an "x" key has occured since the last terminator or "÷" key, X is multiplied by Y and the product is stored in both X and Y; if a "÷" key has occured since the last terminator or "x" key, depression of "÷" will divide the Y-register by the X-register, with the quotient stored in both X and Y.

TABLE 1. Mode Summary

MODE	KEYS THAT SET MODE	DESCRIPTION (See Calculation Examples)
CONSTANT MULTIPLY	CLEAR = = + % Δ Y^x SOD VAL SAV LOAN	Depression of an "=," "= +" or "%" key will multiply the X-register by the Y-register and replace X with the product. Y remains unchanged.
CHAIN MULTIPLY	x, Following a terminator or "÷" or "x" operation	Depression of an "=," "= +" or "%" key will multiply the X-register by the Y-register and place the product in X. Y remains unchanged.
CONSTANT DIVIDE	=, = +, % } With calculator previously in chain divide mode.	Depression of an "=," "= +" or "%" key will divide the X-register by the Y-register and replace X with the quotient. Y is unchanged.
CHAIN DIVIDE	÷, Following a terminator or "÷" or "x" operation	Depression of an "=," "= +" or "%" key will divide the Y-register by the X-register, transfer X to Y, and place the quotient in X.

Equal Key, "="

In the chain multiply mode, the value in the X-register is multiplied by the Y-register with the product stored in X. Register Y remains unchanged. In the chain divide mode, depression of "=" will divide Y by X, transfer X to Y, and place the quotient in X. If the calculator is in constant multiply, "=" will multiply X by Y, place the product in X and retain Y. For constant divide, the X-register is divided by Y, the quotient is stored in X; Y is unchanged.

The "=" key always rounds the answer stored in X to two places to the right of the decimal point, and clears register A.

Percent Key, "%"

This key acts exactly like the "=" key except the value of X is divided by 100 and copied into register A before performing the required operation. Register A is not cleared. The result stored in the X-register is rounded to two decimal positions.

Automatic Accumulation Key, "= +"

It acts just like the "=" key in all modes. After the result is stored in X, the value of X is added to the number in the M-register. The result stored in X and accumulated into M is rounded to two decimal places. Register A is cleared.

Memory Plus Key, "M+"

The number in the X-register is accumulated into the M-register. Registers X and A are not changed, so the repeat addition or subtraction conditions that existed before accumulation to memory are still valid.

Memory Recall/Memory Clear Key, "MR"

Following any key except "MR," the value of the M-register is copied into the X-register. If the preceding key was "+," "−" or "M+" following "+" or "−," the number in the X-register is transferred to the A-register before M is recalled. Following another "MR" key, the M-register is transferred to X, then cleared.

Delta Percent Key, "Δ"

The value of X is subtracted from the Y-register, the difference is divided by the value of X and placed in X. The new value of X is multiplied by 100 and rounded to two digit places. Y retains the difference between the original values of X and Y; register A is unchanged. Calculator mode is set to constant multiply.

Power Key, "Y^X"

When the calculator is in either the chain or constant multiply modes, depression of "Y^X" raises the number in the Y-register to the power of the X-register and replaces X with the result. (Thus, to raise two to the fifth power, use the sequence: "2," "x," "5," "Y^X.") If the calculator is in the constant or chain divide modes, the value of Y is raised to the inverse of X power; i.e., the key sequence "5," "÷," "2," "Y^X," results in the calculation of 5 raised to the 1/2 power. The original value of X is retained in Y and register A is cleared. The calculator is set to the constant multiply mode. Results computed with the "Y^X" key are rounded to five places.

Exchange Key, "↔"

The X and Y-registers are exchanged. No other registers are effected.

Interest Entry Key, "i"

If the sign of the number in the X-register is positive, "i" divides the number by 100 and stores the quotient in X and the I-register. If the value of X is initially negative, "i" changes the sign, divides by 1200 and stores the quotient in both X and I; i.e., the interest will be compounded monthly.

Number of Periods Entry Key, "n"

If the sign of the number in the X-register is positive, X is copied into register N. A negative value of X is changed to a positive number, multiplied by 12 and the product stored in N and X.

Amount Entry Key, "AMT"

The value of the X-register is copied into the Y-register. No other registers are effected.

Value Key, "VAL"

If the number in the X-register is positive, the "VAL" key will compute *future value*: the sum of money available at the end of n periods from the present date (N-register) that is equivalent to the present amount (Y-register) with interest i (I-register). When the sign of the number in X is negative, the "VAL" key will compute *present value:* the sum of money necessary today to accumulate the future amount contained in Y over the n periods of N at the interest rate per interest period that is stored in I. Thus, to compute *future value,* simply enter i, n and amount in any order and press "VAL." For *present value,* precede "VAL" with "CS," setting a negative sign in X. Registers Y, N and I are not altered; X is replaced by the computed value and register A is cleared. The calculator is set to the constant multiply mode. The result is rounded to two decimal places.

Savings Deposit Key, "SAV"

If the number in the X-register is negative, the "SAV" key will compute the amount to be deposited at the end of each period in a *sinking fund* for the number of periods, n, contained in register N, at an interest rate, i, contained in register I, compounded each time period, to accumulate the desired amount, contained in register Y. When the sign of the number in X is positive, the "SAV" key will compute the amount in a sinking fund if the number in Y is deposited at the end of n time periods (N-register) at an interest rate per time period i (I-register), compounded each time period. Thus, to compute the required *sinking fund deposit* to accumulate a desired amount over a given period of time, enter i, n and the amount in any order using the "i," "n" and "AMT" keys, then "CS" and "SAV," To find the amount in the *sinking fund*, simply enter i, n and the periodic amount of deposit and press "SAV." Registers N, I or Y are not altered by the calculation, register A is cleared and register X contains the computed value. The calculator is set to the constant multiply mode. Results are rounded to two decimal places.

Loan Installment Key, "LOAN"

If the number in the X-register is negative, the "LOAN" key will compute the end-of-period payment or receipt required over the number of time periods contained in the N-register at an interest rate per time period equal to the value in the I-register to support a loan equal to the amount stored in the Y-register. When the sign of the X-register is positive, "LOAN" computes the amount that can be loaned for a given end-of-period payment stored in Y over the number of time periods contained in N at the interest rate per time period of I, compounded each time period. Thus, to compute the required installment on a given loan, enter the amount of the loan using the "AMT" key, the interest rate using "i" and the number of periods with "n," press "CS" to enter a negative sign in register X, then "LOAN." To compute how much can be borrowed given a fixed payment, enter the payment amount, number of periods and interest rate, then "LOAN." "AMT," "i" or "n" can always be entered in any order. Registers N, I or Y are not altered by the calculation; register A is cleared and register X will contain the computed value. The calculator is set to the constant multiply mode. The result is rounded to two decimal places.

Sum-of-Digits Key, "SOD"

Following a "+" or "−" key, it transfers the number in register X to register A and computes a first *sum-of-digits* depreciation on that number by multiplying it by the ratio of the number in the N-register to the sum-of-digits of N. The result is rounded to two decimal places and stored in X; the difference between the initial and final values of X, the *depreciable value*, is stored in registers Y and A. N is decremented by one. (Therefore, to find depreciable value, simply use the "←→" key.) Subsequent depressions of the "SOD" key will compute successive depreciation and depreciable value amounts using the original value of N and present values stored in N and A. N is decremented by one after each computation. The number to be depreciated (or the loan amount in a "Rule of 78's" interest calculation) is always entered with a "+" or "−" key and the number of periods with the "n" key, without regard to key order. If the key preceding "SOD" is not "+" or "−," the sum-of-digits computation is performed on the number in the A-register without the number in X first being transferred to A. The result will be rounded to two decimal places; calculator mode is set to constant multiply.

EXAMPLES

1. Addition or subtraction

$$\begin{array}{r} 2.0 \\ 3.2 \\ -12.3 \\ \hline \end{array}$$

KEYS	DISPLAY	COMMENTS
2	2	
+	2.	
3	3	
.	3.	
2	3.2	
+	5.2	
1	1	
2	1 2	
.	1 2.	
3	1 2.3	
−	−7.1	Note adding machine notation

2. Repeat add or subtract

KEYS	DISPLAY	COMMENTS
3	3	
.	3.	
1	3.1	
+	3.1	
+	6.2	
+	9.3	
−	6.2	

3. Chain multiplication or division

	KEYS	DISPLAY	COMMENTS
a)	1	1	
	x	1.	
	2	2	
	x	2.	
	3	3	
	.	3.	
	1	3.1	
	x	6.2	
	4	4	
	.	4.	
	2	4.2	
	=	2 6.0 4	

EXAMPLES (continued)

3. (continued)

	KEYS	DISPLAY	COMMENTS
b)	1	1	
	0	1 0	
	÷	1 0.	
	2	2	
	÷	5.	
	1	1	
	0	1 0	
	÷	.5	
	2	2	
	=	.2 5	
c)	2	2	
	0	2 0	
	x	2 0.	
	4	4	
	÷	8 0.	
	8	8	
	÷	1 0.	
	7	7	
	x	1.4 2 8 5 7 1 4	
	4	4	
	=	5.7 1	"=" rounds to two decimal places

4. Constant multiplication or division.

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	x	3.	
	2	2	
	=	6.	
	4	4	
	=	1 2.	First factor in constant multiply
	5	5	
	.	5.	
	2	5.2	
	=	1 5.6	
	=	4 6.8	15.6 is re-entered and multiplied by constant
b)	5	5	
	÷	5.	
	2	2	
	=	2.5	
	4	4	
	=	2.	Second factor in constant divide
	5	5	
	.	5.	
	2	5.2	
	=	2.6	
	=	1.3	2.6 is re-entered and divided by constant

5. To perform products of sums.

(5 + 4) x (3 + 2)/(6 + 7) = ?

KEYS	DISPLAY	COMMENTS
5	5	
+	5.	
4	4	
+	9.	
x	9.	Chain multiply mode is set
3	3	
+	3.	
2	2	
+	5.	
÷	4 5.	(5 + 4) x (3 + 2) is executed
6	6	
+	6.	
7	7	
+	1 3.	
=	3.4 6	45 ÷ (6 + 7) is executed

6. Calculate percentage.

KEYS	DISPLAY	COMMENTS
3	3	
0	3 0	
0	3 0 0	
.	3 0 0.	
2	3 0 0.2	
5	3 0 0.2 5	
x	3 0 0.2 5	
5	5	
%	1 5.0 1	"Live %" key

7. Perform add on and discount

KEYS	DISPLAY	COMMENTS
a) Add-On: $125 plus 5%		
1	1	
2	1 2	
5	1 2 5.	
x	1 2 5.	
5	5	
%	6.2 5	5% of 125 is displayed
+	1 3 1.2 5	125 + 5% is displayed
b) Discount: $532.10 by 6%		
5	5	
3	5 3	
2	5 3 2	
.	5 3 2.	
1	5 3 2.1	
x	5 3 2.1	
6	6	
%	3 1.9 3	6% of 532.1 is displayed
–	5 0 0.1 7	532.1 – 6% is displayed

8. Perform change sign.

KEYS	DISPLAY	COMMENTS
1	1	
2	1 2	Change sign does not terminate entry.
CS	–1 2	
3	–1 2 3	
.	–1 2 3.	
CS	1 2 3.	
5	1 2 3.5	
CS	–1 2 3.5	
6	–1 2 3.5 6	

9. Perform exchange registers (X ↔ Y).

	KEYS	DISPLAY	COMMENTS
a)	5	5	
	x	5.	
	3	3	
	=	1 5.	5 is initially constant multiplier
	4	4	
	↔	5.	4 is now constant multiplier
	=	2 0.	
b)	6	6	
	÷	6.	
	3	3	Numerator and denominator are exchanged
	↔	6.	
	=	.5	

10. Accumulate in memory, recall and clear memory

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	M+	3.	Accumulate in memory
	4	4	
	M+	4.	Accumulate in memory
	5	5	
	MR	7.	Recall memory
	MR	7.	Recall and clear memory
	MR	0.	Recall and clear memory

8

EXAMPLES (continued)

10. (continued)

	KEYS	DISPLAY	COMMENTS
b)	5	5	
	+	5.	
	6	6	
	+	1 1.	
	M+	1 1.	Accumulate in memory
	7	7	
	+	1 8.	
	M+	1 8.	11 + 18 is accumulated in M
	+	2 5.	Repeat add
	3	3	
	2	3 2	
	.	3 2.	
	2	3 2.2	
	CS	−3 2.2	
	M+	−3 2.2	29 − 32.2 is accumulated in M
	9	9	
	+	3 4.	
	MR	−3.2	Accumulated value of M is recalled
	+	3 0.8	
	MR	−3.2	Accumulated value of M is recalled
	MR	−3.2	M is cleared
	MR	0.	

11. Accumulate in memory with the use of the "=+" key.

KEYS	DISPLAY	COMMENTS
5	5	
x	5.	
3	3	
= +	1 5.	5 x 3 = 15 is added to M
4	4	
.	4.	
2	4.2	
x	4.2	
3	3	
= +	1 2.6	12.6 is added to M
6	6	
÷	6.	
7	7	Rounded to 2 decimal places
= +	.8 6	and added to memory
9	9	Note method of multiplying
CS	−9	negative number
x	−9.	
4	4	
= +	−3 6.	−3 6. added to memory
MR	−7.5 4	

12. Raising a number to a power.

	KEYS	DISPLAY	COMMENTS
a) $2^5 = 32$			
	2	2	
	x	2.	
	5	5	
	Y^x	3 2.	
b) $5^{1.5} = 11.18$			
	5	5	
	x	5.	
	1	1	
	.	1.	
	5	1.5	
	Y^x	1 1.1 8	Rounded to five digits; trailing zero is suppressed
c) $3^{-5} = 0.00412$			
	3	3	
	x	3.	
	5	5	
	CS	−5	
	Y^x	.0 0 4 1 2	Rounded to five digits

13. Raising a number to a fractional power.

	KEYS	DISPLAY	COMMENTS
a) $5^{1/2} = 2.2361$			
	5	5	
	÷	5.	
	2	2	
	Y^x	2.2 3 6 1	Rounded to five digits
b) $6^{1/3} = 1.8171$			
	6	6	
	÷	6.	
	3	3	
	Y^x	1.8 1 7 1	Rounded to five digits

FINANCIAL EXAMPLES

1. Future Value Computations

To find the accumulated amount in a savings account at the end of 9 years when a) $2500.00 is deposited at 5.25% interest compounded monthly. b) $3000. c) $3000 at 5.00% interest. d) $3000 at 5.00% interest for 10 years.

	KEYS	DISPLAY	COMMENTS
a)	9	9	Number of years
	CS	−9	Compounded monthly
	n	1 0 8.	Store 9 x 12 in N
	5.25	5.2 5	Interest
	CS	−5.25	Compounded monthly
	i	.0 0 4 3 7 5	Store 5.25/1200 in I
	2500	2 5 0 0	Original deposit
	AMT	2 5 0 0	Store in Y
	VAL	4 0 0 5.8 7	Rounded to two decimal places
b)	3000	3 0 0 0	
	AMT	3 0 0 0.	New deposit stored in Y
	VAL	4 8 0 7.0 4	
c)	5	5	
	CS	−5	
	i	.0 0 4 1 6 6 6 6	New interest rate in I
	VAL	4 7 0 0.5 3	
d)	10	1 0	
	CS	−1 0	
	n	1 2 0.	Enter 10 x 12 in N
	VAL	4 9 4 1.0 2	

2. Present Value Computations

To find the amount to be deposited to accumulate a) $5000 in 7 years at 4.5% interest compounded monthly. b) $10,000. c) $10,000 in 7.5 years.

	KEYS	DISPLAY	COMMENTS
a)	7	7	Number of years
	CS	−7	Compounded monthly
	n	8 4.	Enter 7 x 12 in N
	4.5	4.5	Interest
	CS	−4.5	Compounded monthly
	i	.0 0 3 7 5	Enter 4.5/1200 in I
	5000	5 0 0 0	Future value
	AMT	5 0 0 0.	Enter amount in Y
	CS	−5 0 0 0.	
	VAL	3 6 5 1.1	Present value required
b)	10000	1 0 0 0 0	
	AMT	1 0 0 0 0.	New future value in Y
	CS	−1 0 0 0 0.	
	VAL	7 3 0 2.1 9	Present value required
c)	7.5	7.5	
	CS	−7.5	
	n	9 0.	New time period in N
	CS	−9 0.	
	VAL	7 1 4 0.0 3	Present value required

FINANCIAL EXAMPLES (continued)

3. To find the amount that a) must be deposited monthly in a savings account at an interest rate of 5.5% compounded monthly for 5 years to accumulate $15,000. b) compounded, and deposited quarterly.

	KEYS	DISPLAY	COMMENTS
a)	5.5	5.5	Interest
	CS	−5.5	Compound monthly
	i	.0 0 4 5 8 3 3 3	Enter 5.5/1200
	5	5	Number of years
	CS	−5	Compound monthly
	n	6 0.	Ent 5 x 12 in N
	15000	1 5 0 0 0.	Future value
	AMT	1 5 0 0 0.	Entered in Y
	CS	−1 5 0 0 0.	
	SAV	2 1 7.7 7	Monthly deposit required
b)	5.5	5.5	Interest
	÷	5.5	
	4	4	Compound quarterly
	÷	1.3 7 5	Use "÷" instead of "=" for maximum accuracy
	i	.0 1 3 7 5	Enter 5.5/400
	C		Terminate chain calculation
	5	5	Number of years
	x	5.	Compound quarterly
	4	4	
	=	2 0.	
	n	2 0.	Enter 5 x 4 in N
	15000	1 5 0 0 0	Re-enter FV in Y
	AMT	1 5 0 0 0.	Amount
	CS	−1 5 0 0 0.	
	SAV	6 5 6.7 1	Quarterly deposit required

4. To find the amount accumulated a) if $100 is deposited at the end of each month for 6 years in a savings account at an interest rate of 4.75%, compounded monthly, b) at 7.5%, c) at 4.75% for 9 years.

	KEYS	DISPLAY	COMMENTS
a)	4.75	4.7 5	Interest
	CS	−4.75	Compounded monthly
	i	.0 0 3 9 5 8 3 3	4.75/1200 entered in I
	6	6	
	CS	−6	
	n	7 2.	
	100	1 0 0	
	AMT	1 0 0.	
	SAV	8 3 1 1.9 3	Accumulated sinking fund
b)	7.5	7.5	
	CS	−7.5	
	n	9 0.	
	SAV	1 0 7 8 6.3 7	
c)	4.75	4.7 5	
	CS	−4.7 5	
	i	.0 0 3 9 5 8 3 3	
	9	9	
	CS	−9	
	n	1 0 8.	
	SAV	1 3 4 4 3.1 7	

5. To find the monthly payments of a loan of $5,000 at an annual percentage rate of a) 18% for 5 years, b) 12%.

	KEYS	DISPLAY	COMMENTS
a)	18	1 8	Interest
	CS	−1 8	Compounded monthly
	i	.0 1 5	18/1200 entered in I
	5	5	Number of years
	CS	−5	Compounded monthly
	n	6 0.	5 x 12 entered in N
	5000	5 0 0 0	Loan amount
	AMT	5 0 0 0.	Entered in Y
	CS	−5 0 0 0.	
	LOAN	1 2 6.9 7	Required monthly installment; rounded to two decimal places

5. (continued)

	KEYS	DISPLAY	COMMENTS
b)	12	1 2	
	CS	−1 2	
	i	.0 1	New interest entered in I
	CS	−.0 1	
	LOAN	1 1 1.2 2	New monthly installment

6. To find the amount of a loan with monthly payments of $125, and an interest rate of 9% for 3 years. b) 4 years. c) $120 for 4 years.

	KEYS	DISPLAY	COMMENTS
a)	9	9	Interest
	CS	−9	Compounded monthly
	i	.0 0 7 5	9/1200 entered in I
	3	3	Number of years
	CS	−3	Compounded monthly
	n	3 6.	3 x 12 entered in N
	125	1 2 5	
	AMT	1 2 5.	Payment amount entered in Y
	LOAN	3 9 3 0.8 5	Loan amount is computed
b)	4	4	
	CS	−4	New number of periods entered in N
	n	4 8.	
	LOAN	5 0 2 3.1	
c)	120	1 2 0	New payment amount entered in Y
	AMT	1 2 0.	
	LOAN	4 8 2 2.1 7	

7. To find the amount of change and the percent change of a house now valued at $56,500 which was previously purchased for $49,750. b) present value of $30,000.

	KEYS	DISPLAY	COMMENTS
a)	56500	5 6 5 0 0	Present value
	AMT	5 6 5 0 0.	Enter in Y
	49750	4 9 7 5 0	Past value
	Δ	1 3.5 7	% change
	↔	6 7 5 0.	Amount change
b)	30000	3 0 0 0 0	New present value
	AMT	3 0 0 0 0.	
	49750	4 9 7 5 0	
	Δ	−3 9.7	Negative % change
	↔	−1 9 7 5 0.	Amount change

8. Performing a sum-of-digits depreciation. Find the depreciation and depreciable value for each year, on an item with an initial cost of $3,500.00 and a salvage value at the end of 8 years of $675.00

KEYS	DISPLAY	COMMENTS
3500	3 5 0 0	
+	3 5 0 0	Enter initial value
675	6 7 5	Enter salvage value
−	2 8 2 5.	Calculate change
8	8	
n	8.	Enter period in N
SOD	6 2 7.7 8	1st year depreciation. Rounded to two decimal places
↔	2 1 9 7.2 2	Depreciable value
SOD	5 4 9.3 1	2nd year depreciation
↔	1 6 4 7.9 1	Depreciable value
SOD	4 7 0.8 3	3rd year depreciation
↔	1 1 7 7.0 8	Depreciable value
SOD	3 9 2.3 6	4th year depreciation
↔	7 8 4.7 2	Depreciable value
SOD	3 1 3.8 9	5th year depreciation
↔	4 7 0.8 3	Depreciable value
SOD	2 3 5.4 2	6th year depreciation
↔	2 3 5.4 1	Depreciable value
SOD	1 5 6.9 4	7th year depreciation
↔	7 8.4 7	Depreciable value
SOD	7 8.4 7	8th year depreciation
	0.	Depreciable value

MM5763 statistical calculator
general description

The single-chip MM5763 Statistical Calculator was developed using a metal-gate, P-channel enhancement and depletion mode MOS/LSI technology with low end-product cost as a primary objective. A complete calculator as shown in *Figure 1* requires only the MM5763, a keyboard, DS8864 digit driver, NSA1298 LED display, 9V battery and appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and 7-segment output display encoding are included on-chip and require no external components. Segments can usually be driven directly from the MM5763, as it typically sources about 8.5 mA of peak current. [Note: The typical duty cycle of each digit is 0.104; average LED segment current is therefore approximately 0.104 (8.5 mA), or 0.9 mA average. Correspondingly the worse-case average segment current is 0.104 (5.0 mA), or 0.52 mA.] The ninth digit (left-most) is used for the negative sign, or the decimal point of a number less than unity.

An internal power-on clear circuit is included that clears all registers, including the memory, when V_{DD} and V_{SS} are initially applied to the chip.

Trailing zero suppresion allows convenient reading of the left justified display, and conserves power. The DS8864 digit driver is capable of sensing a low battery voltage and providing a signal during Digit 9 time that can be used to turn on one of the segments as an indicator. Typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff is included. If no key closure occurs for approximately 25 seconds, all numbers are blanked and all decimal points displayed.

The Ready output signal is used to indicate calculator status. It is useful in providing synchronization information for testing or applications where the MM5763 is used with other logic or integrated circuits; e.g., with the MM5765 Programmer *(Figure 3).*

Thirty-two keys are arranged in a four-by-nine matrix as shown in *Figure 1.* There is an automatic constant feature.

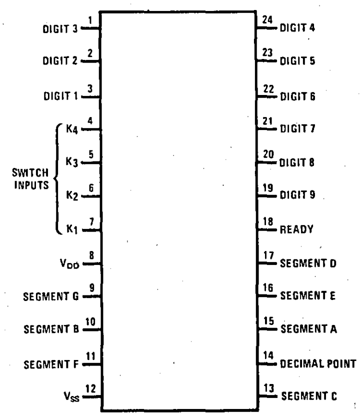
The user has access to eight registers designated X, T, A, C, Y, S, N and M. The X-register is used for keyboard entry and display. The T and A-registers are used in multiply/divide and add/subtract calculations, respectively. C, Y, S and N-registers are used specifically for calculating the statistical functions. M is an accumulating storage memory. Statistical key functions use essentially all registers, including M.

Data is entered into the calculator in floating point business notation. All entries and results are displayed left justified with insignificant zeros to the right of the decimal point suppressed. All intermediate results of a chain calculation are floating point. Terminating keys: equal, percent and "= +" round the display result to two decimal places.

features

- Complete business and statistical capability
  - Arithmetic functions +, −, x, ÷
  - Per cent: includes markup and discount
  - Statistical functions:
    - ▲ "Σx" key sums X, X^2 and N
    - ▲ "Σy" key sums Y, Y^2 and X · Y
    - ▲ "REMOVE x" key corrects "Σx" mistake
    - ▲ "REMOVE y" key corrects "Σy" mistake
    - ▲ "FREQ x" key sums grouped data for standard deviation
    - ▲ "$\overline{X}$, SD" key calculates standard deviation and mean
    - ▲ "COR-SLOPE" key performs linear regression giving coefficient of correlation, slope, and intercept
    - ▲ "INT" key calculates y-intercept on line for given x
- Square root
- Accumulating memory
- Auto constant
- Business notation
  - +, − "adding machine" notation
  - x, ÷, = algebraic notation
- Eight full digits
- Power-on clear
- Display cutoff
- Low system cost

connection diagram (DIP Top View)



Order Number MM5763N
See Package 22

MM5763

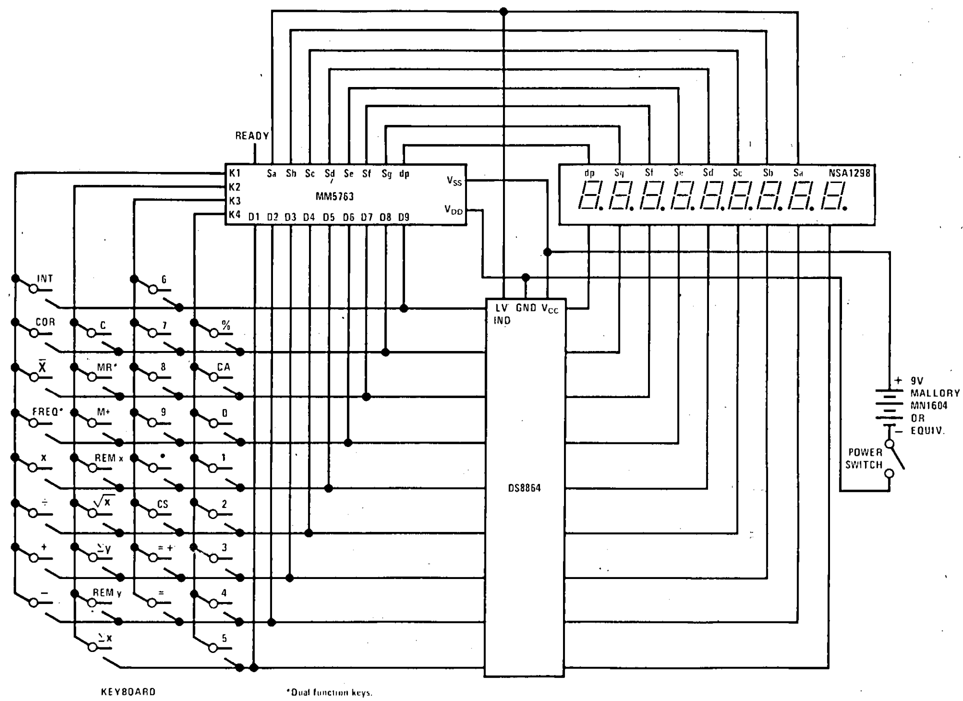


FIGURE 1. Complete Calculator Schematic

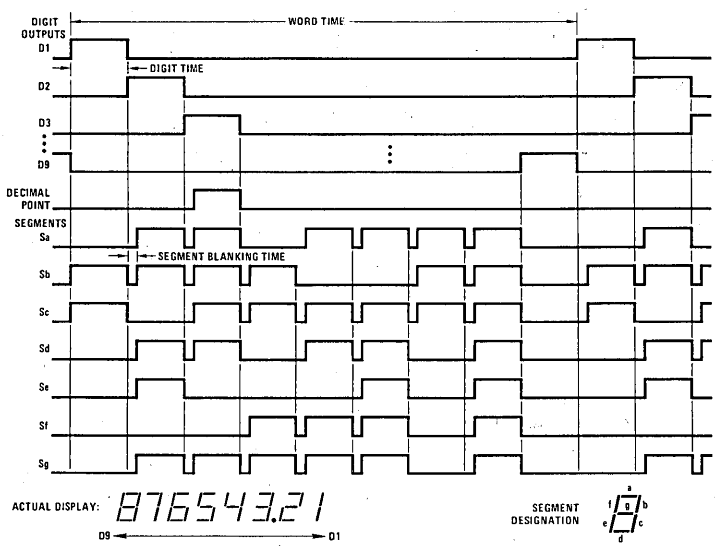


FIGURE 2. Display Timing Diagram.

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}. (All other pins connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12.0
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$
V_{SS} always defined as most positive supply voltage.

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}-9.5V$, $T_A = 25°C$		8.0	16.0	mA
Keyboard Scan Input Levels (K1, K2, K3 and K4)					
Logical High Level	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	$V_{SS}-2.5$			V
Logical Low Level	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-6.0$	V
Digit Output Levels					
Logical High Level (V_{OH})	R_{LOAD} = 3.2 kΩ to V_{DD}				
	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	$V_{SS}-1.5$			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-6.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-7.0$	V
Segment Output Current (Sa through Sg and Decimal Point)	$T_A = 25°C$				
	$V_{OUT} = V_{SS}-3.6V$, $V_{DD} = V_{SS}-6.5V$	−5.0	−8.5		mA
	$V_{OUT} = V_{SS}-5V$, $V_{DD} = V_{SS}-8V$		−10.0		mA
	$V_{OUT} = V_{SS}-6.5V$, $V_{DD} = V_{SS}-9.5V$			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	$I_{OUT} = -0.4$ mA	$V_{SS}-1.0$			V
Logical Low Level (V_{OL})	$I_{OUT} = 10\mu A$			$V_{DD}+1.0$	V

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (*Figure 2*)		0.32	0.8	2.0	ms
Digit Time (*Figure 2*)		36	89	222	μs
Segment Blanking Time (*Figure 2*)		2	5.5	14	μs
Digit Output Transition Times (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF, R_{LOAD} = 9.6 kΩ		2		μs
Keyboard Inputs High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		μs
Ready Output Propagation Time (*Figure 3*)					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	10		50	μs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF			1	ms
Key Input Time-out					
Key Entry		2.8	7.2	18	ms
Key Release		5.1	12.8	32	ms
Display Cutoff Time (The time after the last valid key closure that all numbers will be blanked and all decimal points displayed.)		10	25	63	sec

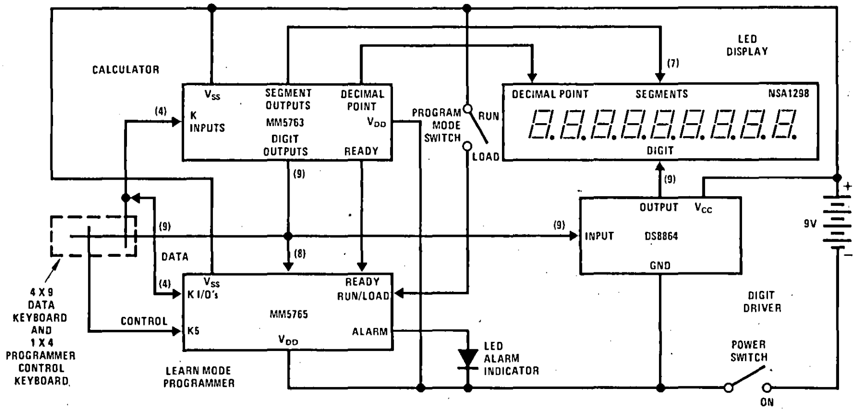


FIGURE 3. Low Cost Handheld Programmable Statistician Computer Using the MM5763 Calculator and MM5765 Programmer.

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5763 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3 or K4 are forced more positive than the Logical High Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after nine word times if the key input is still at a Logical High Level. As long as the key is held down (and the key input remains high) no further entry is allowed. When the key input changes to a Logical Low Level, the internal counter starts a sixteen word time-out for key release. During both entry and release time-outs the key inputs are sampled approximately every other word time for valid levels. If they are found invalid, the counter is reset and the calculator assumes the last valid key input state.

One of the popular types of low-cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5763 defines a series contact resistance up to 50 kΩ as a valid key closure, assuring a reliable interface for that type of keyboard.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately twenty-five seconds, an internal automatic display cutoff circuit will blank all segments and display nine decimal points. Any key depression will restore the display; to restore the display without modifying the status of the calculator, use two Change Sign key depressions.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 4 and 5.* It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

ERROR INDICATION

In the event of an operating error, the MM5763 will display all zeros and all decimal points. The error indication occurs if division by zero is attempted or either a result or intermediate value exceeds 99999999.

The indication is cleared by depressing any key.

If an error results from a "+" or "−" key, the X-register is cleared and the last entry is saved in the A-register; all other registers are not effected. An error condition during "x" or "÷" operations clears X without changing any of the other registers.

Overflow as a result of the statistical keys can effect any register they use; "CA" should be depressed if an error occurs.

Overflow as a result of "M+" saves the value stored in M, clears X and displays the error indication. Calculations are immediately stopped and other registers are not cleared.

AUTOMATIC CONSTANT

The MM5763 retains as a constant the first factor of a multiplication calculation or the second factor of a division calculation, when that calculation is terminated by "=" key, "%" key or "= +" key. Subsequent calculations using the stored constant are made by entering a number and operating upon it with the appropriate terminator ("=," "%" or "= +" key). The T-register is used to store the constant in the constant mode of operation.

The calculator automatically changes to the chain mode when a "x" or "÷" key occurs in the calculation. In the chain mode, the result of each "x" or "÷" key is stored in both X and T-registers. A new entry replaces X without altering T. At the completion of a chain calculation, the T-register will contain the value used as first factor of the last multiply, or the latest entry if the last operation was a divide.

Table I summarizes the four modes.

TABLE I. Mode Summary

MODE	KEYS THAT SET MODE	DESCRIPTION (See Calculation Examples)
CONSTANT MULTIPLY	"CLEAR" "=" "=+" "%"	Depression of an "=," "= +" or "%" key will multiply the X-register by the T-register and replace X with the product. T remains unchanged.
CHAIN MULTIPLY	"x," following a terminator, or "÷" or "x" operation	Depression of an "=," "= +" or "%" key will multiply the X-register by the Y-register and place the product in X. T remains unchanged.
CONSTANT DIVIDE	"=" "= +" "%" } With calculator previously in chain divide mode.	Depression of an "=," "= +" or "%" key will divide the X-register by the T-register and replace X with the quotient. T is unchanged.
CHAIN DIVIDE	"÷," following a terminator or "÷" or "x" operation	Depression of an "=," "= +" or "%" key will divide the T-register by the X-register, transfer X to T, and place the quotient in X.

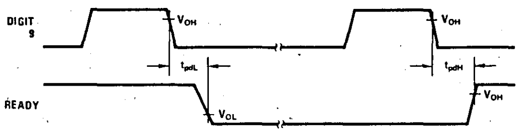


FIGURE 4. Ready Timing.

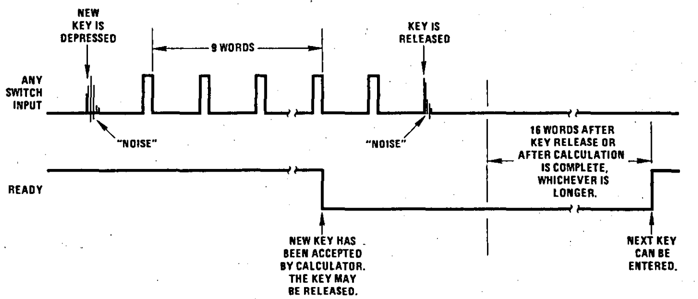


FIGURE 5. Functional Description of Ready Signal and Key Entry.

KEY OPERATIONS

(Note: Register X is always displayed.)

Clear Key, "C"

Following a number entry key, it clears the X-register only (clear entry). Following any other key it clears registers X, K, C, S, N and T.

Clear All Key, "CA"

Clears all registers and sets the calculator to the constant multiply mode.

Number Entries

The first entry clears the X-register and enters the number into the LSD of X. Second through eighth entries (excluding a decimal point) are entered one digit to the right of the last number. The ninth, and subsequent entries are ignored. First entry after a "+," "–," or "M+" following a "+" or "–" key causes the number in the X-register to be transferred to the A-register before clearing and placing the new entry in X.

Decimal Point, "."

As the first depression of a number entry, it clears the X-register and places a point in the left most digit. If the previous key was a number, it enters a decimal point to the right of the last number entered. Following a "+," "–," or "M+" following a "+" or "–," the X-register is transferred to A, cleared and a decimal point entered in the leftmost digit. The last decimal point depression of a number entry is accepted as the valid point.

Change Sign Key, "CS"

Changes sign of register X.

Addition Key, "+"

If the previous key was not a "+" or "–" key, the number in the A-register is added to the X-register, X is transferred to A, and the sum is stored in X. When the last key was a "+" or "–" key, the number in A is added to the number in X without destroying the value of A. The sum is stored in X.

MM5763

Subtraction Key, "–"

If the previous key was not a "+" or "–" key, the number in the X-register is subtracted from the number in the A-register, X is transferred to A, and the difference is stored in X. When the last key was a "+" or "–" key, the number in A is subtracted from X without destroying the value of A. The result is stored in X.

Multiplication Key, "x"

If there has not been a "x" or "÷" key since the last terminator key ("=," "= +" or "%"), the value of the X-register is copied into the T-register and the calculator is set to the chain multiply mode. In a chain calculation in which there has been a "x" key since the last terminator or "÷" key, X is multiplied by T and the resulting product is stored in both X and T; if a "÷" key has occured since the last terminator or "x" key, depression of "x" will divide the T-register by the X-register, with the quotient stored in both X and T.

Division Key, "÷"

If there has not been a "x" or "÷" key since the last terminator key ("=," "= +" or "%"), the value of the X-register is copied into the T-register and the calculator is set to the chain divide mode. In a chain calculation if a "x" key has occured since the last terminator or "÷" key, X is multiplied by T and the product is stored in both X and T; if a "÷" key has occured since the last terminator or "x" key, depression of "÷" will divide the T-register by the X-register, with the quotient stored in both X and T.

Equal Key, "="

In the chain multiply mode, the value in the X-register is multiplied by the T-register with the product stored in X. Register T remains unchanged. In the chain divide mode, depression of "=" will divide Y by X, transfer X to T, and place the quotient in X. If the calculator is in constant multiply, "=" will multiply X by T, place the product in X and retain T. For constant divide, the X-register is divided by T, the quotient is stored in X; T is unchanged.

The "=" key always rounds the answer stored in X to two places to the right of the decimal point, and clears register A.

Per Cent Key, "%"

This key acts exactly like the "=" key except the value of X is divided by 100 and copied in register A before performing the required operation. Register A is not cleared. The result stored in the X-register is rounded to two decimal positions.

Automatic Accumulation Key, "= +"

It acts just like the "=" key in all modes. After the result is stored in X, the value of X is added to the number in the M-register. The result stored in X and accumulated into M is rounded to two decimal places. Register A is cleared.

Memory Recall/Memory Clear Key, "MR"

Following any key except "MR," the value of the M-register is copied in to the X-register. If the preceding key was "+," "–" or "M+" following "+" or "–," the number in the X-register is transferred to the A-register before M is recalled. Following another "MR" key, the M-register is transferred to X, then cleared.

Memory Plus Key, "M+"

The number in the X-register is accumulated in the M-register. Registers X and A are not changed, so the repeat addition or subtraction conditions that existed before accumulation to memory are still valid.

Square Root Key, "$\sqrt{x}$"

The absolute value of the number in the X-register is replaced with its square root.

Sum of X Key, "Σx"

Adds X to the C-register, adds the square of X to the T-register, saves the value of X (to four decimal places) in the Y-register and increments N by one. The operation is completed by copying N into X. The maximum value of N is 99. The register returns to zero on the 100th entry.

Sum of Y Key, "Σy"

Adds the value of X to the A-register, adds the square of X to the M-register, adds the product of X and Y to the S-register, and recalls N to X.

Remove X Key, "REM X"

This is used to delete a data point previously entered by "Σx" key. It subtracts X from C, subtracts the square of X from T, saves X to four decimal places in Y, decrements N by one and copies the new value of N in to X.

Remove Y Key, "REM Y"

This is used to delete an incorrect data point previously entered by the "Σy" key. It subtracts X from A, subtracts the square of X from M, subtracts the product of X and Y from S and copies N to X.

Frequency of X Key, "FREQ"

This is used to sum grouped (identical) data entries for mean and standard deviation computations. If the sign of X is positive, "FREQ" performs the "Σx" operation X – 1 times. When X is negative, "FREQ" performs the "REM X" function $|X| - 1$ times.

Mean and Standard Deviation Key, "$\bar{X}$, SD"

Computes both the arithmetic mean and the standard deviation of data points (entered by the "Σx" and "FREQ" keys) with a single key depression. The mean is stored in register X (and therefore is the initial result displayed). Standard deviation is stored in registers A and M and is displayed by using the "MR" key. Registers T, C and N are saved so that additional data points may be entered or deleted, and new mean and standard deviation values calculated.

8

Correlation Coefficient and Slope Key, "COR SLOPE"

The correlation coefficient and slope of a least squares line fit of accumulated paired data values (that have been entered with the "Σx" and "Σy" keys) are computed with a single key stroke. The correlation coefficient is stored in registers X and S (and therefore is the initial result displayed). Slope is in M and is obtained by using the "MR" key. Registers T and C are lost.

Y-Intercept Key, "INT"

After the "COR SLOPE" key has been used to compute a least squares line fit on a set of paired data values, any y-coordinate corresponding to a given x-coordinate lying on that line can be computed by entering the x-coordinate in X, and depressing "INT."

TABLE II. Summary of Statistical Functions

KEY	REGISTERS	STATISTICAL EQUATION
"Σx"	$X \rightarrow Y$ $X + c \rightarrow C$, where c = original value of C $X^2 + t \rightarrow T$, where t = original value of T $n + 1 \rightarrow N$, where n = original value of N	Σx Σx^2 Increments n
"Σy"	$X + a \rightarrow A$, where a = original value of A $X^2 + m \rightarrow M$, where m = original value of M $(X \cdot Y) + s \rightarrow S$, where s = original value of S	Σy Σy^2 $\Sigma x \cdot y$
"REM x"	$c - X \rightarrow C$ $t - X^2 \rightarrow T$ $n - 1 \rightarrow N$	Delate X_n Delete $x_n{}^2$ Decrement n
"REM y"	$a - X \rightarrow A$ $m - X^2 \rightarrow M$ $s - (X \cdot Y) \rightarrow S$	Delete y_n Delete $y_n{}^2$ Delete $(x \cdot y)_n$
"$\bar{X}$, SD"	$\frac{C}{N} \rightarrow X$ $\sqrt{\frac{T - \frac{C^2}{N}}{N-1}} \rightarrow M$	$\bar{X} = \frac{\Sigma x}{n}$ $SD = \sqrt{\frac{\Sigma x^2 - \frac{(\Sigma x)^2}{n}}{n-1}}$
"COR-SLOPE"	$\frac{S - \frac{C \cdot A}{N}}{\sqrt{\left(T - \frac{C^2}{N}\right)\left(M - \frac{A^2}{N}\right)}} \rightarrow X, S$ $\frac{S - \frac{C \cdot A}{N}}{T - \frac{C^2}{N}} \rightarrow M$ $\frac{A - M \cdot C}{N} \rightarrow A$	$r = \frac{\Sigma x \cdot y - \frac{\Sigma x \cdot \Sigma y}{n}}{\sqrt{\left(\Sigma x^2 - \frac{(\Sigma x)^2}{n}\right)\left(\Sigma y^2 - \frac{(\Sigma y)^2}{n}\right)}}$ $m = \frac{\Sigma x \cdot y - \frac{\Sigma x \cdot \Sigma y}{n}}{\Sigma x^2 - \frac{(\Sigma x)^2}{n}}$ $b = \frac{\Sigma y - m \cdot \Sigma x}{n}$
"INT"	$M \cdot X + A \rightarrow X$	$y_{INT} = mx + b$

EXAMPLES

1. Addition or subtraction

2.0
3.2
−12.3

KEYS	DISPLAY	COMMENTS
2	2	
+	2.	
3	3	
.	3.	
2	3.2	
+	5.2	
1	1	
2	1 2	
.	1 2.	
3	1 2.3	
−	−7.1	
C	0.	

2. Repeat add or subtract

KEYS	DISPLAY	COMMENTS
3	3	
.	3.	
1	3.1	
+	3.1	
+	6.2	
+	9.3	
−	6.2	
C	0.	

3. Chain multiplication or division

	KEYS	DISPLAY	COMMENTS
a)	1	1	
	x	1.	
	2	2	
	x	2.	
	3	3	
	.	3.	
	1	3.1	
	x	6.2	
	4	4	
	.	4.	
	2	4.2	
	=	2 6.0 4	
b)	1	1	
	0	1 0	
	÷	1 0.	
	2	2	
	÷	5.	
	1	1	
	0	1 0	
	÷	.5	
	2	2	
	=	.2 5	

EXAMPLES (Continued)

3. (Continued)

	KEYS	DISPLAY	COMMENTS
c)	2	2	
	0	2 0	
	x	2 0.	
	4	4	
	÷	8 0.	
	8	8	
	÷	1 0.	
	7	7	
	x	1.4 2 8 5 7 1 4	
	4	4	
	=	5.7 1	Result rounded to two places

4. Constant multiplication or division

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	x	3.	
	2	2	
	=	6.	
	4	4	
	=	1 2.	First factor in constant multiply
	5	5	
	.	5.	
	2	5.2	
	=	1 5.6	
	=	4 6.8	
b)	5	5	
	÷	5.	
	2	2	
	=	2.5	
	4	4	
	=	2.	Second factor in constant divide
	5	5	
	.	5.	
	2	5.2	
	=	2.6	
	=	1.3	

5. To perform products of sum; e.g.,

$(5 + 4) \times (3 + 2)/(6 + 7) =$

KEYS	DISPLAY	COMMENTS
5	5	
+	5.	
4	4	
+	9.	
x	9.	
3	3	
+	3.	
2	2	
+	5.	
÷	4 5.	(5 + 4) x (3 + 2) is executed
6	6	
+	6.	
7	7	
+	1 3.	
=	3.4 6	45 ÷ (6 + 7) is executed and rounded to two places

6. Calculate percentage
5% of 300.25

KEYS	DISPLAY	COMMENTS
3	3	
0	3 0	
0	3 0 0	
.	3 0 0.	
2	3 0 0.2	
5	3 0 0.2 5	
x	3 0 0.2 5	
5	5	
%	1 5.0 1	"Live %" key executes operation and rounds two places

7. Perform add-on and discount

	KEYS	DISPLAY	COMMENTS
a) Add-On, 125 + 5%			
	1	1	
	2	1 2	
	5	1 2 5.	
	x	1 2 5.	
	5	5	
	%	6.2 5	5% of 125 is displayed
	+	1 3 1.2 5	125 + 5% is displayed
b) Discount, 532.1 − 6%			
	5	5	
	3	5 3	
	2	5 3 2	
	.	5 3 2.	
	1	5 3 2.1	
	x	5 3 2.1	
	6	6	
	%	3 1.9 3	6% of 532.1 is displayed
	−	5 0 0.1 7	532.1 − 6% is displayed

8. Perform change sign

KEYS	DISPLAY	COMMENTS
1	1	
2	1 2	
CS	−1 2	Change sign does not terminate entry.
3	−1 2 3	
.	−1 2 3.	
CS	1 2 3.	
5	1 2 3.5	
CS	−1 2 3.5	
6	−1 2 3.5 6	
C	0.	

9. Accumulate in memory, recall and clear memory

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	M+	3.	Accumulate in memory
	4	4	
	M+	4.	Accumulate in memory
	5	5	
	MR	7.	Recall memory
	MR	7.	Recall and clear memory
	MR	0.	Recall and clear memory
b)	5	5	
	+	5.	
	6	6	
	+	1 1.	
	M+	1 1.	Accumulate in memory
	7	7	
	+	1 8.	
	M+	1 8.	Accumulate in memory
	+	2 5.	Repeat add
	3	3	
	2	3 2	
	.	3 2.	
	2	3 2.2	
	CS	−3 2.2	
	M+	−3 2.2	
	9	9	
	+	3 4.	
	MR	−3.2	Accumulated value of M is recalled
	+	3 0.8	
	MR	−3.2	Accumulated value of M is recalled
	MR	−3.2	M is cleared
	MR	0.	

EXAMPLES (Continued)

10. Accumulate in memory with the "= +" key

KEYS	DISPLAY	COMMENTS
5	5	
x	5.	
3	3	
= +	1 5.	5 x 3 = 15 is added to M
4	4	
.	4.	
2	4.2	
x	4.2	
3	3	
= +	1 2.6	4.2 x 3 = 12.6 is added to M
6	6	
÷	6.	
7	7	Rounded to 2 decimal places
= +	.8 6	and added to M
9	9	
CS	−9	Note method of multiplying
x	−9.	negative number
4	4	
= +	−3 6.	−9 x 4 = −36 is added to M
MR	−7.5 4	

STATISTICAL FUNCTIONAL EXAMPLES

1. Perform mean and standard deviation

a) Data: 4.0, 5.1, 4.5

KEYS	DISPLAY	COMMENTS
CA	0.	
4	4	
Σx	1.	Display indicates first data point has been entered
5.1	5.1	
Σx	2.	2nd data point entered
4.5	4.5	
Σx	3.	3rd data point entered
$\overline{X}$, SD	4.5 3 3 3 3 3 3	Mean and standard deviation are computed; mean is displayed
MR	.5 5 0 7 5 7 6 5	Standard deviation is recalled from M

b) Data: 3, 3, 3, 3, 4.1, 3.6

KEYS	DISPLAY	COMMENTS
CA	0.	Always use "CA" after mean
3	3	and SD calculation
Σx	1.	
4	4	
FREQ x	4.	Grouped data points may
4.1	4.1	be entered conveniently
Σx	5.	using the "FREQ" key
3.9	3.9	
Σx	6.	Wrong data entry
3.9	3.9	
REM x	5.	Wrong data is removed. Five
3.6	3.6	data points are entered.
Σx	6.	
$\overline{X}$, SD	3.2 8 3 3 3 3 3	Mean and standard deviation are computed: $\overline{X}$ is displayed
MR	.4 6 6 5 4 7 7 4	Standard deviation is recalled from M

c) Correction of group data entered with "FREQ"
Data: 4, 4, 4, 5, 5, 5, 5

KEYS	DISPLAY	COMMENTS
CA	0.	
4	4	
Σx	1.	
3	3	
FREQ x	3.	
5	5	
Σx	4.	
7	7	
FREQ x	10.	7 is incorrectly entered
5	5	
REM x	9.	
7	7	
CS	−7	
FREQ x	3.	Negative x sets "REMOVE x" function
5	5	
Σx	4.	
4	4	
FREQ x	7.	Corrected data has been entered
$\overline{X}$, SD	4.5 7 1 4 2 8 5	
MR	.5 3 4 5 2 3 1 5	

d) Compute running mean and standard deviations
Data: 7, 8, 6, 7, 5

KEYS	DISPLAY	COMMENTS
CA	0.	
7	7	
Σx	1.	
8	8	
Σx	2.	n = 2
$\overline{X}$, SD	7.5	Mean of first two data entries
MR	.7 0 7 1 0 6 7 8	Standard deviation of first two data entries
6	6	
Σx	3.	n = 3
$\overline{X}$, SD	7.	Mean of first three entries
MR	1.	Standard deviation of first three entires
7	7	
Σx	4.	n = 4
$\overline{X}$, SD	7.	Mean of first four entries
MR	.8 1 6 4 9 6 5 7	Standard deviation of first four entries
5	5	
Σx	5.	
$\overline{X}$, SD	6.6	Mean of all five entires
MR	1.1 4 0 1 7 5 4	Standard deviation of all five entires

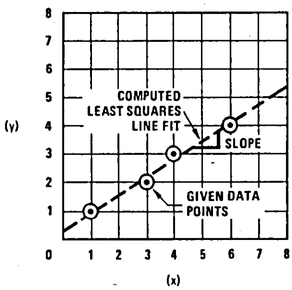
2. To perform least squares line fit on given data (See plotted data on page 10)

a) Data: 1, 1
3, 2
4, 3
6, 4

KEYS	DISPLAY	COMMENTS
CA	0.	
1	1	
Σx	1.	n = 1
1	1	
Σy	1.	
3	3	
Σx	2.	n = 2
2	2	
Σy	2.	
4	4	
Σx	3.	n = 3
3	3	
Σy	3.	
6	6	
Σx	4.	
4	4	
Σy	4.	
COR-SLOPE	.9 9 2 2 7 7 8 8	Correlation coefficient is displayed (perfect correlation = 1.0)
MR	.6 1 5 3 8 4 6 1	Slope of least squares line fit is recalled from M
0	0	x = 0
INT	.3 4 6 1 5 4	y-intercept of least squares line at x = 0 is computed
8	8	x = 8
INT	5. 2 6 9 2 3 0 8	y-intercept of least squares line at x = 0 is computed

STATISTICAL FUNCTION EXAMPLES (Continued)

2. (Continued)



b) Data: 2, 5
1, 4
0, 3

KEYS	DISPLAY	COMMENTS
CA	0.	
2	2	
Σx	1.	$n_x = 1$
5	5	
Σy	1.	$n_y = 1$
8	8	Wrong data point is entered
Σx	2.	$n_x = 2$
9	9	
Σy	2.	$n_y = 2$
8	8.	Wrong data point is removed
REM x	1.	$n_x = 1$
9	9	
REM y	1.	$n_y = 1$
1	1	
Σx	2.	$n_x = 2$
4	4	
Σy	2.	$n_y = 2$
0	0	
Σx	3.	$n_x = 3$
3	3	
Σy	3.	$n_y = 3$
COR-SLOPE	1.	Correlation coefficient is displayed
MR	1.	Slope is displayed
3	3	For x = 3,
INT	6.	the y-intercept is 6

MM5764 conversion calculator

general description

The single-chip MM5764 Conversion Calculator was developed using a metal-gate, P-channel enhancement and depletion mode MOS/LSI technology with low end-product cost as a primary objective. A complete calculator as shown in *Figure 1* requires only the MM5764, a keyboard, DS8864 digit driver, NSA1298 LED display, 9V battery and appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and 7-segment output display encoding are included on-chip and require no external components. Segments can usually be driven directly from the MM5764, as it typically sources about 8.5 mA of peak current. [Note: The typical duty cycle of each digit is 0.104; average LED segment current is therefore approximately 0.104 (8.5 mA), or 0.9 mA average. Correspondingly the worse-case average segment current is 0.104 (5.0 mA), or 0.52 mA.] The ninth digit (left-most) is used for the negative sign, or the decimal point of a number less than unity.

An internal power-on clear circuit is included that clears all registers, including the memory, when V_{DD} and V_{SS} are initially applied to the chip.

Trailing zero suppresion allows convenient reading of the left justified display, and conserves power. The DS8864 digit driver is capable of sensing a low battery voltage and providing a signal during Digit 9 time that can be used to turn on one of the segments as an indicator. Typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff is included. If no key closure occurs for approximately 25 seconds, all numbers are blanked and all decimal points displayed.

The Ready output signal is used to indicate calculator status. It is useful in providing synchronization information for testing or applications where the MM5764 is used with other logic or integrated circuits; e.g., with the MM5765 Programmer *(Figure 3).*

Thirty-two keys are arranged in a four-by-nine matrix as shown in Table I. There is an automatic constant feature.

The user has access to five registers designated X, T, A, K and M. The X-register is used for keyboard entry and display. The T and A-registers are used in multiply/divide and add/subtract calculations, respectively. M is an accumulating storage memory. The K-register is used to store a user defined conversion constant.

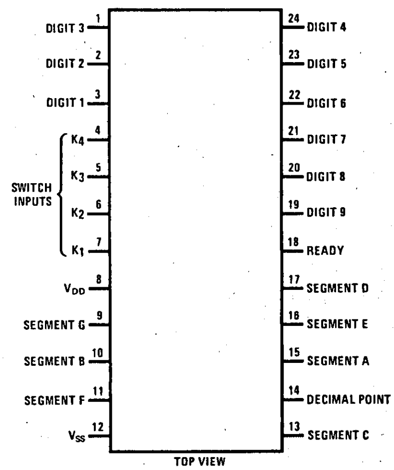
Data is entered into the calculator in floating point business notation. All entries and results are displayed left justified with insignificant zeros to the right of the decimal point suppressed. All intermediate results of a chain calculation are floating point. Terminating keys "=," "%," and "= +" round the displayed result to two decimal places.

features

- Full 8-digit entry and display calculator
- Arithmetic functions: +, −, x, ÷, =, %, 1/x
- Percent mark-up and discount
- Twenty automatic conversions
- A user definable conversion key
- Change sign and "π" keys
- Accumulating memory: MR, M+, =+, MC
- Square root
- Auto constant
- Business notation
  - +, − "adding machine" notation
  - x, ÷, = algebraic notation
- Automatic power-on clear
- Automatic display cutoff
- Direct 9V battery compatibility; low power

connection diagram

Dual-In-Line Package



Order Number MM5764N
See Package 22

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}. (All other pins connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12.0
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

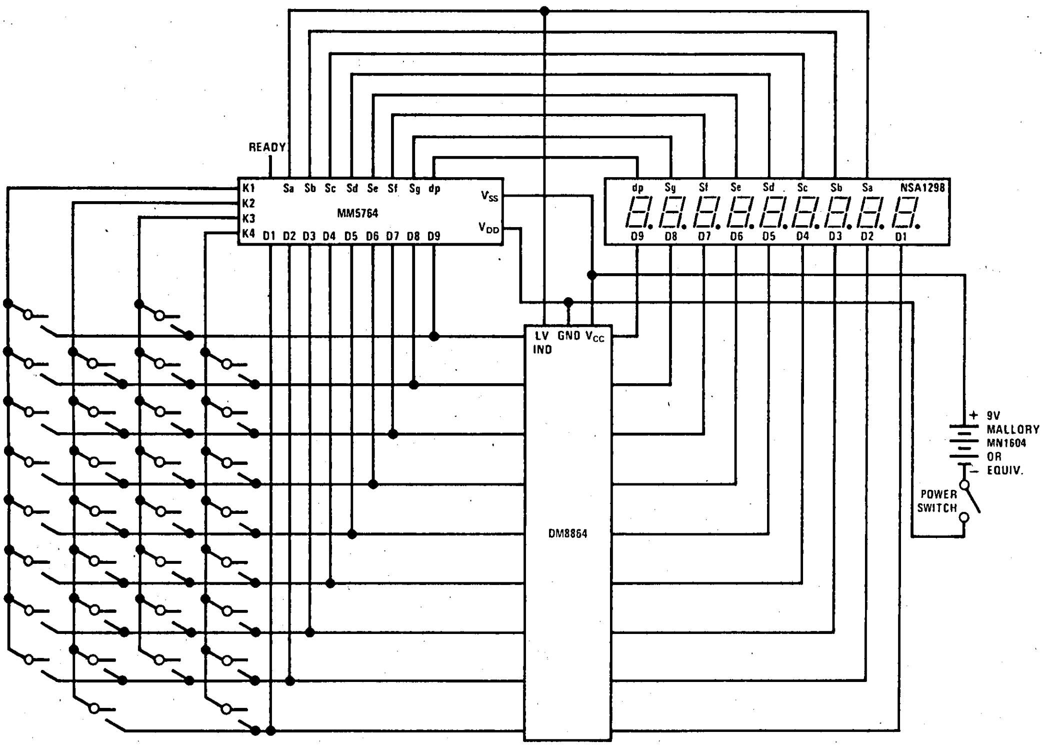
V_{SS} always defined as most positive supply voltage.

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}-9.5V$, $T_A = 25°C$			16.0	mA
Keyboard Scan Input Levels (K1, K2, K3 and K4)					
Logical High Level	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	$V_{SS}-2.5$			V
Logical Low Level	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-6.0$	V
Digit Output Levels					
Logical High Level (V_{OH})	R_{LOAD} = 3.2 kΩ to V_{DD}				
	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	$V_{SS}-1.5$			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-6.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-7.0$	V
Segment Output Current (Sa through Sg and Decimal Point)	$T_A = 25°C$				
	$V_{OUT} = V_{SS}-3.6V$, $V_{DD} = V_{SS}-6.5V$	−5.0	−8.5		mA
	$V_{OUT} = V_{SS}-5V$, $V_{DD} = V_{SS}-8V$		−10.0		mA
	$V_{OUT} = V_{SS}-6.5V$, $V_{DD} = V_{SS}-9.5V$			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	I_{OUT} = −0.4 mA	$V_{SS}-1.0$			V
Logical Low Level (V_{OL})	I_{OUT} = 10μA			$V_{DD}+1.0$	V

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time (*Figure 2*)		0.32	0.8	2.0	ms
Digit Time (*Figure 2*)		36	89	222	μs
Segment Blanking Time (*Figure 2*)		2	5.5	14	μs
Digit Output Transition Times (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF, R_{LOAD} = 9.6 kΩ		2		μs
Keyboard Inputs High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		μs
Ready Output Propagation Time (*Figure 3*)					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	10		50	μs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF			1	ms
Key Input Time-out					
Key Entry		2.8	7.2	18	ms
Key Release		5.1	12.8	32	ms
Display Cutoff Time (The time after the last valid key closure that all numbers will be blanked and all decimal points displayed.)		10	25	63	sec



Note: See Table II for Key Matrix Designations.

FIGURE 1. Complete Calculator Schematic

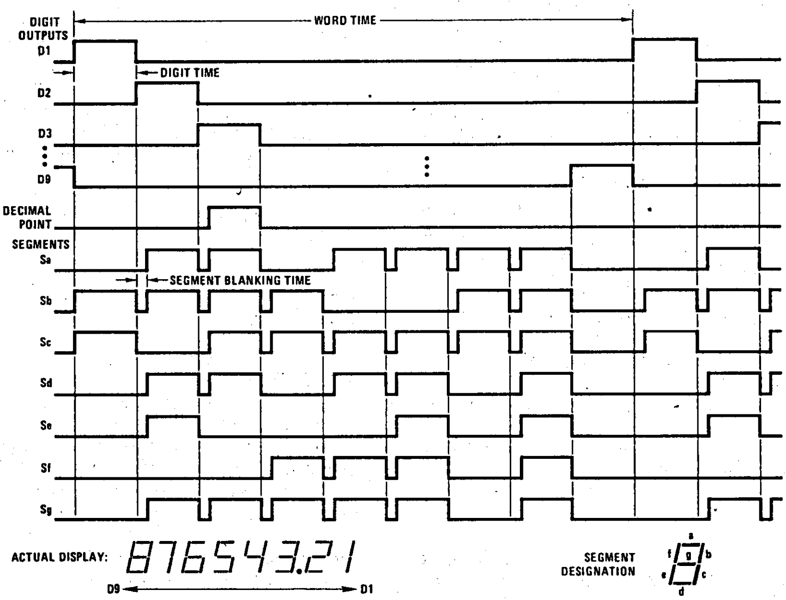


FIGURE 2. Display Timing Diagram

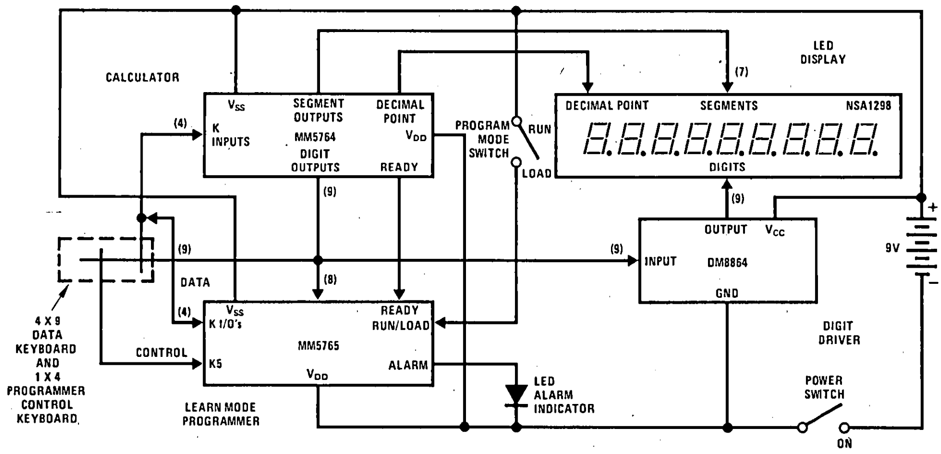


FIGURE 3. Low Cost Handheld Programmable Calculator Using the MM5764 Calculator and MM5765 Programmer.

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5764 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3 or K4 are forced more positive than the Logical High Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after nine word times if the key input is still at a Logical High Level. As long as the key is held down (and the key input remains high) no further entry is allowed. When the key input changes to a Logical Low Level, the internal counter starts a sixteen word time-out for key release. During both entry and release time-outs the key inputs are sampled approximately every other word time for valid levels. If they are found invalid, the counter is reset and the calculator assumes the last valid key input state.

One of the popular types of low-cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5764 defines a series contact resistance up to 50 kΩ as a valid key closure, assuring a reliable interface for that type of keyboard.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately twenty-five seconds, an internal automatic display cutoff circuit will blank all segments and display nine decimal points. Any key depression will restore the display; to restore the display without modifying the status of the calculator, use two Change Sign key depressions.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 4 and 5*. It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

ERROR INDICATION

In the event of an operating error, the MM5764 will display all zeros and all decimal points. The error indication occurs if division by zero is attempted or either a result or intermediate value exceeds 99999999.

The indication is cleared by depressing any key.

If an error results from a "+" or "−" key, the X-register is cleared and the last entry is saved in the A-register; no other registers are affected. An error condition during "x" or "÷" operations clears X without changing any of the other registers.

Overflow as a result of "M+" saves the value stored in M, clears X and displays the error indication. Calculations are immediately stopped and other registers are not cleared.

Overflow as a result of a conversion clears X and saves all other registers.

AUTOMATIC CONSTANT

The MM5764 retains as a constant the first factor of a multiplication calculation or the second factor of a division calculation, when that calculation is terminated by "=" key, "%" key or "= +" key. Subsequent calculations using the stored constant are made by entering a number and operating upon it with the appropriate terminator ("=," "%" or "= +" key). The T-register is used to store the constant in the constant mode of operation.

The calculator automatically changes to the chain mode when a "x" or "÷" key occurs in the calculation. In the chain mode, the result of each "x" or "÷" key is stored in both X and T-registers. A new entry replaces X without altering T. At the completion of a chain

TABLE I. Mode Summary

MODE	KEYS THAT SET MODE	DESCRIPTION (See Calculation Examples)
CONSTANT MULTIPLY	"CLEAR" "=" "=+" "%"	Depression of an "=," "= +" or "%" key will multiply the X-register by the T-register and replace X with the product. T remains unchanged.
CHAIN MULTIPLY	"x," following a terminator, or "÷" or "x" operation	Depression of an "=," "= +" or "%" key will multiply the X-register by the T-register and place the product in X. T remains unchanged.
CONSTANT DIVIDE	"=" "= +" "%" } With calculator previously in chain divide mode.	Depression of an "=," "= +" or "%" key will divide the X-register by the T-register and replace X with the quotient. T is unchanged.
CHAIN DIVIDE	"÷," following a terminator or "÷" or "x" operation	Depression of an "=," "= +" or "%" key will divide the T-register by the X-register, transfer X to T, and place the quotient in X.

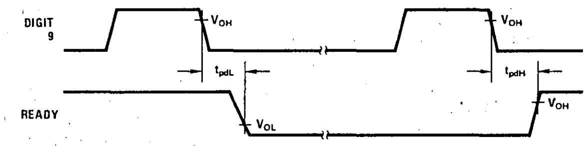


FIGURE 4. Ready Timing

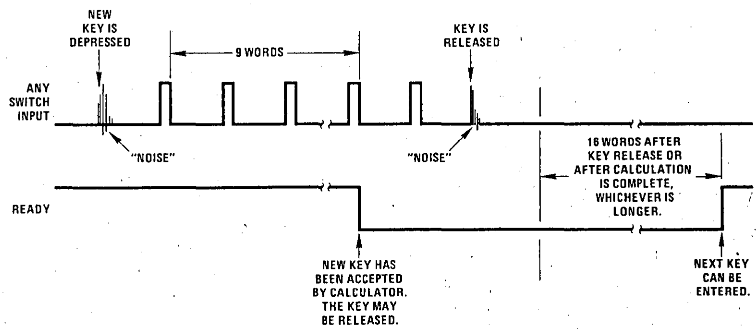


FIGURE 5. Functional Description of Ready Signal and Key Entry.

calculation, the T-register will contain the value used as first factor of the last multiply, or the latest entry if the last operation was a divide.

Table I summarizes the four modes.

KEY OPERATIONS

(Note: X-register is always displayed.)

Clear Key, "C"

Following a number key, it clears only the X-register (clear entry); after any other key, it clears registers X, A and T.

Number Entries

The first entry clears the X-register and enters the number as the LSD of X. Second through eighth entries (excluding a decimal point) are entered one digit to the right of the previous number. The ninth, and subsequent entries, are ignored. First entry after a "+," "−," or "M+" following a "+" or "−" key transfers the existing number in the X-register to the A-register before clearing and placing the new entry in X.

Conversion Functions

With the exception of the six single function conversion keys, all conversions are preceded by either the shift key, "→," or the reverse conversion key, "←." Depression of the appropriate conversion key replaces the value in the X-register with a converted result, as summarized in Table II. The six single function keys (inches → mm," "inches → cm," "ft → inches," "ft → m," "yds → m" and "miles → km") do not need to be preceded by the shift key, "→," for forward conversions. Only the X-register is affected by a conversion operation.

Constant Store Key, "KS"

The value of X is copied into the K-register. Following a forward conversion key, "→," X is multiplied by K and the product stored in X; following a "←" key, X is divided by K, and the quotient is stored in X.

Decimal Point, "."

As the first depression of a number entry, it clears the X-register and places a point in the leftmost digit. If the previous key was a number, it enters a decimal point to the right of the last number entered. Following a "+," "−," or those keys preceding a "M+" key, the X-register is transferred to A, cleared and a decimal point entered in the leftmost digit. The last decimal point depression in a single number entry is accepted as the valid point.

Change Sign Key, "CS"

Changes sign of register X.

Addition Key, "+"

If the previous key was not a "+" or "−" key, the number in the A-register is added to the X-register, X is transferred to A, and the sum is stored in X. When the last key was a "+" or "−" key, the number in A is added to the number in X without destroying the value of A. The sum is stored in X.

Subtraction Key, "−"

If the previous key was not a "+" or "−" key, the number in the X-register is subtracted from the number in the A-register, X is transferred to A, and the difference is stored in X. When the last key was a "+" or "−" key, the number in A is subtracted from X without destroying the value of A. The result is stored in X.

Multiplication Key, "x"

If there has not been an "x" or "÷" key since the last terminator key ("=," "= +" or "%"), the value of the X-register is copied into the T-register and the calculator is set to the chain multiply mode. In a chain calculation in which there has been a "x" key since the last terminator or "÷" key, X is multiplied by T and the resulting product is stored in both X and T; if a "÷" key has occured since the last terminator or "x" key, depression of "x" will divide the T-register by the X-register, with the quotient stored in both X and T.

Division Key, "÷"

If there has not been an "x" or "÷" key since the last terminator key ("=," "= +" or "%"), the value of the X-register is copied into the T-register and the calculator is set to the chain divide mode. In a chain calculation if a "x" key has occured since the last terminator or "÷" key, X is multiplied by T and the product is stored in both X and T; if a "÷" key has occured since the last terminator or "x" key, depression of "÷" will divide the T-register by the X-register, with the quotient stored in both X and T.

Equal Key, "="

In the chain multiply mode, the value in the X-register is multiplied by the T-register with the product stored in X. Register T remains unchanged. In the chain divide mode, depression of "=" will divide T by X, transfer X to T, and place the quotient in X. If the calculator is in constant multiply, "=" will multiply X by T, place the product in X and retain T. For constant divide, the X-register is divided by T, the quotient is stored in X; T is unchanged.

The "=" key always rounds the answer stored in X to two places to the right of the decimal point, and clears register A.

Per Cent Key, "%"

This key acts exactly like the "=" key except the value of X is divided by 100 and copied in register A before performing the required operation. The result stored in X is rounded to two decimal positions.

Memory Plus Key, "M+"

The number in the X-register is accumulated in the M-register. Registers X and A are not changed, so the repeat addition or subtraction conditions that existed before accumulation to memory remain valid.

Memory Recall Key, "MR"

The value of register M is copied into the X-register. If the preceding key was a "+," "−" or "M+" followed by "+" or "−," the value of X is transferred to the A-register before M is copied into it.

Memory Clear Key, "MC"

The M-register is cleared, without affecting any other registers.

Reciprocal Function, "1/x"

If the number entry key "1" is preceded by either the forward or reverse conversion shift keys, "→" or "←," a non-zero value of X is replaced by its reciprocal. Registers A, T, K and M are not altered.

Square Root Function, "$\sqrt{x}$"

If the number entry key "2" is preceded by either the forward or reverse conversion shift keys, "→" or "←," the absolute value of X is replaced by its square root. Registers A, T, K and M are unaltered.

Pi-function, "π"

If the decimal point entry key is preceded by either the forward or reverse conversion shift keys, "→" or "←," the value of X is replaced by the constant 3.1415927.

Equal Plus Key "=+"

This key acts exactly like the "=" key followed by a "M+" key. The multiply or divide is executed the result is rounded to two places then the rounded result is added to the Memory.

TABLE II. Summary of Key Functions

KEY MATRIX DESIGNATION	PRIMARY KEY FUNCTION	IF PRECEDED BY "→" SHIFT KEY	IF PRECEDED BY "←" SHIFT KEY
K1–D1	N/C	–	–
K1–D2	Minus, "–"	"–"	"–"
K1–D3	Plus, "+"	"+"	"+"
K1–D4	Divide, "÷"	"÷"	"÷"
K1–D5	Multiply, "x"	"x"	"x"
K1–D6	Constant Store, "KS" Constant Conversion	$X_o \cdot K \to X$	$X_o \div K \to X$
K1–D7	Ft → in	$X_o \cdot (12) \to X$	$X_o \div (12) \to X$
K1–D8	In → mm	$X_o \cdot (25.4) \to X$	$X_o \div (25.4) \to X$
K1–D9	In → cm	$X_o \cdot (2.54) \to X$	$X_o \div (2.54) \to X$
K2–D1	Mile → km	$X_o \cdot (1.609344) \to X$	$X_o \div (1.609344) \to X$
K2–D2	Ft → m	$X_o \cdot (0.3048) \to X$	$X_o \div (0.3048) \to X$
K2–D3	Forward Shift, "→"	"→"	"→"
K2–D4	Memory Clear, "MC"	"MC"	"MC"
K2–D5	Yard → m	$X_o \cdot (0.9144) \to X$	$X_o \div (0.9144) \to X$
K2–D6	Memory Plus, "M+" MPH → knots	$X_o \cdot (0.86836) \to X$	$X_o \div (0.86836) \to X$
K2–D7	Memory Recall, "MR" Imp. Gal. → U.S. Gal.	$X_o \cdot (1.20094) \to X$	$X_o \div (1.20094) \to X$
K2–D8	Clear, "C"	"C"	"C"
K2–D9	N/C	–	–
K3–D1	N/C	–	–
K3–D2	Equal, "=" Acres → Hectares	$X_o \cdot (0.404687) \to X$	$X_o \div (0.404687) \to X$
K3–D3	Equal Plus, "=+" Cubic Ft → gal	$X_o \cdot (7.4805) \to X$	$X_o \div (7.4805) \to X$
K3–D4	Change Sign, "CS" Atmospheres → PSI	$X_o \cdot (14.696) \to X$	$X_o \div (14.696) \to X$
K3–D5	Decimal Point, "." π	$3.1415927 \to X$	$3.1415927 \to X$
K3–D6	"9" Oz → cc	$X_o \cdot (29.5737) \to X$	$X_o \div (29.5737) \to X$
K3–D7	"8" Quarts → liters	$X_o \cdot (0.946333) \to X$	$X_o \div (0.946333) \to X$
K3–D8	"7" Gal → liters	$X_o \cdot (3.785332) \to X$	$X_o \div (3.785332) \to X$
K3–D9	"6" Lb → oz	$X_o \cdot (16) \to X$	$X_o \div (16) \to X$
K4–D1	"5" Oz → grams	$X_o \cdot (28.3495) \to X$	$X_o \div (28.3495) \to X$
K4–D2	"4" Lb → kilogram	$X_o \cdot (0.453592) \to X$	$X_o \div (0.453592) \to X$
K4–D3	"3" Stone → lb	$X_o \cdot (14) \to X$	$X_o \div (14) \to X$
K4–D4	"2" Square Root, "$\sqrt{X}$"	$\sqrt{X_o} \to X$	$\sqrt{X_o} \to X$
K4–D5	"1" Reciprocal, "1/X"	$1/X_o \to X$	$1/X_o \to X$
K4–D6	"0" °F → °C	$X_o \cdot (9/5) + 32 \to X$	$(X_o - 32) \cdot 5/9 \to X$
K4–D7	Reverse Shift, "←"	"←"	"←"
K4–D8	Percent, "%" Acre → Sq. ft	$X_o \cdot (43560) \to X$	$X_o \div (43560) \to X$

EXAMPLES

1. Addition and subtraction of a column of numbers:

$$\begin{array}{r} 2.0 \\ 3.2 \\ \underline{-12.3} \end{array}$$

KEYS	DISPLAY	COMMENTS
2	2	
+	2.	2 is entered
3	3	
.	3.	
2	3.2	
+	5.2	2 + 3.2 is displayed
1	1	
2	1 2	
.	1 2.	
3	1 2.3	
–	−7.1	12.3 is subtracted from
C	0.	(2 + 3.2)

2. Repeat add or subtract

KEYS	DISPLAY	COMMENTS
3	3	
.	3.	
1	3.1	
+	3.1	3.1 is entered
+	6.2	3.1 + 3.1 computed
+	9.3	3.1 + 3.1 + 3.1 computed
–	6.2	9.3 – 3.1 computed
C	0.	

3. Chain multiplication or division

KEYS	DISPLAY	COMMENTS
a) Multiplication		
1	1	
x	1.	
2	2	
x	2.	1 x 2 is computed
3.1	3.1	
x	6.2	2 x 3.1 is computed
4.2	4.2	
=	26.0 4	6.2 x 4.2 is computed
b) Division		
10	10	
÷	10.	
2	2	
÷	5.	10 ÷ 2 is computed
10	10	
÷	.5	5 ÷ 10 is computed
2	2	
=	.2 5	0.5 ÷ 2 is computed
c) Mixed multiplication and division		
20	20	
x	20.	
4	4	
÷	80.	
8	8	
÷	10.	
7	7	
x	1.4 2 8 5 7 1 4	
4	4	
=	5.7 1	Result rounded to two places

4. Constant multiplication or division

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	x	3.	
	2	2	
	=	6.	
	4	4	
	=	1 2.	First factor in constant multiply
	5	5	
	.	5.	
	2	5.2	
	=	1 5.6	
	=	4 6.8	
b)	5	5	
	÷	5.	
	2	2	
	=	2.5	
	4	4	
	=	2.	Second factor in constant divide
	5	5	
	.	5.	
	2	5.2	
	=	2.6	
	=	1.3	

5. To perform products of sums

(5 + 4) x (3 + 2)/(6 + 7) =

KEYS	DISPLAY	COMMENTS
5	5	
+	5.	
4	4	
+	9.	
x	9.	
3	3	
+	3.	
2	2	
+	5.	
÷	4 5.	(5 + 4) x (3 + 2) is executed
6	6	
+	6.	
7	7	
+	1 3.	
=	3.4 6	45 ÷ (6 + 7) is executed and rounded to two places

6. Calculate percentage

KEYS	DISPLAY	COMMENTS
3	3	
0	3 0	
0	3 0 0	
.	3 0 0.	
2	3 0 0.2	
5	3 0 0.2 5	
x	3 0 0.2 5	
5	5	
%	1 5.0 1	"Live %" key; rounded two places

7. Perform add-on and discount

KEYS	DISPLAY	COMMENTS
a) Add-On		
1	1	
2	1 2	
5	1 2 5.	
x	1 2 5.	
5	5	
%	6.2 5	5% of 125 is displayed
+	1 3 1.2 5	125 + 5% is displayed

EXAMPLES (Continued)

7. (Continued)

KEYS	DISPLAY	COMMENTS
b) Discount		
5	5	
3	5 3	
2	5 3 2	
.	5 3 2.	
1	5 3 2.1	
x	5 3 2.1	
6	6	
%	3 1.9 3	6% of 532.1 is displayed
−	5 0 0.1 7	532.1 − 6% is displayed

8. Perform change sign

KEYS	DISPLAY	COMMENTS
1	1	
2	1 2	
CS	−1 2	Change sign does not terminate entry.
3	−1 2 3	
.	−1 2 3.	
CS	1 2 3.	
5	1 2 3.5	
CS	−1 2 3.5	
6	−1 2 3.5 6	

9. Accumulate in memory, recall and clear memory

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	M+	3.	Accumulate in memory
	4	4	
	M+	4.	Accumulate in memory
	5	5	
	MR	7.	Recall memory
	MC	7.	Clear memory
	MR	0.	
b)	5	5	
	+	5.	
	6	6	
	+	1 1.	
	M+	1 1.	Accumulate in memory
	7	7	
	+	1 8.	
	M+	1 8.	Accumulate 11 + 18 in memory
	+	2 5.	Repeat add
	3	3	
	2	3 2	
	.	3 2.	
	2	3 2.2	
	CS	−3 2.2	
	M+	−3 2.2	(11 + 18) − 32.2 is accumulated in memory
	9	9	
	+	3 4.	
	MR	−3.2	Accumulated value of M is recalled
	+	3 0.8	
	MR	−3.2	Accumulated value of M is recalled
	MC	−3.2	

10. Accumulate in memory with the "= +" key

KEYS	DISPLAY	COMMENTS
MC	0.	
C	0.	
5	5	
x	5.	
3	3	
= +	1 5.	5 x 3 = 15 is added to M
4	4	
.	4.	
2	4.2	
x	4.2	
3	3.	
= +	1 2.6	4.2 x 3 = 12.6 is added to M

10. (Continued)

KEYS	DISPLAY	COMMENTS
6	6	
÷	6.	
7	7	
= +	.8 6	Rounded to 2 decimal places
9	9	
CS	−9	Note method of multiplying negative number
x	−9.	
4	4	
= +	−3 6.	−9 x 4 = −36 is added to M
MR	−7.5 4	

11. Square root and reciprocal calculations. Find square root of 70064:

KEYS	DISPLAY	COMMENTS
70064	70064	
→	70064.	Either shift key could be used to set up $\sqrt{X}$ function
2 ($\sqrt{X}$)	264.6 9 6 0 5	Square root is computed
←		Either shift key could be used to set up 1/X function
1 (1/X)	.0 0 3 7 7 7 9 1	Reciprocal is computed

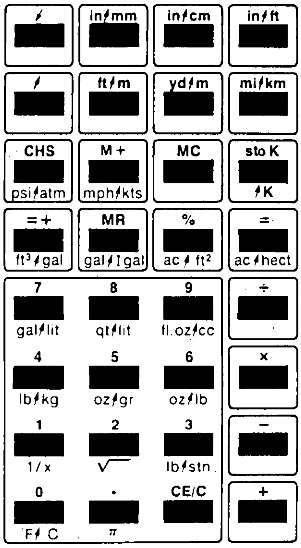
12. Use of constant π: $2\pi r = 2(\pi)$ (6.8)

KEYS	DISPLAY	COMMENTS
2	2	
x	2.	
→		Either shift key could be used to set up π
• (π)	3.1 4 1 5 9 2 7	
x	6.2 8 3 1 8 5 4	2π is computed
6.8	6.8	
=	42.7 3	

13. Use of conversion keys:

KEYS	DISPLAY	COMMENTS
2	2	
in → cm	5.08	Two inches is converted to cm
in → cm	12.9 0 3 2	Two square inches is converted to square cm
in → cm	32.7 7 4 1 2 8	Two cubic inches is converted to cubic cm
←	32.7 7 4 1 2 8	Reverse conversion mode is set
in → cm	12.9 0 3 2	
C	0.	
5	5	
→	5.	Data entry is terminated and forward conversion mode is set
7 (gal → liters)	18.9 2 6 6 6	Five gal. is converted to liters
→		
←		Last shift key is valid direction
8 (qts → liters)	20.	Liters → qts computed
12.5	12.5	
KS	12.5	Entry is stored in K
2	2	
→	2.	Forward shift sets up K conversion
KS	25.	Multiply by K
←		
KS	2.	Divide by K
C	0.	
77	77	77°F is entered
→	77.	
0 (°F → °C)	25.	77°F is converted to °C

keyboard outline



MM5765 calculator programmer

general description

The MM5765 provides a convenient and inexpensive means of adding "learn mode" programmability to many National Semiconductor calculator chips. It interfaces directly by simply adding a single static switch, four dynamic keys and a mean of displaying an alarm condition. The monolithic MOS integrated circuit combines P-channel enhancement and depletion mode technologies to obtain low voltage and low power characteristics necessary for economical battery-powered products.

The MM5765 is a dynamic key sequence programmer that memorizes any combination of key entries while in the Load Mode, then automatically plays back the programmed sequence as often as desired in the Run Mode. Up to 102 characters can be stored in multiprogram sequence blocks. Each block, or program, can be executed individually or the operator can make the decision to branch to specific programs, run each in series or perform intermediate calculations from the keyboard. When programming in the Load Mode, the Delete key provides a convenient editing feature and the Halt key programs variable data entry points where control is temporarily returned to the operator in the Run Mode. Start and Skip keys control operation in both modes.

Synchronization with the calculator chip is accomplished by monitoring its Digit Output and Ready signals. The digit signals give timing information while the Ready indicates status of the calculator and synchronizes the key entry interface between it and the MM5765.

Up to four switch inputs (K1, K2, K3 and K4) and up to twelve digit lines are connected in parallel with the calculator switch and digit terminals that scan the keyboard. Keys stored in the MM5765 that are entered by selecting K1 through K4 are encoded simply as matrix positions, i.e., a particular switch input at a specific digit time. Therefore it is the key matrix address that is stored and not the key function. (Con't on page 4)

features

- Many NSC calculator chips can be provided with programming capability with the addition of only one static switch and four dynamic keys.
- Any key sequence, including constants and date entry points, may be stored automatically in the Load Mode and executed in the Run Mode.
- 102 step storage capacity of up to 47 different keys arranged in a 12 x 4 matrix.
- Multiprogram capability
- Provision for editing in Load Mode using the Delete key
- Convenient verification of programs using a Step Mode feature
- Alarm for full storage condition—or if a deletion of the first step in a program is attempted
- Power-on clear
- Direct 9V battery compatibility

block and connection diagrams

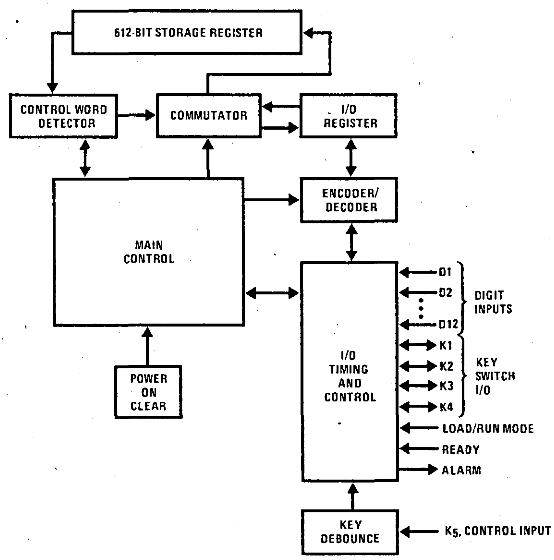
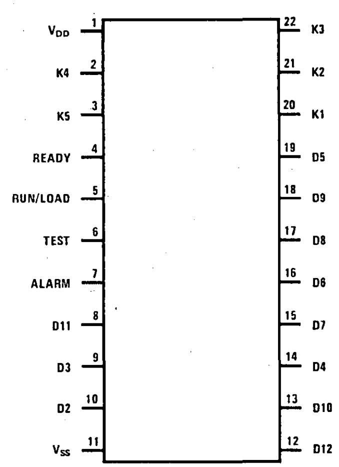


FIGURE 1

Dual-In-Line Package



TOP VIEW

Order Number MM5765N
See Package 21

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All other pins connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$

(V_{SS} is always the most positive supply)

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}-9.5V$, $T_A = 25°C$		8.0		mA
Keyboard Scan Input Levels (K1, K2, K3, K4, K5)					
Logical High Level (V_{IH})		$V_{SS}-2.5$			V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-6.0$	V
Digit Input Levels (D2 through D12)					
Logical High Level (V_{IH})		$V_{SS}-2.5$			V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-6.0$	V
Other Inputs (Ready, Run and Test)					
Logical High Level (V_{IH})		$V_{SS}-2.5$			V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-6.0$	V
Switch Buffer Output Levels (K1, K2, K3, K4)					
Logical High Level (V_{OH})		$V_{SS}-1.5$		V_{SS}	V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-6.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-7.0$	V
Alarm Output Current					
Source Current	$V_{OUT} = V_{SS}-4.5V$, $V_{DD} = V_{SS}-6.5V$	−5.0			mA
	$V_{OUT} = V_{SS}-5.2V$, $V_{DD} = V_{SS}-7.25V$		−8.0		mA
	$V_{OUT} = V_{SS}-7.8V$, $V_{DD} = V_{SS}-9.5V$			−20.0	mA

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digit Input Time (*Figure 3*)		70			µs
Word Time (*Figure 3*)		0.64			ms
Switch Input Time (*Figure 3*)		0.70			µs
Switch Output Time (*Figure 4*)		70			µs
Switch Propagation Delay Output (*Figure 4*)			15	26	µs
Switch Output Transition Time (*Figure 4*)	C_{LOAD} = 100 pF		2		µs
Switch Input K5 Key Bounce-out Stability Time (The time a keyboard input must be continuously higher than the minimum Logical High Level to be accepted as a key closure, or lower than the maximum Logical Low Level to be accepted as a key release, i.e., 6 or 7 cycles of D2.)		4.5		17.0	ms
Key Closure Rate (Time between consecutive key outputs in Run Mode.)			40		ms
Key Acceptance Rate (Time between consecutive key inputs in Load Mode.)				47	ms

8

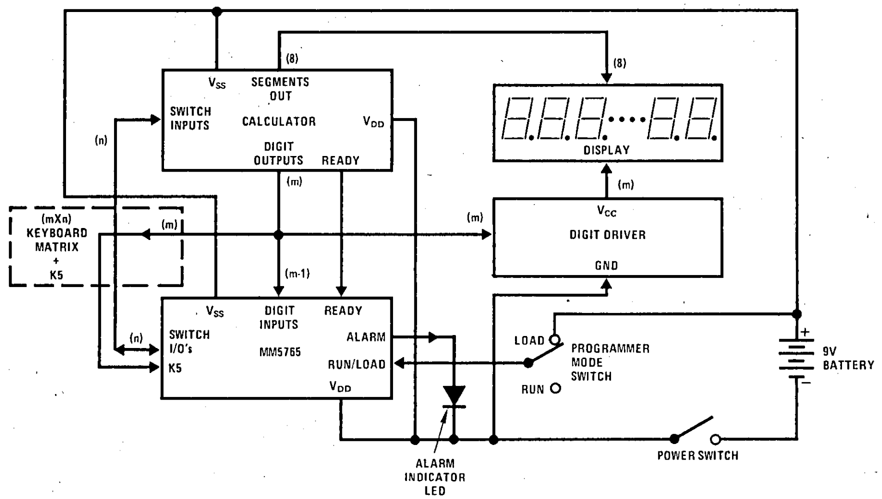


FIGURE 2. MM5765 Programmer Connected in Low-Cost Battery Operated Calculator System

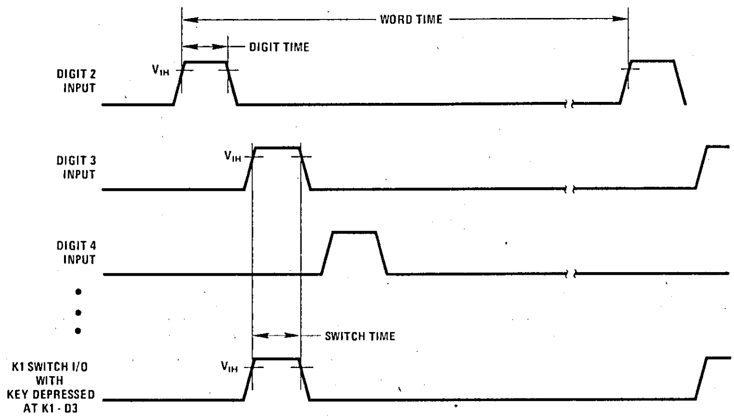


FIGURE 3. Input Timing

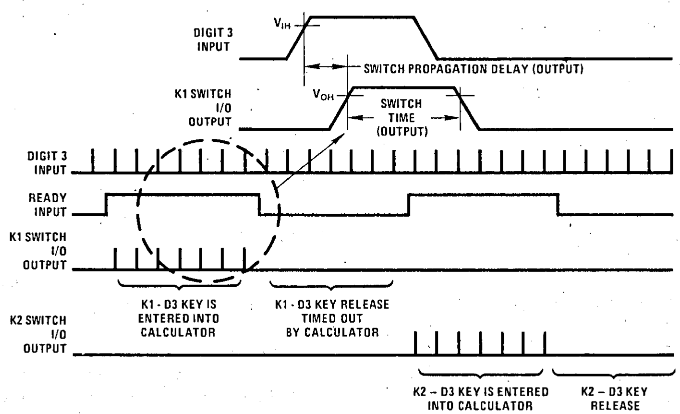


FIGURE 4. Programmer Output Timing

TABLE I. Action of Dynamic Control Keys as a Function of The LOAD/RUN Mode

KEY	LOAD	RUN
START	Clears and initializes program storage area.	Starts program when stopped in *HALT* mode. Starts first program.
SKIP	Terminates current program and initializes a new one.	Skip remainder of current program and begins execution of next one.
HALT	Programs an operator data entry or check point in *RUN MODE*.	
DELETE	Erases the last key entered. (Acts as a backspace key.)	

general description (con't)

Forty-seven different addresses can be stored using a 12x4 keyboard matrix. (The illegal address is Digit 1 and K4.) Switch Input K5 is used to enter programming control signals only and is not connected to the calculator in any way. The K5 input has key debounce protection identical to the calculator chip, which debounces K1 through K4. The MM5765 does not accept a K1, K2, K3 or K4 input until the Ready signal from the calculator goes from an idle, or high state, to a low state—indicating the key has been debounced by the calculator.

The program chip is dynamic, which means power must not be interrupted if a program is to remain stored. When power is applied an internal circuit automatically clears the MM5765, inhibiting false entries to the calculator and conditioning the system for entry of a new program.

Actual storage of the sequential key information is in a 612-bit shift register (see *Figure 1*). Each input character is encoded into a six-bit word and placed in the I/O register. If a Ready input confirms the character has been accepted by the calculator as a valid key entry, or the internal key debounce circuit in the case of Switch Input K5, the new key information is transferred by the commutator to the storage register. It is always placed in sequence at the end of the existing program, and an internal pointer is advanced six bits. The control word detector keeps track of the pointer and special codes required for control and alarm situations. In the Run Mode, characters are sequentially transferred into the I/O register, decoded on command of the Ready signal and entered into the calculator via the appropriate Switch Input Line.

When the MM5765 is used with calculators with long execution times, it may be useful to use a buffered Ready signal to drive a "Busy" indicator. This would give the user a visual feedback of status during Run operations.

PROGRAMMER CONTROL FUNCTIONS

"Load/Run" Mode Control

This control requires a single-pole, single throw static switch. It prepares the MM5765 for either accepting a key sequence or playing it back. Its position controls the function of the dynamic keys as shown in Table I.

Additional steps or programs can be appended to a stored key sequence even after execution simply by switching back to the Load Mode and entering the new steps. The storage register pointer always returns to the end of the previously entered key sequence when the mode is changed from Run to Load, and to the beginning of the first program when changed from Load to Run.

"Start" Key (Refer to Table II for keyboard connections)

The function of this dynamic key depends upon the position of the Load/Run Mode Control Switch:

1. With the Mode Switch in the Load position, Start clears the entire program storage register of all programs and initializes the device for accepting a new set of programs by setting the pointer at the first storage location.

2. With the Mode Switch in the Run position, Start begins execution of the first program, or if pausing in the Halt Mode, continues the program. This key is not seen by the calculator and therefore has no affect on the calculations in progress.

The Start key is timed out by the key bounce-out stability timer of the MM5765 on both key entry and release.

TABLE II. Control Signal Input, K5, Keyboard Matrix

CONTROL KEY FUNCTION	DIGIT TO K5 CONNECTION
START	D5 to K5
SKIP	D6 to K5
DELETE	D7 to K5
HALT	D8 to K5

"Skip" Key

This is the other dynamic key whose function depends on the position of the Load/Run Switch:

1. In the Load Mode, this key terminates the current program and marks the beginning of a new program. Repetitious depressions will be ignored. The Delete key will erase this key from the storage register, but the Alarm will be set indicating to the user that a

complete program has been deleted. A new Skip will reinitiate the deleted program; otherwise, subsequent deletions or additions will be to the previous program.

2. In the Run Mode, if the MM5765 is at a Halt, the Skip key will cause the remaining steps of the current program to be skipped. Execution automatically begins again at the start of the next program and continues to the first programmed Halt; in the absence of a Halt, execution will continue to the end of the program.

Depression of this key is not seen by the calculator and does not affect its status. The Skip key is timed out by the key bounce-out stability timer of the MM5765 on both key entry and key release.

"Halt" Key

The Halt key is a dynamic key that has a function only in the Load Mode. It is ignored in the Run Mode.

The Halt key is used to program a data entry pause in the playback of a key sequence. When a Halt occurs in the program sequence during operation in the Run Mode, the MM5765 ignores all key entries except Start or Skip. The calculator chip accepts all nonprogrammer keys in the normal manner so that constants or variables can be entered, or intermediate calculations can be performed. The operator may use the Halt as a decision making point where he has the option to continue the program in a number of ways based on an intermediate result; e.g., skip to another program, restart the present program, or even go to a co-routine in a second MM5765 program chip.

If the user switches to the Load Mode during a Halt, execution of the current program will be terminated and the MM5765 will be ready to store additional keys at the end of the last program. If the mode is then returned to Run, Start will begin execution at the beginning of the first program.

The Halt key is debounced by the MM5765.

"Delete" Key

The Delete is another dynamic control key that functions only in the Load Mode and is ignored in the Run Mode.

It provides a method of editing by erasing the end step of the program. It is essentially a "backspace" key. Multiple Deletes can be used to remove several steps or even complete programs, but the Alarm will be set if a Skip code is deleted or an attempt is made to delete the Start code (beginning of first program).

The Delete key is debounced by the MM5765.

Switch Input K5 Keyboard Bounce Protection

The MM5765 programmer chip is designed to interface with most low-cost keyboards and has characteristics identical to the standard NSC calculator keyboard bounce protection circuits.

A control key closure is sensed when Switch Input K5 is forced more positive than the Logical High Level specified in the Electrical Specifications. At the instant of closure, an internal "Key Bounce-out and Stability Time" counter is started. Any significant voltage perturbation occurring on the K5 input during timeout will reset the timer. Hence, a key is not accepted as valid until noise or ringing has died out and the stability time counter has timed-out. Noise that persists will inhibit key entry indefinitely. Release is timed in the same manner. The actual control operation is performed by the MM5765 after the release is validated, to differentiate the action from a calculator key.

ALARM CONDITIONS

An alarm condition will be indicated by the MM5765 program chip as a Logical High Level output on pin 7. An alarm condition can exist due to three circumstances:

1. All 102 storage locations in the storage register are full. The Alarm is reset by entering a Delete key or if the mode is changed to Run and any key is pressed. When the storage register is full, subsequent data keys are ignored; the existing program is not disturbed.

2. An attempt is made to delete a Start key code in the storage register during editing of a program. The alarm is set and the Delete key is ignored. Any of the calculator keys, the Skip or Halt keys or moving the Mode Switch to Run and pressing any key will reset the Alarm.

3. A Skip key code is deleted from the storage register while editing. The alarm is set and the Skip is deleted. Any calculator or programmer key, or switching to the Run Mode and pressing a key will reset the alarm condition. If a Skip key is not re-entered, new key entries will be appended to the previous program, and the original program being edited will no longer exist.

TABLE III. Ready Signal Description

CALCULATOR FUNCTION	READY SIGNAL
Idle	Ready is quiescently at a Logical High Level ($\sim V_{SS}$).
Key entry and functional operation	When a key is depressed, the calculator bounce-out stability timer is initiated. Ready remains high until the bounce-out time is completed and the key is entered, at which time it changes to a Logical Low Level ($\sim V_{DD}$).
Key release and return to idle	Ready remains low until key release is debounced and the calculator returns to the idle state. The low to high transition signals the return to idle.

TABLE IV. Mode and Alarm Truth Table

PIN	MODE	LEVEL
Load/Run Input	RUN	LOW
	LOAD	HIGH
Alarm Output	ACTIVE	HIGH
	INACTIVE	LOW

TYPICAL OPERATION

Loading a New Program

At power-on, the MM5765 automatically clears and initializes the storage register. All that is necessary to start programming is to switch to the Load Mode. If unwanted programs already exist in the storage register from previous operations, switching to the Load Mode and depressing Start will clear the memory and initialize a new program.

Programming is accomplished by simply keying the calculator in the normal manner. The MM5765 memorizes each key in the sequence entered. It is usually convenient to have the calculator displaying as the program is entered to catch entry errors and keep track of progress. However, it is necessary to consciously consider the anticipated results when programming to ensure a meaningful display at each step. For example, wherever variables are to be entered in the program, the Halt key is used rather than any numeric value. Because the calculator chip does not see a Halt, the display will no longer be correct as the remainder of the sequence is loaded. One convenient way around the problem is to depress and hold the Halt key down while a dummy variable is entered into the calculator. The depressed Halt key will lock-out the MM5765 without affecting the calculator. An alternate approach would be to enter the Halt and the dummy variable, followed by the proper number of Delete keys required to erase the dummy variable from the storage register. Either approach results in a valid calculator display and stored program during programming.

Because the primary reason for using a key sequence programmer is to allow convenient recall of often used routines or in optimizing a particular solution by iterating a function many times with a variety of input variables—in other words, many iterations of a common sequence—it is always worth the time to spend a few minutes planning the best way of entering the program. Learning what the calculator should be displaying at each step of the programming can be done conveniently by keying the program while in the Run Mode, using the proper dummy variables, and jotting down intermediate results. In this manner potential calculator overflow conditions are caught, and subsequent Load Mode entry errors can be easily detected. When an entry error is made while programming in the Load Mode, use the Delete key to erase as many steps as necessary, switch back to the Run Mode and depress Start to correct the calculator display and return to the Load Mode to finish. If the program does not approach the 102 key capacity of the MM5765, you may wish to simply use the calculator functions (such as Clear Entry) to correct the error situation even though they will be included in the stored program.

When the program is correctly loaded move the Mode Switch to Run. The program is now ready to be executed. Additions can be made to the program (even after execution in the Run Mode) by returning to Load. New key entries will be automatically appended to the end of the existing stored sequence. By executing the program before returning to Load, the calculator display will have a valid display and be in the correct state for properly displaying the new key additions. In this manner long programs may be constructed by connecting together a series of short sequences which are debugged as you go (reducing the possibility of error and minimizing confusion).

Running a Program

Use of a stored program requires only that the calculator be preconditioned, if necessary, and the Start key depressed while in the Run Mode. The program will continue to the end, or until a Halt is encountered in the key sequence.

Halts act as a pause during execution to permit entry of variable data, manual calculation of data, or checking of intermediate values. They are also available as user decision points for jumping to subsequent programs and can provide the capability for multiprogram labeling. When a Halt is encountered during execution, the MM5765 stops making key closures and returns control to the keyboard.

Upon reaching the end of a program, the internal pointer will return to the beginning and wait for another Start key.

As discussed above, programming certain sequences can result in errors in the calculator chip either during loading or during execution. If an error occurs as the program is loaded, the MM5765 will continue to store key depressions as they are made—independent of the calculator. Such a situation exists if a calculation results in overflow during execution of a stored program. The MM5765 continues to step through the sequence completely independent of calculator status as long as the Ready signal responds properly.

Multiple Programs

Use of the Skip key in the Load Mode codes that location as the beginning of a new program, just as the Start key is used to initialize the first program. All other aspects of loading the program are the same.

When a program stops at a Halt during execution, the user has the option of pressing the Skip key to jump to the next program or the Start key if he wishes to continue the original sequence. When control passes to the next program, execution begins and proceeds to the end of that program or until a Halt is encountered.

This property of automatically executing a program down to the first Halt provides a convenient method of labeling multiprograms. For example, entering a program with the sequence:

Start	(Load/Run = Load Mode)
1	
Halt	
C	(Calculator Clear Entry)
⋮ }	Desired key sequence for Program No. 1
Halt	
Skip	
2	
Halt	
C	
⋮ }	Desired key sequence for Program No. 2
Halt	

has stored two program sequences. In the Run Mode, pressing Start will display a "1", a second Start will execute Program 1 (or to the first internal Halt) eventually stopping at the last Halt and displaying a program result. The operator now has the opportunity to make a decision. He may rerun Program 1 by using the Start key, or continue to Program 2 by depressing the Skip key.

If he chooses Skip, a "2" will be displayed indicating that Program 2 has been addressed (as programmed by the Skip-2-Halt sequence at the beginning of Program 2 in the Load Mode). Start will then execute Program 2 down to its first Halt. The Program 2 result can be displayed by inserting another Halt at the end of that sequence. If a third program has been stored in the MM5765, depressing Skip will move the internal pointer to the beginning of that program and execute it to the first Halt. Assuming a Skip-3-Halt sequence was used at the front of the program, a "3" would be displayed by the calculator. If the operator had wished to rerun Program 1, instead of advancing to Program 3, he would have used Start (internal pointer is initialized), Start (displays shows "1") and Start (program is executed). For a rerun of Program 2 from the last Halt of Program 2, he would push Start (internal pointer is initialized) and Skip (pointer locates the top of Program 2, executes to first Halt and calculator displays "2").

Adding a Step Mode Feature

By returning the Ready input of the MM5765 to V_{SS} when the Mode Switch is in the Run Mode position, and depressing any of the control keys (Start, Skip, Halt or Delete) the program stored in the MM5765 may be executed and advanced one step at a time. This provides a convenient method of debugging programs.

Figure 5 shows the wiring of a 2-pole, 3-position switch used as the Mode Switch of a Programmer/Calculator system with the Step Mode as an added feature. Switching from the Load Mode to the Step Mode conditions

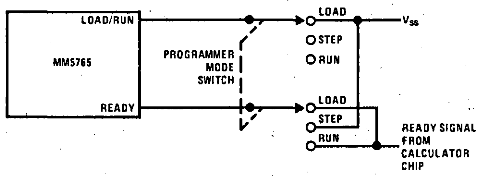


FIGURE 5. Switch Wiring for Adding Step Mode

the programmer to step through the stored program starting from the first entry of the first program. Start must be used to initiate the sequence, then any of the control keys can be used. Each depression of Start, Skip, Halt or Delete will advance the program being executed by the calculator one step. When a Halt is encountered in the program while in the Step Mode, the MM5765 ignores all key entries except Start or Skip just as described in Table I. If the Mode Switch is moved to Step from a Halt point in the Run Mode, the program may be stepped from that point on by using Start or Skip followed by depressions of any of the control keys. Switching to Run from any intermediate point of a Run operation from that point. From a Halt, a Start or Skip Key must be pressed after switching to the Run Mode.

PROGRAMMING EXAMPLES

These examples assume use of the MM5738 calculator, which is an 8-digit, floating point, algebraic notation, single memory chip with constant operation. Please review the MM5738 data sheet for explanation of keyboard notation and function capability.

Example 1

A problem often encountered in communications design is the solution of

$$X = Y\left[\frac{\text{Sin}\,\theta}{\theta}\right]$$

With a programmer and even a simple calculator like the MM5738, this problem can be repetitively solved easily without tables. First, program the sequence for approximating sin θ using

$$\text{Sin}\,\theta \cong \theta - \frac{\theta^3}{3!} + \frac{\theta^5}{5!}\text{, where } \theta \text{ is expressed in radians.}$$

$$= \frac{120\theta - 20\theta^3 + \theta^5}{120}\text{, where } 5! = 120$$

$$= \frac{[(\theta^2 - 20)\,\theta^2 + 120]\,\theta}{120}$$

Example 1 (Con't)

KEY	DISPLAY	RUN/LOAD	COMMENTS
C		Load	
C	0	Load	Clear calculator
2	2	Load	Dummy variable "2" for θ is entered.
Start	2	Load	MM5765 is initialized.
MS	2	Load	
X	2	Load	
=	4	Load	θ^2 is formed
–	4	Load	
20	2 0	Load	
X	– 1 6	Load	
MR	2	Load	
X	– 3 2	Load	
MR	2	Load	
+	– 6 4	Load	$(\theta^2 - 20)\,\theta^2$ is formed.
122	1 2 2	Load	122 is an entry error
C	– 6 4	Load	After entering "C", operator can simply
Delete	– 6 4	Load	continue by entering 120, or can correct
Delete	– 6 4	Load	program sequence by deleting last four
Delete	– 6 4	Load	keys. Result is the same, except the second
Delete	– 6 4	Load	alternative would use less program storage.
120	1 2 0	Load	
X	5 6	Load	
MR	2	Load	
÷	1 1 2	Load	
120	1 2 0	Load	
=	0.9 3 3 3 3 3 3	Load	Sin θ for θ = 2 radians is displayed

Check program by executing with $\theta = \frac{\pi}{4}, \frac{\pi}{3}$

KEY	DISPLAY	RUN/LOAD	COMMENTS
3.14	3.1 4	Run	Enter approximation of π
÷	3.1 4	Run	
4	4	Run	
=	0.7 8 5	Run	$\theta = \frac{\pi}{4}$, in radians
Start	0.7 0 6 8 6 1 3	Run	$\sim \mathrm{Sin}\frac{\pi}{4}$ displayed
3.14	3.1 4	Run	
÷	3.1 4	Run	
3	3	Run	
=	1.0 4 6 6 6 6 6	Run	$\theta = \frac{\pi}{3}$, in radians
Start	0.8 6 6 0 2 8 7	Run	$\sim \mathrm{Sin}\frac{\pi}{3}$ displayed

Now we would like to add to the same program the rest of the expression:

$$Y \frac{\mathrm{Sin}\,\theta}{\theta}$$

KEY	DISPLAY	RUN/LOAD	COMMENTS
1	1	Run	"1" is dummy variable for sin θ
Halt	1	Load	"Halt" is tagged onto end of existing program to allow readout of sin θ during execution
÷	1	Load	
MR	1.0 4 6 6 6 6 6	Load	
X	0.9 5 5 4 1 4	Load	
Halt	0.9 5 5 4 1 4	Load	Allows for Y entry
1	1	Load	Dummy variable for Y
Delete	1	Load	Dummy variable is removed from program
=	0.9 5 5 4 1 4	Load	by Delete, or Halt could have been held down while 1 is entered, in which case Delete would not be required.

8

Example 1 (Con't)

Problems can now be solved using the program.

Evaluate: $0.54 \frac{\text{Sin}(0.72)}{0.72}$

KEY	DISPLAY	RUN/LOAD	COMMENTS
0.72	0.7 2	Run	Enter θ = 0.72 radians
Start	0.6 5 9 4 0 4 4	Run	Sin (0.72) displayed
Start	0.9 1 5 8 3 9 4	Run	
.54	0.5 4	Run	Enter variable Y
		Run	
Start	0.4 9 4 5 5 3 2	Run	$0.54 \frac{\text{Sin}(0.72)}{0.72}$ displayed

A sequence could easily have been included to convert degrees to radians.

PROGRAMMING

As an example of a multiprogram application, consider an automobile salesman who needs to calculate price plus sales tax, down payment and monthly payment on new cars many times a day. Again assume use of the MM5738 (although more powerful NSC calculators could obviously make the problem even easier). To simplify the example, assume the finance time is fixed at 36 months and the interest rate at 12% of the unpaid balance.

KEY	DISPLAY	RUN/LOAD	COMMENTS
C		Load	
Start		Load	Clear calculator and programmer. Label
1	1	Load	Program No. 1
Halt	1	Load	
C	0	Load	Clear program label.
5	5	Load	Sales tax = 5%.
%	0.0 5	Load	
X	0.0 5	Load	
Halt	0.0 5	Load	
100	1 0 0	Run	Load dummy variable for car price. Switching
MS	1 0 0	Load	to Run is another method of entering a dummy
+	5.	Load	variable without having to Delete.
K=	1 0 5.	Load	
Halt	1 0 5	Load	Program No. 1 displays price + tax amount.
Skip	1 0 5	Load	Initialize Program No. 1
2	2	Load	
Halt	2	Load	Label Program No. 2
C	1 0 5	Load	Clear program label.
Halt	1 0 5	Load	"Halt" for down payment %.
20	2 0	Run	Dummy down payment %.
%	0.2 0	Load	
X	0.2 0	Load	
MR	1 0 0	Load	
=	2 0	Load	
Halt	2 0	Load	Program No. 2 displays required down payment.
Skip	2 0	Load	Initialize Program No. 3.
3	3	Load	
Halt	3	Load	Label Program No. 3.
C	2 0	Load	Clear program label.
−	2 0	Load	
MR	1 0 0	Load	
=	−8 0	Load	Program No. 3 computes monthly
MS	−8 0	Load	payment from equation
1.01	1.0 1	Load	
X	1.0 1	Load	Monthly payment = [Total loan $(1 + i/q)^{nq}/nq$]
1.01	1.0 1	Load	i = interest per year, 12% is assumed.
=	1.0 2 0 1	Load	nq = total number of months = 36
			q = 12 months per year
			$(1 + i/q) = 1.01$

PROGRAMMING (CON'T)

KEY	DISPLAY	RUN/LOAD	COMMENTS
=	1.040604	Load	$(1.01)^4$
=	1.0828566	Load	$(1.01)^8$
=	1.1725784	Load	$(1.01)^{16}$
X	1.1725784	Load	
1.01	1.01	Load	
=	1.1843041	Load	$(1.01)^{17}$
K=	1.1961471	Load	$(1.01)^{18}$
=	1.4307678	Load	$(1.01)^{36}$
X	1.4307678	Load	
MR	80	Load	
÷	114.46142	Load	
36	36	Load	
=	3.179483	Load	
Halt	3.179483	Load	Program No. 3 displays required monthly payment.

EXECUTION OF PROGRAM

Salesman has potential customer for $4995.95 automobile. Bank requires 20% down. The customer wants to know amount of down payment and monthly payments over 3 years at 12%.

KEY	DISPLAY	RUN/LOAD	COMMENTS
Start	1	Run	Program No. 1 label.
Start	0.05	Run	Sales tax displayed.
4995.95	4995.95	Run	Price entered.
Start	5245.7475	Run	Price + tax displayed.
Skip	2	Run	Program No. 2 label.
Start	5245.7475	Run	
20	20	Run	Enter % down.
Start	999.19	Run	Down payment displayed.
Skip	3	Run	Program No. 3 label.
Start	158.84543	Run	Monthly payment displayed.

8

Calculators

MM5766 calculator programmer

general description

The MM5766 provides a convenient and inexpensive means of adding "learn mode" programmability to the National Semiconductor MM5758 scientific calculator chip. The monolithic MOS integrated circuit combines P-channel enhancement and depletion mode technologies to obtain low voltage and low power characteristics necessary for economical battery-powered products.

The MM5766 is a dynamic key sequence programmer that memorizes any combination of key entries while in the Load Mode, then automatically plays back the programmed sequence as often as desired in the Run Mode. Up to 102 characters can be stored in multiprogram sequence blocks. Each block, or program, can be executed individually or the operator can make the decision to branch to specific programs, run each in series or perform intermediate calculations from the keyboard. When programming in the Load Mode, the Delete key provides a convenient editing feature and the Halt key programs variable data entry points where control is temporarily returned to the operator in the Run Mode. Start and Skip keys control operation in both modes.

Synchronization with the calculator chip is accomplished by monitoring its Digit Output and Ready signals. The digit signals give timing information while the Ready indicates status of the calculator and synchronizes the key entry interface between it and the MM5766.

Up to four switch inputs (K1, K2, K3 and K4) and up to twelve digit lines are connected in parallel with the calculator switch and digit terminals that scan the keyboard. Keys stored in the MM5766 that are entered by selecting K1 through K4 are encoded simply as matrix positions, i.e., a particular switch input at a specific digit time. Therefore it is the key matrix address that is stored and not the key function. Please refer to the MM5765 data sheet for a detailed functional description.

features

- Any key sequence, including constants and data entry points, may be stored automatically in the Load Mode and executed in the Run Mode.
- 102 step storage capacity of up to 47 different keys arranged in a 12 x 4 matrix.
- Multiprogram capability
- Provision for editing in Load Mode using the Delete key
- Convenient verification of programs using a Step Mode feature
- Alarm for full storage condition—or if a deletion of the first step in a program is attempted
- Power-on clear

block and connection diagrams

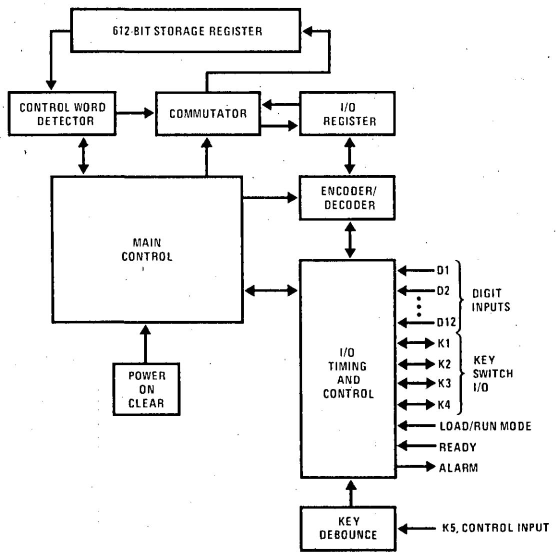
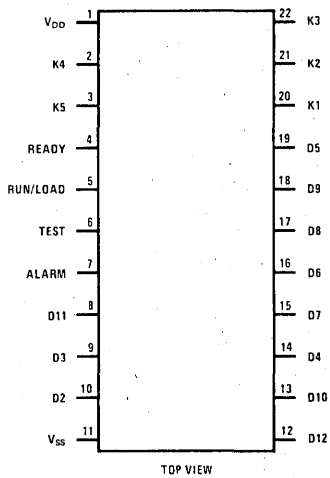


FIGURE 1

Dual-In-Line Package



TOP VIEW

Order Number MM5766N
See Package 21

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All other pins connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$V_{SS}-6.5V \le V_{DD} \le V_{SS}-9.5V$

(V_{SS} is always the most positive supply)

dc electrical characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Operating Supply Current	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		8.0	18.0	mA
	Keyboard Scan Input Levels (K1, K2, K3, K4)					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} - 7.2V$	$V_{SS}-2.5$			V
		$V_{DD} = V_{SS} - 8.8V$	$V_{SS}-4.0$			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{DD}+1.0$	V
		$V_{DD} = V_{SS} - 9.5V$			$V_{DD}+1.5$	V
	K5 and Digit Input Levels (D2 through D12)					
V_{IH}	Logical High Level	$V_{DD} = V_{SS} - 7.2V$; $I_{IH} \ge -200\mu A$	$V_{SS}-2.5$			V
		$V_{DD} = V_{SS} - 8.8V$; $I_{IH} \ge -200\mu A$	$V_{SS}-4.0$			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{DD}+1.0$	V
		$V_{DD} = V_{SS} - 9.5V$			$V_{DD}+1.5$	V
	Other Inputs (Ready, Run and Test)					
V_{IH}	Logical High Level		$V_{SS}-2.5$			V
V_{IL}	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS}-5.0$	V
		$V_{DD} = V_{SS} - 9.5V$			$V_{SS}-6.0$	V
	Switch Buffer Output Levels (K1, K2, K3, K4)					
V_{OH}	Logical High Level	$V_{DD} = V_{SS} - 7.2V$	$V_{SS}-1.5$		V_{SS}	V
		$V_{DD} = V_{SS} - 8.8V$	$V_{SS}-3.0$		V_{SS}	V
V_{OL}	Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			$V_{SS}-6.0$	V
		$V_{DD} = V_{SS} - 9.5V$, $I_{OL} \le -1.5$ mA			$V_{SS}-7.0$	V
	Alarm Output Current					
	Source Current	$V_{OUT} = V_{SS} - 4.5V$, $V_{DD} = V_{SS} - 6.5V$	-5.0			mA
		$V_{OUT} = V_{SS} - 5.2V$, $V_{DD} = V_{SS} - 7.25V$		-8.0		mA
		$V_{OUT} = V_{SS} - 7.8V$, $V_{DD} = V_{SS} - 9.5V$			-20.0	mA

ac electrical characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Digit Input Time	*(Figure 3)*	70			μs
	Word Time	*(Figure 3)*	0.64			ms
	Switch Input Time	*(Figure 3)*	70			μs
	Switch Output Time	*(Figure 4)*	70			μs
	Switch Propagation Delay Output	*(Figure 4)*		15	26	μs
t_R and t_F	Switch Output Transition Time	C_{LOAD} = 100 pF, *(Figure 4)*		2		μs
	Switch Input K5 Key Bounce-out Stability Time (The time a keyboard input must be continuously higher than the minimum Logical High Level to be accepted as a key closure, or lower than the maximum Logical Low Level to be accepted as a key release, i.e., 6 or 7 cycles of D2.)		4.5		17.0	ms
	Ready Timing	*(Figure 3)*				
$t_R=t_F$				3	5	μs
t_D			0.1			μs
$t_{SET\text{-}UP}$			20			μs
t_{PW}			400			μs
	Key Closure Rate (Time between consecutive key outputs in Run Mode.)			40		ms
	Key Acceptance Rate (Time between consecutive key inputs in Load Mode.)				47	ms

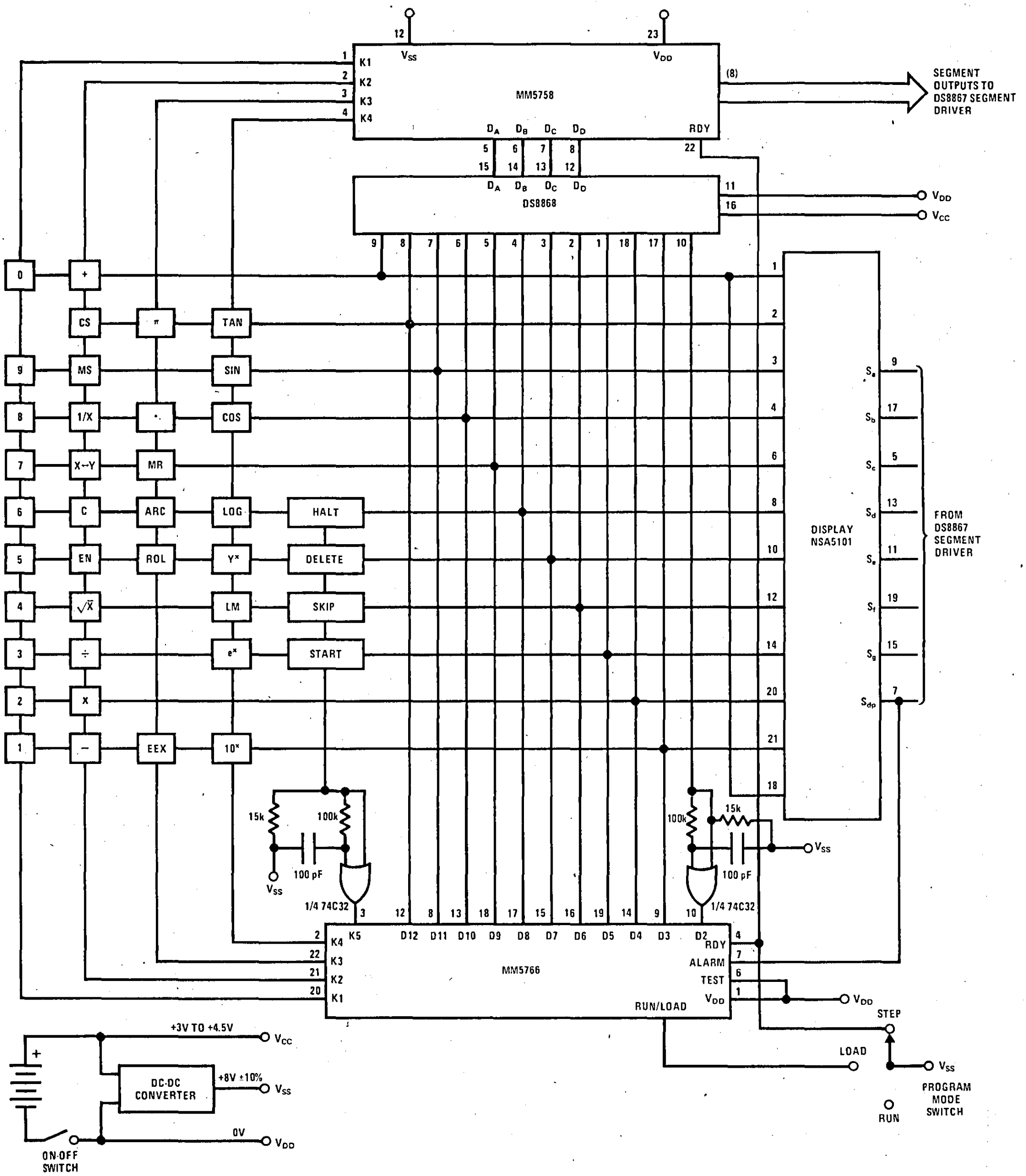


FIGURE 2. Interface of MM5766 Programmer with MM5758 Scientific Calculator

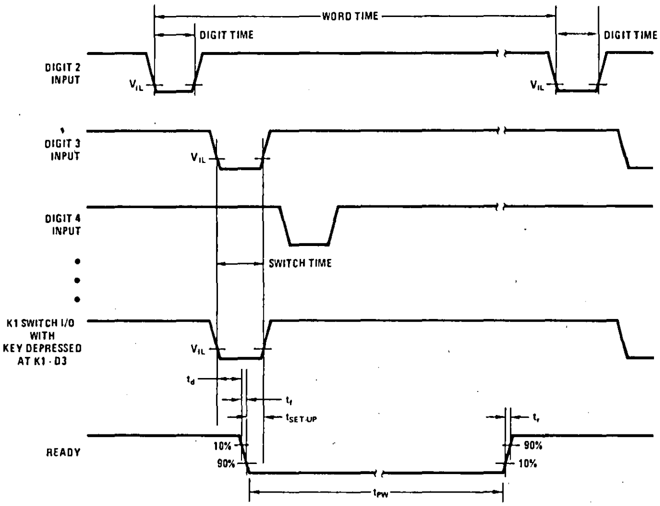


FIGURE 3. Input Timing

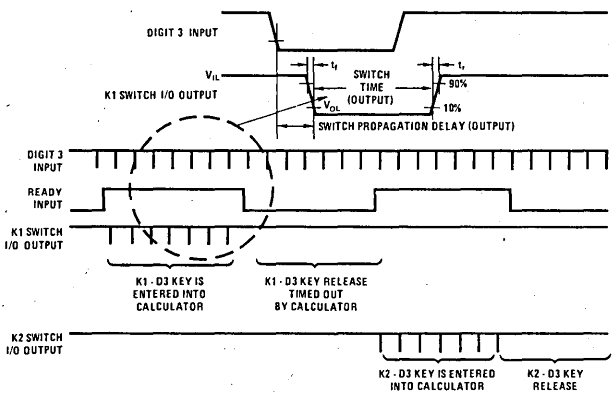


FIGURE 4. Programmer Output Timing

8

Calculators

MM5767 slide rule calculator*

general description

The single-chip MM5767 Slide Rule Calculator was developed with the primary objective of low end-product cost. A complete calculator as shown in *Figure 1* requires only the MM5767, a 20 or 22 key keyboard, DM8864 digit driver, NSA298 LED display and a 9V battery with appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and 7-segment output display encoding are included on-chip and require no external components. Segments can usually be driven directly from the MM5767, as it typically sources about 8.5 mA of peak current. (Note: the typical duty cycle of each digit is 0.104; average LED segment current is therefore approximately 0.89 mA.) The left-most digit is used for the negative sign or the decimal point of a number less than unity.

An internal power-on clear circuit clears all registers, including the memory, when V_{DD} and V_{SS} are initially applied to the chip.

Trailing zero suppression allows convenient reading of the left justified display, and conserves power. The DM8864 digit driver is capable of sensing a low battery voltage and providing a signal during Digit 9 time that can be used to turn on one of the segments as an indicator.

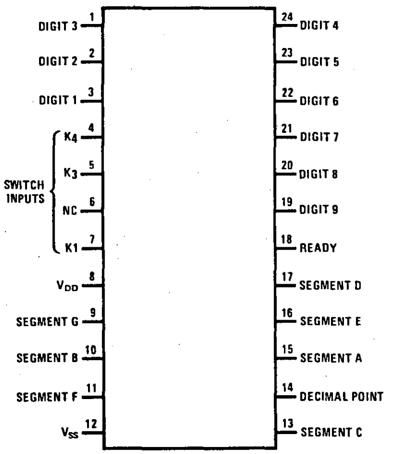
features

- 20 or 22 key keyboard
- Full 8-digit entry and display capacity
- Complete electronic slide rule capability
  - Arithmetic functions: +, −, x, ÷, $\sqrt{x}$, 1/x
  - Logarithmic functions: ln x, log x, e^x
  - Trigonometric functions: sin x, cos x, tan x, arc sin x, arc cos x, arc tan x
  - Other functions: Y^x, π, change sign, exchange, radians to degrees, degrees to radians
- Three-register operational stack
- Independent accumulating storage register with store, recall, memory plus and memory minus functions
- Floating point input and output
- Direct 9V battery compatibility; low power dissipation
- Power-on clear
- No external components required other than display digit driver, keyboard and LED display for complete calculator
- Error indication for over range, overflow and invalid operations
- Left justified entry and results with trailing zero suppression
- Automatic display cutoff
- Reverse polish notation

***Note:** For detailed information on electrical specifications and key operations please refer to the MM5760 data sheet.

connection diagram

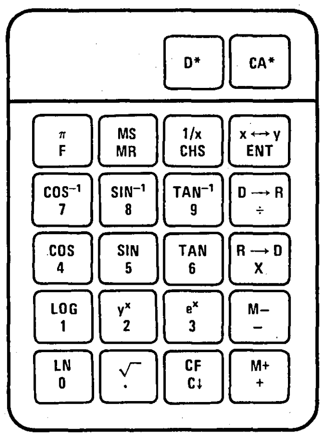
Dual-In-Line Package



TOP VIEW

Order Number MM5767N
See Package 22

keyboard outline

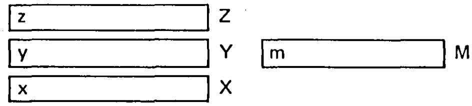


*Optional

Typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff is included. If no key closure occurs for approximately 35 seconds, all numbers are blanked and all decimal points displayed.

The keys are arranged in a three-by-nine matrix *(Figure 2)*. In addition to seven arithmetic functions plus logarithmic, trigonometric and accumulating memory functions, the calculator is capable of calculating Y^x, automatically entering π and providing degrees/radian converions.

The user has access to four registers designated X, Y, Z and M. X is the display and entry register, and is the bottom of a "push-up" stack that also includes registers Y and Z:



Note: Lower case letters designate the data in the register identified by a capital letter.

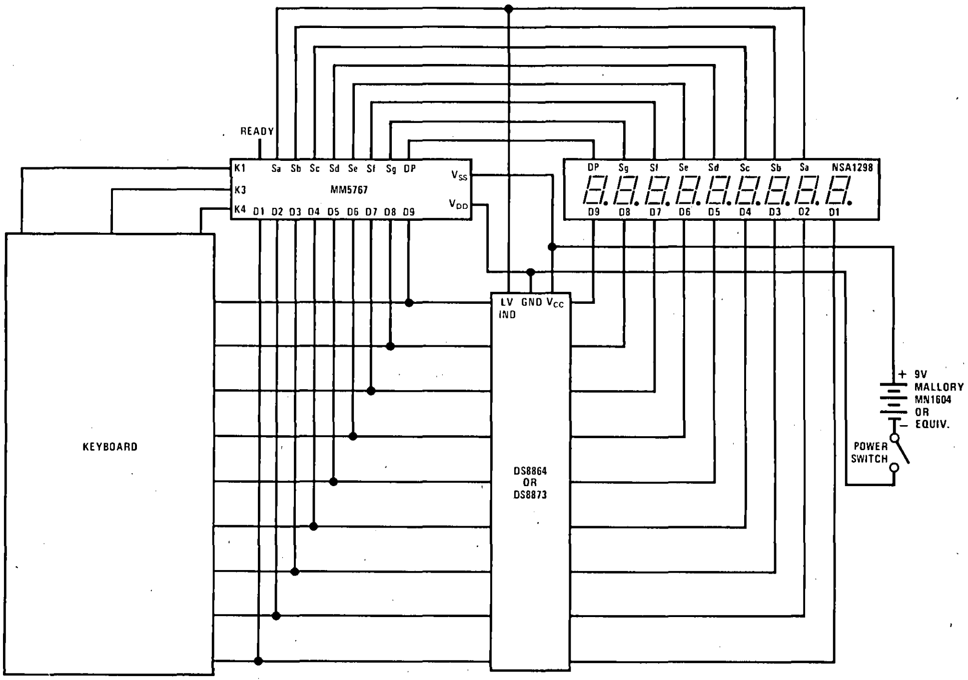


FIGURE 1. Complete Calculator Schematic

	K1	K3	K4
D9		TAN/6	
D8		COS^{-1}/7	π/F
D7	R → D/x	SIN^{-1}/8	D*
D6	D → R/÷	TAN^{-1}/9	LN/0
D5	M+/+	$\sqrt{\ }$/·	Log/1
D4	M−/−	EXC/EN	Y^x/2
D3	CLF/CL	MS/MR	e^x/3
D2	CA*	1/x / CS	COS/4
D1			SIN/5

*Keys not included in 20 key version.

FIGURE 2. Keyboard Matrix

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5767 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K3 or K4 is forced more positive than the Logical High Level specified in the Electrical Specifications. An internal counter is started as a result of the closure. The key operation begins after nine word times if the key input is still at a Logical High Level. As long as the key is held down (and the key input remains high) no further entry is allowed. When the key input changes to a Logical Low Level, the internal counter starts a sixteen word time-out for key release. During both entry and release time-outs the key inputs are sampled approximately every other word time for valid levels. If they are found invalid, the counter is reset and the calculator assumes the last valid key input state.

One of the popular types of low-cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5767 recognizes a series contact resistance up to 50 kΩ as a valid key closure, assuring a reliable interface for that type of keyboard.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately 35 seconds, an internal automatic display cutoff circuit will blank all segments and display nine decimal points. Any key depression will restore the display; to restore the display without modifying the status of the calculator, use two change sign, "CS," depressions.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 3 and 4.* It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

ERROR INDICATION

In the event of an operating error, the MM5767 will display all zeros and all decimal points. In addition to normal calculator overflow situations which occur as a result of adding, subtracting, multiplying or dividing and including division by zero, the error indication is displayed for any other calculation where the result is $|R| > 99999999$ or $|R| \leq 0.00000001$.

For error conditions the Z-register is automatically cleared and the Y- and M-registers are saved. An error condition is cleared by depressing any key except "1/X," "÷," "LOG X" or "LN X." Operation on the X register with an error displayed will be performed as if X contained a zero.

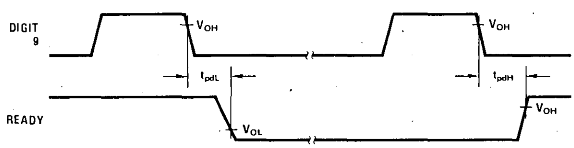


FIGURE 3. Ready Timing

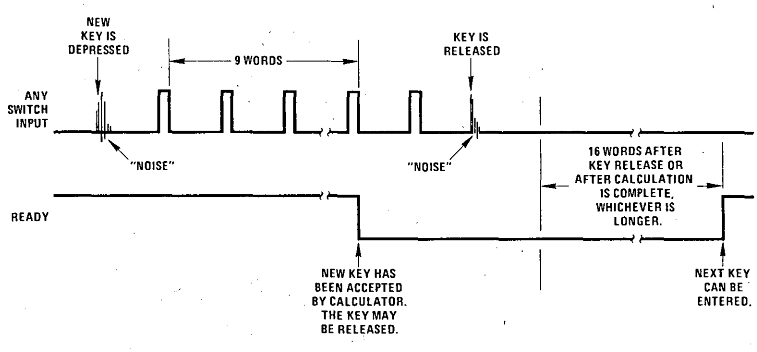


FIGURE 4. Functional Description of Ready Signal and Key Entry

RANGE AND ACCURACY OF FUNCTIONS

The smallest magnitude that can be displayed is ±0.00000001 and the total range is from −99999999 to +99999999. The arithmetic functions (+, −, x, ÷, 1/X, $\sqrt{X}$) have eight digit accuracy. All results are truncated. Table I summarizes range and accuracy of the other functions. Arithmetic calculations will be completed in less than 0.5 second; all others except Y^x in less than 2.5 seconds and Y^x in less than 5 seconds.

TABLE I. Digit Accuracy for Various Functions

FUNCTION	RANGE	APPROXIMATE ACCURACY (Note 1)
SIN, COS, TAN	$\sim -90^\circ$ to $\sim 90^\circ$ $\sim -360^\circ$ to $\sim 360^\circ$	7 Digits 6 Digits
ARC SIN and ARC COS	~ -1 to $\sim +1$	6 Digits
ARC TAN	−99999999 to 99999999	6 Digits
LOG	$X \geq 0$	6 Digits
e^X	$-28 \leq X \leq \ell n\ 99999999$	6 Digits
LN	$X \geq 0$	6 Digits
$\sqrt{X}$	$X \geq 0$	8 Digits
Y^X	$Y > 0$ $X\ \ell n\ Y \leq \ell n\ 99999999$	5 Digits

Note 1: Six digit accuracy, as an example, would be:

1 2 3 4 5 6 X X

±1

n digit accuracy has the n^{th} digit from the MSD being displayed accurate within ±1.

MM5777 calculator 6-digit, 4-function, floating decimal point

general description

The MM5777 single-chip calculator was developed using a metal gate, P-channel, enhancement and depletion mode MOS process with low end-product cost as the primary objective. A complete calculator, as shown in *Figure 1,* requires only a keyboard, DS8977 digit driver, 6 1/4 digit LED display, an NSA1161 and a 9V battery with appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and output 7-segment display decoding are all included on-chip and require no external discrete components. LED segments can be driven directly from the MM5777 as it typically sources 8.0 mA of peak current. [Note: The typical duty cycle of each digit is 0.143; average LED segment current is therefore approximately 0.143 (8.0 mA), or 1.14 mA. Correspondingly, the worst-case average segment current is 0.143 (4.5 mA), or 0.64 mA.] The seventh digit is used for the negative sign of a six digit number and as an error indicator. Negative results less than six digits will have the negative sign displayed one digit to the left of the most-significant-digit (MSD). The DS8977 digit driver is capable of indicating a low battery voltage condition by turning on a seventh digit segment—which does not hinder the actual calculator operation.

Leading and trailing zero suppression allows convenient reading of the right justified display and conserves power. Battery life is estimated to be 10 to 20 hours, depending on battery quality, operating schedule and the average number of digits displayed.

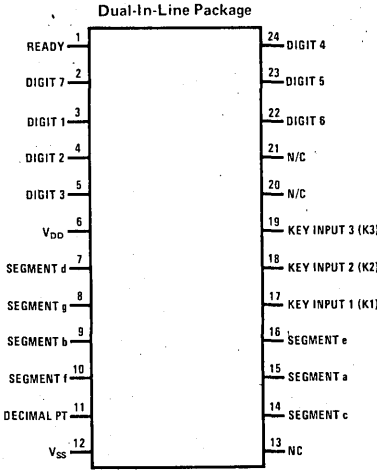
The Ready output signal is used to indicate when the calculator is performing an operation (Table I). It is useful in testing of the device or when the MM5777 is used as part of a larger system and is required to interface with other logic. (Another feature that is important in such applications is the ability to reduce the key debounce time from seven word times to four word times by forcing the Digit 6 output high during Digit 7 time.)

features

- 6-digit entry and display capacity for positive and negative numbers
- Four functions (+, −, x, ÷)
- Floating negative sign indicator is always displayed one digit to left of MSD
- Convenient algebraic key entry notation
- Floating point input and output
- Chain operations
- Direct 9V battery compatibility; low power
- Direct interface to LED segments
- No external components are required other than display digit driver, keyboard and LED display for complete calculator
- Overflow and divide-by-zero error indication
- Right justified entry and results, with leading and trailing zero suppression

connection diagram

Dual-In-Line Package

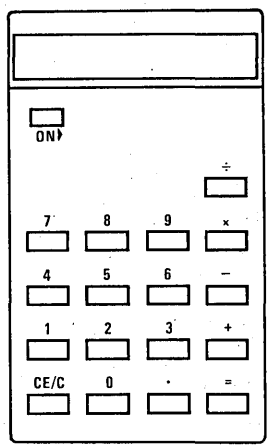


TOP VIEW

Order Number MM5777N

See Package 22

keyboard outline



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}. (All other pins connected to V_{SS}).	V_{SS} + 0.3V to V_{SS} − 12.0
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \le V_{SS} - V_{DD} \le 9.5V$
(V_{SS} always defined as most positive supply voltage.)

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		8.0	14.0	mA
Keyboard Scan Input Levels (K1, K2 and K3)					
Logical High Level (V_{IH})	$V_{SS} - 6.5V \le V_{DD} \le V_{SS} - 9.5V$	V_{SS}−2.5			V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS} - 6.5V$			V_{SS}−5.0	V
	$V_{DD} = V_{SS} - 9.5V$			V_{SS}−6.0	V
Digit Output Levels (Note 1)					
Logical High Level (V_{OH})	$V_{SS} - 6.5V \le V_{DD} \le V_{SS} - 9.5V$	V_{SS}−1.5			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS} - 6.5V$			V_{SS}−6.0	V
	$V_{DD} = V_{SS} - 9.5V$			V_{SS}−7.0	V
Segment Output Current (Sa through Sg and Decimal Point)	$T_A = 25°C$				
	$V_{OUT} = V_{SS} - 3.8V$, $V_{DD} = V_{SS} - 6.5V$	−5.0	−8.0		mA
	$V_{OUT} = V_{SS} - 5.0V$, $V_{DD} = V_{SS} - 8.0V$		−10.0		mA
	$V_{OUT} = V_{SS} - 6.5V$, $V_{DD} = V_{SS} - 9.5V$			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	$I_{OUT} = -0.4$ mA	V_{SS}−1.0			V
Logical Low Level (V_{OL})	$I_{OUT} = 10\mu A$			V_{DD}+1.0	V

Note 1: With digit connected through key to K-line and to DS8977.

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time *(Figure 2)*		0.50	1.20	4.1	ms
Digit Time *(Figure 2)*		70	170	580	µs
Interdigit Blanking Time *(Figure 2)*			4		µs
Digit Output Transition Times (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF		2		µs
Keyboard Inputs High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		µs
Ready Output Propagation Time *(Figure 3)*					
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	60	140	480	µs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF	0.06	0.5	1.5	ms
Key Bounce-out Stability Time (The time a keyboard input must be continuously higher than the minimum logical high level to be accepted as a key closure, or continuously lower than the maximum logical low level to be accepted as a key release.)		3.40	8.20	29.0	ms
Calculation Time for 999999 ÷ 1 = 999999		53.9	128.7	451	ms

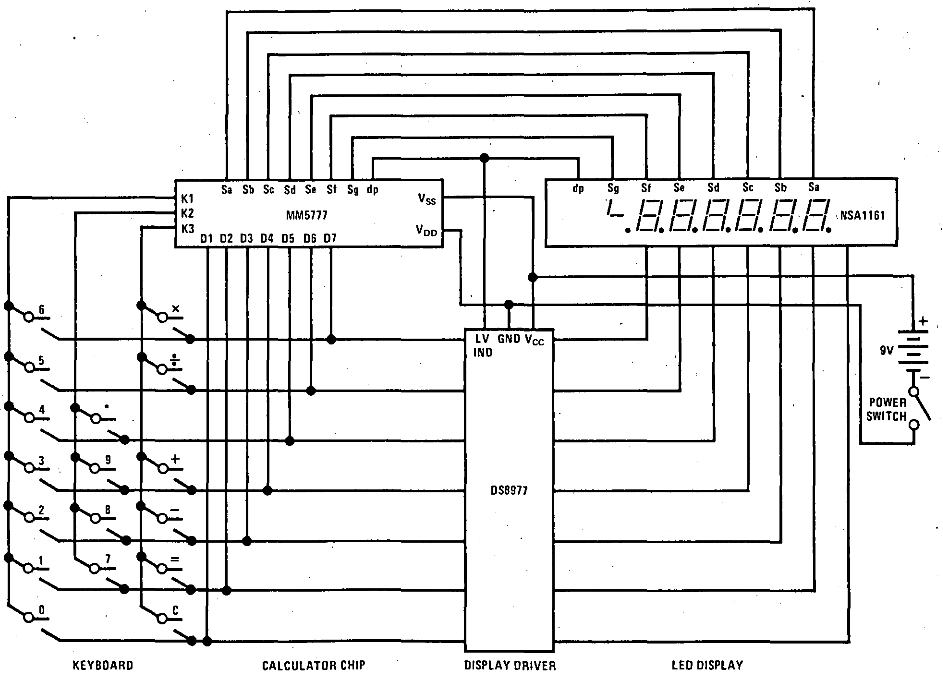


FIGURE 1. Complete Calculator Schematic

TABLE I. Ready Signal Description

CALCULATOR FUNCTION	READY SIGNAL
Idle	*READY* is quiescently at a Logical High Level ($\sim V_{SS}$).
Key Entry and Functional Operation	When a key is depressed, the bounce-out stability timer is initiated. *READY* remains high until the bounce-out time is completed and the key is entered, at which time it changes to a Logical Low Level ($\sim V_{DD}$).
Key Release and Return to Idle	*READY* remains low until key release is debounced and the calculator returns to the idle state. The low to high transition signals the return to idle. (The display may lag the *READY* by up to eight word times.)

KEY INPUT BOUNCE AND NOISE REJECTION

The MM5777 calculator chip is designed to interface with low cost keyboards, which are often the least desirable from a noise and false entry standpoint.

A key closure is sensed by the calculator chip when one of the Key Input Lines, K1, K2 or K3 is forced more positive than the Logical High Level specified in the Electrical Specifications. At the instant of closure, an internal "Key Bounce-out Stability Time" counter is started. Any significant voltage perturbation occurring on the switched key input during timeout will reset the timer. Hence, a key is not accepted as a valid entry until noise or ringing has stopped and the stability time counter has timed out. Noise that persists will inhibit key entry indefinitely. Key release is timed in the same manner.

One of the popular types of low cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5777 defines a series contact resistance up to 50 kΩ as a valid key closure, providing an optimum interface to that type of keyboard as well as more conventional types.

ERROR CONDITIONS

In the event of an overflow, the MM5777 will indicate error in the leftmost digit and at least five of the significant digits of the answer. Division by zero results in an error indication with six trailing zeros. Once in an error condition, all keys except the clear key are ignored. When used with the NSA1161 display, segments f and g will be displayed in the seventh digit in an error condition.

KEY OPERATIONS

Clear Key

Operation after a number entry clears the entry and displays a previous result. Second depression clears all registers and displays a zero without decimal point in the LSD. Operation after a function key (+, −, x, ÷ or =) clears all registers and displays a zero without decimal point. Two depressions are always required after power is applied.

Number Entries

First, entry clears the display register and enters the number into the least significant digit (LSD) of the display register. Second through sixth entry shifts the display register left one digit and enters the number into the LSD. The seventh, and subsequent entries, are ignored and no error condition is generated. Because only five positions are allowed to follow the decimal point, the sixth and subsequent entries after a decimal point entry are ignored.

Decimal Point

First depression of this key in a number entry will enter a decimal point in the LSD position of the display register. Subsequent depressions of the decimal point key before any function key will be ignored.

Add, Subtract, Multiply or Divide Keys

First depression after a number entry will terminate the entry, perform the previously recorded operation, if any, and record the function key depressed as the next operation to be performed after another number entry. Subsequent depressions of any function key, without an interceding number or decimal point entry will supersede the previous function as the next to be performed. After an equal key, the displayed result of the equal operation will be re-entered and the function key depressed will become the next operation to be performed after a number entry is followed by another function key (including equal).

Equal

First depression after a number entry will terminate the entry, perform the previously recorded operation and record the fact that an equal key has been depressed. Depression after the add, subtract or divide keys, without an interceding number or decimal point entry, will be ignored. After a multiply key, the number being displayed will be squared.

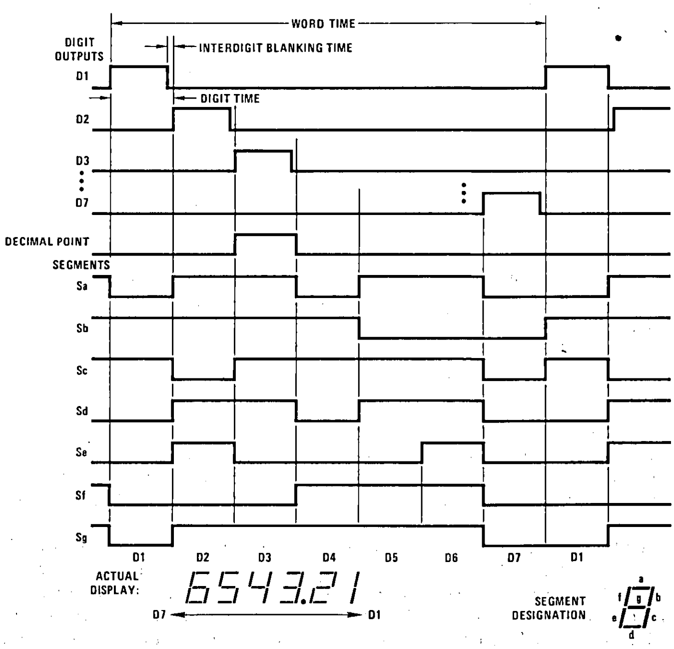


FIGURE 2. Display Timing Diagram

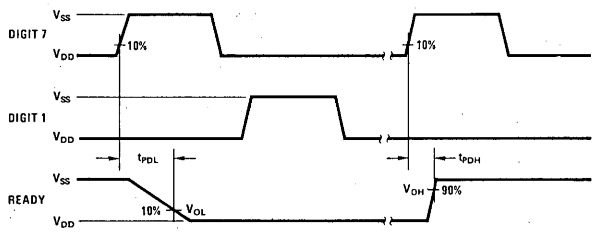


FIGURE 3. Ready Output Timing

sample problems

I. Single Calculations

5 x 3.14 = 15.7

Key	Display	Comments
C		Two clears are required after power-up.
C	0	
5	5	
x	5	
3	3	
.	3.	
1	3.1	
4	3.1 4	
=	1 5.7	

II. Chain Calculations

A. 23.37 + 243.00 − 489.16 = −222.79

Key	Display	Comments
C		
C	0	
23.37	2 3.3 7	
+	2 3.3 7	
243	2 4 3	
x	2 6 6.3 7	Function key completes previously recorded "+" operation.
(Wrong Function Key)		
−	2 6 6.3 7	Wrong "X" function key is updated to "− ."
489.17	4 8 9.1 7	
C	2 6 6.3 7	
489.16	4 8 9.1 6	Number entry error is cleared and corrected. Note the
=	2 2 2.7 9	floating negative sign.

B. Find square root of 169 using a modified Newton approximation method. Let N represent the squared number and X_0 the initial estimate. The first approximation, X_1, is

$X_1 = (N/X_0 + X_0)/2$

If X_0 is 15,

$X_1 = (169/15 + 15)/2$

$X_2 = (169/X_1 + X_1)/2$

$X_3 = (169/X_2 + X_2)/2$, etc.

Key	Display	Comments
C		
C	0	
169	1 6 9	
÷	1 6 9	
15	1 5	
+	1 1.2 6 6 6	
15	1 5	
÷	2 6.2 6 6 6	
2	2	
=	1 3.1 3 3 3	Result is X_1
169	1 6 9	
÷	1 6 9	
13.13	1 3.1 3	Four digits are conveniently remembered

sample problems (con't)

II. Chain Calculations (continued)

Key	Display	Comments
+	1 2.8 7 1 2	
13.13	1 3.1 3	
÷	2 6.0 0 1 2	
2	2	
=	1 3.0 0 0 6	Result is X_2, which is usually adequate. If more accuracy is required, continue the iteration.

III. Auto Squaring

A. $5.25^2 = 27.5625$

Key	Display	Comments
C		
C	0	
5.25	5.2 5	
x	5.2 5	
=	2 7.5 6 2 5	Number in display register is squared.

B. $5.25^5 = 3988.37$

Key	Display	Comments
C		
C	0	
5.25	5.2 5	
x	5.2 5	
=	2 7.5 6 2 5	Auto square = 5.25^2
x	2 7.5 6 2 5	
=	7 5 9.6 9 1	Auto square = 5.25^4
x	7 5 9.6 9 1	
5.25	5.2 5	
=	3 9 8 8.3 7	Result is 5.25^5

MM5780 educational toy calculator general description

The MM5780 single-chip, educational calculator was developed using a metal gate, P-channel, enhancement and depletion mode MOS process. It was designed with low end-product cost as the primary objective and is directed toward the educational toy market. Besides the MM5780, a complete calculator, as shown in *Figure 1*, requires only a keyboard, "Right" and "Wrong" LED display, a 9V battery and an on/off switch. Keyboard encoding and key debounce circuitry, all clock and timing generation and the capability to drive the two LEDs are all included on-chip and require *no* external discrete components.

The MM5780 educational calculator was designed to be a mathematical aid to school age children. Problems are entered into the machine in algebraic form exactly as they are written across a printed page. The student provides the answer or missing factor and when finished, depresses the Test key. "Right" and "Wrong" outputs provide an indication of the results of the test. If wrong, the student trys the problem again. If correct, he can move on to the next problem. Most problems using +, −, x and ÷ can be learned using this machine. The calculator does not have provisions for remainders in division or negative number entries. A negative result can be entered before the Test key is depressed.

The MM5780 is a low power device which operates directly from a 9V battery. Battery life is estimated to be 10 to 30 hours depending on battery quality and operating schedule.

When the battery voltage falls below an operational level, an internal circuit will disable both indicator outputs; i.e., neither indicator will be on after depression of Test.

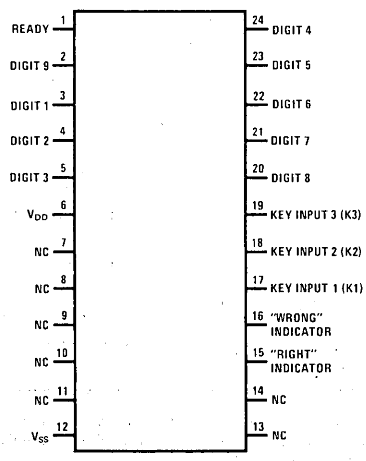
The Ready output signal is used to indicate when the calculator is performing an operation. It is useful in testing of the device or if interfacing with other logic. Another feature that is important in testing is the capability of reducing the key debounce time from seven word times to four word times by forcing the Digit 7 output high during Digit 9 time.

features

- Full 8-digit entry capacity
- Four functions (+, −, x, ÷)
- Convenient algebraic key entry notation
- Floating point input and output
- Chain operations
- Direct 9V battery compatibility; low power
- Direct interface to LED indicators
- No external components required other than keyboard and LED display for complete educational calculator
- Overflow and divide-by-zero error indication
- Low battery voltage sensing

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5780N
See Package 22

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS}. (All other pins connected to V_{SS}.)	V_{SS} + 0.3V to V_{SS} − 12.0
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range (Note 1)

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$
(V_{SS} is always defined as the most positive supply voltage.)

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}-9.5V$, $T_A = 25°C$		8.0	14.0	mA
Keyboard Scan Input Levels (K1, K2 and K3)					
Logical High Level (V_{IH})	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	$V_{SS}-2.5$			V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-5.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-6.0$	V
Digit Output Levels (Note 1)					
Logical High Level (V_{OH})	$V_{SS}-6.5V \leq V_{DD} \leq V_{SS}-9.5V$	$V_{SS}-1.5$			V
Logical Low Level (V_{OL})	$V_{DD} = V_{SS}-6.5V$			$V_{SS}-6.0$	V
	$V_{DD} = V_{SS}-9.5V$			$V_{SS}-7.0$	V
Indicator Output Current					
Source Current	$T_A = 25°C$				
	$V_{OUT} = V_{SS}-4.5$, $V_{DD} = V_{SS}-6.5V$	−10.0	−15.0		mA
	$V_{OUT} = V_{SS}-4.8$, $V_{DD} = V_{SS}-9.5V$		−25.0	−32.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	$I_{OUT} = -0.4$ mA	$V_{SS}-1.0$			V
Logical Low Level (V_{OL})	$I_{OUT} = 10\mu A$			$V_{DD}+1.0$	V

ac electrical characteristics (*Figure 2*)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time		0.6	1.5	5.2	ms
Digit Time		70	170	580	μs
Keyboard Input (K1, K2, K3) High to Low Transition Time After Key Release	C_{LOAD} = 100 pF		4		μs
Ready Propagation Time	C_{LOAD} = 100 pF				
Low to High Level (t_{PDH})		60	140	480	μs
High to Low Level (t_{PDL})			0.5	1.5	ms
Key Bounce-out Stability Time (The time a keyboard input must be continuously higher than the minimum logical high level to be accepted as a key closure, or continuously lower than the maximum logical low level to be accepted as a key release.)		4.2	10.5	35.0	ms
Calculation Time for 99999999 ÷ 1 = 99999999		90	220	765	ms

Note 1: The internal low battery voltage sensing circuit will disable both indicator outputs when $V_{SS}-V_{DD}$ falls below a safe operating voltage. That voltage may be less than or greater than 6.5V depending on process variables; the MM5780 will have been tested to operate correctly for any voltage less than 9.5V at which an indicator output is enabled.

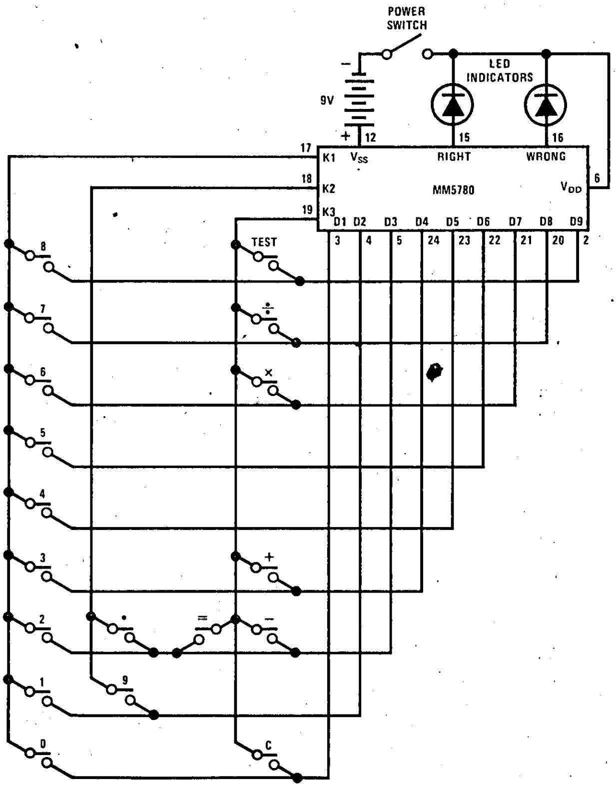


FIGURE 1. Complete Calculator

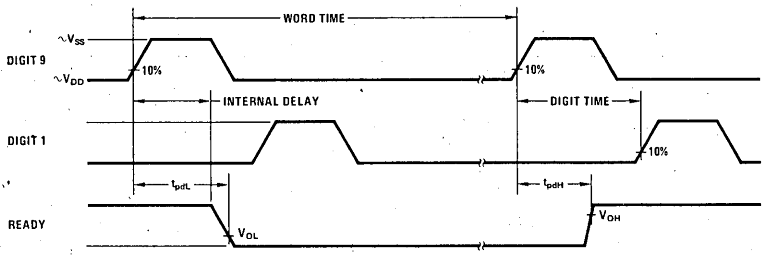


FIGURE 2. Output Timing

KEY INPUT BOUNCE AND NOISE REJECTION

The MM5780 calculator chip is designed to interface with low cost keyboards, which are often the least desirable from a noise and false entry standpoint.

A key closure is sensed by the calculator chip when one of the Key Input Lines, K1, K2 or K3 are forced more positive than the Logical High Level specified in the Electrical Specifications. At the instant of closure, an internal "Key Bounce-out Stability Time" counter is started. Any significant voltage perturbation occurring on the switched key input during timeout will reset the timer. Hence, a key is not accepted as a valid entry until noise or ringing has stopped and the stability time counter has timed out. Noise that persists will inhibit key entry indefinitely. Key release is timed in the same manner.

One of the popular types of low cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM5780 defines a series contact resistance up to 50 kΩ as a valid key closure, providing an optimum interface to that type of keyboard as well as more conventional types.

Error Conditions

In the event of an overflow or divide-by-zero the "Wrong" light will come on and remain on until a Clear key is depressed. Normally the indicator lights are activated only after depression of the TEST key.

KEY OPERATIONS

Clear Key

The Clear key clears all registers to zero and places the machine in an idle state.

Number Entries

First entry clears the entry register and enters the number into the least significant digit (LSD) of the entry register and extinguishes the indicator lights. Second through eighth entry shifts the entry register left one digit and enters the number into the LSD. The ninth and subsequent entries, are ignored and no error condition is generated. Because only seven positions are allowed to follow the decimal point, the eighth and subsequent entries after a decimal point entry are ignored.

Decimal Point

Depression results in a decimal point entry into the entry register.

Add, Subtract, Multiply or Divide Keys

First depression after a number entry will terminate the entry, perform the previously recorded operation, if any, and record the function key depressed as the next operation to be performed after another number entry. Subsequent depressions of any function key, without an interceding number or decimal point entry will supersede the previous function as the next to be performed. If a function key is depressed after an equal key, the result of the operation will be re-entered and the function key depressed will become the next operation to be performed after a number entry is followed by another function key (including equal).

Equal

First depression after a number entry will terminate the entry, perform the previously recorded operation and record the fact that an equal key has been depressed. Depression after the add, subtract or divide keys, without an interceding number or decimal point entry, will be ignored. After a multiply key, the number in the entry register will be squared.

Resultant Entries

Results are entered as number entries after an equal key and before the Test key. Results are assumed positive and a plus key should *not* be entered prior to the resultant. Negative results must be preceded by a minus key.

Test

The Test key is used to terminate computations and to initiate a test of the student's answer versus the calculator's answer. If the answers match, the "Right" indicator is enabled, otherwise the "Wrong" indicator is enabled. If the results are incorrect the problem must be worked again from the beginning.

TABLE I. Ready Signal Description

CALCULATOR FUNCTION	READY SIGNAL
Idle	$\overline{READY}$ is quiescently at a Logical High Level ($\sim V_{SS}$).
Key Entry and Functional Operation	When a key is depressed, the bounce-out stability timer is initiated. $\overline{READY}$ remains high until the bounce-out time is completed and the key is entered, at which time it changes to a Logical Low Level ($\sim V_{DD}$).
Key Release and Return to Idle	$\overline{READY}$ remains low until key release is debounced and the calculator returns to the idle state. The low to high transition signals the return to idle.

TABLE II. Indicator Truth Table

CALCULATOR CONDITION	INDICATOR OUTPUT	
	PIN 15	PIN 16
Test was last key depressed with correct answer entered.	HIGH	LOW
Test was last key depressed with incorrect answer entered or the problem has resulted in an error or overflow condition.	LOW	HIGH
Any key other than Test was last depressed and calculator is not in an error or overflow condition.	LOW	LOW
Clear was last key depressed.	LOW	LOW
The battery supply voltage has fallen below a valid operating voltage for the MM5780. Independent of keys depressed.	LOW	LOW

sample problems

I. Simple Addition: 4 + 5 = ?

Key	Display	Comments
C		
C	N O N E	Clear necessary on power-up
4	N O N E	
+	N O N E	
5	N O N E	
=	N O N E	
8	N O N E	Answer supplied
TEST	W R O N G	Wrong answer
4	N O N E	Indicator goes out
+	N O N E	
5	N O N E	
=	N O N E	
9	N O N E	
TEST	R I G H T	

II. Missing Factor Addition: 6 + ? = 11

Key	Display	Comments
6	N O N E	Indicator goes out
+	N O N E	
5	N O N E	Missing factor supplied
=	N O N E	
11	N O N E	
TEST	R I G H T	

III. Subtraction: 4 – 7 = ?

Key	Display	Comments
4	N O N E	Indicator goes out
–	N O N E	
7	N O N E	
=	N O N E	
–	N O N E	
3	N O N E	Negative answer supplied
TEST	R I G H T	

IV. Multiplication: 7 x 3 = ?

Key	Display	Comments
7	N O N E	Indicator goes out
x	N O N E	
3	N O N E	
=	N O N E	
21	N O N E	Answer supplied
TEST	R I G H T	

sample problems (con't)

V. Missing Factor Multiplication: 6 x ? = 12

Key	Display	Comments
6	N O N E	Indicator goes out
x	N O N E	
3	N O N E	Missing factor supplied
=	N O N E	
12	N O N E	
TEST	W R O N G	Incorrect
6	N O N E	Indicator goes out
x	N O N E	
2	N O N E	Missing factor supplied
=	N O N E	
12	N O N E	
TEST	R I G H T	

VI. Division: 15 ÷ 3 = ?

Key	Display	Comments
15	N O N E	Indicator goes out
÷	N O N E	
3	N O N E	
=	N O N E	
5	N O N E	Answer supplied
TEST	R I G H T	

VII. Complex Chain: (6 + 2 – 10) x 3 = ?

Key	Display	Comments
6	N O N E	Indicator goes out
+	N O N E	
2	N O N E	
–	N O N E	
10	N O N E	
x	N O N E	
3	N O N E	
=	N O N E	
–	N O N E	
6	N O N E	Negative answer supplied
TEST	R I G H T	

Calculators

MM5791 seven-function, accumulating memory calculator

general description

The single-chip MM5791 calculator was developed using a metal-gate, P-channel enhancement and depletion mode MOS/LSI technology with a primary objective of low end-product cost. A complete calculator as shown in *Figure 1* requires only the MM5791, a keyboard, DS8874 digit driver, NSA1198 or NSA1298 LED display and a 9V battery.

Keyboard decoding and key debounce circuitry, all clocks and timing generation, power-on clear, display turnoff and 7-segment output display decoding are included on-chip and require no external components. Segments can usually be driven directly from the MM5791, as it typically sources 8.5 mA of peak current. The left-most, or 9th digit is used to indicate memory in use or the negative sign of an eight digit number.

Leading zero supression and a floating negative sign allows convenient reading of the display and conserves power. The DS8874 digit driver is capable of sensing a low battery voltage and providing a signal during the left-most digit time that can be used to turn on one of the segments as an indicator. Typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff after approximately 25 seconds is included.

The Ready output signal is used to indicate calculator status. It is useful in providing synchronization information during testing and when the MM5791 is used with other logic devices.

Data ($\overline{D}$) and Shift (CP) outputs are the only two connections required between the MM5791 and the digit driver. This reduces the number of pins on both packages and the amount of interconnect on the printed circuit board. *Figure 3* shows the timing relationships between the MM5791 and DS8874.

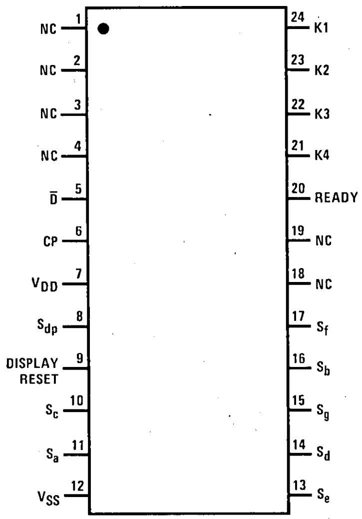
features

- Full 8-digit capacity
- 7-functions (+, −, x, ÷, x^2, $\sqrt{x}$, %)
- Convenient algebraic notation
- Fully protected accumulating memory (M+, M−)
- Automatic constant independent of memory
- Floating input/floating output
- Power-on clear*
- On-chip oscillator*
- Display turnoff after 25 seconds (typical)*
- Direct 9.0V battery compatibility*
- Low system cost
- Direct segment drive of LED display*

*Requires no external components.

connection diagram

Dual-In-Line Package

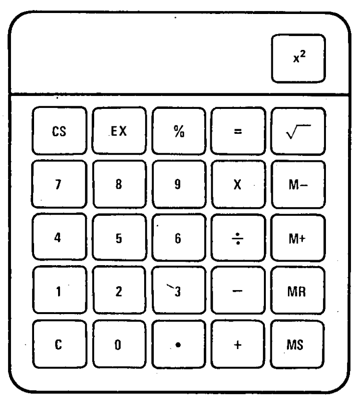


TOP VIEW

Order Number MM5791N
See Package 22

keyboard outline

Sample Keyboard



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} + 0.3V to V_{SS} – 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS}$ –9.5V, T_A = 25°C		8	15	mA
Keyboard Scan Input Levels (K1–K4)					
Logical High Level (V_{IH})	$V_{DD} = V_{SS}$ –6.5V, $I_{IH} \leq$ –300 µA	V_{SS}–2.5		V_{SS}	V
	$V_{DD} = V_{SS}$ –9.5V, $I_{IH} \leq$ –300 µA	V_{SS}–4.7		V_{SS}	V
Logical Low Level (V_{IL})	$V_{DD} = V_{SS}$ –6.5V	V_{DD}		V_{SS}–5.5	V
	$V_{DD} = V_{SS}$ –9.5V	V_{DD}		V_{SS}–8.0	V
Display Reset Input Levels					
Logical High Level	$V_{DD} = V_{SS}$ – 6.5V	V_{SS}–1.5			V
Logical Low Level	$V_{DD} = V_{SS}$ – 9.5V			V_{DD}+1.5	V
Segment Output Current	T_A = 25°C,				
	$V_{OUT} = V_{SS}$ –3.6V, $V_{DD} = V_{SS}$ –6.5V	-5.0			mA
	$V_{OUT} = V_{SS}$ –5.0V, $V_{DD} = V_{SS}$ –8.0V		–10		mA
	$V_{OUT} = V_{SS}$ –6.5V, $V_{DD} = V_{SS}$ –9.5V			–15	mA
Ready Output	$V_{DD} = V_{SS}$ –6.5V				
Logical High Level	I_{OUT} = –250µA	V_{SS}–1.0			V
Logical Low Level	I_{OUT} = 25µA			V_{SS}–5.0	V
$\overline{D}$ and CP Outputs					
Logical High Level	$V_{DD} = V_{SS}$ –6.5V, $V_{OUT} = V_{SS}$ –2.0V	–220			µA
	$V_{DD} = V_{SS}$ –9.5V, $V_{OUT} = V_{SS}$ –5.0V			–1100	µA
Logical Low Level	$V_{DD} = V_{SS}$ –9.5V, $V_{OUT} = V_{DD}$ +0.8V	100			µA

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time	*(Figure 2)*	0.53		3.3	ms
Digit Time	*(Figure 2)*	58		367	µs
Interdigit Blanking Time (Segment Outputs)	*(Figure 2)*		4.0		µs
CP and $\overline{D}$ Transition Times					
High to Low	$V_{DD} = V_{SS}$ –6.5V		5	12	µs
Low to High	C_{LOAD} = 50 pF		0.75	1.5	µs
Ready Transition Times					
High to Low	$V_{DD} = V_{SS}$ –6.5		5	20	µs
Low to High	C_{LOAD} = 50 pF		2.0	4.0	µs
Keyboard Scan Inputs High to Low					
Low-to-High Transition Time After Key Release	C_{LOAD} = 100 pF		4.0		µs
Key Bounce-Out Stability Time (The time a keyboard scan input must be continuously lower than the maximum logical low level to be accepted as a key closure, or higher than the minimum logical high level to be accepted as a key release.)		6.36		39.6	ms
Display Cutoff Time (The time after the last valid key closure at which the 7 most-significant bits will be blanked.)			25		seconds
Worst Case Calculation Time				200	word times

FUNCTIONAL DESCRIPTION

The MM5791 is a calculator chip which contains four data registers: (1) entry, (2) accumulator, (3) working and (4) memory, each consisting of 8 digits, sign, and decimal point. The entry register is always displayed. It contains digit entries from the keyboard, and results of all functions except M+ and M–. The accumulator is used in all arithmetic functions and stores a copy of the entry register on all results. This allows another number to be entered without losing an intermediate result. Multiply and divide requires three registers to perform the function and save the divisor, or multiplier. The working register is provided to perform these functions in conjunction with the entry and accumulator registers.

The memory register is used only to store a number to be used later. It is fully protected during all operations, and is only modified by depressing a "MS," "M+," or "M–" key. Power on clears all of the registers including the memory register.

The MM5791 performs the "+," "–," "x" and "÷" functions using algebraic notation. This requires the use of a mode register and a terminate flag. The mode register directs the machine to the proper function (add, subtract, multiply or divide) with each new key entry. After the function has been performed, the key entered is used to modify the mode register.

The terminate flag is set on "=" and sometimes on "%" and "C." This signifies the end of the problem. The MM5791 allows for full floating entries and intermediate results.

If the terminate flag is set, a "+," "–," "x" or "÷" key signals the beginning of a new problem. The number being displayed is copied into the accumulator register and the mode register assumes the mode of the key entered. The terminate flag is always reset by the "+," "–," "x" and "÷" keys.

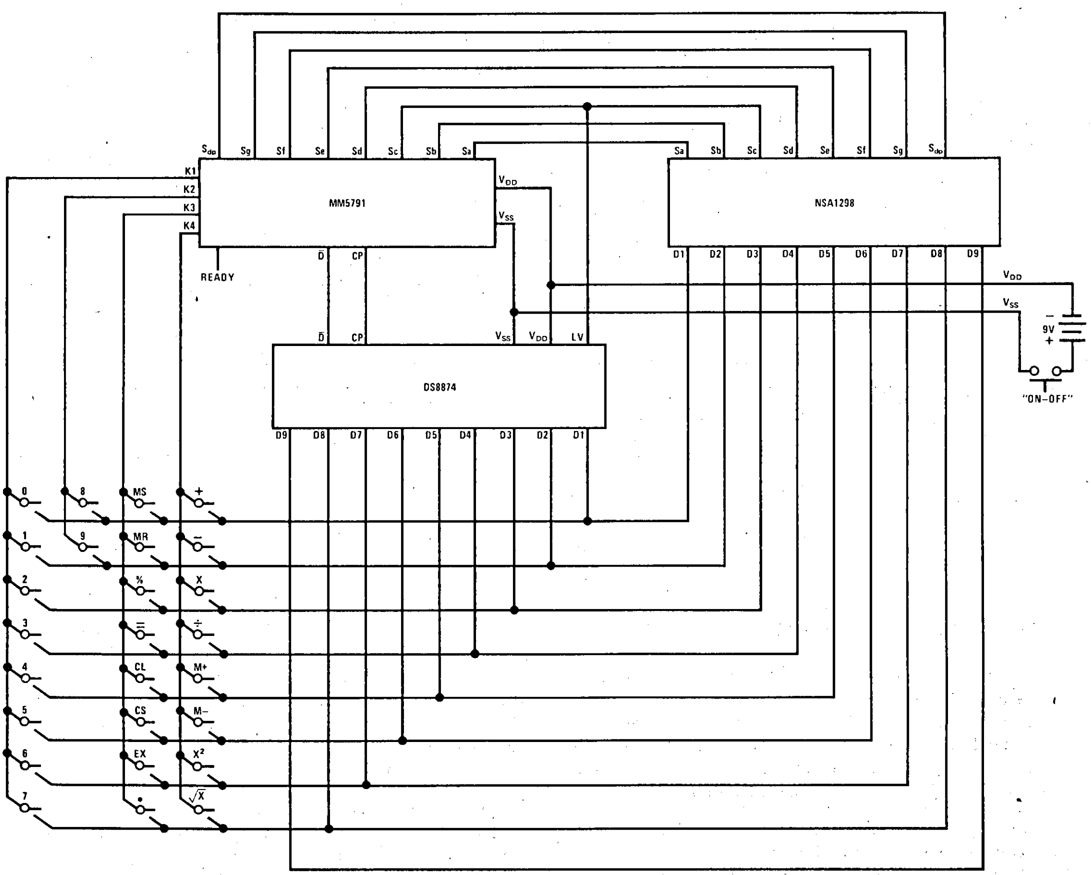


FIGURE 1. Complete Calculator Schematic

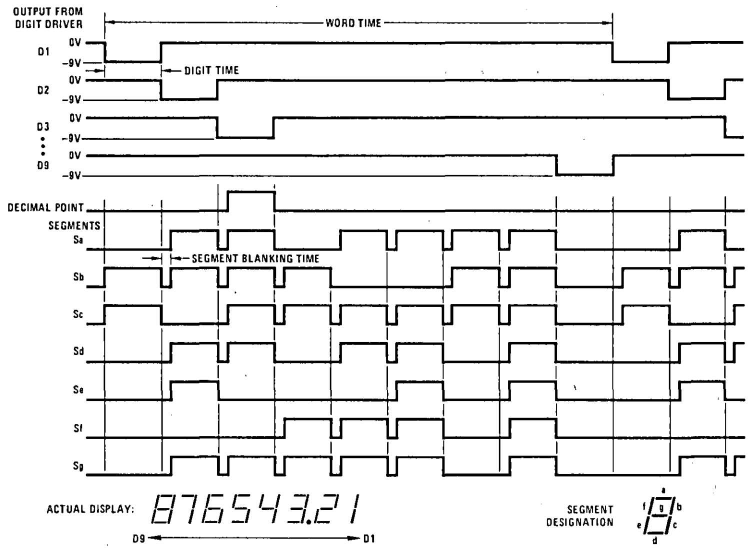


FIGURE 2. Display Timing

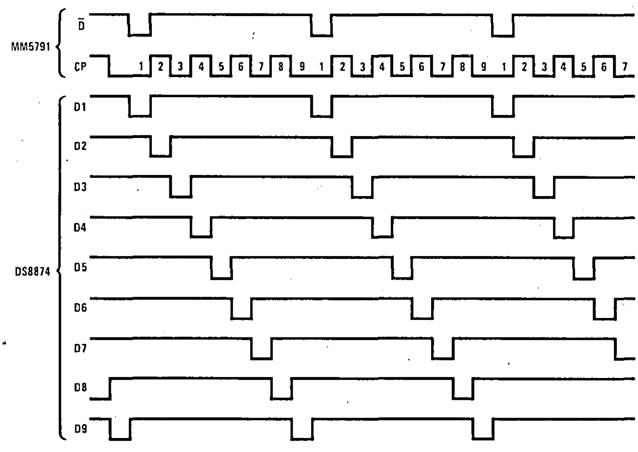


FIGURE 3. Digit Timing

OPERATION IN THE ADD AND SUBTRACT MODE

If the terminate flag is set, an "=" key will result in a constant add/subtract. The number in the accumulator will be added to (or subtracted from) the number being displayed. The result is right-justified and displayed in the entry register. Accumulator and mode registers are not altered, allowing for constant operations.

If the terminate flag is not set and a number has been entered from the keyboard, or memory register, a "+," "−," "x" or "÷" key will result in an addition or subtraction. The entry register will be added to or subtracted from the accumulator and the new running total will be displayed in the entry register and copied into the accumulator register. The mode will be altered according to which key is entered.

If the terminate flag is not set, and a number has not been entered from the keyboard, or memory, a "+," "−," "x" "÷" key will only change the mode register to the new key entry.

If the terminate flag is not set, an "=" key will add/subtract the number being displayed to/from the number in the accumulator register. The number being displayed is transferred to the accumulator, and the result of the operation is displayed in the entry register. The terminate flag is set, conditioning the calculator for constant, add/subtract operation. The number being displayed previous to the "=" key is stored in the accumulator as the constant.

Operation of the "%" key in add/subtract mode, with the terminate flag reset, will multiply the accumulator by the last entry, divide the result by 100, and display it in the entry register. The mode register remains as it was in the add or subtract mode. All of the above is required to perform the percent add on or discount problems. Depression of an "=" key after the "%" key will either tax or discount the original number as a function of the mode register and the last entry.

Operation of the "%" key in add/subtract mode, with the terminate flag set, will shift the decimal point of the number being displayed two places to the left and copy it into the accumulator register. The mode is set to multiply and the terminate flag remains set.

OPERATION IN THE MULTIPLY MODE

If the terminate flag is set, an "=" key will result in a constant multiply operation. The number being displayed is multiplied by the constant stored in the accumulator register. The result is displayed in the entry register and the accumulator and mode registers are not altered, allowing for constant operation. Repeated depressions of the "=" key can be used to raise a number to an integer power, i.e., "C," "C," "5.2," "x," "=," "=," "=," computes 5.2^4.

The constant in multiplication, as well as in addition, subtraction and division is the last number entered. For the sequence: "C," "C," "3," "÷," "4," "x," "2," "=" the constant multiplier for future problems is 2.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the display will be multiplied by the contents of the accumulator, and the results will be displayed in the entry register. The number previously in the entry register is stored in the accumulator register and the terminate flag is set.

If the terminate flag is not set, and a number has been entered from the keyboard or memory register, a "+," "–," "x" or "÷" key will result in a multiplication. The number being displayed will be multiplied by the number residing in the accumulator register. The result will be copied into the accumulator and displayed in the entry register. The mode register is up-dated as a function of the key depressed.

Operation of the "%" key while in multiply mode looks exactly the same as an "=" key except the decimal point of the display is shifted two positions to the left before the multiplication takes place.

OPERATION IN THE DIVIDE MODE

If the terminate flag is set, an "=" key will result in constant divide operation. The number being displayed is divided by the constant stored in the accumulator register. The accumulator and mode registers are not altered allowing for constant operations. Repeated depressions of the "=" key will result in repeated divisions by the constant. Thus, it is possible to raise a number to a negative integer power using the sequence: "C," "C," "1," "÷," "No.," "=," "=," etc.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the accumulator register will be divided by the number being displayed. The result is transferred to the entry register and displayed. The terminate flag is set and the divisor is stored in the accumulator register.

If the terminate flag is not set, a "+," "–," "x" or "÷" key will result in a division. The number in the accumulator register will be divided by the number being displayed. The results are displayed in the entry register, and a copy of the result is stored in the accumulator. The mode register is modified to reflect the latest key entry.

Operation of the "%" key while in divide mode looks exactly the same as the "=" key except the decimal point of the display is shifted two positions to the left before division takes place.

ERROR CONDITIONS

If any of the operations mentioned above generates a number larger than 9999 9999, an error will occur. An error is indicated by displaying the eight most significant digits and sign with all nine decimal points. The first depression of the "C" key will clear the error condition, and all registers except the memory register.

It is not possible to generate an error during number entry. The ninth and subsequent digits entered are ignored.

DISPLAY TURNOFF AND LEADING ZERO SUPPRESSION

In order to conserve battery power, the MM5791 blanks leading zeros and turns off all but the least significant digit, decimal point and sign after 25 seconds (typical) of no activity. Once the display turns off, any key depression will turn it back on and perform the function indicated. Two depressions of the "CS" key will turn on the display with no change to the machine. If Reset Display is hard-wired to V_{DD}, the display will never turn off.

POWER-ON CONDITION

The MM5791 has an internal power-on clear circuit which clears all registers to zero, places the mode to add and sets the terminate flag. A zero and decimal point are displayed.

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5791 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3 or K4 is forced more negative than the Logical Low Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after eleven word times if the Key Input is still at a Logical Low Level. As long as the key is held down (and the Key Input remains low) no further entry is allowed. When the Key Input changes to a Logical High Level, the internal counter starts an eleven word timeout for key release. During both, entry and release timeouts, the Key Inputs are sampled every word time for valid levels. If they are found invalid, the counter is reset and the calculator resumes scanning the keyboard.

READY SIGNAL OPERATIONS

The Ready signal indicates calculator status. When the calculator is in an "idle" state, the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the timeout is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 5 and 6.* It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

TEST FEATURES

Several features have been designed into the MM5791 to facilitate testing. One is to allow the key debounce timing to be modified, and the second performs a "segment test" function which turns on all segments for all digit times, with no interdigit blanking. The key bounce time can be reduced from eleven word times to one if a key closure is made between D9 and K2. Similarly the "Segment Test" occurs when a key closure is made between D9 and K3. Closures for test operations are not debounced, and also may occur simultaneously with normal key closures if diodes are used to isolate the D-Lines from each other. The test features are active for every word time the Test switch closure is maintained. These test matrix entries are isolated internally from the normal calculator keys, allowing simultaneous entry of "test" keys and "calculator" keys.

FUNCTION OF KEYS

Some of the keys operate differently when in the data or number entry condition. The MM5791 switches to entry condition when entering numbers and leaves this condition after most function keys. The following paragraphs discuss each of the keys on a full keyboard and the action taken when they are depressed. The earlier paragraphs which discussed the action of "+," "−," "x," "÷" and "%" keys and the examples given in later sections will aid in further explaining these actions.

Clear Key, "CE/C"

While in the number entry condition, one depression will clear the entry register to zero and recall the accumulator for display. The machine then leaves the number entry state.

If the error condition is displayed, one depression will clear the error, and all registers except the memory register. The machine could not be in the number entry condition with the error flag set.

If the error flag is not set and the machine is not in the number entry condition, one depression of "CE/C" key will clear the entry and accumulator registers. It also places the machine in the add mode and sets the terminate flag. The memory register remains unchanged.

Number Keys 0-9

If *not* in the number entry condition, a number key will clear the display and then enter the value of the key into the LSD. The digits are displayed as they are entered and the machine assumes the number entry condition.

If in the number entry condition, the entry register is shifted left one position and the key depressed is entered into the LSD. If there is a number in the most significant digit position (9th) the entry register is then shifted right one position and the entry is lost.

Square Root Key, "$\sqrt{\ }$"

The square root key extracts the square root of the absolute value of the number being displayed in the entry register.

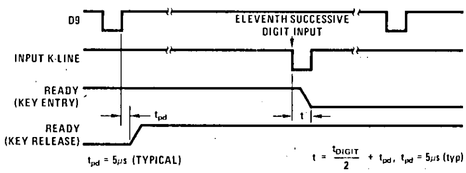


FIGURE 5. Ready Timing

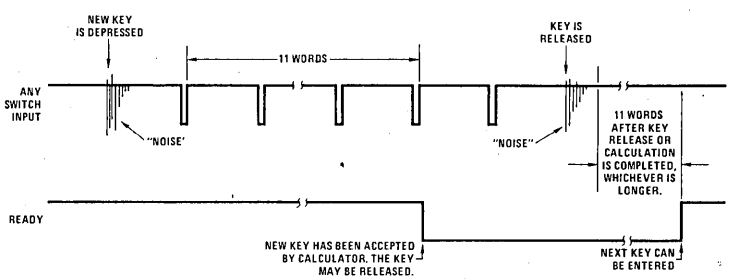


FIGURE 6. Functional Description of Ready Signal and Key Entry

The mode of the calculator remains unchanged. This enables square root operations in the middle of chain calculations. For example:

KEY	DISPLAY	KEY	DISPLAY	KEY	DISPLAY
A	A	A	A	11	11
$\sqrt{\ }$	$\sqrt{A}$	X	A	+	11.
+	$\sqrt{A}$	B	B	5	5
B	B	$\sqrt{\ }$	$\sqrt{B}$	=	16.
$\sqrt{\ }$	$\sqrt{B}$	=	$A\sqrt{B}$	$\sqrt{\ }$	4.
=	$\sqrt{A}+\sqrt{B}$			6	6.
				=	11
				9	9
				$\sqrt{\ }$	3.
				=	8.

Square

Depression of the "Square" key copies the number being displayed into the accumulator register, and performs a multiplication. On completion of the square operation, the results are displayed in the entry register, the original number is stored in the accumulator and the mode of the calculator is unchanged. Entering a number to start a new entry will first clear the entry register.

Memory Plus Key, "M+"

When the "M+" key is depressed, the number being displayed is added to the contents of the memory and the results, providing there is no overflow, are placed in the memory. The calculator will be out of the data entry mode.

If an overflow occurs, the contents of the memory are *not* altered. The display shows the eight most significant digits and sign of the results with all nine decimal points.

Memory Minus Key, "M–"

This key operates like the "M+" key only the displayed number is subtracted from memory.

Plus, Minus, Multiply and Divide Keys, "+," "–," "x," "÷"

These keys terminate a number entry, complete the operation designated by the mode register and update the mode register for the next operation. A more detailed explanation of these keys is found in the description of modes.

Equal Key, "="

This key terminates a number entry, complete the operation designated by the mode register and sets the terminate flag.

Percent Key, "%"

Following a clear-all operation or a number entry proceeded by a clear all operation, this key shifts the decimal point of the number being displayed two places to the left, copies it into the accumulating register and establishes the multiply mode.

While in multiply or divide mode, this key shifts the displayed decimal point two places to the left, completes the multiplication or division and sets the terminate flag.

In add or subtract mode, this key shifts the displayed decimal point two places to the left, multiplies the display times the accumulating register, places the product in the entry register and leaves the accumulator register and mode register undisturbed. This permits automatic calculation of net by depression of the "=" key. The terminate flag is not altered.

SAMPLE PROBLEMS

1. Simple addition or subtraction

KEYS	DISPLAY	COMMENTS
C	0	
3	3	Start addition problem
+	3.	Sets add mode
2	2	
+	5.	Completes addition, sets add mode
–	5.	Sets subtraction mode
4.355	4.3 5 5	
=	0.6 4 5	Completes subtraction. Sets mode terminal
+	0.6 4 5	Sets mode terminal. Sets add mode, resets
3.25	3.2 5	Starts Digit Entry
CS	–3.2 5	Changes Sign
4	–3.2 5 4	Continues Digit Entry
+	–2.6 0 9	Completes signed addition, sets add mode
1	1	
=	–1.6 0 9	Completes signed addition, sets terminate mode

2. Constant addition or subtraction (second factor constant)

KEYS	DISPLAY	COMMENTS
3	3	
–	3.	Sets subtract mode
2	2	
+	1.	Completes subtraction, sets Add mode
6	6	
=	7.	Completes addition, saves (6) as constant, sets terminate mode
.5	.5	
=	6.5	Completes constant addition constant=6
7	7	
–	7.	Sets subtraction mode, resets terminate mode

2. Constant addition or subtraction (second factor constant) (continued)

KEYS	DISPLAY	COMMENTS
3	3	
=	4.	Completes subtraction, sets terminate mode, saves 3 as a constant
8	8	
EX	3.	Exchanges entry, and constant
=	−5.	Completes subtraction constant = .8
9	9	
=	1.	Completes subtraction constant = 8

3. Simple multiplication

KEYS	DISPLAY	COMMENTS
3.1	3.1	Start multiplication problem
X	3.1	Sets multiply mode
6	6	
=	1 8.6	Completes multiplication, sets terminate mode

4. Chain multiplication

KEYS	DISPLAY	COMMENTS
3	3	
+	3	Sets add mode
4	4	
X	7.	Completes addition, sets multiply mode
6	6	
−	4 2.	Completes multiplication, sets subtract mode
2	2	
=	4 0.	Completes subtraction, sets terminate mode, saves 2 as constant

5. Constant multiplication

KEYS	DISPLAY	COMMENTS
3	3	
X	3.	Sets multiply mode
4	4	
=	.1 2.	Completes multiplication, saves '4' as constant, sets termination mode

5. Constant multiplication (continued)

KEYS	DISPLAY	COMMENTS
6	6	
=	2 4.	Completes constant multiplication, constant = 4
3	3	
−	3.	Sets subtract mode, resets termination
4.5	4.5	
X	−1.5	Completes subtraction, sets multiply mode
8	8	
CS	−8	Changes sign
=	1 2.	Completes multiplication '−8' as constant, sets termination mode
EX	−8.	Exchanges entry register, and constant
CS	8.	
3	3	
=	3 6.	Completes constant multiplication constant = 12
=	4 3 2.	Completes constant multiplication constant = 12
3	3	
X	3.	Sets multiply mode, resets termination mode
+	3.	Sets add mode. Second function key only modifies mode
−	3.	Sets subtract mode
X	3.	Sets multiply mode
=	9.	Completes multiplication. Sets termination mode

6. Simple division

KEYS	DISPLAY	COMMENTS
4	4	
÷	4.	
3	3	
CS	−3	
=	−1.3 3 3 3 3 3 3	

7. Chain division

KEYS	DISPLAY	COMMENTS
3	3	
÷	3.	
8	8	
+	0.3 7 5	
2	2	
X	2.3 7 5	
3.1	3.1	

7. Chain division (continued)

KEYS	DISPLAY	COMMENTS
÷	7.3625	
6	6	
=	1.2270833	

8. Constant division

KEYS	DISPLAY	COMMENTS
6	6	
÷	6.	
2	2	
=	3.	
=	1.5	
15	15	
−	15.	
2	2	
X	13.	
8.3	8.3	
÷	107.9	
3	3	
CS	−3	
EX	107.9	
=	−.0278035 2	
EX	107.9	
CS	−107.9	
EX	−.0278035 2	
608.7	608.7	
=	−5.6413345	

9. Add on and discount problems

KEYS	DISPLAY	COMMENTS
695.99	695.99	
−	695.99	
20	20	
%	139.198	
=	556.792	
+	556.792	
6	6	
%	33.40752	
=	590.19952	
17.95	17.95	
−	17.95	
15	15	
%	2.6925	
+	15.2575	
6	6	
%	0.91545	
=	16.17295	

10. Percent in multiplication and division

KEYS	DISPLAY	COMMENTS
308	308	
X	308.	
5	5	
%	15.4	

10. Percent in multiplication and division (continued)

KEYS	DISPLAY	COMMENTS
500	500	
÷	500.	
4	4	
%	12500.	

11. Memory operations

KEYS	DISPLAY	COMMENTS
6	6	
M+	6.	Memory indicator is activated
3	3	
+	3.	
2	2	
M−	2.	
=	5.	
MR	4.	
3.678	3.678	
CS	−3.678	
M+	−3.678	
X	−3.678	
5	5	
M−	5.	
=	−18.39	
MR	−4.678	
5	5	
MS	5.	
3	3	
X	3.	
4	4	
X	12.	
MR	5.	
=	60.	
0	0	
MS	0.	Memory indicator turned off when contents equal zero

12. Square root problems

KEYS	DISPLAY	COMMENTS
3	3	
$\sqrt{}$	1.7320508	
+	1.7320508	
4	4	
$\sqrt{}$	2.	
=	3.7320508	
7	7	
+	7.	
8	8	
=	15.	
$\sqrt{}$	3.8729833	

13. Square problems

KEYS	DISPLAY	COMMENTS
72	72	
X^2	5184.	

MM5794 seven-function, accumulating memory, vacuum fluorescent display calculator

general description

The single-chip MM5794 offers a seven-function, accumulating memory MOS/LSI calculator device capable of directly driving 8-digit vacuum-fluorescent displays. A complete calculator as shown in *Figure 1* requires only the MM5794, a keyboard, vacuum fluorescent display and an appropriate power supply.

Keyboard decoding and key debounce circuitry, all clocks and timing generation, power-on clear and 7-segment output display decoding are included on-chip and require no external components. Segments and digits can be driven directly from the MM5794. The left-most, or 9th digit is used to indicate memory in use or the negative sign of an eight digit number.

Leading zero suppression and a floating negative sign allow convenient reading of the display and conserves power. Typical current drain of a complete calculator displaying five "5's" is 30 mA.

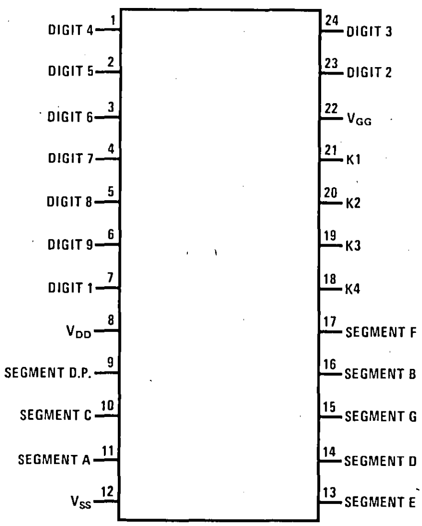
features

- Full 8-digit capacity
- 7-functions (+, −, x, ÷, x^2, $\sqrt{x}$, %)
- Convenient algebraic notation
- Fully protected accumulating memory (M+, M−)
- Automatic constant independent of memory
- Floating decimal input and output format
- Power-on clear*
- On-chip oscillator*
- Low system cost
- Direct segment and digit drive of fluorescent displays
- Memory in-use indicator

*Requires no external components.

connection diagram

Dual-In-Line Package

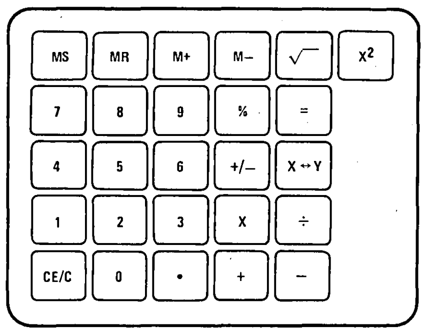


TOP VIEW

Order Number MM5794N
See Package 22

keyboard outline

Typical Keyboard



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} Except V_{GG} (All Other Pins Connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Voltage at V_{GG} Relative to V_{SS}	V_{SS} + 0.3V to V_{SS} − 35V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

$6.5 \leq V_{SS} - V_{DD} \leq 9.8V$
$V_{SS} - V_{GG} \leq 32V$

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current					
I_{DD}	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		8	15	mA
I_{GG}	$V_{GG} = V_{SS} - 32V$		500		μA
Keyboard Scan Input Levels (K1–K4)					
Logical High Level (V_{IH})		V_{SS}−7.0		V_{SS}	V
Logical Low Level (V_{IL})		V_{GG}		V_{SS}−22	V
Source Current, (Segments)	$T_A = 25°C$				
I_{OH}	$V_{OUT} = V_{SS} - 4V$, $V_{DD} = V_{SS} - 6.5V$			−0.6	mA
I_{OL}	$V_{OUT} = V_{SS} - 35V$			10	μA
Digit Outputs					
Logical High Level	$V_{GG} = V_{SS} - 32V$, $V_{OUT} = V_{SS} - 5.0V$			−3.5	mA
	$V_{GG} = V_{SS} - 25V$, $V_{OUT} = V_{SS} - 5.0V$			−2.2	mA
Logical Low Level	$V_{DD} = V_{SS} - 9.5V$, $V_{OUT} = V_{GG} = V_{SS} - 35V$			10	μA

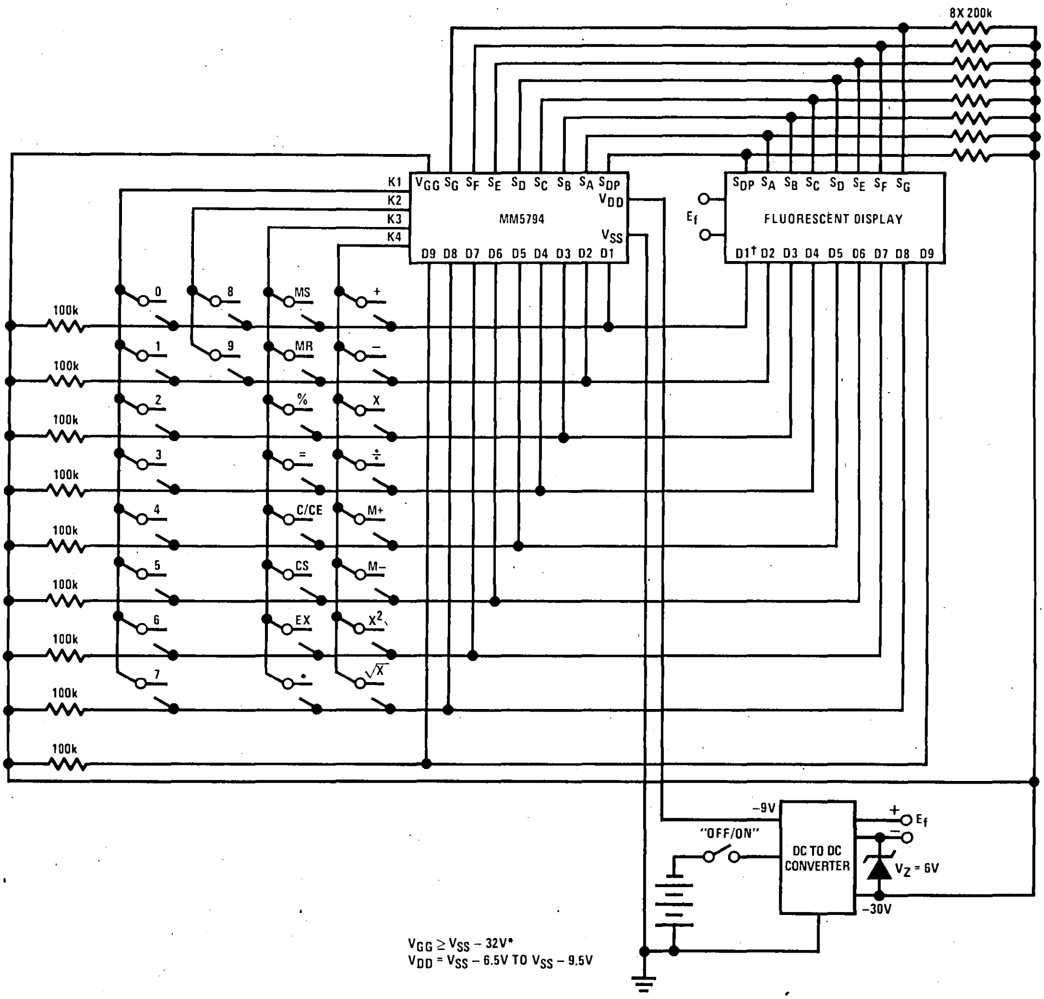
ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time	*(Figure 2)*	0.53		3.3	ms
Digit Time	*(Figure 2)*	58		367	μs
Interdigit Blanking Time (Segment and Digit Outputs)	*(Figure 2)*	14.5	20		μs
Digit Transition Times	100k Resistor to V_{GG}				
High to Low	$V_{DD} = V_{SS} - 6.5V$		20		μs
Low to High	C_{LOAD} = 100 pF			4	μs
Ready Transition Times					
High to Low	$V_{DD} = V_{SS} - 6.5$		5	20	μs
Low to High	C_{LOAD} = 50 pF		2.0	4.0	μs
Keyboard Scan Inputs Transition Times	$V_{GG} = V_{SS} - 35$				
High to Low (After Key Release)	C_{LOAD} = 50 pF			100	μs
Low to High (After Key Release)	C_{LOAD} = 100 pF			4	μs
Key Bounce-Out Stability Time (The time a keyboard scan input must be continuously lower than the maximum logical low level to be accepted as a key closure, or higher than the minimum logical high level to be accepted as a key release.)		6.36		39.6	ms
Worst Case Calculation Time				200	word times

FUNCTIONAL DESCRIPTION

The MM5794 is a calculator chip which contains four data registers: (1) entry, (2) accumulator, (3) working and (4) memory, each consisting of 8 digits, sign, and decimal point. The entry register is always displayed. It contains digit entries from the keyboard, and results of all functions except M+ and M–. The accumulator is used in all arithmetic functions and stores a copy of the entry register on all results. This allows another number to be entered without losing an intermediate result. Multiply and divide require three registers to perform the function and save the divisor, or multiplier. The working register is provided to perform these functions in conjunction with the entry and accumulator registers.

The memory register is used only to store a number to be used later. It is fully protected during all operations, and is only modified by depressing a "MS," "M+," or "M–" key. Power on clears all of the registers including the memory register.



*$V_{SS} - V_{DD}$ must be as specified in this data sheet (6.5–9.5) but $V_{SS} - V_{GG}$, E_f and V_Z are determined by the fluorescent display specifications.
† D1 is the right-most display digit, also see *Figure 2*.

FIGURE 1. Complete Calculator Schematic

The MM5794 performs the "+," "−," "x" and "÷" functions using algebraic notation. This requires the use of a mode register and a terminate flag. The mode register directs the machine to the proper function (add, subtract, multiply or divide) with each new key entry. After the function has been performed, the key entered is used to modify the mode register.

The terminate flag is set on "=" and sometimes on "%" and "C/CE." This signifies the end of the problem. The MM5794 allows for full floating entries and results.

If the terminate flag is set, a "+," "−," "x" or "÷" key signals the beginning of a new problem. The number being displayed is copied into the accumulator register and the mode register assumes the mode of the key entered. The terminate flag is always reset by the "+," "−," "x" and "÷" keys.

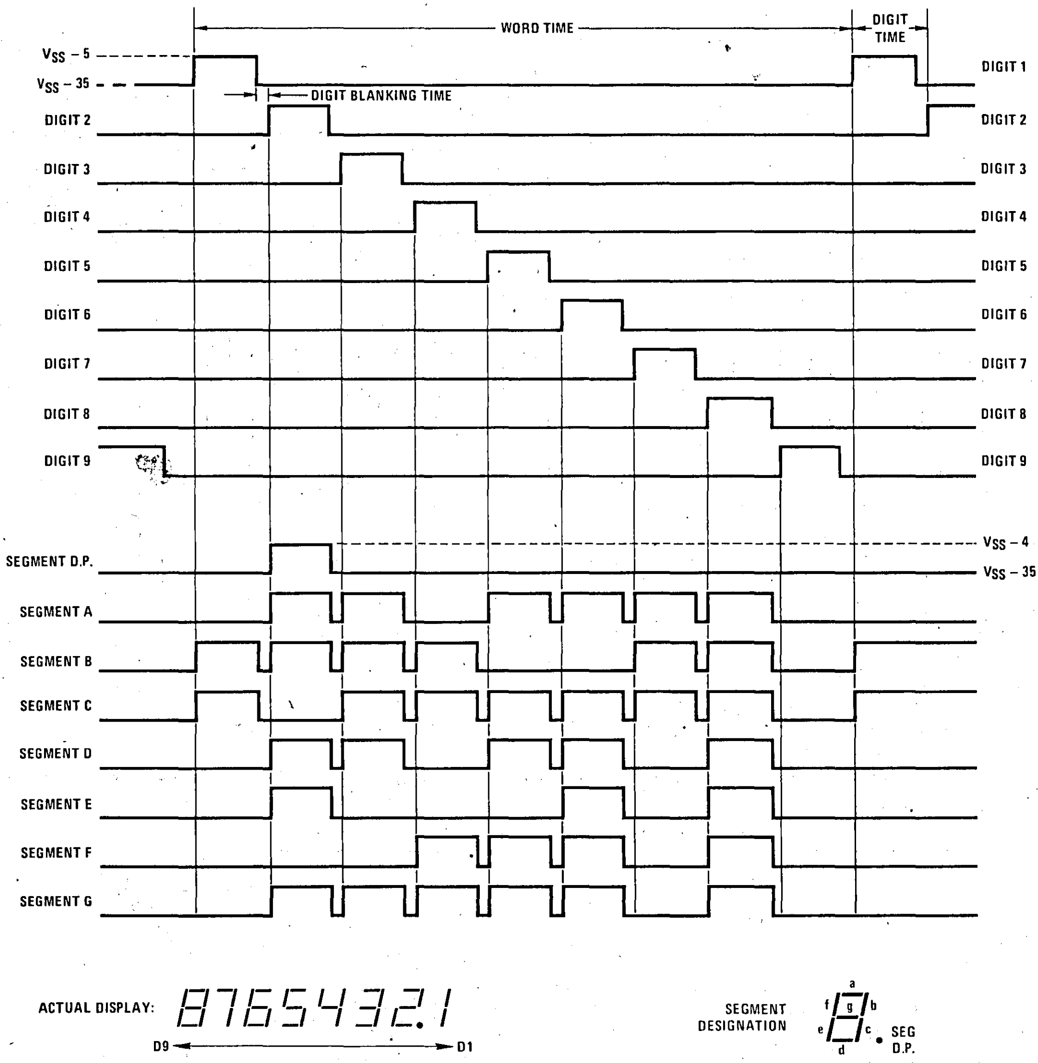


FIGURE 2. Display Timing

OPERATION IN THE ADD AND SUBTRACT MODE

If the terminate flag is set, an "=" key will result in a constant add/subtract. The number in the accumulator will be added to (or subtracted from) the number being displayed. The result is right-justified and displayed in the entry register. Accumulator and mode registers are not altered, allowing for constant operations.

If the terminate flag is not set and a number has been entered from the keyboard, or memory register, a "+," "–," "x" or "÷" key will result in an addition or subtraction. The entry register will be added to or subtracted from the accumulator and the new running total will be displayed in the entry register and copied into the accumulator register. The mode will be altered according to which key is entered.

If the terminate flag is not set, and a number has not been entered from the keyboard, or memory, a "+," "–," "x" "÷" key will only change the mode register to the new key entry.

If the terminate flag is not set, an "=" key will add/subtract the number being displayed to/from the number in the accumulator register. The number being displayed is transferred to the accumulator, and the result of the operation is displayed in the entry register. The terminate flag is set, conditioning the calculator for constant, add/subtract operation. The number being displayed previous to the "=" key is stored in the accumulator as the constant.

Operation of the "%" key in add/subtract mode, with the terminate flag reset, will multiply the accumulator by the last entry, divide the result by 100, and display it in the entry register. The mode register remains as it was in the add or subtract mode. All of the above is required to perform the percent add on or discount problems. Depression of an "=" key after the "%" key will either tax or discount the original number as a function of the mode register and the last entry.

Operation of the "%" key in add/subtract mode, with the terminate flag set, will shift the decimal point of the number being displayed two places to the left and copy it into the accumulator register. The mode is set to multiply and the terminate flag remains set.

OPERATION IN THE MULTIPLY MODE

If the terminate flag is set, an "=" key will result in a constant multiply operation. The number being displayed is multiplied by the constant stored in the accumulator register. The result is displayed in the entry register and the accumulator and mode registers are not altered, allowing for constant operation. Repeated depressions of the "=" key can be used to raise a number to an integer power, i.e., "C/CE," "C/CE," "5.2," "x," "=," "=," "=," computes 5.2^4.

The constant in multiplication, as well as in addition, subtraction and division is the last number entered. For the sequence: "C/CE," "C/CE," "3," "÷," "4," "x," "2," "=" the constant multiplier for future problems is 2.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the display will be multiplied by the contents of the accumulator, and the results will be displayed in the entry register. The number previously in the entry register is stored in the accumulator register and the terminate flag is set.

If the terminate flag is not set, and a number has been entered from the keyboard or memory register, a "+," "–," "x" or "÷" key will result in a multiplication. The number being displayed will be multiplied by the number residing in the accumulator register. The result will be copied into the accumulator and displayed in the entry register. The mode register is up-dated as a function of the key depressed.

Operation of the "%" key while in multiply mode looks exactly the same as an "=" key except the decimal point of the display is shifted two positions to the left before the multiplication takes place.

OPERATION IN THE DIVIDE MODE

If the terminate flag is set, an "=" key will result in constant divide operation. The number being displayed is divided by the constant stored in the accumulator register. The accumulator and mode registers are not altered allowing for constant operations. Repeated depressions of the "=" key will result in repeated divisions by the constant. Thus, it is possible to raise a number to a negative integer power using the sequence: "C/CE," "C/CE," "1," "÷," "No.," "=," "=," etc.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the accumulator register will be divided by the number being displayed. The result is transferred to the entry register and displayed. The terminate flag is set and the divisor is stored in the accumulator register.

If the terminate flag is not set, a "+," "–," "x" or "÷" key will result in a division. The number in the accumulator register will be divided by the number being displayed. The results are displayed in the entry register, and a copy of the result is stored in the accumulator. The mode register is modified to reflect the latest key entry.

Operation of the "%" key while in divide mode looks exactly the same as the "=" key except the decimal point of the display is shifted two positions to the left before division takes place.

ERROR CONDITIONS

If any of the operations mentioned above generates a number larger than 9999 9999, an error will occur. An error is indicated by displaying the eight most significant digits and sign with all nine decimal points. The first depression of the "C/CE" key will clear the error condition, and all registers except the memory register.

It is not possible to generate an error during number entry. The ninth and subsequent digits entered are ignored.

POWER-ON CONDITION

The MM5794 has an internal power-on clear circuit which clears all registers to zero, places the mode to add and sets the terminate flag. A zero and decimal point are displayed.

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5794 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3 or K4 is forced more positive than the Logical High Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after eleven word times if the Key Input is still at a Logical High Level. As long as the key is held down (and the Key Input remains high) no further entry is allowed. When the Key Input changes to a Logical Low Level, the internal counter starts an eleven word timeout for key release. During both, entry and release timeouts, the Key Inputs are sampled every word time for valid levels. If they are found invalid, the counter is reset and the calculator resumes scanning the keyboard.

TEST FEATURES

Several features have been designed into the MM5794 to facilitate testing. One is to allow the key debounce timing to be modified, and the second performs a "segment test" function which turns on all segments for all digit times, with no interdigit blanking. The key bounce time can be reduced from eleven word times to one if a key closure is made between D9 and K2. "Segment Test" occurs when K3 is connected to D9. Closures for test operations are not debounced, and also may occur simultaneously with normal key closures if diodes are used to isolate the D-Lines from each other. The test features are active for every word time the Test switch closure is maintained. These test matrix entries are isolated internally from the normal calculator keys, allowing simultaneous entry of "test" keys and "calculator" keys, except for K3 keys during "Segment Test."

FUNCTION OF KEYS

Some of the keys operate differently when in the data or number entry condition. The MM5794 switches to entry condition when entering numbers and leaves this condition after most function keys. The following paragraphs discuss each of the keys on a full keyboard and the action taken when they are depressed. The earlier paragraphs which discussed the action of "+," "−," "x," "÷" and "%" keys and the examples given in later sections will aid in further explaining these actions.

Clear Key, "CE/C"

While in the number entry condition, one depression will clear the entry register to zero and recall the accumulator for display. The machine then leaves the number entry state.

If the error condition is displayed, one depression will clear the error, and all registers except the memory register. The machine could not be in the number entry condition with the error flag set.

If the error flag is not set and the machine is not in the number entry condition, one depression of "CE/C" key will clear the entry and accumulator registers. It also places the machine in the add mode and sets the terminate flag. The memory register remains unchanged.

Number Keys 0-9

If *not* in the number entry condition, a number key will clear the display and then enter the value of the key into the LSD. The digits are displayed as they are entered and the machine assumes the number entry condition.

If in the number entry condition, the entry register is shifted left one position and the key depressed is entered into the LSD. If there is a number in the most significant digit position (9th) the entry register is then shifted right one position and the entry is lost.

Square Root Key, "$\sqrt{\ }$"

The square root key extracts the square root of the absolute value of the number being displayed in the entry register.

The mode of the calculator remains unchanged. This enables square root operations in the middle of chain calculations. For example:

KEY	DISPLAY	KEY	DISPLAY	KEY	DISPLAY
A	A	A	A	11	11
$\sqrt{\ }$	$\sqrt{A}$	X	A	+	11.
+	$\sqrt{A}$	B	B	5	5
B	B	$\sqrt{\ }$	$\sqrt{B}$	=	16.
$\sqrt{\ }$	$\sqrt{B}$	=	$A\sqrt{B}$	$\sqrt{\ }$	4.
=	$\sqrt{A}+\sqrt{B}$			6	6.
				=	11
				9	9
				$\sqrt{\ }$	3.
				=	8.

Square Key, "X^2"

Depression of the "Square" key copies the number being displayed into the accumulator register, and performs a multiplication. On completion of the square operation, the results are displayed in the entry register, the original number is stored in the accumulator and the mode of the calculator is unchanged. Entering a number to start a new entry will first clear the entry register.

Memory Save Key, "MS"

The "MS" key transfers the number being displayed to the memory register. The display remains unaltered.

Memory Recall Key, "MR"

The "MR" key recalls the number being stored in the memory register and displays it in the entry register. This number can then be used as a new number entry.

Memory Store Key, "MS"

The "MS" key transfers the number being displayed in the entry register to the memory register. The arithmetic status of the calculator is not changed.

Memory Plus Key, "M+"

When the "M+" key is depressed, the number being displayed is added to the contents of the memory and the results, providing there is no overflow, are placed in the memory. The calculator will be out of the data entry mode.

If an overflow occurs, the contents of the memory are *not* altered. The display shows the eight most significant digits and sign of the results with all nine decimal points.

Memory Minus Key, "M–"

This key operates like the "M+" key only the displayed number is subtracted from memory.

Plus, Minus, Multiply and Divide Keys, "+," "–," "x," "÷"

These keys terminate a number entry, complete the operation designated by the mode register and update the mode register for the next operation. A more detailed explanation of these keys is found in the description of modes.

Equal Key, "="

This key terminates a number entry, complete the operation designated by the mode register and sets the terminate flag.

Percent Key, "%"

Following a clear-all operation or a number entry proceeded by a clear all operation, this key shifts the decimal point of the number being displayed two places to the left, copies it into the accumulating register and establishes the multiply mode.

While in multiply or divide mode, this key shifts the displayed decimal point two places to the left, completes the multiplication or division and sets the terminate flag.

In add or subtract mode, this key shifts the displayed decimal point two places to the left, multiplies the display times the accumulating register, places the product in the entry register and leaves the accumulator register and mode register undisturbed. This permits automatic calculation of net by depression of the "=" key. The terminate flag is not altered.

SAMPLE PROBLEMS

1. Simple addition or subtraction

KEYS	DISPLAY	COMMENTS
C/CE	0	
3	3	Start addition problem

1. Simple addition or subtraction (continued)

KEYS	DISPLAY	COMMENTS
+	3.	Sets add mode
2	2	
+	5.	Completes addition, resets add mode
–	5.	Sets subtraction mode
4.355	4.3 5 5	
=	0.6 4 5	Completes subtraction. Sets terminate mode.
+	0.6 4 5	Sets add mode
3.25	3.2 5	Starts Digit Entry
CS	–3.2 5	Changes Sign
4	–3.2 5 4	Continues Digit Entry
+	–2.6 0 9	Completes signed addition, sets add mode
1	1	
=	–1.6 0 9	Completes signed addition, sets terminate mode

2. Constant addition or subtraction (second factor constant)

KEYS	DISPLAY	COMMENTS
3	3	
–	3.	Sets subtract mode
2	2	
+	1.	Completes subtraction, sets add mode
6	6	
=	7.	Completes addition, saves (6) as constant, sets terminate mode
.5	.5	
=	6.5	Completes constant addition constant=6
7	7	
–	7.	Sets subtraction mode, resets terminate mode
3	3	
=	4.	Completes subtraction, sets terminate mode, saves 3 as a constant
8	8	
EX	3.	Exchanges entry, and constant
=	–5.	Completes subtraction constant = .8
9	9	
=	1.	Completes subtraction constant = 8

3. Simple multiplication

KEYS	DISPLAY	COMMENTS
3.1	3.1	Start multiplication problem

3. Simple multiplication (continued)

KEYS	DISPLAY	COMMENTS
X	3.1	Sets multiply mode
6	6	
=	1 8.6	Completes multiplication, sets terminate mode

4. Chain multiplication

KEYS	DISPLAY	COMMENTS
3	3	
+	3	Sets add mode
4	4	
X	7.	Completes addition, sets multiply mode
6	6	
−	4 2.	Completes multiplication, sets subtract mode
2	2	
=	4 0.	Completes subtraction, sets terminate mode, saves 2 as constant

5. Constant multiplication

KEYS	DISPLAY	COMMENTS
3	3	
X	3.	Sets multiply mode
4	4	
=	1 2.	Completes multiplication, saves '4' as constant, sets termination mode
6	6	
=	2 4.	Completes constant multiplication, constant = 4
3	3	
−	3.	Sets subtract mode, resets termination
4.5	4.5	
X	−1.5	Completes subtraction, sets multiply mode
8	8	
CS	−8	Changes sign
=	1 2.	Completes multiplication '−8' as constant, sets termination mode
EX	−8.	Exchanges entry register, and constant
CS	8.	
3	3	
=	3 6.	Completes constant multiplication constant = 12

5. Constant multiplication (continued)

KEYS	DISPLAY	COMMENTS
=	4 3 2.	Completes constant multiplication constant = 12
3	3	
X	3.	Sets multiply mode, resets termination mode
+	3.	Sets add mode. Second function key only modifies mode
−	3.	Sets subtract mode
X	3.	Sets multiply mode
=	9.	Completes multiplication. Sets termination mode

6. Simple division

KEYS	DISPLAY	COMMENTS
4	4	
÷	4.	
3	3	
CS	−3	
=	−1.3 3 3 3 3 3 3	

7. Chain division

KEYS	DISPLAY	COMMENTS
3	3	
÷	3.	
8	8	
+	0.3 7 5	
2	2	
X	2.3 7 5	
3.1	3.1	
÷	7.3 6 2 5	
6	6	
=	1.2 2 7 0 8 3 3	

8. Constant division

KEYS	DISPLAY	COMMENTS
6	6	
÷	6.	
2	2	
=	3.	
=	1.5	
15	1 5	
−	1 5.	
2	2	
X	1 3.	
8.3	8.3	
÷	1 0 7.9	
3	3	
CS	−3	
EX	1 0 7.9	

8. Constant division (continued)

KEYS	DISPLAY	COMMENTS
=	−.0 2 7 8 0 3 5 2	
EX	1 0 7.9	
CS	−1 0 7.9	
EX	−.0 2 7 8 0 3 5 2	
608.7	6 0 8.7	
=	−5.6 4 1 3 3 4 5	

9. Add on and discount problems

KEYS	DISPLAY	COMMENTS
695.99	6 9 5.9 9	
−	6 9 5.9 9	
20	2 0	
%	1 3 9.1 9 8	
=	5 5 6.7 9 2	
+	5 5 6.7 9 2	
6	6	
%	3 3.4 0 7 5 2	
=	5 9 0.1 9 9 5 2	
17.95	1 7.9 5	
−	1 7.9 5	
15	1 5	
%	2.6 9 2 5	
+	1 5.2 5 7 5	
6	6	
%	0.9 1 5 4 5	
=	1 6.1 7 2 9 5	

10. Percent in multiplication and division

KEYS	DISPLAY	COMMENTS
308	3 0 8	
X	3 0 8.	
5	5	
%	1 5.4	
500	5 0 0	
÷	5 0 0.	
4	4	
%	1 2 5 0 0.	

11. Memory operations

KEYS	DISPLAY	COMMENTS
6	6	
M+	I 6.	Memory indicator is activated in left-most digit

11. Memory operations (continued)

KEYS	DISPLAY	COMMENTS
3	I 3	
+	I 3.	
2	I 2	
M−	I 2.	
=	I 5.	
MR	I 4.	
3.678	I 3.6 7 8	
CS	I −3.6 7 8	
M+	I −3.6 7 8	
X	I −3.6 7 8	
5	I 5	
M−	I 5.	
=	I −1 8.3 9	
MR	I −4.6 7 8	
5	I 5	
MS	I 5.	
3	I 3	
X	I 3.	
4	I 4	
X	I 1 2.	
MR	I 5.	
=	I 6 0.	
0	I 0	
MS	0.	Memory indicator turned off when contents equal zero

12. Square root problems

KEYS	DISPLAY	COMMENTS
3	3	
√	1.7 3 2 0 5 0 8	
+	1.7 3 2 0 5 0 8	
4	4	
√	2.	
=	3.7 3 2 0 5 0 8	
7	7	
+	7.	
8	8	
=	1 5.	
√	3.8 7 2 9 8 3 3	

13. Square problems

KEYS	DISPLAY	COMMENTS
72	7 2	
X^2	5 1 8 4.	

8

MM5795 seven-function, accumulating memory, vacuum fluorescent display calculator circuit

general description

The single-chip MM5795 offers a seven-function, accumulating memory MOS/LSI calculator device capable of directly driving 8-digit vacuum-fluorescent displays. A complete calculator as shown in *Figure 1* requires only the MM5795, a keyboard, vacuum fluorescent display and an appropriate power supply.

Keyboard decoding and key debounce circuitry, all clocks and timing generation, power-on clear and 7-segment output display decoding are included on-chip and require no external components. Segments and digits can be driven directly from the MM5795. The left-most, or 9th digit is used to indicate memory in use or the negative sign of an eight digit number.

Leading zero suppression and a floating negative sign allow convenient reading of the display and conserves power. Typical current drain of a complete calculator displaying five "5's" is 30 mA.

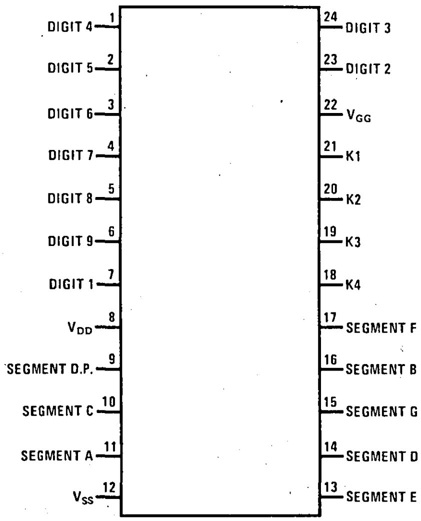
features

- Full 8-digit capacity
- 7-functions (+, −, x, ÷, x^2, $\sqrt{x}$, %)
- Convenient algebraic notation
- Fully protected accumulating memory (M+, M−)
- Automatic constant independent of memory
- Floating decimal input and output format
- Power-on clear*
- On-chip oscillator*
- Low system cost
- Direct segment and digit drive of fluorescent displays
- Memory in-use indicator

*Requires no external components.

connection diagram

Dual-In-Line Package

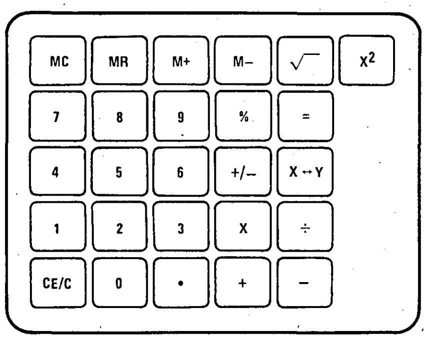


TOP VIEW

Order Number MM5795N
See Package 22

keyboard outline

Typical Keyboard



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} Except V_{GG} (All Other Pins Connected to V_{SS})	V_{SS} + 0.3V to V_{SS} − 12V
Voltage at V_{GG} Relative to V_{SS}	V_{SS} + 0.3V to V_{SS} − 35V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

$6.5 \le V_{SS} - V_{DD} \le 9.8V$

$V_{SS} - V_{GG} \le 32V$

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current					
I_{DD}	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		8	15	mA
I_{GG}	$V_{GG} = V_{SS} - 32V$		500		μA
Keyboard Scan Input Levels (K1–K4)					
Logical High Level (V_{IH})		V_{SS}−7.0		V_{SS}	V
Logical Low Level (V_{IL})		V_{GG}		V_{SS}−22	V
Source Current, (Segments)	$T_A = 25°C$				
I_{OH}	$V_{OUT} = V_{SS} - 4V$, $V_{DD} = V_{SS} - 6.5V$			−0.6	mA
I_{OL}	$V_{OUT} = V_{SS} - 35V$			10	μA
Digit Outputs					
Logical High Level	$V_{GG} = V_{SS} - 32V$, $V_{OUT} = V_{SS} - 5.0V$			−3.5	mA
	$V_{GG} = V_{SS} - 25V$, $V_{OUT} = V_{SS} - 5.0V$			−2.2	mA
Logical Low Level	$V_{DD} = V_{SS} - 9.5V$, $V_{OUT} = V_{GG} = V_{SS} - 35V$			10	μA

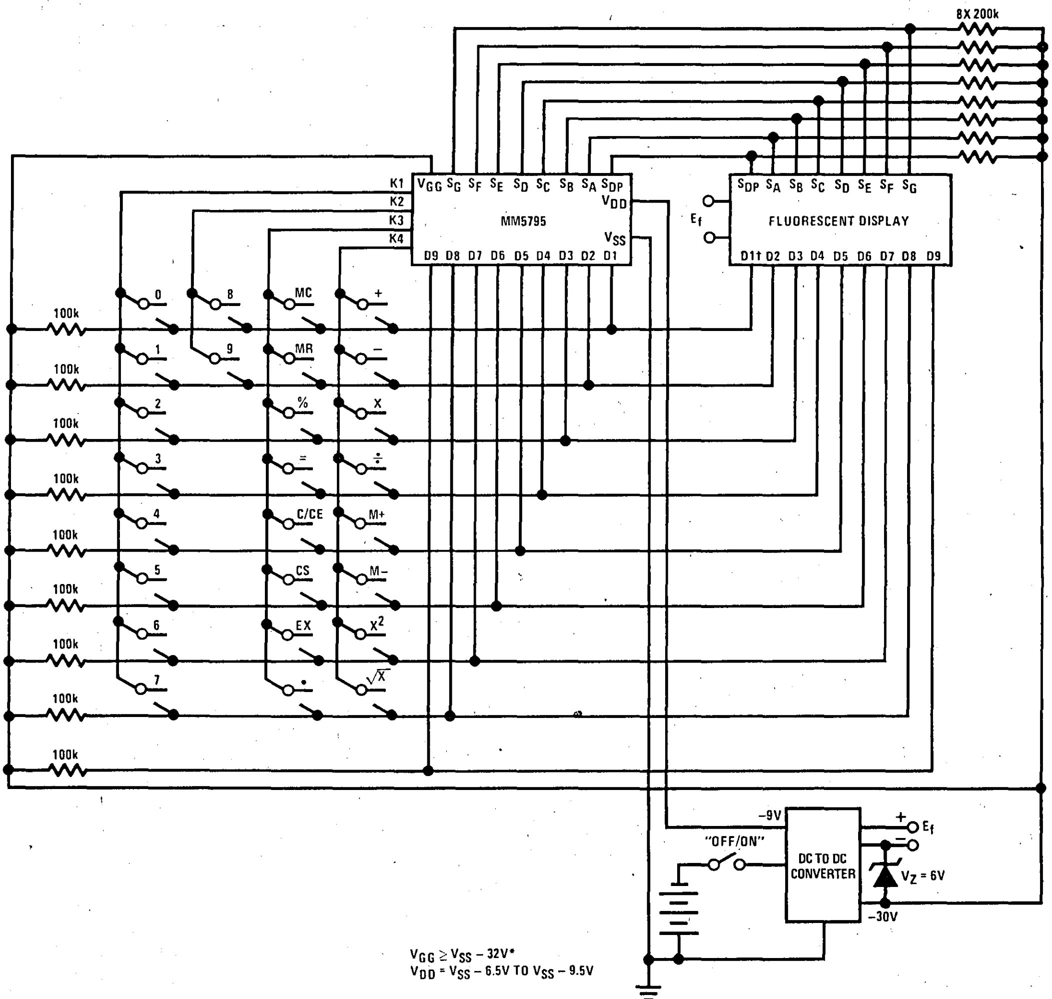
ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Word Time	*(Figure 2)*	0.53		3.3	ms
Digit Time	*(Figure 2)*	58		367	μs
Interdigit Blanking Time (Segment and Digit Outputs)	*(Figure 2)*	14.5	20		μs
Digit Transition Times	100k Resistor to V_{GG}				
High to Low	$V_{DD} = V_{SS}$ −6.5V		20		μs
Low to High	C_{LOAD} = 100 pF			4	μs
Ready Transition Times					
High to Low	$V_{DD} = V_{SS}$ −6.5		5	20	μs
Low to High	C_{LOAD} = 50 pF		2.0	4.0	μs
Keyboard Scan Inputs Transition Times	$V_{GG} = V_{SS}$ − 35				
High to Low (After Key Release)	C_{LOAD} = 50 pF			100	μs
Low-to-High (After Key Closure)	C_{LOAD} = 100 pF			4	μs
Key Bounce-Out Stability Time (The time a keyboard scan input must be continuously lower than the maximum logical low level to be accepted as a key closure, or higher than the minimum logical high level to be accepted as a key release.)		6.36		39.6	ms
Worst Case Calculation Time				200	word times

FUNCTIONAL DESCRIPTION

The MM5795 is a calculator chip which contains four data registers: (1) entry, (2) accumulator, (3) working and (4) memory, each consisting of 8 digits, sign, and decimal point. The entry register is always displayed. It contains digit entries from the keyboard, and results of all functions except M+ and M−. The accumulator is used in all arithmetic functions and stores a copy of the entry register on all results. This allows another number to be entered without losing an intermediate result. Multiply and divide require three registers to perform the function and save the divisor, or multiplier. The working register is provided to perform these functions in conjunction with the entry and accumulator registers.

The memory register is used only to store a number to be used later. It is fully protected during all operations, and is only modified by depressing an "MC," "M+," or "M−" key. Power on clears all of the registers including the memory register.



*$V_{SS} - V_{DD}$ must be as specified in this data sheet (6.5–9.5) but $V_{SS} - V_{GG}$, E_f and V_Z are determined by the fluorescent display specifications.
† D1 is the right-most display digit, also see *Figure 2.*

FIGURE 1. Complete Calculator Schematic

The MM5795 performs the "+," "–," "x" and "÷" functions using algebraic notation. This requires the use of a mode register and a terminate flag. The mode register directs the machine to the proper function (add, subtract, multiply or divide) with each new key entry. After the function has been performed, the key entered is used to modify the mode register.

The terminate flag is set on "=" and sometimes on "%" and "C/CE." This signifies the end of the problem. The MM5795 allows for full floating entries and results.

If the terminate flag is set, a "+," "–," "x" or "÷" key signals the beginning of a new problem. The number being displayed is copied into the accumulator register and the mode register assumes the mode of the key entered. The terminate flag is always reset by the "+," "–," "x" and "÷" keys.

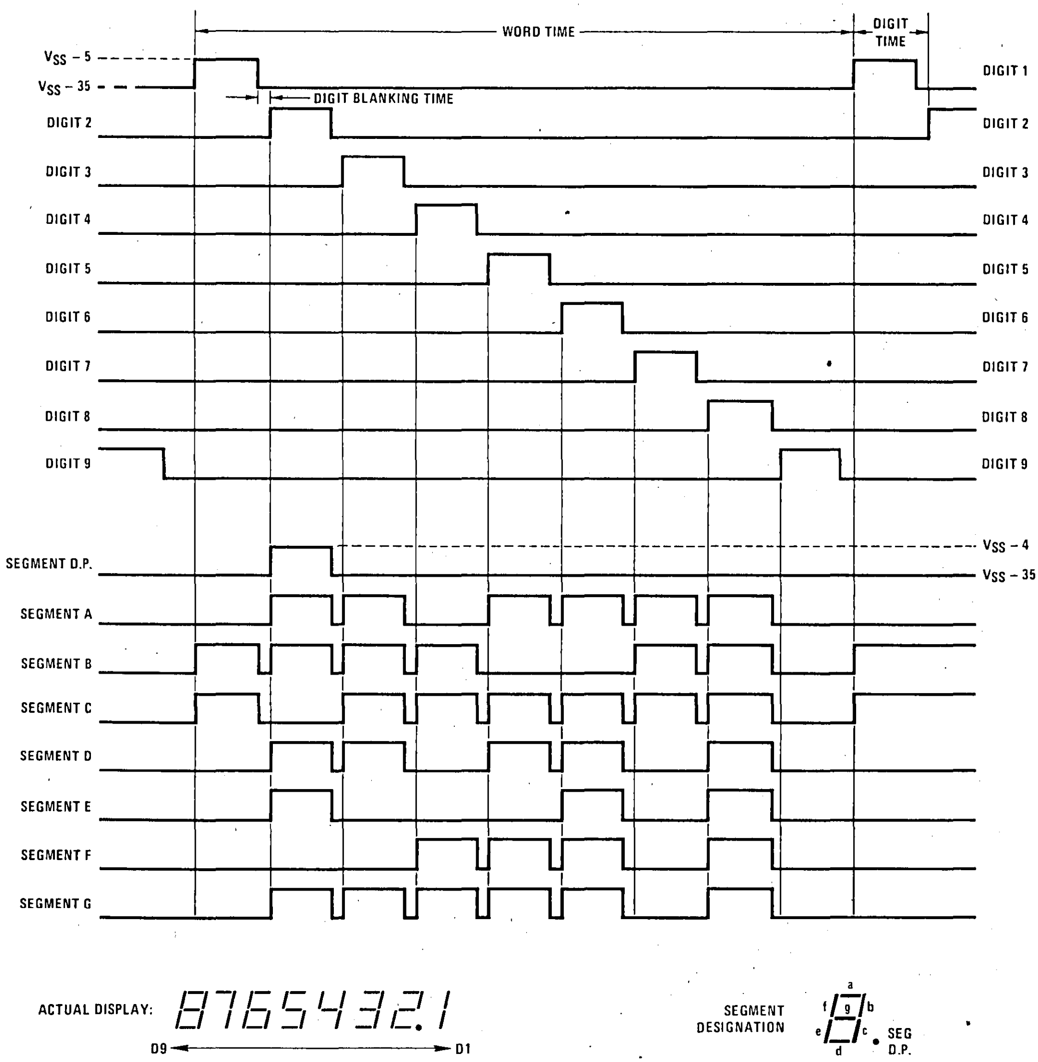


FIGURE 2. Display Timing

OPERATION IN THE ADD AND SUBTRACT MODE

If the terminate flag is set, an "=" key will result in a constant add/subtract. The number in the accumulator will be added to (or subtracted from) the number being displayed. The result is right-justified and displayed in the entry register. Accumulator and mode registers are not altered, allowing for constant operations.

If the terminate flag is not set and a number has been entered from the keyboard, or memory register, a "+," "–," "x" or "÷" key will result in an addition or subtraction. The entry register will be added to or subtracted from the accumulator and the new running total will be displayed in the entry register and copied into the accumulator register. The mode will be altered according to which key is entered.

If the terminate flag is not set, and a number has not been entered from the keyboard, or memory, a "+," "–," "x" "÷" key will only change the mode register to the new key entry.

If the terminate flag is not set, an "=" key will add/subtract the number being displayed to/from the number in the accumulator register. The number being displayed is transferred to the accumulator, and the result of the operation is displayed in the entry register. The terminate flag is set, conditioning the calculator for constant, add/subtract operation. The number being displayed previous to the "=" key is stored in the accumulator as the constant.

Operation of the "%" key in add/subtract mode, with the terminate flag reset, will multiply the accumulator by the last entry, divide the result by 100, and display it in the entry register. The mode register remains as it was in the add or subtract mode. All of the above is required to perform the percent add on or discount problems. Depression of an "=" key after the "%" key will either tax or discount the original number as a function of the mode register and the last entry.

Operation of the "%" key in add/subtract mode, with the terminate flag set, will shift the decimal point of the number being displayed two places to the left and copy it into the accumulator register. The mode is set to multiply and the terminate flag remains set.

OPERATION IN THE MULTIPLY MODE

If the terminate flag is set, an "=" key will result in a constant multiply operation. The number being displayed is multiplied by the constant stored in the accumulator register. The result is displayed in the entry register and the accumulator and mode registers are not altered, allowing for constant operation. Repeated depressions of the "=" key can be used to raise a number to an integer power, i.e., "C/CE," "C/CE," "5.2," "x," "=," "=," "=;" computes 5.2^4.

The constant in multiplication, as well as in addition, subtraction and division is the last number entered. For the sequence: "C/CE," "C/CE," "3," "÷," "4," "x," "2," "=" the constant multiplier for future problems is 2.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the display will be multiplied by the contents of the accumulator, and the results will be displayed in the entry register. The number previously in the entry register is stored in the accumulator register and the terminate flag is set.

If the terminate flag is not set, and a number has been entered from the keyboard or memory register, a "+," "–," "x" or "÷" key will result in a multiplication. The number being displayed will be multiplied by the number residing in the accumulator register. The result will be copied into the accumulator and displayed in the entry register. The mode register is up-dated as a function of the key depressed.

Operation of the "%" key while in multiply mode looks exactly the same as an "=" key except the decimal point of the display is shifted two positions to the left before the multiplication takes place.

OPERATION IN THE DIVIDE MODE

If the terminate flag is set, an "=" key will result in constant divide operation. The number being displayed is divided by the constant stored in the accumulator register. The accumulator and mode registers are not altered allowing for constant operations. Repeated depressions of the "=" key will result in repeated divisions by the constant. Thus, it is possible to raise a number to a negative integer power using the sequence: "C/CE," "C/CE," "1," "÷," "No.," "=," "=," etc.

If the terminate flag is not set, an "=" key will signal the end of a problem. The number in the accumulator register will be divided by the number being displayed. The result is transferred to the entry register and displayed. The terminate flag is set and the divisor is stored in the accumulator register.

If the terminate flag is not set, a "+," "–," "x" or "÷" key will result in a division. The number in the accumulator register will be divided by the number being displayed. The results are displayed in the entry register, and a copy of the result is stored in the accumulator. The mode register is modified to reflect the latest key entry.

Operation of the "%" key while in divide mode looks exactly the same as the "=" key except the decimal point of the display is shifted two positions to the left before division takes place.

ERROR CONDITIONS

If any of the operations mentioned above generates a number larger than 9999 9999, an error will occur. An error is indicated by displaying the eight most significant digits and sign with all nine decimal points. The first depression of the "C/CE" key will clear the error condition, and all registers except the memory register.

It is not possible to generate an error during number entry. The ninth and subsequent digits entered are ignored.

POWER-ON CONDITION

The MM5795 has an internal power-on clear circuit which clears all registers to zero, places the mode to add and sets the terminate flag. A zero and decimal point are displayed.

KEYBOARD BOUNCE AND NOISE REJECTION

The MM5795 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K2, K3 or K4 is forced more positive than the Logical High Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after eleven word times if the Key Input is still at a Logical High Level. As long as the key is held down (and the Key Input remains high) no further entry is allowed. When the Key Input changes to a Logical Low Level, the internal counter starts an eleven word timeout for key release. During both, entry and release timeouts, the Key Inputs are sampled every word time for valid levels. If they are found invalid, the counter is reset and the calculator resumes scanning the keyboard.

TEST FEATURES

Several features have been designed into the MM5795 to facilitate testing. One is to allow the key debounce timing to be modified, and the second performs a "segment test" function which turns on all segments for all digit times, with no interdigit blanking. The key bounce time can be reduced from eleven word times to one if a key closure is made between D9 and K2. "Segment Test" occurs when K3 is connected to D9. Closures for test operations are not debounced, and also may occur simultaneously with normal key closures if diodes are used to isolate the D-Lines from each other. The test features are active for every word time the Test switch closure is maintained. These test matrix entries are isolated internally from the normal calculator keys, allowing simultaneous entry of "test" keys and "calculator" keys, except for K3 keys during "Segment Test."

FUNCTION OF KEYS

Some of the keys operate differently when in the data or number entry condition. The MM5795 switches to entry condition when entering numbers and leaves this condition after most function keys. The following paragraphs discuss each of the keys on a full keyboard and the action taken when they are depressed. The earlier paragraphs which discussed the action of "+," "−," "x," "÷" and "%" keys and the examples given in later sections will aid in further explaining these actions.

Clear Key, "CE/C"

While in the number entry condition, one depression will clear the entry register to zero and recall the accumulator for display. The machine then leaves the number entry state.

If the error condition is displayed, one depression will clear the error, and all registers except the memory register. The machine could not be in the number entry condition with the error flag set.

If the error flag is not set and the machine is not in the number entry condition, one depression of "CE/C" key will clear the entry and accumulator registers. It also places the machine in the add mode and sets the terminate flag. The memory register remains unchanged.

Number Keys 0-9

If *not* in the number entry condition, a number key will clear the display and then enter the value of the key into the LSD. The digits are displayed as they are entered and the machine assumes the number entry condition.

If in the number entry condition, the entry register is shifted left one position and the key depressed is entered into the LSD. If there is a number in the most significant digit position (9th) the entry register is then shifted right one position and the entry is lost.

Square Root Key, "$\sqrt{\ }$"

The square root key extracts the square root of the absolute value of the number being displayed in the entry register.

The mode of the calculator remains unchanged. This enables square root operations in the middle of chain calculations. For example:

KEY	DISPLAY	KEY	DISPLAY	KEY	DISPLAY
A	A	A	A	11	11
$\sqrt{\ }$	$\sqrt{A}$	X	A	+	11.
+	$\sqrt{A}$	B	B	5	5
B	B	$\sqrt{\ }$	$\sqrt{B}$	=	16.
$\sqrt{\ }$	$\sqrt{B}$	=	$A\sqrt{B}$	$\sqrt{\ }$	4.
=	$\sqrt{A}+\sqrt{B}$			6	6.
				=	11
				9	9
				$\sqrt{\ }$	3.
				=	8.

Square Key, "X^2"

Depression of the "Square" key copies the number being displayed into the accumulator register, and performs a multiplication. On completion of the square operation, the results are displayed in the entry register, the original number is stored in the accumulator and the mode of the calculator is unchanged. Entering a number to start a new entry will first clear the entry register.

Memory Recall Key, "MR"

The "MR" key recalls the number being stored in the memory register and displays it in the entry register. This number can then be used as a new number entry.

Memory Clear Key, "MC"

The "MC" key clears the memory register. The status of the calculator remains unchanged.

Memory Plus Key, "M+"

When the "M+" key is depressed, the number being displayed is added to the contents of the memory and the results, providing there is no overflow, are placed in the memory. The calculator will be out of the data entry mode.

If an overflow occurs, the contents of the memory are *not* altered. The display shows the eight most significant digits and sign of the results with all nine decimal points.

Memory Minus Key, "M–"

This key operates like the "M+" key only the displayed number is subtracted from memory.

Plus, Minus, Multiply and Divide Keys, "+," "–," "x," "÷"

These keys terminate a number entry, complete the operation designated by the mode register and update the mode register for the next operation. A more detailed explanation of these keys is found in the description of modes.

Equal Key, "="

This key terminates a number entry, complete the operation designated by the mode register and sets the terminate flag.

Percent Key, "%"

Following a clear-all operation or a number entry proceeded by a clear all operation, this key shifts the decimal point of the number being displayed two places to the left, copies it into the accumulating register and establishes the multiply mode.

While in multiply or divide mode, this key shifts the displayed decimal point two places to the left, completes the multiplication or division and sets the terminate flag.

In add or subtract mode, this key shifts the displayed decimal point two places to the left, multiplies the display times the accumulating register, places the product in the entry register and leaves the accumulator register and mode register undisturbed. This permits automatic calculation of net by depression of the "=" key. The terminate flag is not altered.

SAMPLE PROBLEMS

1. Simple addition or subtraction

KEYS	DISPLAY	COMMENTS
C/CE	0	
3	3	Start addition problem

1. Simple addition or subtraction (continued)

KEYS	DISPLAY	COMMENTS
+	3.	Sets add mode
2	2	
+	5.	Completes addition, sets add mode
–	5.	Resets addition mode, sets subtraction mode
4.355	4.3 5 5	
=	0.6 4 5	Completes subtraction. Sets terminate mode.
+	0.6 4 5	Sets add mode
3.25	3.2 5	Starts Digit Entry
CS	–3.2 5	Changes Sign
4	–3.2 5 4	Continues Digit Entry
+	–2.6 0 9	Completes signed addition, sets add mode
1	1	
=	–1.6 0 9	Completes signed addition, sets terminate mode

2. Constant addition or subtraction (second factor constant)

KEYS	DISPLAY	COMMENTS
3	3	
–	3.	Sets subtract mode
2	2	
+	1.	Completes subtraction, sets add mode
6	6	
=	7.	Completes addition, saves (6) as constant, sets terminate mode
.5	.5	
=	6.5	Completes addition constant=6
7	7	
–	7.	Sets subtraction mode, resets terminate mode
3	3	
=	4.	Completes subtraction, sets terminate mode, saves 3 as a constant
8	8	
EX	3.	Exchanges entry, and constant
=	–5.	Completes subtraction constant = 8
9	9	
=	1.	Completes subtraction constant = 8

3. Simple multiplication

KEYS	DISPLAY	COMMENTS
3.1	3.1	Start multiplication problem

3. Simple multiplication (continued)

KEYS	DISPLAY	COMMENTS
X	3.1	Sets multiply mode
6	6	
=	1 8.6	Completes multiplication, sets terminate mode

4. Chain multiplication

KEYS	DISPLAY	COMMENTS
3	3	
+	3	Sets add mode
4	4	
X	7.	Completes addition, sets multiply mode
6	6	
–	4 2.	Completes multiplication, sets subtract mode
2	2	
=	4 0.	Completes subtraction, sets terminate mode, saves 2 as constant

5. Constant multiplication

KEYS	DISPLAY	COMMENTS
3	3	
X	3.	Sets multiply mode
4	4	
=	1 2.	Completes multiplication, saves '4' as constant, sets termination mode
6	6	
=	2 4.	Completes constant multiplication, constant = 4
3	3	
–	3.	Sets subtract mode, resets termination
4.5	4.5	
X	–1.5	Completes subtraction, sets multiply mode
8	8	
CS	–8	Changes sign
=	1 2.	Completes multiplication '–8' as constant, sets termination mode
EX	–8.	Exchanges entry register, and constant
CS	8.	
3	3	
=	3 6.	Completes constant multiplication constant = 12

5. Constant multiplication (continued)

KEYS	DISPLAY	COMMENTS
=	4 3 2.	Completes constant multiplication constant = 12
3	3	
X	3.	Sets multiply mode, resets termination mode
+	3.	Sets add mode. Second function key only modifies mode
–	3.	Sets subtract mode
X	3.	Sets multiply mode
=	9.	Completes multiplication. Sets termination mode

6. Simple division

KEYS	DISPLAY	COMMENTS
4	4	
÷	4.	
3	3	
CS	–3	
=	–1.3 3 3 3 3 3 3	

7. Chain division

KEYS	DISPLAY	COMMENTS
3	3	
÷	3.	
8	8	
+	0.3 7 5	
2	2	
X	2.3 7 5	
3.1	3.1	
÷	7.3 6 2 5	
6	6	
=	1.2 2 7 0 8 3 3	

8. Constant division

KEYS	DISPLAY	COMMENTS
6	6	
÷	6.	
2	2	
=	3.	
=	1.5	
15	1 5	
–	1 5.	
2	2	
X	1 3.	
8.3	8.3	
÷	1 0 7.9	
3	3	
CS	–3	
EX	1 0 7.9	

8. Constant division (continued)

KEYS	DISPLAY	COMMENTS
=	−.02780352	
EX	107.9	
CS	−107.9	
EX	−.02780352	
608.7	608.7	
=	−5.6413345	

9. Add on and discount problems

KEYS	DISPLAY	COMMENTS
695.99	695.99	
−	695.99	
20	20	
%	139.198	
=	556.792	
+	556.792	
6	6	
%	33.40752	
=	590.19952	
17.95	17.95	
−	17.95	
15	15	
%	2.6925	
+	15.2575	
6	6	
%	0.91545	
=	16.17295	

10. Percent in multiplication and division

KEYS	DISPLAY	COMMENTS
308	308	
X	308.	
5	5	
%	15.4	
500	500	
÷	500.	
4	4	
%	12500.	

11. Memory operations

KEYS	DISPLAY	COMMENTS
6	6	
M+	I 6.	Memory indicator is activated in left-most digit

11. Memory operations (continued)

KEYS	DISPLAY	COMMENTS
3	I 3	
+	I 3.	
2	I 2	
M−	I 2.	
=	I 5.	
MR	I 4.	
3.678	I 3.678	
CS	I −3.678	
M+	I −3.678	
X	I −3.678	
5	I 5	
M−	I 5.	
=	I −18.39	
MR	I −4.678	
5	I 5	
MC	5.	Memory indicator turned off when contents equal zero
3	3	
X	3.	
4	4	
X	12.	
MR	0.	
=	0.	

12. Square root problems

KEYS	DISPLAY	COMMENTS
3	3	
√	1.7320508	
+	1.7320508	
4	4	
√	2.	
=	3.7320508	
7	7	
+	7.	
8	8	
=	15.	
√	3.8729833	

13. Square problems

KEYS	DISPLAY	COMMENTS
72	72	
X^2	5184.	

MM57103 scientific calculator circuit

general description

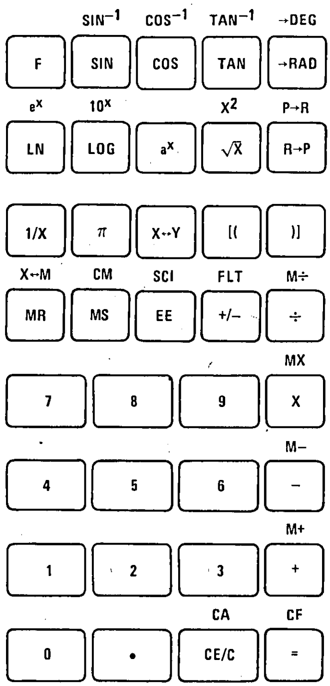
The MM57103 is a powerful one-chip scientific calculator device designed to provide the features and functions most desired by professionals. An 8-digit mantissa plus sign with a 2-digit exponent plus sign is featured. A 36-position keyboard (such as that illustrated below) was designed for convenience. Algebraic logic, combined with a fully accumulating 8-function memory in addition to two levels of parentheses are features most asked for in professional scientific calculators. With a simple pin connection, the MM57103 offers RPN logic with a 4-level stack in addition to the 8-function memory.

features

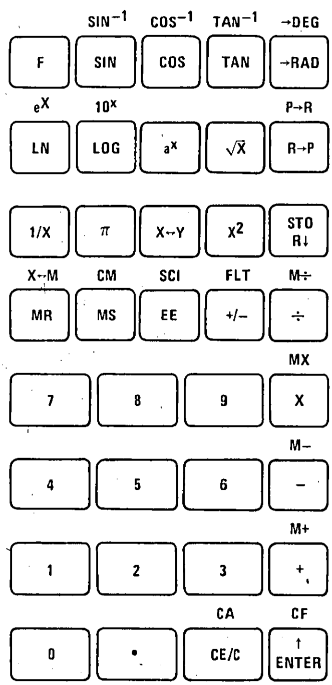
- Enters and displays ±9.9999999 x 10^{99} to ±1. x 10^{-99}
- Left justified entry with trailing zero suppression
- Selectable Reverse Polish Notation (RPN) or Algebraic notation with 2 levels of parentheses
- Arithmetic functions: +, –, X, ÷, 1/X, $\sqrt{X}$, X^2
- Constant operations in algebraic mode
- Power function: Y^X
- Logarithmic functions: LN X, LOG X, e^X, 10^X
- Trigonometric functions: SIN, COS, TAN, SIN^{-1}, COS^{-1}, TAN^{-1}
- Full-function, addressable memory
- 4-register working stack with ROLL capability (RPN) or EQUAL with 2 levels of parentheses (algebraic)
- π, change sign, clear, clear-all and exchange
- Auto power-on clear
- Degree/radian conversion
- Rectangular/polar conversion
- Two output modes: floating or scientific

sample keyboards

Algebraic



RPN



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics 0°C ≤ T_A ≤ +70°C, 7.9V ≤ $V_{SS} - V_{DD}$ ≤ 9.5V unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage ($V_{SS} - V_{DD}$)		7.9		9.5	V
Operating Supply Current (I_{DD})	$V_{SS} - V_{DD}$ = 9.5V, T_A = 25°C, (Excluding Outputs)		12	18	mA
Osc. Input Voltage Levels					
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−1.0			V
Logic Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 9.5V			V_{DD}+1.5	V
Osc. Input Resistance To V_{SS}			3		kΩ
K1–K4	(For Keyboard)				
Input Voltage Levels					
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−3.2		V_{SS}	V
	$V_{SS} - V_{DD}$ = 9.5V	V_{SS}−4.5		V_{SS}	V
Logic Low Level (V_{IL})				V_{DD}+1.5	V
K1–K4 Input Current Levels	(Through Keyboard)				
Input High Level (I_{IH})	$V_{IH} = V_{SS}$ − 3.2V			−350	μA
D03 Input Voltage Levels					
Logic High Level (V_{IH})	7.9V ≤ $V_{SS} - V_{DD}$ ≤ 9.5V	V_{SS}−3.5			V
Logic Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 7.9V			V_{DD}+2.5	V
	$V_{SS} - V_{DD}$ = 9.5V			V_{DD}+3.0	V
SI and Sync Input Voltage Levels					
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−1.2			V
Logic Low Level (V_{IL})	$V_{SS} - V_{DD}$ = 7.9V			V_{SS}−4.0	V
D01, D02, D04 Output Voltage Levels (Encoded Digit)					
Logic High Level (V_{OH})	R_L = 150 kΩ	V_{SS}−1.0		V_{SS}	V
Logic Low Level (V_{OL})	I_{OL} = 3 μA	V_{DD}		V_{DD}+0.5	V
Logic High Level Current (I_{OH})	$V_{SS} - V_{DD}$ = 7.9V				
	$V_{OH} = V_{DD}$ + 1.5V			−260	μA
D03 Output Voltage Levels					
Logic High Level (V_{OH})	R_L = 150 kΩ	V_{SS}−1.0		V_{SS}	V
Logic Low Level (V_{OL})	I_{OL} = 3 μA	V_{DD}		V_{DD}+0.5	V
Logic High Level Current (I_{OH})	Battery Low "OFF", from DS8664				
	$V_{OH} = V_{DD}$ + 3V				
	$V_{SS} - V_{DD}$ = 9.5V	−1.3		−0.3	mA
	$V_{OH} = V_{DD}$ + 2.5V				
	$V_{SS} - V_{DD}$ = 7.9V	−1.0		−0.4	mA
	Battery Low "ON", from DS8664				
	$V_{OH} = V_{SS}$ − 3V				
	$V_{SS} - V_{DD}$ = 7.9V			−0.3	mA
	$V_{OH} = V_{SS}$ − 3V				
	$V_{SS} - V_{DD}$ = 9.5V			−0.4	mA
Sa–Sg and Sp Output Current Levels					
Logic High Level Current (I_{OH})	$V_{OH} = V_{DD}$ + 3V	−20	−10	−5	mA

dc electrical characteristics (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sync Output Voltage Levels	(With Load and Driver to V_{DD}) $V_{SS} - V_{DD} = 7.9V$				
Logic High Level (V_{OH})	$I_{OH} = -100\,\mu A$	V_{SS}−0.5		V_{SS}	V
Logic Low Level (V_{OL})	$I_{OL} = 15\,\mu A$	V_{DD}		V_{DD}+3.7	V
F1, F2, F3 Output Voltage Levels					
Logic High Level (V_{OH})	$I_{OH} = -30\,\mu A$	V_{SS}−1.5			V
Logic Low Level (V_{OL})	$I_{OL} = 3\,\mu A$			V_{DD}+1.0	V
BLK Output Voltage Levels					
Logic High Level (V_{OH})	$I_{OH} = -0.5$ mA	V_{SS}−1.5			V
Logic Low Level (V_{OL})	$I_{OL} = 5\,\mu A$			V_{DD}+1.0	V
Keyboard Key Resistance (R_{KEY}) (INB, K1–K4, F1–F3)	LED Display Interface			200	Ω

ac electrical characteristics $0°C \le T_A \le +70°C$, $7.9V \le V_{SS} - V_{DD} \le 9.5V$ unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Osc. Input Frequency		320		400	kHz
Osc. Duty Cycle *(Figure 2)*		46	56	66	%
Osc. Input					
Rise Time (t_r)	$C_L = 25$ pF, $R_L = 6$ kΩ			350	ns
Fall Time (t_f)	RC = 0.15 µs			50	ns
K1–K4, D03					
Input Timing					
t_{SK}		1.75			µs
t_{LK}		1.0			µs
BLK Output Timing					
t_{pdBLK}	$C_{LOAD} = 50$ pF			4.4	µs
t_{rb}	$C_{LOAD} \le 20$ pF	0.3			µs
F1, F2, F3 Output Timing	$C_{LOAD} = 100$ pF			4.4	µs
t_{pdf}					
Sync Output Timing					
Interval (t_B, Bit Time)	(For On-Chip Oscillator)	8.8		30	µs
t_{pdsL}	$C_L = 250$ pF	0.1		1.65	µs
t_{pdsH}		0.1		1.25	µs
t_{HS}		0.1		0.8	µs
D01, D02, D03, D04 Output Timing	$C_L = 100$ pF (D01–D04) $C_L = 250$ pF (S0)				
t_{pd}		0.5		4.0	µs
S_a–S_g, S_p Output Timing (t_{pdSEG})				6.0	µs
Interdigit Blanking Time (T1)				7.5	µs

functional description

REGISTER CONFIGURATION

The user has access to 5 registers designated X, Y, Z, T, and M. X is the display and entry register and the bottom of an "operational" stack that includes Y, Z and T. M is an independent user-addressable memory register that can be stored, recalled, added, multiplied, subtracted or divided with X. In the algebraic mode, Z and T are used as parenthesis registers.

All registers contain 8 mantissa digits with sign and 2 exponent digits with sign.

DISPLAY CONFIGURATION

The X-register is always displayed and shown as 8 digits of mantissa with sign and 2 digits of exponent with sign. Numbers are entered left justified with trailing zeros suppressed.

DISPLAY FORMAT

Floating point display output format is "F", "•". If X is greater than 99999999. or less than .1, the display is in scientific notation.

By pressing "F", "EE" all results are displayed in scientific notation.

READY SIGNAL OPERATION

Output F1 of the MM57103 can be used as a "ready signal" to indicate calculator status. It can be useful in providing synchronization information during testing and if used with other logic.

When the calculator is in the "idle state" and ready to accept a key, F1 is high (near V_{SS}). It remains high until a key is depressed and accepted, then goes low. It goes low until the calculator is complete then goes high again to indicate that a new key may be entered.

KEYBOUNCE AND NOISE REJECTION

When a key is depressed, a time-out is started. A key is accepted as valid if it remains depressed for approximately 12 ms. The key must be released for at least 12 ms before a new key can be entered.

ERROR CONDITIONS AND INDICATION

In the event of an illegal operation, the calculator will display "Error" and X will be cleared. Any key depressed after an error will use X = 0 for the next operator. Table I summarizes results and operations that will give an error indication.

RANGE ACCURACY AND SPEED

All functions work over the full mathematically allowable range as defined by the error conditions.

All functions take less than 1 second and are accurate to 8 digits.

ALGEBRAIC OR RPN SELECTION

Connect pin 5 (INB) to V_{DD} to select algebraic mode. Connect to V_{SS} to select RPN mode.

TABLE I. Results and Operations Resulting in an Error Indication

Results $> 9.9999999 \times 10^{99}$
Results $< 1 \times 10^{-99}$
Division by 0
LOG, LN < 0
TAN, SIN, COS $> 9000°$
TAN 90°, 270°, etc.
SIN^{-1}, $COS^{-1} > 1$ or $\leq 10^{-50}$
$\sqrt{X} < 0$
More than two open parentheses without a close
More close parentheses than open

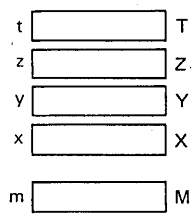


FIGURE 1. User Register Configuration

functional description (Continued)

KEY OPERATIONS

Clear Key "C"

a) In RPN mode: Pushes down stack and clears T. Four "C" depressions will clear a completely full stack
b) After "F": Clears all registers including the memory
c) In algebraic mode after number key: Copy Y to X
d) In algebraic mode after function key: Clears all modes and X, Y, Z and T

Number Keys, "0" ~ "9", "."

a) In RPN mode after any function key except "EN": Clears X and enters number left justified to X
b) After any number key: Enters next digit into X. All entries after eighth are ignored
c) After "EE": Enters number to exponent. Last 2 entries are used
d) After "EN": Clears X and enters number in X
e) In algebraic mode, after function key: Clears X and enters number

Change Sign Key, "CS"

a) After "EE": Change sign of exponent of X
b) After any other key: Changes sign of X mantissa

Coordinate Conversion Key, "R ↔ P"

a) Converts contents of X and Y in rectangular coordinates to polar coordinates:
$\sqrt{X^2+Y^2}$ to Y
TAN^{-1} Y/X to X
b) After "F": (P → R): Converts contents of X and Y in polar coordinates to rectangular coordinates:
Y SIN X → Y (Ω SIN 0)
Y COS X → X (Ω COS 0)

Square Root/Square Key, "$\sqrt{X}$/X^2"

a) Square root of X to X
b) After "F": (X^2) X-squared to X

Reciprocal/"1/x"

Reciprocal of X to X

Power Key "Y^X"

a) In RPN mode: Computes Y^X power, pushes down stack, clears T
b) In algebraic mode, not in chain mode: Copy X to Y, set Y^X chain mode
c) In algebraic mode, in chain mode: Perform the specified function of X and Y, putting the result to both X and Y, set Y^X chain mode

Enter Key, "EN"

a) Pushes up stack, retains X
b) After F: (CF) resets F mode

Second Function Key, "F"

Sets F mode

Memory Store/Clear "MS/"MC"

a) Copy X to memory
b) After F: (CM) clear memory

Memory Recall/Exchange Memory "MR/X–M"

a) In RPN mode: Pushes up stack, recall memory to X
b) In algebraic mode: Recall X to M
c) After F: Exchange X and M

Enter Exponent Key, "EE"

Sets enter exponent mode, displaying 00 in exponent position.

Stack Rotate Key "ROLL", RPN Only

Rolls stack down

Exchange Key, "X ↔ Y"

Exchanges X and Y

Common Log Key, "LOG/10^X"

a) Common logarithm of X to X (base 10)
b) After "F": (10^X) 10^X to X

Natural Log Key, "LN/e^X"

a) Natural logarithm of X to X (base e)
b) After "F": (e^X) e^X to X

Trigonometric Keys, "SIN, COS, TAN"

a) Replaces the decimal angle in X with the indicated trigonometric function
b) After F: (SIN^{-1}, COS^{-1}, TAN^{-1}) Replaces X with the decimal angle of the indicated inverse trigonometric function

The Four Function Keys, "+, –, X, ÷", In RPN Mode

a) Add key, "+": Y + X → X
Subtract key, "–": Y – X → X
Multiply key, "X": Y x X → X
Divide key, "÷": Y/X → X
Then push down stack and clear T
0 → T → Z → Y
b) After F: +: X + M to M
–: M – X to M
X: M x X to M
÷: M/X to M

8

functional description (Continued)

The Four Function Keys, "+", "–", "X", "÷", In Algebraic Mode

a) If not in chain mode: Copy X to Y, set the specified chain mode
b) After "+, –, X, ÷" key: Copy X to Y, set chain mode
c) In chain mode: Perform the specified function of X and Y putting the result to X and Y, set the specified chain mode

π Key, "π"

a) In RPN mode: Pushes up stack enter π to X (3.1415927)
b) In algebraic mode: Enter π to X

Degree to Radian Key, "D → R"

a) Converts X in degrees to radians X = Xo/180 x π
b) Converts X in radians to degrees X = Xo/π x 180

Equal Key, "="

a) In chain mode: Perform the specified function of X and Y putting the result to X and save the last number displayed in Y, set the constant mode
b) In constant mode: Perform the specified function of X, Y putting the result in X
c) After F: (CF) reset F mode

Open Parenthesis, "[("

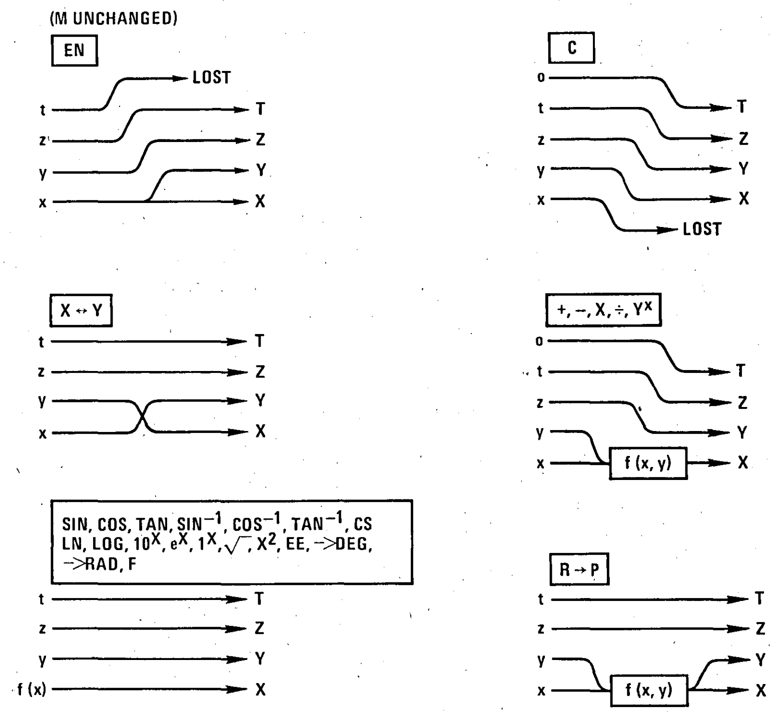
Copy Z to T, copy X to Z; copy P1 mode to P2 mode; copy the calculator mode to P1 mode, reset calculator mode

Close Parenthesis ")] ", Algebraic Mode

a) In chain mode: Perform the specified function of X, Y putting the result to X. Copy Z to Y, copy T to Z, clear T2. Copy P2 mode to P1 mode, copy P1 mode to the calculator mode, reset P2 mode
b) Not in chain mode: Z to Y, T to Z, clear T, P1 mode to calculator mode, P2 mode to P1 mode, reset P2 mode

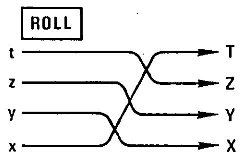
summary

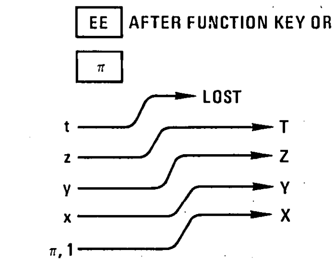
Stack Operations in RPN Mode

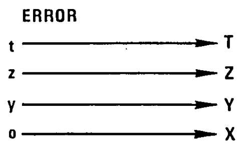


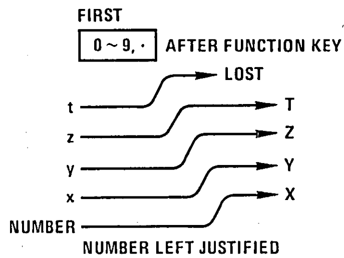
summary (Continued)

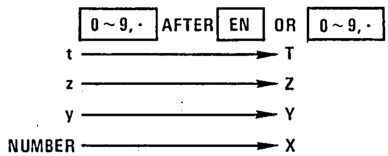
Stack Operations in RPN Mode (Continued)



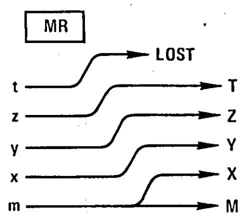


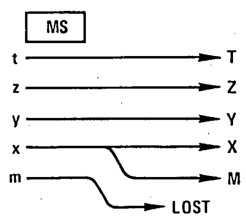


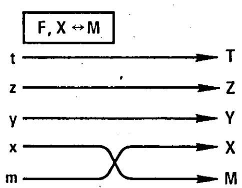


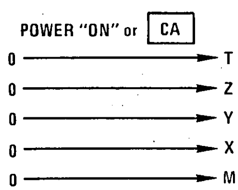


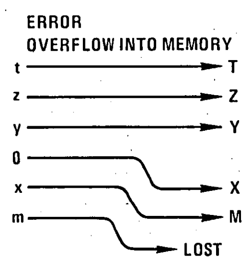
Operations Using Memory(s)











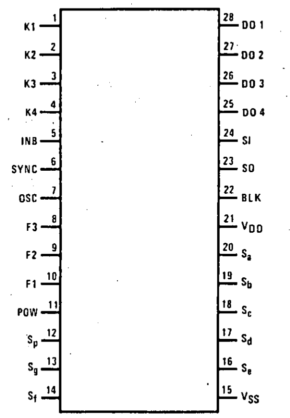
Example Showing Parentheses Registers and Modes in Algebraic Mode

$6 \times (2^{(8-5)} + 2)$

	X	Y & MODE	P1 Z & MODE	P2 T & MODE
6	6			
X	6	6x		
(	6	6	6x	
2	2	6	6x	
FY^X	2	2Y^X	6x	
(	2	2	2Y^X	6x
8	8	2	2Y^X	6x
–	8	8+	2Y^X	6x
5	5	8–	2Y^X	6x
)	3	2Y^X	6x	
+	8	8+	6x	
Z	Z	8+	6x	
)	10	6x		
=	60	10x (constant)		

connection diagram

Dual-In-Line Package

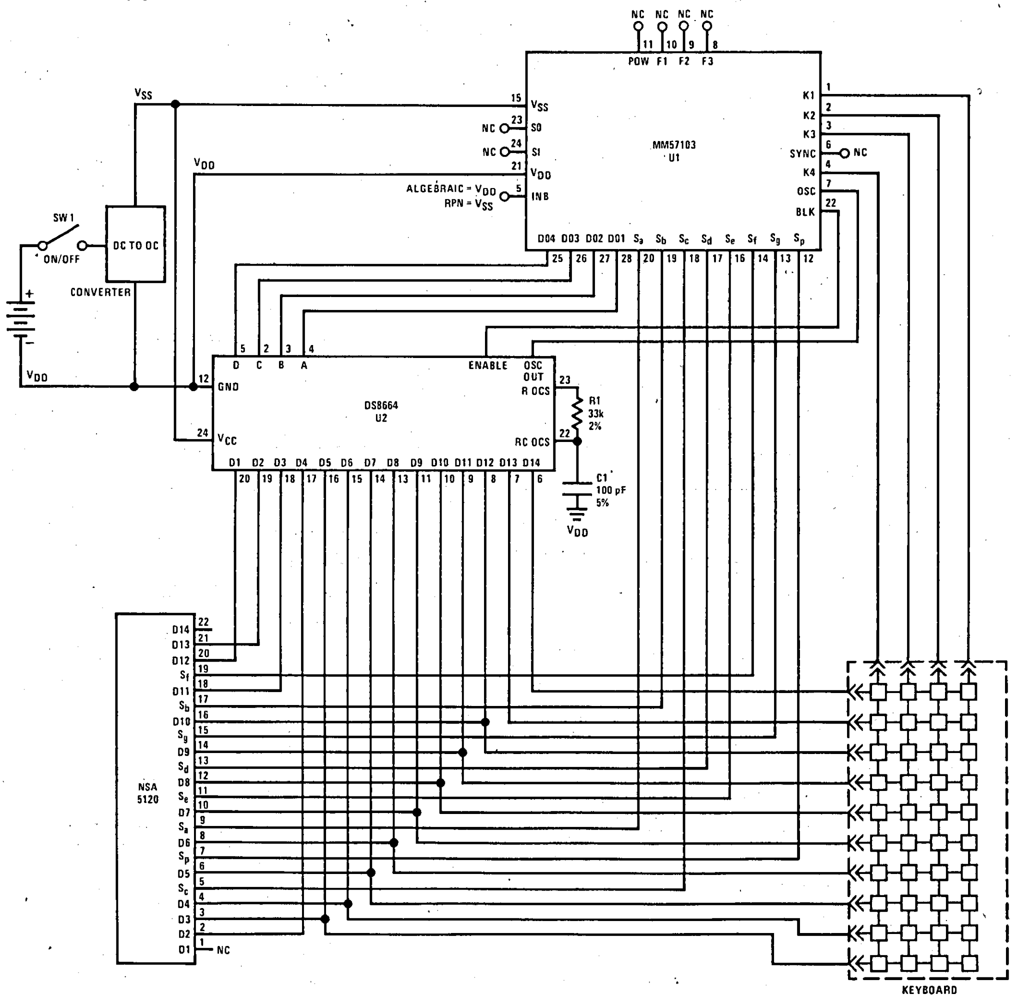


TOP VIEW

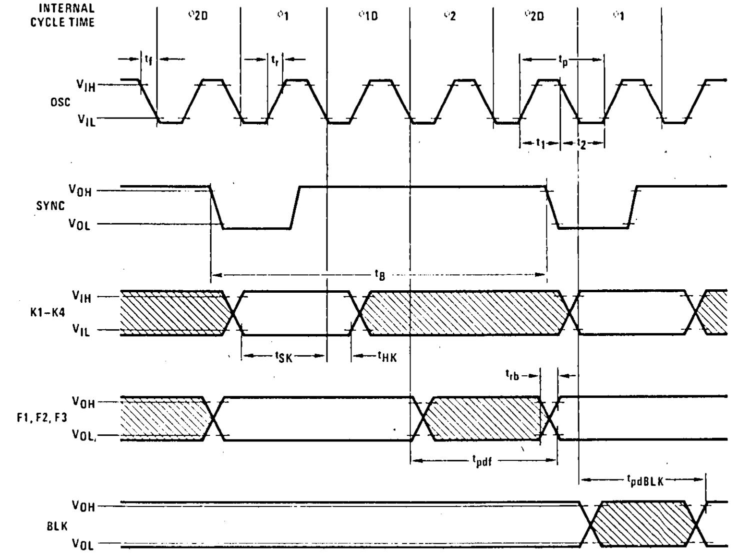
Order Number MM57103N
See Package 23

typical application

Typical Scientific Calculator Schematic



switching time waveforms



Note. OSC Duty Cycle = $\frac{t_1}{t_1 + t_2} = \frac{t_1}{t_p}$

FIGURE 2(a). Input/Output Timing Diagram

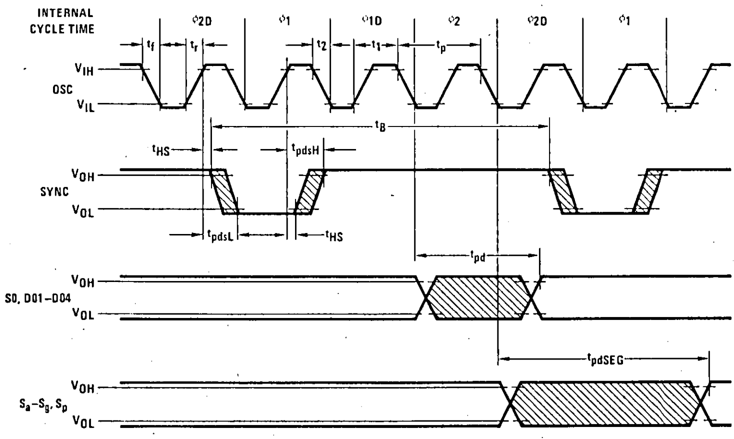


FIGURE 2(b). Input/Output Timing Diagram

keyboard matrix connection table

SWITCH INPUTS	DIGIT TIMING STATE									
	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5
K1		=	+	C	•	0	3	2	1	
K2		X	–	9	8	7	6	5	4	
K3	M+	[(	÷	)]	%	Σ+	CS	EE	MS	MR
K4	F	D.MS	R → P	TAN	COS	SIN	$\sqrt{\ }$	1/X	LOG	LN

MM57104 scientific calculator circuit

general description

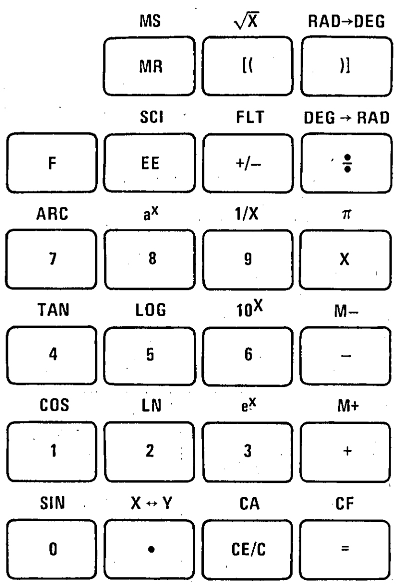
The MM57104 features the most essential and desirable scientific functions microprogrammed onto a single economical MOS/LSI device. Use of a 9-digit display with a 5-digit mantissa plus sign and a 2-digit exponent plus sign is featured even though internal numbers use a full 8-digit mantissa for accuracy. Low system cost without sacrificing features has been achieved with the MM57104; direct operation from an inexpensive throw-away 9V battery, eliminating the need for a dc/dc converter, minimal cost 23-position keyboard and a standard 9-digit low cost LED display. National's built-in reliability and rugged 24-lead DIP add further to the MM57104's total system efficiency.

features

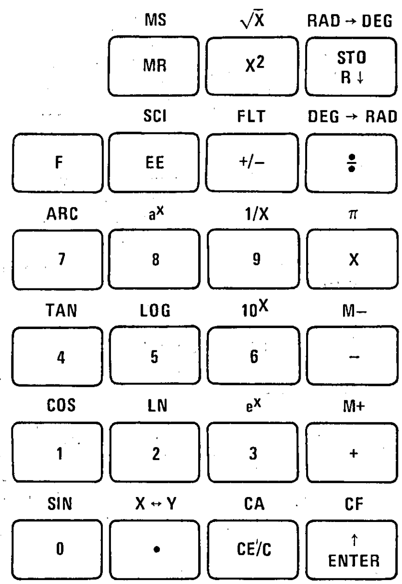
- Enters $\pm 9.9999999 \times 10^{99}$ to $\pm 1 \times 10^{-99}$
- 9-position display: 5-digit mantissa plus sign and 2-digit exponent with sign
- Left justified entry with trailing zero suppression
- Selectable Reverse Polish Notation (RPN) or Algebraic notation with 2 levels of parentheses
- Arithmetic functions: +, −, X, ÷, 1/X, $\sqrt{X}$, X^2
- Constant operations in algebraic mode
- Power function: Y^X
- Logarithmic functions: LN X, LOG X, e^X, 10^X
- Trigonometric functions: SIN, COS, TAN, SIN^{-1}, COS^{-1}, TAN^{-1}
- Full-function, addressable memory
- 4-register working stack with ROLL capability (RPN) or EQUAL with 2 levels of parentheses (algebraic)
- π, change sign, clear, clear-all and exchange
- Auto power-on clear
- Degree/radian conversion
- Two output modes: floating or scientific

sample keyboards

Algebraic



RPN



absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

$0°C \leq T_A \leq +70°C$, $7.9V \leq V_{SS} - V_{DD} \leq 9.5V$ unless otherwise stated

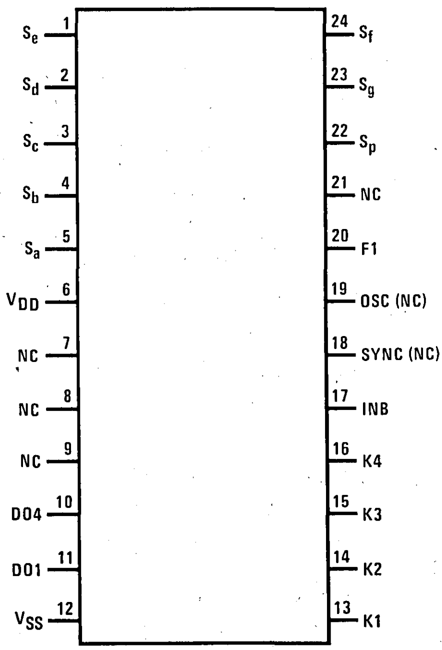
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage ($V_{SS} - V_{DD}$)		7.0		9.5	V
Operating Supply Current (I_{DD})	$V_{SS} - V_{DD}$ = 9.5V, T_A = 25°C (Excluding Outputs)		12	18	mA
K1–K4					
Input Voltage Levels					
Logic High Level (V_{IH})	$V_{SS} - V_{DD}$ = 7.9V	V_{SS}−3.2		V_{SS}	V
	$V_{SS} - V_{DD}$ = 9.5V	V_{SS}−4.5		V_{SS}	V
Logic Low Level (V_{IL})				V_{DD}+1.5	V
K1–K4 Input Current Levels	(Through Keyboard)				
Input High Level (I_{IH})	$V_{IH} = V_{SS}$ − 3.2V			−350	µA
D01, D04 Output Voltage Levels (Encoded Digit)					
Logic High Level (V_{OH})	R_L = 150 kΩ	V_{SS}−1.0		V_{SS}	V
Logic Low Level (V_{OL})	I_{OL} = 3 µA	V_{DD}		V_{DD}+0.5	V
Logic High Level Current (I_{OH})	$V_{SS} - V_{DD}$ = 7.9V				
	$V_{OH} = V_{DD}$ + 1.5V			−260	µA
S_a–S_g and S_p Output Current Levels					
Logic High Level Current (I_{OH})	$V_{OH} = V_{DD}$ + 3V				
Open Drain Outputs		−20	−10	−5	mA
Sync Output Voltage Levels	(With Load and Driver to V_{DD})				
	$V_{SS} - V_{DD}$ = 7.9V				
Logic High Level (V_{OH})	I_{OH} = −100 µA	V_{SS}−0.5		V_{SS}	V
Logic Low Level (V_{OL})	I_{OL} = 15 µA	V_{DD}		V_{DD}+3.7	V
F1 Output Voltage Levels					
Logic High Level (V_{OH})	I_{OH} = −30 µA	V_{SS}−1.5			V
Logic Low Level (V_{OL})	I_{OL} = 3 µA			V_{DD}+1.0	V
Osc. Output Current Levels	(Output with Load to V_{DD})				
Logic High Level Current (I_{OH})	$V_{OH} = V_{DD}$ + 1.5V			−1.0	mA
Logic Low Level Current (I_{OL})	$V_{OL} = V_{DD}$ + 0.5V	3.0			µA
Keyboard Key Resistance (R_{KEY}) (K1–K4)	LED Display Interface			200	Ω

ac electrical characteristics $0°C \leq T_A \leq +70°C$, $7.9V \leq V_{SS} - V_{DD} \leq 9.5V$ unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Osc. Output Frequency		130		450	kHz
Osc. Duty Cycle *(Figure 2)*		33	56	68	%
K1–K4, INB					
Input Timing					
t_{SK}		1.75			μs
t_{LK}		1.0			μs
F1 Output Timing	C_{LOAD} = 100 pF			4.4	μs
t_{pdf}					
Sync. Output Timing					
Interval (t_B, Bit Time)		8.8		30	μs
t_{pdsL}	C_L = 250 pF	0.1		1.65	μs
t_{pdsH}		0.1		1.25	μs
t_{HS}		0.1		0.8	μs
D01, D04 Output Timing	C_L = 100 pF (D01–D04) C_L = 250 pF (S0)				
t_{pd}		0.5		4.0	μs
S_a–S_g, S_p Output Timing (t_{pdSEG})				6.0	μs
Interdigit Blanking Time (T1)				7.5	μs

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM57104N
See Package 22

functional description

REGISTER CONFIGURATION

The user has access to 5 registers designated X, Y, Z, T, and M. X is the display and entry register and the bottom of an "operational" stack that includes Y, Z and T. M is an independent user-addressable memory register that can be stored, recalled, added, multiplied, subtracted or divided with X. In the algebraic mode, Z and T are used as parenthesis registers.

All registers contain 8 mantissa digits with sign and 2 exponent digits with sign.

DISPLAY CONFIGURATION

The X-register is always displayed and shown as 8 digits of mantissa with sign or 5 digits of mantissa with sign and 2 digits of exponent with sign. Numbers are entered left justified with trailing zeros suppressed.

DISPLAY FORMAT

Floating point display output format is "F", "CS". If X is greater than 99999999. or less than 0.001, the display is in scientific notation.

By pressing "F", "EE" all results are displayed in scientific notation.

READY SIGNAL OPERATION

Output F1 of the MM57104 can be used as a "ready signal" to indicate calculator status. It can be useful in providing synchronization information during testing and if used with other logic.

When the calculator is in the "idle state" and ready to accept a key, F1 is high (near V_{SS}). It remains high until a key is depressed and accepted, then goes low. It goes low until the calculator is complete then goes high again to indicate that a new key may be entered.

KEYBOUNCE AND NOISE REJECTION

When a key is depressed, a time-out is started. A key is accepted as valid if it remains depressed for approximately 12 ms. The key must be released for at least 12 ms before a new key can be entered.

ERROR CONDITIONS AND INDICATION

In the event of an illegal operation, the calculator will display "Error" and X will be cleared. Any key depressed after an error will use X = 0 for the next operator. Table I summarizes results and operations that will give an error indication.

RANGE ACCURACY AND SPEED

All functions work over the full mathematically allowable range as defined by the error conditions.

All functions take less than 1 second and are accurate to 8 digits.

ALGEBRAIC OR RPN SELECTION

Leaving pin 17 (INB) open selects algebraic. Connect pin 17 to V_{SS} to select RPN.

TABLE I. Results and Operations Resulting in an Error Indication

Results $> 9.9999999 \times 10^{99}$
Results $< 1 \times 10^{-99}$
Division by 0
LOG, LN < 0
TAN, SIN, COS $> 9000°$
TAN 90°, 270°, etc.
SIN^{-1}, $COS^{-1} > 1$ or $\leq 10^{-50}$
$\sqrt{X} < 0$
More than two open parentheses without a close
More close parentheses than open

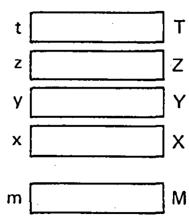


FIGURE 1. User Register Configuration

functional description (Continued)

KEY OPERATION

Clear Key, "C"

a) In RPN mode: Pushes down stack and clears T. Four "C" depressions will clear a completely full stack
b) After "F": Clears all registers including the memory
c) In algebraic mode after number key: Copy Y to X
d) In algebraic mode after function key: Clears all modes and all registers except M

Number Keys, "0" ~ "9", "•"

a) In RPN mode after any function key except "EN": Copies X to Y and clears X and enters number left justified to X
b) After any number key: Enters next digit –> X. All entries after eighth are ignored
c) After "EE": Enters number to exponent. Last 2 entries are used
d) After "EN": Clears X and enters number in X
e) In algebraic mode, after function key: Clears X and enters number

Change Sign Key, "CS"/"FLT"

a) After "EE": Change sign of exponent of X
b) After "F": Set floating point mode
c) After any other key: Changes sign of X mantissa

"F" "9" Reciprocal/"1/X"

Reciprocal of X to X

"F" "8" Power Key, "Y^X"

a) In RPN mode: Computes Y^X power, pushes down stack, clears T
b) In algebraic mode, not in chain mode: Copy X to Y, set Y^X chain mode
c) In algebraic mode, in chain mode: Perform the specified function of X and Y, putting the result to both X and Y, set Y^X chain mode

Enter Key, "EN", RPN Only

a) Pushes up stack, retains X
b) After F: (CF) resets F mode

Second Function Key, "F"

Sets F mode

Memory Recall/Memory Store, "MR/MS"

a) In RPN mode: Pushes up stack, recall memory to X
b) In algebraic mode: Recall X to M
c) After F: Copy X to M

Enter Exponent/Scientific Notation Key, "EE"/"SCI"

a) Sets enter exponent mode, displaying 00 in exponent position
b) After F: Set calculator to scientific notation

"X^2"/"$\sqrt{\ }$" Key, RPN Only

a) X squared to X
b) After F: Square root of X to X

Stack Rotate Key "ROLL"/"DEG" Key, RPN Only

a) Rolls stack down
b) After F: Convert radians to degrees

"F", "•" Exchange Key, "X↔Y"

Exchanges X and Y

"F", "5" Common Log Key

Common logarithm of X to X (Base 10)

"F" "6" 10^X Key

10^X to X

"F" "2" Natural Log Key

Natural logarithm of X to X (base e)

"F" "3" e^X Key

e^X to X

Trigonometic Keys, "F" "0", "F" "1", "F" "4" "SIN", COS, TAN"

a) Replaces the decimal angle in X with the indicated trigonometric function
b) After ARC: (SIN^{-1}, COS^{-1}, TAN^{-1}), replaces X with the decimal angle of the indicated inverse trigonometric function

The Four Function Keys, "+, –, X, ÷", In RPN Mode

a) Add key, "+": Y + X → X
Subtract key, "–": Y – X → X
Multiply key, "X": Y x X → X
Divide key, "÷": Y/X → X
Then push down stack and clear T
0 → T → Z → Y
b) After F: +: X + M to M
–: M – X to M
X: π to X
÷: Convert X from degrees to radians

functional description (Continued)

The Four Function Keys, "+", "–", "X", "÷", In Algebraic Mode

a) If not in chain mode: Copy X to Y, set the specified chain mode
b) After "+, –, X, ÷" key: Copy X to Y, set chain mode
c) In chain mode: Perform the specified function of X and Y putting the result to X and Y, set the specified chain mode

"F" "7" ARC Key

Set ARC mode

Equal Key "=", Algebraic Mode Only

a) In chain mode: Perform the specified function of X and Y putting the result to X' and save the last number displayed in Y, set the constant mode
b) In constant mode: Perform the specified function of X, Y putting the result in X
c) After F: (CF) reset F mode

Open Parenthesis, "[(", Algebraic Mode Only

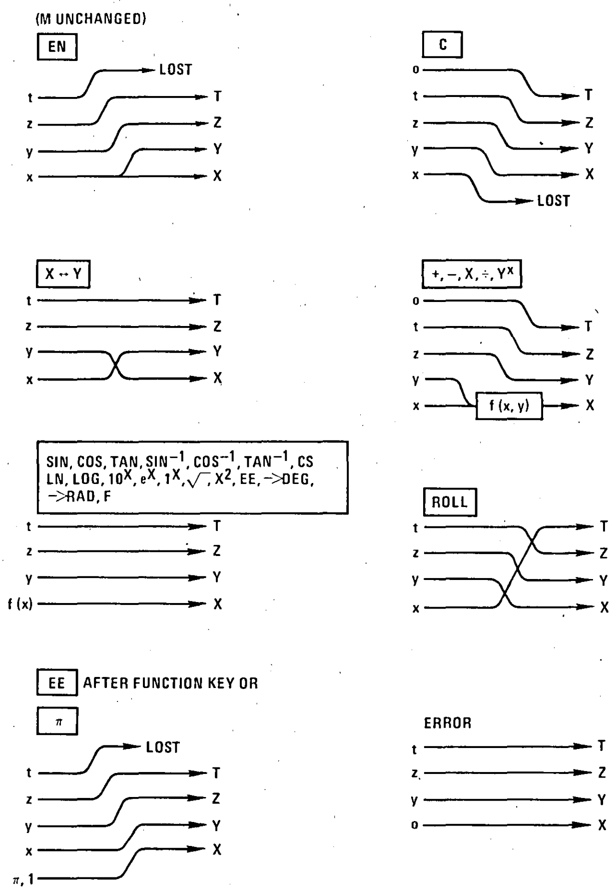
a) Copy X, T copy X to Z, copy P mode to P2 mode: Copy the calculator mode to P1 mode, reset calculator mode
b) After F: Square root of X to X

Close Parenthesis ")] ", Algebraic Mode Only

a) In chain mode: Perform the specified function of X, Y putting the result to X. Copy Z to Y, copy T to Z, clear T2. Copy P2 mode to P1 mode, copy P1 mode to the calculator mode, reset P2 mode
b) Not in chain mode: Z to Y, T to Z, clear T. P1 mode to calculator mode, P2 mode to P1 mode, reset P2 mode
c) After F; Convert radians to degrees

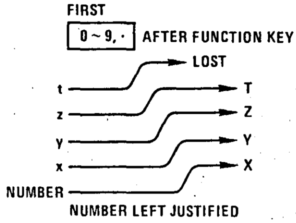
summary

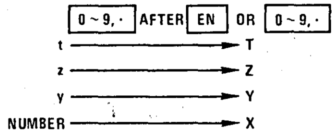
Stack Operations in RPN Mode



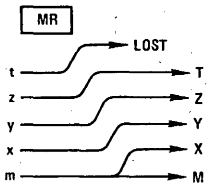
summary (Continued)

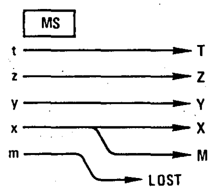
Stack Operations in RPN Mode (Continued)

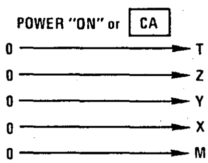


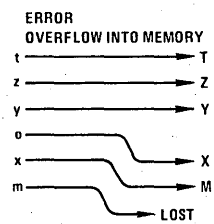


Operations Using Memory(s)







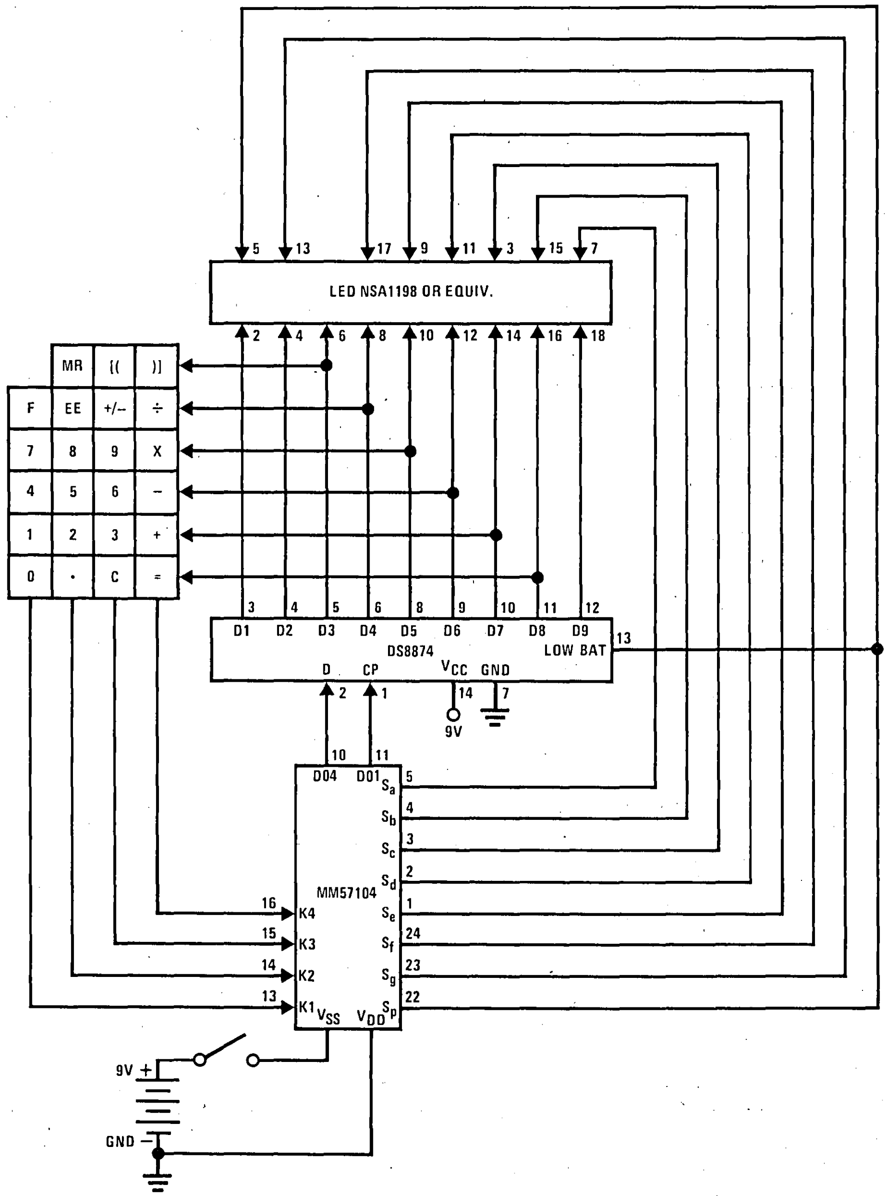


Example Showing Parenthesis Registers and Modes in Algebraic Mode

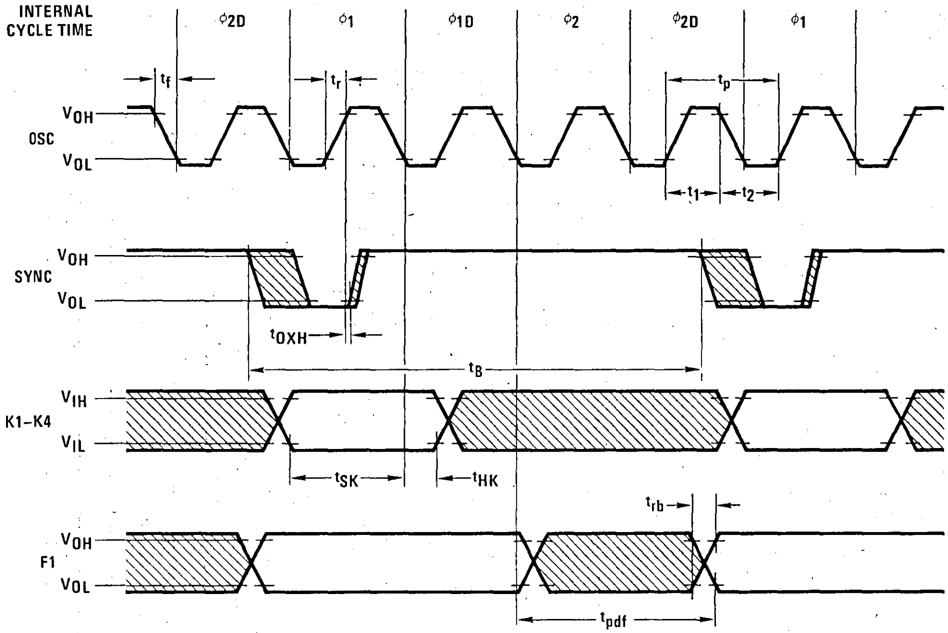
$6 \times (2^{(8-5)} + 2)$

	X	Y & MODE	P1 Z & MODE	P2 T & MODE
6	6			
X	6	6x		
(	6	6	6x	
2	2	6	6x	
FY^X	2	$2Y^X$	6x	
(	2	2	$2Y^X$	6x
8	8	2	$2Y^X$	6x
–	8	8–	$2Y^X$	6x
5	5	8–	$2Y^X$	6x
)	3	$2Y^X$	6x	
+	8	8+	6x	
2	2	8+	6x	
)	10	6x		
=	60	10x (constant)		

system interconnection diagram



switching time waveforms



Note. OSC Duty Cycle = $\frac{t_1}{t_1 + t_2} = \frac{t_1}{t_p}$

FIGURE 2(a). Input/Output Timing Diagram

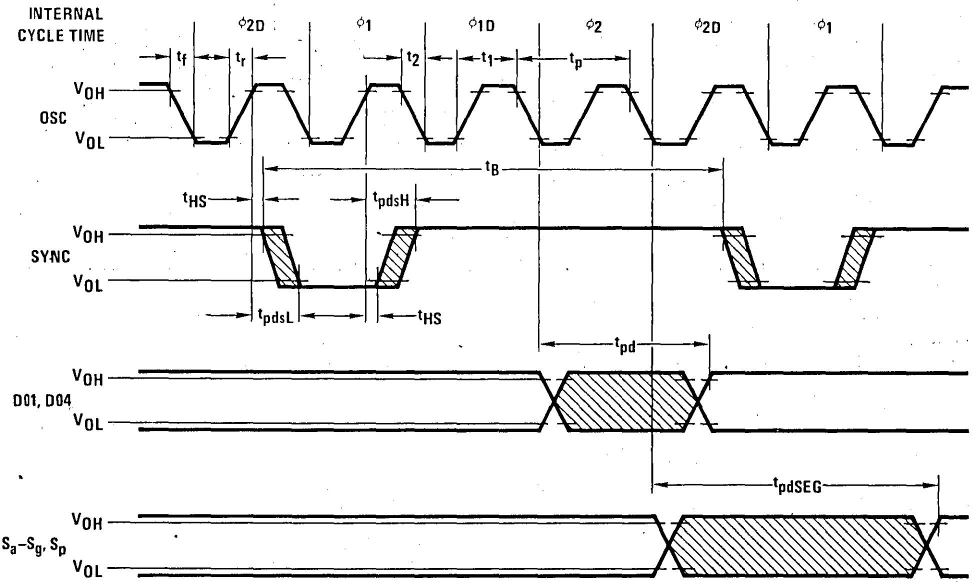


FIGURE 2(b). Input/Output Timing Diagram

MM57123 business/financial calculator circuit

general description

The single-chip MM57123 Business and Financial Calculator was developed using a metal-gate, P-channel enhancement and depletion-mode MOS/LSI technology with low end-product cost as a primary objective. A complete calculator as shown in *Figure 1* requires only the MM57123, a keyboard, digit driver, LED display, 9V battery and appropriate hardware.

Keyboard decoding and key debounce circuitry, all clock and timing generation and 7-segment output display encoding are included on-chip and require no external components. Segments can usually be driven directly from the MM57123, as it typically sources about 8.5 mA of peak current.

An internal power-on clear circuit is included that clears all registers, including the memory, when V_{DD} and V_{SS} are initially applied to the chip.

Trailing zero suppression allows convenient reading of the left justified display, and conserves power; typical current drain of a complete calculator displaying five "5's" is 30 mA. Automatic display cutoff is also included: if no key closure occurs for approximately 35 seconds, all numbers are blanked and all decimal points are displayed.

The Ready output signal is used to indicate calculator status. It is useful in providing synchronization information for testing or applications where the MM57123 is used with other logic or integrated circuits; e.g., with the MM5765 Programmer *(Figure 3)*.

Twenty-two dual-function keys are arranged in a three-by-nine matrix as shown in *Figure 1.* There are the standard four-function keys (+, −, x, ÷), Change Sign, Exchange X and Y, Percent, $\sqrt{x}$, Power, four accumulating memory control keys, plus 12 unique business or financially oriented computation keys; an automatic constant feature is also included.

The MM57123 is physically and electrically compatible with the MM5767 slide-rule calculator IC so that two different models can be produced using the exact same components, even the keyboard; only the keyboard overlay need be changed to show respective keystroke functions.

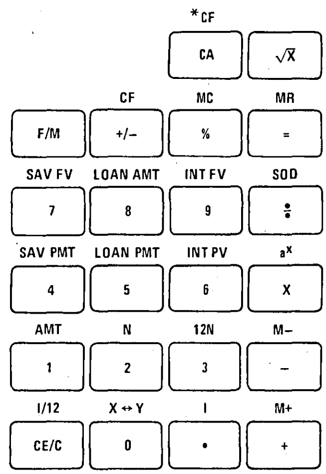
The user has access to six registers designated X, Y, A, I, N and M. The X-register is used for keyboard entry and display. The Y and A-registers are used in multiply/divide and add/subtract calculations, respectively. Interest values are held in the I-register and the N-register stores the number of time periods in financial calculations. M is an accumulating storage memory and is completely independent of the others.

Data is entered into the calculator in floating point business notation. All entries and results are displayed as floating point, left justified with insignificant zeros to the right of the decimal point suppressed.

features

- Complete business and financial capability
  - Arithmetic functions: +, −, x, ÷.
  - Power function: Y^X (power)
  - Live percent
  - Sum-of-digits capability for computing depreciation or "Rule of 78's" loan costs
  - Financial functions:
    - ▲ "N" keys enter number of periods
    - ▲ "I" keys enter interest rate per period
    - ▲ "AMT" key enters given amount
    - ▲ "INT" keys compute PV or FV (compound interest)
    - ▲ "SAV" keys compute deposit or sinking fund amounts
    - ▲ "LOAN" keys compute payment or loan amounts
- Accumulating memory
- Automatic constant
- Convenient business (adding machine) entry notation
- Eight full digits
- Power-on clear
- Automatic display cutoff

keyboard outline



*Optional

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All other pins connected to V_{SS}).	V_{SS} + 0.3V to V_{SS} − 12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating voltage range

$6.5V \leq V_{SS} - V_{DD} \leq 9.5V$

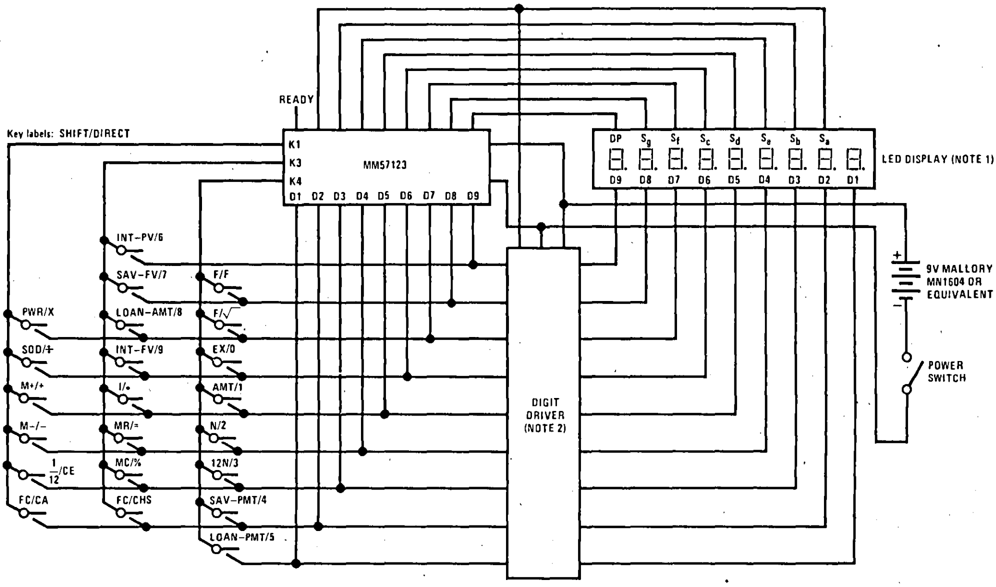
V_{SS} is always defined as the most positive supply voltage

dc electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current (I_{DD})	$V_{DD} = V_{SS} - 9.5V$, $T_A = 25°C$		8.0		mA
Keyboard Scan Input Levels (K1, K2, and K4)					
Logical High Level	$V_{SS} - 6.5V \leq V_{DD} \leq V_{SS} - 9.5V$	V_{SS}−2.5			
Logical Low Level	$V_{DD} = V_{SS} - 6.5V$			V_{SS}−5.0	V
	$V_{DD} = V_{SS} - 9.5V$			V_{SS}−6.0	V
Digit Output Levels					
Logical High Level (V_{OH})	$R_{LOAD} = 3.2\ k\Omega$ to V_{DD}				
	$V_{SS} - 6.5V \leq V_{DD} \leq V_{SS} - 9.5V$	V_{SS}−1.5			
Logical Low Level (V_{OL})	$V_{DD} = V_{SS} - 6.5V$			V_{SS}−6.0	V
	$V_{DD} = V_{SS} - 9.5V$			V_{SS}−7.0	V
Segment Output Current	$T_A = 25°C$				
(Sa through Sg and Decimal Point)	$V_{OUT} - V_{SS} - 3.6V$, $V_{DD} = -6.5V$	−5.0	−8.5		mA
	$V_{OUT} = V_{SS} - 5V$, $V_{DD} - 8V$		−10.0		mA
	$V_{OUT} = V_{SS} - 6.5V$, $V_{DD} - 9.5V$			−15.0	mA
Ready Output Levels					
Logical High Level (V_{OH})	$I_{OUT} = -0.4$ mA	V_{SS}−1.0			V
Logical Low Level (V_{OL})	$I_{OUT} = 10\ \mu A$			V_{DD}−1.0	V

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
World Time	*(Figure 2)*	0.32	0.75	2.0	ms
Digit Time	*(Figure 2)*	36	83	220	µs
Segment Blanking Time	*(Figure 2)*	2	4.5	14	µs
Digit Output Transition Time (t_{RISE} and t_{FALL})	C_{LOAD} = 100 pF, $R_{LOAD} = 9.6\ k\Omega$		2		µs
Keyboard Inputs High to Low Transition Time after Key Release	C_{LOAD} = 100 pF		4		µs
Ready Output Propagation Time	*(Figure 4)*				
Low to High Level (t_{PDH})	C_{LOAD} = 100 pF	10		50	µs
High to Low Level (t_{PDL})	C_{LOAD} = 100 pF			1	ms
Key Input Time-out	*(Figure 5)*				
Key Entry		2.8	7.0	18	ms
Key Release		5.1	12	32	ms
Display Cutoff Time (The time after the last valid key closure that all numbers will be blanked and all decimal points displayed).		15	35	92	sec



Note 1: Display: Use NSA1198, NSA1298 or NSA0098.

Note 2: Driver: Use DS8864 or DS8873 (with low-battery indicator), or DS8855 or DS8872 (without low-battery indicator).

FIGURE 1. Complete Calculator Schematic

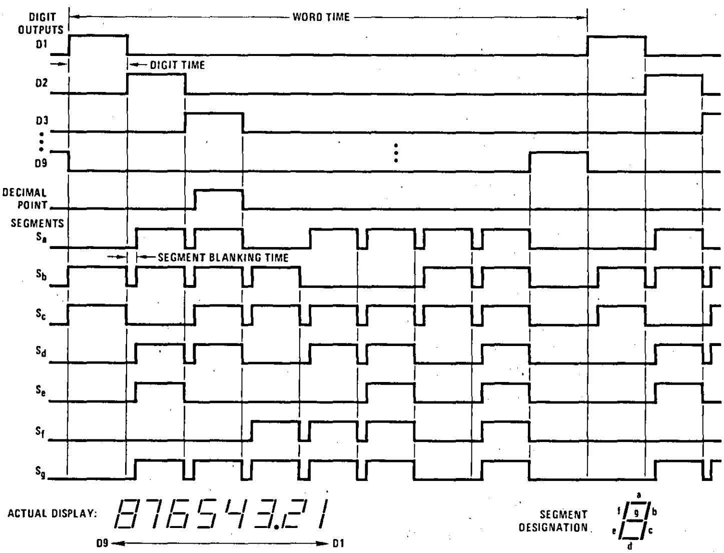


FIGURE 2. Display Timing Diagram

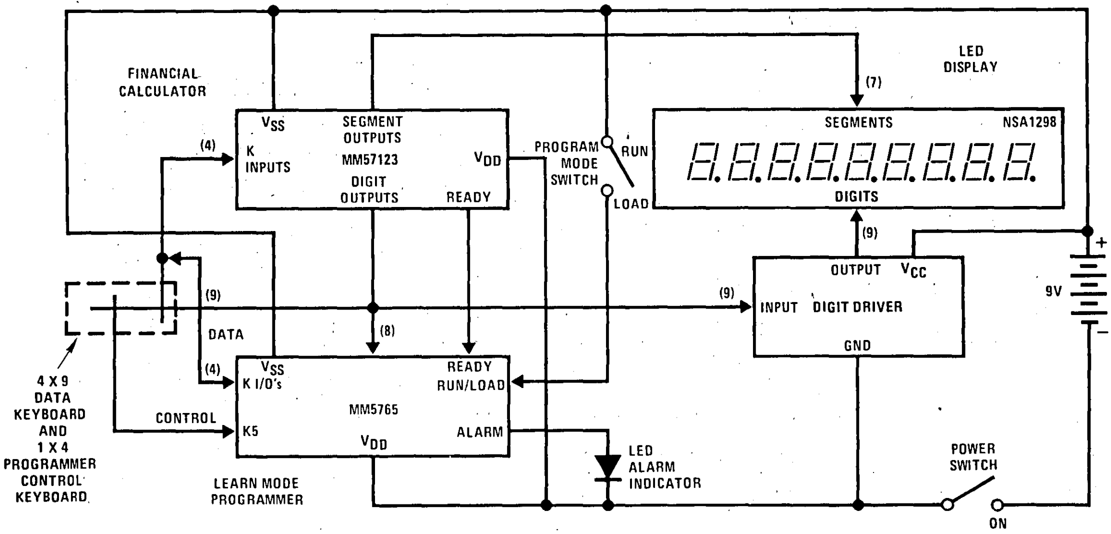


FIGURE 3. Low Cost Hand-Held Programmable Financial Computer Using the MM57123 Calculator and MM5765 Programmer

KEYBOARD BOUNCE AND NOISE REJECTION

The MM57123 is designed to interface with most low cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

A key closure is sensed by the calculator chip when one of the key inputs, K1, K3 or K4 are forced more positive than the Logical High Level specified in the electrical specifications. An internal counter is started as a result of the closure. The key operation begins after nine word times if the key input is still at a Logical High Level. As long as the key is held down (and the key input remains high) no further entry is allowed. When the key input changes to a Logical Low Level, the internal counter starts a sixteen word time-out for key release. During both entry and release time-outs the key inputs are sampled approximately every other word time for valid levels. If they are found invalid, the counter is reset and the calculator assumes the last valid key input state.

One of the popular types of low-cost keyboards available, the elastomeric conductor type, has a key pressure versus contact resistance characteristic that can generate continuous noise during "teasing" or low pressure key depressions. The MM57123 defines a series contact resistance up to 50 kΩ as a valid key closure, assuring a reliable interface for that type of keyboard.

AUTOMATIC DISPLAY CUTOFF

If no key is depressed for approximately thirty-five seconds, an internal automatic display cutoff circuit will blank all segments and display nine decimal points. Any key depression will restore the display; to restore the display without modifying the status of the calculator, use two Change Sign "+/−" key depressions.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state, the output is at a Logical High Level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is completed and the key entry is accepted as valid, then goes low as indicated in *Figures 4 and 5.* It remains at a Logical Low Level until the function initiated by the key is completed and the key is released. The low to high transition indicates the calculator has returned to an idle state and a new key can be entered.

ERROR INDICATION

In the event of an operating error, the MM57123 will display all zeros and all decimal points. The error indication occurs if division by zero is attempted or either a result or intermediate value exceeds 99999999.

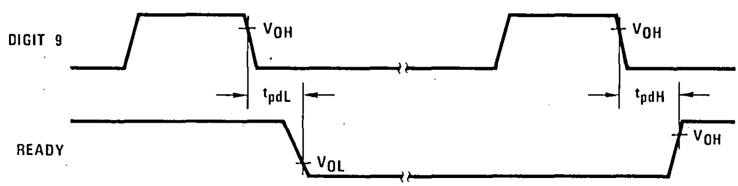


FIGURE 4. Ready Timing

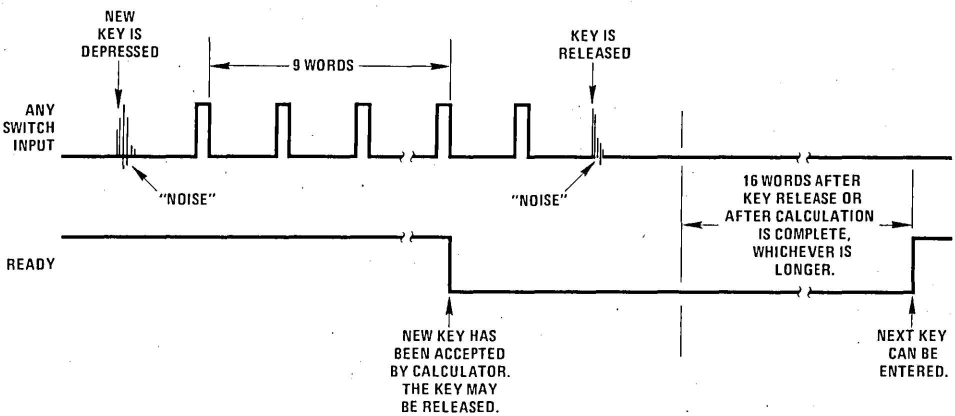


FIGURE 5. Functional Description of Ready Signal and Key Entry.

The indication is cleared by depressing any key.

If an error results from a "+" or "−" key, the X-register is cleared and the last entry is saved in the A-register; all other registers are not effected. An error condition during "x" or "÷" operations clears X without changing any of the other registers.

Overflow as a result of the "POWER," "INT," "SAV" or "LOAN" keys clears the X-register and destroys the values in N, I and A. Y is not changed.

An attempt to raise a negative number to a power will cause the error indication to appear, the X-register will be cleared and the exponent will be stored in Y. The other registers are not changed.

Overflow as a result of "M+" destroys the value stored in M, clears X and displays the error indication. Calculations are immediately stopped and other registers are not cleared.

AUTOMATIC CONSTANT

The MM57123 retains as a constant the first factor of a multiplication calculation or the second factor of a division calculation, when that calculation is terminated by an "=" key or "%" key. Subsequent calculations using the stored constant are made by entering a number and operating upon it with the appropriate terminator ("=," or "%" key). The Y-register is used to store the constant in the constant mode of operation.

The calculator automatically changes to the chain mode when an "x" or "÷" key occurs in the calculation. In the chain mode, the result of each "x" or "÷" key is stored in both X and Y-registers. A new entry replaces X without altering Y. At the completion of a chain calculation, the Y-register will contain the value used as first factor of the last multiply, or the latest entry if the last operation was a divide.

Table I summarizes the four modes.

KEY OPERATIONS

(Note: Register X is always displayed.)

Clear Entry Key, "CE"

Following a number entry or an "MR" key, it clears the X-register only (clear entry). Following any other key it clears registers X, Y and A.

Clear All Key, "CA"

Pressing "CA" once clears all registers including M (memory).

Number Entries

The first entry clears the X-register and enters the number into the LSD of X. Second through eighth entries (excluding a decimal point) are entered one digit to the right of the last number. The ninth, and subsequent entries are ignored. First entry after a "+", "–", "M+" or "M–" following a "+" or "–" key causes the number in the X-register to be transferred to the A-register before clearing and placing the new entry in X.

Decimal Point, "."

At the first depression of a number entry, it clears the X-register and places a point in the leftmost digit. If the previous key was a number, it enters a decimal point to the right of the last number entered. Following a "+", "–" or those keys preceding a "M+" or "M–" key, the X-register is transferred to A, cleared and a decimal point entered in the leftmost digit. The last decimal point depression in a single number entry is accepted as the valid point.

Change Sign Key, "+/–"

Changes sign of register X.

Addition Key, "+"

If the previous key was not a "+" or "–" key, the number in the A-register is added to the X-register, X is transferred to A, and the sum is stored in X. When the last key was a "+" or "–" key, the number in A is added to the number in X without destroying the value of A. The sum is stored in X.

Subtraction Key, "–"

If the previous key was not a "+" or "–" key, the number in the X-register is subtracted from the number in the A-register, X is transferred to A, and the difference is stored in X. When the last key was a "+" or "–" key, the number in A is subtracted from X without destroying the value of A. The result is stored in X.

Multiplication Key, "x"

If there has not been a "x" or "÷" key since the last terminator key ("=" or "%"), the value of the X-register is copied into the Y-register and the calculator is set to the chain multiply mode. In a chain calculation in which there has been an "x" key since the last terminator c "÷" key, X is multiplied by Y and the resulting product is stored in both X and Y; if a "÷" key has occurred since the last terminator or "x" key, depression of "x" will divide the Y-register by the X-register, with the quotient stored in both X and Y.

Division Key, "÷"

If there has not been an "x" or "÷" key since the last terminator key ("=", or "%"), the value of the X-register is copied into the Y-register and the calculator is set to the chain divide mode. In a chain calculation, if an "x" key has occurred since the last terminator or "÷" key, X is multiplied by Y and the product is stored in both X and Y; if a "÷" key has occurred since the last terminator or "x" key, depression of "÷" will divide the Y-register by the X-register, with the quotient stored in both X and Y.

TABLE I. Mode Summary

MODE	KEYS THAT SET MODE	DESCRIPTION (See Calculation Examples)
CONSTANT MULTIPLY	CE = } With calculator previously % } in chain multiply PWR SOD INT SAV LOAN	Depression of an "=" or "%" key will multiply the X-register by the Y-register and replace X with the product. Y remains unchanged.
CHAIN MULTIPLY	X Following a terminator or "÷" or "x" operation	Depression of an "=" or "%" key will multiply the X-register by the Y-register and place the product in X. Y remains unchanged.
CONSTANT DIVIDE	= } With calculator previously % } in chain multiply	Depression of an "=" or "%" key will divide the X-register by the Y-register and replace X with the quotient. Y is unchanged.
CHAIN DIVIDE	÷ Following a terminator or "÷" or "x" operation	Depression of an "=" or "%" key will divide the Y-register by the X-register, transfer X to Y, and place the quotient in X.

Equal Key, "="

In the chain multiply mode, the value in the X-register is multiplied by the Y-register with the product stored in X. Register Y remains unchanged. In the chain divide mode, depression of "=" will divide Y by X, transfer X to Y, and place the quotient in X. If the calculator is in constant multiply, "=" will multiply X by Y, place the product in X and retain Y. For constant divide, the X-register is divided by Y, the quotient is stored in X; Y is unchanged.

Percent Key, "%"

This key acts exactly like the "=" key except the value of X is copied into A, then divided by 100 before performing the required operation.

Square-root Key, "$\sqrt{\ }$"

Depression of this key will compute the square-root of the number contained within the X-register; no other registers are affected. The same results can be achieved by using the power "PWR" key (requires extra key-strokes) as shown in example 12; this allows producing a 20-key calculator (leaving off "CA" and "$\sqrt{\ }$") with no sacrifice in performance.

Function Key, "F"

Depression of this key shifts the entry scheme from a direct or "primary" function mode to the secondary function or "shift key" mode.

Memory Plus Key, "M+" (shift mode)

The number in the X-register is accumulated into the M-register. Registers X and A are not changed, so the repeat addition or subtraction conditions that existed before accumulation to memory are still valid.

Memory Recall Key, "MR" (shift mode)

Following "MR", the value of the M-register is copied into the X-register.

Power Key, "PWR" (shift mode)

When the calculator is in either the chain or constant multiply modes, depression of "PWR" raises the number in the Y-register to the power of the X-register and replaces X with the result. Thus, to raise two to the fifth power use the sequence: "2, X, 5, F, PWR." If the calculator is in the constant or chain divide modes, the value of Y is raised to the inverse of X power; i.e., the key sequence "5, ÷, 2, F, PWR" results in the calculation of 5 raised to the 1/2 power. The original value of X is retained in Y and register A is cleared. The calculator is set to the constant multiply mode. Results computed with the "PWR" key are rounded to five places.

Exchange Key, "EX" (shift mode)

The X and Y-registers are exchanged. No other registers are effected.

Interest Entry Keys "I" and "I/12" (shift mode)

"I" divides the number by 100 and stores the quotient in X and the I-register. "I/12" divides by 1200 and stores the quotient in both X and I; i.e., the interest will be compounded monthly.

Number of Periods Entry Keys, "N" and "12N" (shift mode)

The "N" key copies X directly into register N. The "12N" key multiplies X by 12; the product is stored in register N and displayed in X.

Amount Entry Key, "AMT" (shift mode)

The value of the X-register is copied into the Y-register. No other registers are effected.

"INT" (compound interest) Keys, "FV" and "PV" (shift mode)

The "INT-FV" key will compute future value: the sum of money available at the end of n periods from the present date (N-register) that is equivalent to the present amount (Y-register) with interest i (I-register). The "INT-PV" key will compute present value: the sum of money necessary today to accumulate the future amount contained in Y over n periods stored in N at the interest rate per interest period that is stored in I. Thus, to compute future value, simply enter i, n, and amount in any order and press "INT-FV". For present value, press "INT-PV". Registers Y, N and I are not altered; X is replaced by the computed value and register A is cleared. The calculator is set to the constant multiply mode.

Savings Deposit Keys, "SAV-PMT" and "SAV-FV" (shift mode)

The "SAV-PMT" key will compute the amount to be deposited at the end of each period in a *sinking fund* for the number of periods, n, contained in register N, at an interest rate, i, contained in register I, compounded each time period, to accumulate the desired amount, contained in register Y. The "SAV-FV" key will compute the amount in a *sinking fund*. The number in Y is deposited at the end of n time periods (N-register) at an interest rate per time period i (I-register), compounded each time period. Thus, to compute the required *sinking fund deposit* to accumulate a desired amount over a given period of time, enter i, n and the amount in any order using the "I," "N" and "AMT" keys, then "SAV-PMT". To find the amount in the *sinking fund,* simply enter i, n and the periodic amount of deposit and press "SAV-FV". Registers N, I or Y are not altered by the calculation, register A is cleared and register X contains the computed value. The calculator is set to the constant multiply mode.

Loan Installment Keys, "LOAN-PMT" and "LOAN-AMT" (shift mode)

The "LOAN-PMT" key will compute the end-of-period payment or receipt required over the number of time periods contained in the N-register at an interest rate per time period equal to the value in the I-register to support a loan equal to the amount stored in the Y-register. "LOAN-AMT" computes the amount that can be loaned for a given end-of-period payment stored in Y over the number of time periods contained in N at the interest rate per time period of I, compounded each time period. Thus, to compute the required installment on a given loan, enter the amount of the loan using the "AMT" key, the interest rate using "I" and the number of periods with "N", then press "LOAN-PMT". To compute how much can be borrowed given a fixed payment, enter the payment amount, number of periods and interest rate, then "LOAN-AMT". "AMT", "I", or "N" can always be entered in any order. Registers N, I or Y are not altered by the calculation; register A is cleared and register X will contain the computed value. The calculator is set to the constant multiply mode.

NOTE: in the above explanations, only "I" and "N" have been referenced for simplicity; these relate to interest per period ("I") and number of periods ("N"). In business sense, a period can be either one-month (i.e., interest compounded monthly) or one year (interest rate is compounded yearly, use the "I" key, if monthly, use the I/12 key. Correspondingly, the "N" key (for number of periods) should be used whenever "I" is used and 12N whenever I/12 is used. The only exception would be if the interest were given as monthly for a period of less than one year; in this case, use "I" and "N".

Sum-of-Digits Key, "SOD" (shift mode)

Following a "+" or "−" key, it transfers the number in register X to register A and computes a *first sum-of-digits* depreciation on that number by multiplying it by the ratio of the number in the N-register to the sum-of-digits of N. The result is stored in X; the difference between the initial and final values of X, the *depreciable value,* is stored in registers Y and A. N is decremented by one. (Therefore, to find depreciable value, simply use the "EX" key.) Subsequent depressions of the "SOD" key will compute successive depreciation and depreciable value amounts using the original value of N and present values stored in N and A. N is decremented by one after each computation. The number to be depreciated (or the loan amount in a "Rule of 78's" interest calculation) is always entered with a "+" or "−" key and the number of periods with the "N" key, without regard to key order. If the key preceding "SOD" is not "+" or "−," the sum-of-digits computation is performed on the number in the A-register without the number in X first being transferred to A. Calculator mode is set to constant multiply.

examples

1. Addition or Subtraction 2.0, 3.2, −12.3

KEYS	DISPLAY	COMMENTS
2	2	
+	2.	
3	3	
.	3.	
2	3.2	
+	5.2	
1	1	
2	12	
.	12.	
3	12.3	
−	−7.1	Note adding machine notation

2. Repeat Add or Subtract

KEYS	DISPLAY	COMMENTS
3	3	
.	3.	
1	3.1	
+	3.1	
+	6.2	
+	9.3	
−	6.2	

3. Chain Multiplication or Division

KEYS	DISPLAY	COMMENTS
a) 1	1	
x	1.	
2	2	
x	2.	
3	3	
.	3.	
1	3.1	
x	6.2	
4	4	
.	4.	
2	4.2	
=	26.04	
b) 1	1	
0	10	
÷	10.	
2	2	
÷	5.	
1	1	
0	10	
÷	.5	
2	2	
=	.25	
c) 2	2	
0	20	
x	20.	
4	4	
÷	80.	

examples (Continued)

8	8	
÷	10.	
7	7	
x	1.4285714	
4	4	
=	5.7142856	

4. Constant Multiplication or Division

	KEYS	DISPLAY	COMMENTS
a)	3	3	
	x	3.	
	2	2	
	=	6	
	4	4	
	=	12.	First factor in constant multiply
	5	5	
	.	5.	
	2	5.2	
	=	15.6	
	=	46.8	15.6 is re-entered and multiplied by constant
b)	5	5	
	÷	5.	
	2	2	
	=	2.5	
	4	4	
	=	2.	Second factor in constant divide
	5	5	
	.	5.	
	2	5.2	
	=	2.6	
	=	1.3	2.6 is re-entered and divided by constant

5. To Perform Products of Sums
(5+4) x (3+2)/(6+7) = ?

KEYS	DISPLAY	COMMENTS
5	5	
+	5.	
4	4	
+	9.	
x	9.	Chain multiply mode is set
3	3	
+	3.	
2	2.	
+	5.	
÷	45.	(5+4)x(3+2) is executed
6	6	
+	6.	
7	7	
+	13.	
=	3.4615384	45 ÷ (6+7) is executed

6. Calculate Percentage

KEYS	DISPLAY	COMMENTS
3	3	
0	30	
0	300	
.	300.	
2	300.2	
5	300.25	
x	300.25	
5	5	
%	15.0125	"Live %" key

7. Perform Add On and Discount

	KEYS	DISPLAY	COMMENTS
a)	Add-On: $125 plus 5%		
	1	1	
	2	12.	
	5	125.	
	x	125.	
	5	5	
	%	6.25	5% of 125 is displayed
	+	131.25	125+5% is displayed
b)	Discount: $532.10 by 6%		
	5	5	
	3	53	
	2	532	
	.	532.	
	1	532.1	
	x	532.1	
	6	6	
	%	31.96	6% of 532.1 is displayed
	–	500.174	532.1 – 6% is displayed

8. Perform Change Sign

KEYS	DISPLAY	COMMENTS
1	1	
2	12	Change sign does not terminate entry.
+/–	–12	
3	–123	
.	–123.	
+/–	123.	
5	123.5	
+/–	–123.5	
6	–123.56	

9. Perform Exchange Registers (X↔Y)

	KEYS	DISPLAY	COMMENTS
a)	5	5	
	x	5.	
	3	3	
	=	15.	5 is initially constant multiplier
	4	4	
	F, EX	5.	4 is now constant multiplier
	=	20	

examples (Continued)

b)

KEYS	DISPLAY	COMMENTS
6	6	
÷	6.	
3	3	
F, EX	6.	Numerator and denominator are exchanged.
=	.5	

10. Accumulate in Memory, Recall and Clear Memory

KEYS	DISPLAY	COMMENTS
a) 3	3	
F, M+	3	Accumulate in memory
4	4	
F, M+	4	Accumulate in memory
F, MR	7	Recall memory
F, MC	7	Clear memory
F, MR	0	Recall memory
b) 5	5	
+	5	
6	6	
+	11	
F, M+	11	Accumulate in memory
7	7	
+	18	
F, M+	18	11+18 is accumulated in M
+	25	Repeat add
3	3	
2	32	
.	32.	
2	32.2	
+/−	−32.2	
F, M+	−32.2	29−32.2 is accumulated in M
9	9	
+	34	
F, MR	−3.2	Accumulated value of M is recalled
+	30.8	
F, MC	30.8	M is cleared
F, MR	0	M = 0

11. Raising a Number to a Power

KEYS	DISPLAY	COMMENTS
a) $2^5 = 32$		
2	2	
x	2	
5	5	
F, PWR	32	
b) $5^{1.5} = 11.18$		
5	5	
x	5	
1	1	
.	1.	
5	1.5	
F, PWR	11.18	Rounded to 5 digits; trailing zero is suppressed
c) $3^{-5} = 0.00412$		
3	3	
x	3	
5	5	
+/−	−5	Change sign
F, PWR	.00412	Rounded to five digits

12. Calculating Roots

KEYS	DISPLAY	COMMENTS
a) $2\sqrt{5} = 2.2361$		
5	5	
÷	5	
2	2	
F, PWR	2.2361	Rounded to five digits
b) $3\sqrt{6} = 1.8171$		
6	6	
÷	6	
3	3	
F, PWR	1.8171	Rounded to five digits

financial examples

1. Future Value Compound Interest Computations

To find the accumulated amount in a savings account at the end of 9 years when a) $2,500 is deposited at 5.25% interest compounded monthly, b) $3,000, c) $3,000 at 5% interest, d) $3,000 at 5% interest for 10 years.

KEYS	DISPLAY	COMMENTS
a) 9	9	Number of years
F, 12N	108	Compounded monthly, stored in N
5.25	5.25	
F, I/12	.004375	Compounded monthly, stored in I
2500	2500	Original deposit
F, AMT	2500	Stored in Y
F, INT-FV	4005.8665	Future value
b) 3000	3000	New deposit amount
F, AMT	3000	New deposit stored in Y
F, INT-FV	4807.0398	Future value
c) 5	5	New interest rate
F, I/12	.00416666	New interest rate stored in I
F, INT-FV	4700.5347	Future value
d) 10	10	New number of years
F, 12N	120	Compounded monthly, stored in N
F, INT-FV	4941.0234	Future value

2. Present Value Compound Interest Computations

To find the amount to be deposited to accumulate a) $5,000 in 7 years at 4.5% interest compounded monthly b) $10,000, c) $10,000 in 7.5 years.

financial examples (Continued)

KEYS	DISPLAY	COMMENTS
a) 7	7	Number of years
F, 12N	84	Compounded monthly, stored in N
4.5	4.5	Interest
F, I/12N	.00375	Compounded monthly, stored in I
5000	5000	Future value
F, AMT	5000	Future value stored in Y
F, INT-PV	3651.0957	Present value required
b) 10000	10000	New future value
F, AMT	10000	Futue value stored in Y
F, INT-PV	7302.1914	Present value required
c) 7.5	7.5	New number of years
F, 12N	90	Compounded monthly, stored in N
F, INT-PV	7140.0271	Present value required

3. Savings Computations – Period Payments

To find the amount that a) must be deposited monthly in a savings account at an interest rate of 5.5% compounded monthly for 5 years to accumulate $15,000, b) compounded, and deposited quarterly.

KEYS	DISPLAY	COMMENTS
a) 5.5	5.5	Interest
F, I/12	.00458333	Compounded monthly, stored in I
5	5	Number of years
F, 12N	60	Compounded monthly, stored in N
15000	15000	Future value
F, AMT	15000	Future value stored in Y
F, SAV-PMT	217.7676	Monthly deposit required
b) 5.5	5.5	Interest
÷	5.5	
4	4	Compound quarterly
=	1.375	
F, I	.01375	Quarterly interest stored in I
5	5	Number of years
x	5	
4	4	Compound quarterly
=	20	
F, N	20	Quarter periods, stored in N
15000	15000	Re-enter future value
F, AMT	15000	Future value stored in Y
F, SAV-PMT	656.7085	Quarterly deposit required

4. Savings Computations – Accumulated Value

To find the amount accumulated a) if $100 is deposited at the end of each month for 6 years in a savings account at an interest rate of 4.75%, compounded monthly, b) 7.5%, c) at 4.75% for 9 years.

KEYS	DISPLAY	COMMENTS
a) 4.75	4.75	Interest
F, I/12	.00395833	Compounded monthly, stored in I
6	6	Number of years
F, 12N	72	Compounded monthly, stored in N
100	100	Monthly payment
F, AMT	100	Monthly payment stored in Y
F, SAV-FV	8311.9301	Accumulated sinking fund
b) 7.5	7.5	New interest rate
F, I/12	.00625	Compounded monthly, stored in I
F, SAV-FV	9057.8807	Accumulated sinking fund
c) 4.75	4.75	New interest rate
F, I/12	.00395833	Compounded monthly, stored in I
9	9	New number of years
F, 12N	108	Compounded monthly, stored in N
F, SAV-FV	13443.173	Accumulated sinking fund

5. Loan Computations – Monthly Payment

To find the monthly payments of a loan of $5,000 paid over 5 years at an annual percentage rate of a) 18%, b) 12%, c) 7.5% for 10 years.

KEYS	DISPLAY	COMMENTS
a) 18	18	Interest rate
F, I/12	.015	Compounded monthly, stored in I
5	5	Number of years
F, 12N	60	Compounded monthly, stored in N
5000	5000	Loan amount
F, AMT	5000	Loan amount stored in Y
F, LOAN-PMT	126.9671	Monthly installment
b) 12	12	New interest rate
F, I/12	.01	Compounded monthly, stored in I
F, LOAN-PMT	111.22225	New monthly installment
c) 7.5	7.5	New interest rate
F, I/12	.00625	Compounded monthly, stored in I
10	10	New number of years
F, 12N	120	Compounded monthly, stored in N
F, LOAN-PMT	59.35085	New monthly installment

financial examples (Continued)

6. Loan Computations – Loan Amount

To find the amount of a loan with monthly payments of $125, and an interest rate of 9% for 3 years, b) 4 years, c) $120 for 4 years.

KEYS	DISPLAY	COMMENTS
a) 9	9	Interest rate
F, I/12	.0075	Compounded monthly, stored in I
3	3	Number of years
F, 12N	36	Compounded monthly, stored in N
125	125	Payment amount
F, AMT	125	Payment amount stored in Y
F, LOAN-AMT	3930.8485	Computed loan amount
b) 4	4	New number of years
F, 12N	48	Compounded monthly, stored in N
F, LOAN-AMT	5023.0982	Computed loan amount
c) 120	120	New payment amount
F, AMT	120	New payment stored in Y
F, LOAN-AMT	4822.1742	Computed loan amount

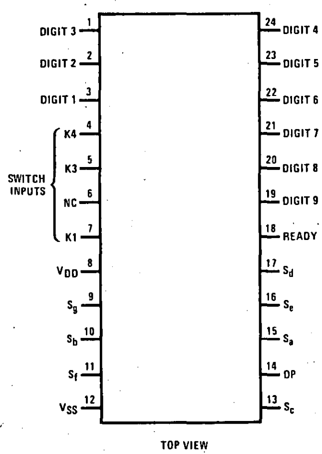
7. Performing a Sum-of-Digits Depreciation

Find the depreciation and depreciable value for each year, on an item with an initial cost of $3,500.00 and a salvage value at the end of 8 years of $675.00.

KEYS	DISPLAY	COMMENTS
3500	3500	
+	3500	Enter initial value
675	675	Enter salvage value
–	2825.	Calculate change
8	8	
F, N	8.	Enter period in N
F, SOD	627.77777	1st year depreciation
F, EX	2197.2223	Depreciable value
F, SOD	549.30557	2nd year depreciation
F, EX	1647.9168	Depreciable value
F, SOD	470.83396	3rd year depreciation
F, EX	1177.0835	Depreciable value
F, SOD	392.36116	4th year depreciation
F, EX	784.7224	Depreciable value
F, SOD	313.88896	5th year depreciation
F, EX	470.83344	Depreciable value
F, SOD	235.41672	6th year depreciation
F, EX	235.41672	Depreciable value
F, SOD	156.94447	7th year depreciation
F, EX	78.47225	Depreciable value
F, SOD	78.47225	8th year depreciation
F, EX	0.	Depreciable value

connection diagram

Dual-In-Line Package



Order Number MM57123N
See Package 22

MM57135 scientific calculator ROM

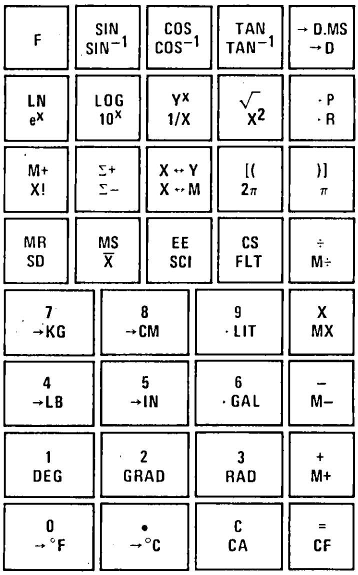
general description

The MM57135 Control ROM is programmed to perform the functions described when used with the MM5782 Processor and RAM chip. Complete electrical specifications and application data may be found in the MM5781 and MM5782 data sheet.

features

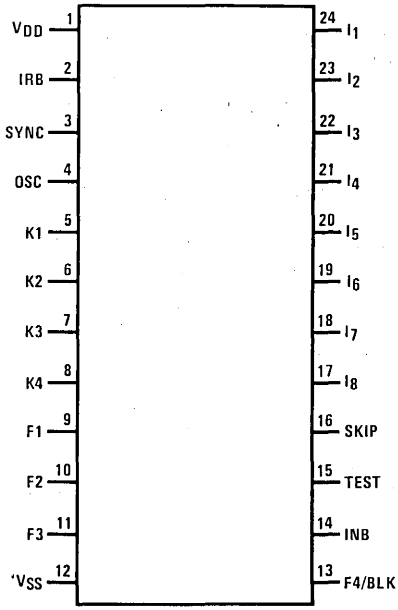
- Enters and displays ±9.999999999 x 10^{99} to ±1 x 10^{-99}
- Calculates internally using 12 mantissa digits to insure all ten displayed digits are correct
- Left justified entry with trailing zero suppression
- Algebraic Notation with 2 levels of parentheses
- Arithmetic functions: +, −, X, ÷, 1/X, $\sqrt{X}$, X^2
- Constant operations (second factor)
- Power function: Y^X
- Logarithmic functions: LN X, LOG X, e^x, 10^x
- Trigonometric functions: SIN, COS, TAN, SIN^{-1}, COS^{-1}, TAN^{-1}
- Compute in degrees, radians or gradian mode
- Rectangular/Polar conversions
- Degrees, minutes, seconds conversions
- 3 full-function, addressable memories
- Statistical functions: standard deviation and mean
- 2 display output modes: floating or scientific
- Factorial: n!
- Conversions: °F/°C, LB/KG, IN/CM and GAL/LITERS
- π, change sign, clear-all and exchange
- Auto power-on clear

keyboard



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM57135N
See Package 22

Keyboard Matrix, Primary Functions

SWITCH INPUTS	DIGIT TIMING STATES									
	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
K1		1	2	3	0	•	C	+	=	
K2		4	5	6	7	8	9	−	X	
K3	MR	MS	EE	CS	Σ+	X↔Y	[(	÷	)]	M+
K4	LN	LOG	Y^X	$\sqrt{}$	SIN	COS	TAN	R→P	→D.MS	F

functional description

REGISTER CONFIGURATION

The user has access to 7 registers designated X, Y, P1, P2, M1, M2 and M3. X is the display and entry register. Y is the constant register. M1, M2 and M3 are independent user-addressable memory registers that can be stored, recalled, added, multiplied, subtracted or divided with X. P1 and P2 are parentheses registers.

All registers contain 12 mantissa digits with sign and 2 exponent digits with sign.

DISPLAY CONFIGURATION

The X-register is always displayed and shown as 10 digits of mantissa with sign and 2 digits of exponent with sign. All internal calculations are done with 12 digits and displayed rounded to ten; therefore, all displayed digits are accurate for all functions. Numbers are entered left justified with trailing zeros suppressed.

DISPLAY FORMAT

Floating point display output format is selected at power-on or by pressing "F", "FLT". If X is greater than 9999999999. or less than 0.000000001, the display is automatically in scientific notation.

By pressing "F", "EE" all results are displayed in scientific notation.

All results maintain 12 digits internally at all times.

BATTERY LOW INDICATION

The DS8664 digit driver can sense a low battery voltage condition and send a signal to input IRB of the MM5781 which causes the display to show an "L" in the left-most sign position.

READY SIGNAL OPERATION

Output FIP of the MM5781 can be used as a "ready signal" to indicate calculator status. It can be useful in providing synchronization information during testing and if used with other logic.

When the calculator is in the "idle state" and ready to accept a key, FIP is high (near V_{SS}). It remains high until a key is depressed and accepted, then goes low. It stays low until the calculation is complete then returns to a high state which signifies a new key may be entered.

KEYBOUNCE AND NOISE REJECTION

When a key is depressed, a time-out is started. A key is accepted as valid if it remains depressed for approximately 12 ms. The key must be released for at least 12 ms before a new key can be entered.

ERROR CONDITIONS AND INDICATION

In the event of an illegal operation, the calculator will display "Error" and X will be cleared. All other registers and memories are protected. Any key depressed after an error will use X = 0 for the next operator. Table I summarizes results and operations that will give an error indication.

RANGE, ACCURACY AND SPEED

All functions work over the mathematically allowable range defined by Table I.

Transcendental functions give 10 digits of accuracy except near normal limits and all other functions are internally accurate to 12 digits.

The calculation time of all transcendental functions takes less than a second; all other functions, with the exception of factorial computations, are executed in less than 1/3 second. Factorial of 69, the longest calculation possible, takes less than 3 seconds.

TABLE I. Results and Operations that Result in an Error Indication

Results $> 9.999999999 \times 10^{99}$
Results $< 1 \times 10^{-99}$
Division by 0
LOG, LN ≤ 0
Y^X for $Y \leq 0$
TAN, SIN, COS $\geq$ 25 revolutions (9000°)
TAN of 90°, 270°, etc.
SIN^{-1}, $COS^{-1} > 1$ or $\leq 10^{-50}$
$\sqrt{X} < 0$
DMS Conversion $\geq 10^{10}$
X! < 0, or not an integer
More than two open parentheses
More closed parentheses than open parentheses

functional description (con't)

KEY OPERATIONS

Clear Key, "C"

a) After number keys: copies Y to X
b) After function key: clears all modes and X, Y, P1 and P2
c) After "F": clears all modes and all registers

Number Keys, "0" ~ "9," "•"

a) After any function key: clears X and enters number left justified to X
b) After any number key: enters next number. All entries after tenth are ignored
c) After "EE": enters number to exponent. Last two entries are used
d) After "F":

(→°C)	"•"	Converts X in °F to °C (°C = (°F – 32)/1.8)
(→°F)	"0"	Converts X in °C to °F (°F = 1.8°C + 32)
(DEG)	"1"	Set calc to degrees mode
(GRAD)	"2"	Set calc to gradians mode
(RAD)	"3"	Set calc to radians mode
(→ LB)	"4"	Replace X with X ÷ 0.4535924
(→ IN)	"5"	Replace X with X ÷ 2.54
(→ GAL)	"6"	Replace X with X ÷ 3.785412
(→ KG)	"7"	Replace X with X • 0.4535924
(→ CM)	"8"	Replace X with X • 2.54
(→ LIT)	"9"	Replace X with X • 3.785412

e) 1, 2, 3 after:

"MR"	Recall selected memory to X
"MS"	X to selected memory
"M+ mode"	M + X to selected memory
"M– mode"	M – X to selected memory
"MX mode"	M • X to selected memory
"M÷ mode"	M ÷ X to selected memory
"MEXC mode"	X is exchanged with selected memory

Change Sign Key, "CS"

a) After "EE": change sign of exponent of X
b) After "F": (FLT) set calc to Floating Point mode
c) After any other key: changes sign of X mantissa

Positive/Negative Summing Key, "Σ+/Σ–"

a) Used to enter data points for computation of mean and standard deviation:
   Sums X to M1 (Σx)
   Sums X^2 to M2 (Σx^2)
   Adds 1 to M3 (N)
b) After "F": (Σ–) used to delete data points:
   Subtracts X from M1
   Subtracts X^2 from M2
   Subtracts 1 from M3

Accumulative/Factorial Key, "M+/X!"

a) Sums X to M1
b) After "F": (X!) replaces X with X-factorial

Coordinate Conversion Key, "R ↔ P"

a) Converts contents of X and Y in rectangular coordinates to polar coordinates: reset calculator mode

$\sqrt{X^2 + Y^2}$ to Y

TAN^{-1} Y/X to X

b) After "F": (P → R) converts contents of X and Y in polar coordinates to rectangular coordinates: resets calculator mode:
   Y SIN X → Y
   Y COS X → X
   Note: R ↔ P works in all four quadrants

Square Root/Square Key, "$\sqrt{X}/X^2$"

a) Square root of positive value of X to X
b) After "F": (X^2) X-squared to X

Second Function Key, "F"

Sets F mode

Memory Store/Mean Key, "MS/$\bar{X}$"

a) Sets memory store mode
b) After "F": ($\bar{X}$) divides M1 by M3 and puts result in X; this gives mean of data summed using Σ+ key

Memory Recall/Standard Deviation Key, "MR/SD"

a) Sets Memory Recall mode
b) After F: (S.D.) computes standard deviation of data entered with the Σ+ key, using the relationship:

$$SD = \sqrt{\frac{\Sigma X^2 - \frac{(\Sigma X)^2}{N}}{N-1}} \equiv \sqrt{\frac{M2 - \frac{(M1)^2}{M3}}{M3 - 1}} \rightarrow X$$

ΣX, ΣX^2 and N may be recovered from M1, M2 and M3

Enter Exponent Key, "EE/SCI"

a) Sets enter exponent mode, displaying 00 in exponent position
b) After F: (SCI) sets the calculator to display using scientific notation

Common Log Key, "LOG/10^x"

a) Common logarithm of X to X (base 10)
b) After "F": (10^x) 10^x to X

Natural Log Key, "Ln/e^x"

a) Natural logarithm of X to X (base e)
b) After "F": (e^x) e^x to X

functional description (con't)

Decimal to Degrees Conversion Key, "D.MS"

a) Replaces the decimal angle in X with its degrees (or hours), minutes and seconds conversion
b) After "F": (DMS) degrees (or hours) minutes and seconds in X is converted to decimal angle

Trigonometric Keys, "SIN, COS, TAN"

a) Replaces the decimal angle in X with the indicated trigonometric function
b) After "F": replaces X with the decimal angle of the indicated inverse trigonometric function

Power/Reciprocal Key, "Y^X/1/X"

a) If not in chain mode: copy X to Y set Y^X chain mode
b) After "+, −, X, ÷, Y^X key: copy X to Y, set Y^X chain mode
c) In chain mode: perform the specified function of X and Y putting the result to X and Y, set Y^X chain mode
d) After "F": reciprocal of non-zero value of X to X

The Four Function Keys, "+, −, X, ÷"

a) If not in chain mode: copy X to Y, set the specified chain mode
b) After "+, −, X, ÷, Y^X " key: copy X to Y, set chain mode
c) In chain mode: perform the specified function of X and Y putting the result to X and Y, set the specified chain mode
d) After "F," "MS" or "MR": set the appropriate memory mode (M+, M−, MX, M÷)

Equal Key, "="

a) In chain mode: perform the specified function of X and Y, putting the result to X and save the last number displayed in Y, set the constant mode
b) In constant mode: perform the specified function of X, Y putting the result in X
c) After "F": (CF) reset F mode

Exchange Key, "X ↔ Y/X ↔ M"

a) Exchange X and Y
b) After "MS," "MR" or "F": (X ↔ M) sets calculator to MEXC mode

Open Parentheses, "[(/2π"

a) Copy P1 to P2, copy Y to P1. Copy P1 mode to P2 mode, copy the calculator mode to P1 mode, reset calculator mode
b) After "F": (2π) enter 2 Pi to X (6.283185307)

Close Parentheses/Pi Key, ")]/π"

a) In chain mode: perform the specified function of X, Y putting the result to X. Copy P1 to Y, copy P2 to P1, clear P2. Copy P2 mode to P1 mode, copy P1 mode to the calculator mode, reset P2 mode
b) Not in chain mode: P1 to Y, P2 to P1, clear P2, P1 mode to calculator mode, P2 mode to P1 mode, reset P2 mode
c) After "F": (π) enter Pi to X (3.14159765359)

TABLE II. Example Showing Parentheses Registers and Modes

$6 \text{ X } (2^{(8-5)} + 2)$

	X	Y MODE	P1 MODE	P2 MODE
6	6			
X	6	6 X		
(	6	6	6 X	
2	2	6	6 X	
Y^X	2	2 Y^X	6 X	
(	2	2	2 Y^X	6 X
8	8	2	2 Y^X	6 X
−	8	8 −	2 Y^X	6 X
5	5	8 −	2 Y^X	6 X
)	3	2 Y^X	6 X	
+	8	8 +	6 X	
2	2	8 +	6 X	
)	10	6 X		
=	60	10 X (const)		

10 is constant multiplier

Calculators

MM57136 RPN scientific calculator control ROM

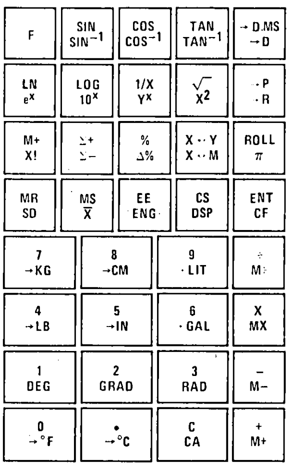
general description

The MM57136 Control ROM is programmed to perform the functions described when used with the MM5782 Processor and RAM chip. Complete electrical specifications and application data may be found in the MM5781 and MM5782 data sheet.

features

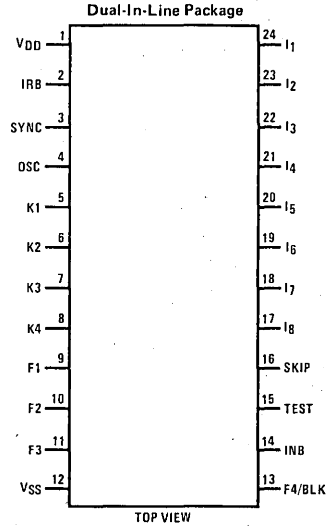
- Enters and displays ±9.999999999 X 10^{99} to ±1 X 10^{-99}
- Calculates internally using 12 mantissa digits to insure all ten displayed digits are correct
- Left justified entry with trailing zero suppression
- Reverse Polish Notation (RPN)
- Arithmetic functions: +, –, X, ÷, 1/X, $\sqrt{X}$, X^2
- Power function: Y^X
- Logarithmic functions: LN X, LOG X, e^X, 10^X
- Trigonometric functions: SIN, COS, TAN, SIN^{-1}, COS^{-1}, TAN^{-1}
- Compute in degrees, radians or gradian mode
- Rectangular/Polar conversions
- Degrees, minutes, seconds conversions
- 3 full-function, addressable memories
- 4-register working stack with ROLL, CLEAR and EXCHANGE capability
- Statistical functions: standard deviation and mean
- 4 display output modes: floating, scientific, fixed or engineering
- Factorial: n!
- Conversions: °F/°C, LB/KG, IN/CM and GAL/LITERS
- π, change sign and clear-all
- Percent and percent difference functions: %, Δ%
- Auto power-on clear
- Auto display cut-off for extended battery life

keyboard



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM57136N
See Package 22

Keyboard Matrix, Primary Functions

SWITCH INPUTS	DIGIT TIMING STATES								
	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
K1		1	2	3	0	•	C	–	+	
K2		4	5	6	7	8	9	X	÷	
K3	MR	MS	EE	CS	Σ+	%	EXC	EN	ROLL	M+
K4	LN	LOG	1/X	√	SIN	COS	TAN	R → P	→ D.MS	F

functional description

REGISTER CONFIGURATION

The user has access to 7 registers designated X, Y, Z, T, M1, M2 and M3. X is the display and entry register and the bottom of an "operational" stack that includes Y, Z and T. M1, M2 and M3 are independent user-addressable memory registers that can be stored, recalled, added, multiplied, subtracted, divided or exchanged with X.

All registers contain 12 mantissa digits with sign and 2 exponent digits with sign.

DISPLAY CONFIGURATION

The X-register is always displayed and shown as 10 digits of mantissa with sign and 2 digits of exponent with sign. All internal calculations are done with 12 digits and rounded to ten; therefore, all displayed digits are accurate for all functions. Numbers are entered left justified with trailing zeros suppressed.

DISPLAY FORMAT

Floating point display output format is selected at power-on or by pressing "F", "DS", ".". If X is greater than 9999999999. or less than 0.1, the display is automatically in scientific notation.

The number of decimal places displayed can be selected by pressing "F", "DSP" and a number key (0–9). The display is rounded to the selected decimal position. A result too large or small to show with the selected position is displayed in scientific notation.

By pressing "F", "ENG" all results are displayed in modified scientific notation with exponents of 10 that are multiples of 3.

All results maintain 12 digits internally at all times. Only the display is affected when "DS" is used to reduce the number of decimal positions. The unrounded result may be viewed by returning to the floating point mode.

DISPLAY CUT-OFF

If no key is depressed for approximately 32 seconds, an internal display cut-off circuit will turn off the entire display except for segments C, D, E and G of the left-most digit. Depression of any key will restore the display. Input INB of the MM5781 must be wired to V_{DD} to enable the display cut-off feature. If INB is left floating, no display cut-off will occur.

BATTERY LOW INDICATION

The DS8664 digit driver can sense a low battery voltage condition and send a signal to input IRB of the MM5781, which causes the display to flash an "L" in the left-most sign position.

READY SIGNAL OPERATION

Output FIP of the MM5781 can be used as a "ready signal" to indicate calculator status. It can be useful in providing synchronization information during testing and if used with other logic.

When the calculator is in the "idle state" and ready to accept a key, FIP is high (near V_{SS}). It remains high until a key is depressed and accepted, then goes low. It stays low until the calculation is complete, then returns to a high state which signifies a new key may be entered.

KEYBOUNCE AND NOISE REJECTION

When a key is depressed, a time-out is started. A key is accepted as valid if it remains depressed for approximately 12 ms. The key must be released for at least 12 ms before a new key can be entered.

ERROR CONDITIONS AND INDICATION

In the event of an illegal operation, the calculator will display "Error" and X will be cleared. The other registers in the stack and all memories are protected. Any key depressed after an error will use X = 0 for the next operator. Table 2 summarizes results and operations that will give an error indication.

TABLE II. Results and Operations that Result in an Error Indication

Results $> 9.999999999 \times 10^{99}$
Results $< 1 \times 10^{-99}$
Division by 0
LOG, LN ≤ 0
Y^X for $Y \leq 0$
TAN, SIN, COS > 25 revolutions (9000°)
TAN of angles at or near $\pm\infty$ asymptotes
SIN^{-1}, $COS^{-1} > 1$ or $\leq 10^{-50}$
$\sqrt{X} < 0$
DMS Conversion $\geq 10^{10}$
X! < 0, not an integer, or > 69

RANGE, ACCURACY AND SPEED

All functions work over the mathematically allowable range defined by Table II.

Transcendental functions give 10 digits of accuracy except near normal limits and all other functions are internally accurate to 12 digits.

The calculation time of all transcendental functions takes less than a second; all other functions, with the exception of factorial computations, are executed in less than 1/3 second. Factorial of 69, the longest calculation possible, takes less than 3 seconds.

functional description (con't)

t	T		
z	Z	m3	M3
y	Y	m2	M2
x	X	m1	M1

FIGURE 1. User Register Configuration

KEY OPERATIONS

Clear Key, "C"

a) Pushes down stack and clears T. Four "C" depressions will clear a completely full stack
b) After "F": Clears all registers including the memories

Number Keys, "0" ~ "9," "•"

a) After any function key except "EN": pushes up stack, clears X and enters number left justified to X
b) After any number key: enters next number. All entries after tenth are ignored
c) After "EE": enters number to exponent. Last two entries are used
d) After "EN": clears X and enters number in X
e) After "DS": load decimal select position for fixed decimal output mode
f) After "F":

(→°C) "•"	Converts X in °F to °C ($°C = (°F - 32)/1.8$)
(→°F) "0"	Converts X in °C to °F ($°F = 1.8°C + 32$)
(DEG) "1"	Set calc to degrees mode
(GRAD) "2"	Set calc to gradians mode
(RAD) "3"	Set calc to radians mode
(→LB) "4"	Replace X with X ÷ 0.4535924
(→IN) "5"	Replace X with X ÷ 2.54
(→GAL) "6"	Replace X with X ÷ 3.785412
(→KG) "7"	Replace X with X • 0.4535924
(→CM) "8"	Replace X with X • 2.54
(→LIT) "9"	Replace X with X • 3.785412

g) 1, 2, 3 after:

"MR"	Push up stack, recall selected memory to X
"MS"	X to selected memory
"M+ mode"	M + X to selected memory
"M– mode"	M – X to selected memory
"MX mode"	M • X to selected memory
"M÷ mode"	M ÷ X to selected memory
"MEXC mode"	X is exchanged with selected memory

Change Sign Key, "CS/DS"

a) After "EE": change sign of exponent of X
b) After "F": (DS) set calc to Decimal Select mode
c) After any other key: changes sign of X mantissa

Positive/Negative Summing Key, "Σ+/Σ–"

a) Used to enter data points for computation of mean and standard deviation:
   Sums X to M1 (ΣX)
   Sums X^2 to M2 (ΣX^2)
   Adds 1 to M3 (N)
b) After "F": (Σ–) used to delete data points:
   Subtracts X from M1
   Subtracts X^2 from M2
   Subtracts I from M3

Accumulative/Factorial Key, "M+/X!"

a) Sums X to M1
b) After "F": (X!) replaces X with X-factorial

Coordinate Conversion Key, "R ↔ P"

a) Converts contents of X and Y in rectangular coordinates to polar coordinates:

$\sqrt{X^2 + Y^2}$ to Y

TAN^{-1} Y/X to X

b) After "F": (P → R) converts contents of X and Y in polar coordinates to rectangular coordinates:
   Y SIN X → Y
   Y COS X → X

Note: R ↔ P works in all four quadrants

Square Root/Square Key, "$\sqrt{X}/X^2$"

a) Square root of positive value of X to X
b) After "F": (X^2) X-squared to X

functional description (con't)

Reciprocal/Power Key, "1/X/Y^X"

a) Reciprocal of non-zero value of X to X
b) After "F": (Y^X) computes power, pushes down stack, clears T

Enter Key, "ENT/CF"

a) Pushes up stack, retains X
b) After F: (CF) resets F mode

Second Function Key, "F"

Sets F mode

Memory Store/Mean Key, "MS/$\overline{X}$"

a) Sets memory store mode
b) After "F": ($\overline{X}$) divides M1 by M3 and puts result in X, this gives mean of data summed using Σ+ key

Memory Recall/Standard Deviation Key, "MR/SD"

a) Sets Memory Recall mode
b) After F: (S.D.) computes standard deviation of data entered with the Σ+ key using the relationship:

$$SD = \sqrt{\frac{\Sigma X^2 - \frac{(\Sigma X)^2}{N}}{N-1}} \equiv \sqrt{\frac{M2 - \frac{(M1)^2}{M3}}{M3-1}} \to X$$

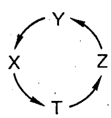
ΣX, ΣX^2 and N may be recovered from M1, M2 and M3

Enter Exponent Key, "EE/ENG"

a) Sets enter exponent mode, displaying 00 in exponent position
b) After F: (ENG) sets the calculator to the engineering mode, which displays all numbers with an exponent in multiples of 3.

Stack Rotate/Pi Key, "ROLL/π"

a) Rolls stack down



b) After F: (π) pushes up stack and enters π, 3.14159265359 to X

Exchange Key "X ↔ Y/X↔ M"

a) Exchanges X and Y
b) After MS, MR or F: (X ↔ M) sets calculator to MEXC mode

Percent/Delta Percent Key, "%/Δ%"

a) Calculates percent by:

$$\frac{X \cdot Y}{100} \to X$$

b) After F:(Δ%) percent change between X and Y to X, and difference to Y:

$$\frac{Y-X}{X} \cdot 100 \to X, \text{ and } Y - X \to Y$$

Common Log Key, "LOG/10^X"

a) Common logarithm of X to X (base 10)
b) After "F": (10^X) 10^X to X

Natural Log Key, "Ln/e^X"

a) Natural logarithm of X to X (base e)
b) After "F": (e^X) e^X to X

Decimal to Degrees Conversion Key, "D.MS"

a) Replaces the decimal angle in X with its degrees (or hours), minutes and seconds conversion and sets the decimal select to four.
b) After "F": (DMS) degrees (or hours), minutes and seconds in X is converted to decimal angle

Trigonometric Keys, "SIN, COS, TAN"

a) Replaces the decimal angle in X with the indicated trigonometric function
b) After F: replaces X with the decimal angle of the indicated inverse trigonometric function

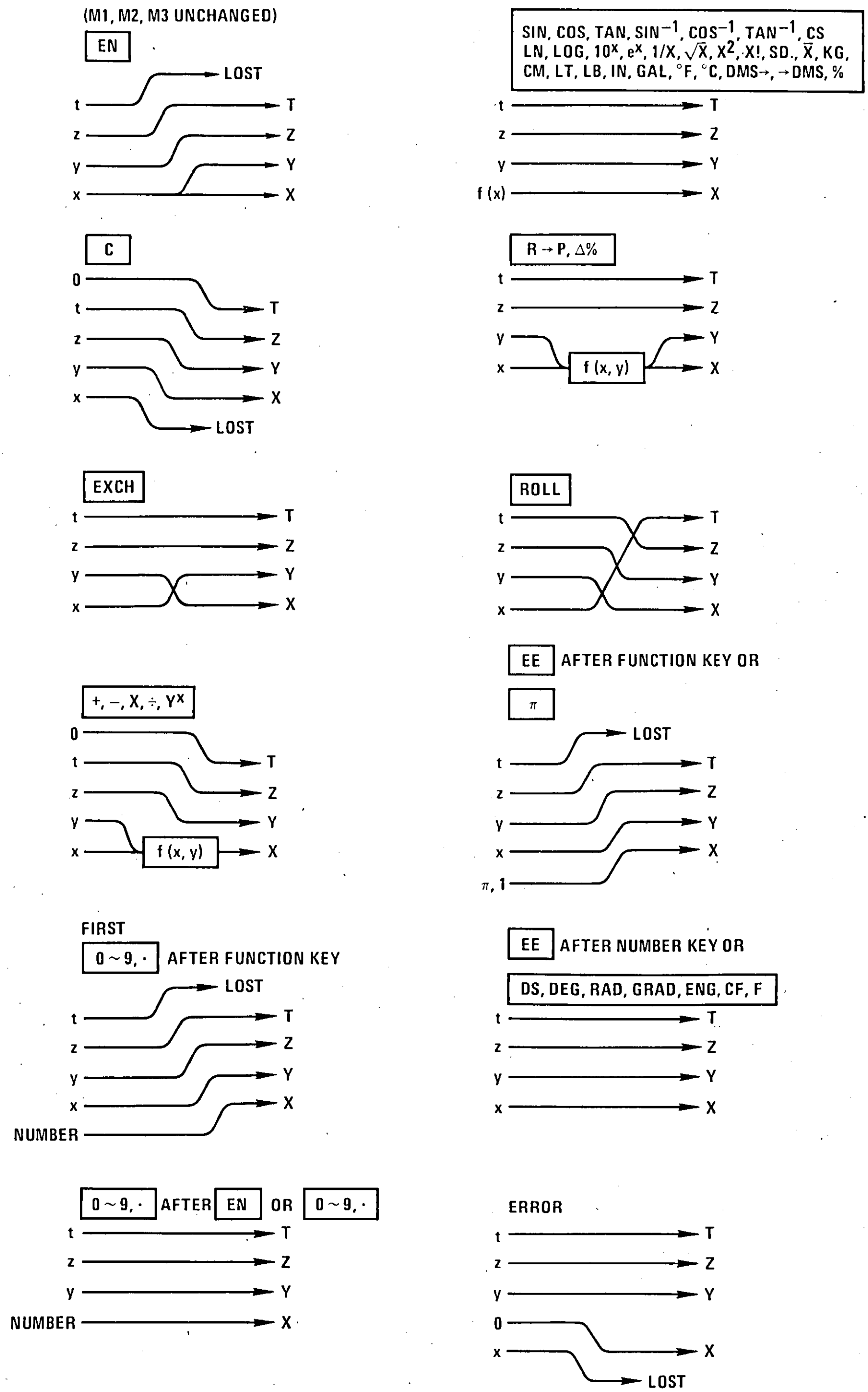
The Four Function Keys, "+, –, x, ÷"

a)
$$\left.\begin{array}{l} \text{Add key: } Y + X \to X \\ \text{Subtract key: } Y - X \to X \\ \text{Multiply key: } Y \cdot X \to X \\ \text{Divide key: } Y \div X \to X \end{array}\right\} \begin{array}{l} \text{Then push down} \\ \text{stack and clear T:} \\ 0 \to T \to Z \to Y \end{array}$$

b) After MS, MR or F:
"+" Sets M+ mode
"–" Sets M– mode
"X" Sets Mx mode
"÷" Sets M÷ mode

summary

Summary of Stack Operations

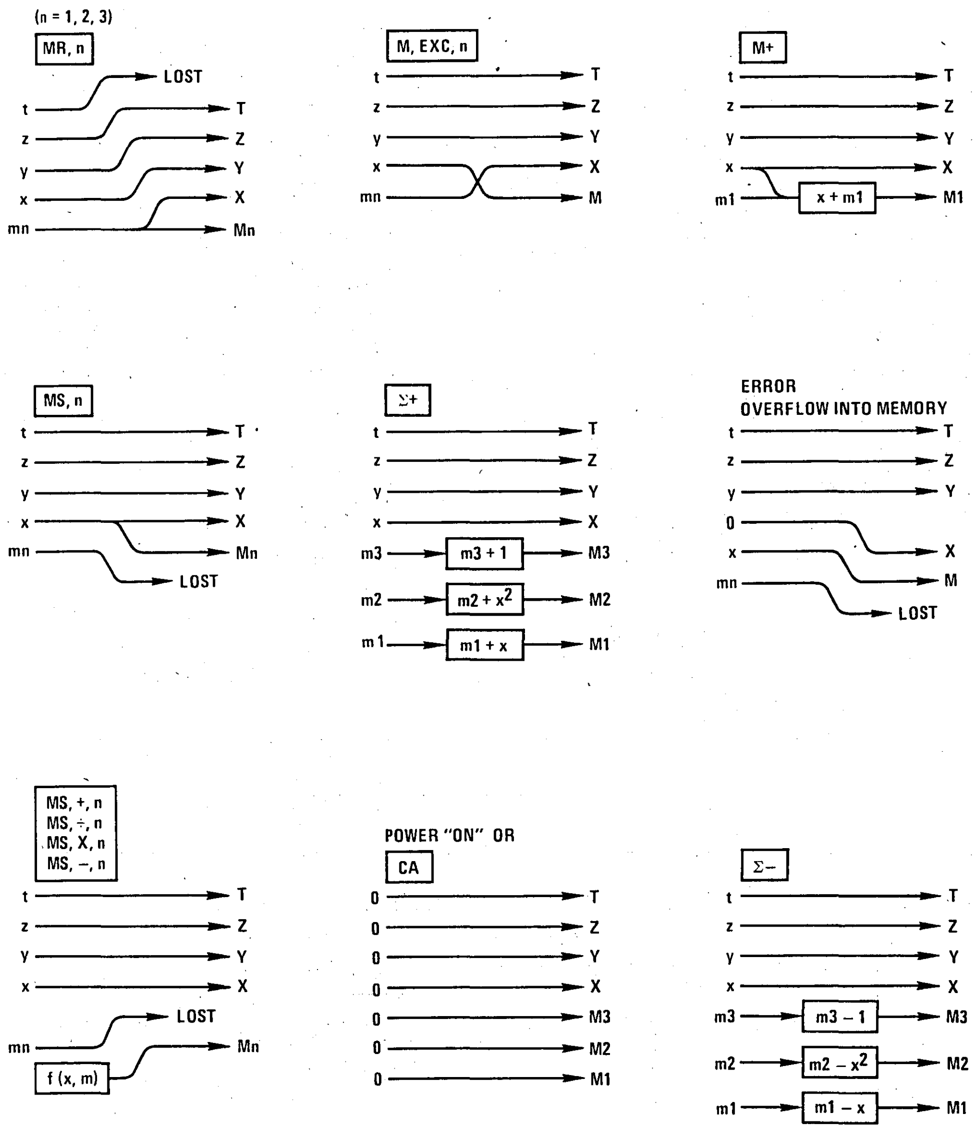


MM57136

8

summary (con't)

Summary of Operations Using Memory(s)



CALCULATOR CHIP MAKES A COUNTER

INTRODUCTION

In applications that require counting at fairly low rates and display of the accumulated total, the MM5736 calculator chip can be used to yield a very low parts count solution. Such applications include: timers, stopwatches, bin counters, digital panel meters, coordinate counters and nearly all applications that currently use mechanical counters. A 6 digit counter that will drive a LED display and count at a maximum rate of about 60 Hz can be constructed with only 2 integrated circuits. Higher counting rates, simplified control, and more versatile display driving capability can be obtained with the addition of a few more components. Counting is accomplished by loading a "1" into the calculator and causing an "add" each time the counter is incremented. But before describing any actual counters, a brief explanation of the calculator's operation is in order.

GENERAL DESCRIPTION

The MM5736 is a 6 digit, no decimal point, five function calculator. These five functions are: ADD, SUBTRACT, MULTIPLY, DIVIDE, and CLEAR. The calculator has 3 inputs (K_1, K_2, K_3) that are designed to be driven by a keyboard matrix and two sets of outputs: 6 "digit" outputs and 7 "segment" outputs. The segment outputs provide a positive true, 7 segment code that represents the information in the calculator's display register. These outputs are multiplexed such that the 7 segment code for digit 1 appears on the segment outputs during digit time 1. The code for digit 2 appears during digit time 2 and so on as illustrated in *Figure 1.* These outputs are designed to drive a LED readout in a "digit" multiplexed manner by strobing the LED characters with the digit outputs. The digit outputs can not drive the LED display directly and must be buffered

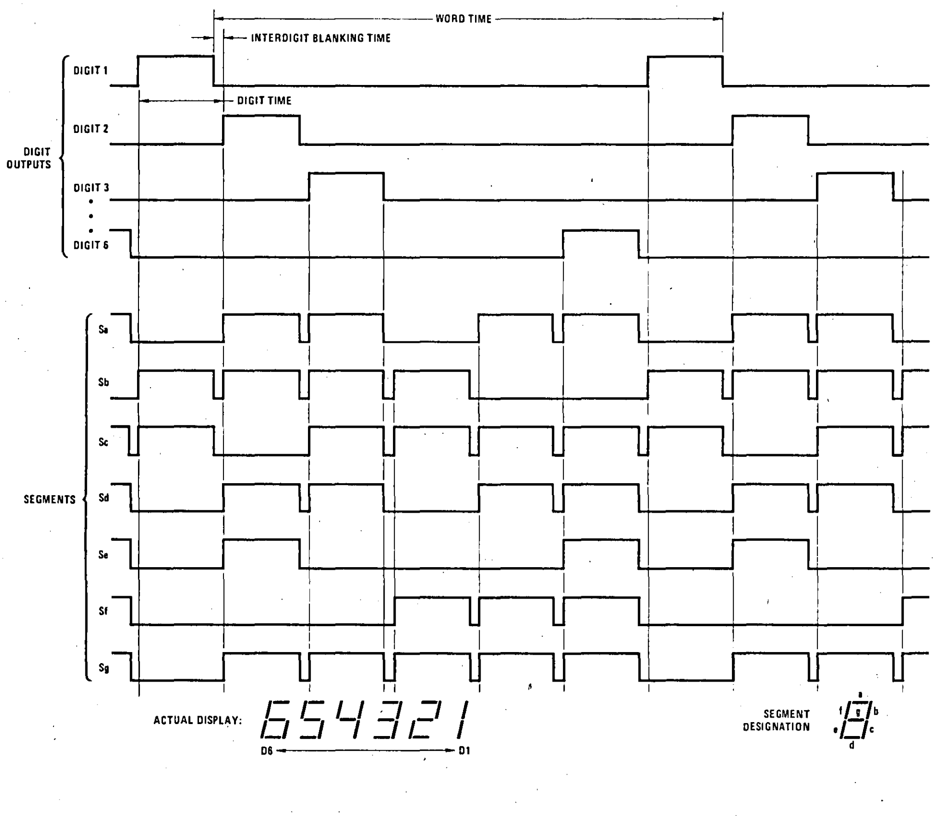


FIGURE 1. Display Timing Diagram

with a DM75492 digit driver. The segment outputs will drive some LED displays directly but the designer must choose the display carefully if he does not wish to use segment drivers. National's line of low current LED displays, such as the NSN66A and NSN98A, can be driven directly by the calculator chip.

ENTRY INTO THE CALCULATOR

Numbers are entered into the calculator by connecting the appropriate digit output to either the K_1 or K_2 input. Arithmetic operations (and the clear operation) are initiated by connecting the appropriate digit output to the K_3 input. Table I shows the combinations of digit outputs and K inputs.

TABLE I.

Digit #	K_1	K_2	K_3
1	0		CLR
2	1	6	
3	2	7	–
4	3	8	+
5	4	9	X
6	5		÷

Note: Blanks are illegal connections.

Switch debounce is done in the calculator chip and is accomplished by requiring that the digit output of interest be connected to the proper input for at least 8 consecutive word times (see *Figure 1*). Before another entry can be made, at least 8 word times must elapse during which none of the digits outputs are applied to the K inputs. This requirement limits the speed of the calculator but is necessary to provide an adequate debounce timeout. A method of speeding up this timeout is discussed later.

POWER REQUIREMENTS

The MM5736 will operate from a single supply voltage anywhere between 6.5V and 9.5V. The calculator chip itself will draw about 6 mA. If a LED display is driven directly, without segment drivers, the current that drives the display must come through the calculator so the total power supply current could be as high as 110 mA but will typically be about 50 mA. This is dependent to some extent on the supply voltage and the nature of the particular digit drivers that are used.

NO POWER SUPPLY RAMP ALLOWED

The power supply voltage must come up to an operational level fairly quickly since a slow ramp will not always initialize the calculator properly. The chip was designed for battery operation where the dc source is switched. If the chip is used in a system with a heavily filtered power supply, some provision should be made to allow the V_{SS} terminal of the calculator to rise abruptly. After power up, the calculator should be cleared twice to ensure that all registers are reset to zero. The first CLEAR operation affects only the display register, the second CLEAR affects all other registers.

CMOS COMPATIBILITY

The MM5736 is directly compatible with Nationals' 74C line of CMOS. The number of CMOS loads the calculator can drive is limited only by degradation in waveshape due to capacitive loading. Loads of 200 pF or less should present no problem to the digit outputs but the segment outputs should not be loaded with more than about 50 pF. This means fanout should be limited to about 10 on the digit outputs and 4 on the segment outputs. The CMOS can be run from the same supply as the calculator and still drive the calculator inputs directly. This compatibility makes interfacing with the calculator a breeze.

SIMPLEST COUNTER

Figure 2 shows a 6 decade counter that drives a display and requires a minimum of parts. This circuit's maximum counting rate will typically be about 60 Hz. Some chips may run as slow as about 40 Hz while some may run as fast as 150 Hz due to inherent variations of the on-chip oscillator from calculator to calculator. This counter is useful in applications where speed is not

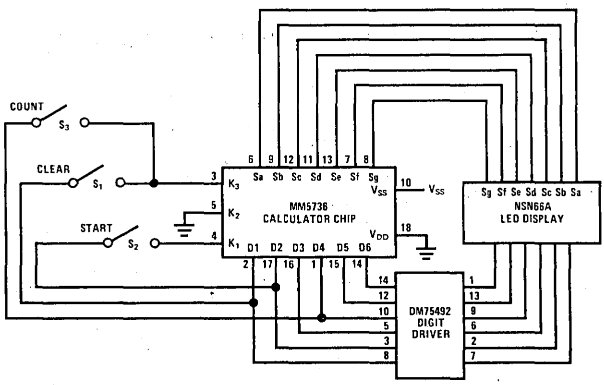


FIGURE 2. Simplest Counter

an important factor and where the counter is reset manually. The resetting of this circuit consists of two operations, clearing the calculator and entering a 1 into it again (only one CLEAR operation is needed following an arithmetic operation). The circuit in *Figure 2* leaves these two operations to the operator; he must first clear the counter by depressing S_1 to the CLEAR position and then he must enter a 1 into the machine by depressing S_2 to the START position. This allows the operator to control when the counting starts without gating the "count" input.

In case the impact of this escaped you, let's repeat it: the circuit in *Figure 2* demonstrates a 6 decade counter and everything that is needed to drive a 6 digit LED display, yet this circuit requires only two integrated circuits!

Figure 3 indicates how to build this same counter using segment drivers. The DM8895 segment driver can be mask programmed to source several values of current. Since the values of current that are readily available will change from time to time, National should be consulted about the DM8895 before a design using it is undertaken. The general range of currents available is from 5.0 mA up to about 17 mA per segment. This means that fairly large displays can be used. Noteworthy is the fact that the current that drives the display in this configuration is not supplied by the calculator chip. Instead, this current comes from the V_{CC} supply terminal of the DM8895. The DM8895 will continue to operate as long as the voltage between the V_{CC} terminal and each output is at least 1.6V. This means V_{CC} can be operated at a lower level than V_{SS}, resulting in a power saving. The voltage on an output of the DM8895 when the segment is ON is determined by the saturation voltage of the digit driver (typically 1.0V for the DM75492) and the voltage across the LED (typically about 1.8V). Consequentially the typical minimum value of V_{CC} is about 4.4V. Worst case conditions will result in a minimum V_{CC} of about 5.3V.

Figure 4 again indicates how to build this same counter but this time using different segment drivers. In this circuit, the current drive to the LED's is determined by the external current limiting resistors. Here again the current to the display is supplied by V_{CC} which can be less than V_{SS}, again resulting in a power saving and the ability to drive large LED displays.

SELF STARTING COUNTER

With the addition of only one package of CMOS gates, a counter can be built that does not require a separate "start" operation to enter an initial 1 into the calculator chip. This circuit is shown in *Figure 5*. When the RESET switch is returned to its normal position after clearing the calculator, the additional parts generate a delayed pulse that gates digit output 2 into the calculator and thus enters a 1. This allows the counter to be reset in a single operation.

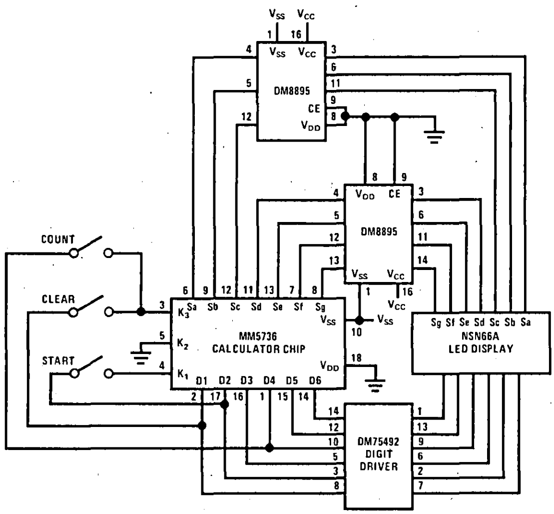


FIGURE 3. Counter with Segment Drivers

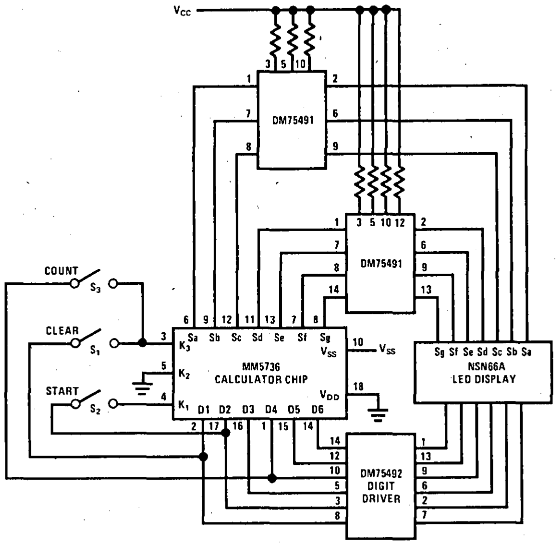


FIGURE 4. Counter with Segment Drivers and External Current Limiting Resistors

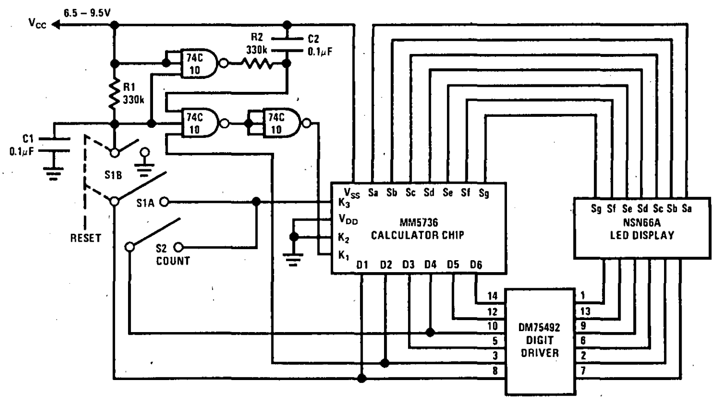


FIGURE 5. Counter with a Single Clear Switch

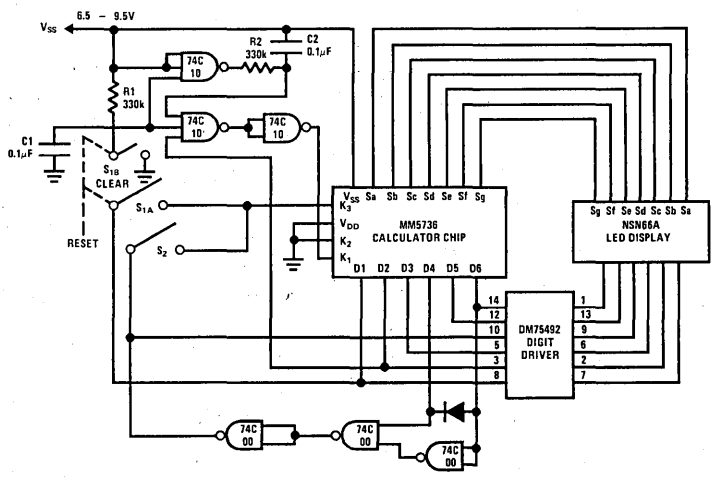


FIGURE 6. Counter with Increased Speed

FASTER COUNTING RATES

Figure 6 illustrates how to speed up the circuit shown in *Figure 5* so that it will count at a higher rate. The actual maximum counting rate attainable with this circuit will depend on the particular MM5736 used but will run from about 80 Hz up to about 300 Hz. A reasonably typical speed is about 120 Hz. This circuit could also be used with segment drivers as previously described. The increase in counting rate is obtained by feeding digit output 6 back to the digit 4 output thereby fooling some internal logic. However this results in a double pulse on the digit 4 output which must be gated back to a single pulse at the normal digit 4 time. This requires one diode and one additional package of CMOS gates. In reality, very few relays or switches will operate at these speeds. Consequently, applications requiring these higher counting rates may have a normal logic signal to count rather than relay closures. *Figure 8* illustrates this. In this configuration the input must be high at least 4 word times and the duty cycle cannot exceed 50%. A word time will vary from 420μs to 1.6 ms with 1.0 ms being typical.

MORE VERSATILITY

These counters can be made to count by numbers other than 1 by causing the desired number to be entered into the calculator during the START operation. Table I indicates which connections must be made. The counters can also be made to count down by doing successive subtractions rather than successive additions. Both could be used to build an up/down counter, the only restriction being that trying to count up and down at the same time is no fair. *Figure 7* shows a circuit that counts up and down by 4's. Such a counter might be used to keep track of inventory in a bin. In this case, the parts to be inventoried are packaged in groups of 4. When a package is put into the bin, switch S_2 is activated and the counter adds 4 to the accumulated total. When a package is taken out of the bin, switch S_3 is activated and the counter subtracts 4 from the accumulated total.

RETAINING FULL USE OF THE CALCULATOR

Counters can be built such that full use of the calculator is retained. This requires that the usual keyboard arrangement of the calculator be undisturbed by the counting logic. *Figure 8* illustrates a circuit that uses MOS transistors to accomplish this. In this circuit, normal calculator operation is retained when S_2 is in the "calculate" position since all four MOS transistors (Q1–Q4) are "off" (gates are at V_{CC}) and the circuit is essentially the same as the "recommended calculator" circuit in the MM5736 data sheet. If the "RESET" switch is activated D1 is connected to K_3 and the calculator is cleared. Capacitors C1 and C2 are discharged while S_1 is activated but as soon as S_1 is released C1 and C2 will charge up generating a delayed pulse (negative going) on the gate of Q2 which gates D2 into K_1 and causes a 1 to be entered into the calculator. The delay caused by C1 is necessary to allow the CLEAR function to be debounced by the calculator chip as mentioned earlier. When S_2 is in the "COUNT" mode Q4 is turned on and D6 is tied to D4. This doubles the maximum counting rate by reducing the internal debounce timeout. The count input is now enabled and an input pulse will turn Q1 on. This gates D4 into the K_3 input and causes the calculator to perform an addition. Each subsequent input pulse causes 1 to be added to the sum. When S_2 is returned to the "calculate" position the count input is disabled and Q4 is turned off returning the keyboard logic to its normal state. This same circuit can be implemented with MM74C02 NOR gates instead of MM74C00 NAND gates. The MOS transistors can then be replaced with an MM5616 CMOS switch.

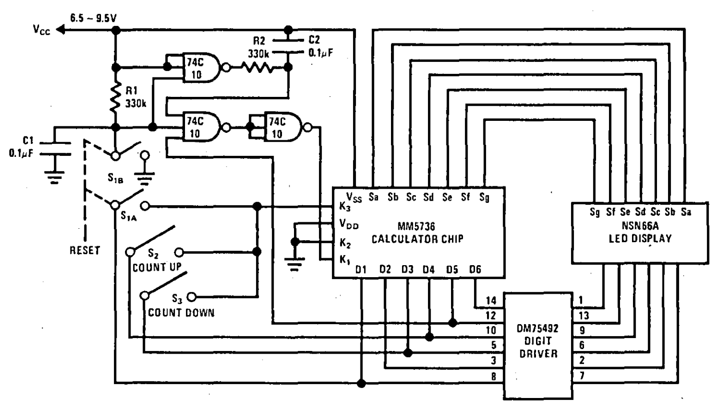


FIGURE 7. Up-Down Counter

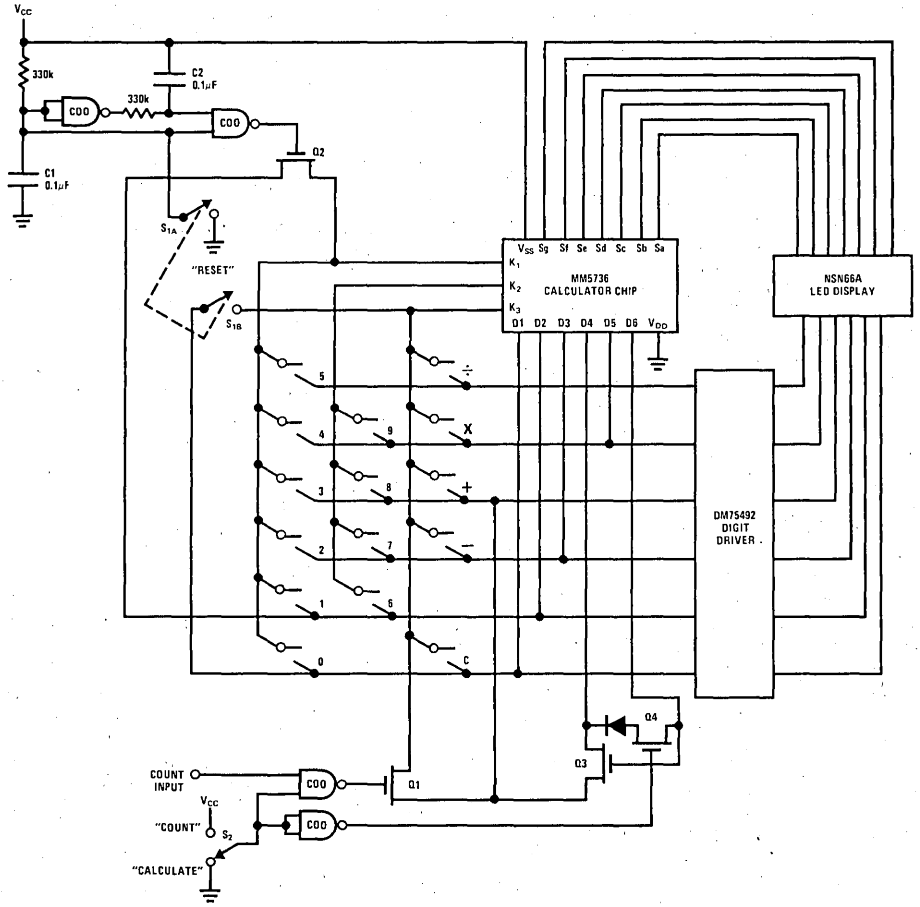


FIGURE 8. Calculator/Counter

SUMMARY

Many versatile counters can be built using the MM5736 or its 9-digit equivalent, the MM5739, calculator chips. These counters should yield very cost effective solutions to a variety of counting applications. The major disadvantage of these counters is that they are relatively slow. The major advantages these counters offer are:

1. The ability to directly drive a LED display.
2. The ability to debounce switch or relay inputs.
3. 6 decades of counting in one DIP.
4. Low cost.
5. Low parts count.

CALCULATOR LEARNS TO KEEP TIME

INTRODUCTION

A number of interesting stopwatch and elapsed time functions can be implemented using the MM5736 calculator chip and a few packages of CMOS gates. This note describes six different circuits that are intended to stimulate thinking along these lines. The circuits to be described are listed below.

1. Stopwatch with 1/10 second resolution
2. Stopwatch with 1/100 second resolution
3. Stopwatch/calculator (1/10 second resolution)
4. Stopwatch/calculator (1/100 second resolution)
5. Stopwatch with 1/10 secs, secs, mins display
6. Interval timer with keyboard and alarm

With the exception of circuits 5 and 6 all of these circuits work in decimal fractions of seconds. They do not display in seconds and minutes. Circuit 6 displays minutes and tenths of minutes but not seconds. Circuit 5 displays tenths of seconds, seconds and minutes. It is anticipated that a number of applications can be satisfied by counting in only one unit, either seconds or minutes.

In all these circuits, the MM5736 calculator chip is used in the autosumming mode as a counting and display element. Application note AN-112 illustrates how to accomplish this counting. A thorough understanding of the calculator's operation as a counter can be gained from AN-112 and the MM5736 data sheet. Consequently, the emphasis in this note is on controlling the counter in such a way that useful timing functions are performed.

Two types of timebases are also described. The first, a CMOS RC oscillator, is depicted in all the circuits described but may not be stable enough for some applications. Consequently, a simple crystal controlled timebase is also described.

STOPWATCH WITH 0.1 SECOND RESOLUTION

The circuit in *Figure 1* provides the classic stopwatch functions of:

A) START
B) STOP
C) RESET

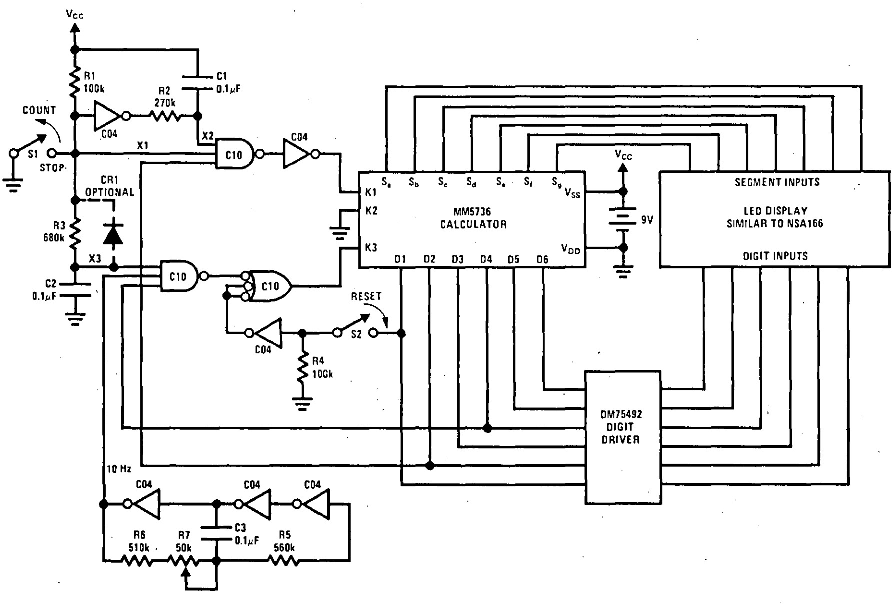


FIGURE 1. 1/10 Second Stopwatch

This implies that timing may continue after it has been stopped without resetting to zero. The display will be in tenths of seconds and seconds. Thus, 3 minutes 11 1/2 seconds would be displayed as 191.5 seconds.

Circuit Description

The RESET switch simply gates D1 into the K3 input of the calculator and clears it. Upon initial power up it will be necessary to activate RESET twice. From then on, only one RESET activation is necessary.

When the COUNT switch is activated, R1 pulls up signal X1. This makes all the inputs to the 3 input gate high and gates D2 into input K1. This will cause a 1 to be entered into the calculator. Signal X2 is delayed by R2 and C1 and will go low about 25 ms after X1 and shut off the D2 pulses being gated into input K1. About 40 ms after this, signal X3 (which is delayed through R3) goes high and D4 is gated into the K3 input at a 10 Hz rate. This causes repeated additions and results in the calculator counting at this rate. When the COUNT switch (S1) is returned to the STOP position the additions will be stopped about 60 ms later (after X3 is delayed through R3). This delay hardly seems objectionable since it is less than the resolution of the counter. However, purists may feel the addition of CR1 is necessary. This will cause the counting to stop immediately after S1 is returned to the STOP position since C2 will be discharged immediately.

The LED display shown differs from the NSA166 only in the placement of the decimal point.

STOPWATCH WITH 0.01 SECOND RESOLUTION

Figure 2 depicts a circuit that is identical to the one shown in *Figure 1* except that it has a resolution of 0.01 sec. This means the counter must run at a 100 Hz rate which is normally beyond the capability of the MM5736. However, as described in AN-112, a trick can be played with D6 and D4 that will double the effective counting rate of the calculator. This trick is accomplished by forcing D4 high during D6 time. SWD is a bilateral switch that connects D6 to D4. CR2 keeps D4 off D6. SWC is turned off during D6 time so the extra pulse on the D4 line will not get to either the LED display or the data entry logic.

The remainder of the circuit operates exactly like the one in *Figure 1* with the exception that some of the gating is implemented with the MM5616 switches.

STOPWATCH/CALCULATOR WITH 0.1 SECOND RESOLUTION

Figure 3 depicts a combination stopwatch and calculator. Stopwatch operation is the same as described earlier with the following exceptions: Transistors Q1 and Q2 (which are small GP switches) are used to switch either D2 or D4 to the calculator inputs. This allows the keyboard and the stopwatch logic to operate in parallel in what amounts to a "wire OR'ed" arrangement. Also there is no RESET switch in this circuit since the calculator's CLEAR key can be used to reset the time to zero.

Normal "four function" calculator operation is available when S1 is in the "CALCULATE" position.

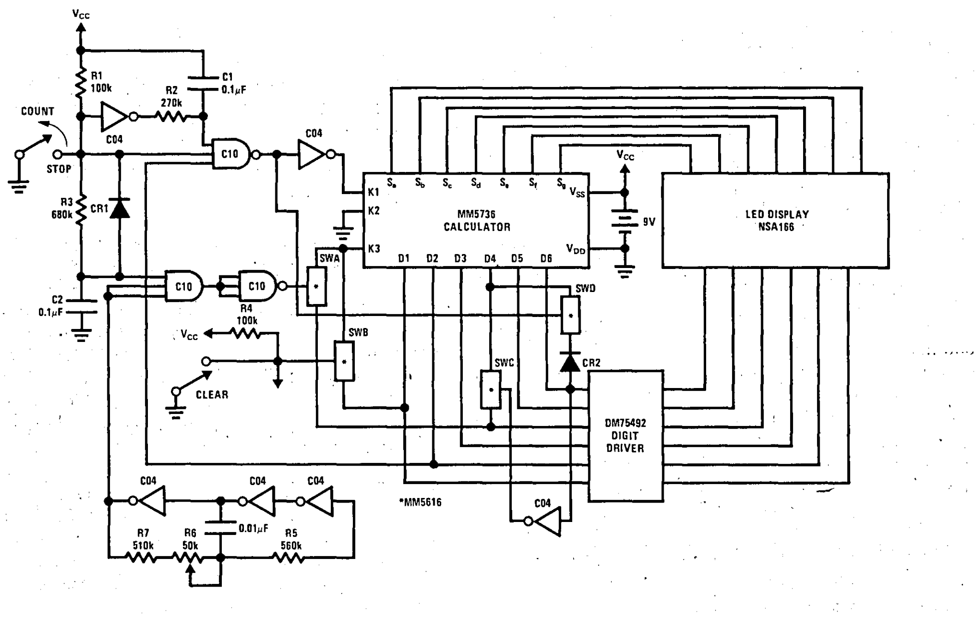


FIGURE 2. 1/100 Second Stopwatch

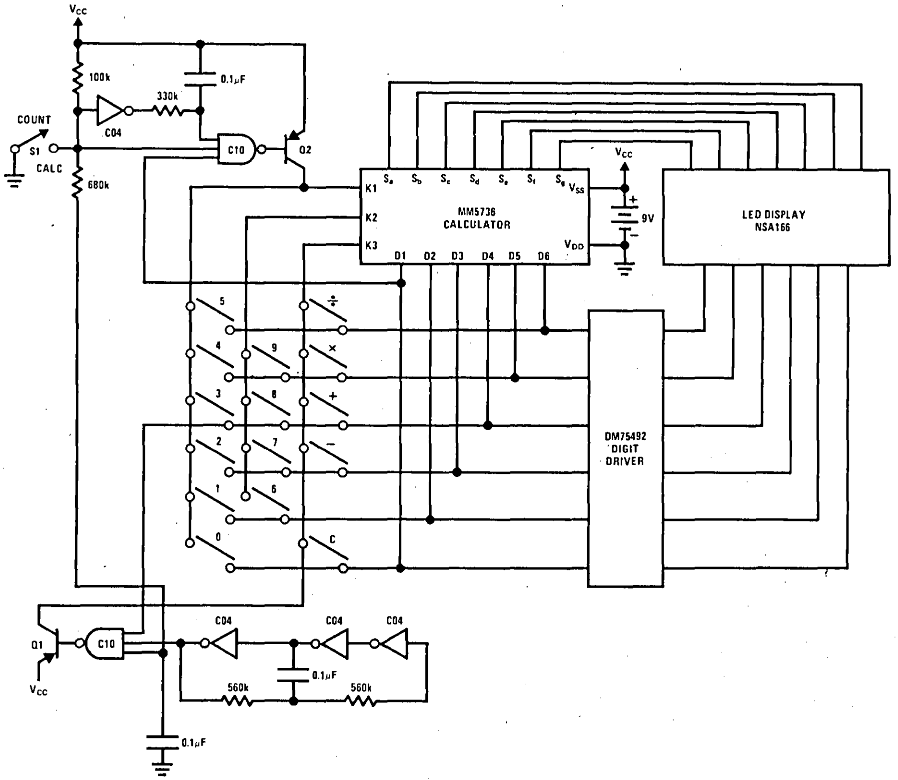


FIGURE 3. 1/10 Second Stopwatch/Calculator

STOPWATCH/CALCULATOR WITH 0.01 SECOND RESOLUTION

Figure 4 is just a souped up version of *Figure 3.* It will count at a 100 Hz rate giving a 0.01 second resolution to the stopwatch. Switch S2 now needs to be DPDT type. One pole of the switch provides the start-stop function and one pole is used to switch in the "speed-up" circuit involving D4 and D6. The additional gating keeps the extra pulse from reaching the display and keyboard.

STOPWATCH/CALCULATOR DISPLAYS MINUTES AND SECONDS

The conventional time keeping format of minutes and seconds can be obtained with the additional logic shown in *Figure 5.* This circuit provides a display of time up to 999 minutes, 59.9 seconds. But this requires a base sixty counting capability that is not inherent in the calculator chip. This conversion is accomplished by recognizing when the count has gone to 60.0 seconds and then quickly adding 40.0 to the count, thus giving an apparent base 60 carry. The sequence of operations required to do this is:

1. Recognize 6 in 3rd digit
2. Enter 3 into calculator
3. Enter 9 into calculator
4. Enter 9 into calculator
5. Enter + into calculator
6. Enter 1 into calculator
7. Enter + into calculator
8. Resume normal operation

This sequence leaves the calculator properly initialized with a "1" in it ready for more counting. This would not be the case if 400 was entered directly rather than as 399 + 1.

Circuit Description

The base 60 conversion is accomplished with a little controller that switches the Digit outputs to the proper calculator inputs through some FET switches. The sequencing it provided by an 8-bit counter and a decoder. If desired, the circuit could be re-implemented to use MM5616 quad switches rather than the MM552's shown. But, since the simplest device that will do this job is a MOS transistor, it was chosen in this particular case. It also lends itself to the negative going outputs of the MM74C42 decoder.

When the stopwatch is counting normally (rather than doing a base 60 conversion) the MSB (Q_D) of the sequence counter will be low which inhibits counting. It also turns on transistor Q1 which will allow the counter to be preset by the output of the gate that decodes a "6" according to the expression $S_e \cdot S_b$, which is a simplified version of the seven segment code for "6."

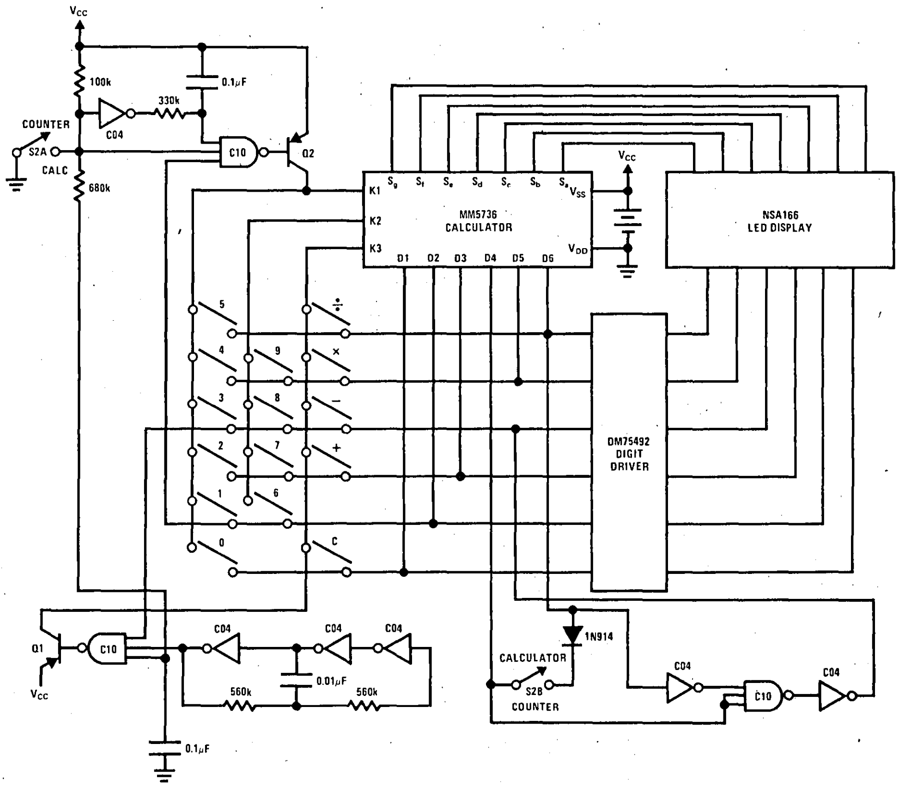


FIGURE 4. 1/100 Second Stopwatch/Calculator

Since the counter is clocked by D3, only a 6 in the 3rd digit will cause the counter to be present. This corresponds to a time of 60.0 seconds and signals the beginning of a base 60 conversion. The counter is preset to the state 1001 0000. Since the MSB is a 1, the counter's count enable term is enabled and its load term is disabled. It will now count word times on every D3.

Reference to AN-112 will reveal that with the calculator "speeded up" it is necessary to allow a digit output to be connected to the inputs for a minimum of 4 word times and then there must be at least 4 word times during which nothing is applied to the calculator inputs before the next entry is allowed. This timing is accomplished by Q_D of the low order counter. It toggles with a half period of 8 word times. This Q_D is connected to the D input of the decoder which is used as an enable input. When this signal is high, all outputs of the decoder are high and all the MOS transistors are off. When this signal is low the proper decoder output is low. So the first 4 bits of the counter provide timing and the next 3 bits provide the necessary sequence of entries. The last bit turns the sequence on or off. The sequence of entries is as described earlier and is implemented by transistors Q2–Q7.

Initialization

When S1 is first switched to the stopwatch mode, a burst of D2 pulses is gated into the K1 input by the one shot comprised of R2, C1 and the gate that drives Q8. This enters a "1" to get the calculator ready to count. A little later, Q9 will be turned on by the timebase oscillator at a 10 Hz rate and counting will begin.

Segment Drivers

Two DM8895 segment drivers are used in *Figure 5*. This is not absolutely necessary. The calculator can drive some displays directly. However, it is necessary to buffer both segment e and segment b to preserve proper logic levels for the CMOS decoding gates. This could be done by non-inverting CMOS buffers like the MM80C96 or 2 inverters in series. But if only S_e and S_b are buffered, there is no guarantee of segment intensity uniformity. Therefore, it is more desireable to buffer all segments. The DM8895 is a segment driver with internal current limiting resistors that are mask programmable. The DM75491 could also be used if external resistors are not objectionable.

"Speed Up" Circuit

Transistors Q11 and Q10 implement the "speed up" function in the same way as that described in *Figure 2* except that naked MOS transistors are used in place of the MM5616 CMOS switch.

AN INTERVAL TIMER WITH A KEYBOARD

An interval timer that can be programmed to time out long intervals can also be made using the calculator chip. The desired time interval is entered from a keyboard. When the interval is complete, a tone is emitted by a small speaker until the operator activates a RESET switch. The timer (as described) will handle intervals as long as 99999.9 minutes, which is about 69 1/2 days. This is probably too long an interval for an RC oscillator to be acceptable as a timebase. *Figure 6* shows an RC oscillator but it could be replaced by the crystal oscillator described later in this note. Counting speeds other than 0.1 minutes could be used as long as the counting speed of the calculator is not exceeded.

Circuit Description

As was the case for the stopwatch described in *Figure 5,* a small controller made from a counter and a decoder is used to switch Digit outputs to the proper K input to create the sequence of entries required. The counter is clocked by a 30 Hz oscillator whose output is also gated with all the Digit lines to create the proper "key down" and "key up" times.

There are two sequences of entries required: one for RESET and one for START, the beginning of the timing interval.

Reset Sequence

When the RESET switch is activated, it is debounced by a latch and differentiated by C1 to generate a positive going pulse that clears the MM74C193 controller counter and the sequence proceeds as follows:

1. **Reset Latches:** The "0" output of the decoder resets the zero decode latch and the buzzer latch.

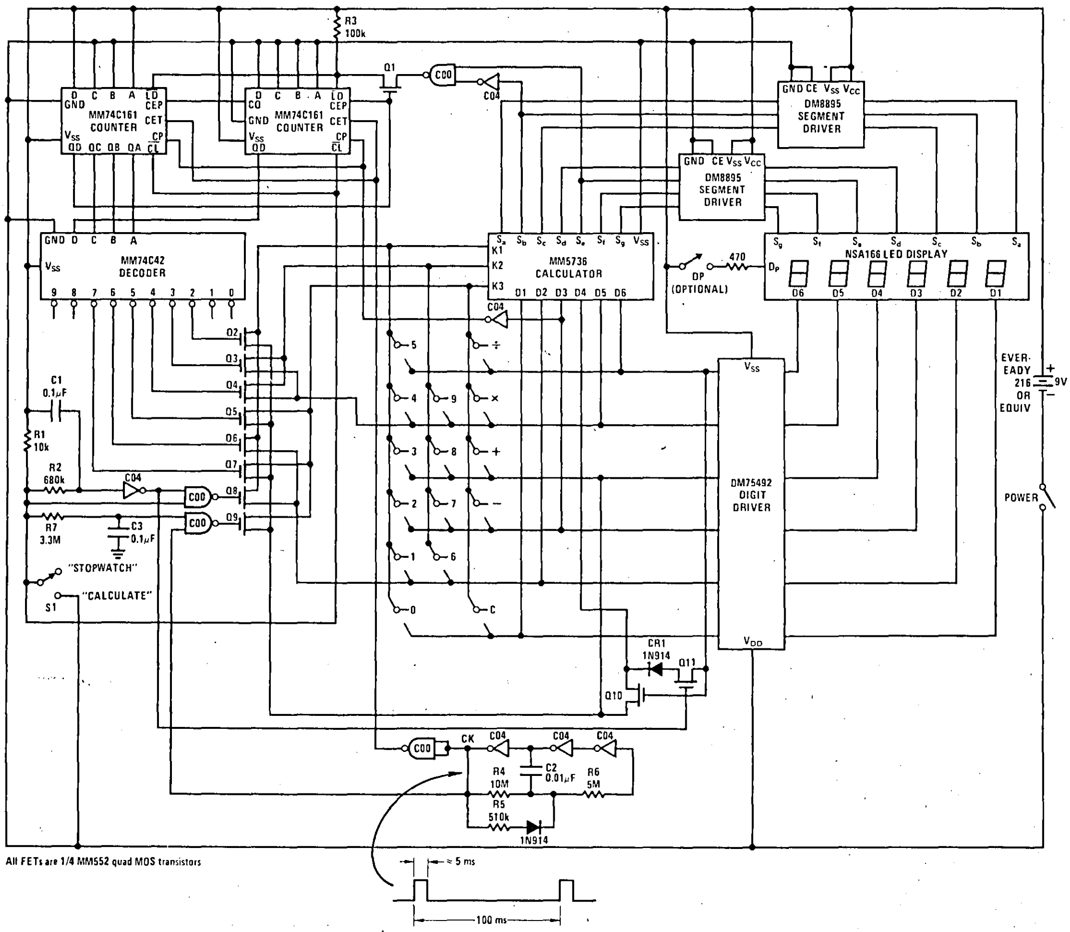


FIGURE 5. 1/10 Second, Seconds, Minutes Stopwatch/Calculator

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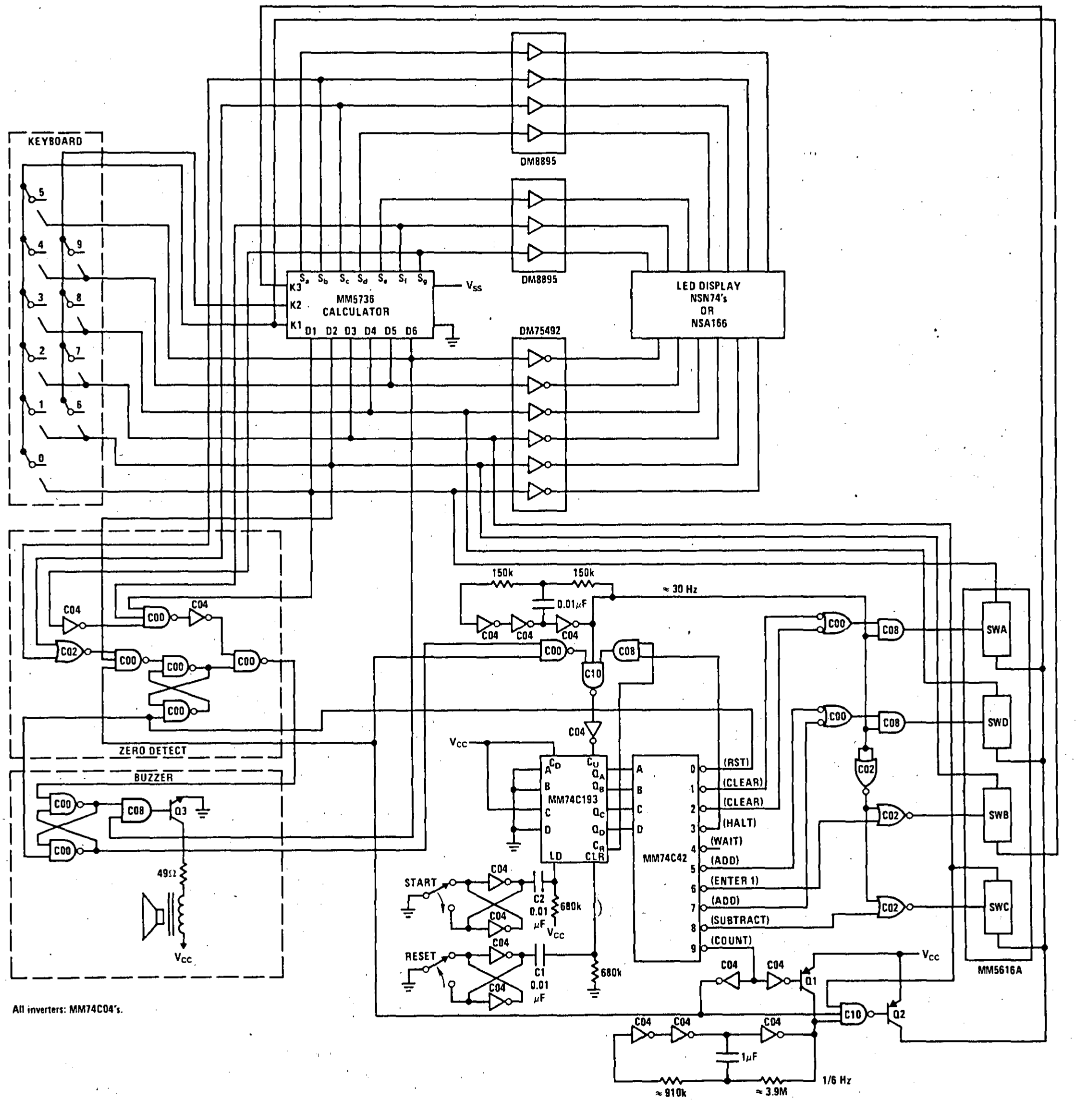


FIGURE 6. Interval Timer

2. **Clear Calculator**
3. **Clear Calculator:** Both outputs 1 and 2 of the decoder are "or'ed" and then gated to switch D1 into the K3 input of the Calculator to cause a clear. Two clears are necessary to insure that all registers are reset to zero.
4. **Halt:** Decoder output 3 forces count enable low and hangs up the counter.

Start Sequence

When the START switch is activated, C2 differentiates the latch output and generates a negative going pulse that loads the counter to state 4. Since this can happen at any time with respect to the 30 Hz clock, it is necessary to wait until the counter goes to the next count before trying to enter anything into the calculator. This is done to insure that a full cycle of the 30 Hz clock elapses during the time an entry is being made. The sequence then proceeds:

1. **Synchronize:** Decoder output 4 does nothing but insure that the first application of signals to the calculator will last for a complete interval.
2. **Add:** Decoder output 5 causes D4 to be gated into input K3 causing an add. This will enter (in normal Polish notation) the number already entered from the keyboard.

3. **Enter 1:** Decoder output 6 gates D2 into K1 to enter a 1. This is the number that will be repeatedly subtracted to make the total count down.
4. **Add:** This simply causes the 1 just entered to be added to the number that was entered from the keyboard. The total will now be one count higher than desired. Since this would shake up most users, the next step corrects this.
5. **Subtract:** Decoder output 8 causes a subtraction which decrements the display by 1 and brings it back to the correct reading.
6. **Count:** Decoder output 9 makes the controller halt and also turns transistor Q1 off. Q1 was initializing the timebase oscillator so the timer won't begin to count down prematurely. D3 is also gated into the base of Q2 which causes repeated subtractions at the timebase rate.

At this point the timer simply chugs away decrementing until it reaches zero. Time remaining to zero is continuously displayed. When zero has been detected, the controller's count enable term will go high and it will advance to state 15 at which time the "carry out" term will go high and inhibit any further counting. It will stay this way until the RESET button is activated.

Zero Decode Logic

A zero is detected by recognizing that a blank exists in digit 2 and a 0 exists in digit 1. A blank is decoded with the expression $S_b + S_c$ since one of these two segments is always on when any number is being displayed. When BLANK · D2 exists, a latch is set. Then when a zero is detected in digit 1 according to the expression $S_f \cdot \overline{S_g}$ the buzz latch is set. This gates D6 into the base of Q3 which turns the speaker on at about a 1 kHz rate with a 1/6 duty cycle and generates a buzz. The buzz latch will be reset during the RESET sequence.

OSCILLATORS

Two CMOS oscillators have been mentioned: one RC and one crystal controlled. These oscillators are analyzed elsewhere in National's applications literature (AN-118) so only a summary is given here.

RC Oscillator

An odd number of inverting gates (NAND, NOR, INVERTERS) will always oscillate if tied around on themselves as in *Figure 7.* Most beginning logic designers have discovered this fact of life by accident at one time or another.

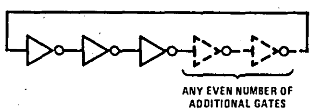


FIGURE 7. Odd Number of Gates Always Oscillates

Odd Number of Gates Always Oscillates

The oscillator will generate a square wave whose frequency will be determined by the propagation delay through the gates. All that remains to make this a useful oscillator is to control the frequency of oscillation. *Figure 8* depicts a simple and foolproof way to do this.

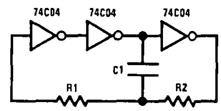


FIGURE 8. RC–CMOS Oscillator

The frequency of oscillation will be about f = 0.55/R2 C if R1 = R2. R2 has the most effect on frequency and in most applications it would be a pot. Stability of the oscillator as a function of time is dominated by the passive elements, especially at frequencies as low as 100 Hz or less. Variations in output drive capability of the CMOS will be swamped if R2 is 100k or more. Stability with respect to supply voltage in the range of voltages that can be used with the calculator chip (6.5–9.5V) is a function of frequency but the following is representative:

FREQUENCY	VARIATION (6.5–9.5V)
100 Hz	≈3%
10 Hz	≈0.5%

Empirically determined temperature drift of this oscillator due only to the CMOS is:

FREQUENCY	DRIFT
100 Hz	0.03%/°C (−15 → +50°C)
10 Hz	0.01%/°C

Crystal Oscillator

Figure 9 illustrates how to build a crystal oscillator using CMOS. This oscillator is also described in AN-118.

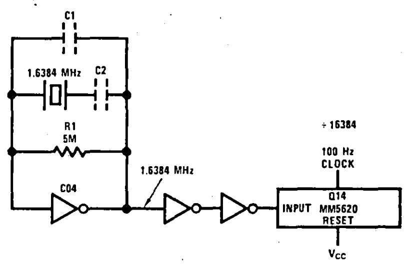


FIGURE 9. CMOS Crystal Oscillator and Divider for 100 Hz

The CMOS inverter is biased into its linear region by resistor R1. This dc path around the inverter ensures that the oscillator will start. C1 can be used to pull the crystal down and C2 to pull it up. The output of the oscillator is cleaned up by the next two inverters. This signal then is divided by 2^{14} or 16384 to yield the 100 Hz clock needed for the 0.01 second resolution timers.

The 0.1 second resolution timers could be obtained by using the dividing logic as suggested in *Figures 10 and 11.* The interval timer could use the 0.1 minute time base shown in *Figure 12.*

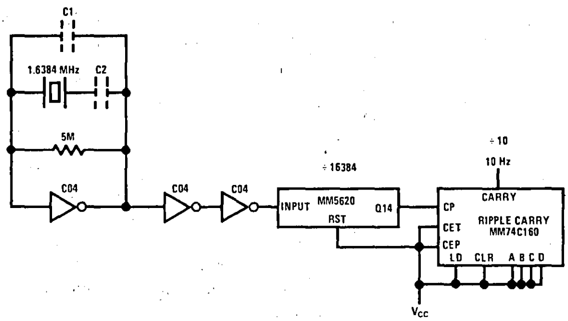


FIGURE 10. Divider for 10 Hz

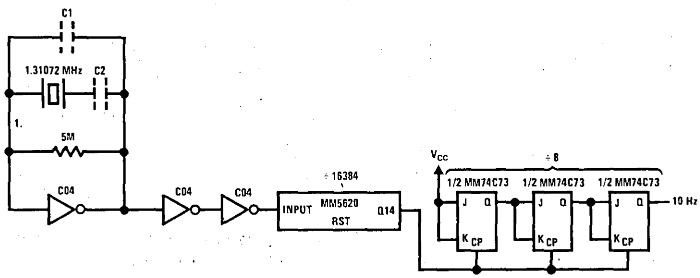


FIGURE 11. Alternate Divider for 10 Hz

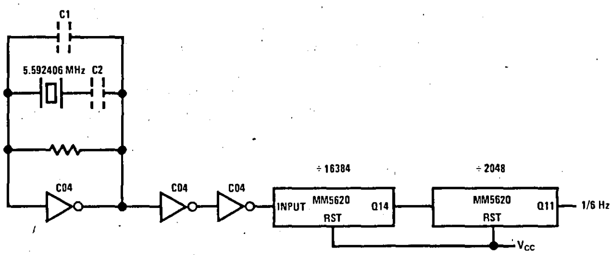


FIGURE 12. Divider for 1/6 Hz

SUMMARY

A rich variety of timing functions can be done digitally and many of these can be implemented with the MM5736 calculator chip. The MM5736 offers six decades of counting and display in one package and will yield low parts count solutions to many of these problems. It can be used in a variety of ways, it interfaces ideally with the 74C line of CMOS and consumes little power.

HANDHELD CALCULATOR BATTERY SYSTEMS

INTRODUCTION

Batteries suitable for handheld calculator applications can be categorized into two groups: primary cells and secondary cells. Primary cells cannot be recharged efficiently or safely and are used in "throw away" systems, i.e., the end user must replace the calculator batteries at end of life. Secondary cells can be recharged after being discharged under specified conditions.

PRIMARY CELLS

Carbon-zinc and alkaline are the best known non-rechargeable cells available for calculators. Carbon-zinc cells are low cost, but have relatively high internal resistance characteristics that reduce efficiency under high current drain conditions. They are widely available around the world in a variety of voltages, capacity and form factor options. Alkaline cells offer 300 to 400 per cent more capacity than carbon-zinc batteries of the same size and have excellent characteristics under the high drain conditions typical of LED display calculators. Both types have voltage discharge curves that fall gradually over life. Shelf life for alkaline is good, carbon-zinc poor; an important parameter if batteries are to be shipped with the finished calculator and may sit on warehouse or display shelves for unknown periods of time. Not surprisingly, alkaline cells are also three to four times more expensive than carbon-zinc. Silver oxide batteries have been used in throw-away calculator applications to achieve a more desirable form factor. Although replacements are available (the cells are often used in hearing aids and cameras) the high current drain inefficiency of the cell results in poor utilization of available capacity, and battery life is short.

SECONDARY CELLS

Nickel-cadmium batteries have become the standard for rechargeable systems. They exhibit relatively constant discharge voltages and can be recharged many times. Internal resistance is low so they are capable of supplying high peak currents.

Figure 1 indicates the discharge characteristics of carbon-zinc, alkaline and nickel-cadmium cells.

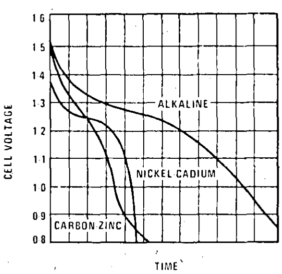


Figure 1. Comparison of Discharge Characteristics

THE SIMPLEST SYSTEM – A 9 V BATTERY

Most National Semiconductor calculator circuits use a P-channel, metal gate MOS process with enhancement and depletion mode transistors. They are designed to operate directly from a nine volt alkaline or carbon-zinc battery. Operating voltage range is 6.5 V to 9.5 V. A nine volt battery is simply six series cells with characteristics similar to those shown in Figure 1, allowing an end-point voltage for each cell of just under 1.1 V for a worst-case calculator.

A complete calculator using a nine volt battery is shown in Figure 2. This is undoubtedly the simplest battery system available for a low cost calculator, as well as being the most efficient. The current required to drive the display and MOS circuit comes directly from the battery without any conversion of voltage.

Battery life estimates are straightforward. Assuming a nine digit calculator using the National MM5760 slide rule chip, and five "8s" as a typical display condition, it is easy to calculate total battery current drain and battery life:

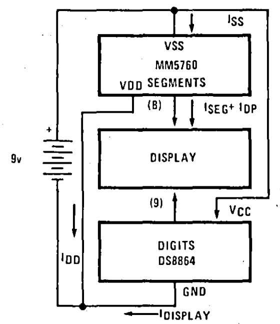


Figure 2. Power Supply Current for 9 V Calculator

Referring to Figure 2 and using typical values from the 5760 data sheet,

$$I_{DISPLAY} = I_{SEG}(Ave) + I_{DP}(Ave)$$

$$= (I_{SEG})\left(\begin{matrix}\text{no. of segments}\\ \text{on per digit}\end{matrix}\right)\left(\begin{matrix}\text{no. of digits}\\ \text{on per word}\end{matrix}\right)\left(\begin{matrix}\text{Digit Duty}\\ \text{Cycle}\end{matrix}\right) + I_{DP}$$

where I_{SEG} = Peak Segment Current

$$\text{Digit Duty Cycle} = \frac{(\text{Digit Time}) - (\text{Segment Blanking Time})}{(\text{Word Time})}$$

$$= \frac{70\ \mu s - 4.5\ \mu s}{650\ \mu s} \sim 0.100$$

Therefore, for a display of five "8s:"

$$I_{DISPLAY} = \left(\frac{8.5\text{ mA}}{\text{Seg}}\right)\left(\frac{7\text{Seg}}{\text{Digit}}\right)(5\text{ digits})(0.100)$$

$$= 29.75\text{ mA}$$

$$I_{BATTERY DRAIN} = I_{SS} = I_{DD} + I_{DISPLAY}$$

$$= 8.0\text{ mA} + 29.8\text{ mA} = 37.8\text{ mA}$$

Battery life is a function of the battery being used, of course, and its capacity. An alkaline 9 V battery has a capacity of approximately 550 mA-hr.

$$\text{Battery Life} = \frac{\text{Battery Capacity}}{I_{\text{BATTERY DRAIN}}} = \frac{550\ \text{mA-hr}}{37.8\ \text{mA}}$$

$$= 14.3\ \text{hr, typical}$$

As a comparison, a carbon-zinc 9 V battery is rated at only 125 mA-hr, giving a typical battery life of only 3.24 hr.

SOMETIMES SIMPLEST ISN'T BEST

In some cases it is not advantageous to design the calculator with a 9 V battery system. If the calculator is to be marketed in an area of the world where 9 V replacements are difficult to find, or a unique form factor is required to optimize overall calculator shape or size, alternate battery systems may be preferable.

Rechargeable systems are usually more cost effective as two, three or four cell systems. If it is decided to market both throw-away and rechargeable models of the same calculator, the battery system should allow the use of all the same hardware in both models; this means both primary and secondary batteries should be essentially the same form factor and voltage. N, AA and AAA cells all meet that requirement, and are often used in handheld calculators. Alkaline N and AAA cells are usually rated around 550 mA-hr and AA at over 1500 mA-hr. Nickel-cadmium cells supply about one third the capacity of physically equivalent alkaline cells, e.g., AA nickel-cadmium cells are rated about 500 mA-hr.

THE TWO CELL SYSTEM

Figure 3 shows the MM5760 in a two cell battery system. All the display and MOS current must be converted up to the 6.5 V to 9.5 V range needed to drive the MM5760.

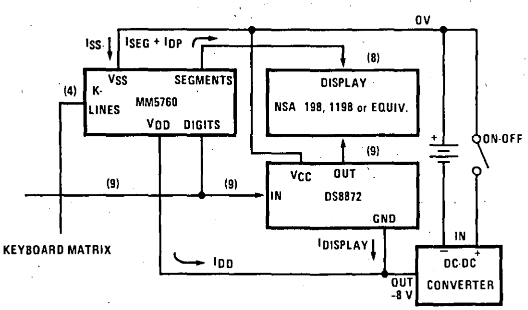


Figure 3. Two Cell Battery System

The DC-DC converter must supply greater than V_{SS} - 6.5 V with an input voltage range of 2.2 V to 2.5 V for nickel-cadmium cells or 2.2 V to 3.0 V for alkaline. Battery drain will be increased due to the voltage conversion and efficiency of the converter.

$$I_{\text{BATTERY DRAIN}} = (I_{DD} + I_{\text{DISPLAY}}) \frac{(V_{\text{CONVERTER}})}{(V_{\text{BAT}})(\text{EFF}_{\text{CONVERTER}})}$$

$(I_{DD} + I_{\text{DISPLAY}})$ will be the same as the 9 V case.

Assume the DC-DC converter has a nominal output voltage of 8.0 V, and an efficiency of 75%:

$$I_{\text{BATTERY DRAIN}} = (37.8\ \text{mA})\left(\frac{8.0\ \text{V}}{2.6\ \text{V}}\right)\left(\frac{1}{0.75}\right) = 155.1\ \text{mA}$$

If two AA alkaline cells were used, average battery life would be (1500 mA-hr/155.1 mA), or just over 9.6 hours; 500 mA-hr nickel-cadmium batteries would typically give 3.2 hours between recharges.

THREE CELLS INCREASE EFFICIENCY

Three cell systems provide a significant improvement in efficiency by reducing the converted power compared to a two cell system. Three cells have a minimum operating voltage of roughly 3.3 V. By using a bipolar segment driver chip to supply the required segment current at a low voltage, the display current loop can be separated from the higher-voltage MOS current path and operated directly off the three cell battery system. Now the low MOS supply current is the only component magnified by the voltage conversion, and the total power efficiency is greatly enhanced.

Figure 4(a) schematically shows the display interface of a three cell system. The DS8867 Segment Driver is guaranteed to supply a minimum of 8 mA of peak segment current to the LED display at an output voltage of 2.3 V (or higher) with respect to the negative terminal of the battery. The 2.3 V must be divided between the LED and "ON" digit driver output voltage; single output transistor (non-darlington) types of bipolar digit drivers such as the DS8868, DS8873, DS8973 or DS8879 have worst-case "ON" voltages of 0.5 V or less. With both worst-case digit and segment drivers, the LED will have 2.3 V - 0.5 V = 1.8 V as an "ON" voltage. GaAsP displays like the NSA1198 and NSA1298 show typical voltage drops of around 1.65 V at 10 mA of segment current on their data sheets. (If all worst-case components, including the LED were combined, a reduction in peak current could occur at minimum battery voltage.) For nine digit calculators using the NSA1198 and NSA1298 displays, the minimum peak current required for reliable operation is 3.0 mA/segment and 5.0 mA/segment, respectively, well below actual limits even with worst-case components.

To guarantee adequate digit output signals for scanning the keyboard, external series resistors (~ 2.4k) would be required if DS8873 digit drivers were used rather than the DS8973. Calculators requiring a shift driver, such as the MM5784 or MM5791, use a DS8879 digit driver in three cell systems.

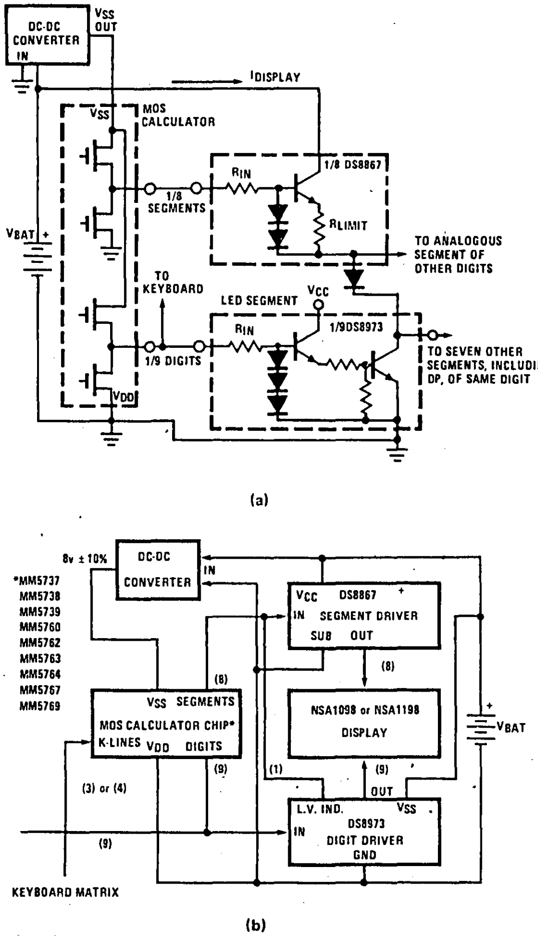


Figure 4 (a) Schematic Diagram, and (b) Block Diagram

With the exception of the MM5758 which is designed specifically to operate with a three cell battery system, all other National Semiconductor single chip calculators have low impedance segment output buffers suitable for driving LEDs directly. In a three cell system they will be capable of over-driving the DS8867. Typical input current to the DS8867 is about 1.5 mA per segment, which unfortunately must be converted up to the V_{SS} supply and therefore does impact battery life to some degree.

Using three AA alkaline cells would give a battery life of (1500 mA-hr/100.5 mA), or almost 15 hours; a 56% improvement over the two cell system for the additional cost of the DS8867 and an additional battery. 500 mA/hr ni-cad cells would provide 5.0 hours of continuous life. Note that this extended battery life is with higher display current than the two cell system, which will result in a brighter display as an added bonus.

FOUR CELL SYSTEM

A four cell battery system offers even higher power efficiency than the three cell system and the additional battery cost is offset somewhat by the removal of the DS8867. If the DC-DC converter output voltage is regulated between V_{SS} - 7.5 V and V_{SS} - 9.5 V, segments can be driven directly (Figure 5). Figure 6 shows the system diagram.

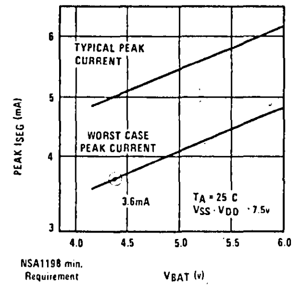


Figure 5. Guaranteed Peak Display Current vs. Battery Voltage in a Four Cell Battery System.

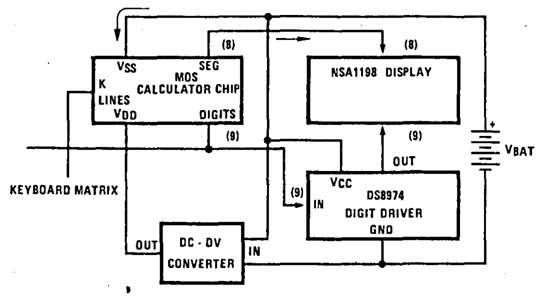


Figure 6. Four Cell Battery System

Like the three cell system, only the calculator supply needs to be converted up from the battery voltage. The display current flows in a loop from the positive terminal of the batteries, through V_{SS} and the segment buffers of the calculator chip to the LED, then the digit driver and back to the negative side of the batteries.

Typical battery drain for a display of five "8s" in a three cell system is:

$$I_{BAT} \cong \left\{ \left[I_{DD\,MOS} + (I_{SEG\,DRIVE\,MOS}) \begin{pmatrix}\text{Digit Duty}\\ \text{Cycle}\end{pmatrix} \begin{pmatrix}\text{no. of}\\ \text{segments on}\end{pmatrix} \right] \cdot \frac{V_{CONVERTER}}{V_{BAT} \cdot E_{FF\,CONVERTER}} + I_{SEG\,BAT} \begin{pmatrix}\text{Digit Duty}\\ \text{Cycle}\end{pmatrix} \cdot \begin{pmatrix}\text{no. of}\\ \text{segments on}\end{pmatrix} \right\}$$

$$I_{BAT} \cong \left\{ \left[8\text{ mA} + (1.5\text{ mA}) \left(\frac{5}{9}\right) (7) \right] \frac{8.0}{(3.6)\,(0.75)} + (17\text{ mA})\,(0.1)\,(5\text{ digits}) \left(\frac{7\text{ seg}}{\text{Digit}}\right) \right\}$$

$$= 100.49\text{ mA}$$

Battery drain current with five "8s" displayed is:

$$I_{BAT} = I_{DDMOS}\left(\frac{V_{CONVERTER}}{V_{BAT}\cdot E_{FF\,CONVERTER}}\right) + I_{DISPLAY}$$

$$\cong (10\text{ mA})\left[\frac{8.75}{(4.8)\,(0.75)}\right] + \left(\frac{8.5\text{ mA}}{\text{seg}}\right)\left(\frac{7\text{ seg}}{\text{Digit}}\right)(5\text{ Digits})\,(0.1)$$

$$= 54.0\text{ mA}$$

Using four AA cells would give a battery life of at least (1500 mA-hr/54.0 mA), or almost 28 hours of continuous use. Four smaller capacity cells could be used to improve the form factor of the finished calculator and still maintain a reasonable battery life. For example, four alkaline N cells would give almost 10 hours of operation.

Table 1.

No. of Battery Cells	Calculator Type	Segment Driver	Digit Driver	DC-DC Converter	Typical Battery Life with AA Alkaline Cells
2	Group A	None	DS8872	$2.0\text{ V} \leqslant V_{IN} \leqslant 3.0\text{ V}$ $6.5\text{ V} \leqslant V_{OUT} \leqslant 9.5\text{ V}$ $I_{OUT} \leqslant -125\text{ mA}$	9.6 hours
2	Group B	None	DS8874	$2.0\text{ V} \leqslant V_{IN} \leqslant 3.0\text{ V}$ $6.5\text{ V} \leqslant V_{OUT} \leqslant 9.5\text{ V}$ $I_{OUT} \leqslant -125\text{ mA}$	7.7 hours
3	Group A	DS8867	DS8872 or DS8973	$3.0\text{ V} \leqslant V_{IN} \leqslant 4.5\text{ V}$ $7.2\text{ V} \leqslant V_{OUT} \leqslant 8.8\text{ V}$ $I_{OUT} \leqslant 20\text{ mA}$	15.0 hours
3	Group B	DS8867	DS8879	$3.0\text{ V} \leqslant V_{IN} \leqslant 4.5\text{ V}$ $7.2\text{ V} \leqslant V_{OUT} \leqslant 8.8\text{ V}$ $I_{OUT} \leqslant -20\text{ mA}$	15.0 hours
3	MM5758	DS8867	DS8868	$3.0\text{ V} \leqslant V_{IN} \leqslant 4.5\text{ V}$ $7.2\text{ V} \leqslant V_{OUT} \leqslant 8.8\text{ V}$ $I_{OUT} \leqslant -25\text{ mA}$	14.5 hours
4	Group A	None	DS8872 or DS8974	$4.4\text{ V} \leqslant V_{IN} \leqslant 6.0\text{ V}$ $-7.5\text{ V} \leqslant V_{OUT} \leqslant -9.5\text{ V}$ $I_{OUT} \leqslant 20\text{ mA}$	28.0 hours
4	Group B	None	DS8876	$4.4\text{ V} \leqslant V_{IN} \leqslant 6.0\text{ V}$ $-7.5\text{ V} \leqslant V_{OUT} \leqslant -9.5\text{ V}$ $I_{OUT} \leqslant 20\text{ mA}$	23.5 hours
9 V	Group A	None	DS8873 or DS8864	None	14.0 hours
9 V	Group B	None	DS8874	None	11.3 hours

Group A Calculators

MM5737 MM5762
MM5738 MM5763
MM5739 MM5764
MM5760 MM5767
MM5769

Group B Calculators

MM5784
MM5791

Calculators

USING STANDARD NATIONAL CALCULATORS IN INDUSTRIAL AND MICROPROCESSOR APPLICATIONS

It is frequently desirable to utilize a calculator component in non-calculator applications. Because of their low cost, these devices represent a cost effective method of sophisticated number processing. A few hints that are worthwhile to keep in mind when applying calculators are listed below.

KEYBOUNCE AND NOISE REJECTION

The National line of calculators are designed to interface with low-cost keyboards, which are often the least desirable from a false or multiple entry standpoint.

When a key closure is sensed by the calculator, an internal time-out is started. Any voltage perturbations of significant magnitude which occur on the Key Input Lines during the time-out will reset the timer to zero. A key is accepted as valid only after a noise-free time-out period: noise that persists indefinitely will inhibit key entry. Key releases are checked in the same manner.

READY SIGNAL OPERATION

The Ready signal indicates calculator status. When the calculator is in an "idle" state, the output is at a logical high level (near V_{SS}). When a key is closed, the internal key entry timer is started. Ready remains high until the time-out is complete and the key entry is accepted as valid. As the calculator begins to process the key, Ready goes low (near V_{DD}).

Ready remains at a low level until the function initiated by the key is complete *and* the key is released and timed out. The low-to-high transition indicates the calculator has returned to the "idle" state and a new key can be entered. *Figure 1* shows the relationship between keyboard entries and Ready.

Ready can be very helpful in a non-calculator application. It can be used in the following manner:

1) Whenever Ready is at a logic high, enter keys.
2) Whenever Ready is at a logic low, inhibit all keys and wait.
3) The transition from low to high indicates that an external machine can change states. Also, after a period of time, the display is valid and can be sampled.

ZERO SUPPRESSION

All calculators have some form of zero suppression. For left-justified displays, it is trailing zero suppression which is relatively easy to implement and fast. Right-justified displays require leading zero suppression. While this doesn't require much more logic, it is much slower. This can play an important role in using a calculator which must transfer results to other logic elements. After Ready goes high, it can take up to 7 word times before the segment information is correct. Consult Table I for specifics.

Figure 2 illustrates circuits for accomplishing the speed-ups given in Table I.

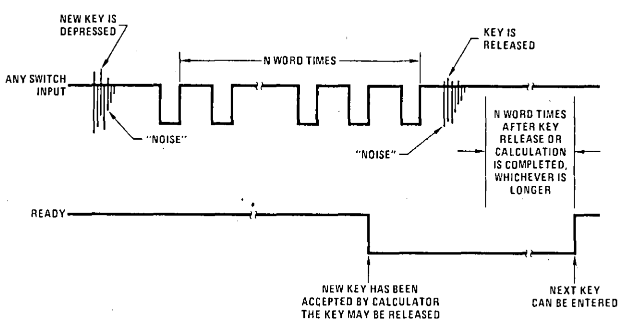
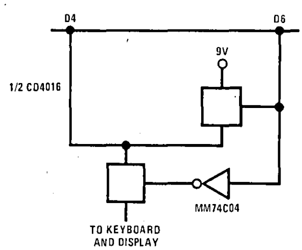


FIGURE 1. Functional Description of Ready Signal and Key Entry



If the inverter is unavailable, a CD4016 and resistor suffice.

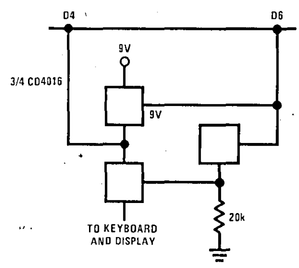


FIGURE 2. Calculator Speed Up Circuits

In many cases, a calculator circuit can be applied in a microprocessor system to eliminate the necessity of writing extensive floating point software routines. *Figure 3* shows such a system developed for a SC/MP microprocessor. Due to variations in power supply voltages and logic levels between SC/MP and the MM5760 Mathematician calculator, a combination of CMOS and low power Schottky components has been used. The MM5760 was chosen for this particular application because 3 other pin compatible calculators, the MM5762, MM5763 and MM5764 (Statistical, Financial and Metric Conversion) calculators will fit into the same socket and provide different algorithms.

Table II describes these functions and the codes that the SC/MP must present to the input register. SC/MP may operate either in an interrupt driven mode or through the use of the sense input. When programming the SC/MP calculator systems, it is advisable to perform the functions in the same manner as one would when operating the corresponding Novus or National Semiconductor calculator.

TABLE I

CALCULATOR	NORMAL KEY BOUNCE TIME	DEFEATED KEY BOUNCE TIME	HOW TO DEFEAT KEYBOUNCE	READY	DISPLAY CORRECT FOLLOWING READY PLUS	POWER ON CLEAR	LONG CAL	WHEN CAN SEGMENTS BE SAMPLED
MM5736, MM5749 MM5757	7–8 words	3-4 words	D4 high during D6	No		No	220 ms	Middle of digits
MM5737	7–8 words	3–4 words	D7 high during D9	Yes	7 words	No	350 ms	Trailing edge of digits
MM5738	7–8 words	3–4 words	D7 high during D9	Yes	7 words	No	350 ms	Trailing edge of digits
MM5739	7–8 words	3–4 words	D4 high during D9	No		No	300 ms	Middle of digits
MM5758	7 words	4 words	TC high during D3	Yes	0 words	Yes	3.1 sec	Middle of digits
MM5760, MM5762, MM5763, MM5764	9 words down, 16 words up	same	none	Yes	0 words	Yes	3 sec	Middle of digits
MM5765	Uses ready					Yes	40 ms	
MM5766	Uses ready					Yes	40 ms	
MM5780	7–8 words	3–4 words	D7 high during D9	Yes	0 words	No	350 ms	
MM5784	7–8 words	3–4 words	Connect K2 to D9	Yes	7 words	Yes	580 ms	Middle of digits
MM5791	11 words	2 words	Connect K2 to D9	Yes	7 words	Yes	580 ms	Middle of digits
MM5777	7–8 words	3–4 words	D6 high during D7	Yes	5 words	No	300 ms	Trailing edge of digits

TABLE II

CONTROL BYTE (HEXIDECIMAL)	FUNCTION OUTPUT SELECT FOR DIGITS 1–9			
00–08	MM5760	MM5762	MM5763	MM5764
11	–*	–	–	–
12	+*	+	+	+
13	÷*			
14	X*	X	X	X
15	–		Freq*	KS*
16	TAN	JAL*	$\bar{X}$	Ft–in
17	SIN	LOAN*	COR	In–mm
18	COS	SAV*	INT	IN–cm
20	1/X	SOD	Ex	mile-km
21	e^X	i*	REMy	Ft–m
22	y^X	AMT	y	–
23	LOG	–	x	MC
24	Ln	$Y^{\bar{X}}$	REMx	yd–m
25	Vx*	M+	M+	M+*
26	STO*	MR*	MR*	MR*
27	C	C	C	C
41	EN	=	=	=*
42	RCL	=+	=+	=+
43	k	CS	CS	CS*
44	•	•	•	•*
45	9	9	9	9*
46	8	8	8	8*
47	7	7	7	7*
48	6	6	6	6*
80	5	5	5	5*
81	4	4	4	4*
82	3	3	3	3*
83	2	2	2	2*
84	1	1	1	1*
85	0	0	0	0*
86	ARC*	n*	CA*	–
87	CS	%	%	%*

*Multiple function key—refer to individual data sheets

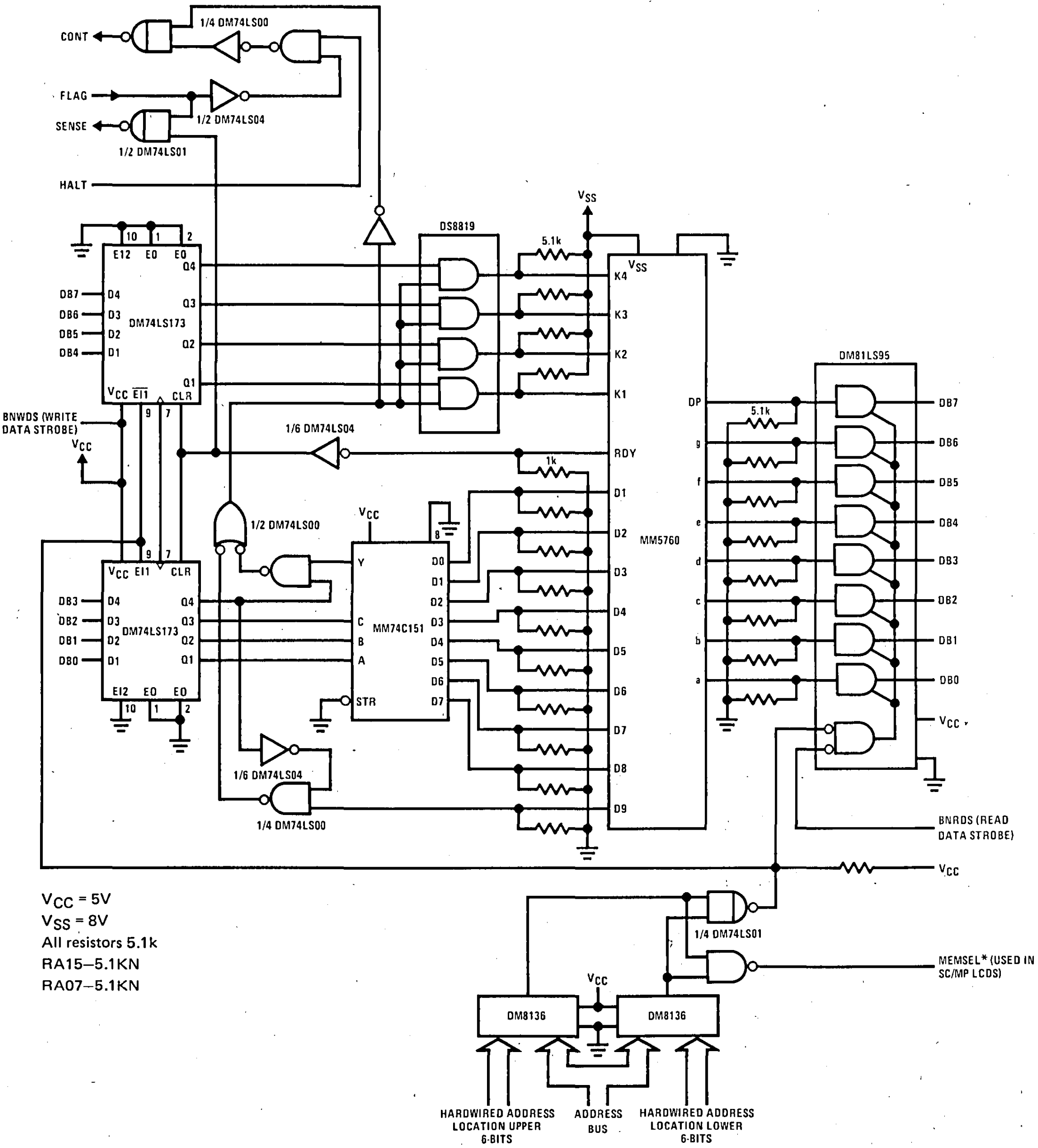


FIGURE 3. MM5760 SC/MP Interface

Operation of the circuit is straight forward; when the 8-bit control word is applied to the input register, a 9-bit multiplexer is addressed by the lower 4 bits, selecting a digit line. The upper 4 bits then gate the digit output through to the key inputs; the Ready line clears the input register and indicates acceptance to the processor. When the Ready line returns to its original state, another command may be entered. To receive the output of the calculator, the processor should load the lower 4 digits of the input register with the code corresponding to the digits required and the upper 4 digits with zeroes—the multiplexer output signal then indicates availability of data.

In an SC/MP system, synchronization with data is accomplished by first loading the digit code as described and immediately entering the HALT state. The multiplexer output then drives the CONTINUE input. On start-up, the processor immediately loads the data.

In the application shown, 7-segment data plus decimal point is output to the data bus. Alternatively, one can use a 7-segment to BCD converter, DM86L25 or MM74C915, to connect the calculator output to BCD data.

A sample flow chart for the microcomputer program is depicted in *Figure 4*.

In summary, a reasonably low cost, low speed, arithmetic capability may be added to most systems using existing calculator components and standard logic.

TABLE III. Hexidecimal Conversion for 7-Segment Output

DIGIT	WITHOUT DECIMAL POINT	WITH DECIMAL POINT
0	3F	BF
1	06	86
2	5B	DB
3	4F	CF
4	66	E6
5	6D	ED
6	7D	FD
7	07	87
8	7F	FF
9	6F	EF
•		80
BLANK	00	80

Note: 0.0.0.0.0.0.0.0. indicates an illegal entry. All decimal points indicate the battery save mode.

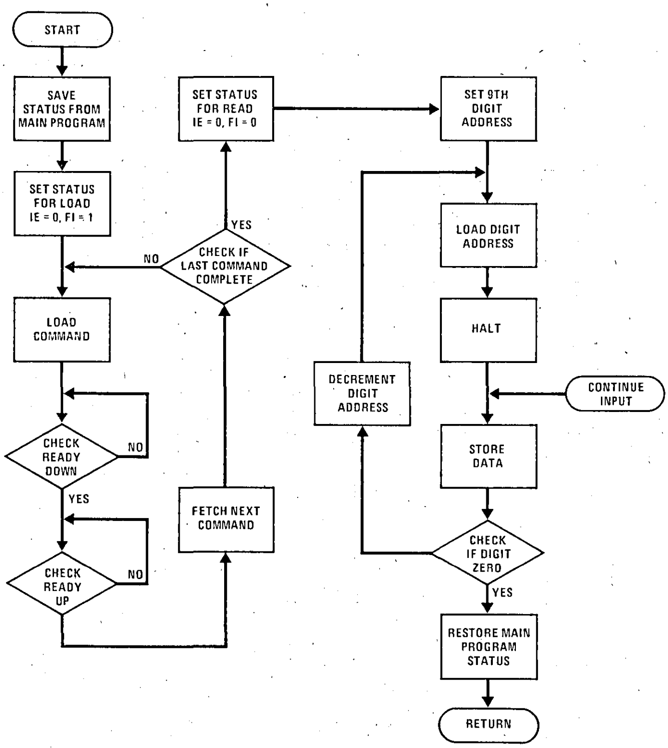


FIGURE 4

SECTION 9
CONTROLLER ORIENTED PROCESSOR SYSTEMS (COPS)

COPS

National's Controller Oriented Processor Systems

introduction

National's Controller Oriented Processor Systems provide a low cost solution to low end computing and control problems. Manufactured by NSC's volume proven P-channel MOS/LSI controller process, the COPS offers an attractive, low risk alternative to custom LSI when available development time is short and cost is critical. Single mask programming of the on-chip control ROM allows delivery of prototype devices directly from the calculator production lines.

Architectural features of the COPS permit rapid efficient design and implementation of systems using key or switch inputs and display or printer outputs. Interface circuits in the COPS are designed to allow expansion of system memory and I/O capability without sacrificing the "lowest component count" features of the set.

Elements in the COPS family provide four levels of processing capability from the dedicated MM57140 single chip system with direct display and keyboard interface to the highly flexible MM5782 based multi-chip systems.

features

- National's COPS feature P-channel metal gate process for lowest cost
- Single power supply operation
- CMOS compatibility
- Serial I/O ports for easy communication between processor and peripheral circuits
- Expandable RAM and ROM
- BCD in/out option for applications flexibility
- Direct interfacing to keyboard and display
- 10 μs instruction cycle
- 4-bit data/8-bit instruction word
- Single mask programmable
- Learn mode programmability

COPS elements

- Automobile displays
- Oven controllers
- Vending machines
- Specialty calculators
- Simple electronic cash registers
- Computing instruments
- Electronic scales
- Printer/display controller
- Appliance controller
- Data terminal controller
- Automated gasoline pumps
- Alpha/numeric programmable calculators

applications

MM5781	– 16k control and ROM element
MM57129	– 32k control and ROM element
MM5782	– Memory and processor element
MM5785	– Memory interface to 1024 x 1 RAM devices
MM5788	– Printer interface to Seiko printers
MM5799	– Single chip microcomputer
MM57140	– Single chip microcomputer
DS8664/5/6	– Decoder, digit driver and oscillator
DS8692	– Hex power driver (single)
DS8693	– 8-bit latch and driver (source)
MM57126	– Programmer shift register

MM5781, MM5782 Controller Oriented Processor Systems

general description

The National MM5781, MM5782 is a set of MOS/LSI circuits designed for application in low cost, versatile, dedicated or custom programmed calculator and control systems.

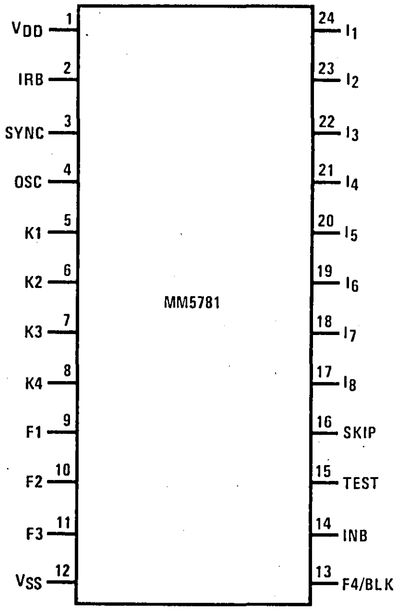
A full capability scientific or business calculator system can be built using only four circuits, plus the keyboard, case, battery and LED display. Application as a printing calculator or in electronic cash registers is possible using National's MM5788 printer interface circuit. Both the basic ROM instruction store and read/write store are expandable.

features

- 2048 x 8-bit ROM, expandable to 8192 x 8
- 640 bits (160 digits) RAM, expandable using MM5785
- 8 parallel outputs, coded as 7-segment + d.p. or BCD
- Serial data I/O for easy interface to peripheral circuits
- 3 general purpose I/O latches
- Blanking output
- 4 strobed key inputs
- $10\mu s$ micro-instruction cycle time
- Single power supply operation
- 4-bit data/8-bit instruction words

connection diagrams

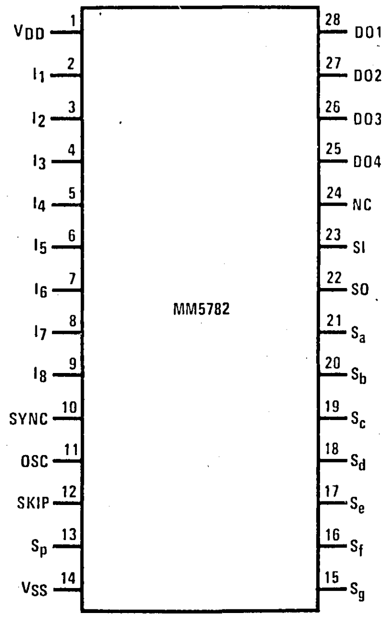
Dual-In-Line Package



TOP VIEW

Order Number MM5781N
See Package 22

Dual-In-Line Package



TOP VIEW

Order Number MM5782N
See Package 23

absolute maximum ratings

Voltage at Any Pin Relative to V_{SS} (All Other Pins Connected to V_{SS})	V_{SS} +0.3V to V_{SS} −12V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

(0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage (V_{SS} − V_{DD})		7.9		9.5	V
Operating Supply Current (I_{DD})	V_{SS} − V_{DD} = 9.5V, T_A = 25°C				
MM5781			−7	−12	mA
MM5782			−15	−25	mA
OSC Input Voltage Levels					
Logical High Level (V_{IH})	V_{SS} − V_{DD} = 7.9V	V_{SS}−1.0			V
Logical Low Level (V_{IL})	V_{SS} − V_{DD} = 9.5V			V_{DD}+1.5	V
OSC Input Resistance to V_{SS}	(Note 3), *(Figure 2)*				
MM5781 Only (R_{IN})			3	6	kΩ
INB, K1–K4, F1–F3 Input Voltage Levels					
Logical High Level (V_{IH})	V_{SS} − V_{DD} = 7.9V	V_{SS}−3.2			V
	V_{SS} − V_{DD} = 9.5V	V_{SS}−4.5			V
Logical Low Level (V_{IL})	7.9V ≤ V_{SS} − V_{DD} ≤ 9.5V			V_{DD}+1.5	V
INB, K1–K4 Input Current Levels					
Logical High Level Current (I_{IH})	V_{IH} = V_{SS} − 3.2V (LED Display Interface)			−350	μA
Logical Low Level Current (I_{IL})	V_{IL} = V_{SS} − 32V (Fluorescent Display Interface)	−20		1	μA
IRB Input Voltage Levels					
Logical High Level (V_{IH})	7.9V ≤ V_{SS} − V_{DD} ≤ 9.5V	V_{SS}−3.5			V
Logical Low Level (V_{IL})	V_{SS} − V_{DD} = 7.9V			V_{DD}+2.5	V
	V_{SS} − V_{DD} = 9.5V			V_{DD}+3.0	V
I_1–I_8, SI, SKIP, SYNC and TEST Input Voltage Levels	V_{SS} − V_{DD} = 7.9V				
Logical High Level (V_{IH})		V_{SS}−1.2			V
Logical Low Level (V_{IL})				V_{SS}−4.0	V
DO 1, DO 2 and DO 4 Output Voltage Levels					
Logical High Level (V_{OH})	R_L = 150k, to V_{DD}	V_{SS}−1.0		V_{SS}	V
Logical Low Level (V_{OL})	I_{OL} = 3μA	V_{DD}		V_{DD}+0.5	V
Logical High Level Current (I_{OH})	V_{OH} = V_{DD} + 1.5V, V_{SS} − V_{DD} = 7.9V			−260	μA

dc electrical characteristics (con't)

(0°C to +70°C unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DO 3 Output Voltage Levels					
Logical High Level (V_{OH})	R_L = 150k, to V_{DD}	V_{SS}−1.0		V_{SS}	V
Logical Low Level (V_{OL})	I_{OL} = 3μA	V_{DD}		V_{DD}+0.5	V
Logical High Level Current (I_{OH})	Battery Low "OFF"				
	V_{OH} = V_{DD} + 3V, V_{SS} − V_{DD} = 9.5V	−1.3		−0.3	mA
	V_{OH} = V_{DD} + 2.5V, V_{SS} − V_{DD} = 7.9V	−1.0		−0.4	mA
	Battery Low "ON"				
	V_{OH} = V_{SS} − 3V, V_{SS} − V_{DD} = 7.9V			−0.3	mA
	V_{OH} = V_{SS} − 3V, V_{SS} − V_{DD} = 9.5V			−0.4	mA
S_a through S_g and S_p Output Current Levels	LED Display Interface to DS8867				
Logical High Level Current (I_{OH})	V_{OH} = V_{DD} + 5.4V			−500	μA
Logical Low Level Current (I_{OL})	V_{OL} = V_{DD} + 0.5V	−1		1	μA
	Fluorescent Display Interface				
Logical High Level Current (I_{OH})	V_{SS} − V_{DD} = 7.9V, V_{OH} = V_{SS} − 6V			−300	μA
Logical Low Level Current (I_{OL})	V_{OL} = V_{SS} − 32V, R_{EXT} = 150k to V_{GG} = V_{SS} − 35V	−20			μA
I_1 − I_8, S0, SYNC and SKIP Output Voltage Levels	V_{SS} − V_{DD} = 7.9V				
Logical High Level (V_{OH})	I_{OH} = −100μA	V_{SS}−0.5		V_{SS}	V
Logical Low Level (V_{OL})	I_{OL} = 15μA	V_{DD}		V_{DD}+3.7	V
F1 − F3 Output Voltage Levels	7.9V $\leq$ V_{SS} − V_{DD} $\leq$ 9.5V				
Logical High Level (V_{OH})	I_{OH} = −30μA	V_{SS}−1.5			V
Logical Low Level (V_{OL})	I_{OL} = 3μA			V_{DD}+1.0	V
F4 (BLK) Output Voltage Levels	7.9V $\leq$ V_{SS} − V_{DD} $\leq$ 9.5V				
Logical High Level (V_{OH})	I_{OH} = −0.5 mA	V_{SS}−1.5			V
Logical Low Level (V_{OL})	I_{OL} = 5μA			V_{DD}+1.0	V
Voltage Levels for All Outputs into CMOS Level					
Logical High Level (V_{OH})	I_{OH} = −10μA	V_{SS}−0.5		V_{SS}	V
Logical Low Level (V_{OL})	R_L = 200k (to V_{DD})	V_{DD}		V_{DD}+0.5	V
Maximum Allowable Keyboard Closed Key Resistance Using INB, F1−F3 or K1−K4 as Inputs					
R_{KEY}	LED Display Interface			200	Ω
R_{KEY}	Fluorescent Display Interface			50	kΩ

ac electrical characteristics MM5781 – 0°C to +70°C, unless otherwise noted *(Figure 1)*

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSC Input Frequency ($1/t_p$)		320		400	kHz
OSC Input Duty Cycle		46	56	66	%
OSC Input Transition Times	(Note 3), *(Figure 2)*				
Fall Time (t_f)	C_L = 25 pF, R_L = 6 kΩ, to V_{SS}			50	ns
Rise Time (t_r)	RC = 0.15µs			350	ns
SYNC Input Timing (Bit Time)					
Interval Time (t_b)		10		12.5	µs
Hold Time (t_{osch})		100			ns
High-to-Low Set-Up Time (t_{stl})		680			ns
Low-to-High Set-Up Time (t_{sth})		100			ns
K1 – K4, INB, F1 – F3 Input Timing					
Set-Up Time (t_{sk})		6.5			µs
Hold Time (t_{hk})		1.0			µs
SKIP Input Timing					
Set-Up Time (t_{sx})		280			ns
Hold Time (t_{hx})		1.0			µs
IRB, $I_1 - I_8$ Input Timing					
Set-Up Time (t_{si})		1.75			µs
Hold Time (t_{hi})		1.0			µs
SKIP Output Propagation Delay (t_{pdx})	C_{LOAD} = 250 pF			4.4	µs
$I_1 - I_8$ Output Propagation Delays	C_{LOAD} = 250 pF				
Low-to-High (t_{pdhi})				3.6	µs
High-to-Low (t_{pdli})				3.0	µs
F1 – F3 Output Propagation Delay (t_{pdf})	C_{LOAD} = 100 pF			4.4	µs
F4 Output Propagation Delay (t_{pdf})	C_{LOAD} = 50 pF			4.4	µs
F4 Output Transition Time					
Rise Time (t_r)	$C_{LOAD} \geq 20$ pF	0.3			µs

timing diagram (See notes in *Figure 2.*)

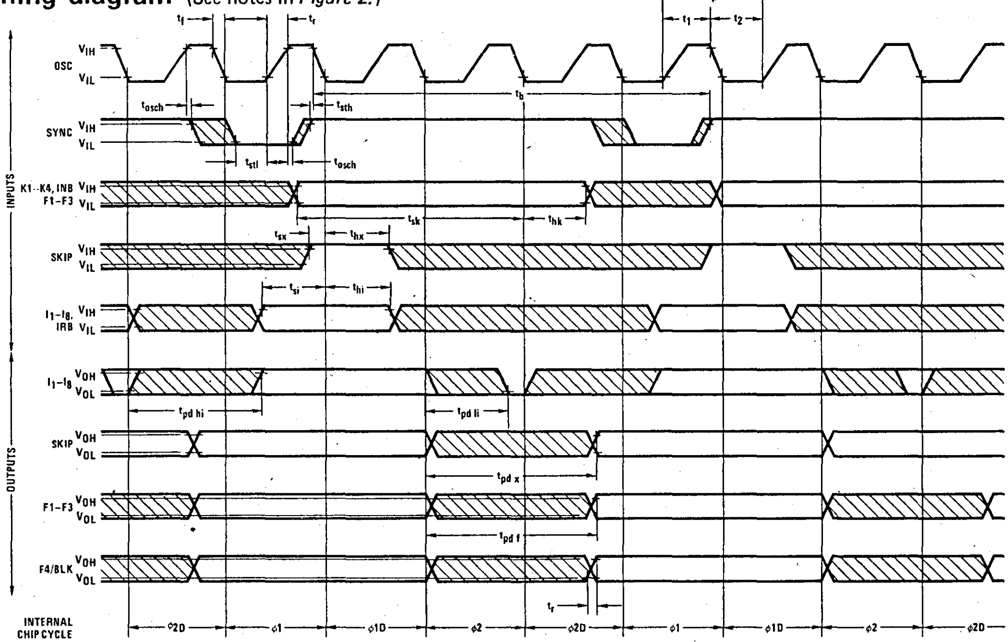


FIGURE 1. MM5781 Input/Output Waveform Timing