Programming the NS32FX200 for Use with a Contact Image Sensor (CIS) Scanner

National Semiconductor
Application Note 821
Varda Karpati
April 1992

INTRODUCTION

The NS32FX200 is a highly integrated system chip designed especially for a FAX voice application based on a National Semiconductor NS32FX161, NS32FX164 or NS32FV16 embedded processor. The NS32FX200 provides a complete video (scanner) solution.

The main features of the scanner controller are:

- Programmable generation of synchronization signals for CIS or Charge Coupled Device (CCD) scanners
- Two on-chip Digital-to Analog Convertors (DAC) for shading correction, dithering and Gamma correction
- Automatic writing of scanned bitmap to memory via a DMA channel
- Support for line scan times of 2.5 ms, 5 ms, 10 ms and 20 ms
- Support for external image enhancement

The NS32FX200 system chip supports a wide range of CIS scanners. This application note uses the scanner input signals of the Seiko Epson LSA4U130 CIS scanner as an example.

This document describes how to program the NS32FX200 for use with your CIS scanner. It should be considered an addition to, and be used with, the NS32FX200 Data Sheet.

1.0 SCANNING WITH THE NS32FX200

The scanning process in the NS32FX200 includes the following operations:

- Synchronization Signals generation
- Video Signal processing
- Pixel digitization
- Pixel Bitmap generation

The software activates the signal generator block by setting the SCAN bit in the MCFG register to 1. The signal generator block then generates five synchronization pulses, SNH, $\overline{\text{SDIS}}$, $\overline{\text{SLS}}$, SPDW and SCLK2. See block diagram in *Figure 1.*

The Scan Line Synchronization ($\overline{\text{SLS}}$) signal indicates the beginning of a new scanned line. The frequency of the $\overline{\text{SLS}}$ pulse is controlled by the Scanner Period Pulse (SPP) register, and may be 400 Hz (2.5 ms per line), 200 Hz (5 ms per line), 100 Hz (10 ms per line), or 50 Hz (20 ms per line).

When DMA channel 0 is enabled, it is synchronized by the NS32FX200 scanner controller to the internal Scanner Active Video Window (SAVW) signal, which defines the total time during which the scanner controller collects data. The NS32FX200 scanner controller outputs a Scanner Peak Detect Window (SPDW) signal to the sample and hold circuit. This signal defines the time period during which the scanner controller calculates the peak current of the input pixels. The time period defined by SPDW occurs during the time period defined by the SAVW signal.

When the software activates the DMA0 bit in the MCFG register and the CHEN bit in the CNTL0 register, it enables DMA channel 0 to operate with the internal scanner controller. The channel starts the required DMA operation, i.e., it requests the first two bytes, to fill the double buffer reference line. This line is then sent to the CIS scanner.

For each scanner pixel, the NSFAX software uses a successive approximation algorithm to evaluate the exact correction value needed to compensate for the difference between the maximum (white) analog value and the actual value of these pixels. These 8-bit correction values are stored in memory as ''white line correction values''. After the white line correction values are evaluated, scanning may start.

During scanning, the white line correction value for each pixel that was synchronized to the Sample and Hold (SNH) signal, is transferred to the double buffer reference line. The correction value from the compensation MDAC, and the analog input, Scanner Video Input (SVI) signal, are both fed into the video DAC from the sample and hold circuit. The video DAC then produces the compensated analog level of the pixel, Scanner Compensated Video Output (SCVO). The SVCO signal is input to the current comparator and to the Automatic Background Control (ABC) circuit.

At the same time, for each pixel, 8-bit data from the eight dithering registers, and the Scanner Background (SBG) signal from the ABC circuit, are fed into a second Multiplying Threshold DAC (MDAC) that produces a darkness threshold level.

During bi-level dithering, each of the eight dithering registers contains a constant threshold value, and the peak detected value of the SCVO register is input to the MDAC via the SBG input signal.

During gray scale dithering, the eight dithering registers contain eight different threshold levels, and the SBG input signal is forced to a constant level.

The compensated analog value of a pixel, and its darkness threshold level, are fed to the current comparator that creates a digital 0 or 1 signal. This bit is input to a pixel generator. The output from the pixel generator is shifted into a shift register. When the shift register is full, and DMA channel 2 is enabled by setting the Channel Enable (CHEN) bit in the CNTL2 register, the shifted word is written to the output buffer, and via DMA channel 2 to memory.

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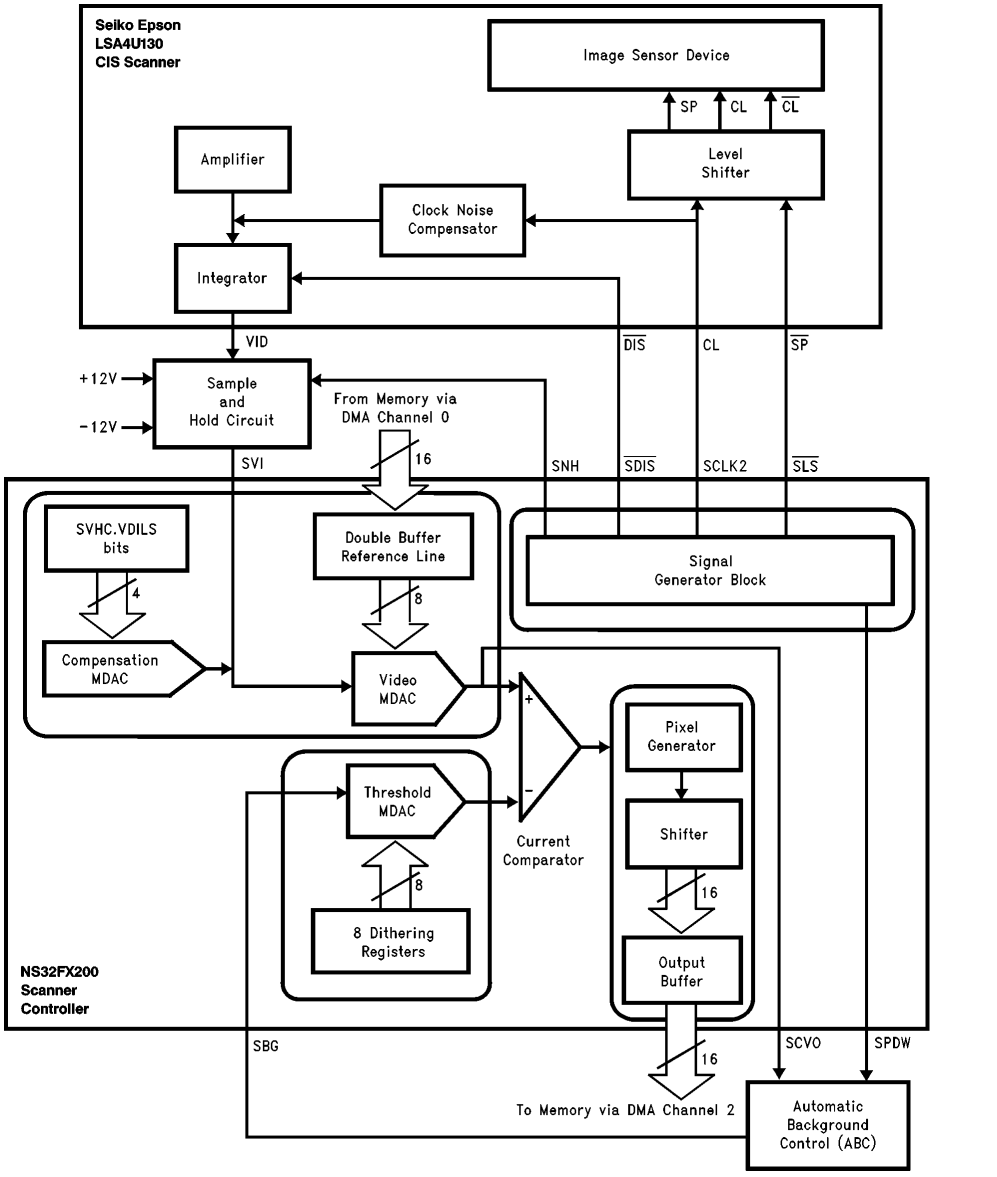

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FIGURE 1. CIS Scanner Block Diagram

2.0 LSA4U130 CIS SCANNER SIGNALS

The Seiko Epson LSA4U130 CIS scanner requires three synchronization signals as input. The input signals are generated in the NS32FX200 by the signal block generator. In addition, one output signal is generated by the CIS scanner.

$\overline{SP}$ **Synchronization Pulse of the Scanned Line.** This signal indicates the beginning of a scan line.

CL **Scanner Clock.** The clock frequency equals 200 kHz. CIS scanners use a single phase clock, unlike CCD scanners which use a dual-phase clock.

$\overline{DIS}$ **Discharge Signal.** This signal discharges the VID output signal.

VID **Video Output Signal.** This signal contains the current level of the scanned pixel.

Figure 2, together with the following table, shows the timing requirement of the Seiko Epson LSA4U130 CIS Scanner signals, and the relations between these requirements.

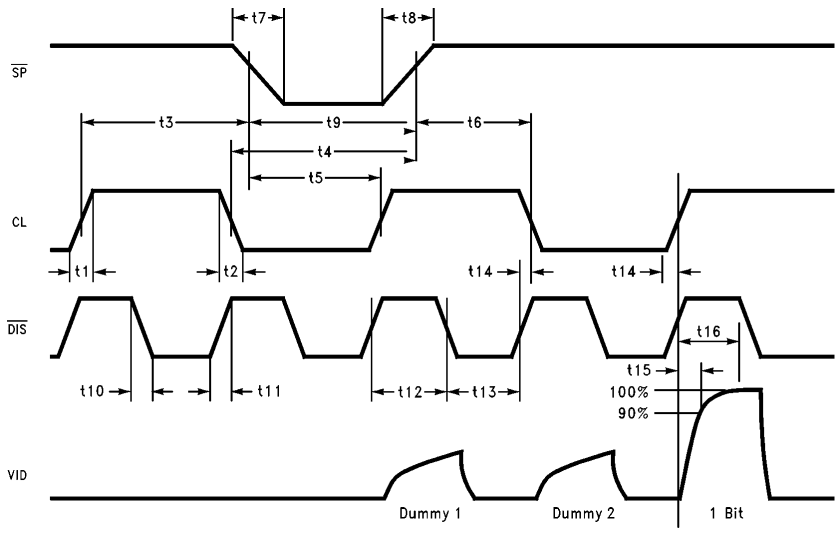

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FIGURE 2. Scanner Signal Timing Requirements

Item		Min	Max	Units	Description
CL Rise & Fall Time	t1, t2		100	ns	
CL and $\overline{SP}$ Relationship	t3	600		ns	t3 defines the time between the rising edge of CL and the falling edge of $\overline{SP}$.
	t4	800		ns	t4 defines the time between the falling edge of CL and the rising edge of $\overline{SP}$.
	t5	800		ns	t5 defines the time between the falling edge of $\overline{SP}$ and the rising edge of CL.
	t6	800		ns	t6 defines the time between the rising edge of $\overline{SP}$ and the falling edge of CL.
$\overline{SP}$ Rise & Fall Time	t7, t8		100	ns	
$\overline{SP}$ Pulse Width	t9	1000		ns	t9 defines $\overline{SP}$ pulse width.
$\overline{DIS}$ Rise and Fall Time	t10, t11		100	ns	
$\overline{DIS}$ Pulse Width	t12	1875		ns	t12 defines $\overline{DIS}$ high level time (The time between the rising edge of CL and the falling edge of $\overline{DIS}$).
	t13	625		ns	t13 defines $\overline{DIS}$ pulse width.
$\overline{DIS}$ and CL Relate	t14	0	100	ns	
VID(0%–90%)	t15		1500	ns	t15 defines the time in which VID output changes from 0% to 90% of its value.
VID Sampling Period	t16	1600	t12	ns	t16 defines VID sampling period (SNH active time) limits.
$\overline{SP}$, CL, $\overline{DIS}$ Input Voltage	V_{IH}	4.0	V_{DD}	V	
	V_{IL}	GND	1.0	V	

The signal block generator also generates, in addition to the CIS scanner control signals, an SNH signal that is sent to the sample and hold circuit. The sample and hold circuit uses it to sample the VID signal that is output from the CIS scanner.

When the VID signal reaches about 90 percent of its maximum value, the sample and hold circuit generates a signal that holds the pixel value for approximately 80 per cent of the pixel cycle, in order to ease the digital and analog signal timing requirements of the internal NS32FX200 scanner controller.

Approximately 90 per cent of the value of the pixel should be sampled and held. The SNH signal should not be active when the output line is discharged. The minimum delay between any edge of CL and the rising edge of SNH for the Seiko Epson LSA4U130 scanner is 1.6 μs (t16).

After the sample and hold operation is finished, the scanner output should be prepared for the next pixel by the $\overline{DIS}$ signal.

The minimum delay between an edge of CL and the falling edge of $\overline{DIS}$, for the LSA4U130 scanner, is 1.875 μs (t12). The minimum width of the $\overline{DIS}$ signal is 0.625 μs (t13).

The delay plus the width of the $\overline{DIS}$ signal is 2.5 μs, i.e., CL phase width.

Note 1: The frequency of the SNH and $\overline{DIS}$ signals (400 kHz) is twice that of the CL signal (200 kHz).

Note 2: The minimum time required by the scanner to scan one pixel is 2.5 μs. The maximum time per pixel is limited by the maximum time from the beginning of one line to the beginning of the next line, which may not exceed 5 ms. There may be up to 1728 pixels plus four to six dummy pixels in a line.

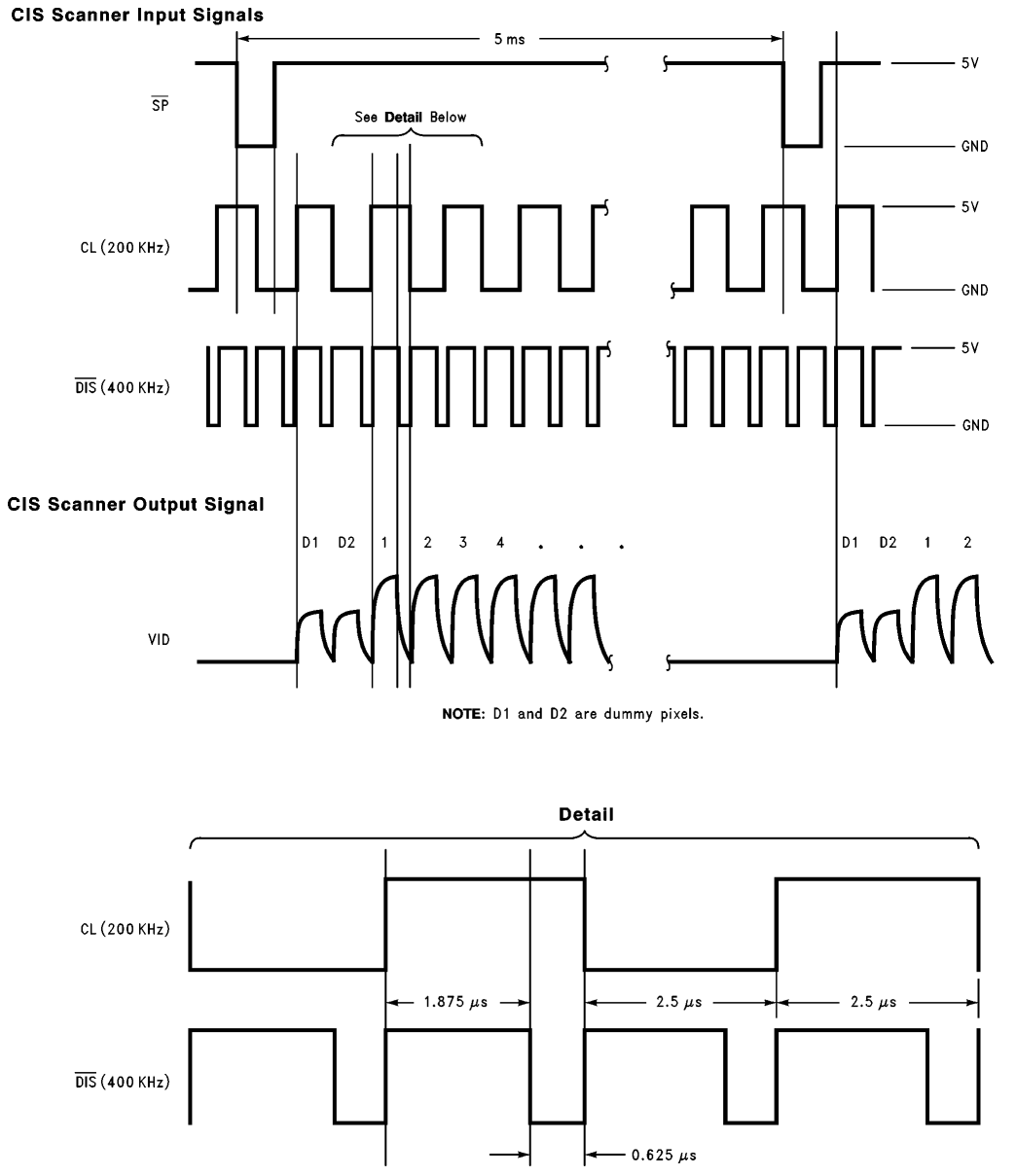

FIGURE 3. Timing for CIS Scanner Signals Produced by the NS32FX200

3.0 PROGRAMMING THE SCANNER CONTROLLER

This section describes how the NS32FX200 scanner controller supports CIS scanners. It is divided as follows:

- Generation of synchronization signals
- DMA and ports support
- Values to be loaded to NS32FX200 registers to meet the requirements of the Seiko Epson LSA4U130 CIS scanner.

3.1 Generation of Synchronization Signals

The synchronization signals are generated by the signal generator block, shown in the block diagram in *Figure 1.* The internal synchronization signals are described here, in the order in which they occur in the scanning operation. This section also includes descriptions of the NS32FX200 registers that configure the signal generator block.

Note that the frequency used in calculations in this application note is 19.6608 MHz and $CTTL_{cycle\ time} = 50.86$ ns.

3.1.1 The Synchronization Signals

SPP **Scanner Period Pulse Signal.** All scanner signals are synchronized by this internal signal, which defines a period of 2.5 ms, 5 ms, 10 ms, or 20 ms, i.e., the line scan time. Line scan time is calculated by dividing each 20 ms into 256 time slots, and monitoring the Time Slot (TSL) bus. The SPP is defined by the SPP register.

(SPP = EF)

The period of each pulse is 2.5 ms (TSL = 255, 31, 63, 95, 127, 159, 191 and 223)

(SPP = DF)

The period of each pulse is 5 ms (TSL = 255, 63, 127 and 191)

(SPP = BF)

The period of each pulse is 10 ms (TSL = 255 and 127)

(SPP = 7F)

The period of each pulse is 20 ms (TSL = 255)

The Seiko Epson LSAU4130 CIS Scanner requires a scan line time of 5 ms. SPP should, therefore, be programmed with the value of ''DF''.

SCLK2 **Scanner Clock Signal.** This signal corresponds to the CL signal in the Seiko Epson LSA4U130 scanner. SCLK2 is generated by dividing CTTL by the prescaled value that is in the SPRES register.

The CL frequency is determined by the scanner $\overline{DIS}$ signal timing requirements. In order to determine the pixel clock frequency, we must first fulfill the $\overline{DIS}$ signal timing requirements.

$\overline{SDIS}$ **Scanner Discharge Signal.** This signal corresponds to the $\overline{DIS}$ signal in the Seiko Epson LSA4U130 scanner. The $\overline{SDIS}$ signal should meet the Seiko Epson LSA4U130 timing requirements of a minimum value of 1.875 μs for (t12) $\overline{SDIS}$ hightime, and a minimum value of 0.625 μs for (t13) $\overline{SDIS}$ width. The parameters of SDIS are programmed using the following two control registers:

SDISD **Scanner Discharge Delay Register.** SDISD is a write-only, byte-wide register at address $FE0204_{16}$. SDISD controls the delay between the edge of SCLK2 and the leading edge of $\overline{SDIS}$.

The delay is (SDISD + 1) CTTL cycles.

The value programmed by this register should produce a hightime that meets the t12 requirement of a minimum of 1.875 μs.

CTTL = 50.86 μs
(SDISD + 1) * CTTL $\geq$ 1.875 μs
SDISD $\geq$ (1.875 μs/50.86 ns) $-$ 1
SDISD $\geq$ 35.87

Minimum SDISD = 36

We recommend programming the minimum value for every signal timing requirement, so as to define the minimum pixel clock.

The time between one scanner period pulse and the next (5 ms) is divided into the scanning line time and the software interrupt handling time. If the line scanning time is minimized, then more time is left for the interrupt handling.

We will program SDISD with its minimum value, SDISD = 36.

SDISW **Scanner Discharge Width Register.** SDISW is a write-only, byte-wide register at address $FE0206_{16}$.

The width of the signal is (SDISW + 1) CTTL cycles.

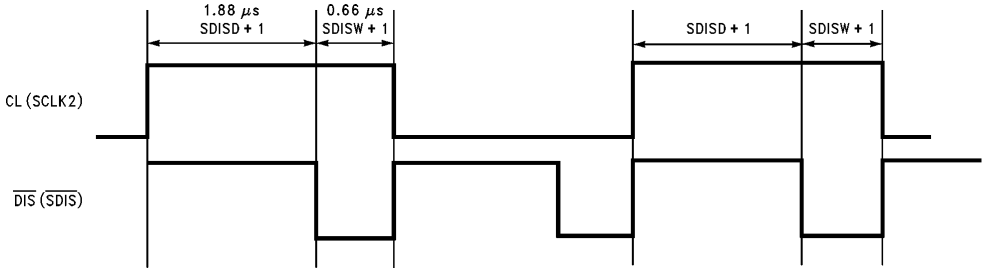

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FIGURE 4. $\overline{SDIS}$ Signal

The value programmed by this register should produce a Scanner Discharge width time that meets the t13 requirements of a minimum of 0.625 μs.

(SDISW + 1) * CTTL $\geq$ 0.625 μs

SDISW $\geq$ (0.625 μs/50.86 ns) $-$ 1

SDISW $\geq$ 11.28

We will program the minimum SDISW value = 12.

The programmed values define delay and width times of:

$SDIS_{delay}$ = (36 + 1) * 50.86 ns = 1.88 μs

$SDIS_{width}$ = (12 + 1) * 50.86 ns = 0.66 μs

The pixel clock is, therefore:

$\overline{SDIS}_{hightime}$ + $\overline{SDIS}_{width}$ = 1.88 μs + 0.66 μs = 2.54 μs

The pixel clock cycle time defines CL (SCLK2) phase time. SCLK2 cycle time is 5.08 μs. SCLK2 (CL) frequency is defined by using the prescale value programmed in the SPRES register.

SPRES **Scanner Prescale Register.** SPCLK = CTTL/(SPRES + 1). SPRES is a write-only, byte-wide register at address $FE0222_{16}$.

$SPCLK_{cycle\ time}$ = $CTTL_{cycle\ time}$ * [2 * (SPRES + 1)] = 2 * 2.54 μs = 5.08 μs

5.08 μs = 50.86 ns * [2 * (SPRES + 1)]

SPRES = (5.08 μs/2 * 50.86 ns) $-$ 1 = 49

The timing requirements of t1, t2, t7, t8, t10, t11 are guaranteed by design.

The next signal to determine is the Sample and Hold (SNH) pulse.

SNH **Sample and Hold Pulse.** This signal corresponds to the SNH in the Seiko Epson LSA4U130 scanner. The SNH signal should meet the Seiko Epson LSA4U130 timing requirements of a maximum t15 (VID 0%–90%) of 1.5 μs, and a t16 (VID sampling period) which extends from a minimum of 1.6 μs to a maximum of 1.87 μs. The parameters of SNH are programmed using the following two control registers:

SNHD **Sample and Hold Delay Register.** SNHD is a write-only, byte-wide register at address $FE0208_{16}$. SNHD controls the delay between the edge of SCLK2 and the leading edge of SNH.

The delay is (SNHD + 1) CTTL cycles.

(SNHD + 1) * 50.86 ns $\geq$ 1.6 μs

SNHD $\geq$ 30.46

Min SNHD = 31

Programmed value should be 31

SNH_{delay} = 32 * 50.86 ns = 1.63 μs

SNHW **Sample and Hold Width Register.** SNHW is a write-only, byte-wide register at address $FE020A_{16}$.

The width of the signal is (SNHW + 1) CTTL cycles.

The SNH signal should be deactivated before $\overline{SDIS}$ goes low—1.88 μs after the edge of SCLK2.

SNH_{delay} + SNH_{width} should not exceed 1.88 μs.

[(SNHD + 1) + (SNHW +1)] * 50.86 ns $\leq$ 1.88 μs

SNHW $\leq$ 3.864

SNHW will be programmed with the value of 3.

SNH_{width} = (3 + 1) * 50.86 ns = 0.2 μs

SNH_{delay} + SNH_{width} = 1.63 μs + 0.2 μs = 1.83 μs $\leq$ 1.88 μs

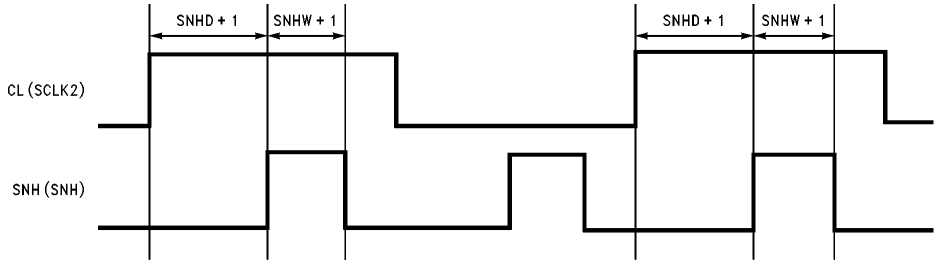

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FIGURE 5. SNH Signal

SCLK2, SNH and SDIS are signals related to pixel scan:

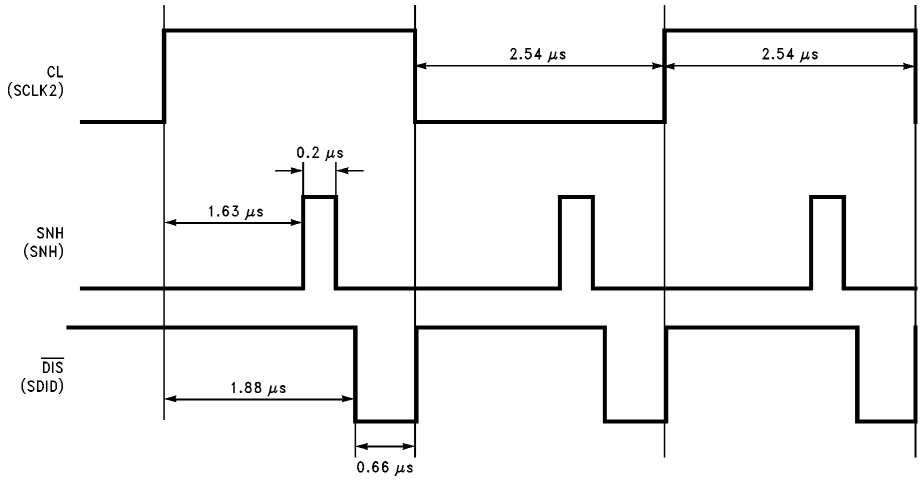

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FIGURE 6. Pixel Synchronization Signals

There is another internal signal related to pixel scan.

The internal comparator reset signal controls the window of time during which the current comparator operates. The signal resets the comparator from the SNH leading edge till the end of the programmed time delay. During this time the SNH circuit prepares its output (SVI), and the internal VIDEO MDAC and the threshold MDAC prepare their outputs. When the internal comparator reset signal becomes inactive, the comparator is activated. The comparator remains active till the end of the pixel cycle. During this time it compares the compensated video with the threshold; the result is then sampled into the bitmap shifter, at the rising edge of SNH. The internal reset comparator signal active time is controlled by the SCMPRW register.

SCMPRW Scanner Comparator Preset Width Register. The preset signal divides the pixel clock time, between two consecutive SNH leading edges, into comparator reset time and comparator active time.

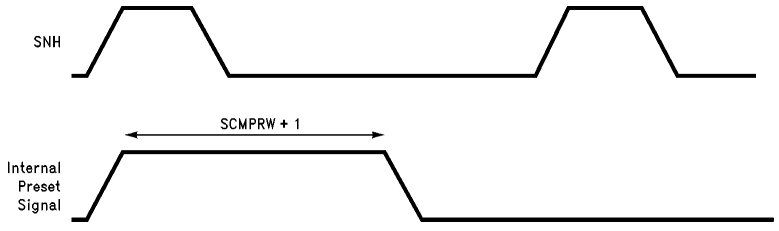

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FIGURE 7. Scanner Comparator Preset Signal

The internal analog reset width (SCMPRW + 1) is equal to, or greater than the SVI set-up time plus 200 ns.

The SVI set-up time is determined by the performance of the SNH circuit. The analog reset should be terminated at least 300 ns before the next SNH leading edge.

min SCMPRW $\rightarrow$ (SCMPRW + 1) * $CTTL_{cycle\ time} \geq SVI_{setup}$ + 200 ns

max SCMPRW $\rightarrow$ [(SPRES + 1) − (SCMPRW + 1)] * $CTTL_{cycle\ time} \geq$ 300 ns

min SCMPRW = $(SVI_{setup}/CTTL_{cycle\ time})$ + 3

max SCMPRW $\rightarrow$ SCMPRW $\leq$ 50 − 1 − (300 ns/50.86 ns) = 43.1

max SCMPRW = 43

To achieve the highest possible speed and accurately the reset signal should be active during 70 percent of the pixel cycle, starting from the leading edge of SNH

SCMPRW + 1 = 70% (SPRES + 1) $\rightarrow$ SCMPRW = 50 * 0.7 − 1 = 34

SCMPRW = 34

The next stage, after the signals related to pixel processing have been calculated, is to calculate the signals related to the whole line.

$\overline{SLS}$ **Scan Line Synchronization Pulse.** This pulse indicates the beginning of a new scan line. SLS corresponds to the SP signal in the Seiko Epson LSA4U130 scanner. $\overline{SLS}$ signal timing is determined according to Seiko Epson LSA4U130 timing requirements t3, t4, t5, t6, and t9 (see *Figure 2*). $\overline{SLS}$ parameters are programmed using the following two control registers:

SLSD **Scanner Line Synchronization Delay Register.** SLSD is a write-only, byte-wide register at address $FE020C_{16}$. SLSD controls the delay from SPP to the leading edge of $\overline{SLS}$.

t3 defines the minimum time between the rising edge of SCLK2 and the falling edge of $\overline{SP}$ ($\overline{SLS}$). The minimum time for t3 is 0.6 μs.

SCLK2, after SPP, is low, therefore the SLSD should take into consider- ation the SCLK2 lowtime plus the t3 requirement.

(SLSD + 1) * 50.86 ns $\geq$ 2.54 μs + 0.6 μs

SLSD $\geq$ 60.74

SLSD = 61

SLSW **Scan Line Synchronization Pulse Width Register.** SLSW is a write-only, byte-wide register at address $FE020E_{16}$. The width of the signal is (SLSW + 1) CTTL cycles.

t9 defines the pulse width minimum time. The minimum time for t9 is 1 μs

(SLSW + 1) * 50.86 ns $\geq$ 1 μs

SLSW $\geq$ 18.66

The minimum value is 19.

$CTTL_{cycle\ time}$ * [(SLSD + 1) + (SLSW + 1)] + t6 = 4 * 2.54 μs

t6 minimum time is 0.8 μs.

therefore:

max (SLSD + SLSW) $\leq$ 184.03

max (SLSD + SLSW) = 184

80 (minimum value) $\leq$ SLSD + SLSW $\leq$ 184 (maximum value)

We shall program the registers with the values:

SLSD = 73, SLSW = 49.

80 < SLSD + SLSW = 122 < 184

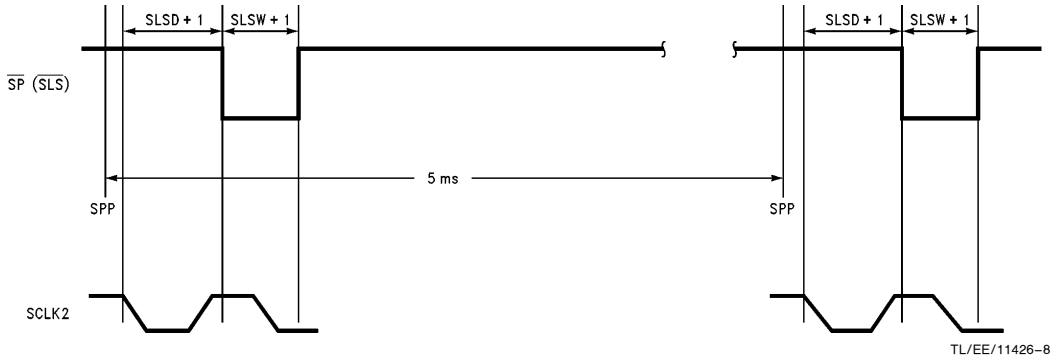

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FIGURE 8. SLS Signal

The following calculations confirm that the delay and width of the SLS signal meet t3, t4, t5, t6 and t9 requirements.

t3 = [(73 + 1) − (49 + 1)] * 50.86 ns = 1.22 μs > 0.6 μs

t9 = $\overline{\text{SLS}}_{\text{width}}$ = 50 * 50.86 ns = 2.54 μs > 1 μs

t3 + t9 + t6 =

3*(CL phase time) = 3*2.54 μs

1.22 μss + 2.54 μs + t6 = 7.62 μs

t6 = 3.86 μs > 0.8 μs

t6 + t4 = 2 * (CL phase time) = 2 * 2.54 μs

3.86 μs + t4 = 5.08 μs

t4 = 1.22 μs > 0.8 μs

t5 + t3 = 2 * (CL phase time) = 5.08 μs

t5 = 5.08 μs − 1.22 μs = 3.86 μs

t5 = 3.86 μs > 0.8 μs

The following signal timing to determine is SAVW.

SAVW **Scanner Active Window Signal.** This signal defines the time interval during which reference lines are applied via DMA channel 0, and sampled pixels are stored as digital data via DMA channel 2. SAVW signal timing is calculated so that 1728 pixels will be scanned during the signal active time, and ignored pixels during the signal delay time. During SCLK2 phase one pixel is scanned. SCLK2 phase time is pixel clock SP.

The parameters of SAVW are programmed using the two following control registers:

SAVWD **Active Video Window Delay Register.** SAVWD is a write-only, word-wide register at address $FE0210_{16}$ that controls the delay between the leading edge of the Scanner's Period Pulse (SPP) and the beginning of the active video window, i.e., the number of ignored pixels. The number of ignored pixels is four. This includes the delay of two pixels from SPP to the end of SLS plus a further two dummy pixels.
(SAVWD + 1) = number of ignored pixels = 4
SAVWD = 3

SAVWW **Active Video Window Width Register.** SAVWW is a write-only, word-wide register at address $FE0212_{16}$.

The width of the signal is (SAVWW + 1) pixels.

During the SAVW width 1728 pixels should be scanned.
1728 = (SAVWW + 1)
SAVWW = 1727

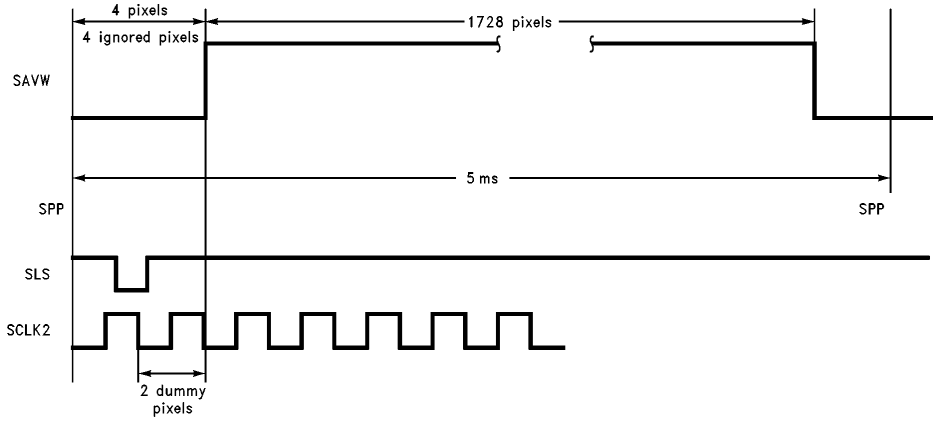

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FIGURE 9. SAVW Signal

SPDW **Scanner Peak Detection Window Signal.** This signal enables definition of a time interval during which the peak detector of the ABC is changed. To achieve the best results, charge the ABC only when the real document is scanned. In the following example, we assume that the width of the narrowest document scanned is half an A4 page, and that the document is centered. In other mechanical set-ups, the document is adjusted to either the left or the right of the scanner, and the ABC window will be shifted accordingly

The parameters of SPDW are programmed using the following two control registers:

SPDWD **Peak Detection Window Delay Register.** SPDWD is a write-only, word-wide register at address $FE0214_{16}$ that controls the delay between the leading edge of the scanner's period pulse (SPP) and the beginning of the peak detector window.
SPDWD + 1 = (1728/4) + 4 ignored pixels = 436 ⟶ SPDWD = 435

SPDWW **Peak Detection Window Width.** SPDWW is a write-only, word-wide register at address $FE0216_{16}$.
The width of the signal is (SPDWW + 1) pixels. 1728/2 = SPDWW + 1 = 864 ⟶ SPDWW = 863

3.1.2 Signal Generation Block Configuration Registers

The registers described in this section configure the signal generation block of the NS32FX200 for use with a Seiko Epson LAU4130 CIS scanner.

SGC **Signals Generator Control Register.** The polarity of the synchronization signals is controlled by programming the SGC register.

7 4	3	2	1	0
reserved	LSPP	PDWP	SNHP	DISP

DISP **Scanner Discharge Pulse Polarity.**
0 = Active low
1 = Active high

SNHP **Sample and Hold Pulse Polarity.**
0 = Active low
1 = Active high

PDWP **Peak Detector Window Polarity.**
0 = Active low
1 = Active high

LSPP **Line Synchronization Pulse Polarity ($\overline{SLS}$).**
0 = Active low
1 = Active high

SVHC **Scanner Video Handling Control Register.**

7	6	5	4 0
reserved	BYPASS	INVERT	VDILS

VDILS **Video DAC Input Level Shift.** (Sign bit + 4 bits) This field indicates the number of current steps to be added to the input of the Video DAC.
Each step is 8 μA.

INVERT The pixel is inverted by the pixel generator if this bit is set to 1.

BYPASS The SBYPS input signal is selected by the pixel generator, and the comparator output is ignored, if this bit is set to 1.

3.2 Scanner Controller DMA and Ports Support

This section describes how to configure and program DMA channels 0 and 2 to function as internal channels. When so configured, DMA channels 0 and 2 provide the scanner controller with reference lines, and enable the scanner to output bitmap data.

3.2.1 Configuring DMA Channels 0 and 2 as Internal

To configure DMA channels 0 and 2, of the NS32FX200, to function as internal channels, perform the following operations:

1. Define DMA channel 0 as internal, by setting bit 4, DMA0, in the MCFG register to 1.
2. Define scanner signals SCLK, SDIS, SPDW and SLS as outputs from the scanner controller module, by setting bits 4, 6, 9 and 11 of the Port B Module Select (PBMS) register to 1.
3. Enable scanner output signals by setting bit 0 of the Port B Output Enable (PBEN) register to 1.
4. Define SNH scanner signal as output from the scanner controller module by setting bit 2 of the Port C Module Select (PCMS) register) to 1.
5. Enable the scanners SNH signal as output by setting bit 2 of the Port C Output Enable (PCEN) register to 1.

3.2.2 Programming Internal DMA Channels 0 and 2

ADCA0, ADCA2

Device Address Counters for DMA Channels 0 and 2, respectively. Bits 0–23 hold the current address of the source data in the addressed device. Bits 24–31 are reserved, and should be cleared to 0. After each DMA transfer, if the ADA bit of the MODE0 register or MODE2 corresponding register is set to 1, the corresponding ADCA is updated as defined by the DEC bit in that MODE register. ADCA0 and ADCA2 should be programmed to have even addresses.

BLTC0, BLTC2

Block Length Counters for DMA Channels 0 and 2, respectively. Bits 0-23 hold the current number of bytes to be transferred. Bits 24-31 are reserved, and should be cleared to 0. The appropriate BLTC counter is decremented by 2 after each DMA transfer.

MODE0, MODE2

Mode Control Registers for DMA Channels 0 and 2, respectively. The appropriate MODE register is used to specify the operating mode of each channel.

15 10	9	8 4	3	2	1	0
reserved	ADA	reserved	DIR	res	DEC	res

DEC **Decrement/Increment the appropriate ADCA Register.**
0 = Increment ADCA0 or ADCA2 after each transfer cycle, if ADA is set to 1.
1 = Decrement ADCA0 or ADCA2 after each transfer cycle, if ADA is set to 1.

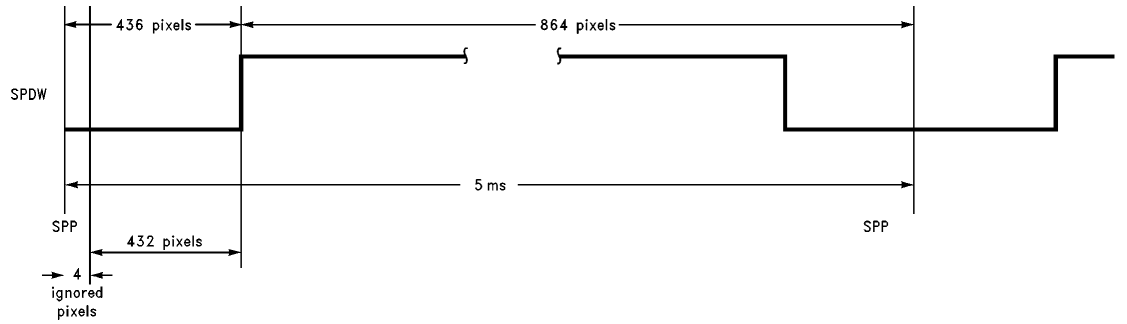

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FIGURE 10. SPDW Signal

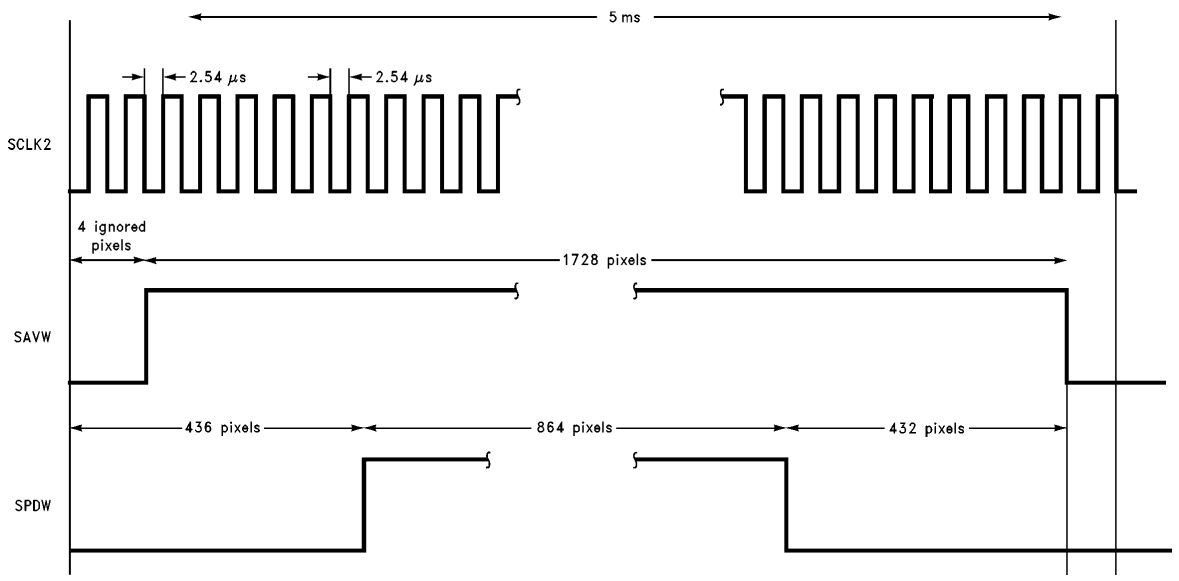

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FIGURE 11. Line Synchronization Signals

DIR **Transfer Direction.** In MODE0 this bit should be cleared to 0. Implied I/O is the destination. In MODE2 this bit should be set to 1. Implied I/O is the source.

ADA **Device Address Control.** The ADA bit controls updating of the corresponding ADCA counter, after each transfer cycle, as follows:

0 = Do not change the address stored in the relevant ADCA.

1 = Change the address stored in the relevant ADCA.

STAT0, STAT2

Status Register for DMA Channels 0 and 2, respectively. These registers hold status information for DMA channels 0 and 2 respectively, and are used to enable or mask the appropriate DMA interrupt when the corresponding counter reaches 0, i.e., when the transfer is completed.

7 5	4	3	2 1	0
reserved	ETC	CHAC	reserved	TC

TC **Terminal Count.** The appropriate TC is set to 1 when its corresponding BLTC counter reaches 0, i.e., when the transfer is completed.

CHAC **Channel Active.** The appropriate CHAC bit is set to 1 when DMA channel 0 or 2 is active, i.e., when the CHEN bit in the corresponding CNTL register is set to 1, and the corresponding BLTC counter is greater than 0. CHAC is read only.

ETC **Enable Terminal Count.** ETC enables an interrupt when its corresponding BLTC counter reaches 0.

0 = Disable interrupt.

1 = Enable interrupt.

CNTL0 Only bit number 0, the Channel Enable bit, CHEN, is used to enable or disable DMA channels. This bit should only be set to 1 after all the other registers for the relevant channel have been programmed.

CHEN **Channel Enable.**

0 = Disable channel 0.

1 = Enable channel 0.

3.3 Loading the NS32EX200 Registers

Use the values provided in this section to program the registers of the NS32FX200 CIS scanner controller to meet the requirements of the Seiko Epson LSA4U130 CIS scanner for scanning at 19.6608 MHz. These values will generate the synchronization signals that are output to the CIS scanner, SNH circuit and the ABC circuit, and will provide the necessary ports and DMA support.

Four groups of registers should be programmed: the signal generation block registers, the frequency controller registers, the I/O port registers and the DMA controller registers.

3.3.1 The Signal Generation Block Registers

SPP = DF_{16}

A period pulse is issued every 5 ms (TSL = 255,63, 127 and 191).

SPRES = 49

SPCLK = CTTL/(SPRES + 1) = 19.6608/(49 + 1) = 0.394 MHz = 394 kHz

CTTL/2(SPRES + 1) = 19.6608/2 (49 + 1) = 0.197 MHz = 197 kHz

SLSD = 73

The delay from SPP is (SLSD + 3) CTTL cycles, or 3.87 μs.

SLSW = 49

The width of $\overline{SLS}$ is (SLSW + 1) CTTL cycles, or 2.54 μs.

SDISD = 36

The delay from SCLK2 edge is (SDISD + 1) CTTL cycles, or 1.88 μs.

SDISW = 12

The width of $\overline{SDIS}$ is (SDISW + 1) CTTL cycles, or 0.66 μs.

SNHD = 31

The delay from SCLK2 edge is (SNHD + 1) CTTL cycles, or 1.63 μs.

SNHW = 3

The width of SNH is (SNHW + 1) CTTL cycles, or 0.20 μs.

SGC = 6

$\overline{SDIS}$ active low

SNH active high

SPDW active high

$\overline{SLS}$ active low

SAVWD = 3

The delay in CTTL cycles from first SCLK2 rising edge is ((SAVWD * (SPRES + 1)) − 1), or 7.58 μs.

SAVWW = 1727

The width of SAVW is (SAVWW + 1) SPCLK cycles, or 4.39 ms.

SPDWD = 435

The delay in CTTL cycles, from the first rising edge of SCLK2 is (SPDWD * (SPRES + 1)), or 1.11 ms.

SPDWW = 863

Width of SPDW is (SPDWW + 1) SPCLK cycles, or 2.19 ms.

SCMPRW = 34

It is recommended the internal comparator reset signal be activated when: SPCLK reaches 70 per cent of its cycle time

or:

(SPRES + 1) * 70% = (SCMPRW + 1) or:

(49 + 1) * 70% = 35 = (34 + 1)

3.3.2 The Frequency Controller Registers

MCLON and MCLOFF define the frequency as 19.6608 MHz.

MCLON = 7_{16}

MCLOFF = 7_{16}

3.3.3 The I/O Port Registers

PBMS = Logical OR between PBMS and $A50_{16}$

Bits 4, 6, 9 and 11 should be set to 1. Scanner signals SCLK2, $\overline{SDIS}$, SPDW and $\overline{SLS}$ are defined as outputs from the scanner controller module.

PBEN = 1_{16}

Enable scanner signals as output.

PCMS = Logical OR between PCMS and 4_{16}

Port C module select register bit 2 (SNH port) must be set to 1. Scanner signal SNH is defined as output from the scanner controller module.

PCEN = Logical OR between PCEN and 4_{16}

Enable scanner signal SNH as output.

3.3.4 The DMA Controller Registers

MODE0 = 200_{16}

ADCA is incremented after each transfer cycle, if ADA = 1. Implied 1/0 is destination. ADCA address is updated.

CNTL0 = 1_{16}

Enable DMA channel 0.

MODE2 = 208_{16}

ADCA is incremented after each transfer cycle, if ADA = 1. Implied 1/0 is source. ADCA address updated.

CNTL2 = 1_{16}

Enable DMA channel 2.

MCFG = Logical OR between MCFG and 19_{16}

DMA channel 0 is defined as internal channel.

Scanner Controller (SCANC) module and counters module are both active.

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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