Dynamic Specifications for Sampling A/D Converters

National Semiconductor
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1.0 INTRODUCTION

Traditionally, analog-to-digital converters (ADCs) have been specified by their static characteristics, such as integral and differential nonlinearity, gain error, and offset error. These specifications are important for determining the DC accuracy of an A/D converter, and are very important in applications such as weighing, temperature measurement, and other situations where the input signal varies slowly over time.

Many applications, however, require digitizing a signal which varies quickly over time. These include digital signal processing (DSP) applications, such as digital audio, spectral analysis, and motion control. For these applications, DC accuracy is not as crucial as AC accuracy. The important specifications for these applications are the dynamic specifications, such as signal-to-noise ratio, total harmonic distortion, intermodulation distortion, and input bandwidth. An A/D converter by itself cannot accurately digitize high frequency signals, due to limitations imposed by its conversion time. (If the signal varies by more than ½ LSB during the conversion time of the ADC, the conversion will not be fully accurate.) To digitize a high frequency signal, one must use a sample-and-hold (S/H) amplifier to ''freeze'' the signal long enough so that the ADC can make an accurate conversion. Hence, the dynamic specifications are not unique to the ADC, but are properties of the S/H-ADC system. With the advent of sampling ADCs, which have a S/H built onto the chip with the ADC, it is now possible to meaningfully characterize the dynamic specifications of a single device.

In this application note, we discuss the meaning and significance of the various dynamic specifications for sampling ADCs, and in the appendix we give a table which has typical values for these specifications for a number of sampling ADCs.

2.0 MEANING OF THE DYNAMIC SPECIFICATIONS

Signal-to-Noise Ratio. The signal-to-noise (S/N) ratio is the ratio of the signal amplitude to the noise level. It is generally specified in the data sheets at a set of input signal frequencies, at a specific sampling rate, and with the signal amplitude at or near the maximum allowable level.

There is some ambiguity regarding the composition of the noise component of the S/N ratio. Some manufacturers reserve the term S/N ratio to include only the background noise and the spurious noise, whereas others also include the harmonics of the signal.

When comparing the S/N ratio for several sampling ADCs, one should look in the data sheets to see how it is measured. When the harmonics are included, the S/N specification is frequently referred to as the **Signal-to-(Noise + Distortion)** or **SINAD**. Both signal-to-noise specifications exclude any DC offset from the noise component. To determine the background noise level, one must integrate the noise spectral density over the bandwidth of interest.

Even a perfect ADC will have some noise, which arises from the quantization process. If one treats this quantization noise as white noise and considers no other noise sources, the maximum S/N ratio attainable for an n-bit ADC is [1].

$$S/N = 6.02n + 1.76 \text{ dB}.$$

Hence, one can see that the S/N ratio can be increased by going to the higher resolution ADCs.

Total Harmonic Distortion, or THD, relates the rms sum of the amplitudes of the digitized signal's harmonics to the amplitude of the signal:

$$\text{THD} = \left(\frac{V_{f2}^2 + V_{f3}^2 + \ldots}{V_{f1}^2}\right)^{1/2},$$

where V_{f1} is the amplitude of the fundamental and V_{fi} is the amplitude of the i th harmonic. One generally includes all harmonics within the bandwidth of interest; however, sometimes in practice only the first five harmonics are taken into account, because higher order harmonics have a negligible effect on the THD.

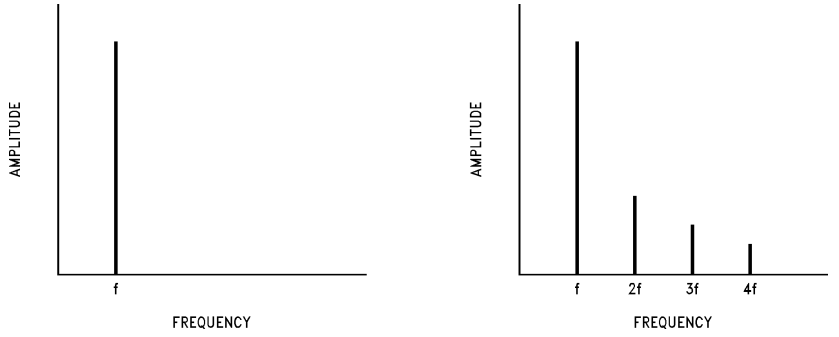

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FIGURE 1. A Signal with a Single Frequency Component (left) Suffers Harmonic Distortion after A/D Conversion (right)

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ADCs produce harmonics of an input signal because an ADC is an inherently nonlinear device. This can be easily seen by looking at the transfer curve of an ideal ADC, which looks like a staircase with equal-sized steps *(Figure 2)* . In a real ADC, ''bowing'' and other nonlinearities add to the distortion. If the output of an ADC is fed to a perfect DAC, then the transfer function of this system can be represented in principle as a polynomial

$$V_{OUT} = a_0 + a_1(V_{IN}) + a_2(V_{IN})^2 + a_3(V_{IN})^3 + \ldots$$

A perfectly linear system would have all the a_j zero except for a_0 and a_1. The second harmonic appears, for example, because a_2 is nonzero. If one uses the trigonometric identity

$$(\cos \omega t)^2 = \frac{1 + \cos 2\omega t}{2},$$

one can see how a second-order nonlinearity produces an output that has a frequency that is twice that of the fundamental.

As one goes to higher resolution converters, the THD will decrease because the transfer curve of the ADC more closely resembles a straight line. (We are assuming that the integral and differential nonlinearities are going down, proportionately, as the resolution increases. This is generally the case.) Like the S/N ratio, the THD is generally specified in the data sheets at a set of frequencies and with the signal amplitude at or near the maximum allowable level. It is usually specified in decibels or as a percentage.

Having a low THD is especially important in applications such as audio and spectral analysis because in these applications, particularly, one does not want the conversion process to add new frequency components to the signal.

Intermodulation Distortion, or IMD, results when two frequency components in a signal interact through the nonlinearities in the ADC to produce signals at additional frequencies. If f_a and f_b are the signal frequencies at the input of the device, the possible IMD products f_{mn} are given by $f_{mn} = m\ f_a \pm n\ f_b$, where *m* and *n* take on positive integer values, and are such that f_{mn} is positive. The *j* th order IMD products are those for which $m + n = j$.

The second order intermodulation products of f_a and f_b, which occur when *m* and *n* both equal 1, are given by the sum and difference frequencies of f_a and f_b.

Using the formula

$$(\cos \omega_1 t + \cos \omega_2 t)^2 = \cos^2\omega_1 t + 2(\cos \omega_1 t)(\cos \omega_2 t) + \cos^2\omega_2 t$$

and the trigonometric identity

$$2(\cos \omega_1 t)(\cos \omega_2 t) = \cos (\omega_1 + \omega_2)t + \cos (\omega_1 - \omega_2)t$$

one can see how a second-order nonlinearity leads to the production of an output that has components at the sum and difference frequencies of the inputs (and also at the second harmonics). The intermodulation distortion due to second order terms is commonly defined as

$$\text{IMD} = \left(\frac{V_{1,1}^2 + V_{1,-1}^2}{V_a^2 + V_b^2}\right)^{1/2},$$

where V_a and V_b are the amplitudes of the fundamentals and $V_{1,1}$ and $V_{1,-1}$ are the amplitudes of the sum and difference frequencies, respectively. *Figure 3* shows a particularly bad case of intermodulation distortion; harmonic distortion products are also visible. In calculating the IMD for this example, one must include the higher order IMD products to get an accurate measure of the distortion.

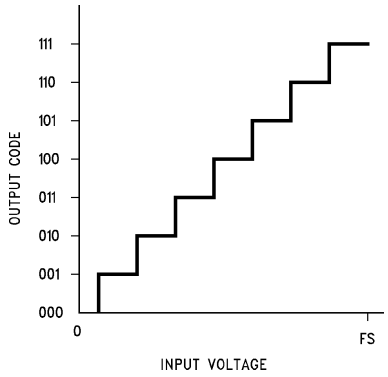

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FIGURE 2. The Nonlinear Nature of the ADC Transfer Curve is the Cause of THD and IMD

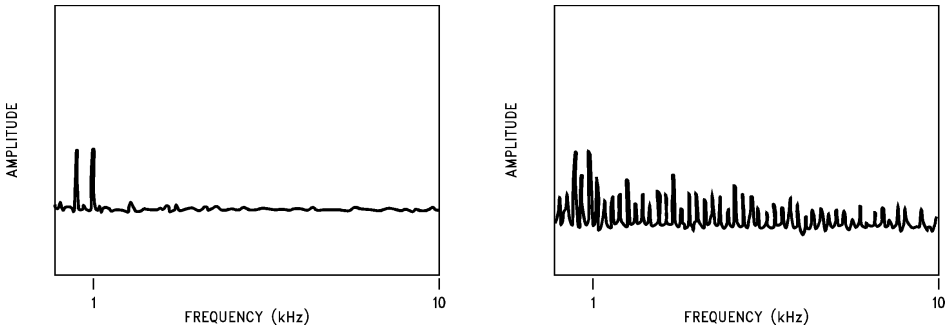

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FIGURE 3. An Input Signal with Frequency Components at 600 Hz and 1 kHz (left) Suffers Severe IMD after A/D Conversion (right)

The way IMD is specified for sampling ADCs varies from manufacturer to manufacturer. Variations occur in the number of IMD products that are included in the measurement, whether the two input frequencies have equal or unequal amplitudes, and whether the distortion is referenced to the rms sum of the input amplitudes or to the amplitude of the larger input. When comparing the IMD for several sampling ADCs, especially if they are from different manufacturers, one must know how it is measured in each case.

As one can infer from *Figure 3*, an ADC with a poor IMD specification would lead to very poor performance in an audio or spectral analysis application. Another reason for wanting a good IMD specification is to prevent the appearance of spurious signals produced by the coupling of strong out-of-band frequency components with signals in the band of interest.

Peak Harmonic is the amplitude, relative to the fundamental, of the largest harmonic resulting from the A/D conversion of a signal. The peak harmonic is usually, but not always, the second harmonic. It is usually specified in decibels.

Peak Harmonic or Spurious Noise is the amplitude, relative to the signal level, of the next largest frequency component (other than DC). Spurious noise components are noise components which are not integral multiples of the input signal, and are often aliased harmonics if the signal frequency is a significant fraction of the sampling rate. This specification is important because some applications require that the harmonics and spurious noise components be smaller than the lowest amplitude signal of interest.

Spurious-Free Dynamic Range is the ratio of the signal amplitude to the amplitude of the highest harmonic or spurious noise component; the input signal amplitude is at or near full scale *(Figure 4)* . This specification is simply the reciprocal of the ''Peak harmonic or spurious noise'' if in the measurement of that specification the input signal amplitude is at full scale.

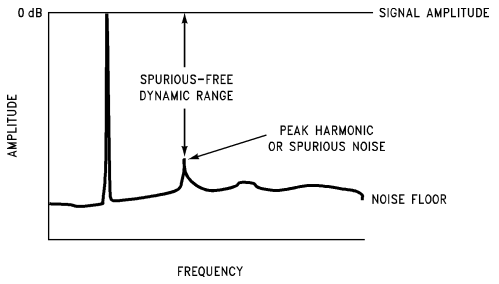

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FIGURE 4. Spurious-Free Dynamic Range Indicates How Far below Full Scale One Can Distinguish Signals from Noise and Distortion

Dynamic Differential Nonlinearity is the differential nonlinearity of the ADC for an AC input. It is frequently measured at the maximum sampling rate and with an input that is at the Nyquist frequency (half the sampling rate). Differential nonlinearity is the deviation from the ideal 1 LSB input voltage span that is associated with each output code *(Figure 5)* . It is measured using the histogram test.

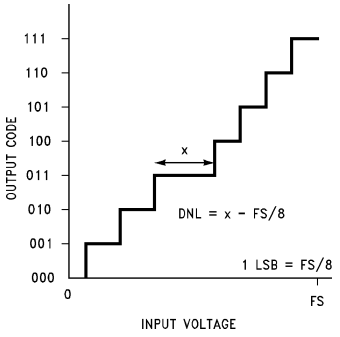

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FIGURE 5. Differential Nonlinearity is a Measure of the Deviation from the Ideal 1 LSB Input Voltage Span Associated with Each Output Code

Dynamic Integral Nonlinearity is the integral nonlinearity of the ADC for an AC input. Like the dynamic differential nonlinearity, it is frequently measured at Nyquist operation. Integral nonlinearity describes the departure of the ADC transfer curve from the ideal transfer curve, excluding the effects of offset, gain and quantization errors *(Figure 6)* .

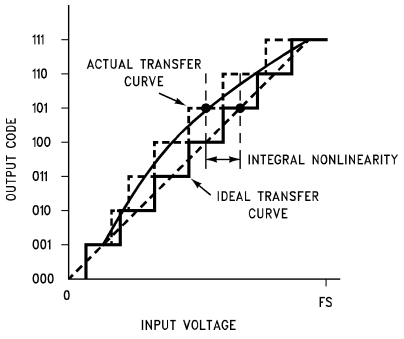

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FIGURE 6. Integral Nonlinearity Measures such Features as "Bowing" in an ADC Transfer Curve

Effective Number of Bits (ENOB) is a specification that is closely related to the signal-to-noise ratio. It is determined by measuring the S/N and using the equation

$$\text{ENOB} = \frac{\text{S/N} - 1.76}{6.02}$$

Some manufacturers define the effective number of bits using the SINAD instead of the signal-to-noise ratio. The ENOB generally decreases at high frequencies, and one frequently sees it plotted as a function of frequency, along with the SINAD *(Figure 7)* . The effective number of bits specification combines the effects of many of the other dynamic specifications. Errors resulting from dynamic differential and integral nonlinearity, missing codes, total harmonic distortion, and aperture jitter show up in the effective number of bits specification.

Full Power Bandwidth has several definitions. A common definition is that it is the frequency at which the S/N ratio has dropped by 3 dB (relative to its low frequency level) for an input signal that is at or near the maximum allowable level. This corresponds to a drop in the ENOB by ½ bit relative to its low-frequency level. Another definition is that it is the frequency at which the input signal appears to have been attenuated by 3 dB. Some manufacturers of flash converters define full power bandwidth as the frequency at which spurious or missing codes begin to appear. (Missing codes will occur if the dynamic differential nonlinearity is greater than +1 LSB.)

Small Signal Bandwidth is the frequency at which the S/N ratio has dropped by 3 dB for an input signal that is much smaller than the full-scale input, 20 dB or 40 dB below full-scale, for example. The small signal bandwidth is generally larger than the full power bandwidth. This will be the case if the bandwidth is slew rate limited, for example. The small signal bandwidth is important for those applications which do not require the conversion of large amplitude, high frequency signals. Relying on the full power bandwidth specification in these cases would constrain one to a smaller bandwidth than can actually be attained.

Sampling Rate, or throughput rate, depends on the length of the conversion time, acquisition time, and other time delays associated with carrying out a conversion. Signals which have frequencies exceeding the Nyquist frequency (half the sampling rate) will be aliased to frequencies below the Nyquist frequency. In order to prevent this signal degradation, one must sample the signal at a rate that is more than twice the highest frequency component in the signal, and/or process the signal through a low pass (anti-aliasing filter) before it reaches the ADC. In some applications one wants to sample at a rate much higher than the highest frequency component of interest in order to reduce the complexity of the anti-aliasing filter that is required.

SAMPLE-AND-HOLD CIRCUITRY SPECIFICATIONS

Aquisition time, aperture time, and aperture jitter are specifications that relate to the internal sampling circuitry within the ADC. These specifications can be easily explained with the aid of the simple sample-and-hold circuit shown in *Figure 8*. The S/H amplifier is in ''Sample'' mode when the switch is closed. In this case, the output of the amplifier is following the input. When the switch is opened, the S/H amplifier is in ''Hold'' mode; in this case, the output retains the input voltage that was present before the switch was opened.

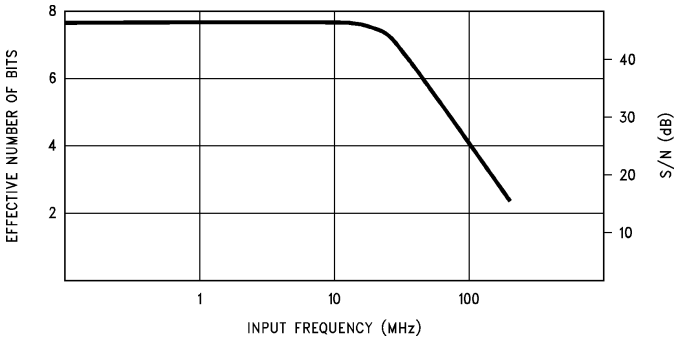

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FIGURE 7. Effective Number of Bits and S/N Generally Drop at High Frequencies

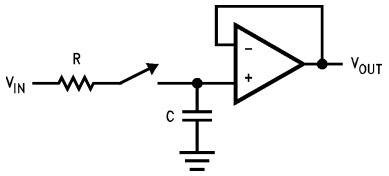

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FIGURE 8. Simple S/H Circuit

Acquisition Time is the maximum time required to acquire a new input voltage once a ''Sample'' command has been given *(Figure 9)* . A signal is ''acquired'' when it has settled to within a specified tolerance, usually ½ LSB, of the input voltage. The maximum value of the acquisition time occurs when the hold capacitor must charge up from zero to its full-scale value (or the other way around, if it is larger). Acquisition time is important because it makes a significant contribution to the total time required to make a conversion.

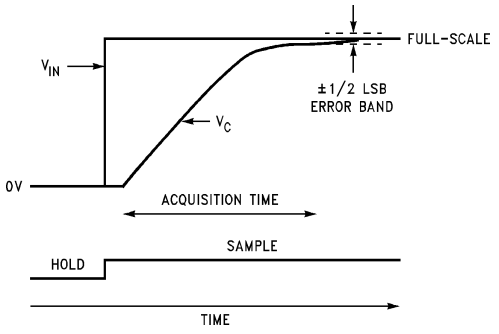

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FIGURE 9. Acquisition Time

Aperture Time is another specification that is defined differently by different manufacturers. The strict definition is that it is the time during which the signal is being disconnected from the hold capacitor after a ''Hold'' command has been given. The broader definition is that it is the time between the application of the ''Hold'' command and when the signal has been completely disconnected from the hold capacitor. The second definition includes the digital delay which occurs between when the ''Hold'' command is applied and when the ''switch'' connecting the input signal to the hold capacitor *begins* to open.

Aperture time is important if one needs to acquire the value of a signal at a precise time. Since the signal is not held instantaneously upon application of the ''Hold'' command, this command must be given roughly an ''aperture time'' before one wants the signal to be ''frozen''.

The aperture time is not a limiting factor on the frequency for sinusoidal signals because for a sinusoidal signal, the voltage error caused by the aperture time manifests itself as a phase change, not an amplitude or frequency change.

Aperture Jitter is the uncertainty in the aperture time. Aperture jitter results from noise which is superimposed on the ''Hold'' command, which affects its timing. Aperture jitter is generally specified as an rms value, which represents the standard deviation in the aperture time.

The aperture jitter sets an upper limit on the maximum frequency sinusoidal signal that can be accurately converted.

In order not to lose accuracy, the rule of thumb is that the signal must not change by more than $\pm$½ LSB during the aperture jitter time. Using a full-scale sinusoidal signal $V = A \sin(2\pi ft)$, we have

$$\frac{dV}{dt} = 2\pi fA \cos(2\pi ft) < \frac{\pm ½\ \text{LSB}}{t_{aj}}$$

where t_{aj} is the aperture jitter. Since ½ LSB = $A/2^n$, where n is the resolution of the converter, we get

$$f < \frac{1}{2\pi \bullet 2^n \bullet t_{aj}}$$

As an example of using Ithis criterion, a 12-bit converter whose S/H amplifier has an aperture jitter of 100 ps could convert full-scale signals having frequencies as high as 388 kHz. Of course, this would only be possible if the converter's sampling rate is at least twice as high as this frequency, in order to satisfy the Nyquist criterion.

3.0 CONCLUSION

It is important to have a working knowledge of the dynamic specifications of sampling ADCs in order to be able to select a converter that is suitable for a specific system need. One must also be aware that the test conditions and even the definitions of the specifications may vary from manufacturer to manufacturer. One must take these variations into account when comparing ADCs. Using the information in this note, one should be able to understand the meanings of the various specifications and determine which ones are important for the particular application at hand.

REFERENCE:

1. B. Blesser, ''Digitization of Audio,'' *J. Audio Eng. Soc.,* vol. 26, no. 10, pp. 742-743 (1978).

APPENDIX

What follows is a table which presents values of the dynamic specifications for a number of National's sampling ADCs. Additional information, such as the values of S/N and THD at frequencies not listed here, can be found in the data sheets. The reference voltage that all of these parts are specified at is +5V, and the supply voltage is +5V for the ADC10461 and ADC10662 and ±5V for the ADC12441 and ADC12451. The only other test conditions included here are the input frequencies and signal amplitudes. Additional test conditions, such as the ambient temperature, can be found in the data sheets. Only the sampling ADCs whose dynamic specifications are tested and guaranteed are included here[1,2]. Additional sampling ADCs made by National are the ADC0820, ADC1061, ADC1241, ADC1251; and the ADC08031, ADC08061, ADC08131, ADC08161, ADC08231, ADC10061, and ADC1031 families.

Dynamic Specifications for Selected Sampling ADCs

Spec	ADC10461 (Note 1)	ADC10662 (Note 2)	ADC12441	ADC12451
Resolution	10	10	12 + sign	12 + sign
Conversion Time	900 ns	466 ns	13.8 μs	7.7 μs
S/N Unipolar (Note 3) Bipolar (Note 4)	58 dB	58 dB	71.5 dB 76.5 dB	68.7 dB 73.5 dB
THD Unipolar (Note 5) Bipolar (Note 6)	−60 dB	−60 dB	−75 dB −75 dB	−73.1 dB −78.0 dB
IMD Unipolar (Note 7) Bipolar (Note 8)			−73 dB −74 dB	−78 dB −78 dB
ENOB Unipolar (Note 9) Bipolar (Note 10)	9	9	11.6 12.4	11.1 11.9
Peak Harmonic Uni. (Note 11) or Spurious Noise Bi. (Note 12)			−82 dB −80 dB	−82 dB −80 dB
Full Power BW			20 kHz	20.67 kHz
Sampling Rate	800 kHz	1.5 MHz	55 kHz	83 kHz
Acquisition Time			3.5 μs	3.5 μs
Aperture Time			100 ns	100 ns
Aperture Jitter			100 ps_{rms}	100 ps_{rms}

Note 1: There are two and four input channel members of the ADC10461 family, namely the ADC10462 and ADC10464. These products have the same dynamic specifications as the ADC10461.

Note 2: The ADC10664 is a 4-input channel member of the ADC10662 family (the ADC10662 has two input channels). These two products have the same dynamic specifications.

Note 3: ADC10461: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC10662: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC12441: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = 4.85 V_{p-p}

Note 4: ADC12441: f_{IN} = 20 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = ±4.85V

Note 5: ADC10461: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC10662: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC12441: f_{IN} = 19.688 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = 4.85 V_{p-p}

Note 6: ADC12441: f_{IN} = 19.688 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = ±4.85V

Note 7: ADC12441: f_{IN1} = 19.375 kHz; f_{IN2} = 20.625 kHz; V_{IN} = 4.85 Vp-p
ADC12451: f_{IN1} = 19.375 kHz; f_{IN2} = 20 kHz; V_{IN} = 4.85 Vp-p

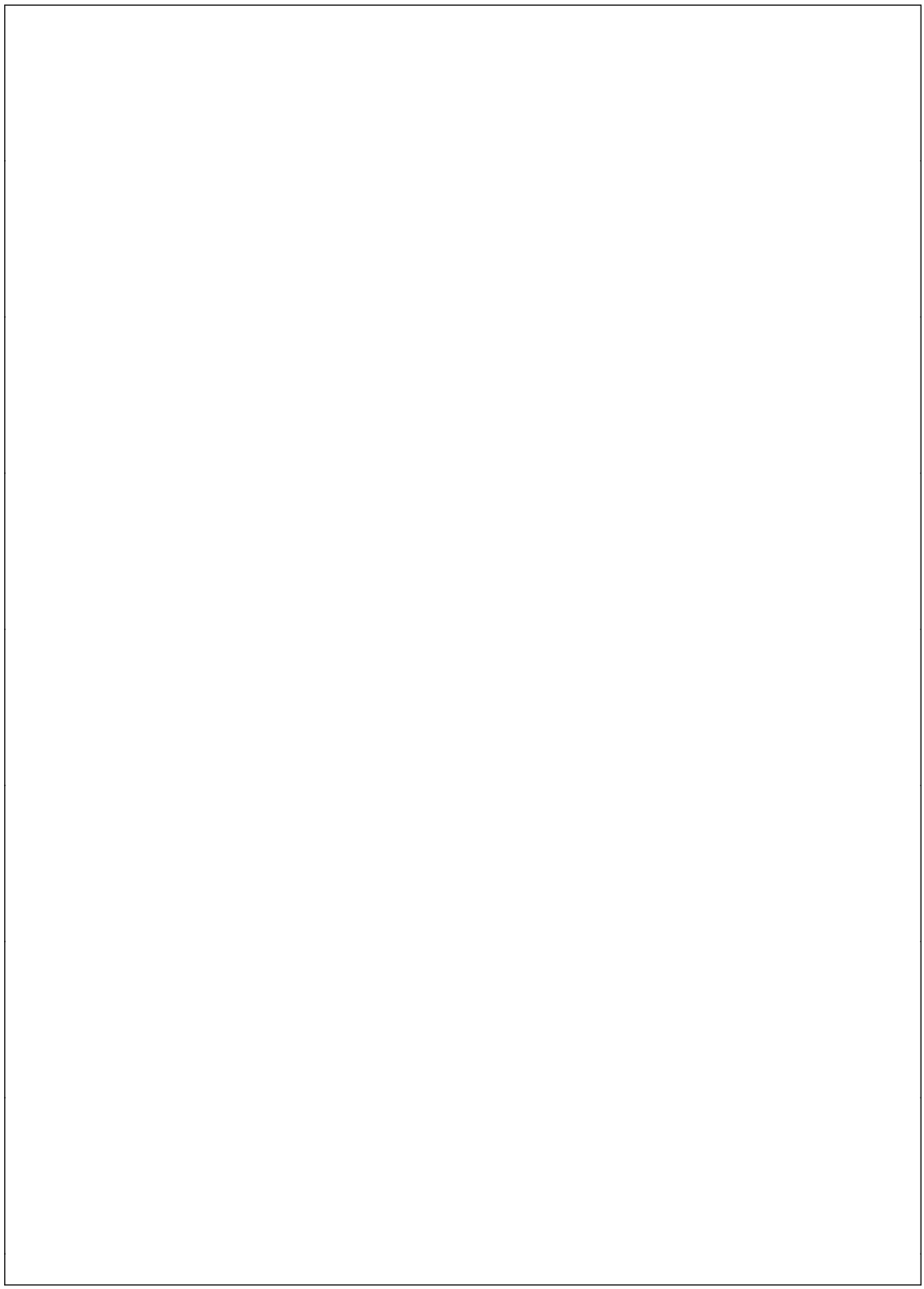
Note 8: ADC12441: f_{IN1} = 19.375 kHz; f_{IN2} = 20.625 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN1} = 19.375 kHz; f_{IN2} = 20 kHz; V_{IN} = ±4.85V

Note 9: ADC10461: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC10662: f_{IN} = 50 kHz; V_{IN} = 4.85 V_{p-p}
ADC12441: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = 4.85 V_{p-p}

Note 10: ADC12441: f_{IN} = 20 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20.67 kHz; V_{IN} = ±4.85V

Note 11: ADC12441: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}
ADC12451: f_{IN} = 20 kHz; V_{IN} = 4.85 V_{p-p}

Note 12: ADC12441: f_{IN} = 20 kHz; V_{IN} = ±4.85V
ADC12451: f_{IN} = 20 kHz; V_{IN} = ±4.85V



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