Introduction to Power MOSFETs and Their Applications

INTRODUCTION

The high voltage power MOSFETs that are available today are N-channel, enhancement-mode, double diffused, Metal-Oxide-Silicon, Field Effect Transistors. They perform the same function as NPN, bipolar junction transistors except the former are voltage controlled in contrast to the current controlled bi-polar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown.

MOSFET OPERATION

An understanding of the operation of MOSFETs can best be gleaned by first considering the later MOSFET shown in *Figure 1*.

With no electrical bias applied to the gate G, no current can flow in either direction underneath the gate because there will always be a blocking PN junction. When the gate is forward biased with respect to the source S, as shown in *Figure 2*, the free hole carriers in the p-epitaxial layer are repelled away from the gate area creating a channel, which allows electrons to flow from the source to the drain. Note that since the holes have been repelled from the gate channel, the electrons are the "majority carriers" by default. This mode of operation is called "enhancement" but it is easier to think of enhancement mode of operation as the device being "normally off", i.e., the switch blocks current until it receives a signal to turn on. The opposite is depletion mode, which is a normally "on" device.
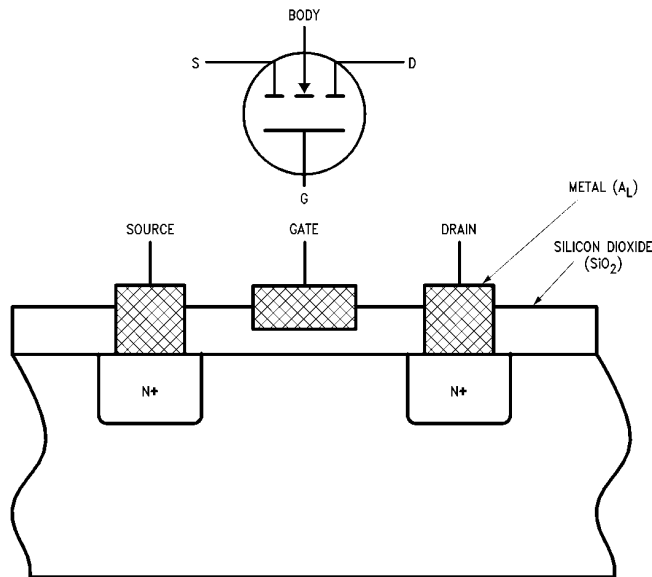

FIGURE 1. Lateral N-Channel MOSFET Cross-Section

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The advantages of the lateral MOSFET are:

1. Low gate signal power requirement. No gate current can flow into the gate after the small gate oxide capacitance has been charged.
2. Fast switching speeds because electrons can start to flow from drain to source as soon as the channel opens. The channel depth is proportional to the gate volage and pinches closed as soon as the gate voltage is removed, so there is no storage time effect as occurs in bipolar transistors.

The major disadvantages are:

1. High resistance channels. In normal operation, the source is electrically connected to the substrate. With no gate bias, the depletion region extends out from the N+ drain in a pseudo-hemispherical shape. The channel length L cannot be made shorter than the minimum depletion width required to support the rated voltage of the device.
2. Channel resistance may be decreased by creating wider channels but this is costly since it uses up valuable silicon real estate. It also slows down the switching speed of the device by increasing its gate capacitance.
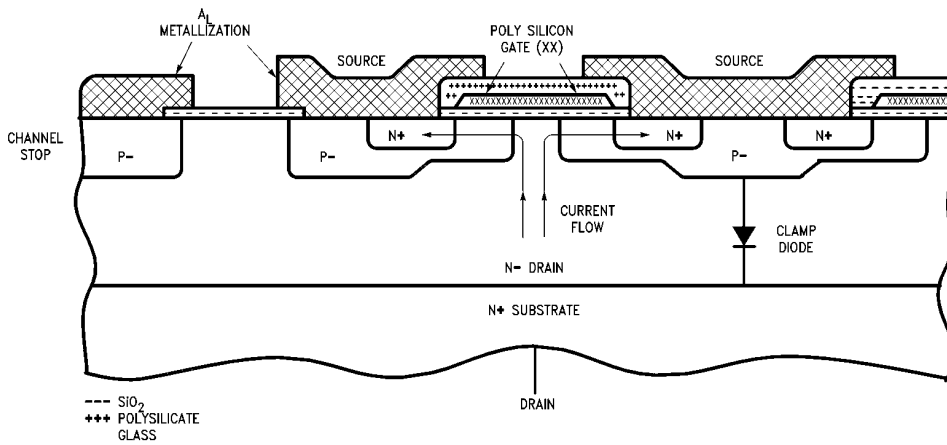
Enter vertical MOSFETs!

The high voltage MOSFET structure (also known as DMOS) is shown in *Figure 3*.
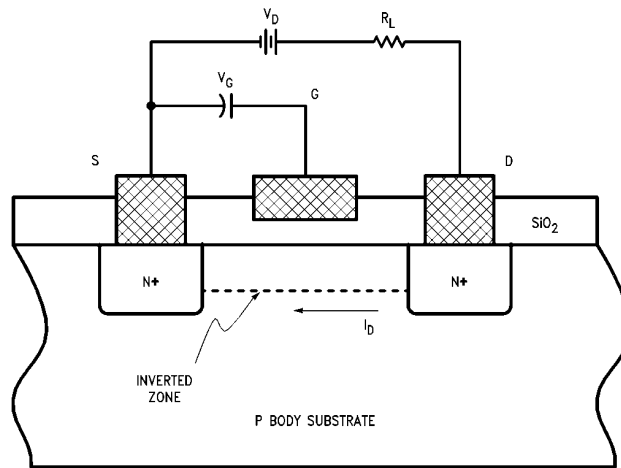
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FIGURE 2. Lateral MOSFET Transistor Biased for Forward Current Conduction

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FIGURE 3. Vertical DMOS Cross-Sectional View

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The current path is created by inverting the p-layer underneath the gate by the identical method in the lateral FETs. Source current flows underneath this gate area and then vertically through the drain, spreading out as it flows down. A typical MOSFET consists of many thousands of N+ sources conducting in parallel. This vertical geometry makes possible lower on-state resistances ($R_{DS(on)}$) for the same blocking voltage and faster switching than the lateral FET.

There are many vertical construction designs possible, e.g., V-groove and U-groove, and many source geometries, e.g., squares, triangles, hexagons, etc. All commercially available power MOSFETs with blocking voltages greater than 300V are manufactured similarly to *Figure 3*. The many considerations that determine the source geometry are $R_{DS(on)}$, input capacitance, switching times and transconductance.
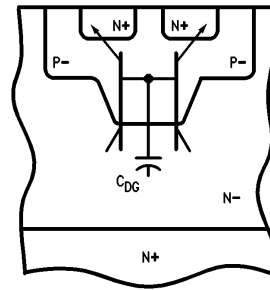
PARASITIC DIODE

Early versions of MOSFETs were very susceptible to voltage breakdown due to voltage transients and also had a tendency to turn on under high rates of rise of drain-to-source voltage (dV/dt), both resulting in catastrophic failures. The dV/dt turn-on was due to the inherent parasitic NPN transistor incorporated within the MOSFET, shown schematically in *Figure 4a*. Current flow needed to charge up junction capacitance C_{DG} acts like base current to turn on the parasitic NPN.

The parasitic NPN action is suppressed by shorting the N+ source to the P+ body using the source metallization. This now creates an inherent PN diode in anti-parallel to the MOSFET transistor (see *Figure 4b*). Because of its extensive junction area, the current ratings and thermal resistance of this diode are the same as the power MOSFET. This parasitic diode does exhibit a very long reverse recovery time and large reverse recovery current due to the long minority carrier lifetimes in the N-drain layer, which precludes the use of this diode except for very low frequency applications, e.g., motor control circuit shown in *Figure 5*. However in high frequency applications, the parasitic diode must be paralleled externally by an ultra-fast rectifier to ensure that the parasitic diode does not turn on. Allowing it to turn on will substantially increase the device power dissipation due to the reverse recovery losses within the diode and also leads to higher voltage transients due to the larger reverse recovery current.

CONTROLLING THE MOSFET

A major advantage of the power MOSFET is its very fast switching speeds. The drain current is strictly proportional to gate voltage so that the theoretically perfect device could switch in 50 ps–200 ps, the time it takes the carriers to flow from source to drain. Since the MOSFET is a majority carrier device, a second reason why it can outperform the bipolar junction transistor is that its turn-off is not delayed by minority carrier storage time in the base. A MOSFET begins to turn off as soon as its gate voltage drops down to its threshold voltage.
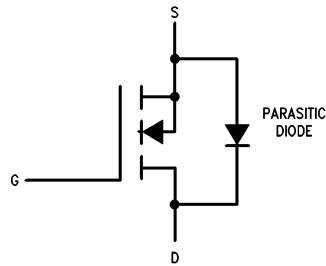

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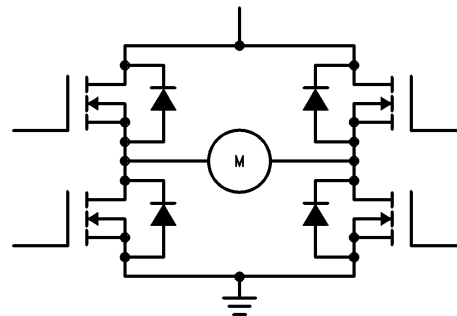**a. MOSFET Transistor Construction Showing Location of the Parasitic NPN Transistor**
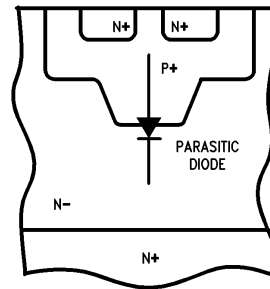
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b. Parastic Diode

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c. Circuit Symbol
FIGURE 4

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FIGURE 5. Full-Wave Motor Control Circuit

SWITCHING BEHAVIOR

Figure 6 illustrates a simplified model for the parasitic capacitances of a power MOSFET and switching voltage waveforms with a resistive load.

There are several different phenomena occurring during turn-on. Referring to the same figure:

Time interval $t_1 < t < t_2$:

The initial turn-on delay time $t_{d(on)}$ is due to the length of time it takes V_{GS} to rise exponentially to the threshold voltage $V_{GS(th)}$. From *Figure 6*, the time constant can be seen to be $R_S \times C_{GS}$. Typical turn-on delay times for the National Semiconductor IRF330 are:

$$t_{d(on)} = R_S \times C_{GS} \times \ln(1 - V_{GS(th)}/V_{PK})$$

For an assumed gate signal generator impedance of R_S of 50Ω and C_{GS} of 600 pF, t_d comes to 11 ns. Note that since the signal source impedance appears in the t_d equation, it is very important to pay attention to the test conditions used in measuring switching times.

Physically one can only measure input capacitance C_{iss}, which consists of C_{GS} in parallel with C_{DG}. Even though $C_{GS} >> C_{DG}$, the latter capacitance undergoes a much larger voltage excursion so its effect on switching time cannot be neglected.

Plots of C_{iss}, C_{rss} and C_{oss} for the National Semiconductor IRF330 are shown in *Figure 7* below. The charging and discharging of C_{DG} is analogous to the "Miller" effect that was first discovered with electron tubes and dominates the next switching interval.

Time interval $t_2 < t < t_3$:

Since V_{GS} has now achieved the threshold value, the MOSFET begins to draw increasing load current and V_{DS} decreases. C_{DG} must not only discharge but its capacitance value also increases since it is inversely proportional to V_{DG}, namely:

$$C_{DG} = C_{DG}(0)/(V_{DG})^n \qquad (2)$$

Unless the gate driver can quickly supply the current required to discharge C_{DG}, voltage fall will be slowed with the attendant increase in turn-on time.

Time interval $t_3 < t < t_4$:

The MOSFET is now on so the gate voltage can rise to the overdrive level.

Turn-off interval $t_4 < t < t_6$:

Turn-off occurs in reverse order. V_{GS} must drop back close to the threshold value before $R_{DS}(on)$ will start to increase. As V_{DS} starts to rise, the Miller effect due to C_{DG} re-occurs and impedes the rise of V_{DS} as C_{DG} recharges to V_{CC}.

Specific gate drive circuits for different applications are discussed and illustrated below.
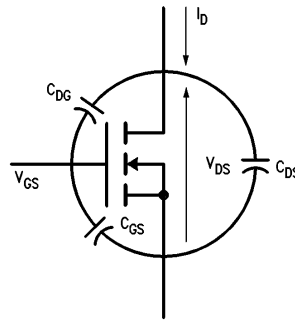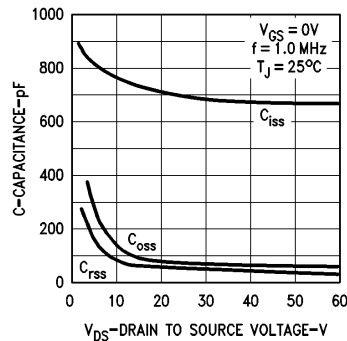

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a. MOSFET Capacitance Model for Power MOSFET
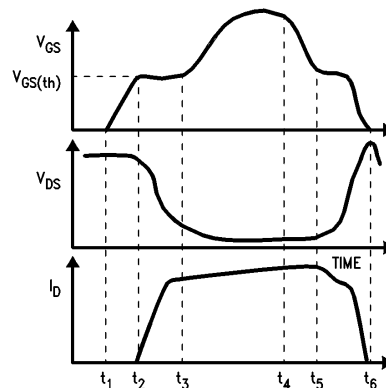
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b. Switching Waveforms for Resistive Load

FIGURE 6

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FIGURE 7. Typical Capacitances of the National IRF330

MOSFET CHARACTERIZATION

The output characteristics (I_D vs V_{DS}) of the National Semiconductor IRF330 are illustrated in *Figures 8* and *9*.

The two distinct regions of operation in *Figure 8* have been labeled "linear" and "saturated". To understand the difference, recall that the actual current path in a MOSFET is horizontal through the channel created under the gate oxide and then vertical through the drain. In the linear region of operation, the voltage across the MOSFET channel is not sufficient for the carriers to reach their maximum drift velocity or their maximum current density. The static $R_{DS(on)}$, defined simply as V_{DS}/I_{DS}, is a constant.

As V_{DS} is increased, the carriers reach their maximum drift velocity and the current amplitude cannot increase. Since the device is behaving like a current generator, it is said to have high output impedance. This is the so-called "saturation" region. One should also note that in comparing MOSFET operation to a bipolar transistor, the linear and saturated regions of the bipolar are just the opposite to the MOSFET. The equal spacing between the output I_D curves for constant steps in V_{GS} indicates that the transfer characteristic in *Figure 9* will be linear in the saturated region.

IMPORTANCE OF THRESHOLD VOLTAGE

Threshold voltage $V_{GS(th)}$ is the minimum gate voltage that initiates drain current flow. $V_{GS(th)}$ can be easily measured on a Tektronix 576 curve tracer by connecting the gate to the drain and recording the required drain voltage for a specified drain current, typically 250 μA or 1 mA. ($V_{GS(th)}$ in *Figure 9* is 3.5V. While a high value of $V_{GS(th)}$, can apparently lengthen turn-on delay time, a low value for power MOSFET is undesirable for the following reasons:

1. $V_{GS(th)}$ has a negative temperature coefficient -7 mV/°C.

2. The high gate impedance of a MOSFET makes it susceptible to spurious turn-on due to gate noise.

3. One of the more common modes of failure is gate-oxide voltage punch-through. Low $V_{GS(th)}$ requires thinner oxides, which lowers the gate oxide voltage rating.
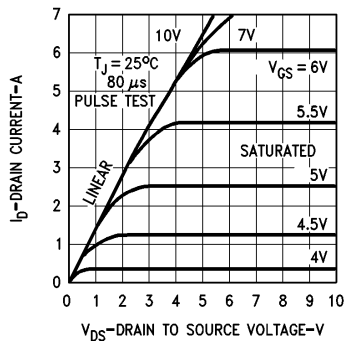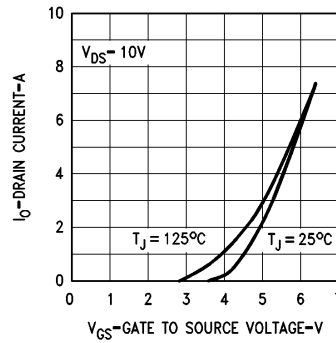

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FIGURE 8. Output Characteristics

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FIGURE 9. Transfer Characteristics

POWER MOSFET THERMAL MODEL

Like all other power semiconductor devices, MOSFETs operate at elevated junction temperatures. It is important to observe their thermal limitations in order to achieve acceptable performance and reliability. Specification sheets contain information on maximum junction temperature ($T_{J(max)}$), safe areas of operation, current ratings and electrical characteristics as a function of T_J where appropriate. However, since it is still not possible to cover all contingencies, it is still important that the designer perform some junction calculations to ensure that the device operate within its specifications.

Figure 10 shows an elementary, stead-state, thermal model for any power semiconductor and the electrical analogue. The heat generated at the junction flows through the silicon pellet to the case or tab and then to the heat sink. The junction temperature rise above the surrounding environment is directly proportional to this heat flow and the junction-to-ambient thermal resistance. The following equation defines the steady state thermal resistance $R_{(th)JC}$ between any two points x and y:

$$R_{(th)JC} = (T_y - T_x)/P \qquad (3)$$

where:

T_x = average temperature at point x (°C)

T_y = average temperature at point y (°C)

P = average heat flow in watts.

Note that for thermal resistance to be meaningful, two temperature reference points must be specified. Units for $R_{(th)JC}$ are °C/W.

The thermal model show symbolically the locations for the reference points of junction temperature, case temperature, sink temperature and ambient temperature. These temperature reference define the following thermal references:

$R_{(th)JC}$: Junction-to-Case thermal resistance.

$R_{(th)CS}$: Case-to-Sink thermal resistance.

$R_{(th)SA}$: Sink-to-Ambient thermal resistance.

Since the thermal resistances are in series:

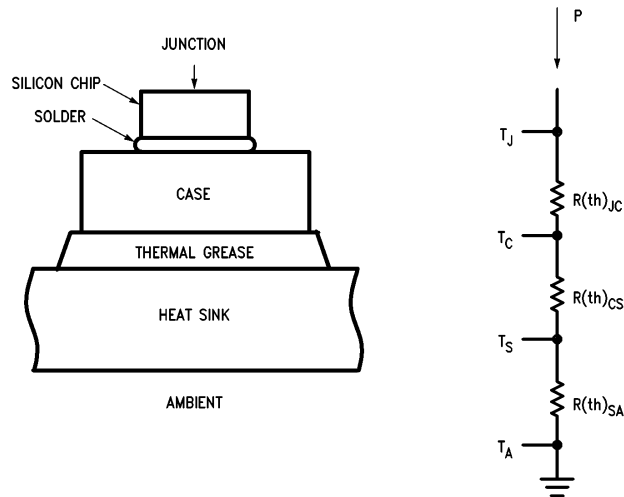$$R_{(th)JA} = R_{(th)JC} + R_{(th)CS} + R_{(th)SA}. \qquad (4)$$

FIGURE 10. MOSFET Steady State Thermal Resistance Model

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The design and manufacture of the device determines $R_{(th)JC}$ so that while $R_{(th)JC}$ will vary somewhat from device to device, it is the sole responsibility of the manufacturer to guarantee a maximum value for $R_{(th)JC}$. Both the user and manufacturer must cooperate in keeping $R_{(th)CS}$ to an acceptable maximum and finally the user has sole responsibility for the external heat sinking.

By inspection of *Figure 10*, one can write an expression for T_J:

$$T_J = T_A + Px\,[R_{(th)JC} + R_{(th)CS} + R_{(th)SA}] \qquad (5)$$

While this appears to be a very simple formula, the major problem in using it is due to the fact that the power dissipated by the MOSFET depends upon T_J. Consequently one must use either an iterative or graphical solution to find the maximum $R_{(th)SA}$ to ensure stability. But an explanation of transient thermal resistance is in order to handle the case of pulsed applications.

Use of steady state thermal resistance is not satisfactory for finding peak junction temperatures for pulsed applications. Plugging in the peak power value results in overestimating the actual junction temperature while using the average power value underestimates the peak junction temperature value at the end of the power pulse. The reason for the discrepancy lies in the thermal capacity of the semiconductor and its housing, i.e., its ability to store heat and to cool down before the next pulse.

The modified thermal model for the MOSFET is shown in *Figure 11*. The normally distributed thermal capacitances have been lumped into single capacitors labeled C_J, C_C,

and C_S. This simplification assumes current is evenly distributed across the silicon chip and that the only significant power losses occur in the junction. When a step pulse of heating power P is introduced at the junction, *Figure 12a* shows that T_J will rise at an exponential rate to some steady state value dependent upon the response of the thermal network. When the power input is terminated at time t_2, T_J will decrease along the curve indicated by T_{cool} in *Figure 12a* back to its initial value. Transient thermal resistance at time t is thus defined as:

$$Z_{(th)JC} = \frac{\Delta T_{JC}(t)}{P} \qquad (6)$$

The transient thermal resistance curve approaches the steady state vaule at long times and the slope of the curve for short times is inversely proportional to C_J. In order that this curve can be used with confidence, it must represent the highest values of $Z_{(th)JC}$ for each time interval that can be expected from the manufacturing distribution of products.

While predicting T_J in response to a series of power pulses becomes very complex, superposition of power pulses offers a rigorous numerical method of using the transient thermal resistance curve to secure a solution. Superposition tests the response of a network to any input function by replacing the input with an equivalent series of superimposed positive and negative step functions. Each step function must start from zero and continue to the time for which T_J is to be computed. For example, *Figure 13* illustrates a typical train of heating pulses.
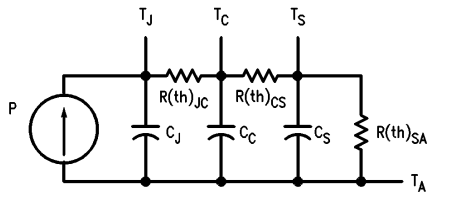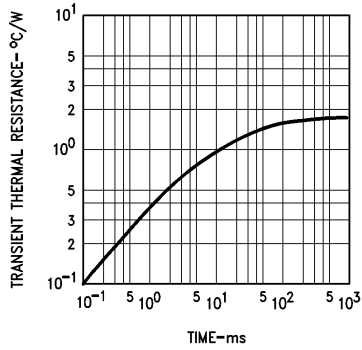
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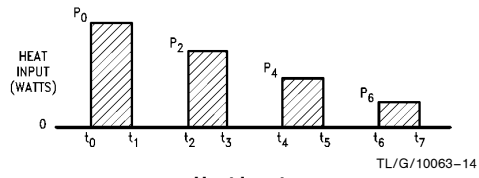**FIGURE 11. Transient Thermal Resistance Model**
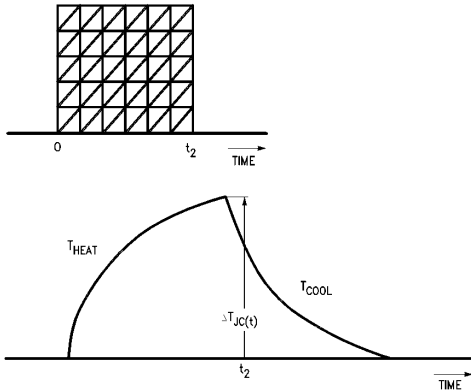
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**a. Junction Temperature Response to a
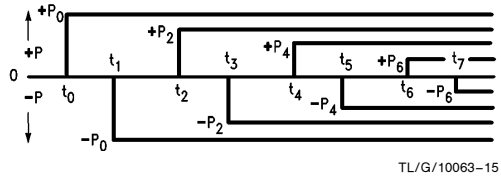Step Pulse of Heating Power**

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**b. Transient Thermal Resistance Curve
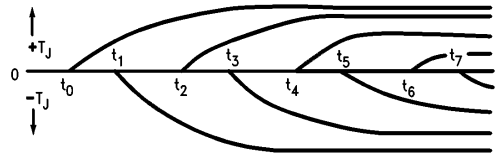for National Semiconductor IRF330 MOSFET**
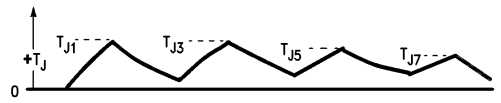
FIGURE 12

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a. Heat Input

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**b. Equivalent Heat Input by
Superposition of Power Pulses**

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**c. Junction Temperature Response
to Individual Power Pulses of b**

TL/G/10063–17

d. Actual T_J

FIGURE 13. Use of Superposition to Determine Peak T_J

T_J at time t is given by:

$$T_J(t) = T_J(0) + \sum_{i=0}^{\eta} Pi \qquad (7)$$

$$[Z_{(th)JC}(t_n - t_i) - Z_{(th)JC}(t_n - t_{i+1})]$$

The usual use condition is to compute the peak junction temperature at thermal equilibrium for a train of equal amplitude power pulses as shown in *Figure 14*.

To further simplify this calculation, the bracketed expression in equation (G) has been plotted for all National Semiconductor power MOSFETs, as exemplified by the plot of $Z_{(th)JC}$ in *Figure 14b*. From this curve, one can readily calculate T_J if one knows P_M, $Z_{(th)JC}$ and T_C using the expression:

$$T_J = T_C + P_M \times Z_{(th)JC} \qquad (8)$$

Example: Compute the maximum junction temperature for a train of 25W, 200 μs wide heating pulses repeated every 2 ms. Assume a case temperature of 95°C.

Duty factor = 0.1

From *Figure 14b:* $Z_{(th)JC} = 0.55°C/W$

Substituting into Equation (H):

$$T_{J(Max)} = 95 + 25 \times 0.55 = 108.75\,°C$$

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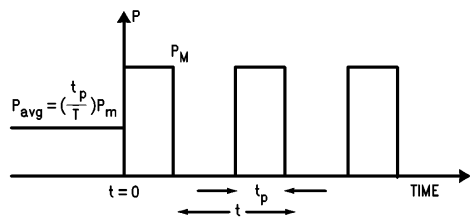
a. Train of Power Pulses

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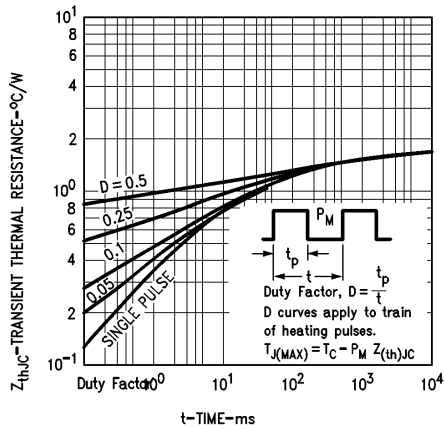
**b. Normalized $Z_{(th)JC}$ for National Semiconductor
IRF330 for Power Pulses Typified in *Figure 14a***

FIGURE 14

SAFE AREA OF OPERATION

The power MOSFET is not subject to forward or reverse bias second breakdown, which can easily occur in bipolar junction transistors. Second breakdown is a potentially catastrophic condition in bi-polar transistors caused by thermal hot spots in the silicon as the transistor turns on or off. However in the MOSFET, the carriers travel through the device much as if it were a bulk semiconductor, which exhibits a positive temperature coefficient of 0.6%/°C. If current attempts to self-constrict to a localized area, the increasing temperature of the spot will raise the spot resistance due to the positive temperature coefficient of the bulk silicon. The ensuing higher voltage drop will tend to redistribute the current away from the hot spot. *Figure 15* delineates the safe areas of operation of the National Semiconductor IRF330 device.

Note that the safe area boundaries are only thermally limited and exhibit no derating for second breakdown. This shows that while the MOSFET transistor is very rugged, it may still be destroyed thermally by forcing it to dissipate too much power.
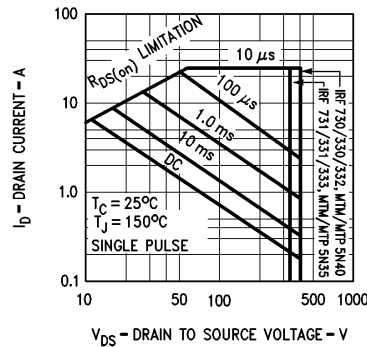

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**FIGURE 15. Safe Area of Operation of the
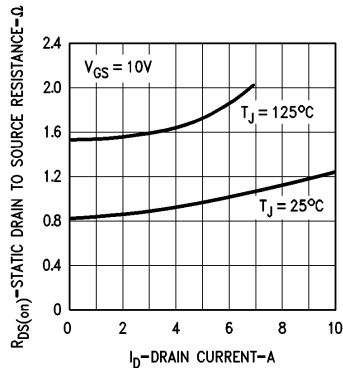National Semiconductor IRF330 MOSFET Transistor**

ON-RESISTANCE $R_{DS(on)}$

The on-resistance of a power MOSFET is a very important parameter because it determines how much current the device can carry for low to medium frequency (less than 200 kHz) applications. After being turned on, the on-state voltage of the MOSFET falls to a low value and its $R_{DS(on)}$ is defined simply as its on-state voltage divided by on-state current. When conducting current as a switch, the conduction losses P_C are:

$$P_C = I^2_{D(RMS)} \times R_{DS(on)} \qquad (9)$$

To minimize $R_{DS(on)}$, the applied gate signal should be large enough to maintain operation in the linear or ohmic region as shown in *Figure 8*. All National Semiconductor MOSFETs will conduct their rated current for $V_{GS} = 10V$, which is also the value used to generate the curves of $R_{DS(on)}$ vs I_D and T_J that are shown in *Figure 16* for the National Semiconductor IRF330. Since $R_{DS(on)}$ increases with T_J, *Figure 16* plots this parameter as a function of current for room ambient and elevated temperatures.

FIGURE 16. $R_{DS(on)}$ of the
National Semiconductor IRF330

Note that as the drain current rises, $R_{DS(on)}$ increases once I_D exceeds the rated current value. Because the MOSFET is a majority carrier device, the component of $R_{DS(on)}$ due to the bulk resistance of the $N-$ silicon in the drain region increases with temperature as well. While this must be taken into account to avoid thermal runaway, it does facilitate parallel operation of MOSFETs. Any inbalance between MOSFETs does not result in current hogging because the device with the most current will heat up and the ensuing higher on-voltage will divert some current to the other devices in parallel.

TRANSCONDUCTANCE

Since MOSFETs are voltage controlled, it has become necessary to resurrect the term transconductance g_{fs}, commonly used in the past with electron tubes. Referring to *Figure 8*, g_{fs} equals the change in drain current divided by the change in gate voltage for a constant drain voltage. Mathematically:

$$g_{fs} \, (\text{Siemens}) = \frac{dI_D(A)}{dV_{GS}(V)} \qquad (10)$$

Transconductance varies with operating conditions, starting at 0 for $V_{GS} < V_{GS(th)}$ and peaking at a finite value when the device is fully saturated. It is very small in the ohmic region because the device cannot conduct any more current. Typically g_{fs} is specified at half the rated current and for $V_{DS} = 20V$. Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies.

GATE DRIVE CIRCUITS FOR POWER MOSFETs

The drive circuit for a power MOSFET will affect its switching behavior and its power dissipation. Consequently the type of drive circuitry depends upon the application. If on-state power losses due to $R_{DS(on)}$, will predominate, there is little point in designing a costly drive circuit. This power dissipation is relatively independent of gate drive as long as the gate-source voltage exceeds the threshold voltage by several volts and an elaborate drive circuit to decrease switching times will only create additional EMI and voltage ringing. In contrast, the drive circuit for a device switching at

200 kHz or more will affect the power dissipation since switching losses are a significant part of the total power dissipation.

Compare to a bi-polar junction transistor, the switching losses in a MOSFET can be made much smaller but these losses must still be taken into consideration. Examples of several typical loads along with the idealized switching waveforms and expressions for power dissipation are given in *Figures 17* to *19*.

Their power losses can be calculated from the general expression:

$$P_D = \left(\frac{1}{\tau} \int_o^\tau I_D(t) \bullet V_{DS}(t)dt \right) \bullet f_s \qquad (11)$$

where: $f_s =$ Switching frequency.

For the idealized waveforms shown in the figures, the integration can be approximated by the calculating areas of triangles:

Resistive load:

$$P_D = \frac{V^2_{DD}}{R} \left[\frac{t_{(on)} + t_{(off)}}{6} + R_{DS(on)} \bullet T \right] \bullet f_s$$

Inductive load:

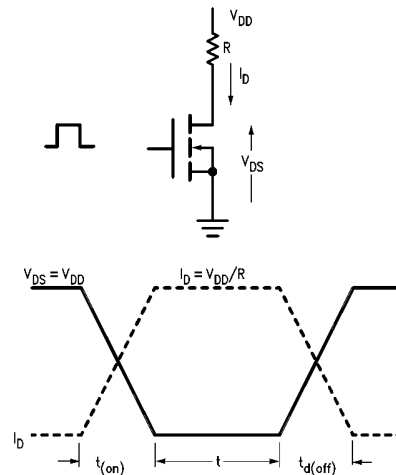$$P_D = \frac{V_{CL} \, I_m \, t_{(off)} f_s}{2} + P_c$$

where:

$P_C =$ conduction loss during period T.

Capacitive load:

$$P_D = \left(\frac{CV^2_{DD}}{2} + \frac{V^2_{DD}R_{DS(on)}}{R^2} T \right) f_s$$

Gate losses and blocking losses can usually be neglected. Using these equations, the circuit designer is able to estimate the required heat sink. A final heat run in a controlled temperature environment is necessary to ensure thermal stability.
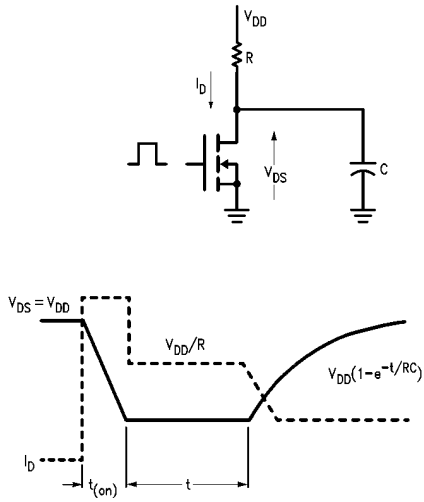

FIGURE 17. Resistive Load Switching Waveforms

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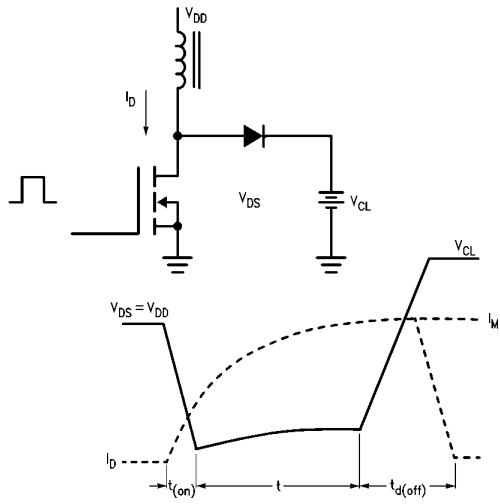
FIGURE 18. Clamped Inductive
Load Switching Waveforms

FIGURE 19. Capacitive Load Switching Waveforms

Since a MOSFET is essentially voltage controlled, the only gate current required is that necessary to charge the input capacitance C_{iss}. In contrast to a 10A bipolar transistor, which may require a base current of 2A to ensure saturation, a power MOSFET can be driven directly by CMOS or open-collector TTL logic circuit similar to that in *Figure 20*.

Turn-on speed depends upon the selection of resistor R_1, whose minimum value will be determined by the current sinking rating of the IC. It is essential that an open collector TTL buffer be used since the voltage applied to the gate must exceed the MOSFET threshold voltage of 5V. CMOS devices can be used to drive the power device directly since they are capable of operating off 15V supplies.

Interface ICs, originally intended for other applications, can also be used to drive power MOSFETs, as shown below in *Figure 21*.

Most frequently switching power supply applications employ a pulse width modulator IC with an NPN transistor output stage. This output transistor is ON when the MOSFET should be ON, hence the type of drive used with open-collector TTL devices cannot be used. *Figures 22* and *23* give examples of typical drive circuits used with PWM ICs.
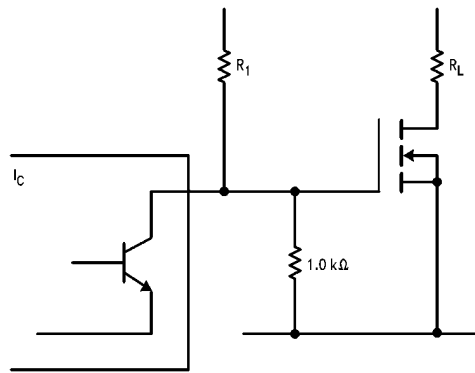
FIGURE 20. Open Collector TTL Drive Circuit

10
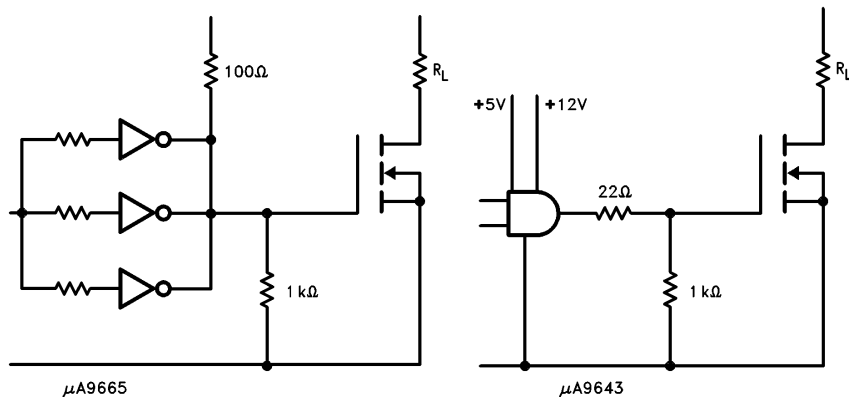
FIGURE 21. Interface ICs Used to
Drive Power MOSFETs

TL/G/10063–27
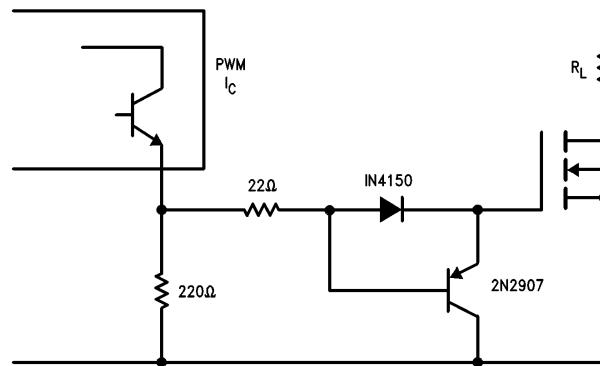
FIGURE 22. Circuit for PWM IC Driving MOSFET.
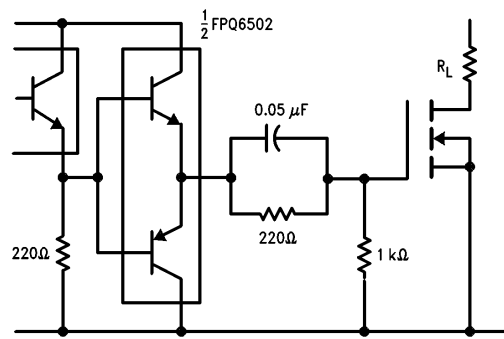The PNP Transistor Speeds Up Turn-Off

TL/G/10063–28

FIGURE 23. Emitter Follower with Speed-Up Capacitor

TL/G/10063–29

Isolation: Off-line switching power supplies use power MOS-FETs in a half-bridge configuration because inexpensive, high voltage devices with low $R_{DS(on)}$ are not available.

Since one of the power devices is connected to the positive rail, its drive circuitry is also floating at a high potential. The most versatile method of coupling the drive circuitry is to use a pulse transformer. Pulse transformers are also normally used to isolate the logic circuitry from the MOSFETs operating at high voltage to protect it from a MOSFET failure.

The zener diode shown in *Figure 25* is included to reset the pulse transformer quickly. The duty cycle can approach 50% with a 12V zener diode. For better performance at turn-off, a PNP transistor can be added as shown in *Figure 26*.

Figure 27 illustrates an alternate method to reverse bias the MOSFET during turn-off by inserting a capacitor in series with the pulse transformer. The capacitor also ensures that the pulse transformer will not saturate due to DC bias.

TL/G/10063–30
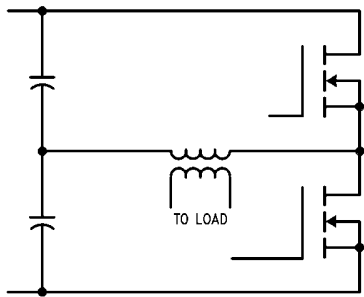
FIGURE 24. Half-Bridge Configuration

TL/G/10063–31
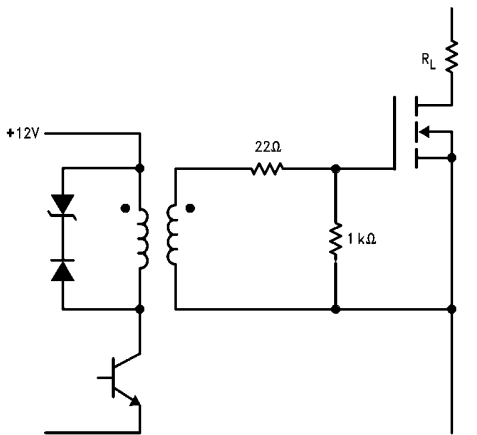
FIGURE 25. Simple Pulse Transformer Drive Circuit. The Transistor May Be a Part of a PWM IC if Applicable.

TL/G/10063–32
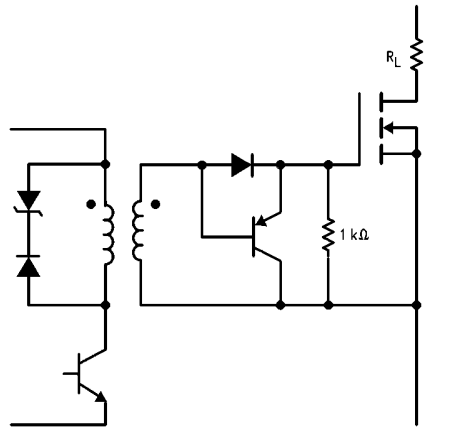
FIGURE 26. Improved Performance at Turn-Off with a Transistor
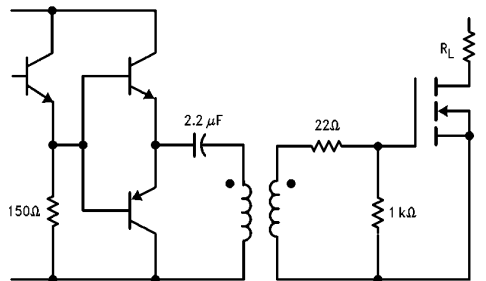

TL/G/10063–33

FIGURE 27. Emitter Follower Driver with Speed-Up Capacitor

Opto-isolators may also be used to drive power MOSFETs but their long switching times make them suitable only for low frequency applications.

SELECTING A DRIVE CIRCUIT

Any of the circuits shown are capable of turning a power MOSFET on and off. The type of circuit depends upon the application. The current sinking and sourcing capabilities of the drive circuit will determine the switching time and switching losses of the power device. As a rule, the higher the gate current at turn-on and turn-off, the lower the switching losses will be. However, fast drive circuits may produce ringing in the gate and drain circuits. At turn-on, ringing in the gate circuit may produce a voltage transient in excess of the maximum V_{GS} rating, which will puncture the gate oxide and destroy it. To prevent this occurrence, a zener diode of the appropriate value may be added to the circuit as shown in *Figure 28*. Note that the zener should be mounted as close as possible to the device.

At turn-off, the gate voltage may ring back up to the threshold voltage and turn on the device for a short period. There is also the possibility that the drain-source voltage will exceed its maximum rated voltage due to ringing in the drain circuit. A protective RC snubber circuit or zener diode may be added to limit drain voltage to a safe level.

Figures 29–34 give typical turn-on and turn-off times of various drive circuits for the following test circuit:
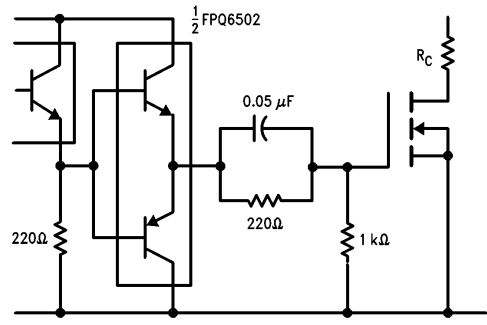
Device: National Semiconductor IRF450, V_{DD} = 200V, Load = 33Ω resistor.

DRIVE CIRCUIT TURN-ON/TURN-OFF TIMES
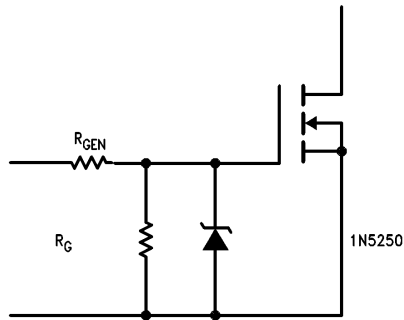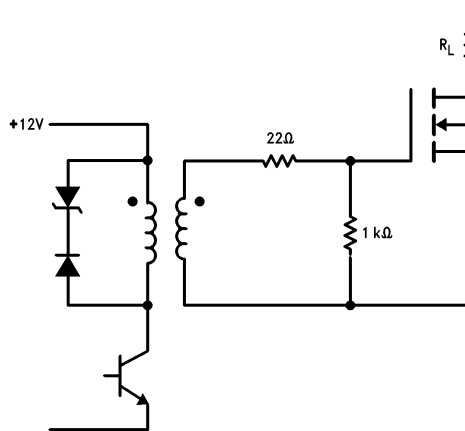

TL/G/10063–34

FIGURE 28. Zener Diode to Prevent Excessive Gate-Source Voltages

TL/G/10063–35

Note: Voltage Fall Time = 17 ns, Voltage Rise Time = 20 ns

FIGURE 29. Emitter Follower PWM
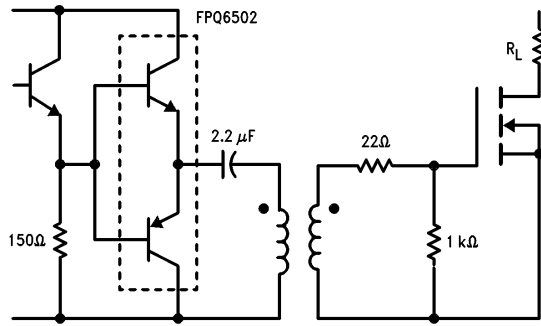

TL/G/10063–36

Note: Voltage Fall Time = 50 ns, Voltage Rise Time = 112 ns

FIGURE 30. Simple Pulse Transformer
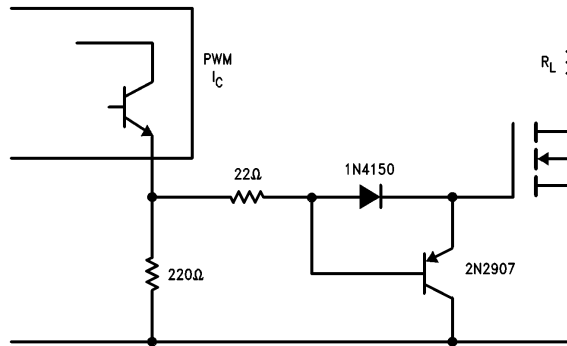
TL/G/10063–37

Note: Voltage Fall Time = 50 ns, Voltage Rise Time = 16 ns

FIGURE 31. Pulse Width Modulator

TL/G/10063–38

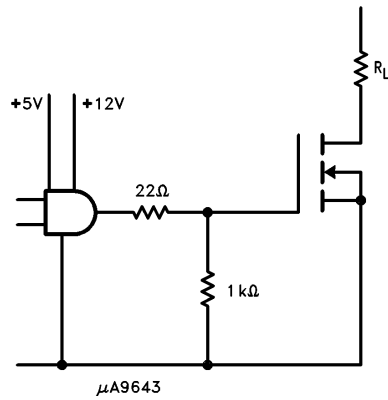**Note:** Voltage Fall Time = 63 ns, Voltage Rise Time = 74 ns

FIGURE 32. Pulse Transformer with Speed-Up Capacitor
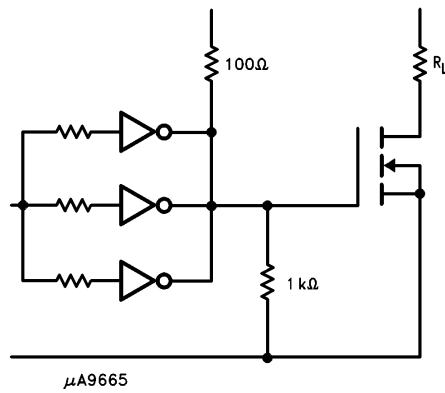
TL/G/10063–39

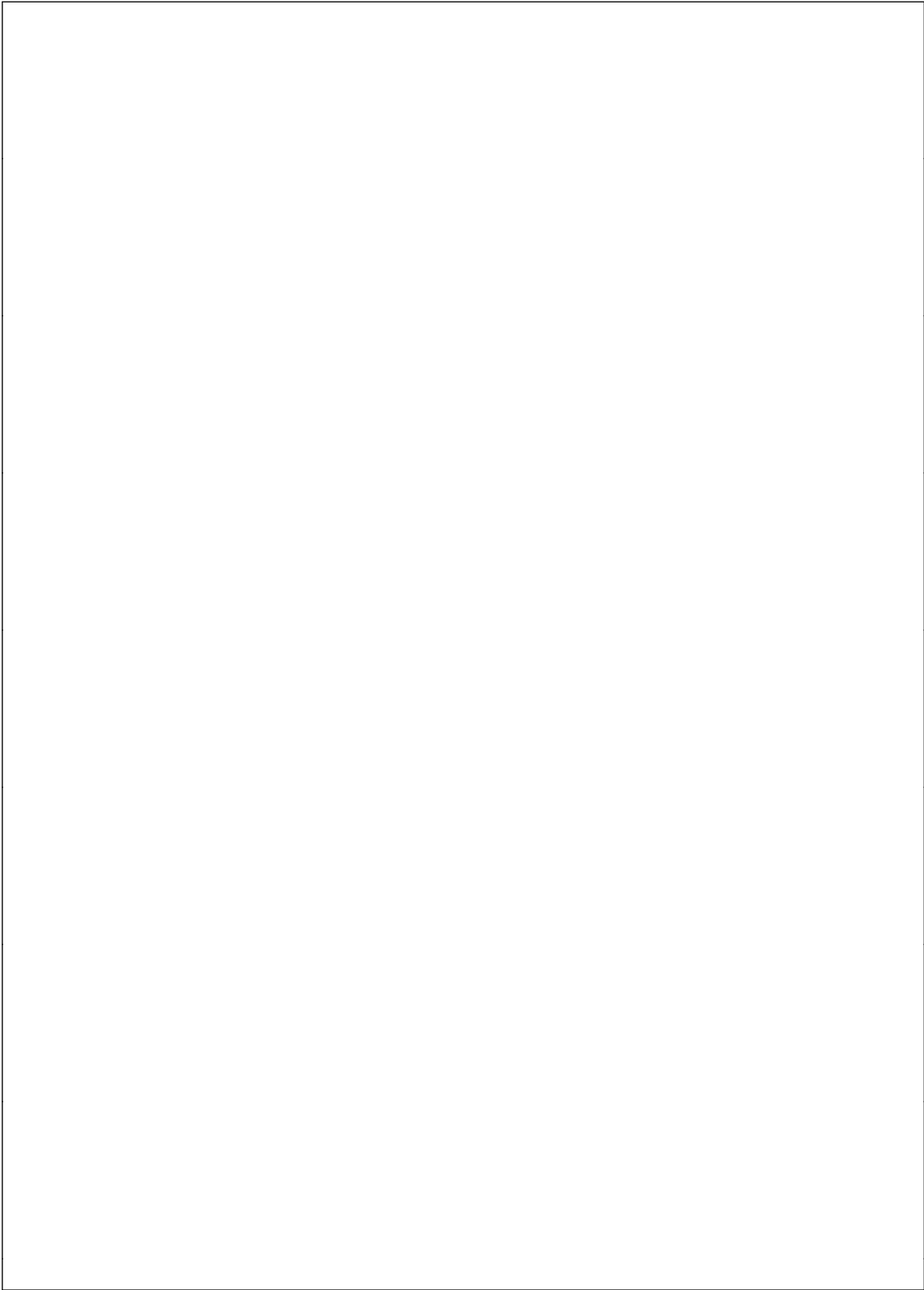**Note:** Voltage Fall Time = 200 ns, Voltage Rise Time = 84 ns

FIGURE 33. Interface Drive

TL/G/10063–40

Note: Voltage Fall Time = 70 ns, Voltage Rise Time = 30 ns

FIGURE 34. Interface Drive

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.