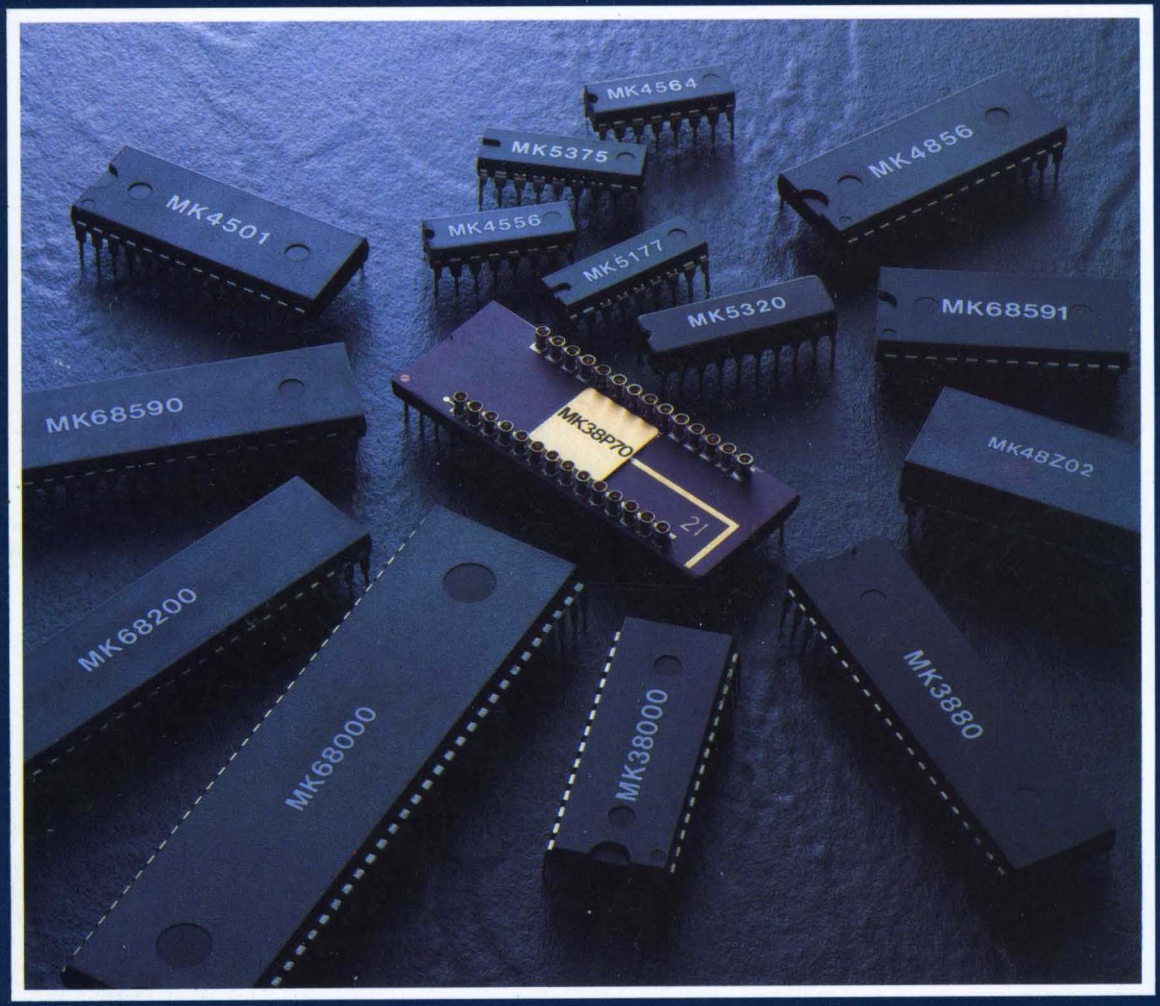
MOSTEK 1984/1985

MICROELECTRONIC DATA BOOK



1984/1985
MICROELECTRONIC
DATA BOOK

PRINTED IN USA July 1984
Publication No. 4420479

1984/1985 MICROELECTRONIC DATA BOOK

1984/1985 MICROELECTRONIC DATA BOOK

TABLE OF CONTENTS

MICROCOMPUTER COMPONENTS

VI. 68000 Family

VII. Z80 Family

VIII. 3870 Single Chip Family

IX. Microcomputer Peripherals

X. Programmed Microcomputer Products

XI. 68000, 68200, Z80 and 3870 Development System Products

TELECOMMUNICATIONS

XII. Integrated Tone Dialers

XIII. Integrated Pulse Dialers with Redial

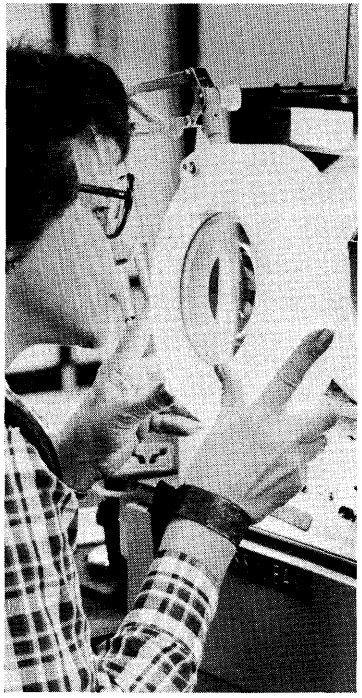
XIV. Repertory Dialers

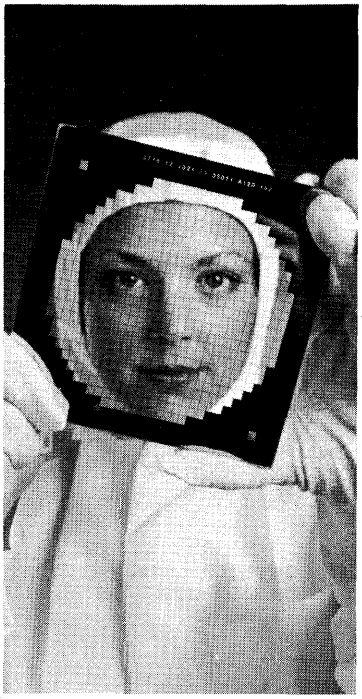
XV. Integrated Tone Decoders

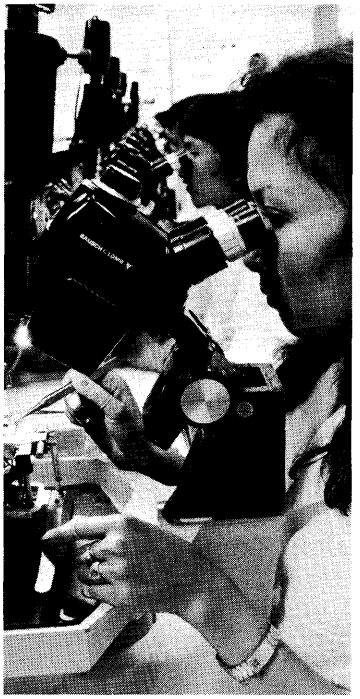
XVI. CODECs & Filters

XVII. Ethernet

1984/1985 MICROELECTRONIC DATA BOOK







Quality products based on efficient, innovative designs.

Today's sophisticated applications require electronic components and subsystems that deliver high performance, high reliability. Mostek dedicates vast resources to research and development to give you exactly what you need: efficient, cost-effective solutions to your specific design needs.

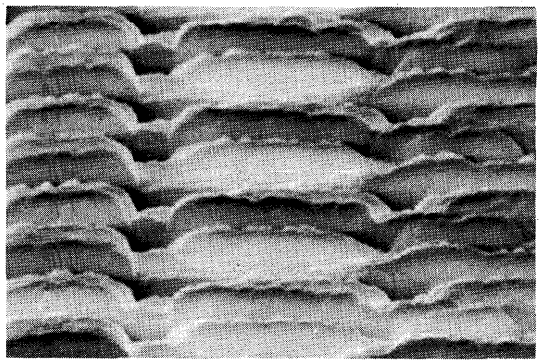
Quality and reliability are built into Mostek products every step of the way, from the initial design stages through manufacturing and testing. And we follow up with extensive product training, sales and customer support. All to achieve Mostek's final objective—outstanding performance in your system.

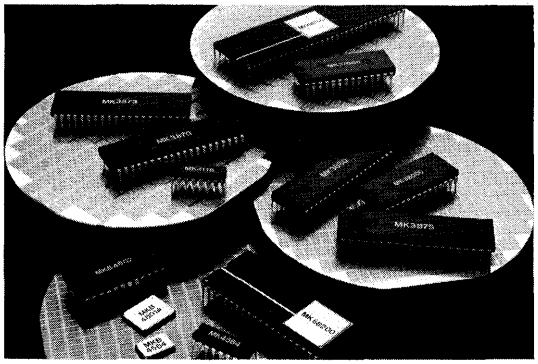
Mostek combines state-of-the-art NMOS and CMOS process technology with smart design to develop high-quality products that are also highly manufacturable. Because of the efficient design of our 64K DRAM, it was possible to increase production from six million units in 1982 to more than 41 million in 1983.

At Mostek, our goal is to provide faster, denser, lower power products—at competitive prices. Through aggressive research and development, innovative design and commitment to quality, Mostek is ready to anticipate and meet your needs now, and in the future.

MEMORIES

Mostek is an industry leader in the design and manufacture of dynamic RAMs, including the MK45H64, the world's fastest DRAM, and the MK4856, the first 32K×8 256K DRAM. To meet the precise manufacturing requirements of the 256K DRAM, Mostek has more direct-step-on-wafer (DSW) machines on-line than any other manufacturer in the world. And more experience with those machines as well. Other Mostek memory product innovations include the first true non-volatile RAM and the BiPORT™ series of interconnect devices.





MEMORY SYSTEMS

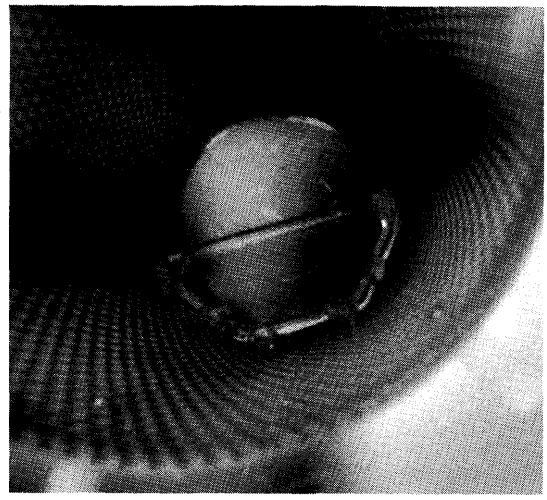
The performance and reliability of Mostek industry-standard circuits is built into all of our memory systems products. For example, the MK8200 general-purpose mass memory system delivers the fastest throughput and highest density currently available anywhere.

SEMICUSTOM CIRCUITS

Mostek now offers the designer a way to reduce part count and increase system reliability and performance: a full family of 2- and 3-micron gate arrays. Mostek semicustom circuits let you design your circuits to your specific applications. And our captive photomask facility and large-scale wafer production and assembly facilities make Mostek a turn-key vendor, unlike other semicustom suppliers.

MILITARY

Mostek delivers the latest state-of-the-art microelectronics in military versions.



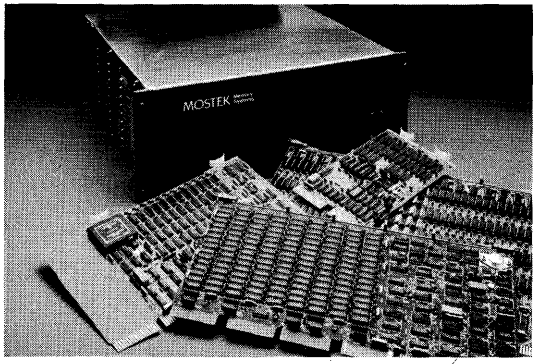
Many of our products are qualified to meet stringent military requirements, including the new MKB4501 BiPORT FIFO memory chip, screened to MIL-STD-883, Class B. And the MKB45H64, the world's fastest DRAM, is also now available to the armed forces through Mostek.

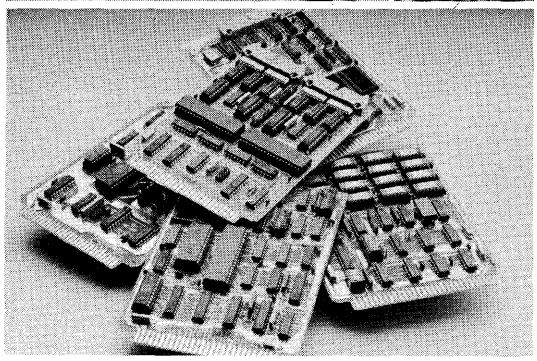
MICROCOMPONENTS

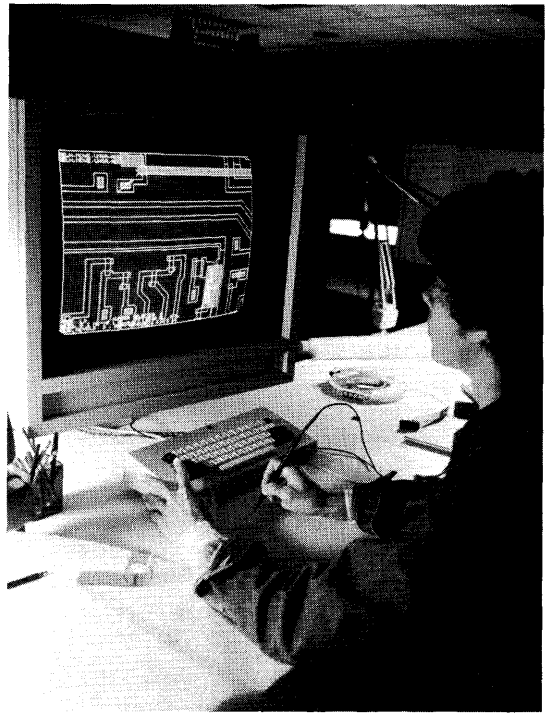
At Mostek, we're dedicated to improving the power and versatility of our MK68200 16-bit single-chip microcomputer and MK68000 microprocessor families. For example, our high-performance MK68200 microcomputer has the speed and power ideal for robotics and other complex tasks. And our MK68000 family of microprocessors and peripherals lets you quickly develop even the most sophisticated I/O-intensive applications.

MICROCOMPONENT SUPPORT

Mostek manufactures a complete line of emulation tools. With four different cards, Mostek supports its four different microprocessor families, including the new MK68200 microcomputer. By using any of our four Mostek AIM™ modules with either the Mostek RADIUS™ remote development station or the Mostek MATRIX™ stand-alone development system, you get complete hardware/software development and debug capabilities at competitive prices.







MICROCOMPUTER SYSTEMS

Mostek offers a full line of 8-bit STD-Z80 BUS microcomputer boards and systems. For 16-bit applications, Mostek VMEbus systems deliver high performance and expandability. And our new VME MATRIX 68K™ is a multi-user, 16-bit development system featuring the UniPlus+™ UNIX™ System III operating system.

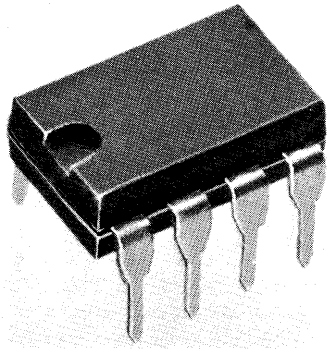
COMMUNICATIONS

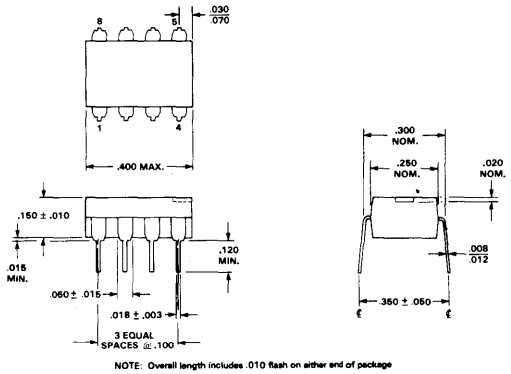
Mostek is the world's largest independent supplier of large-scale integrated circuits for telecommunications applications. Mostek participates in three major market segments—analog applications, digital applications (such as PBXs), and computer information networks. To meet the growing needs of the communications industry, our product line has been expanded recently to include single and repertory integrated dialer circuits capable of both tone and pulse dialing.

SOFTWARE

Mostek provides powerful software development packages for 8- and 16-bit systems. For 8-bit microprocessors, Mostek offers the CP/M™ V3.0 industry-standard operating system. To meet the needs of rapildly growing 16-bit applications, Mostek offers the versatile VME MATRIX 68K, a multi-user development system which employs the UniPlus™ UNIX operating system. UniPlus+ is derived from the UNIX System III.

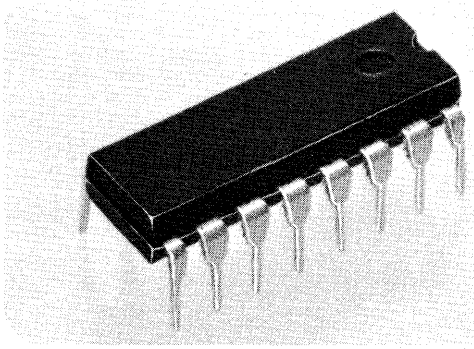
Plastic Dual-In-Line Package (N)
8 Pin

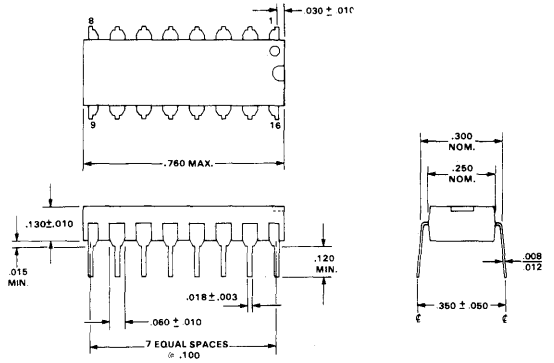




NOTE: Overall length includes .010 flash on either end of package

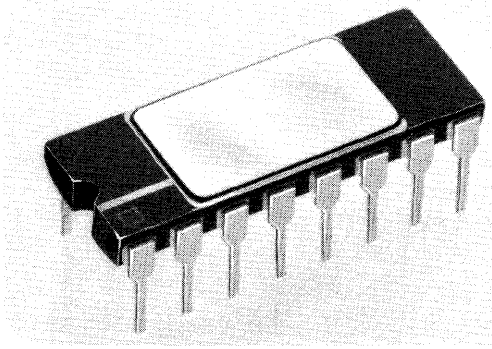
Plastic Dual-In-Line Package (N)
16 Pin

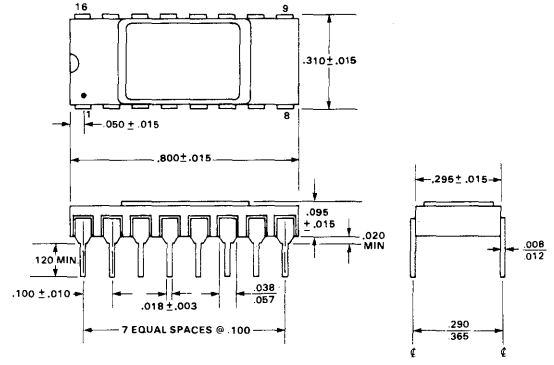




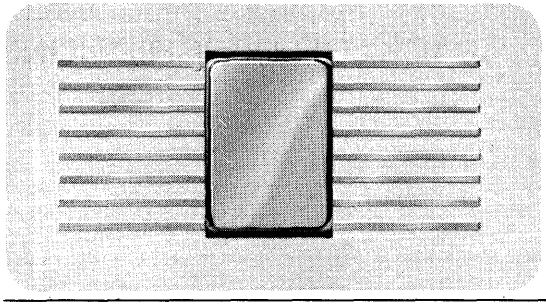
NOTE: Overall length includes .010 flash on either end of package

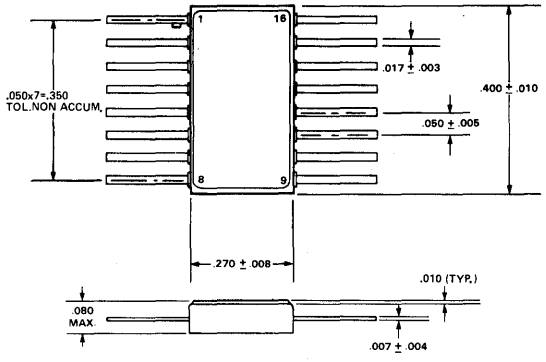
Ceramic Dual-In-Line Package (P)
16 Pin



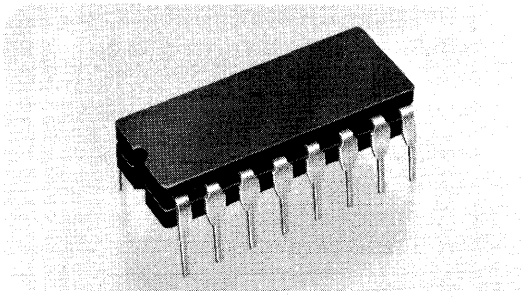


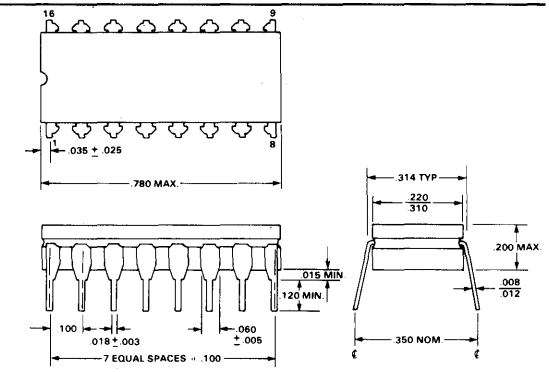
Ceramic Flat Package (F)
16 Pin



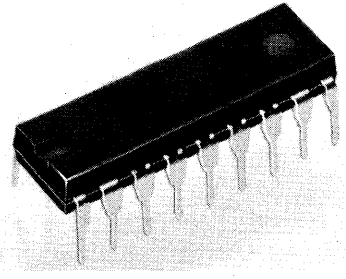


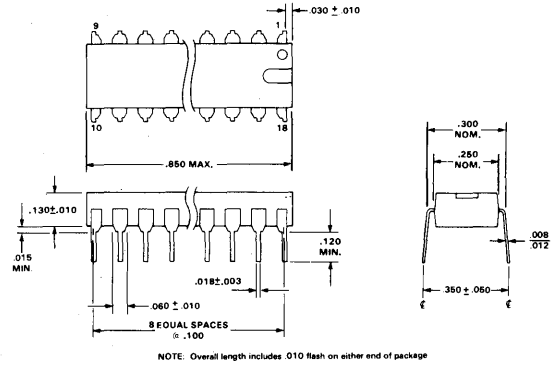
Cerdip Hermetic Package (J)
16 Pin





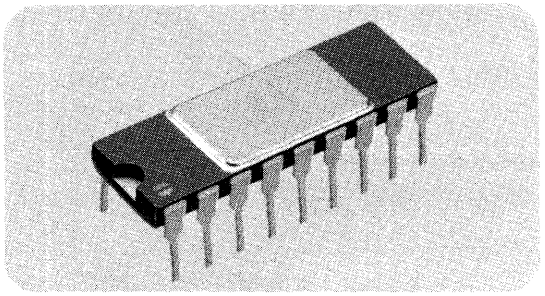
Plastic Dual-In-Line Package (N)
18 Pin

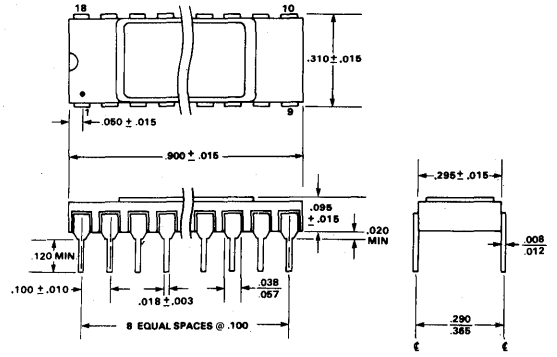




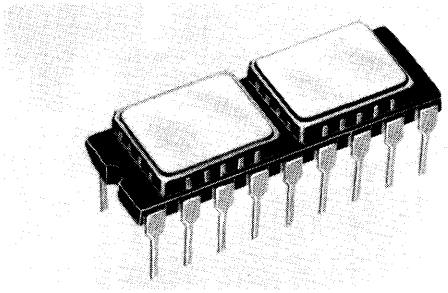
NOTE: Overall length includes .010 flash on either end of package

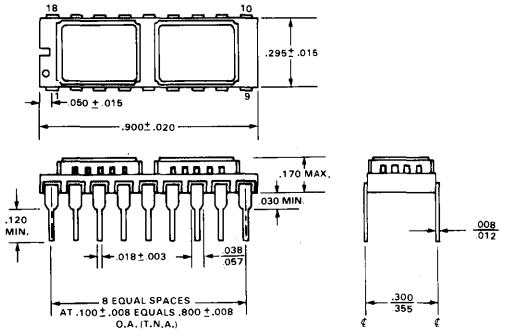
Ceramic Dual-In-Line Package (P)
18 Pin



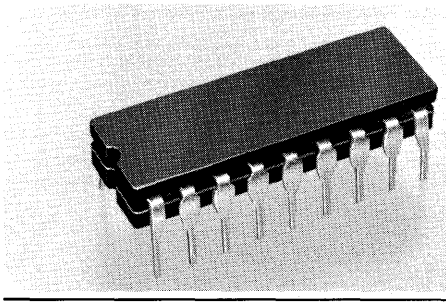


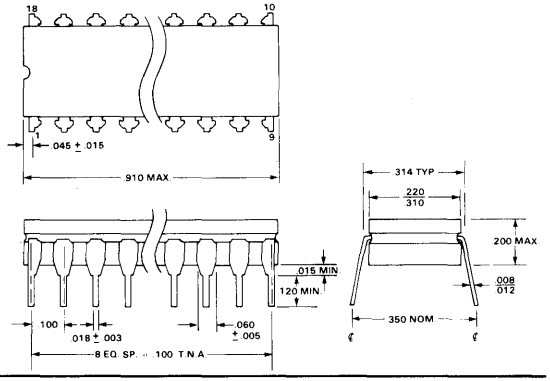
Dual-In-Line Double Density Ceramic Package (D)
18 Pin



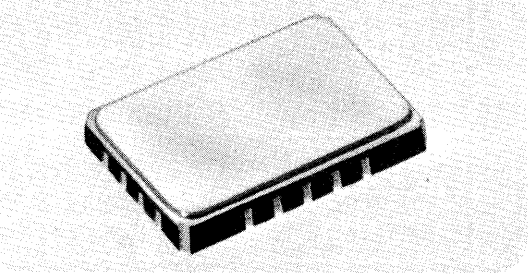


Cerdip Hermetic Package (J)
18 Pin





Leadless Hermetic Chip Carrier (E)
18 Pin (Proposed JEDEC Type F)



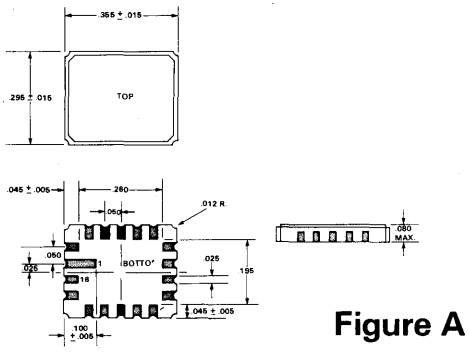
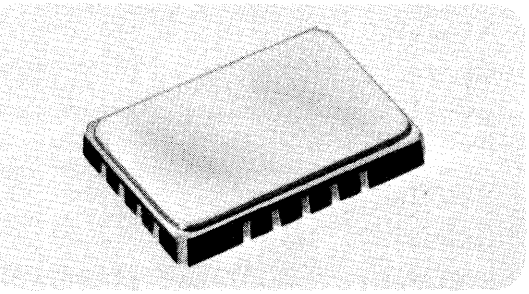


Figure A

Leadless Hermetic Chip Carrier (E)
18 Pin (Proposed JEDEC Type F)



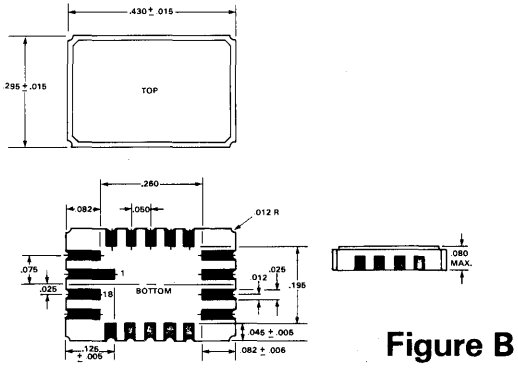
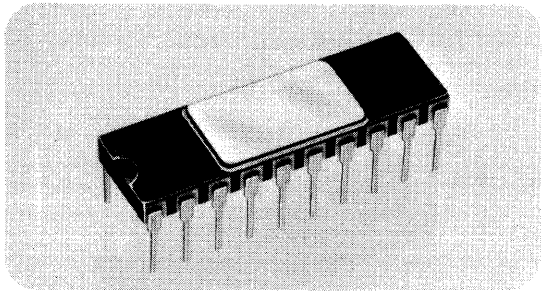
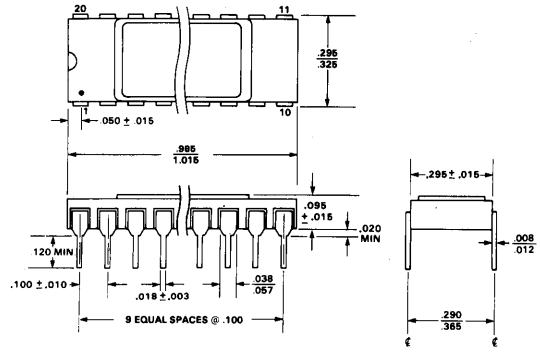


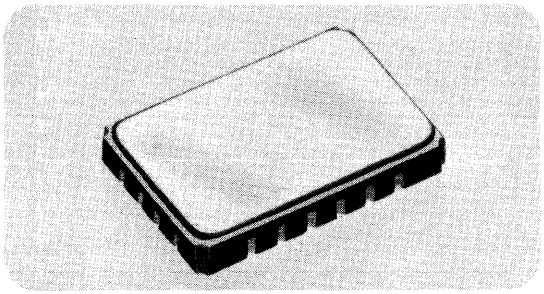
Figure B

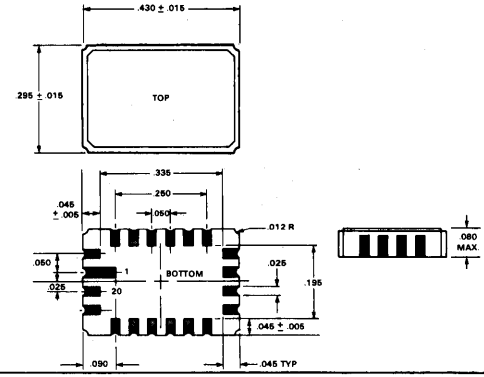
Ceramic Dual-In-Line Package (P)
20 Pin



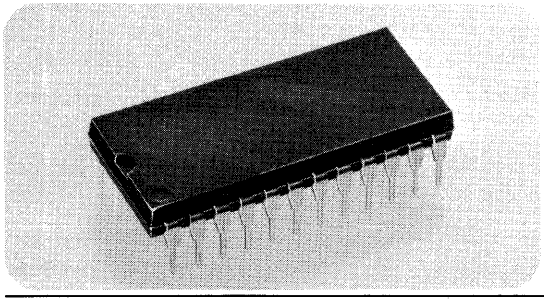


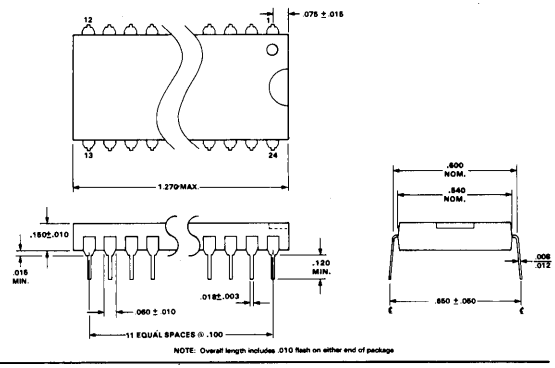
Leadless Hermetic Chip Carrier (E)
20 Pin



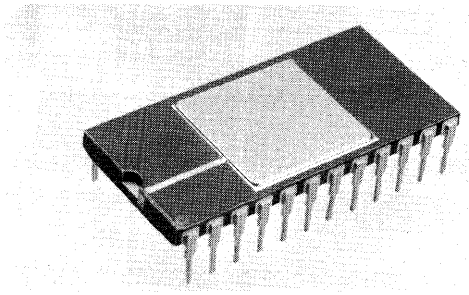


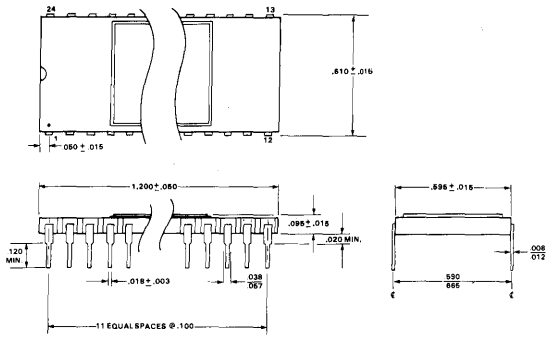
Plastic Dual-In-Line Package (N)
24 Pin





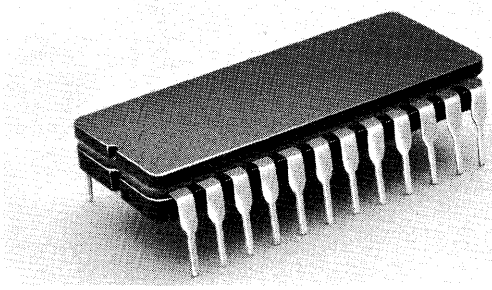
Ceramic Dual-In-Line Package (P)
24 Pin

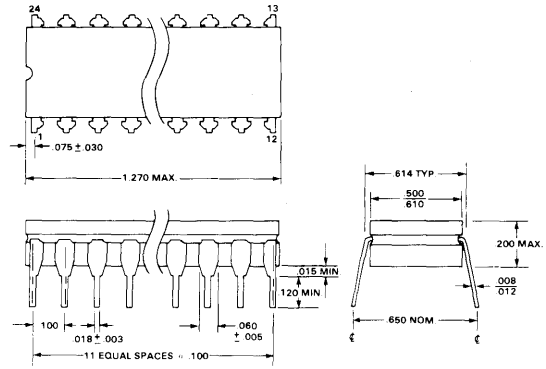




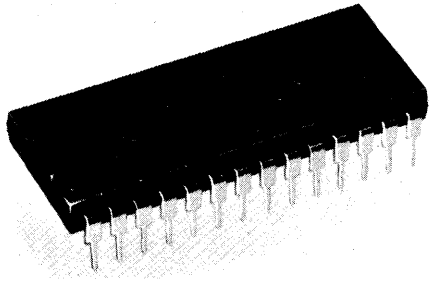
II

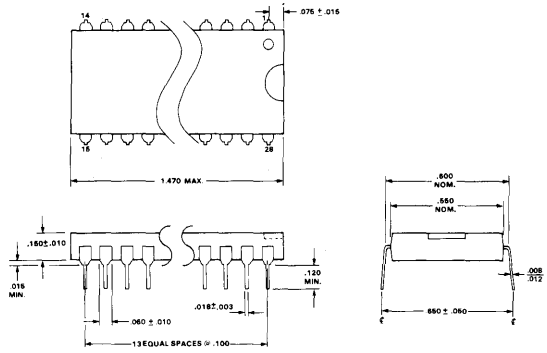
Cerdip Hermetic Package (J)
24 Pin





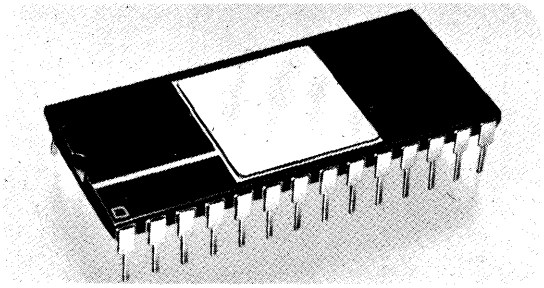
Plastic Dual-In-Line Package (N)
28 Pin

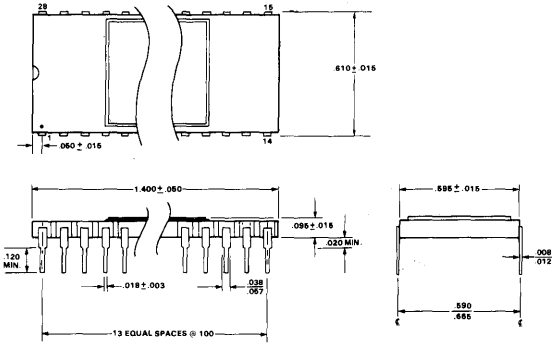




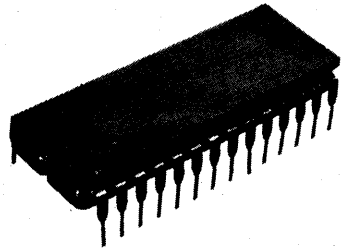
NOTE: Overall length includes .010 flash on either end of package

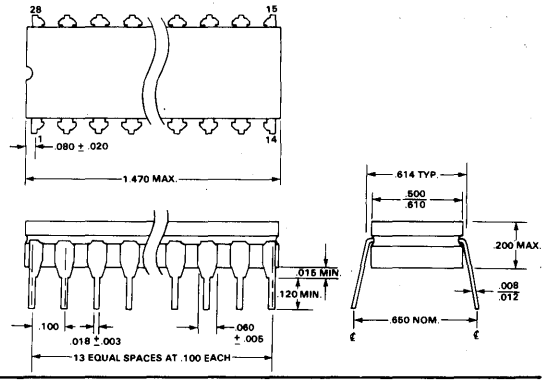
Ceramic Dual-In-Line Package (P)
28 Pin



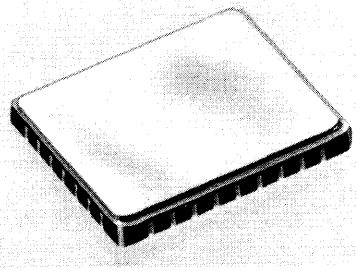


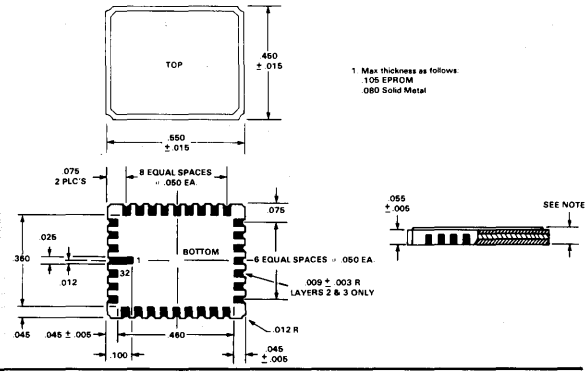
Cerdip Hermetic Package (J)
28 Pin



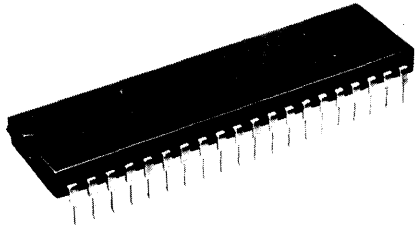


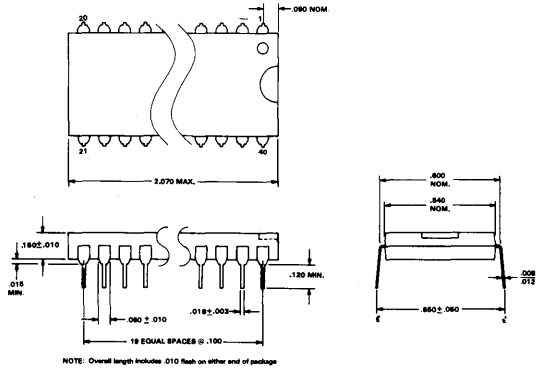
Leadless Hermetic Chip Carrier (E)
32 Pin (Proposed JEDEC Type E)



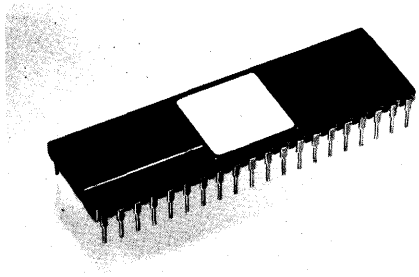


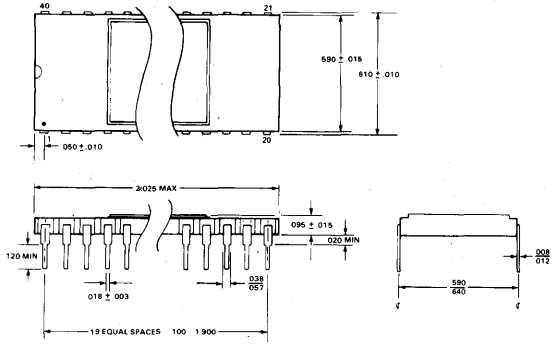
Plastic Dual-In-Line Package (N)
40 Pin



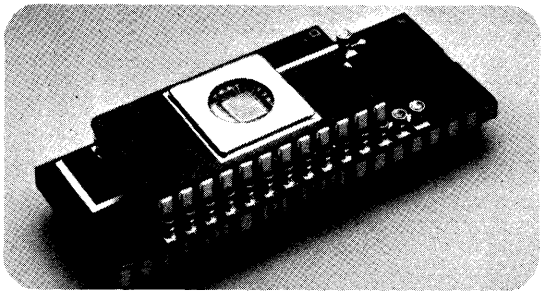


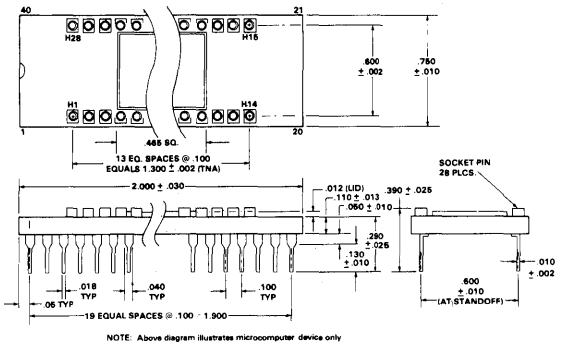
Ceramic Dual-In-Line Package (P)
40 Pin





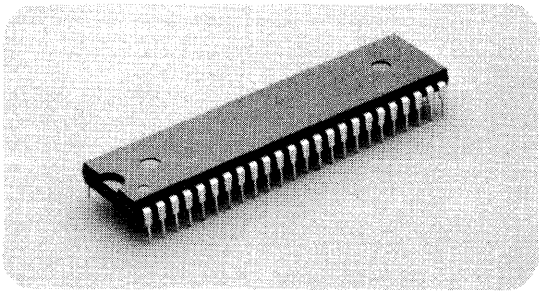
P-PROM Package (R)
40 Pin

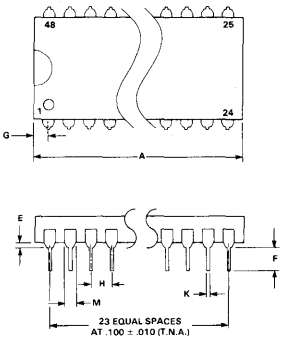




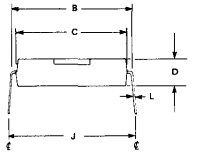
NOTE: Above diagram illustrates microcomputer device only

Plastic Dual-In-Line Plastic (N)
48 Pin

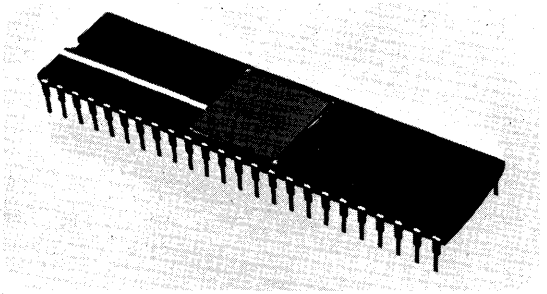


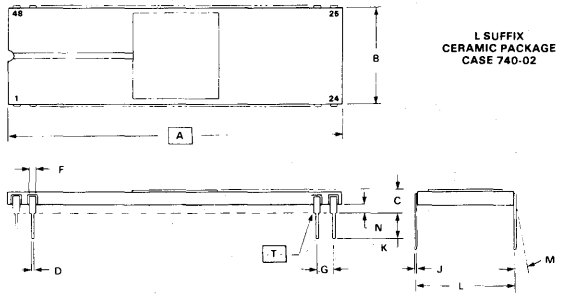


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	61.468	62.738	2.420	2.470
B	14.986	16.256	.590	.640
C	13.462	13.97	.530	.550
D	3.556	4064	.140	.160
E	0.381	1.524	.015	060
F	3048	3.81	.120	.150
G	1.524	2.286	.060	.090
H	1.186	1.794	.090	.110
J	15.24	17.78	.600	.700
K	0.381	0.533	.015	.021
L	0.203	0.305	.008	.012
M	1.143	1.778	.045	.070



Ceramic Dual-In-Line Package (P)
48 Pin



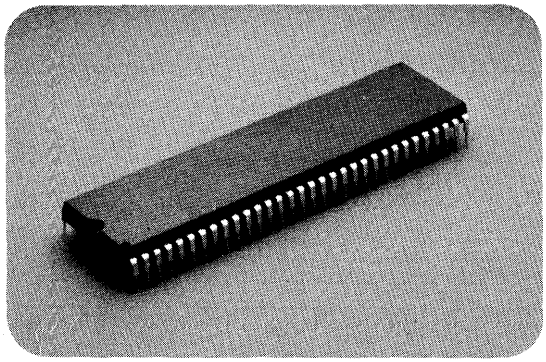


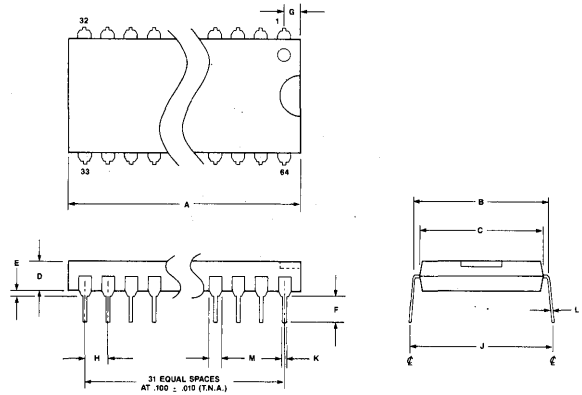
L SUFFIX
CERAMIC PACKAGE
CASE 740-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   Ø 0.25 (0.010) T AM
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

Plastic Dual-In-Line Plastic (N)
64 Pin



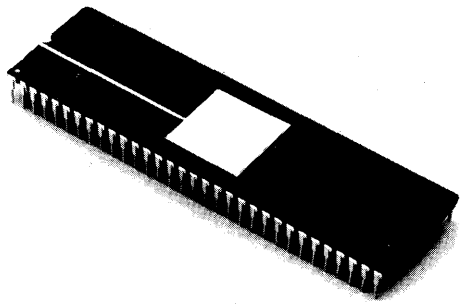


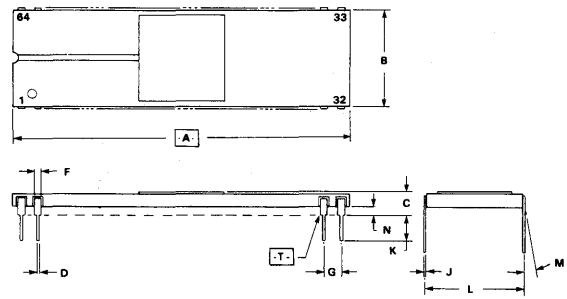
DIM.	INCHES		NOTES
	MIN.	MAX.	
A	3.180	3.230	2
B	.890	.940	
C	.790	.810	
D	.170	.190	
E	.020	.060	3
F	.120	.150	
G	.040	.070	
H	.090	.110	
J	.900	1.000	4
K	.015	.021	5
L	.008	.012	5
M	.045	.070	

5. WHEN THE SOLDER LEAD FINISH IS SPECIFIED, THE MAXIMUM LIMIT SHALL BE INCREASED BY .003 IN.
4. MEASURED FROM CENTERLINE TO CENTERLINE AT LEAD TIPS.
3. PACKAGE STANDOFF TO BE MEASURED PER JEDEC REQUIREMENTS.
2. OVERALL LENGTH INCLUDES .010 IN. FLASH ON EITHER END OF THE PACKAGE.
1. LEAD FINISH IS TO BE SPECIFIED ON THE DETAIL SPECIFICATION.

NOTES;

68000 Family
Ceramic Dual-In-Line Package (P)
64 Pin



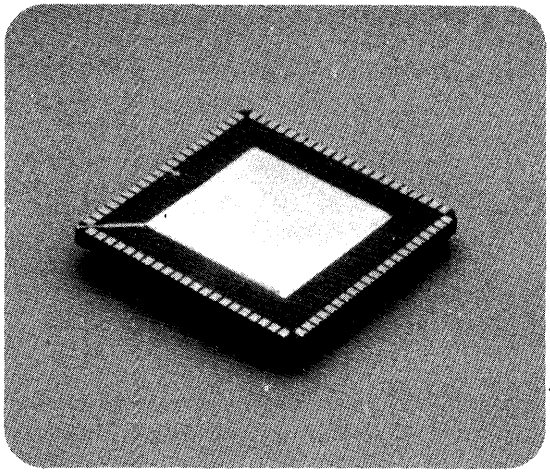


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	80.52	82.04	3.170	3.240
B	22.25	22.96	0.900	0.920
C	3.05	4.32	0.120	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.057
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	22.61	23.11	0.890	0.910
M	-	10°	-	10°
N	1.02	1.52	0.020	0.060

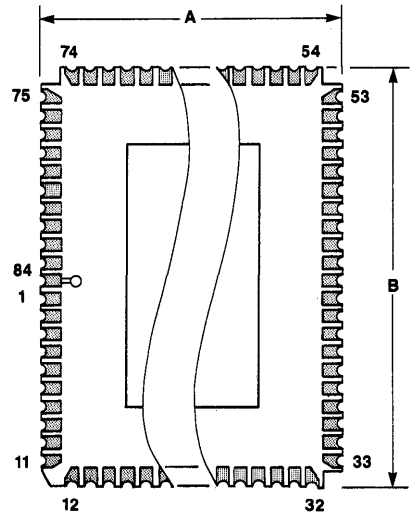
Case 746.01

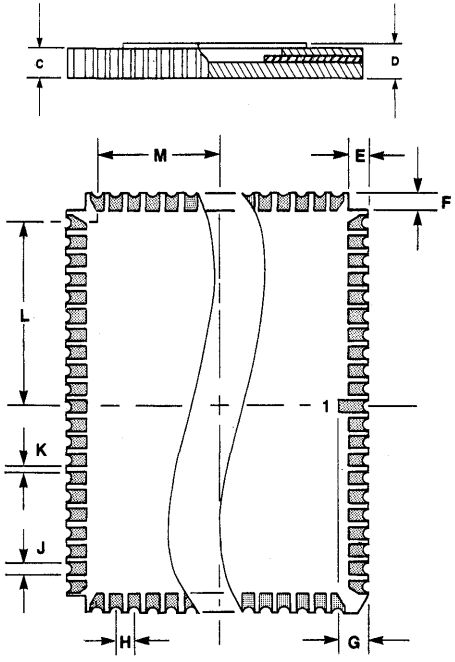
NOTES:
1. Dimension -A- is datum.
2. Positional tolerance for leads: ⌖ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- is seating plane.
4. Dimension "L" to center of leads when formed parallel.
5. Dimensioning and tolerancing per ANSI Y14.5, 1973.

Ceramic Leadless Chip Carrier (E)
84 Pin



TOP VIEW





BOTTOM

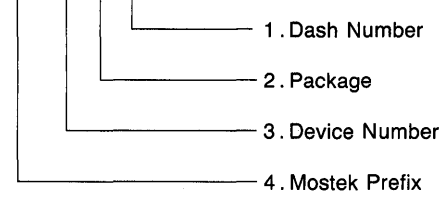
DIM.	INCHES		NOTES
	MIN.	MAX.	
A	1.138	1.167	
B	1.138	1.167	
C	.070	.090	
D	.080	.110	
E	.044	.056	
F	.044	.056	
G	.075	.095	
H	.048	.052	
H	.048	.052	
J	.033	.039	
K	.010	.018	
L	.495	.505	
M	.495	.505	

NOTES
1. BODY MATERIAL SHALL BE $A1_2O_3$
2. PLATING SHALL BE GOLD OVER NICKEL AS SPECIFIED IN THE DETAIL SPECIFICATION

ORDERING INFORMATION

Factory orders for parts described in this book should include a four-part number as explained below:

Example: MK 4167 P - 3



1. Dash Number

One or two numerical characters defining specific device performance characteristics and operating temperature range.

2. Package

P - Gold side-brazed ceramic DIP
J - CER-DIP
N - Epoxy DIP (Plastic)
K - Tin-side-brazed ceramic DIP
T - Ceramic DIP with transparent lid
E - Ceramic leadless chip carrier
D - Dual density RAM-PAC
F - Flat pack

3. Device Number

1XXX or 1XXXX - Shift Register, ROM
2XXX or 2XXXX - ROM, EPROM
3XXX or 3XXXX - ROM, EPROM
38XX - Microcomputer Components
4XXX or 4XXXX - RAM
5XXX or 5XXXX - Telecommunication and Industrial
7XXX or 7XXXX - Microcomputer Systems

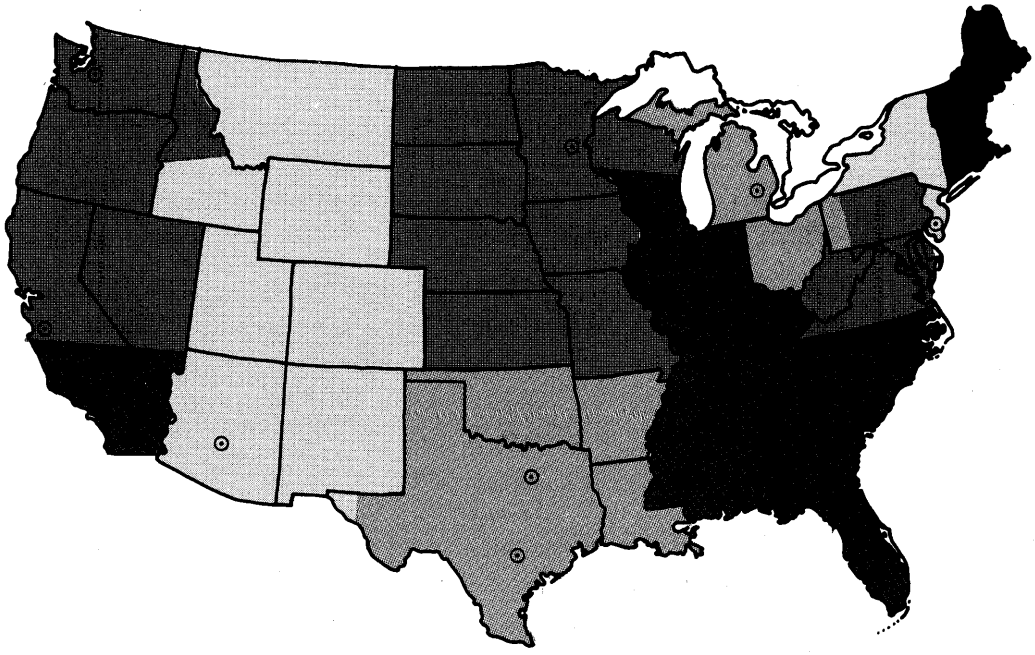
4. Mostek Prefix

MK - Standard Prefix

MKB - Military Hi-Rel screening to MIL-STD-883 Class B for extended temperature range operation.

MKI - Industrial Hi-Rel screening for −40°C to +85°C operation.

U.S. AND CANADIAN SALES OFFICES



CORPORATE HEADQUARTERS

Mostek Corporation
1215 W. Crosby Rd.
P.O. Box 110169
Carrollton, Texas 75006
214/466-6000
TWX 910-860-5975

REGIONAL OFFICES

Northeastern Area
Mostek
777 West Putnam
Greenwich, Conn. 06830
203/531-1146
TWX 710-579-2928

Northeast U.S.
Mostek
83 Cambridge St.
Suite 2-D
Burlington, Mass. 01803
617/273-3310
TWX 710-348-0459

Southeastern Area
Mostek
Pavilions at Greentree
Suite 101
Marlton, New Jersey 08053
609/596-9200
TWX 710-940-0103

Southeast U.S.
Mostek
13907 N. Dale Mabry Highway
Suite 201
Tampa, Florida 33618
813/962-8338
TWX 810-876-4611

Mostek
303 Williams Ave.
Suite 1031
Huntsville, AL 35801
205/539-2061
TWX 910-997-0411

Upstate NY Region
Mostek
4651 Crossroads Park Dr., Suite 201
Liverpool, NY 13088
315/457-2160
TWX 710-545-0255

Chicago Region
Mostek
Two Crossroads of Commerce
Suite 360
Rolling Meadows, Ill. 60008
312/577-9870
TWX 910-291-1207

North Central U.S.
Mostek
6101 Green Valley Dr.
Bloomington, Mn. 55438
612/831-2322
TWX 910-576-2802

Michigan
Mostek
Orchard Hill Place
21333 Haggerty Road
Suite 321
Novi, MI 48050
313/348-8360
TWX 810-242-1471

Central U.S.
Mostek
4100 McEwen Road
Suite 151
Dallas, Texas 75234
214/386-9340
TWX 910-860-5437

Southwest Region
Mostek
4100 McEwen Road
Suite 237
Dallas, Texas 75234
214/386-9141
TWX 910-860-5437

Chevy Chase #4
7715 Chevy Chase Dr., Suite 116
Austin, TX 78752
512/458-5226
TWX 910-874-2007

Western Region
Northern California
Mostek
1762 Technology Drive
Suite 126
San Jose, Calif. 95110
408/287-5080
TWX 910-338-2219

Seattle Region
Mostek
1107 North East 45th St.
Suite 411
Seattle, WA 98105
206/632-0245
TWX 910-444-4030

Southern California
Mostek
18004 Skypark Circle
Suite 140
Irvine, Calif. 92714
714/250-0455
TWX 910-595-2513

Arizona Region
Mostek
Camelback Arboleda Office Park
1661 E. Camelback
Suite 179
Phoenix, AZ 85016
602/279-0713
TWX 910-957-4581

U.S. AND CANADIAN REPRESENTATIVES

ALABAMA
Conley & Associates, Inc.
3322 Memorial Pkwy., S.W.
Suite 19
Huntsville, AL 35801
205/882-0316
TWX 810-726-2159

ARIZONA
Summit Sales
7825 E. Redfield Rd.
Scottsdale, AZ 85260
602/998-4850
TWX 910-950-1283

CALIFORNIA
CK Associates
8333 Clairemont Mesa Blvd.
Suite 105
San Diego, CA 92111
619/279-0420

Quality Peripherals
1210 S. Bascom Ave.
Suite 10
San Jose, CA 95128
408/559-3882

Quality Peripherals
17941 Skypark Circle
Suite H
Irvine, CA 92714
714/250-1033

COLORADO
Waugaman Associate*
4800 Van Gordon
Wheat Ridge, CO 80033
303/423-1020
TWX 910-938-0750

CONNECTICUT
New England Technical Sales
240 Pomeroy Ave.
Meriden, CT 06450
203/237-8827
TWX 710-461-1126

FLORIDA
Conely & Associates, Inc.*
P.O. Box 309
235 S. Central
Oviedo, FL 32765
305/365-3283
TWX 810-856-3520

Conely & Associates, Inc.
4019 W. Waters
Suite 2
Tampa, FL 33614
813/885-7658
TWX 810-876-9136

Conely & Associates, Inc.
P.O. Box 700
1612 N.W. 2nd Avenue
Boca Raton, FL 33432
305/395-6108
TWX 510-953-7548

Remtek, Inc.
728 Degan Drive
Port St. Lucie, FL 33452
305/878-6771

GEORGIA
Conely & Associates, Inc.
3951 Pleasantdale Road
Suite 201
Doraville, GA 30340
414/447-6992
TWX 810-766-0488

Remtek, Inc.
18 Perimeter Park
Suite 100
Atlanta, GA 30341
404/453-4705

ILLINOIS
Carlson Electronic Sales*
Associates, Inc.
600 East Higgins Road
Elk Grove Village, IL 60007
312/956-8240
TWX 910-222-1819

Mar-Con Associates Inc.
4836 Main St.
Skokie, IL 60077
312/675-6450
910-223-3645
Compucon
312/677-3230

INDIANA
Technology Marketing* Corp.
599 Industrial Drive
Carmel, IN 46032
317/844-8462
TWX 910-997-0194

Technology Marketing Corp.
3428 West Taylor St.
Fort Wayne, IN 46804
219/432-5553
TWX 810-499-4111

IOWA
Carlson Electronic Sales
204 Collins Road, N.E.
Cedar Rapids, IA 52402
319/377-6341
TWX 910-222-1819

KANSAS
Rush & West Associates*
107 N. Chester Street
Olathe, KS 66061
913/764-2700
Wichita 316/683-0206
TWX 910-749-6404

KENTUCKY
Technology Marketing Corp.
8819 Roman Court
P.O. Box 91147
Louisville, KY 40291
502/499-7808
TWX 810-535-3757

MARYLAND
Arbotek Associates
102 W. Joppa Road
Towson, MD 21204
301/825-0775
TWX 710-862-1874

KD Associates
201 Benton Avenue
Linthicum, MD 21090
301/859-5151 (Baltimore Area)
301/261-1311 (Washington Area)
TWX 710-862-9320

MASSACHUSETTS
New England Technical Sales*
101 Cambridge Street
Burlington, MA 01803
617/272-0434
603/778-8495 (Home)
TWX 710-332-0435

MICHIGAN
Action Components
21333 Haggerty Road
Suite 310B
Novi, MI 48050
313/349-3940

Comp-U-Tronics, Inc.
Route 2, Box 98
Blue Springs, MI 64015
816/229-3370

MINNESOTA
Cahill, Schmitz & Cahill, Inc.*
315 N. Pierce
St. Paul, MN 55104
612/646-7217
TWX 910-563-3737

Dytec/North, Inc.
1821 University Ave.
Suite 173 South
St. Paul, MN 55104
612/645-5816
TWX 910-563-3724

Micro Resources, Inc.
4640 W. 77th St.
Suite 109
Edina, MN 55435
612/830-1454

MISSOURI
Rush & West Associates
720 Manchester Road
Suite 211
Ballwin, MO 63011
314/394-7271
TWX 910-752-653

NORTH CAROLINA
Conely & Associates, Inc.
4050 Wake Forest Road
Suite 102
Raleigh, NC 27609
919/876-9862
TWX 510-928-1829

NEW JERSEY
Datronix
1930 E. Marlton Pike
Executive News, Suite P-79
Cherry Hill, NJ 08003
609/424-6622

Tritek Sales, Inc.
21 E. Euclid Ave.
Haddonfield, NJ 08033
609/429-1551
215/627-0149 (Philadelphia Line)
TWX 710-896-0881

NEW MEXICO
Waugaman Associates
P.O. Box 14894
Albuquerque, NM 871111
or
9004 Menaul NE
Suite 7
Albuquerque, NM 87112
505/294-1436

NEW YORK
ERA Inc.
354 Veterans Memorial Highway
Commack, NY 11725
516/543-0510
TWX 510-226-1485
(New Jersey Phone #
800/645-5500, 5501)

Tri-Tech Electronics Inc.*
6836 East Genesse St.
Fayetteville, NY 13066
315/446-2881
TWX 710-541-0604

Tri-Tech Electronics, Inc.
3215 East Main St.
Endwell, NY 13760
607/754-1094
TWX 510-252-0891

Tri-Tech Electronics, Inc.
300 Main St.
E. Rochester, NY 14445
716/385-6500
TWX 510-253-6356

Tri-Tech Electronics, Inc.
14 Westview Dr.
Fishkill, NY 12524
914/897-5611
TWX 710-541-0604

OHIO
The Lyons Corp.
4812 Frederick Rd.
Dayton, Ohio 45414
513/278-0714
TWX 810-459-1754

The Lyons Corp.
4615 N. Streetsboro Rd.
Richfield, Ohio 44286
216/659-9224
TWX 810-427-9103

OREGON
Northwest Marketing Assoc.
9999 S.W. Wilshire St.
Suite 124
Portland, OR 97225
503/297-2581
TELEX 910-464-5157

TEXAS
Technological System Sales
4255 LBJ Freeway
Suite 282
Dallas, TX 75234
214/458-0644

UTAH
Waugaman Associates
5258 Pinemont Dr.
Suite B-100
Salt Lake City, UT 84107
801/261-0802
TLX 757949

WASHINGTON
Northwest Marketing Assoc.*
12835 Bellevue-Redmond Rd.
Suite 330N
Bellevue, WA 98005
206/455-5846
TWX 910-443-2445

WISCONSIN
Carlson Electronic* Sales
Associates, Inc.
Northbrook Executive Ctr.
10701 West North Ave.
Suite 12
Milwaukee, WI 53226
414/476-2790
TWX 910-222-1819

CANADA
Cantec Representatives Inc.*
1573 Laperriere Ave.
Ottawa, Ontario
Canada, K1Z 7T3
613/725-3704
TWX 610-562-8967

Cantec Representatives Inc.
8 Strathearn Ave., Unit 18
Brampton, Ontario
Canada L6T 4L8
416/791-5922
TWX 610-492-2683

Cantec Representatives Inc.
3639 Sources Blvd.
Suite 116
Dollard Des Ormeaux, Quebec
Canada H9B 2K4
514/683-6131
TWX 610-422-3985

PUERTO RICO
Jose L. Puig
New England Technical Sales Cor
P.O. Box 8804
Ponce, Puerto Rico PR00732
809/843-7139

*Home Office

U.S. AND CANADIAN DISTRIBUTORS

ALABAMA
Schweber Electronics
2227 Drake Avenue S.W.
Suite 14
Huntsville, ALA 35805
205/882-2200

ARIZONA
Kierulff Electronics
4134 E. Wood St.
Phoenix, AZ 85040
602/437-0750
TWX 910/951-1550

Schweber Electronics
11049 North 23rd Drive
Phoenix, AZ 85029
602/997-4874
TWX 910/950-1174

CALIFORNIA
Arrow Electronics
2961 Dow Avenue
Tustin, CA 92680
714/838-5422
TWX 910-595-2860

Arrow Electronics
19748 Dearborn St.
Chatsworth, CA 91311
213/701-7500
TWX 910-493-2086

Arrow Electronics
9511 Ridgehaven Court
San Diego, CA 92123
619/565-4800
TWX 310/371-8757

Arrow Electronics
521 Weddell Dr.
Sunnyvale, CA 94086
408/745-6600
TWX 910/339-9371

Kierulff Electronics
2585 Commerce Way
Los Angeles, CA 90040
213/725-0325
TWX 910/580-3106

Kierulff Electronics
3969 E. Bayshore Rd.
Palo Alto, CA 94303
415/968-6292
TWX 910/379-6430

Kierulff Electronics
8797 Balboa Avenue
San Diego, CA 92123
619/278-2112
TWX 910/335-1182

Kierulff Electronics
14101 Franklin Avenue
Tustin, CA 92680
714/731-5711
TWX 910/595-2599

Schweber Electronics
17822 Gillette Avenue
Irvine, CA 92714
714/863-0200
TWX 910/595-1720

Schweber Electronics
3110 Patrick Henry Dr.
Santa Clara, CA 95050
408/748-4700
TWX 910/338-2043

COLORADO
Arrow Electronics
1390 S. Potomac Street
Suite 136
Aurora, CO 80012
303/696-1111
TWX 910/932-2999

Kierulff Electronics
7060 S. Tucson Way
Englewood, CO 80112
303/790-4444
TWX 910/932-0169

CONNECTICUT
Arrow Electronics
12 Beaumont Rd.
Wallingford, CT 06492
203/265-7741
TWX 710/476-0162

Kierulff Electronics
165 N. Plains Industrial Rd.
Wallingford, CT 06492
203/265-1115
TWX 710/476-0450

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, CT 06810
203/792-3500
TWX 710/456-9405

FLORIDA
Arrow Electronics
1001 N.W. 62nd St.
Suite 108
Ft. Lauderdale, FL 33309
305/776-7790
TWX 510/955-9456

Arrow Electronics
50 Woodlake Dr.
Palm Bay, FL 32905
305/725-1480
TWX 510/959-6337

Kierulff Electronics
4850 N. State Road 7
Suite E
Ft. Lauderdale, FL 33319
305/486-4004
TWX 510/955-9801

Kierulff Electronics
3247 Tech Drive
St. Petersburg, FL 33702
813/576-1966
TWX 810/863-5625

Schweber Electronics
2830 North 28th Terrace
Hollywood, FL 33020
305/927-0511
TWX 510/954-0304

Schweber Electronics
181 Whooping Loop
Altamonte Springs, FL 32701
(Orlando)
305/331-7555

GEORGIA
Arrow Electronics
2979 Pacific Drive
Norcross, GA 30071
404/449-8252
TWX 810/766-0439

Kierulff Electronics
5824 E. Peachtree Corner East
Norcross, GA 30092
404/447-5252
TWX 810/766-4527

Schweber Electronics
303 Research Drive, Suite 210
Norcross, GA 30092
404/449-9170
TWX 810/766-1592

ILLINOIS
Arrow Electronics
2000 Algonquin Road
Schaumburg, IL 60195
312/397-3440
TWX 910/291-3544

Kierulff Electronics
1536 Landmeier Rd.
Elk Grove Village, IL 60007
312/640-0200
TWX 910/222-0351

Schweber Electronics
904 Cambridge Dr.
Elk Grove Village, IL 60007
312/364-3750
TWX 910/222-3453

INDIANA
Advent Electronics Electronics
8446 Moller
Indianapolis, IN 46268
317/872-4910
TWX 810/341-3228

Arrow Electronics
2718 Rand Road
Indianapolis, IN 46241
317/243-9353
TWX 810/341-3119

Pioneer Electronics
6408 Castleplace Drive
Indianapolis, IN 46250
317/849-7300
TWX 810/260-1794

IOWA
Advent Electronics
682 58th Avenue
Court South West
Cedar Rapids, IA 52404
319/363-0221
TWX 910/525-1337

Arrow Electronics
1930 St. Andrews Dr., NE
Cedar Rapids, IA 52402
319/395-7230

Schweber Electronics
5270 North Park Place, N.E.
Cedar Rapids, IA 52402
319/373-1417

KANSAS
Schweber Electronics
Wycliff Commercial Center
10300 West 103rd Street
Suite 103 Building F
Overland Park, KS 66214
913/492-2921

MARYLAND
Arrow Electronics
4801 Benson Avenue
Baltimore, MD 21227
301/247-5200
TWX 710/236-9005

Kierulff Electronics
825 D. Hammonds Ferry Road
Linthicum, MD 21090
301/636-5800
TWX 710/234-1971

Pioneer Electronics
9100 Gaither Road
Gaithersburg, MD 20877
301/921-0660
TWX 710/828-0545

Schweber Electronics
9218 Gaither Rd.
Gaitherbursg, MD 20877
301/840-5900
TWX 710/828-9749

MASSACHUSETTES
Arrow Electronics
Arrow Drive
Woburn, MA 01801
617/933-8130
TWX 710/393-6770

Kierulff Electronics
13 Fortune Drive
Billerica, MA 01865
617/935-5134
TWX 710/390-1449

Lionex Corporation
1 North Avenue
Burlington, MA 01803
617/272-9400
TWX 710/332-1387

Schweber Electronics
25 Wiggins Avenue
Bedford, MA 01730
617/275-5100
TWX 710/326-0268

MICHIGAN
Arrow Electronics
3810 Varsity Drive
Ann Arbor, MI 48104
313/971-8220
TWX 810/223-6020

Pioneer Electronics
13485 Stamford
Livonia, MI 48150
313/525-1800
TWX 810/242-3271

Schweber Electronics
12060 Hubbard Ave.
Livonia, MI 48150
313/525-8100
TWX 810/242-2983

MINNESOTA
Arrow Electronics
5230 W. 73rd Street
Edina, MN 55435
612/830-1800
TWX 910/576-3125

Kierulff Electronics
7667 Cahill Rd.
Edina, MN 55435
612/941-7500
TWX 910/576-2721

Schweber Electronics
7424 W. 78th Street
Edina, MN 55345
612/941-5280
TWX 910/576-3167

MISSOURI
Arrow Electronics
2380 Schuetz Road
St. Louis, MO 63141
314/567-6888
TWX 910/764-0882

Kierulff Electronics
2608 Metro Park Blvd.
Maryland Heights, MO 63043
314/739-0855
TWX 910/762-0721

Olive Electronics
9910 Page Blvd.
St. Louis, MO 63132
314/426-4500
TWX 910/763-0720

Schweber Electronics
502 Earth City Expressway
Suite 203
Earth City, MO 63045
314/739-0526

Semiconductor Spec
3805 N. Oak Trafficway
Kansas City, MO 64116
816/452-3900

NEW HAMPSHIRE
Arrow Electronic
1 Perimeter Rd.
Manchester, NH 03103
603/668-6968
TWX 710/220-1684

Schweber Electronics
Farms Bld'g #2 1st Floor
Kilton & South River Road
Manchester, NH 03102
603/625-2550
TWX 710/220-7572

NEW JERSEY
Arrow Electronics
6000 Lincoln Drive East
Marlton, NJ 08053
609/596-8000
TWX 710/897-0829

Arrow Electronics
2 Industrial Rd.
Fairfield, NJ 07006
201/575-5300
TWX 710/734-4403

Kierulff Electronics
37 Kulick Road
Fairfield, NJ 07006
201/575-6750
TWX 710/734-4372

Schweber Electronics
18 Madison Road
Fairfield, NJ 07006
201/227-7880
TWX 710/734-4305

NEW MEXICO
Arrow Electronics
2460 Alamo Ave. S.E.
Albuquerque, NM 87106
505/243-4566
TWX 910/989-1679

NEW YORK
Add Electronic
7 Adler Drive
E. Syracuse, NY 13057
315/437-0300

Arrow Electronics
25 Hub Drive
Melville, NY 11747
516/391-1300
TWX 510/224-6155

Arrow Electronics
7705 Maltlage Drive
P.O. Box 370
Liverpool, NY 13088
315/652-1000
TWX 710/545-0230

Arrow Electronics
3000 S. Winton Road
Rochester, NY 14623
716/427-0300
TWX 510/253-4766

Arrow Electronics
20 Oser Ave.
Hauppauge, NY 11787
516/231-1000
TWX 510/227-6623

Lionex Corporation
400 Oser Ave.
Hauppauge, NY 11787
516/273-1660
TWX 510/227-1042

Schweber Electronics
3 Town Line Circle
Rochester, NY 14623
716/424-2222

Schweber Electronics
34 Jericho Turnpike
Westbury, NY 11590
516/334-7474
TWX 510/222-3660

U.S. AND CANADIAN DISTRIBUTORS

NORTH CAROLINA
Arrow Electronics
938 Burke St.
Winston Salem, NC 27102
919/725-8711
TWX 510/931-3169

Arrow Electronics
3117 Poplarwood Court
Suite 123, P.O. Box 95163
Raleigh, NC 27625
919/876-3132
TWX 510/928-1856

Hammond Electronics
2923 Pacific Avenue
Greensboro, NC 27406
919/275-6391
TWX 510/925-1094

Kierulff Electronics
1 North Commerce Center
5249 North Blv'd.
Raleigh, NC 27604
919/872-8410
TWX 310/377-2204

Schweber Electronics
1 Commerce Center
5285 North Blv'd.
Raleigh, NC 27604
919/876-0000
TWX 510/928-0531

OHIO
Arrow Electronics
7620 McEwen Road
Centerville, OH 45459
513/435-5563
TWX 810/459-1611

Arrow Electronics
6238 Cochran Road
Solon, OH 44139
216/248-3990
TWX 810/427-9409

Kierulff Electronics
23060 Miles Road
Cleveland, OH 44128
216/587-6558
TWX 810/427-2282

Pioneer Electronics
4800 East 131st Street
Cleveland, OH 44105
216/587-3600
TWX 810/422-2211

Pioneer Electronics
4433 Interpoint Blvd.
Dayton, OH 45424
513/236-9900
TWX 810/459-1622

Schweber Electronics
23880 Commerce Park Road
Beachwood, OH 44122
216/464-2970
TWX 810/427-9441

Schweber Electronics
7865 Paragon Road
Suite 210
Dayton, OH 45459
513/439-1800

OKLAHOMA
Arrow Electronics
4719 S. Memorial
Tulsa, OK 74745
918/665-7700

Kierulff Electronics
12318 E. 60th St.
Tulsa, OK 74145
918/252-7537
TWX 910/845-2150

Quality Components
9934 East 21st South
Tulsa, OK 74129
918/664-8812

Schweber Electronics
4815 South Sheridan
Fountain Plaza
Suite 109
Tulsa, OK 74145
918/622-8000

OREGON
Arrow Electronics
10160 S.W. Nimbus Ave., F-3
Portland, OR 97223
503/684-1690

PENNSYLVANIA
Arrow Electronics
650 Seco Rd.
Monroeville, PA 15146
412/856-7000
TWX 710/797-3894

Pioneer Electronics
259 Kappa Drive
Pittsburgh, PA 15238
412/782-2300
TWX 710/795-3122

Pioneer Electronics
261 Gibraltar
Horsham, PA 19044
215/674-4000
TWX 510/665-6778

Schweber Electronics
231 Gibraltar Rd.
Horsham, PA 19044
215/441-0600
TWX 510/665-6778

Schweber Electronics
1000 R.I.D.C. Plaza
Suite 203
Pittsburgh, PA 15238
412/782-1600

SOUTH CAROLINA
Hammond Electronics
1035 Lowndes Hill Rd.
Greenville, SC 29602
803/233-4121
TWX 810/281-2233

TEXAS
Arrow Electronics
10125 Metropolitan Dr.
Austin, TX 78758
512/835-4180
TWX 910/874-1348

Arrow Electronics
13715 Gamma Road
Dallas, TX 75240
214/386-7500
TWX 910/860-5377

Arrow Electronics
10899 Kinghurst Drive
Suite 100
Houston, TX 77099
713/530-4700
TWX 910/880-4439

Kierulff Electronics
3007 Longhorn Blv'd.
Suite 105
Austin, TX 78758
512/835-2090
TWX 910/874-1359

Kierulff Electronics
9610 Skillman Ave.
Dallas, TX 75243
214/343-2400
TWX 910/861-9149

Kierulff Electronics
10415 Landsbury Dr.
Suite 210
Houston, TX 77099
713/530-7030
TWX 910/880-4057

Quality Components
4257 Kellway Circle
Addison, TX 75001
214/387-4949
TWX 910/860-5459

Quality Components
2427 Rutland Drive
Austin, TX 78758
512/835-0220
TWX 910/874-1377

Quality Components
1005 Industrial Blv'd.
Sugarland, TX 77478
713/491-2255
TWX 910/880-4893

Schweber Electronics
4202 Beltway Drive
Dallas, TX 75234
214/661-5010
TWX 910/860-5493

Schweber Electronics
6300 La Calma Dr.
Suite 240
Austin, TX 78752
512/458-8253

Schweber Electronics
10625 Richmond
Suite 100
Houston, TX 77042
713/784-3600
TWX 910/881-4836

UTAH
Arrow Electronics
4980 Amelia Earhart Dr.
Salt Lake City, UT 84116
801/539-1135

Kierulff Electronics
2121 South 3600 West
Salt Lake City, UT 84119
801/973-6913
TWX 910/925-4072

WASHINGTON
Arrow Electronics
14320 NE 21st
Bellevue, WA 98005
206/643-4800
TWX 910/444-3033

Kierulff Electronics
1053 Andover Park East
Tukwila, WA 98188
206/575-4420
TWX 910/444-2034

WISCONSIN
Arrow Electronics
434 Rawson Avenue
Oak Creek, WI 53154
414/764-6600
TWX 910/262-1193

Kierulff Electronics
2236 G.W. Bluemound Road
Waukesha, WI 53186
414/784-8160
TWX 910/265-3653

Schweber Electronics
150 Sunnyslope Road
Suite 120
Brookfield, WI 53005
414/784-9020

CANADA
Prelco Electronics
7611 Bath Road
Mississauga, Ontario
Toronto L4T 3T1
416/678-0401
Telex 06-96-8915

Prelco Electronics
480 Port Royal St. W.
Montreal 357 P.Q. H3L 2B9
514/389-8051
Telex 05-82-7590

Prelco Electronics
215 Stafford Road
Nepean, Ontario K2E 7K1
613/726-1800

R.A.E. Industrial
3455 Gardner Court
Burnaby, B.C. V5G 4J7
604/291-8866
TWX 610/929-3065

R.A.E. Industrial
11680 170th Street
Edmonton, Alberta T5S 1J7
403/451-4001
Telex 037-2653

Zentronics
155 Colonnade Rd.
Nepean, Ontario
K2E7K1
613/226-8840

Zentronics
8 Tilbury Court
Brampton, Ontario
(Toronto) L6V 2L1
416/451-9600
Telex 06-97678

Zentronics
505 Locke St.
St. Laurent, Quebec
H4T IX7
514/735-5361
Telex 058-27535

Zentronics
590 Berry Street
Winnipeg, Manitoba R3H 0S1
204/775-8661

Zentronics
564/10 Weber Street, N.
Waterloo, Ontario N2L 5C6
519/884-5700

Zentronics
11400 Brideport Road
Unit 108
Richmond, BC V6X IT2
604/273-5575

Zentronics
3300-14 Avenue, N.E. Bay #1
Calgary, Alberta T2A 6J4
403/272-1021

*Franchised for USA and Canada excluding California for military products

INTERNATIONAL SALES REPRESENTATIVES AND DISTRIBUTORS

ARGENTINA
Rayo Electronics S.R.L.
Belgrano 990, Pisos 6y2
1092 Buenos Aires,
Republic of Argentina
(38)-1779,
Telex: 122153 ANS BK RAYO

AUSTRALIA
Amtron Tyree Pty. Ltd.
176 Cope Street
Waterloo, N.S.W. 2017
Australia
(02) 69-89.666
Telex: 25643 ANS BK TYREE

BRAZIL
Cosele, Ltd.
Rua da Consolachao, 867 2 and
Conj 22
01301 Sao Paulo - Sp,
Brazil
(11) 259 3719/255 1733
Telex: 1130869 ANS BK CSLE BR

HONG KONG
CET
1402 Tung Wah Mansion
199 - 203 Hennessy Road
Wanchai, Hong Kong
(5) 729 376
Telex: 85148 ANS BK CET HX

ISRAEL
Telsys Ltd.
12 Kehilat Venetsia St.
69010 Tel-Aviv, Israel
(3) 494891-2, 494881-2
Telex: 032392

JAPAN
Systems Marketing, Inc.
Shin - kanda Bldg. 1-8-5 Kaji-cho
Chiyoda-ku
Tokyo 101, Japan
32542751
Telex: 25276 ANS BK SMITOK
FAX 3 254 3288

Tomen Electronics Corp.
2-1-1 Uchisaiwai - Cho
Chiyoda - Ku
Tokyo, Japan 100
(03) 506 3670
Telex: J23548 ANS BK TMELC

KOREA
Vine Overseas Trading Corp.
Room 308 Korea Electric
Association Bldg.
11-4, Supyo-Dong, Jung-Ku
CPO Box 3154
Seoul, Korea
(02) 266 1663
Telex: K24154 ANS BK VINEJO

Seoul Corp LTD.
CPO Box 5003
Seoul 100, Korea
(02) 752 6121
FAX (02) 754 1348
Telex: K28641 ANS BK SJLEE

NEW ZEALAND
E.C.S. Div. of Airspares
P.O. Box 1048
Airport Palmerston North,
New Zealand
(63) 77-407
Telex: 791 3766 ANS BK Airspare
3766 NZ

SINGAPORE
Dynamar International, LTD.
12 Lorong Bakar Batu Unit 05-11
Kolam Ayer-Industrial Park,
Singapore 1334
7476188
TLX RS26283
ANS BK DYNAMA
FAX 7472648

SOUTH AFRICA
Promilect
P.O. Box 56310
Pinegowrie, 2123,
Transvaal
789-1400
Telex: 424822

TAIWAN
Dynamar Taiwan Ltd.
P.O. Box 67 - 445
Taipei, Taiwan
(2) 541 8251
Telex: 11064 ANS BK 11064
DYNAMAR

FOR ALL OTHER COUNTRIES
Mostek Corporation
International Dept.
MS 2220
P.O. Box 110169
Carrollton, Texas 75006, USA
214/466-6000
Telex: 4630093 ANS BK MSTA
FAX 466 7602

INTERNATIONAL MARKETING OFFICES

EUROPEAN HEAD OFFICE
Mostek International
Av de Tervuren 270-272 Bte 21
B-1150 Brussels/Belgium
02/762.18.80
Telex: 62011

FRANCE
Mostek France s.a.r.l.
35 Rue de Montjean
Z.A.C. Sud, Sentiers 504
F-94266 Fresnes Cedex
(1)666.21.25
Telex: 204049

GERMANY
PLZ 1-5 **Mostek GmbH**
Friedlandstrasse 1
D-2085 Quickborn
(04106) 2077/78
Telex: 213685

PLZ 6-7 **Mostek GmbH**
Schurwaldstrasse 15
D-7303 Neuhausen/Filder
(07158) 66.45
Telex: 72.38.86

PLZ 8 **Mostek GmbH**
Freischutzstrasse 92
D-8000 Munchen 81
(089) 95.10.71
Telex: 5216516

IRELAND
Mostek Ireland B.V.
Irish Sales Office
Snugboro Industrial Park
Blanchardstown, Co. Dublin
(1) 217333
Telex: 30958

ITALY
Mostek Italia SRL
Via F.D. Guerrazzi 27
1-20145 Milano
(02) 318.5337/349.2696
and 34.23.89
Telex: 333601

SWEDEN
Mostek Scandinavia AB
Spjutvagen 7
S-17561 Jarfalla
Sweden
08-362820
Telex: 12997

UNITED KINGDOM
Mostek U.K. Ltd.
Masons House,
1-3 Valley Drive
Kingsbury Road
London, N.W.9
01-2049322
Telex: 25940

JAPAN
Mostek Japan KK
3 - 24 Sakuragaoka - Machi
Shibuya - ku
Tokyo 150
(03) 496 4221
TLX 78123686 ANS BK
MKJAPAN
FAX (03) 496 4787

FAR EAST
Mostek Asia LTD
Suite 613 - 617
Mount Parker House
1111 Kings Road
Hong Kong
Phone: 5-681157-9
Telex: 72585 MKHK HX
FAX 5 - 665450

EUROPEAN SALES REPRESENTATIVES AND DISTRIBUTORS

AUSTRIA
Transistor Vertreibsges, mbH
Auhofstrasse 41 A
A-1130 Vienna
(0222) 829451, 829404
Telex: 0133738

DENMARK
Semicap APS
Alhambravej 3
DK-1826 Kobenhavn V
01-22.15.10
Telex: 15987

FINLAND
Insele Oy
Kumpulantie 1
SF-00520 Helsinki 52
90-750.600
Telex: 122217

FRANCE
Copel
Rue Fourny, Z.I.
B.P. 22, F-78530 BUC
(1) 956 10.18
Telex: 698965

Facen
110 Av de Flandre
F59290 Wasquehal. Nord
(20) 98.92.15

Branch Offices in:
Lille, Lyon,
Nancy, Rouen, Strasbourg

Mecodis
33-35, Rue Pierre Brossolette
F-94000 Creteil
(1) 898.-1111
Telex: 231160

P.E.P.
541, Av. du General de Gaulle
F-92140 Clamart
(1)630.24.56
Telex: 204534

Scaib
80 Rue d'Arcueil
SILIC 137
F-94523 Rungis Cedex
(1)-687.23.13
Telex: 204674
Branch offices:
Blanquefort, La Madeleine, Lyon,
Meylan, Nantes

Sorhodis
150-152, Rue A. France
F-69100 Villeurbanne
(7) 855 0044
Telex: 380181

GERMANY
Dr Dohrenberg
Bayreuther Strasse 3
D-1000 Berlin 30
(030) 213.80.43
Telex: 0184860

Retron GmbH
Rodeweg 18
Postfach 3143
3400 Goettingen
(0551) 9040
Telex: 96733

Branch Offices in:
Hannover, Frankfurt,
Stuttgart, Krailling

Raffel-Electronic GmbH
Lochnerstrasse 1
D-4030 Ratingen 1
(02102) 280.24
Telex: 8585180

Ecker
Koenigsberger Strasse 2
D-6120 Michelstadt
(06061) 2233
Telex: 4191630

POSITRON GmbH
Benzstrasse 1
Postfach 100364
D-7016 Gerlingen/Stuttgart
(07156) 3560
Telex: 7245266
Branch Offices in:
Hamburg, Dusseldorf, Munchen

Matronic GmbH
Lichtenberger Weg 3
D-7400 Tubingen
(07071) 45031
Telex: 17707111

Dema-Electronic GmbH
Turkenstrasse 11
D-8000 Munchen 2
(089) 2724053
Telex: 0529345

ITALY
Comprel S.p.A.
via le Fulvio Testi 115
1-20092 Cinisello B. (Mi)
(02) 61.20.641/2/3/4/5
Telex: 332484

Branch Offices in:
Bologna, Civitanova Marche,
Firenze,
Vicenza, Roma, Torino

Kontron S.p.A.
Via Medici del Vascello.26
1-20138 Milano
(02) 50721
Telex: 312288

Branch Offices in:
Padova, Torino,
Modena, Roma, Genova

THE NETHERLANDS
Nijkerk Elektronika BV
Drentestraat 7
NL - 1083 HK Amsterdam
(020) 462221
Telex: 11625

NORWAY
Satt Electronics A/S
P.O. Box 70
O.H. Bangs Vei 17
N-1322 Hovik
02-12.36.00
Telex: 72558

PORTUGAL
Digicontrole LDA
Av. de Roma 105
Sexto Esquerdo
1700 Lisboa
(19) 923924
Telex: 15084

SPAIN
Comelta S.A.
Emilio Munoz 41, ESC 1
Planta 1 Nave 2
Madrid-17
(01) 754 3001
Telex: 42007

Branch Office:
C. Pedro IV, 84-5^{a} Planta
Barcelona 5
(03) 300-7712
Telex: 51934

SWEDEN
Nordisk Elektronik AB
Box 27301
S-102 54 Stockholm
08-6350 40
Telex: 10547

SWITZERLAND
Memotec AG
Gaswerkstrasse, 32
CH-4901 Langenthal
063-28.11.22
Telex: 68636

UNITED KINGDOM
Celdis Limited
37-39 Loverock Road
Reading
Berks RG 31 ED
0734-58.51.71
Telex: 8483770

Hill Electronics
290 Antrim Road
Belfast
(0232) 755611
Telex: 747103

Pronto Electronic Systems Ltd
466-478 Cranbrook Road,
Gants Hill, Ilford
Essex 1G2 6LE
01-554 62.22
Telex: 8954213

VSI Electronics (UK) Ltd.
Roydonbury Industrial Park
Horsecroft Road
Harlow, Essex
CM195 BY
(0279) 35477
Telex: 81387

Thame Components Ltd.
Thame Park Road
Thame, Oxon
OX9 3XD
084 421.31.46
Telex: 837917

1984/1985 MICROELECTRONIC DATA BOOK

64K-BIT READ-ONLY MEMORY MK36000(P/J/N) SERIES

FEATURES

- MK36000 8K x 8 Organization— "Edge Activated" * operation ($\overline{CE}$)
- Access Time/Cycle Time

P/N	Access	Cycle
MK36000-4	250 ns	375 ns
MK36000-5	300 ns	450 ns

- Single +5V ± 10% Power Supply
- Standard 24 pin DIP
- Low Power Dissipation - 220mW Max Active
- Low Standby Power Dissipation - 45mW Max, ($\overline{CE}$ High)
- On chip latches for addresses
- Inputs and three-state outputs - TTL compatible
- Outputs drive 2 TTL loads and 100pF
- MKB version screened to MIL-STD-883

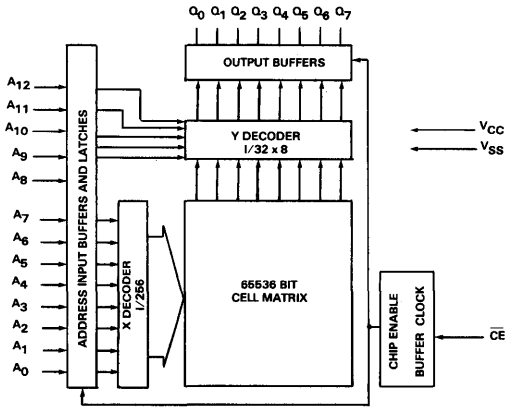
DESCRIPTION

The MK36000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK36000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

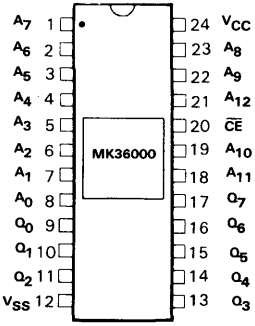
Use of a static storage cell with clocked control periphery allows the circuit to be put into an automatic low power standby mode. This is accomplished by maintaining the chip enable ($\overline{CE}$) input at a TTL high level. In this mode, power dissipation is reduced to typically 45mW, as compared to unclocked devices which draw full power continuously. In system operation, a device is selected by the $\overline{CE}$ input, while all others are in a low power mode, reducing the overall system power. Lower power means reduced power supply cost, less heat to dissipate and an increase in device and system reliability.

The edge activated chip enable also means greater system flexibility and an increase in system speed.

FUNCTIONAL DIAGRAM (MK36000)



PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	Address	V_{SS}	GND
O_0-O_7	Outputs	$\overline{CE}$	Chip Enable
V_{CC}	+5V		

* Trademark of Mostek Corporation

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature - Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature - Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	6
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%) ($0°C \leq T_A \leq +70°C$) [6]

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3 mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -220 μA	2.4			V	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%) ($0°C \leq T_A \leq +70°C$)[6]

SYM	PARAMETER	-4		-5		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_C	Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10000	300	10000	ns	4
t_{AC}	$\overline{CE}$ Access Time		250		300	ns	4
t_{OFF}	Output Turn Off Delay		60		75	ns	4
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_p	$\overline{CE}$ Precharge Time	125		150		ns	

NOTES:

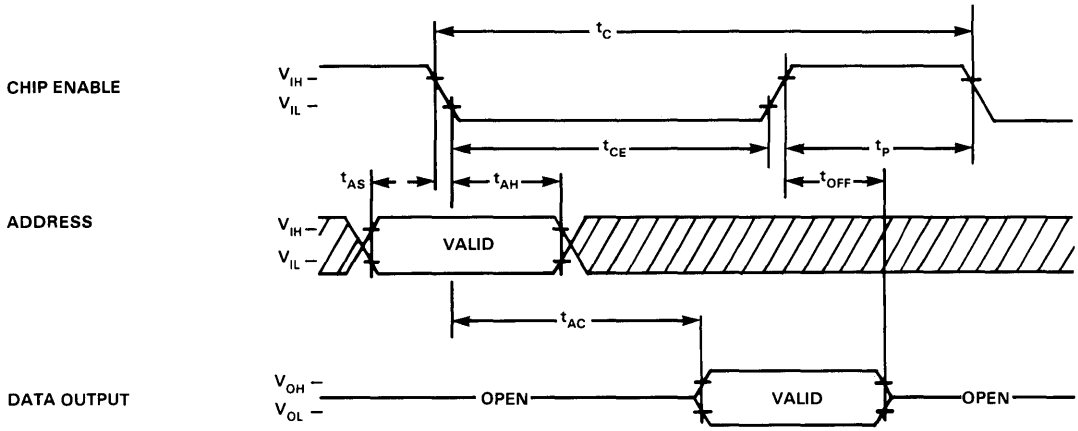
1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0 V to 5.5 V (V_{CC} = 5 V)
3. Device unselected; V_{OUT} = 0 V to 5.5 V
4. Measured with 2 TTL loads and 100 pF, transition times = 20 ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation: $C = \frac{\Delta Q}{}$ with ΔV = 3 volts
6. A minimum 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high.

CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM



DESCRIPTION (Continued)

The MK36000 features onboard address latches controlled by the $\overline{CE}$ input. Once the address hold time specification has been met, new address data can be applied in anticipation of the next cycle. Outputs can be wire 'OR'ed together, and a specific device can be selected by utilizing the $\overline{CE}$ input with no bus conflict on the outputs. The $\overline{CE}$ input allows the fastest access times yet available in 5 volt only ROM's and imposes no loss in system operating flexibility over an unclocked device.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{CE}$ input, will drive a minimum of 2 standard TTL loads. The MK36000 operates from a single +5 volt power supply with a wide ±10% tolerance, providing the widest operating margins available. The MK36000 is packaged in the industry standard 24 pin DIP.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK36000 ROM. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the Z80. It can offer significant cost advantages over PROM.

OPERATION

The MK36000 is controlled by the chip enable ($\overline{CE}$) input. A negative going edge at the $\overline{CE}$ input will activate the device as well as strobe and latch the inputs into the on-chip address registers. At access time the outputs will become active and contain the data read from the selected location. The outputs will remain latched and active until $\overline{CE}$ is returned to the inactive state.

64K-BIT MOS READ-ONLY MEMORY
MK37000(P/J/N) SERIES

FEATURES

- Organization: 8K x 8 Bit ROM - JEDEC Pinout
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Access Time/Cycle Time

P/N	ACCESS	CYCLE
MK37000-5	300 ns	450 ns
MK37000-4	250 ns	375 ns

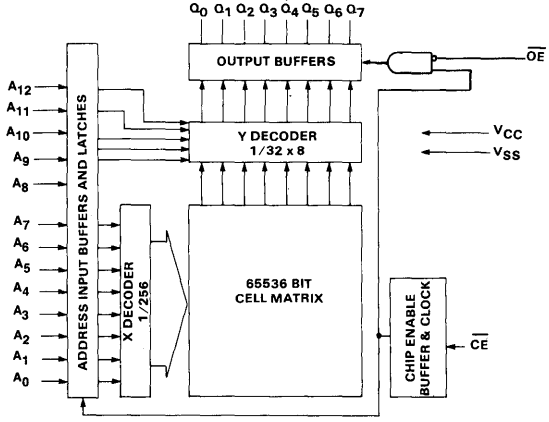
- Mask ROM replacement for 2764 EPROM
- No Connections allow easy upgrade to future generation higher density ROMs
- Low power dissipation: 220mW max active, 45mW max standby
- $\overline{CE}$ and $\overline{OE}$ functions facilitate Bus control
- MKB version screened to MIL-STD-883

DESCRIPTION

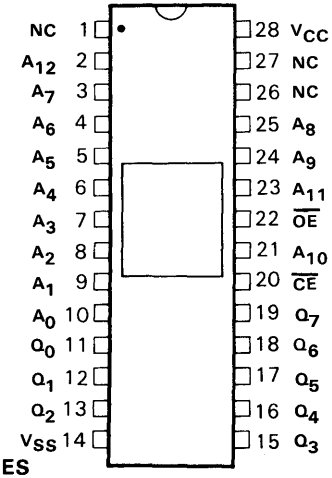
The MK37000 is a N-channel silicon gate MOS Read Only Memory, organized as 8192 words by 8 bits. As a state-of-the-art device, the MK37000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins. The MK37000 is to be used as a pin/function compatible mask programmable alternative to the 2764 8K x 8 bit EPROM. As a member of the Mostek BYTEWYDE Memory Family, the MK37000 brings to the memory market a new era of ROM, PROM and EPROM compatibility previously unavailable.

Use of clocked control periphery and a standard static ROM cell makes the MK37000 the lowest power 64K ROM available. Active power is a mere 220mW while standby ($\overline{CE}$ high) is only 45mW. To provide greater system flexibility an output enable ($\overline{OE}$) function has been added using one of the extra pins available on the

FUNCTIONAL DIAGRAM (MK37000)



PIN CONNECTIONS



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

X = Don't Care

PIN NAMES

A0 - A12-Address	NC - No Connection
$\overline{CE}$ - Chip Enable	$\overline{OE}$ - Output Enable
Q_0 - Q_7 - Outputs	V_{CC} - +5V supply
	V_{SS} - Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to V_{SS} ..... -1.0V to +7V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	
V_{IL}	Input Logic 0 Voltage	-1.0		0.8	V	
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS [6]

(V_{CC} = 5V ± 10%) ($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)			40	mA	1
I_{CC2}	V_{CC} Power Supply Current (Standby)			8	mA	7
$I_{I(L)}$	Input Leakage Current	-10		10	μA	2
$I_{O(L)}$	Output Leakage Current	-10		10	μA	3
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 3.3mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -220μA	2.4			V	

AC ELECTRICAL CHARACTERISTICS[6]

(V_{CC} = 5V ± 10%) ($0°C \leq T_A \leq +70°C$)

		-4		-5			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	375		450		ns	4
t_{CE}	$\overline{CE}$ Pulse Width	250	10,000	300	10,000	ns	4
t_{CEA}	$\overline{CE}$ Access Time		250		300	ns	4
t_{CEZ}	Chip Enable Data Off Time		60		75	ns	
t_{AH}	Address Hold Time Referenced to $\overline{CE}$	60		75		ns	
t_{AS}	Address Setup Time Referenced to $\overline{CE}$	0		0		ns	
t_P	$\overline{CE}$ Precharge Time	125		150		ns	
t_{OEA}	Output Enable Access Time		80		100	ns	
t_{OEZ}	Output Enable Data Off Time		60		75	ns	

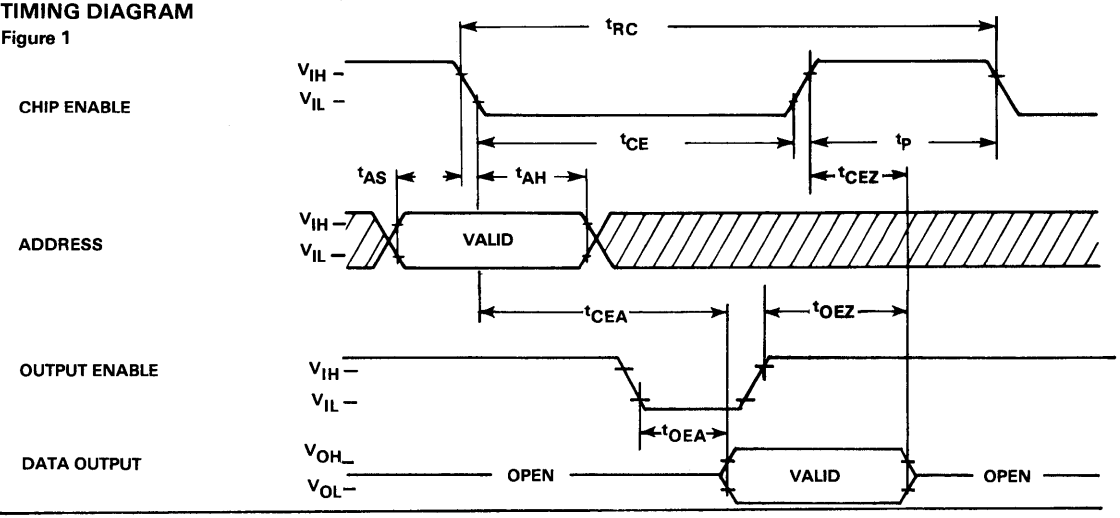
CAPACITANCE

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5	8	pF	5
C_O	Output Capacitance	7	15	pF	5

TIMING DIAGRAM

Figure 1



NOTES:

1. Current is proportional to cycle rate. I_{CC1} is measured at the specified minimum cycle time. Data Outputs open.
2. V_{IN} = 0V to 5.5V
3. Device unselected; V_{OUT} = 0V to 5.5V
4. Measured with 2 TTL loads and 100pF, transition times = 20ns
5. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:
   $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts
6. A minimum 2ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved. $\overline{CE}$ must be at V_{IH} for this time period.
7. $\overline{CE}$ high

DESCRIPTION (Continued)

28 pin DIP. This function matches that found on all of the new BYTEWYDE family of memories available from Mostek.

The use of clocked $\overline{CE}$ mode of operation provides an automatic power down mode of operation. The MK37000 features on chip address latches controlled by the $\overline{CE}$ input. Once address hold time is met, new address data can be provided to the device in anticipation of a subsequent cycle. It is not necessary to maintain the address up to access time to access valid data. The output enable function controls only the outputs and is not latched by $\overline{CE}$. The $\overline{CE}$ input can be used for device selection and the $\overline{OE}$ input used to avoid bus conflicts so that outputs can be 'OR'ed together when using multiple devices.

Other system oriented features include fully TTL compatible inputs and outputs. The three state outputs, controlled by the $\overline{OE}$ input, will drive a minimum of 2 standard TTL loads. The MK37000 operates from a single +5 volt power supply with a wide ± 10% tolerance, providing the widest operating margins available. The MK37000 is packaged in the industry standard 28 pin DIP. Pin 1 and 26 are not connected to allow easy upward compatibility with next generation higher density ROM which will use these pins for addresses. Pin 27 is not connected in order to maintain compatibility with RAMs which use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK37000. This device is ideally suited for 8 bit microprocessor systems such as those which utilize the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK37000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A negative going edge at the $\overline{CE}$ input will activate the device and latch the addresses into the on chip address registers. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access

time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met. The on chip address register allows addresses to be changed after the specified hold time (t_{AH}) in preparation for the next cycle. The outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the inactive state. After chip deselect time (t_{CEZ}) the output buffers will go to a high impedance state. The $\overline{CE}$ input must remain inactive (high) between subsequent cycles for time t_P to allow for precharging the nodes of the internal circuitry.

MK37000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 07FF for a 2K x 8 device. EPROM #2 would then start at address space 0800 and so on. A total of (4) 2K x 8 devices would be required to totally describe the address space of the 8K x 8 MK37000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be excepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

Acceptable EPROMs for Code Data

Table 1

EPROM	# REQUIRED
2716/2516	4
2732	2
2764	1

256K-BIT MOS READ-ONLY MEMORY
MK38000(P/N)-25

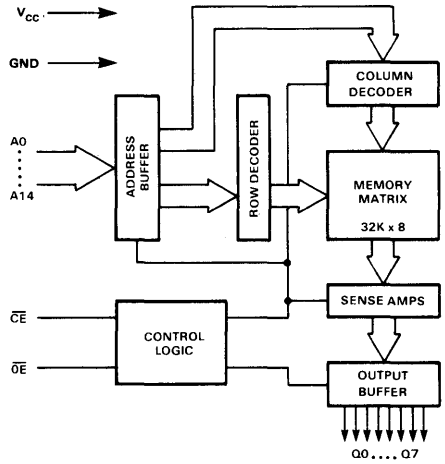
FEATURES

- Organized 32K x 8
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Access Time equals Cycle Time
- Static Operation
- Automatic Power Down
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- Pin 27, logical don't care (X), permits interchange with BYTEWYDE™ RAM ($\overline{WE}$)
- High performance

Part No.	Access Time	Cycle Time
MK38000-25	250 ns	250 ns

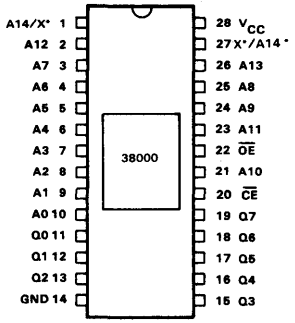
FUNCTIONAL DIAGRAM (MK38000)

Figure 1



PIN CONNECTIONS

Figure 2



PIN NAMES

A0-A14	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5 V
X	Logical Don't Care	GND	Ground
		Q0-Q7	Data Outputs

*Alternate pinout see Note 11. Must be defined with ROM code.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
H	X	Deselect	High-Z	Standby
L	H	Inhibit	High-Z	Active
L	L	Read	D_{OUT}	Active

DESCRIPTION

The MK38000 is a N-channel, silicon gate MOS Read Only Memory, organized as 32,768 words by 8 bits. As a state-of-the-art device, the MK38000 incorporates advanced circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

As a member of the Mostek BYTEWYDE Memory Family, the MK38000 allows compatibility between RAM, ROM, and EPROM. The MK38000 can be used as a pin/function density upgrade to the MK37000 8K x 8 bit ROM.

The output enable function controls only the outputs. The $\overline{CE}$ input can be used for device selection, and the $\overline{OE}$ input can be used to avoid bus conflicts so that outputs can be 'OR'ed together when using a multiplexed or bi-directional bus.

Other system-oriented features include fully TTL compatible inputs and outputs. The MK38000 operates from a single +5 volt power supply. It is packaged in the industry standard 28-pin Dual In-line Package. Pin 27 may be a logical don't care in order to maintain compatiblity with RAMs that use this pin as a write enable ($\overline{WE}$) control function.

Any application requiring a high performance, high bit density ROM can be satisfied by the MK38000. This device is ideally suited for 8-bit microprocessor systems, such as those utilizing the MK3880. It can offer significant cost advantages over PROM.

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -0.5 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.50	5.0	5.50	V	
V_{IL}	Input Logic "0" Voltage	-0.3		0.8	V	8
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

($V_{CC} = 5\ V \pm 10\%$) ($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	V_{CC} Power Supply Current (Active)		50	90	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		25	35	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	10	μA	2
V_{OL}	Output Logic "0" Voltage @ $I_{OUT} = 4$ mA			0.4	V	
V_{OH}	Output Logic "1" Voltage @ $I_{OUT} = -1$ mA	2.4			V	

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	250		ns	
t_{AA}	Address Access Time		250	ns	
t_{CEA}	$\overline{CE}$ Access Time		250	ns	
t_{CEZ}	Chip Enable Data Off Time		40	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		ns	
t_{OEA}	Output Enable Access Time		50	ns	
t_{OEZ}	Output Enable Data Off Time		40	ns	
t_{OH}	Output Hold from Address Change	5		ns	

III

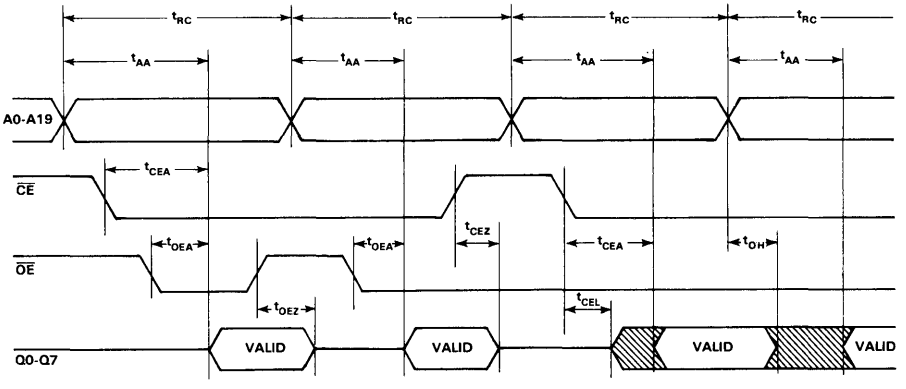
CAPACITANCE

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5		pF	
C_O	Output Capacitance	7		pF	5

TIMING DIAGRAM

Figure 3

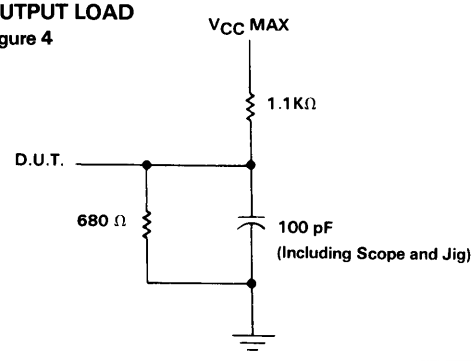


NOTES:

1. All voltages referenced to GND.
2. Measured with 0.4 V ≤ V_O ≤ 5.0 V outputs deselected and V_{CC} = 5 V.
3. V_{IN} = 0 V to V_{CC} (max).
4. Input and output timing reference levels are at 1.5 V for inputs and .8 and 2.0 for outputs.
5. Measured with outputs open during valid cycles.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.
7. $\overline{CE}$ at V_{IH}.
8. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 10 ns pulse width.
9. Measured with a load as shown in Figure 4.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.
11. A_{14} pin out must be defined with ROM code. If a connection is made to the logical don't care pin, the voltage applied must be within the "Absolute Maximum Ratings".

OUTPUT LOAD

Figure 4



OPERATION

The MK38000 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A low level at the $\overline{CE}$ input powers up the memory for an active cycle. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}) or output enable deselect time (t_{OEZ}), the output buffers will go to a high impedance state.

MK38000 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see Table 1). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc. As an example, EPROM #1 would start with address space 0000 and go to 1FFF for an 8K x 8 device. EPROM #2 would then start at address space 2000 and so on. A total of four 8K x 8 devices would be required to totally describe the address space of the 32K x 8 MK38000.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

BYTEWYDE is a trademark of Mostek Corporation

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2732	8
2764	4
27128	2

GUIDELINES FOR SUBMITTING AND VERIFYING CUSTOMER ROM PATTERNS

ROM PROGRAMMING GUIDE

It has always been Mostek's policy to service its customers ROM needs in the most efficient way possible. In continuing with this effort, Mostek has revised its ROM procedure to better facilitate the market we serve. This new ROM programming guide and information form will insure that all pertinent information is received with the purchase order. This will reduce the unnecessary delays which develop when sufficient information is not available.

DESCRIPTION OF ROM FORM

The first part of the ROM programming form is concerned with providing all necessary customer information to Mostek. This will simplify any correspondence which may be necessary to complete the order in question.

The ROM generic type simply indicates the ROM series the customer wishes to purchase. This includes the following Mostek series.

MK34000 Series
MK36000 Series
MK37000 Series
MK38000 Series

PACKAGE TYPE

The package type must be included on both the ROM form and the purchase order to prevent parts being produced in the wrong package. Currently, all prototypes and any follow-on quantities built in Dallas will be ceramic. Remember: P = Ceramic, N = Plastic, J = Cerdip.

CUSTOMER NUMBERS

In the event the customer assigns a part number to the Mostek ROM selected, this number should be entered on the ROM form. This number will simplify any communication which may be necessary between the customer and Mostek.

SPECIAL BRANDING

Special branding of Mostek ROMs is possible if the instructions are indicated on the ROM programming form. But due to space and printing limitations, any special branding desired must be limited to 12 characters on one line.

CUSTOMER SPECIFICATIONS

If the customer desires different specifications for the ROM selected than appears on the appropriate Mostek data sheet; it is imperative that these specification changes be well documented and sent to Mostek as early as possible. This is important because any specification change must be reviewed and accepted by Mostek before the ROM order can be processed.

ROM DATA

Mostek will accept a number of media and formats for the inputting of programming data. This flexibility will make it easy for a customer to have his ROM order processed as quickly as possible. The following table shows the media that can be most easily processed by Mostek. When filling out the ROM programming form, check the appropriate block under pattern media.

PATTERN MEDIA

ROMs/PROMs: On Mostek's ROMs of 16K bit and larger density, PROMs of the 2716, 2732, or 2764 type or pin compatible ROMs may be submitted for the ROM contents. They must, however, be accompanied by the information required for the Mostek ROM type in written form. Each PROM or ROM submitted must also be clearly marked so that no question arises as to its starting memory location. (See ROM Programming Form on last page).

VERIFICATION MEDIA

For pattern verification, Mostek will supply a printout and reprogrammed PROMs or magnetic tape.

To insure rapid turnaround of data verification information, acceptable media should be used as outlined in the table. If another method is desired, contact Mostek so that all arrangements can be made and an accurate schedule can be generated. Quick turnaround of verification information cannot be guaranteed in cases where new software has to be developed. Remember, when filling out the ROM programming form, check the appropriate block under verification media.

HOW THE PROGRAM WORKS

Mostek's ROM program is designed for maximum safety with two verification steps that limit the liability of both the

customer and Mostek. However, if circumstances dictate, Mostek is flexible enough to vary its procedures to better serve its customers.

PATTERN VERIFICATION

Upon receipt of the ROM programming information form and the ROM input data, Mostek engineering will re-generate the pattern data for customer verification. At this point the only customer liability is a nominal data charge in the event of a pattern change. Following customer verification, Mostek begins prototype production. Customer is now liable for mask charge and minimum order quantity work in process.

The verification step can be waived so that prototype production begins immediately upon receipt of the input data. The time savings is the time for Mostek engineering to generate verification plus the time necessary for the customer to receive and verify the data. This savings is usually less than two weeks. If data verification is waived, the customer is liable for the mask charge plus the minimum order quantity work-in-process material.

PROTOTYPE VERIFICATION

The second verification step in Mostek's ROM program is that of prototype verification. The prototype quantity is usually 25 parts which are considered part of the order quantity for billing purposes. After the customer has verified the prototype, in writing, as being correct, Mostek will proceed with the production of the total remaining order.

The prototype verification step can also be waived and Mostek will immediately begin production instead of prototyping. The time savings gained from waiving prototype verification is usually 5-6 weeks. If prototype verification is waived, the customer is liable for the mask charge plus all work-in-process material. If only prototype verification is waived Mostek guaranties ROM data to agree with data verified by customer.

WAIVERS OF VERIFICATION

Arrangements must be worked out with Mostek prior to committing deliveries based on verification waivers. If an order is accepted by Mostek waiving pattern verification, the quoted cycle time begins upon receipt of the input data and only a small quantity of parts will be produced as prototypes. If Mostek accepts an order waiving prototype verification, the quoted cycle time will begin upon notification of pattern verification and placement of order.

GENERAL INFORMATION

Production capacity cannot be reserved without written verification in house and a purchase order. Therefore any quotes for delivery will be subject to change until a purchase order is obtained.

Limited quantities of parts are usually available from the Mostek Dallas assembly facility shortly after prototype shipments, but prior to standard follow on production. These units will require an expedite adder in addition to the standard price.

The appropriate Mostek price sheet contains information on order minimums and price adders.

ACCEPTABLE MEDIA

Table 1

MK Type	ROM	PROM	Magnetic Tape
MK34000P/N/J	X	X	X
MK36000P/N/J	X	X	X
MK37000P/N/J	X	X	X
MK38000P/N/J	X	X	X

READ ONLY MEMORIES

Table 2

Device	Organization	Logic	Number Bits	Access	Supply Voltages		Power Dis (mW) Max	Package		BYTEWYDE Pinout
					V_{CC}	V_{SS}		Type	Pins	
MK34000	2048x8	Static	16384	350 ns	+5	0	330	P/N/J	24	Yes
MK36000	8192x8	Dynamic	65536	200 ns	+5	0	220	P/N/J	24	No
MK37000	8192x8	Dynamic	65536	200 ns	+5	0	220	P/N/J	28	Yes
MK38000	32768x8	Static	262144	150 ns	+5	0	495	P/N/J	28	Yes

ROM CROSS REFERENCE

Table 3

Mostek	AMD	NEC	Motorola	AMI	GI	Synertek	National	Signetics	Toshiba	SMC
MK34000	AM9218	μPD2316E	MCM68316E	S6831B	RO-3-9316	SY2316B	MM52116	2616	TMM334P	2316E
MK36000		μPD2364	MCM68364	S4264	RO-3-9364	SY2364	MM52164	2664A		36000
MK37000	AM9265								TMM2364P	
MK38000									TMM 23256	

ROM PROGRAMMING FORM

Customer Name _____

Address _____

City _____ State _____ Zip _____

Phone ( ) _____ Extension _____

Customer Contact _____ Title _____

Mostek Rep or Dist _____

ROM Generic Type _____	Customer Part #	Brand
(Including Pkg, Speed)	_____	_____
☐ Standard data sheet part	_____	_____
☐ Customer Spec # _____	_____	_____
Date customer spec sent	_____	_____
to Mostek _____	_____	_____
Spec review complete ☐ Yes	_____	_____

Pattern Media	Verification Media
☐ PROM type _____	☐ PROM type _____
☐ Pin Compatible ROMs - Note 1	☐ Pin Compatible ROMs - Note 1
☐ Magnetic Tape - Note 1	☐ Magnetic Tape - Note 1
☐ Other - Note 1	☐ Other - Note 1 (Note 1-Requires Factory Coordination)

Date Pattern Data Sent to Mostek _____

Does Customer Require Prototypes	Yes _____	No _____
Pattern Verification Required by Customer	Yes _____	Waived _____
Prototype Verification Required by Customer	Yes _____	Waived _____
Pattern Verification To Be Sent To	Rep _____	Customer _____

Customer signature approving waivers _____

Customer Order Number _____ Date _____

Order Quantity and Price _____

Delivery Requested/Committed Prototypes _____ Production _____

Form Completed By _____ Date _____

ADVANCE INFORMATION

64K x 16/128K x 8-BIT ROM MK3901M (P/N) SERIES

FEATURES

- ☐ Flexible control functions allow direct interface to popular microprocessor families
- ☐ x16 organization matches 16-bit microprocessors
- ☐ Optional x8 organization provided for use with 8-bit multiplexed microprocessors
- ☐ Multiplexed address and data bus reduces pin count
- ☐ Standard 28-pin DIP
- ☐ High performance

TRUTH TABLE

BHE	A_0	D_0-D_7	D_8-D_{15}	Operation
L	L	Lower Byte	Upper Byte	Word
L	H		Upper Byte	
H	L	Lower Byte		Byte
H	H	Upper Byte		Byte

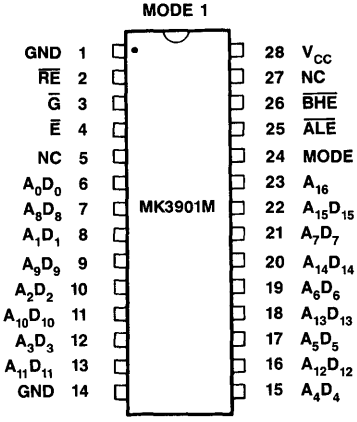
Part No.	Access Time	Cycle Time
MK3901M-15	150 ns	200 ns

DESCRIPTION

The MK3901M is a CMOS silicon gate Read Only Memory organized as either a 128K x 8 BYTEWIDE memory or a 64K x 16 WORDWIDE memory. As a state-of-the art device, the MK3901M incorporates advanced CMOS processing and circuit techniques designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

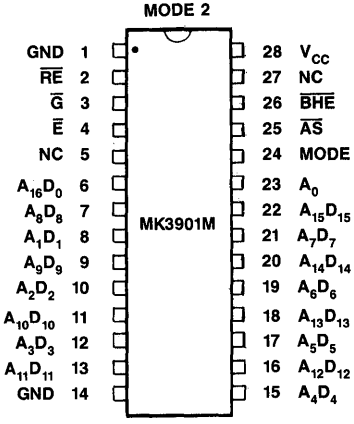
PIN CONFIGURATION - MODE 1

Figure 1



PIN CONFIGURATION - MODE 2

Figure 2



PIN NAMES

RE	Multifunction ROM Enable	ALE	Address Latch Enable
G	Output Enable	AS	Address Strobe
E	Chip Enable	BHE	Byte High Enable
A_0D_0-$A_{15}D_{15}$	Muxed Address/Data	NC	No Connection
$A_{16}D_0$-$A_{15}D_{15}$	Muxed Address/Data	V_{CC}	+5V ± 10%
A_{16}	Most Significant Address	GND	Ground
A_0	Least Significant Address	MODE	Pin/Function Select

PRELIMINARY

64K-BIT MOS READ-ONLY MEMORY
MK2364(P/N)-20,25

FEATURES

- Organized 8K x 8
- Static Operation
- Pin compatible with the 68A754 pin 64K EPROM
- Access Time = Cycle Time
- Automatic Power Down
- High performance

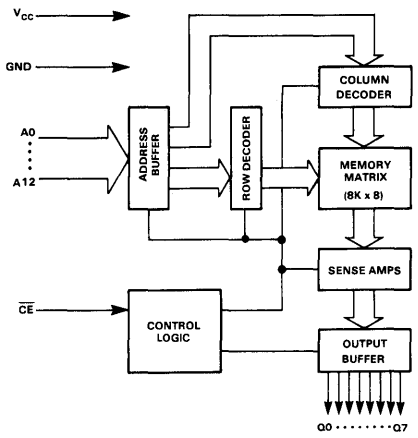
Part No.	Access Time	Cycle Time
MK2364-25	250 ns	250 ns
MK2364-20	200 ns	200 ns

DESCRIPTION

The MK2364 is an N-channel, silicon gate MOS Read Only Memory, organized as 8,192 words by 8 bits. As a state-of-the-art device, the MK2364 incorporates advanced circuit techniques, designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

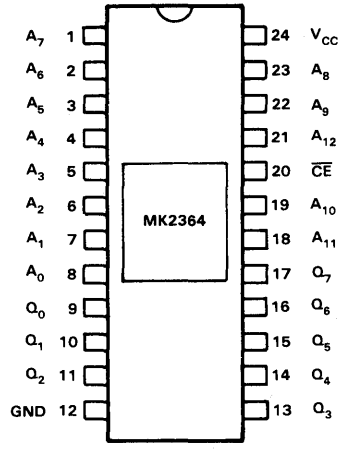
FUNCTIONAL DIAGRAM (MK2364)

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	MODE	OUTPUTS	POWER
V_{IH}	Deselect	High-Z	Standby
V_{IL}	Read	D_{OUT}	Active

PIN NAMES

A0-A12	Address	V_{CC}	+5 V
$\overline{CE}$	Chip Enable	GND	Ground
		Q0-Q7	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -0.5 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

(0°C ≤ T_A ≤ + 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.50	5.0	5.50	V	
V_{IL}	Input Logic 0 Voltage	-0.3		0.8	V	8
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP		MAX		UNITS	NOTES
			-20	-25	-20	-25		
I_{CC1}	V_{CC} Power Supply Current (Active)		65	50	100	80	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		10	7	15	12	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	0.1	10	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	0.1	10	10	μA	2
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 4 mA				0.4	0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -1 mA	2.4					V	

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	200		250		ns	
t_{AA}	Address Access Time		200		250	ns	
t_{CEA}	Chip Enable Access Time		200		250	ns	
t_{CEZ}	Chip Enable Data Off Time		35		40	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		5		ns	
t_{OH}	Output Hold from Address Change	5		5		ns	

CAPACITANCE

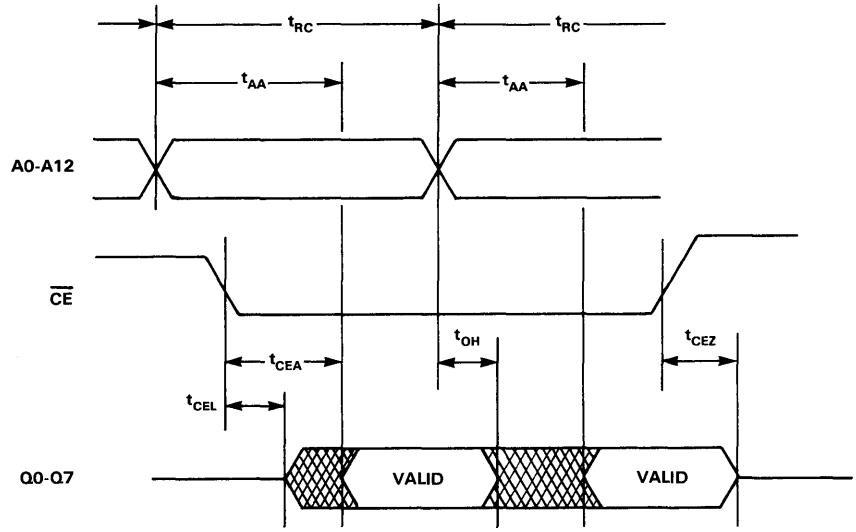
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5		pF	
C_O	Output Capacitance	7		pF	5

III

TIMING DIAGRAM

Figure 3

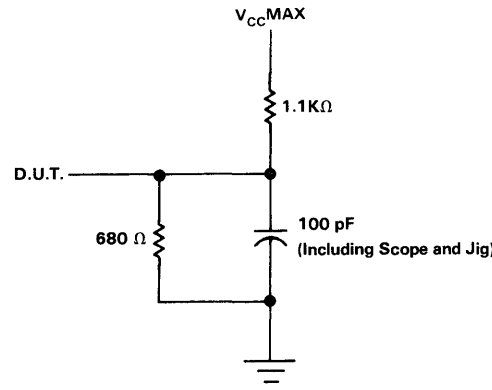


NOTES:

1. All voltages referenced to GND.
2. Measured with $0.4\ V \leq V_O \leq 5.0\ V$, outputs deselected and $V_{CC} = 5\ V$.
3. $V_{IN} = 0\ V$ to V_{CC} (max).
4. Input and output timing reference levels are at 1.5 V for inputs and 0.8 and 2.0 for outputs.
5. Measured with outputs open during valid cycles.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.
7. $\overline{CE}$ at V_{IH}.
8. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 10 ns pulse width once per cycle.
9. Measured with a load as shown in Figure 4.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.

OUTPUT LOAD

Figure 4



OPERATION

The MK2364 is controlled by the chip enable ($\overline{CE}$) input. A low level at the $\overline{CE}$ input powers up the memory for an active cycle.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}), the output buffers will go to a high impedance state.

MK2364 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification.

When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2732	2
2764	1

PRELIMINARY

64K-BIT MOS READ-ONLY MEMORY
MK2365(P/N)-20,25

FEATURES

- Organized 8K x 8
- Pin compatible with Mostek's BYTEWYDE™ Memory Family and the 2764 64K EPROM
- Access Time = Cycle Time
- Static Operation
- Automatic Power Down
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- High performance

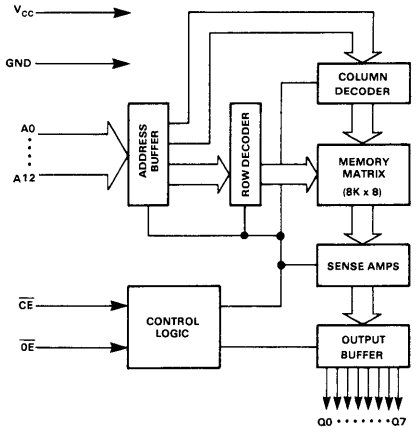
Part No.	Access Time	Cycle Time
MK2365-25	250 ns	250 ns
MK2365-20	200 ns	200 ns

DESCRIPTION

The MK2365 is an N-channel, silicon gate MOS Read Only Memory, organized as 8,192 words by 8 bits. As a state-of-the-art device, the MK2365 incorporates advanced circuit techniques, designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

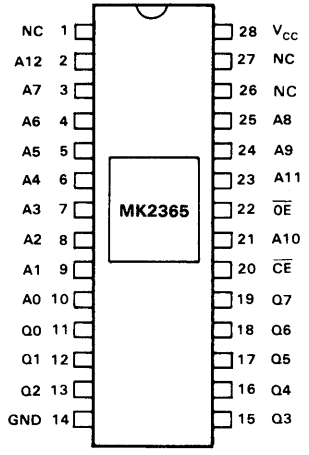
FUNCTIONAL DIAGRAM (MK2365)

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

PIN NAMES

A0-A12	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5 V
		GND	Ground
		Q0-Q7	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -0.5 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

(0°C ≤ T_A ≤ + 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.50	5.0	5.50	V	
V_{IL}	Input Logic 0 Voltage	-0.3		0.8	V	8
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP		MAX		UNITS	NOTES
			-20	-25	-20	-25		
I_{CC1}	V_{CC} Power Supply Current (Active)		65	50	100	80	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		10	7	15	12	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	0.1	10	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	0.1	10	10	μA	2
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 4 mA				0.4	0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -1 mA	2.4					V	

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	200		250		ns	
t_{AA}	Address Access Time		200		250	ns	
t_{CEA}	Chip Enable Access Time		200		250	ns	
t_{CEZ}	Chip Enable Data Off Time		35		40	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		5		ns	
t_{OEA}	Output Enable Access Time		40		50	ns	
t_{OEZ}	Output Enable Data Off Time		35		40	ns	
t_{OH}	Output Hold from Address Change	5		5		ns	

CAPACITANCE

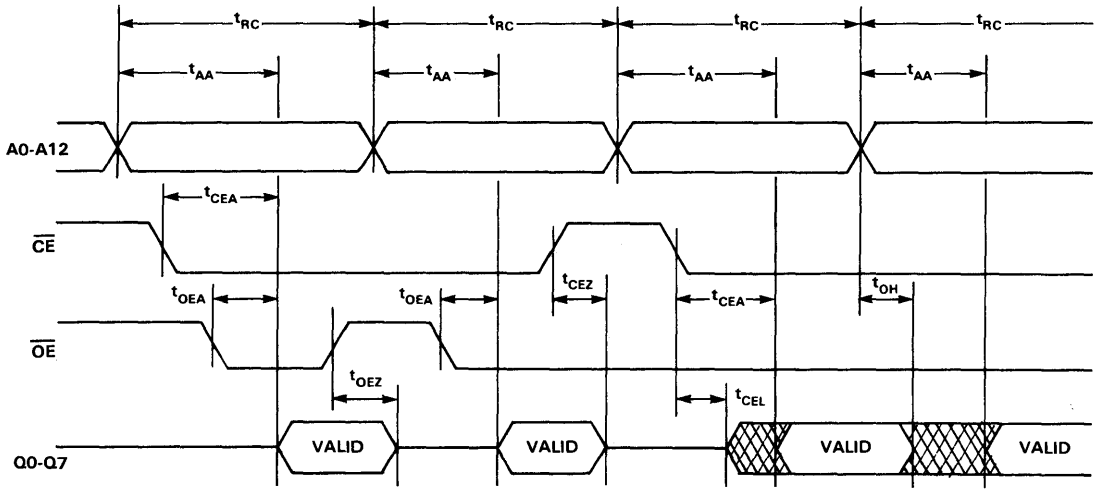
($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5		pF	
C_O	Output Capacitance	7		pF	5

III

TIMING DIAGRAM

Figure 3

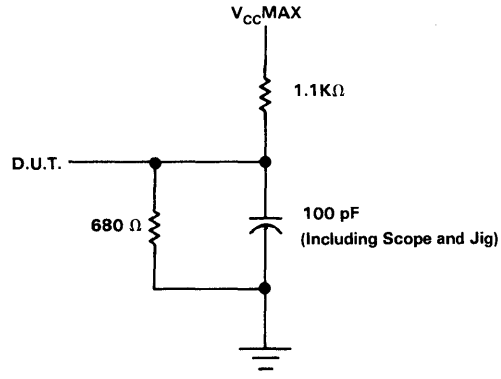


NOTES:

1. All voltages referenced to GND.
2. Measured with $0.4\ V \leq V_O \leq 5.0\ V$, outputs deselected and $V_{CC} = 5\ V$.
3. $V_{IN} = 0\ V$ to V_{CC} (max).
4. Input and output timing reference levels are at 1.5 V for inputs and 0.8 and 2.0 for outputs.
5. Measured with outputs open during valid cycles.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.
7. $\overline{CE}$ at V_{IH}.
8. Negative undershoots to a minimum of −1.5 V are allowed with a maximum of 10 ns pulse width once per cycle.
9. Measured with a load as shown in Figure 4.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.

OUTPUT LOAD

Figure 4



DESCRIPTION (continued)

As a member of the Mostek BYTEWYDE Memory Family, the MK2365 allows compatibility between RAM, ROM, and EPROM.

The output enable ($\overline{OE}$) function controls only the outputs. The $\overline{CE}$ input can be used for device selection, and the $\overline{OE}$ input can be used to avoid bus conflicts so that outputs can be ORed together when using multiplexed or bi-directional busses.

Other system oriented features include fully TTL compatible inputs and outputs. The 2365 operates from a single +5 volt power supply. It is packaged in the industry standard 28-pin DIP.

Any application requiring a high performance ROM can be satisfied by the MK2365. This device is ideally suited for 8-bit microprocessor systems such as those utilizing the

MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK2365 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A low level at the $\overline{CE}$ input powers up the memory for an active cycle. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}) or output enable deselect time (t_{OEZ}), the output buffers will go to a high impedance state.

MK2365 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2732	2
2764	1

PRELIMINARY

128K-BIT MOS READ-ONLY MEMORY
MK23128(P/N)-20,25

FEATURES

- Organized 16K x 8
- Pin compatible with Mostek's BYTEWYDE™ Memory Family
- Access Time = Cycle Time
- Static Operation
- Automatic Power Down
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control
- High performance

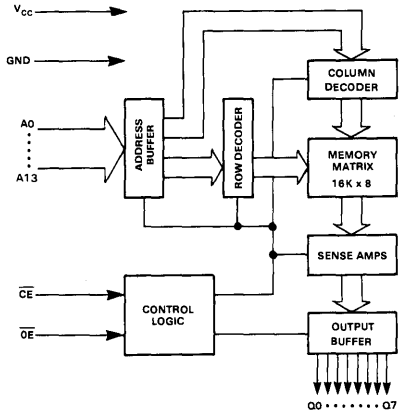
Part No.	Access Time	Cycle Time
MK23128-25	250 ns	250 ns
MK23128-20	200 ns	200 ns

DESCRIPTION

The MK23128 is an N-channel, silicon gate MOS Read Only Memory, organized as 16,384 words by 8 bits. As a state-of-the-art device, the MK23128 incorporates advanced circuit techniques, designed to provide maximum circuit density and reliability with the highest possible performance, while maintaining low power dissipation and wide operating margins.

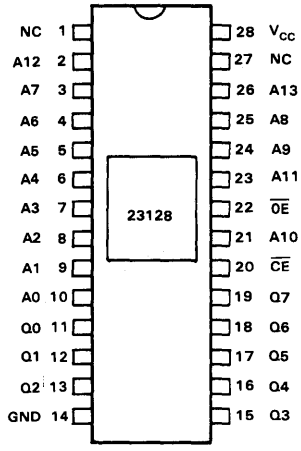
FUNCTIONAL DIAGRAM (MK23128)

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	OUTPUTS	POWER
V_{IH}	X	Deselect	High-Z	Standby
V_{IL}	V_{IH}	Inhibit	High-Z	Active
V_{IL}	V_{IL}	Read	D_{OUT}	Active

PIN NAMES

A0-A13	Address	$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable	V_{CC}	+5 V
		GND	Ground
		Q0-Q7	Data Outputs

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Terminal Relative to GND ..... -0.5 V to +7 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature—Ceramic (Ambient) ..... -65°C to +150°C
Storage Temperature—Plastic (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS[1,6]

(0°C ≤ T_A ≤ + 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Power Supply Voltage	4.50	5.0	5.50	V	
V_{IL}	Input Logic 0 Voltage	-0.3		0.8	V	8
V_{IH}	Input Logic 1 Voltage	2.0		V_{CC}	V	

DC ELECTRICAL CHARACTERISTICS[1,6]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP		MAX		UNITS	NOTES
			-20	-25	-20	-25		
I_{CC1}	V_{CC} Power Supply Current (Active)		75	60	100	80	mA	5
I_{CC2}	V_{CC} Power Supply Current (Standby)		15	10	20	15	mA	7
$I_{I(L)}$	Input Leakage Current	-10	0.1	0.1	10	10	μA	3
$I_{O(L)}$	Output Leakage Current	-10	0.1	0.1	10	10	μA	2
V_{OL}	Output Logic "0" Voltage @ I_{OUT} = 4 mA				0.4	0.4	V	
V_{OH}	Output Logic "1" Voltage @ I_{OUT} = -1 mA	2.4					V	

AC ELECTRICAL CHARACTERISTICS[1,4,6,9,10]

(V_{CC} = 5 V ± 10%) (0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	200		250		ns	
t_{AA}	Address Access Time		200		250	ns	
t_{CEA}	Chip Enable Access Time		200		250	ns	
t_{CEZ}	Chip Enable Data Off Time		35		40	ns	
t_{CEL}	Chip Enable to Data Bus Active	5		5		ns	
t_{OEA}	Output Enable Access Time		40		50	ns	
t_{OEZ}	Output Enable Data Off Time		35		40	ns	
t_{OH}	Output Hold from Address Change	5		5		ns	

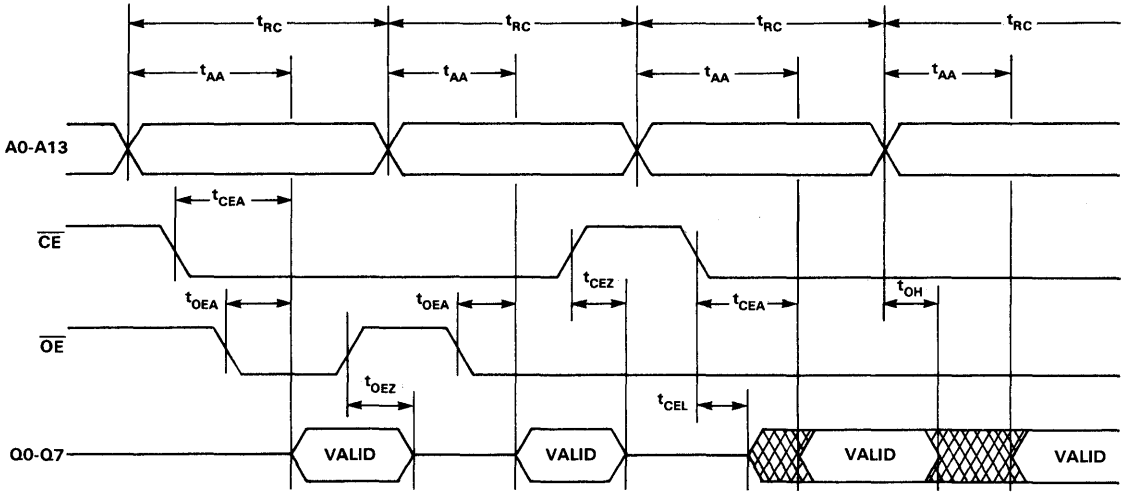
CAPACITANCE

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_I	Input Capacitance	5		pF	
C_O	Output Capacitance	7		pF	5

TIMING DIAGRAM

Figure 3

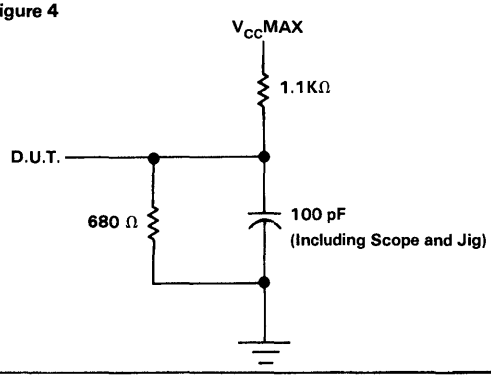


NOTES:

1. All voltages referenced to GND.
2. Measured with $0.4\ V \leq V_O \leq 5.0\ V$, outputs deselected and $V_{CC} = 5\ V$.
3. $V_{IN} = 0\ V$ to V_{CC} (max).
4. Input and output timing reference levels are at 1.5 V for inputs and 0.8 and 2.0 for outputs.
5. Measured with outputs open during valid cycles.
6. A minimum of 2 ms time delay is required after the application of V_{CC} (+5) before proper device operation is achieved.
7. $\overline{CE}$ at V_{IH}.
8. Negative undershoots to a minimum of −1.5 V are allowed with a maximum of 10 ns pulse width once per cycle.
9. Measured with a load as shown in Figure 4.
10. A.C. measurements assume transition time = 5 ns levels GND to 3 V.

OUTPUT LOAD

Figure 4



DESCRIPTION (continued)

As a member of the Mostek BYTEWYDE Memory Family, the MK23128 allows compatibility between RAM, ROM, and, EPROM. The MK23128 can be used as a pin/function density upgrade to the MK37000 and MK2365 8K x 8 bit ROMs.

The output enable $\overline{OE}$ function controls only the outputs. The $\overline{CE}$ input can be used for device selection, and the $\overline{OE}$ input can be used to avoid bus conflicts so that outputs can be ORed together when using multiplexed or bidirectional busses.

Other system oriented features include fully TTL compatible inputs and outputs. The MK23128 operates from a single +5 volt power supply. It is packaged in the industry standard 28 pin DIP.

Any application requiring a high performance bit density ROM can be satisfied by the MK23128. This is ideally suited for 8-bit microprocessor systems such as those utilizing the MK3880. It can offer significant cost advantages over PROM.

OPERATION

The MK23128 is controlled by the chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) inputs. A low level at the $\overline{CE}$ input powers up the memory for an active cycle. The output buffers, under the control of $\overline{OE}$, will become active in $\overline{CE}$ access time (t_{CEA}) if the output enable access time (t_{OEA}) requirement is met.

By maintaining valid address, the outputs will remain valid and active until either $\overline{CE}$ or $\overline{OE}$ is returned to the high state or until an address is changed. After chip deselect time (t_{CEZ}) or output enable deselect (t_{OEZ}), the output buffers will go to a high impedance state.

MK23128 ROM CODE DATA INPUT PROCEDURE

The preferred method of supplying code data to Mostek is in the form of programmed EPROMs (see table). In addition to the programmed set, Mostek requires an additional set of blank EPROMs for supplying customer code verification. When multiple EPROMs are required to describe the ROM, they shall be designated in ascending address space with the numbers 1, 2, 3, etc.

A paper printout and verification approval letter will accompany each verification EPROM set returned to the customer. Approval is considered to be accepted when the signed verification letter is returned to Mostek. The original set of EPROMs will be retained by Mostek for the duration of the prototyping process.

ACCEPTABLE EPROMs FOR CODE DATA

Table 1

EPROM	# REQUIRED
2764	2
27128	1

1984/1985 MICROELECTRONIC DATA BOOK

4096 × 1-BIT DYNAMIC RAM
MK4027(J/N)-2/3

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ 120ns access time, 320ns cycle (MK4027-1)
  150ns access time, 320ns cycle (MK4027-2)
  200ns access time, 375ns cycle (MK4027-3)
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ ECL compatible on V_{BB} power supply (−5.7V)
- ☐ Low Power: 462mW active (max)
  27mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle
- ☐ MKB version screened to MIL-STD-883

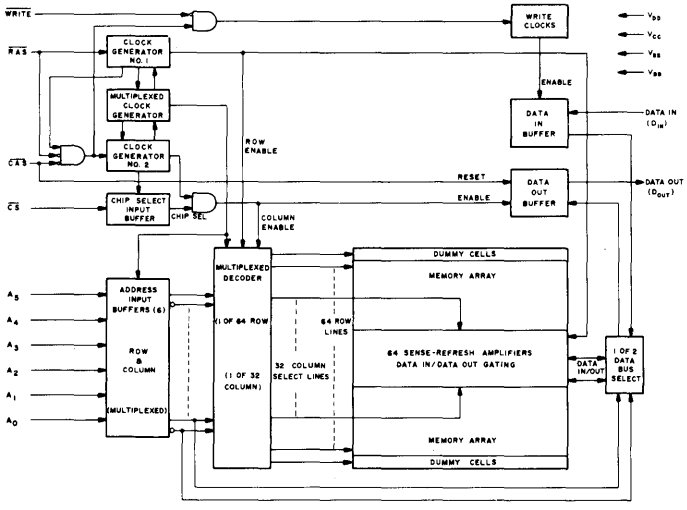
DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

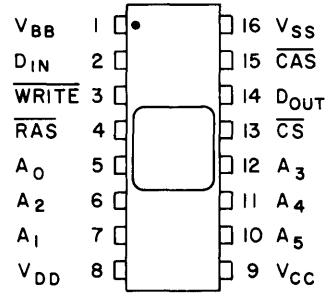
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]

($0°C \leq T_A \leq 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met. See figure 2 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate, I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{OUT} \leq +10V$.
10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS(4, 11, 17)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MK4027-2		MK4027-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{RC}	Random read or write cycle time	320		375		ns	12
t_{RWC}	Read write cycle time	320		375		ns	12
t_{RMW}	Read modify write cycle time	320		405		ns	12
t_{PC}	Page mode cycle time	170		225		ns	12
t_{RAC}	Access time from row address strobe		150		200	ns	13, 15
t_{CAC}	Access time from column address strobe		100		135	ns	14, 15
t_{OFF}	Output buffer turn-off delay		40		50	ns	
t_{RP}	Row address strobe precharge time	100		120		ns	
t_{RAS}	Row address strobe pulse width	150	10,000	200	10,000	ns	
t_{RSH}	Row address strobe hold time	100		135		ns	
t_{CAS}	Column address strobe pulse width	100		135		ns	
t_{CSH}	Column address strobe hold time	150		200		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	ns	16
t_{ASR}	Row address set-up time	0		0		ns	
t_{RAH}	Row address hold time	20		25		ns	
t_{ASC}	Column address set-up time	−10		−10		ns	
t_{CAH}	Column address hold time	45		55		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		ns	
t_{CSC}	Chip select set-up time	−10		−10		ns	
t_{CH}	Chip select hold time	45		55		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		ns	
t_T	Transition time (rise and fall)	3	35	3	50	ns	17
t_{RCS}	Read command set-up time	0		0		ns	
t_{RCH}	Read command hold time	0		0		ns	
t_{WCH}	Write command hold time	45		55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		ns	
t_{WP}	Write command pulse width	45		55		ns	
t_{RWL}	Write command to row strobe lead time	50		70		ns	
t_{CWL}	Write command to column strobe lead time	50		70		ns	
t_{DS}	Data in set-up time	0		0		ns	18
t_{DH}	Data in hold time	45		55		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		ns	
t_{CRP}	Column to row strobe precharge time	0		0		ns	
t_{CP}	Column precharge time	60		80		ns	
t_{RFSH}	Refresh period		2		2	ms	
t_{WCS}	Write command set-up time	0		0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	110		145		ns	19
t_{DOH}	Data out hold time	10		10		μs	

Notes Continued

12. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured. See figure 2 for derating curve.

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

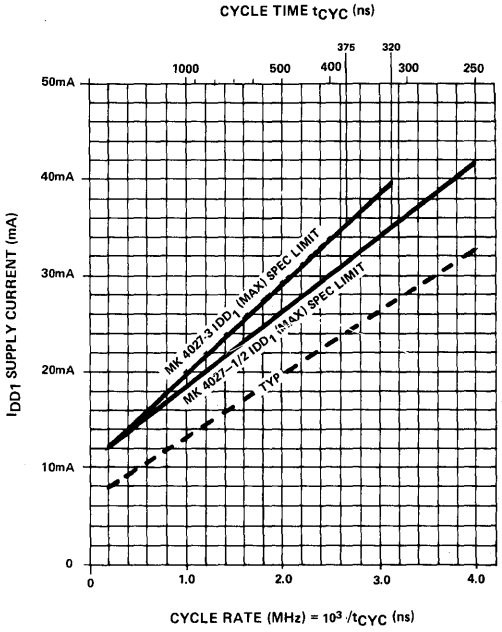


Figure 1. Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

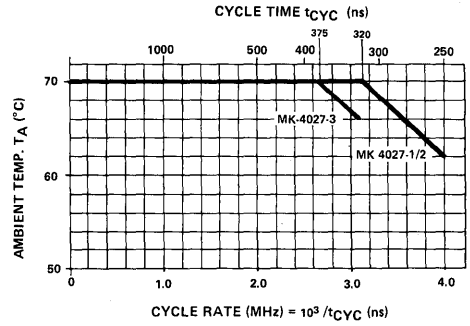
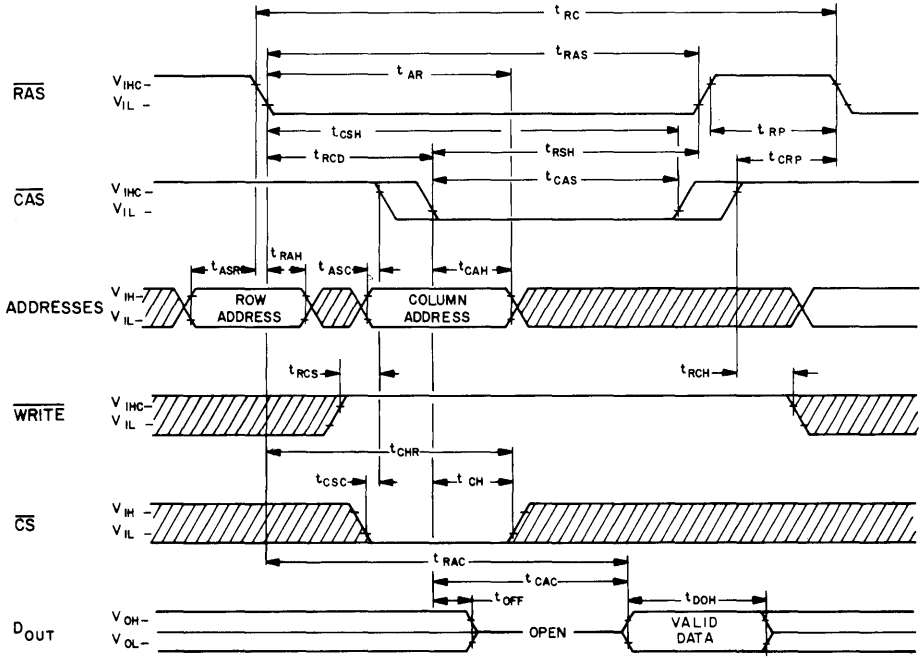
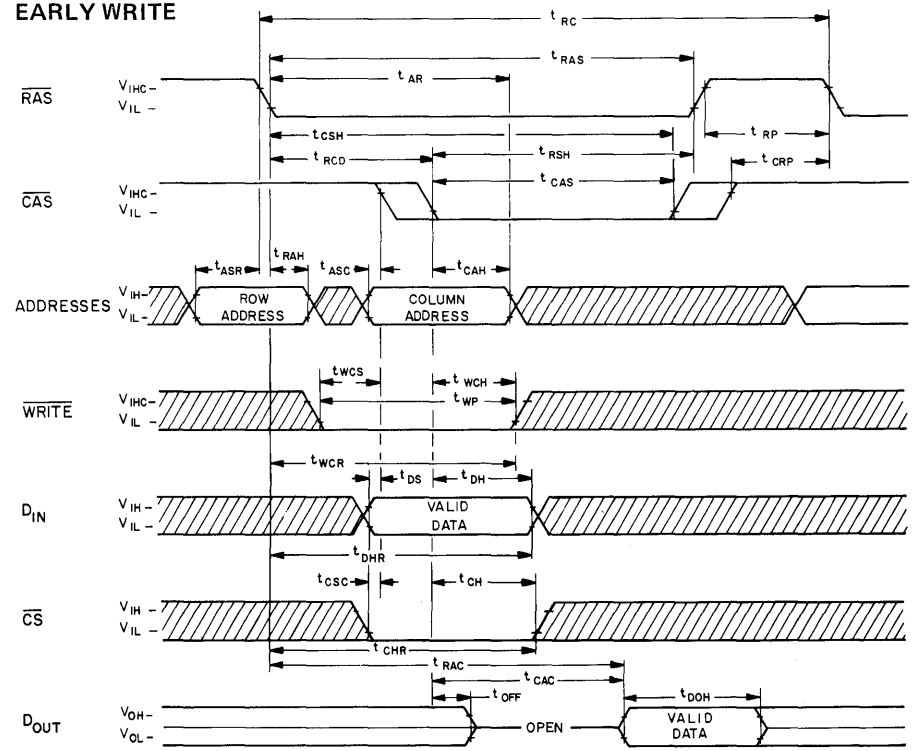


Figure 2. Maximum ambient temperature versus cycle rate for extended frequency operation.

READ CYCLE

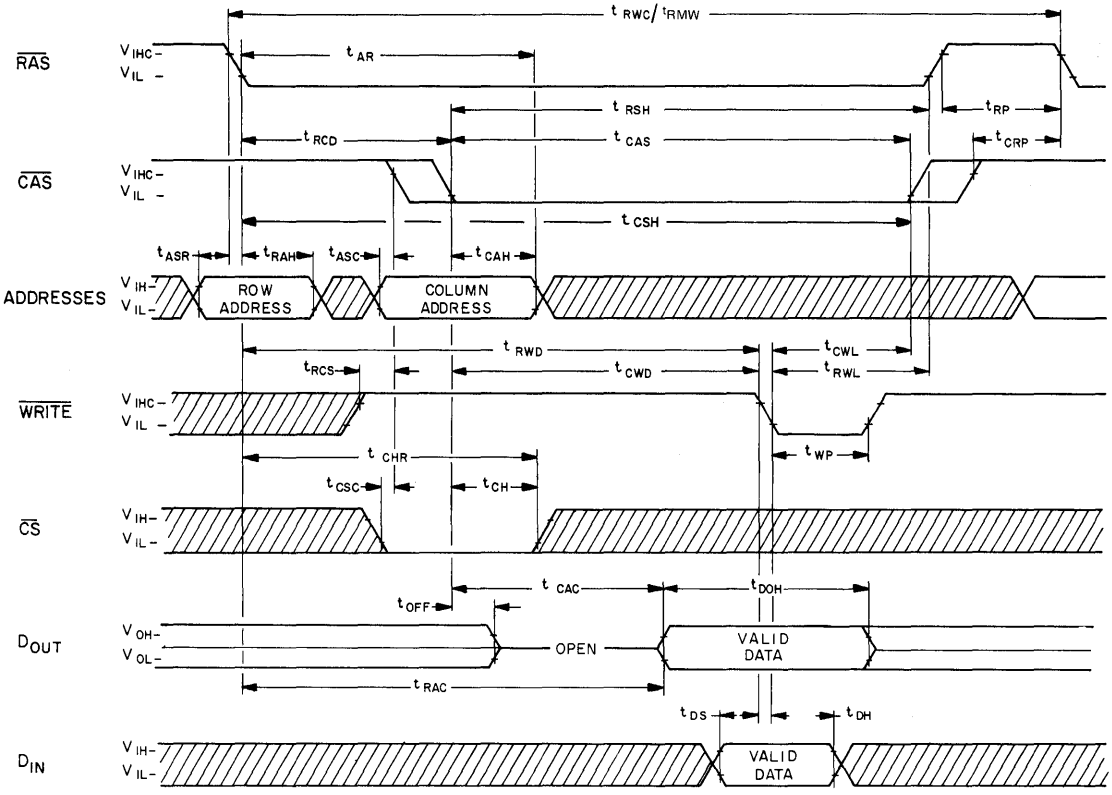


EARLY WRITE

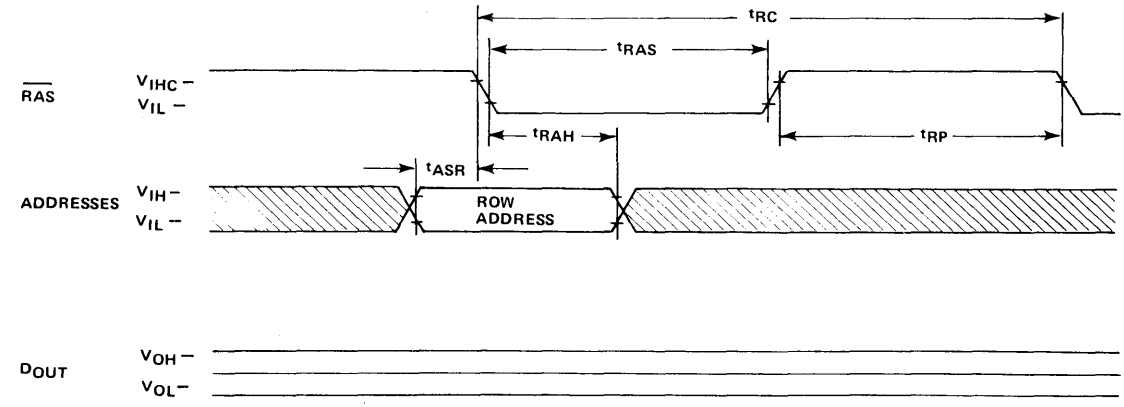


IV

READ-WRITE / READ-MODIFY-WRITE CYCLE

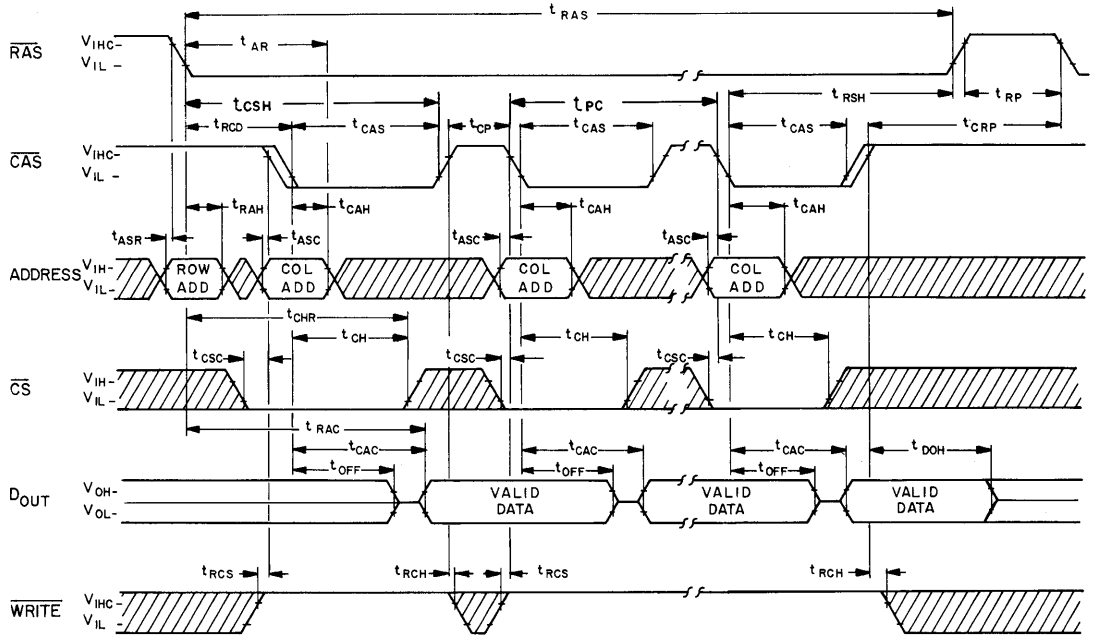


"RAS ONLY" REFRESH CYCLE

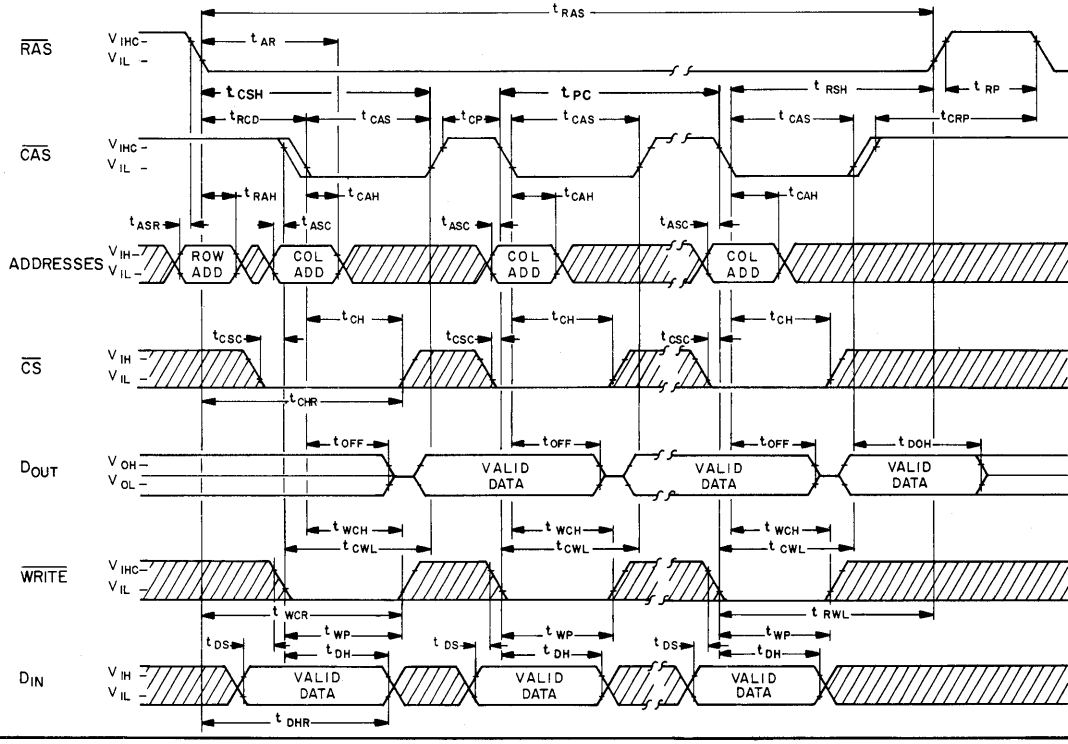


NOTE: D_{OUT} remains unchanged from previous cycle.

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 12 address bits required to decode1 of the 4096 cell locations within the MK 4027 are multiplexed onto the 6 address inputs and latched into the on-chip address latches by externally applying two negative going TTL level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 6 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 6 column address bits plus Chip Select ($\overline{CS}$) into the chip. The internal circuitry of the MK 4027 is designed to allow the column information to be externally applied to the chip before it is actually required. Because of this, the hold time requirements for the input signals associated with the Column Address Strobe are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the system designer to compensate for timing skews that may be encountered in the multiplexing operation. Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low prior to $\overline{CAS}$, the Data In is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the data input is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$.) Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT LATCH

Any change in the condition of the Data Out Latch is initiated by the $\overline{CAS}$ signal. The output buffer is not affected by memory (refresh) cycles in which only the $\overline{RAS}$ signal is applied to the MK 4027. Whenever $\overline{CAS}$ makes a negative transition, the output will go unconditionally open-circuited, independent of the state of any other input to the chip. If the cycle in progress is a read, read-modify-write, or a delayed write cycle and the chip is selected, then the output latch and buffer will again go active and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle in progress is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then at access time the output latch and buffer will contain the input data. Once having gone active, the output will remain valid until the MK 4027 receives the next $\overline{CAS}$ negative edge. Intervening refresh cycles in which a $\overline{RAS}$ is received (but no $\overline{CAS}$) will not cause valid data to be affected. Conversely, the output will assume the open-circuit state during any cycle in which the MK 4027 receives a $\overline{CAS}$ but no $\overline{RAS}$ signal (regardless of the state of any other inputs). The output will also assume the open circuit state in normal cycles (in which both $\overline{RAS}$ and $\overline{CAS}$ signals occur) if the chip is unselected.

The three-state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The output resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135 Ω typically. The output resistance to V_{SS} (logic 0 state) is 125 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4027 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row addresses within each 2 millisecond time interval. Any cycle in which a $\overline{RAS}$ signal occurs, accomplishes a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input. A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell. If, during a refresh cycle, the MK 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (where $\overline{RAS}$ is the only signal applied to the chip) are continued for extended periods, the output buffer may eventually lose proper data and go open-circuit. The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the MK 4027 is dynamic and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the whole time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle. Typically, the power is 170mW at 1 μsec cycle rate for the MK 4027 with a worse case power of less than 470mW at 320nsec cycle time. To minimize the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips. The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output). Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs. If the $\overline{RAS}$ signal is decoded and supplied only to the selected chips, then the Chip Select ($\overline{CS}$) input of all chips can be at a logic 0. The chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input. For refresh cycles, however, either the $\overline{CS}$ input of all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR'd" outputs from turning on with opposing force. Note that the MK 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4027 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page mode cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in a sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles. This feature allows the page boundary to be extended beyond the 64 column locations in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and decoding $\overline{CS}$ to select the proper block.

POWER UP

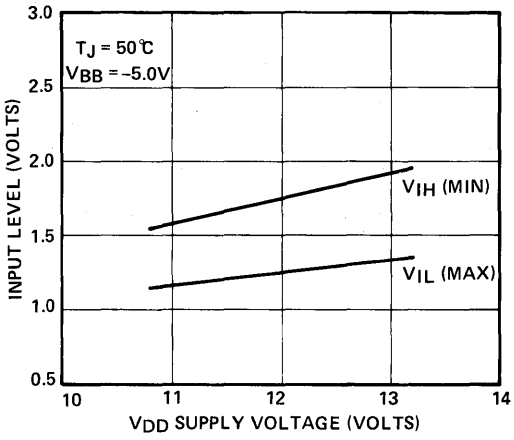
The MK 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state.

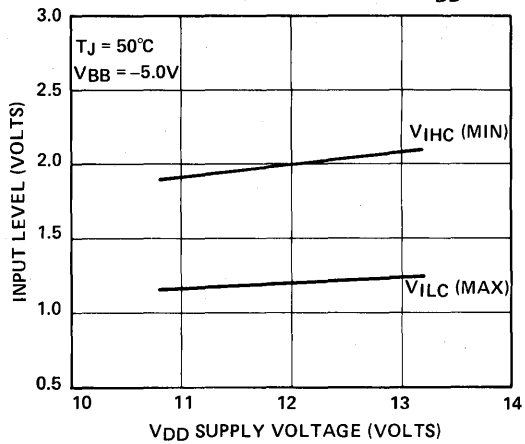
After power is applied to the device, the MK 4027 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

TYPICAL DEVICE CHARACTERISTICS

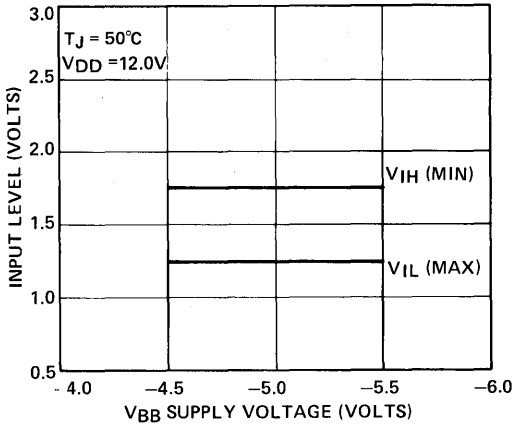
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}



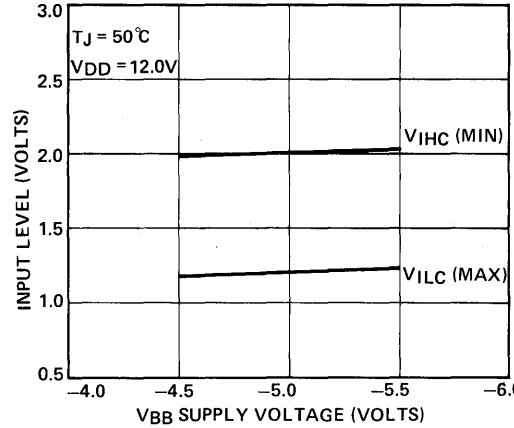
TYPICAL CLOCK INPUT LEVELS vs. V_{DD}



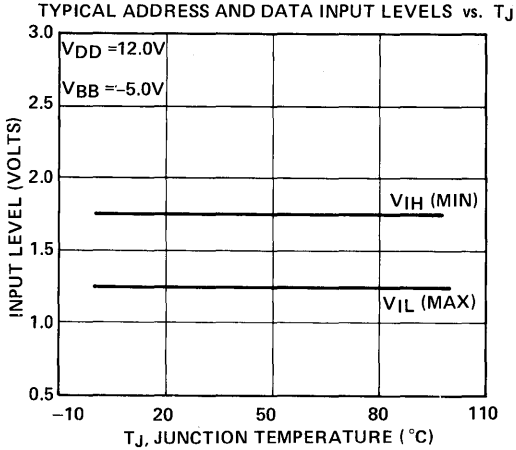
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}



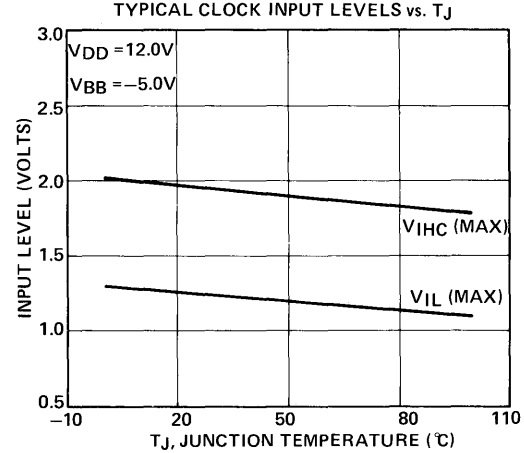
TYPICAL CLOCK INPUT LEVELS vs. V_{BB}



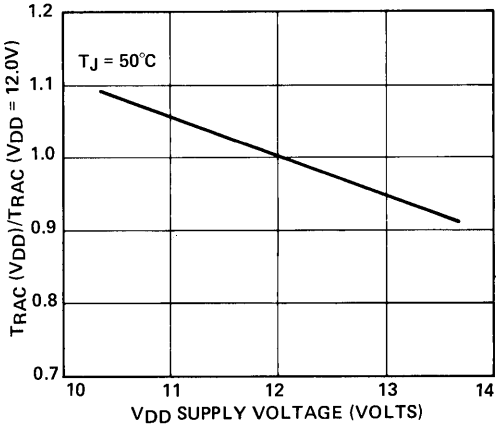
TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J



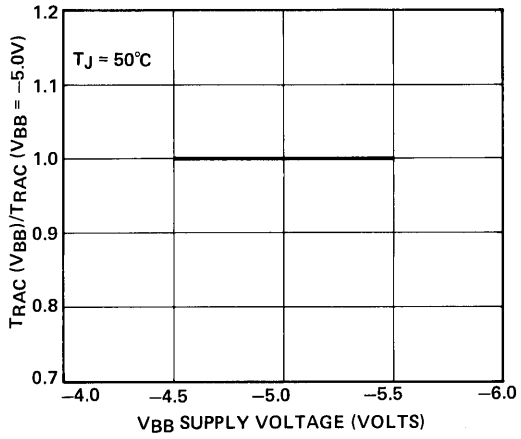
TYPICAL CLOCK INPUT LEVELS vs. T_J



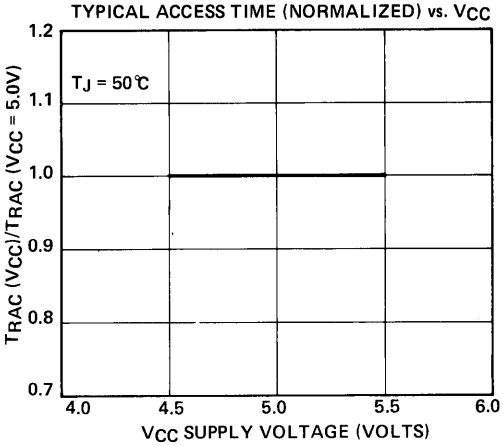
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}



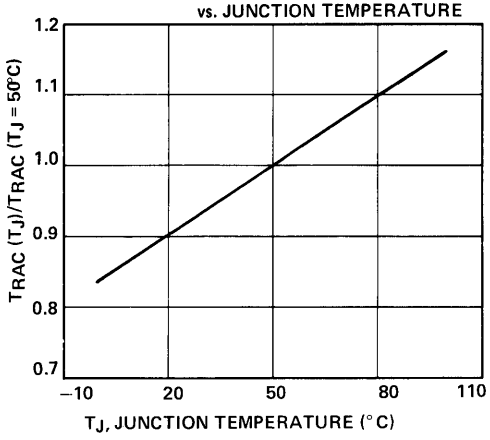
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{BB}



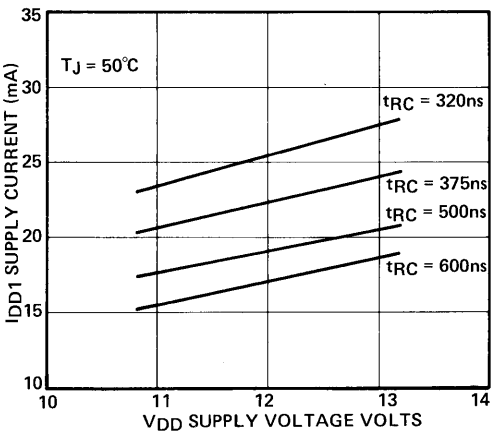
TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}



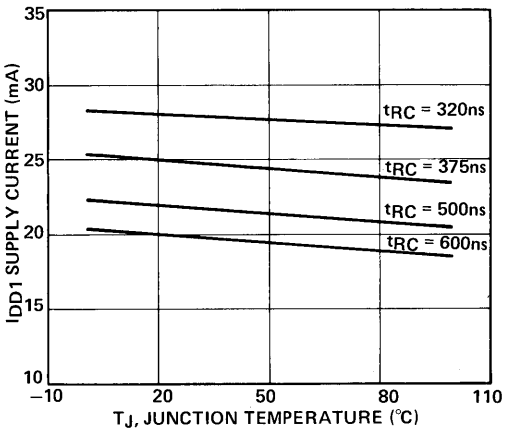
TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE



TYPICAL I_{DD1} vs. V_{DD}



TYPICAL I_{DD1} vs. JUNCTION TEMPERATURE



SUPPLEMENT

4096 × 1-BIT DYNAMIC RAM
MK4027(J/N)-4

FEATURES

- ☐ Industry standard 16-pin DIP (MK 4096) configuration
- ☐ 250ns access time, 380ns cycle
- ☐ ±10% tolerance on all supplies (+12V, ±5V)
- ☐ ECL compatible on V_{BB} power supply (−5.7V)
- ☐ Low Power: 462mW active (max)
  27mW standby (max)
- ☐ Improved performance with "gated $\overline{CAS}$", "$\overline{RAS}$ only" refresh and page mode capability
- ☐ All inputs are low capacitance and TTL compatible
- ☐ Input latches for addresses, chip select and data in
- ☐ Three-state TTL compatible output
- ☐ Output data latched and valid into next cycle
- ☐ MKB version screened to MIL-STD-883

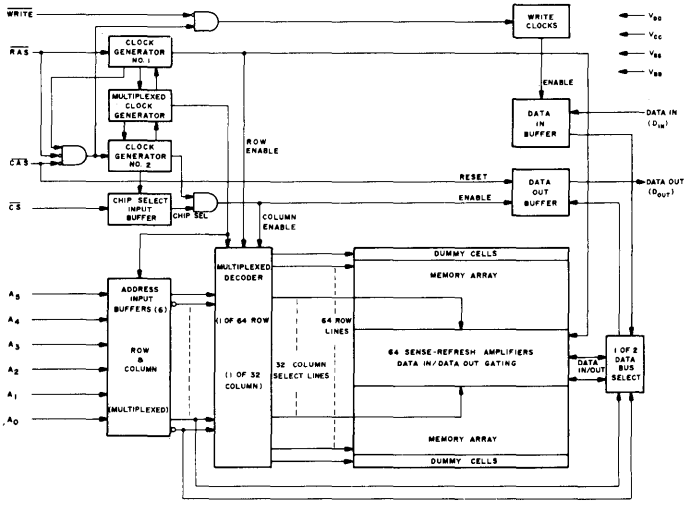
DESCRIPTION

The MK 4027 is a 4096 word by 1 bit MOS random access memory circuit fabricated with MOSTEK's N-channel silicon gate process. This process allows the MK 4027 to be a high performance state-of-the-art memory circuit that is manufacturable in high volume. The MK 4027 employs a single transistor storage cell utilizing a dynamic storage technique and dynamic control circuitry to achieve optimum performance with low power dissipation.

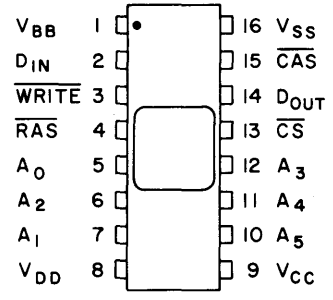
A unique multiplexing and latching technique for the address inputs permits the MK 4027 to be packaged in a standard 16-pin DIP on 0.3 in. centers. This package size provides high system-bit densities and is compatible with widely available automated testing and insertion equipment.

System oriented features include direct interfacing capability with TTL, only 6 very low capacitance address lines to drive, on-chip address and data registers which eliminates the need for interface registers, input logic levels selected to optimize noise immunity, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4027 also incorporates several flexible operating modes. In addition to the usual read and write cycles, read-modify write, page-mode, and $\overline{RAS}$-only refresh cycles are available with the MK 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA) operation.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_5	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{CS}$	CHIP SELECT
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{WRITE}$	READ/WRITE INPUT
V_{BB}	POWER (−5V)
V_{CC}	POWER (+5V)
V_{DD}	POWER (+ 12V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} relative to V_{SS} ..... −1.0V to +15V
$V_{BB}-V_{SS}$ ($V_{DD}-V_{SS} > 0$) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient)(Ceramic) ..... −65°C to + 150°C
Storage temperature (Ambient)(Plastic) ..... −55°C to + 125°C
Short Circuit Output Current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS [4]

($0°C \leq T_A \leq 70°C$) [1]

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD}	Supply Voltage	10.8	12.0	13.2	volts	2
V_{CC}	Supply Voltage	4.5V	5.0	5.5	volts	2,3
V_{SS}	Supply Voltage	0	0	0	volts	2
V_{BB}	Supply Voltage	−4.5	−5.0	−5.7	volts	2
V_{IHC}	Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7.0	volts	2
V_{IH}	Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7.0	volts	2
V_{IL}	Logic 0 Voltage, all inputs	−1.0		.8	volts	2

DC ELECTRICAL CHARACTERISTICS [4]

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%; V_{CC} = 5.0V ± 10%; V_{SS} = 0V; $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{DD1}	Average V_{DD} Power Supply Current			35	mA	5
I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	8
I_{DD3}	Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} Power Supply Current				mA	6
I_{BB}	Average V_{BB} Power Supply Current			150	μA	
$I_{I(L)}$	Input Leakage Current (any input)			10	μA	7
$I_{O(L)}$	Output Leakage Current			10	μA	8,9
V_{OH}	Output Logic 1 Voltage @ I_{OUT} = −5mA	2.4			volts	
V_{OL}	Output Logic 0 Voltage @ I_{OUT} = 3.2mA			0.4	volts	

NOTES

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$ (min).
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min). See figure 1 for I_{DD1} limits at other cycle rates.
6. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
7. All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leq V_{OUT} \leq +10V$.
10. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

11. A.C. measurements assume t_T = 5ns.
12. The specifications for tRC (min) and tRWC (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0° \leq TA \leq 70°C$) is assured.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS[4, 11, 17]

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ± 10%, V_{CC} = 5.0V ± 10%, V_{SS} = 0V, $-5.7V \leq V_{BB} \leq -4.5V$)

	PARAMETER	MK4027-4 MIN	MK4027-4 MAX	UNITS	NOTES
t_{RC}	Random read or write cycle time	380		ns	12
t_{RWC}	Read write cycle time	395		ns	12
t_{RMW}	Read modify write cycle time	470		ns	12
t_{PC}	Page mode cycle time	285		ns	12
t_{RAC}	Access time from row address strobe		250	ns	13,15
t_{CAC}	Access time from column address strobe		165	ns	14,15
t_{OFF}	Output buffer turn-off delay	0	60	ns	
t_{RP}	Row address strobe precharge time	120		ns	
t_{RAS}	Row address strobe pulse width	250	10,000	ns	
t_{RSH}	Row address strobe hold time	165		ns	
t_{CAS}	Column address strobe pulse width	165		ns	
t_{CSH}	Column address strobe hold time	250		ns	
t_{RCD}	Row to column strobe delay	35	85	ns	16
t_{ASR}	Row address set-up time	0		ns	
t_{RAH}	Row address hold time	35		ns	
t_{ASC}	Column address set-up time	-10		ns	
t_{CAH}	Column address hold time	75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	160		ns	
t_{CSC}	Chip select set-up time	-10		ns	
t_{CH}	Chip select hold time	75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	160		ns	
t_T	Transition time (rise and fall)	3	50	ns	17
t_{RCS}	Read command set-up time	0		ns	
t_{RCH}	Read command hold time	0		ns	
t_{WCH}	Write command hold time	75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	160		ns	
t_{WP}	Write command pulse width	75		ns	
t_{RWL}	Write command to row strobe lead time	85		ns	
t_{CWL}	Write command to column strobe lead time	85		ns	
t_{DS}	Data in set-up time	0		ns	18
t_{DH}	Data in hold time	75		ns	18
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	160		ns	
t_{CRP}	Column to row strobe precharge time	0		ns	
t_{CP}	Column precharge time	110		ns	
t_{RFSH}	Refresh period		2	ms	
t_{WCS}	Write command set-up time	0		ns	19
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	90		ns	19
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	175		ns	19
t_{DOH}	Date out hold time	10		μs	

Notes Continued

13. Assumes that $t_{RCD} \leq t_{RCD}$ (max).

14. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

15. Measured with a load circuit equivalent to 2 TTL loads and 100pF

16. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

17. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

18. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

19. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

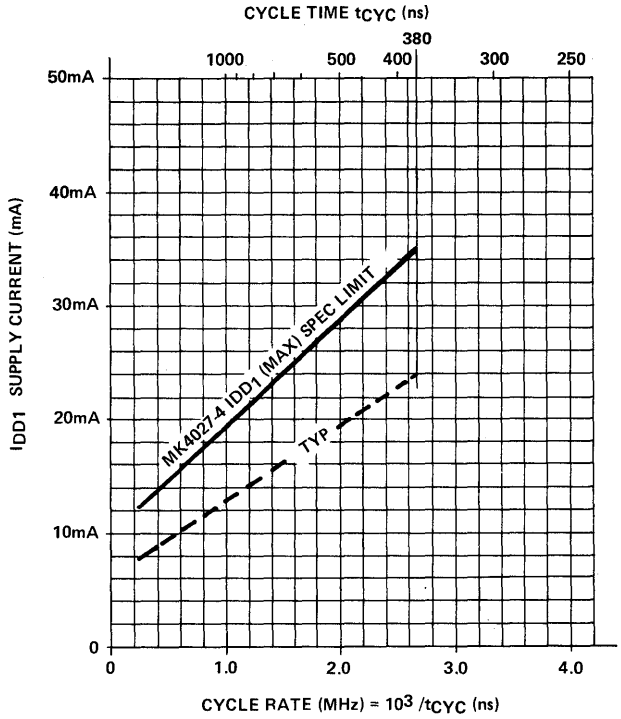
AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V ; −5.7V ≤ V_{BB} ≤ −4.5V)

	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	10
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	10
C_O	Output Capacitance (D_{OUT})	5	7	pF	8,10

MAXIMUM I_{DD1} vs. CYCLE RATE FOR DEVICE OPERATION AT EXTENDED FREQUENCIES

Figure 1



SUPPLEMENT - To be used in conjunction with MK4027(J/N)-1/2/3 data sheet.

16,384 × 1-BIT DYNAMIC RAM
MK4116(J/N/E)-2/3

FEATURES

- ☐ Recognized industry standard 16-pin configuration from MOSTEK
- ☐ 150ns access time, 320ns cycle (MK 4116-2)
  200ns access time, 375ns cycle (MK 4116-3)
- ☐ ± 10% tolerance on all power supplies (+12V, ±5V)
- ☐ Low power: 462mW active, 20mW standby (max)
- ☐ Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- ☐ Common I/O capability using "early write" operation
- ☐ Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-mode capability
- ☐ All inputs TTL compatible,low capacitance, and protected against static charge
- ☐ 128 refresh cycles
- ☐ ECL compatible on VBB power supply (-5.7V)
- ☐ MKB version screened to MIL-STD-883
- ☐ JAN version available to MIL-M-38510/240

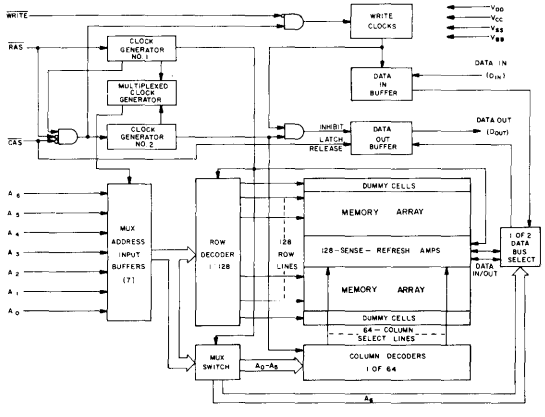
DESCRIPTION

The MK 4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK 4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK 4027 (4K RAM).

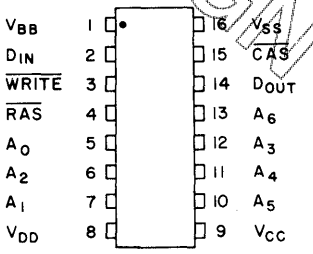
The technology used to fabricate the MK 4116 is MOSTEK's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK 4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMS) permits the MK 4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_6	ADDRESS INPUTS	$\overline{WRITE}$	READ/WRITE INPUT
$\overline{CAS}$	COLUMN ADDRESS STROBE	V_{BB}	POWER (−5V)
D_{IN}	DATA IN	V_{CC}	POWER (+5V)
D_{OUT}	DATA OUT	V_{DD}	POWER (+12V)
$\overline{RAS}$	ROW ADDRESS STROBE	V_{SS}	GROUND

Available per MIL-STD-883 B. Mostek is qualified per JM-38150 Class B.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... −0.5V to +20V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... −1.0V to +15.0V
V_{BB}−V_{SS} (V_{DD}−V_{SS} ≥0V) 0V
Operating temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage temperature (Ambient) Ceramic ..... −55°C to + 150°C
Storage temperature, (Ambient) Plastic ..... −55°C to +125°C
Short circuit output current 50mA
Power dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

($0°C \leq T_A \leq 70°C$)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	10.8 4.5 0 −4.5	12.0 5.0 0 −5.0	13.2 5.5 0 −5.7	Volts Volts Volts Volts	2 2,3 2 2
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	–	7.0	Volts	2
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.2	–	7.0	Volts	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0	–	.8	Volts	2

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%; −5.7V ≤ V_{BB} ≤ −4.5V; V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min	I_{DD1} I_{CC1} I_{BB1}		35 200	mA µA	4 5
STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	I_{DD2} I_{CC2} I_{BB2}	 −10 	1.5 10 100	mA µA µA	
REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = t_{RC} Min	I_{DD3} I_{CC3} I_{BB3}	 −10 	25 10 200	mA µA µA	4
PAGE MODE CURRENT Average power supply current, page-mode operation ($\overline{RAS}$ =V_{IL}, $\overline{CAS}$ cycling; t_{PC} = t_{PC} Min	I_{DD4} I_{CC4} I_{BB4}		27 200	mA µA	4 5
INPUT LEAKAGE Input leakage current, any input (V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7.0V, all other pins not under test = 0 volts)	$I_{I(L)}$	−10	10	µA	
OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V)	$I_{O(L)}$	−10	10	µA	
OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = −5mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	V_{OH} V_{OL}	2.4 	 0.4	Volts Volts	3

NOTES:

1. T_A is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met. See figure 1 for derating curve.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See figures 2,3, and 4 for I_{DD} limits at other cycle rates.
5. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (6,7,8)

($0°C \leq T_A \leq 70°C$)[1] (V_{DD} = 12.0V ±10%; V_{CC} = 5.0V ±10%, V_{SS} = 0V, V_{BB} = **-5.7V ≤ VBB ≤ -4.5V**)

PARAMETER	SYMBOL	MK 4116-2		MK 4116-3		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	320		375		ns	9
Read-write cycle time	t_{RWC}	320		375		ns	9
Read modify write cycle time	t_{RMW}	320		405		ns	9
Page mode cycle time	t_{PC}	170		225		ns	9
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	10,12
Access time from $\overline{CAS}$	t_{CAC}		100		135	ns	11,12
Output buffer turn-off delay	t_{OFF}	0	40	0	50	ns	13
Transition time (rise and fall)	t_T	3	35	3	50	ns	8
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		135		ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10,000	135	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	65	ns	14
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		ns	
Row Address set-up time	t_{ASR}	0		0		ns	
Row Address hold time	t_{RAH}	20		25		ns	
Column Address set-up time	t_{ASC}	−10		−10		ns	
Column Address hold time	t_{CAH}	45		55		ns	
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	95		120		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time	t_{RCH}	0		0		ns	
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	95		120		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		70		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	50		70		ns	
Data-in set-up time	t_{DS}	0		0		ns	15
Data-in hold time	t_{DH}	45		55		ns	15
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	95		120		ns	
$\overline{CAS}$ precharge time (for page-mode cycle only)	t_{CP}	60		80		ns	
Refresh period	t_{REF}		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	-20		-20		ns	16
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	60		80		ns	16
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	110		145		ns	16

NOTES (Continued)

6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume tT = 5ns.
8. VIHC (min) or VIH (min) and VIL (max) are reference levels for measuring timing of input signals. Also transition times are measured between VIHC or VIH and VIL.
9. The specifications for tRC (min) tRMW (min) and tRWC (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq TA \leq 70°C$) is assured
10. Assumes that $tRCD \leq tRCD$ (Max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
11. Assumes that tRCD (max).
12. Measured with a load equivalent to 2 TTL loads and 100pF.
13. tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the tRCD (max) limit insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.
15. These parameters are referenced to CAS leading edge in early write cycles and to WRITE leading edge in delayed write or read-modify-write cycles.
16. tWCS, tCWD and tRWD are restrictive operating parameters in read write and read modify write cycles only. If $tWCS \geq tWCS$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $tCWD \geq tCWD$ (min) and $tRWD \geq tRWD$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = 1\frac{\Delta t}{\Delta V}$ with $\Delta V = 3$ volts and power supplies at nominal levels.
18. $\overline{CAS}$ = VIHC to disable DOUT.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{DD} = 12.0V ± 10%; V_{SS} = 0V; V_{BB} = -5.7V ≤ VBB ≤ -4.5V)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance (A_0–A_6), D_{IN}	C_{I1}	4	5	pF	17
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8	10	pF	17
Output Capacitance (D_{OUT})	C_O	5	7	pF	17,18

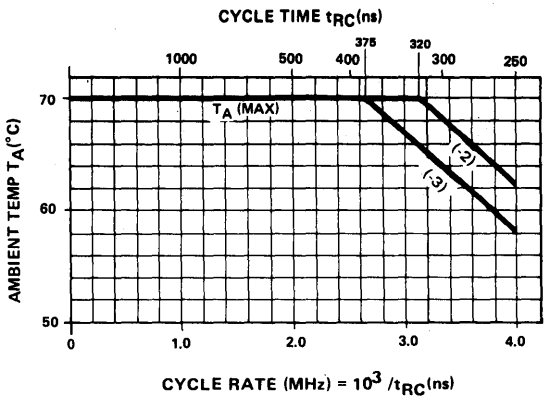


Fig. 1 Maximum ambient temperature versus cycle rate for extended frequency operation. T_A (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375ns) is determined by T_A (max)° C = 70 – 9.0 x (cycle rate MHz – 2.66) for -3. T_A (max) °C = 70 – 9.0 x cycle rate MHz – 3.125MHz) for -2 only.

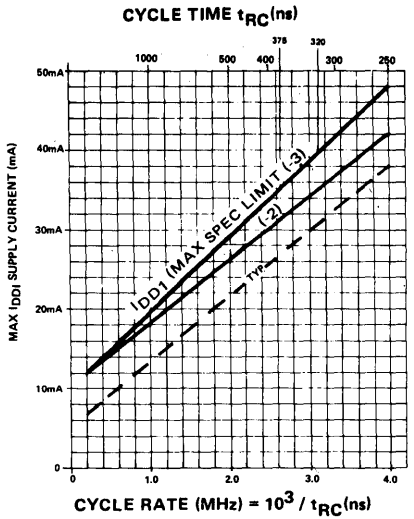


Fig. 2 Maximum I_{DD1} versus cycle rate for device operation at extended frequencies. I_{DD1} (max) curve is defined by the equation:

I_{DD1} (max) mA = 10 + 9.4 x cycle rate [MHz] for -3
I_{DD1} (max) mA = 10 + 8.0 x cycle rate [MHz] for -2

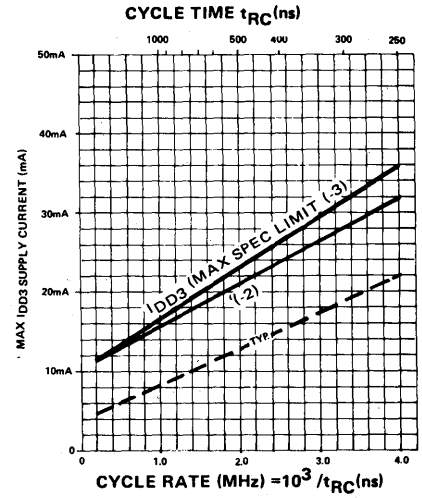


Fig. 3 Maximum I_{DD3} versus cycle rate for device operation at extended frequencies. I_{DD3} (max) curve is defined by the equation:

I_{DD3}(max) mA = 10 + 6.5 x cycle rate [MHz] for -3
I_{DD3}(max) mA = 10 + 5.5 x cycle rate [MHz] for -2

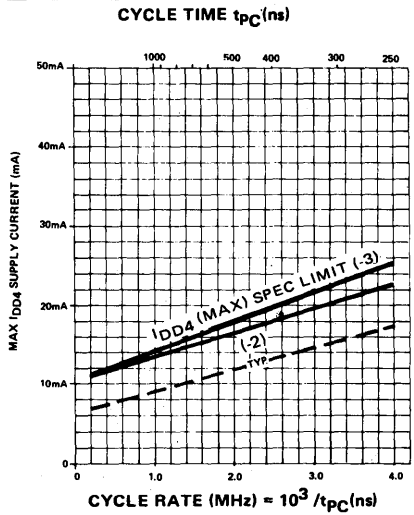
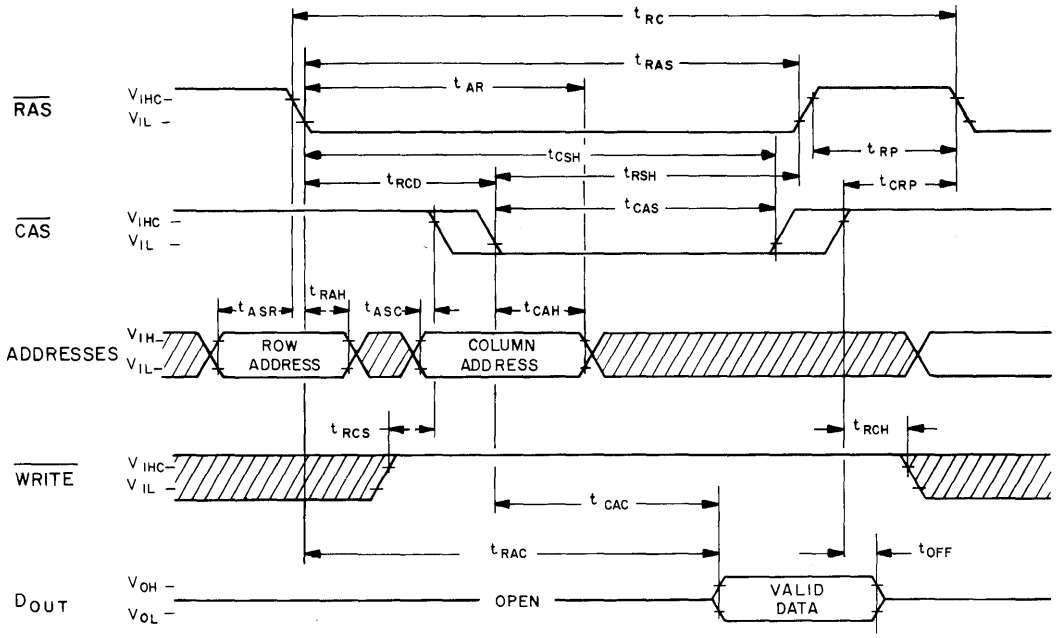


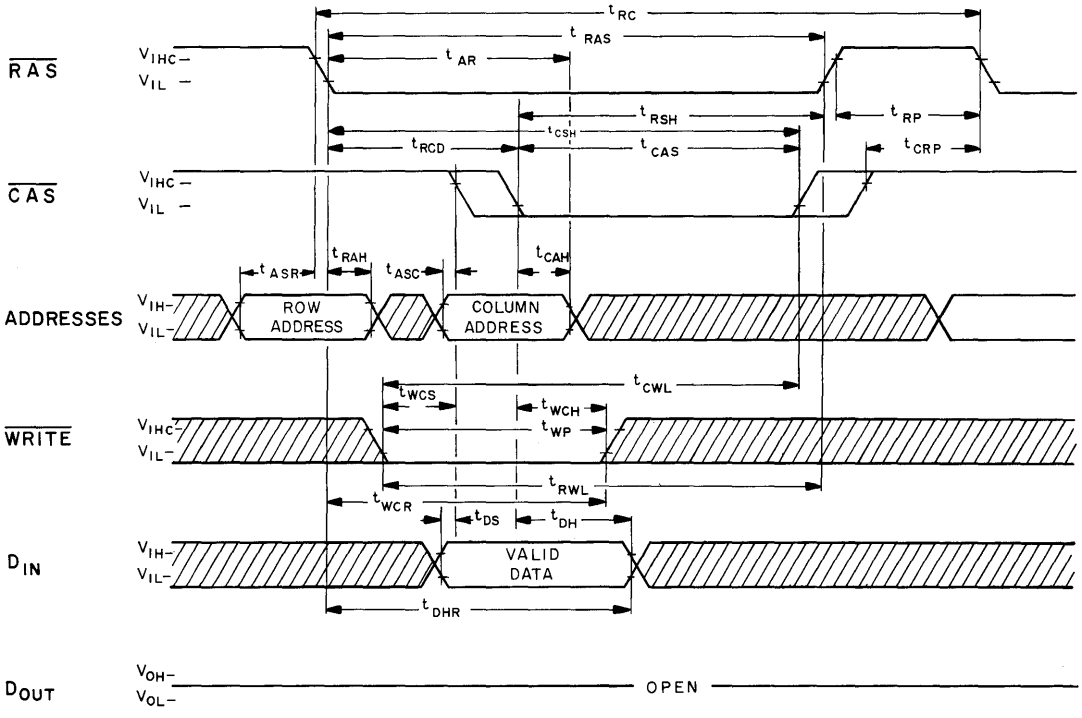
Fig. 4 Maximum I_{DD4} versus cycle rate for device operation in page mode. I_{DD4} (max) curve is defined by the equation:

I_{DD4} (max) mA = 10 + 3.75 x cycle rate [MHz] for -3
I_{DD4} (max) mA = 10 + 3.2 x cycle rate [MHz] for -2

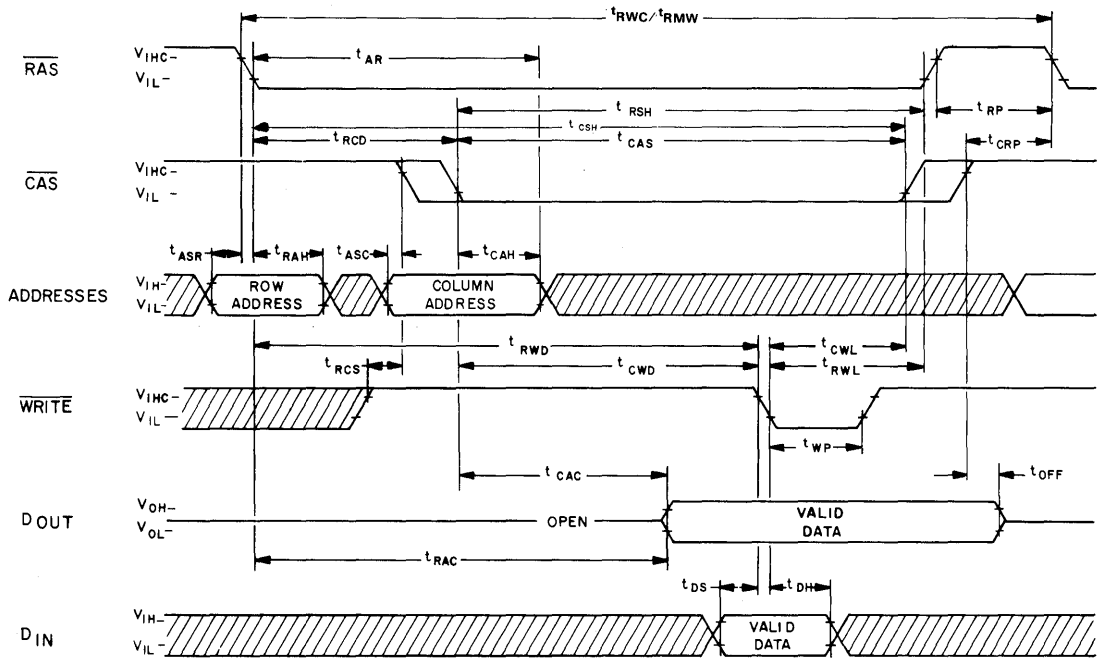
READ CYCLE



WRITE CYCLE (EARLY WRITE)

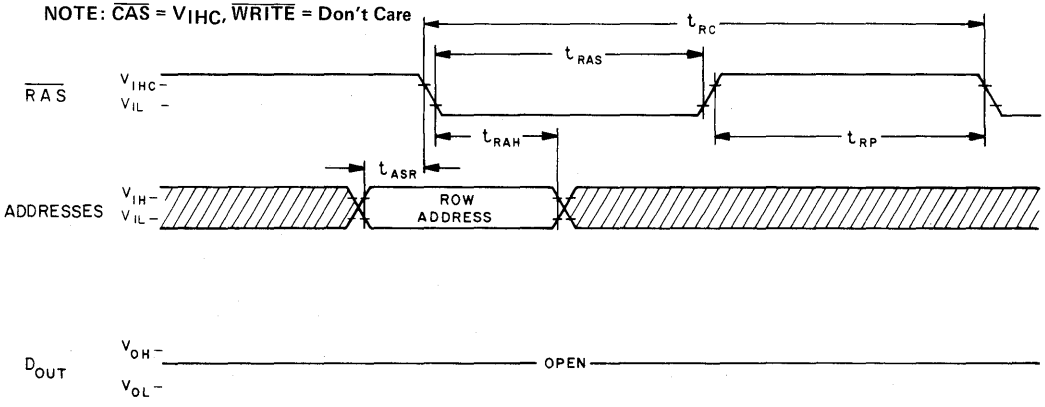


READ–WRITE/READ–MODIFY–WRITE CYCLE

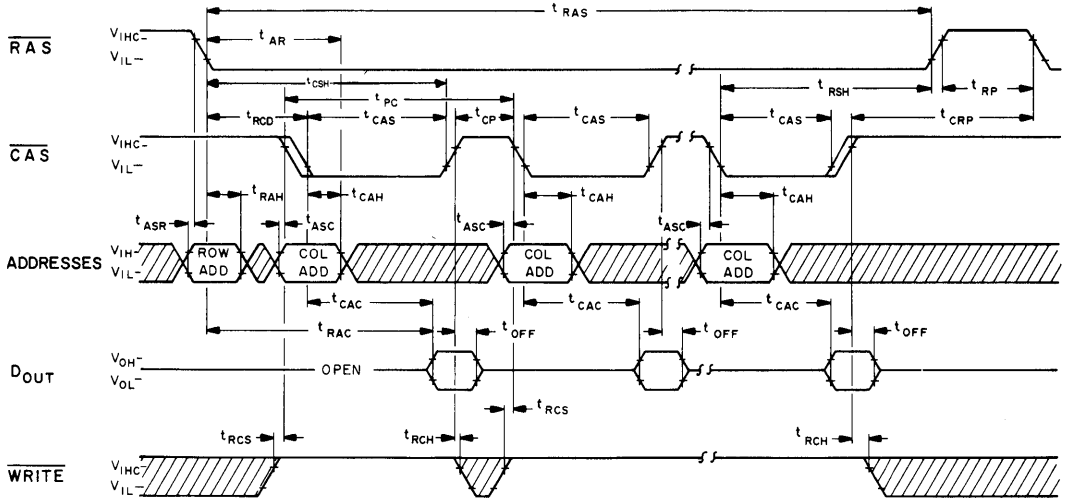


"RAS–ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

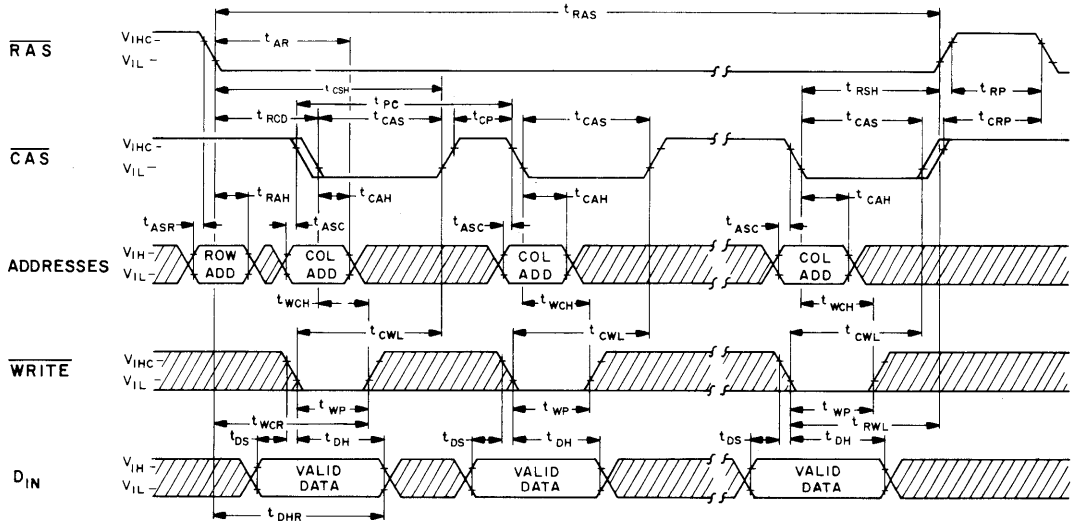


PAGE MODE READ CYCLE



IV

PAGE MODE WRITE CYCLE



DESCRIPTION (continued)

System oriented features include ± 10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The MK 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK 4116 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

Note that $\overline{CAS}$ can be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK 4116 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and access time from $\overline{RAS}$ will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, D_{IN} is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows D_{IN} referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the D_{OUT} pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. D_{OUT} will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until $\overline{CAS}$ is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.

If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the D_{OUT} pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even though data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).

This type of output operation results in some very significant system implications.

Common I/O Operation – If all write operations are handled in the "early write" mode, then D_{IN} can be connected directly to D_{OUT} for a common I/O data bus.

Data Output Control – D_{OUT} will remain valid during a read cycle from t_{CAC} until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the $\overline{RAS}/\overline{CAS}$ clock timing relationship very flexible.

Two Methods of Chip Selection – Since D_{OUT}

is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X,Y) chip select array can be realized.

Extended Page Boundary – Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column locations in a single chip. (See page-mode operation).

OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to V_{CC} for a logic 1 and a low impedance to V_{SS} for a logic 0. The effective resistance to V_{CC} (logic 1 state) is 420 Ω maximum and 135Ω typically. The resistance to V_{SS} (logic 0 state) is 95 Ω maximum and 35 Ω typically. The separate V_{CC} pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the V_{CC} pin may have power removed without affecting the MK 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

PAGE MODE OPERATION

The "Page Mode" feature of the MK 4116 allows for successive memory operations at multiple column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.

The page boundary of a single MK 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and then $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 millisecond time interval. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only refresh results in a substantial reduction in operating power. This reduction in power is reflected in the I_{DD3} specification.

POWER CONSIDERATIONS

Most of the circuitry used in the MK 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather than active duty cycle (refer to the MK 4116 current waveforms in figure 5). This current characteristic of the MK 4116 precludes inadvertent burn out of the device in the event that the clock inputs become shorted to ground due to system malfunction.

Although no particular power supply noise restriction exists other than the supply voltages remain within the specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise resulting from the transient current of the device. This insures optimum system performance and reliability. Bulk capacitance requirements are minimal since the MK 4116 draws very little steady state (DC) current.

In system applications requiring lower power dissipation, the operating frequency (cycle rate) of the MK 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be lowered in accordance with the I_{DD1} (max) spec limit curve illustrated in figure 2. NOTE: The MK 4116 family is guaranteed to have a maximum I_{DD1} requirement of 35mA @ 375ns cycle (320ns cycle for the -2) with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum Idd1 requirement of under 20mA with an ambient temperature range from 0° to 70°C.

It is possible the MK4116 family (-2 and 3 speed selections for example) at frequencies higher than specified, provided all AC operating parameters are met. Operation at shorter cycle times (<tRC min) results in higher power dissipation and, therefore, a reduction in ambient temperature is required. Refer to Figure 1 for derating curve.

NOTE: Additional power supply tolerance has been included on the VBB supply to allow direct interface capability with both -5V systems -5.2V ECL systems.

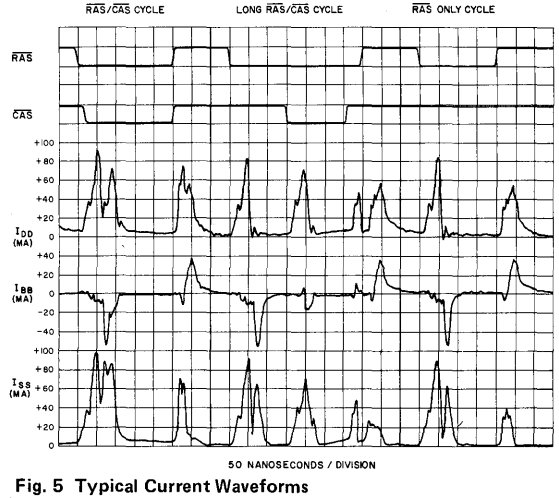


Fig. 5 Typical Current Waveforms

Although $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the MK 4116, overall system power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices (those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state of $\overline{CAS}$.

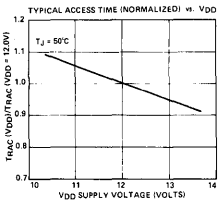
POWER UP

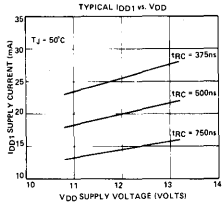
The MK 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, MOSTEK recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.

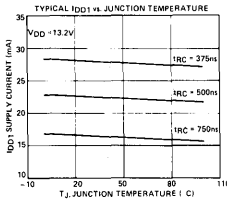
Under system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).

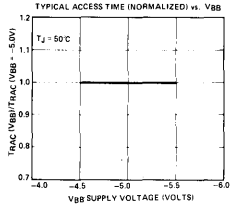
After power is applied to the device, the MK 4116 requires several cycles before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

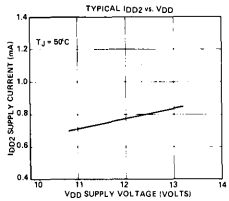
TYPICAL CHARACTERISTICS

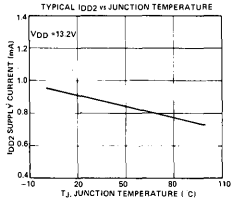


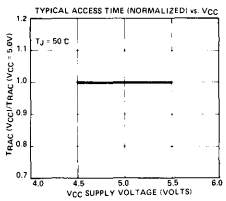


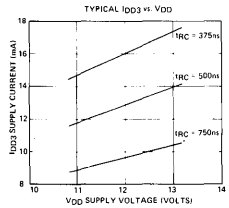


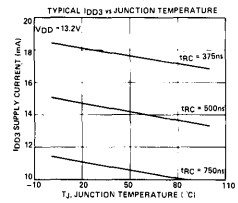


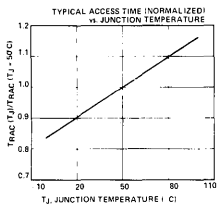


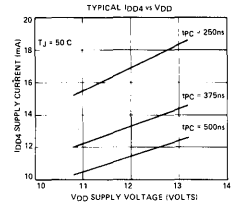


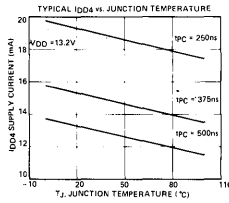


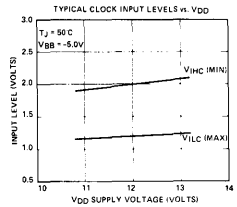


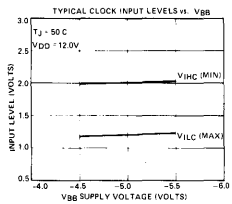


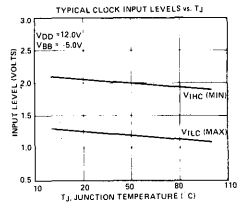


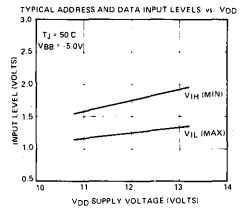


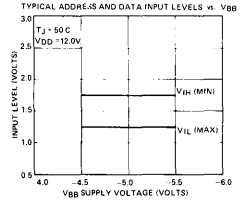


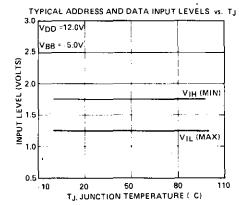












PRELIMINARY

16,384 x 1-BIT DYNAMIC RAM MK4116-53 (N)

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- 200 ns access time, 375 ns cycle
- Low power: 462 mW active, 20 mW standby (max)
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh and Page-mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- 128 refresh cycles

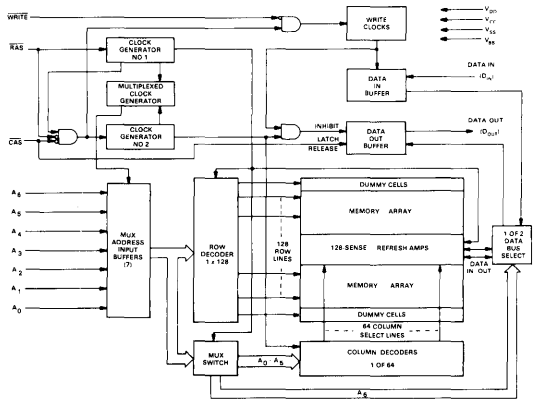
DESCRIPTION

The MK4116 is a new generation MOS dynamic random access memory circuit organized as 16,384 words by 1 bit. As a state-of-the-art MOS memory device, the MK4116 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in Mostek's high performance MK4027 (4K RAM).

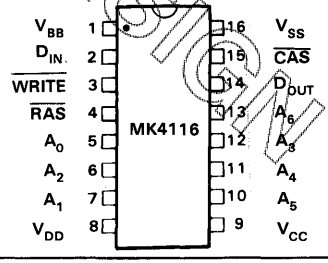
The technology used to fabricate the MK4116 is Mostek's double-poly, N-channel silicon gate, POLY II™ process. This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the MK4116 a truly superior RAM product.

Multiplexed address inputs (a feature pioneered by Mostek for its 4K RAMs) permits the MK4116 to be packaged in a standard 16-pin DIP. This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs for new generation applications. Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_6	Address Inputs	$\overline{WRITE}$	Read/Write Input
$\overline{CAS}$	Column Address Strobe	V_{BB}	Power (–5 V)
D_{IN}	Data In	V_{CC}	Power (+5 V)
D_{OUT}	Data Out	V_{DD}	Power (+12 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{BB} ..... -0.5 V to +20 V
Voltage on V_{DD}, V_{CC} supplies relative to V_{SS} ..... -1.0 V to +15.0 V
V_{BB} - V_{SS} (V_{DD} - V_{SS} > 0 V) ..... 0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +55°C
Storage Temperature (Ambient) (Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient) (Plastic) ..... -55°C to +125°C
Short Circuit Output Circuit ..... 50 mA
Power Dissipation ..... 1 Watt

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 55°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{DD} V_{CC} V_{SS} V_{BB}	Supply Voltage	10.8 4.5 0 -4.5	12.0 5.0 0 -5.0	13.2 5.5 0 -5.7	V V V V	1 1,2 1 1
V_{IHC}	Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4	—	7.0	V	1
V_{IH}	Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2	—	7.0	V	1
V_{IL}	Input Low (Logic 0) Voltage, all inputs	-1.0	—	0.8	V	1

DC ELECTRICAL CHARACTERISTICS

0°C ≤ T_A ≤ 55°C) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%; V_{BB} = -5.0 V ± 10%; V_{SS} = 0 V)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1} I_{CC1} I_{BB1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns)		35 200	mA μA	3 4
I_{DD2} I_{CC2} I_{BB2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance)	 -10	1.5 10 100	mA μA μA	
I_{DD3} I_{CC3} I_{BB3}	REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, CAS = V_{IHC}; t_{RC} = 375 ns	 -10	27 10 200	mA μA μA	3
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (V_{BB} = -5 V, 0 V ≤ V_{IN} ≤ +7.0 V, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ V_{OUT} ≤ +5.5 V)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output high (Logic 1) voltage (I_{OUT} = -5 mA) Output low (Logic 0) voltage (I_{OUT} = 4.2 mA)	 2.4	 0.4	 V V	 3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS [5,6,7]
($0°C \leq T_A \leq 55°C$) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_B = -5.0 V ± 10%)

SYM	PARAMETER	MK4116-53**		UNITS	NOTES
		MIN	MAX		
t_{RC}	Random read or write cycle time	375		ns	17
t_{RWC}	Read-write cycle time	375		ns	17
t_{RMW}	Read Modify Write	405		ns	
t_{RAC}	Access time from $\overline{RAS}$		200	ns	8,10
t_{CAC}	Access time from $\overline{CAS}$		135	ns	9,10
t_{OFF}	Output buffer turn-off delay	0	50	ns	11
t_T	Transition time (rise and fall)	3	50	ns	7
t_{RP}	$\overline{RAS}$ precharge time	120		ns	
t_{RAS}	$\overline{RAS}$ pulse width	200	10000	ns	
t_{RSH}	$\overline{RAS}$ hold time	135		ns	
t_{CAS}	$\overline{CAS}$ pulse width	135	10000	ns	
t_{CSH}	$\overline{CAS}$ hold time	200		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	65	ns	12
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	-20		ns	
t_{ASR}	Row Address set-up time	0		ns	
t_{RAH}	Row Address hold time	25		ns	
t_{ASC}	Column Address set-up time	-10		ns	
t_{CAH}	Column Address hold time	55		ns	
t_{AR}	Column Address hold time referenced to $\overline{RAS}$	120		ns	
t_{RCS}	Read command set-up time	0		ns	
t_{RCH}	Read command hold time	0		ns	
t_{WCH}	Write command hold time	55		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	120		ns	
t_{WP}	Write command pulse width	55		ns	
t_{RWL}	Write command to $\overline{RAS}$ lead time	70		ns	
t_{CWL}	Write command to $\overline{CAS}$ lead time	70		ns	
t_{DS}	Date-in set-up time	0		ns	13
t_{DH}	Date-in hold time	55		ns	13

**This device can be operated at an ambient temperature of 70°C if the refresh interval is changed to 128 refresh cycles every 1.1 ms.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (5,6,7)

(0°C ≤ T_A ≤ 55°C) (V_{DD} = 12.0 V ± 10%; V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, V_{BB} = -5.0 V ± 10%)

SYM	PARAMETER	MK4116-53**		UNITS	NOTES
		MIN	MAX		
t_{DHR}	Date-in hold time referenced to $\overline{RAS}$	120		ns	
t_{REF}	Refresh Period		2	ms	
t_{WCS}	$\overline{WRITE}$ command set-up time	-20		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	80		ns	14
t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	145		ns	14

NOTES:

1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} min specification is not guaranteed in this mode.
3. I_{DD1} and I_{DD3} depend on cycle rate. The maximum specified current values are for t_{RC} = 375 ns. I_{DD} limit at other cycle rates are determined by the following equations:
   I_{DD1} (max) [MA] = 10 + 10.25 x cycle rate [MHz]
   I_{DD3} (max) [MA] = 10 + 7 x cycle rate [MHz]
4. I_{CC1} depends upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135 typ) to data out. At all other times I_{CC} consists of leakage currents only.
5. Eight cycles are required after power-up or prolonged periods (greater than 2 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. AC measurements assume t_T = 5 ns.
7. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Measured with a load equivalent to 2 TTL loads and 100pF.
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD} and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
15. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV=3 volts and power supplies at nominal levels.
16. CAS = V_{IHC} to disable D_{OUT}.
17. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 55°C) is assured.

AC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 55°C) (V_{DD} = 12.0 V ± 10%, V_{SS} = 0V; V_{BB} = -5.0 V ± 10%)

SYM	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0-A_6), D_{IN}	4	5	pF	15
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	15
C_O	Output Capacitance (D_{OUT})	5	7	pF	15,16

DESCRIPTION (Continued)

System oriented features include direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize "false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of this memory system. The MK4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the MK4116 is capable of delayed write cycles, and $\overline{RAS}$-only refresh. Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, and two dimensional chip selection.

16,384 x 1-BIT DYNAMIC RAM MK4516(N/J)-9

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Active power 193 mW maximum
  Standby power 20 mW maximum
- 90 ns access time, 200 ns cycle time
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4564 (64K RAM)
- 128 refresh cycles (2 msec)

DESCRIPTION

The MK4516 is a single +5 V power supply version of the industry standard MK4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MK4516 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatability, and +5 V only operation.

The MK4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH.

The MK4516 is designed to be compatible with the JEDEC standards for the 16K x 1 dynamic RAM. The MK4516 is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance.

The compatibility with the MK4564 will also permit a common board design to service both the MK4516 and MK4564 (64K RAM) designs. Therefore, the MK4516 will permit a smoother transition to the 64K RAM, as the industry standard MK4027 did for the MK4116.

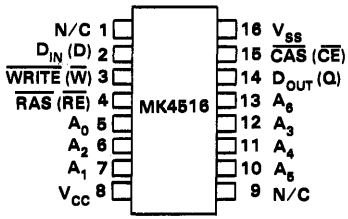
The user requiring only a small memory size need no longer pay the three power supply penalty for achieving the economics of using dynamic RAM over static RAM when using this new generation device.

PIN FUNCTIONS

A_0-A_6	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Col. Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/Write Input
D_{IN} (D)	Data In	N/C	Not connected
D_{OUT} (Q)	Data Out	V_{CC}	Power (+5V)
		V_{SS}	GND

DUAL IN-LINE PACKAGE PIN OUT

Figure 1



Available soon in MIL-STD-883 Class B (MKB4516)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	2
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	0.8	V	2,19

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)		35	mA	3
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		3.5	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		30	mA	3
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		32	mA	3,20
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq +5.5$ V, all other pins not under test = 0 volts)	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq +5.5$ V)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA	2.4	0.4	V V	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS [4,5,6,16]
$(0°C \leq T_A \leq 70°C)$, $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL		PARAMETER	MK4516-9		UNITS
STD	ALT		MIN	MAX	
t_{RELREL}	t_{RC}	Random read or write cycle time	200		ns
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	250		ns
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	100		ns
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		90	ns
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		50	ns
t_{CEHQZ}	t_{OFF}	Output buffer turn off delay	0	40	ns
t_T	t_T	Transition time (rise and fall)	3	50	ns
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	100		ns
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	90	10000	ns
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	60		ns
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	90		ns
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	50		ns
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	40	ns
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0		ns
t_{AVREL}	t_{ASR}	Row Address set-up time	0		ns
t_{RELAX}	t_{RAH}	Row Address hold time	15		ns
t_{AVCEL}	t_{ASC}	Column Address set-up time	0		ns
t_{CELAX}	t_{CAH}	Column Address hold time	15		ns
$t_{RELA(C)X}$	t_{AR}	Column Address hold time referenced to $\overline{RAS}$	55		ns
t_{WHCEL}	t_{RCS}	Read command set-up time	0		ns
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		ns
t_{CELWX}	t_{WCH}	Write command hold time	25		ns
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	65		ns
t_{WLWH}	t_{WP}	Write command pulse width	25		ns
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	50		ns
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	50		ns

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL		PARAMETER	MK4516-9		UNITS
STD	ALT		MIN	MAX	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		ns
t_{CELDX}	t_{DH}	Data-in hold time	25		ns
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	65		ns
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	45		ns
t_{RVRV}	t_{REF}	Refresh period		2	ms
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	0		ns
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	50		ns
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	90		ns
t_{CEHREL}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		ns

CAPACITANCE

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0\ V \pm 10\%$)

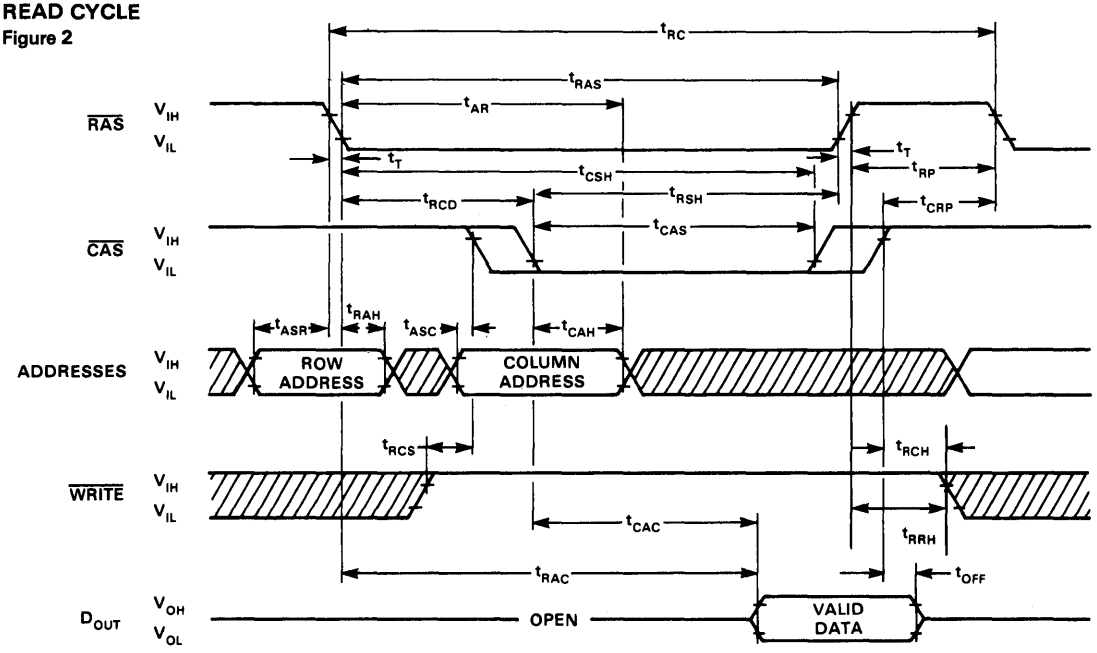
SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input (A_0-A_6), D_{IN}	4	5	pF	17
C_{I2}	Input $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	17
C_O	Output (D_{OUT})	5	7	pF	17,18

NOTES:

1. No user connection to Pin 1 (Leadless Chip Carrier only). This pin must be left floating.
2. All voltages referenced to V_{SS}.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
4. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ start-up cycles before proper device operation is achieved. $\overline{RAS}$ may be cycled during the initial pause. If $\overline{RAS}$ inactive interval exceeds 2ms, the device must be re-initialized by a minimum of 8 $\overline{RAS}$ start-up cycle.
5. AC characteristics assume $t_T = 5$ ns
6. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
8. Load = 2 TTL loads and 100 pF.
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
11. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$, (min) the cycle is an EARLY WRITE cycle, and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a READ/WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Effective capacitance calculated from the equation $c = I \frac{\Delta T}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level.
18. $\overline{CAS} = V_{IH}$ to disable D_{OUT}.
19. Includes the dc level and all instantaneous signal excursions.
20. Page Mode operation is not guaranteed on the standard MK4516. This function is available on request.

READ CYCLE

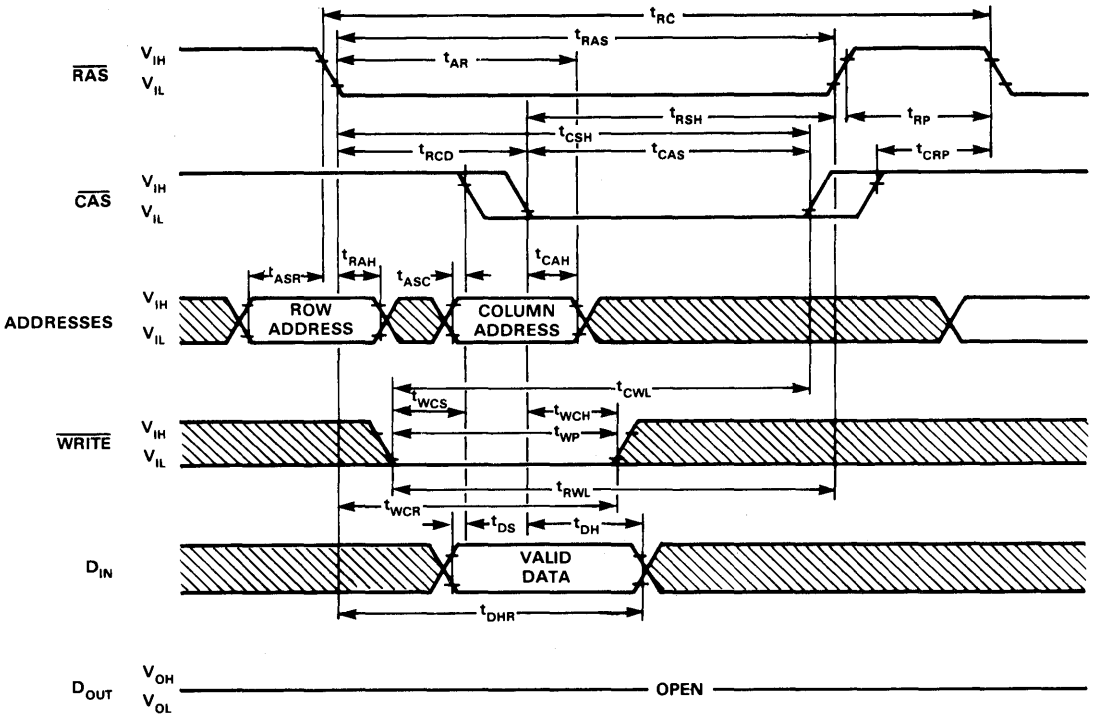
Figure 2



IV

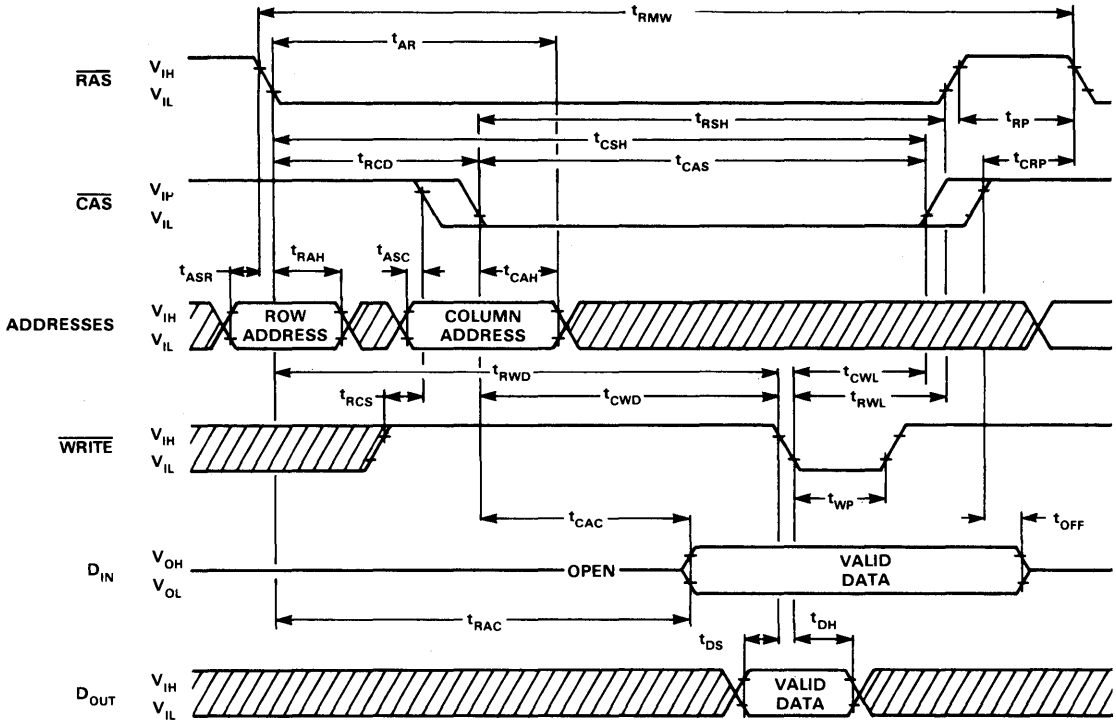
WRITE CYCLE (EARLY WRITE)

Figure 3



READ-WRITE/READ-MODIFY-WRITE CYCLE

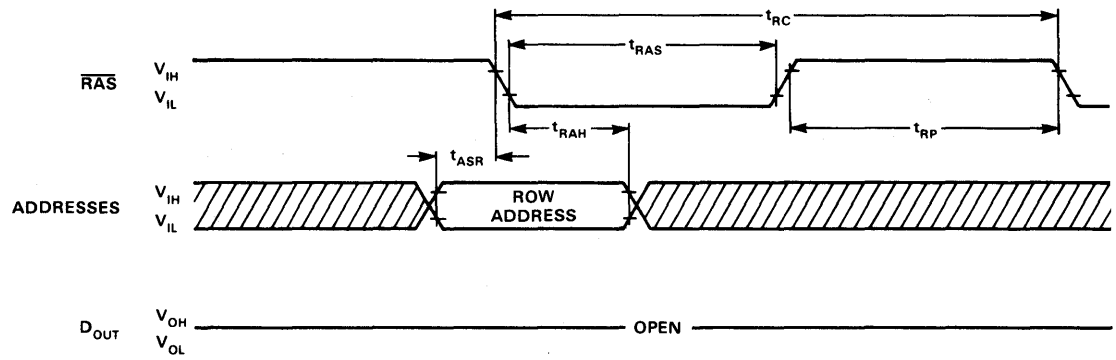
Figure 4



"RAS-ONLY" REFRESH CYCLE

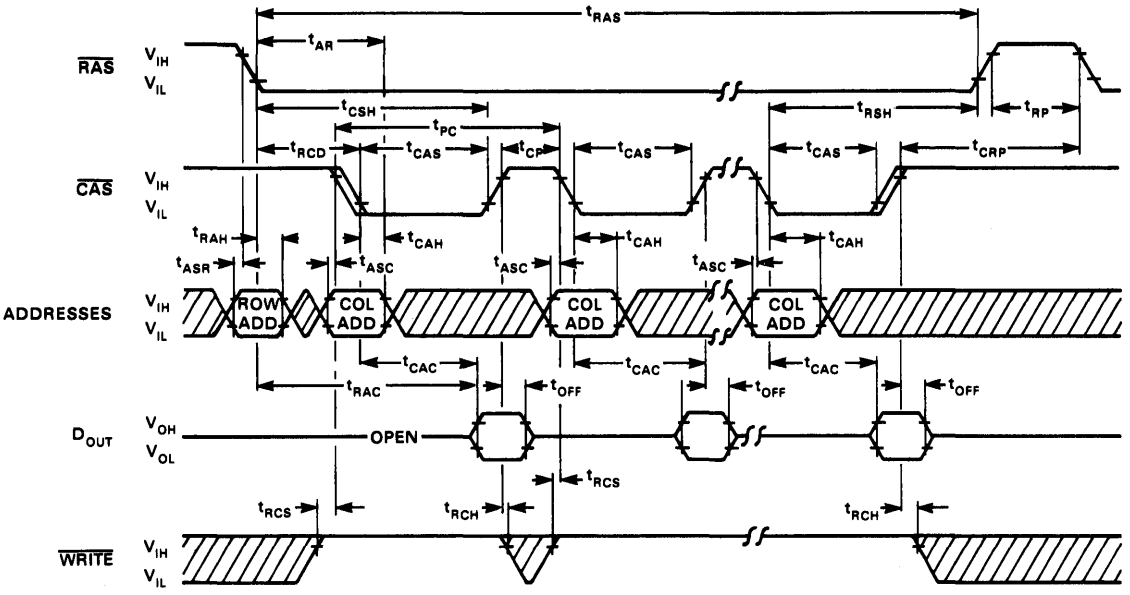
NOTE: CAS = V_{IH}, WRITE = DON'T CARE

Figure 5



PAGE MODE READ CYCLE (20)

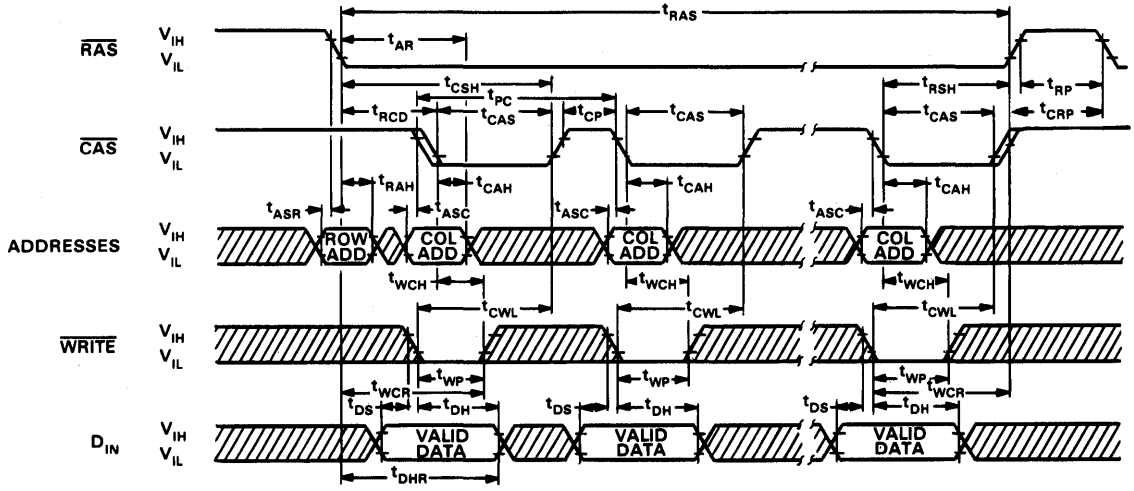
Figure 6



IV

PAGE MODE WRITE CYCLE (20)

Figure 7



OPERATION

The 14 address bits required to decode one of the 16,384 cell locations within the MK4516 are multiplexed onto the seven address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the seven row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the seven column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied, and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH}, and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$, which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while RAS is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$, to make its negative transition, is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle", the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

Data Output Control

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive), the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at all 128 combinations of the seven row address bits within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

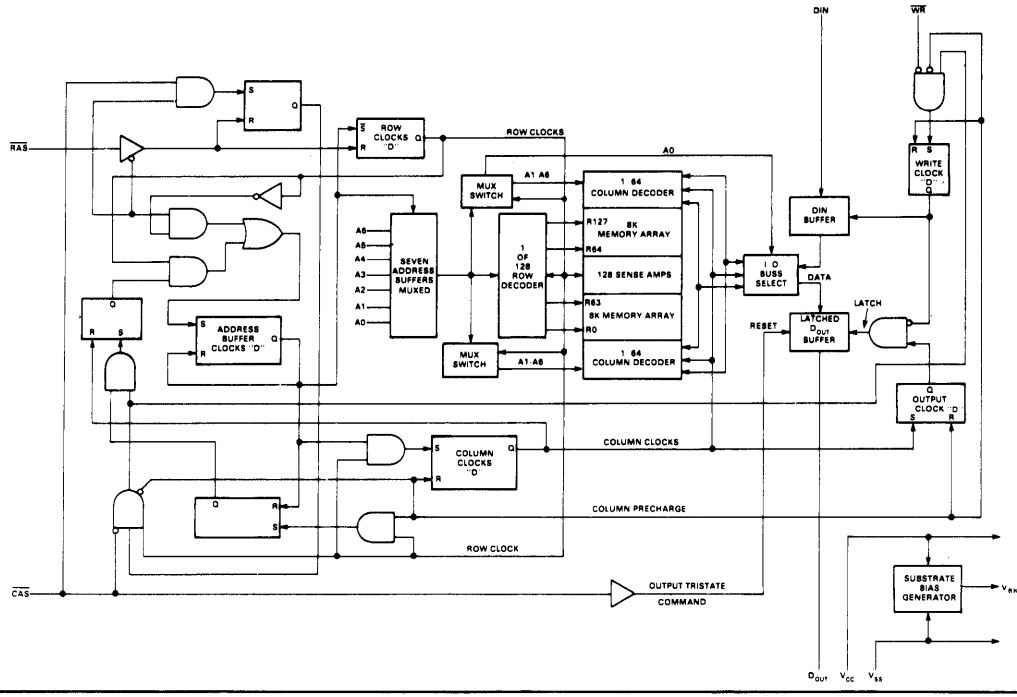
Page Mode Operation *

The Page Mode feature of the MK4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4516, this results in as much as a 55% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4516 is limited to the 128 column locations determined by all combinations of the seven column address bits. Operations within the page boundary need not be sequentially addressed, and any combination of read-write and read-modify-write cycles are permitted within the page mode operation.

* see note 20

MK4516A FUNCTIONAL BLOCK DIAGRAM



16,384 × 1-BIT DYNAMIC RAM
MK4516(N/J/E)-10/12/15

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Active power 193 mW maximum
  Standby power 20 mW maximum (MK4516-10)
  Standby power 17 mW maximum (MK4516-12/15)
- 100 ns access time, 235 ns cycle time (MK4516-10)
  120 ns access time, 270 ns cycle time (MK4516-12)
  150 ns access time, 320 ns cycle time (MK4516-15)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4564 (64K RAM)
- 128 refresh cycles (2 msec)

DESCRIPTION

The MK4516 is a single +5 V power supply version of the industry standard MK4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MK4516 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatability, and +5 V only operation.

The MK4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH.

The MK4516 is designed to be compatible with the JEDEC standards for the 16K x 1 dynamic RAM. The MK4516 is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance. The compatability with the MK4564 will also permit a common board design to service both the MK4516 and MK4564 (64K RAM) designs. The MK4516 will therefore permit a smoother transition to the 64K RAM as the industry standard MK4027 did for the MK4116.

The user requiring only a small memory size need no longer pay the three power supply penalty for achieving the economics of using dynamic RAM over static RAM when using this new generation device.

PIN FUNCTIONS

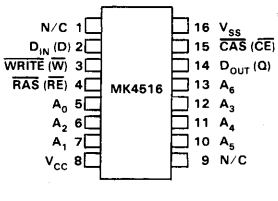
A_0-A_6	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Col. Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/Write Input
D_{IN} (D)	Data In	N/C	Not connected
D_{OUT} (Q)	Data Out	V_{CC}	Power (+5V)
		V_{SS}	GND

Available soon in MIL-STD-883 Class B (MKB4516)

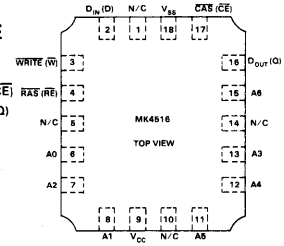
PIN OUT

Figure 1

DUAL-IN-LINE PACKAGE



LEADLESS CHIP CARRIER (1)



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	2
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	2,19

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)		35	mA	3
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH},		3	mA	
	D_{OUT} = High Impedance)		3.5	mA	21
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		30	mA	3
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		32	mA	3,20
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input (0 V ≤ V_{IN} ≤ +5.5 V, all other pins not under test = 0 volts)	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, 0 V ≤ V_{OUT} ≤ +5.5 V)	-10	10	μA	
	OUTPUT LEVELS				
V_{OH}	Output High (Logic 1) voltage (I_{OUT} = -5 mA)	2.4		V	
V_{OL}	Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA		0.4	V	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS [4,5,6,16]

($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL			MK4516-10		MK4516-12		MK4516-15			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	235		270		320		ns	7,8
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	285		320		410		ns	7,8
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	125		145		190		ns	7,8,20
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		100		120		150	ns	8,9
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		55		65		80	ns	8,10
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	45	0	50	0	60	ns	11
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	6,16
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	110		120		135		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	115	10^4	140	10^4	175	10^4	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	70		85		105		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	100		120		165		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	55	10^4	65	10^4	95	10^4	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	45	25	55	25	70	ns	12
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0		0		0		ns	13
t_{AVREL}	t_{ASR}	Row Address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row Address hold time	15		15		15		ns	
t_{AVCEL}	t_{ASC}	Column Address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column Address hold time	15		15		20		ns	
$t_{RELA(C)X}$	t_{AR}	Column Address hold time referenced to $\overline{RAS}$	60		70		90		ns	
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	13
t_{CELWX}	t_{WCH}	Write command hold time	25		30		45		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_{WLWH}	t_{WP}	Write command pulse width	25		30		50		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	60		65		110		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	45		50		100		ns	

IV

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL			MK4516-10		MK4516-12		MK4516-15			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	14
t_{CELDX}	t_{DH}	Data-in hold time	25		30		45		ns	14
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	70		85		115		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	60		70		85		ns	20
t_{RVRV}	t_{REF}	Refresh period		2		2		2	ms	
t_{WLCEL}	t_{WCS}	WRITE command set-up time	0		0		0		ns	15
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		65		80		ns	15
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	100		120		150		ns	15
t_{CEHREL}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		0		0		ns	

CAPACITANCE

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0\ V \pm 10\%$)

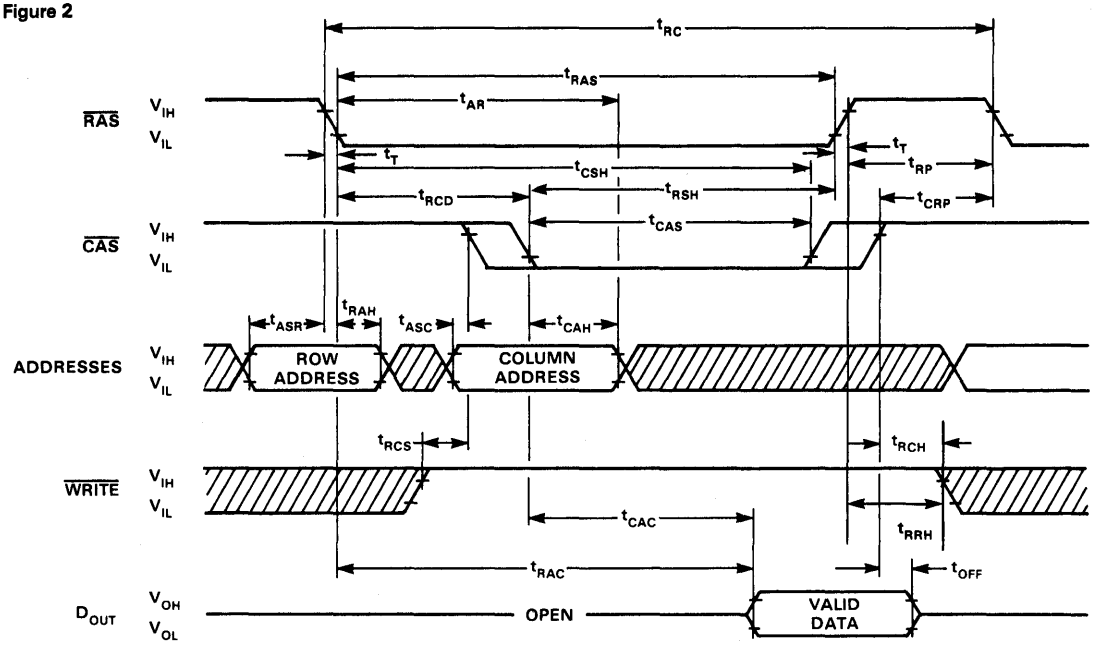
SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input (A_0-A_6), D_{IN}	4	5	pF	17
C_{I2}	Input $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	17
C_O	Output (D_{OUT})	5	7	pF	17,18

NOTES:

1. No user connection to Pin 1 (Leadless Chip Carrier only). This pin must be left floating.
2. All voltages referenced to V_{SS}.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
4. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ start-up cycles before proper device operation is achieved. $\overline{RAS}$ may be cycled during the initial pause. If $\overline{RAS}$ inactive interval exceeds 2ms, the device must be re-initialized by a minimum of 8 $\overline{RAS}$ start-up cycle.
5. AC characteristics assume $t_T = 5$ ns
6. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
8. Load = 2 TTL loads and 100 pF.
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
11. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Effective capacitance calculated from the equation $c = I \frac{\Delta T}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level.
18. $\overline{CAS} = V_{IH}$ to disable D_{OUT}.
19. Includes the dc level and all instantaneous signal excursions.
20. Page Mode operation is not guaranteed on the standard MK4516. This function is available on request.
21. Applies to MK4516-10 only.

READ CYCLE

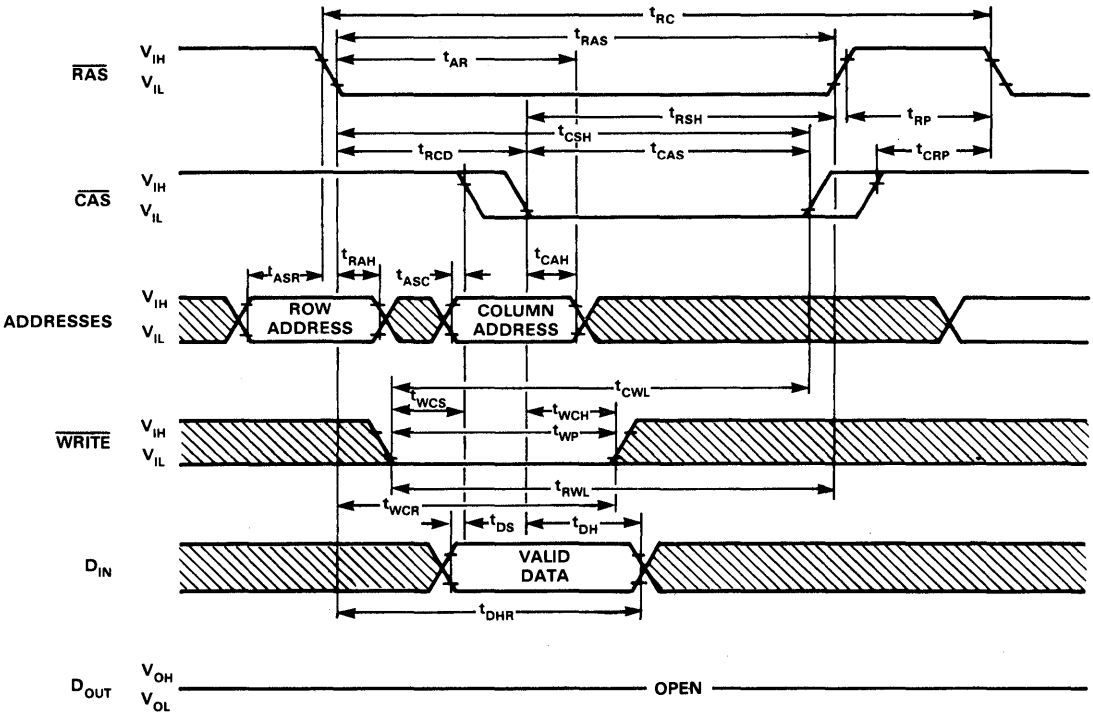
Figure 2



IV

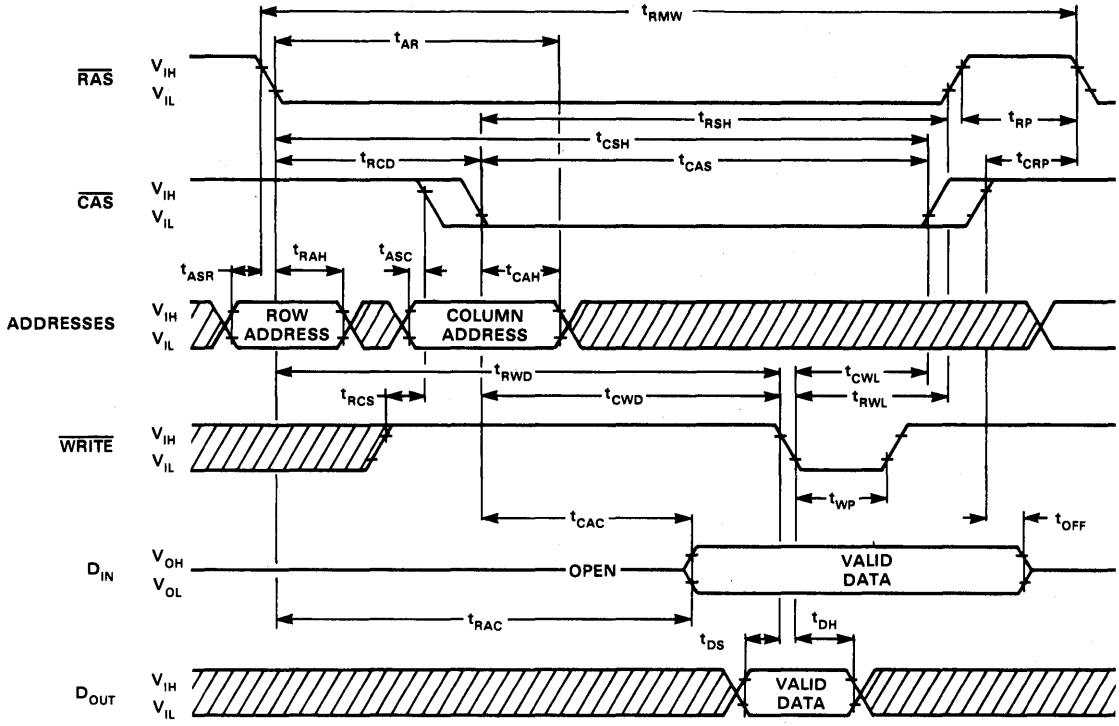
WRITE CYCLE (EARLY WRITE)

Figure 3



READ-WRITE/READ-MODIFY-WRITE CYCLE

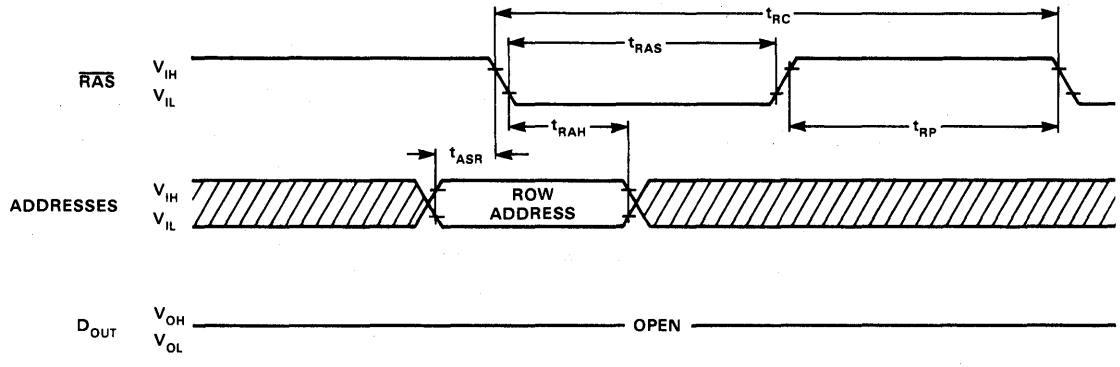
Figure 4



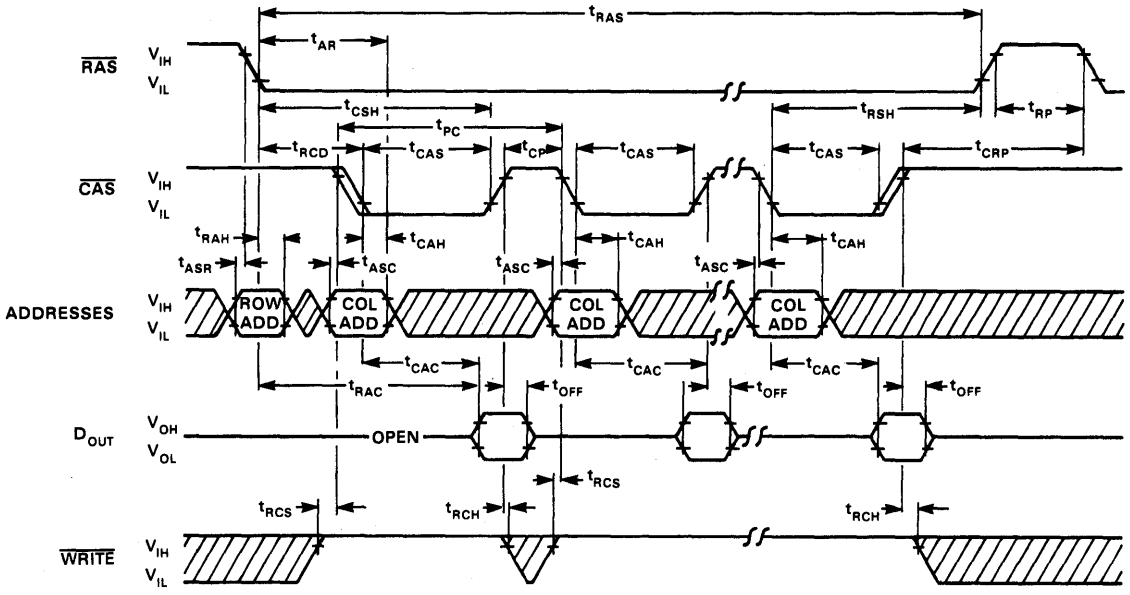
"RAS-ONLY" REFRESH CYCLE

NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WRITE}$ = DON'T CARE

Figure 5

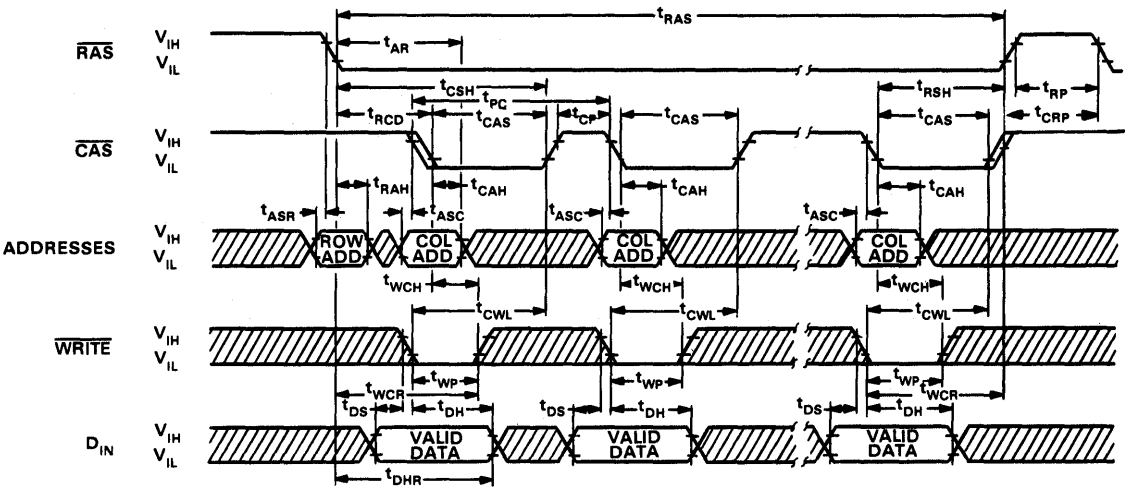


PAGE MODE READ CYCLE (20)
Figure 6



IV

PAGE MODE WRITE CYCLE (20)
Figure 7



OPERATION

The 14 address bits required to decode 1 of the 16,384 cell locations within the MK4516 are multiplexed onto the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the 7 row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

Data Output Control

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

Refresh

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at all 128 combinations of the seven row address bits within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

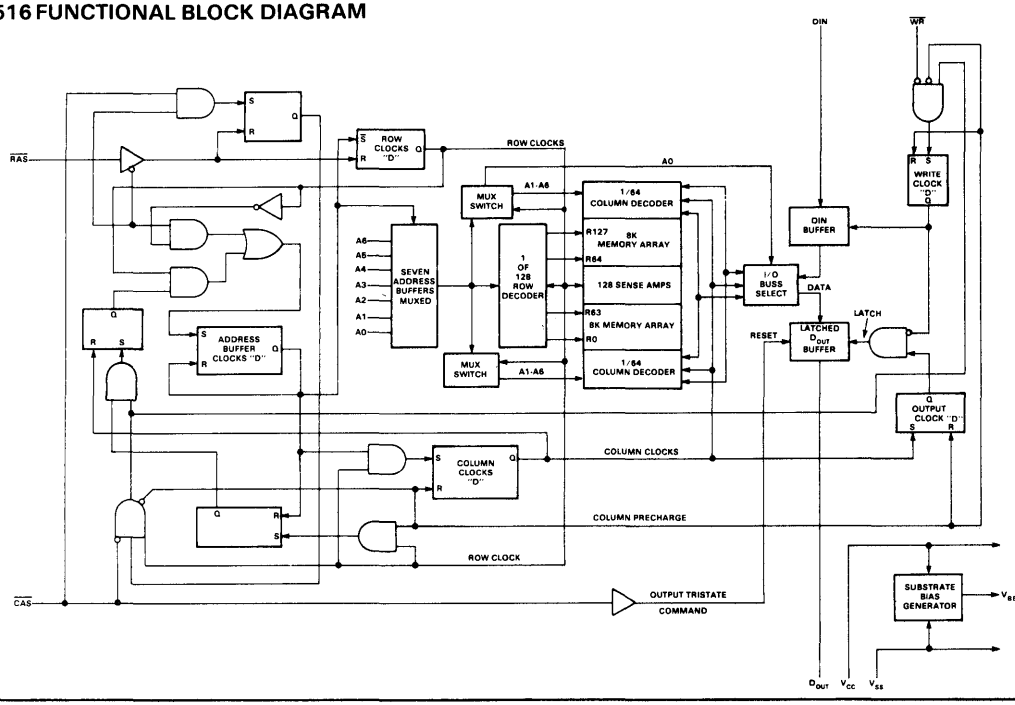
Page Mode Operation *

The Page Mode feature of the MK4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4516, this results in as much as a 55% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4516 is limited to the 128 column locations determined by all combinations of the seven column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read-write and read-modify-write cycle are permitted within the page mode operation.

* see footnote 20

MK4516 FUNCTIONAL BLOCK DIAGRAM



IV

16,384 x 1-BIT DYNAMIC RAM
MK4516(N/J)-20

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Active power 193 mW maximum
  Standby power 17 mW maximum
- 200 ns access time, 450 ns cycle time
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5 technology
- Pin compatible with the MK4564 (64K RAM)
- 128 refresh cycles (2 msec)

DESCRIPTION

The MK4516 is a single +5 V power supply version of the industry standard MK4116, 16,384 x 1 bit dynamic RAM.

The high performance features of the MK4516 are achieved by state-of-the-art circuit design techniques as well as utilization of Mostek's "Scaled POLY 5" process technology. Features include access times starting where the current generation 16K RAMs leave off, TTL compatability, and +5 V only operation.

The MK4516 is capable of a variety of operations including READ, WRITE, READ-WRITE, READ-MODIFY-WRITE, PAGE MODE, and REFRESH.

The MK4516 is designed to be compatible with the JEDEC standards for the 16 K x 1 dynamic RAM. The MK4516 is intended to extend the life cycle of the 16K RAM, as well as create new applications due to its superior performance.

The compatibility with the MK4564 will also permit a common board design to service both the MK4516 and MK4564 (64K RAM) designs. Therefore, the MK4516 will permit a smoother transition to the 64K RAM, as the industry standard MK4027 did for the MK4116.

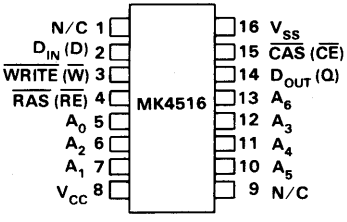
The user requiring only a small memory size need no longer pay the three power supply penalty for achieving the economics of using dynamic RAM over static RAM when using this new generation device.

PIN FUNCTIONS

A_0-A_6	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Col. Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/Write Input
D_{IN} (D)	Data In	N/C	Not connected
D_{OUT} (Q)	Data Out	V_{CC}	Power (+5V)
		V_{SS}	GND

DUAL IN-LINE PACKAGE PIN OUT

Figure 1



Available soon in MIL-STD-883 Class B (MKB4516)

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	2
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	0.8	V	2,19

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)		35	mA	3
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		3	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		30	mA	3
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		32	mA	3,20
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq +5.5$ V, all other pins not under test = 0 volts)	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq +5.5$ V)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA	2.4	 0.4	V V	

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS [4,5,6,16]
($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0\ V \pm 10\%$

SYMBOL		PARAMETER	MK4516-20		UNITS
STD	ALT		MIN	MAX	
t_{RELREL}	t_{RC}	Random read or write cycle time	450		ns
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	525		ns
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	220		ns
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		200	ns
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		100	ns
t_{CEHQZ}	t_{OFF}	Output buffer turn off delay		50	ns
t_T	t_T	Transition time (rise and fall	3	50	ns
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	200		ns
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	200	10000	ns
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	100		ns
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	200		ns
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	120	10000	ns
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	30	100	ns
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	45		ns
t_{AVREL}	t_{ASR}	Row Address set-up time	0		ns
t_{RELAX}	t_{RAH}	Row Address hold time	20		ns
t_{AVCEL}	t_{ASC}	Column Address set-up time	0		ns
t_{CELAX}	t_{CAH}	Column Address hold time	20		ns
$t_{RELA(C)X}$	t_{AR}	Column Address hold time referenced to $\overline{RAS}$	150		ns
t_{WHCEL}	t_{RCS}	Read command set-up time	0		ns
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		ns
t_{CELWX}	t_{WCH}	Write command hold time	60		ns
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	160		ns
t_{WLWH}	t_{WP}	Write command pulse width	60		ns
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	110		ns
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	100		ns

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (Continued)

SYMBOL		PARAMETER	MK4516-20		UNITS
STD	ALT		MIN	MAX	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		ns
t_{CELDX}	t_{DH}	Data-in hold time	60		ns
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	160		ns
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page mode cycle only)	110		ns
t_{RVRV}	t_{REF}	Refresh period		2	ms
t_{WLCEL}	t_{WCS}	WRITE command set-up time	0		ns
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	100		ns
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	200		ns
t_{CEHREL}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	0		ns

CAPACITANCE

($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0\ V \pm 10\%$)

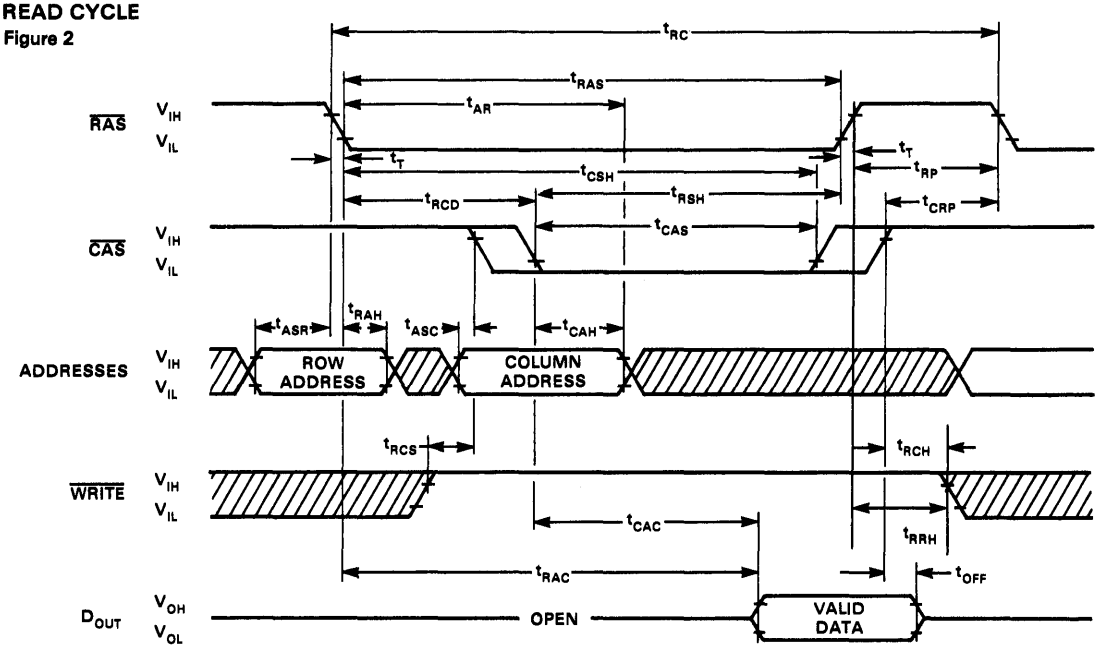
SYMBOL	PARAMETER	TYP	MAX	UNITS	NOTES
C_{I1}	Input (A_0-A_6), D_{IN}	4	5	pF	17
C_{I2}	Input $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	17
C_O	Output (D_{OUT})	5	7	pF	17,18

NOTES:

1. No user connection to Pin 1 (Leadless Chip Carrier only). This pin must be left floating.
2. All voltages referenced to V_{SS}.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
4. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ start-up cycles before proper device operation is achieved. $\overline{RAS}$ may be cycled during the initial pause. If $\overline{RAS}$ inactive interval exceeds 2ms, the device must be re-initialized by a minimum of 8 $\overline{RAS}$ start-up cycle.
5. AC characteristics assume $t_T = 5$ ns
6. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
8. Load = 2 TTL loads and 100 pF.
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
11. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
12. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write.
15. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$, (min) the cycle is an EARLY WRITE cycle, and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a READ/WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
16. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
17. Effective capacitance calculated from the equation $c = I \frac{\Delta T}{\Delta V}$ with $\Delta V = 3$ volts and power supply at nominal level.
18. $\overline{CAS} = V_{IH}$ to disable D_{OUT}.
19. Includes the dc level and all instantaneous signal excursions.
20. Page Mode operation is not guaranteed on the standard MK4516. This function is available on request.

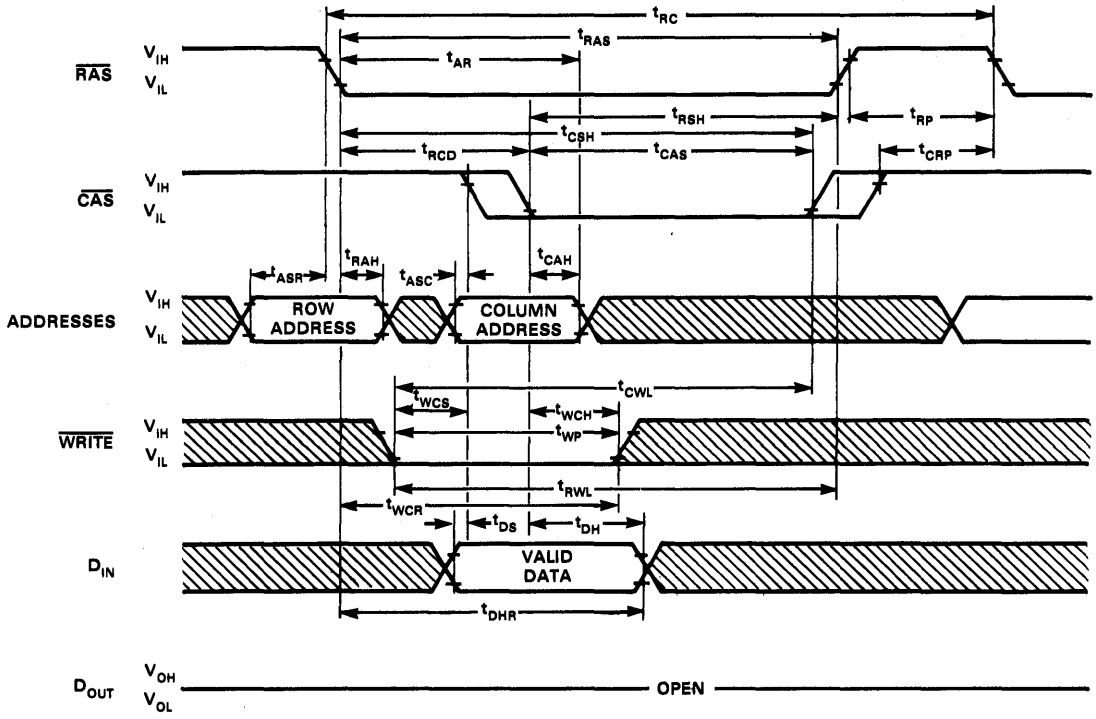
READ CYCLE

Figure 2



WRITE CYCLE (EARLY WRITE)

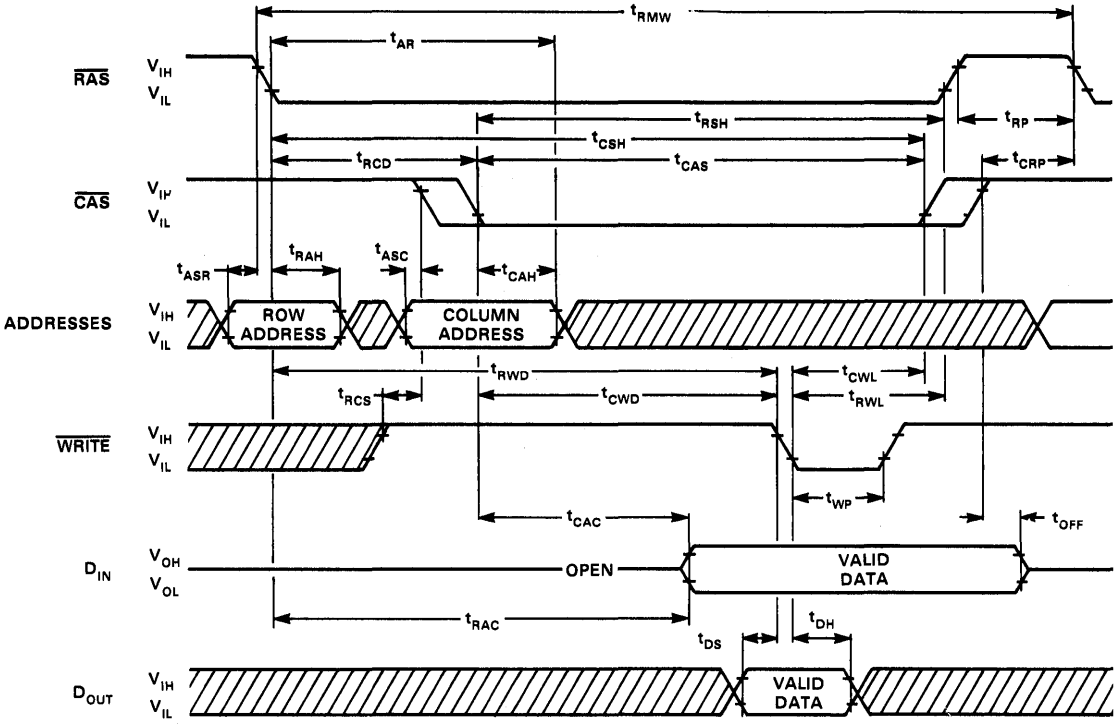
Figure 3



IV

READ-WRITE/READ-MODIFY-WRITE CYCLE

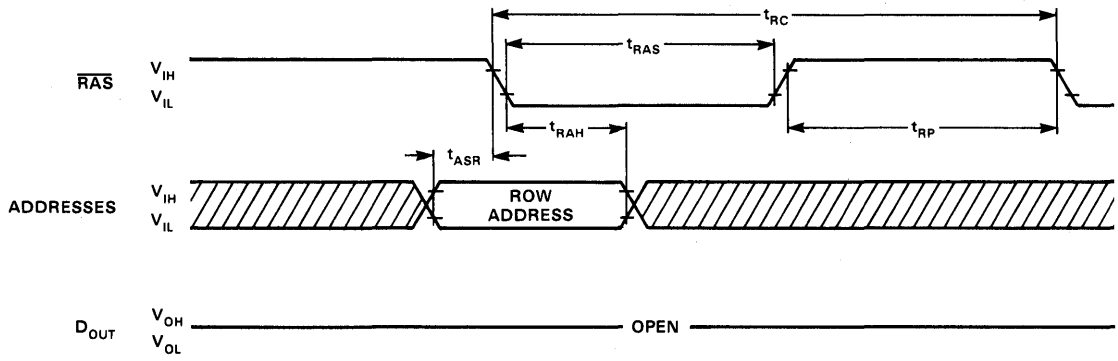
Figure 4



"$\overline{RAS}$-ONLY" REFRESH CYCLE

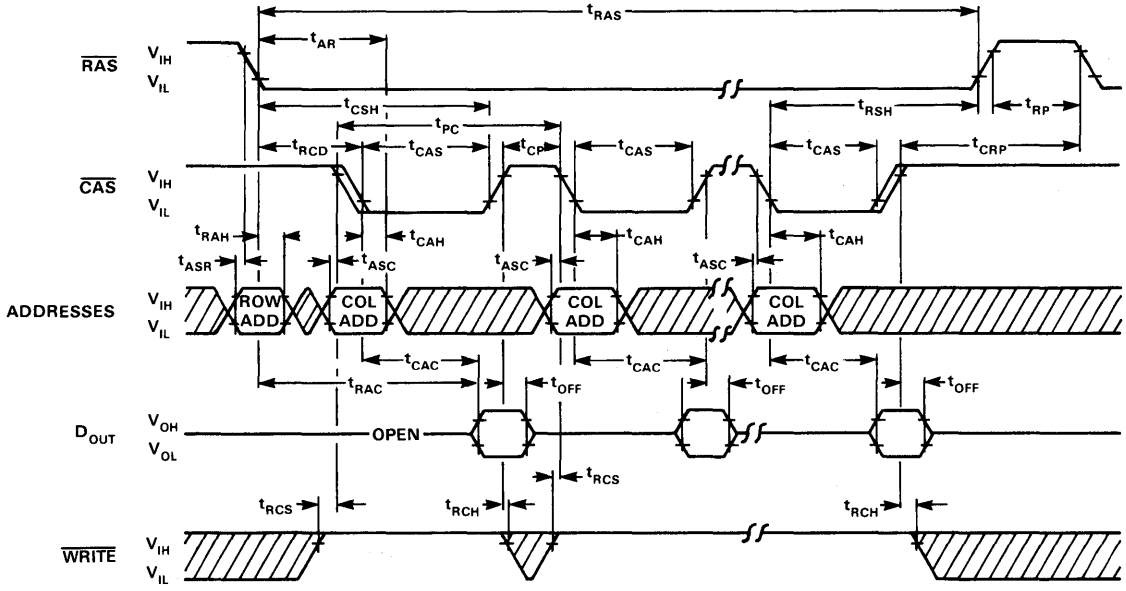
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WRITE}$ = DON'T CARE

Figure 5



PAGE MODE READ CYCLE (20)

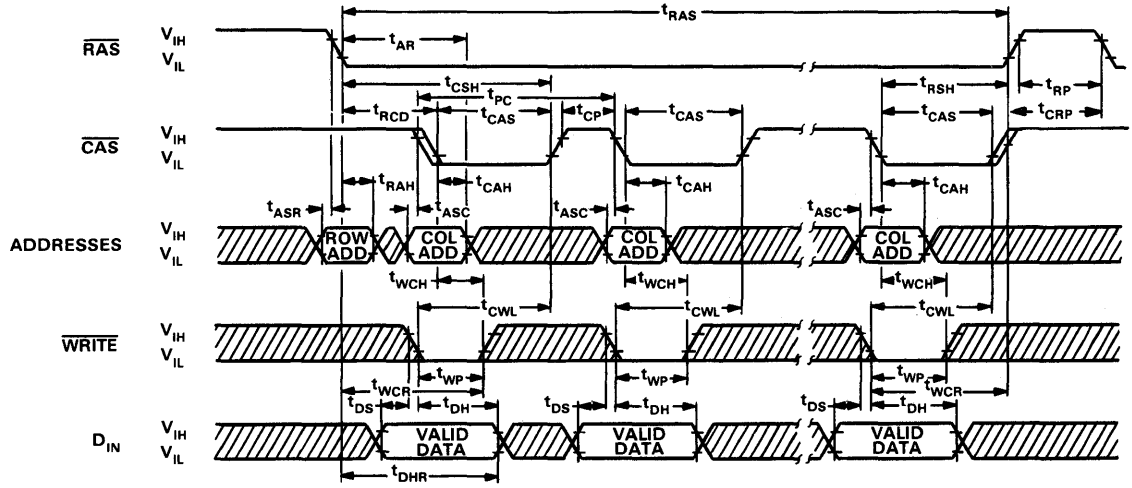
Figure 6



IV

PAGE MODE WRITE CYCLE (20)

Figure 7



OPERATION

The 14 address bits required to decode one of the 16,384 cell locations within the MK4516 are multiplexed onto the seven address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the seven row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the seven column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH}, and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$, which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4516 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

Data Input/Output

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$, to make its negative transition, is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle", the data input set-up and hold times are referenced to the negative edge of WRITE rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

Data Output Control

The normal condition of the Data Output (D_{OUT}) of the MK4516 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive), the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

Refresh

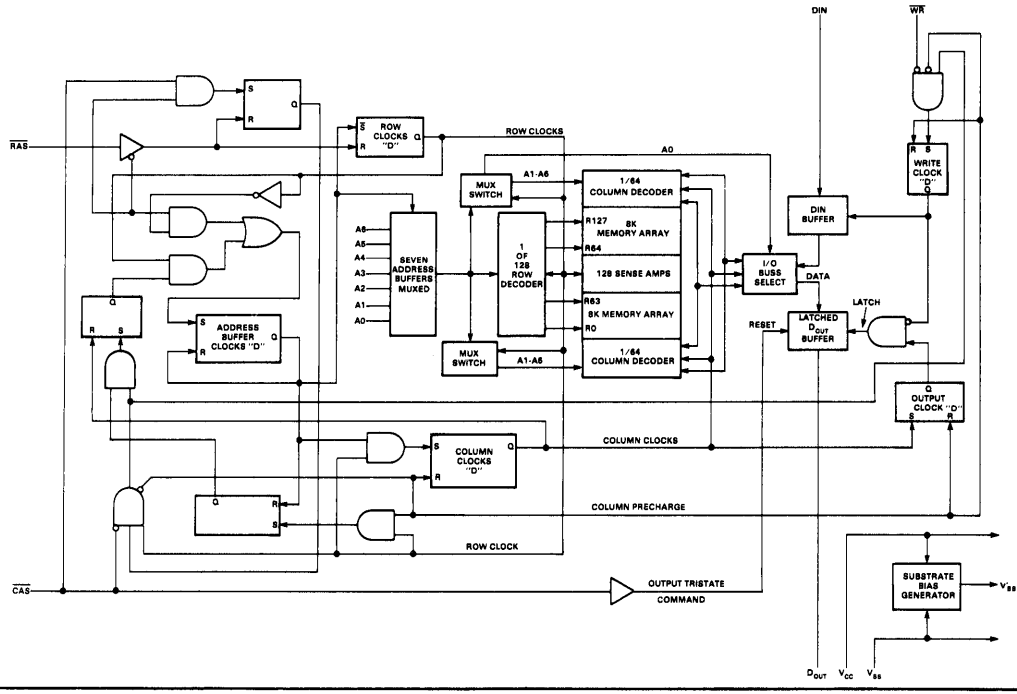
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at all 128 combinations of the seven row address bits within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

Page Mode Operation *

The Page Mode feature of the MK4516 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4516, this results in as much as a 55% improvement in access times! Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4516 is limited to the 128 column locations determined by all combinations of the seven column address bits. Operations within the page boundary need not be sequentially addressed, and any combination of read-write and read-modify-write cycle are permitted within the page mode operation.

MK4516 FUNCTIONAL BLOCK DIAGRAM



IV

65,536 x 1-BIT DYNAMIC RAM
MK4564(P/N/J/E)-12

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5 V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Low power: 330 mW active, max
  22 mW standby, max
- 120 ns access time, 220 ns cycle time
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5™ technology
- 128 refresh cycles (2 msec)
  Pin 9 is not needed for refresh

DESCRIPTION

The MK4564 is the new generation dynamic RAM. Organized 65,536 words by 1 bit, it is the successor to the industry standard MK4116. The MK4564 utilizes Mostek's Scaled Poly 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permits the MK4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MK4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The output of the MK4564 can be held valid up to 10 μsec by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

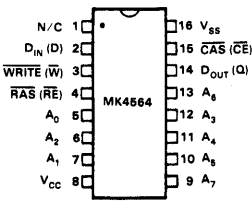
PIN FUNCTIONS

A_0-A_7	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/ Write Input
D_{IN} (D)	Data In	V_{CC}	Power (5V)
D_{OUT} (Q)	Data Out	V_{SS}	GND
		N/C	Not Connected

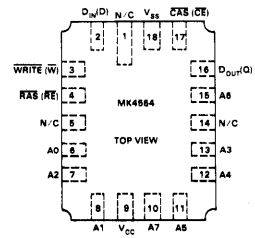
PIN OUT

Figure 1

DUAL-IN-LINE PACKAGE



LEADLESS CHIP CARRIER



Available soon in MIL-STD-883 Class B (MKB).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1,18

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min.)		60	mA	2
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)		4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{PC} = t_{PC} min.)		50	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		40	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0 volts	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq V_{CC}$)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	V V	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Load = 2 TTL loads and 50 pF.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max) limit permits t_{RAC} (max) to be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
15. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
16. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.
17. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.
18. Includes the DC level and all instantaneous signal excursions.
19. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, the data output will contain data from the last valid read cycle.

IV

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(3,4,5,15) (0°C ≤ T_A ≤ 70°C), V_{CC} = 5.0 V ± 10%

SYMBOL		PARAMETER	MK4564-12		UNITS	NOTES
STD	ALT		MIN	MAX		
t_{RELREL}	t_{RC}	Random read or write cycle time	220		ns	6,7
t_{RELREL} (RMW)	t_{RMW}	Read-modify-write cycle time	260		ns	6,7
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	145		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		120	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		75	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	40	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	90		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	120	10,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	75		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	120		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	75	10,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	15	45	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	10		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	15		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	15		ns	
$t_{RELA(C)X}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	70		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
(3,4,5,15) ($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0\ V \pm 10\%$

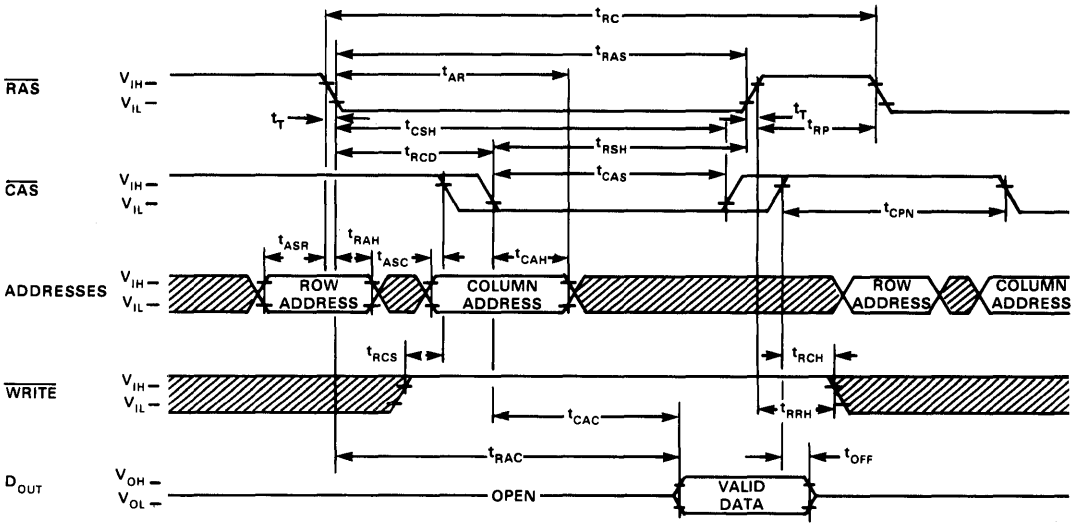
SYMBOL			MK4564-12			
STD	ALT	PARAMETER	MIN	MAX	UNITS	NOTES
t_{WHCEL}	t_{RCS}	Read command set-up time	0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	30		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	75		ns	
t_{WLWH}	t_{WP}	Write command pulse width	15		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	35		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	35		ns	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	30		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	75		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		ns	
t_{RVRV}	t_{REF}	Refresh Period		2	ms	
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	0		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	50		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	95		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	25		ns	

AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0\ V \pm 10\%$)

SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_7), D_{IN}	5	pF	16
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	10	pF	16
C_O	Output Capacitance (D_{OUT})	7	pF	16,17

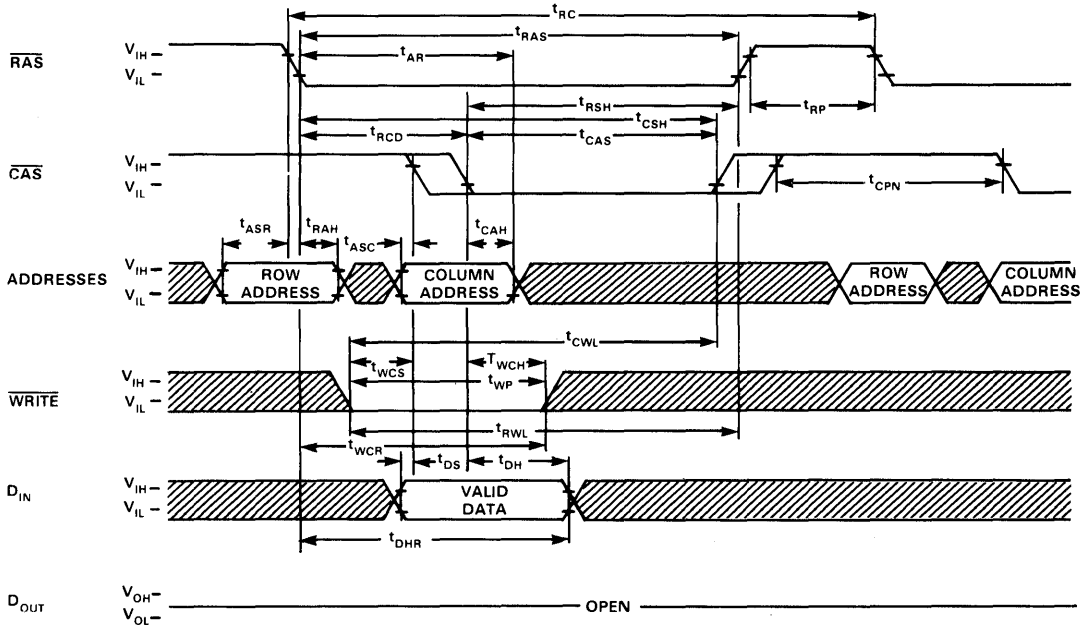
READ CYCLE

Figure 2



WRITE CYCLE (EARLY WRITE)

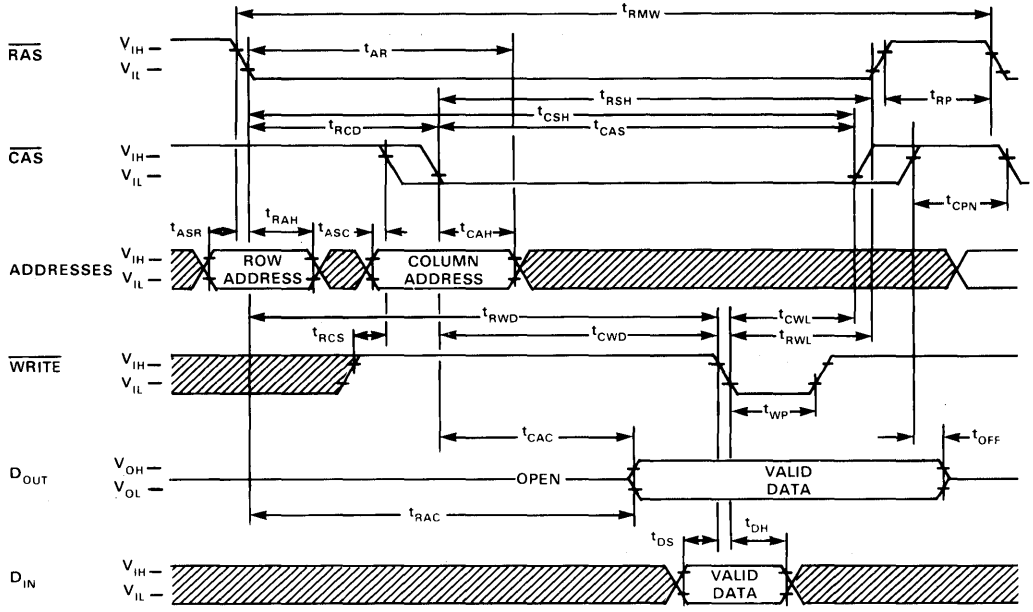
Figure 3



IV

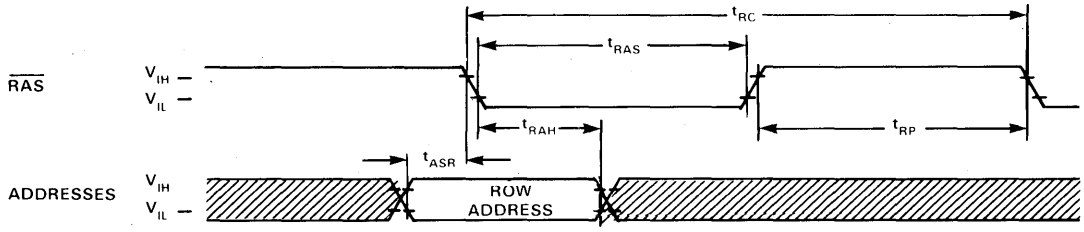
READ-WRITE/READ-MODIFY-WRITE CYCLE

Figure 4



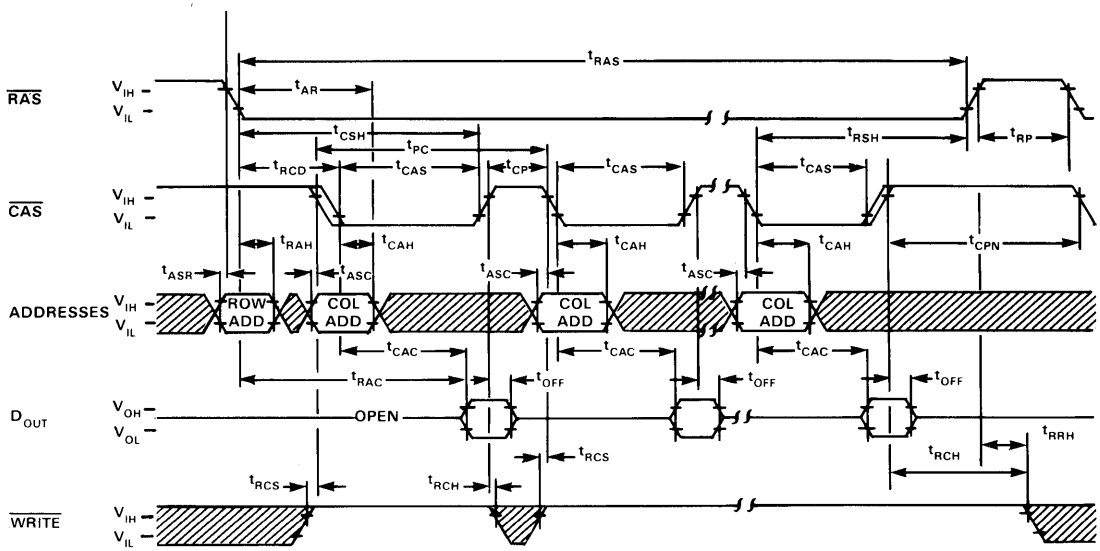
"RAS-ONLY" REFRESH CYCLE

Figure 5



PAGE MODE READ CYCLE

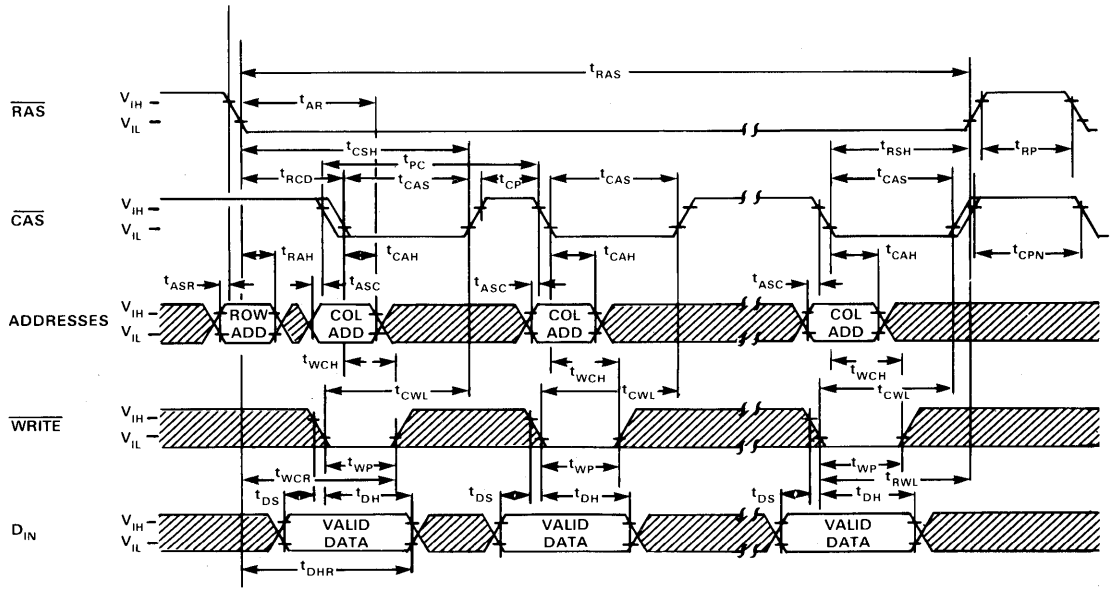
Figure 6



IV

PAGE MODE WRITE CYCLE

Figure 7



OPERATION

The eight address bits required to decode 1 of the 65,536 cell locations within the MK4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the eight row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the eight column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4564 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while RAS is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4564 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MK4564 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4564 this results in approximately a 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

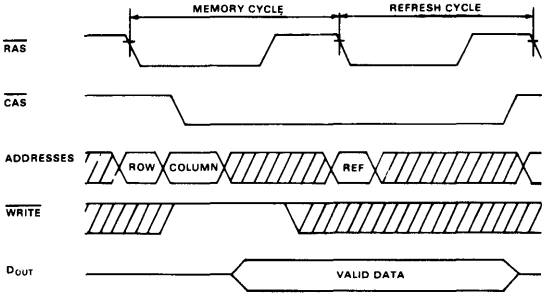
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time the $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, the $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)



65,536 x 1-BIT DYNAMIC RAM
MK4564(P/N/J/E)-15/20

FEATURES

- Recognized industry standard 16-pin configuration from Mostek
- Single +5V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Low power: 300 mW active, max
  22 mW standby, max
- 150 ns access time, 260 ns cycle time (MK4564-15)
  200 ns access time, 330 ns cycle time (MK4564-20)
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static charge
- Scaled POLY 5™ technology
- 128 refresh cycles (2 msec)
  Pin 9 is not needed for refresh

DESCRIPTION

The MK4564 is the new generation dynamic RAM. Organized 65,536 words by 1 bit, it is the successor to the industry standard MK4116. The MK4564 utilizes Mostek's Scaled POLY 5 process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, including the 512 sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or internal and external operating margins. Refresh characteristics have been chosen to maximize yield (low cost to user) while maintaining compatibility between dynamic RAM generations.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MK4564 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MK4564 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The output of the MK4564 can be held valid up to 10 μsec by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

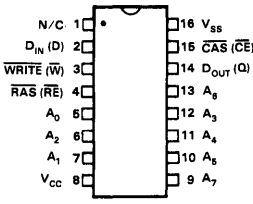
The 64K RAM from Mostek is the culmination of several years of circuit and process development, proven in predecessor products.

PIN FUNCTIONS

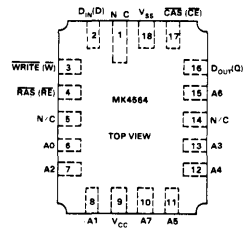
A_0-A_7	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/ Write Input
D_{IN} (D)	Data In	V_{CC}	Power (5V)
D_{OUT} (Q)	Data Out	V_{SS}	GND
		N/C	Not Connected

PIN OUT

DUAL-IN-LINE PACKAGE



LEADLESS CHIP CARRIER



Available soon in MIL-STD-883 Class B (MKB).

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Short Circuit Output Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1,18

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 330 ns)		54.0	mA	2
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{RAS}$ = V_{IH}, D_{OUT} = High Impedance)		4	mA	
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min.)		45	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, t_{RAS} = t_{RAS} max., $\overline{CAS}$ cycling; t_{PC} = t_{PC} min.)		40	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0 V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0 V	-10	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0 V \leq V_{OUT} \leq V_{CC}$)	-10	10	μA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	 V V	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Load = 2 TTL loads and 50 pF.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a READ/WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
15. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
16. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.
17. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.
18. Includes the DC level and all instantaneous signal excursions.
19. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, the data output will contain data from the last valid read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(3,4,5,15) (0°C ≤ T_A ≤ 70°C), V_{CC} = 5.0 V ± 10%

SYMBOL		PARAMETER	MK4564-15		MK4564-20		UNITS	NOTES
STD	ALT		MIN	MAX	MIN	MAX		
t_{RELREL}	t_{RC}	Random read or write cycle time	260		330		ns	6,7
t_{RELREL} (RMW)	t_{RMW}	Read modify write cycle time	300		390		ns	6,7
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	155		200		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		150		200	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		85		115	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	40	0	50	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	100		120		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	150	10,000	200	10,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	85		115		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	150		200		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	85	10,000	115	10,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	20	65	25	85	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	20		25		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	20		25		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	25		35		ns	
$t_{RELA(C)X}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	90		120		ns	

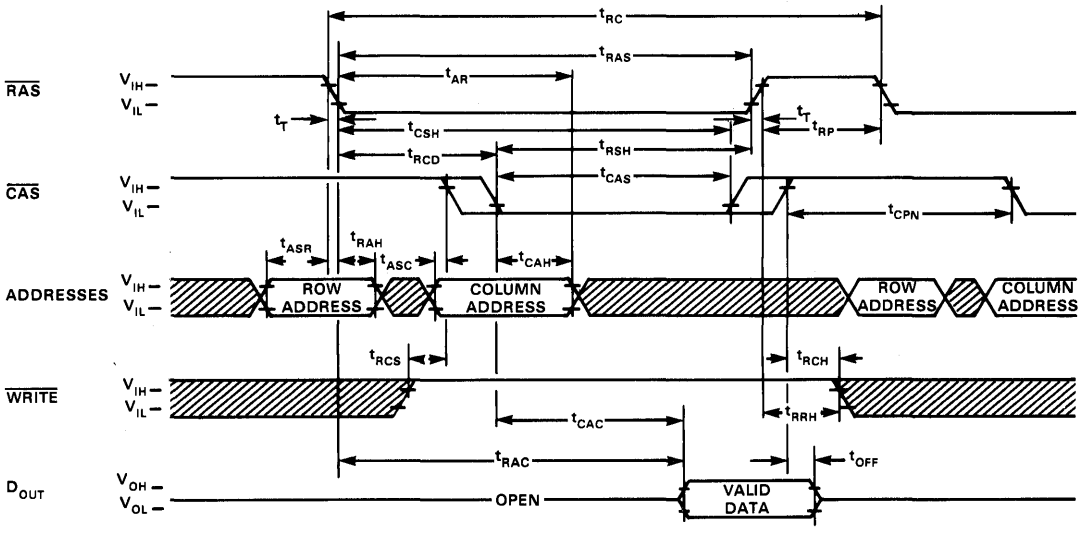
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
(3,4,5,15) (0°C ≤ T_A ≤ 70°C), V_{CC} = 5.0V ± 10%

SYMBOL			MK4564-15		MK4564-20			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	35		55		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	100		140		ns	
t_{WLWH}	t_{WP}	Write command pulse width	25		45		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	35		55		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	35		55		ns	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	30		55		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	95		140		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	60		75		ns	
t_{RVRV}	t_{REF}	Refresh Period		2		2		ms
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	-10		-10		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	55		80		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	120		165		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	30		35		ns	

AC ELECTRICAL CHARACTERISTICS
(0° ≤ T_A ≤ 70°C), V_{CC} = 5.0 V ± 10%

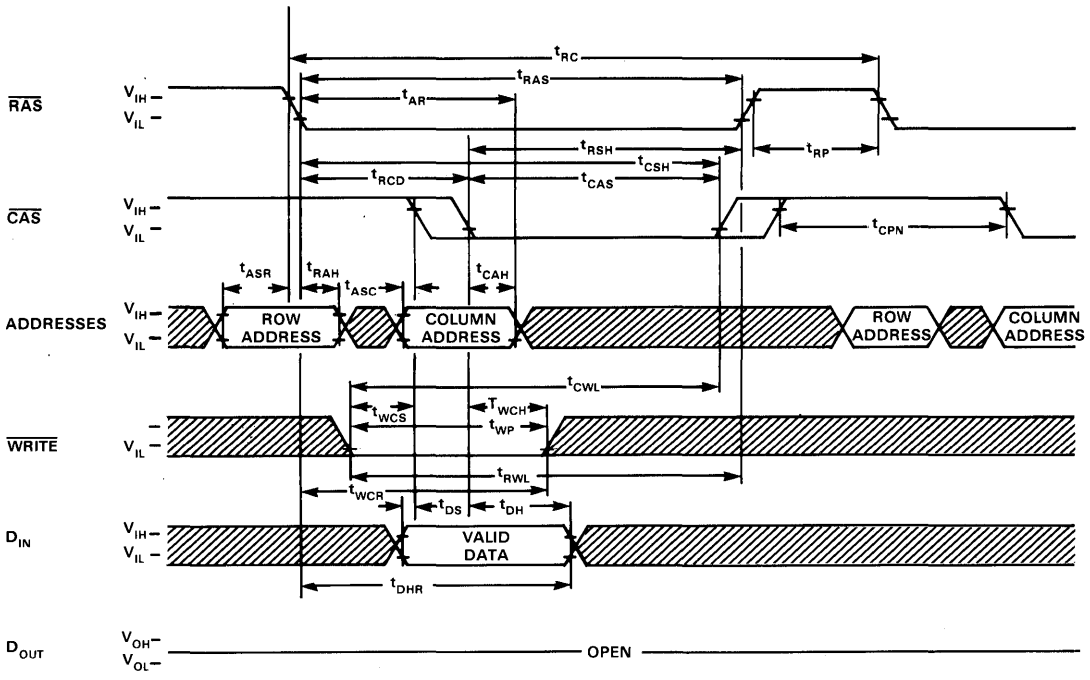
SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_7), D_{IN}	5	pF	16
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	10	pF	16
C_O	Output Capacitance (D_{OUT})	7	pF	16,17

READ CYCLE

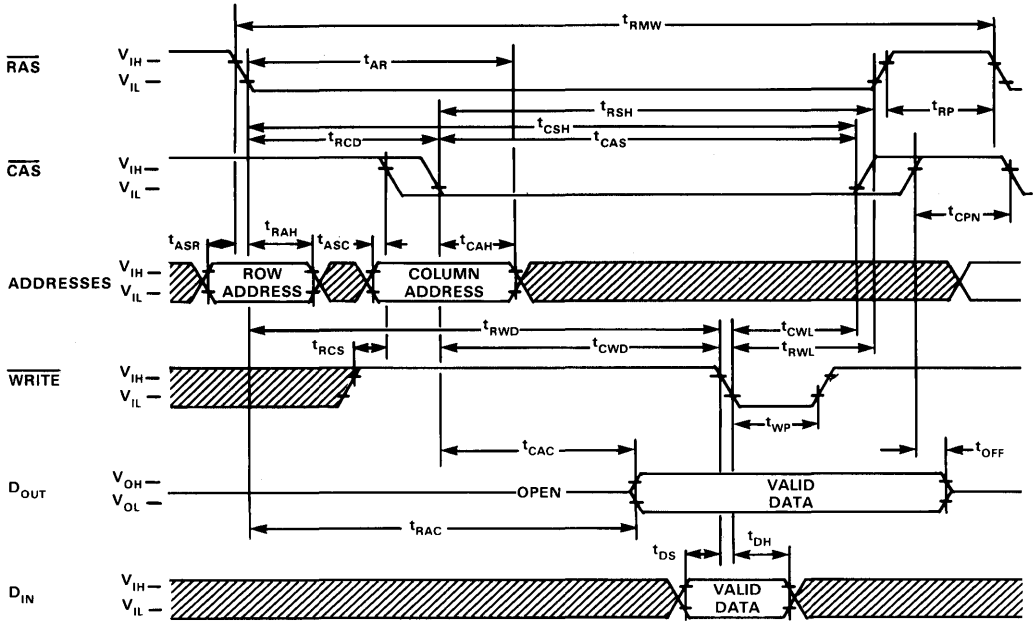


IV

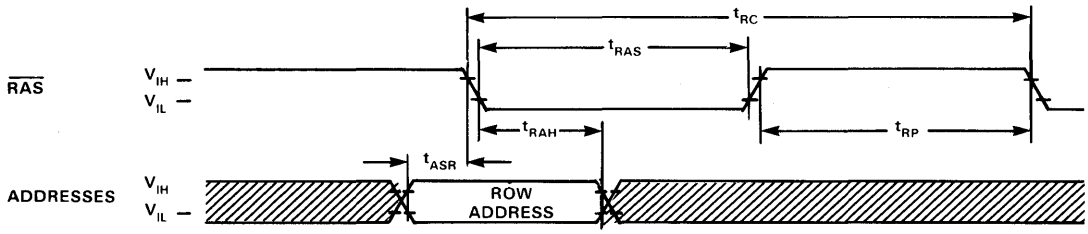
WRITE CYCLE (EARLY WRITE)



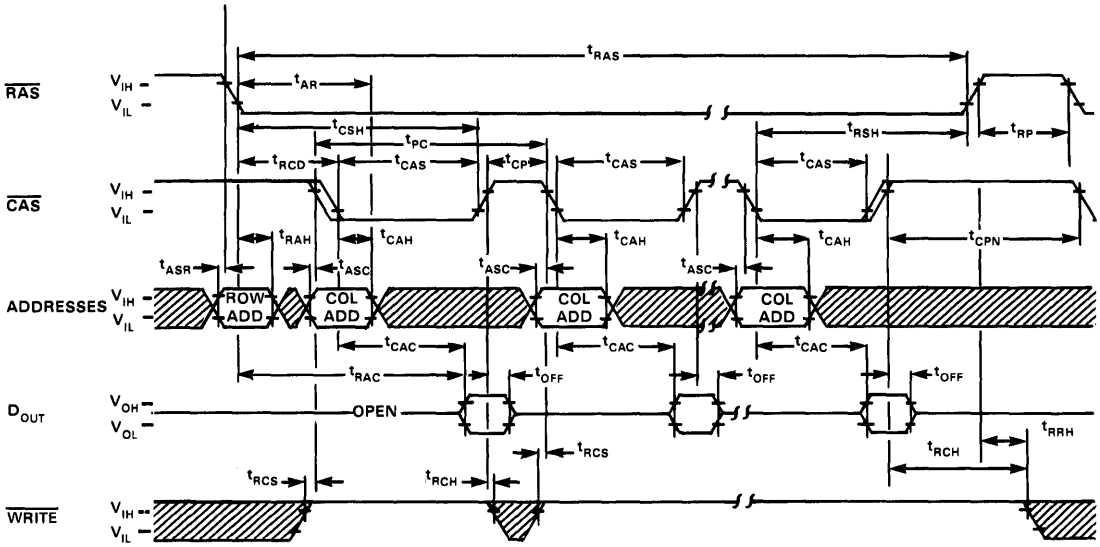
READ-WRITE/READ-MODIFY-WRITE CYCLE



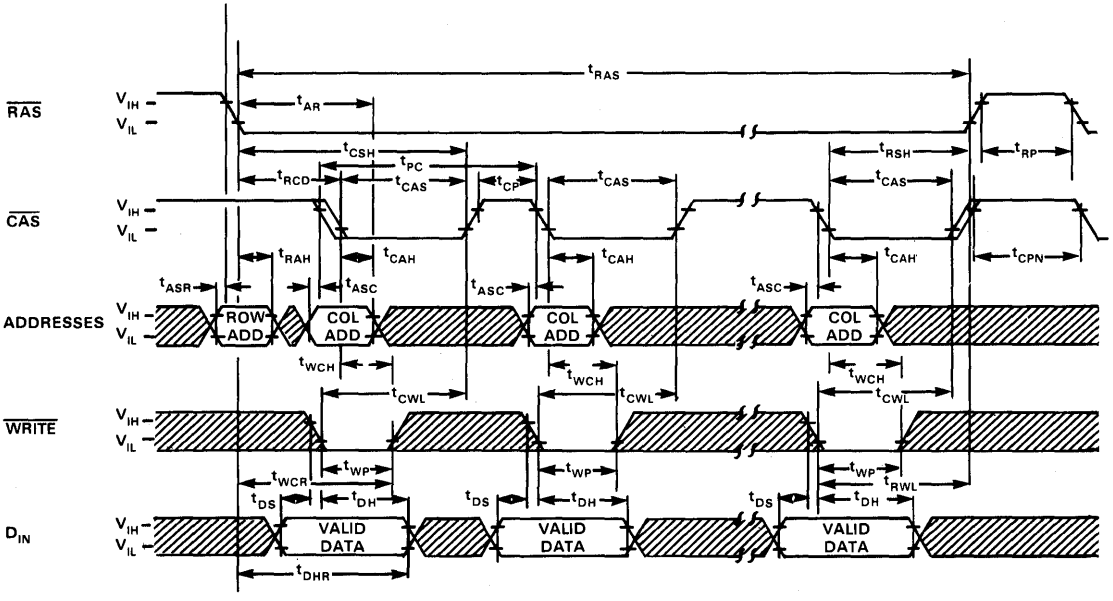
"$\overline{RAS}$-ONLY" REFRESH CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



OPERATION

The eight address bits required to decode 1 of the 65,536 cell locations within the MK4564 are multiplexed onto the eight address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the eight row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the eight column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH} and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$ which are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK4564 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ or $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle the $\overline{WRITE}$ signal should be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK4564 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive) the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MK4564 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK4564 this results in approximately a 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK4564 is limited to the 256 column locations determined by all combinations of the eight column address bits. Operations within the page boundary need not be sequentially addressed and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

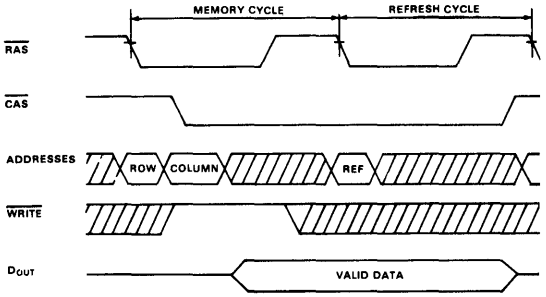
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 row addresses within each 2ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that a 7 bit refresh address (A0-A6) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time that $\overline{RAS}$ is asserted, the output port will remain in the same state that it was prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)



65,535 × 1-BIT DYNAMIC RAM
MK45H64(P/N/J/E)-8/10/12

FEATURES

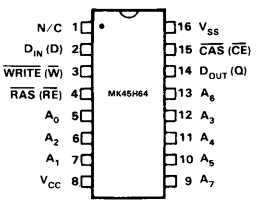
- Recognized industry standard 16-pin configuration from Mostek
- Single +5V (± 10%) supply operation
- On chip substrate bias generator for optimum performance
- Low power: 330 mW active, max (-10)
  22 mW standby, max
- 80 ns access time, 145 ns cycle time (MK45H64-8)
  100 ns access time, 175 ns cycle time (MK45H64-10)
  120 ns access time, 210 ns cycle time (MK45H64-12)
- Fast page mode cycle time, 100 nsec for -10
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write, and Page-Mode capabilities
- All inputs TTL compatible, low capacitance, and protected against static discharge.
- 128 refresh cycles (2 msec)
  Pin 9 is not needed for refresh

PIN FUNCTIONS

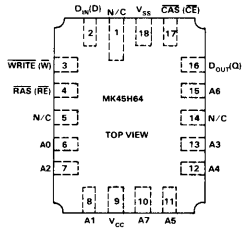
A_0-A_7	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/ Write Input
D_{IN} (D)	Data In	V_{CC}	Power (5V)
D_{OUT} (Q)	Data Out	V_{SS}	GND
		N/C	Not Connected

PIN OUT

DUAL-IN-LINE PACKAGE



LEADLESS CHIP CARRIER



DESCRIPTION

The MK45H64 is a second generation, 64K dynamic RAM. Organized as 65,536 words by 1 bit, it is optimized for high speed, minimum cycle time applications such as video and graphics memory, buffer memory, and mainframe memory. The MK45H64 utilizes Mostek's latest scaled NMOS process technology for maximum circuit density, wide operating margins, and optimum reliability. Some features of this process include silicon gate, double layer poly interconnect, 1.5 μ channel lengths, and 200 Å capacitor oxide for maximum critical charge.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MK45H64 to be packaged in a standard 16-pin DIP with only 15 pins required for basic functionality. The MK45H64 is designed to be compatible with the JEDEC standards for the 64K x 1 dynamic RAM.

The MK45H64 features very fast page mode cycle times (equal to $\overline{RAS}$ access). Additionally, TRAS (max) is specified at 40 μsec to allow an entire page of 256 bits to be accessed within a single $\overline{RAS}$ cycle.

The output of the MK45H64 can be held valid up to 40 μsec by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

PRELIMINARY

262,144 x 1-BIT DYNAMIC RAM
MK45H56(P/N/E)-8/10/12

FEATURES

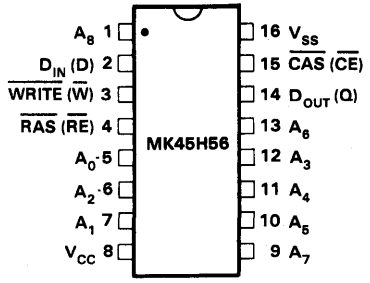
- Recognized industry standard 16-pin configuration from Mostek
- Single +5V (± 10%) supply operation
- On-chip substrate bias generator for optimum performance
- Low power: 412 mW active, max
  22 mW standby, max
- 80 ns access time, 145 ns cycle time (MK45H56-8)
  100 ns access time, 175 ns cycle time (MK45H56-10)
  120 ns access time, 210 ns cycle time (MK45H56-12)
- Fast page mode cycle time, 100 ns for -10
- Extended D_{OUT} hold using $\overline{CAS}$ control (Hidden Refresh)
- Common I/O capability using "early write"
- Read, Write, Read-Write, Read-Modify-Write, and Page-Mode capability
- All inputs TTL compatible, low capacitance, and protected against static discharge
- 256 refresh cycles (4 ms)
  Pin 1 is not needed for refresh

PIN FUNCTIONS

A_0-A_8	Address Inputs	$\overline{RAS}$ ($\overline{RE}$)	Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$)	Column Address Strobe	$\overline{WRITE}$ ($\overline{W}$)	Read/ Write Input
D_{IN} (D)	Data In	V_{CC}	Power (5V)
D_{OUT} (Q)	Data Out	V_{SS}	GND

PIN OUT

DUAL-IN-LINE PACKAGE



DESCRIPTION

The MK45H56 is a 256K dynamic RAM, organized as 262,144 words by 1 bit. It is optimized for high speed, minimum cycle time applications such as video and graphics memory, buffer memory, and mainframe memory. The MK45H56 utilizes Mostek's latest scaled NMOS process technology for maximum circuit density, wide operating margins, and optimum reliability. Some features of this process include silicon gate, double layer metal and poly interconnects, 1.5 micron channel lengths, and 200 A capacitor oxide for maximum critical charge.

Multiplexed address inputs (a feature dating back to the industry standard MK4096, 1973) permit the MK45H56 to be packaged in a standard 16-pin DIP. The MK45H56 is designed to be compatible with the JEDEC standards for the 256K x 1 dynamic RAM.

The MK45H56 features very fast page mode cycle times (equal to RAS access). Additionally, t_{RAS} (max) is specified at 40 μs to allow an entire page of data to be accessed within a single RAS cycle.

The output of the MK45H56 can be held valid up to 40 μs by holding $\overline{CAS}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as Hidden Refresh.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... -1.0 V to +7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ceramic) ..... -65°C to +150°C
Storage Temperature (Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Data Out Current ..... 50 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq 70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) Voltage, All Inputs	2.4	—	V_{CC}+1	V	1
V_{IL}	Input Low (Logic 0) Voltage, All Inputs	-2.0	—	.8	V	1,18

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0 V ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average power supply operating current (RAS, CAS cycling; t_{RC} = 175 ns)		75	mA	2
I_{CC2}	STANDBY CURRENT Power supply standby current (RAS = V_{IH}, D_{OUT} = High Impedance)		4	mA	
I_{CC3}	RAS ONLY REFRESH CURRENT Average power supply current, refresh mode (RAS cycling, CAS = V_{IH}; t_{RC} = 175 ns)		60	mA	2
I_{CC4}	PAGE MODE CURRENT Average power supply current, page mode operation (RAS = V_{IL}, t_{RAS} = t_{RAS} max., CAS cycling; t_{PC} = t_{PC} min.)		50	mA	2
$I_{I(L)}$	INPUT LEAKAGE Input leakage current, any input ($0V \leq V_{IN} \leq V_{CC}$), all other pins not under test = 0 volts	-10	10	µA	
$I_{O(L)}$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0V \leq V_{OUT} \leq V_{CC}$)	-10	10	µA	
V_{OH} V_{OL}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -5 mA) Output Low (Logic 0) voltage (I_{OUT} = 4.2 mA)	2.4	 0.4	V V	

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500 μs is required after power-up, followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} min. and V_{IL} max. are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Load = 2 TTL loads and 100 pF.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
10. t_{OFF} max. defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
11. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
14. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in READ/WRITE and READ/MODIFY/WRITE cycles only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an EARLY WRITE cycle, and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a READ/WRITE, and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.
15. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
16. Capacitance with Boonton meter or effective capacitance calculated from the equation $C = \frac{I\,\Delta t}{\Delta V}$ with Δ V = 3 volts and power supply at nominal level.
17. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.
18. Includes the DC level and all instantaneous signal excursions.
19. $\overline{WRITE}$ = don't care. Data out depends on the state of $\overline{CAS}$. If $\overline{CAS}$ = V_{IH}, data output is high impedance. If $\overline{CAS}$ = V_{IL}, the data output will contain data from the last valid read cycle.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(3,4,5,15) (0°C ≤T_A ≤ 70°C), V_{CC} = 5.0V ± 10%

SYMBOL			MK45H56-8		MK45H56-10		MK45H56-12			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RELREL}	t_{RC}	Random read or write cycle time	145		175		210		ns	6,7
t_{RELREL}	t_{RMW}	Read-modify-write cycle time	166		200		239		ns	6,7
(RMW)	t_{RW}	Read-write cycle time	149		180		216			
t_{RELREL} (PC)	t_{PC}	Page mode cycle time	80		100		120		ns	6,7
t_{RELQV}	t_{RAC}	Access time from $\overline{RAS}$		80		100		120	ns	7,8
t_{CELQV}	t_{CAC}	Access time from $\overline{CAS}$		45		55		65	ns	7,9
t_{CEHQZ}	t_{OFF}	Output buffer turn-off delay	0	30	0	30	0	35	ns	10
t_T	t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	5,15
t_{REHREL}	t_{RP}	$\overline{RAS}$ precharge time	55		65		80		ns	
t_{RELREH}	t_{RAS}	$\overline{RAS}$ pulse width	80	40,000	100	40,000	120	40,000	ns	
t_{CELREH}	t_{RSH}	$\overline{RAS}$ hold time	45		55		65		ns	
t_{RELCEH}	t_{CSH}	$\overline{CAS}$ hold time	80		100		120		ns	
t_{CELCEH}	t_{CAS}	$\overline{CAS}$ pulse width	45	40,000	55	40,000	65	40,000	ns	
t_{RELCEL}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	8	35	10	45	12	55	ns	11
t_{REHWX}	t_{RRH}	Read command hold time referenced to $\overline{RAS}$	0		0		0		ns	12
t_{AVREL}	t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RELAX}	t_{RAH}	Row address hold time	8		10		12		ns	
t_{AVCEL}	t_{ASC}	Column address set-up time	0		0		0		ns	
t_{CELAX}	t_{CAH}	Column address hold time	12		15		18		ns	

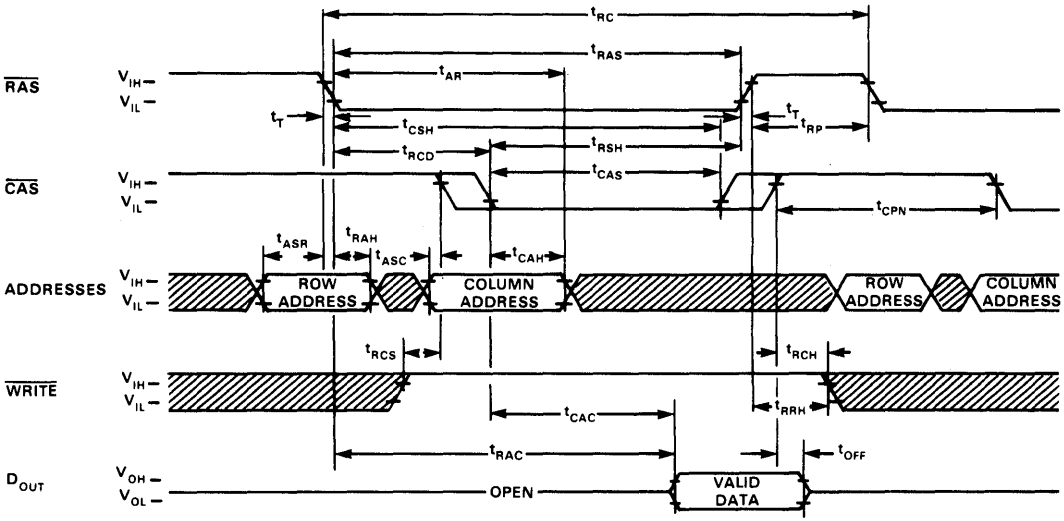
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
(3,4,5,15) ($0°C \leq T_A \leq 70°C$), $V_{CC} = 5.0V \pm 10\%$

SYMBOL			MK45H56-8		MK45H56-10		MK45H56-12			
STD	ALT	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
$t_{RELA(C)X}$	t_{AR}	Column address hold time referenced to $\overline{RAS}$	47		60		73		ns	
t_{WHCEL}	t_{RCS}	Read command set-up time	0		0		0		ns	
t_{CEHWX}	t_{RCH}	Read command hold time referenced to $\overline{CAS}$	0		0		0		ns	12
t_{CELWX}	t_{WCH}	Write command hold time	16		20		24		ns	
t_{RELWX}	t_{WCR}	Write command hold time referenced to $\overline{RAS}$	51		65		79		ns	
t_{WLWH}	t_{WP}	Write command pulse width	10		10		12		ns	
t_{WLREH}	t_{RWL}	Write command to $\overline{RAS}$ lead time	16		20		24		ns	
t_{WLCEH}	t_{CWL}	Write command to $\overline{CAS}$ lead time	20		24		28		ns	
t_{DVCEL}	t_{DS}	Data-in set-up time	0		0		0		ns	13
t_{CELDX}	t_{DH}	Data-in hold time	16		20		24		ns	13
t_{RELDX}	t_{DHR}	Data-in hold time referenced to $\overline{RAS}$	51		65		79		ns	
t_{CEHCEL} (PC)	t_{CP}	$\overline{CAS}$ precharge time (for page-mode cycle only)	25		35		45		ns	
t_{RVRV}	t_{REF}	Refresh Period		4		4		4		ms
t_{WLCEL}	t_{WCS}	$\overline{WRITE}$ command set-up time	0		0		0		ns	14
t_{CELWL}	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	28		35		42		ns	14
t_{RELWL}	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ delay	63		80		97		ns	14
t_{CEHCEL}	t_{CPN}	$\overline{CAS}$ precharge time	15		20		25		ns	

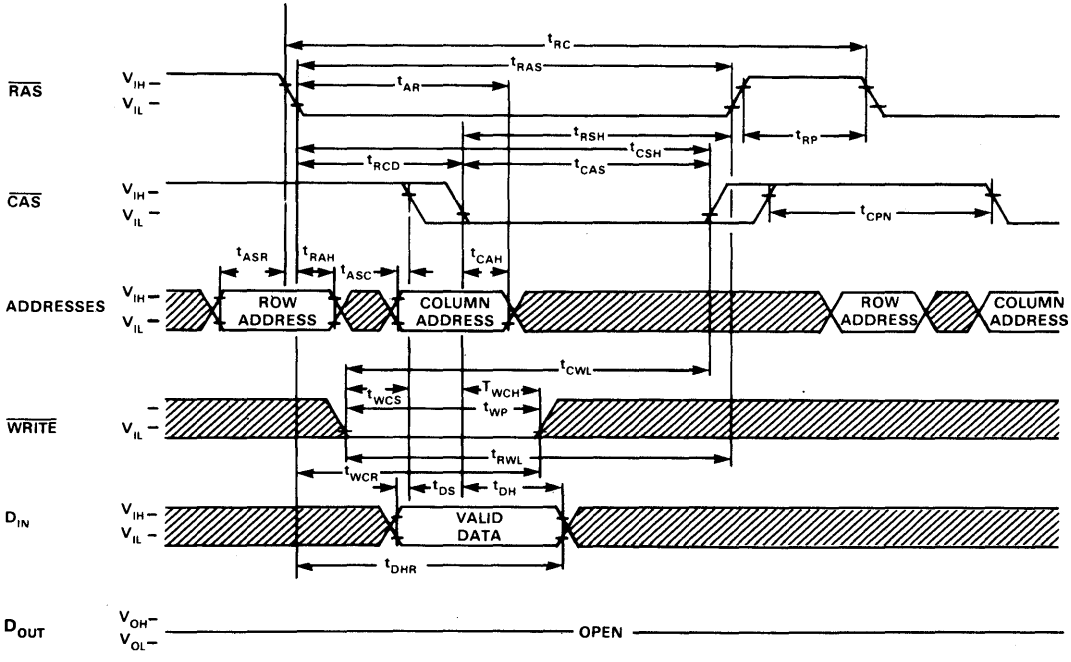
AC ELECTRICAL CHARACTERISTICS
($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYM	PARAMETER	MAX	UNITS	NOTES
C_{I1}	Input Capacitance (A_0 - A_8), D_{IN}	5	pF	16
C_{I2}	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	5	pF	16
C_O	Output Capacitance (D_{OUT})	7	pF	16,17

READ CYCLE

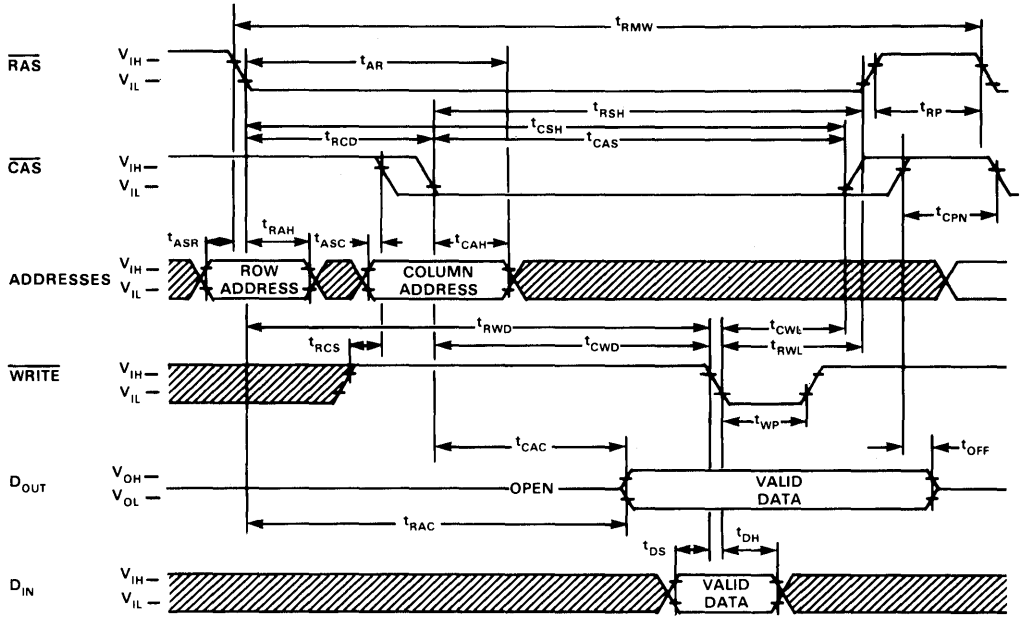


WRITE CYCLE (EARLY WRITE)

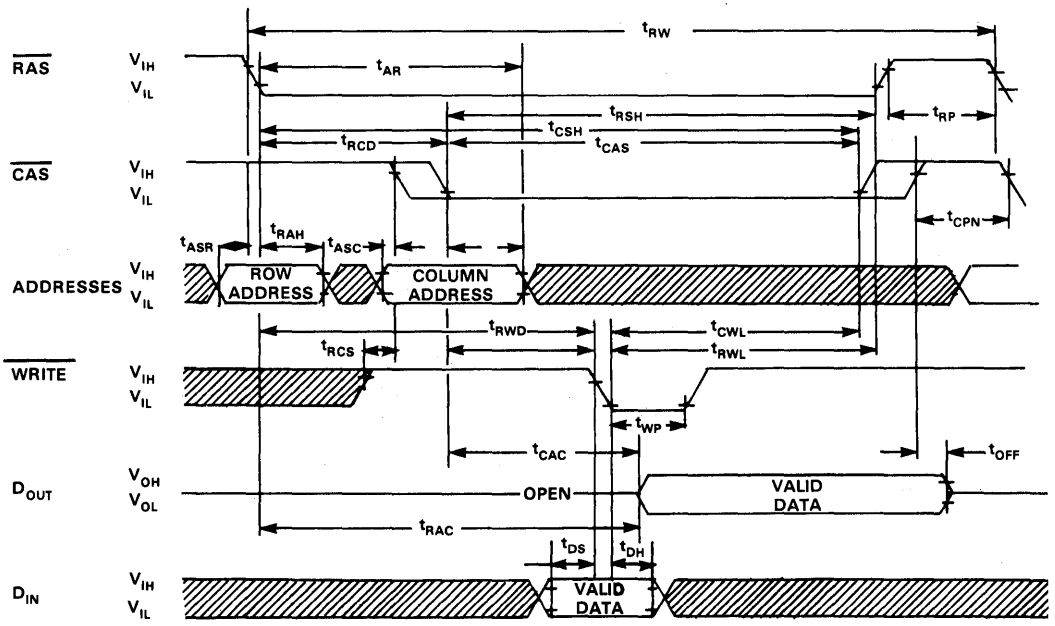


IV

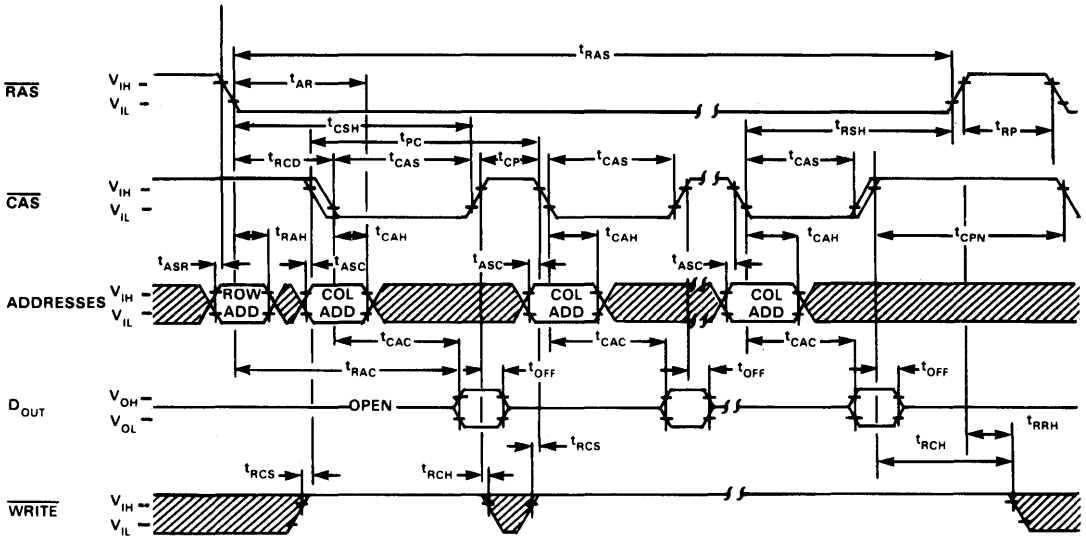
READ-MODIFY-WRITE CYCLE



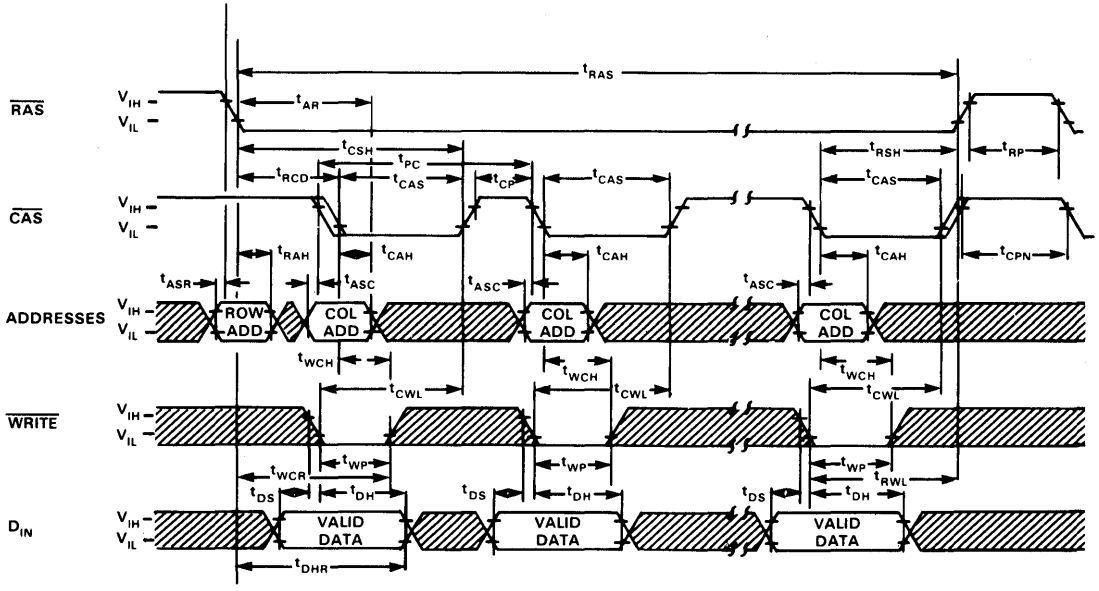
READ-WRITE CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



IV

OPERATION

The 18 address bits required to decode one of the 262,144 cell locations within the MK45H56 are multiplexed onto the nine address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, Row Address Strobe ($\overline{RAS}$), latches the nine row addresses into the chip. The high-to-low transition of the second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the nine column addresses into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events that are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical timing path for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold specification (t_{RAH}) has been satisfied and the address inputs have been changed from Row address to Column address information.

The "gated $\overline{CAS}$" feature permits $\overline{CAS}$ to be activated at any time after t_{RAH}, and it will have no effect on the worst case data access time (t_{RAC}) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing endpoints result from the internal gating of $\overline{CAS}$, and they are called t_{RCD} (min) and t_{RCD} (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the MK45H56 at a point in time beyond the t_{RCD} (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ (t_{CAC}) rather than from $\overline{RAS}$ (t_{RAC}), and $\overline{RAS}$ access time will be lengthened by the amount that t_{RCD} exceeds the t_{RCD} (max) limit.

DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The latter of $\overline{WRITE}$ and $\overline{CAS}$ to make its negative transition is the strobe for the Data In (D_{IN}) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$ being brought low (active), the D_{IN} is strobed by $\overline{CAS}$, and the Input Data set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time (late write) or if it is desired that the cycle be a read-write or read-modify-write cycle, the $\overline{WRITE}$ signal should be delayed until $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$.

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which both the $\overline{RAS}$ and $\overline{CAS}$ are low (active). Data read from the selected cell is available at the output port within the specified access time. The output data is the same polarity (not inverted) as the input data.

DATA OUTPUT CONTROL

The normal condition of the Data Output (D_{OUT}) of the MK45H56 is the high impedance (open-circuit) state; anytime $\overline{CAS}$ is high (inactive), the D_{OUT} pin will be floating. Once the output data port has gone active, it will remain valid until $\overline{CAS}$ is taken to the precharge (inactive high) state.

PAGE MODE OPERATION

The Page Mode feature of the MK45H56 allows for successive memory operations at multiple column locations within the same row address. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal low (active) throughout all successive memory cycles in which the row address is common. The first access within a page mode operation will be available at t_{RAC} or t_{CAC} time, whichever is the limiting parameter. However, all successive accesses within the page mode operation will be available at t_{CAC} time (referenced to $\overline{CAS}$). With the MK45H56, this results in an approximate 45% improvement in access times. Effective memory cycle times are also reduced when using page mode.

The page mode boundary of a single MK45H56 is limited to the 512 column locations determined by all combinations of the nine column address bits. Operations within the page boundary need not be sequentially addressed, and any combination of read, write, and read-modify-write cycles is permitted within the page mode operation.

REFRESH

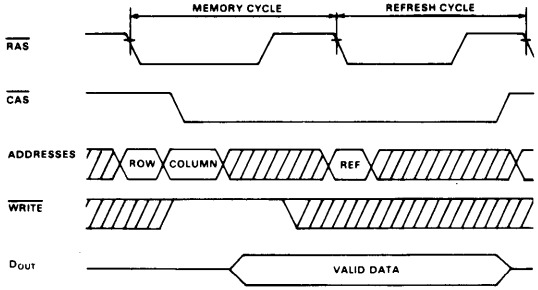
Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 256 row addresses within each 4 ms interval. Although any normal memory cycle will perform the required refreshing, this function is most easily accomplished with "$\overline{RAS}$-only" cycles.

The $\overline{RAS}$-only refresh cycle requires that an 8-bit refresh address (A0-A7) be valid at the device address inputs when $\overline{RAS}$ goes low (active). The state of the output data port during a $\overline{RAS}$-only refresh is controlled by $\overline{CAS}$. If $\overline{CAS}$ is high (inactive) during the entire time that $\overline{RAS}$ is asserted, the output will remain in the high impedance state. If $\overline{CAS}$ is low (active) the entire time the $\overline{RAS}$ is asserted, the output port will remain in the same state as prior to the issuance of the $\overline{RAS}$ signal. If $\overline{CAS}$ makes a low-to-high transition during the $\overline{RAS}$-only refresh cycle, the output data buffer will assume the high impedance state. However, $\overline{CAS}$ may not make a high to low transition during the $\overline{RAS}$-only refresh cycle since the device interprets this as a normal $\overline{RAS}/\overline{CAS}$ (read or write) type cycle.

HIDDEN REFRESH

A $\overline{RAS}$-only refresh cycle may take place while maintaining valid output data by extending the $\overline{CAS}$ active time from a previous memory read cycle. This feature is referred to as a hidden refresh. (See figure below.)

HIDDEN REFRESH CYCLE (SEE NOTE 19)



PRELIMINARY

32K x 8-BIT DYNAMIC RAM
MK4856 (N/P/J/E) - 10/12/15

FEATURES

- □ LD³ ™ Technology
- □ Single +5 V (± 10%) Supply Operation
- □ On-Chip Substrate Bias Generator
- □ Low Power 275 mW active, max
  27.5 mW standby, max
- □ 100 ns Access Time (MK4856-10)
- □ 120 ns Access Time (MK4856-12)
- □ 150 ns Access Time (MK4856-15)
- □ Extended Data Output Using G control
- □ Hidden Refresh
- □ Read, Write, Read-Modify-Write capability
- □ All inputs TTL compatible, low capacitance, and protected against static charge
- □ 256 Refresh Cycles (4msec)
- □ Non-Multiplexed for easy user interface
- □ Density Extension of JEDEC standard 28-pin static RAM family

PIN FUNCTIONS

A_0 - A_{14}	Address Inputs
DQ_0 - DQ_7	Data Input/Output
$\overline{E}$	Chip Enable/Address Strobe
$\overline{G}$	Output/Refresh Control
$\overline{W}$	Read/Write Input
V_{CC}	Power (+5)
V_{SS}	Ground

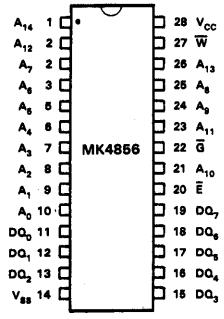
DESCRIPTION

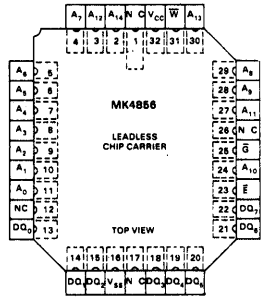
The MK4856 is the new generation, dynamic RAM. Organized 32,768 words by 8 bits, it is the successor to the industry standard 64K x 1. The MK4856 utilizes Mostek's LD³ ™ process technology as well as advanced circuit techniques to provide wide operating margins, both internally and to the system user. The use of dynamic circuitry throughout, and a novel sense amplifier scheme, assures maximum device signal margins while maintaining high performance. Refresh characteristics have been chosen to minimize external interface circuitry.

The output of the MK4856 can be held valid up to 10 μsec by holding $\overline{G}$ active low. This is quite useful since refresh cycles can be performed while holding data valid from a previous cycle. This feature is referred to as hidden refresh.

PIN CONNECTION

Figure 1





ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} supply relative to V_{SS} ..... - 1.0 V to 7.0 V
Operating Temperature, T_A (Ambient) ..... 0°C to + 70°C
Storage Temperature (Ceramic) ..... - 65°C to + 150°C
Storage Temperature (Plastic) ..... - 55°C to + 125°C
Power Dissipation ..... 1 watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High (Logic 1) voltage, All Inputs	2.4	—	V_{CC} + 1	V	1
V_{IL}	Input Low (logic 0) voltage, All Inputs	-2.0	—	0.8	V	1,12

AC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 volts ± 10%)

SYMBOL	PARAMETER	TYP	MAX	NOTES
C_{IN1}	Input Capacitance A_0 - A_{14}		5 pF	10
C_{IN2}	Input Capacitance $\overline{E}$, $\overline{G}$, $\overline{W}$,		10 pF	10
C_{DQ}	Input/output capacitance of DQ		8 pF	10,11

DC ELECTRICAL CHARACTERISTICS
(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0 V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	OPERATING CURRENT Average Power supply operating current ($\overline{E}$ cycling; t_{RC} = t_{RC} min)		50	mA	2
I_{CC2}	STANDBY CURRENT Power supply standby current ($\overline{E}$ = V_{IH}; DQ = High Impedance)		5	mA	2
I_{CC3}	$\overline{G}$ BEFORE $\overline{E}$ REFRESH CURRENT Average power supply current; refresh mode ($\overline{E}$ cycling; t_{RC} = t_{RC} min)		50	mA	2,13
I_{CC4}	$\overline{G}$ BEFORE $\overline{E}$ REFRESH CURRENT Average power supply current; Hidden refresh mode ($\overline{E}$ cycling; t_{RC} = t_{RC} (min), DQ active)		50	mA	2,14

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC5}	$\overline{E}$ ONLY REFRESH CURRENT Average power supply current, refresh mode ($\overline{E}$ cycling; $t_{RC} = t_{RC}$ (min); $\overline{W} = V_{IH}$; $\overline{G} = V_{IH}$)		50	mA	2
$I_I(L)$	INPUT LEAKAGE Input leakage current, any input ($0\ V \leq V_{IN} \leq V_{CC}$, all other pins not under test = 0 V)	-10	10	μA	
$I_O(L)$	OUTPUT LEAKAGE Output leakage current (D_{OUT} is disabled, $0\ V \leq V_{OUT} \leq V_{CC}$)	-10	10	μA	
V_{OH}	OUTPUT LEVELS Output High (Logic 1) voltage (I_{OUT} = -1 ma)	2.4		V	
V_{OL}	Output Low (Logic 0) voltage (I_{OUT} = 4.2 ma)		0.4	V	

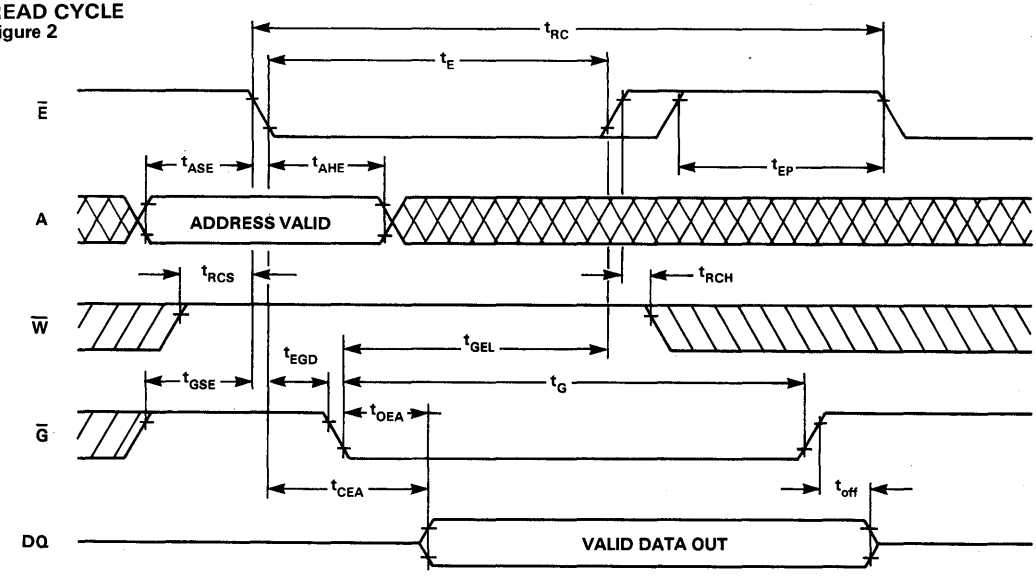
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(3, 4, 5, 6) ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0 \pm 10\%$)

SYMBOL		PARAMETER	MK4856-10		MK4856-12		MK4856-15		UNITS	NOTES
ALT	STD		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	TEL2EL2 (R/W)	Random read or write cycle	180		210		260		ns	7,8
t_{RMW}	TEL2EL2 (RMW)	Read-Modify-Write Cycle Time	260		295		355		ns	7,8
t_{CEA}	TEL1DQV	Chip Enable ($\overline{E}$) Access Time		100		120		150	ns	16
t_{OEA}	TGL1DQV	Output Enable access		30		35		40	ns	
t_{OFF}	TGH2DQZ	Output Buffer turn-off delay	0	40	0	40	0	40	ns	9
t_T	t_T	Transition Time (rise and fall)	3	50	3	50	3	50	ns	6
t_{EP}	TEH2EL2	Chip Enable ($\overline{E}$) precharge time	70 ns	4 ms	80 ns	4 ms	100 ns	4 ms		
t_E	TEL1EH1	Chip Enable ($\overline{E}$) pulse width	100	10,000	120	10,000	150	10,000	ns	
t_G	TGL1GH1	Output Enable pulse width	30	10000	35	10000	40	10000	ns	
t_{ASE}	TAVEL2	Address Set up time	0		0		0		ns	
t_{AHE}	TEL1AX	Address Hold Time	20		20		25		ns	
t_{GSE}	TGH2EL2	Output Enable set up time	0		0		0		ns	
t_{GWD}	TGH2WL2	Output Enable to write delay time	40		40		40		ns	
t_{GEL}	TGL1EH1	Output Enable to Chip Enable Lead Time	0		0		0		ns	
t_{RCS}	TWH2EL2	Read command ($\overline{W}$) set up time	0		0		0		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

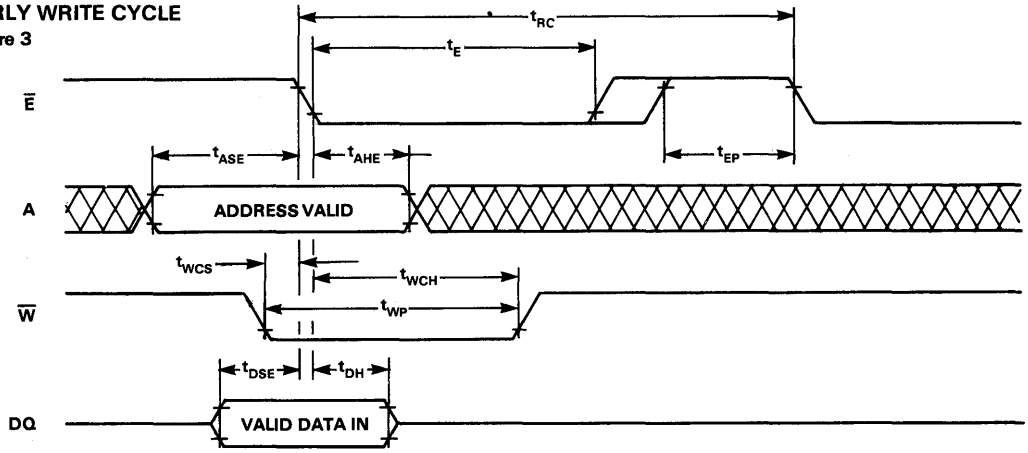
SYMBOL		PARAMETER	MK4856-10		MK4856-12		MK4856-15		UNITS	NOTES
ALT	STD		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RCH}	TEH2WL2	Read Command hold time	0		0		0		ns	
t_{WCS}	TWL1EL2	Write command ($\overline{W}$) set up time for early write	0		0		0		ns	
t_{WCH}	TEL1WH1	Write ($\overline{W}$) hold time	35		40		50		ns	
t_{WP}	TWL1WH1	Write command ($\overline{W}$) pulse width	35		40		50		ns	
t_{WEL}	TWL1EH1	Write command ($\overline{W}$) to chip enable ($\overline{E}$) lead time	35		40		50		ns	
t_{DSE}	TDQVEL2	Data In, Set up Time referenced to E for early write	0		0		0		ns	
t_{DSW}	TDQVWL2	Data In Set Up Time referenced to W for late write	0		0		0		ns	
t_{DH}	TEL1DQX	Data In Hold Time, Early Write	35		40		50		ns	
t_{DHW}	TWL1DQX	Data In hold time, Late Write	20		20		25		ns	
t_{EGD}	TEL1GL2	Chip Enable ($\overline{E}$) to output enable ($\overline{G}$) delay time	30		35		40		ns	
t_{REF}	TRVRV	Refresh Interval		4		4		4	ms	
t_{GSER}	TGL1EL2	Output Enable ($\overline{G}$) set up time for refresh	0		0		0		ns	
t_{GEH}	TEL1GH1	Output Enable ($\overline{E}$) hold time for refresh	30		35		40		ns	

READ CYCLE
Figure 2



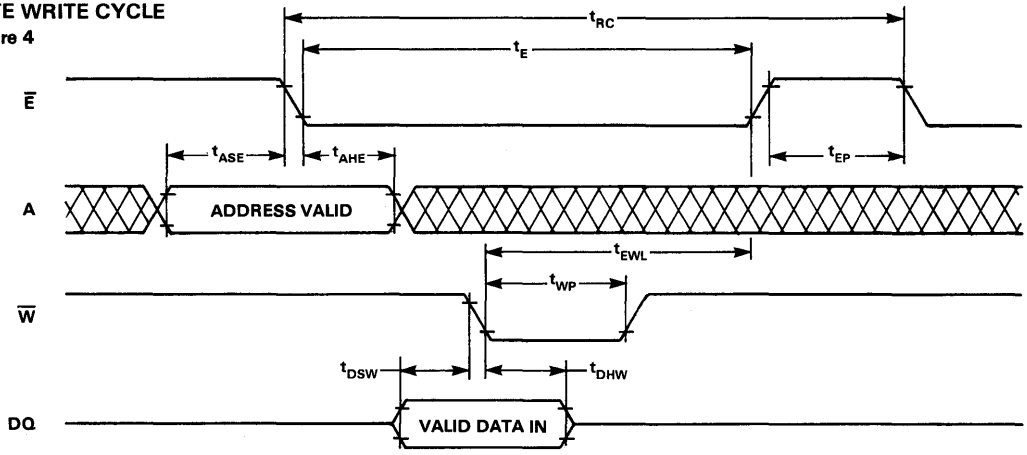
EARLY WRITE CYCLE

Figure 3



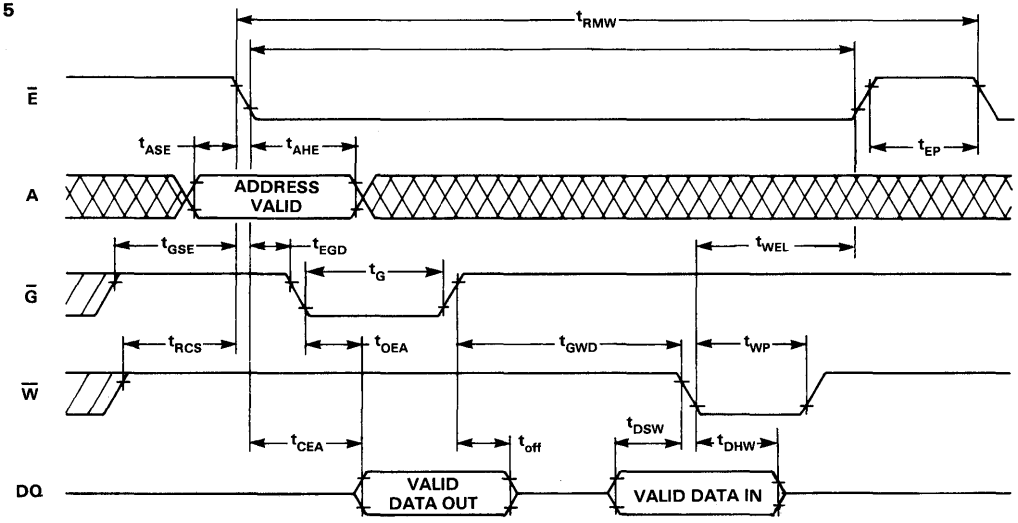
LATE WRITE CYCLE

Figure 4



READ-MODIFY-WRITE CYCLE

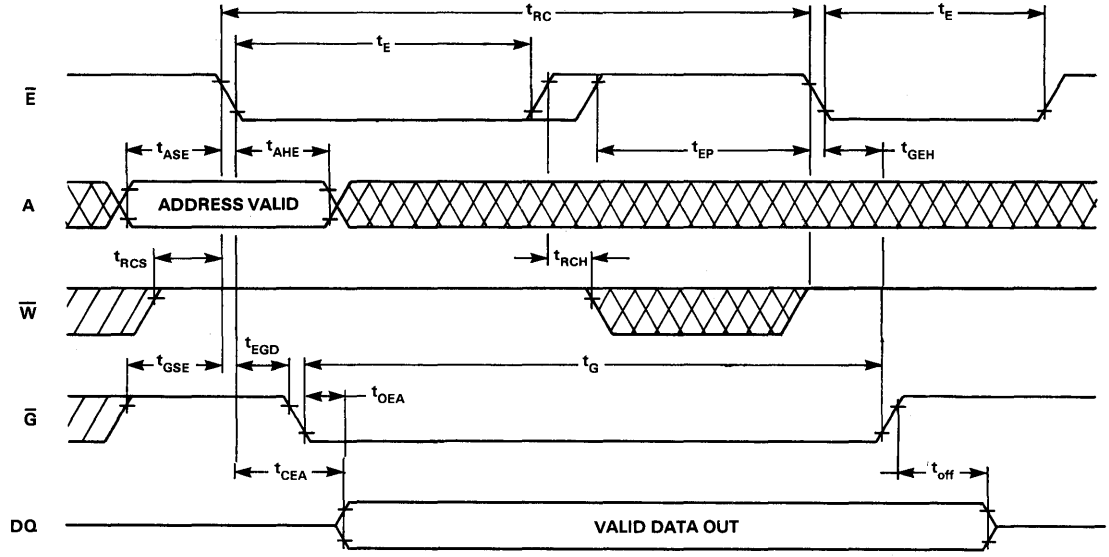
Figure 5



IV

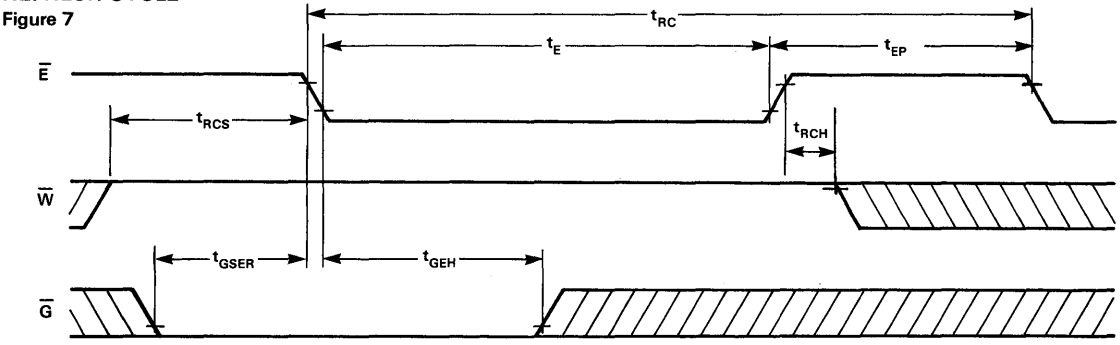
HIDDEN REFRESH CYCLE

Figure 6

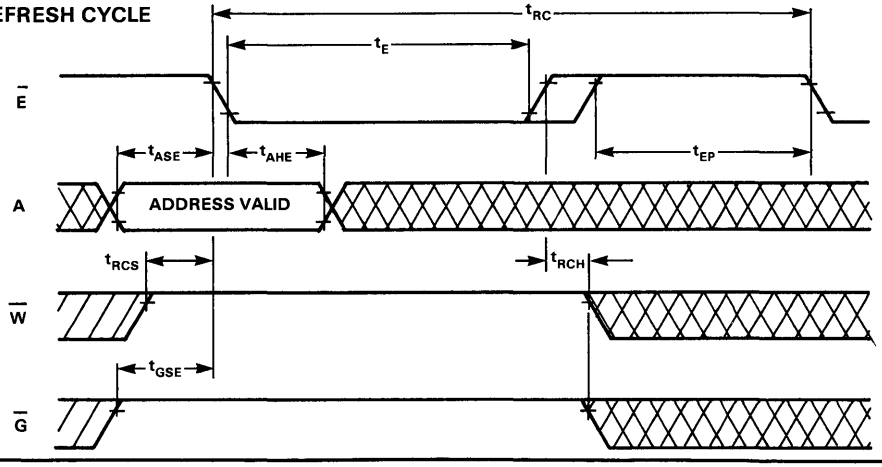


REFRESH CYCLE

Figure 7



CHIP ENABLE REFRESH CYCLE
Figure 8



IV

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
3. An initial pause of 500μs is required after power-up followed by any 8 cycles before proper device operation is achieved. Note that E may be cycled during the intial pause. On chip refresh counter is static and does not require initialization.
4. AC characteristics assume t_T = 5 ns.
5. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. In addition to meeting the transition time specification, all input signals must transit between V_{IH} and V_{IL} (or V_{IL} and V_{IH}) in a monotonic manner.
7. The minimum specifications are used only to indicate cycle times at which proper operation over the full temperature range (0°C $\leq T_A \leq$ 70°C) is assured.
8. Load = 4 ma and 100 pF.
9. t_{off} max defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
10. Capacitance measured with a Boonton meter or equivalent.
11. G = V_{IH} to disable DQ.
12. Includes the DC level and all instantaneous signal excursions.
13. DQ Tri-state prior to $\overline{E}$ going low, DQ remains tri-state through refresh.
14. DQ active prior to $\overline{E}$ going low, DQ determined by $\overline{G}$.
15. Write starts with the later of $\overline{E}$ or $\overline{W}$ going low (except during a refresh cycle).
16. t_{CEA} assumes $t_{OEA} \geq t_{OEA}$ (max).
17. Any memory cycle will refresh a segment of the MK4856. All combinations of address bits A0-A7 (256 memory cycles) are required.

1984/1985 MICROELECTRONIC DATA BOOK

4096 × 1-BIT STATIC RAM
MK4104 (P/J/N) SERIES

FEATURES

- ☐ Combination static storage cells and dynamic control circuitry for truly high performance

PART NUMBER	ACCESS TIME	CYCLE TIME
MK4104-3/-33	200ns	310ns
MK4104-4/-34	250ns	385ns
MK4104-5/-35	300ns	460ns
MK4104-6	350ns	535ns

- ☐ Low Active Power Dissipation: 150mW (Max)
- ☐ Battery backup mode (3V/10mW on -33, -34 and -35)
- ☐ Standby Power Dissipation less than 28 mW (at V_{CC} = 5.5V)
- ☐ Single +5V Power Supply (± 10% tolerance)
- ☐ Fully TTL Compatible

  Fanout: 2 – Standard TTL
  2 – Schottky TTL
  12 – Low Power Schottky TTL

- ☐ Standard 18-pin DIP

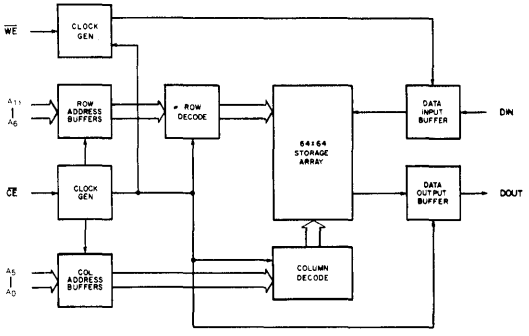
DESCRIPTION

The MOSTEK MK 4104 is a high performance static random access memory organized as 4096 one bit words. The MK 4104 combines the best characteristics of static and dynamic memory techniques to achieve a TTL compatible, 5 volt only, high performance, low power memory device. It utilizes advanced circuit design concepts and an innovative state-of-the-art N-channel silicon gate process specially tailored to provide static data storage with the performance (speed and power) of dynamic RAMs. Since the storage cell is static the device may be stopped indefinitely with the $\overline{CE}$ clock in the off (Logic 1) state.

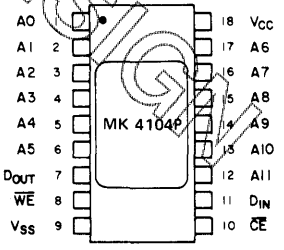
All input levels, including write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) are TTL compatible with a one level of 2.2 volts and a zero level of 0.8 volts. This gives the system designer for a logic "1" state, at least 200mV of noise margin when driven by standard TTL and a minimum of 500mV when used with high performance Schottky TTL. These margins are wider than on most TTL compatible MOS memories available. The push-pull output (no pull-up resistor required) delivers a one level of 2.4V minimum and a zero level of .4 volts maximum. The output has a fanout of 2 standard TTL loads or 12 low power Schottky loads.

The RAM employs an innovative static cell which occupies a mere 2.75 square mils (½ the area of previous cells) and dissipates power levels comparable

FUNCTIONAL DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	V_{SS}	GROUND
$\overline{CE}$	CHIP ENABLE	V_{CC}	POWER (+5V)
D_{IN}	DATA INPUT	$\overline{WE}$	WRITE ENABLE
D_{OUT}	DATA OUTPUT		

DESCRIPTION (Cont'd)

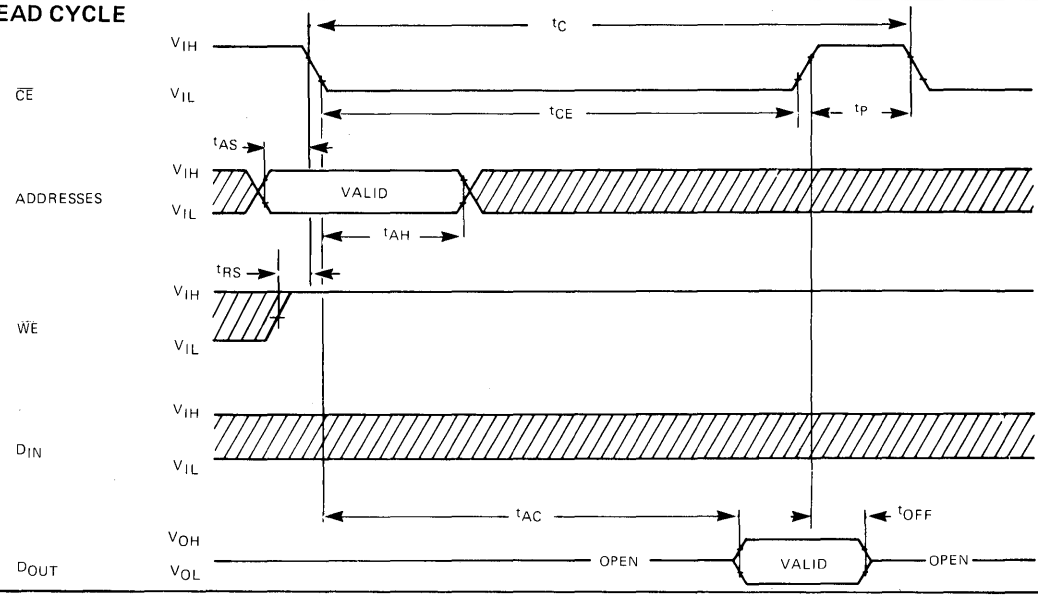
to CMOS. The static cell eliminates the need for refresh cycles and associated hardware thus allowing easy system implementation.

Power supply requirements of +5V ± 10% tolerance combined with TTL compatability on all I/O pins permits easy integration into large memory configurations. The single supply reduces capacitor count and permits denser packaging on printed circuit boards. The 5V only supply requirement and TTL compatible I/O makes this part an ideal choice for next generation +5V only microprocessors such as MOSTEK's MK3880 (Z80). The early write mode ($\overline{WE}$ active prior to $\overline{CE}$) permits common I/O operation, needed for Z80 interfacing, without external circuitry.

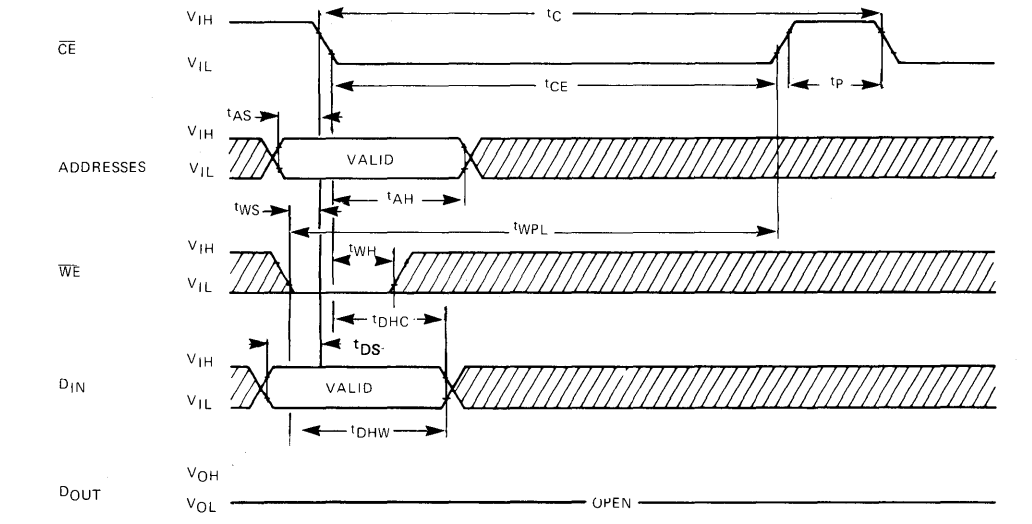
The MK4104-3X series has the added capability of retaining data in a reduced power mode. V_{CC} maybe lowered to 3V with a guaranteed power dissipation of only 10mW maximum. This makes the MK4104 ideal for those applications requiring data retention at the lowest possible power as in battery operation.

Reliability is greatly enhanced by the low power dissipation which causes a maximum junction rise of only at 8°C at 1.86 Megahertz operation. The MK 4104 was designed for the system designer and user who require the highest performance available along with MOSTEK's proven reliability.

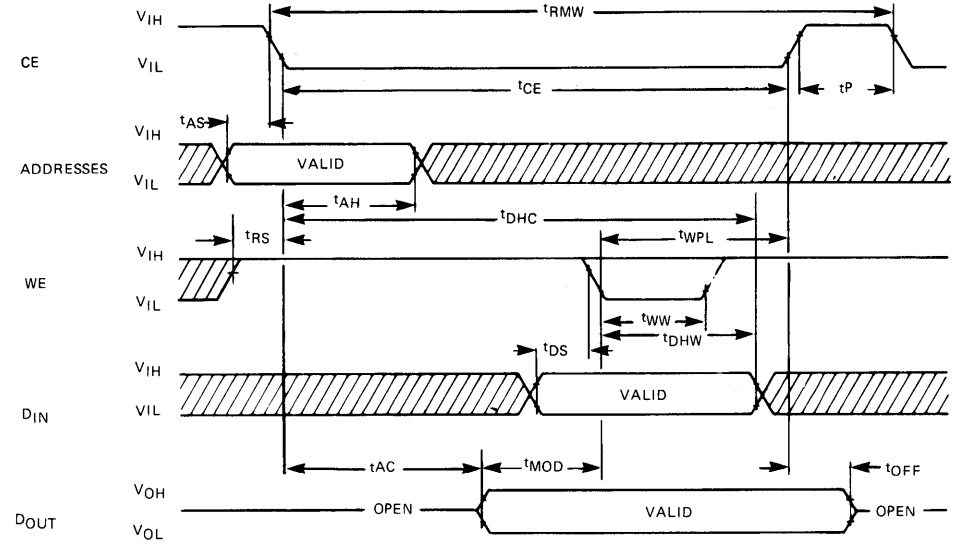
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



OPERATION

READ CYCLE

The circuit offers one bit of the possible 4096 by decoding the 12 address bits presented at the inputs. The address bits are strobed into the chip by the negative-going edge of the Chip Enable ($\overline{CE}$) clock. A read cycle is accomplished by holding the 'write enable' ($\overline{WE}$) input at a high level (V_{IH}) while clocking the $\overline{CE}$ input to a low level (V_{IL}). At access time (t_{AC}) valid data will appear at the output. The output is unlatched by a positive transition of $\overline{CE}$ and therefore will be open circuited (high impedance state) from the previous cycle to access time and will go open again at the end of the present cycle when $\overline{CE}$ goes high.

Once the address hold time has been satisfied, the addresses may be changed for the next cycle.

WRITE CYCLE

Data that is to be written into a selected cell is strobed into the chip on the later occurring negative edge of $\overline{CE}$ or $\overline{WE}$. If the negative transition of $\overline{WE}$ occurs prior to the leading edge of $\overline{CE}$ as in an "early" write cycle then the $\overline{CE}$ input serves as the strobe for data-in. If $\overline{CE}$ leading edge occurs prior to the leading edge of $\overline{WE}$ as in a read-modify-write cycle then data-in is strobed by the $\overline{WE}$ input. Due to the internal timing generator, two independent timing parameters must be satisfied for DI hold time, these are, t_{DHW} and t_{DHC}. For a R/W or RMW cycle t_{DHC} is automatically satisfied making t_{DHW} the more restrictive parameter. For a write only cycle either parameter can be more restrictive depending on the position of $\overline{WE}$ relative to $\overline{CE}$. In any event both parameters must be satisfied.

In an 'early' write cycle the output will remain in an open or high impedance state. In a read-modify write operation the output will go active through the modify and write period until $\overline{CE}$ goes to precharge. If the cycle is such that $\overline{WE}$ goes active after $\overline{CE}$ but before valid data appears on the output (prior to t_{AC}) then the output may not remain open. However, if data-in is valid on the leading edge of $\overline{WE}$, and $\overline{WE}$ occurs prior to the positive transition of $\overline{CE}$ by the minimum lead time t_{WPL}, then valid data will be written into the selected cell. The Data in hold time parameters t_{DHW} and t_{DHC} must be satisfied.

READ-MODIFY-WRITE CYCLE

The read-modify-write (RMW) cycle is no more than an extension of the read and write cycles. Data is read at access time, modified during a period determined by the user and the same or new data written between $\overline{WE}$ active (low) and the rising edge of $\overline{CE}$ (t_{WPL}). Data out will remain valid until the rising edge of $\overline{CE}$. A minimum RMW cycle time can be approximated by the following equation (t_{RMW} = RMW cycle time and t_P = $\overline{CE}$ precharge time).

$$t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3t_T$$

POWER DOWN MODE

In power down data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leq$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −1.0V to +7.0V
Operating Temperature T_A (Ambient) . . . . . 0° C to + 70° C
Storage Temperature (Ambient) (Ceramic) . . . . . −65° C to +150° C
Storage Temperature (Ambient) (Plastic) . . . . . −55° C to +125° C
Power Dissipation . . . . . 1 Watt
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[6]

(0° C ≤ T_A ≤ + 70° C)

	PARAMETER	MK4104 Series MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	Volts	1
V_{SS}	Supply Voltage	0	0	0	Volts	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	Volts	1
V_{IL}	Logic "0" Voltage All Inputs	-1.0		.8	Volts	1

DC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = 5.0 volts ± 10%)

	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		27	mA	2
I_{CC2}	Standby V_{CC} Power Supply Current		5	mA	3
I_{IL}	Input Leakage Current (Any Input)	−10	10	μA	4
I_{OL}	Output Leakage Current	−10	10	μA	3, 5
V_{OH}	Output Logic "1" Voltage I_{OUT}=−500μA	2.4		Volts	
V_{OL}	Output Logic "0" Voltage I_{OUT}= 5mA		0.4	Volts	

AC ELECTRICAL CHARACTERISTICS[1]

(0° C ≤ T_A ≤ + 70° C) (V_{CC} = + 5.0 volts ± 10%)

	PARAMETER	TYP	MAX	NOTES
C_I	Input Capacitance	4pF	6pF	14
C_O	Output Capacitance	6pF	7pF	14

NOTES:

1. All voltages referenced to V_{SS}.
2. I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by:
   I_{CC1} [ma] = $(5t_P + 15(t_C - t_P) + 4720) \div t_C$
   where t_P and t_C are expressed in nanoseconds. Equation is referenced to the -3 device, other devices derate to the same curve.
3. Output is disabled (open circuit), $\overline{CE}$ is at logic 1.
4. All device pins at 0 volts except pin under test at $0 \leq V_{IN} \leq 5.5$ volts.
5. $0V \leq V_{OUT} \leq +5.5V$.
6. During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.
7. Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.
8. If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.
9. Determined by user. Total cycle time cannot exceed t_{CE} max.
10. Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.
11. AC measurements assume t_T = 5ns. Timing points are taken at .8V and 2.0V on inputs and .8V and 2.0V on the output. Transition times are also taken between these levels.
12. $t_C = t_{CE} + t_P + 2t_T$.
13. The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.
14. Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.
15. $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3t_T + t_{MOD}$

AC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[6,11]

($0°C \leq T_A \leq +70°C$) (V_{CC} = + 5.0 volts ± 10%)[1]

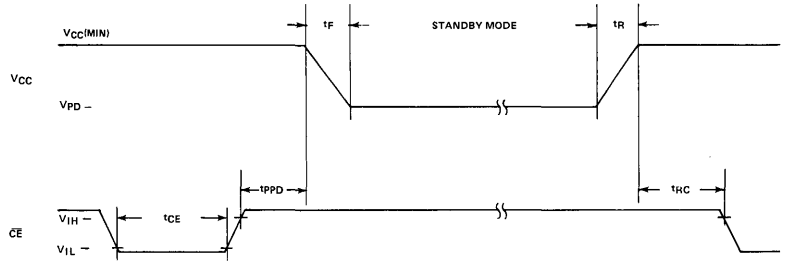
SYMBOL	PARAMETER	MK4104-3/33 MIN	MK4104-3/33 MAX	MK4104-4/34 MIN	MK4104-4/34 MAX	MK4104-5/35 MIN	MK4104-5/35 MAX	MK4104-6 MIN	MK4104-6 MAX	UNITS	NOTES
t_C	Read or Write Cycle Time	310		385		460		535		ns	12
t_{AC}	Random Access		200		250		300		350		7
t_{CE}	Chip Enable Pulse Width	200	10,000	250	10,000	300	10,000	350	10,000		
t_P	Chip Enable Precharge Time	100		125		150		175			
t_{AH}	Address Hold Time	110		135		165		190			
t_{AS}	Address Set-Up Time	0		0		0		0			
t_{OFF}	Output Buffer Turn-Off Delay	0	50	0	65	0	75	0	100		13
t_{RS}	Read Command Set-Up Time	0		0		0		0			8
t_{WS}	Write Enable Set-Up Time	-20		-20		-20		-20			8
t_{DHC}	Data Input Hold Time Referenced to $\overline{CE}$	170		210		250		285			
t_{DHW}	Data Input Hold Time Referenced to $\overline{WE}$	70		90		105		125			
t_{WW}	Write Enabled Pulse Width	60		75		90		105			
t_{MOD}	Modify Time	0	10,000	0	10,000	0	10,000	0	10,000		9
t_{WPL}	$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	70		85		105		120			10
t_{DS}	Data Input Set-Up Time	0		0		0		0			
t_{WH}	Write Enable Hold Time	150		185		225		260			
t_T	Transition Time	5	50	5	50	5	50	5	50		
t_{RMW}	Read-Modify-Write Cycle Time	385		475		570		660			16

STANDBY CHARACTERISTICS

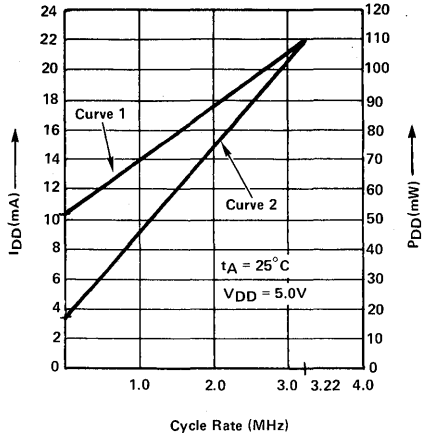
(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MK4104-33 MIN	MK4104-33 MAX	MK4104-34 MIN	MK4104-34 MAX	MK4104-35 MIN	MK4104-35 MAX	UNITS
V_{PD}	V_{CC} In Standby	3.0		3.0		3.0		Volts
I_{PD}	Standby Current		3.3		3.3		3.3	mA
t_F	Power Supply Fall Time	100		100		100		µsec
t_R	Power Supply Rise Time	100		100		100		µsec
t_{CE}	Chip Enable Pulse Width	200		250		300		µsec
t_{PPD}	Chip Enable Precharge To Power Down Time	100		125		150		nsec
V_{IH}	Min CE High "I" Level	2.2		2.2		2.2		Volts
t_{RC}	Standby Recovery Time	500		500		500		µsec

POWER DOWN WAVEFORM



OPERATING POWER VS CYCLE TIME



Characterization data plot of frequency vs power dissipation for a typical MK4104 device.

Curve 1 - Clock on time (low level) is bottom scale minus 100 NSEC

Curve 2 - Clock off time (high level) is bottom scale minus 200 NSEC

1K × 8-BIT STATIC RAM
MK4801A(P/J/N)-1/2/3/4

FEATURES

- □ Static operation
- □ Organization: 1K x 8 bit RAM JEDEC pinout
- □ High performance
- □ Pin compatible with Mostek's BYTEWYDE™ memory family
- □ 24/28 pin ROM/PROM compatible pin configuration
- □ CE and OE functions facilitate bus control
- □ MKB version screened to MIL-STD-883

Part No.	R/W Access Time	R/W Cycle Time
MK4801A-1	120 nsec	120 nsec
MK4801A-2	150 nsec	150 nsec
MK4801A-3	200 nsec	200 nsec
MK4801A-4	250 nsec	250 nsec

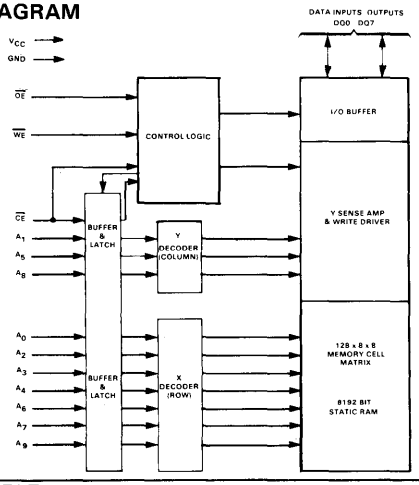
DESCRIPTION

The MK4801A uses Mostek's advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents to the user a high density cost effective N-MOS memory with the performance characteristics necessary for today's microprocessor applications.

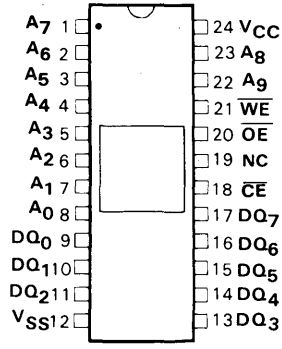
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

CE	OE	WE	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	WE	Write Enable
CE	Chip Enable	OE	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		.8	V	1, 9

DC ELECTRICAL CHARACTERISTICS[1,7]

($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0\ V \pm 5\%$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		50	80	mA	8
I_{IL}	Input Leakage Current (Any Input)	-10		10	μA	2
I_{OL}	Output Leakage Current	-10		10	μA	2
V_{OH}	Output Logic "1" Voltage $I_{OUT} = 1$ mA	2.4			V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 4$ mA			0.4	V	

CAPACITANCE[1,7]

($0°C \leq T_A \leq +70°C$) ($V_{CC} = +5.0\ V \pm 5\%$)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF	6 pF	
$C_{D/Q}$	D/Q pins	10 pF	12 pF	6

C ELECTRICAL CHARACTERISTICS [3,4]

°C ≤ T_A ≤ 70°) (V_{CC} = 5.0 V ± 5%)

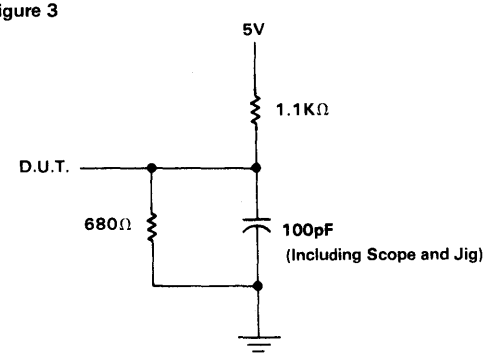
SYM	PARAMETER	-1		-2		-3		-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	120		150		200		250		ns	
t_{AA}	Address Access Time		120		150		200		250	ns	5
t_{CEA}	Chip Enable Access Time		60		75		100		125	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{OEA}	Output Enable Access Time		60		75		100		125	ns	5
t_{OEZ}	Output Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{AZ}	Address Data Off Time	10		10		10		10		ns	
t_{WC}	Write Cycle Time	120		150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		0		ns	see text
t_{AH}	Address Hold Time	40		50		65		80		ns	see text
t_{DSW}	Data To Write Setup Time	10		10		15		20		ns	
t_{DHW}	Data From Write Hold Time	10		10		10		10		ns	
t_{WD}	Write Pulse Duration	45		50		60		70		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	30	5	35	5	40	5	45	ns	
t_{WPL}	Write Pulse Lead Time	75		90		130		170		ns	

V

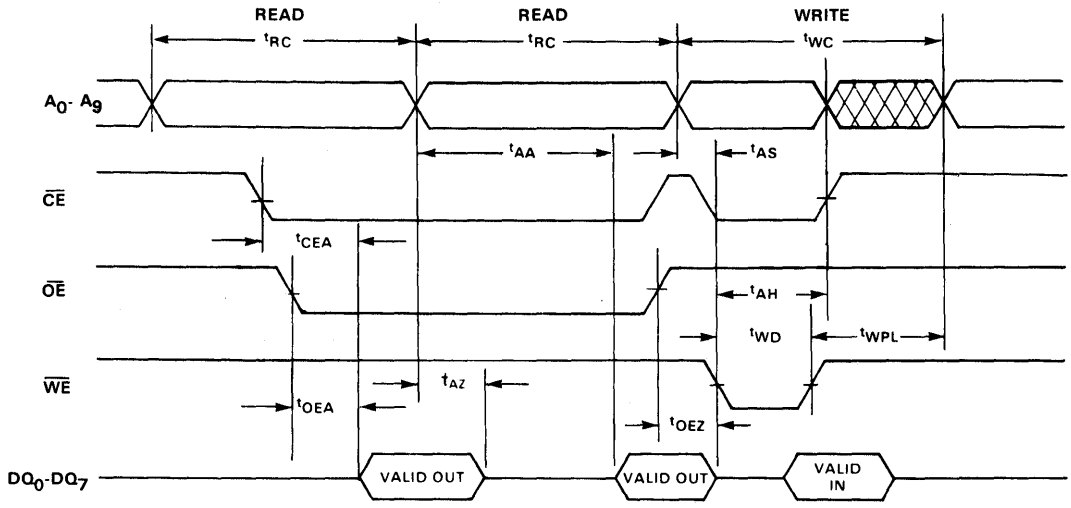
NOTES:
1. All voltages referenced to V_{SS}
2. Measured with .4 ≤ V_I ≤ 5.0 V, outputs deselected and V_{CC} = 5 V
3. AC measurements assume Transition Time = 5 ns, levels V_{SS} to 3.0 V
4. Input and output timing reference levels are at 1.5 V
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC} measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

OUTPUT LOAD

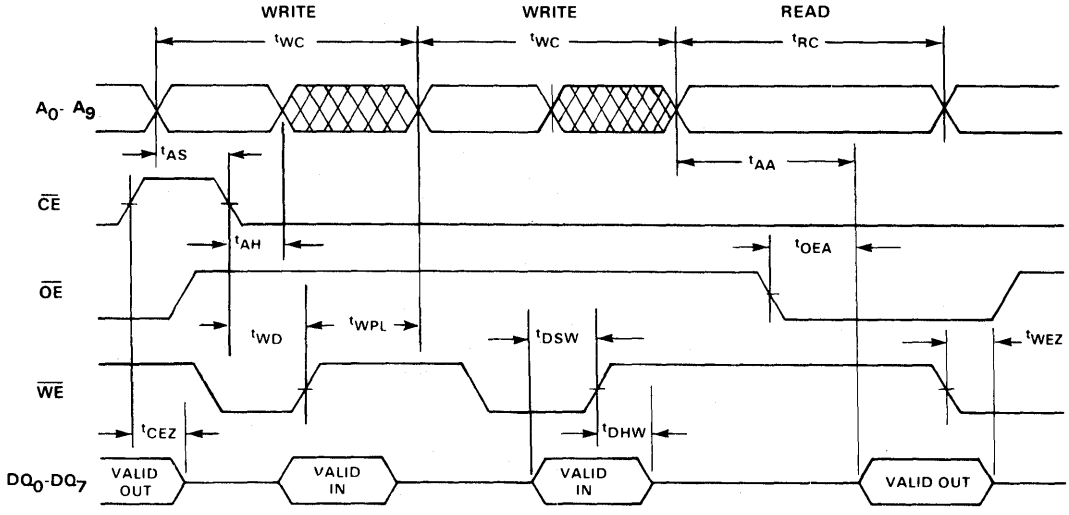
Figure 3



TIMING DIAGRAM
Figure 4



TIMING DIAGRAM
Figure 5



The MK4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs. Mostek also offers a higher performance version of the MK4801A designated the MK4801A.

OPERATION

Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

V

1K × 8-BIT STATIC RAM
MK4801A(P/J/N)-55/70/90

FEATURES

- Static operation
- Organization: 1K x 8 bit RAM JEDEC pinout
- Pin compatible with Mostek's BYTEWYDE™ memory family
- 24/28 pin ROM/PROM compatible pin configuration
- High performance
- $\overline{CE}$ and $\overline{OE}$ functions facilitate bus control

Part No.	Access Time	R/W Cycle Time
MK4801A-55	55 nsec	55/65 nsec
MK4801A-70	70 nsec	70/80 nsec
MK4801A-90	90 nsec	90/100 nsec

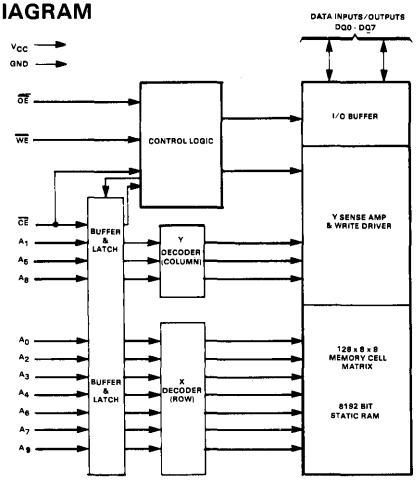
DESCRIPTION

The MK4801A uses Mostek's Scaled POLY 5™ process and advanced circuit design techniques to package 8,192 bits of static RAM on a single chip. Static operation is achieved with high performance and low power dissipation by utilizing Address Activated™ circuit design techniques.

The MK4801A excels in high speed memory applications where the organization requires relatively shallow depth with a wide word format. The MK4801A presents the user a high density cost effective alternative to bipolar and previous generation N-MOS fast memory.

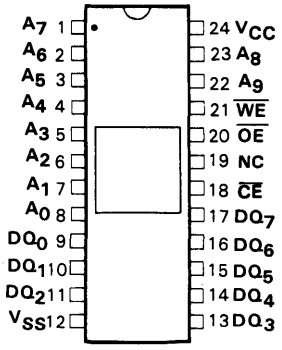
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	DQ
V_{IH}	X	X	Deselect	High Z
V_{IL}	X	V_{IL}	Write	D_{IN}
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
V_{IL}	V_{IH}	V_{IH}	Read	High Z

X = Don't Care

PIN NAMES

A_0-A_9	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable	$\overline{OE}$	Output Enable
V_{SS}	Ground	NC	No Connection
V_{CC}	Power (+5V)	DQ_0-DQ_7	Data In/ Data Out

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -.5V to + 7.0V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient)(Ceramic) ..... -65°C to +150°C
Storage Temperature (Ambient)(Plastic) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current 20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[7]

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.0	5.25	V	1
V_{SS}	Supply Voltage	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		7.0	V	1
V_{IL}	Logic "0" Voltage All Inputs	-2.0		.8	V	1,9

DC ELECTRICAL CHARACTERISTICS[1,7]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 V ± 5%)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		60	125	mA	8
I_{IL}	Input Leakage Current (Any Input)	-10		10	μA	2
I_{OL}	Output Leakage Current	-10		10	μA	2
V_{OH}	Output Logic "1" Voltage I_{OUT} = 1 mA	2.4			V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA			0.4	V	

CAPACITANCE[1,7]

(0°C ≤ T_A ≤ +70°C) (V_{CC} = +5.0 V ± 5%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	All pins (except D/Q)	4 pF	6 pF	
$C_{D/Q}$	D/Q pins	10 pF	12 pF	6

AC ELECTRICAL CHARACTERISTICS [3,4]

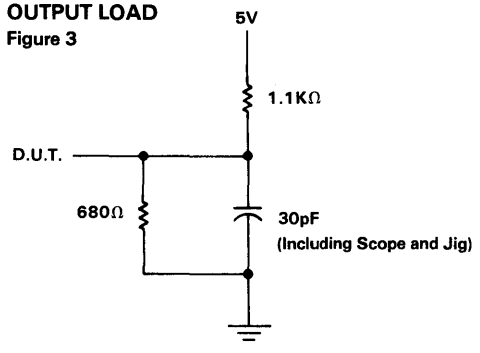
(0°C ≤ T_A ≤ 70°) (V_{CC} = 5.0 V ± 5%)

SYM	PARAMETER	MK4801A-55		MK4801A-70		MK4801A-90		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	55		70		90		ns	
t_{AA}	Address Access Time		55		70		90	ns	5
t_{CEA}	Chip Enable Access Time		25		35		45	ns	5
t_{CEZ}	Chip Enable Data Off Time	5	15	5	20	5	30	ns	
t_{OEA}	Output Enable Access Time		25		35		45	ns	5
t_{OEZ}	Output Enable Data Off Time	5	15	5	20	5	30	ns	
t_{AZ}	Address Data Off Time	10		10		10		ns	
t_{WC}	Write Cycle Time	65		80		100		ns	
t_{AS}	Address Setup Time	0		0		0		ns	see text
t_{AH}	Address Hold Time	15		20		30		ns	see text
t_{DSW}	Data To Write Setup Time	5		5		5		ns	
t_{DHW}	Data From Write Hold Time	10		10		10		ns	
t_{WD}	Write Pulse Duration	25		30		40		ns	see text
t_{WEZ}	Write Enable Data Off Time	5	10	5	15	5	25	ns	
t_{WPL}	Write Pulse Lead Time	40		50		60		ns	

V

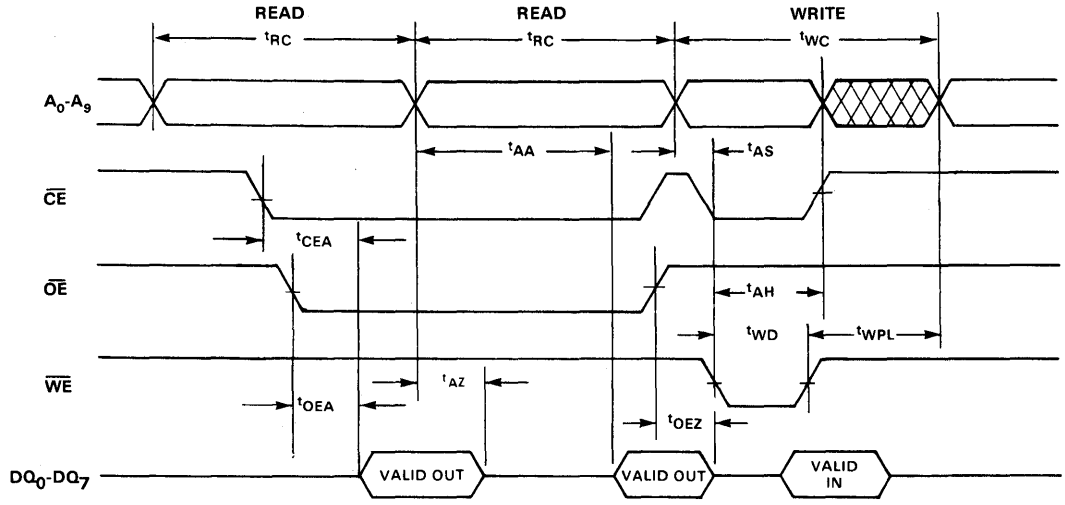
NOTES:
1. All voltages referenced to V_{SS}.
2. Measured with .4 ≤ V_I ≤ 5.0 V, outputs deselected and V_{CC} = 5 V.
3. AC measurements assume Transition Time = 5 ns, levels V_{SS} to 3.0 V.
4. Input and output timing reference levels are at 1.5 V.
5. Measured with a load as shown in Figure 3.
6. Output buffer is deselected.
7. A minimum of 2 ms time delay is required after application of V_{CC} (+5 V) before proper device operation can be achieved.
8. I_{CC} measured with outputs open.
9. Negative undershoots to a minimum of -1.5 V are allowed with a maximum of 50 ns pulse width.

OUTPUT LOAD
Figure 3



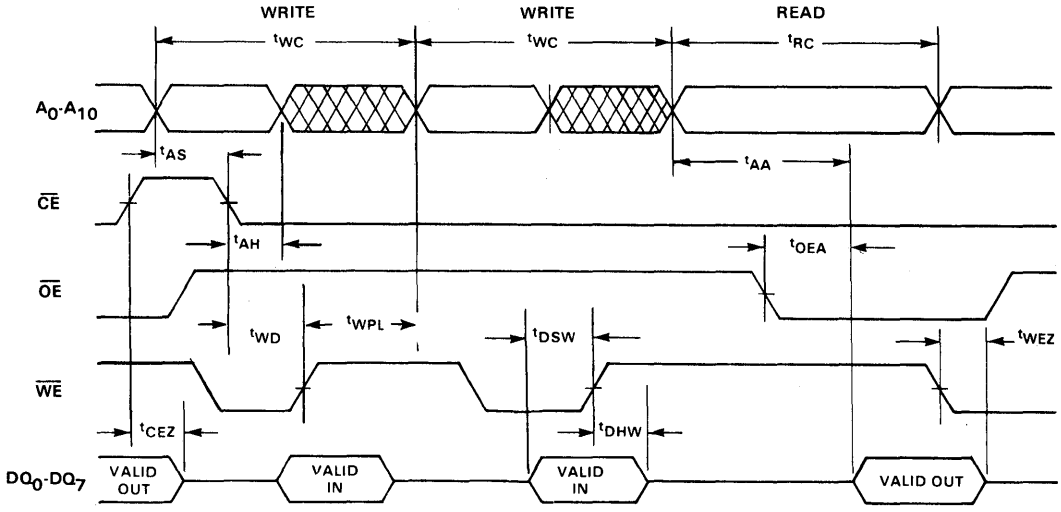
TIMING DIAGRAM

Figure 4



TIMING DIAGRAM

Figure 5



The MK4801A features a fast $\overline{CE}$ (50% of Address Access) function to permit memory expansion without impacting system access time. A fast $\overline{OE}$ (50% of access time) is included to permit data interleaving for enhanced system performance.

The MK4801A is pin compatible with Mostek's BYTEWYDE™ memory family of RAMs, ROMs and EPROMs.

OPERATION

Read Mode

The MK4801A is in the READ MODE whenever the Write Enable Control input ($\overline{WE}$) is in the high state.

In the READ mode of operation, the MK4801A provides a fast address ripple-through access of data from 8 of 8192 locations in the static storage array. Thus, the unique address specified by the 10 Address Inputs (An) define which 1 of 1024 bytes of data is to be accessed.

A transition on any of the 10 address inputs will disable the 8 Data Output Drivers after t_{AZ}. Valid Data will be available to the 8 Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the 8 data I/O signals is controlled by the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) control signals.

Write Mode

The MK4801A is in the Write Mode whenever the Write Enable ($\overline{WE}$) and Chip Enable ($\overline{CE}$) control inputs are in the low state.

The WRITE cycle is initiated by the $\overline{WE}$ pulse going low provided that $\overline{CE}$ is also low. The leading edge of the $\overline{WE}$ pulse is used to latch the status of the address bus.

NOTE: In a write cycle the latter occurring edge of either $\overline{WE}$ or $\overline{CE}$ will determine the start of the write cycle. Therefore, t_{AS}, t_{WD} and t_{AH} are referenced to the latter occurring edge of $\overline{CE}$ or $\overline{WE}$. Addresses are latched at this time. All write cycles whether initiated by $\overline{CE}$ or $\overline{WE}$ must be terminated by the rising edge of $\overline{WE}$. If the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ low) then $\overline{WE}$ will cause the output to go to the high Z state in t_{WEZ}.

Data In must be valid t_{DSW} prior to the low to high transition of $\overline{WE}$. The Data In lines must remain stable for t_{DHW} after $\overline{WE}$ goes inactive. The write control of the MK4801A disables the data out buffers during the write cycle; however, $\overline{OE}$ should be used to disable the data out buffers to prevent bus contention between the input data and data that would be output upon completion of the write cycle.

V

ADVANCE INFORMATION

128 x 8 NON-VOLATILE RAM MK4701 (N)-20

FEATURES

- ☐ Data retention in the absence of power
- ☐ Data security provided by automatic write protection during power failure
- ☐ Direct replacement for volatile byte wide Static RAM
- ☐ +5 Volt only Operation
- ☐ Unlimited write cycles
- ☐ Low Power--75MW standby; 385 MW active
- ☐ 24-pin Dual In-Line Package with JEDEC standard pinout
- ☐ Read Cycle time equals Write Cycle time
- ☐ Optional address signature simplifies external decoder circuitry
- ☐ High performance

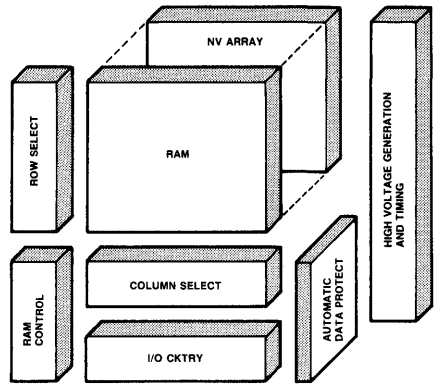
Part No.	Access Time	R/W Cycle Time
MK4701-20	200 ns	200 nsec

TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	DQ
<5.5V volts	V_{IH}	X	X	Deselect	High Z
	V_{IL}	V_{IH}	V_{IL}	Write	D_{IN}
>4.75 volts	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}
	V_{IL}	V_{IH}	V_{IH}	Read	High Z
<4.5	X	X	X	Write Protect	High Z

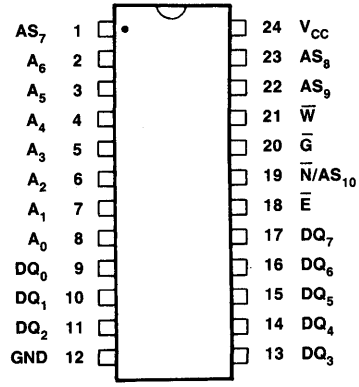
BLOCK DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



PIN NAMES

AS_7-AS_{10} Address Signature Inputs	
$\overline{N}$ - Non Volatile Enable	
A_0-A_6 Address Inputs	V_{CC} Power (+5V)
$\overline{E}$ Chip Enable	$\overline{W}$ Write Enable
GND Ground	$\overline{G}$ Output Enable
DQ_0-DQ_7 Data In/Data Out	

PRELIMINARY

2K × 8 CMOS STATIC RAM
MK6116 (J/N) - 15/20/25
MK6116L (J/N) - 15/20/25

FEATURES

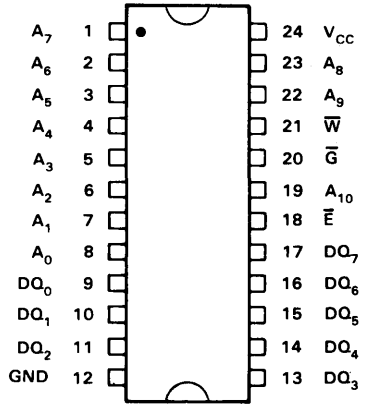
- ☐ Direct replacement for 2K × 8 Byte Wide Static RAM
- ☐ +5 Volt only Read/Write
- ☐ 24-Pin Dual in Line package, JEDEC pinout
- ☐ Read Cycle time equals write cycle time
- ☐ High Performance

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0 - DQ_7	Data In/Data Out		

PIN CONNECTIONS

Figure 1



TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
V_{IH}	X	X	Deselect	High Z	Standby
V_{IL}	X	V_{IL}	Write	D_{IN}	Active
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active

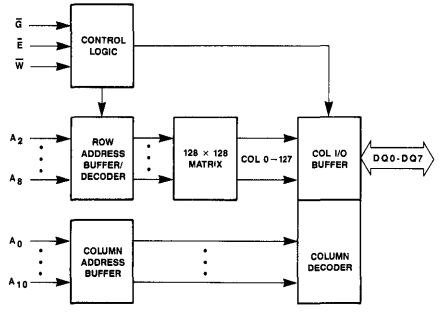
Part No.	Access Time	R/W Cycle Time
MK6116/L-25	250 nsec	250 nsec
MK6116/L-20	200 nsec	200 nsec
MK6116/L-15	150 nsec	150 nsec

DESCRIPTION

The MK6116/6116L are 16,384-bit, CMOS Static RAMS, organized 2K × 8 using advanced HCMOS process technology. They are direct replacements for the popular 24-pin 6116/6116L type static CMOS RAMS. Both devices have the same functional operating characteristics except for active and standby power levels.

BLOCK DIAGRAM

Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −0.3 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient) (Plastic) ..... −55°C to +125°C
Storage Temperature (Ambient) (Cerdip) ..... −65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	4.50	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.5V	V	1
V_{IL}	Logic "0" Voltage All Inputs	−0.3	0.8	V	1,6

DC ELECTRICAL CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0 volts ± 10%)

		MK6116		MK6116L			
SYM	PARAMETER	MIN	MAX	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		70		60	mA	5
I_{CC2}	TTL Standby Current ($\overline{E} \geq V_{IH}$)		15		12	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ −0.2V)		2ma		100μa		
I_{IL}	Input Leakage Current (Any Input)	−1	+1	−1	+1	μA	2
I_{OL}	Output Leakage Current	−5	+5	−5	+5	μA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} = −1.0 mA)	2.4	V_{CC} + 0.5V	2.4	V_{CC} + 0.5V	V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)	−0.3	0.8	−0.3	0.8	V	

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V ± 10%)

		MK6116/L-15		MK6116/L-20		MK6116/L-25			
SYM	**PARAMETER**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	3
t_{CEA}	Chip Enable Access Time		150		200		250	ns	3
t_{CEZ}	Chip Enable Data Off Time		50		60		70	ns	
t_{OEA}	Output Enable Access Time		75		100		125	ns	3
t_{OEZ}	Output Enable Data Off Time		50		60		70	ns	
t_{OH}	Output Hold from Address Change	15		15		15		ns	
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{WD}	Write Pulse Width	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{WEZ}	Write Enable Data Off Time		60		60		80	ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

V

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	7
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,7

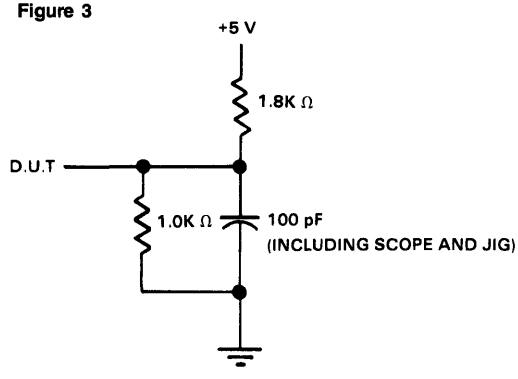
NOTES:
1. All voltages referenced to GND.
2. Measured with GND $\leq V_I \leq V_{CC}$ and outputs deselected.
3. Measured with load as shown in Figure 3.
4. Output buffer is deselected.
5. I_{CC1} measured with outputs open.
6. Negative spikes of −1.0 volts allowed for up to 10 ns once per cycle.
7. Effective capacitance calculated from the equation $C = I \frac{\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

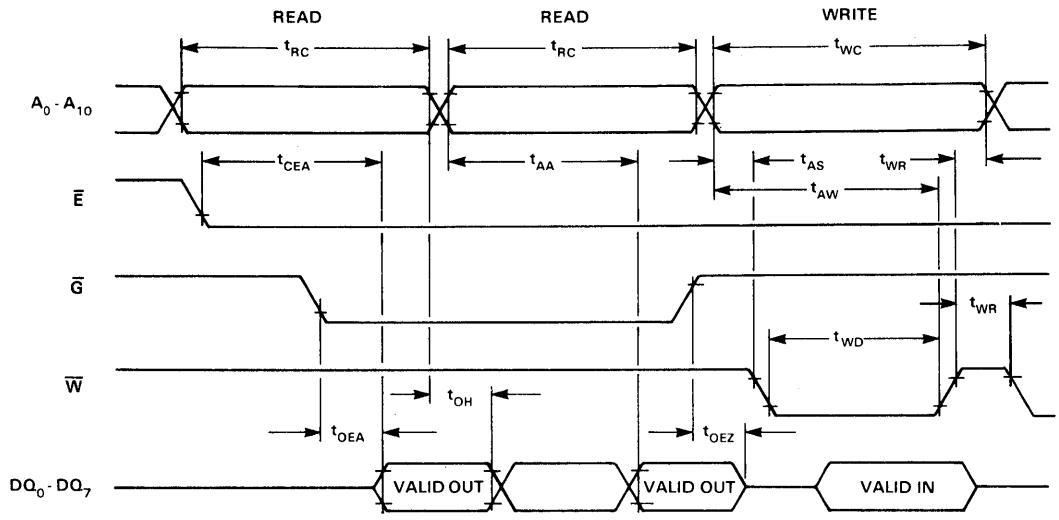
Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels:	0.8 V or 2.2 V

OUTPUT LOAD DIAGRAM

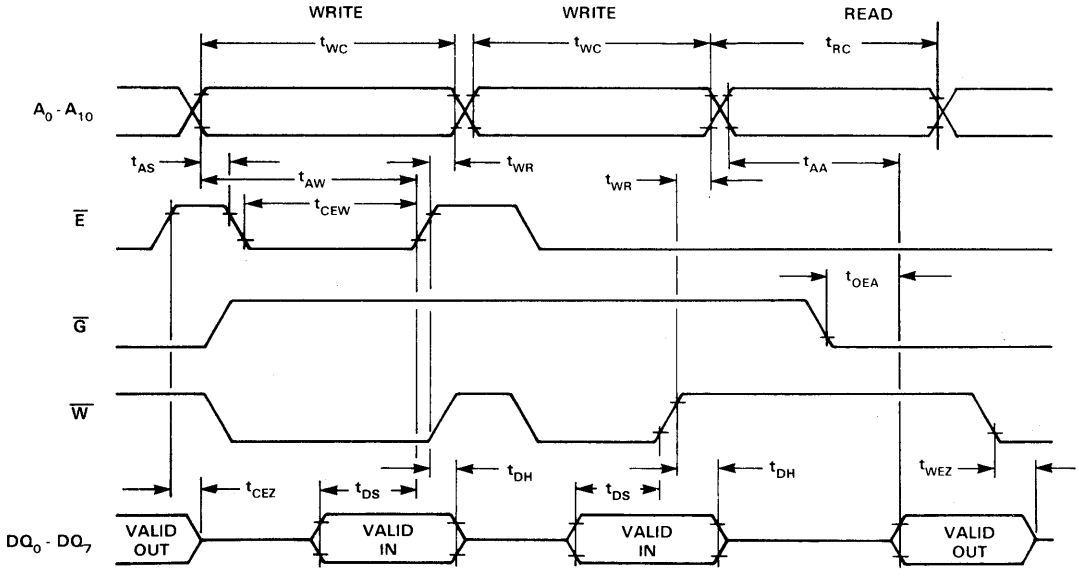
Figure 3



TIMING DIAGRAM
Figure 4



TIMING DIAGRAM
Figure 5



OPERATION

Read Mode

The MK6116/6116L is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2048 bytes of data is to be accessed.

Valid data will be available to the eight Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Write Mode

The MK6116/6116L is in the Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are in the low state. The latter occurring falling edge of either $\overline{W}$ or $\overline{E}$ will determine the start of the Write Cycle. Therefore, t_{AS}, t_{WD}, and t_{CEW} are referenced to the latter occurring edge of $\overline{E}$ or $\overline{W}$. The Write Cycle is terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$. The addresses must be held valid throughout the cycle. $\overline{W}$ must return to the high state for a minimum of t_{WR} prior to the initiation of another cycle.

If the output bus has been enabled ($\overline{E}$ or $\overline{G}$ low), then $\overline{W}$ will disable the outputs in t_{WEZ} from its falling edge; however, care must be taken to avoid a potential bus contention. Data-In must be valid t_{DS} prior to the rising edge of $\overline{E}$ or $\overline{W}$ and must remain valid for t_{DH} after the rising edge of $\overline{E}$ or $\overline{W}$.

V

ORDERING INFORMATION

PART NO.	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK6116N-15	150 ns	Plastic	0° to 70°C
MK6116LN-15	150 ns	Plastic	0° to 70°C
MK6116N-20	200 ns	Plastic	0° to 70°C
MK6116LN-20	200 ns	Plastic	0° to 70°C
MK6116N-25	250 ns	Plastic	0° to 70°C
MK6116LN-25	250 ns	Plastic	0° to 70°C
MK6116J-15	150 ns	Cerdip	0° to 70°C
MK6116LJ-15	150 ns	Cerdip	0° to 70°C
MK6116J-20	200 ns	Cerdip	0° to 70°C
MK6116LJ-20	200 ns	Cerdip	0° to 70°C
MK6116J-25	250 ns	Cerdip	0° to 70°C
MK6116LJ-25	250 ns	Cerdip	0° to 70°C

PRELIMINARY

512 x 9 BiPORT™ PARALLEL IN-OUT FIFO MK4501 (N)-8,10

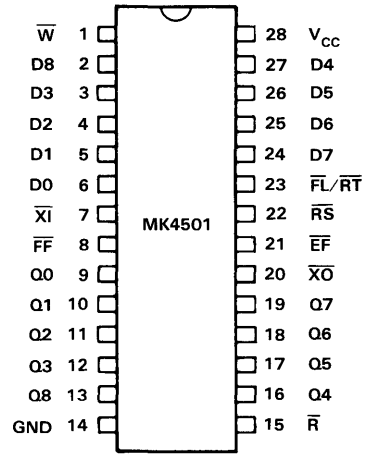
FEATURES

- First-In, First-Out Dual Port Memory
- Flexible 512 x 9 organization
- State-of-the-art HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Retransmit capability
- High performance

Part No.	Access Time	R/W Cycle Time
MK4501-8	80 ns	100 ns
MK4501-10	100 ns	120 ns

PIN CONNECTIONS - DIP

Figure 1



PIN NAMES

$\overline{W}$ = Write	$\overline{XI}$ = Expansion In
$\overline{R}$ = Read	$\overline{XO}$ = Expansion Out
$\overline{RS}$ = Reset	$\overline{FF}$ = Full Flag
$\overline{FL}/\overline{RT}$ = First Load/Retransmit	$\overline{EF}$ = Empty Flag
D = Data In	V_{CC} = 5 Volts
Q0 = Data Out	GND = Ground

DESCRIPTION

The MK4501 is a member of the BiPORT™ Memory Series, which utilizes special two port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g. interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data underflow and overflow. The data is loaded and emptied on a First-In, First-Out basis (FIFO), and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher density devices. The ninth bit is provided to support control or parity functions.

PRELIMINARY

512 x 9 BiPORT™ PARALLEL IN-OUT FIFO MK4501 (N)-12,15,20

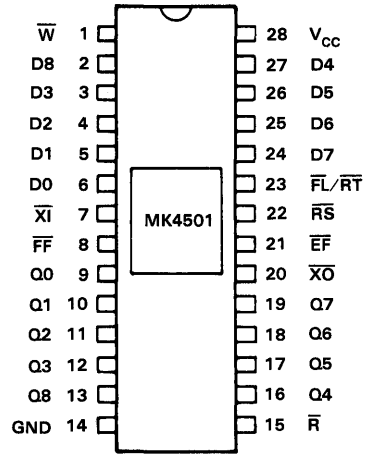
FEATURES

- First-In, First-Out Dual Port Memory
- Flexible 512 x 9 organization
- State-of-the-art HCMOS technology
- Asynchronous and simultaneous read/write
- Bidirectional applications
- Fully expandable by word width or depth
- Empty and full warning flags
- Retransmit capability
- High performance

Part No.	Access Time	R/W Cycle Time
MK4501-12	120 ns	140 ns
MK4501-15	150 ns	175 ns
MK4501-20	200 ns	235 ns

PIN CONNECTIONS - DIP

Figure 1



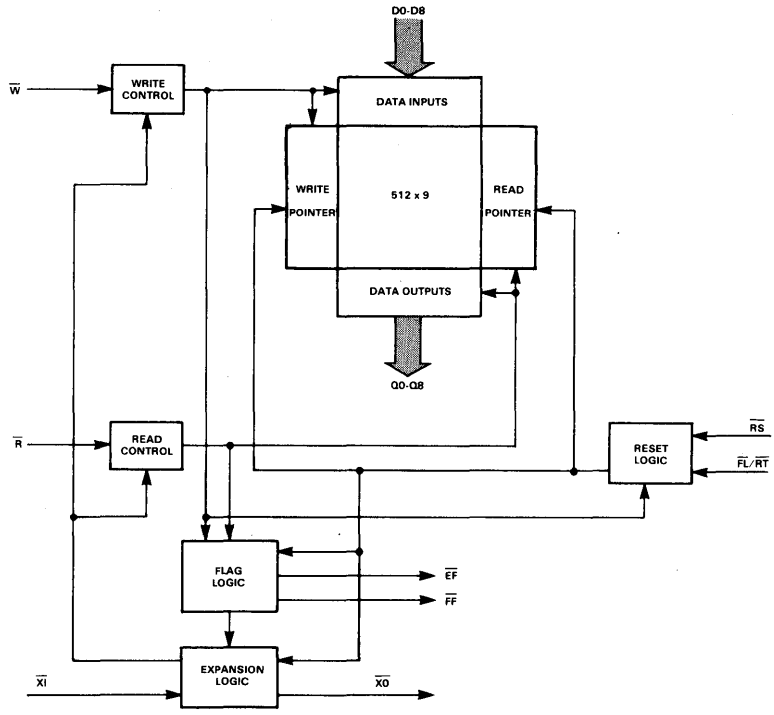
PIN NAMES

$\overline{W}$ = Write	$\overline{XI}$ = Expansion In
$\overline{R}$ = Read	$\overline{XO}$ = Expansion Out
$\overline{RS}$ = Reset	$\overline{FF}$ = Full Flag
$\overline{FL}/\overline{RT}$ = First Load/Retransmit	$\overline{EF}$ = Empty Flag
D = Data In	V_{CC} = 5 Volts
QO = Data Out	GND = Ground

DESCRIPTION

The MK4501 is a member of the BiPORT™ Memory Series, which utilizes special two port cell techniques. Specifically, this device implements a First-In, First-Out algorithm, featuring asynchronous read/write operations, full and empty flags, and unlimited expansion capability in both word size and depth. The main application of the MK4501 is as a rate buffer, sourcing and absorbing data at different rates, (e.g. interfacing fast processors and slow peripherals). The full and empty flags are provided to prevent data underflow and overflow. The data is loaded and emptied on a First-In, First-Out basis (FIFO), and the latency for the retrieval of data is approximately one load cycle (write). Since the writes and reads are internally sequential, thereby requiring no address information, the pinout definition will serve this and future higher density devices. The ninth bit is provided to support control or parity functions.

MK4501 BLOCK DIAGRAM
Figure 2



RESET

The MK4501 is reset whenever the Reset Enable Control input ($\overline{RS}$) is in the low state. During a RESET, both the internal read and write pointers are set to the first location. A RESET is required after power up before a Write operation can begin. Both $\overline{W}$ and $\overline{R}$ must be in the high state during a RESET (refer to the following discussion for required state of $\overline{FL}/\overline{RT}$ and $\overline{XI}$).

READ MODE

The MK4501 initiates a READ CYCLE on the falling edge of Read Enable Control Input ($\overline{R}$), provided that the EMPTY FLAG ($\overline{EF}$) is not set. In the READ mode of operation, the MK4501 provides a fast access of data from 9 of 4608 locations in the static storage array. The data is accessed on a First In, First Out basis independent of any ongoing WRITE operations. After $\overline{R}$ goes high, the data outputs will return to a high impedance condition until the next READ operation.

In the event that all data has been read from the FIFO, the $\overline{EF}$ will go low, and further READ operations will be inhibited (the data outputs will remain in high impedance). Upon completion of a valid WRITE operation, the $\overline{EF}$ will go high after t_{WEF}, and a valid READ can begin.

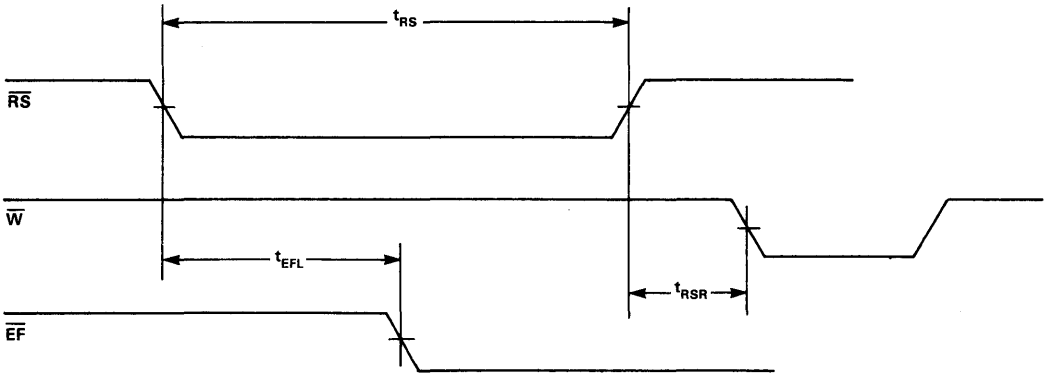
WRITE MODE

The MK4501 initiates a WRITE CYCLE on the falling edge of the Write Enable Control Input ($\overline{W}$) provided that the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold time requirements must be satisfied with respect to the rising edge of $\overline{W}$. The data is stored sequentially and independently of any ongoing READ operations.

To prevent a data overflow condition, the ($\overline{FF}$) will go low, and further WRITE operations will be inhibited. Upon completion of a valid READ operation, the $\overline{FF}$ will go high after t_{RFF}, and a valid WRITE can begin.

RESET

Figure 3

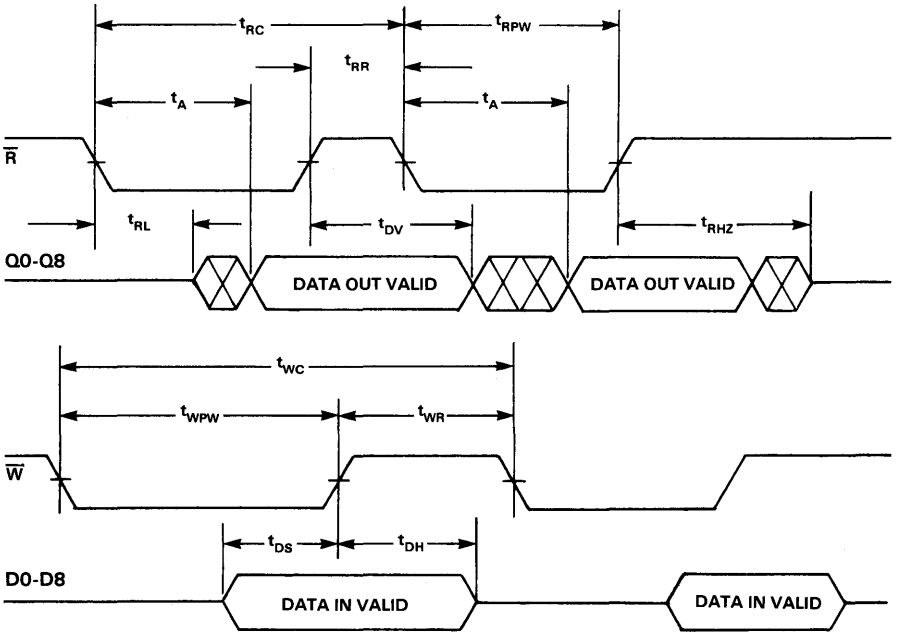


NOTES:

1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R} = V_{IH}$ during RESET.

ASYNCHRONOUS WRITE AND READ OPERATION

Figure 4

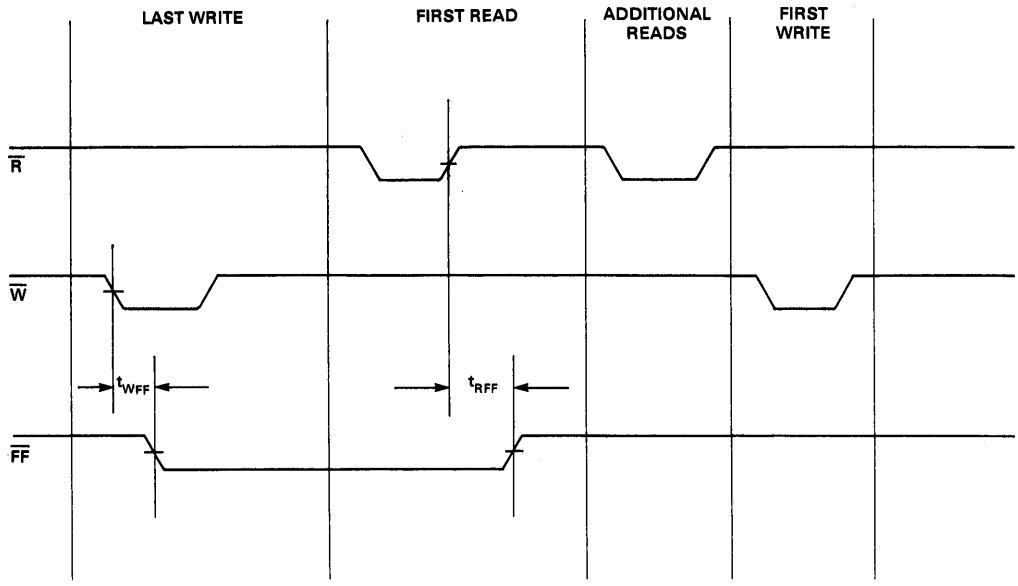


NOTE:

1. $t_{RC} = t_{RR} + t_{RPW}$
2. $t_{WC} = t_{WR} + t_{WPW}$

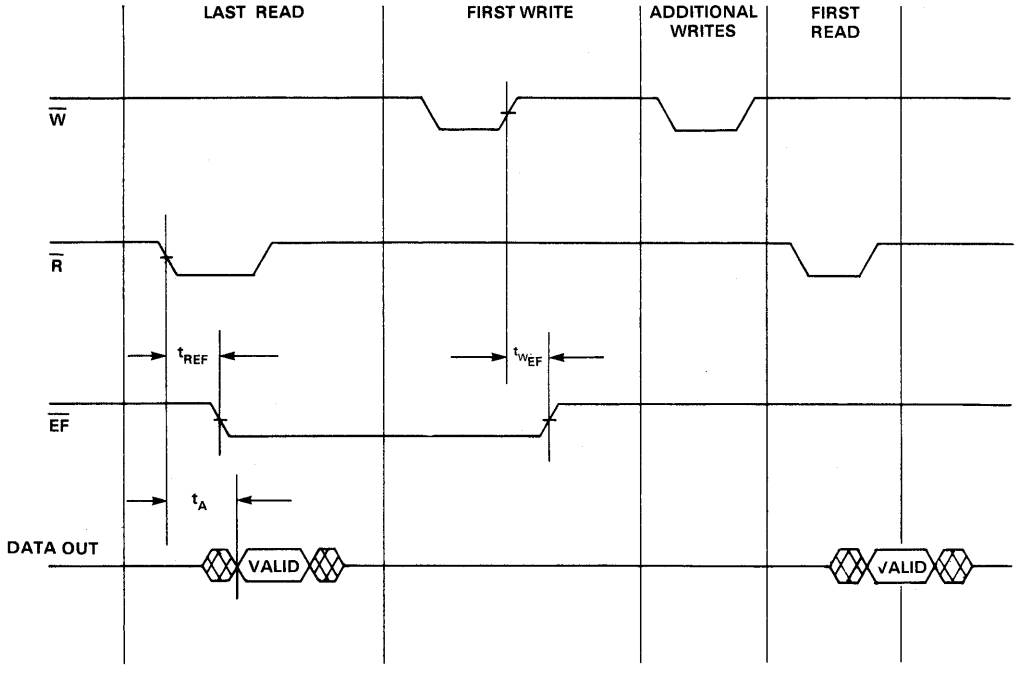
FULL FLAG FROM LAST WRITE TO FIRST READ

Figure 5



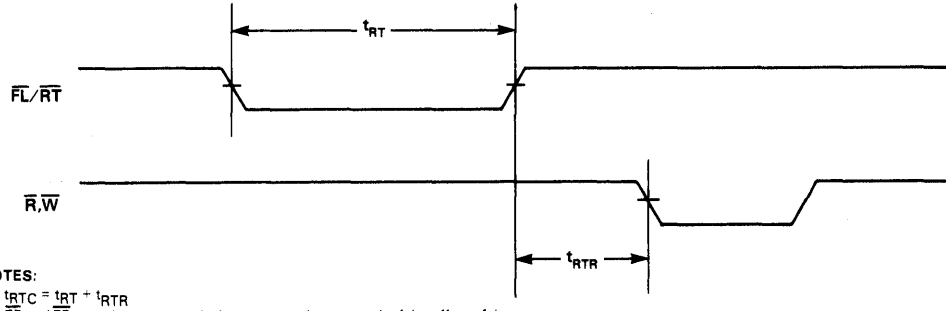
EMPTY FLAG FROM LAST READ TO FIRST WRITE

Figure 6



RETRANSMIT

Figure 7



NOTES:
1. $t_{RTC} = t_{RT} + t_{RTR}$
2. $\overline{EF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

RETRANSMIT

The MK4501 can be made to retransmit data when the Retransmit Enable Control input ($\overline{RT}$) is pulsed low. A RETRANSMIT operation will set the internal read pointer to the first location and will not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be inactive during RETRANSMIT. This feature is useful when less than 512 Writes are performed between RESETs. The RETRANSMIT feature is not compatible with Depth Expansion. (See page 6).

SINGLE DEVICE CONFIGURATION

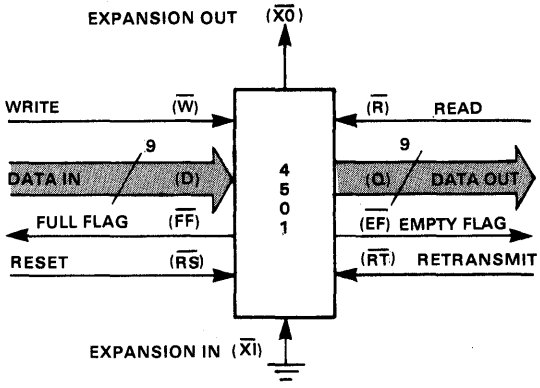
A single MK4501 may be used when the application requirements are for 512 words or less. The MK4501 is in a Single Device Configuration when the Expansion In Control input ($\overline{XI}$) is grounded. (See Figure 8).

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status Flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two MK4501s. Any word width can be attained by adding additional MK4501s.

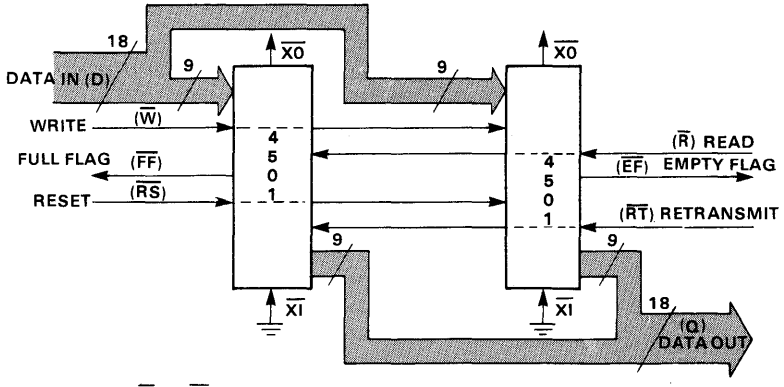
BLOCK DIAGRAM OF SINGLE 512 x 9 FIFO

Figure 8



BLOCK DIAGRAM OF 512 x 18 FIFO MEMORY (WIDTH EXPANSION)

Figure 9



NOTE:
Flag detection is accomplished by monitoring the $\overline{FF}$ and $\overline{EF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

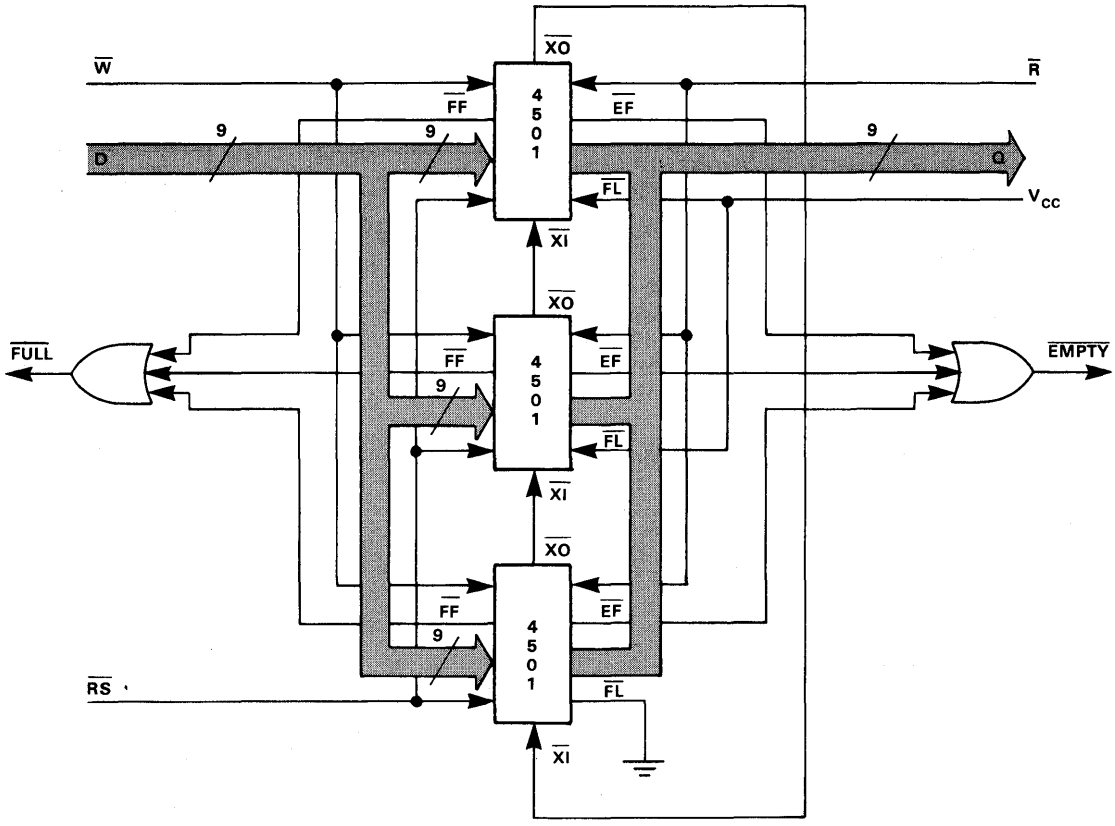
DEPTH EXPANSION (DAISY CHAIN)

The MK4501 can easily be adapted to applications when the requirements are for greater than 512 words. Figure 10 demonstrates Depth Expansion using three MK4501s. Any depth can be attained by adding additional MK4501s. The MK4501 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load Control input ($\overline{FL}$).
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 10.
4. External logic is needed to generate a composite Full Flag and Empty Flag. This requires the ORing of all $\overline{EF}$s and the ORing of all $\overline{FF}$s. (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 10.
5. The Retransmit function is not allowed in the Depth Expansion Mode.

BLOCK DIAGRAM OF 1536 X9 FIFO MEMORY (DEPTH EXPANSION)

Figure 10



COMPOUND EMPANSION

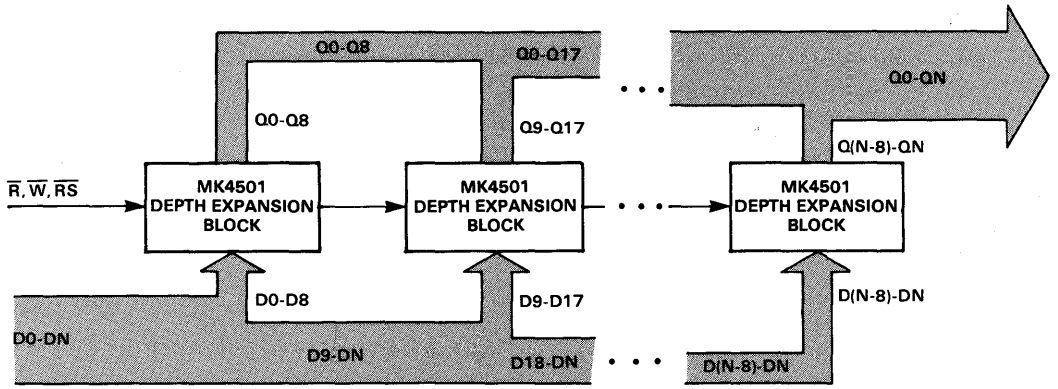
The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays. (See Figure 11).

BIDIRECTIONAL APPLICATIONS

Applications, which require data buffering between two systems (each system capable of READ and WRITE operations), can be achieved by pairing MK4501s, as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system. (i.e. $\overline{FF}$ is monitored on the device where W is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used.) Both Depth Expansion and Width Expansion may be used in this mode.

COMPOUND FIFO EXPANSION

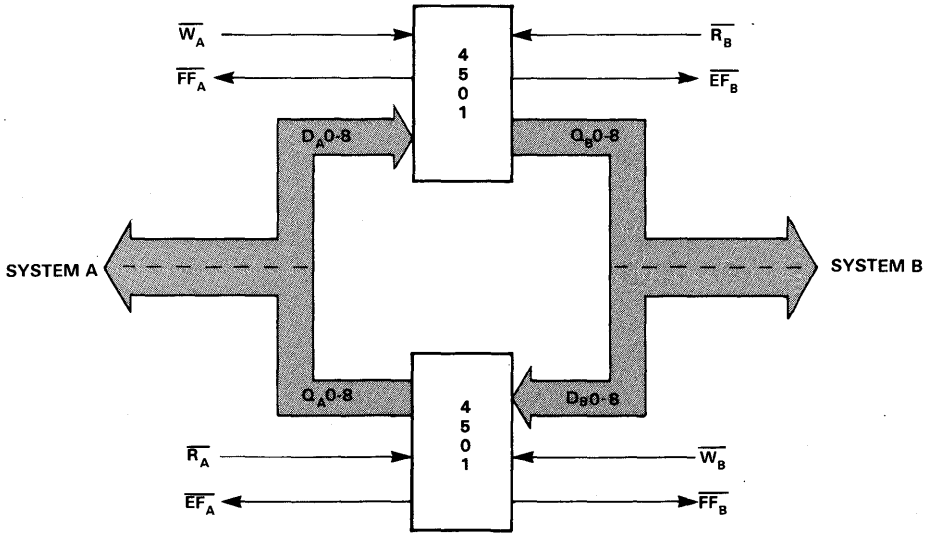
Figure 11



NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

BIDIRECTIONAL FIFO APPLICATION

Figure 12



RESET AND RETRANSMIT TRUTH TABLE - SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Table 1

	INPUTS			INTERNAL STATUS		OUTPUTS	
Mode	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	**Read Pointer**	**Write Pointer**	$\overline{EF}$	$\overline{FF}$
Reset	0	X	0	Location Zero	Location Zero	0	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X
Read/Write	1	1	0	Increment*	Increment*	X	X

*Pointer will increment if flag is high.

RESET AND FIRST LOAD TRUTH TABLE - DEPTH EXPANSION/COMPOUND EXPANSION MODE

Table 2

	INPUTS			INTERNAL STATUS		OUTPUTS	
Mode	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	**Read Pointer**	**Write Pointer**	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	†	Location Zero	Location Zero	0	1
Reset all other Devices	0	1	†	Location Zero	Location Zero	0	1
Read/Write	1	X	†	X	X	X	X

† $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 10.

$\overline{RS}$	=	Reset Input	$\overline{FF}$	=	Full Flag Output
$\overline{FL}/\overline{RT}$	=	First Load/Retransmit	$\overline{XI}$	=	Expansion Input
$\overline{EF}$	=	Empty Flag Output			

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to GND ..... -0.5 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or any other conditions above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED D.C. OPERATING CONDITIONS[1]

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
GND	Ground	0	0	0	V	
V_{IH}	Logic "1" Voltage All Inputs	2.0		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	4

DC ELECTRICAL CHARACTERISTICS[1]

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts ± 10%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{IL}	Input Leakage Current (Any Input)	-1	1	μA	5
I_{OL}	Output Leakage Current	-10	10	μA	6
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1 mA	2.4		V	
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4 mA		0.4	V	
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	3
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})		8	mA	3
I_{CC3}	Power Down Current (All Inputs = V_{CC} -0.2 V)		500	μA	3

V

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

SYM	PARAMETER	TYP	MAX	NOTES
C_I	Capacitance on Input Pins		7 pF	
C_O	Capacitance on Output Pins		12 pF	2

AC ELECTRICAL CHARACTERISTICS[8]

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

		4501-12		4501-15		4501-20			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	140		175		235		ns	
t_A	Access Time		120		150		200	ns	
t_{RR}	Read Recovery Time	20		25		35		ns	
t_{RPW}	Read Pulse Width	120		150		200		ns	7
t_{RL}	Read Pulse Low to Data Bus at Low Z	20		25		25		ns	
t_{DV}	Data Valid from Read Pulse High	5		5		5		ns	
t_{RHZ}	Read Pulse High to Data Bus at High Z		35		50		60	ns	
t_{WC}	Write Cycle Time	140		175		235		ns	
t_{WPW}	Write Pulse Width	120		150		200		ns	7
t_{WR}	Write Recovery Time	20		25		35		ns	

AC ELECTRICAL CHARACTERISTICS[8] (Cont.)

($0°C \leq T_A \leq +70°C$) (V_{CC} = +5.0 volts ± 10%)

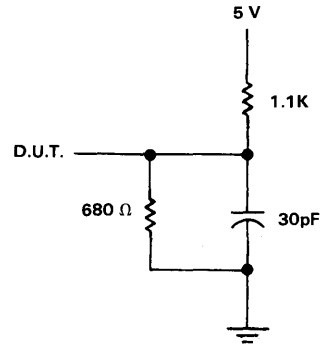
SYM	PARAMETER	4501-12 MIN	4501-12 MAX	4501-15 MIN	4501-15 MAX	4501-20 MIN	4501-20 MAX	UNITS	NOTES
t_{DS}	Data Set Up Time	40		50		65		ns	
t_{DH}	Data Hold Time	10		10		10		ns	
t_{RSC}	Reset Cycle Time	140		175		235		ns	
t_{RS}	Reset Pulse Width	120		150		200		ns	7
t_{RSR}	Reset Recovery Time	20		25		35		ns	
t_{RTC}	Retransmit Cycle Time	140		175		235		ns	
t_{RT}	Retransmit Pulse Width	120		150		200		ns	7
t_{RTR}	Retransmit Recovery Time	20		25		35		ns	
t_{EFL}	Reset to Empty Flag Low		140		175		235	ns	
t_{REF}	Read Low to Empty Flag Low		115		145		195	ns	
t_{RFF}	Read High to Full Flag High		110		140		190	ns	
t_{WEF}	Write High to Empty Flag High		110		140		190	ns	
t_{WFF}	Write Low to Full Flag Low		115		145		195	ns	

NOTES:

1. All voltages are referenced to ground.
2. Output buffer is deselected.
3. I_{CC} measurements are made with outputs open.
4. 1.5 volt undershoots are allowed for 10 ns once per cycle.
5. Measured with $0.4 \leq V_{IN} \leq V_{CC}$.
6. $\overline{R} \geq V_{IH}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
7. Pulse widths less than minimum values are not allowed.
8. Timings referenced as in Figure 14.

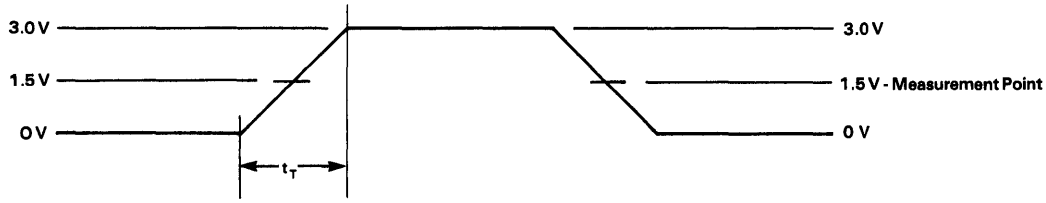
OUTPUT LOAD

Figure 13



TRANSITION WAVEFORMS

Figure 14



NOTES:
1. Inputs swing 0-3 volts
2. t_T = 5 ns.
3. All timing is measured at 1.5 volts
4. Measured with a load shown in Figure 13.

ORDERING INFORMATION

V

PART NO.	ACCESS TIME	R/W CYCLE TIME (CLOCK FREQUENCY)	PACKAGE TYPE	TEMPERATURE RANGE
MK4501-12	120 ns	140 ns (7.1 MHz)	Plastic	0° to 70°C
MK4501-15	150 ns	175 ns (5.7 MHz)	Plastic	0° to 70°C
MK4501-20	200 ns	235 ns (4.2 MHz)	Plastic	0° to 70°C

ADVANCE INFORMATION

512 x 9 BIPORT™ RAM MK4511 (N/E)-15

FEATURES

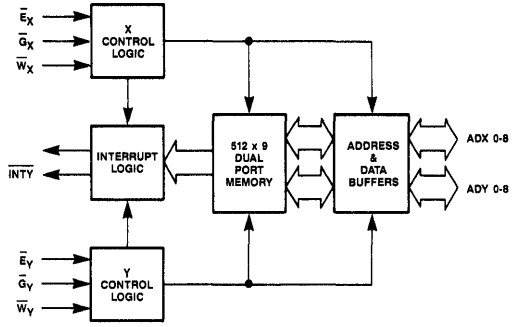
- ☐ 512 x 9 bit Dual Port RAM utilizes unique BiPORT™ Cell/Array
- ☐ Simplifies "multi-processing"
- ☐ Provides convenient method of tightly coupling microprocessors with "shared store"
- ☐ Usable as "controller" for expansion of "shared store" multiport systems
- ☐ Requires no external "arbitration" - totally asynchronous operation
- ☐ Symmetrical control functions including Chip Enable ($\overline{E}$), Output Enable ($\overline{G}$), and Write Enable ($\overline{W}$)
- ☐ Hardwired INTERRUPT control supports multiport "handshake" operation
- ☐ Utilizes MOSTEK's high technology HCMOS process
- ☐ High Speed - 130 ns (Access Time)
  150 ns (READ/WRITE) Cycle Time)
- ☐ Low Power - 80 mA (Active)
  200 μA (Standby)
- ☐ 28-pin dual-in-line low cost plastic package
- ☐ Address-Data multiplexing

PIN NAMES

$\overline{E}$ = Chip Enable	AD = Address/Data
$\overline{G}$ = Output Enable	V_{CC} = 5 Volts
$\overline{W}$ = Write Enable	GND = Ground
$\overline{INT}$ = Interrupt Out	

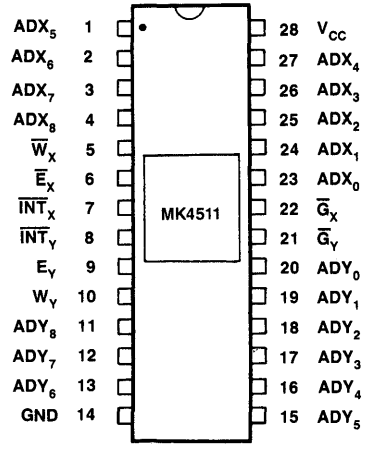
FUNCTIONAL DIAGRAM

Figure 1



PIN CONNECTIONS

Figure 2



2K x 8 BATTERY BACK-UP RAM
MK48C02, MK48C02L (N) -15/20/25

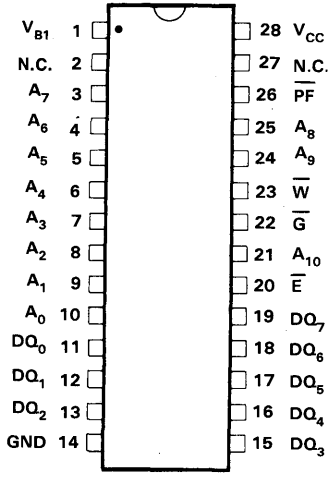
FEATURES

- Ideal Non-Volatile RAM with a single external Lithium Cell
- Data security provided by automatic write protection during power failure
- No battery drain during normal operating conditions
- Ultra low battery drain during battery back-up
- Data retention down to 1.8 V
- Low battery warning
- Power fail detect signal available for memory expansion
- Fully static Chip Enable and Output Enable facilitate bus control
- High performance

Part No.	Access Time	R/W Cycle Time
MK48C02-15 MK48C02L-15	150 ns	150 ns
MK48C02-20 MK48C02L-20	200 ns	200 ns
MK48C02-25	250 ns	250 ns

PIN CONNECTIONS

Figure 1

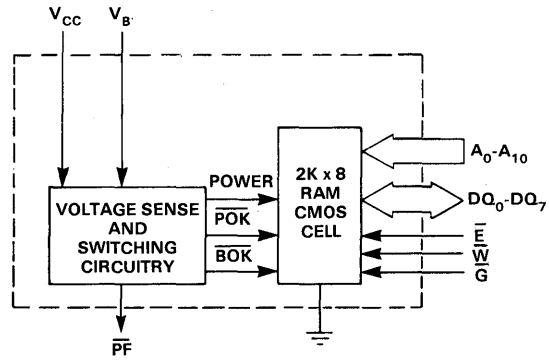


PIN NAMES

A_0 - A_{10} = Address Inputs	E = Chip Enable
DQ_0 - DQ_7 = Data In/Data Out	W = Write Enable
GND = Ground	G = Output Enable
V_{CC} = Power (+5 V) VB = Battery Inputs	PF = Power Fail Detect Output

BLOCK DIAGRAM

Figure 2



TRUTH TABLE

V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
≤5.5 volts	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
≥4.75 volts	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
<4.5 volts	X	X	X	Write Protect	High Z	CMOS Standby

DESCRIPTION

The MK48C02/MK48C02L is a CMOS RAM with integral power fail support circuitry for battery backup applications. The fully static RAM uses a HCMOS six transistor cell and is organized 2K x 8. Included in the device is a feature to conserve battery energy and a method of providing data security during V_{CC} transients. Battery voltage is checked on each power-up with the status communicated via the V_{LB} pin. A precision voltage detector, nominally set at 4.60 volts, write-protects the RAM to prevent inadvertent loss of data when V_{CC} is out of tolerance. In this way, all input and output pins (including $\overline{E}$ and $\overline{W}$) become "don't care". The device permits full functional ability of the RAM for V_{CC} above 4.75 volts, provides write protection for V_{CC} less than 4.50 volts, and maintains data in the absence of V_{CC} with no additional support circuitry other than a primary cell. The current supplied by the battery during data retention is for junction leakage only (typically less than 5 na) because all power-consuming circuitry is turned off. The low battery drain allows the use of a long life Lithium primary cell.

OPERATION

Read Mode

The MK48C02/MK48C02L is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) define which one of 2048 bytes of data is to be accessed.

Valid data will be available to the eight Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Write Mode

The MK48C02/MK48C02L is in the Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are in the low state. The latter occurring falling edge of either $\overline{W}$ or $\overline{E}$ will determine the start of the Write Cycle. Therefore, t_{AS}, t_{WD}, and t_{CEW} are referenced to this latter occurring edge of $\overline{E}$ or $\overline{W}$. The Write Cycle is terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$. The addresses must be held valid throughout the cycle. $\overline{W}$ must return to the high state for a minimum of t_{WR} prior to the initiation of another cycle. If the output bus has been enabled ($\overline{E}$ and $\overline{G}$ low), then $\overline{W}$ will disable the outputs in t_{WEZ} from its falling edge; however care must be taken to avoid a potential bus contention. Data-In must be valid t_{DS} prior to the rising edge of $\overline{E}$ or $\overline{W}$ and must remain valid for t_{DH} after the rising edge of $\overline{E}$ or $\overline{W}$.

Data Retention Mode

In the normal mode of operation, the MK48C02/MK48C02L operates as a static RAM. However, V_{CC} is being constantly monitored. Should the supply voltage decay, the RAM will automatically write-protect itself in the V_{CC} range between 4.75 and 4.50 volts as long as the slew rate (t_f) specification is satisfied. The open collector output, $\overline{PF}$, will go low when the RAM is write-protected. By holding $\overline{E}$ or $\overline{W}$ above V_{IH} for a minimum of t_{PD} before power-down, incomplete write cycles to the RAM will be avoided. Once V_{CC} falls below 4.50 volts, all inputs to the RAM become "don't care" and may be as high as 5.50 volts.

As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the external energy source to supply power to the RAM. In the Data Retention mode, the current drain on the energy source will be less than I_{BAT} max.

This redundant battery scheme has been provided to enhance data retention reliability. If only one battery is used, VB_1 and VB_2 should be connected together.

When V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the external energy source. As V_{CC} rises from a 4.50 to 4.75 volts, the external energy source is checked. If the voltage is below V_{LB}, a BOK (Battery OK) flag will be set. Normal RAM operation can resume t_{REC} after V_{CC} exceeds 4.75 volts. Whenever V_{CC} is between 4.50 and 4.75 volts, $\overline{E}$ or $\overline{W}$ must be in the high state to prevent inadvertant write cycles. The BOK flag can be checked on the first write cycle after a power-up. This write cycle will not be executed if either battery is below V_{LB}.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.3 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient) ..... -55°C to +125°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.5 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,6
V_B	Battery Voltage	1.8	3.5	V	1,7
V_{LB}	Low Battery Warning (I_{LOAD} = 10μA)	1.8	2.4	V	1
ΔV_B	Battery Switch Differential Voltage		0.7	V	

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts + 10% - 5%)

SYM	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current			80	mA	5
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)			3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ - 0.2 V)			1	mA	
I_{IL}	Input Leakage Current (Any Input)		-1	+1	μA	2
I_{OL}	Output Leakage Current		-5	+5	μA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} = -1.0 mA)		2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)			0.4	V	
V_{PFL}	$\overline{PF}$ Logic "0" Voltage I_{OUT} = 50 μA			0.4	V	
I_{BAT}	Battery Back-Up Current V_B = 3.5 V, V_{CC} = 0 V	MK48C02L		1	μA	
		MK48C02		50	μA	
I_{CHG}	Battery Charging Current V_B = 1.8 V, V_{CC} = 5.5 V		-5	+5	na	

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V + 10% - 5%)

SYM	PARAMETER	MK48C02-15 MK48C02L-15		MK48C02-20 MK48C02L-20		MK48C02-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	3
t_{CEA}	Chip Enable Access Time		150		200		250	ns	3
t_{CEZ}	Chip Enable Data Off Time		35		40		50	ns	
t_{OEA}	Output Enable Access Time		70		80		90	ns	3
t_{OEZ}	Output Enable Data Off Time		35		40		50	ns	
t_{OH}	Output Hold from Address Change	15		15		15		ns	
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{WD}	Write Pulse Width	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{WEZ}	Write Enable Data Off Time		50		60		80	ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

CAPACITANCE

(T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	8
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,9

NOTES:

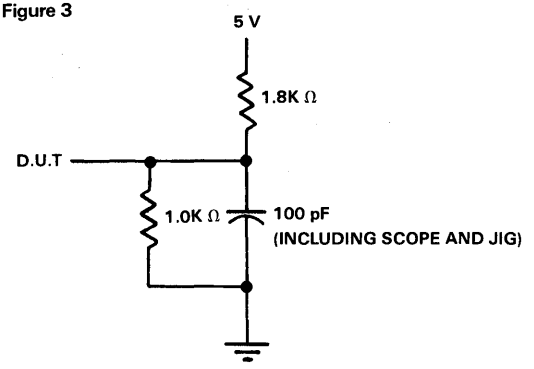
1. All voltages referenced to GND.
2. Measured with GND $\leq V_I \leq V_{CC}$ and outputs deselected.
3. Measured with load as shown in Figure 3.
4. Output buffer is deselected.
5. I_{CC1} measured with outputs open.
6. Negative spikes of -1.0 volts allowed for up to 10 ns once per cycle.
7. Battery voltages below V_B min may allow loss of data.
8. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with ΔV = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

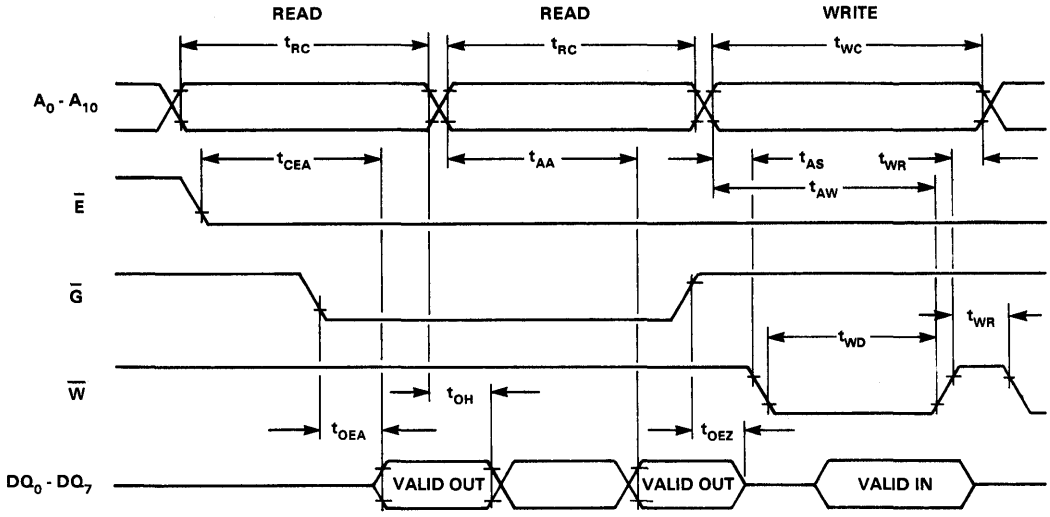
Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels:	0.8 V or 2.2 V

OUTPUT LOAD DIAGRAM

Figure 3

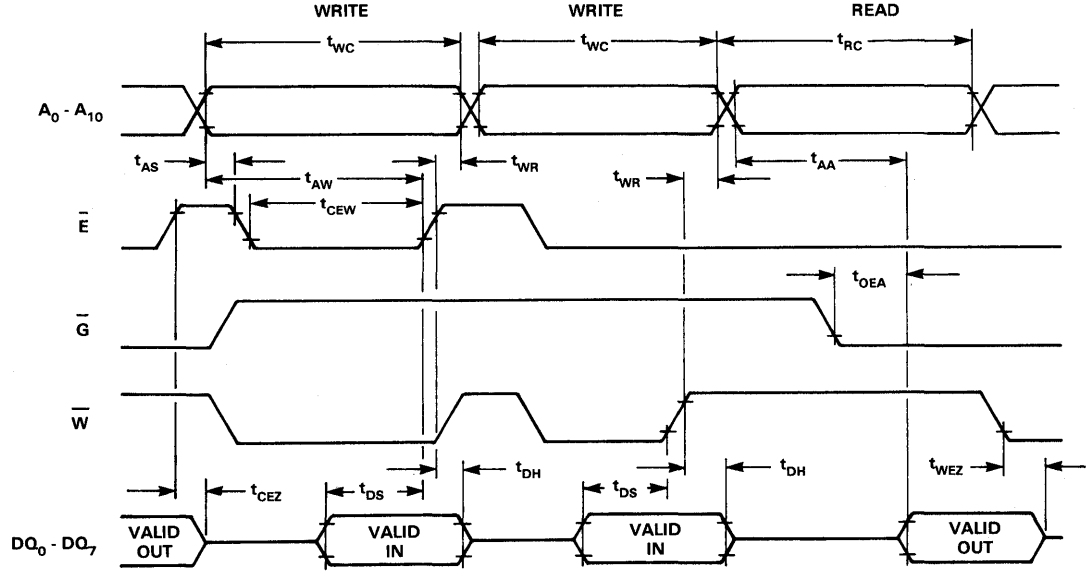


TIMING DIAGRAM
Figure 4



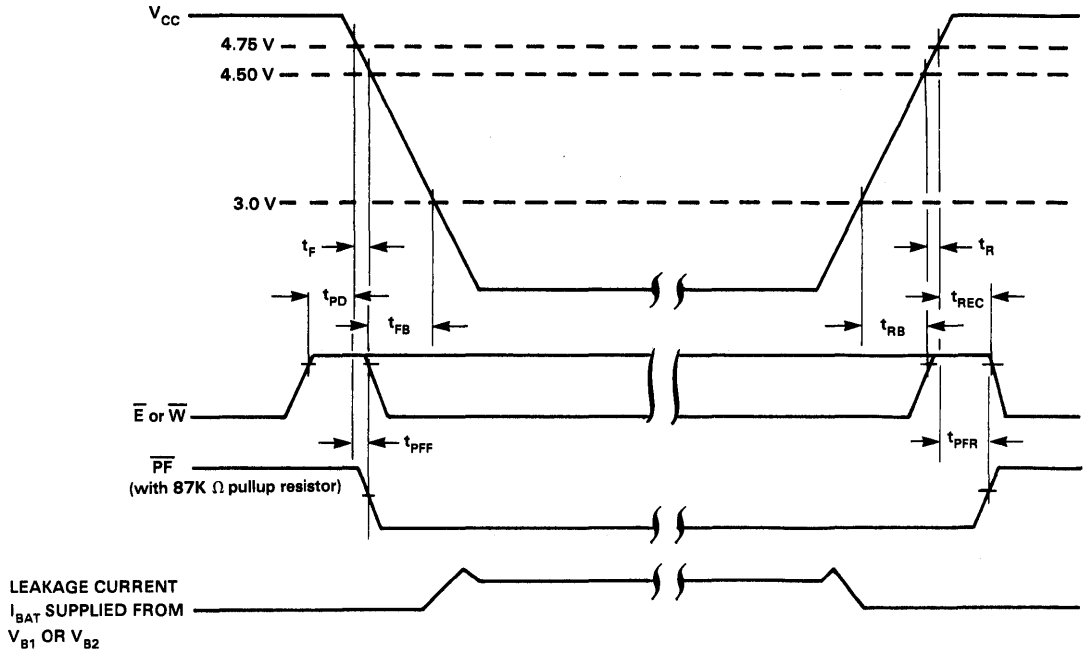
V

TIMING DIAGRAM
Figure 5



POWER-DOWN, POWER-UP CONDITIONS

Figure 6



POWER-DOWN/POWER-UP TIMING

(0°C ≤ T_A ≤ +70°C)

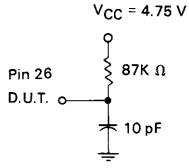
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		μS	
t_F	V_{CC} slew from 4.75 V to 4.50 V ($\overline{E}$ or $\overline{W}$ at V_{IH})	300		μS	
t_{FB}	V_{CC} slew from 4.50 to 3.0 V	10		μS	
t_{RB}	V_{CC} slew from 3.0 V to 4.50 V	1		μS	
t_R	V_{CC} slew from 4.50 to 4.75 V ($\overline{E}$ or $\overline{W}$ at V_{IH})	0		μS	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	
t_{PFF}	$\overline{PF}$ at logic '0' (V_{CC} ≤ 4.50 V)		0	ns	1,2
t_{PFR}	$\overline{PF}$ at logic '1' (V_{CC} ≥ 4.75 V)		2	ms	2

NOTES:

1. $\overline{PF}$ starts to go low when V_{CC} < 4.75 V. It is guaranteed to be at a logic '0' when V_{CC} ≤ 4.50 V.

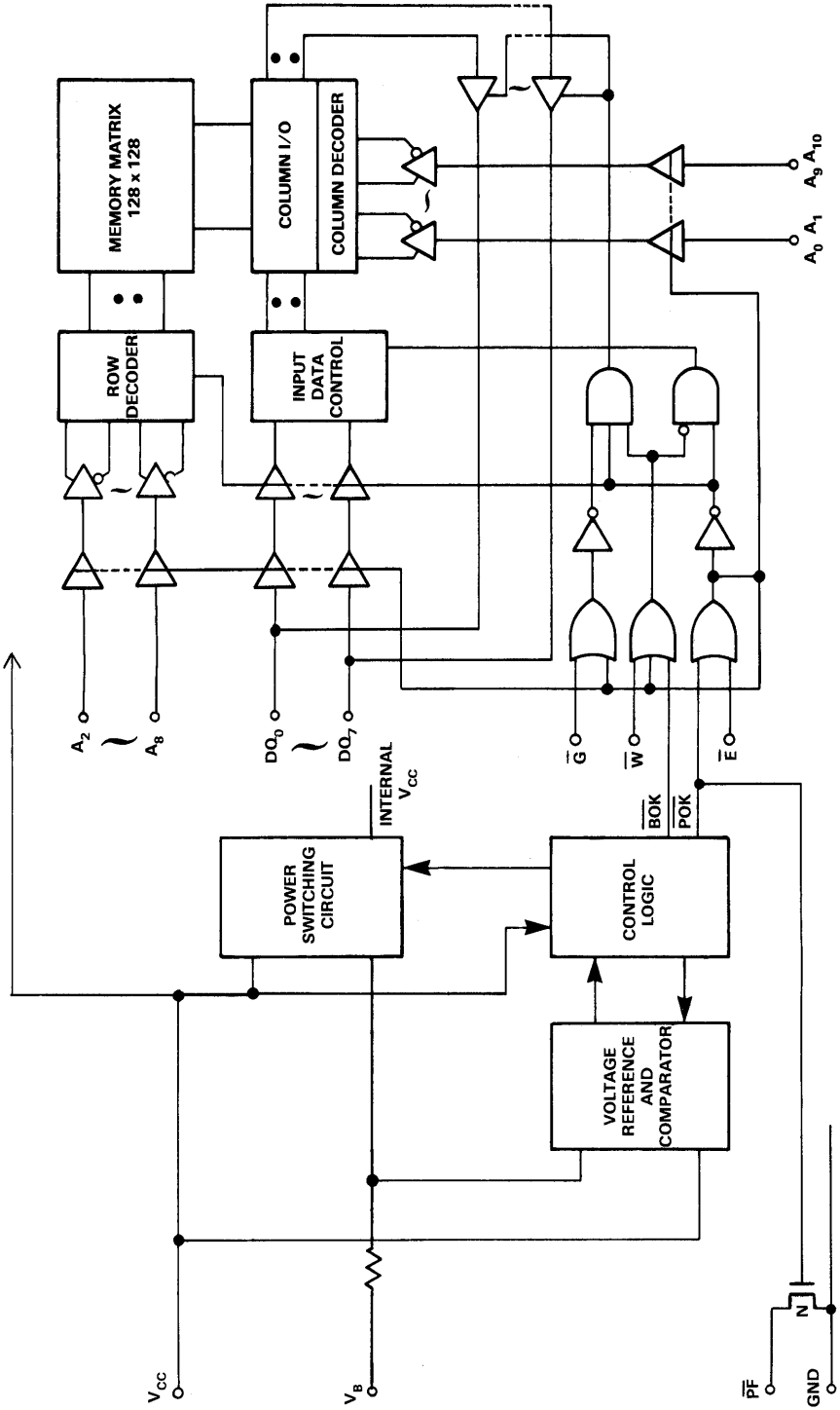
WARNING: Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

2. Measured with load



2K x 8 BATTERY BACK-UP RAM FUNCTIONAL DIAGRAM

Figure 7



ORDERING INFORMATION

PART NO.	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48C02N-15	150 ns	Plastic	0° to 70°C
MK48C02LN-15	150 ns	Plastic	0° to 70°C
MK48C02N-20	200 ns	Plastic	0° to 70°C
MK48C02LN-20	200 ns	Plastic	0° to 70°C
MK48C02N-25	250 ns	Plastic	0° to 70°C

2K x 8 ZEROPOWER™ RAM MK48Z02 (B) -15/20/25

FEATURES

- Data retention in the absence of power
- Data security provided by automatic write protection during power failure
- Direct replacement for volatile 2K x 8 Byte Wide Static RAM
- +5 Volt only Read/Write
- Unlimited write cycles
- CMOS - 440 MW active; 5.5 MW standby
- 24-Pin Dual in Line package, JEDEC pinout
- Read cycle time equals write cycle time
- Low Battery Warning

Part No.	Access Time	R/W Cycle Time
MK48Z02-25	250 nsec	250 nsec
MK48Z02-20	200 nsec	200 nsec
MK48Z02-15	150 nsec	150 nsec

DESCRIPTION

The MK48Z02 is a 16,384-bit, Non-Volatile Static RAM, organized 2K x 8 using HCMOS and an integral Lithium energy source. The ZEROPOWER™ RAM has the characteristics of a CMOS static RAM, with the important added benefit of data being retained in the absence of power. Data retention current is so small that a miniature Lithium cell contained within the package provides an energy source to preserve data. Low current drain has been attained by the use of a full CMOS memory cell, novel analog support circuitry, and carefully controlled junction leakage by an all implanted CMOS process. Safeguards

TRUTH TABLE

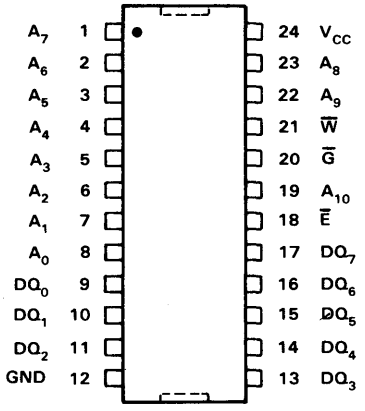
V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	POWER
≤5.5 volts	V_{IH}	X	X	Deselect	High Z	Standby
	V_{IL}	X	V_{IL}	Write	D_{IN}	Active
≥4.75 volts	V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
	V_{IL}	V_{IH}	V_{IH}	Read	High Z	Active
<4.5 volts	X	X	X	Write Protect	High	Zero

PIN NAMES

A_0 - A_{10}	Address Inputs	V_{CC}	System Power (+5 V)
$\overline{E}$	Chip Enable	$\overline{W}$	Write Enable
GND	Ground	$\overline{G}$	Output Enable
DQ_0 - DQ_7 Data In/Data Out			

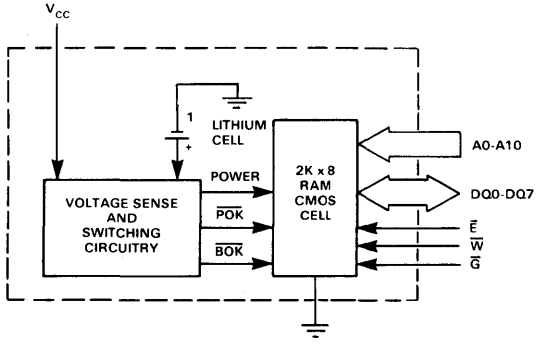
PIN CONNECTIONS

Figure 1



BLOCK DIAGRAM

Figure 2



ZEROPOWER™ is a trademark of Mostek Corporation.

against inadvertent data loss have been incorporated to maintain data integrity during the uncertain operating environment associated with power-up and power-down transients. The ZEROPOWER™ RAM can replace existing 2K x 8 static RAM, directly conforming to the popular Byte Wide 24-pin DIP package (JEDEC). MK48Z02 also matches the pinning of 2716 EPROM and 2K x 8 E²PROM. Like other static RAM, there is no limit on the number of write cycles that can be performed. Since the access time, read cycle, and write cycle are less than 250 ns and require +5 volts only, no additional support circuitry is needed to interface to a microprocessor.

OPERATION

Read Mode

The MK48Z02 is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low, providing a ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs (A_n) defines which one of 2048 bytes of data is to be accessed.

Valid data will be available to the eight Data Output Drivers within t_{AA} after the last address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ (Output Enable) access times are satisfied. If $\overline{E}$ or $\overline{G}$ access times are not met, data access will be measured from the limiting parameter (t_{CEA} or t_{OEA}) rather than the address. The state of the eight Data I/O signals is controlled by the $\overline{E}$ and $\overline{G}$ control signals. The data lines may be in an indeterminate state between t_{OH} and t_{AA}, but the data lines will always have valid data at t_{AA}.

Write Mode

The MK48Z02 is in the Write Mode whenever the $\overline{W}$ and $\overline{E}$ inputs are in the low state. The latter occurring falling edge of either $\overline{W}$ or $\overline{E}$ will determine the start of the Write Cycle. Therefore, t_{AS}, t_{WD}, and t_{CEW} are referenced to the latter occurring edge of $\overline{E}$ or $\overline{W}$. The Write Cycle is terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$. The addresses must be held valid throughout the cycle. $\overline{W}$ must return to the high state for a minimum of t_{WR} prior to the initiation of another cycle. If the output bus has been enabled ($\overline{E}$ and $\overline{G}$ low), then $\overline{W}$ will disable the outputs in t_{WEZ} from its falling edge; however, care must be taken to avoid a potential bus contention. Data-In must be valid t_{DS} prior to the rising edge of $\overline{E}$ or $\overline{W}$ and must remain valid for t_{DH} after the rising edge of $\overline{E}$ or $\overline{W}$.

Data Retention Mode

The ZEROPOWER™ RAM provides full functional capability for V_{CC} above 4.75 volts, guarantees write protection for V_{CC} less than 4.50 volts, maintains data in the absence of V_{CC}, and needs no additional support circuitry. The block diagram shown in Figure 7 illustrates this self-contained solution.

The MK48Z02 constantly monitors V_{CC}. Should the supply voltage decay, the RAM will automatically write-protect itself in the V_{CC} range between 4.75 and 4.50 volts (Figure 6). Once V_{CC} falls below 4.50 volts, all inputs to the RAM become "DON'T CARE" ($-0.3 \leq V_{IN} \leq 5.5$ volts), and all outputs are high impedance.

During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the Lithium cell. As V_{CC} rises from 4.50 to 4.75 volts, the Lithium cell is checked; if the voltage is below 2.0 V, a flag will be set. Normal RAM operation can resume after V_{CC} exceeds 4.75 volts. The flag can be checked on the first write cycle after a power-up. This first write cycle will not be executed if a Lithium cell has been depleted, thereby warning of an impending data loss. This can be easily implemented in a power-up.

As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the internal Lithium power source to the memory matrix, maintaining the voltage required to retain data. Junction leakage is the only current consumption mechanism in the data retention mode. The internal Lithium source supplies this current, which is typically 300 pA at room temperature.

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... -0.3 V to +7.0 V
Operating Temperature T_A (Ambient) ..... 0°C to +70°C
Storage Temperature (Ambient) ..... -20°C to +70°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAUTION: Under no conditions can the "Absolute Maximum Rating" for the voltage on any pin be exceeded since it will cause permanent damage. Specifically, do not perform the "standard" continuity test on any input or output pin, i.e. do not force these pins below -0.3 V DC.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.75	5.50	V	1
GND	Supply Voltage	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2	V_{CC} + 0.5 V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3	0.8	V	1,6

V

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 volts + 10% - 5%)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		80	mA	5
I_{CC2}	TTL Standby Current ($\overline{E} = V_{IH}$)		3	mA	
I_{CC3}	CMOS Standby Current ($\overline{E} \geq V_{CC}$ - 0.2 V)		1	mA	
I_{IL}	Input Leakage Current (Any Input)	-1	+1	μA	2
I_{OL}	Output Leakage Current	-5	+5	μA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} = -1.0 mA)	2.4		V	
V_{OL}	Output Logic "0" Voltage (I_{OUT} = 2.1 mA)		0.4	V	

AC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V + 10% - 5%)

		MK48Z02-15		MK48Z02-20		MK48Z02-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{RC}	Read Cycle Time	150		200		250		ns	
t_{AA}	Address Access Time		150		200		250	ns	3
t_{CEA}	Chip Enable Access Time		150		200		250	ns	3
t_{CEZ}	Chip Enable Data Off Time		35		40		50	ns	
t_{OEA}	Output Enable Access Time		70		80		90	ns	3
t_{OEZ}	Output Enable Data Off Time		35		40		50	ns	

AC ELECTRICAL CHARACTERISTICS (Cont.)

($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0 V + 10% – 5%)

		MK48Z02-15		MK48Z02-20		MK48Z02-25			
SYM	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
t_{OH}	Output Hold from Address Change	15		15		15		ns	
t_{WC}	Write Cycle Time	150		200		250		ns	
t_{AS}	Address Setup Time	0		0		0		ns	
t_{CEW}	Chip Enable to End of Write	90		120		160		ns	
t_{AW}	Address Valid to End of Write	120		140		180		ns	
t_{WD}	Write Pulse Width	90		120		160		ns	
t_{WR}	Write Recovery Time	10		10		10		ns	
t_{WEZ}	Write Enable Data Off Time		50		60		80	ns	
t_{DS}	Data Setup Time	40		60		100		ns	
t_{DH}	Data Hold Time	0		0		0		ns	

CAPACITANCE (T_A = 25°C)

SYM	PARAMETER	MAX	NOTES
C_I	Capacitance on all pins (except D/Q)	7 pF	8
$C_{D/Q}$	Capacitance on D/Q pins	10 pF	4,8

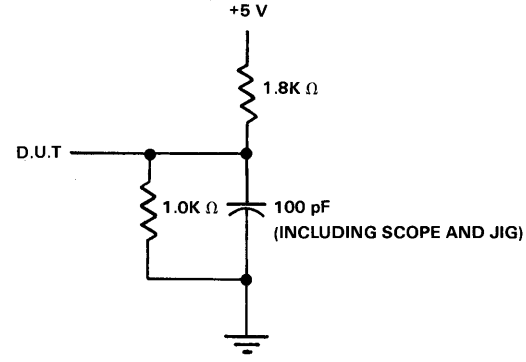
NOTES:
1. All voltages referenced to GND.
2. Measured with GND $\leq V_I \leq V_{CC}$ and outputs deselected.
3. Measured with load as shown in Figure 3.
4. Output buffer is deselected.
5. I_{CC1} measured with outputs open.
6. Negative spikes of –1.0 volts allowed for up to 10 ns once per cycle.
7. Each MK48Z02 is marked with a 4 digit data code XXYY, XX designates the year of manufacture and YY designates the week in that year. Example 8340 would be interpreted as year 1983 week 40 or September 25, 1983. The expected t_{DR} is defined as starting at date of manufacture and proceeding without interruption.
8. Effective capacitance calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with Δ = 3 volts and power supply at nominal level.

AC TEST CONDITIONS

Input Levels:	0.6 V to 2.4 V
Transition Times:	5 ns
Input and Output Timing Reference Levels:	0.8V or 2.2 V

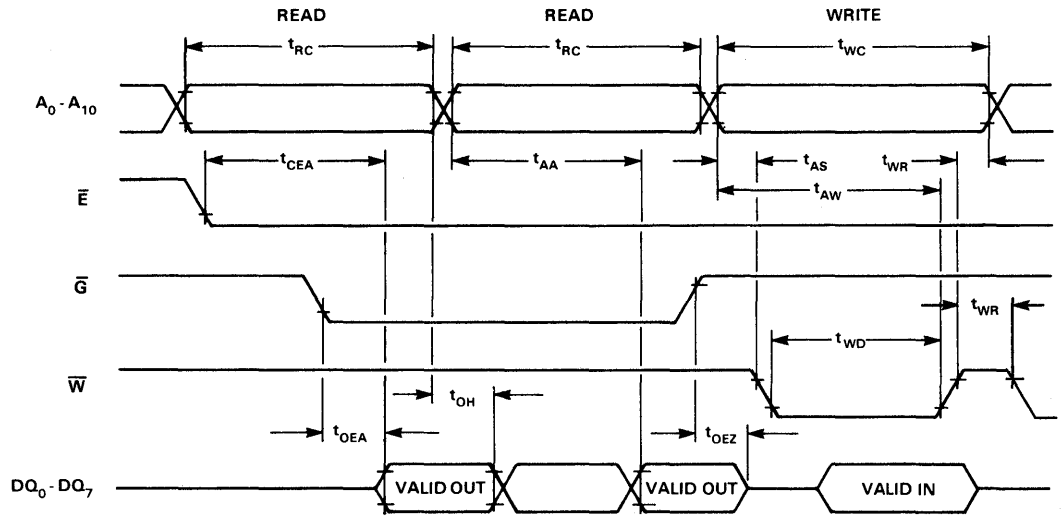
OUTPUT LOAD DIAGRAM

Figure 3



TIMING DIAGRAM

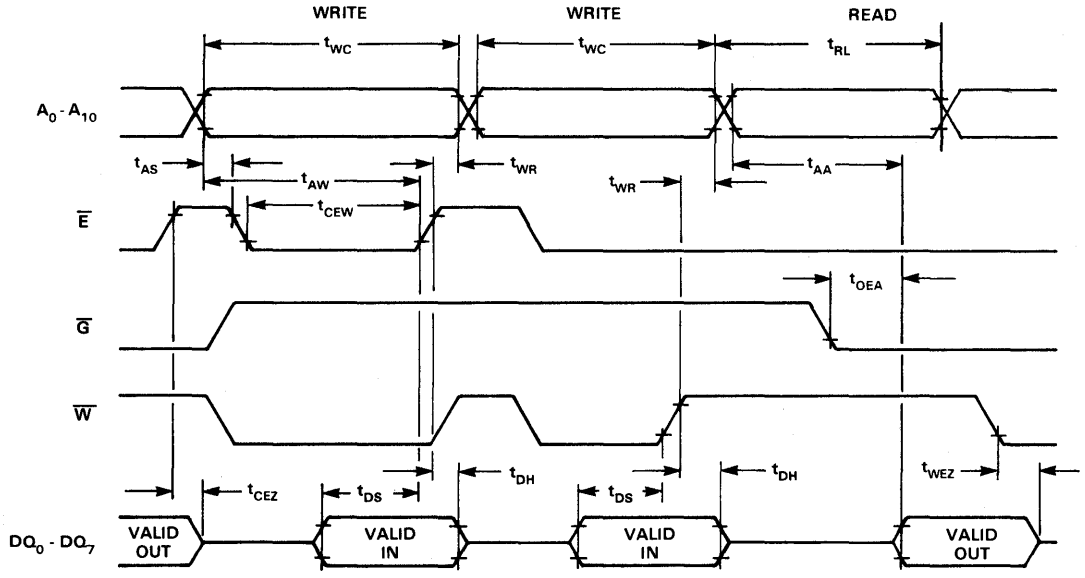
Figure 4



V

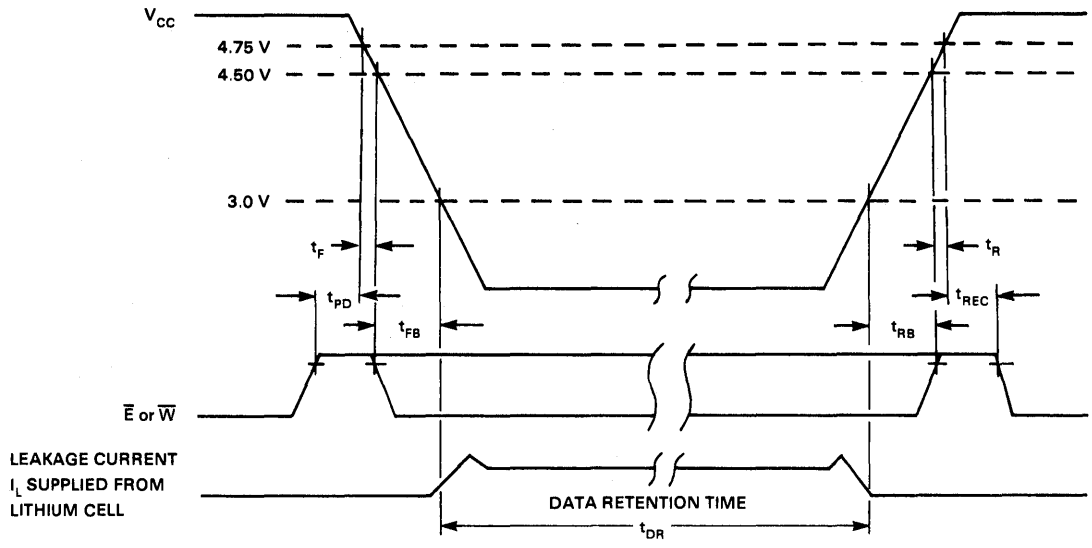
TIMING DIAGRAM

Figure 5



POWER-DOWN, POWER-UP CONDITIONS

Figure 6



POWER-DOWN/POWER-UP TIMING

($0°C \leq T_A \leq +70°C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	$\overline{E}$ or $\overline{W}$ at V_{IH} before Power Down	0		μS	
t_F	V_{CC} slew from 4.75 V to 4.50 V ($\overline{E}$ or $\overline{W}$ at V_{IH})	300		μS	
t_{FB}	V_{CC} slew from 4.50 V to 3.0 V	10		μS	
t_{RB}	V_{CC} slew from 3.0 V to 4.50 V	1		μS	
t_R	V_{CC} slew from 4.50 V to 4.75 V ($\overline{E}$ or $\overline{W}$ at V_{IH})	0		μS	
t_{REC}	$\overline{E}$ or $\overline{W}$ at V_{IH} after Power Up	2		ms	

(T_A = 25°C)

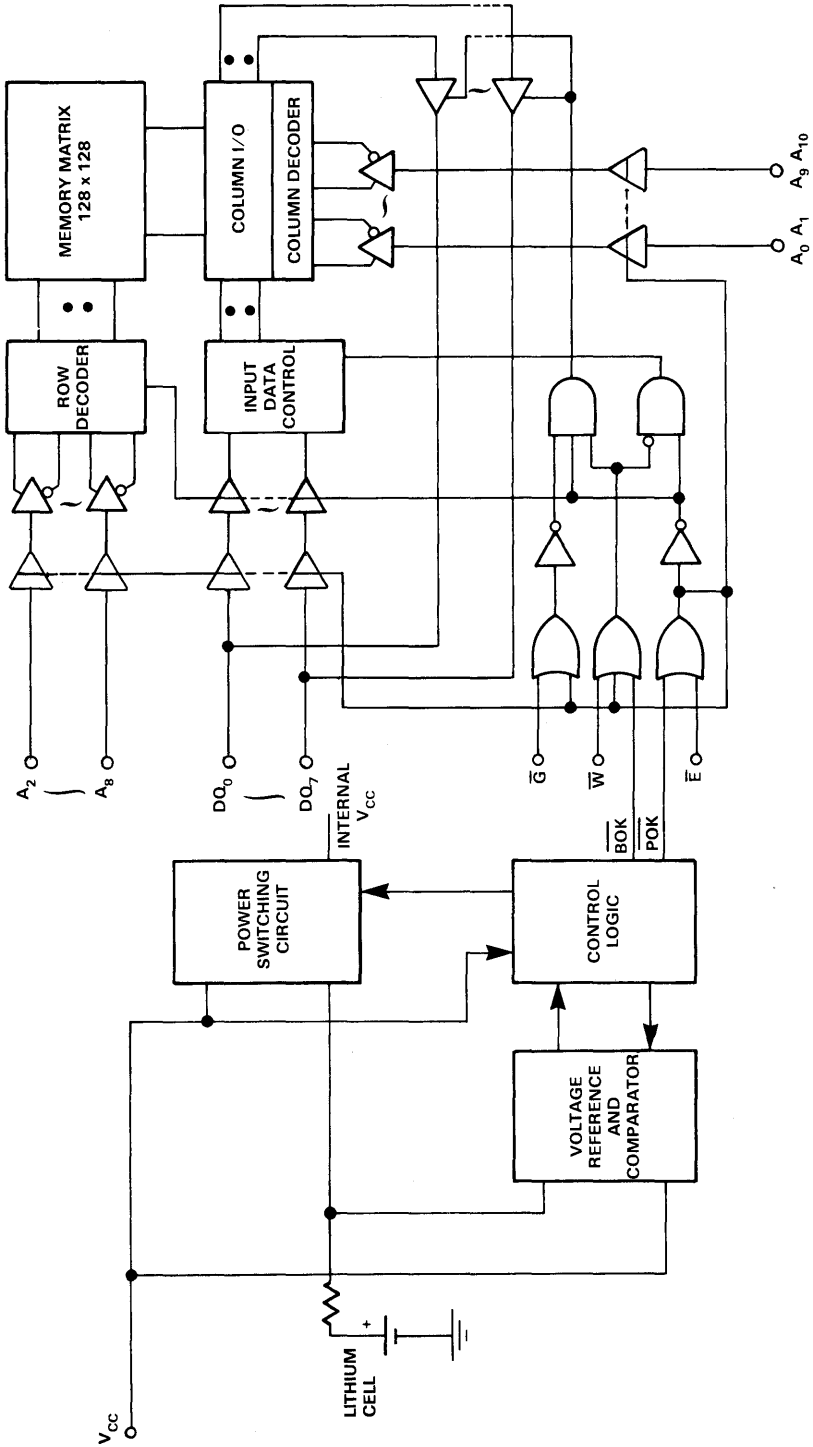
SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	7

WARNING:

Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

ZEROPOWER RAM FUNCTIONAL DIAGRAM

Figure 7



V

ORDERING INFORMATION

PART NO.	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48Z02B-15	150 ns	Plastic	0° to 70°C
MK48Z02B-20	200 ns	Plastic	0° to 70°C
MK48Z02B-25	250 ns	Plastic	0° to 70°C

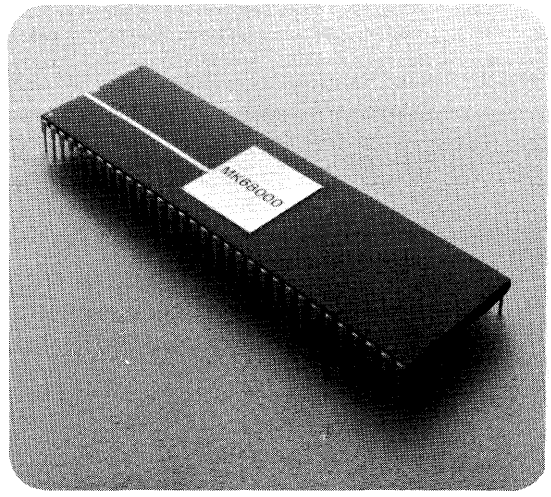
1984/1985 MICROELECTRONIC DATA BOOK

16-BIT MICROPROCESSOR MK68000

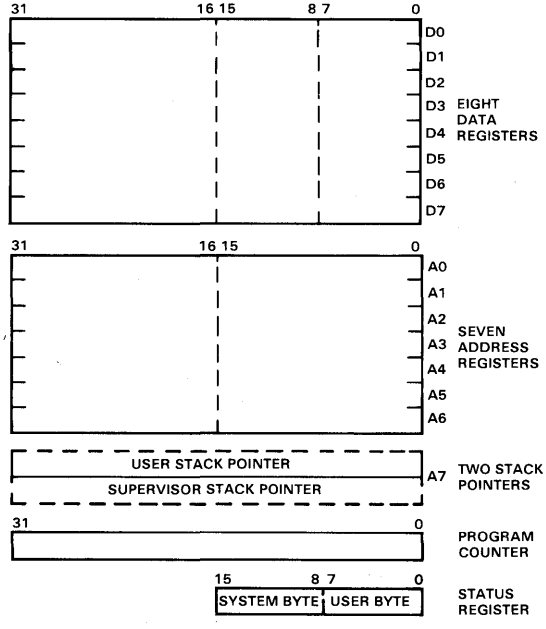
Advances in semiconductor technology have provided the capability to place on a single silicon chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The MK68000 is the first of a family of such VLSI microprocessors from Mostek. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessor.

The resources available to the MK68000 user consist of the following:

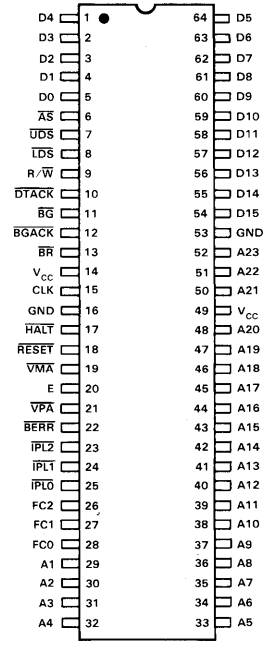
- 17 32-Bit Data and Address Registers
- 16 Megabyte Direct Addressing Range
- 56 Powerful Instruction Types
- Operations on Five Main Data Types
- Memory Mapped I/O
- 14 Addressing Modes



PROGRAMMING MODEL



PIN ASSIGNMENT



As shown in the programming model, the MK68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0-A6) and the system stack pointer may be used as software stack pointers and base address registers. In addition, these registers may be used for word and long word address operations. All 17 registers may be used as index registers.

A 23-bit address bus provides a memory addressing range of greater than 16 megabytes. This large range of addressing capability, coupled with a memory management unit, allows large, modular programs to be developed and operated without resorting to cumbersome and time consuming software bookkeeping and paging techniques.

The status register contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in a trace (T) mode and/or in a supervisor (S) state.

Five basic data types are supported. These data types are:

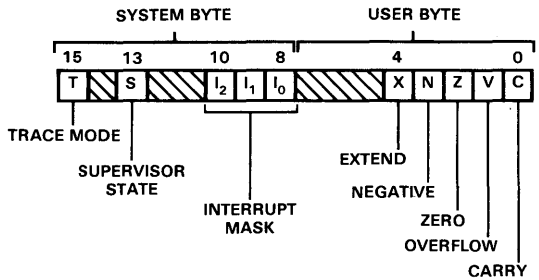
- Bits
- BCD Digits (4-bits)
- Bytes (8-bits)
- Word (16-bits)
- Long Words (32-bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided for in the instruction set.

The 14 addressing modes, shown in Table 1, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Immediate
- Program Counter Relative
- Implied

STATUS REGISTER



Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting and indexing. Program counter relative mode can also be modified via indexing and offsetting.

The MK68000 instruction set is shown in Table 2. Some additional instructions are variations, or subsets, of these and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic and expanded operations (through traps).

DATA ADDRESSING MODES

Table 1

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N
Predecrement Register Indirect	An ← An – N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SP, PC

NOTES:

EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of
d_8 = Eight-bit Offset (displacement)
d_{16} = Sixteen-bit Offset (displacement)
N = 1 for Byte, 2 for Word, and 4 for Long Word. If An is the Stack Pointer and the operand size is byte, N = 2 to keep the Stack Pointer on a word boundary.
← = Replaces

INSTRUCTION SET

Table 2

Mnemonic	Description	Mnemonic	Description	Mnemonic	Description
ABCD	Add Decimal with Extend	EOR	Exclusive Or	PEA	Push Effective Address
ADD	Add	EXG	Exchange Registers	RESET	Reset External Devices
AND	Logical And	EXT	Sign Extend	ROL	Rotate Left without Extend
ASL	Arithmetic Shift Left	JMP	Jump	ROR	Rotate Right without Extend
ASR	Arithmetic Shift Right	JSR	Jump to Subroutine	ROXL	Rotate Left with Extend
B_{CC}	Branch Conditionally	LEA	Load Effective Address	ROXR	Rotate Right with Extend
BCHG	Bit Test and Change	LINK	Link Stack	RTE	Return from Exception
BCLR	Bit Test and Clear	LSL	Logical Shift Left	RTR	Return and Restore
BRA	Branch Always	LSR	Logical Shift Right	RTS	Return from Subroutine
BSET	Bit Test and Set	MOVE	Move	SBCD	Subtract Decimal with Extend
BSR	Branch to Subroutine	MOVEM	Move Multiple Registers	S_{CC}	Set Conditional
BTST	Bit Test	MOVEP	Move Peripheral Data	STOP	Stop
CHK	Check Register Against Bounds	MULS	Signed Multiply	SUB	Subtract
		MULU	Unsigned Multiply	SWAP	Swap Data Register Halves
CLR	Clear Operand	NBCD	Negate Decimal with Extend	TAS	Test and Set Operand
CMP	Compare	NEG	Negate	TRAP	Trap
DB_{CC}	Test Condition, Decrement and Branch	NOP	No Operation	TRAPV	Trap on Overflow
		NOT	One's Complement	TST	Test
DIVS	Signed Divide	OR	Logical Or	UNLK	Unlink
DIVU	Unsigned Divide				

VI

VARIATIONS OF INSTRUCTION TYPES

Table 3

Instruction Type	Variation	Description	Instruction Type	Variation	Description
ADD	**ADD**	Add	**MOVE**	**MOVE**	MOVE
	ADDA	Add Address		MOVEA	Move Address
	ADDQ	Add Quick		MOVEQ	Move Quick
	ADDI	Add Immediate		MOVE from SR	Move from Status Register
	ADDX	Add with Extend		MOVE to SR	Move to Status Register
AND	**AND**	Logical And		MOVE to CCR	Move to Condition Codes
	ANDI	And Immediate		MOVE USP	Move User Stack Pointer
	ANDI to CCR	AND Immediate to Condition Codes			
	ANDI to SR	AND Immediate to Status Register			
CMP	**CMP**	Compare	**NEG**	**NEG**	Negate
	CMPA	Compare Address		NEGX	Negate with Extend
	CMPM	Compare Memory	**OR**	**OR**	Logical Or
	CMPI	Compare Immediate		ORI	Or Immediate
				ORI to CCR	Or Immediate to Condition Codes
				ORI to SR	OR Immediate to Status Register
EOR	**EOR**	Exclusive Or	**SUB**	**SUB**	Subtract
	EORI	Exclusive Or Immediate		SUBA	Subtract Address
	EORI to CCR	Exclusive OR Immediate to Condition Codes		SUBI	Subtract Immediate
				SUBQ	Subtract Quick
	EORI to SR	Exclusive OR Immediate to Status Register		SUBX	Subtract with Extend

DATA ORGANIZATION AND ADDRESSING CAPABILITIES

The following paragraphs describe the data organization and addressing capabilities of the MK68000.

OPERAND SIZE

Operand sizes are defined as follows: a byte equals 8 bits, a word equals 16 bits, and a long word equals 32 bits. The operand size for each instruction is either explicitly encoded in the instruction or implicitly defined by the instruction operation. All explicit instructions support byte, word or long word operands. Implicit instructions support some subset of all three sizes.

DATA ORGANIZATION IN REGISTERS

The eight data registers support data operands of 1, 8, 16, or 32 bits. The seven address registers together with the active stack pointer support address operands of 32 bits.

DATA REGISTERS. Each data register is 32 bits wide. Byte operands occupy the low order 8 bits, word operands the low order 16 bits, and long word operands the entire 32 bits. The least significant bit is addressed as bit zero; the most significant bit is addressed as bit 31.

When a data register is used as either a source or destination operand, only the appropriate low-order portion is changed; the remaining high-order portion is neither used nor changed.

ADDRESS REGISTERS. Each address register and the stack pointer is 32 bits wide and holds a full 32 bit address. Address registers do not support byte sized operands. Therefore, when an address register is used as a source operand, either the low order word or the entire long word operand is used depending upon the operation size. When an address register is used as the destination operand, the entire register is affected regardless of the operation size. If the operation size is word, any other operands are sign extended to 32 bits before the operation is performed.

DATA ORGANIZATION IN MEMORY

Bytes are individually addressable with the high order byte having an even address the same as the word, as shown in Figure 1. The low order byte has an odd address that is one count higher than the word address. Instructions and multibyte data are accessed only on word (even byte) boundaries. If a long word datum is located at address n (n even), then the second word of that datum is located at address n + 2.

The data types supported by the MK68000 are: bit data, integer data of 8, 16, or 32 bits, 32-bit addresses and binary coded decimal data. Each of these data types is put in memory, as shown in Figure 2.

ADDRESSING

Instructions for the MK68000 contain two kinds of information: the type of function to be performed, and the location of the operand(s) on which to perform that function. The methods used to locate (address) the operand(s) are explained in the following paragraphs.

Instructions specify an operand location in one of three ways:

Register Specification - the number of the register is given in the register field of the instruction.
Effective Address - use of the different effective address modes.
Implicit Reference - the definition of certain instructions implies the use of specific registers.

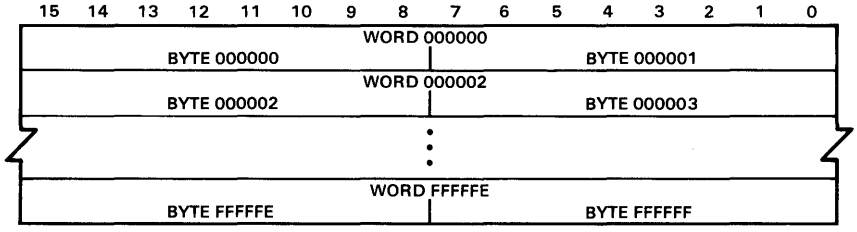
INSTRUCTION FORMAT

Instructions are from one to five words in length, as shown in Figure 3. The length of the instruction and the operation to be performed is specified by the first word of the instruction which is called the operation word. The remaining words further specify the operands. These words are either immediate operands or extensions to the effective address mode specified in the operation word.

PROGRAM/DATA REFERENCES

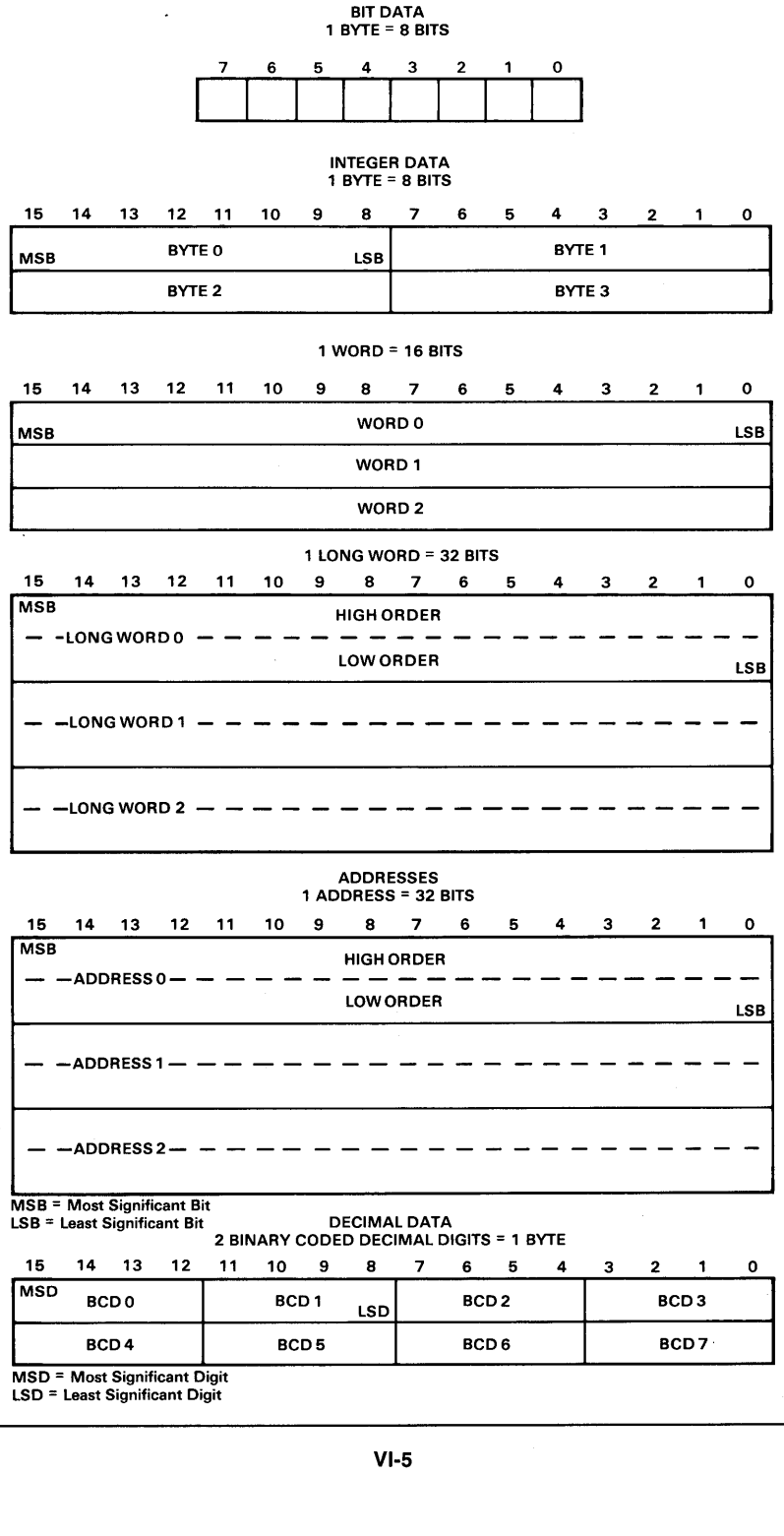
The MK68000 separates memory references into two classes: program references, and data references. Program references, as the name implies, are references to that section of memory that contains the program being

WORD ORGANIZATION IN MEMORY
Figure 1



DATA ORGANIZATION IN MEMORY

Figure 2



VI

executed. Data references refer to that section of memory that contains data. Generally, operand reads are from the data space. All operand writes are to the data space.

REGISTER SPECIFICATION

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register selected is an address or data register and how the register is to be used.

EFFECTIVE ADDRESS

Most instructions specify the location of an operand by using the effective address field in the operation word. For example, Figure 4 shows the general format of the single effective address instruction operation word. The effective address is composed of two 3-bit fields: the mode field, and the register field. The value in the mode field selects the different address modes. The register field contains the number of a register.

The effective address field may require additional information to fully specify the operand. This additional information, called the effective address extension, is contained in the following word or words and is considered part of the instruction, as shown in Figure 3. The effective address modes are grouped into three categories: register direct, memory addressing, and special.

REGISTER DIRECT MODES

These effective addressing modes specify that the operand is in one of the 16 multifunction registers.

Data Register Direct. The operand is in the data register specified by the effective address register field.

Address Register Direct. The operand is in the address register specified by the effective address register field.

MEMORY ADDRESS MODES

These effective addressing modes specify that the operand is in memory and provide the specific address of the operand.

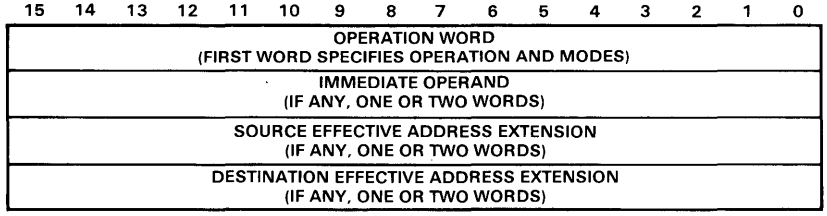
Address Register Indirect. The address of the operand is in the address register specified by the register field. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Postincrement. The address of the operand is in the address register specified by the register field. After the operand address is used, it is incremented by one, two, or four depending upon whether the size of the operand is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is incremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

Address Register Indirect With Predecrement. The address of the operand is in the address register specified by the register field. Before the operand address is used, it is decremented by one, two, or four depending upon whether the operand size is byte, word, or long word. If the address register is the stack pointer and the operand size is byte, the address is decremented by two rather than one to keep the stack pointer on a word boundary. The reference is classified as a data reference.

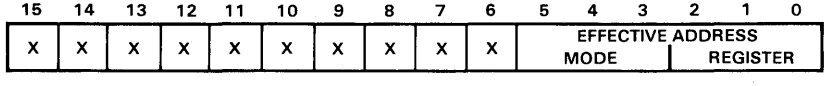
INSTRUCTION OPERATION WORD GENERAL FORMAT

Figure 3



SINGLE-EFFECTIVE-ADDRESS INSTRUCTION OPERATION WORD

Figure 4



Address Register Indirect With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register and the sign-extended 16-bit displacement integer in the extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Address Register Indirect With Index. This address mode requires one word of extension. The address of the operand is the sum of the address in the address register, the sign-extended displacement integer in the low order eight bits of the extension word, and the contents of the index register. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

SPECIAL ADDRESS MODES

The special address modes use the effective address register field to specify the special addressing mode instead of a register number.

Absolute Short Address. This address mode requires one word of extension. The address of the operand is the extension word. The 16-bit address is sign extended before it is used. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Absolute Long Address. This address mode requires two words of extension. The address of the operand is developed by the concatenation of the extension words. The high-order part of the address is the first extension word; the low-order part of the address is the second extension word. The reference is classified as a data reference with the exception of the jump and jump to subroutine instructions.

Program Counter With Displacement. This address mode requires one word of extension. The address of the operand is the sum of the address in the program counter and the sign-extended 16-bit displacement integer in the extension word. The value in the program counter is the address of the extension word. The reference is classified as a program reference.

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4

Addressing Mode	Mode	Register
Data Register Direct	000	register number
Address Register Direct	001	register number
Address Register Indirect	010	register number
Address Register Indirect with Postincrement	011	register number
Address Register Indirect with Predecrement	100	register number
Address Register Indirect with Displacement	101	register number
Address Register Indirect with Index	110	register number
Absolute Short	111	000
Absolute Long	111	001
Program Counter with Displacement	111	010
Program Counter with Index	111	011
Immediate or Status Register	111	100

IMPLICIT INSTRUCTION REFERENCE SUMMARY

Table 5

Instruction	Implied Register(s)
Branch Conditional (B_{CC}), Branch Always (BRA)	PC
Branch to Subroutine (BSR)	PC, SP
Check Register against Bounds (CHK)	SSP, SR
Test Condition, Decrement and Branch (DB_{CC})	PC
Signed Divide (DIVS)	SSP, SR
Unsigned Divide (DIVU)	SSP, SR
Jump (JMP)	PC
Jump to Subroutine (JSR)	PC, SP
Link and Allocate (LINK)	SP
Move Condition Codes (MOVE CCR)	SR
Move Status Register (MOVE SR)	SR
Move User Stack Pointer (MOVE USP)	USP
Push Effective Address (PEA)	SP
Return from Exception (RTE)	PC, SP, SR
Return and Restore Condition Codes (RTR)	PC, SP, SR
Return from Subroutine (RTS)	PC, SP
Trap (TRAP)	SSP, SR
Trap on Overflow (TRAPV)	SSP, SR
Unlink (UNLK)	SP

Program Counter With Index. This address mode requires one word of extension. The address is the sum of the address in the program counter, the sign-extended displacement integer in the lower eight bits of the extension word, and the contents of the index register. The value in the program counter is the address of the extension word. This reference is classified as a program reference.

Immediate Data. This address mode requires either one or two words of extension depending on the size of the operation.

Byte operation - operand is low order byte of extension word
Word operation - operand is extension word
Long word operation - operand is in the two extension words, high-order 16 bits are in the first extension word, low-order 16 bits are in the second extension word.

Condition Codes or Status Register. A selected set of instructions may reference the status register by means of the effective address field. These are:

ANDI to CCR
ANDI to SR
EORI to CCR
EORI to SR
ORI to CCR
ORI to SR

EFFECTIVE ADDRESS ENCODING SUMMARY

Table 4 is a summary of the effective addressing modes discussed in the previous paragraphs.

IMPLICIT REFERENCE

Some instructions make implicit reference to the program counter (PC), the system stack pointer (SP), the supervisor stack pointer (SSP), the user stack pointer (USP), or the status register (SR). Table 5 provides a list of these instructions and the registers implied.

SYSTEM STACK

The system stack is used implicitly by many instructions; user stacks and queues may be created and maintained through the addressing modes. Address register seven (A7) is the system stack pointer (SP). The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S-bit in the status register. If the S-bit indicates supervisor state, SSP is the active system stack pointer, and the USP cannot be referenced as an address register. If the S-bit indicates user state, the USP is the active system stack pointer, and the SSP cannot be referenced. Each system stack fills from high memory to low memory.

INSTRUCTION SET SUMMARY

The following paragraphs contain an overview of the form and structure of the MK68000 instruction set. The instructions form a set of tools that include all the machine functions to perform the following operations:

Data Movement
Integer Arithmetic
Logical
Shift and Rotate
Bit Manipulation
Binary Coded Decimal
Program Control
System Control

The complete range of instruction capabilities combined with the flexible addressing modes described previously provide a very flexible base for program development.

DATA MOVEMENT OPERATIONS

The basic method of data acquisition (transfer and storage) is provided by the move (MOVE) instruction. The move instruction and the effective addressing modes allow both address and data manipulation. Data move instructions allow byte, word, and long word operands to be transferred from memory to memory, memory to register, register to memory, and register to register. Address move instructions allow word and long word operand transfers and ensure that only legal address manipulations are executed. In addition to the general move instruction there are several special data movement instructions: move multiple registers (MOVEM), move peripheral data (MOVEP), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), unlink stack (UNLK), and move quick (MOVEQ). Table 6 is a summary of the data movement operations.

INTEGER ARITHMETIC OPERATIONS

The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP), clear (CLR), and negate (NEG). The add and subtract instructions are available for both address and data operations, with data operations accepting all operand sizes. Address operations are limited to legal address size operands (16 or 32 bits). Data, address, and memory compare operations are also available. The clear and negate instructions may be used on all sizes of data operands.

The multiply and divide operations are available for signed and unsigned operands using word multiply to produce a long word product, and a long word dividend with word divisor to produce a word quotient with a word remainder.

Multiprecision and mixed size arithmetic can be accomplished using a set of extended instructions. These instructions are: add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX).

A test operand (TST) instruction that will set the condition codes as a result of a compare of the operand with zero is also available. Test and set (TAS) is a synchronization

instruction useful in multiprocessor systems. Table 7 is a summary of the integer arithmetic operations.

DATA MOVEMENT OPERATIONS

Table 6

Instruction	Size	Operation
EXG	32	Rx ⟷ Ry
LEA	32	EA → An
LINK	—	An → -(SP) SP → An SP + displacement → SP
MOVE	8, 16, 32	(EA)s → EAd
MOVEM	16, 32	(EA) → An, Dn An, Dn → EA
MOVEP	16, 32	(EA) → Dn Dn → EA
MOVEQ	8	#xxx → Dn
PEA	32	EA → -(SP)
SWAP	32	Dn[31:16] Dn[15:0]
UNLK	—	An → Sp (SP)+ → An

NOTES:

s = source
d = destination
[ ] = bit numbers
-( ) = indirect with predecrement
( )+ = indirect with postincrement
= immediate data

LOGICAL OPERATIONS

Logical operation instructions AND, OR, EOR, and NOT are available for all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provides these logical operations with all sizes of immediate data. Table 8 is a summary of the logical operations.

SHIFT AND ROTATE OPERATIONS

Shift operations in both directions are provided by the arithmetic instructions ASR and ASL and logical shift instructions LSR and LSL. The rotate instructions (with and without extend) available are ROXR, ROXL, ROR, and ROL. All shift and rotate operations can be performed in either registers or memory. Register shifts and rotates support all operand sizes and allow a shift count specified in the instruction of one to eight bits, or 0 to 63 specified in a data register.

INTEGER ARITHMETIC OPERATIONS

Table 7

Instruction	Operand Size	Operation
ADD	8, 16, 32 16, 32	Dn + (EA) → Dn (EA) + Dn → EA (EA) + #xxx → EA An + (EA) → An
ADDX	8, 16, 32 16, 32	Dx + Dy + X → Dx -(Ax) + -(Ay) + X → (Ax)
CLR	8, 16, 32	0 → EA
CMP	8, 16, 32 16, 32	Dn - (EA) (EA) - #xxx -(Ax) - (Ay)+ An - (EA)
DIVS	32 — 16	Dn/(EA) → Dn
DIVU	32 — 16	Dn/(EA) → Dn
EXT	8 → 16 16 → 32	$(Dn)_8 \rightarrow Dn_{16}$ $(Dn)_{16} \rightarrow Dn_{32}$
MULS	16* 16 → 32	Dn* (EA) → Dn
MULU	16* 16 → 32	Dn* (EA) → Dn
NEG	8, 16, 32	0 - (EA) → EA
NEGX	8, 16, 32	0 - (EA) - X - EA
SUB	8, 16, 32 16, 32	Dn - (EA) → Dn (EA) - Dn → EA (EA) - #xxx → EA An - (EA) → An
SUBX	8, 16, 32	Dx - Dy - X → Dx -(Ax) - - (Ay) - X → (Ax)
TAS	8	(EA) - 0, 1 → EA[7]
TST	8, 16, 32	(EA) - 0

NOTE: [ ] = bit number **x = extend bit**

Memory shifts and rotates are for word operands only and allow only single-bit shifts or rotates.

Table 9 is a summary of the shift and rotate operations.

BIT MANIPULATION OPERATIONS

Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). Table 10 is a summary of the bit manipulation operations. (Bit 2 of the status register is Z.)

LOGICAL OPERATIONS

Table 8

Instruction	Operand Size	Operation
AND	8, 16, 32	Dn∧(EA) → Dn (EA)∧Dn → EA (EA)∧#xxx → EA
OR	8, 16, 32	Dn v (EA) → Dn (EA) v Dn → EA (EA) v #xxx → EA
EOR	8, 16, 32	(EA) ⊕ Dy → EA (EA) ⊕ #xxx → EA
NOT	8, 16, 32	~(EA) → EA

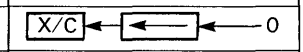
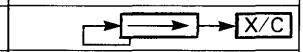
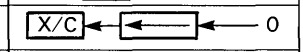
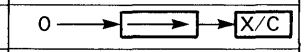
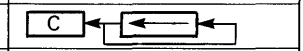
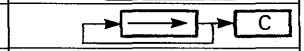
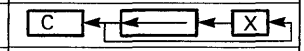
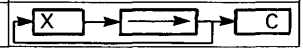
NOTE: ~ = invert

BINARY CODED DECIMAL OPERATIONS

Multiprecision arithmetic operations on binary coded decimal numbers are accompolished using the following instructions: add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 11 is a summary of the binary coded decimal operations.

SHIFT AND ROTATE OPERATIONS

Table 9

Instruction	Operand Size	Operation
ASL	8, 16, 32	
ASR	8, 16, 32	
LSL	8, 16, 32	
LSR	8, 16, 32	
ROL	8, 16, 32	
ROR	8, 16, 32	
ROXL	8, 16, 32	
ROXR	8, 16, 32	

BIT MANIPULATION OPERATIONS

Table 10

Instruction	Operand Size	Operation
BTST	8, 32	~bit of (EA) → Z
BSET	8, 32	~bit of (EA) → Z 1 → bit of EA
BCLR	8, 32	~bit of (EA) → Z 0 → bit of EA
BCHG	8, 32	~bit of (EA) → Z ~bit of (EA) → bit of EA

BINARY CODED DECIMAL OPERATIONS

Table 11

Instruction	Operand Size	Operation
ABCD	8	$Dx_{10}+Dy_{10}+X \rightarrow Dx$ $-(Ax)_{10} + -(Ay)_{10} + X \rightarrow (Ax)$
SBCD	8	$Dx_{10} - Dy_{10} - X \rightarrow Dx$ $-(Ax)_{10} - -(Ay)_{10} - X \rightarrow (Ax)$
NBCD	8	$0 - (EA)_{10} - X \rightarrow EA$

PROGRAM CONTROL OPERATIONS

Program control operations are accomplished using a series of conditional and unconditional branch instructions and return instructions. These instructions are summarized in Table 12.

The conditional instructions provide setting and branching for the following conditions:

CC - carry clear
CS - carry set
EQ - equal
F - never true
GE - greater or equal
GT - greater than
HI - high
LE - less or equal
LS - low or same
LT - less than
MI - minus
NE - not equal
PL - plus
T - always true
VC - no overflow
VS - overflow

PROGRAM CONTROL OPERATIONS

Table 12

Instruction	Operation
Conditional	
B_{CC}	Branch conditionally (14 conditions) 8- and 16-bit displacement
DB_{CC}	Test condition, decrement, and branch 16-bit displacement
S_{CC}	Set byte conditionally (16 conditions)
Unconditional	
BRA	Branch always 8- and 16-bit displacement
BSR	Branch to subroutine 8- and 16-bit displacement
JMP	Jump
JSR	Jump to subroutine
Returns	
RTR	Return and restore condition codes
RTS	Return from subroutine

SYSTEM CONTROL OPERATIONS

System control operations are accomplished by using privileged instructions, trap generating instructions, and instructions that use or modify the status register. These instructions are summarized in Table 13.

SIGNAL AND BUS OPERATION DESCRIPTION

The following paragraphs contain a brief description of the input and output signals. A discussion of bus operation during the various machine cycles and operations is also given.

SIGNAL DESCRIPTION

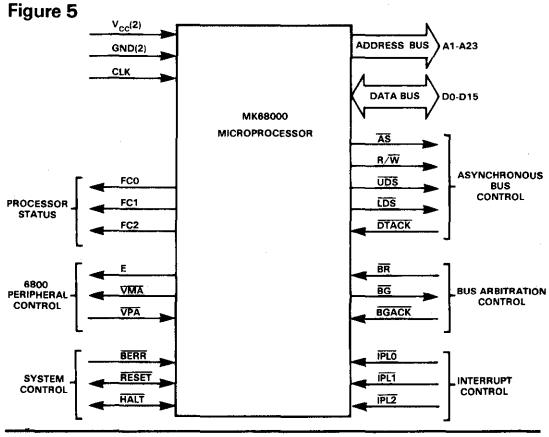
The input and output signals can be functionally organized into the groups shown in Figure 5. The following paragraphs provide a brief description of the signals and also a reference (if applicable) to other paragraphs that contain more detail about the function being performed.

ADDRESS BUS (A1 THROUGH A23). This 23-bit, unidirectional, three-state bus is capable of addressing 8 megawords of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A4 through A23 are all set to a logic high.

DATA BUS (D0 THROUGH D15). This 16-bit bidirectional, three-state bus is the general purpose data path. It can transfer and accept data in either word or byte length. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0-D7.

ASYNCHRONOUS BUS CONTROL. Asynchronous data transfers are handled using the following control signals: address strobe, read/write, upper and lower data strobes, and data transfer acknowledge. These signals are explained in the following paragraphs.

INPUT AND OUTPUT SIGNALS
Figure 5



SYSTEM CONTROL OPERATIONS
Table 13

Instruction	Operation
Privileged	
RESET	Reset external devices
RTE	Return from exception
STOP	Stop program execution
ORI to SR	Logical OR to status register
MOVE USP	Move user stack pointer
ANDI to SR	Logical AND to status register
EORI to SR	Logical EOR to status register
MOVE EA to SR	Load new status register
Trap Generating	
TRAP	Trap
TRAPV	Trap on overflow
CHK	Check data register against upper bounds
Status Register	
ANDI to CCR	Logical AND to condition codes
EORI to CCR	Logical EOR to condition codes
MOVE EA to CCR	Load new condition codes
ORI to CCR	Logical OR to condition codes
MOVE SR to EA	Store status register

Address Strobe ($\overline{AS}$). This signal indicates that there is a valid address on the address bus.

Read/Write (R/$\overline{W}$). This signal defines the data bus transfer as a read or write cycle. The R/$\overline{W}$ signal also works in conjunction with the upper and lower data strobes as explained in the following paragraph.

Upper And Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$). These signals control the data on the data bus, as shown in Table 14. When the R/$\overline{W}$ line is high, the processor will read from the data bus as indicated. When the R/$\overline{W}$ line is low, the processor will write to the data bus as shown.

Data Transfer Acknowledge ($\overline{DTACK}$). This input indicates that the data transfer is completed. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

An active transition of data transfer acknowledge, $\overline{DTACK}$, indicates the termination of a data transfer on the bus.

If the system must run at a maximum rate determined by RAM access times, the relationship between the times at which $\overline{DTACK}$ and DATA are sampled are important.

VI

All control and data lines are sampled during the MK68000's clock high time. The clock is internally buffered, which results in some slight differences in the sampling and recognition of various signals. The $\overline{DTACK}$ signal, like other control signals, is internally synchronized to allow for valid operation in an asynchronous system. If the required setup time (#47) is met during S4, $\overline{DTACK}$ will be recognized during S5 and S6, and data will be captured during S6. The data must meet the required setup time (#27).

DATA STROBE CONTROL OF DATA BUS
Table 14

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D8-D15	D0-D7
High	High	-	No valid data	No valid data
Low	Low	High	Valid data bits 8-15	Valid data bits 0-7
High	Low	High	No valid data	Valid data bits 0-7
Low	High	High	Valid data bits 8-15	No valid data
Low	Low	Low	Valid data bits 8-15	Valid data bits 0-7
High	Low	Low	Valid data bits 0-7*	Valid data bits 0-7
Low	High	Low	Valid data bits 8-15	Valid data bits 8-15*

*These conditions are a result of current implementation and may not appear on future devices.

If an asynchronous control signal does not meet the required setup time, it is possible that it may not be recognized during that cycle. Because of this, asynchronous systems must not allow $\overline{DTACK}$ to precede data by more than parameter #31.

Asserting $\overline{DTACK}$ (or $\overline{BERR}$) on the rising edge of a clock (such as S4) after the assertion of address strobe will allow an MK68000 system to run at its maximum bus rate. If setup times #27 and #47 are guaranteed, #31 may be ignored. If $\overline{DTACK}$ and $\overline{BERR}$ are asserted at the same time, the MK68000 will recognize the $\overline{BERR}$ and abort the cycle.

BUS ARBITRATION CONTROL. These three signals form a bus arbitration circuit to determine which device will be the bus master device.

Bus Request ($\overline{BR}$). This input is write ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master.

Bus Grant ($\overline{BG}$). This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$). This input indicates that some other device has become the bus master. This signal cannot be asserted until the following four conditions are met:

1. a bus grant has been received
2. address strobe is inactive which indicates that the microprocessor is not using the bus
3. data transfer acknowledge is inactive which indicates that either memory or the peripherals are not using the bus
4. bus grant acknowledge is inactive which indicates that no other device is still claiming bus mastership

INTERRUPT CONTROL ($\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$). These input pins indicate the encoded priority level of the device requesting an interrupt. Level seven is the highest priority while level zero indicates that no interrupts are requested. The least significant bit is given in $\overline{IPL0}$ and the most significant bit is contained in $\overline{IPL2}$. These lines must remain stable until the processor signals interrupt acknowledge (FC0-FC2 are all high) to insure that the interrupt is recognized.

SYSTEM CONTROL. The system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred. The three system control inputs are explained in the following paragraphs.

Bus Error ($\overline{BERR}$). This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. nonresponding devices
2. interrupt vector number acquisition failure
3. illegal access request as determined by a memory management unit
4. other application dependent errors.

The bus error signal interacts with the halt signal to determine if exception processing should be performed or the current bus cycle should be retried.

Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction of the bus error and halt signals.

Reset ($\overline{RESET}$). This bidirectional signal line acts to reset (initiate a system initialization sequence) the processor in response to an external reset signal. An internally generated reset (result of RESET instruction) causes all external devices to be reset and the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external halt and reset signals applied at the same time. Refer to RESET OPERATION paragraph for additional information about reset operation.

Halt ($\overline{HALT}$). When this bidirectional line is driven by an external device, it will cause the processor to stop at the completion of the current bus cycle. When the processor

FUNCTION CODE OUTPUTS

Table 15

FC2	FC1	FC0	Cycle Type
Low	Low	Low	(Undefined, Reserved)
Low	Low	High	User Data
Low	High	Low	User Program
Low	High	High	(Undefined, Reserved)
High	Low	Low	(Undefined, Reserved)
High	Low	High	Supervisor Data
High	High	Low	Supervisor Program
High	High	High	Interrupt Acknowledge

has been halted using this input, all control signals are inactive and all three-state lines are put in their high-impedance state. Refer to BUS ERROR AND HALT OPERATION paragraph for additional information about the interaction between the halt and bus error signals.

When the processor has stopped executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

6800 PERIPHERAL CONTROL. These control signals are used to allow the interfacing of synchronous 6800 peripheral devices with the asynchronous MK68000. These signals are explained in the following paragraphs.

SIGNAL SUMMARY

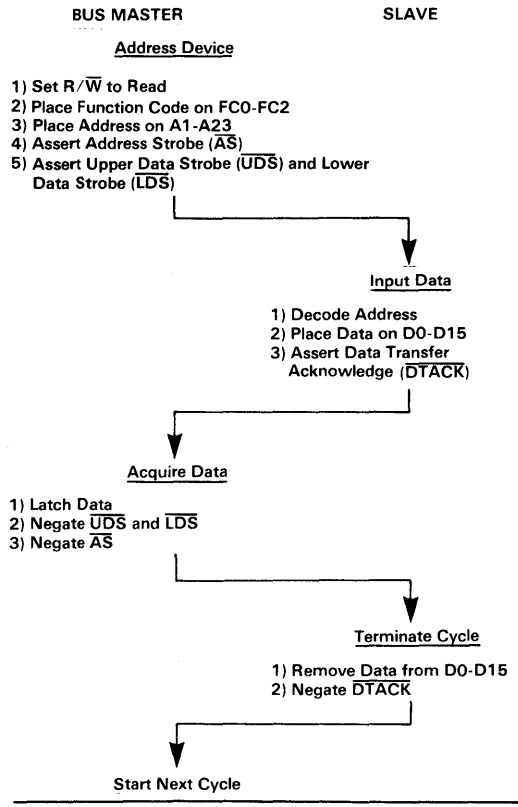
Table 16

Signal Name	Mnemonic	Input/Output	Active State	Three State	
				On $\overline{HALT}$	On $\overline{BGACK}$
Address Bus	A1-A23	output	high	yes	yes
Data Bus	D0-D15	input/output	high	yes	yes
Address Strobe	$\overline{AS}$	output	low	no	yes
Read/Write	R/$\overline{W}$	output	read-high write-low	no	yes
Upper and Lower Data Strobes	$\overline{UDS}$, $\overline{LDS}$	output	low	no	yes
Data Transfer Acknowledge	$\overline{DTACK}$	input	low	no	no
Bus Request	$\overline{BR}$	input	low	no	no
Bus Grant	$\overline{BG}$	output	low	no	no
Bus Grant Acknowledge	$\overline{BGACK}$	input	low	no	no
Interrupt Priority Level	$\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$	input	low	no	no
Bus Error	$\overline{BERR}$	input	low	no	no
Reset	$\overline{RESET}$	input/output	low	no*	no*
Halt	$\overline{HALT}$	input/output	low	no*	no*
Enable	E	output	high	no	no
Valid Memory Address	$\overline{VMA}$	output	low	no	yes
Valid Peripheral Address	$\overline{VPA}$	input	low	no	no
Function Code Output	FC0, FC1, FC2	output	high	no	yes
Clock	CLK	input	high	no	no
Power Input	V_{CC}	input	—	—	—
Ground	GND	input	—	—	—

* open drain

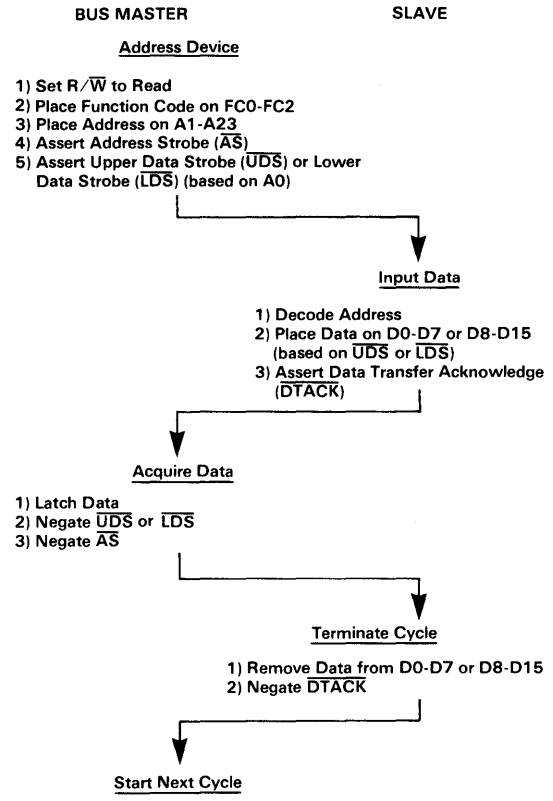
WORD READ CYCLE FLOW CHART

Figure 6



BYTE READ CYCLE FLOW CHART

Figure 7



Enable (E). This signal is the standard enable signal common to all 6800 type peripheral devices. The period for this output is ten MK68000 clock periods (six clocks low; four clocks high). Enable is generated by an internal ring counter which may come up in any state. (i.e., at power on, it is impossible to guarantee phase relationship of E to CLK). E is a free-running clock and runs regardless of the state of the bus on the MPU.

Valid Peripheral Address (VPA). This input indicates that the device or region addressed is a 6800 family device and that data transfer should be synchronized with the enable (E) signal. This input also indicates that the processor should use automatic vectoring for an interrupt. Refer to INTERFACE WITH 6800 PERIPHERALS.

Valid Memory Address (VMA). This output is used to indicate to 6800 peripheral devices that there is a valid address on the address bus and the processor is synchronized to enable. This signal only responds to a valid peripheral address (VPA) input which indicates that the peripheral is a 6800 family device.

PROCESSOR STATUS (FC0, FC1, FC2). These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed, as shown in Table 15. The information indicated by the function code outputs is valid whenever address strobe (AS) is active.

CLOCK (CLK). The clock input is a TTL compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should not be gated off at any time, and the clock signal must conform to minimum and maximum pulse width times.

SIGNAL SUMMARY. Table 16 is a summary of all the signals discussed in the previous paragraphs.

BUS OPERATION

The following paragraphs explain control signal and bus operation during data transfer operations, bus arbitration, bus error and halt conditions, and reset operation.

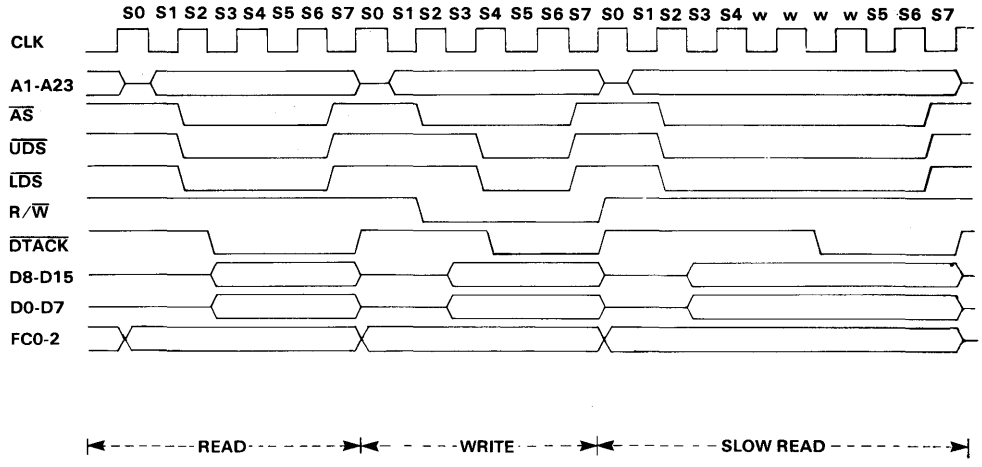
DATA TRANSFER OPERATIONS. Transfer of data between devices involves the following leads:

- Address Bus A1 through A23
- Data Bus D0 through D15
- Control Signals

The address and data buses are separate parallel buses

READ AND WRITE CYCLE TIMING DIAGRAM

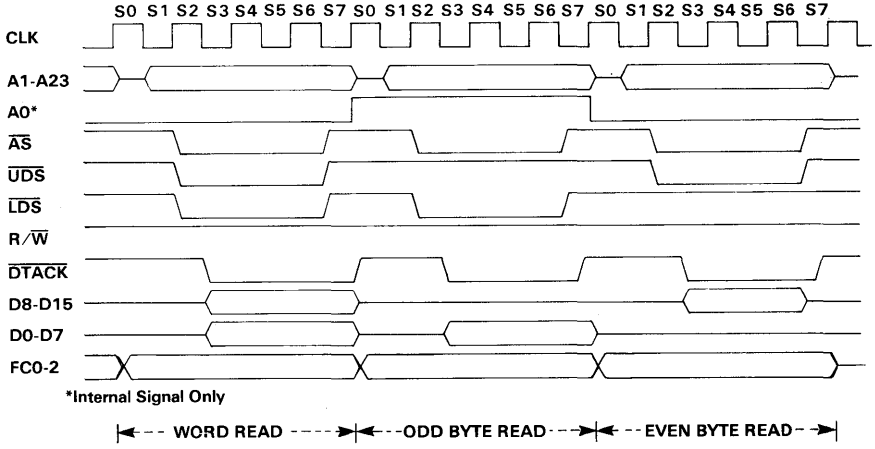
Figure 8



VI

WORD AND BYTE READ CYCLE TIMING DIAGRAM

Figure 9



used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the MK68000 for interlocked multiprocessor communications.

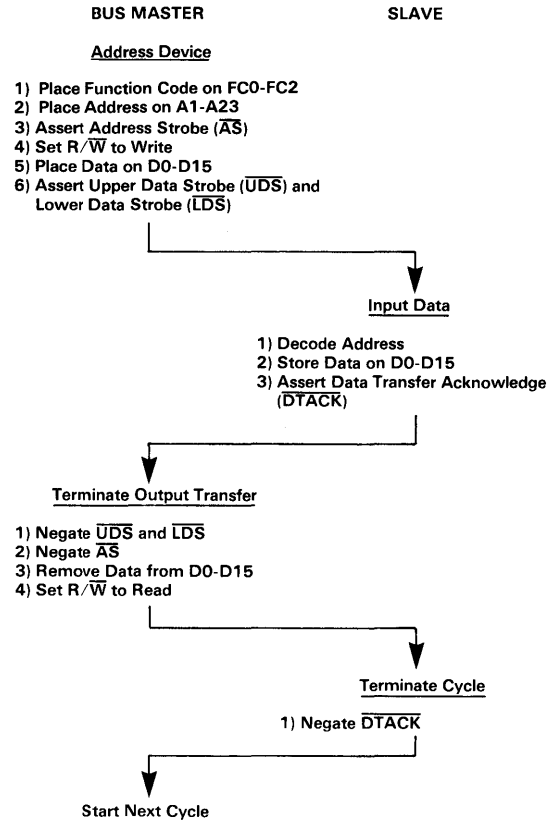
NOTE

The terms assertion and negation will be used extensively. This is done to avoid confusion when dealing with a mixture of "active-low" and "active-high" signals. The term assert or assertion is used to indicate that a signal is active or true independent of whether that voltage is low or high. The term negate or negation is used to indicate that a signal is inactive or false.

Read Cycle. During a read cycle, the processor receives data from memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both bytes. When the instruction specifies byte operation, the processor uses an internal A0 bit to determine which byte to read and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. When the data is received, the processor correctly positions it internally.

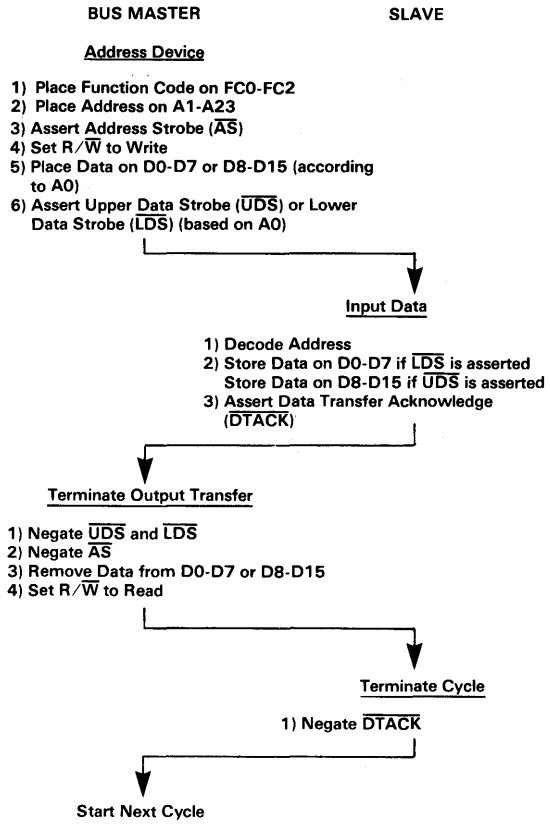
WORD WRITE CYCLE FLOW CHART

Figure 10



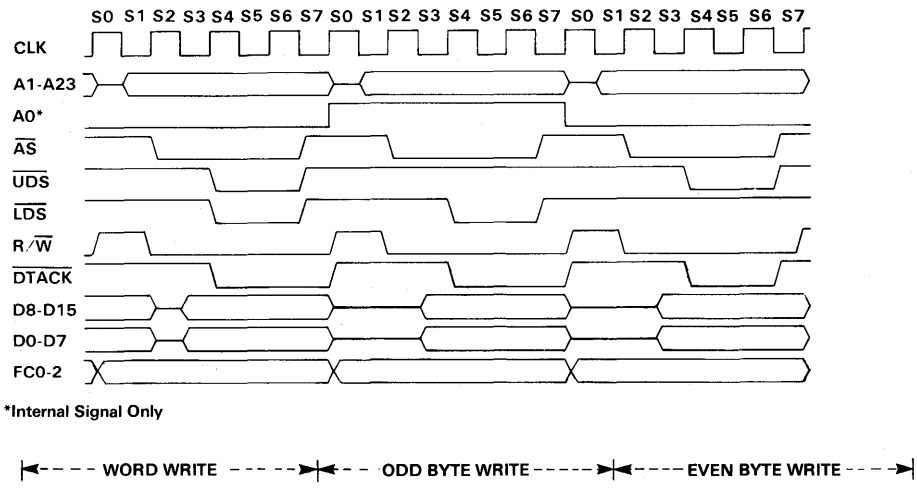
BYTE WRITE CYCLE FLOW CHART

Figure 11



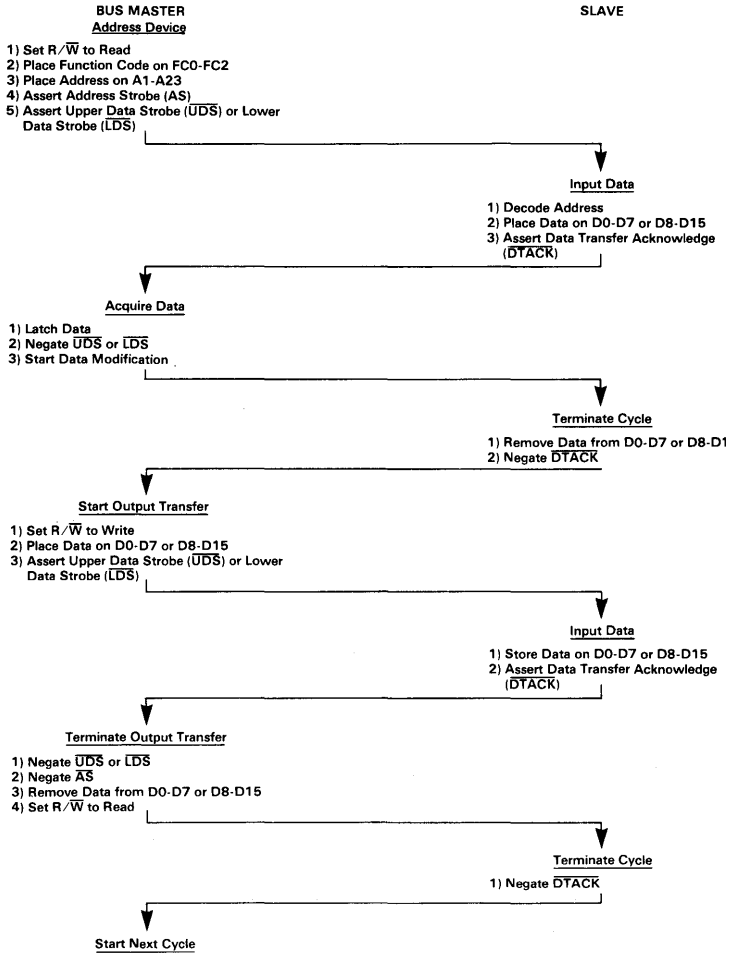
WORD AND BYTE WRITE CYCLE TIMING DIAGRAM

Figure 12



READ-MODIFY-WRITE CYCLE FLOW CHART

Figure 13



A word read cycle flow chart is given in Figure 6. A byte read cycle flow chart is given in Figure 7. Read cycle timing is given in Figure 8 and Figure 9 details word and byte read cycle operation.

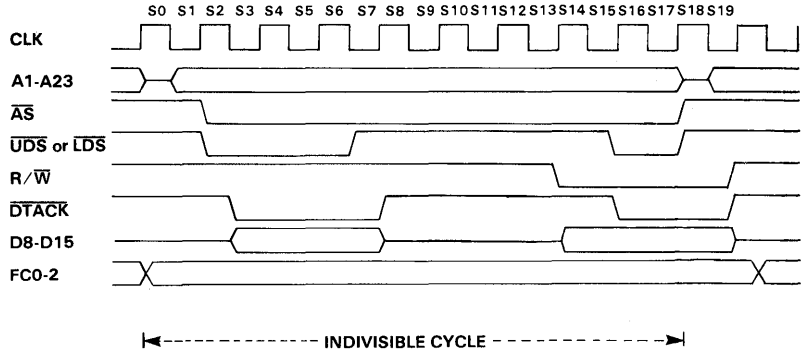
Write Cycle. During a write cycle, the processor sends data to memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes. When the instruction specifies a byte operation, the processor uses an internal A0 bit to determine which byte to write and then issues the data strobe required for that byte. For byte operations, when the A0 bit equals zero, the upper data strobe is issued. When the A0 bit equals one, the lower data strobe is issued. A word write cycle flow chart is given in Figure 10. A byte write cycle flow chart is given in Figure 11. Write cycle timing is given in Figure 8 and Figure 12 details word and byte write cycle operation.

Read-Modify-Write Cycle. The read-modify-write cycle performs a read, modifies the data in the arithmetic-logic unit, and writes the data back to the same address. In the MK68000 this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The test and set (TAS) instruction uses this cycle to provide meaningful communication between processors in a multiple processor environment. This instruction is the only instruction that uses the read-modify-write cycles and since the test and set instruction only operates on bytes, all read-modify-write cycles are byte operations. A read-modify-write cycle flow chart is given in Figure 13 and a timing diagram is given in Figure 14.

BUS ARBITRATION. Bus arbitration is a technique used by master-type devices to request, be granted, and acknowledge bus mastership. In its simplest form, it consists of:

READ—MODIFY-WRITE CYCLE TIMING DIAGRAM

Figure 14



1. Asserting a bus mastership request.
2. Receiving a grant that the bus is available at the end of the current cycle.
3. Acknowledging that mastership has been assumed.

Figure 15 is a flow chart showing the detail involved in a request from a single device. Figure 16 is a timing diagram for the same operations. This technique allows processing of bus requests during data transfer cycles.

The timing diagram shows that the bus request is negated at the time that an acknowledge is asserted. This type of operation would be true for a system consisting of the processor and one device capable of bus mastership. In systems having a number of devices capable of bus mastership, the bus request line from each device is wire ORed to the processor. In this system, it is easy to see that there could be more than one bus request being made. The timing diagram shows that the bus grant signal is negated a few clock cycles after the transition of the acknowledge (BGACK) signal.

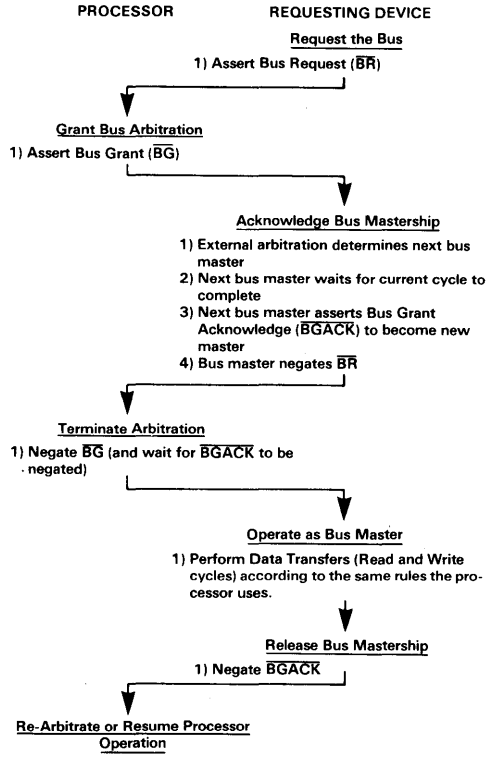
However, if the bus requests are still pending, the processor will assert another bus grant within a few clock cycles after it was negated. This additional assertion of bus grant allows external arbitration circuitry to select the next bus master before the current bus master has completed its requirements. The following paragraphs provide additional information about the three steps in the arbitration process.

Requesting the Bus. External devices capable of becoming bus masters request the bus by asserting the bus request (BR) signal. This is a wire ORed signal (although it need not be constructed from open collector devices) that indicates to the processor that some external device requires control of the external bus. The processor is effectively at a lower bus priority level than the external device and will relinquish the bus after it has completed the last bus cycle it has started.

When no acknowledge is received before the bus request signal goes inactive, the processor will continue processing when it detects that the bus request is inactive. This allows ordinary processing to continue if the arbitration circuitry responded to noise inadvertently.

BUS ARBITRATION CYCLE FLOW-CHART

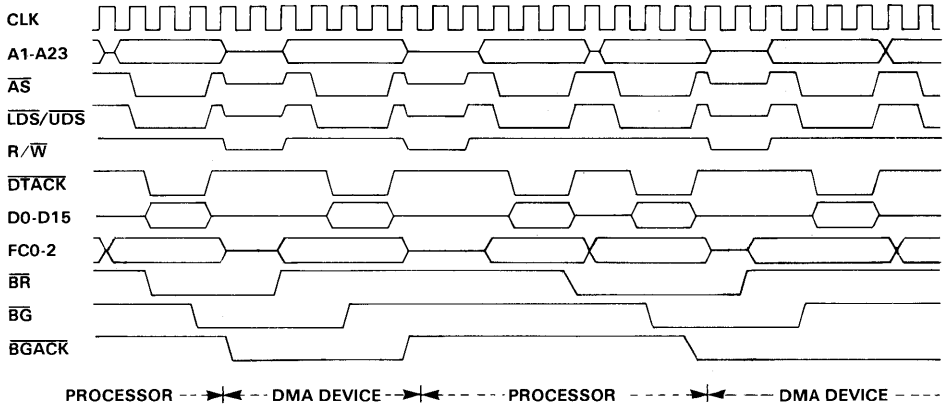
Figure 15



Receiving the Bus Grant. The processor asserts bus grant (BG) as soon as possible. Normally this is immediately after internal synchronization. The only exception to this occurs when the processor has made an internal decision to execute the next bus cycle but has not progressed far enough into the cycle to have asserted the address strobe

BUS ARBITRATION CYCLE TIMING DIAGRAM

Figure 16



(AS) signal. In this case, bus grant will not be asserted until one clock after address strobe is asserted to indicate to external devices that a bus cycle is being executed.
The bus grant signal may be routed through a daisy-chained network or through a specific priority-encoded network. The processor is not affected by the external method of arbitration as long as the protocol is obeyed.

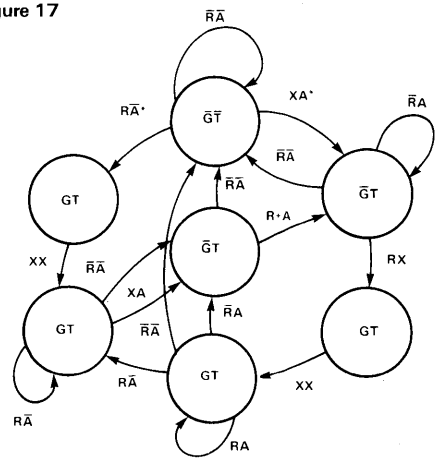
Acknowledgement of Mastership. Upon receiving a bus grant, the requesting device waits until address strobe, data transfer acknowledge, and bus grant acknowledge are negated before issuing its own BGACK. The negation of the address strobe indicates that the previous master has completed its cycle, the negation of bus grant acknowledge indicates that the previous master has released the bus. (While address strobe is asserted no device is allowed to "break into" a cycle.) The negation of data transfer acknowledge indicates the previous slave has terminated its connection to the previous master. Note that in some applications data transfer acknowledge might not enter into this function. General purpose devices would then be connected such that they were only dependent on address strobe. When bus grant acknowledge is issued the device is bus master until it negates bus grant acknowledge. Bus grant acknowledge should not be negated until after the bus cycle(s) is (are) completed. Bus mastership is terminated at the negation of bus grant acknowledge.

The bus request from the granted device should be dropped when bus grant acknowledge is asserted. If bus request is still asserted after bus grant acknowledge is negated, the processor performs another arbitration sequence and issues another bus grant. Note that the processor does not perform any external bus cycles before it re-asserts bus grant.

BUS ARBITRATION CONTROL. The bus arbitration control unit in the MK68000 is implemented with a finite state machine. A state diagram of this machine is shown in Figure 17. All asynchronous signals to the MK68000 are

STATE DIAGRAM OF MK68000 BUS ARBITRATION UNIT

Figure 17



R = Bus Request Internal
A = Bus Grant Acknowledge Internal
G = Bus Grant
T = Three-state Control to Bus Control Logic**
X = Don't Care

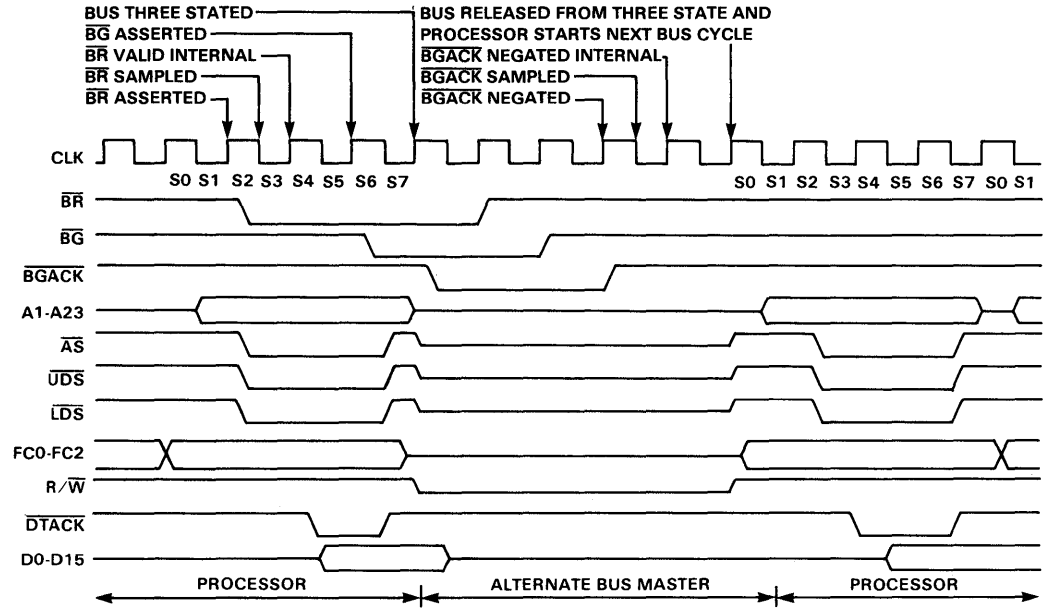
*State machine will not change state if bus is in S0. Refer to BUS ARBITRATION CONTROL for additional information.
**The address bus will be placed in the high impedance state if T is asserted and AS is negated.

synchronized before being used internally. This synchronization is accomplished in a maximum of one cycle of the system clock, assuming that the asynchronous input setup time (#47) has been met. The input signal is sampled on the falling edge of the clock and is valid internally after the next falling edge.

As shown in Figure 17, input signals labeled R and A are internally synchronized on the bus request and bus grant acknowledge pins respectively. The bus grant output is labeled G and the internal three-state control signal T. If T is true, the address, data, and control buses are placed in a

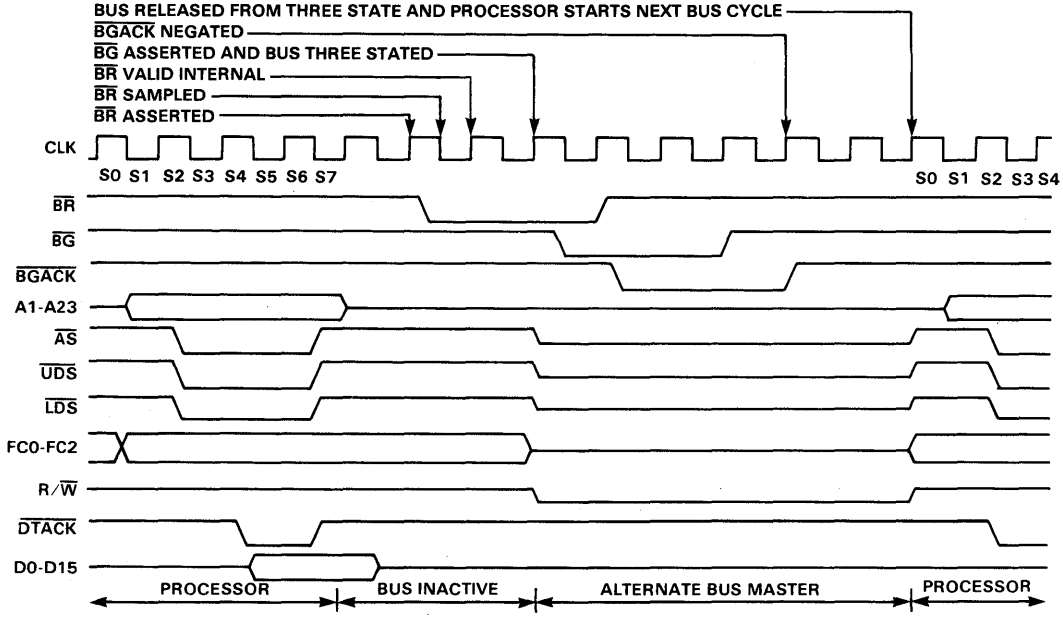
BUS ARBITRATION DURING PROCESSOR BUS CYCLE

Figure 18



BUS ARBITRATION WITH BUS INACTIVE

Figure 19



high-impedance state when $\overline{AS}$ is negated. All signals are shown in positive logic (active high) regardless of their true active voltage level.

State changes (valid outputs) occur on the next rising edge after the internal signal is valid.

A timing diagram of the bus arbitration sequence during a processor bus cycle is shown in Figure 18. The bus arbitration sequence while the bus is inactive (i.e., executing internal operations such as a multiply instruction) is shown in Figure 19.

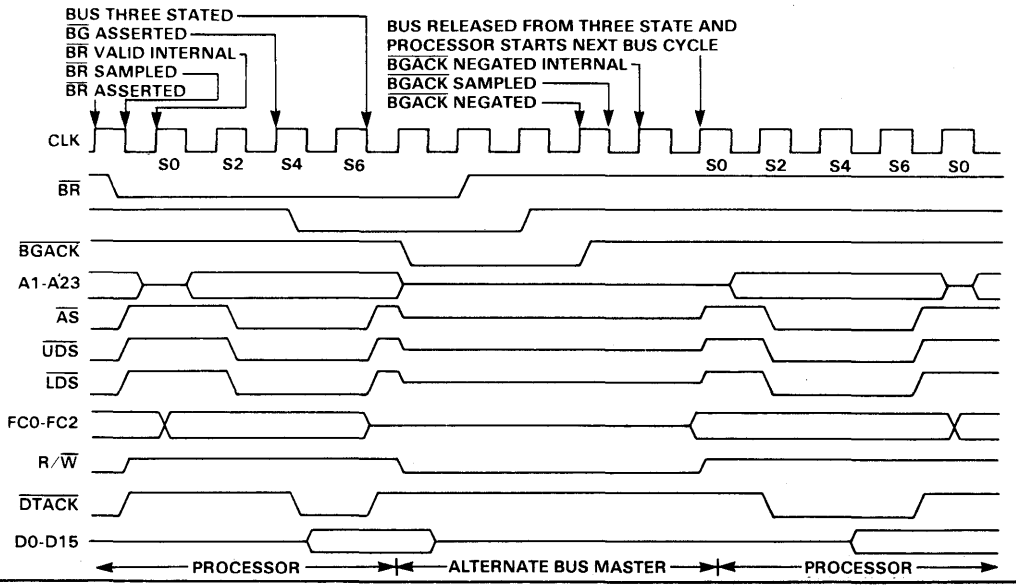
If a bus request is made at a time when the MPU has already begun a bus cycle but $\overline{AS}$ has not been asserted (bus state S0), $\overline{BG}$ will not be asserted on the next rising edge. Instead, $\overline{BG}$ will be delayed until the second rising edge following its internal assertion. This sequence is shown in Figure 20.

BUS ERROR AND HALT OPERATION. In a bus architecture that requires a handshake from an external device, the possibility exists that the handshake might not occur. Since different systems will require a different maximum response time, a bus error input is provided. External circuitry must be used to determine the duration between address strobe and data transfer acknowledge before issuing a bus error signal. When a bus error signal is received, the processor has two options: initiate a bus error exception sequence or try running the bus cycle again.

Exception Sequence. When the bus error signal is asserted, the current bus cycle is terminated. If $\overline{BERR}$ is asserted before the falling edge of S2, $\overline{AS}$ will be negated in S7 in either a read or write cycle. As long as $\overline{BERR}$ remains asserted, the data and address buses will be in the high-impedance state. When the $\overline{BERR}$ is negated, the processor will begin stacking for exception processing. The bus error exception sequence is entered when the processor receives

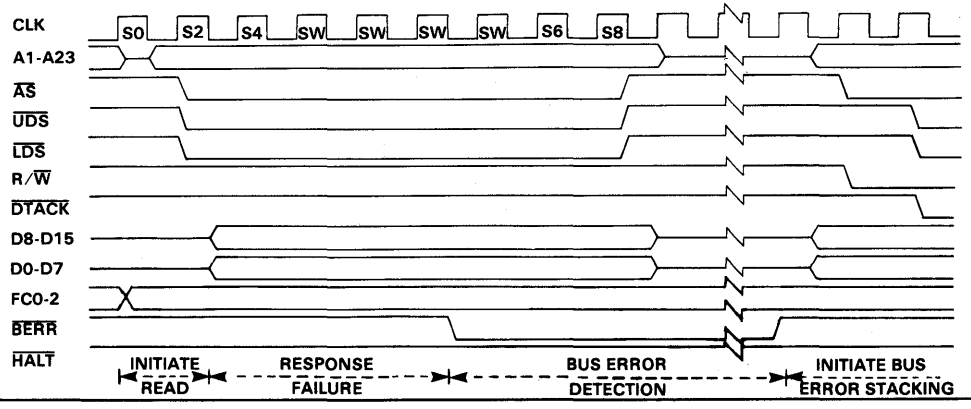
BUS ARBITRATION SPECIAL CASE

Figure 20



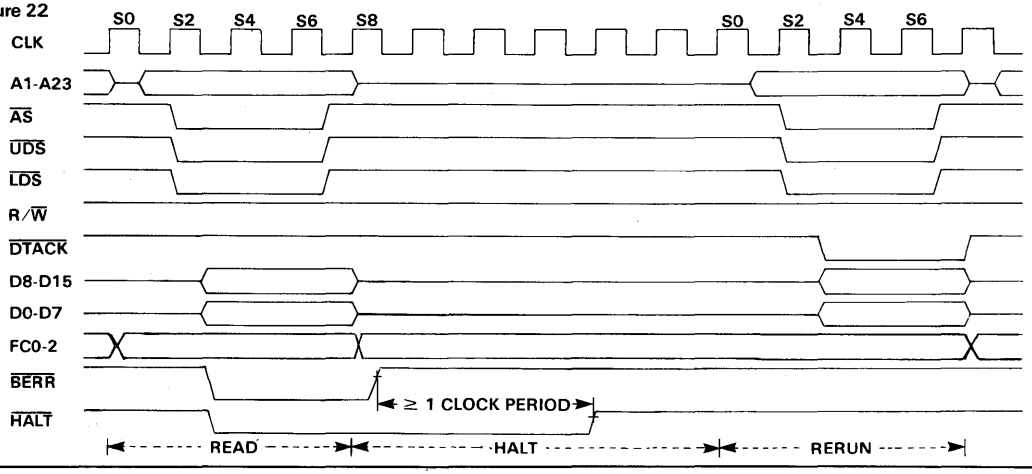
BUS ERROR TIMING DIAGRAM

Figure 21



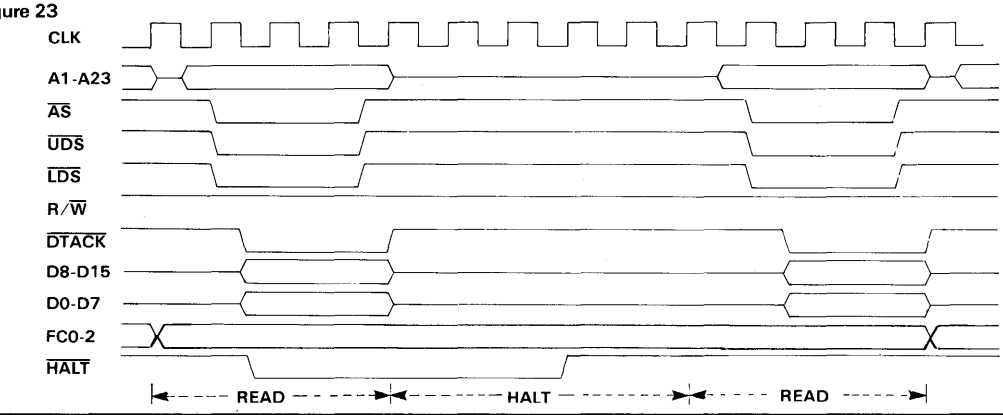
RE-RUN BUS CYCLE TIMING INFORMATION

Figure 22



HALT SIGNAL TIMING CHARACTERISTICS

Figure 23



a bus error signal and the halt pin is inactive. Figure 21 is a timing diagram for the exception sequence. The sequence is composed of the following elements:

1. Stacking the program counter and status register
2. Stacking the error information
3. Reading the bus error vector table entry
4. Executing the bus error handler routine

The stacking of the program counter and the status register is the same as if an interrupt had occurred. Several additional items are stacked when a bus error occurs. These items are used to determine the nature of the error and correct it, if possible. The bus error vector is vector number two located at address $000008. The processor loads the new program counter from this location. A software bus error handler routine is then executed by the processor. Refer to EXCEPTION PROCESSING for additional information.

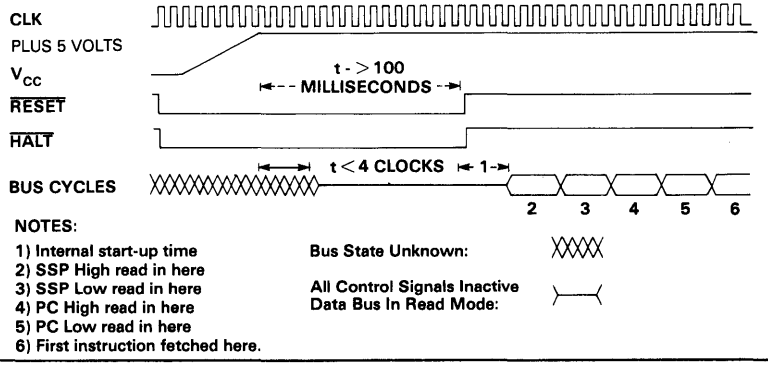
Re-Running the Bus Cycle. When the processor receives a bus error signal and the halt pin is being driven by an external device, the processor enters the re-run sequence. Figure 22 is a timing diagram for re-running the bus cycle. The processor terminates the bus cycle, then puts the address and data lines in the high-impedance state. The processor remains "halted," and will not run another bus cycle until the halt signal is removed by external logic. Then the processor will re-run the previous bus cycle using the same address, the same function codes, the same data (for a write operation), and the same controls. The bus error signal should be removed at least one clock cycle before the halt signal is removed.

NOTE

The processor will not re-run a read-modify-write cycle. This restriction is made to guarantee that the entire cycle runs correctly and that the write operation of a Test-and-Set operation is performed without ever releasing $\overline{AS}$. If $\overline{BERR}$ and $\overline{HALT}$ are asserted during a read-modify-write bus cycle, a bus error operation results.

Halt Operation with No Bus Error. The halt input signal to the MK68000 performs a Halt/Run/Single-Step function. The halt and run modes are somewhat self explanatory in that when the halt signal is constantly active the processor

RESET OPERATION TIMING DIAGRAM
Figure 24



"halts" (does nothing) and when the halt signal is constantly inactive the processor "runs" (does something).

The single-step mode is derived from correctly timed transitions on the halt signal input. It forces the processor to execute a single bus cycle by entering the "run" mode until the processor starts a bus cycle then changing to the "halt" mode. Thus, the single-step mode allows the user to proceed through (and therefore debug) processor operations one bus cycle at a time.

Figure 23 details the timing required for correct single-step operations. Some care must be exercised to avoid harmful interactions between the bus error signal and the halt pin when using the single cycle mode as a debugging tool. This is also true of interactions between the halt and reset lines, since these can reset the machine.

When the processor completes a bus cycle after recognizing that the halt signal is active, most three-state signals are put in the high-impedance state. These include:

1. address lines
2. data lines

This is required for correct performance of the re-run bus cycle operation.

While the processor is honoring the halt request, bus arbitration performs as usual. That is, halting has no effect on bus arbitration. It is the bus arbitration function that removes the control signals from the bus.

The halt function and the hardware trace capability allow the hardware debugger to trace single bus cycles or single instructions at a time. These processor capabilities, along with a software debugging package, give total debugging flexibility.

Double Bus Faults. When a bus error exception occurs, the processor will attempt to stack several words containing information about the state of the machine. If a bus error exception occurs during the stacking operation, there have been two bus errors in a row. This is commonly referred to as a double bus fault. When a double bus fault occurs, the processor will halt. Once a bus error exception has occurred, any bus error exception occurring before the execution of the next instruction constitutes a double bus fault.

Note that a bus cycle which is re-run does not constitute a bus error exception, and does not contribute to a double bus fault. Note also that this means that as long as the external hardware requests it, the processor will continue to re-run the same bus cycle.

The bus error pin also has an effect on processor operation after the processor receives an external reset input. The processor reads the vector table after a reset to determine the address to start program execution. If a bus error occurs while reading the vector table (or at any time before the first instruction is executed), the processor reacts as if a double bus fault has occurred and it halts. Only an external reset will start a halted processor.

RESET OPERATION. The reset signal is a bidirectional signal that allows either the processor or an external signal to reset the system. Figure 24 is a timing diagram for reset operations. Both the halt and the reset lines must be applied to ensure total reset of the processor.

When the reset and halt lines are driven by an external device, it is recognized as an entire system reset, including the processor. The processor responds by reading the reset vector table entry (vector number zero, address $000000) and loads it into the supervisor stack pointer (SSP). Vector table entry number one at address $000004 is read next and loaded into the program counter. The processor initializes the status register to an interrupt level of seven. No other registers are affected by the reset sequence.

When a RESET sequence is executed, the processor drives the reset pin for 124 clock periods. In this case, the processor is trying to reset the rest of the system. Therefore, there is no effect on the internal state of the processor. All of the processor's internal registers and the status register are unaffected by the execution of a RESET instruction. All external devices connected to the reset line will be reset at

$\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, $\overline{\text{HALT}}$ ASSERTION RESULTS

Table 17

Case No.	Control Signal	Asserted on Rising Edge of State		Result
		N	N+2	
1	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	S X X	Normal cycle terminate and continue.
2	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA A	S X S	Normal cycle terminate and halt. Continue when HALT removed.
3	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	A NA S	Normal cycle terminate and halt. Continue when HALT removed.
4	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A NA	X S NA	Terminate and take bus error trap.
5	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	X A A	X S S	Terminate and re-run.
6	$\overline{\text{DTACK}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA NA A	X A S	Terminate and re-run when HALT removed.

Legend:
- N — the number of the current even bus state (e.g., S4, S6, etc.)
- A — signal is asserted in this bus state
- NA — signal is not asserted in this state
- X — don't care
- S — signal was asserted in previous state and remains asserted in this state

$\overline{\text{BERR}}$ AND $\overline{\text{HALT}}$ NEGATION RESULTS

Table 18

Conditions of Termination in Table 17	Control Signal	Negated on Rising Edge of State			Results — Next Cycle
		N		N+2	
Bus Error	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• •	or or	• •	Takes bus error trap.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• •	or	•	Illegal sequence, usually traps to vector number 0.
Re-run	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	•		 •	Re-runs the bus cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	• •	 or	 •	May lengthen next cycle.
Normal	$\overline{\text{BERR}}$ $\overline{\text{HALT}}$	 •	 or	• none	If next cycle is started it will be terminated as a bus error.

Legend:
- • = signal is negated in this bus state

the completion of the RESET instruction.

Asserting the reset and halt pins for 10 clock cycles will cause a processor reset, except when V_{CC} is initially applied to the processor. In this case, an external reset must be applied to the reset pin for at least 100 milliseconds.

THE RELATIONSHIP OF $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, AND $\overline{\text{HALT}}$

In order to control termination of a bus cycle for a re-run or a bus error condition properly, $\overline{\text{DTACK}}$, $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ should be asserted and negated on the rising edge of the MK68000 clock. This will assure that when two signals are asserted simultaneously, the required setup time (#47) for both of them will be met during the same bus state.

This, or some equivalent precaution, should be designed external to the MK68000. Parameter #48 is intended to ensure this operation in a totally asynchronous system, and may be ignored if the above conditions are met.

The preferred bus cycle terminations may be summarized as follows (case numbers refer to Table 17):

Normal Termination: $\overline{\text{DTACK}}$ occurs first (case 1).
Halt Termination: $\overline{\text{HALT}}$ is asserted at same time, or precedes $\overline{\text{DTACK}}$ (no $\overline{\text{BERR}}$) cases 2 and 3.
Bus Error Termination: $\overline{\text{BERR}}$ is asserted in lieu of, at same time, or preceding $\overline{\text{DTACK}}$ (case 4); $\overline{\text{BERR}}$ negated at same time, or after $\overline{\text{DTACK}}$.
Re-Run Termination: $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ asserted at the same time, or before $\overline{\text{DTACK}}$ (cases 5 and 6); $\overline{\text{HALT}}$ must be negated at least 1 cycle after $\overline{\text{BERR}}$.

Table 17 details the resulting bus cycle termination under various combinations of control signal sequences. The negation of these same control signals under several conditions is shown in Table 18 ($\overline{\text{DTACK}}$ is assumed to be negated normally in all cases; for best results, both $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$ should be negated when address strobe is negated.)

Example A: A system uses a watch-dog timer to terminate accesses to un-populated address space. The timer asserts $\overline{\text{DTACK}}$ and $\overline{\text{BERR}}$ simultaneously after time-out. (case 4)

Example B: A system uses error detection on RAM contents. Designer may (a) delay $\overline{\text{DTACK}}$ until data verified, and return $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ simultaneously to re-run error cycle (case 5), or if valid, return $\overline{\text{DTACK}}$; (b) delay $\overline{\text{DTACK}}$ until data verified, and return $\overline{\text{BERR}}$ at same time as $\overline{\text{DTACK}}$ if data in error (case 4); (c) return $\overline{\text{DTACK}}$ prior to data verification, as described in previous section. If data invalid, $\overline{\text{BERR}}$ is asserted (case 1) in next cycle. Error-handling software must know how to recover error cycle.

PROCESSING STATES

The MK68000 is always in one of three processing states: normal, exception, or halted. The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands, and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made.

The exception processing state is associated with interrupts, trap instructions, tracing and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, by a bus error, or by a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

The halted processing state is an indication of catastrophic hardware failure. For example, if during the exception processing of a bus error another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

PRIVILEGE STATES

The processor operates in one of two states of privilege: the "user" state or the "supervisor" state. The privilege state determines which operations are legal, is used by the external memory management device to control and translate accesses, and is used to choose between the supervisor stack pointer and the user stack pointer in instruction references.

The privilege state is a mechanism for providing security in a computer system. Programs should access only their own code and data areas, and ought to be restricted from accessing information which they do not need and must not modify.

The privilege mechanism provides security by allowing most programs to execute in user state. In this state, the accesses are controlled, and the effects on other parts of the system are limited. The operating system executes in the supervisor state, has access to all resources, and performs the overhead tasks for the user state programs.

SUPERVISOR STATE. The supervisor state is the higher state of privilege. For instruction execution, the supervisor state is determined by the S-bit of the status register; if the S-bit is asserted (high), the processor is in the supervisor state. All instructions can be executed in the supervisor state. The bus cycles generated by instructions executed in the supervisor state are classified as supervisor references. While the processor is in the supervisor privilege state, those instructions which use either the system stack pointer implicity or address register seven explicitly access the supervisor stack pointer.

All exception processing is done in the supervisor state, regardless of the setting of the S-bit. The bus cycles generated during exception processing are classified as supervisor references. All stacking operations during exception processing use the supervisor stack pointer.

USER STATE. The user state is the lower state of privilege. For instruction execution, the user state is determined by the S-bit of the status register; if the S-bit is negated (low), the processor is executing instructions in the user state.

Most instructions execute the same in user state as in the supervisor state. However, some instructions which have important system effects are made privileged. User programs are not permitted to execute the STOP instruction, or the RESET instruction. To ensure that a user program cannot enter the supervisor state except in a controlled manner, the instructions which modify the whole status register are privileged. To aid in debugging programs which are to be used as operating systems, the move to user stack pointer (MOVE USP) and move from user stack pointer (MOVE from USP) instructions are also privileged.

The bus cycles generated by an instruction executed in user state are classified as user state references. This allows an external memory management device to translate the address and to control access to protected portions of the address space. While the processor is in the user privilege state, those instructions which use either the system stack pointer implicity, or address register seven explicitly, access the user stack pointer.

PRIVILEGE STATE CHANGES. Once the processor is in the user state and executing instructions, only exception processing can change the privilege state. During exception processing, the current setting of the S-bit of the status register is saved and the S-bit is asserted, putting the processing in the supervisor state. Therefore, when instruction execution resumes at the address specified to process the exception, the processor is in the supervisor privilege state.

REFERENCE CLASSIFICATION. When the processor makes a reference, it classifies the kind of reference being made, using the encoding on the three function code output lines. This allows external translation of addresses, control of access, and differentiation of special processor states, such as interrupt acknowledge. Table 19 lists the classification of references.

REFERENCE CLASSIFICATION
Table 19

Function Code Output			
FC2	FC1	FC0	Reference Class
0	0	0	(Unassigned)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Unassigned)
1	0	0	(Unassigned)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

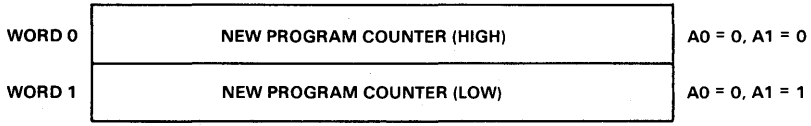
EXCEPTION PROCESSING

Before discussing the details of interrupts, traps, and tracing, a general description of exception processing is in order. The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary copy of the status register is made, and the status register is set for exception processing. In the second step the exception vector is determined, and the third step is the saving of the current processor context. In the fourth step a new context is obtained, and the processor switches to instruction processing.

EXCEPTION VECTORS. Exception vectors are memory locations from which the processor fetches the address of a routine which will handle that exception. All exception vectors are two words in length (Figure 25), except for the reset vector, which is four words. All exception vectors lie in the supervisor data space, except for the reset vector which is in the supervisor program space. A vector number is an eight-bit number which, when multiplied by four, gives the address of an exception vector. Vector numbers are generated internally or externally, depending on the cause of the exception. In the case of interrupts, during the interrupt acknowledge bus cycle, a peripheral provides an 8-bit vector number (Figure 26) to the processor on data bus lines D0 through D7. The processor translates the vector number into a full 24-bit address, as shown in Figure 27. The memory layout for exception vectors is given in Table 20.

As shown in Table 20, the memory layout is 512 words long (1024 bytes). It starts at address 0 and proceeds through address 1023. This provides 255 unique vectors; some of these are reserved for TRAPS and other system functions. Of the 255, these are 192 reserved for user interrupt vectors. However, there is no protection on the first 64 entries, so user interrupt vectors may overlap at the discretion of the systems designer.

EXCEPTION VECTOR FORMAT
Figure 25



EXCEPTION VECTOR ASSIGNMENT

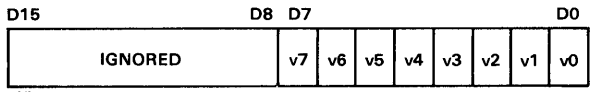
Table 20

Vector Number(s)	Address			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset Initial SSP
—	4	004	SP	Reset Initial PC
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Divide
6	24	018	SD	CHK Instruction
7	28	01C	SD	TRAPV Instruction
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12*	48	030	SD	(Unassigned, reserved)
13*	52	034	SD	(Unassigned, reserved)
14*	56	038	SD	(Unassigned, reserved)
15	60	03C	SD	Uninitialized Interrupt Vector
16-23*	64	040	SD	(Unassigned, reserved)
	92	05C		—
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32-47	128	080	SD	TRAP Instruction Vectors
	188	0BC		—
48-63*	192	0C0	SD	(Unassigned, reserved)
	252	0FC		—
64-255	256	100	SD	User Interrupt Vectors
	1020	3FC		—

*Vector numbers 12, 13, 14, 16 through 23 and 48 through 63 are reserved for future enhancements by Mostek. No user peripheral devices should be assigned these numbers.

PERIPHERAL VECTOR NUMBER FORMAT

Figure 26

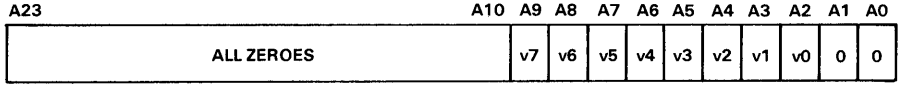


Where:

v7 is the MSB of the Vector Number
v0 is the LSB of the Vector Number

ADDRESS TRANSLATED FROM 8-BIT VECTOR NUMBER

Figure 27



KINDS OF EXCEPTIONS. Exceptions can be generated by either internal or external causes. The externally generated exceptions are the interrupts and the bus error and reset requests. The interrupts are requests from peripheral devices for processor action while the bus error and reset inputs are used for access control and processor restart. The internally generated exceptions come from instructions, or from address errors or tracing. The trap (TRAP), trap on overflow (TRAPV), check register against bounds (CHK) and divide (DIV) instructions all can generate exceptions as part of their instruction execution. In addition, illegal instructions, word fetches from odd addresses and privilege violations cause exceptions. Tracing behaves like a very high priority, internally generated interrupt after each instruction execution.

EXCEPTION PROCESSING SEQUENCE. Exception processing occurs in four identifiable steps. In the first step, an internal copy is made of the status register. After the copy is made, the S-bit is asserted, putting the processor into the supervisor privilege state. Also, the T-bit is negated which will allow the exception handler to execute unhindered by tracing. For the reset and interrupt exceptions, the interrupt priority mask is also updated.

In the second step, the vector number of the exception is determined. For interrupts, the vector number is obtained by a processor fetch, classified as an interrupt acknowledge. For all other exceptions, internal logic provides the vector number. This vector number is then used to generate the address of the exception vector.

The third step is to save the current processor status, except for the reset exception. The current program counter value and the saved copy of the status register are stacked using the supervisor stack pointer. The program counter value stacked usually points to the next unexecuted instruction, however for bus error and address error, the value stacked for the program counter is unpredictable, and may be incremented from the address of the instruction which caused the error. Additional information defining the current context is stacked for the bus error and address error exceptions.

The last step is the same for all exceptions. The new program counter value is fetched from the exception vector. The processor then resumes instruction execution. The instruction at the address given in the exception vector is fetched, and normal instruction decoding and execution is started.

MULTIPLE EXCEPTIONS. These paragraphs describe the processing which occurs when multiple exceptions arise simultaneously. Exceptions can be grouped according to their occurrence and priority. The Group 0 exceptions are reset, bus error, and address error. These exceptions cause the instruction currently being executed to be aborted, and the exception processing to commence at the next minor cycle of the processor. The Group 1 exceptions are trace and interrupt, as well as the privilege violations and illegal instructions. These exceptions allow the current instruction to execute to completion, but preempt the execution of the next instruction by forcing exception processing to occur (privilege violations and illegal instructions are detected when they are the next instruction to be executed). The Group 2 exceptions occur as part of the normal processing of instructions. The TRAP, TRAPV, CHK, and zero divide exceptions are in this group. For these exceptions, the normal execution of an instruction may lead to exception processing.

Group 0 exceptions have highest priority, while Group 2 exceptions have lowest priority. Within Group 0, reset has highest priority, followed by bus error and then address error. Within Group 1, trace has priority over external interrupts, which in turn takes priority over illegal instruction and privilege violation. Since only one instruction can be executed at a time, there is no priority relation within Group 2.

The priority relation between two exceptions determines which is taken, or taken first, if the conditions for both arise simultaneously. Therefore, if a bus error occurs during a TRAP instruction, the bus error takes precedence, and the TRAP instruction processing is aborted. In another example, if an interrupt request occurs during the execution of an instruction while the T-bit is asserted, the trace exception has priority, and is processed first. Before instruction

EXCEPTION GROUPING AND PRIORITY

Table 21

Group	Exception	Processing
0	Reset Bus Error Address Error	Exception processing begins within two clock cycles
1	Trace Interrupt Illegal Privilege	Exception processing begins before the next instruction
2	TRAP, TRAPV, CHK, Zero Divide	Exception processing is started by normal instruction execution

processing resumes, however, the interrupt exception is also processed, and instruction processing commences finally in the interrupt handler routine. A summary of exception grouping and priority is given in Table 21.

EXCEPTION PROCESSING DETAILED DISCUSSION

Exceptions have a number of sources, and each exception has processing which is peculiar to it. The following paragraphs detail the sources of exceptions, how each arises, and how each is processed.

RESET. The reset input provides the highest exception level. The processing of the reset signal is designed for system initiation, and recovery from catastrophic failure. Any processing in progress at the time of the reset is aborted and cannot be recovered. The processor is forced into the supervisor state, and the trace state is forced off. The processor interrupt priority mask is set at level seven. The vector number is internally generated to reference the reset exception vector at location 0 in the supervisor program space. Because no assumptions can be made about the validity of register contents, in particular the supervisor stack pointer, neither the program counter nor the status register is saved. The address contained in the first two words of the reset exception vector is fetched as the initial supervisor stack pointer, and the address in the last two words of the reset exception vector is fetched as the initial program counter. Finally, instruction execution is started at the address in the program counter. The power-up/restart code should be pointed to by the initial program counter.

The RESET instruction does not cause loading of the reset vector, but does assert the reset line to reset external devices. This allows the software to reset the system to a known state and then continue processing with the next instruction.

INTERRUPTS. Seven levels of interrupt priorities are provided. Devices may be chained externally within interrupt priority levels, allowing an unlimited number of peripheral devices to interrupt the processor. Interrupt priority levels are numbered from one to seven, level seven being the highest priorty. The status register contains a three-bit mask which indicates the current processor priority, and interrupts are inhibited for all priority levels less than or equal to the current processor priority.

An interrupt request is made to the processor by encoding the interrupt request level on the interrupt request lines; a zero indicates no interrupt request. Interrupt requests arriving at the processor do not force immediate exception processing, but are made pending. Pending interrupts are detected between instruction executions. If the priority of the pending interrupt is lower than or equal to the current processor priority, execution continues with the next instruction and the interrupt exception processing is postponed. (The recognition of level seven is slightly different, as explained in a following paragraph.)

If the priority of the pending interrupt is greater than the current processor priority, the exception processing sequence is started. First a copy of the status register is saved, and the privilege state is set to supervisor, tracing is suppressed, and the processor priority level is set to the level of the interrupt being acknowledged. The processor fetches the vector number from the interrupting device, classifying the reference as an interrupt acknowledge and displaying the level number of the interrupt being acknowledged on the address bus. If external logic requests an automatic vectoring, the processor internally generates a vector number which is determined by the interrupt level number. If external logic indicates a bus error, the interrupt is taken to be spurious, and the generated vector number references the spurious interrupt vector. The processor then proceeds with the usual exception processing, saving the program counter and status register on the supervisor stack. The saved value of the program counter is the address of the instruction which would have been executed had the interrupt not been present. The content of the interrupt vector whose vector number was previously obtained is fetched and loaded into the program counter, and normal instruction execution commences in the interrupt handling routine. A flow chart for the interrupt acknowledge sequence is given in Figure 28; a timing diagram is given in Figure 29, and the interrupt processing sequence is shown in Figure 30.

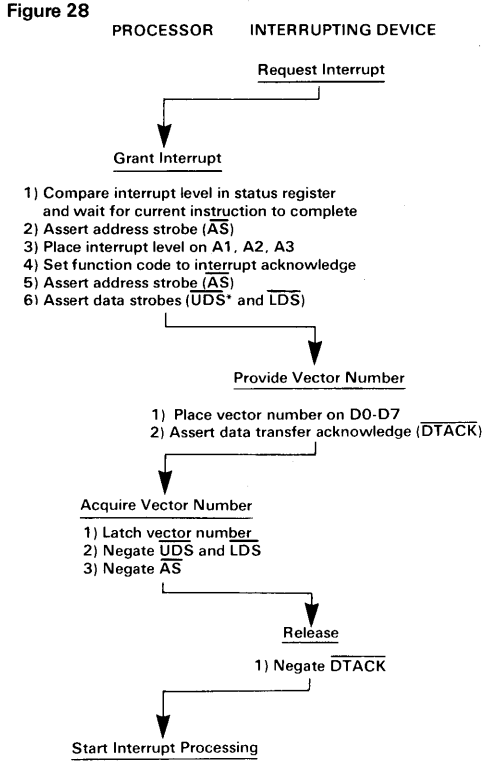
Priority level seven is a special case. Level seven interrupts cannot be inhibited by the interrupt priority mask, thus providing a "non-maskable interrupt" capability. An interrupt is generated each time the interrupt request level changes from some lower level to level seven. Note that a level seven interrupt may still be caused by the level comparison if the request level is a seven and the processor priority is set to a lower level by an instruction.

UNINITIALIZED INTERRUPT. An interrupting device asserts $\overline{\text{VPA}}$ or provides an interrupt vector during an interrupt acknowledge cycle to the MK68000. If the vector register has not been initialized, the responding MK68000 Family peripheral will provide vector 15, the uninitialized

VI

INTERRUPT ACKNOWLEDGE SEQUENCE FLOW CHART

Figure 28



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

interrupt vector. This provides a uniform way to recover from a programming error.

SPURIOUS INTERRUPT. If during the interrupt acknowledge cycle no device responds by asserting DTACK or VPA, the bus error line should be asserted to terminate the vector acquisition. The processor separates the processing of this error from bus error by fetching the spurious interrupt vector instead of the bus error vector. The processor then proceeds with the usual exception processing.

INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise either from processor recognition of abnormal conditions during instruction execution, or from use of instructions whose normal behavior is trapping.

Some instructions are used specifically to generate traps. The TRAP instruction always forces an exception, and is useful for implementing system calls for user programs. The TRAPV and CHK instructions force an exception if the user program detects a runtime error, which may be an arithmetic overflow or a subscript out of bounds.

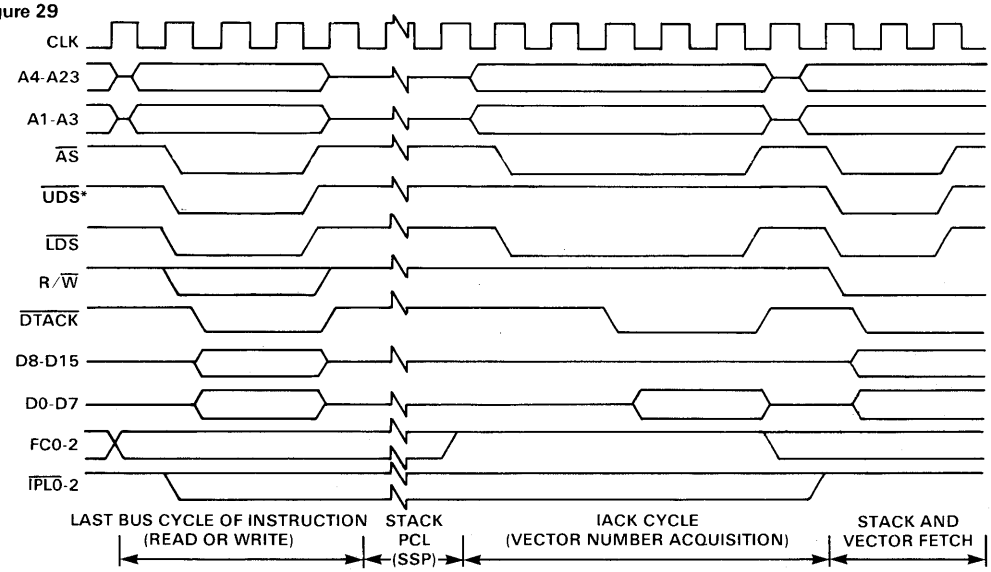
The signed divide (DIVS) and unsigned divide (DIVU) instructions will force an exception if a division operation is attempted with a divisor of zero.

ILLEGAL AND UNIMPLEMENTED INSTRUCTIONS. Illegal instruction is the term used to refer to any of the word bit patterns which are not the bit pattern of the first word of a legal instruction. During instruction execution, if such an instruction is fetched, an illegal instruction exception occurs.

Word patterns with bits 15 through 12 equaling 1010 or 1111 are distinguished as unimplemented instructions and

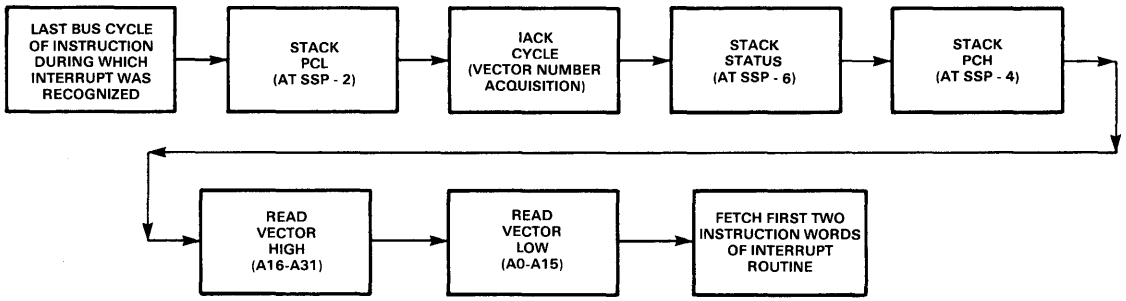
INTERRUPT ACKNOWLEDGE SEQUENCE TIMING DIAGRAM

Figure 29



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

INTERRUPT PROCESSING SEQUENCE
Figure 30



NOTE:
SSP refers to the value of the supervisor stack pointer before the interrupt occurs.

separate exception vectors are given to these patterns to permit efficient emulation. This facility allows the operating system to detect program errors, or to emulate unimplemented instructions in software.

PRIVILEGE VIOLATIONS. In order to provide system security, various instructions are privileged. An attempt to execute one of the privileged instructions while in the user state will cause an exception. The privileged instructions are:

STOP	AND (word) Immediate to SR
RESET	EOR (word) Immediate to SR
RTE	OR (word) Immediate to SR
MOVE to SR	MOVE USP

TRACING. To aid in program development, the MK68000 includes a facility to allow instruction by instruction tracing. In the trace state, after each instruction is executed an exception is forced, allowing a debugging program to monitor the execution of the program under test.

The trace facility uses the T-bit in the supervisor portion of the status register. If the T-bit is negated (off), tracing is disabled, and instruction execution proceeds from instruction to instruction as normal. If the T-bit is asserted (on) at the beginning of the execution of an instruction, a trace exception will be generated after the execution of that instruction is completed. If the instruction is not executed, either because an interrupt is taken, or the instruction is illegal or privileged, the trace exception does not occur. The trace exception also does not occur if the instruction is aborted by a reset, bus error, or address error exception. If the instruction is indeed executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception. If, during the execution of the instruction, an exception is forced by that instruction, the forced exception is processed before the trace exception.

As an extreme illustration of the above rules, consider the arrival of an interrupt during the execution of a TRAP instruction while tracing is enabled. First the trap exception is processed, then the trace exception, and finally the interrupt exception. Instruction execution resumes in the interrupt handler routine.

BUS ERROR. Bus error exceptions occur when the external logic requests that a bus error be processed by an exception. The current bus cycle which the processor is making is then aborted. Whether the processor was doing instruction or exception processing, that processing is terminated, and the processor immediately begins exception processing.

Exception processing for bus error follows the usual sequence of steps. The status register is copied, the supervisor state is entered, and the trace state is turned off. The vector number is generated to refer to the bus error vector. Since the processor was not between instructions when the bus error exception request was made, the context of the processor is more detailed. To save more of this context, additional information is saved on the supervisor stack. The program counter and the copy of the status register are of course saved. The value saved for the program counter is advanced by some amount, two to ten bytes beyond the address of the first word of the instruction which made the reference causing the bus error. If the bus error occurred during the fetch of the next instruction, the saved program counter has a value in the vicinity of the current instruction, even if the current instruction is a branch, a jump, or a return instruction. Besides the usual information, the processor saves its internal copy of the first word of the instruction being processed and the address which was being accessed by the aborted bus cycle. Specific information about the access is also saved whether it was a read or a write, whether the processor was processing an instruction or not, and the classification

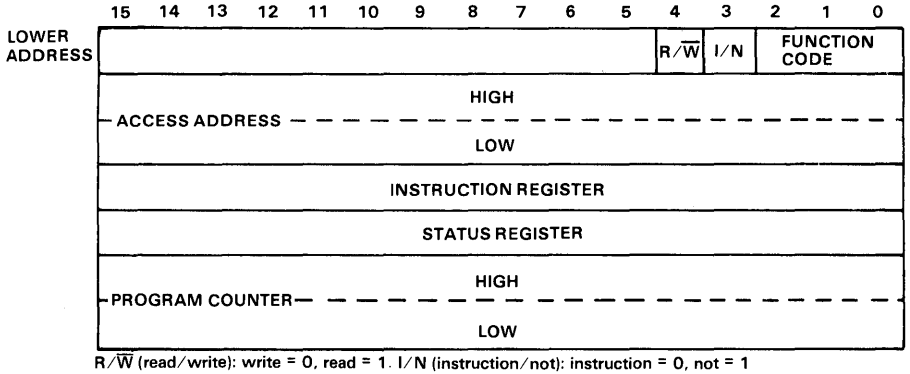
displayed on the function code outputs when the bus error occurred. The processor is processing an instruction if it is in the normal state or processing a Group 2 exception; the processor is not processing an instruction if it is processing a Group 0 or a Group 1 exception. Figure 31 illustrates how this information is organized on the supervisor stack. Although this information is not sufficient in general to effect full recovery from the bus error, it does allow software diagnosis. Finally, the processor commences instruction processing at the address contained in the vector. It is the responsibility of the error handler routine to clean up the stack and determine where to continue execution.

If a bus error occurs during the exception processing for a bus error, address error, or reset, the processor is halted, and all processing ceases. This simplifies the detection of catastrophic system failure, since the processor removes itself from the system rather than destroy all memory contents. Only the $\overline{\text{RESET}}$ pin can restart a halted processor.

ADDRESS ERROR. Address error exceptions occur when the processor attempts to access a word or a long word operand or an instruction at an odd address. The effect is much like an internally generated bus error, so that the bus cycle is aborted, and the processor ceases whatever processing it is currently doing and begins exception processing. After exception processing commences, the sequence is the same as that for bus error including the information that is stacked, except that the vector number refers to the address error vector instead. Likewise, if an address error occurs during the exception processing for a bus error, address error, or reset, the processor is halted. As shown in Figure 32, an address error will execute a short bus cycle followed by exception processing.

SUPERVISOR STACK ORDER

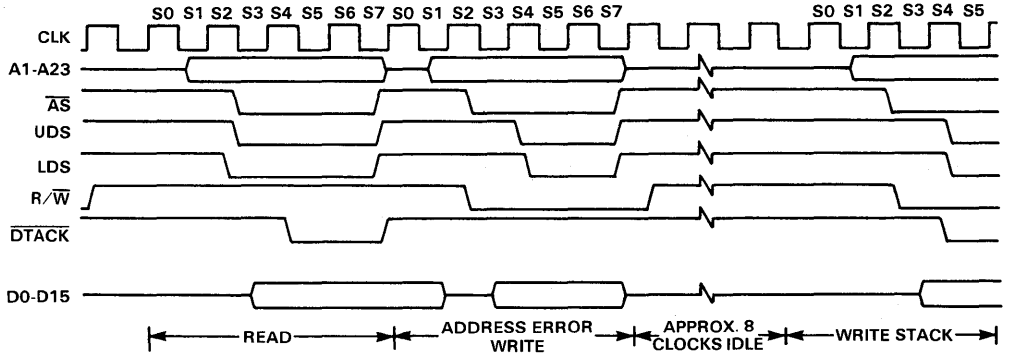
Figure 31



R/$\overline{\text{W}}$ (read/write): write = 0, read = 1. I/N (instruction/not): instruction = 0, not = 1

ADDRESS ERROR TIMING

Figure 32



INTERFACE WITH 6800 PERIPHERALS

To interface the synchronous 6800 peripherals with the asynchronous MK68000, the processor modifies its bus cycle to meet the 6800 cycle requirements whenever a 6800 device address is detected. This is possible since both processors use memory mapped I/O. Figure 33 is a flow chart of the interface operation between the processor and 6800 devices.

DATA TRANSFER OPERATION

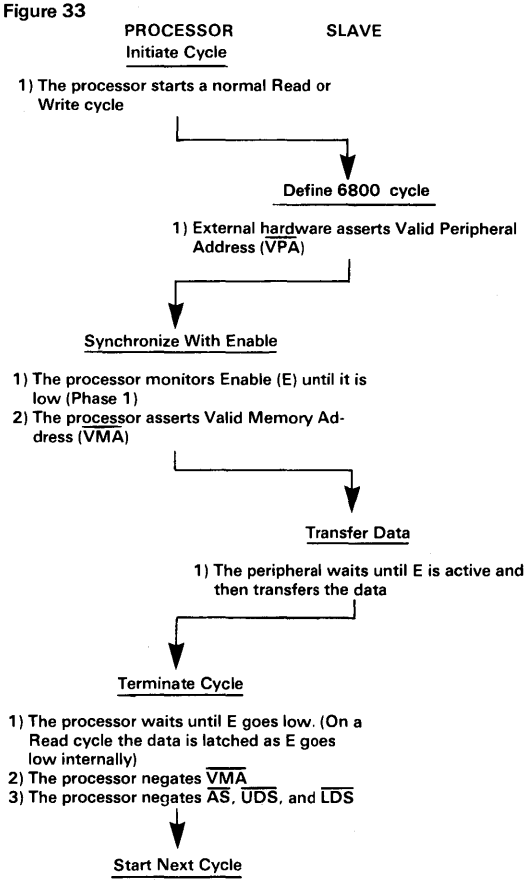
Three signals on the processor provide the 6800 interface. They are: enable (E), valid memory address ($\overline{VMA}$), and valid peripheral address ($\overline{VPA}$). Enable corresponds to the E or $\Phi 2$ signal in existing 6800 systems. It is the bus clock used by the frequency clock that is one tenth of the incoming MK68000 clock frequency. The timing of E allows 1 MHz peripherals to be used with an 8 MHz MK68000. Enable has a 60/40 duty cycle; that is, it is low for six input clocks and high for four input clocks. This duty cycle allows the processor to do successive $\overline{VPA}$ accesses on successive E pulses.

6800 cycle timing is given in Figure 34. At state zero (S0) in the cycle, the address bus and function codes are in the high-impedance state. One half clock later, in state 1, the address bus and function code outputs are released from the high-impedance state.

During state 2, the address strobe ($\overline{AS}$) is asserted to indicate that there is a valid address on the address bus. If the bus cycle is a read cycle, the upper and/or lower data strobes are also asserted in state 2. If the bus cycle is a write cycle, the read/write (R/$\overline{W}$) signal is switched to low (write) during state 2. One half clock later, in state 3, the write data

6800 INTERFACING FLOW CHART

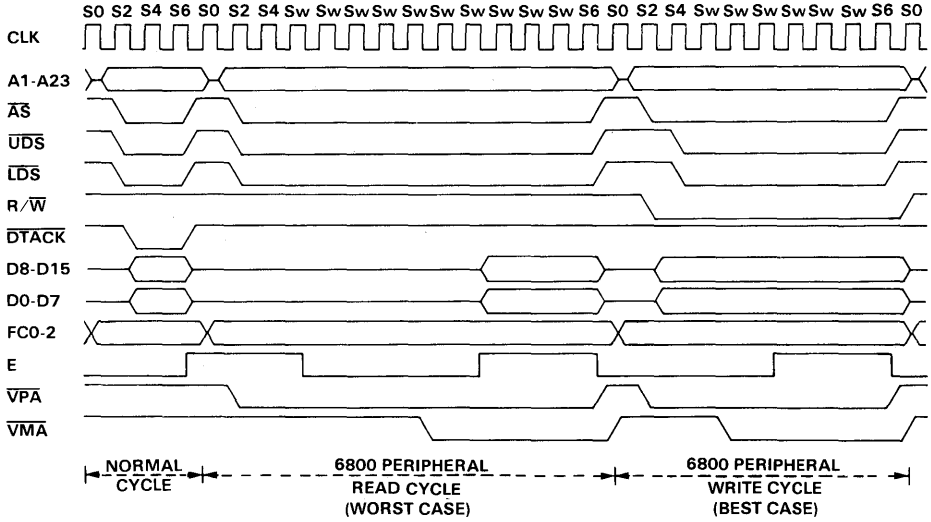
Figure 33



VI

6800 CYCLE OPERATION

Figure 34



is placed on the data bus, and in state 4 the data strobes are issued to indicate valid data on the data bus.

The processor now inserts wait states until it recognizes the assertion of $\overline{VPA}$. The $\overline{VPA}$ input signals the processor that the address on the bus is the address of a 6800 device (or an area reserved for 6800 devices) and that the bus should conform to the Φ2 transfer characteristics of the 6800 bus. Valid peripheral address is derived by decoding the address bus, conditioned by address strobe.

After the recognition of $\overline{VPA}$, the processor assures that the Enable (E) is low, by waiting if necessary, and subsequently asserts $\overline{VMA}$. Valid memory address is then used as part of the chip select equation of the peripheral. This ensures that the 6800 peripherals are selected and deselected at the correct time. The peripheral now runs its cycle during the high portion of the E signal.

During a read cycle, the processor latches the peripheral data in state 6. For all cycles, the processor negates the address and data strobes one half clock cycle later in state 7 and the Enable signal goes low at this time. Another half clock later, the address bus is put in the high-impedance state. During a write cycle, the data bus is put in the high-impedance state and the read/write signal is switched high at this time. The peripheral logic must remove $\overline{VPA}$ within one clock after address strobe is negated. $\overline{DTACK}$ should not be asserted while $\overline{VPA}$ is asserted.

Notice that the MK68000 VMA is active low, contrasted with the active high 6800 VMA. This allows the processor to put its buses in the high-impedance state on DMA requests without inadvertently selecting peripherals.

INTERRUPT INTERFACE OPERATION

During an interrupt acknowledge cycle while the processor is fetching the vector, if $\overline{VPA}$ is asserted, the MK68000 will assert $\overline{VMA}$ and complete a normal 6800 read cycle as shown in Figure 35. The processor will then use an internally generated vector that is a function of the interrupt being serviced. This process is known as autovectoring. The seven autovectors are vector numbers 25 through 31 (decimal).

This operates in the same fashion (but is not restricted to) the 6800 interrupt sequence. The basic difference is that there are six normal interrupt vectors and one NMI type vector. As with both the 6800 and the MK68000's normal vectored interrupt, the interrupt service routine can be located anywhere in the address space. This is due to the fact that while the vector numbers are fixed, the contents of the vector table entries are assigned by the user.

Since $\overline{VMA}$ is asserted during autovectoring, the 6800 peripheral address decoding should prevent unintended accesses.

INSTRUCTION SET

The following paragraphs provide information about the addressing categories and instruction set of the MK68000.

ADDRESSING CATEGORIES

Effective address modes may be categorized by the ways in which they may be used. The following classifications will be used in the instruction definitions.

Data	If an effective address mode may be used to refer to data operands, it is considered a data addressing effective address mode.
Memory	If an effective address mode may be used to refer to memory operands, it is considered a memory addressing effective address mode.
Alterable	If an effective address mode may be used to refer to alterable (writeable) operands, it is considered an alterable addressing effective address mode.
Control	If an effective address mode may be used to refer to memory operands without an associated size, it is considered a control addressing effective address mode.

Table 22 shows the various categories to which each of the effective address modes belong. Table 23 is the instruction set summary.

The status register addressing mode is not permitted unless it is explicitly mentioned as a legal addressing mode.

These categories may be combined, so that additional, more restrictive, classifications may be defined. For example, the instruction descriptions use such classifications as alterable memory or data alterable. The former refers to those addressing modes which are both alterable and memory addresses, and the latter refers to addressing modes which are both data and alterable.

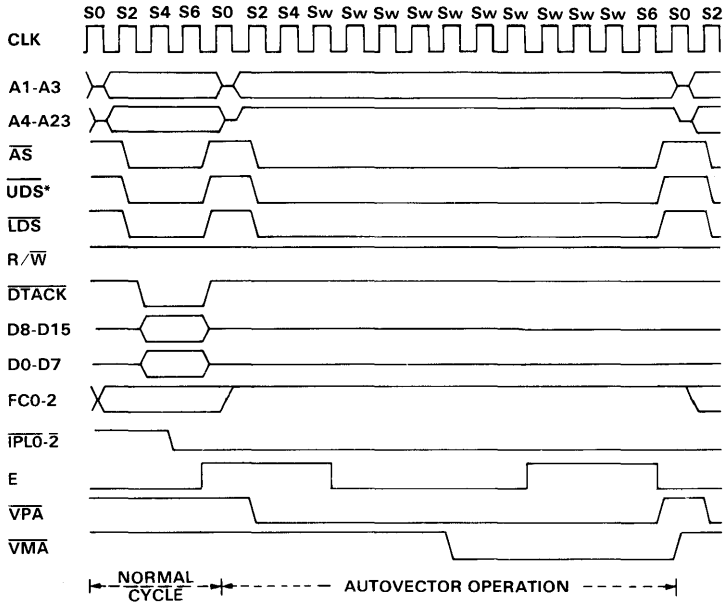
INSTRUCTION PRE-FETCH

The MK68000 uses a 2-word tightly-coupled instruction prefetch mechanism to enhance performance. This mechanism is described in terms of the microcode operations involved. If the execution of an instruction is defined to begin when the microroutine for that instruction is entered, some features of the prefetch mechanism can be described.

1) When execution of an instruction begins, the operation word and the word following have already been

AUTOVECTOR OPERATION TIMING DIAGRAM

Figure 35



*Although a vector number is one byte, both data strobes are asserted due to the microcode used for exception processing. The processor does not recognize anything on data lines D8 through D15 at this time.

VI

EFFECTIVE ADDRESSING MODE CATEGORIES

Table 22

Effective Address Modes	Mode	Register	Data	Addressing Categories		
				Memory	Control	Alterable
Dn	000	register number	X	–	–	X
An	001	register number	–	–	–	X
(An)	010	register number	X	X	X	X
(An)+	011	register number	X	X	–	X
-(An)	100	register number	X	X	–	X
d(An)	101	register number	X	X	X	X
d(An,ix)	110	register number	X	X	X	X
xxx.W	111	000	X	X	X	X
xxx.L	111	001	X	X	X	X
d(PC)	111	010	X	X	X	–
d(PC,ix)	111	011	X	X	X	–
#xxx	111	100	X	X	–	–

INSTRUCTION SET

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ABCD	Add Decimal with Extend	$(Destination)_{10}+(Source)_{10} \rightarrow Destination$	*	U	*	U	*
ADD	Add Binary	(Destination)+(Source) → Destination	*	*	*	*	*

* affected 0 cleared U undefined – unaffected 1 set [ ] = bit number d = displacement

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ADDA	Add Address	(Destination)+(Source) → Destination	–	–	–	–	–
ADDI	Add Immediate	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDQ	Add Quick	(Destination)+Immediate Data → Destination	*	*	*	*	*
ADDX	Add Extended	(Destination)+(Source)+ X → Destination	*	*	*	*	*
AND	AND Logical	(Destination) Λ (Source) → Destination	–	*	*	0	0
ANDI	AND Immediate	(Destination) Λ Immediate Data → Destination	–	*	*	0	0
ANDI to CCR	AND Immediate to Condition Codes	(Source) Λ CCR → CCR	*	*	*	*	*
ANDI to SR	AND Immediate to Status Register	(Source) Λ SR → SR	*	*	*	*	*
ASL, ASR	Arithmetic Shift	(Destination) Shifted by <count> → Destination	*	*	*	*	*
B_{CC}	Branch Conditionally	If $_{CC}$ then PC+d → PC	–	–	–	–	–
BCHG	Test a Bit and Change	~(<bit number>) OF Destination → Z ~(<bit number>) OF Destination → <bit number> OF Destination	–	–	*	–	–
BCLR	Test a Bit and Clear	~(<bit number>) OF Destination → Z 0 → <bit number> → OF Destination	–	–	*	–	–
BRA	Branch Always	PC + d → PC	–	–	–	–	–
BSET	Test a Bit and Set	~(<bit number>) OF Destination → Z 1 → <bit number> OF Destination	–	–	*	–	–
BSR	Branch to Subroutine	PC → –(SP), PC+d → PC	–	–	–	–	–
BTST	Test a Bit	~(<bit number>) OF Destination → Z	–	–	*	–	–
CHK	Check Register against Bounds	If Dn <0 or Dn> (<ea>) then TRAP	–	*	U	U	U
CLR	Clear an Operand	0 → Destination	–	0	1	0	0
CMP	Compare	(Destination) – (Source)	–	*	*	*	*
CMPA	Compare Address	(Destination) – (Source)	–	*	*	*	*
CMPI	Compare Immediate	(Destination) – Immediate Data	–	*	*	*	*
CMPM	Compare Memory	(Destination) – (Source)	–	*	*	*	*
DB_{CC}	Test Condition, Decrement and Branch	If ~ $_{CC}$ then Dn – 1 → Dn; if Dn ≠ – 1 then PC + d → PC	–	–	–	–	–
DIVS	Signed Divide	(Destination)/(Source) → Destination	–	*	*	*	0
DIVU	Unsigned Divide	(Destination)/(Source) → Destination	–	*	*	*	0
EOR	Exclusive OR Logical	(Destination) ⊕ (Source) → Destination	–	*	*	0	0

* affected 0 cleared U undefined – unaffected 1 set [ ] = bit number d = displacement

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
EORI	Exclusive OR Immediate	(Destination) ⊕ Immediate Data → Destination	–	*	*	0	0
EORI to CCR	Exclusive OR Immediate to Condition Codes	(Source) ⊕ CCR → CCR	*	*	*	*	*
EORI to SR	Exclusive OR Immediate to Status Register	(Source) ⊕ SR → SR	*	*	*	*	*
EXG	Exchange Register	Rx ⟷ Ry	–	–	–	–	–
EXT	Sign Extend	(Destination) Sign-extended → Destination	–	*	*	0	0
JMP	Jump	Destination → PC	–	–	–	–	–
JSR	Jump to Subroutine	PC → –(SP); Destination → PC	–	–	–	–	–
LEA	Load Effective Address	Destination → An	–	–	–	–	–
LINK	Link and Allocate	An → –(SP); SP → An; SP + d → SP	–	–	–	–	–
LSL, LSR	Logical Shift	(Destination) Shifted by <count> → Destination	*	*	*	0	*
MOVE	Move Data from Source to Destination	(Source) → Destination	–	*	*	0	0
MOVE to CCR	Move to Condition Code	(Source) → CCR	*	*	*	*	*
MOVE to SR	Move to the Status Register	(Source) → SR	*	*	*	*	*
MOVE from SR	Move from the Status Register	SR → Destination	–	–	–	–	–
MOVE USP	Move User Stack Pointer	USP → An, An → USP	–	–	–	–	–
MOVEA	Move Address	(Source) → Destination	–	–	–	–	–
MOVEM	Move Multiple Registers	Registers → Destination (Source) → Registers	–	–	–	–	–
MOVEP	Move Peripheral Data	(Source) → Destination	–	–	–	–	–
MOVEQ	Move Quick	Immediate Data → Destination	–	*	*	0	0
MULS	Signed Multiply	(Destination)* (Source) → Destination	–	*	*	0	0
MULU	Unsigned Multiply	(Destination)* (Source) → Destination	–	*	*	0	0
NBCD	Negate Decimal with Extend	$0 - (\text{Destination})_{10} - X \rightarrow$ Destination	*	U	*	U	*
NEG	Negate	0 – (Destination) → Destination	*	*	*	*	*
NEGX	Negate with Extend	0 – (Destination) – X → Destination	*	*	*	*	*
NOP	No Operation	–	–	–	–	–	–
NOT	Logical Complement	~ (Destination) → Destination	–	*	*	0	0
OR	Inclusive OR Logical	(Destination) v (Source) → Destination	–	*	*	0	0

* affected 0 cleared U undefined – unaffected 1 set [ ] = bit number d = displacement

INSTRUCTION SET (CONTINUED)

Table 23

Mnemonic	Description	Operation	Condition Codes				
			X	N	Z	V	C
ORI	Inclusive OR Immediate	(Destination) v Immediate Data → Destination	–	*	*	0	0
ORI to CCR	Inclusive OR Immediate to Condition Codes	(Source) V CCR → CCR	*	*	*	*	*
ORI to SR	Inclusive OR Immediate to Status Register	(Source) V SR → SR	*	*	*	*	*
PEA	Push Effective Address	Destination → –(SP)	–	–	–	–	–
RESET	Reset External Devices	–	–	–	–	–	–
ROL, ROR	Rotate (Without Extend)	(Destination) Rotated by <count> → Destination	–	*	*	0	*
ROXL, ROXR	Rotate with Extend	(Destination) Rotated by <count> → Destination	*	*	*	0	*
RTE	Return from Exception	(SP)+ → SR, (SP)+ → PC	*	*	*	*	*
RTR	Return and Restore Condition Codes	(SP)+ → CC; (SP)+ → PC	*	*	*	*	*
RTS	Return from Subroutine	(SP)+ → PC	–	–	–	–	–
SBCD	Subtract Decimal with Extend	$(Destination)_{10} - (Source)_{10} - X \rightarrow Destination$	*	U	*	U	*
S_{CC}	Set According to Condition	If $_{CC}$ then 1's→ Destination else 0's→ Destination	–	–	–	–	–
STOP	Load Status Register and Stop	Immediate Data → SR; STOP	*	*	*	*	*
SUB	Subtract Binary	(Destination) – (Source) → Destination	*	*	*	*	*
SUBA	Subtract Address	(Destination) – (Source) → Destination	–	–	–	–	–
SUBI	Subtract Immediate	(Destination) – Immediate Data → Destination	*	*	*	*	*
SUBQ	Subtract Quick	(Destination) – Immediate Data → Destination	*	*	*	*	*
SUBX	Subtract with Extend	(Destination) – (Source) – X → Destination	*	*	*	*	*
SWAP	Swap Register Halves	Register [31:16] ←→ Register [15:0]	–	*	*	0	0
TAS	Test and Set an Operand	(Destination) Tested → CC; 1 → [7] OF Destination	–	*	*	0	0
TRAP	Trap	PC → –(SSP); SR → –(SSP) –; (Vector) → PC	–	–	–	–	–
TRAPV	Trap on Overflow	If V then TRAP	–	–	–	–	–
TST	Test an Operand	(Destination) Tested → CC	–	*	*	0	0
UNLK	Unlink	An → SP; (SP)+ → An	–	–	–	–	–

* affected 0 cleared U undefined – unaffected 1 set [ ] = bit number d = displacement

fetched. The operation word is in the instruction decoder.

2) In the case of multi-word instructions, as each additional word of the instruction is used internally, a fetch is made to the instruction stream to replace it.
3) The last fetch from the instruction stream is made when the operation word is discarded and decoding is started on the next instruction.
4) If the instruction is a single-word instruction causing a branch, the second word is not used. But because this word is fetched by the preceding instruction, it is impossible to avoid this superfluous fetch. In the case of

an interrupt or trace exception, both words are not used.

5) The program counter usually points to the last word fetched from the instruction stream.

INSTRUCTION EXECUTION TIMES

The following paragraphs contain listings of the instruction execution times in terms of external clock (CLK) periods. In this timing data, it is assumed that the memory cycle time is 4 clock periods. Any wait states caused by a longer memory cycle must be added to the total instruction time. The number of bus read and write cycles for each instruction is also included with the timing data. This data is enclosed in parenthesis following the execution periods and is shown as: (r/w) where r is the number of read cycles and w is the number of write cycles.

NOTE

The number of periods includes instruction fetch and all applicable operand fetches and stores.

EFFECTIVE ADDRESS CALCULATION TIMING

Table 24

	Addressing Mode	Byte, Word	Long
	Register		
Dn	Data Register Direct	0(0/0)	0(0/0)
An	Address Register Direct	0(0/0)	0(0/0)
	Memory		
(An)	Address Register Indirect	4(1/0)	8(2/0)
(An)+	Address Register Indirect with Postincrement	4(1/0)	8(2/0)
-(An)	Address Register Indirect with Predecrement	6(1/0)	10(2/0)
d(An)	Address Register Indirect with Displacement	8(2/0)	12(3/0)
d(An,ix)*	Address Register Indirect with Index	10(2/0)	14(3/0)
xxx.W	Absolute Short	8(2/0)	12(3/0)
xxx.L	Absolute Long	12(3/0)	16(4/0)
d(PC)	Program Counter with Displacement	8(2/0)	12(3/0)
d(PC,ix)*	Program Counter with Index	10(2/0)	14(3/0)
#xxx	Immediate	4(1/0)	8(2/0)

*The size of the index register (ix) does not affect execution time.

MOVE BYTE AND WORD INSTRUCTION CLOCK PERIODS

Table 25

Source	Destination								
	Dn	An	(An)	(An)+	-(An)	d(An)	d(An,ix)*	xxx.W	xxx.L
Dn	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
An	4(1/0)	4(1/0)	8(1/1)	8(1/1)	8(1/1)	12(2/1)	14(2/1)	12(2/1)	16(3/1)
(An)	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
(An)+	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)
-(An)	10(2/0)	10(2/0)	14(2/1)	14(2/1)	14(2/1)	18(3/1)	20(3/1)	18(3/1)	22(4/1)
d(An)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(An,ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
xxx.W	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
xxx.L	16(4/0)	16(4/0)	20(4/1)	20(4/1)	20(4/1)	24(5/1)	26(5/1)	24(5/1)	28(6/1)
d(PC)	12(3/0)	12(3/0)	16(3/1)	16(3/1)	16(3/1)	20(4/1)	22(4/1)	20(4/1)	24(5/1)
d(PC,ix)*	14(3/0)	14(3/0)	18(3/1)	18(3/1)	18(3/1)	22(4/1)	24(4/1)	22(4/1)	26(5/1)
#xxx	8(2/0)	8(2/0)	12(2/1)	12(2/1)	12(2/1)	16(3/1)	18(3/1)	16(3/1)	20(4/1)

*The size of the index register (ix) does not affect execution time.

MOVE LONG INSTRUCTION CLOCK PERIODS

Table 26

Source	Destination								
	Dn	**An**	**(An)**	**(An)+**	**-(An)**	**d(An)**	**d(An,ix)***	**xxx.W**	**xxx.L**
Dn	4(1/0)	4(1/0)	12(1/2)	12(1/2)	14(1/2)	16(2/2)	18(2/2)	18(2/2)	20(3/2)
An	4(1/0)	4(1/0)	12(1/2)	12(1/2)	14(1/2)	16(2/2)	18(2/2)	16(2/2)	20(3/2)
(An)	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
(An)+	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)
-(An)	14(3/0)	14(3/0)	22(3/2)	22(3/2)	22(3/2)	26(4/2)	28(4/2)	26(4/2)	30(5/2)
d(An)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
d(An,ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
xxx.W	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(6/2)
xxx.L	20(5/0)	20(5/0)	28(5/2)	28(5/2)	28(5/2)	32(6/2)	34(6/2)	32(6/2)	36(7/2)
d(PC)	16(4/0)	16(4/0)	24(4/2)	24(4/2)	24(4/2)	28(5/2)	30(5/2)	28(5/2)	32(5/2)
d(PC,ix)*	18(4/0)	18(4/0)	26(4/2)	26(4/2)	26(4/2)	30(5/2)	32(5/2)	30(5/2)	34(6/2)
#xxx	12(3/0)	12(3/0)	20(3/2)	20(3/2)	20(3/2)	24(4/2)	26(4/2)	24(4/2)	28(5/2)

*The size of the index register (ix) does not affect execution time.

STANDARD INSTRUCTION CLOCK PERIODS

Table 27

Instruction	Size	op <ea>, An	op <ea>, Dn	op Dn, <M>
ADD	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) +**	6(1/0) +**	12(1/2) +
AND	Byte, Word	-	4(1/0) +	8(1/1)+
	Long	-	6(1/0) +**	12(1/2)+
CMP	Byte, Word	6(1/0)+	4(1/0) +	-
	Long	6(1/0) +	6(1/0) +	-
DIVS	-	-	158(1/0) +*	-
DIVU	-	-	140(1/0) +*	-
EOR	Byte, Word	-	4(1/0)***	8(1/1)+
	Long	-	8(1/0)***	12(1/2) +
MULS	-	-	70(1/0) +*	-
MULU	-	-	70(1/0) +*	-
OR	Byte, Word	-	4(1/0) +	8(1/1) +
	Long	-	6(1/0) +**	12(1/2) +
SUB	Byte, Word	8(1/0) +	4(1/0) +	8(1/1) +
	Long	6(1/0) +**	6(1/0) +**	12(1/2) +

+ add effective address calculation time
* indicates maximum value
** total of 8 clock periods for instruction if the effective address is register direct
*** only available effective address mode is data register direct
DIVS, DIVU - The divide algorithm used by the MK68000 provides less than 10% difference between the best and worst case timings
MULS, MULU - The multiply algorithm requires 38+ 2n clocks, where n is defined as:
MULU: n = the number of ones in the <ea>
MULS: n = concatenate of the <ea> with a zero as the LSB; n is the resultant number of 10 or 01 patterns in the 17-bit source; i.e., worst case happens when the source is $5555

IMMEDIATE INSTRUCTION CLOCK PERIODS

Table 28

Instruction	Size	op #, Dn	op #, M	op #, An
ADDI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
ADDQ	Byte, Word	4(1/0)	8(1/1) +	8(1/0)*
	Long	8(1/0)	12(1/2) +	8(1/0)
ANDI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/1) +	–
CMPI	Byte, Word	8(2/0)	8(2/0) +	8(2/0)**
	Long	14(3/0)	12(3/0) +	14(3/0)
EORI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
MOVEQ	Long	4(1/0)	–	–
ORI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
SUBI	Byte, Word	8(2/0)	12(2/1) +	–
	Long	16(3/0)	20(3/2) +	–
SUBQ	Byte, Word	4(1/0)	8(1/1) +	8(1/0)*
	Long	8(1/0)	12(1/2) +	8(1/0)

+ add effective address calculation time

*word only

** uses CMPA instruction and only supports word or long word immediate values

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 29

Instruction	Size	Register	Memory
CLR	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NBCD	Byte	6(1/0)	8(1/1) +
NEG	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NEGX	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
NOT	Byte, Word	4(1/0)	8(1/1) +
	Long	6(1/0)	12(1/2) +
S_{CC}	Byte, False	4(1/0)	8(1/1) +
	Byte, True	6(1/0)	8(1/1) +
TAS	Byte	4(1/0)	10(1/1) +
TST	Byte, Word	4(1/0)	4(1/0)
	Long	4(1/0)	4(1/0) +

+ add effective address calculation time

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 30

Instruction	Size	Register	Memory
ASR, ASL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–
LSR, LSL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–
ROR, ROL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–
ROXR, ROXL	Byte, Word	6 + 2n(1/0)	8(1/1) +
	Long	8 + 2n(1/0)	–

+ add effective address calculation time
n is the shift or rotate count

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 31

Instruction	Size	Dynamic		Static	
		Register	Memory	Register	Memory
BCHG	Byte	–	8(1/1)+	–	12(2/1)+
	Long	8(1/0)*	–	12(2/0)*	–
BCLR	Byte	–	8(1/1)+	–	12(2/1)+
	Long	10(1/0)*	–	14(2/0)*	–
BSET	Byte	–	8(1/1)+	–	12(2/1)+
	Long	8(1/0)*	–	12(2/0)*	–
BTST	Byte	–	4(1/0)+	–	8(2/0)+
	Long	6(1/0)	–	10(2/0)	–

+ add effective address calculation time
* indicates maximum value

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 32

Instruction	Displacement	Trap or Branch Taken	Trap or Branch Not Taken
B_{CC}	Byte	10(2/0)	8(1/0)
	Word	10(2/0)	12(2/0)
BRA	Byte	10(2/0)	–
	Word	10(2/0)	–
BSR	Byte	18(2/2)	–
	Word	18(2/2)	–
DB_{CC}	CC true	–	12(2/0)
	CC false	10(2/0)	14(3/0)
CHK	–	40(5/3)+ *	8(1/0)+
TRAP	–	34(4/3)	–
TRAPV	–	34(5/3)	4(1/0)

+ add effective address calculation time
* indicates maximum value

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 33

Instr	Size	(An)	(An)+	-(An)	d(An)	d(An,ix)+	xxx.W	xxx.L	d(PC)	d(PC,ix)*
JMP	-	8(2/0)	-	-	10(2/0)	14(3/0)	10(2/0)	12(3/0)	10(2/0)	14(3/0)
JSR	-	16(2/2)	-	-	18(2/2)	22(2/2)	18(2/2)	20(3/2)	18(2/2)	22(2/2)
LEA	-	4(1/0)	-	-	8(2/0)	12(2/0)	8(2/0)	12(3/0)	8(2/0)	12(2/0)
PEA	-	12(1/2)	-	-	16(2/2)	20(2/2)	16(2/2)	20(3/2)	16(2/2)	20(2/2)
MOVEM	Word	12 + 4n (3 + n/0)	12 + 4n (3 + n/0)	- -	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)	16 + 4n (4 + n/0)	20 + 4n (5 + n/0)	16 + 4n (4 + n/0)	18 + 4n (4 + n/0)
M→R	Long	12 + 8n (3 + 2n/0)	12 + 8n (3 + 2n/0)	- -	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)	16 + 8n (4 + 2n/0)	20 + 8n (5 + 2n/0)	16 + 8n (4 + 2n/0)	18 + 8n (4 + 2n/0)
MOVEM	Word	8 + 5n (2/n)	- -	8 + 5n (2/n)	12 + 5n (3/n)	14 + 5n (3/n)	12 + 5n (3/n)	16 + 5n (4/n)	- -	- -
R→M	Long	8 + 10n (2/2n)	- -	8 + 10n (2/2n)	12 + 10n (3/2n)	14 + 10n (3/2n)	12 + 10n (3/2n)	16 + 10n (4/2n)	- -	- -

n is the number of registers to move
* is the size of the index register (ix) does not affect the instruction's execution time

VI

EFFECTIVE ADDRESS OPERAND CALCULATION TIMING

Table 24 lists the number of clock periods required to compute an instruction's effective address. It includes fetching of any extension words, the address computation, and fetching of the memory operand. The number of bus read and write cycles is shown in parenthesis as (r/w). Note there are no write cycles involved in processing the effective address.

MOVE INSTRUCTION CLOCK PERIODS

Tables 25 and 26 indicate the number of clock periods for the move instruction. This data includes instruction fetch, operand reads, and operand writes. The number of bus read and write cycles is shown in parenthesis as: (r/w).

STANDARD INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 27 indicates the time required to perform the operations, store the results, and read the next instruction. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 27, the headings have the following meanings. An = address register operand, Dn = data register operand, ea = an operand specified by an effective address, and M = memory effective address operand.

IMMEDIATE INSTRUCTION CLOCK PERIODS

The number of clock periods shown in Table 28 includes the time to fetch immediate operands, perform the operations, store the results, and read the next operation. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

In Table 28, the headings have the following meanings: # = immediate operand, Dn = data register operand, M = memory operand, and An = address register operand.

SINGLE OPERAND INSTRUCTION CLOCK PERIODS

Table 29 indicates the number of clock periods for the single operand instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 34

Instruction	Size	op Dn, Dn	op M, M
ADDX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
CMPM	Byte, Word	-	12(3/0)
	Long	-	20(5/0)
SUBX	Byte, Word	4(1/0)	18(3/1)
	Long	8(1/0)	30(5/2)
ABCD	Byte	6(1/0)	18(3/1)
SBCD	Byte	6(1/0)	18(3/1)

be added to those of the effective address calculation where indicated.

SHIFT/ROTATE INSTRUCTION CLOCK PERIODS

Table 30 indicates the number of clock periods for the shift and rotate instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

BIT MANIPULATION INSTRUCTION CLOCK PERIODS

Table 31 indicates the number of clock periods required for the bit manipulation instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 35

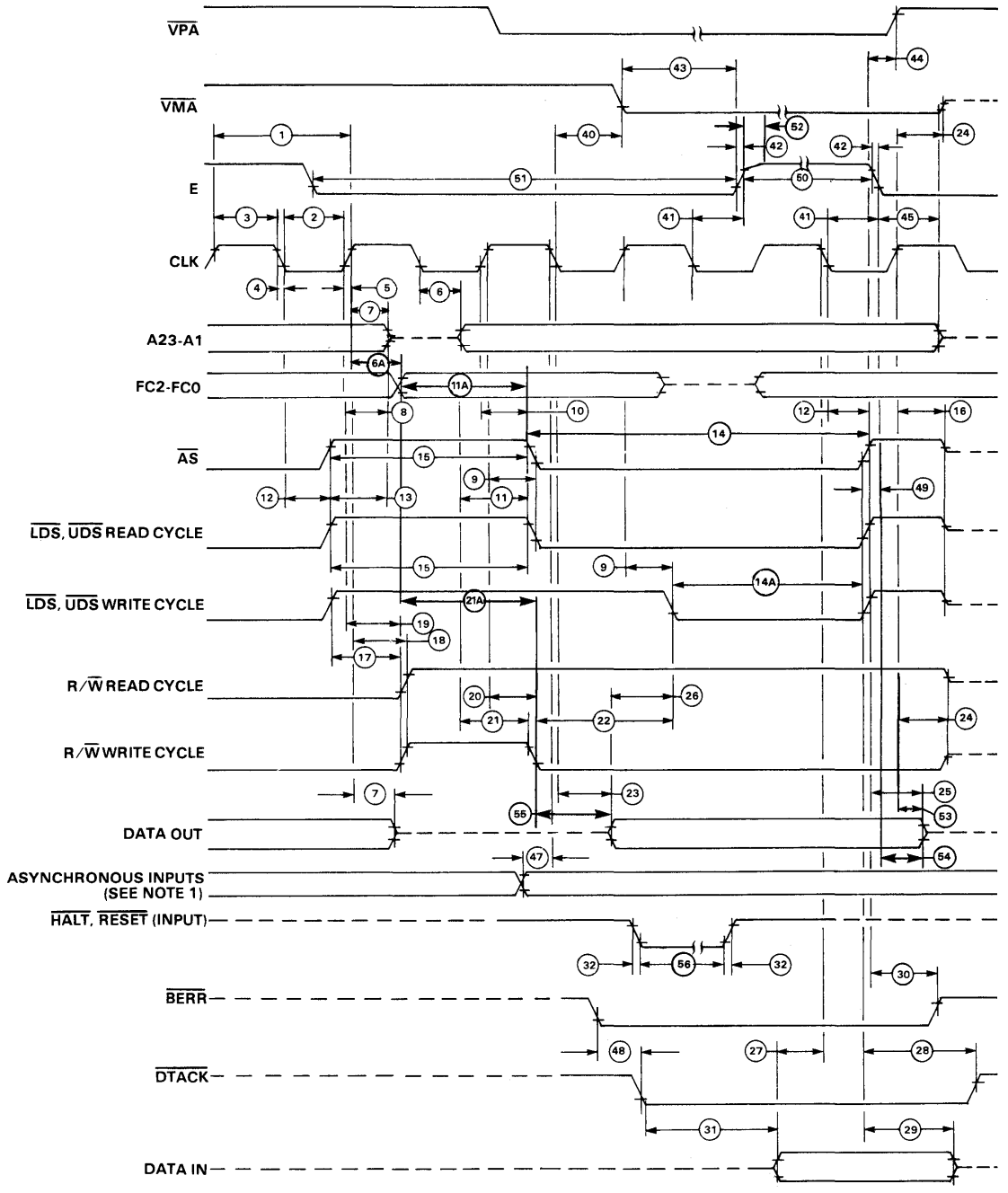
Instruction	Size	Register	Memory	Register → Memory	Memory → Register
ANDI to CCR	Byte	20(3/0)	-	-	-
ANDI to SR	Word	20(3/0)	-	-	-
EORI to CCR	Byte	20(3/0)	-	-	-
EORI to SR	Word	20(3/0)	-	-	-
ORI to CCR	Byte	20(3/0)	-	-	-
ORI to SR	Word	20(3/0)	-	-	-
MOVE from SR	–	6(1/0)	8(1/1)+	–	–
MOVE to CCR	–	12(2/0)	12(2/0)+	–	–
MOVE to SR	–	12(2/0)	12(2/0)+	–	–
MOVEP	Word	–	–	16(2/2)	16(4/0)
	Long	–	–	24(2/4)	24(6/0)
EXG	–	6(1/0)	–	–	–
EXT	Word	4(1/0)	–	–	–
	Long	4(1/0)	–	–	–
LINK	–	16(2/2)	–	–	–
MOVE from USP	–	4(1/0)	–	–	–
MOVE to USP	–	4(1/0)	–	–	–
NOP	–	4(1/0)	–	–	–
RESET	–	132(1/0)	–	–	–
RTE	–	20(5/0)	–	–	–
RTR	–	20(5/0)	–	–	–
RTS	–	16(4/0)	–	–	–
STOP	–	4(0/0)	–	–	–
SWAP	–	4(1/0)	–	–	–
UNLK	–	12(3/0)	–	–	–

+ add effective address calculation time

AC ELECTRICAL WAVEFORMS

Figure 36

These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.



NOTE 1: Setup time for the asynchronous inputs BERR, BGACK, BR, DTACK, IPL0-IPL2, and VPA guarantees their recognition at the next falling edge of the clock.

NOTE 2: Waveform measurements for all inputs and outputs are specified at: logic high = 2.0 volts, logic low = 0.8 volts.

cycles must be added to those of the effective address calculation where indicated.

CONDITIONAL INSTRUCTION CLOCK PERIODS

Table 32 indicates the number of clock periods required for the conditional instructions. The number of bus read and write cycles is indicated in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

JMP, JSR, LEA, PEA, MOVEM INSTRUCTION CLOCK PERIODS

Table 33 indicates the number of clock periods required for the jump, jump to subroutine, load effective address, push effective address, and move multiple registers instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w).

MULTI-PRECISION INSTRUCTION CLOCK PERIODS

Table 34 indicates the number of clock periods for the multi-precision instructions. The number of clock periods includes the time to fetch both operands, perform the operations, store the results, and read the next instructions. The number of read and write cycles is shown in parenthesis as: (r/w).

In Table 34, the headings have the following meanings: Dn = data register operand and M = memory operand.

MISCELLANEOUS INSTRUCTION CLOCK PERIODS

Table 35 indicates the number of clock periods for the following miscellaneous instructions. The number of bus read and write cycles is shown in parenthesis as: (r/w). The number of clock periods plus the number of read and write cycles must be added to those of the effective address calculation where indicated.

EXCEPTION PROCESSING CLOCK PERIODS

Table 36 indicates the number of clock periods for exception processing. The number of clock periods includes the time for all stacking, the vector fetch, and the fetch of the first instruction of the handler routine. The number of bus read and write cycles is shown in parenthesis as: (r/w).

EXCEPTION PROCESSING CLOCK PERIODS

Table 36

Exception	Periods
Address Error	50(4/7)
Bus Error	50(4/7)
Interrupt	44(5/3)*
Illegal Instruction	34(4/3)
Privileged Instruction	34(4/3)
Trace	34(4/3)

*The interrupt acknowledge bus cycle is assumed to take four external clock periods

AC ELECTRICAL SPECIFICATIONS

(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 34)

No.	Characteristic	Symbol	4 MHz MK68000-4		6 MHz MK68000-6		8 MHz MK68000-8		10 MHz MK68000-10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
1	Clock Period	t_{cyc}	250	500	167	500	125	500	100	500	ns
2	Clock Width Low	t_{CL}	115	250	75	250	55	250	45	250	ns
3	Clock Width High	t_{CH}	115	250	75	250	55	250	45	250	ns
4	Clock Fall Time	t_{Cf}	–	10	–	10	–	10	–	10	ns
5	Clock Rise Time	t_{Cr}	–	10	–	10	–	10	–	10	ns
6	Clock Low to Address	t_{CLAV}	–	90	–	80	–	70	–	55	ns
6A	Clock High to FC Valid	t_{CHFCV}	–	90	–	80	–	70	–	60	ns
7	Clock High to Address/Data High Impedance (maximum)	t_{CHAZx}	–	120	–	100	–	80	–	70	ns
8	Clock High to Address/FC Invalid (minimum)	t_{CHAZn}	0	–	0	–	0	–	0	–	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Low (maximum)	t_{CHSLx}	–	80	–	70	–	60	–	55	ns
10	Clock High to $\overline{AS}$, $\overline{DS}$ Low (minimum)	t_{CHSLn}	0	–	0	–	0	–	0	–	ns
11[2]	Address to $\overline{AS}$, $\overline{DS}$ (read) Low/$\overline{AS}$ Write	t_{AVSL}	55	–	35	–	30	–	20	–	ns
11A[2]	FC valid to $\overline{AS}$, $\overline{DS}$ (read) Low/$\overline{AS}$ Write	t_{FCVSL}	80	–	70	–	60	–	50	–	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ High	t_{CLSH}	–	90	–	80	–	70	–	55	ns
13[2]	$\overline{AS}$, $\overline{DS}$ High to Address/FC Invalid	t_{SHAZ}	60	–	40	–	30	–	20	–	ns
14[2]	$\overline{AS}$, $\overline{DS}$ Width Low (read)/ $\overline{AS}$ Write	t_{SL}	535	–	337	–	240	–	195	–	ns
14A[2]	$\overline{DS}$ Width Low (Write)	–	285	–	170	–	115	–	95	–	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width High	t_{SH}	285	–	180	–	150	–	105	–	ns
16	Clock High to $\overline{AS}$, $\overline{DS}$ High Impedance	t_{CHSZ}	–	120	–	100	–	80	–	70	ns
17[2]	$\overline{AS}$, $\overline{DS}$ High to R/$\overline{W}$ High	t_{SHRH}	60	–	50	–	40	–	20	–	ns
18[1]	Clock High to R/$\overline{W}$ High (maximum)	t_{CHRHx}	–	90	–	80	–	70	–	60	ns
19	Clock High to R/$\overline{W}$ High (minimum)	t_{CHRHn}	0	–	0	–	0	–	0	–	ns
20[1]	Clock High to R/$\overline{W}$ Low	t_{CHRL}	–	90	–	80	–	70	–	60	ns
20A	$\overline{AS}$ Low to R/$\overline{W}$ Valid	t_{ASRV}	–	20	–	20	–	20	–	20	ns
21[2]	Address/Valid to R/$\overline{W}$ Low	t_{AVRL}	45	–	25	–	20	–	0	–	ns

VI

AC ELECTRICAL SPECIFICATIONS (Continued)
(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 34)

No.	Characteristic	Symbol	4 MHz		6 MHz		8 MHz		10 MHz		Unit
			MK68000-4		MK68000-6		MK68000-8		MK68000-10		
			Min	Max	Min	Max	Min	Max	Min	Max	
21A[2]	FC Valid to R/$\overline{W}$ Low	t_{FCVRL}	80	–	70	–	60	–	50	–	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Low (write)	t_{RLSL}	200	–	140	–	80	–	50	–	ns
23	Clock Low to Data Out Valid	t_{CLDO}	–	90	–	80	–	70	–	55	ns
24	Clock High to R/$\overline{W}$, $\overline{VMA}$ High Impedance	t_{CHRZ}	–	120	–	100	–	80	–	70	ns
25[2]	$\overline{DS}$ High to Data Out Invalid	t_{SHDO}	60	–	40	–	30	–	20	–	ns
26[2]	Data Out Valid to $\overline{DS}$ Low (write)	t_{DOSL}	55	–	35	–	30	–	20	–	ns
27[5]	Data In to Clock Low (set up time)	t_{DICL}	30	–	25	–	15	–	10	–	ns
28[2]	$\overline{AS}$, $\overline{DS}$ High to $\overline{DTACK}$ High	t_{SHDAH}	0	490	0	325	0	245	0	190	ns
29	$\overline{DS}$ High to Data Invalid (hold time)	t_{SHDI}	0	–	0	–	0	–	0	–	ns
30	$\overline{AS}$, $\overline{DS}$ High to $\overline{BERR}$ High	t_{SHBEH}	0	–	0	–	0	–	0	–	ns
31[2,5]	$\overline{DTACK}$ Low to Data In (setup time)	t_{DALDI}	–	180	–	120	–	90	–	65	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{RHrf}	0	200	0	200	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Low	t_{CHGL}	–	90	–	80	–	70	–	60	ns
34	Clock High to $\overline{BG}$ High	t_{CHGH}	–	90	–	80	–	70	–	60	ns
35	$\overline{BR}$ Low to $\overline{BG}$ Low	t_{BRLGL}	1.5	3.5	1.5	3.5	1.5	3.5	1.5	3.5	clk. per.
36	$\overline{BR}$ High to $\overline{BG}$ High	t_{BRHGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37	$\overline{BGACK}$ Low to $\overline{BG}$ High	t_{GALGH}	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	clk. per.
37A	$\overline{BGACK}$ Low to $\overline{BR}$ High (to Prevent Rearbitration)	t_{BGKBR}	30	–	25	–	20	–	20	–	ns
38	$\overline{BG}$ Low to Bus High Impedance (with $\overline{AS}$ high)	t_{GLZ}	–	120	–	100	–	80	–	70	ns
39	$\overline{BG}$ Width High	t_{GH}	1.5	–	1.5	–	1.5	–	1.5	–	clk. per.
40	Clock Low to $\overline{VMA}$ Low	t_{CLVML}	–	90	–	80	–	70	–	70	ns
41	Clock Low to E Transition	t_{CLE}	–	100	–	85	–	70	–	55	ns
42	E Output Rise and Fall Time	t_{Erf}	–	25	–	25	–	25	–	25	ns
43	$\overline{VMA}$ Low to E High	t_{VMLEH}	325	–	240	–	200	–	150	–	ns
44	$\overline{AS}$, $\overline{DS}$ High to $\overline{VPA}$ High	t_{SHVPH}	0	240	0	160	0	120	0	90	ns
45	E Low to Address/$\overline{VMA}$/FC Invalid	t_{ELAI}	55	–	35	–	30	–	10	–	ns
46	$\overline{BGACK}$ Width	t_{BGL}	1.5	–	1.5	–	1.5	–	1.5	–	clk. per.
47[5]	Asynchronous Input Setup Time	t_{ASI}	30	–	25	–	20	–	20	–	ns

AC ELECTRICAL SPECIFICATIONS (Continued)

(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figure 34)

No.	Characteristic	Symbol	4 MHz MK68000-4		6 MHz MK68000-6		8 MHz MK68000-8		10 MHz MK68000-10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
48[3]	$\overline{BERR}$ Low to $\overline{DTACK}$ Low	t_{BELDAL}	50	–	50	–	50	–	50	–	ns
49	E Low to $\overline{AS}$, $\overline{DS}$ Invalid	t_{ELSI}	-80	–	-80	–	-80	–	-80	–	ns
50	E Width High	t_{EH}	900	–	600	–	450	–	350	–	ns
51	E Width Low	t_{EL}	1400	–	900	–	700	–	550	–	ns
52	E Extended Rise Time	t_{CIEHX}	80	–	80	–	80	–	80	–	ns
53	Data Hold from Clock High	t_{CHDO}	0	–	0	–	0	–	0	–	ns
54	Data Hold from E Low (Write)	t_{ELDOZ}	60	–	40	–	30	–	20	–	ns
55	R/$\overline{W}$ to Data bus Impedance change	t_{RLDO}	55	–	35	–	30	–	20	–	ns
56	Halt/$\overline{RESET}$ Pulse Width (Note 4)	t_{HRPW}	10	–	10	–	10	–	10	–	clk. per.

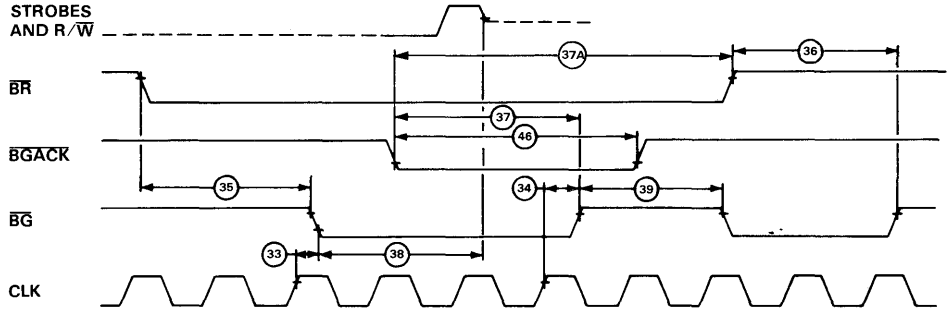
NOTES:

1. For a loading capacitance of less than or equal to 50 picofarads, subtract 5 nanoseconds from the values given in these columns.
2. Actual value depends on actual clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be 0 ns.
4. After V_{CC} has been applied for 100 ms.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{DTACK}$ low-to-data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock-low setup time (#27) for the following cycle.

VI

AC ELECTRICAL WAVEFORMS - BUS ARBITRATION

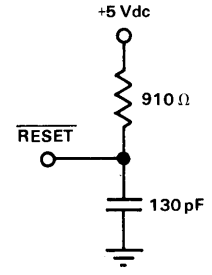
Figure 37



These waveforms should only be referenced in regard to the edge-to-edge measurement of the timing specifications. They are not intended as a functional description of the input and output signals. Refer to other functional descriptions and their related diagrams for device operation.

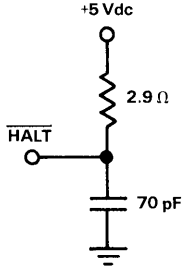
$\overline{RESET}$ TEST LOAD

Figure 38



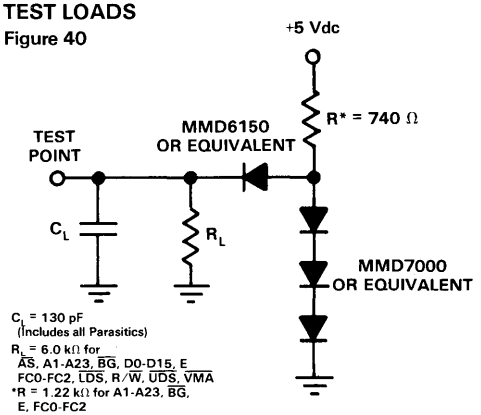
$\overline{HALT}$ TEST LOAD

Figure 39



TEST LOADS

Figure 40



DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%; V_{SS} = 0 Vdc; T_A = 0°C to 70°C, Figures 35, 36, 37)

Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} - 0.3	0.8	Vdc
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{VPA}$, $\overline{DTACK}$, CLOCK, $\overline{IPL0}$-$\overline{IPL2}$, $\overline{HALT}$, $\overline{RESET}$	I_{in}	– –	2.5 20	μAdc
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A1-A23, D0-D15, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	I_{TSI}	–	20	μAdc
Output High Voltage (I_{OH} = –400 μAdc)	$\overline{AS}$, A1-A23, $\overline{BG}$, E*** D0-D15, E, FC0-FC2, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$ E*	V_{OH}	2.4 V_{CC}–0.75	–	Vdc
Output Low Voltage (I_{OL} = 1.6mA) (I_{OL} = 3.2mA) (I_{OL} = 5.0mA) (I_{OL} = 5.3mA)	 $\overline{HALT}$ A1-A23, $\overline{BG}$, FC0-FC2 $\overline{RESET}$ E, $\overline{AS}$, D0-D15, $\overline{LDS}$, R/$\overline{W}$, $\overline{UDS}$, $\overline{VMA}$	V_{OL}	 – – – –	 0.5 0.5 0.5 0.5	Vdc
Power Dissipation (Clock Frequency = 8 MHz)****		P_D	–	1.5	W
Capacitance (Package Type Dependent) (V_{in} = 0 Vdc; T_A = 25°C; Frequency = 1 MHz**)		C_{in}	–	20.0	pF

*with external pullup resistor of 1.1K Ω
**capacitance is periodically sampled rather than 100% tested
***without external pullup resistor
****During normal operation instantaneous V_{CC} current requirements may lbe as high as LSA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.3 to + 7.0	Vdc
Input Voltage	V_{in}	–0.3 to + 7.0	Vdc
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

MK68000 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX. CLOCK FREQUENCY	TEMPERATURE RANGE
MK68000P-4	Ceramic	4.0 MHz	0° to 70°C
MK68000P-6	Ceramic	6.0 MHz	
MK68000P-8	Ceramic	8.0 MHz	
MK68000P-10	Ceramic	10.0 MHz	

PRELIMINARY

16-BIT MICROPROCESSOR WITH 8-BIT DATA BUS MK68008

FEATURES

- ☐ 17 32-bit data and address registers
- ☐ 56 basic instruction types
- ☐ Extensive exception processing
- ☐ Memory mapped I/O
- ☐ 14 addressing modes
- ☐ Complete code compatibility with the MK68000

GENERAL DESCRIPTION

The MK68008 is a member of the MK68000 family of advanced microprocessors. This device allows the design of cost effective systems using 8-bit data buses, while providing the benfits of a 32-bit microprocessor architecture. The performance of the MK68008 is greater than any 8-bit microprocessor and superior to several 16-bit microprocessors.

A system implementation based on an 8-bit data bus reduces system cost, in compairson to 16-bit systems, due to a more effective use of components, byte-wide memories, and peripherals. In addition , the non-multiplexed address and data buses eliminate the need for external demultiplexers, thus further simplifying the system.

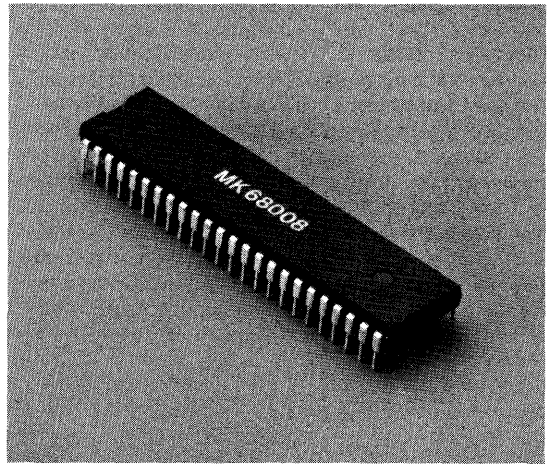
The MK68008 has full code compatibility (source and object) with the MK68000, which allows programs to be run on either MPU, depending on performance requirements and cost objectives.

The 1 megabyte, non-segmented linear address space of the MK68008 allows large modular programs to be developed and executed efficiently. A large linear address space allows program segment sizes to be determined by the application, rather than forcing the designer to adopt an arbitrary segment size without regard to his individual requirements.

The programmer's model, as shown in Figure 3, is identical to that of the MK68000, with 17 32-bit registers, a 32-bit program counter, and a 16-bit status register. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations.

MK68008

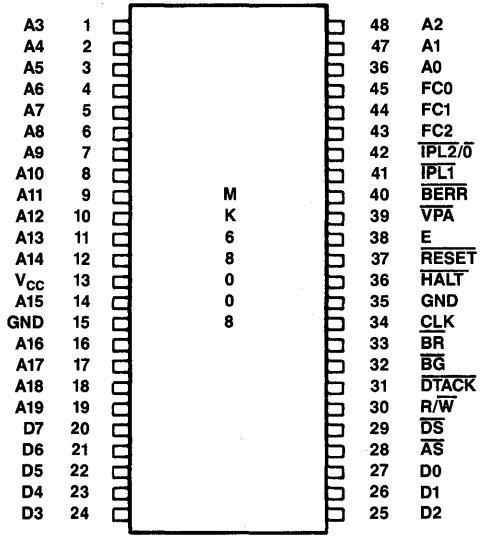
Figure 1



VI

PIN ASSIGNMENT

Figure 2



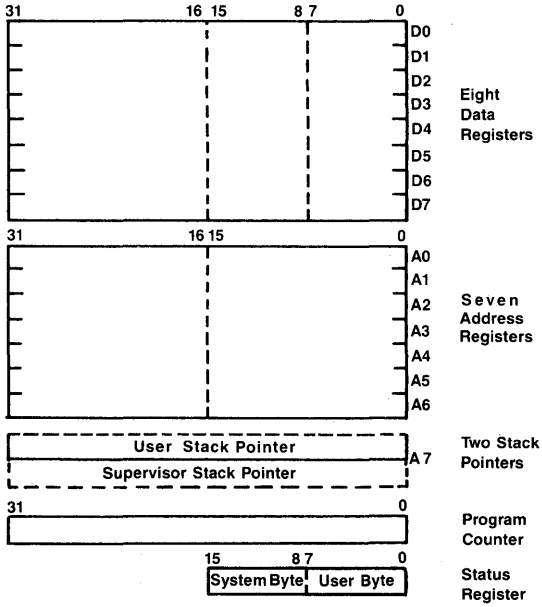
The second set of seven registers (A0-A6) and the system stack pointer (A7) may be used as software stack pointers and base address registers. In addition, the registers may be used for word and long word operations. All of the 17 registers may be used as index registers.

The system stack is used by many instructions. The 14 addressing modes allow the creation of user stacks and queues. The system stack pointer is either the supervisor stack pointer (SSP) or the user stack pointer (USP), depending on the state of the S bit in the status register. If the S bit indicates that the processor is in the user state, then the USP is the active system stack pointer, and the SSP is protected from user modification.

The status register, as shown in Figure 4, may be considered as two bytes: the user byte and the system byte. The user byte contains five bits defining the overflow (V), zero (Z), negative (N), carry (C), and extended (X) condition codes. The system byte contains five bits. Three bits are used to define the current interrupt priority; any interrupt level higher than the current mask level will be recognized. (Note that level 7 interrupts are non-maskable—that is, level 7 interrupts are always processed). Two additional bits indicate whether the processor is in the trace (T) mode and/or in the supervisor (S) state.

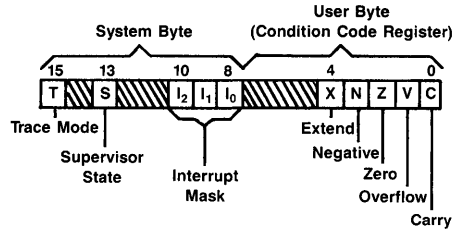
PROGRAMMER'S MODEL

Figure 3



STATUS REGISTER

Figure 4



DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

- Bits
- Words (16 bits)
- BCD Digits (4 bits)
- Long Words (32 bits)
- Bytes (8 bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided in the instruction set.

Most instructions can use any of the 14 addressing modes which are listed in Table 1. These addressing modes consist of six basic types:

- Register Direct
- Register Indirect
- Absolute
- Program Counter Relative
- Immediate
- Implied

ADDRESSING MODES

Table 1

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA=Dn
Address Register Direct	EA=An
Absolute Data Addressing	
Absolute Short	EA=(Next Word)
Absolute Long	EA=(Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA=(PC)+d_{16}
Relative with Index and Offset	EA=(PC)+(Xn)+d_8
Register Indirect Addressing	
Register Indirect	EA=(An)
Postincrement Register Indirect	EA=(An), An←An+N
Predecrement Register Indirect	An←An−N, EA=(An)
Register Indirect with Offset	EA=(An)+d_{16}
Indexed Register Indirect with Offset	EA=(An)+(Xn)+d_8
Immediate Data Addressing	
Immediate	DATA=Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA=SR, USP, SP, PC

NOTES:
EA=Effective Address
An=Address Register
Dn=Data Register
Xn=Address or Data Register used as Index Register
SR=Status Register
PC=Program Counter
( )=Contents of
d_8=8-Bit Offset (Displacement)
d_{16}=16-Bit Offset (Displacement)
N=1 for byte, 2 for word, and 4 for long word. If An is the stack pointer and the operand is byte, N=2 to keep the stack pointer on a word boundary.
←=Replaces

The register indirect addressing modes also have the capability to perform post-incrementing, pre-decrementing, offsetting, and indexing. The program counter relative mode may be used in combination with indexing and offseting for writing relactable programs.

INSTRUCTION SET OVERVIEW

The MK68008 is completely code compatible with the MK68000. This means that programs developed for the MK68000 will run on the MK68008 and vice versa. This applies equally to either source code or object code.

The instruction set was designed to minimized the number of mnemonics remembered by the programmer. To further reduce the programmer's burden, the addressing modes are orthogonal.

The instruction set, shown in Table 2, forms a set of programming tools that include all processor functions to perform data movement, integer arithmetic, logical operations, shift and rotate operations, bit manipulation, BCD operations, and both program and system control. Some additional instructions are variations or subsets of these and appear in Table 3.

INSTRUCTION SET

Table 2

Mnemonic	Description
ABCD	Add Decimal With Extend
ADD	Add
AND	Logical And
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
B_{CC}	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR	Clear Operand
CMP	Compare
DB_{CC}	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive Or
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral Data
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical Or
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
S_{CC}	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

VARIATIONS OF INSTRUCTION TYPES

Table 3

Instruction Type	Variation	Description
ADD	ADD	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	AND	Logical And
	ANDI	And Immediate
	ANDI to CCR	And Immediate to Condition Codes
	ANDI to SR	And Immediate to Status Register
CMP	CMP	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	EOR	Exclusive Or
	EORI	Exclusive Or Immediate
	EORI to CCR	Exclusive Or Immediate to Condition Codes
	EORI to SR	Exclusive Or Immediate to Status Register
MOVE	MOVE	Move
	MOVEA	Move Address
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG	Negate
	NEGX	Negate with Extend
OR	OR	Logical Or
	ORI	Or Immediate
	ORI to CCR	Or Immediate to Condition Codes
	ORI to SR	Or Immediate to Status Register
SUB	SUB	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

ORDERING INFORMATION

Part No.	Package Type	Max. Clock Frequency	Temperature Range
MK68008N-8	Plastic	8.0 MHz	0° to 70°C
MK68008N-10	Plastic	10.0 MHz	0° to 70°C

ADVANCE INFORMATION

VIRTUAL MEMORY MICROPROCESSOR MK68010

FEATURES

- ☐ 17 32-bit data and address registers
- ☐ 16-megabyte direct addressing range
- ☐ Virtual memory/machine support
- ☐ 57 powerful instruction types
- ☐ High-performance looping instructions
- ☐ Operations on five main data types
- ☐ Memory mapped I/O
- ☐ 14 addressing modes

GENERAL DESCRIPTION

The MK68010 is the third in a family of advanced microprocessors from Mostek. Utilizing VLSI technology, the MK68010 is a fully implemented 16-bit microprocessor with 32-bit registers, a rich basic instruction set, and versatile addressing modes.

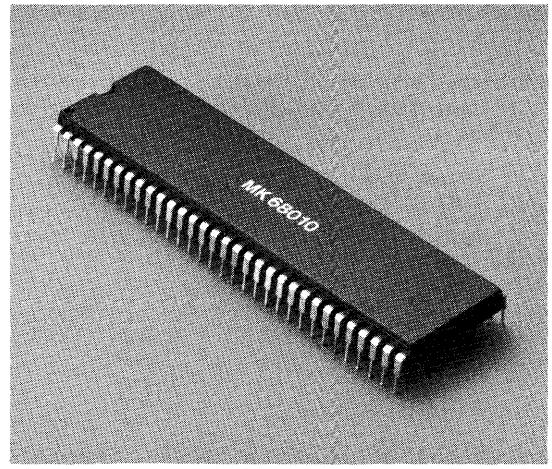
The MK68010 is fully object code compatible with the earlier members of the MK68000 family and has the added features of virtual memory support and enhanced instruction execution timing.

The MK68010 possesses an asynchronous bus structure with a 24-bit address bus and a 16-bit data bus.

As shown in the programming model (Figures 3 and 4), the MK68010 offers 17 32-bit general purpose registers, a 32-bit program counter, a 16-bit status register, a 32-bit vector base register, and two 3-bit alternate function code registers. The first eight registers (D0-D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0-A6) and the stack pointers (SSP, USP) may be used as software stack pointers and base address registers. In addition, the address registers may be used for word and long word operations. All of the 17 registers may be used as index registers.

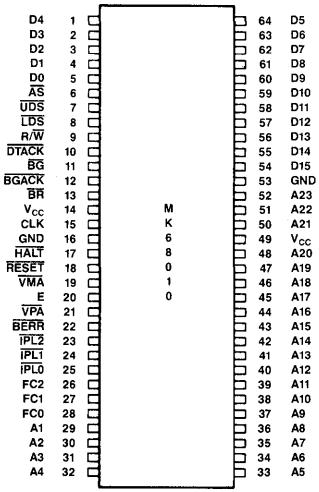
The status register, as shown in Figure 5, contains the interrupt mask (eight levels available) as well as the condition codes; extend (X), negative (N), zero (Z), overflow (V), and carry (C). Additional status bits indicate that the processor is in the trace (T) mode and in the supervisor (S) or user state.

MK68010
Figure 1



PIN ASSIGNMENT

Figure 2



The vector base register is used to determine the location of the exception vector table in memory to support multiple vector tables. The alternate function code registers allow the supervisor to access user data space or emulate CPU space cycles.

FUNCTIONAL DESCRIPTION

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported. These data types are:

- Bits
- BCD Digits (4 bits)
- Bytes (8 bits)
- Words (16 bits)
- Long Words (32 bits)

In addition, operations on other data types such as memory addresses, status word data, etc., are provided in the instruction set.

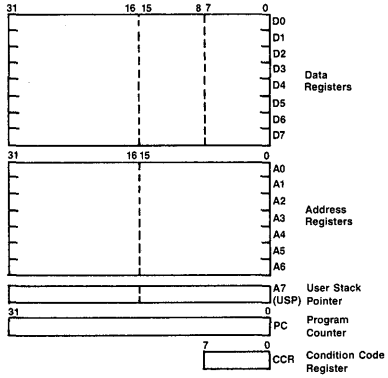
The 14 address modes, shown in Table 1, include six basic types:

- Register Direct
- Register Indirect
- Absolute
- Program Counter Relative
- Immediate
- Implied

Included in the register indirect addressing modes is the capability to do post-incrementing, pre-decrementing, offsetting, and indexing. The program counter relative mode can also be modified via indexing and offsetting.

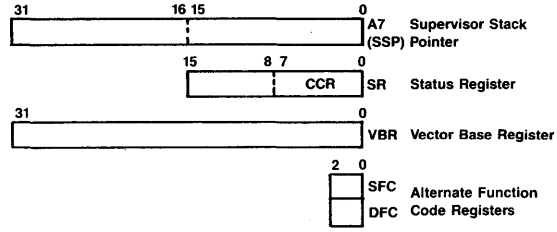
PROGRAMMING MODEL

Figure 3



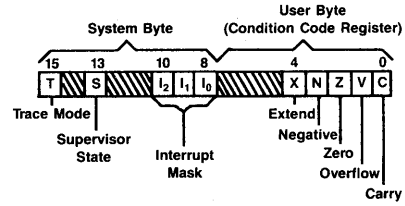
SUPERVISOR PROGRAMMING MODEL SUPPLEMENT

Figure 4



STATUS REGISTER

Figure 5



INSTRUCTION SET OVERVIEW

The MK68010 instruction set is shown in Table 2. Some additional instructions are variations, or subsets, of these, and they appear in Table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with few exceptions, operates on bytes, words, and long words, and most instructions can use any of the 14 addressing modes. By combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, "quick" arithmetic operations, BCD arithmetic, and expanded operations (through traps). Also, 33 instructions may be used in the loop mode with certain addressing modes and the DB_{CC} instruction to provide 230 high performance string, block manipulation, and extended arithmetic operations.

VIRTUAL MEMORY/MACHINE CONCEPTS

In most systems that use the MK68010 as the central processor, only a fraction of the 16 megabyte address space will actually contain physical memory. However, by using virtual memory techniques, the system can appear to the user to have 16 megabytes of physcial memory available. These techniques have been used for several years in large mainframe computers and more recently in minicomputers. Now, with the MK68010, they can be fully supported in microprocessor-based systems.

In a virtual memory system, a user program can be written as though it has a large amount of memory available when it actually has only a small amount of memory physically present in the system. In a similar fashion, a system can be designed to allow user programs to access other types of devices not physically present in the system, such as tape drives, disk drives, printers, or CRTs. With proper software emulation, a physical system can be made to appear to a user program as any other computer system, and the program may be given full access to all the resources of that emulated system. Such an emulated system is called a virtual machine.

VIRTUAL MEMORY

The basic mechanism for supporting virtual memory in computers is to provide only a limited amount of high-speed physical memory that can be accessed directly by the processor, while maintaining an image of a much larger "virtual" memory on secondary storage devices such as large capacity disk drives. When the processor attempts to access a location in the virtual memory map that is not currently residing in physical memory (referred to as a page fault), the access to that location is temporarily suspended while the necessary data is fetched from the secondary storage and placed in physical memory; the suspended acccess is then completed. The MK68010 provides hardware support for virtual memory with the capability of suspending an instruction's execution when a bus error is signaled and then completing the instruction after the physical memory has been updated as necessary.

The MK68010 uses instruction continuation rather than instruction restart to support virtual memory. With instruction restart, the processor must remember the exact state of the system before each instruction is started to restore that state if a page fault occurs during its execution. Then, after the page fault has been repaired, the entire instruction that caused the fault is re-executed. With instruction continuation, when a page fault occurs, the processor stores its internal state and then, after the page fault is repaired, restores that internal state and continues execution of the instruction. For the MK68010 to utilize instruction continuation, it stores its internal state on the supervisor stack when a bus cycle is terminated with a bus error signal. It then loads the program counter from vector table entry number two (offset $008) and resumes program execution at that new addresss. When the bus error exception handler routine has completed execution, an RTE instruction is executed that reloads the MK68010 with the internal state stored on the stack, re-runs the faulted bus cycle, and continues the suspended instruction. Instruction continuation has the additional advantage of allowing hardware support for virtual I/O devices. Since virtual registers may be simulated in the memory map, an access to such a register will cause a fault, and the function of the register can be emulated by software.

VIRTUAL MACHINE

One typical use for a virtual machine system is in the development of software which is an operating system for another machine that has hardware also under development and is not available for programming use. In such a system, the governing operating system (OS) emulates the hardware of the new system and allows the new OS to be executed and debugged as though it were running on the new hardware. Since the new OS is controlled by the governing OS, the new one must execute at a lower privilege level than the governing OS so that any attempts by the new OS to use virtual resources that are not physically present, and should be emulated, will be trapped by the governing OS and handled in software. In the MK68010, a virtual machine may be fully supported by running the new OS in the user mode and the governing OS in the supervisor mode so that any attempts to access supervisor resources or execute privileged instructions by the new OS will cause a trap to the governing OS.

In order to fully support a virtual machine, the MK68010 must protect the supervisor resources from access by user programs. The one supervisor resource not fully protected in the MK68000 is the system byte of the status register. In the MK68000, the MOVE from SR instruction allows user programs to test the S bit (in addition to the T bit and interrupt mask) and thus determine that they are running in the user mode. For full virtual machine support, a new OS must not be aware that it is running in the user mode and thus should not be allowed to access the S bit. For this reason, the MOVE from SR instruction on the MK68010 is a privileged instruction, and the MOVE from CCR instruction has been added to allow user programs unhindered access to the condition codes. By making the MOVE from SR instruction privileged, when the new OS attempts to access the S bit, a trap to the governing OS will occur and the SR image passed to the new OS by the governing OS will have the S bit set.

ADDRESSING MODES

Table 1

Mode	Generation
Register Direct Addressing	
Data Register Direct	EA=Dn
Address Register Direct	EA=An
Absolute Data Addressing	
Absolute Short	EA=(Next Word)
Absolute Long	EA=(Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA=(PC)+d_{16}
Relative with Index and Offset	EA=(PC)+(Xn)+d_8
Register Indirect Addressing	
Register Indirect	EA=(An)
Postincrement Register Indirect	EA=(An), An←An+N
Predecrement Register Indirect	An←An−N, EA=(An)
Register Indirect with Offset	EA=(An)+d_{16}
Indexed Register Indirect with Offset	EA=(An)+(Xn)+d_8
Immediate Data Addressing	
Immediate	DATA=Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA=SR, USP, SSP, PC, VBR, SFC, DFC

NOTES:
EA=Effective Address
An=Address Register
Dn=Data Register
Xn=Address or Data Register used as Index Register
SR=Status Register
PC=Program Counter
( )=Contents of
d_8=8-Bit Offset (Displacement)
d_{16}=16-Bit Offset (Displacement)
N=1 for byte, 2 for word, and 4 for long word. If An is the stack pointer and the operand size is byte, N=2 to keep the stack pointer on a word boundary.
←=Replaces

INSTRUCTION SET SUMMARY

Table 2

Mnemonic	Description
ABCD*	Add Decimal with Extend
ADD*	Add
AND*	Logical And
ASL*	Arthmetic Shift Left
ASR*	Arthmetic Shift Right
B_{CC}	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register Against Bounds
CLR*	Clear Operand
CMP*	Compare
DB_{CC}	Decrement and Branch Conditionally
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR*	Exclusive Or
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL*	Logical Shift Left
LSR*	Logical Shift Right
MOVE*	Move Source to Destination
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD*	Negate Decimal with Extend
NEG*	Negate
NOP	No Operation
NOT*	One's Complement
OR*	Logical Or
PEA	Push Effective Address
RESET	Reset External Devices
ROL*	Rotate Left without Extend
ROR*	Rotate Right without Extend
ROXL*	Rotate Left with Extend
ROXR*	Rotate Right with Extend
RTD	Return and Deallocate
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD*	Subtract Decimal with Extend
S_{CC}	Set Conditional
STOP	Stop
SUB*	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST*	Test
UNLK	Unlink

*Loopable Instructions

VARIATIONS OF INSTRUCTION TYPES

Table 3

Instruction Type	Variation	Description
ADD	ADD*	Add
	ADDA*	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX*	Add with Extend
AND	AND*	Logical And
	ANDI	And Immediate
	ANDI to CCR	And Immediate to Condition Codes
	ANDI to SR	And Immediate to Status Register
CMP	CMP*	Compare
	CMPA*	Compare Address
	CMPM*	Compare Memory
	CMPI	Compare Immediate
EOR	EOR*	Exclusive Or
	EORI	Exclusive Or Immediate
	EORI to CCR	Exclusive Or Immediate to Condition Codes
	EORI to SR	Exclusive Or Immediate to Status Register
MOVE	MOVE*	Move Source to Destination
	MOVEA*	Move Address
	MOVEC	Move Control Register
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVES	Move Alternate Address Space
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE from CCR	Move from Condition Codes
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG*	Negate
	NEGX*	Negate with Extend
OR	OR*	Logical Or
	ORI	Or Immediate
	ORI to CCR	Or Immediate to Condition Codes
	ORI to SR	Or Immediate to Status Register
SUB	SUB*	Subtract
	SUBA*	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subract Quick
	SUBX*	Subtract with Extend

*Loopable Instructions

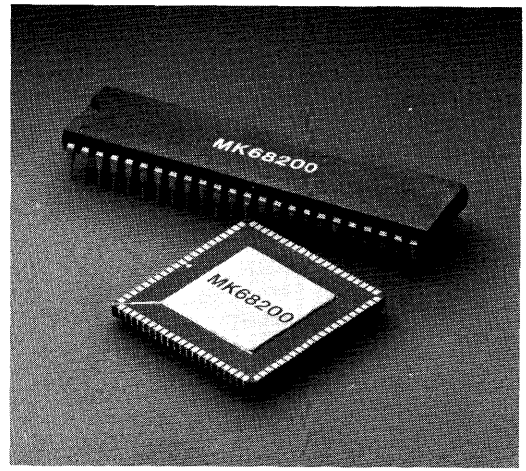
PRELIMINARY

68200 16-BIT SINGLE-CHIP MICROCOMPUTERS MK68201/MK68E201/MK68211/MK68E211

FEATURES

- ☐ 16-bit, high performance, single-chip microcomputer
- ☐ 14 address and data registers
  - Eight 16-bit or sixteen 8-bit data registers
  - Six 16-bit address registers
- ☐ Advanced 16-bit instruction set
  - Bit, byte, and word operands
  - Nine addressing modes
  - Byte and word BCD arithmetic
- ☐ High performance (6 MHz instruction clock)
  - 500 ns register-to-register move or add
  - 3.5 μs 16 x 16 multiply
  - 4.0 μs 32/16 divide
- ☐ Available with 0 or 4K (2K x 16) bytes of ROM
- ☐ 256 byte RAM (128 x 16)
- ☐ Three 16-bit timers
  - Interval modes
  - Event modes
  - One-shot modes
  - Pulse and period measurement modes
  - Two input and two output pins
- ☐ Serial channel
  - Double-buffered receive and transmit
  - Asynchronous to 375 Kbps
  - Synchronous to 1.5 Mbps
  - Address wake-up recognition and generation
  - Internal/external baud rate generation
- ☐ Parallel I/O
  - Up to 40 pins
  - Direction programmable by bit
  - One 16-bit or two 8-bit port(s) with handshaking
- ☐ Interrupt controller
  - 16 independent vectors
  - Eight external interrupt sources
  - One non-maskable interrupt
  - Individual interrupt masking

MK68200
Figure 1

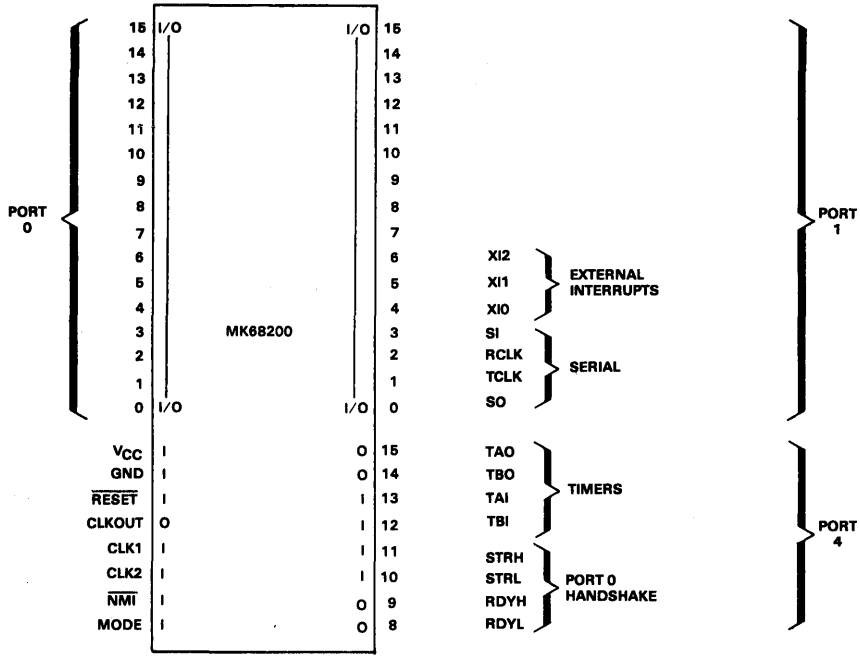


- ☐ Optional external bus
  - 16-bit, multiplexed address/data bus
  - Automatic bus request/grant arbitration
  - Two control bus versions:
    - 68000-compatible bus (UPC)
    - General Purpose Bus (GP)
- ☐ 8 and 12 MHz time base versions produce 4 and 6 MHz instruction clock rates, respectively.
  - Crystal or external TTL clock
- ☐ Single +5 volt power supply
- ☐ 48-pin DIP or 84-pin LCC

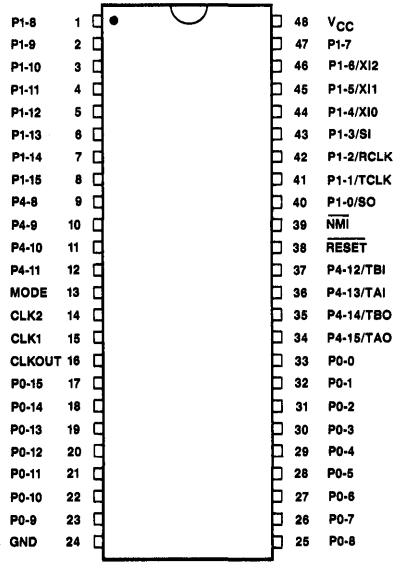
GENERAL DESCRIPTION

MK68200 designates a series of new, high-performance, 16-bit, single-chip microcomputers from Mostek. Implemented in Scaled Poly-5 NMOS, they incorporate an architecture designed for superior performance in computation-intensive control applications. A modern, comprehensive instruction set, which features both high speed execution and code space efficiency, is combined on-chip along with extensive, flexible I/O capabilities. On-chip RAM and optional on-chip ROM are provided within a full 64K byte addressing space.

MK68200 LOGICAL PINOUT SINGLE-CHIP MODE
Figure 2



MK68200 SINGLE-CHIP PIN ASSIGNMENT (48-PIN DIP)
Figure 3



The MK68200 is designed to serve the needs of a wide variety of control applications, which require high performance operation with a minimal parts count implementation. Industrial controls, instrumentation, and intelligent computer peripheral controls are all examples of applications served by the MK68200. High speed mathematical ability, rapid I/O addressing and interrupt response, and powerful bit manipulation instructions provide the necessary tools for these applications. In addition to its single-chip microcomputer configuration, both distributed intelligence and parallel multiprocessing system configurations are supported by the MK68200, as illustrated in Figures 12 and 13.

In applications requiring loosely coupled, distributed intelligence, several MK68200's may be interconnected on a common serial network. The on-chip USART supports a wake-up mode in which an additional bit is appended to the data stream to distinguish a serial data word as address or data. The wake-up logic prevents the serial channel from generating interrupts unless a specific address is recognized.

Alternately, the MK68200 may be configured as an expandable CPU device which can access external memory and I/O resources. In this operating mode, parallel I/O pins are replaced by multiplexed address/data and control lines. Bus arbitration logic is incorporated on the chip to support a direct interface in parallel shared bus multiprocessor system configurations. Two versions exist which support two types of control signals present on the expanded bus configuration. The General Purpose (GP) bus option allows the MK68200 to operate either as an executive or a peripheral processor. As an executive procesor, the MK68200 can control an external system bus and grant the use of it to requesting devices, such as DMA controllers and/or peripheral processors. As a peripheral control processor, the MK68200 can provide intelligent local control of an I/O device in a computer system and, thereby, relieve the executive processor of these tasks. In this configuration, the MK68200 has the capability of effectively performing DMA transfers between system memory and the I/O device. The on-chip resources of ROM, RAM, and I/O are accessed within the MK68200 without affecting the utilization of the shared system bus so that only external communications compete for bus bandwidth.

The Universal Peripheral Controller (UPC) bus option supports a direct interface to a 68000 executive processor. Thus, the MK68200 can be used as a cost-effective, intelligent peripheral controller in 68000 systems. The UPC version's direct bus interface to the 68000 makes the MK68200 particularly well-suited for performing many intelligent I/O functions in a 68000 system. For example, since the MK68200 includes both a serial channel and an external bus capable of performing DMA transfers, it can be programmed to act as serial protocol controller with DMA capability, as shown in Figure 4.

Table 1 summarizes the specific MK68200 device types that are discussed in this data sheet. A complete guide to the part numbering scheme used throughout this document may be found in the Ordering Information section. All MK68200 devices retain most of the I/O features when they are used in the expanded bus mode; however, 24 pins of parallel I/O are sacrificed when this mode is used. When the expanded bus mode is selected, the MK68201/XX generates UPC (68000-compatible) control signals, while the MK68211/XX generates GP control signals. Also available are 84-pin emulator versions of these devices that do not have on-chip ROM, but instead have additional pins to support a second complete address/data bus to access off-chip ROM, RAM, EPROM, or I/O devices. This bus is referred to as the private bus and is not bonded out on 48-pin versions.

For additional information on the MK68200, refer to the MK68200 Principles of Operation Manual, publication number 4420399, and to the MK68200 Programming Reference Guide, publication number 4420465.

VI

SINGLE-CHIP DESCRIPTION

Figure 2 is a diagram which illustrates the functions of specific pins for a MK68201 or MK68211, operating in a single-chip mode. When the device is operating in one of the expanded bus modes, the pins on Port 0 become the multiplexed address/data bus, and the upper half of Port 1 becomes the control signals (GP or UPC) for the bus. The following description applies to the pins only when the device is used in the non-expanded or single-chip mode. Descriptions of the pin functions for the expanded bus modes may be found in the Expanded Bus Operation section of this data sheet.

V_{CC}, GND
(Power, Ground)
Power Supply pins.
(single +5 V)

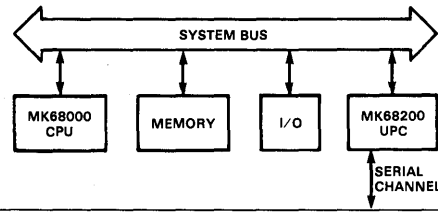
$\overline{\text{RESET}}$
Input, active low. $\overline{\text{RESET}}$ input overrides ongoing execution (including interrupts) and resets the chip to its initial power-up condition. $\overline{\text{RESET}}$ cannot be masked.

CLKOUT
(Clock Output)
Output. CLKOUT will output the instruction clock rate, which is one-half of the frequency provided on CLK1 and CLK2.

CLK1, CLK2
(Time base Inputs)
Inputs. CLK1 and CLK2 may be connected to a crystal, or CLK1 may be connected to an external TTL-compatible oscillator while CLK2 is left floating. The

SERIAL DMA CONTROLLER

Figure 4



DEVICE TYPE SUMMARY

Table 1

Device Type	Expanded Bus Version	ROM (Bytes)	RAM (Bytes)	PKG.
MK68201/04	UPC	0	256	48-pin DIP
MK68201/44	UPC	4096	256	48-pin DIP
MK68E201/04	UPC	0	256	84-pin LCC
MK68211/04	GP	0	256	48-pin DIP
MK68211/44	GP	4096	256	48-pin DIP
MK68E211/04	GP	0	256	84-pin LCC

instruction clock rate is one-half of the frequency provided on CLK1 and CLK2.

$\overline{NMI}$
(Non-Maskable Interrupt)
Input, active low, negative edge triggered. The NMI request line has a higher priority than all of the maskable interrupts. NMI is always enabled regardless of whether the L1E (Level 1 Interrupt Enable) bit is set in the Status Register.

MODE
Input. The MODE pin is used to configure the MK68200 on power-up and reset to one of the following states:

Mode Pin
V_{CC} - No expansion (single chip mode)
GND - Partial Expansion
CLKOUT - Full Expansion

P0-0 - P0-15
(Port 0)
Input/Output. Each bit in Port 0 may be individually programmed for general purpose input or output. Port 0 also has several handshaking modes to allow parallel, asynchronous communication with other devices. The high and low bytes may be programmed individually or jointly to be inputs, outputs, or bidirectional.

P1-0 - P1-15
(Port 1)
Input/Output. Each of the 16 bits in Port 1 may be individually programmed for input or output. Additionally, the lowest seven bits of Port 1 may be programmed to serve specific alternate functions, as listed below.

P1-6/XI2
(External Interrupt 2)
Input, rising or falling edge triggered. The programmer may select the rising or falling edge as active for XI2.

P1-5/XI1
(External Interrupt 1)
Input, fixed falling edge triggered. The XI1 interrupt may be used to interrupt the MK68200 on the falling edge of an input pulse.

P1-4/$\overline{XI0}$
(External Interrupt 0)
Input, low level triggered. The XI0 interrupt input is level-triggered (unlike XI1, XI2). It may be used to produce an internally vectored interrupt or to cause an external fetch of an interrupt vector number when the MK68200 is used in an expanded mode with the GP bus.

P1-3/SI
(Serial Input)
Input, active high. SI is used to input receive serial data when the receiver is enabled.

P1-2/RCLK
(Receive Clock)
Input/Output, active high. Depending on the mode programmed, RCLK can be used by the serial port as either an input or an output pin. When used as an input pin, RCLK provides the receive clock and/or the transmit clock. When RCLK is not providing the transmit or receive clock, it can be used as an output for Timer C. In this mode, the receive clock is being provided by Timer C.

P1-1/TCLK
(Transmit-Clock)
Input/Output, active high. Depending on the mode programmed, TCLK can be used by the serial port as either an input or an output pin. When used as an input pin, TCLK provides the transmit clock. When TCLK is not providing the transmit clock, it can be used as an output for Timer C. In this mode, the transmit clock is being provided by either Timer C or RCLK.

P1-1/SO
(Serial Output)
Output, active high. SO is used to output transmit serial data when the transmitter is enabled.

P4-8 - P4-15
(Port 4)
Inputs and Outputs. P4-8, P4-9, P4-14, and P4-15 may be used as general purpose outputs, and P4-10, P4-11, P4-12, and P4-13 may be used as general purpose inputs. Interrupts may be generated on the positive transitions on P4-10 and P4-11. Depending on the mode selected, interrupts may be generated on the positive or negative transitions on P4-12, or they may be generated on the positive, negative, or combined transitions on P4-13. Additionally, these bits may be programmed to serve specific alternate functions, as listed below.

P4-15/TAO
(Timer A Output)
Output. TAO may be programmed for special functions in the interval, event, and pulse modes for Timer A. In the interval mode, TAO's state is determined by the Timer A latch (high or low) that is currently active. That is, if the counter is using the high latch for comparison, TAO is high. If the counter is using the low latch for comparison, TAO is low. In the event mode, TAO is initialized to a "1" state and toggles each time the counter matches the Timer A high latch. In the pulse/period modes, TAO is initiated to a "1" state and toggles on positive transitions on TAI.

P4-14/TBO
(Timer B Ouput)
Output. TBO may be programmed for special functions in the interval and one-shot modes for Timer B. In the interval mode, TBO is initialized to a "1" state and toggles each time the counter matches the Timer B latch value. In the one-shot modes, TBO is initialized to a "1" state, and the counter begins counting in response to the occurrence of an active edge on TBI. TBO will not go low until the counter matches the value loaded into the Timer B latch.

P4-13/TAI
(Timer A Input)
Input, positive and/or negative edge triggered. TAI may be programmed for special functions in the event mode or pulse/period modes for Timer A. In the event mode, the counter is incremented on each active transition (positive or negative edge programmable) on TAI. In the pulse/period modes, the counter measures the time during which the signal on TAI remains high and low.

P4-12/TBI
(Timer B Input)
Input, positive or negative edge triggered. TBI may be programmed for special functions for the Timer B one-shot modes. In the one-shot modes, TBI acts as a trigger input

P4-11/STRH, P4-10/STRL
(Strobe High Byte, Strobe Low Byte)
Input, active high. STRH and STRL are both used for input, output, and bidirectional handshaking on Port 0.

1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the MK68200.

2) Input mode: The stobe is issued by the peripheral to load data from the peripheral into the Port 0 input register. Data is latched into the MK68200 on the negative edge of this signal.

3) Bidirectional mode: When the STRH signal is active, data from the Port 0 output register is gated onto the Port 0 bidirectional data bus.

The negative edge of STRH acknowledges the receipt of the output data. The negative edge of the signal applied to the STRL signal is used to latch input data into Port 0.

P4-9/RDYH, P4-8/RDYL
(Ready High Byte, Ready Low Byte)
Output, active high. RDYH and RHYL are used for input, output, and bidirectional handshaking on Port 0.

1) Output mode: The ready signal goes active to indicate that the Port 0 output register has been loaded, and the peripheral data is stable and ready for transfer to the peripheral device.

2) Input mode: The ready signal is active when the Port 0 input register is empty and is ready to accept data from the peripheral device.

3) Bidirectional mode: The RDYH signal is active when data is available in Port 0 output register for transfer to the peripheral device. In this mode, data is not placed on the Port 0 data bus unless STRH is active. The RDYL signal is active when the Port 0 input register is empty and is ready to accept data. from the peripheral device.

PROCESSOR ARCHITECTURE

The MK68200 microcomputer contains an advanced processor architecture, combining the best properties of both 8- and 16-bit processors. Thus a large majority of instructions operate on either byte or word operands. A block diagram shown in Figure 5 summarizes the internal architecture of the MK68200.

REGISTERS

The MK68200 register set includes three system registers, six address registers, and eight data registers. The three 16-bit system registers, as shown in Figure 6, include a Program Counter, a Status Register, and a Stack Pointer. The six address registers may be used either for 16-bit data or for memory addressing. The eight 16-bit data registers are used for data and may also be referenced as sixteen 8-bit registers, providing great flexibility in register allocation.

ADDRESSING

The MK68200 directly addresses a 64K byte memory space, which is organized as 32K 16-bit words. The memory is byte-addressable, but most transfers occur 16 bits at a time for increased performance over 8-bit microcomputers. All input/output is memory-mapped, and the on-chip I/O is situated in the top 1K bytes of the address space. In the single-chip mode, all resources including ROM, RAM, and I/O, are accessed via an internal or private bus. The memory map, which is accessed by this bus in the single-chip mode, is depicted in Figure 7.

Nine addressing modes provide ease of access to data in the MK68200, as depicted in Table 2. The four register indirect forms utilize the address registers and the Stack Pointer and support many common data structures such as arrays, stacks, queues, and linked lists. I/O Port addressing is a short form addressing mode for the first 16 words of the I/O port space and allows most instructions to access the most often referenced I/O ports in just one word. Many microcomputer applications are I/O intensive and short, fast addressing of I/O has a significant impact on performance.

INSTRUCTION SET

The MK68200 instruction set has been designed with regularity and ease of programming in mind. In addition, instructions have been encoded to minimize code space, a feature which is especially important in single-chip microcomputers. Small code space is related to execution speed, and most instructions execute in either three or six instruction clock periods. (An instruction clock period is equal to 167 ns with a 6 MHz instruction clock). See Table 3.

In addition to operations on bytes and words, the MK68200 has rapid bit manipulation instructions that can operate on registers, memory, and ports. The bit to be affected may be an immediate operand of the instruction, or it may be dynamically specified in a register. Operations available include bit set, clear, test, change, and exchange; and all bit operations perform a bit test as well. Since each instruction is indivisible, this provides the necessary test-and-set function for the implementation of semaphores.

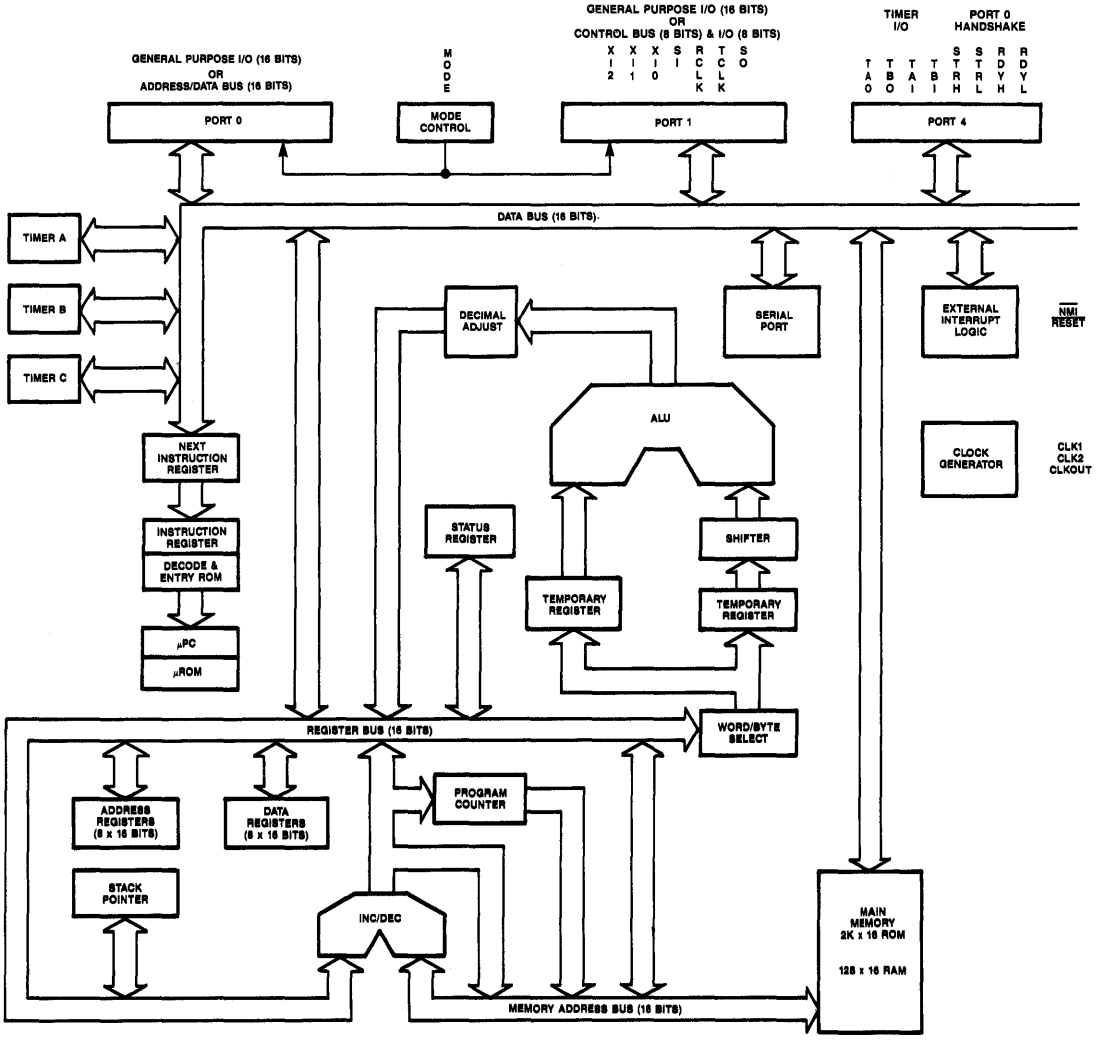
The MOVE group of instructions has the most extensive capabilities. A wide variety of addressing mode combinations is supported including memory-to-memory transfers. A special move multiple is included to save and restore a specified portion of the registers rapidly.

In total, the MK68200 instruction set provides a programming environment, similar to the 68000, which has been optimized for the needs of the single-chip microcomputer marketplace. A summary of the instruction set is provided in Table 4.

ADDRESSING MODES
Table 2

Register
Register Indirect
Register Indirect with Post-increment
Register Indirect with Pre-decrement
Register Indirect with Displacement
Program Counter Relative
Memory Absolute
Immediate
I/O Port

MK68200 BLOCK DIAGRAM
Figure 5

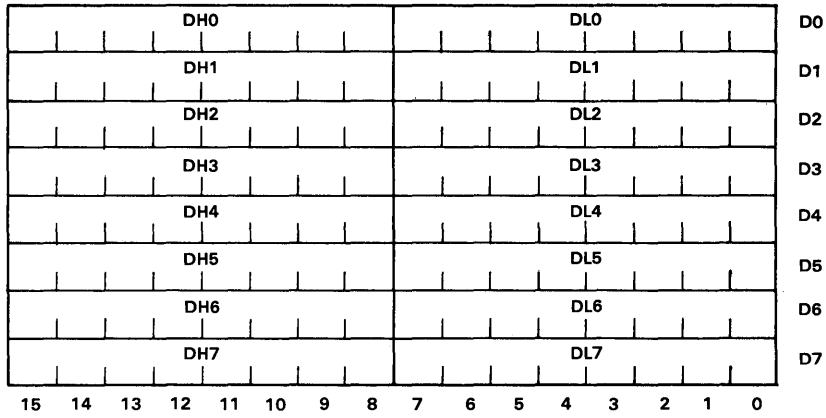


VI

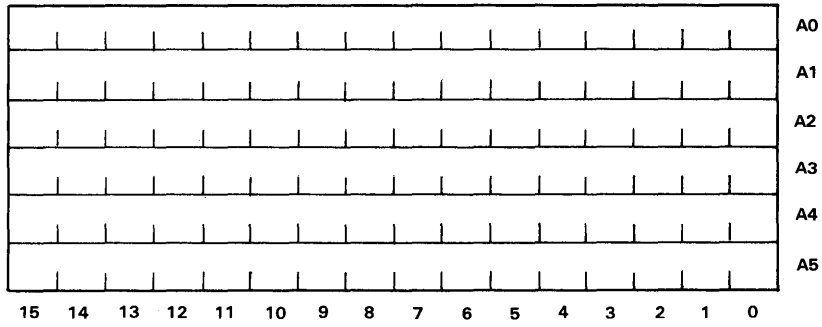
REGISTER SET

Figure 6

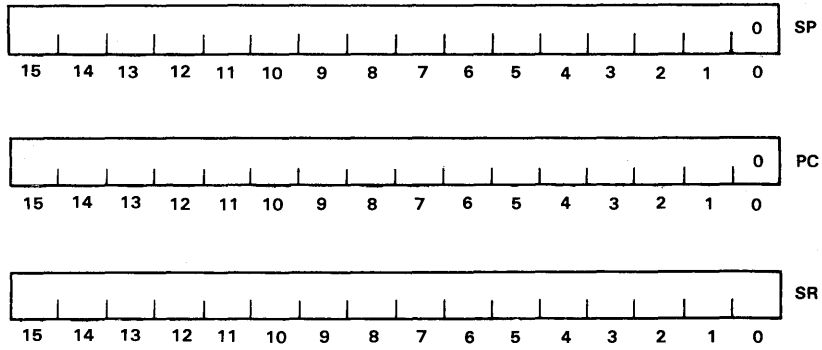
DATA REGISTERS:



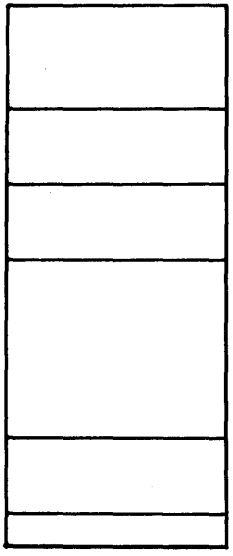
ADDRESS REGISTERS:



SYSTEM REGISTERS:



ADDRESSING SPACE FOR SINGLE-CHIP CONFIGURATION
Figure 7



VI

INSTRUCTION EXECUTION TIMES
Table 3

Instruction Type	Clock Periods	Execution Time with 6 MHz clock (μs)
Move Register-to-register	3	0.5
Add Register-to-register (binary or BCD)	3	0.5
Move Memory-to-register	6	1.0
Add Register-to-memory	9	1.5
Multiply (16 x 16)	21	3.5
Divide (32/16)	23	3.84
Move Multiple (save or restore all registers)	55	9.2

INSTRUCTION SET SUMMARY

Table 4

INST.	DESCRIPTION	INST.	DESCRIPTION
ADD	ADD	HALT	HALT
ADD.B	ADD BYTE	JMPA	JUMP ABSOLUTE
ADDC	ADD WITH CARRY	JMPR	JUMP RELATIVE
ADDC.B	ADD WITH CARRY BYTE	LIBA	LOAD INDEXED BYTE ADDRESS
AND	LOGICAL AND	LIWA	LOAD INDEXED WORD ADDRESSED
AND.B	LOGICAL AND BYTE	LSR	LOGICAL SHIFT RIGHT
ASL	ARITHMETIC SHIFT LEFT	LSR.B	LOGICAL SHIFT RIGHT BYTE
ASL.B	ARITHMETIC SHIFT LEFT BYTE	MOVE	MOVE
ASR	ARITHMETIC SHIFT RIGHT	MOVE.B	MOVE BYTE
ASR.B	ARITHMETIC SHIFT RIGHT BYTE	MOVEM	MOVE MULTIPLE REGISTERS
BCHG	BIT CHANGE	MOVEM.B	MOVE MULTIPLE REGISTERS BYTE
BCLR	BIT CLEAR	MULS	MULTIPLY SIGNED
BEXG	BIT EXCHANGE	MULU	MULTIPLY UNSIGNED
BSET	BIT SET	NEG	NEGATE
BTST	BIT TEST	NEG.B	NEGATE BYTE
CALLA	CALL ABSOLUTE	NEGC	NEGATE WITH CARRY
CALLR	CALL RELATIVE	NEGC.B	NEGATE WITH CARRY BYTE
CLR	CLEAR	NOP	NO OPERATION
CLR.B	CLEAR BYTE	NOT	ONE'S COMPLEMENT
CMP	COMPARE	NOT.B	ONE'S COMPLEMENT BYTE
CMP.B	COMPARE BYTE	OR	LOGICAL OR
DADD	DECIMAL ADD	OR.B	LOGICAL OR BYTE
DADD.B	DECIMAL ADD BYTE	POP	POP
DADDC	DECIMAL ADD WITH CARRY	POPM	POP MULTIPLE REGISTERS
DADDC.B	DECIMAL ADD WITH CARRY BYTE	PUSH	PUSH
DI	DISABLE INTERRUPTS	PUSHM	PUSH MULTIPLE REGISTERS
DIVU	DIVIDE UNSIGNED	RET	RETURN FROM SUBROUTINE
DJNZ	DECREMENT COUNT AND JUMP IF NON-ZERO	RETI	RETURN FROM INTERRUPT
		ROL	ROTATE LEFT
DJNZ.B	DECREMENT COUNT BYTE AND JUMP IF NON-ZERO	ROL.B	ROTATE LEFT BYTE
		ROLC	ROTATE LEFT THROUGH CARRY
DNEG	DECIMAL NEGATE	ROLC.B	ROTATE LEFT THROUGH CARRY BYTE
DNEG.B	DECIMAL NEGATE BYTE		
DNEGC	DECIMAL NEGATE WITH CARRY	ROR	ROTATE BYTE
DNEGC.B	DECIMAL NEGATE WITH CARRY BYTE	ROR.B	ROTATE RIGHT BYTE
		RORC	ROTATE RIGHT THROUGH CARRY
DSUB	DECIMAL SUBTRACT	RORC.B	ROTATE RIGHT THROUGH CARRY BYTE
DSUB.B	DECIMAL SUBRTRACT BYTE		
DSUBC	DECIMAL SUBTRACT WITH CARRY	SUB	SUBTRACT
DSUBC.B	DECIMAL SUBTRACT WITH CARRY BYTE	SUB.B	SUBTRACT BYTE
		SUBC	SUBTRACT WITH CARRY
EI	ENABLE INTERRUPTS	SUBC.B	SUBTRACT WITH CARRY BYTE
EOR	EXCLUSIVE OR	TEST	TEST
EOR.B	EXCLUSIVE OR BYTE	TEST.B	TEST BYTE
EXG	EXCHANGE	TESTN	TEST NOT
EXG.B	EXCHANGE BYTE	TESTN.B	TEST NOT BYTE
EXT	EXTEND SIGN		

INPUT/OUTPUT ARCHITECTURE

The I/O capabilities of the MK68200 are extensive, encompassing timers, a serial channel, parallel I/O, and an interrupt controller. All of these devices are accessible to the programmer as ports within the top 1K bytes of the address space, and the most commonly accessed ports may be accessed with the short port addressing mode. A description of these ports is given in Table 5.

In total, 40 pins out of the 48 are used for I/O, and the functions they perform are highly programmable by the user. In particular, many pins can perform multiple functions, and the programmer selects which ones are to be used. For example, TAI may be used as an input for Timer A, an interrupt source, or a general purpose input pin, and the interrupt source may be selected simultaneously with either of the other functions.

PORT DESCRIPTIONS

Table 5

PORT	ADDRESS	READ/WRITE	BYTE-ADDRESSABLE	FUNCTION
0	$FC00	READ/WRITE	YES	16 EXTERNAL I/O PINS OR ADDRESS/DATA BUS
1	$FC02	READ/WRITE	YES	16 EXTERNAL I/O PINS (INCLUDING INTERRUPT, SERIAL I/O PINS, AND BUS CONTROL)
2	$FC04	—	—	(RESERVED)
3	$FC06	LOW BYTE: READ/WRITE HIGH BYTE: READ	YES	SERIAL TRANSMIT (LOW BYTE) AND RECEIVE (HIGH BYTE) BUFFER
4	$FC08	INPUTS: READ ONLY OUTPUTS: READ/WRITE	NO	8 EXTERNAL I/O PINS (TIMER CONTROL AND PORT 0 HANDSHAKE CONTROL)
5	$FC0A	—	—	(RESERVED)
6	$FC0C	—	—	(RESERVED)
7	$FC0E	READ/WRITE	NO	INTERRUPT LATCH REGISTER
8	$FC10	READ/WRITE	NO	INTERRUPT MASK REGISTER
9	$FC12	STATUS: READ ONLY CONTROL: READ/WRITE	NO	SERIAL I/O RECEIVE CONTROL AND STATUS
10	$FC14	STATUS: READ ONLY CONTROL: READ/WRITE	NO	SERIAL I/O TRANSMIT CONTROL AND STATUS
11	$FC16	READ GETS COUNTER WRITE GOES TO LATCH	NO	TIMER B LATCH
12	$FC18	READ GETS COUNTER OR LATCH WRITE GOES TO LATCH	NO	TIMER A, LOW LATCH
13	$FC1A	READ GETS COUNTER OR LATCH WRITE GOES TO LATCH	NO	TIMER A, HIGH LATCH
14	$FC1C	READ/WRITE	NO	TIMER CONTROL, INTERRUPT EDGE SELECT
15	$FC1E	READ/WRITE	NO	PORT 0 HANDSHAKE MODE BITS, FAST/STANDARD, BUS LOCK, BUS SEGMENT BITS
16	$FC20	READ/WRITE	NO	PORT 0 DIRECTION CONTROL (DDR0)
17	$FC22	READ/WRITE	NO	PORT 1 DIRECTION CONTROL (DDR1)
18	$FC24	READ/WRITE	NO	SERIAL I/O MODE AND SYNC REGISTER
19	$FC26	READ GETS COUNTER WRITE GOES TO LATCH AND COUNTER	NO	TIMER C LATCH

TIMERS

The MK68200 includes three on-chip timers, each with unique features. They are denoted Timer A, Timer B, and Timer C. All three timers are a full 16 bits in width, and count at the instruction clock rate of the MK68200 processor. Thus, this rate provides a resolution equal to the instruction clock period (tc) of the MK68200. The maximum count interval is equal to tc $*2^{16}$. For a 6 MHz MK68200, a 167 nanosecond clock is provided with a maximum count interval of 10.945 milliseconds. Each timer has the capability to interrupt the processor when it matches a predetermined value stored in an associated latch.

Timer A is capable of operating in interval, event, and two pulse/period modes. There is one 16-bit counter and two 16-bit latches (high and low) associated with Timer A. Once Timer A is initialized in the interval mode, the counter is reset, and then it increments at the instruction clock rate until the value loaded into the high latch is reached. The counter is then reset, and it increments until the low latch value is reached, and the cycle is repeated. In the event mode, the counter is incremented for every active edge on TAI (programmable as positive or negative) until the value in the high latch is reached, at which time the counter is reset, and the cycle repeats. In the pulse/period modes, the time that the pulse applied stays high and low is measured. The counter is reset on the occurrence of any transition on TAI, and it increments at the instruction clock rate until occurrence of the next transition. The value in the counter at the end of the high level or low level time is loaded into the appropriate latch. Interrupts may be generated each time the counter reaches the high latch or low latch value in the interval mode or when the counter reaches the high latch in the event mode. An interrupt is also generated whenever the counter overflows. See the Pin Description section of this data sheet for TAI and TAO functions in the various Timer A modes.

Timer B is capable of operating in interval and one-shot modes. There is one 16-bit counter and one 16-bit latch associated with Timer B. In the interval mode, the counter is initially reset and incremented at the instruction clock rate until the value in the latch is reached. The counter is then reset, and the cycle repeats. In the one-shot modes, the counter begins incrementing in response to an active transition (programmable as positive or negative) on TBI. The counter is reset when the value in the Timer B latch is reached. In the retriggerable one-shot mode, active transitions on TBI always cause the counter to reset and begin incrementing. In the non-retriggerable one-shot mode, active transitions on TBI have no effect until the counter reaches the latch value. Interrupts may be generated each time the counter reaches the latch value. See the Pin Description section of this data sheet for TBI and TBO functions in the various Timer B modes.

Timer C has a 16-bit down counter and latch associated with it and operates only in the interval mode. The output of Timer C toggles each time the counter value rolls over from 0 to the latch value and may be used to internally supply the baud rate clock for the serial port. An interrupt may also be generated each time the counter rolls over to the latch value. Timer C may be output on the TCLK pin (P1-3) depending on the mode programmed.

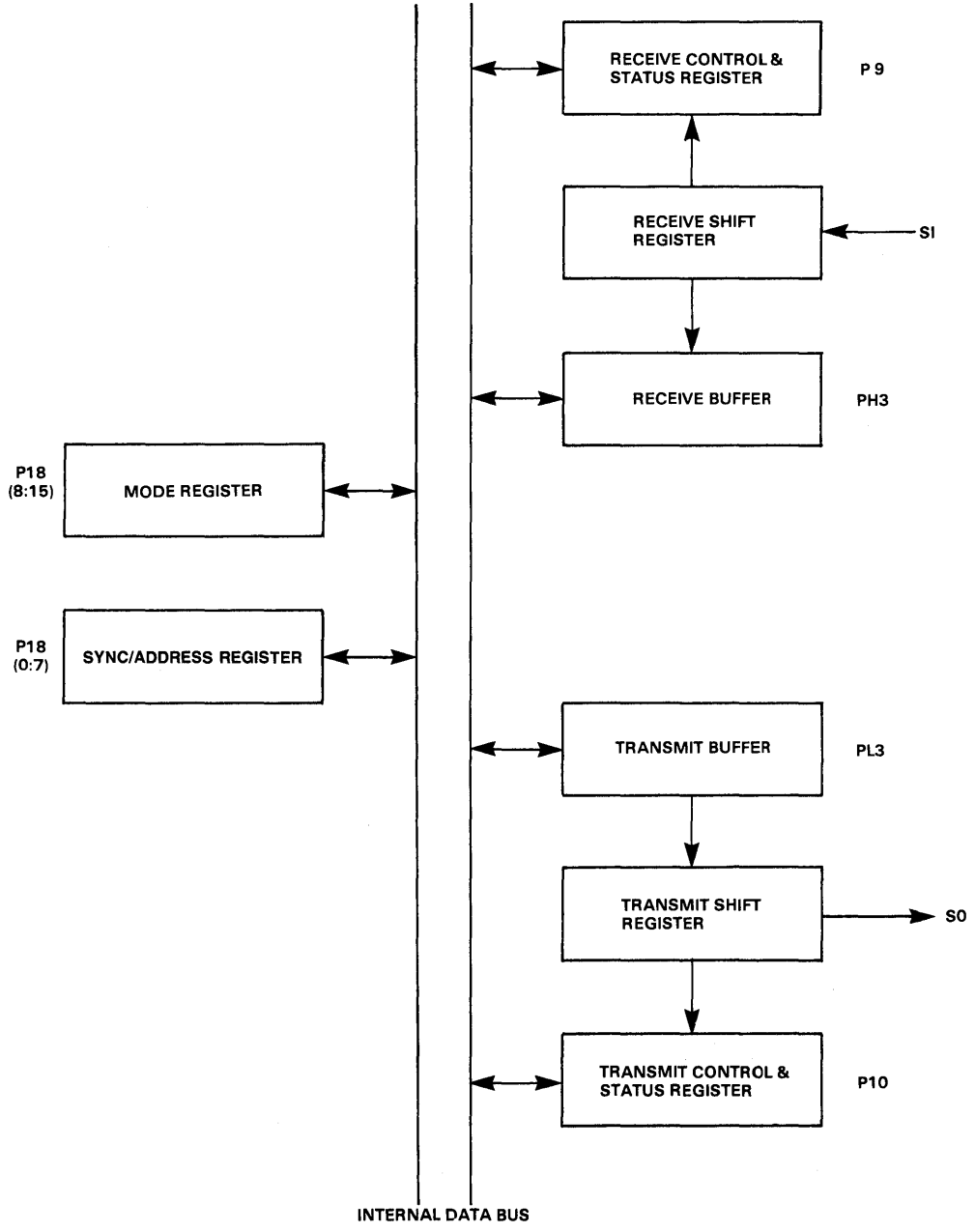
TIMER MODES
Table 6

Timer	Modes
A	Interval
A	Event
A	Pulse Width and Period Measurement
B	Interval
B	Retriggerable One-shot
B	Non-retriggerable One-shot
C	Interval
C	Baud Rate Generation

SERIAL CHANNEL

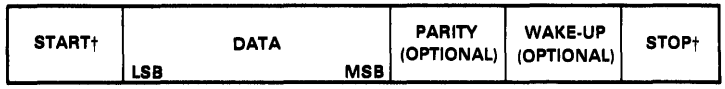
The serial channel on the MK68200, as shown in Figure 8, is a full-duplex USART with double buffering on both transmit and receive. Word length, parity, stop bits, and modes are fully programmable. The asynchronous mode supports bit rates up to 375 Kbps, and the byte synchronous mode operates up to 1.5 Mbps. Either internal or external clocks may be used.

SERIAL CHANNEL
Figure 8



In addition to the typical USART functions, the serial channel can operate in a special wake-up mode with a wake-up bit appended to each data word, as illustrated in Figure 9. This wake-up bit is used to differentiate normal data words and special address words. The receiver can be programmed to receive only address words or only address words with a specific data value. In this way, the processor can be interrupted only when it receives its particular address and can then change mode to receive the following data words. Wake-up capability is especially useful when several MK68200 microcomputers are interconnected on one serial link.

SERIAL FRAME FORMAT
Figure 9



†USED IN ASYNCHRONOUS MODE ONLY

PARALLEL I/O

Two 16-bit ports, P0 and P1, may be used for parallel I/O. If individual bits are desired, each of the 32 bits may be separately defined as input or output. Bits may be grouped to provide the exact data widths desired. Port 0 has the additional capability of operating under the control of external handshaking signals. Eight- or sixteen-bit sections of P0 may be individually controlled as input, output, or bidirectional I/O. Two pairs of Ready and Strobe signals, which are available as programmable options on Port 4, provide the necessary control.

INTERRUPT CONTROLLER

The MK68200 interrupt controller provides rapid service of up to 15 interrupt sources, each with a unique internal vector. The lowest 16 words of the address space contain the starting addresses of the service routines of each potential interrupt source and reset, as shown in Figure 10.

INTERRUPT AND RESET VECTORS
Figure 10

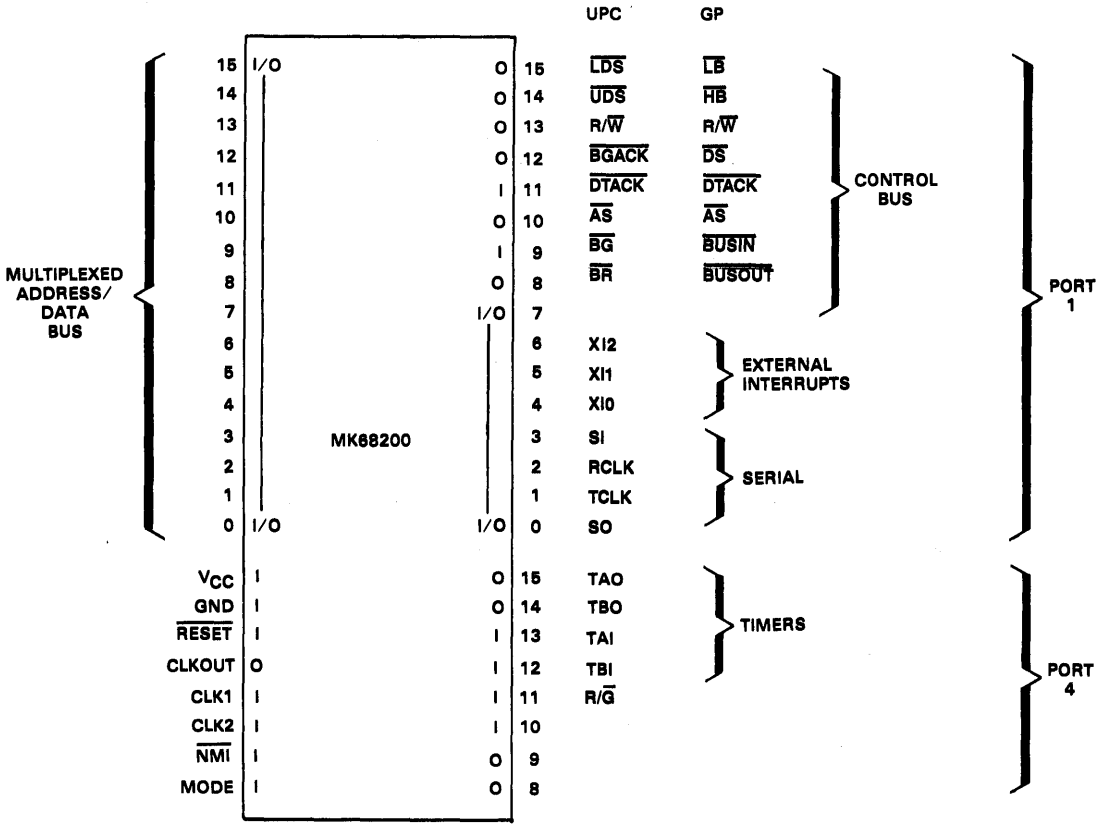
VECTOR NUMBER	NAME	MNEMONIC	VECTOR LOCATION	
0	RESET	RESET	0000	
1	NON-MASKABLE INTERRUPT	NMI	0002	LEVEL 2
2	SPARE	SPARE	0004	
3	EXTERNAL INTERRUPT 2	XI2	0006	
4	STROBE LOW	STRL	0008	
5	TIMER A OUTPUT	TAO	000A	
6	TIMER A INPUT	TAI	000C	
7	STROBE HIGH	STRH	000E	
8	RECEIVE SPECIAL CONDITION	RSC	0010	LEVEL 1
9	RECEIVE NORMAL	RN	0012	
A	EXTERNAL INTERRUPT 1	XI1	0014	
B	TIMER B OUTPUT	TBO	0016	
C	TIMER B INPUT	TBI	0018	
D	EXTERNAL INTERRUPT 0	XI0	001A	
E	TRANSMIT	XMT	001C	
F	TIMER C	TC	001E	

Interrupt sources and RESET are prioritized in the order shown in Figure 10, with RESET having the highest priority. NMI is the only non-maskable interrupt. All of the other sources share an interrupt enable bit in the processor Status Register. This bit is automatically cleared whenever an interrupt is acknowledged. Also, each of these sources has a corresponding individual mask bit. This feature allows selective masking of particular interrupts, including the ability to choose any priority scheme desired with only minimal software overhead. In fact, 15 levels of nested priority may be programmed.

EXPANDED BUS OPERATION

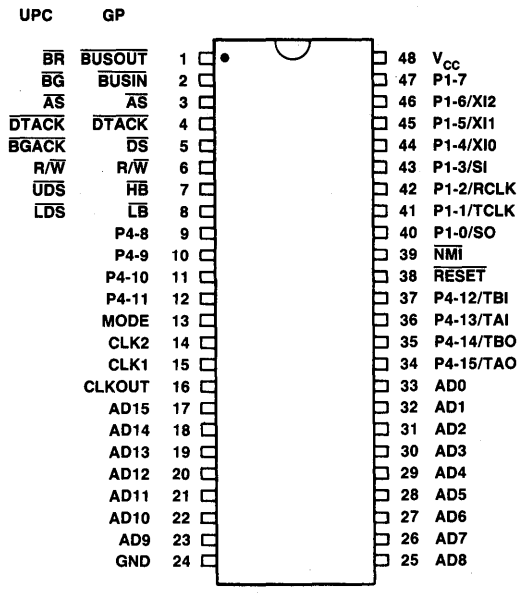
When it is necessary to expand beyond the on-chip complement of RAM, ROM, or I/O, or when operation in a parallel multiprocessing system is desired, the MK68200 may be placed in an external bus mode. The MODE pin is used to select the expansion capability on reset. The MODE pin has three states, which select fully expanded external bus, partially expanded external bus, or no expanded bus (single-chip configuration). The MK68200 may also be reconfigured dynamically through software. In an expansion mode, Port 0 becomes the 16-bit multiplexed, address/data bus, and eight bits from Port 1 become control signals which handle data transfer and bus arbitration. Sixteen lines are still available for I/O functions, including eight lines from Port 1 and all eight lines of Port 4.

MK68200 LOGICAL PINOUT EXPANDED BUS
Figure 11



MK68200 EXPANDED BUS

Figure 12

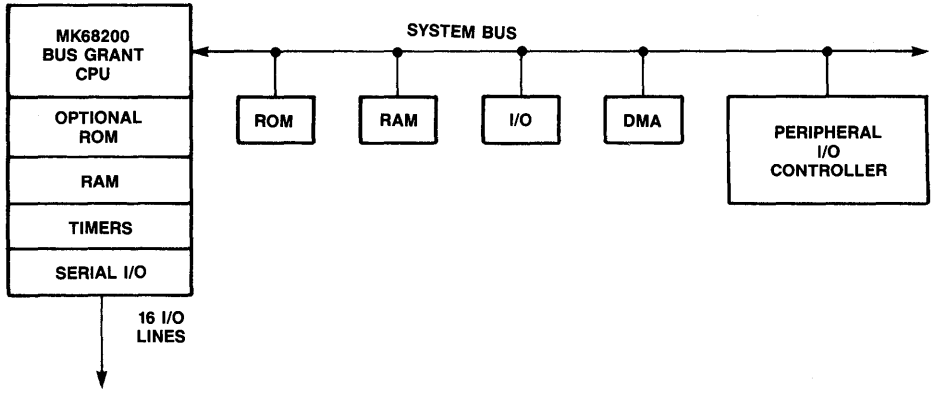


As shown in Figure 11, two different control bus versions are available : a Universal Peripheral Controller (UPC), which generates 68000-compatible signals, and a General Purpose (GP) bus, which can be used to interface to a wide variety of existing microprocessor buses. With the selection of an expanded bus mode, the MK68200 can act either as a general purpose CPU chip (bus grant device) or as an intelligent peripheral I/O controller to a host CPU (bus request device). These two system configurations are illustrated in Figures 13 and 14.

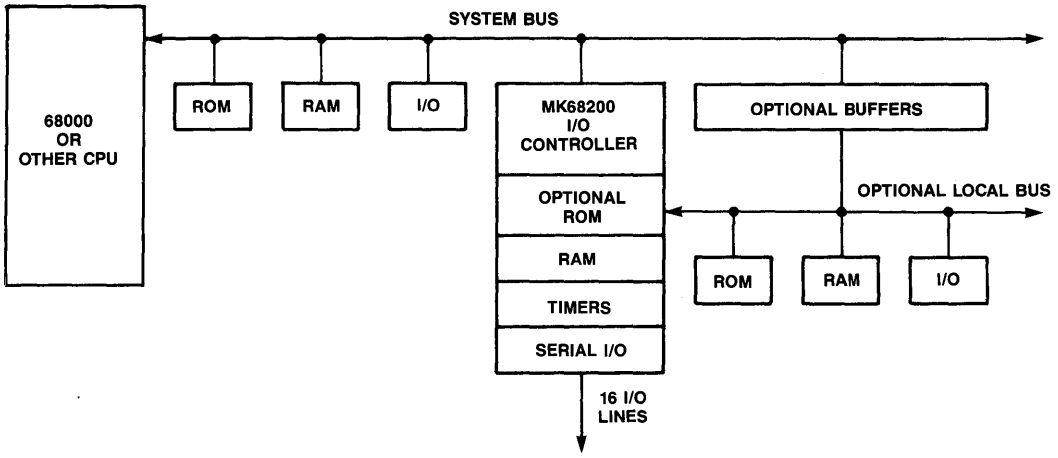
With the GP bus option, the user may configure the MK68200 in either of the two ways shown in Figures 13 and 14. As a host CPU (Figure 13), the MK68200 bus arbitration logic causes the device to act as the system bus grantor. In other words, the MK68200 would normally have control of the system bus and would grant its use to DMA devices or peripheral CPUs. Alternately, the MK68200 may be configured as a peripheral CPU (Figure 14) that must issue a request to the bus grant device before being allowed to use the system bus. The selection of one of these two configurations is accomplished by the P4-11 pin at reset time. During reset, P4-11 serves as the R/$\overline{G}$ input (0 = bus grantor, 1 = bus requestor). Following reset and at all times during program execution, P4-11 may be used as a general purpose input pin.

HOST CPU HARDWARE CONFIGURATION

Figure 13



PERIPHERAL I/O CONTROLLER CONFIGURATION
Figure 14

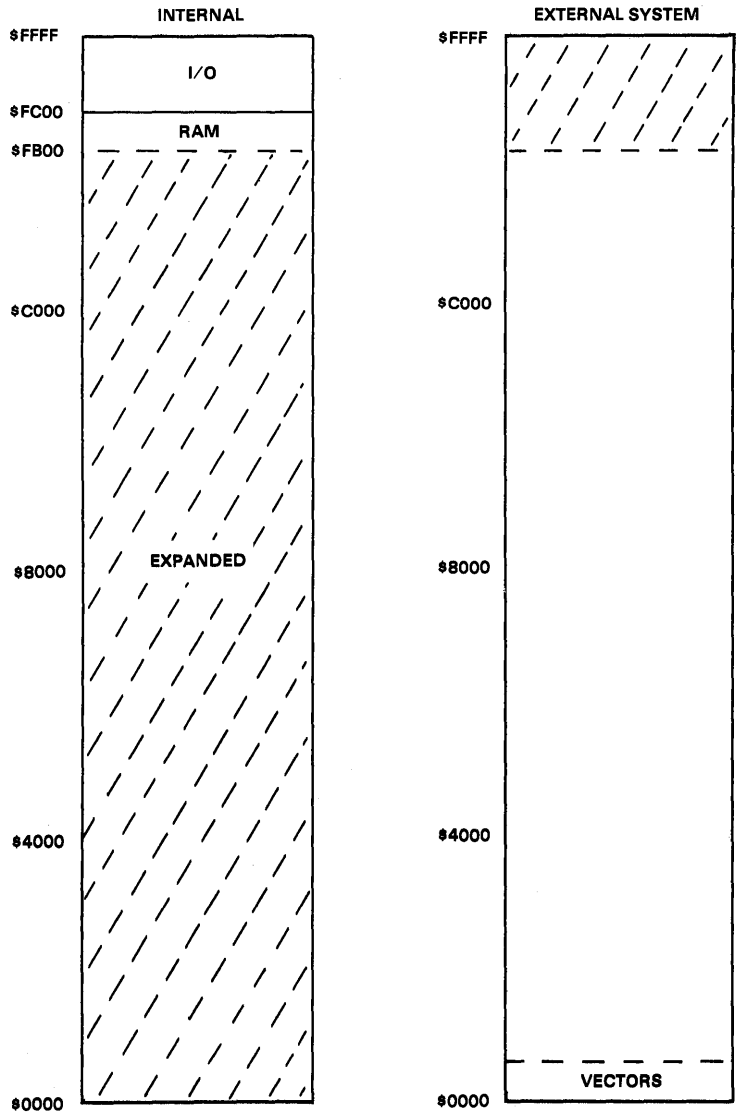


With the GP bus operating in the host CPU configuration, the MK68200 may be used to interface with external memory and I/O devices in a manner that is analogous to any general purpose microprocessor. Additionally, the MK68200 retains its on-chip RAM and I/O resources, with on-chip ROM as an option, depending on the expansion configuration selected. $\overline{\text{BUSIN}}$ and $\overline{\text{BUSOUT}}$ are used to perform the bus arbitration handshake function, where $\overline{\text{BUSIN}}$ acts as the bus request input and $\overline{\text{BUSOUT}}$ as the bus grant output.

In the full expansion configuration, any on-chip ROM which may exist on the device is disabled, and program memory starting at location $0000 is located off-chip and is addressed via the expanded bus, as shown in Figure 15. In effect, the internal bus from locations $0000-$FAFF is mapped onto the external bus. In the partially expanded configuration (Figure 16), on-chip ROM may be accessed on the internal bus. To gain greater addressability in the partial expansion configuration, a scheme is implemented to allow access of a full 64K-byte address space in four segments on the expanded system bus through the 16K byte "window" on the internal bus. Basically, the most significant two bits of address on the expanded bus are replaced with two user-defined segment bits available to the programmer in an internal I/O control port location.

As a peripheral I/O controller, the MK68200 operates as a bus requestor that gains mastership of the system bus from the bus grant CPU. The GP bus version may be selected to implement this system configuration in cases where an interface to a general purpose CPU is desired. In this case, the $\overline{\text{BUSIN}}$ and $\overline{\text{BUSOUT}}$ lines are again used to perform the bus arbitration handshake function, where $\overline{\text{BUSOUT}}$ now acts as bus request output, and $\overline{\text{BUSIN}}$ acts as bus grant input. In this configuration, the MK68200 can conceivably act as a complete peripheral I/O control subsystem on a single chip, with 16 lines of I/O and its on-chip ROM, RAM, timers, and serial I/O performing the necessary interface to the I/O device. The UPC bus version provides the peripheral I/O control function with a direct interface to a 68000 bus grant CPU. Note that the UPC bus version can operate only as a bus request device. Once the MK68200 has gained mastership of the system bus via the 68000 bus arbitration handshake lines ($\overline{\text{BR}}$, $\overline{\text{BG}}$, and $\overline{\text{BGACK}}$), it may proceed to perform DMA transfers and communicate with system memory or other I/O devices in the system.

FULL EXPANSION BUS GRANTOR MEMORY MAP
Figure 15



As in the case of the GP bus grant configuration, the portion of the internal (or private) bus address space that is mapped onto the expanded bus when the part is operating as either a GP or a UPC bus request device is determined by the expansion configuration selected. In the partial expansion bus requestor case, the resulting memory map is identical to that shown for the GP grant configuration in Figure 16. During the time the MK68200 is executing its program from ROM and accessing internal RAM and I/O resources, the expanded bus is held in a tri-state condition. The bus arbitration logic within the MK68200 monitors each memory reference to detect external bus addresses (referenced in segments via the 16K byte DMA window). Whenever such an external reference occurs, the logic automatically holds the processor in a wait state as it proceeds to obtain mastership of the bus. As soon as use of the system bus is obtained, the processor is allowed to continue the reference. This procedure is transparent to the programmer. In the case of successive external references, the expanded bus is retained until an internal reference is encountered.

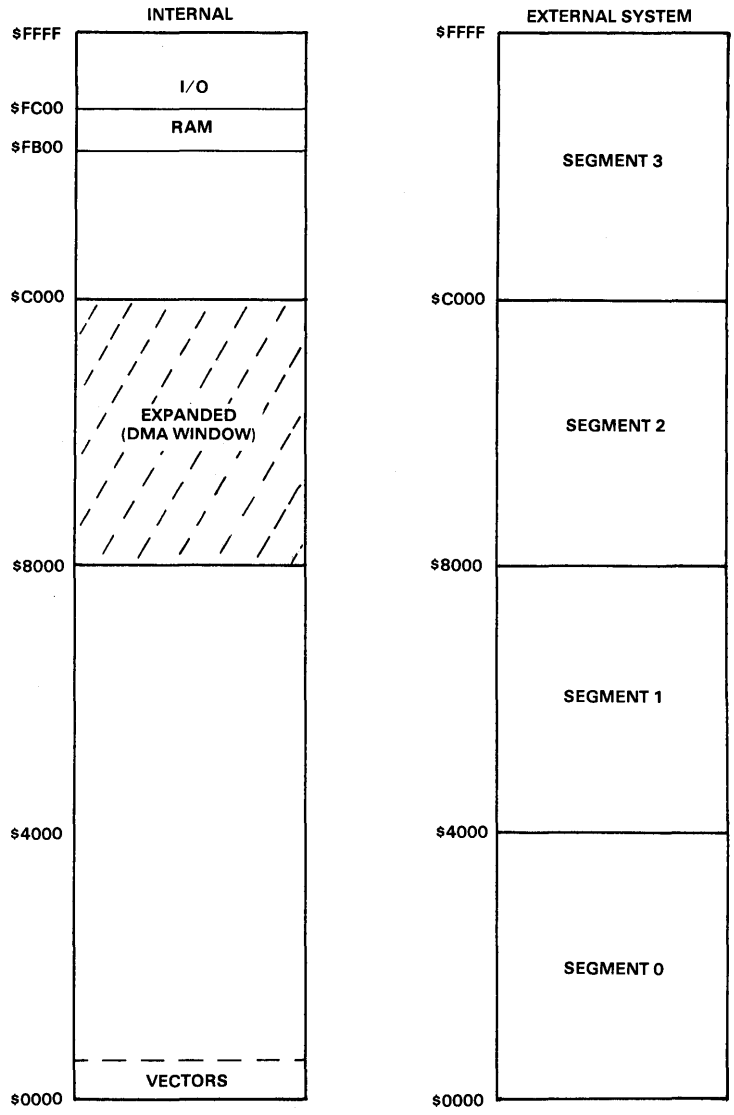
Finally, if the on-chip resources are insufficient to perform the control task in the bus requestor configuration, the internal bus address range (excluding on-chip RAM, I/O) may be mapped onto an external local bus, which is physically the same as the system bus but logically separated with bus buffers. This is the full expansion bus requestor configuration. The memory map for this configuration is shown in Figure 17. The bus arbitration sequence is still performed only when a reference to the system bus through the DMA window is made. In this manner, the I/O subsystem is isolated from the host CPU.

When operating as a bus request device, it is possible to retain the external bus for an indefinite period of time using a bus lock feature. This will help facilitate the transfer of large blocks of data. Thus, the on-chip bus arbitration logic allows a maximum amount of concurrent processing in parallel, multiprocessing configurations with a minimum of hardware and software overhead. The bus lock feature may be used by the MK68200 in a bus grantor mode to keep any peripheral from gaining mastership of the bus.

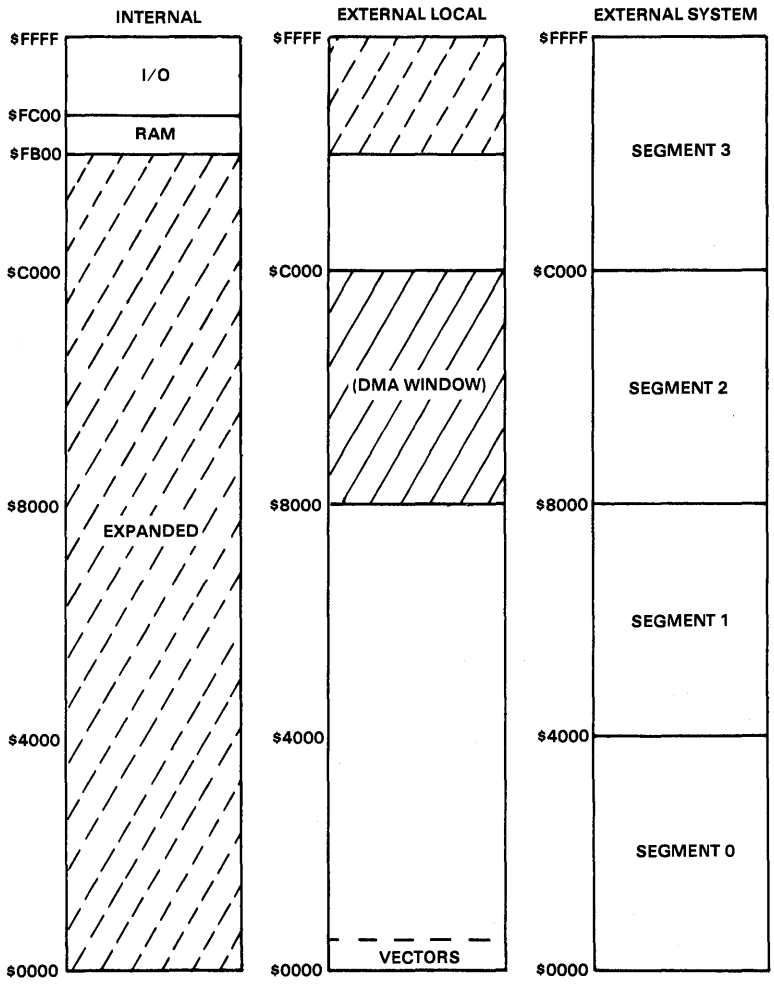
In any of the GP expanded bus modes, the MK68200 may respond to peripheral devices on the expanded bus which generate an interrupt request on XI0. The MK68200 will obtain the XI0 interrupt vector number from the requesting peripheral on the bus during an interrupt acknowledge cycle. When responding to an interrupt on XI0, the MK68200 will wait for the bus arbitration logic to gain control of the bus and then asserts neither $\overline{HB}$ nor $\overline{LB}$ while asserting $\overline{AS}$ to signify that an interrupt acknowledge cycle is in progress.

Timing diagrams and design parameters for the read, write, and bus arbitration cycles are given in the AC Electrical Specifications section for both the GP and the UPC bus options. Bus timing for the interrupt acknowledge cycle is given for the GP device in the AC Electrical Specifications section. There is a user-programmable speed selection associated with the read and write cycles for both the UPC and GP mask option parts. A bit in an internal I/O port allows the user to select either the standard or the fast read/write cycle on the expanded bus. The standard bus cycle is four clock periods, while the fast bus cycle is three clock periods.

PARTIAL EXPANSION MEMORY MAP
Figure 16



FULL EXPANSION BUS REQUESTOR MEMORY MAP
Figure 17



VI

EXPANDED BUS SIGNALS (Common for GP and UPC Options)

R/$\overline{W}$
(Read/Write)
Output, active high and low. R/$\overline{W}$ determines whether a read or a write is being performed during the current bus cycle. It is stable for the entire bus operation. A high signal denotes a read, and a low signal denotes a write.

$\overline{DTACK}$
(Data Transfer Acknowledge)
Input, active low. When the addressed device has either placed the requested read data on the bus or taken the write data from the bus, $\overline{DTACK}$ should be brought low to signify completion. The data portion of the bus cycle will be extended indefinitely until this signal is asserted. For systems using the GP bus, in which no devices need wait states, $\overline{DTACK}$ may be strapped low.

$\overline{AS}$
(Address Strobe)
Output, active low. $\overline{AS}$ is used to signify that the address is stable on the multiplexed bus. $\overline{AS}$ is high at the beginning of each bus cycle and goes low after the address has stabilized. It then returns to the high state near the end of the bus cycle.

UPC BUS SIGNALS

$\overline{UDS}$
(Upper Data Strobe)
Output, active low. $\overline{UDS}$ is used to signify the data portion of the bus cycle for the upper byte of the data bus. For read operations, $\overline{UDS}$ should be used by the external device to gate its most significant byte onto the multiplexed address/data bus. For writes, $\overline{UDS}$ signifies that the upper byte of the bus contains valid data to be written from the processor.

$\overline{LDS}$
(Lower Data Strobe)
Output, active low. $\overline{LDS}$ is used to signify the data portion of the bus cycle for the lower byte of the data bus. For read operations, $\overline{LDS}$ should be used by the external device to gate its least significant byte onto the multiplexed address/data bus. For writes, $\overline{LDS}$ signifies that the lower byte of the bus contains valid data to be written from the processor.

$\overline{BR}$
(Bus Request)
Output, active low, open drain. $\overline{BR}$ goes low when the MK68200 requires the use of the external bus as a bus master.

$\overline{BG}$
(Bus Grant)
Input, active low. $\overline{BG}$ notifies the MK68200 that it has been granted the external bus.

$\overline{BGACK}$
(Bus Grant Acknowledge)
Output, active low, open drain. The MK68200 will assert $\overline{BGACK}$ when it assumes mastership of the system bus.

GP BUS SIGNALS

P4-11 / R/$\overline{G}$
(Request/Grant)
During reset, P4-11 serves as the R/$\overline{G}$ input (0 = bus grantor, 1 = bus requestor). Following reset, and at all times during program execution, P4-11 may be used as a general purpose input pin.

$\overline{DS}$
(Data Strobe)
Output, active low. $\overline{DS}$ is used to signify the data portion of the bus cycle. For read operations, $\overline{DS}$ should be used by the external device to gate its contents onto the multiplexed address/data bus. For writes, $\overline{DS}$ signifies that valid data from the processor is on the bus.

$\overline{HB}$
(High Byte)
Output, active low. $\overline{HB}$ signifies that the upper byte of the data is to be read or written. It remains active for the entire bus cycle.

$\overline{LB}$
(Low Byte)
Output, active low. $\overline{LB}$ signifies that the lower byte of the data bus is to be read or written. (Both $\overline{HB}$ and $\overline{LB}$ active imply that an entire word is to be read or written). $\overline{LB}$ remains active for the entire bus cycle.

$\overline{BUSIN}$
(Bus Input)
Input, active low. $\overline{BUSIN}$ provides one of two functions: bus request or bus grant. When the MK68200 is the bus grant device, its $\overline{BUSIN}$ signal is a bus request input from a requesting device on the bus. When the MK68200 is a bus request device, its $\overline{BUSIN}$ signal is a bus grant from the granting device on the bus.

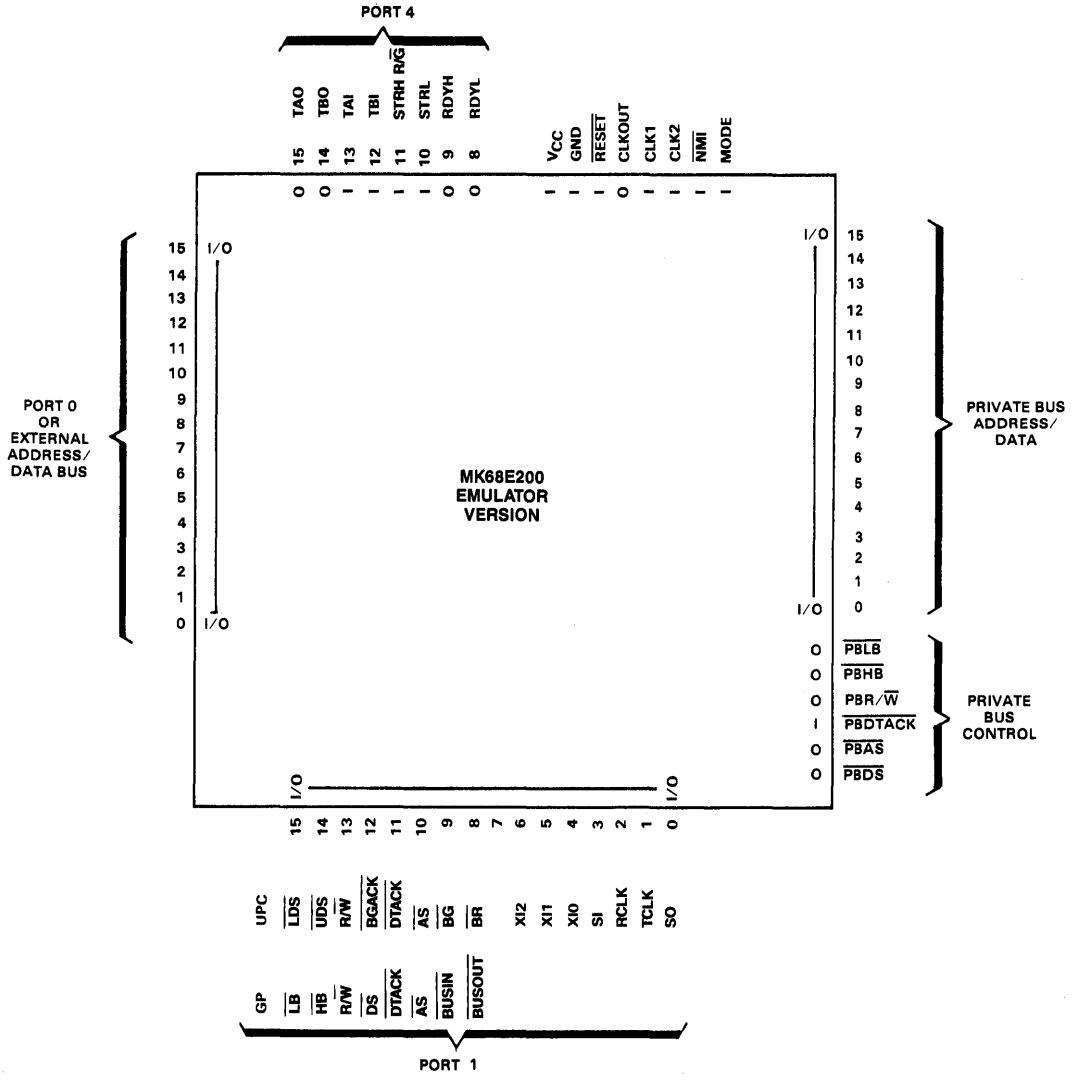
$\overline{BUSOUT}$
(Bus Output)
Output, active low. $\overline{BUSOUT}$ provides the opposite function of $\overline{BUSIN}$. When $\overline{BUSIN}$ is a bus request signal, $\overline{BUSOUT}$ is the corresponding bus grant, and vice versa.

EMULATOR VERSION

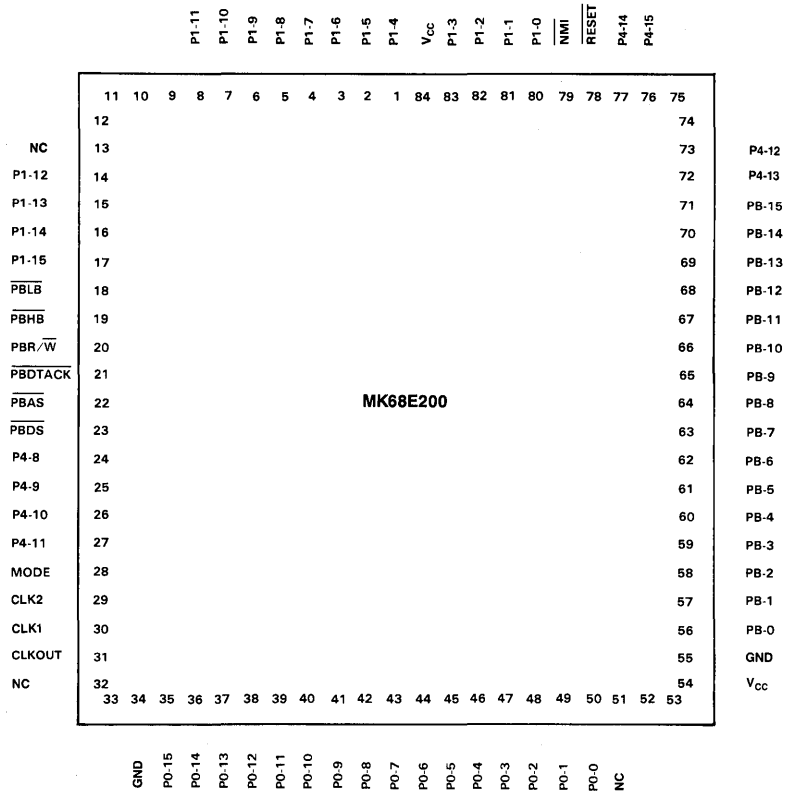
The emulator versions of the MK68200 are available in 84-pin, leadless chip carrier packages. Figure 18 illustrates the logical pinout of the emulator version. Table 1 summarizes the emulator parts described in this data sheet. The emulator versions have no on-chip ROM, but instead they include a second complete bus, referred to as the private bus. The private bus includes a multiplexed address/data bus as well as bus control signals. There are 22 pins associated with the private bus. All of the 40 I/O port pins that exist on the 48-pin versions are available to the user for configuration either as general purpose or special I/O pins, or as expanded bus pins.

MK68E200 LOGICAL PINOUT

Figure 18



MK68E200 PIN ASSIGNMENT (84-PIN LCC)
EMULATOR VERSION
Figure 19



PRIVATE BUS OPERATION

The address/data lines and control signals that constitute the private bus are functionally equivalent to the internal signals used to access internal resources on the 48-pin versions of the MK68200. Thus, the private bus may be used to interface EPROM memory in emulating mask ROM versions of the MK68200. Alternately, any combination of ROM, RAM, and I/O may reside on the private bus.

The address that is generated on the private bus is identical to that which is internally generated for 48-pin versions. When the part is used in a configuration that supports system bus addressing through the DMA window, any references in this region of the memory map produce an address on the private bus identical to that specified by the programmer. In other words, the segment bits have no effect on the private bus address. Write data appears on the private bus pins for all write operations, regardless of whether the reference is on-chip or off-chip. The MK68200 emulator version reads data from the private bus, unless data is read from on-chip RAM or I/O or from the external bus formed by the Port 0 and Port 1 I/O pins.

The I/O port range of the memory map ($FC00-$FFFF) is actually subdivided into space which is exclusively reserved for on-chip I/O ($FC00-$FDFF) and space which is exclusively reserved for in-circuit-emulator, or AIM, use ($FE00-$FFFF). The user should ensure that no external devices reside in the in-circuit-emulator area.

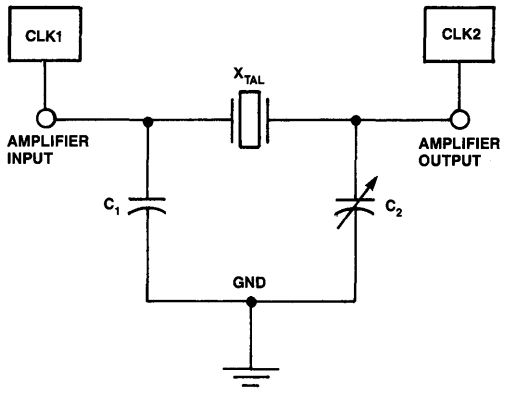
The private bus interface is the same as that for the GP expanded bus. All read/write transfers made exclusively on the private bus are three clock periods, regardless of the state of the Fast/Standard (F/S) bus timing selection bit. The user should ignore all activity on the private bus while accesses are in progress on the expanded bus. Care should also be taken that no external devices reside on the private bus in the memory space intended for expanded bus accesses. Note that there are three pins shown on the pin diagram of Figure 19 which are labeled "NC" and are not to be connected. They are reserved for use in future versions of the emulator device.

CRYSTAL SELECTION

The wide frequency range of crystals that can be chosen for the MK68200 offers the user a large degree of flexibility. To aid in the selection of a suitable crystal, the suggestions shown in Figure 20 should be considered by the user. The MK68200 offers an output pin that will provide a system clock signal at one-half of the crystal frequency.

VI

CRYSTAL CONNECTION
Figure 20



C_1 = 10 pf typical
C_2 = 20 pf typical

If it is desirable to "tune" the oscillator to a precise frequency, C_2 may be a variable capacitor.

C_2 should be in the range of $C_1 \leq C_2 \leq 2\ C_1$.

For a high frequency operation
$C_1 \approx 5 - 10$ pf.

SUMMARY OF CRYSTAL SPECIFICATIONS

Figure 21

FREQUENCY RANGE	SPECIFICATION
1 MHz - 12.0 MHz	PARALLEL RESONANCE FUNDAMENTAL MODE C_L = 20 pf to 40 pf AT CUT

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −.3 V to +7 V
Power Dissipation . . . . . 1.5 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MK68200 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, T_a = 0° to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input low voltage; all inputs	−0.3	0.8	V	
V_{IH}	Input high voltage; all inputs	2.0	V_{CC}	V	
V_{OL}	Output low voltage; all outputs		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output high voltage; all outputs	2.4		V	I_{OH} = −250μA
I_{CC}	Input power supply current		200	mA	
I_{LI}	Input leakage current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Tri-state output leakage current in float		±10	μA	V_{OUT} = 0.4 V to V_{CC}

CAPACITANCE

TA = 25°C, f = 12 MHz with unmeasured pins returned to ground.

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance	10	pf	Unmeasured pins returned to ground
C_{OUT}	Tri-state Output Capacitance	10	pf	

MK68200 AC ELECTRICAL SPECIFICATIONS

NO.	DESCRIPTION	4 MHz		6MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
1	$\overline{\text{RESET}}$ low time	20		20		state times	1
2	CLK 1 width high (external clock input)	45		30		ns	
3	CLK 1 width low (external clock input)	45		30		ns	
4	CLK 1 period (external clock input)	125	1000	83	1000	ns	
5	Crystal input frequency	1.000	8.000	1.000	12.000	MHz	
6	Clock Period (PHI 1)	250		167		ns	
7	PHI 1 low to PHI 1 high	125		83		ns	
8	PHI 1 high to PHI 1 low	125		83		ns	
9	PHI 1 low to CLKOUT low		40		27	ns	
10	PHI 1 high to CLKOUT high		40		27	ns	

VI

MK68200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (UPC, GP, AND PRIVATE BUSES)

NO.	DESCRIPTION	4MHz		6MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
11	PHI 1 low to R/$\overline{\text{W}}$, $\overline{\text{HB}}$, or $\overline{\text{LB}}$ valid		115		76	ns	2
12	PHI 1 high to $\overline{\text{AS}}$ low		115		76	ns	2
13	PHI 1 low to address valid		115		76	ns	2
14	$\overline{\text{AS}}$ low to address invalid	70		50		ns	2
15	PHI 1 low to tristate address		90		60	ns	2
16	Tristate address to $\overline{\text{DS}}$, $\overline{\text{LDS}}$, or $\overline{\text{UDS}}$ starting low (fast cycle)	10		10		ns	2
17	PHI 1 low to $\overline{\text{DS}}$, $\overline{\text{LDS}}$, or $\overline{\text{UDS}}$ low (fast cycle)		165		110	ns	2
18	PHI 1 low to data out valid during write		115		76	ns	2
19	PHI 1 low to R/$\overline{\text{W}}$, $\overline{\text{HB}}$, $\overline{\text{LB}}$ invalid	0		0		ns	2
20	PHI 1 low to address/data bus driven	0		0		ns	2
21	$\overline{\text{AS}}$ low to $\overline{\text{DS}}$, $\overline{\text{LDS}}$, or $\overline{\text{UDS}}$ starting low (fast cycle)	100	225	70	150	ns	2

MK68200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (UPC AND GP BUSES)

NO.	DESCRIPTION	4 MHz		6MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
22	Tristate address to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ starting low (standard cycle)	135		90		ns	
23	PHI 1 high to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ low (standard cycle)		165		110	ns	2
24	Valid Data Setup to PHI 1 low	10		5		ns	2
25	$\overline{AS}$ low to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ starting low (standard cycle)	225	350	150	230	ns	2
26	R/$\overline{W}$, $\overline{HB}$, or $\overline{LB}$ valid to $\overline{AS}$ starting low	60		60		ns	
27	Address valid to $\overline{AS}$ starting low	60		60		ns	
28	Input data hold time from PHI 1 low	45		30		ns	
29	Input data hold time from $\overline{DS}$, $\overline{LDS}$ or $\overline{UDS}$ high	0		0		ns	
30	PHI 1 low to $\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ high		180		120	ns	
31	$\overline{DTACK}$ low setup to PHI 1 high	15		10		ns	
32	$\overline{LDS}$, $\overline{UDS}$, or $\overline{DS}$ high to $\overline{DTACK}$ high (hold time)	−30		−30		ns	
33	$\overline{LDS}$, $\overline{UDS}$, or $\overline{DS}$ pulse width	240		150		ns	
34	PHI 1 high to $\overline{AS}$ high		90		60	ns	
35	PHI 1 low to data out invalid	0		0		ns	
36	$\overline{AS}$ inactive	235		150		ns	
37	$\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ high to data out invalid	180		110		ns	
38	$\overline{DS}$, $\overline{LDS}$, or $\overline{UDS}$ high to $\overline{AS}$ high	5		5		ns	

MK68200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (UPC BUS)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
39	$\overline{BGACK}$ low to $\overline{BR}$ high	100	450	100	300	ns	
40	$\overline{BG}$ low to $\overline{BGACK}$ low	50	600	50	400	ns	
41	$\overline{BGACK}$, $\overline{AS}$, $\overline{DTACK}$, inactive to $\overline{BGACK}$ low; $\overline{BG}$ already low	0	600	0	400	ns	
42	$\overline{BGACK}$ low to $\overline{AS}$, $\overline{UDS}$, $\overline{LDS}$, or address/data bus driven	40	135	40	90	ns	
43	$\overline{AS}$, $\overline{LDS}$, $\overline{UDS}$ or address/data bus tristate to $\overline{BGACK}$ high	0	180	0	120	ns	

MK68211 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (GP BUS)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
44	Tristate $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$ to $\overline{BUSOUT}$ low (bus grantor, fast cycle, no wait states)	175		100		ns	
45	$\overline{BUSIN}$ low to $\overline{BUSOUT}$ low (bus grantor, fast cycle, no wait states)		1900		1200	ns	
46	$\overline{BUSOUT}$ high to $\overline{AS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$ driven (bus grantor)	15		15		ns	
47	$\overline{BUSIN}$ high to $\overline{BUSOUT}$ high (bus grantor)	520	900	300	600	ns	
48	Tristate address/data bus to $\overline{BUSOUT}$ low (bus grantor)	70		70		ns	
49	$\overline{BUSOUT}$ high to address/data bus driven (bus grantor)	50		50		ns	
50	$\overline{BUSOUT}$ low to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$ driven (bus requestor, $\overline{BUSIN}$ low)	240		150		ns	
51	$\overline{BUSIN}$ low to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$,$\overline{LB}$, $\overline{HB}$ driven (bus requestor, $\overline{BUSOUT}$ low)	270	650	180	500	ns	
52	Tristate $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{LB}$, $\overline{HB}$, to $\overline{BUSOUT}$ high (bus requestor)	180		100		ns	
53	$\overline{BUSOUT}$ high to $\overline{BUSIN}$ high (bus requestor)		530		400	ns	
54	$\overline{BUSIN}$ low to address/data bus driven (bus requestor)	350		250		ns	
55	Tristate address/data bus to $\overline{BUSOUT}$ high (bus requestor)	100		65		ns	

MK68E200 BUS AC ELECTRICAL SPECIFICATIONS (PRIVATE BUS)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
56	Valid Data Setup to PHI 1 low	30		20		ns	
57	PBR/$\overline{W}$ valid to $\overline{PBAS}$ starting low	40		40		ns	
58	Address valid to $\overline{PBAS}$ starting low	35		35		ns	
59	Input data hold time from PHI 1 low	0		0		ns	
60	Input data hold time from $\overline{PBDS}$ high	−25		−25		ns	

MK68E200 EXPANDED BUS AC ELECTRICAL SPECIFICATIONS (PRIVATE BUS) (Cont.)

NO.	DESCRIPTION	4 MHz		6 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX		
61	PHI 1 low to $\overline{\text{PBDS}}$ high		130		105	ns	
62	$\overline{\text{PBDTACK}}$ low setup to PHI 1 high	20		15		ns	
63	$\overline{\text{PBDS}}$ high to $\overline{\text{PBDTACK}}$ high (hold time)	−15		−15		ns	
64	$\overline{\text{PBDS}}$ pulse width	190		125		ns	
65	PHI 1 high to $\overline{\text{PBAS}}$ high		100		75	ns	
66	PHI 1 low to data out invalid	10		10		ns	
67	$\overline{\text{PBAS}}$ inactive	200		135		ns	
68	$\overline{\text{PBDS}}$ high to data out invalid	200		135		ns	
69	$\overline{\text{PBDS}}$ high to $\overline{\text{PBAS}}$ high	15		15		ns	

MK68200 INPUT/OUTPUT AC ELECTRICAL CHARACTERISTICS

NO.	DESCRIPTION		4 MHz		6 MHz		UNITS	NOTES
			MIN	MAX	MIN	MAX		
70	Active and inactive pulse times	For XI2, XI1, STRH, STRL, TAI, TBI, $\overline{\text{NMI}}$	5		5		state times	1
		For XI0	3		3			
71	Input data setup to falling edge of STRH, STRL		50		35		ns	
72	Input data hold from the falling edge of STRH, STRL		60		40		ns	
73	RDYH, RDYL low time		1	3	1	3	state times	1
74	Delay from STRH, STRL high to RDYH, RDYL low			110		75	ns	
75	Delay from data valid to RDYH, RDYL high during output			3		3	state times	1
76	Delay from STRH high to data out			125		85	ns	
77	Port 0 data hold time from STRH low		15		10		ns	
78	Delay to Port 0 float from STRH low			75		50	ns	
79	TCLK,RCLK period (asynchronous) TCLK,RCLK period (synchronous)		4.0 1.0	DC DC	2.67 .667	DC DC	μs	
80	TCLK, RCLK width low		4	DC	4	DC	state times	1
81	TCLK, RCLK width high		4	DC	4	DC	state times	1

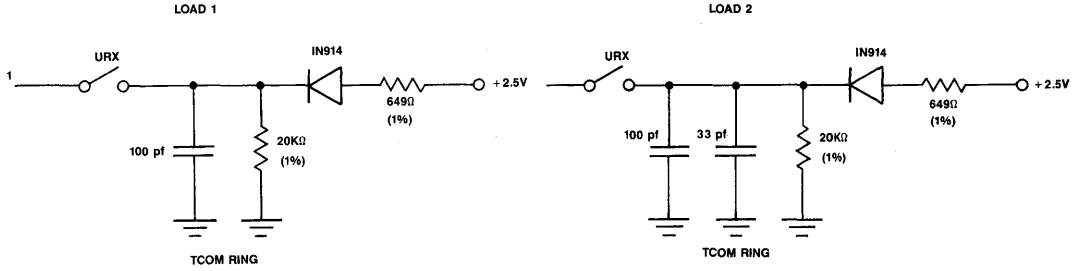
MK68200 INPUT/OUTPUT AC ELECTRICAL SPECIFICATIONS

NO.	DESCRIPTION		4 MHz		6 MHz		UNITS	NOTES
			MIN	MAX	MIN	MAX		
82	TCLK low to SO delay (sync mode)	TCLK as input	330		220		ns	
		TCLK as output	75		50			
83	SI to RCLK high setup time (sync mode)	RCLK as input	30		20		ns	
		RCLK as output	180		120			
84	SI hold time from RCLK high (sync mode)	RCLK as input	45		30		ns	
		RCLK as output	0		0			

NOTES
1. One state time is equal to one-half of the instruction clock (PHI 1) period.
2. For the private bus case, the signals referenced apply to the equivalent private bus signals.

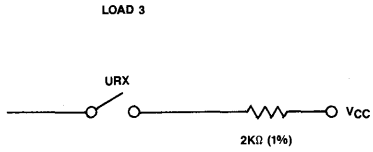
VI

OUTPUT TEST LOAD
Figure 22



TEST LOAD 1 IS APPLICABLE TO ALL PINS EXCEPT THOSE LISTED UNDER TEST LOAD 2 AND TEST LOAD 3.

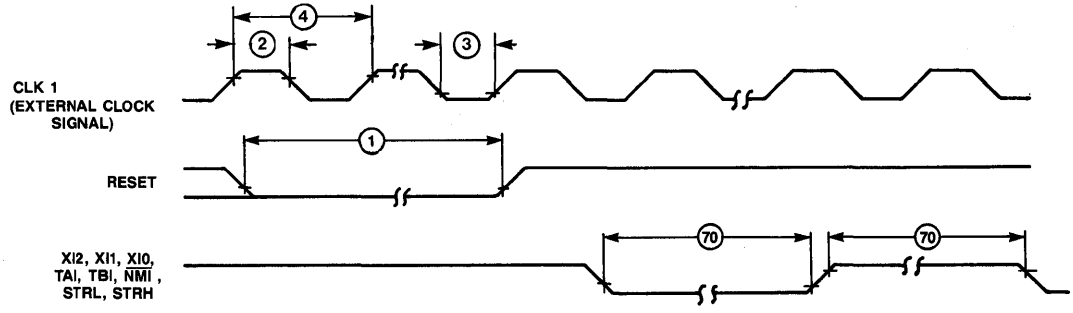
TEST LOAD 2 IS APPLICABLE TO THE FOLLOWING PINS: CLKOUT, $\overline{PBLB}$, $\overline{PBHB}$, PBR/$\overline{W}$, $\overline{PBDS}$, P4-15, P4-14, P4-9, P4-8, AND $\overline{PBAS}$.



TEST LOAD 3 IS APPLICABLE TO THE FOLLOWING PINS: P1-12 AND P1-8.

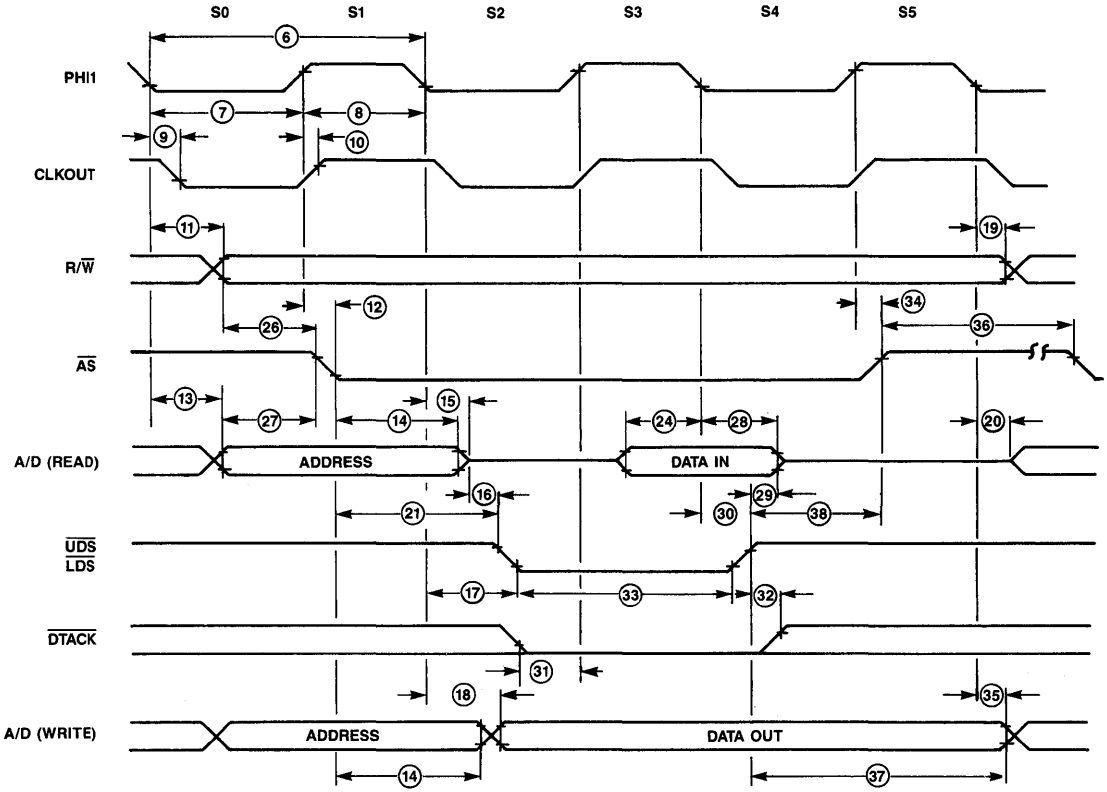
MK68200 AC TIMING

Figure 23



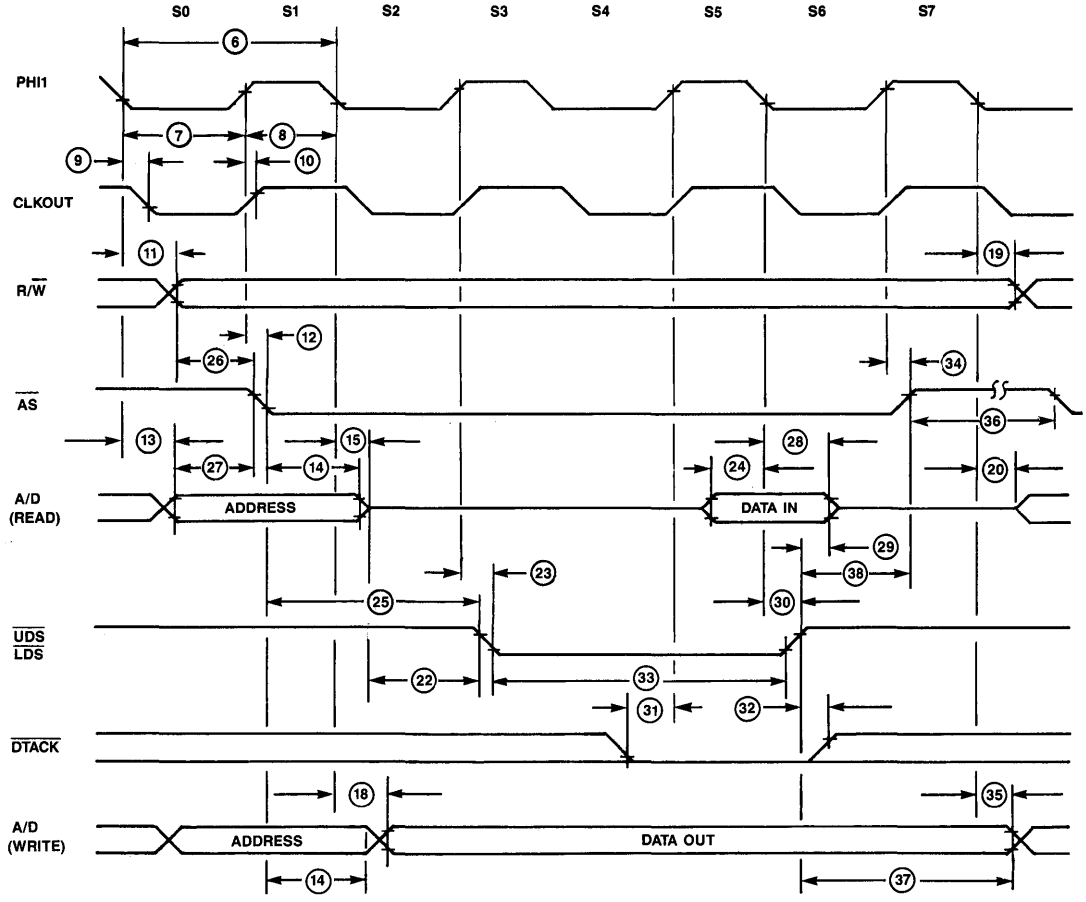
MK68201 UPC BUS TIMING (FAST CYCLE)

Figure 24



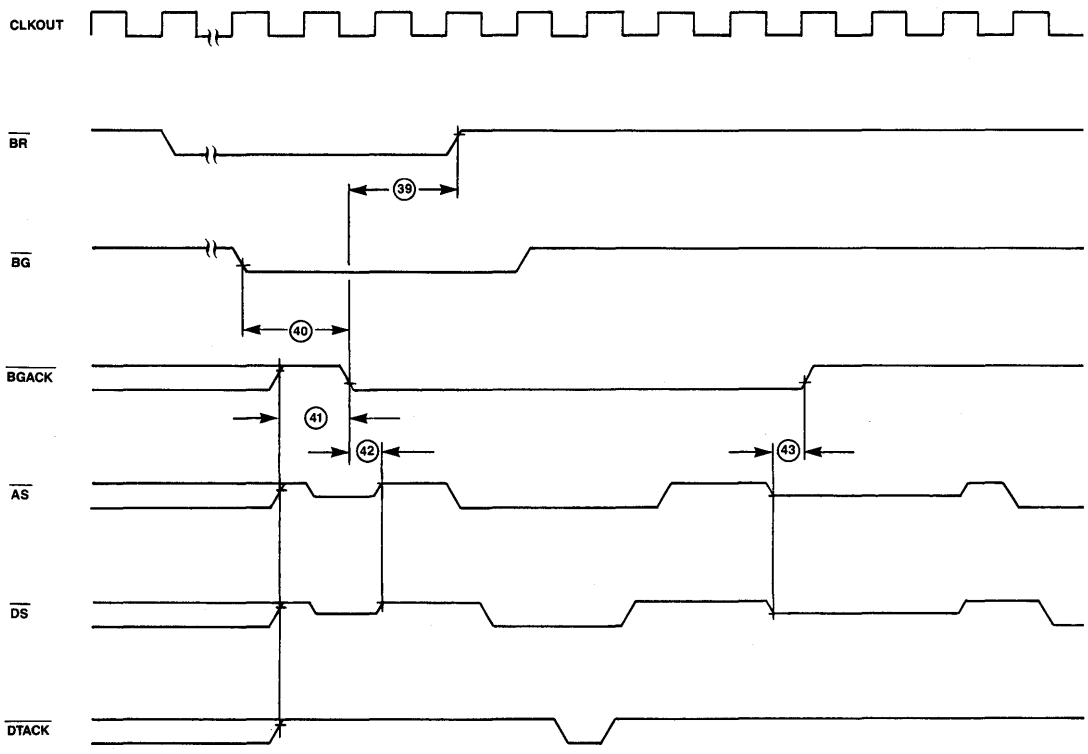
MK68201 UPC BUS TIMING (STANDARD CYCLE)

Figure 25

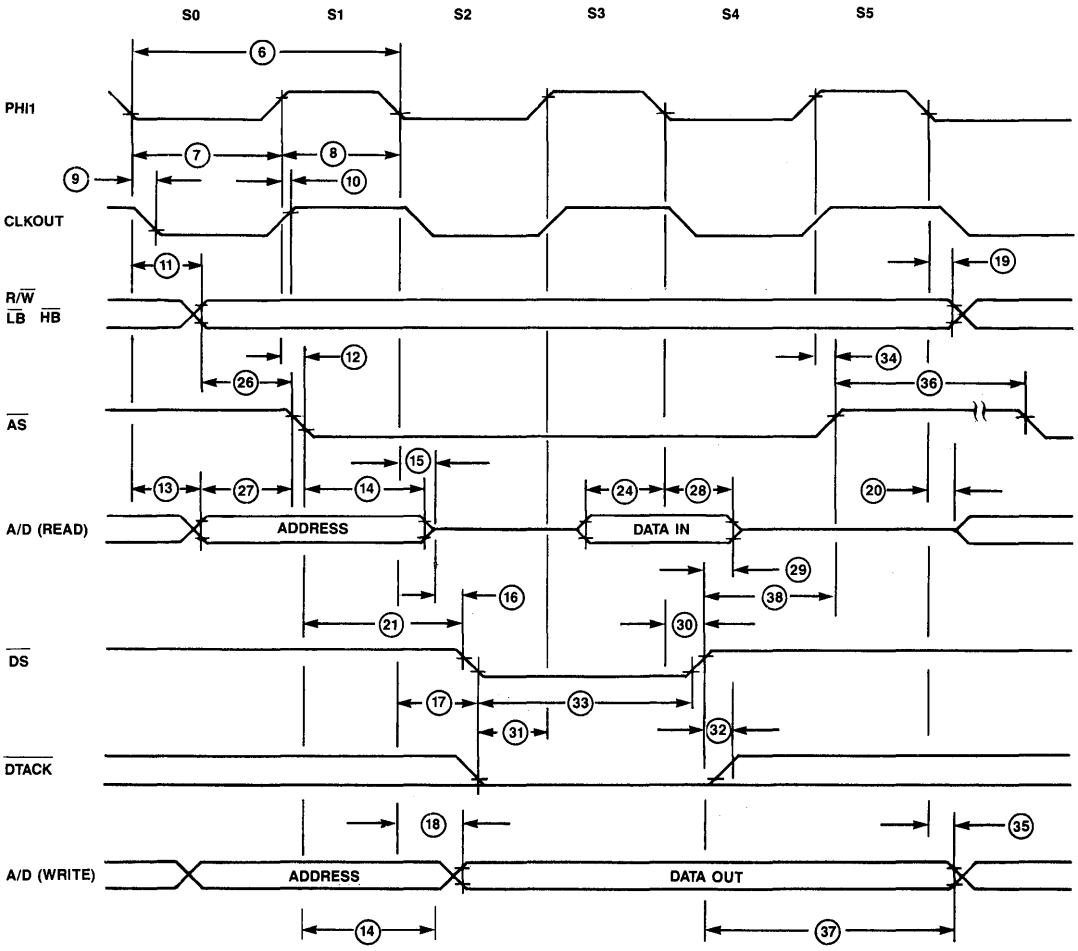


VI

MK68201 UPC BUS ARBITRATION TIMING
Figure 26



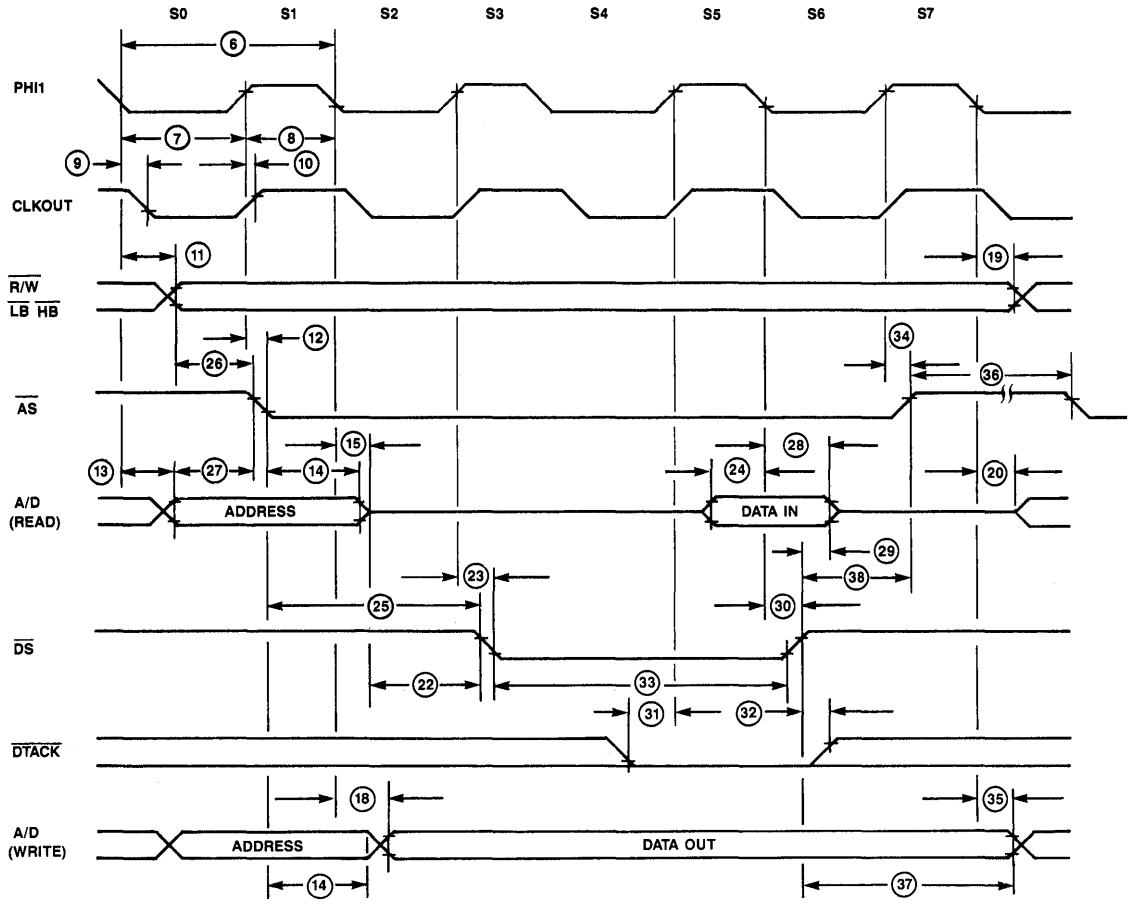
MK68211 GP BUS TIMING (FAST CYCLE)
Figure 27



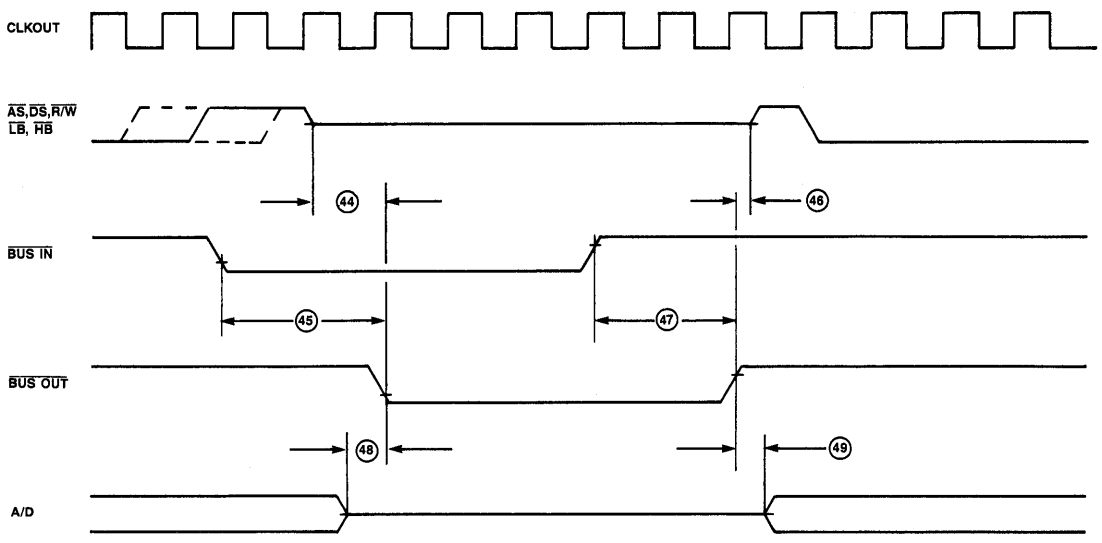
VI

MK68211 GP BUS TIMING (STANDARD CYCLE)

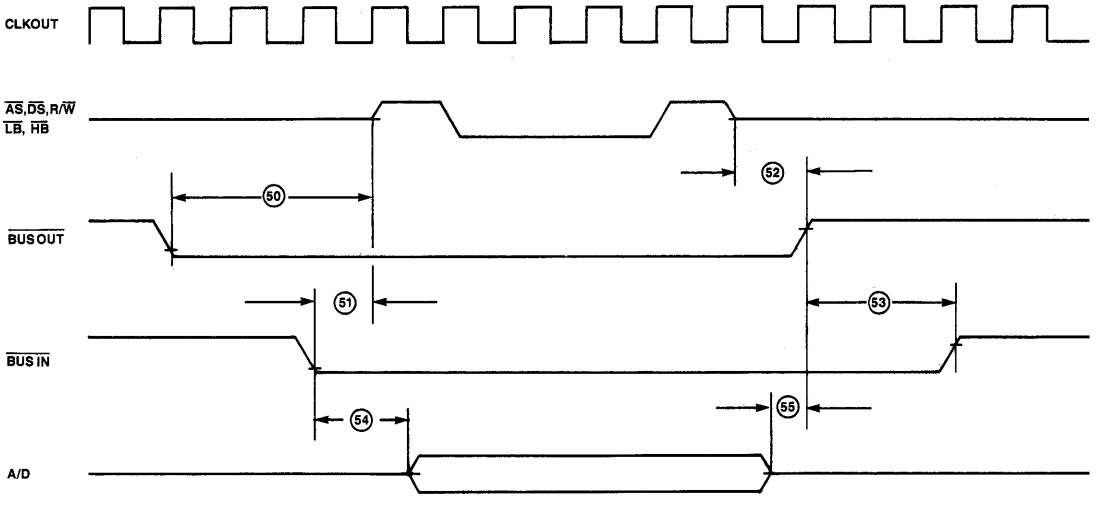
Figure 28



MK68211 GP BUS ARBITRATION TIMING (BUS GRANTOR)
Figure 29

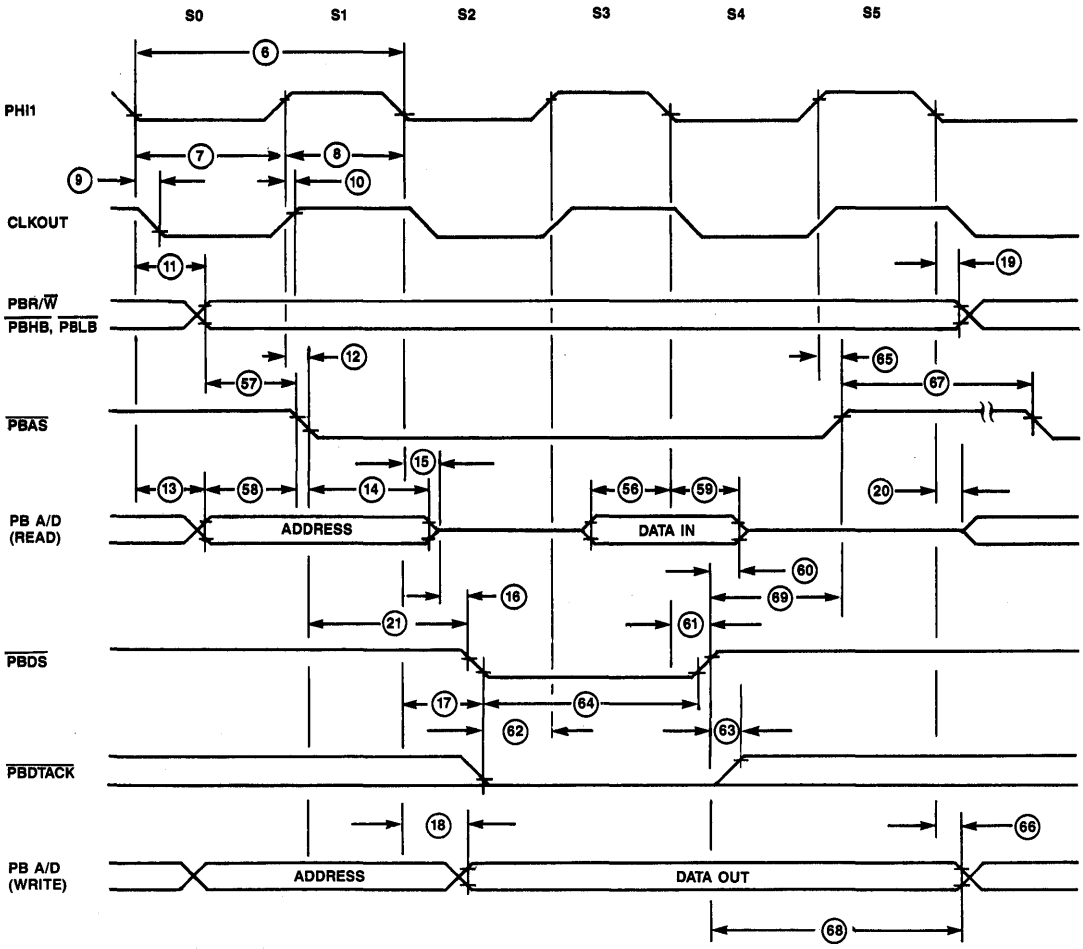


MK68211 GP BUS ARBITRATION TIMING (BUS REQUESTOR)
Figure 30

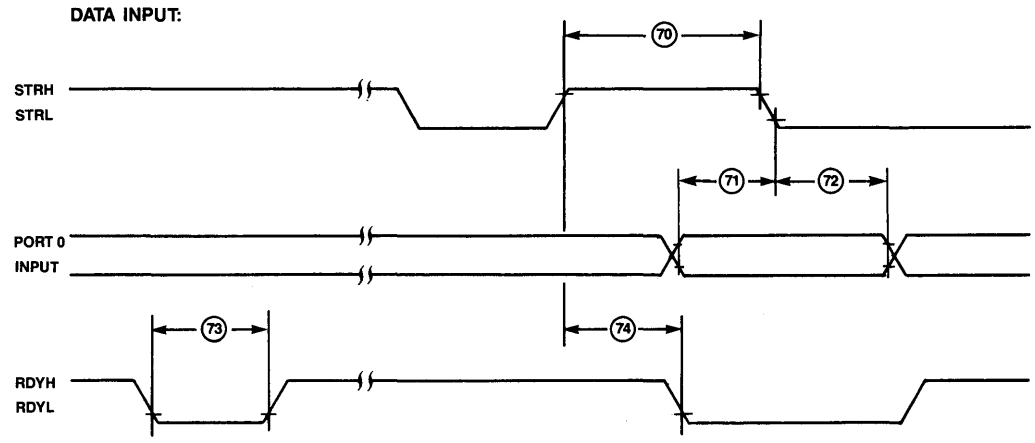


MK68200 PRIVATE BUS TIMING (FAST CYCLE)

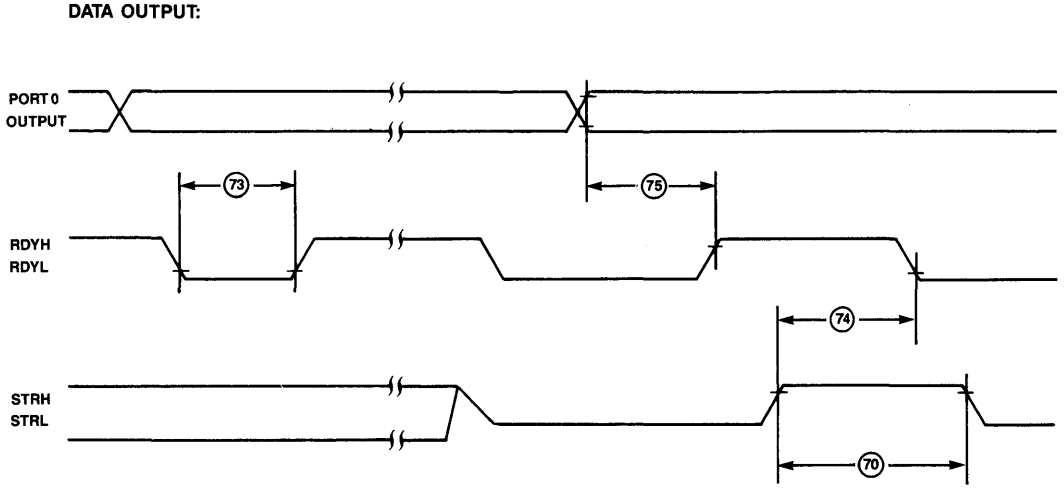
Figure 31



INPUT/OUTPUT AC TIMING
Figure 32

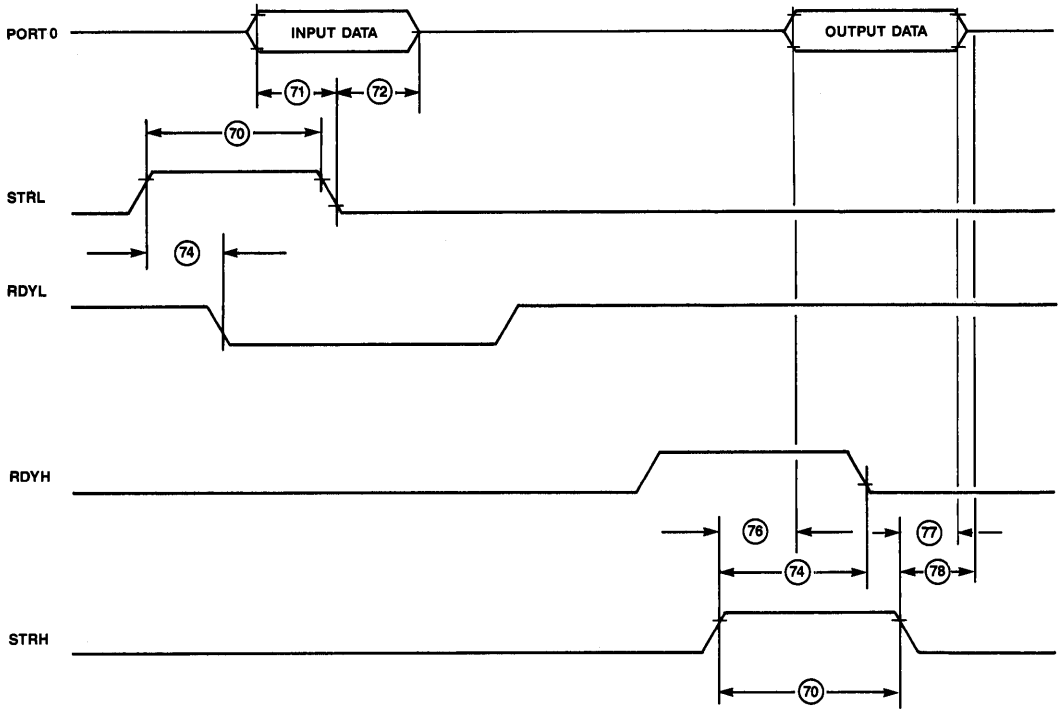


INPUT/OUTPUT AC TIMING
Figure 33

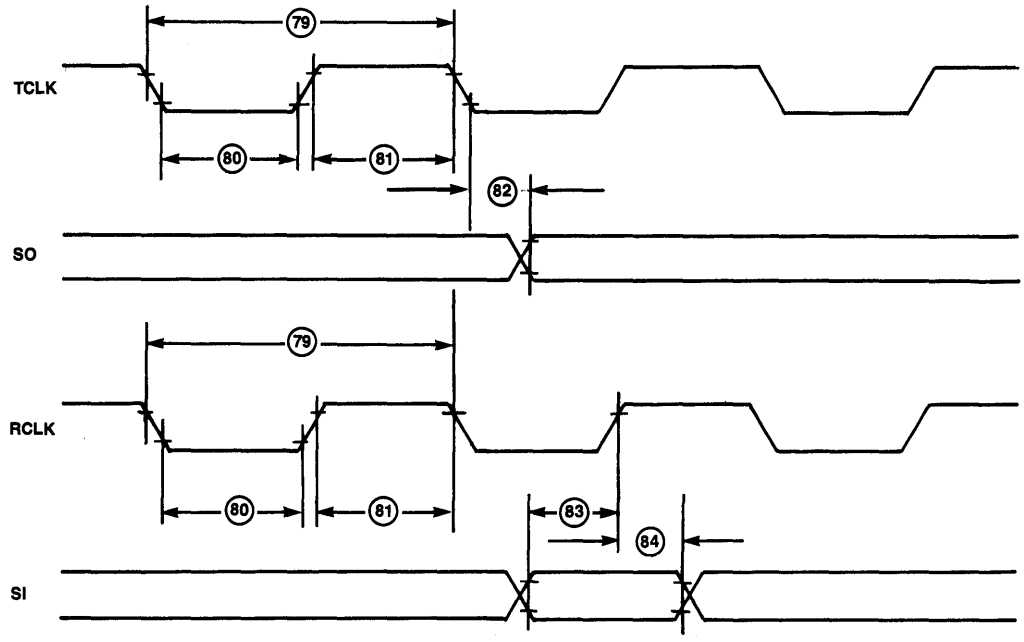


INPUT/OUTPUT AC TIMING
Figure 34

BIDIRECTIONAL I/O:



SERIAL I/O:

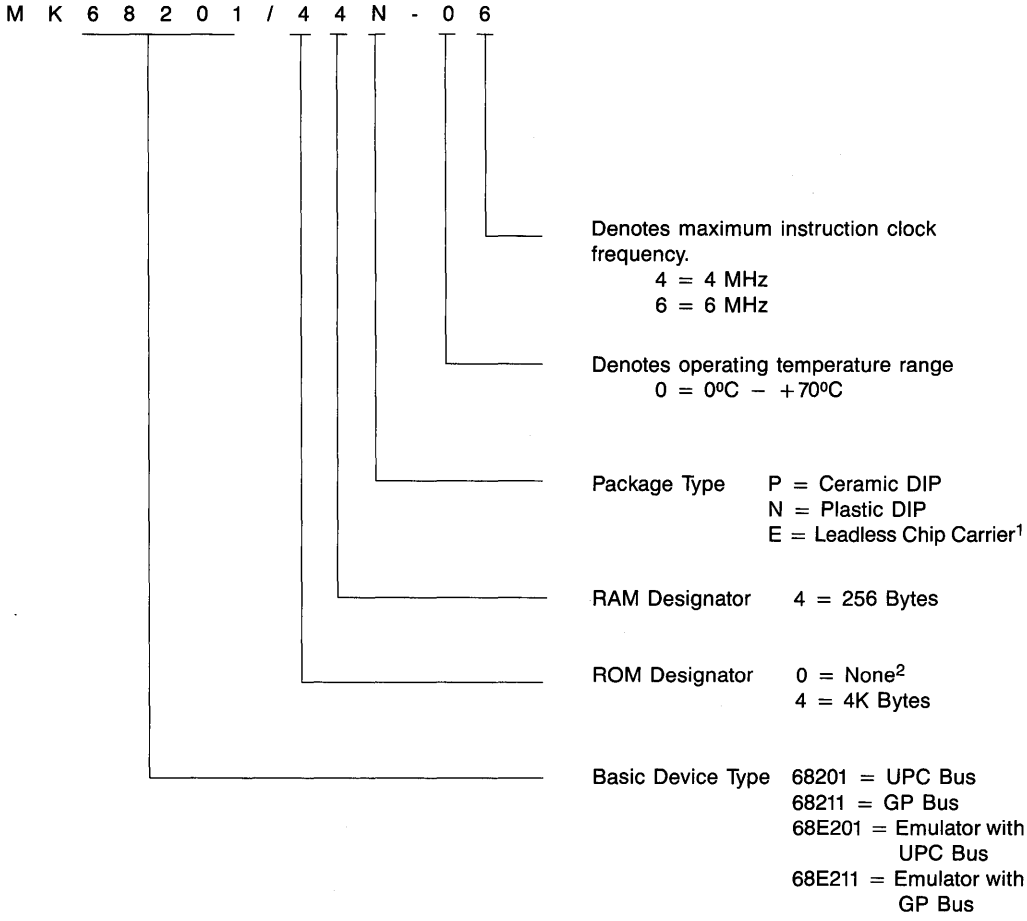


PART NUMBERING INFORMATION

There are two types of part numbers for the 68200 family of devices. The generic part number describes the basic device type, the amount of ROM and RAM, the desired package type, temperature range, power supply tolerance, and expandable bus interface type.

Generic Part Number

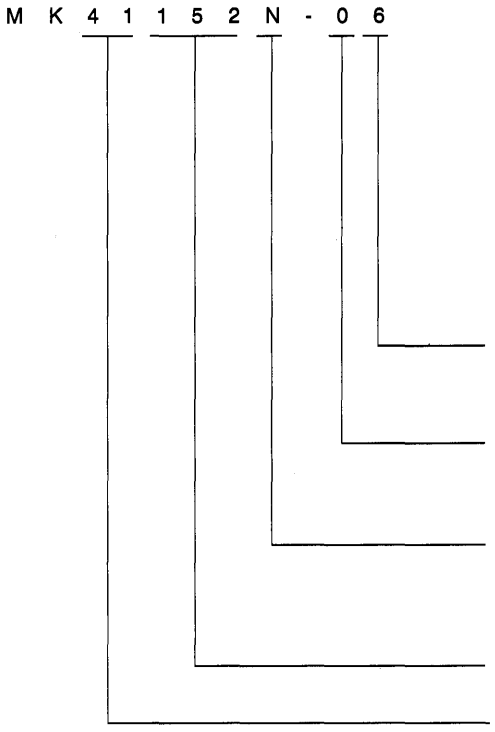
An example of the generic part number is shown below:



NOTES
1. Available for emulator only.
2. Must be "0" when specifying the emulator.

Device Order Number

An example of the device order number is shown below:



VI

NOTES
1. Available for emulator only.

ORDERING INFORMATION

The device selection table shown below lists available versions of the 68200.

GENERIC PART NO.	DEVICE ORDER NO.	PACKAGE TYPE	MAXIMUM CLOCK FREQUENCY	TEMPERATURE RANGE
MK68201/04-06	MK41000N-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68201/44-06	MK41XXXN-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68E201/04-06	MK40000E-06	Ceramic LCC	6 MHz	0° to 70°C
MK68211/04-06	MK42000N-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68211/44-06	MK42XXXN-06	Plastic 48-pin	6 MHz	0° to 70°C
MK68E211/04-06	MK40010E-06	Ceramic LCC	6 MHz	0° to 70°C
MK68201/04-04	MK41000N-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68201/44-04	MK41XXXN-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68E201/04-04	MK40000E-04	Ceramic LCC	4 MHz	0° to 70°C
MK68211/04-04	MK42000N-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68211/44-04	MK42XXXN-04	Plastic 48-pin	4 MHz	0° to 70°C
MK68E211/04-04	MK40010E-04	Ceramic LCC	4 MHz	0° to 70°C

PRELIMINARY

PARALLEL INTERFACE/TIMER (PI/T) MK68230

FEATURES

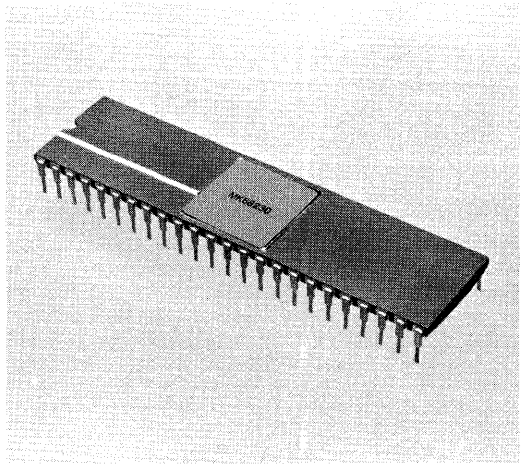
- ☐ 68000 Bus Compatible
- ☐ Port Modes Include:
  - Bit I/O
  - Unidirectional 8-bit and 16-bit
  - Bidirectional 8-bit and 16-bit
- ☐ Programmable Handshaking Options
- ☐ 24-bit Programmable Timer Modes
- ☐ Five Separate Interrupt Vectors
- ☐ Separate Port and Timer Interrupt Service Requests
- ☐ Registers are Read/Write and Directly Addressable
- ☐ Registers are Addressed for MOVEP (Move Peripheral) and DMAC Compatibility

GENERAL DESCRIPTION

The MK68230 Parallel Interface/Timer (PI/T) provides versatile double-buffered parallel interfaces and an operating system oriented timer to MK68000 systems. The parallel interfaces operate in unidirectional or bidirectional modes, either 8 or 16 bits wide. In the unidirectional modes, an associated data direction register determines whether the port pins are inputs or outputs. In the bidirectional modes, the data direction registers are ignored, and the direction is determined dynamically by the state of four handshake pins. These programmable handshake pins provide an interface flexible enough for connection to a wide variety of low, medium, or high speed peripherals or other computer systems. The PI/T ports allow use of vectored or autovectored interrupts, and also provide a DMA request pin for connection to the Direct Memory Access Controller or a similar circuit. The PI/T timer contains a 24-bit wide counter and a 5-bit prescaler. The timer may be clocked by the system clock (PI/T CLK pin) or by an external clock (TIN pin), with the option of using a 5-bit prescaler. It can generate periodic interrupts, a square wave, or a single interrupt after a programmed timer period. Also, it can be used for elapsed time measurement or as a device watchdog.

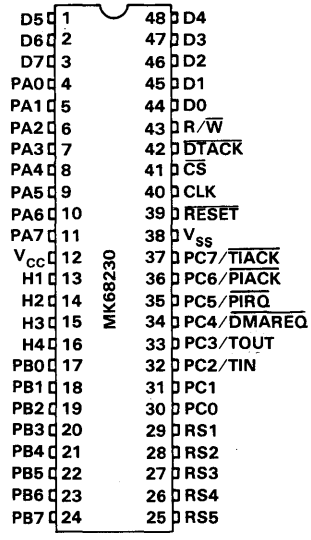
The PI/T consists of two logically independent sections: the ports and the timer. The port section consists of Port

MK68230
Figure 1



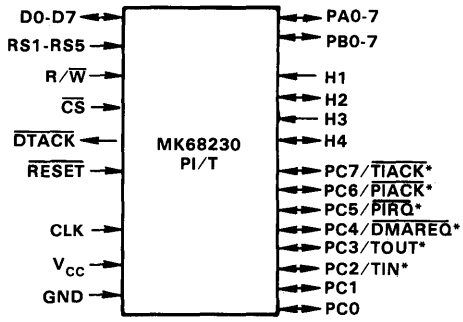
VI

PIN ASSIGNMENT
Figure 2



LOGICAL PIN ASSIGNMENT

Figure 3



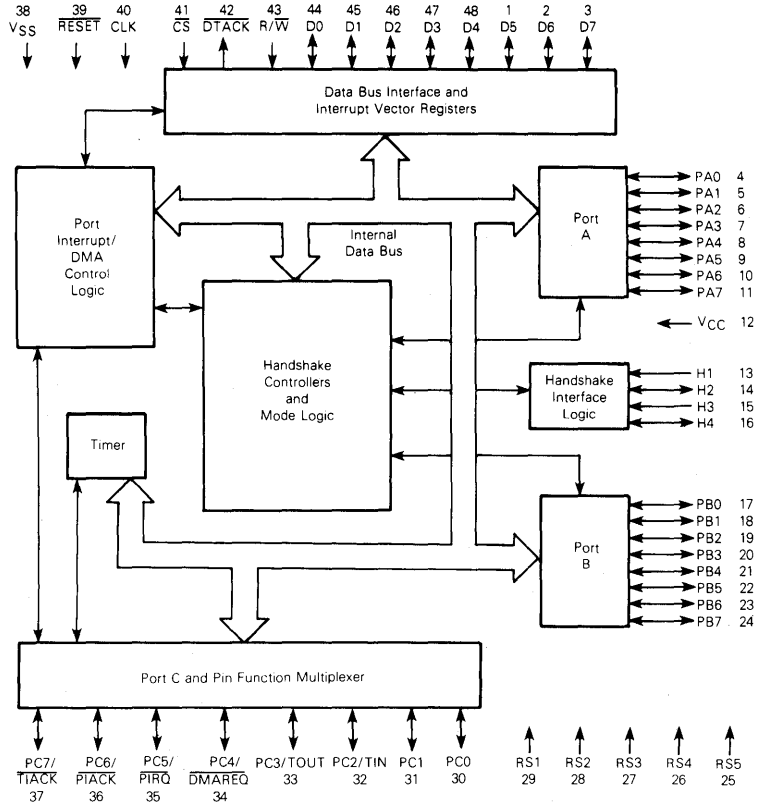
*Individually Programmable Dual-Function Pin

A (PA0-PA7), Port B (PB0-PB7), four handshake pins (H1, H2, H3, and H4), two general I/O pins, and six dual-function pins. The dual-function pins can individually operate as a third port (Port C) or as an alternate function related to either Ports A and B, or the timer. The four programmable handshake pins, depending on the mode, can control data transfer to and from the ports, can be used as interrupt generating inputs, or can be used as I/O pins. The timer consists of a 24-bit counter, optionally clocked by a 5-bit prescaler. Three pins provide complete timer I/O: PC2/TIN, PC3/TOUT, and PC7/TIACK. Of course, only the ones needed for the given configuration perform the timer function, while the others remain Port C I/O.

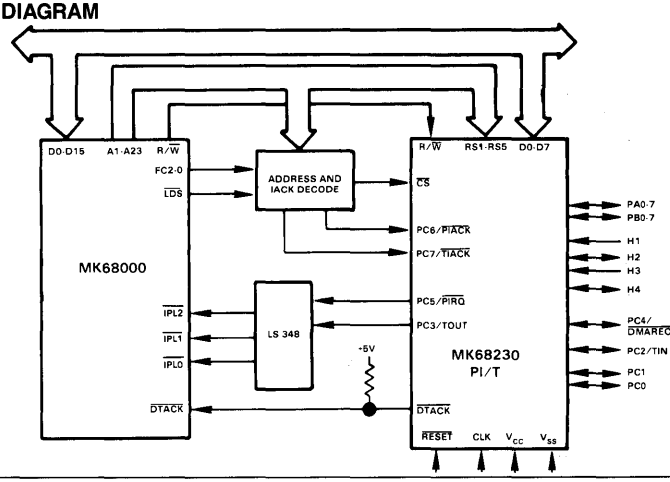
The system bus interface provides for asynchronous transfer of data from the PI/T to a bus master over the data bus (D0-D7). Data transfer acknowledge (DTACK), register selects (RS1-RS5), chip select, the read/write line (R/W), and Port Interrupt Acknowledge (PIACK) or Timer Interrupt Acknowledge (TIACK) control data transfer between the PI/T and the MK68000.

MK68320 BLOCK DIAGRAM

Figure 4



PI/T SYSTEM BLOCK DIAGRAM
Figure 5



PIN DESCRIPTION

Throughout this data sheet, signals are presented using the terms active and inactive, or asserted and negated independent of whether the signal is active in the high-voltage state or low-voltage state. (The active state of each logic pin is given below.) Active low signals are denoted by a superscript bar. R/W indicates a "write" is active low and a "read" active high.

D0-D7 (Bidirectional Data Bus) — The data bus pins D0-D7 form an 8-bit bidirectional data bus to/from the MK68000 or other bus master. These pins are active high.

RS1-RS5 (Register Selects) — RS1-RS5 are active high, high-impedance inputs that determine which of the 25 possible registers is being addressed. They are provided by the MK68000 or other bus master.

R/$\overline{W}$ (Read/Write Input) — R/$\overline{W}$ is the high-impedance Read/$\overline{\text{Write}}$ signal from the MK68000 or bus master, indicating whether the current bus cycle is a read (high cycle) or write (low cycle).

$\overline{CS}$ (Chip Select Input) — $\overline{CS}$ is a high-impedance input that selects the PI/T registers for the current bus cycle. Address strobe and the data strobe (upper and lower) of the bus master, along with the appropriate address bits, must be included in the chip select equation. A low level corresponds to an asserted chip select.

$\overline{DTACK}$ (Data Transfer Acknowledge Output) — $\overline{DTACK}$ is an active low output that signals the completion of the bus cycle. During read or interrupt acknowledge cycles, $\overline{DTACK}$ is asserted by the MK68230 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted at the data bus. Data transfer acknowledge is compatible with the MK68000 and with other Mostek bus masters. A holding resistor is required to maintain $\overline{DTACK}$ high between bus cycles.

$\overline{RESET}$ (Reset Input) — $\overline{RESET}$ is a high-impedance input used to initialize all PI/T functions. All control and data direction registers are cleared and most internal operations are disabled by the assertion of $\overline{RESET}$ (low).

CLK (Clock Input) — The clock pin is a high-impedance, TTL-compatible signal with the same specifications as the MK68000. The PI/T contains dynamic logic throughout, and hence this clock must not be gated off at any time. It is not necessary that this clock maintain any particular phase relationship with the MK68000 clock. It may be connected to an independent frequency source (faster or slower) as long as all bus specifications are met.

PA0-PA7 and PB0-PB7 (Port A and Port B) — Ports A and B are 8-bit ports that may be concatenated to form a 16-bit port in certain modes. The ports may be controlled in conjunction with the handshake pins H1-H4. For stabilization during system power-up, Ports A and B have internal pull up resistors to Vcc. All port pins are active high.

H1-H4 (Handshake Pins Inputs or Output) — Handshake pins H1-H4 are multi-purpose pins that (depending on operational mode) may provide an interlocked handshake, a pulsed handshake, an interrupt input (independent of data transfers), or simple I/O pins. For stabilization during system power-

VI

up, H-2 and H4 have internal pullup resistors to Vcc. Their sense (active high or low) may be programmed in the Port General Control Register bits 3-0. Independent of the mode, the instantaneous level of the handshake pins can be read from the Port Status Register.

Port C (PC0-PC7/ Alternate Function)

This port can be used as eight general purpose I/O pins (PC0-PC7) or any combination of six special function pins and two general purpose I/O pins (PC0-PC1). (Each dual function pin can be standard I/O or a special function independent of the other Port C pins.) The dual function pins are defined in the following paragraphs. When used as a Port C pin, these pins are active high. They may be individually programmed as inputs or outputs by the Port C Data Direction Register.

The alternate functions (TIN, TOUT, $\overline{\text{TIACK}}$) are timer I/O pins. TIN may be used as a rising-edge triggered external clock input or an external run/halt control pin (the timer is in the run state if run/halt is high and in the halt state if run/halt is low). TOUT may provide an active low timer interrupt request output or a general-purpose square-wave output, initially high. $\overline{\text{TIACK}}$ is an active low high-impedance input used for timer interrupt acknowledge.

Port A and B functions have an independent pair of active low interrupts request ($\overline{\text{PIRQ}}$) and interrupt acnkowledge ($\overline{\text{PIACK}}$) pins.

The $\overline{\text{DMAREQ}}$ (Direct Memory Access Request) pin provides an active low Direct Memory Access Controller (DMAC) request pulse of three clock cylcles.

MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE:
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, T_A = 0 to 70°C, unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Input High Voltage — All inputs	V_{IH}	V_{SS} +2.0	V_{CC}	V
Input Low Voltage — All inputs	V_{IL}	V_{SS} −0.3	V_{SS} +0.8	V
Input Leakage Current (V_{in} = 0 to 5.25 V) H1, H3, R/$\overline{W}$, $\overline{RESET}$, CLK, RS1-RS5, $\overline{CS}$	I_{in}	—	10.0	μA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4) $\overline{DTACK}$, PC0-PC7, D0-D7	I_{TSI}	—	20	μA
Hi-Z (Off State) Input Current (V_{in} = 0.4 to 2.4) H2, H4, PA0-PA7, PB0-PB7	I_{TSI}	−0.1	−1.0	mA
Output High Voltage (I_{LOAD} = −400μA, V_{CC} = min) (I_{LOAD} = −150μA, V_{CC} = min) (I_{LOAD} = −100μA, V_{CC} = min) — $\overline{DTACK}$, D0-D7; H2, H4, PB0-PB7, PA0-PA7; PC0-PC7	V_{OH}	V_{SS} +2.4	—	V
Output Low Voltage (I_{LOAD} = 8.8 mA, V_{CC} = min) — PC3/TOUT, PC5/$\overline{PIRQ}$	V_{OL}	—	0.5	V
Output Low Voltage (I_{LOAD} = 5.3 mA, V_{CC} = min) — D0-D7, $\overline{DTACK}$	V_{OL}	—	0.5	V
Output Low Voltage (I_{LOAD} = 2.4 mA, V_{CC} = min) — PA0-PA7, PB0-PB7, H2, H4, PC0-PC2, PC4, PC6,PC7	V_{OL}	—	0.5	V
Internal Power Dissipation (Measured at T_A = 0°C)	P_{INT}	—	750	mW
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)	C_{in}	—	15	pF

VI

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING

Characteristics	Symbol	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Frequency of Operation	f	2.0	8.0	2.0	10.0	4.0	12.0	MHz
Cycle Time	t_{cyc}	125	500	100	500	80	250	ns
Clock Pulse Width	t_{CL}	55	250	45	250	35	125	ns
	t_{CH}	55	250	45	250	35	125	
Clock Rise and Fall Times	t_{Cr}	—	10	—	10	—	5	ns
	t_{Cf}	—	10	—	10	—	5	

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C, unless otherwise noted)

Number	Characteristics	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
1	R/$\overline{W}$, RS1-RS5 Valid to CS Low (Setup Time)	0	—	0	—	0	—	ns
2	$\overline{CS}$ Low to R/$\overline{W}$ and RS1-RS5 Invalid (Hold Time)	100	—	65	—	60	—	ns
3(1)	$\overline{CS}$ Low to CLK Low (Setup Time)	30	—	20	—	20	—	ns
4(2)	$\overline{CS}$ Low to Data Out Valid	—	75	—	65	—	55	ns
5	RS1-RS5, R/$\overline{W}$ Valid to Data Out	—	140	—	100	—	80	ns
6	CLK Low to $\overline{DTACK}$ Low (Read/Write Cycle)	0	70	0	60	0	55	ns
7(3)	$\overline{DTACK}$ Low to $\overline{CS}$ High (Hold Time)	0	—	0	—	0	—	ns
8	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to Data Out Invalid (Hold Time)	0	—	0	—	0	—	ns
9	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to D0-D7 High Impedance	—	50	—	45	—	45	ns

AC ELECTRICAL SPECIFICATIONS (Continued)

Number	Characteristic	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
10	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High	—	50	—	45	—	40	ns
11	$\overline{CS}$ or $\overline{PIACK}$ or $\overline{TIACK}$ High to $\overline{DTACK}$ High Impedance	—	100	—	55	—	45	ns
12	Data In Valid to $\overline{CS}$ Low (Setup Time)	0	—	0	—	0	—	ns
13	$\overline{CS}$ Low to Data In Invalid (Hold Time)	100	—	65	—	60	—	ns
14	Port Input Data Valid to H1(H3) Asserted (Setup Time)	100	—	60	—	50	—	ns
15	H1(H3) Asserted to Port Input Data Invalid (Hold Time)	20	—	20	—	20	—	ns
16	Handshake Input H1(H4) Pulse Width Asserted	40	—	40	—	40	—	ns
17	Handshake Input H1(H4) Pulse Width Negated	40	—	40	—	40	—	ns
18	H1(H3) Asserted to H2(H4) Negated (Delay Time)	—	150	—	120	—	100	ns
19	CLK Low to H2(H4) Asserted (Delay Time)	—	100	—	100	—	80	ns
20(4)	H2(H4) Asserted to H1(H3) Asserted	0	—	0	—	0	—	ns
21(5)	CLK Low to H2(H4) Pulse Negated (Delay Time)	—	125	—	125	—	100	ns
22(9,10)	Synchronized H1(H3) to CLK Low on which $\overline{DMAREQ}$ is Asserted	2.5	3.5	2.5	3.5	2.5	3.5	CLK Per.
23	CLK Low on which $\overline{DMAREQ}$ is Asserted to CLK Low on which $\overline{DMAREQ}$ is Negated	2.5	3	2.5	3	2.5	3	CLK Per.
24	CLK Low to Port Output Data Valid (Delay Time) (Modes 0 and 1)	—	150	—	120	—	100	ns
25(9,10)	Synchronized H1(H3) to Port Output Data Invalid (Modes 0 and 1)	1.5	2.5	1.5	2.5	1.5	2.5	CLK Per.
26	H1 Negated to Port Output Data Valid (Modes 2 and 3)	—	70	—	50	—	50	ns
27	H1 Asserted to Port Output Data High Impedance (Modes 2 and 3)	0	70	0	70	0	70	ns
28	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	0	—	0	—	0	—	ns
29	CLK Low to Data Output Valid, Interrupt Acknowledge Cycle	—	120	—	100	—	80	ns
30(7)	H1(H3) Asserted to CLK High (Setup Time)	50	—	40	—	40	—	ns
31	$\overline{PIACK}$ or $\overline{TIACK}$ Low to CLK Low (Setup Time)	50	—	40	—	30	—	ns

AC ELECTRICAL SPECIFICATIONS (Continued)

Number	Characteristic	8 MHz		10 MHz		12.5 MHz		Unit
		Min	Max	Min	Max	Min	Max	
32(10)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{DMAREQ}$ is Asserted	3	3	3	3	3	3	CLK Per.
33(9,10)	Synchronized H1(H3) to CLK Low on which H2(H4) is Asserted	3.5	4.5	3.5	4.5	3.5	4.5	CLK Per.
34	CLK Low to $\overline{DTACK}$ Low Interrupt Acknowledge Cycle (Delay Time)	—	100	—	100	—	80	ns
35	CLK Low to $\overline{DMAREQ}$ Low (Delay Time)	0	120	0	100	0	80	ns
36	CLK Low to $\overline{DMAREQ}$ High (Delay Time)	0	120	0	100	0	80	ns
37(10)	Synchronized H1(H3) to CLK Low on which $\overline{PIRQ}$ is Asserted	2.5	3.5	2.5	3.5	2.5	3.5	CLK Per.
38(10)	Synchronized $\overline{CS}$ to CLK Low on which $\overline{PIRQ}$ is High Impedance	3	3	3	3	3	3	CLK Per.
39	CLK Low to PIRQ Low or High Impedance	0	250	0	225	0	200	ns
40(8)	TIN Frequency (External Clock) - Prescaler Used	0	1	0	1	0	1	f_{clk} (Hz) (6)
41	TIN Frequency (External Clock) - Prescaler Not Used	0	1/8	0	1/8	0	1/8	f_{clk} (Hz) (6)
42	TIN Pulse Width High or Low (External Clock)	55	—	45	—	45	—	ns
43	TIN Pulse Width Low (Run/Halt Clock)	1	—	1	—	1	—	CLK Per.
44	CLK Low to TOUT High, Low, or High Impedance	0	250	0	225	0	200	ns
45	$\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACH}$ High to $\overline{CS}$, $\overline{PIACK}$, or $\overline{TIACK}$ Low	50	—	30	—	30	—	ns

VI

NOTES:

1. This specification only applies if the PI/T had completed all operations initiated by the previous bus cycle when $\overline{CS}$ was asserted. Following a normal read or write bus cycle, all operations are complete within three clocks after the falling edge of the CLK pin on which $\overline{DTACK}$ was asserted. If $\overline{CS}$ is asserted prior to completion of these operations, the new bus cycle, and hence, $\overline{DTACK}$ is postponed.

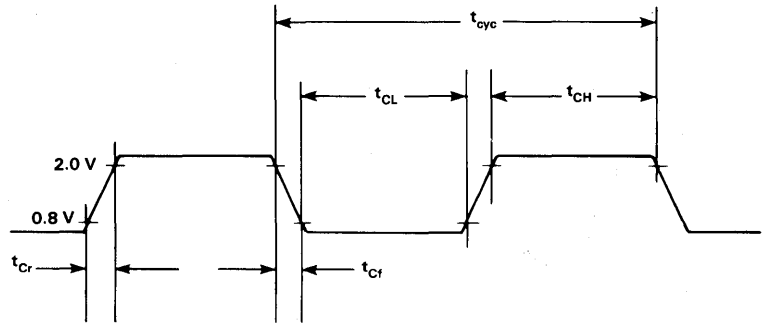
   If all operations of the previous bus cycle were complete when $\overline{CS}$ was asserted, this specification is made only to insure that $\overline{DTACK}$ is asserted with respect to the falling edge of the CLK pin as shown in the timing diagram, not to guarantee operation of the part. If the $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later.
2. Assuming the RS1-RS5 to data valid time has also expired.
3. This specification imposes a lower bound on $\overline{CS}$ low time, guaranteeing that $\overline{CS}$ will be low for at least 1 CLK period.
4. This specification assures recognition of the asserted edge of H1(H3).
5. This specification applies only when a pulsed handshake option is chosen and the pulse is not shortened due to an early asserted edge of H1(H3).
6. CLK refers to the actual frequency of the CLK pin, not the maximum allowable CLK frequency.
7. If the setup time on the rising edge of the clock is not met, H1(H3) may not be recognized until the next rising of the clock.
8. This limit applies to the frequency of the signal at TIN compared to the frequency of the CLK signal during each clock cycle. If any period of the waveform at TIN is smaller than the period of the CLK signal at that instant, then it is likely that the timer circuit will completely ignore one cycle of the TIN signal.

   If these two signals are derived from different sources, they will have different instantaneous frequency variations. In this case the frequency applied to the TIN pin must be distinctly less than the frequency at the CLK pin to avoid lost cycles of the TIN signal. With signals derived from different crystal oscillators applied to the TIN and CLK pins with fast rise and fall times, the TIN frequency can approach 80 to 90% of the frequency of the CLK signal without a loss of a cycle of the TIN signal.

   If these two signals are derived from the same frequency source then the frequency of the signal applied to TIN can be 100% of the frequency at the CLK pin. They may be generated by different buffers from the same signal or one may be an inverted version of the other. The TIN signal may be generated by and 'AND' function of the clock and a control signal.
9. The maximum value is caused by a peripheral access (H1 (H3) asserted) and bus access ($\overline{CS}$ asserted) occurring at the same time.
10. Synchronized means that the input signal has been seen by the PI/T on the appropriate edge of the clock (rising edge for H1(H3) and falling edge for $\overline{CS}$).

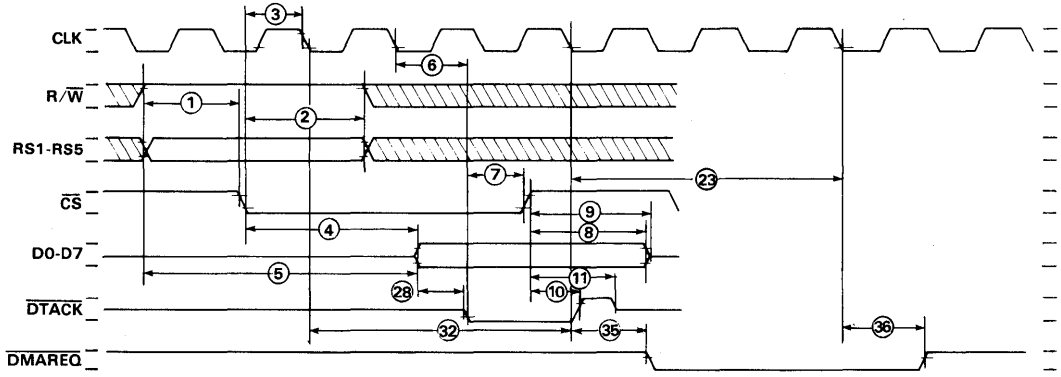
CLOCK INPUT TIMING DIAGRAM

Figure 6



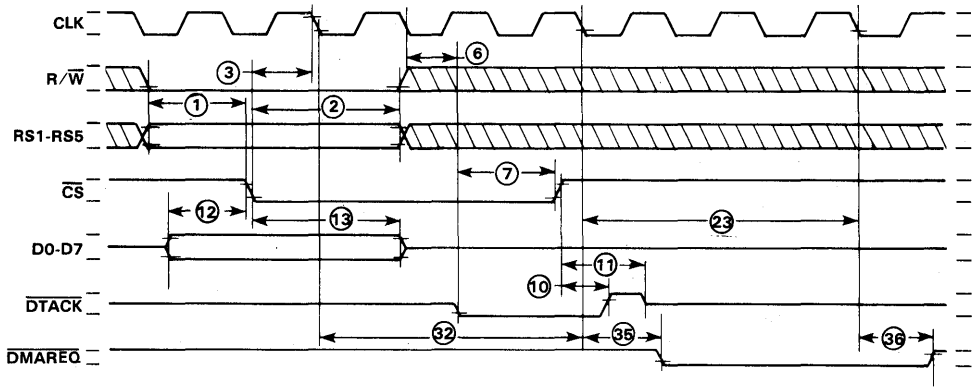
READ CYCLE TIMING DIAGRAM

Figure 7



WRITE CYCLE TIMING DIAGRAM

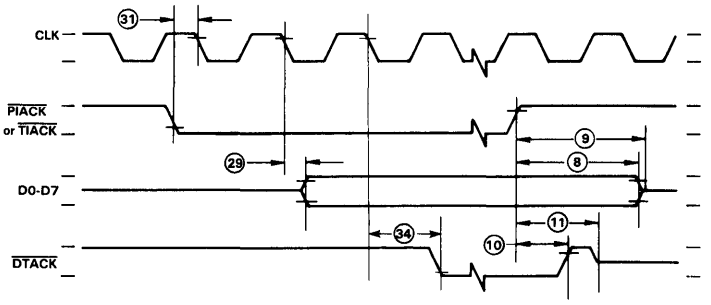
Figure 8



NOTE:
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

IACK TIMING DIAGRAM

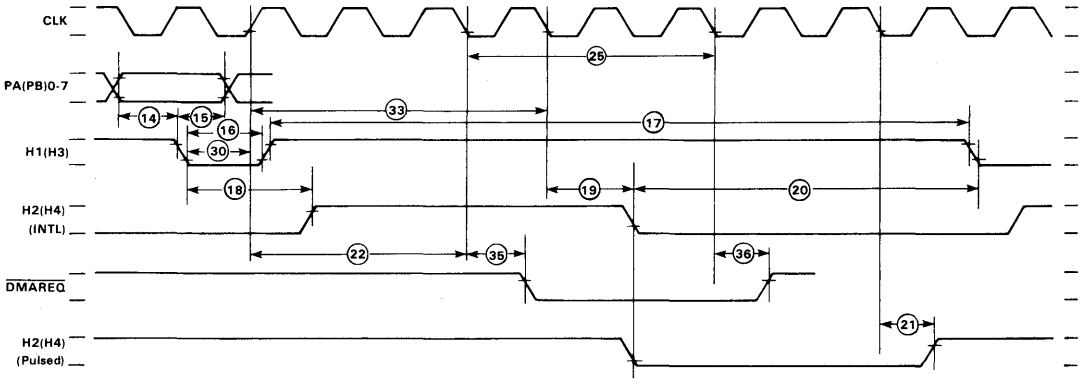
Figure 9



NOTE:
Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise needed.

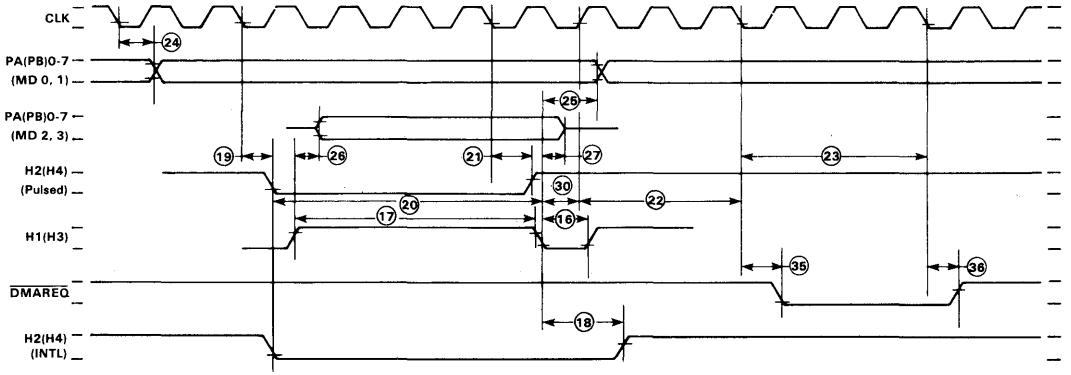
PERIPHERAL INPUT TIMING DIAGRAM

Figure 10



PERIPHERAL OUTPUT TIMING DIAGRAM

Figure 11



NOTES:
1. Timing diagram shows H1, H2, H3, and H4 asserted low.
2. Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

MK68230 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMP. RANGE
MK68230N-8	48 Pin Plastic DIP	8.0 MHz	0° to 70°C
MK68230N-10		10.0 MHz	

ADVANCE INFORMATION

MEMORY MANAGEMENT UNIT MK68451

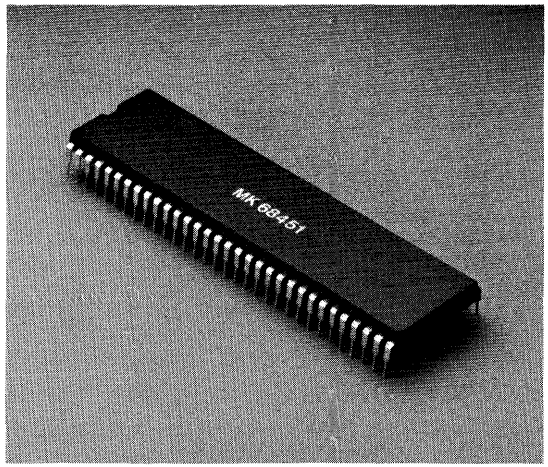
FEATURES

- ☐ Compatible with MK68000 and MK68008
- ☐ Provides virtual memory support for the MK68010
- ☐ Provides efficient memory allocation
- ☐ Seperates address spaces of system and user resources
- ☐ Provides write protection
- ☐ Supports paging and segmentation
- ☐ 32 segments of variable size with each MMU
- ☐ Multiple MMU capability to expand to any number of segments
- ☐ Allows inter-task communication through shared segments
- ☐ Quick context switching to cut operating system overhead
- ☐ Simplifies programming model of address space
- ☐ Increases system reliability
- ☐ DMA-compatible

GENERAL DESCRIPTION

The MK68451 memory management unit (MMU) provides address translation and protection for the 16 megabyte addressing range of the MK68000 MPU. Each bus master (or processor) in the MK68000 family provides a function code and an address during each bus cycle. The function code specifies an address space, and the address specifies a location within that address space. The function codes distinguish between user and supervisor spaces and, within these, between data and program spaces. This separation of address spaces provides the basis for memory management and protection by the operating system. Provision is also made for other bus masters to have separate address spaces for logical DMA.

MK68451
Figure 1



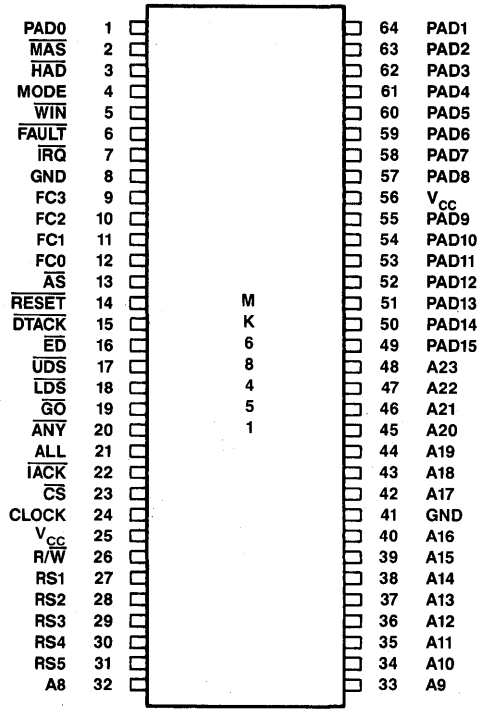
A multitasking operating system is simplified, and reliability is enhanced, through the use of the MMU.

The MK68451 memory management unit (MMU) is the basic element of a memory management mechanism (MMM) in an MK68000 family system. The operating system is responsible for insuring the proper execution of user tasks in the system environment, and memory management is basic to this responsibility. The MMM provides the operating system with the capability to allocate, control, and protect the system memory. A block diagram of a single-MMU system is shown in Figure 3.

An MMM, implemented with one or more MK68451 MMUs, can provide address translation, separation, and write protection for the system memory. The MMM can be programmed to cause an interrupt when a chosen section of memory is accessed, and can directly translate a logical address into a physical address, making it available to the MPU for use by the operating system. Using these features, the MMM can provide separation and security for user programs and allow the operating system to manage the memory in an efficient fashion for multitasking.

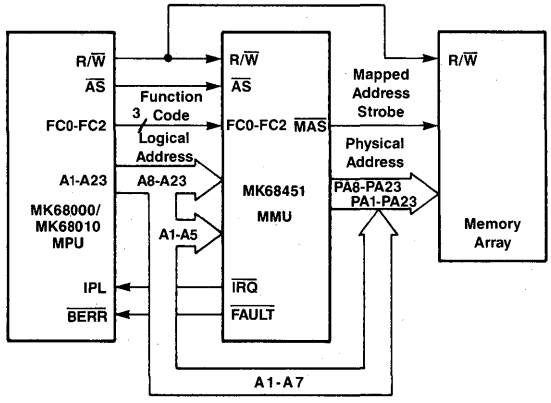
PIN ASSIGNMENT

Figure 2



SIMPLIFIED BLOCK DIAGRAM OF SINGLE-MMU SYSTEM

Figure 3



FUNCTIONAL DESCRIPTION

MEMORY SEGMENTS

The MMM partitions the logical address space into contiguous pieces called segments. Each segment is a section of the logical address space of a task which is mapped via the MMM into the physical address space. Each task may have any number of segments. Segments may be defined as user or supervisor, data-only or program-only, or program and data. They may be accessed by only one task or shared between two or more tasks. In addition, any segment can be write protected to insure system integrity. A fault (MK68000 bus error) is generated by the MMM if an undefined segment is accessed.

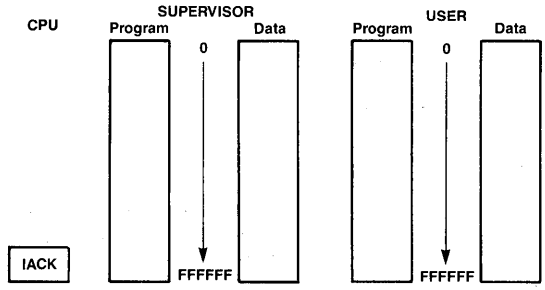
FUNCTION CODES AND ADDRESS SPACES

Each bus master in the MK68000 family provides a function code during each bus cycle to indicate the address space to be used for that cycle. The address bus then specifies a location within this address space for the operation taking place during that bus cycle.

The function codes appear on the FC0-FC2 lines of the MK68000 and divide the memory references into two logical address spaces—the supervisor and the user spaces. Each of these is further divided into program and data spaces. A separate address space is also provided for internal CPU-related activities, such as interrupt acknowledge, giving a total of five defined function codes. The address space of the MK68000 is shown in Figure 4.

ADDRESS SPACE OF MK68000

Figure 4



In addition to the 3-bit function code provided by the MK68000, the MK68451 MMU also allows a fourth bit (FC3) which provides for the possibility of another bus master in the system. In this case, FC3 would be a function of bus grant acknowledge ($\overline{BGACK}$) of the MK68000 to enable a second set of eight function codes. This raises the total number of possible function codes to 16. If there

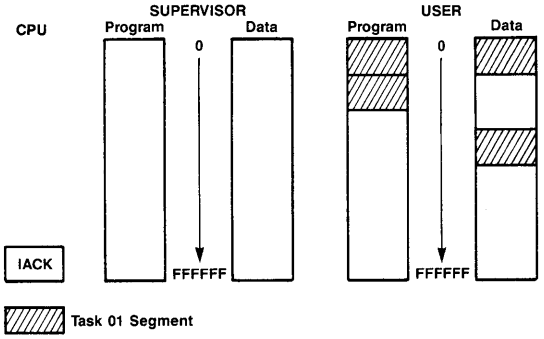
is only one bus master (the MPU), the FC3 pin on the MMU should be tied low, and only eight address spaces can then be used.

ADDRESS SPACE NUMBER

Each task in a system has an address space comprised of all the segments defined for that task. This address space is assigned a number by programming all the address space number (ASN) fields in its descriptors with the same value. This value can be considered a task number. The currently active task's number is kept in the appropriate entry(s) in the address space table (AST).

The AST is a set of MMU registers that defines which task's segments are to be used in address translation for each cycle type (supervisor program, supervisor data, etc.). The AST contains an 8-bit entry for each possible function code. Each entry is assigned an ASN (task number) and this is used to select which descriptors may be used for translation. The logical address is then translated by one of these to produce the physical address. Figure 5 is a typical memory map of a task's address space.

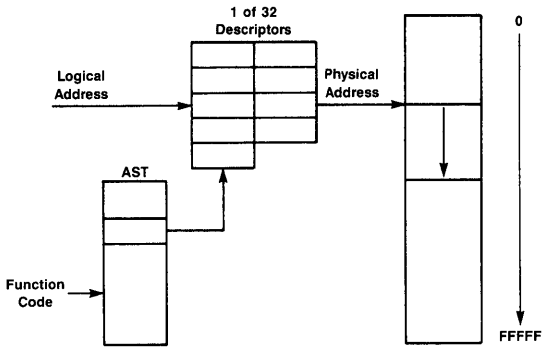
MEMORY MAP OF TYPICAL TASK ADDRESS SPACE
Figure 5



DESCRIPTORS

Address translation is done using descriptors. A descriptor is a set of six registers (nine bytes) which describe a memory segment and how that segment is to be mapped to the physical addresses. Each descriptor contains base addresses for the logical address masks. The size of the segment is then defined by "don't cares" in the masks. This method allows segment sizes from a minimum of 256 bytes to a maximum of 16 megabytes in binary increments (i.e., powers of two). This also forces both logical and physical addresses of segment boundaries to lie on a segment size boundary. That is, a segment can only start on an address which is a multiple of 2k. The segments can be defined in such a way to allow them to be logically or physically shared between tasks. Descriptor mapping is shown schematically in Figure 6.

SCHEMATIC DIAGRAM OF DESCRIPTOR MAPPING
Figure 6

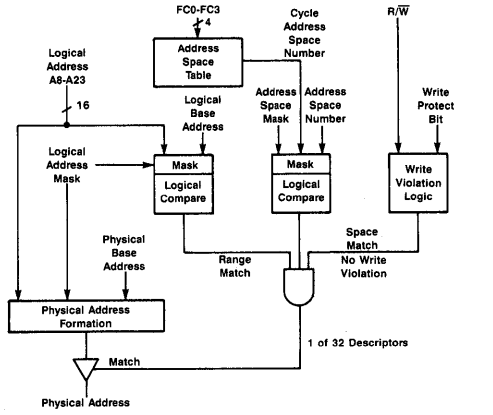


TRANSLATION

During normal translation, the MMU translates the logical address provided by the MK68000 to produce a physical address which is then presented to the memory array. This is accomplished by matching the logical address with the information in the descriptors and then mapping it into the physical address space. A block diagram of the MK68451 is shown in Figure. 7

Refer to Figure 3 for the following information. The logical address is composed of address lines A1-A23. The upper 16 bits of this address (A8-A23) are translated by the MMU and mapped into a physical address (PA8-PA23). The lower seven bits of the logical address (A1-A7) bypass the MMU and become the low-order physical address bits (PA1-PA7). In addition, the data strobes ($\overline{UDS}$ and $\overline{LDS}$) remain unmapped to become the physical data strobes for a total of eight unmapped address lines.

FUNCTIONAL BLOCK DIAGRAM
Figure 7



ORDERING INFORMATION

Part Number	Package Type	Max Clock Frequency	Temperature Range
MK68451N-8	Plastic	8.0 MHz	0° to 70°C
MK68451N-10	Plastic	10.0 MHz	0° to 70°C

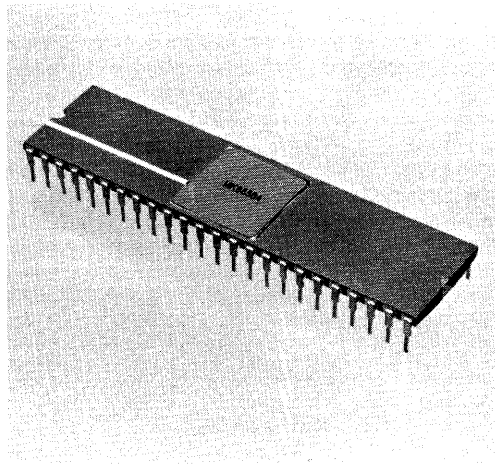
PRELIMINARY

SERIAL INPUT/OUTPUT CONTROLLER MK68564

FEATURES

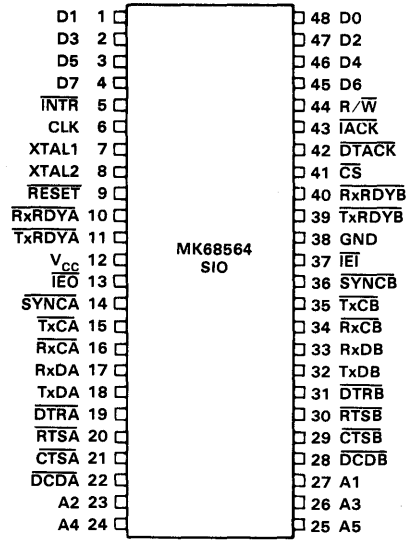
- ☐ Compatible with MK68000 CPU
- ☐ Compatible with MK68000 Series DMA's
- ☐ Two independent, full-duplex channels
- ☐ Two independent baud rate generators
  - Crystal oscillator input
  - Single-phase TTL clock input
- ☐ Directly addressable registers (all control registers are read/write)
- ☐ Data rate in synchronous or asynchronous modes
  - 0-1 M bits/second with 5.0 MHz system clock rate
- ☐ Self-test capability
- ☐ Receive data registers are quadruply buffered; transmit data registers are doubly buffered
- ☐ Daisy-chain priority interrupt logic provides automatic interrupt vectoring without external logic
- ☐ Modem status can be monitored
  - Separate modem controls for each channel
- ☐ Asynchronous features
  - 5, 6, 7, or 8 bits/character
  - 1, 1½, or 2 stop bits
  - Even, odd, or no parity
  - x1, x16, x32, and x64 clock modes
  - Break generation and detection
  - Parity, overrun, and framing error detection
- ☐ Byte synchronous features
  - Internal or external character synchronization
  - One or two sync characters in separate registers
  - Automatic sync character insertion
  - CRC-16 or CRC-CCITT block check generation and checking
- ☐ Bit synchronous features
  - Abort sequence generation and detection
  - Automatic zero insertion and deletion
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - Valid receive messages protected from overrun
  - CRC-CCITT block check generation and checking

MK68564
Figure 1



PIN DESCRIPTION

Figure 2



GENERAL DESCRIPTION

The MK68564 SIO is a dual-channel, Serial Input/Output Controller, designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller; however, within that role, it is systems software configurable so that it may be optimized for any given serial data communications application.

The MK68564 is capable of handling asynchronous protocols, synchronous byte-oriented protocols (such as IBM Bisync), and synchronous bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device can also be used to support virtually any serial protocol for applications other than data communications (cassette or floppy disk interface, for example).

The MK68564 can generate and check CRC codes in any synchronous mode and may be programmed to check data integrity in various modes. The device also has facilities for modem controls in each channel. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O.

SIO PIN DESCRIPTION

GND:	Ground.
V_{CC}:	+5 volts (±5%).
$\overline{CS}$: Chip Select	Input active low. $\overline{CS}$ is used to select the MK68564 SIO for access to the internal registers. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.
R/$\overline{W}$: Read/Write	Input. R/$\overline{W}$ is the signal from the bus master, indicating whether the current bus cycle is a read (high) or write (low) cycle.
$\overline{DTACK}$: Data Transfer Acknowledge	Output, active low, tri-stateable. $\overline{DTACK}$ is used to signal the bus master that data is ready or that data has been accepted by the MK68564 SIO.
A1-A5: Address Bus	Inputs. The address bus is used to select one of the internal registers during a read or write cycle.
D0-D7: Data Bus	Bidirectional, tri-stateable. The data bus is used to transfer data to or from the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.
CLK: Clock	Input. This input is used to provide the internal timing for the MK68564 SIO.
$\overline{RESET}$ Device Reset	Input, active low. $\overline{Reset}$ disables both receivers and transmitters, forces TxDA and TxDB to a marking condition, forces the modem controls high, and disables all interrupts. With the exception of the status registers, data registers, and the vector register, all internal registers are cleared. The vector register is reset to "0FH".
$\overline{INTR}$ Interrupt Request	Output, active low, open drain. $\overline{INTR}$ is asserted when the MK68564 SIO is requesting an interrupt. $\overline{INTR}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.
$\overline{IACK}$ Interrupt Acknowledge	Input, active low. $\overline{IACK}$ is used to signal the MK68564 SIO that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time. If interrupts are not used then $\overline{IACK}$ should be pulled high.
$\overline{IEI}$ Interrupt Enable In	Input, active low. $\overline{IEI}$ is used to signal the MK68564 SIO that no higher priority device is requesting interrupt service.
$\overline{IEO}$ Interrupt Enable Out	Output, active low. $\overline{IEO}$ is used to signal lower priority peripherals that neither the MK68564 SIO nor another higher priority peripheral is requesting interrupt service.
XTAL1 XTAL2 Baud Rate Generator Inputs	Inputs.A crystal may be connected between XTAL1 and XTAL2, or XTAL1 may be driven with a TTL level clock. When using a crystal, external capacitors must be connected. When driving XTAL1 with a TTL level clock, XTAL2 must be allowed to float.
$\overline{RxRDYA}$ $\overline{RxRDYB}$ Receiver Ready	Outputs, active low. Programmable DMA output for the receiver. The $\overline{RxRDY}$ pins pulse low when a character is available in the receive buffer.
$\overline{TxRDYA}$ $\overline{TxRDYB}$ Transmitter Ready	Outputs, active low. Programmable DMA output for the transmitter. The $\overline{TxRDY}$ pins pulse low when the transmit buffer is empty.
$\overline{CTSA}$ $\overline{CTSB}$ Clear to Send	Inputs, active low. If Tx Auto Enables is selected, these inputs enable the transmitter of their respective channels. If Tx Auto Enables is not selected, these inputs may be used as general purpose input pins. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.

$\overline{DCDA}$ $\overline{DCDB}$ Data Carrier Detect	Inputs, active low. If Rx Auto Enables is selected, these inputs enable the receiver of their respective channels. If Rx Auto Enable is not selected, these inputs may be used as general purpose input pins. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.
RxDA RxDB Receive Data	Inputs, active high. Serial data input to the receiver.
TxDA TxDB Transmit Data	Outputs, active high. Serial data output of the transmitter.
$\overline{RxCA}$ $\overline{RxCB}$ Receiver Clocks	Input/output. Programmable pin, receive clock input, or baud rate generator output. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.
$\overline{TxCA}$ $\overline{TxCB}$ Transmitter Clocks	Input/output. Programmable pin, transmit clock input, or baud rate generator output. The inputs are Schmitt-trigger buffered to allow slow rise-time input signals.
$\overline{RTSA}$ $\overline{RTSB}$ Request to Send	Outputs, active low. These outputs follow the inverted state programmed into the RTS bit. When the RTS bit is reset in the asynchronous mode, the output will not change until the character in the transmitter is completely shifted out. These pins may be used as general purpose outputs.
$\overline{DTRA}$ $\overline{DTRB}$ Data Terminal Ready	Outputs, active low. These outputs follow the inverted state programmed into the DTR bit. These pins may also be used as general purpose outputs.
$\overline{SYNCA}$ $\overline{SYNCB}$ Synchroníz-ation	Input/output, active low. The $\overline{SYNC}$ pin is an output when Monosync, Bisync, or SDLC mode is programmed. It is asserted when a sync/flag character is detected by the receiver. The $\overline{SYNC}$ pin is a general purpose input in the Asynchronous mode and an input to the receiver in the External Sync mode.

MK68564 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −.3 V to +7 V
Power Dissipation . . . . . 1.5 Watt

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 V ± 5%, GND = 0 Vdc, T_A = 0 to 70°C)

CHARACTERISTIC	SYM	MIN	MAX	UNIT
INPUT HIGH VOLTAGE ALL INPUTS	V_{IH}	GND + 2.0	V_{CC}	V
INPUT LOW VOLTAGE ALL INPUTS	V_{IL}	GND −0.3	GND +0.8	V
POWER SUPPLY CURRENT OUTPUTS OPEN	I_{LL}		190	mA
INPUT LEAKAGE CURRENT (V_{IN} = 0 to 5.25)	I_{IN}		±10	μA
THREE-STATE (OFF STATE) INPUT CURRENT $0 < V_{IN} < V_{CC}$ $\overline{DTACK}$, D0-D7, $\overline{SYNC}$, $\overline{TxC}$, $\overline{RxC}$, $\overline{INTR}$	I_{TSI}		20 ±10	μA μA
OUTPUT HIGH VOLTAGE (I_{LOAD} = −400 μA, V_{CC}=MIN) $\overline{DTACK}$, D0-D7 (I_{LOAD} = −150μA, V_{CC}=MIN) ALL OTHER OUTPUTS (EXCEPT XTAL2 & $\overline{INTR}$)*	V_{OH}	GND+2.4		V
OUTPUT LOW VOLTAGE (I_{LOAD}=5.3 mA, V_{CC}=MIN) $\overline{INTR}$, $\overline{DTACK}$, D0-D7 (I_{LOAD}=2.4 mA, V_{CC}=MIN) ALL OTHER OUTPUTS (EXCEPT XTAL2)*	V_{OL}		0.5	V

*XTAL2 SPECIAL
$\overline{INTR}$ (OPEN DRAIN)

CAPACITANCE

T_A=25°C, f=1 MHz unmeasured pins returned to ground.

CHARACTERISTIC	SYM	MAX	UNIT	TEST CONDITION
Input Capacitance $\overline{CS}$, $\overline{IACK}$	C_{IN}	15	pf	Unmeasured pins returned to ground
ALL OTHERS		10	pf	
Tri-state Output Capacitance	C_{OUT}	10	pf	

AC ELECTRICAL CHARACTERISTICS
(V_{CC}=5.0 Vdc±5%, GND=0 Vdc, T_A=0 to 70°C)

NUMBER	PARAMETER	3.0 MHz		4.0 MHz		5.0 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
1	CLK Period	330	1000	250	1000	200	1000	ns	
2	CLK Width High	145		105		80		ns	
3	CLK Width Low	145		105		80		ns	
4	CLK Fall Time		30		30		30	ns	
5	CLK Rise Time		30		30		30	ns	
6	$\overline{CS}$ Low to CLK High (Setup Time)	0		0		0		ns	1
7	A1-A5 Valid to $\overline{CS}$ Low (Setup Time)	0		0		0		ns	
8	DATA Valid to $\overline{CS}$ Low (Write Cycle)	0		0		0		ns	
9	$\overline{CS}$ Width High	50		50		50		ns	1
10	$\overline{DTACK}$ Low to A1-A5 Invalid (Hold Time)	0		0		0		ns	
11	$\overline{DTACK}$ Low to DATA Invalid (Write Cycle Hold Time)	0		0		0		ns	
12	$\overline{CS}$ High to $\overline{DTACK}$ High (Delay)		60		55		50	ns	
13	CLK High to $\overline{DTACK}$ Low		325		320		295	ns	
14	R/$\overline{W}$ Valid to $\overline{CS}$ Low (Setup Time)	0		0		0		ns	
15	$\overline{DTACK}$ Low to R/$\overline{W}$ Invalid (Hold Time)	0		0		0		ns	
16	CLK Low to DATA Out		550		450		450	ns	
17	$\overline{CS}$ High to DATA Out Invalid (Hold Time)	0		0		0		ns	
18	$\overline{CS}$ High to $\overline{DTACK}$ High Impedance		110		105		100	ns	
19	$\overline{DTACK}$ Low to $\overline{CS}$ High	0		0		0		ns	
20	DATA Valid to $\overline{DTACK}$ Low	70		70		70		ns	
21	$\overline{IACK}$ Width High	50		50		50		ns	1
22	$\overline{IACK}$ Low to CLK High (Setup Time)	0		0		0		ns	1
23	CLK Low to $\overline{INTR}$ Disabled		410		410		410	ns	2
24	CLK Low to DATA Out		330		330		330	ns	2
25	$\overline{DTACK}$ Low to $\overline{IACK}$ High	0		0		0		ns	
26	$\overline{IACK}$ High to $\overline{DTACK}$ High		60		55		50	ns	
27	$\overline{IACK}$ High to $\overline{DTACK}$ High Impedance		110		105		100	ns	
28	$\overline{IACK}$ High to DATA Out Invalid (Hold Time)	0		0		0		ns	
29	DATA Valid to $\overline{DTACK}$ Low	195		195		195		ns	2
30	CLK Low to $\overline{IEO}$ Low		220		220		220	ns	3

VI

AC ELECTRICAL CHARACTERISTICS (Cont.)
(V_{CC}=5.0 Vdc±5%, GND=0 Vdc, T_A=0 to 70°C)

NUMBER	PARAMETER	3.0 MHz		4.0 MHz		5.0 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
31	$\overline{IEI}$ Low to $\overline{IEO}$ Low		140		140		140	ns	3
32	$\overline{IEI}$ High to $\overline{IEO}$ High		190		190		190	ns	4
33	$\overline{IACK}$ High to $\overline{IEO}$ High		190		190		190	ns	4
34	$\overline{IACK}$ High to $\overline{INTR}$ Low		200		200		200	ns	5
35	$\overline{IEI}$ Low to CLK Low (Setup Time)	10		10		10		ns	
36	$\overline{IEI}$ Low to $\overline{INTR}$ Disabled		500		425		425	ns	6
37	$\overline{IEI}$ Low to DATA Out Valid		225		225		225	ns	6
38	DATA Out Valid to $\overline{DTACK}$ Low	55		55		55		ns	6
39	$\overline{IACK}$ High to DATA Out High Impedance		150		120		90	ns	
40	$\overline{CS}$ High to DATA Out High Impedance		150		120		90	ns	
41	$\overline{CS}$ or $\overline{IACK}$ High to CLK Low	100		100		100		ns	7
42	$\overline{TxRDY}$ or $\overline{RxRDY}$ Width Low		3		3		3	CLK Period	8,10
43	CLK High to $\overline{TxRDY}$ or $\overline{RxRDY}$ Low		300		300		300	ns	
44	CLK High to $\overline{TxRDY}$ or $\overline{RxRDY}$ High		335		300		300	ns	
	$\overline{IACK}$ High to $\overline{CS}$ Low or $\overline{CS}$ High to $\overline{IACK}$ Low (not shown)	50		50		50		ns	1
45	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ Pulse Width High	200		200		200		ns	
46	$\overline{CTS}$, $\overline{DCD}$, $\overline{SYNC}$ Pulse Width Low	200		200		200		ns	
47	$\overline{TxC}$ Period	1320	DC	1000	DC	800	DC	ns	9
48	$\overline{TxC}$ Width Low	180	DC	180	DC	180	DC	ns	
49	$\overline{TxC}$ Width High	180	DC	180	DC	180	DC	ns	
50	$\overline{TxC}$ Low to TxD Delay (X1 Mode)		300		300		300	ns	
51	$\overline{TxC}$ Low to $\overline{INTR}$ Low Delay	5	9	5	9	5	9	CLK Period	10
52	$\overline{RxC}$ Period	1320	DC	1000	DC	800	DC	ns	9
53	$\overline{RxC}$ Width Low	180	DC	180	DC	180	DC	ns	
54	$\overline{RxC}$ Width High	180	DC	180	DC	180	DC	ns	
55	RxD to $\overline{RxC}$ High Setup Time (X1 Mode)	0		0		0		ns	
56	$\overline{RxC}$ High to RxD Hold Time (X1 Mode)	140		140		140		ns	
57	$\overline{RxC}$ High to $\overline{INTR}$ Low Delay	10	13	10	13	10	13	CLK Period	10
58	$\overline{RxC}$ High to $\overline{SYNC}$ Low Delay (Output Modes)	4	7	4	7	4	7	CLK Period	10

AC ELECTRICAL CHARACTERISTICS (Cont.)

(V_{CC}=5.0 Vdc±5%, GND=0 Vdc, T_A=0 to 70°C)

NUMBER	PARAMETER	3.0 MHz		4.0 MHz		5.0 MHz		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
59	$\overline{\text{RESET}}$ Low	1		1		1		CLK Period	10
60	XTAL 1 Width High (TTL in)	145		100		80		ns	
61	XTAL 1 Width Low (TTL in)	145		100		80		ns	
62	XTAL 1 Period (TTL in)	330	2000	250	2000	200	2000	ns	
63	XTAL 1 Period (Crystal in)	330	1000	250	1000	200	1000	ns	

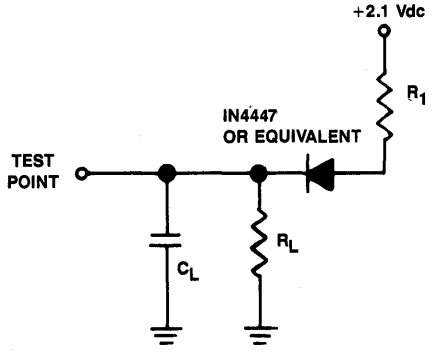
NOTES:

1. This specification only applies if the SIO has completed all operations initiated by the previous bus cycle, when $\overline{CS}$ or $\overline{IACK}$ was asserted. Following a read, write, or interrupt acknowledge cycle, all operations are complete within two CLK cycles after the rising edge of $\overline{CS}$ or $\overline{IACK}$. If $\overline{CS}$ or $\overline{IACK}$ is asserted prior to the completion of the internal operations, the new bus cycle will be postponed.
2. If $\overline{IEI}$ meets the setup time to the falling edge of CLK, 1½ cycles following the clocking in of $\overline{IACK}$.
3. No internal interrupt request pending at the start of an interrupt acknowledge cycle.
4. Time starts when first signal goes invalid (high).
5. If an internal interrupt is pending at the end of the interrupt acknowledge cycle.
6. If Note 2 timing is not met.
7. If this spec is met, the delay listed in note 1 will be one CLK cycle instead of two.
8. Ready signals will be negated asynchronous to the CLK, if the condition causing the assertion of the signals is cleared.
9. If $\overline{RxC}$ and $\overline{TxC}$ are asynchronous to the System Clock, the maximum clock rate into $\overline{RxC}$ and $\overline{TxC}$ should be no more than one-fifth the System Clock rate. If $\overline{RxC}$ and $\overline{TxC}$ are synchronized to the falling edge of the System Clock, the maximum clock rate into $\overline{RxC}$ and $\overline{TxC}$ can be one-fourth the System Clock rate.
10. SIO Clock (CLK) Cycles as defined in Parameter 1.

VI

OUTPUT TEST LOAD

Figure 3



for all outputs except $\overline{DTACK}$, D0-D7, $\overline{INTR}$, XTAL2

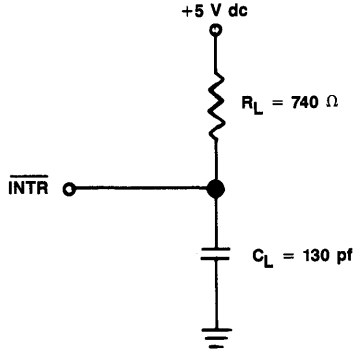
C_L = 130 pf
R_L = 16K Ω
R_1 = 450 Ω

for $\overline{DTACK}$, D0-D7

C_L = 130 pf
R_L = 6K Ω
R_1 = 200 Ω

$\overline{INTR}$ TEST LOAD

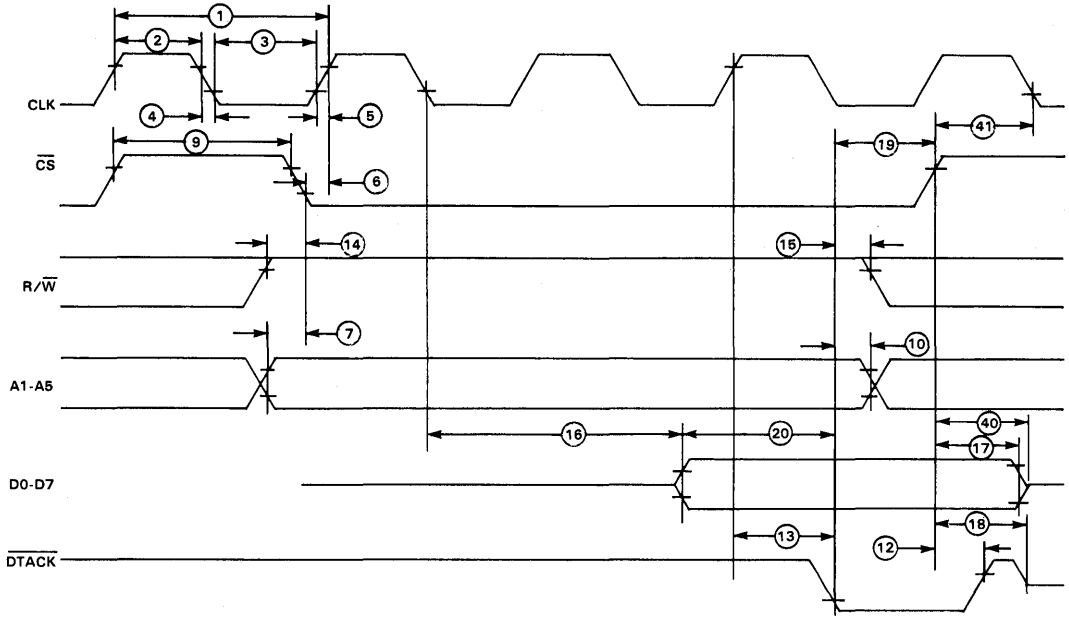
Figure 4



NOTE:
XTAL2 output test load is a cyrstal.

READ CYCLE

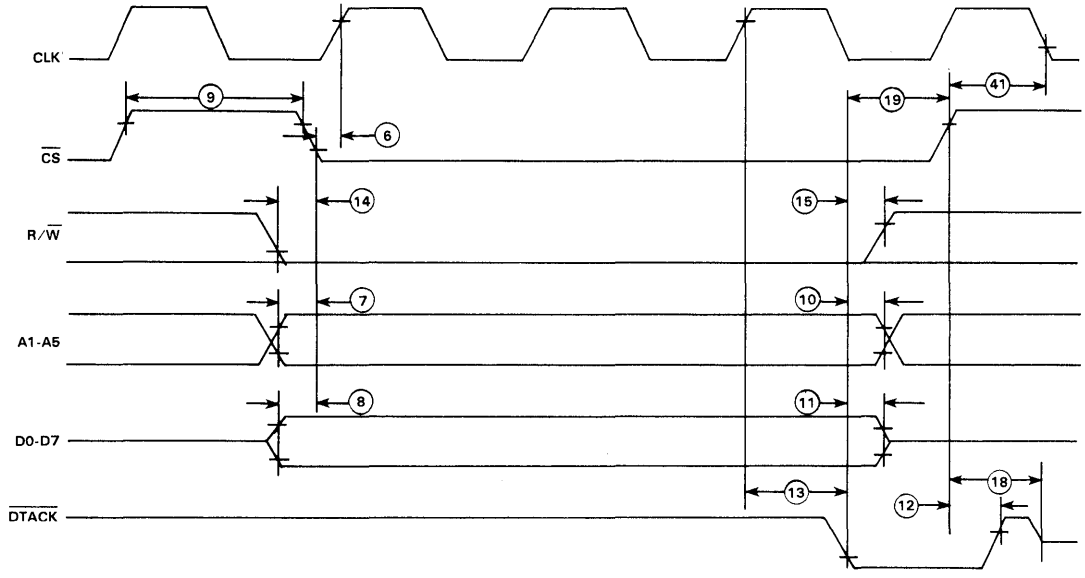
Figure 5



NOTE:
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

WRITE CYCLE

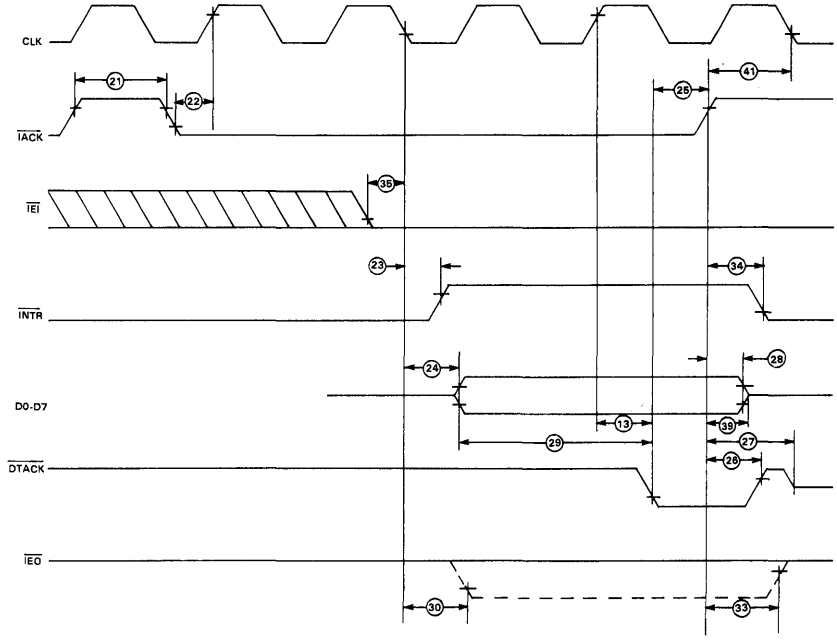
Figure 6



NOTE:
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ LOW)

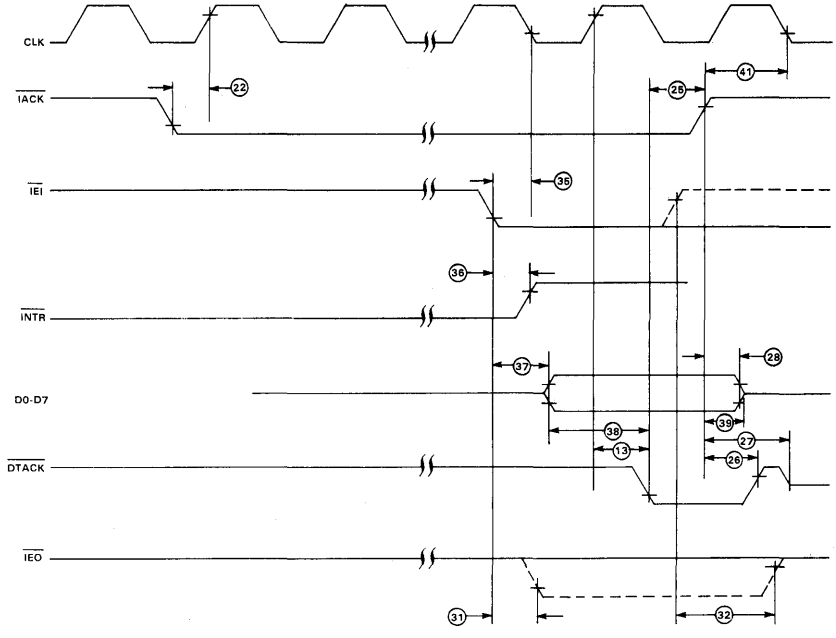
Figure 7



NOTE:
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ HIGH)

Figure 8

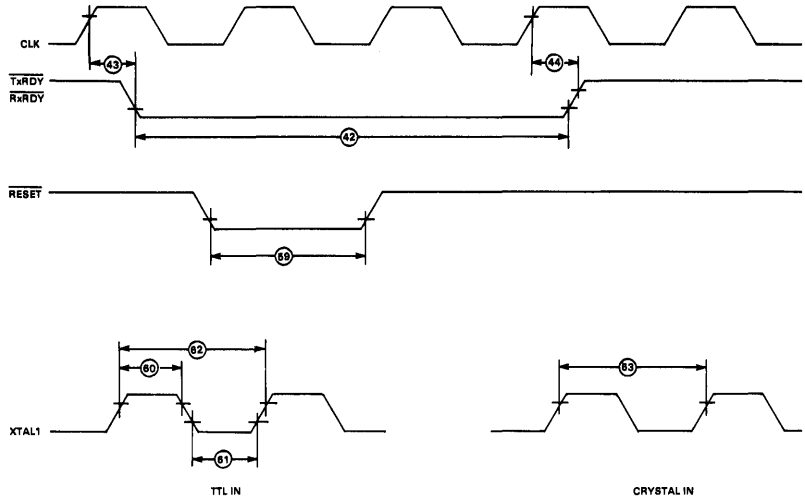


NOTE:
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

VI

DMA INTERFACE TIMING

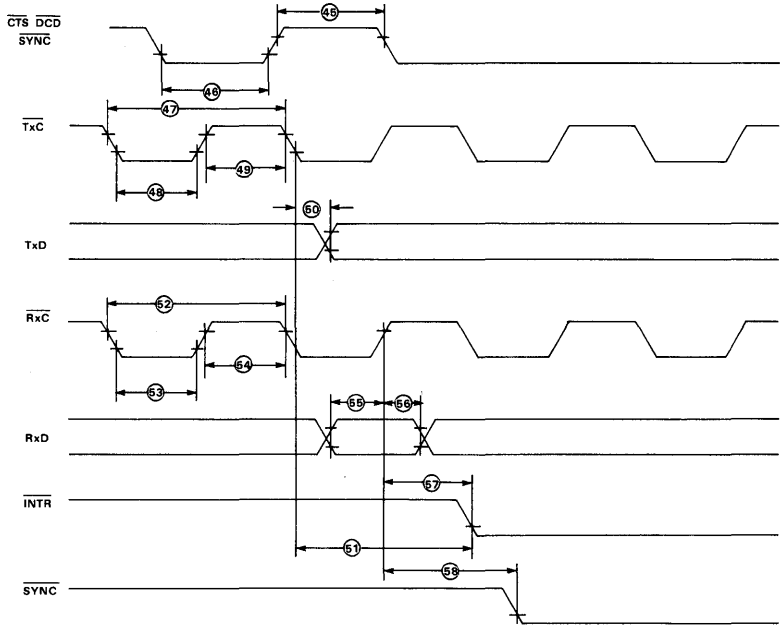
Figure 9



NOTE:
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

SERIAL INTERFACE TIMING

Figure 10



NOTE:
Waveform measurements for all inputs and outputs are specified at logic high = 2.0 volts, logic low = 0.8 volts.

MK68564 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX. CLOCK FREQUENCY	TEMPERATURE RANGE
MK68564N-03	Plastic	3.0 MHz	0° to 70°C
MK68564N-04	Plastic	4.0 MHz	0° to 70°C
MK68564N-05	Plastic	5.0 MHz	0° to 70°C

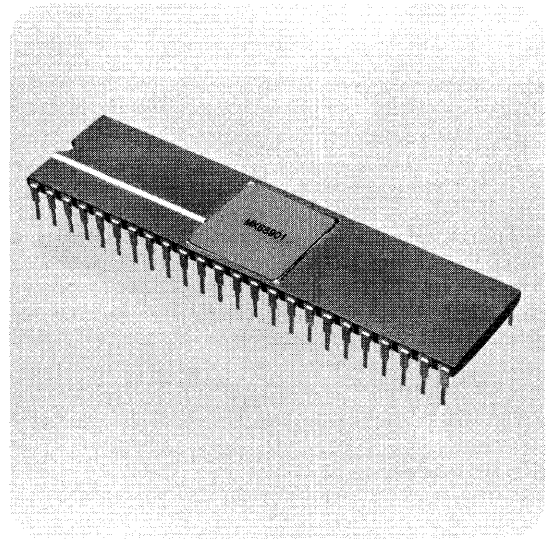
PRELIMINARY

MK68901
MULTI-FUNCTION PERIPHERAL

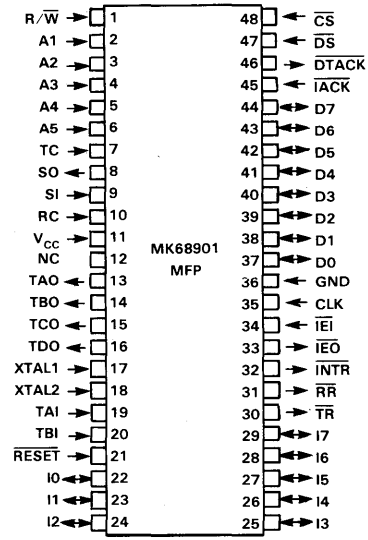
FEATURES

- 8 Input/Output Pins
  - Individually programmable direction
  - Individual interrupt source capability
    - Programmable edge selection
- 16 Source interrupt controller
  - 8 Internal sources
  - 8 External sources
  - Individual source enable
  - Individual source masking
  - Programmable interrupt service modes
    - Polling
    - Vector generation
      - Optional In-service status
  - Daisy chaining capability
- Four timers with individually programmable prescaling
  - Two multimode timers
    - Delay mode
    - Pulse width measurement mode
    - Event counter mode
  - Two delay mode timers
  - Independent clock input
  - Time out output option
- Single channel USART
  - Full Duplex
  - Asynchronous to 62.5 kbps
  - Byte synchronous to 1 Mbps
  - Internal/external baud rate generation
  - DMA handshake signals

MK68901
Figure 1



DEVICE PINOUT
Figure 2



- Modem control
- Loop back mode

□ 68000 Bus compatible

□ 48 Pin DIP

INTRODUCTION

The MK68901 MFP (Multi-Function Peripheral) is a combination of many of the necessary peripheral functions in a microprocessor system. Included are:

Eight parallel I/O lines

Interrupt controller for 16 sources

Four timers

Single channel full duplex USART

The use of the MFP in a system can significantly reduce chip count, thereby reducing system cost. The MFP is completely 68000 bus compatible, and 24 directly addressable internal registers provide the necessary control and status interface to the programmer.

The MFP is a derivative of the MK3801 STI, a Z80 family peripheral.

PIN DESCRIPTION

GND: Ground

Vcc: +5 volts (± 5%)

$\overline{CS}$: Chip Select (input, active low). $\overline{CS}$ is used to select the MK68901 MFP for accesses to the internal registers. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

$\overline{DS}$: Data Strobe (input, active low). $\overline{DS}$ is used as part of the chip select and interrupt acknowledge functions.

R/$\overline{W}$: Read/Write (input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle.

$\overline{DTACK}$: Data Transfer Acknowledge. (output, active low, tri-stateable). $\overline{DTACK}$ is used to signal the bus master that data is ready, or that data has been accepted by the MK68901 MFP.

A1-A5: Address Bus (inputs). The address bus is used to address one of the internal registers during a read or write cycle.

D_0-D_7: Data Bus (bi-directional, tri-stateable). The data bus is used to receive data from or transmit data to one of the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.

CLK: Clock (input). This input is used to provide the internal timing for the MK68901 MFP.

$\overline{RESET}$: Device reset. (input, active low). Reset disables the USART receiver and transmitter, stops all timers and forces the timer outputs low, disables all interrupt channels and clears any pending interrupts. The General Purpose Interrupt/ I/O lines will be placed in the tri-state input mode. All internal registers (except the timer, USART data registers, and transmit status register) will be cleared.

$\overline{INTR}$: Interrupt Request (output, active low, open drain). $\overline{INTR}$ is asserted when the MK68901 MFP is requesting an interrupt. $\overline{INTR}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.

$\overline{IACK}$: Interrupt Acknowledge (input, active low). $\overline{IACK}$ is used to signal the MK68901 MFP that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

$\overline{IEI}$: Interrupt Enable In (input, active low). $\overline{IEI}$ is used to signal the MK68901 MFP that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the MK68901 MFP nor another higher priority peripheral is requesting interrupt service.

I_0-I_7: General Purpose Interrupt I/O lines. These lines may be used as interrupt inputs and/or I/O lines. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.

SO: Serial Output. This is the output of the USART transmitter.

SI: Serial Input. This is the input to the USART receiver.

RC: Receiver Clock. This input controls the serial bit rate of the USART receiver.

TC: Transmitter Clock. This input controls the serial bit rate of the USART transmitter.

$\overline{RR}$: Receiver Ready. (output, active low) DMA output for receiver, which reflects the status of Buffer Full in port number 15.

$\overline{TR}$: Transmitter Ready. (output, active low) DMA output for transmitter, which reflects the status of Buffer Empty in port number 16.

TAO,TBO, TCO, TDO: Timer Outputs. Each of the four timers has an output which can produce a square wave. The output will change states each timer cycle; thus one full period of the timer out signal is equal to two timer cycles. TAO or TBO can be reset (logic "0") by a write to TACR, or TBCR respectively.

XTAL1, XTAL2: Timer Clock inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with a TTL level clock. When driving XTAL1 with a TTL level clock, XTAL2 must be allowed to float. When using a crystal, external capacitors are required. See Figure 27. All chip accesses are independent of the timer clock.

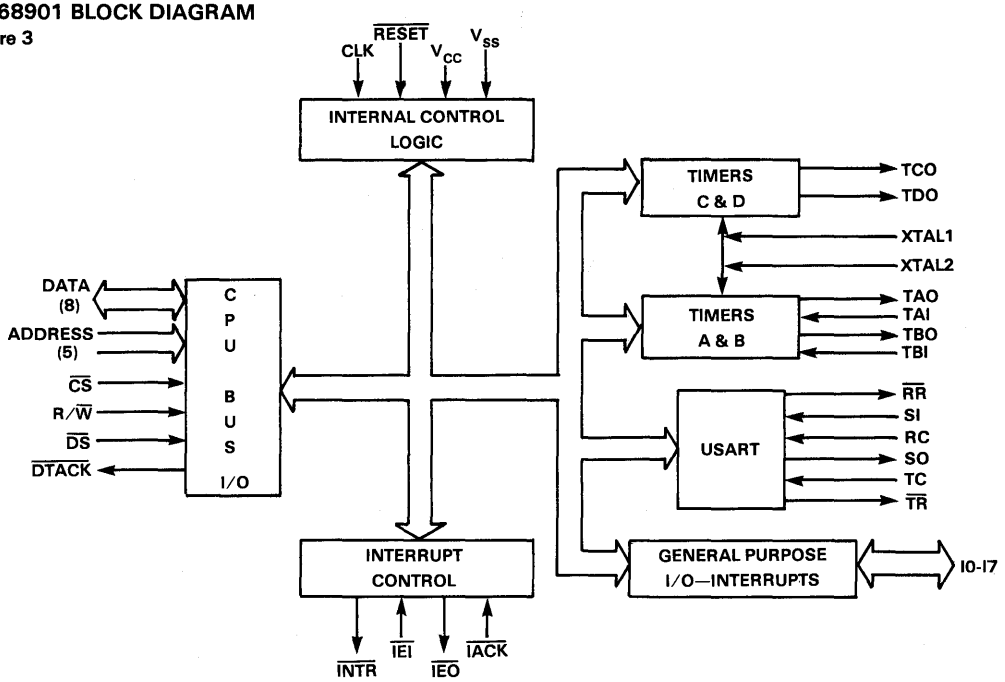
TAI,TBI: Timer A,B inputs. Used when running the timers in the event count or the pulse width measurement mode. The interrupt channels associated with I4 and I3 are used for TAI and TBI, respectively. Thus, when running a timer in the pulse width measurement mode, I4 or I3 can be used for I/O only.

REGISTER MAP
Figure 4

Address Port No.	Abbreviation	Register Name
0	GPIP	GENERAL PURPOSE I/O
1	AER	ACTIVE EDGE REGISTER
2	DDR	DATA DIRECTION REGISTER
3	IERA	INTERRUPT ENABLE REGISTER A
4	IERB	INTERRUPT ENABLE REGISTER B
5	IPRA	INTERRUPT PENDING REGISTER A
6	IPRB	INTERRUPT PENDING REGISTER B
7	ISRA	INTERRUPT IN-SERVICE REGISTER A
8	ISRB	INTERRUPT IN-SERVICE REGISTER B
9	IMRA	INTERRUPT MASK REGISTER A
A	IMRB	INTERRUPT MASK REGISTER B
B	VR	VECTOR REGISTER
C	TACR	TIMER A CONTROL REGISTER
D	TBCR	TIMER B CONTROL REGISTER
E	TCDCR	TIMERS C AND D CONTROL REGISTER
F	TADR	TIMER A DATA REGISTER
10	TBDR	TIMER B DATA REGISTER
11	TCDR	TIMER C DATA REGISTER
12	TDDR	TIMER D DATA REGISTER
13	SCR	SYNC CHARACTER REGISTER
14	UCR	USART CONTROL REGISTER
15	RSR	RECEIVER STATUS REGISTER
16	TSR	TRANSMITTER STATUS REGISTER
17	UDR	USART DATA REGISTER

VI

MK68901 BLOCK DIAGRAM
Figure 3



INTERRUPTS

The General Purpose I/O-Interrupt Port (GPIP) provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt on either a positive going edge or a negative going edge of the input signal.

The GPIP has three associated registers. One allows the programmer to specify the Active Edge for each bit that will trigger an interrupt. Another register specifies the Data Direction (input or output) associated with each bit. The third register is the actual data I/O register used to input or output data to the port. These three registers are illustrated in Figure 5.

The Active Edge Register (AER) allows each of the General Purpose Interrupts to produce an interrupt on either a 1-0 transition or a 0-1 transition. Writing a zero to the appropriate bit of the AER causes the associated input to produce an interrupt on the 1-0 transition, while a 1 causes the interrupt on the 0-1 transition. The edge bit is simply one input to an exclusive-or gate, with the other input coming from the input buffer and the output going to a 1-0 transition detector. Thus, depending upon the state of the input, writing the AER can cause an interrupt-producing transition, which will cause an interrupt on the associated channel, if that channel is enabled. One would then normally configure the AER before enabling interrupts via IERA and IERB. Note: changing the edge bit, with the interrupt enabled, may cause an interrupt on that channel.

The Data Direction Register (DDR) is used to define I0-I7 as inputs or as outputs on a bit by bit basis. Writing a zero into a bit of the DDR causes the corresponding Interrupt-I/O pin to be a Hi-Z input. Writing a one into a bit of the DDR causes the corresponding pin to be configured as a push-pull output. When data is written into the GPIP, those pins defined as inputs will remain in the Hi-Z state while those pins defined as outputs will assume the state (high or low) of their corresponding bit in the GPIP. When the GPIP is read, the data read will come directly from the corresponding bit of the GPIP register for all pins defined as output, while the data read on all pins defined as inputs will come from the input buffers.

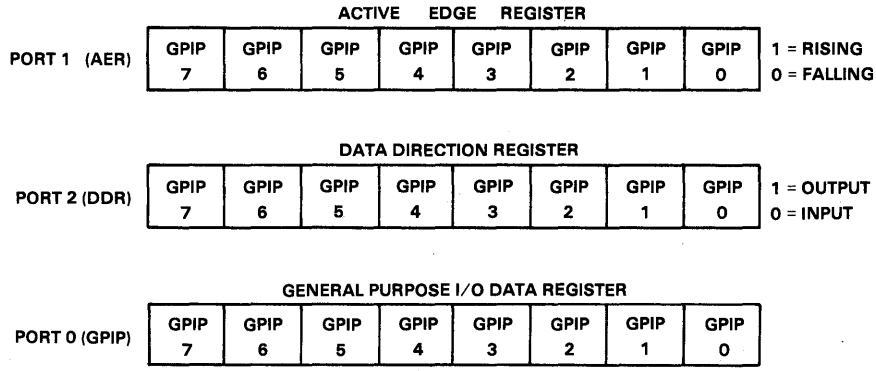
Each individual function in the MK68901 is provided with a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during the interrupt acknowledge cycle is shown in Figure 6, while the vector register is shown in Figure 7.

There are 16 vector addresses generated internally by the MK68901, one for each of the 16 interrupt channels.

The Interrupt Control Registers (Figure 8) provide control of interrupt processing for all I/O facilities of the MK68901. These registers allow the programmer to enable or disable

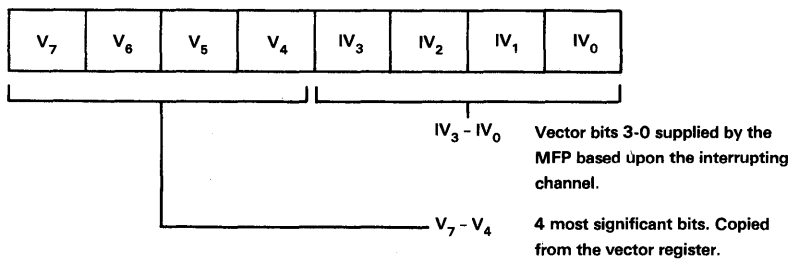
GENERAL PURPOSE I/O REGISTERS

Figure 5



INTERRUPT VECTOR

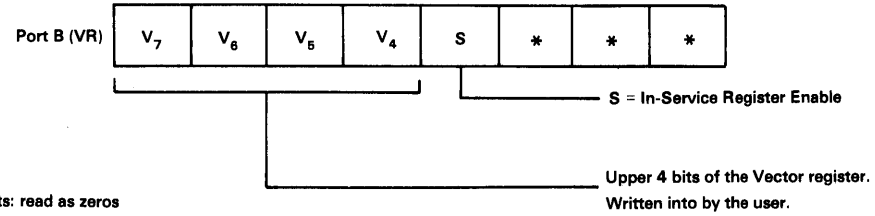
Figure 6



any or all of the 16 interrupts, providing masking for any interrupts, and provide access to the pending and in-service status of the interrupts. Optional end-of-interrupt modes are available under software control. All the interrupts are prioritized as shown in Figure 9.

VECTOR REGISTER

Figure 7



INTERRUPT CONTROL REGISTERS

Figure 8

INTERRUPT ENABLE REGISTERS

ADDRESS		7	6	5	4	3	2	1	0
PORT 3	A (IERA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
PORT 4	B (IERB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

INTERRUPT PENDING REGISTERS

		7	6	5	4	3	2	1	0
PORT 5	A (IPRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
PORT 6	B (IPRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

WRITING 0 = CLEAR
WRITING 1 = UNCHANGED

INTERRUPT IN-SERVICE REGISTERS

		7	6	5	4	3	2	1	0
PORT 7	A (ISRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
PORT 8	B (ISRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

INTERRUPT MASK REGISTERS

		7	6	5	4	3	2	1	0
PORT 9	A (IMRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
PORT A	B (IMRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

1 = UNMASKED 0 = MASKED

INTERRUPT CONTROL REGISTER DEFINITIONS

Figure 9

Priority	Channel	Description
HIGHEST	1111	General Purpose Interrupt 7(I7)
	1110	General Purpose Interrupt 6(I6)
	1101	Timer A
	1100	Receive Buffer Full
	1011	Receive Error
	1010	Transmit Buffer Empty
	1001	Transmit Error
	1000	Timer B
	0111	General Purpose Interrupt 5(I5)
	0110	General Purpose Interrupt 4(I4)
	0101	Timer C
	0100	Timer D
	0011	General Purpose Interrupt 3(I3)
	0010	General Purpose Interrupt 2(I2)
	0001	General Purpose Interrupt 1(I1)
LOWEST	0000	General Purpose Interrupt 0(I0)

Interrupts may be either polled or vectored. Each channel may be individually enabled or disabled by writing a one or a zero in the appropriate bit of Interrupt Enable Registers (IERA,IERB--see Figure 8 for all registers in this section). When disabled, an interrupt channel is completely inactive. Any internal or external action which would normally produce an interrupt on that channel is ignored and any pending interrupt on that channel will be cleared by disabling that channel. Disabling an interrupt channel has no effect on the corresponding bit in Interrupt In-Service Registers (ISRA,ISRB); thus, if the In-service Registers are used and an interrupt is in service on that channel when the channel is disabled, it will remain in service until cleared in the normal manner. IERA and IERB are also readable.

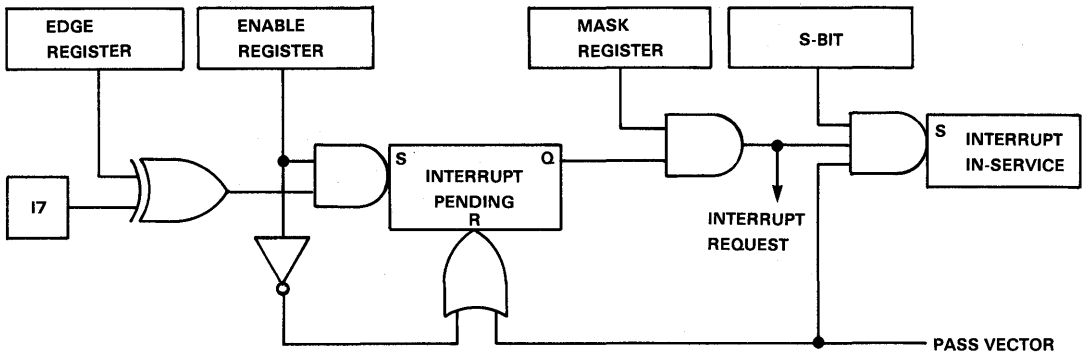
When an interrupt is received on an enabled channel, its corresponding bit in the pending register will be set. When that channel is acknowledged it will pass its vector, and the corresponding bit in the Interrupt Pending Register (IPRA or IPRB) will be cleared. IPRA and IPRB are readable; thus by polling IPRA and IPRB, it can be determined whether a channel has a pending interrupt. IPRA and IPRB are also writeable and a pending interrupt can be cleared without going through the acknowledge sequence by writing a zero to the appropriate bit. This allows any one bit to be cleared, without altering any other bits, simply by writing all ones except for the bit position to be cleared to IPRA or IPRB. Thus a fully polled interrupt scheme is possible. Note: writing a one to IPRA, IPRB has no effect on the interrupt pending register.

The interrupt mask registers (IMRA and IMRB) may be used to block a channel from making an interrupt request. Writing a zero into the corresponding bit of the mask register will still allow the channel to receive an interrupt and latch it into its pending bit (if that channel is enabled), but will prevent that channel from making an interrupt request. If that channel is causing an interrupt request at the time the corresponding bit in the mask register is cleared, the request will cease. If no other channel is making a request, $\overline{INTR}$ will go inactive. If the mask bit is re-enabled, any pending interrupt is now free to resume its request unless blocked by a higher priority request for service. IMRA and IMRB are also readable. A conceptual circuit of an interrupt channel is shown in Figure 10.

There are two end-of-interrupt modes: the automatic end-of-interrupt mode and the software end-of-interrupt mode. The mode is selected by writing a one or a zero to the S bit of the Vector Register(VR). If the S bit of the VR is a one, all channels operate in the software end-of-interrupt mode. If the S bit is a zero, all channels operate in the automatic end-of-interrupt mode, and a reset is held on all in-service bits. In the automatic end-of-interrupt mode, the pending bit is cleared when that channel passes its vector. At that point, no further history of that interrupt remains in the MK68901 MFP. In the software end-of-interrupt mode, the in-service

A CONCEPTUAL CIRCUIT OF AN INTERRUPT CHANNEL

Figure 10



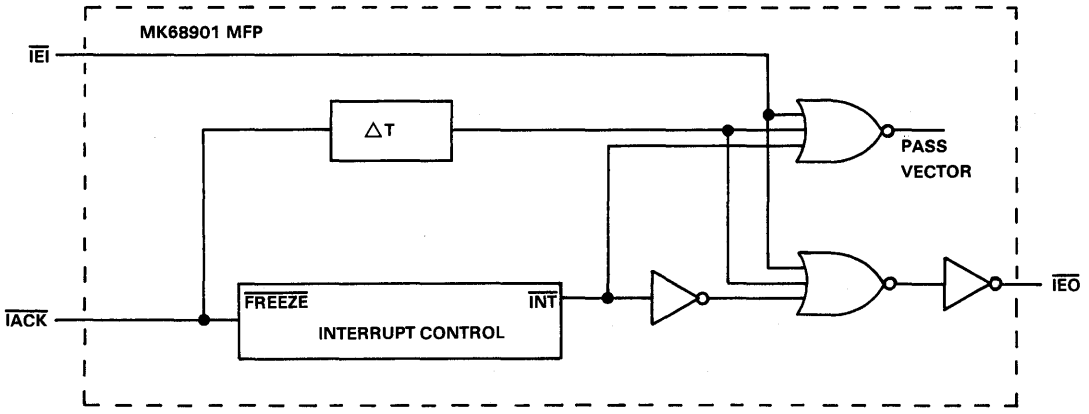
bit is set and the pending bit is cleared when the channel passes its vector. With the in-service bit set, no lower priority channel is allowed to request an interrupt or to pass its vector during an acknowledge sequence; however, a lower priority channel may still receive an interrupt and latch it into the pending bit. A higher priority channel may still request an interrupt and be acknowledged. The in-service bit of a particular channel may be cleared by writing a zero to the corresponding bit in ISRA or ISRB. Typically, this will be done at the conclusion of the interrupt routine just before the return. Thus no lower priority channel will be allowed to request service until the higher priority channel is complete, while channels of still higher priority will be allowed to request service. While the in-service bit is set, a second interrupt on that channel may be received and latched into the pending bit, though no service request will be made in response to the second interrupt until the in-service bit is cleared. ISRA and ISRB may be read at any time. Only a zero may be written into any bit of ISRA and ISRB; thus the in-service bits may be cleared in software but cannot be set in software. This allows any one bit to be cleared, without altering any other bits, simply by writing all ones except for the bit position to be cleared to ISRA or ISRB, as with IPRA and IPRB.

Each interrupt channel responds with a discrete 8-bit vector when acknowledged. The upper four bits of the vector are set by writing the upper four bits of the VR. The four low order bits (Bit 3-Bit 0) are generated by the interrupting channel.

To acknowledge an interrupt, $\overline{IACK}$ goes low, the $\overline{IEI}$ input must go low (or be tied low) and the MK68901 MFP must have an acknowledgeable interrupt pending. The Daisy Chaining capability (Figure 11) requires that all parts in a chain have a common $\overline{IACK}$. When the common $\overline{IACK}$ goes

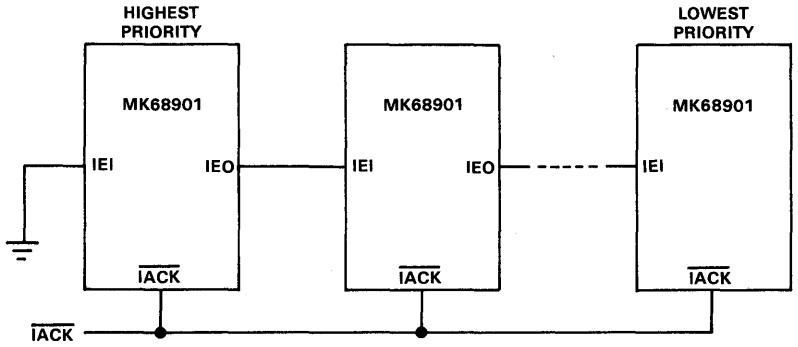
A CONCEPTUAL CIRCUIT OF THE MK68901 MFP DAISY CHAINING

Figure 11a



DAISY CHAINING

Figure 11b



low, all parts freeze and prioritize interrupts in parallel. Then priority is passed down the chain, via $\overline{IEI}$ and $\overline{IEO}$, until a part which has a pending interrupt is reached. The part with the pending interrupt, passes a vector, does not propagate $\overline{IEO}$, and generates $\overline{DTACK}$.

Figure 9 describes the 16 prioritized interrupt channels. As shown, General Purpose Interrupt 7 has the highest priority, while General Purpose Interrupt 0 is assigned the lowest priority. Each of these channels may be reprioritized, in effect, by selectively masking interrupts under software control. The binary numbers under "channel" correspond to the modified bits IV3, IV2, IV1, and IV0, respectively, of the Interrupt Vector for each channel (see Figure 6).

Each channel has an enable bit contained in IERA or IERB, a pending latch contained in IPRA or IPRB, a mask bit contained in IMRA or IMRB, and an in-service latch contained in ISRA or ISRB. Additionally, the eight General Purpose Interrupts each have an edge bit contained in the Active Edge Register (AER), a bit to define the line as input or output contained in the Data Direction Register (DDR) and an I/O bit in the General Purpose Interrupt-I/O Port (GPIP).

TIMERS

There are four timers on the MK68901 MFP. Two of the timers (Timer A and Timer B) are full function timers which can perform the basic delay function and can also perform event counting, pulse width measurement, and waveform generation. The other two timers (Timer C and Timer D) are delay timers only. One or both of these timers can be used to supply the baud rate clocks for the USART. All timers are prescaler/counter timers with a common independent clock input (XTAL1, XTAL2). In addition, all timers have a time-out output function that toggles each time the timer times out.

The four timers are programmed via three Timer Control Registers and four Timer Data Registers. Timers A and B are controlled by the control registers TACR and TBCR, respectively (see Figure 12), and by the data registers TADR and TBDR (Figure 13). Timers C and D are controlled by the control register TCDCR (see Figure 14) and two data registers TCDR and TDDR. Bits in the control registers allow the selection of operational mode, prescale, and control, while the data registers are used to read the timer or write into the time constant register. Timer A and B input pins, TAI and TBI, are used for the event and pulse width modes for timers A and B.

With the timer stopped, no counting can occur. The timer contents will remain unaltered while the timer is stopped (unless reloaded by writing the Timer Data Register), but any residual count in the prescaler will be lost.

In the delay mode, the prescaler is always active. A count pulse will be applied to the main timer unit each time the prescribed number of timer clock cycles has elapsed. Thus, if the prescaler is programmed to divide by ten, a count pulse will be applied to the main counter every ten cycles of the timer clock.

Each time a count pulse is applied to the main counter, it will decrement its contents. The main counter is initially loaded by writing to the Timer Data Register. Each count pulse will cause the current count to decrement. When the timer has decremented down to "01", the next count pulse will not cause it to decrement to "00". Instead, the next count pulse will cause the timer to be reloaded from the Timer Data Register. Additionally, a "Time out" pulse will be produced. This Time Out pulse is coupled to the timer interrupt channel, and, if that channel is enabled, an interrupt will be produced. The Time Out pulse is also coupled to the timer output pin and will cause the pin to change states. The

TIMER A AND B CONTROL REGISTERS
Figure 12

Port C (TACR)	*	*	*	TIMER A RESET	AC_3	AC_2	AC_1	AC_0
Port D (TBCR)	*	*	*	TIMER B RESET	BC_3	BC_2	BC_1	BC_0

C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷ 4 Prescale
0	0	1	0	Delay Mode, ÷ 10 Prescale
0	0	1	1	Delay Mode, ÷ 16 Prescale
0	1	0	0	Delay Mode, ÷ 50 Prescale
0	1	0	1	Delay Mode, ÷ 64 Prescale
0	1	1	0	Delay Mode, ÷ 100 Prescale
0	1	1	1	Delay Mode, ÷ 200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷ 4 Prescale
1	0	1	0	Pulse Width Mode, ÷ 10 Prescale
1	0	1	1	Pulse Width Mode, ÷ 16 Prescale
1	1	0	0	Pulse Width Mode, ÷ 50 Prescale
1	1	0	1	Pulse Width Mode, ÷ 64 Prescale
1	1	1	0	Pulse Width Mode, ÷ 100 Prescale
1	1	1	1	Pulse Width Mode, ÷ 200 Prescale

* Unused bits: read as zeros

output will remain in this new state until the next Time Out pulse occurs. Thus the output will complete one full cycle for each two Time Out pulses.

If, for example, the prescaler were programmed to divide by ten, and the Timer Data Register were loaded with 100 (decimal), the main counter would decrement once for every ten cycles of the timer clock. A Time Out pulse will occur (hence an interrupt if that channel is enabled) every 1000 cycles of the timer clock, and the timer output will complete one full cycle every 2000 cycles of the timer clock.

The main counter is an 8-bit binary down counter. It may be read at any time by reading the Timer Data Register. The information read is the information last clocked into the timer read register when the $\overline{DS}$ pin had last gone high prior to the current read cycle. When written, data is loaded into the Timer Data Register, and the main counter, if the timer is stopped. If the Timer Data Register is written while the timer is running, the new word is not loaded into the timer until it counts through H"01". However, if the timer is written while it is counting through H"01", an indeterminate value will be written into the time constant register. This may be circumvented by ensuring that the data register is not written when the count is H"01".

If the main counter is loaded with "01", a Time Out Pulse will occur every time the prescaler presents a count pulse to the main counter. If loaded with "00", a Time Out pulse will occur after every 256 count pulses.

Changing the prescale value with the timer running can cause the first Time Out pulse to occur at an indeterminate time, (no less than one nor more than 200 timer clock cycles times the number in the time constant register), but subsequent Time Out pulses will then occur at the correct interval.

In addition to the delay mode described above, Timers A and B can also function in the Pulse Width Measurement mode or in the Event Count mode. In either of these two modes, an auxiliary control signal is required. The auxiliary control input for Timer A is TAI, and for Timer B, TBI is used. The interrupt channels associated with I4 and I3 are used for TAI and TBI, respectively, in Pulse Width mode. See Figure 15.

The pulse width measurement mode functions much like the delay mode. However, in this mode, the auxiliary control signal on TAI or TBI acts as an enable to the timer. When the control signal on TAI or TBI is inactive, the timer will be stopped. When it is active, the prescaler and main counter are allowed to run. Thus the width of the active pulse on TAI or TBI is determined by the number of timer counts which occur while the pulse allows the timer to run. The active state of the signal on TAI or TBI is dependent upon the associated Interrupt Channel's edge bit (GPIP 4 for TAI and GPIP 3 for TBI; see Active Edge Register in Figure 5.) If the edge bit associated with the TAI or TBI input is a one, it will be active high; thus the timer will be allowed to run when the input is at a high level. If the edge bit is a zero, the TAI or TBI input will be active low. As previously stated, the

VI

TIMER DATA REGISTERS (A, B, C, AND D)

Figure 13

	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Port F (TADR)								
Port 10 (TBDR)								
Port 11 (TCDR)								
Port 12 (TDDR)								

TIMER C AND D CONTROL REGISTER

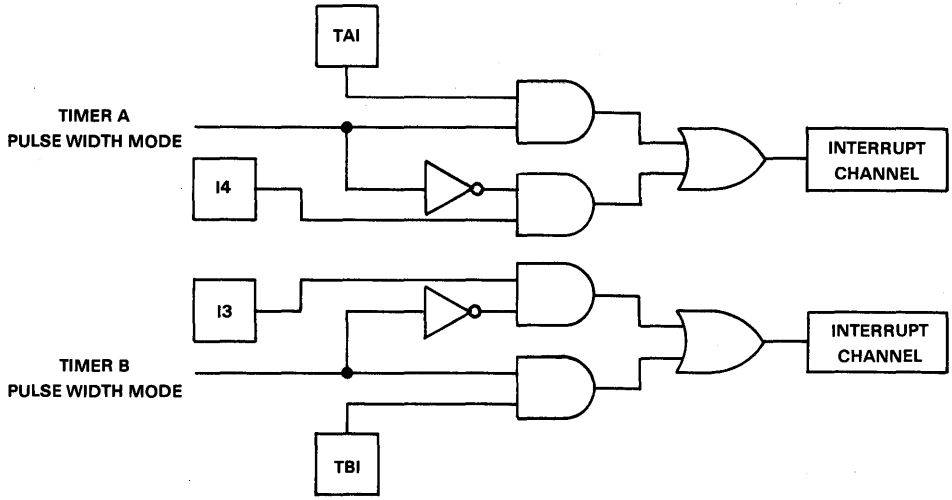
Figure 14

Port E (TCDCR)	*	CC_2	CC_1	CC_0	*	DC_2	DC_1	DC_0

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, ÷ 4 Prescale
0	1	0	Delay Mode, ÷ 10 Prescale
0	1	1	Delay Mode, ÷ 16 Prescale
1	0	0	Delay Mode, ÷ 50 Prescale
1	0	1	Delay Mode, ÷ 64 Prescale
1	1	0	Delay Mode, ÷ 100 Prescale
1	1	1	Delay Mode, ÷ 200 Prescale

* Unused bits: read as zeros

A CONCEPTUAL CIRCUIT OF THE MFP TIMERS IN THE PULSE WIDTH MEASUREMENT MODE
Figure 15



interrupt channel (I3 or I4) associated with the input still functions when the timer is used in the pulse width measurement mode. However, if the timer is programmed for the pulse width measurement mode, the interrupt caused by transitions on the associated TAI or TBI input will occur on the opposite transition.

For example, if the edge bit associated with the TAI input (AER-GPIP 4) is a one, an interrupt would normally be generated on the 0-1 transition of the I4 input signal. If the timer associated with this input (Timer A) is placed in the pulse width measurement mode, the interrupt will occur on the 1-0 transition of the TAI signal instead. Because the edge bit (AER-GPIP 4) is a one, Timer A will be allowed to count while the input is high. When the TAI input makes the high to low transition, Timer A will stop, and it is at this point that the interrupt will occur (assuming that the channel is enabled). This allows the interrupt to signal the CPU that the pulse being measured has terminated; thus Timer A may now be read to determine the pulse width. (Again note that I3 and I4 may still be used for I/O when the timer is in the pulse width measurement mode.) If Timer A is re-programmed for another mode, interrupts will again occur on the transition, as normally defined by the edge bit. Note that, like changing the edge bit, placing the timer into or taking it out of the pulse width mode can produce a transition on the signal to the interrupt channel and may cause an interrupt. If measuring consecutive pulses, it is obvious that one must read the contents of the timer and then reinitialize the main counter by writing to the timer data register. If the timer data register is written while the pulse is going to the active state, the write operation may result in an indeterminate value being written into the main counter. If the timer is written after the pulse goes active, the timer counts from the previous contents, and when it counts through H"01", the correct value is written into the timer. The pulse width then includes counts from before the timer was reloaded.

In the event count mode, the prescaler is disabled. Each time the control input on TAI or TBI makes an active transition as defined by the associated Interrupt Channel's edge bit, a count pulse will be generated, and the main counter will decrement. In all other respects, the timer functions as previously described. Altering the edge bit while the timer is in the event count mode can produce a count pulse. The interrupt channel associated with the input (I3 for TBI or I4 for TAI) is allowed to function normally. To count transitions reliably, the input must remain in each state (1/0) for a length of time equal to four periods of the timer clock; thus signals of a frequency up to one fourth of the timer clock can be counted.

The manner in which the timer output pins toggle states has previously been described. All timer outputs will be forced low by a device RESET. The output associated with Timers A and B will toggle on each Time Out pulse regardless of the mode the timers are programmed to. In addition, the outputs from Timers A and B can be forced low at any time by writing a "1" to the reset location in TACR and TBCR, respectively. The output will be forced to the low state during the WRITE operation, and at the conclusion of the operation, the output will again be free to toggle each time a Time Out pulse occurs. This feature will allow waveform generation.

During reset, the Timer Data Registers and the main counters are not reset. Also, if using the reset option on Timers A or B, one must make sure to keep the other bits in the correct state so as not to affect the operation of Timers A and B.

USART

Serial Communication is provided by a full-duplex double-buffered USART, which is capable of either asynchronous or synchronous operation. Variable word length and start/stop bit configurations are available under software control for asynchronous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for transmission. Moreover, the MK68901 allows stripping of all Sync Words received in synchronous operation. The handshake control lines RR (Receiver Ready) and TR (Transmitter Ready) allow DMA operation. Separate receive and transmit clocks are available, and separate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

The USART is provided with three Control/Status Registers and a Data Register. The USART Data Register form is illustrated in Figure 16. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 17. Status of both the Receiver and Transmitter sections is accessed by means of the two Status Registers, as shown in Figures 18 and 19. Data written to the Data Register is passed to the transmitter, while reading the Data Register will access data received by the USART.

USART DATA REGISTER

Figure 16

Port 17 (UDR)	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

USART CONTROL REGISTER (UCR)

Figure 17

	UCR_7							UCR_0
Port 14 (UCR)	1 = ÷ 16 0 = ÷ 1	WL_1	WL_0	ST_1	ST_0	PARITY ENABLED ON 1	1 = EVEN 0 = ODD	*

* Unused bits; read as zero

÷16/÷1 : When this bit is zero, data will be clocked into and out of the receiver and transmitter at the frequency of their respective clocks. When this bit is loaded with a one, data will be clocked into and out of the receiver and transmitter at one sixteenth the frequency of their respective clocks. Additionally, when placed in the divide by sixteen mode, the receiver data transition resynchronization logic will be enabled.

WL0-WL1 : Word Length Control. These two bits set the length of the data word (exclusive of start bits, stop bits,and parity bits) as follows:

WL1	WL0	Word Length
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

ST0-ST1 : Start/Stop bit control (format control). These two bits set the format as follows:

ST1	ST0	Start Bits	Stop Bits	Format
0	0	0	0	SYNC
0	1	1	1	ASYNC
†1	0	1	1½	ASYNC
1	1	1	2	ASYNC

† NOTE ÷16 only

PARITY : Parity Enabled. When set ("1"), parity will be checked by the receiver, parity will be calculated, and a parity bit will be inserted by the transmitter. When cleared ("0"), no parity check will be made and no parity bit will be inserted for transmission.

For a word length of 8 the MFP calculates the parity and appends it when transmitting a sync character. For shorter lengths, the parity must be stored in the Sync Character Register (SCR) along with the sync character.

E/O : Even-Odd. When set ("1"), even parity will be used if parity is enabled. When cleared ("0"), odd parity will be used if parity is enabled.

Note that the synchronous or asynchronous format may be selected independently of a ÷ 1 or ÷ 16 clock. Thus it is possible to clock data synchronously into the device but still use start and stop bits. In this mode, all normal asynchronous format features still apply. Data will be shifted in after a start bit is encountered, and a stop bit will be checked to determine proper framing. If a transmit underrun condition occurs, the output will be placed in a marking state, etc. It is conversely possible to clock data in asynchronously using a synchronous format. There is data transition detection logic built into the receive clock circuitry which will re-synchronize the internal shift clock on each data transition so that, with sufficiently frequent data transitions, start bits are not required. In this mode, all other common synchronous features function normally. This re-synchronization logic is only active in ÷ 16 clock mode.

RECEIVER

The receiver section of the USART is configured by the UCR as previously described. The status of the receiver can be determined by reading and writing to the Receiver Status Register (RSR). The RSR is configured as follows:

RECEIVER STATUS REGISTER (RSR)

Figure 18

	RSR_7							RSR_0
Port 15 (RSR)	BUFFER FULL	OVERRUN ERROR	PARITY ERROR	FRAME ERROR	FOUND/$\overline{\text{SEARCH}}$ OR BREAK DETECT	MATCH/CHARACTER IN PROGRESS	SYNC STRIP ENABLE	RECEIVER ENABLE

BF : Buffer Full. This bit is set when the incoming word is transferred to the receive buffer. The bit is cleared when the receive buffer is read by reading the UDR. This bit of the RSR is read only.

OE : Overrun Error.This flag is set if the incoming word is completely received and due to be transferred to the receive buffer, but the last word in the receive buffer has not yet been read. When this condition occurs, the word in the receive buffer is not overwritten by the new word. Note that the status flags always reflect the status of the data word currently in the receive buffer. As such, the OE flag is not actually set until the good word currently in the buffer has been read. The interrupt associated with this error will also not be generated until the old word in the receive buffer has been read.

OE flag is cleared by reading the receiver status register, and new data words cannot be shifted to the receive buffer until this is done.

PE : Parity Error. This flag is set if the word received has a parity error. The flag is set when the received word is transferred from the shift register to the receive buffer if the error condition exists. The flag is cleared when the next word which does not have a parity error is transferred to the receive buffer.

FE : Frame Error. This flag only applies to the asynchronous format. A frame error is defined as a non-zero data word which is not followed by a stop bit. Like the PE flag, the FE flag is set or cleared when a word is transferred to the receive buffer.

F/$\overline{\text{S}}$: Found/$\overline{\text{Search}}$. This combination control bit and flag bit is only used with the synchronous format. It can be set or cleared by writing to this bit of the RSR. When this bit is cleared, the receiver is placed in the search mode. In this mode, a bit by bit comparison of the incoming data to the character in the Sync Character Register (SCR) is made. The word length counter is disabled. When a match is found, this bit will be set automatically, and the word length counter will start as sync has now been achieved. An interrupt will be generated on the receive error channel when the match occurs. The word just shifted in will, of necessity, be equal to the sync character, and it will not be transferred to the receive buffer.

B : Break. This flag is used only when the asynchronous format is selected. This flag will be set when an all zero data word, followed by no stop bit, is received. The flag will stay set until both a non-zero bit is received and the RSR has been read at least once since the flag was set. Break indication will not occur if the receive buffer is full.

M/CIP : Match/Character in Progress. If the synchronous format is selected, this flag is the Match flag. It will be set each time the word transferred to the receive buffer matches the sync character. It will be reset each time the word transferred to the receive buffer does not match the sync

character. If the asynchronous format is selected, this flag represents Character in Progress. It will be set upon a start bit detect and cleared at the end of the word.

SS : Sync Strip Enable. If this bit is set to a one, data words that match the sync character will not be loaded into the receive buffer, and no buffer full signal will be generated.

RE: : Receiver Enable. This control bit is used to enable or disable the receiver. If a zero is written to this bit of the RSR, the receiver will turn off immediately. All flags including the F/$\overline{S}$ bit will be cleared. If a one is written to this bit, normal receiver operation is enabled. The receive clock has to be running before the receiver is enabled.

There are two interrupt channels associated with the receiver. One channel is used for the normal Buffer Full condition, while the other channel is used whenever an error condition occurs. Only one interrupt is generated per word received, but dedicating two channels allows separate vectors: one for the normal condition, and one for an error condition. If the error channel is disabled, an interrupt will be generated via the Buffer Full Channel, whether the word received is normal or in error. Those conditions which produce an interrupt via the error channel are: Overrun, Parity Error, Frame Error, Sync Found, and Break. If a received word has an error associated with it, and the error interrupt channel is enabled, an interrupt will occur on the error channel only.

Each time a word is transferred into the receive buffer, a corresponding set of flags is latched into the RSR. No flags (except CIP) are allowed to change until the data word has been read from the receive buffer. Reading the receive buffer allows a new data word to be transferred to the receive buffer when it is received. Thus one should first read the RSR then read the receive buffer (UDR) to ensure that the flags just read match the data word just read. If done in the reverse order, it is possible that subsequent to reading the data word from the receive buffer, but prior to reading the RSR, a new word may be received and transferred to the receive buffer and, with it, its associated flags latched into the RSR. Thus, when the RSR is read, those flags may actually correspond to a different data word. It is good practice, also, to read the RSR prior to a data read as, when an overrun error occurs, the receiver will not assemble new characters until the RSR has been read.

As previously stated, when overrun occurs, the OE flag will not be set and the associated interrupt will not be generated until the receive buffer has been read. If a break occurs, and the receive buffer has not yet been read, only the B flag will be set (OE will not be set). Again, this flag will not be set until the last valid word has been read from the receive buffer. If the break condition ends and another whole data word is received before the receive buffer is read, both the B and OE flags will be set once the receive buffer is read.

If a break occurs while the OE flag is set, the B flag will also be set.

A break generates an interrupt when the condition occurs and again when the condition ends. If the break condition ends before it is acknowledged by reading the RSR, the receiver error interrupt indicating end of break will be generated once the RSR is read.

Anytime the asynchronous format is selected, start bit detection is enabled. New data is not shifted into the shift register until a zero bit is detected. If a $\div 16$ clock is selected, along with the the asynchronous format, false start bit detection is also enabled. Any transition has to be stable for 3 positive going edges of the receive clock to be called a valid transition. For a start bit to be good, a valid 0-1 transition must not occur for 8 positive clock transitions after the initial valid 1-0 transition.

After a good start bit has been detected, valid transitions in the data are checked for continously. When a valid transition is detected, the counter is forced to state zero, and no more transition checking is started until state four. At state eight, the "previous state" of the transition checking logic is clocked into the receiver.

As a result of this resynchronization logic, it is possible to run with asynchronous clocks without start and stop bits if there are sufficient valid transitions in the data stream. This logic also makes the unit more tolerant of clock skew for normal asynchronous communications than a device which employs only start bit synchronization.

TRANSMITTER STATUS REGISTER (TSR)

Figure 19

	TSR_7							TSR_0
Port 16 (TSR)	BUFFER EMPTY	UNDERRUN ERROR	AUTO TURNAROUND	END OF TRANSMISSION	BREAK	HIGH	LOW	TRANSMITTER ENABLE

TRANSMITTER

The transmitter section of the USART is configured as to format, word length, etc. by the UCR, as previously described. The status of the transmitter can be determined by reading or writing the Transmitter Status Register (TSR). The TSR is configured as follows:

BE : Buffer Empty. This status bit is set when the word in the transmit buffer is transferred to the output shift register and thus the transmit buffer may be reloaded with the next data word. The flag is cleared when the transmit buffer is reloaded. The transmit buffer is loaded by writing to the UDR.

UE : This bit is set when the last word has been shifted out of the transmit shift register before a new word has been loaded into the transmit buffer. It is not necessary to clear this bit before loading the UDR.

This bit may be cleared by either reading the TSR or by disabling the transmitter. After the setting of the UE bit, one full transmitter clock cycle is required before this bit can be cleared by a read. The timing in some systems may allow a read of the TSR before the required clock cycle has been completed. This would result in the UE bit not being cleared until the following read. To avoid this problem, a dummy read of the TSR should be performed at the end of the UE service routine.

Only one underrun error may be generated between loads of the UDR regardless of the number of transmitter clock cycles between UDR loads.

AT : This bit causes the receiver to be enabled at the end of the transmission of the last word in the transmitter if the transmitter has been disabled. The AT bit is cleared at the end of the transmission.

END : End of transmission. When the transmitter is turned off with a character still in the output shift register, transmission will continue until that character is shifted out. Once it has cleared the output register, the END bit will be set. If no character is being transmitted when the transmitter is disabled, the transmitter will stop at the next rising edge of the internal shift clock, and END will immediately be set. The END bit is cleared by re-enabling the transmitter.

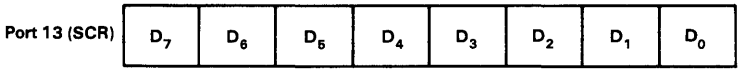
B : Break. This control bit will cause a break to be transmitted. When a "1" is written to the B bit of the TSR, a break will be transmitted upon completion of the character (if any) currently being transmitted. A break will continue to be transmitted until the B bit is cleared by writing a "0" to this bit of the TSR. At that time, normal transmission will resume. The B bit has no function in the synchronous format. Setting the "B" bit to a one keeps the "BE" bit from being set to a one. So, if there were a word in the buffer at the start of break, it would remain there until the end of break, at which time it would be transmitted (if the transmitter is still enabled). If the buffer were not full at the start of break, it could be written at any time during the break. If the buffer is empty at the end of break, the underrun flag will be set (unless the transmitter is disabled).

The BREAK bit cannot be set until the transmitter has been enabled and the transmitter has had sufficient time (one clock cycle) to perform the internal reset and initialization functions.

H,L : High and Low. These two control bits are used to configure the transmitter output, when the transmitter is disabled, as follows:

H	L	Output State
0	0	Hi-Z
0	1	Low ("0")
1	0	High
1	1	Loop -Connects transmitter output to receiver input, and TC to Receiver Clock (RC and SI are not used; they are bypassed internally). In loop back mode, transmitter output goes high when disabled.

SYNC CHARACTER REGISTER
Figure 20



Altering these two bits after Transmitter Enable (XE) is set will alter the output state until END is false. These bits should be set prior to enabling the transmitter. The state of these bits determine the state of the first transmitted character after the transmitter is enabled. If the high impedance mode was selected prior to the transmitter being enabled, the first bit transmitted is indeterminate.

XE : Transmitter Enable. This control bit is used to enable or disable the transmitter. When set, the transmitter is enabled. When cleared, the transmitter will be disabled. If disabled, any word currently in the output register will continue to be transmitted until finished. If a break is being transmitted when XE is cleared, the transmitter will turn off at the end of the break character boundary, and no end of break stop bit is transmitted. The transmit clock must be running before the transmitter is enabled. A "one" bit always precedes the first word out of the transmitter after the transmitter is enabled. There is a delay between the time the transmitter enable bit is written and when the transmitter reset goes low; therefore, the H & L bits should be written with the desired state prior to enabling the transmitter.

Like the receiver section, there are two separate interrupt channels associated with the transmitter. The buffer Empty condition causes an interrupt via one channel, while the Underrun and END conditions will cause an interrupt via the second channel. When underrun occurs in the synchronous format, the character in the SCR will be transmitted until a new word is loaded into the transmit buffer. In the asynchronous format, a "Mark" will be continuously transmitted when underrun occurs.

The transmit buffer can be loaded prior to enabling the transmitter. When the transmitter is disabled, any character currently in the process of being transmitted will continue to conclusion, but any character in the transmit buffer will not be transmitted and will remain in the buffer. Thus no buffer empty interrupt will occur nor will the BE flag be set. If the buffer were already empty, the BE flag would be set and would remain set. When the transmitter is disabled with a character in the output register but with no character in the transmit buffer, an Underrun Error will not occur when the character in progress concludes.

Often it is necessary to send a break for some particular period. To aid in timing a break transmission, a transmit error interrupt will be generated at every normal character boundary time during a break transmission. The status register information is unaffected by this error condition interrupt. It should be noted that an underrun error, if present, must be cleared from the TSR, and the interrrupt pending register must be cleared of pending transmitter errors at the beginning of the break transmission or no interrupts will be generated at the character boundary time.

If the synchronous format is selected, the sync character should be loaded into the Sync Character Register (SCR) as shown in Figure 20. This character is compared to the received serial data during a Search, and will be continuously transmitted during an underrun condition.

All flags in the RSR or TSR will continue to function as described whether their associated interrupt channel is disabled or enabled. All interrupt channels are edge triggered and, in many cases, it is the actual output of a flag bit or flag bits which is coupled to the interrupt channel. Thus, if a normal interrupt producing condition occurs while the interrupt channel is disabled, no interrupt would be produced even if the channel was subsequently enabled, because a transition did not occur while the interrupt channel was enabled. That particular flag bit would have to occur a second time before another "edge" was produced, causing an interrupt to be generated.

Error conditions in the USART are determined by monitoring the Receive Status Register and the Transmitter Status Register. These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save error conditions during data transfer, the MK68901 MFP interrupt controller may be used by enabling error interrupts for the desired channel (Receive error or Transmit error) and by masking these bits off. Once the transfer is complete, the Interrupt Pending Register can be polled,to determine the presence of a pending error interrupt, and therefore an error.

Unused bits in the sync character register are zeroed out; therefore, word length should be set up prior to writing the sync word in some cases. Sync word length is the word length plus one when parity is enabled. The user has to determine the parity of the sync word when the word length

is not 8 bits. The MK68901 MFP does not add a parity bit to the sync word if the word length is less than 8 bits. The extra bit in the sync word is transmitted as the parity bit. With a word length of eight, and parity selected, the parity bit for the sync word is computed and added on by the MK68901 MFP.

$\overline{RR}$ RECEIVER READY

$\overline{RR}$ is asserted when the Buffer Full bit is set in the RSR unless a parity error or frame error is detected by the receiver.

$\overline{TR}$ TRANSMITTER READY

$\overline{TR}$ is asserted when the Buffer Empty bit is set in the TSR unless a break is currently being transmitted.

REGISTER ACCESSES

All register accesses are dependent on CLK as shown in the timing diagrams. To read a register, $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be high. The internal read control signal is essentially the combination of $\overline{CS}$, $\overline{DS}$, and RD/$\overline{WR}$. Thus, the read operation will begin when $\overline{CS}$ and $\overline{DS}$ go active and will end when either $\overline{CS}$ or $\overline{DS}$ goes inactive. The address bus must be stable prior to the start of the operation and must remain stable until the end of the operation. Unless a read operation or interrupt acknowledge cycle is in progress the data bus (D_0-D_7) will remain in the tri-state condition.

To write a register, $\overline{CS}$ and $\overline{DS}$ must be asserted and R/$\overline{W}$ must be low. The address must be stable prior to the start of the operation and must remain stable until the end of the operation. After the MK68901 asserts $\overline{DTACK}$, the CPU negates $\overline{DS}$. At this time, the MFP latches the data bus and writes the contents into the appropriate register. Also, when $\overline{DS}$ is negated, the MFP rescinds $\overline{DTACK}$.

For an interrupt acknowledge, the operation starts when $\overline{IACK}$ goes low, and ends when $\overline{IACK}$ goes high. The data bus is tri-stated when either $\overline{IACK}$ or $\overline{DS}$ goes high.

MK68901 ELECTRICAL SPECIFICATIONS - PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -25°C to +100°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3 V to +7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

D. C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5 V ± 5% unless otherwise specified.

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input High Voltage	2.0	V_{CC} + .3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OH}	Output High Voltage (except $\overline{DTACK}$)	2.4		V	I_{OH} = -120 μA
V_{OL}	Output Low Voltage (except $\overline{DTACK}$)		0.5	V	I_{OL} = 2.0 mA
I_{LL}	Power Supply Current		180	mA	Outputs Open
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.5 V
I_{OH}	$\overline{DTACK}$ output source current		-400	μA	V_{OUT} = 2.4
I_{OL}	$\overline{DTACK}$ output sink current		5.3	mA	V_{OUT} = 0.5

All voltages are referenced to ground

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground.

SYM	PARAMETER	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance	10	pf	Unmeasured pins returned to ground
C_{OUT}	Tri-state Output Capacitance	10	pf	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, GND = 0 Vdc, T_A = 0°C to 70°C)

NUM	CHARACTERISTIC	MK68901 MIN	MK68901 MAX	UNIT	FIG	NOTE
1	$\overline{CS}$, $\overline{DS}$ Width High	50		ns	21,22	
2	R/$\overline{W}$, A1-A5 Valid to falling $\overline{CS}$ (Setup)	0		ns	21,22	
3	Data Valid Prior to Rising $\overline{DS}$ (Setup)	280		ns	21	
4	$\overline{CS}$, $\overline{IACK}$ Valid to Falling Clock (Setup)	50		ns	21-24	3
5	CLK Low to $\overline{DTACK}$ Low		220	ns	21,22	
6	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ High to $\overline{DTACK}$ high		60	ns	21-24	
7	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ High to $\overline{DTACK}$ Tri-state		100	ns	21-24	
8	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ High to Data Invalid (Hold Time)	0		ns	21-24	
9	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ High to Data Tri-state		50	ns	21-24	
10	$\overline{CS}$ or $\overline{DS}$ High to R/$\overline{W}$, A1-A5 Invalid (Hold Time)	0		ns	21,22	
11	Data Valid from $\overline{CS}$ Low		310	ns	21	
12	Read Data Valid to $\overline{DTACK}$ Low (Setup Time)	50		ns	21	
13	$\overline{DTACK}$ Low to $\overline{DS}$, $\overline{CS}$ or $\overline{IACK}$ High (Hold Time)	0		ns	21-24	
14	$\overline{IEI}$ low to falling $\overline{CLK}$ (Setup)	50		ns	23	2
15	$\overline{IEO}$ Valid from Clock Low (Delay)		180	ns	23	1
16	Data Valid From Clock Low (Delay)		300	ns	23	
17	$\overline{IEO}$ Invalid from $\overline{IACK}$ High (Delay)		150	ns	23,24	
18	$\overline{DTACK}$ Low from Clock High (Delay)		180	ns	23,24	2
19	$\overline{IEO}$ Valid from $\overline{IEI}$ Low (Delay)		100	ns	24	1
20	Data Valid from $\overline{IEI}$ Low (Delay)		220	ns	24	
21	Clock Cycle Time	250	1000	ns	21-24	
22	Clock Width Low	110		ns	21-24	
23	Clock Width High	110		ns	21-24	
24	$\overline{CS}$, $\overline{IACK}$ Inactive to Rising Clock (Setup)	100		ns	21-24	4
25	I/O Minimum Active Pulse Width	100		ns		
26	$\overline{IACK}$ width High	150		ns	23-24	

AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0 Vdc ± 5%, GND = 0 Vdc, T_A = 0°C to 70°C)

NUM	CHARACTERISTIC	MK68901 MIN	MK68901 MAX	UNIT	FIG	NOTE
27	I/O Data valid from Rising $\overline{CS}$ or $\overline{DS}$		450	ns		
28	Receiver Ready Delay from Rising RC		600	ns		
29	Transmitter Ready Delay from Rising TC		600	ns		
30	Timer Output Low from Rising Edge of $\overline{CS}$ or $\overline{DS}$ (A & B) (Reset T_{OUT})		450	ns		
31	T_{OUT} Valid from Internal Timeout		2 t_{CLK} +300	ns		
32	Timer Clock Low Time	110		ns		
33	Timer Clock High Time	110		ns		
34	Timer Clock Cycle Time	250	1000	ns		
35	$\overline{RESET}$ Low Time	2		μs		
36	Delay to Falling $\overline{INTR}$ from External Interrupt Active Transition		380	ns		
37	Transmitter Internal Interrupt Delay from Rising of Falling Edge of TC	550		ns		
38	Receiver Buffer Full Interrupt Transition Delay from Rising Edge of RC	800		ns		
39	Receiver Error Interrupt Transition Delay from Falling Edge of RC	800		ns		
40	Serial In Set Up Time to Rising Edge of RC (Divide by one only)	80		ns		
41	Data Hold Time from rising edge of RC (Divide by one only)	350		ns		
42	Serial Output Data Valid from Falling Edge of TC (÷1)		440	ns		
43	Transmitter Clock Low Time	500		ns		
44	Transmitter Clock High Time	500		ns		
45	Transmitter Clock Cycle Time	1.05	∞	μs		
46	Receiver Clock Low Time	500		ns		
47	Receiver Clock High Time	500		ns		
48	Receiver Clock Cycle Time	1.05	∞	μs		
49	$\overline{CS}$, $\overline{IACK}$, $\overline{DS}$ Width Low		80	T_{CLK}		
50	Serial Output Data Valid from Falling Edge of TC (÷16)		490	ns		

NOTES:

1. $\overline{IEO}$ only goes low if no acknowledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain tri-stated.
2. $\overline{DTACK}$ will go low at A if spec. 14 is met; otherwise, $\overline{DTACK}$ will go low at B.
3. If the setup time is not met, $\overline{CS}$ or $\overline{IACK}$ will not be recognized until the next falling CLK.
4. If this setup time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off will be two clock cycles.

TIMER A. C. CHARACTERISTICS

Definitions:

Error = Indicated Time Value - Actual Time Value

tpsc = t_{CLK}x Prescale Value

Internal Timer Mode

Single Interval Error (free running) (Note 2)	± 100 ns
Cumulative Internal Error	0
Error Between Two Timer Reads	± (tpsc + 4 t_{CLK})
Start Timer to Stop Timer Error	2 t_{CLK} + 100 ns to - (tpsc + 6t_{CLK} + 100 ns)
Start Timer to Read Timer Error	0 to - (tpsc + 6t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (Note 3)	-2 t_{CLK} to - (4t_{CLK} +800 ns)

Pulse Width Measurement Mode

Measurement Accuracy (Note 1)	2 t_{CLK} to - (tpsc + 4t_{CLK})
Minimum Pulse Width	4t_{CLK}

Event Counter Mode

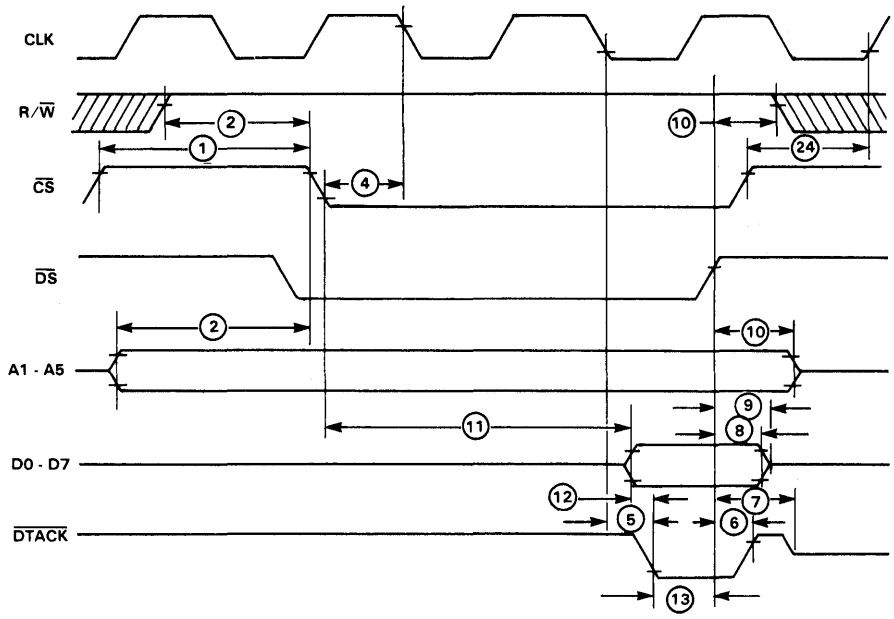
Minimum Active Time of TAI, TBI	4t_{CLK}
Minimum Inactive Time of TAI, TBI	4t_{CLK}

NOTES:

1. Error may be cumulative if repetitively performed.
2. Error with respect to T_{OUT} or INT if note 3 is true.
3. Assuming it is possible for the timer to make an interrupt request immediately.

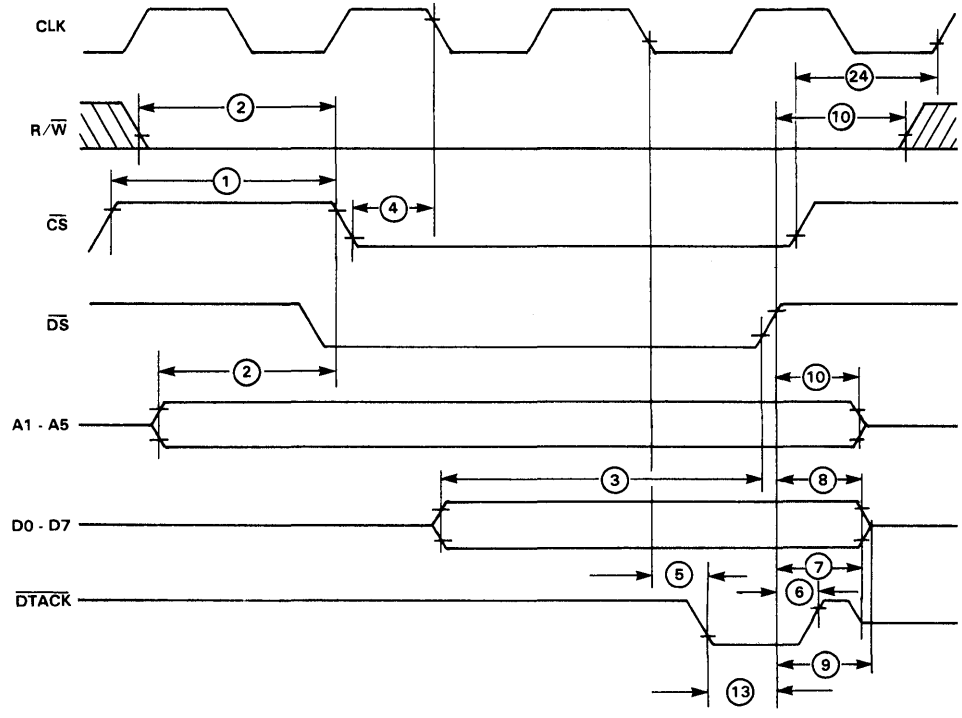
READ CYCLE

Figure 21



WRITE CYCLE

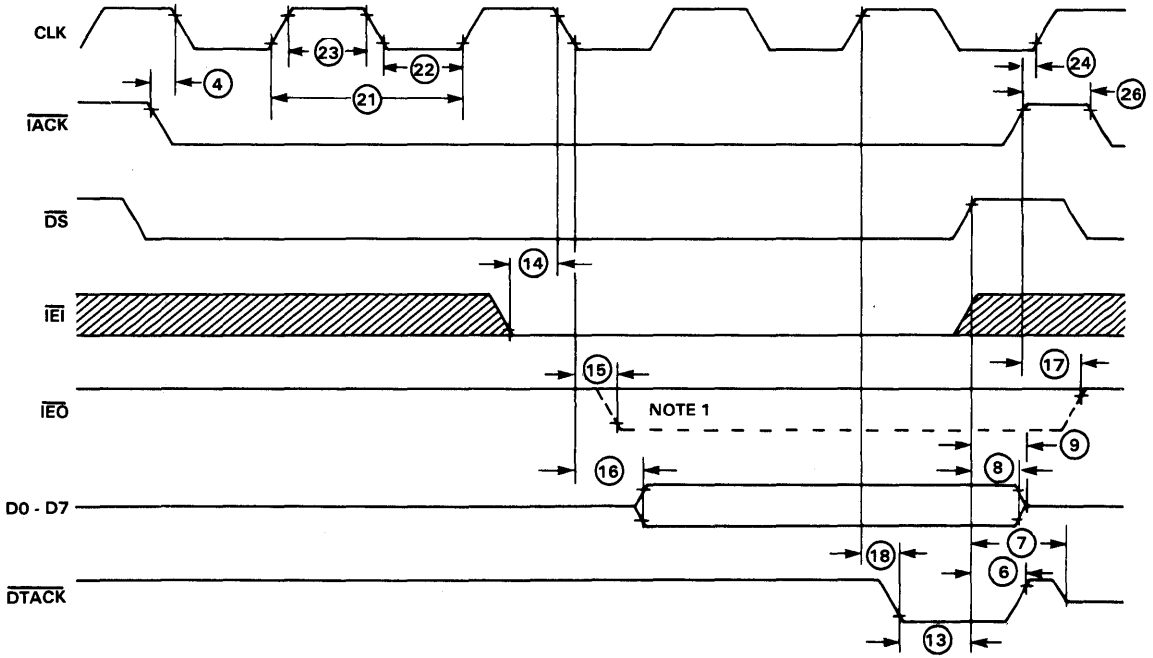
Figure 22



NOTE:
$\overline{CS}$ and $\overline{IACK}$ must be a function of $\overline{DS}$.

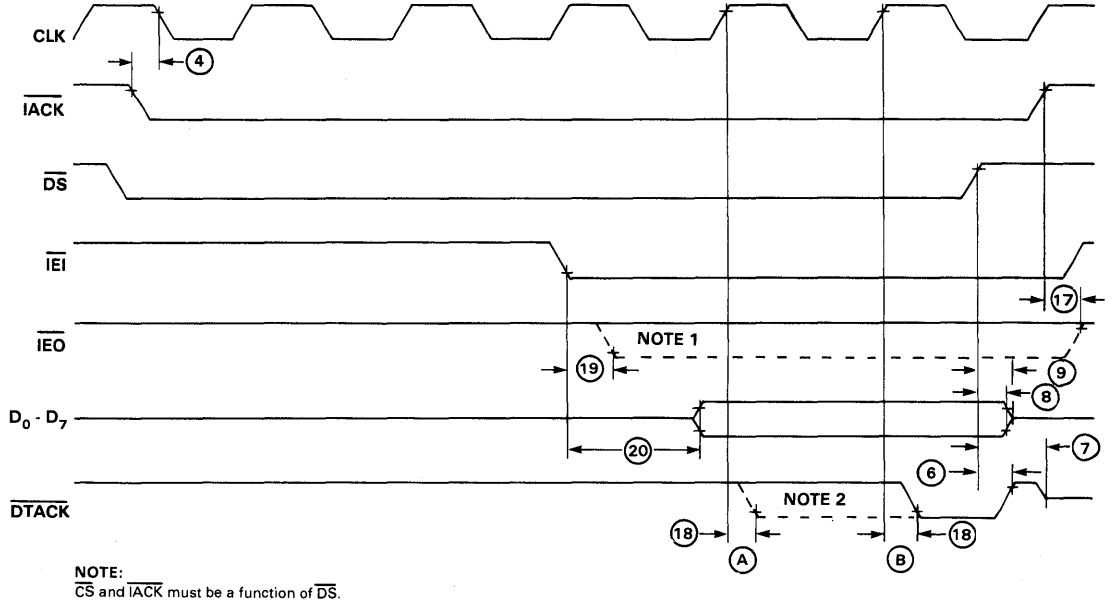
INTERRUPT ACKNOWLEDGE ($\overline{IEI}$ LOW)

Figure 23



INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ HIGH)

Figure 24

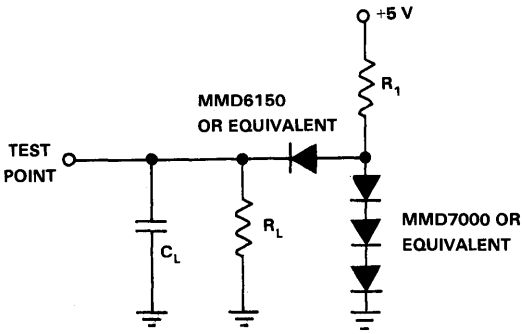


NOTE:
$\overline{CS}$ and $\overline{IACK}$ must be a function of $\overline{DS}$.

VI

TYPICAL OUTPUT

Figure 25



for all outputs except $\overline{DTACK}$

C_L = 100 pf

R_L = 20 k Ω

R_1 = 1.90 k Ω

for $\overline{DTACK}$

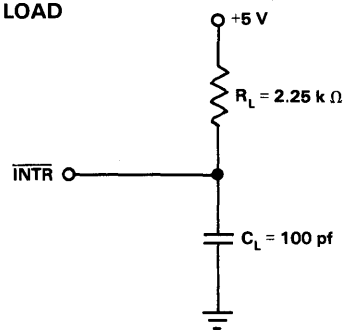
C_L = 130 pf

R_L = 6 k Ω

R_1 = 740 Ω

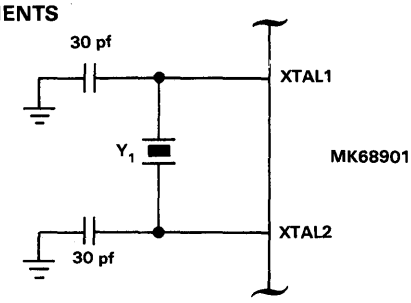
$\overline{INTR}$ TEST LOAD

Figure 26



MK68901 MFP EXTERNAL OSCILLATOR COMPONENTS

Figure 27



CRYSTAL PARAMETERS:

Parallel resonance, fundamental mode AT cut

$R_S \leq 150\ \Omega$ (F_R = 2.8 - 4.0 MHz);

$R_S \leq 300\ \Omega$ (F_R = 2.0 - 2.7 MHz)

C_L = 18 pf; C_M = 0.02 pf; C_h = 5 pf; L_M = 96 MHz

F_R (typ) = 2.4576 MHz

MK68901 ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX. CLOCK FREQUENCY	TEMPERATURE RANGE
MK68901	Ceramic	4.0 MHz	0° to 70°C

TEMPORARY ERRATA SHEET

MK68901 REV C

ERRATA SHEET FOR MK68901 REV C

The counters are initially loaded by writing to the Timer Data Register. When the timers are stopped, the information that was written to the TDR may not be correctly transferred to the internal time constant register. This would cause the first count sequence of the timer to be incorrect, but subsequent count sequences would be correct. If the initial count sequence is critical to system operation, a read should be used to verify that the correct data was loaded. If the readback indicates an error, the write/read loop should be performed until the data is verified.

1984/1985 MICROELECTRONIC DATA BOOK

MK3880A & B Z80 MICROCOMPUTER CENTRAL PROCESSING UNIT

FEATURES

- The Z80 is fully software compatible with the 8080A CPU. The 78 instructions of the 8080A are a subset of the Z80's 158 instructions.
- The extensive instruction set includes relative and indexed addressing, block searches and block transfers, word, byte, and bit data operations.
- The architecture provides duplicate sets of general purpose Flag and Index registers to allow background/foreground programming and easier single level interrupt processing. The registers also facilitate array and table processing.
- On chip Dynamic memory refresh counter
- Single +5 V supply
- Single phase system clock
- Vectored interrupt handling system. This system allows for a Daisy Chain arrangement of a priority interrupt scheme with little if any additional hardware.

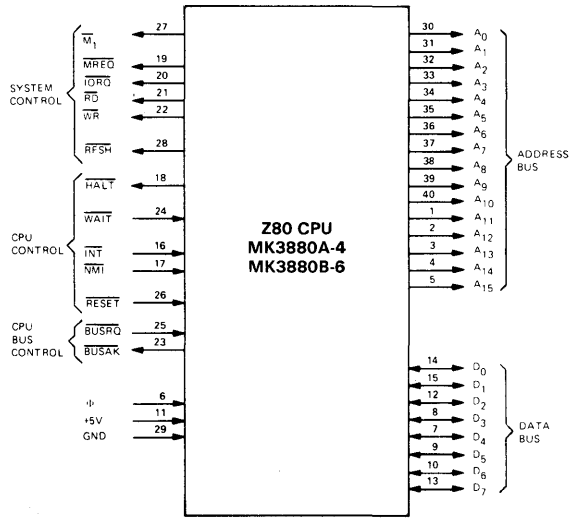
INTRODUCTION

The Mostek Z80 family of components is a significant advancement in the state-of-the-art of microcomputers. These components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices, a computer can be constructed with capabilities that only a minicomputer could deliver previously. This wide range of computational power allows standard modules to be constructed by a user that can satisfy the requirements of an extremely wide range of applications.

The Z80 Central Processing Unit is the heart of the Z80 family. It provides arithmetic and bus control to operate with the bussed peripheral controllers such as the Parallel I/O, Serial I/O, Counter/Timer, and Direct Memory Access Circuits. The Z80-CPU utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP.

Z80 PIN CONFIGURATION

Figure 1



Z80-CPU PIN DESCRIPTION

The Z80-CPU is packaged in an industry-standard 40 pin Dual In-Line Package. The I/O pins are shown in Figure 1, and the function of each is described below.

A_0-A_{15} (Address Bus) — Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes), data exchanges, and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to select up to 256 input or 256 output ports directly. A_0 is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D_0-D_7 (Data Bus) — Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

VII

$\overline{M_1}$ (Machine Cycle one)

Output, active low, $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, $\overline{M_1}$ is generated as each op-code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH, or FDH. $\overline{M_1}$ also occurs with $\overline{IORQ}$ to indicate an interrupt acknowledge cycle.

$\overline{MREQ}$ (Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/Output Request)

Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An $\overline{IORQ}$ signal is also generated with an M_1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during $\overline{M_1}$ time while I/O operations never occur during $\overline{M_1}$ time.

$\overline{RD}$ (Memory Read)

Tri-state output, active low. RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write)

Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh)

Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories. A_7 is a logic zero and the upper 8 bits of the Address Bus contain the I Register.

$\overline{HALT}$ (Halt state)

Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$* (Wait)

Output, active low. $\overline{WAIT}$ indicates to the Z80-CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

$\overline{INT}$ (Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the $\overline{BUSRQ}$ signal is not active. When the CPU accepts the interrupt, an acknowledge signal ($\overline{IORQ}$ during M_1 time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes.

$\overline{NMI}$

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z80-CPU to restart to location 0066_H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a $\overline{BUSRQ}$ will override an $\overline{NMI}$.

$\overline{RESET}$

Input, active low. $\overline{RESET}$ forces that program counter to zero and intializes the CPU. The CPU initialization will:

1) Disable the interrupt enable flip-flop
2) Set Register I = 00H
3) Set Register R = 00H
4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state. No refresh occurs.

$\overline{BUSRQ}$ Bus Request)

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control buses to a high impedance state as soon as

the current CPU machine cycle is terminated.

$\overline{BUSAK}$* Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Φ Single phase system clock.

*While the Z80-CPU is in either a $\overline{WAIT}$ state or a Bus Acknowledge condition, Dynamic Memory Refresh will not occur.

For further details on this device, please consult the MK3880 Z80 CPU Technical Manual.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... Specified Operating Range
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... -0.3 V to +7V
Power Dissipation ..... 1.5 W

All ac parameters assume a load capacitance of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

VII

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{ILC}	Clock Input Low Voltage	-0.3		0.8	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-6		V_{CC}+3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250 μA
I_{CC}	Power Supply Current			200	mA	
I_{LI}	Input Leakage Current			±10	μA	V_{IN} = 0 to V_{CC}
I_{LO}	Tri-State Output Leakage Current in Float			±10	μA	V_{OUT} = 0.4 V to V_{CC}

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground

SYMBOL	PARAMETER	MAX	UNIT
CΦ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, Unless Otherwise Noted

SIGNAL	SYMBOL	PARAMETER	3880A-4		3880B-6	
			MIN (ns)	MAX (ns)	MIN (ns)	MAX (ns)
Φ	t_c	Clock Period	250	[12]	165	[12]
	$t_w(\Phi H)$	Clock Pulse Width, Clock High	110	500	70	500
	$t_w(\Phi L)$	Clock Pulse Width, Clock Low	110	500	70	500
	$t_{r,f}$	Clock Rise and Fall Time		30		20
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110		90
	$t_{F(AD)}$	Delay to Float		90		80
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[13]		[24]	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[14]		[25]	
	t_{ca}	Address Stable From $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[15]		[26]	
	t_{caf}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[16]		[27]	
D_{0-7}	$t_{D(D)}$	Data Output Delay		150		130
	$t_{F(D)}$	Delay to Float During Write Cycle		90		80
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		30	
	$t_{S\Phi(D)}$	Data Setup Time to Falling Edge at Clock During M2 to M5	50		40	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[17]		[28]	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[18]		[29]	
	t_{cdf}	Data Stable from $\overline{WR}$	[19]		[30]	
	t_H	Input Hold Time	0		0	
$\overline{MREQ}$	$t_{DL\Phi(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low	20	85	20	70
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		85		70
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		85		70
	$t_{w(MRL)}$	Pulse Width, $\overline{MREQ}$ Low	[20]		[20]	
	$t_{w(MRH)}$	Pulse Width, $\overline{MREQ}$ High	[21]		[21]	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		75		65
	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		85		70
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		85		70
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		85		70
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		85		70
	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		95		80
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High	15	85	15	70
	$t_{DH\Phi(BD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		85		70
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		65		60
	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		80		70
	$t_{DH\Phi(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		80		70
	$t_{w(WRL)}$	Pulse Width, $\overline{WR}$ Low	[22]		[22]	

NOTES:

A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles. [Cont'd. on next page].

SIGNAL	SYMBOL	PARAMETER	3880 A-4 MIN (ns)	3880 A-4 MAX (ns)	3880 B-6 MIN (ns)	3880 B-6 MAX (ns)
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock M1 Low		100		80
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock M1 High		100		80
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		130		110
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		120		100
$\overline{WAIT}$	$t_{S(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		60	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300		260
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		70	
$\overline{NMI}$	$t_{w(NMI)}$	Pulse Width, $\overline{NMI}$ Low	80		70	
$\overline{BUSRQ}$	$t_{S(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	50	nsec	50	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		100		90
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		100		90
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	60		60	
	$t_{F(C)}$	Delay to/from Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		80		70
	t_{mr}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[23]		[31]	

[1] $t_{ACM} = t_w(\Phi H) + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{CA} = t_w(\Phi L) + t_r - 40$

[4] $t_{caf} = t_w(\Phi L) + t_r - 60$

[5] $t_{dcm} = t_C - 210$

[6] $t_{dci} = t_w(\Phi L) + t_r - 210$

[7] $t_{cdf} = t_w(\Phi L) + t_r - 80$

[8] $t_w(MRL) = t_c - 40$

[9] $t_w(MRH) = t_w(\Phi H) + t_f - 30$

[10] $t_w(WR) = t_c - 40$

[11] $t_{mr} = 2\,t_c + t_w(\Phi H) + t_f - 80$

[12] $t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$

[13] $t_{acm} = t_w(\phi H) + t_f - 65$

[14] $t_{aci} = t_c - 70$

[15] $t_{ca} = t_w(\Phi L) + t_r - 50$

[16] $t_{caf} = t_w(\Phi L) + t_r - 45$

[17] $t_{dcm} = t_c - 170$

[18] $t_{dci} = t_w(\Phi L) + t_r - 170$

[19] $t_{cdf} = t_w(\Phi L) + t_r - 70$

[20] $t_w(\overline{MRL}) = t_c - 30$

[21] $t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 20$

[22] $t_w(\overline{WR}) = t_c - 30$

[23] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$

[24] $t_{ACM} = t_w(\Phi H) + t_f - 50$

[25] $t_{aci} = t_c - 55$

[26] $t_{CA} = t_w(\Phi L) + t_r - 50$

[27] $t_{caf} = t_w(\Phi L) + t_r - 45$

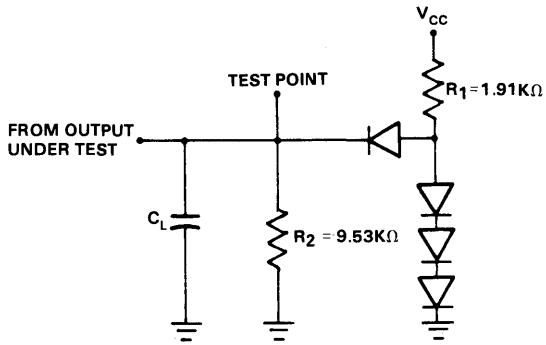
[28] $t_{dcm} = t_C - 140$

[29] $t_{dci} = t_w(\Phi L) + t_r - 140$

[30] $t_{cdf} = t_w(\Phi L) + t_r - 55$

[31] $t_{mr} = 2t_c + t_w(\Phi H) + t_f - 50$

LOAD CIRCUIT FOR OUTPUT



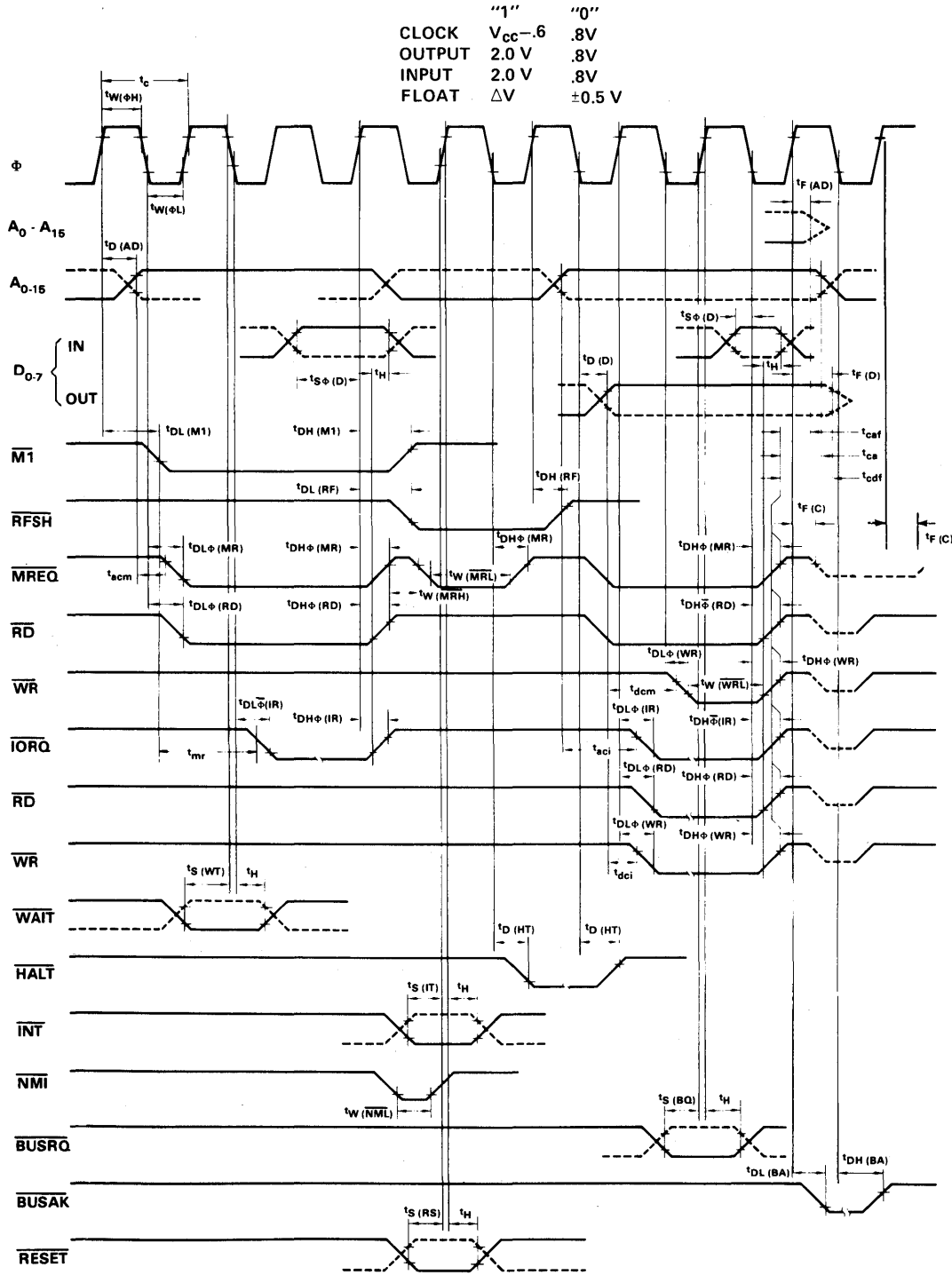
NOTES (Cont'd.)

Output Delay vs. Load Capacitance
$T_A = 70°C$ $V_{CC} = 5\ V \pm 5\%$
Add 10 nsec delay for each 50 pF increase in load up to a maximum of 200 pF for the data bus and 100 pF for address and control lines.

VII

A.C. TIMING DIAGRAM

Timing measurements are made at the following voltages, unless otherwise specified:



ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3880AN-04 Z80-CPU	Plastic	4.0 MHz	0° to +70°C
MK3880BN-06 Z80-CPU	Plastic	6.0 MHz	0° to +70°C

PARALLEL I/O CONTROLLER MK3881

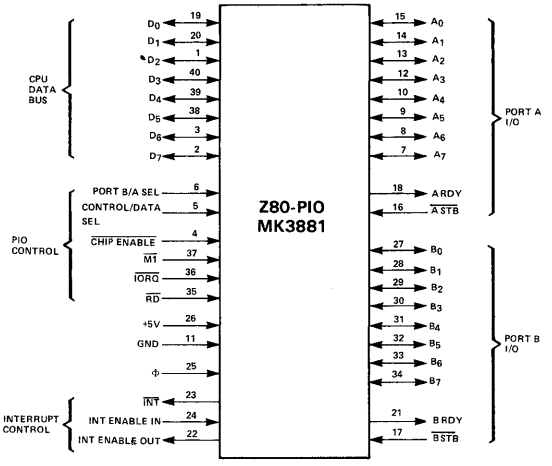
FEATURES

- Two independent 8 bit bidirectional peripheral interface ports with 'handshake' data transfer control
- Interrupt driven 'handshake' for fast response
- Any one of four distinct modes of operation may be selected for a port, including:
  - Byte output
  - Byte input
  - Byte bidirectional bus (Available on Port A only)
  - Bit control mode

  All with interrupt controlled handshake
- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Eight outputs are capable of driving Darlington transistors
- All inputs and outputs fully TTL compatible
- Single 5 volt supply and single phase clock required.

PIO PIN CONFIGURATION

Figure 1



INTRODUCTION

The Z80 Parallel I/O Circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z80-CPU. The CPU can configure the Z80-PIO to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the Z80-PIO include most keyboard, paper tape readers and punches, printers, PROM programmers, etc. The Z80-PIO utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP.

One of the unique features of the Z80-PIO that separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under total interrupt control. The interrupt logic of the PIO permits full usage of the efficient interrupt capabilities of the Z80-CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO so that additional circuits are not required. Another unique feature of the PIO is that it can be programmed to interrupt the CPU on the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the amount of time that the processor must spend in polling peripheral status.

PIN DESCRIPTION

A diagram of the Z80-PIO pin configuration is shown in Figure 1. This section describes the function of each pin.

D_7-D_0 — Z80-CPU Data Bus (bidirectional, tristate)
This bus is used to transfer all data and commands between the Z80-CPU and the Z80-PIO. D_0 is the least significant bit of the bus.

B/$\overline{A}$ Sel — Port B or A Select (input, active high)
This pin defines which port will be accessed during a data transfer between the Z80-CPU and the Z80-PIO. A low level on this pin selects Port A while a high level selects Port B. Often Address Bit A_0 from the CPU will be used for this selection function.

C/$\overline{D}$ Sel — Control or Data Select (input, active high)
This pin defines the type of data transfer to be performed between the CPU and the PIO. A

VII

high level on this pin during a CPU write to the PIO causes the Z80 data bus to be interpreted as a command for the port selected by the B/A Select line. A low level on this pin means that the Z80 data bus is being used to transfer data between the CPU and the PIO. Often Address bit A_1 from the CPU will be used for this function.

$\overline{CE}$ Chip Enable (input, active low)
A low level on this pin enables the PIO to accept command or data inputs from the CPU during a write cycle or to transmit data to the CPU during a read cycle. This signal is generally a decode of four I/O port numbers that encompass port A and B, data and Control.

Φ System Clock (input)
The Z80-PIO uses the standard Z80 system clock to synchronize certain signals internally. This is a single phase clock.

$\overline{M1}$ Machine Cycle One Signal from CPU (input, active low)
This signal from the CPU is used as a sync pulse to control several internal PIO operations. When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the Z80-CPU is fetching an instruction from memory. Conversely, when $\overline{M1}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrupt. In addition, the $\overline{M1}$ signal has two other functions within the Z80-PIO.

1. $\overline{M1}$ synchronizes the PIO interrupt logic.
2. When $\overline{M1}$ occurs without an active $\overline{RD}$ or $\overline{IORQ}$ signal, the PIO logic enters a reset state.

$\overline{IORQ}$ Input/Output Request from Z80-CPU (input, active low)
The $\overline{IORQ}$ signal is used in conjunction with the B/A Select, C/D Select, $\overline{CE}$, and $\overline{RD}$ signals to transfer commands and data between the Z80-CPU and the Z80-PIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are active, the port addressed by B/A will transfer data to the CPU (a read operation). Conversely, when $\overline{CE}$ and $\overline{IORQ}$ are active but $\overline{RD}$ is not active, then the port addressed by B/A will be written into from the CPU with either data or control information as specified by the C/D Select signal. Also, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the interrupting port will automatically place its interrupt vector on the CPU data bus if it is the highest device requesting an interrupt.

$\overline{RD}$ Read Cycle Status from the Z80-CPU (input, active low)
If $\overline{RD}$ is active a MEMORY READ or I/O READ operation is in progress. The $\overline{RD}$ signal is used with B/A Select, C/D Select, $\overline{CE}$ and $\overline{IORQ}$ signals to transfer data from the Z80-PIO to the Z80-CPU.

IEI Interrupt Enable In (input, active high)
This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

IEO Interrupt Enable Out (output, active high)
The IEO signal is the other signal required to form a daisy chain priority scheme. It is high only if IEI is high and the CPU is not servicing an interrupt from this PIO. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$ Interrupt Request (output, open drain, active low)
When INT is active the Z80-PIO is requesting an interrupt from the Z80-CPU.

A_0-A_7 Port A Bus (bidirectional, tri-state)
This 8 bit bus is used to transfer data and/or status or control information between Port A of the Z80-PIO and a peripheral device. A_0 is the least significant bit of the Port A data bus.

$\overline{A\ STB}$ Port A Strobe Pulse from peripheral Device (input, active low)
The meaning of this signal depends on the mode of operation selected for Port A as follows:

1) Output mode: The positive edge of this strobe is issued by the peripheral to acknowledge the receipt of data made available by the PIO.

2) Input mode: The strobe is issued by the peripheral to load data from the peripheral into the Port A input register. Data is loaded into the PIO when this signal is active.

3) Bidirectional mode: When this signal is active, data from the Port A output register is gated onto Port A bidirectional data bus. The positive edge of the strobe acknowledges the receipt of the data.

4) Control mode: The strobe is inhibited internally.

A RDY — Register A Ready (output, active high)
The meaning of this signal depends on the mode of operation selected for Port A as follows:

1) Output mode: This signal goes active to indicate that the Port A output register has been loaded and the peripheral data bus is stable and ready for transfer to the peripheral device.

2) Input mode: This signal is active when the Port A input register is empty and is ready to accept data from the peripheral device.

3) Bidirectional mode: This signal is active when data is available in Port A output register for transfer to the peripheral device. In this mode data is not placed on the Port A data bus unless $\overline{A\ STB}$ is active.

4) Control mode: This signal is disabled and forced to a low state.

B_0 - B_7 — Port B (bidirectional, tristate)
This 8 bit bus is used to transfer data and/or status or control information between Port B of the PIO and a peripheral device. The Port B data bus is capable of supplying 1.5 ma@ 1.5 V to drive Darlington transistors. B_0 is the least significant bit of the bus.

$\overline{B\ STB}$ — Port B Strobe Pulse from Peripheral Device (input, active low)
The meaning of this signal is similar to that of $\overline{A\ STB}$ with the following exception:

In the Port A bidirectional mode this signal strobes data from the peripheral device into the Port A input register.

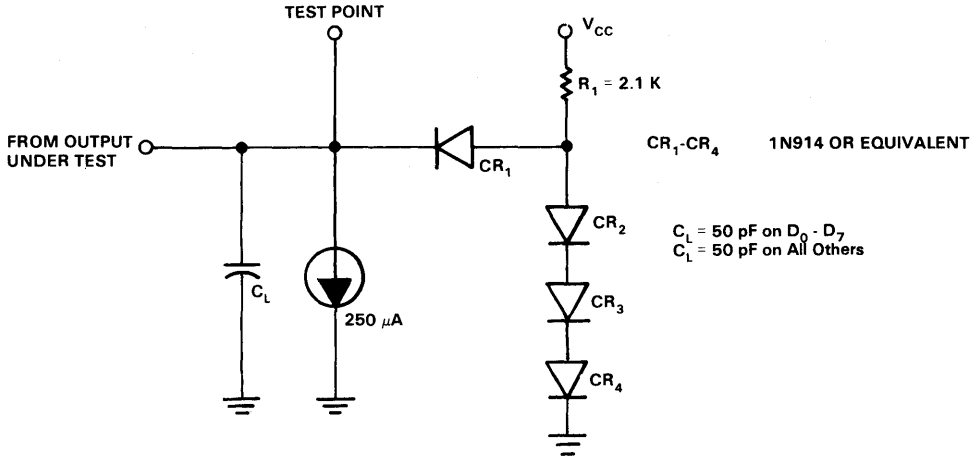
B RDY — Register B Ready (output, active high)
The meaning of this signal is similar to that of A Ready with the following exception:

In the Port A bidirectional mode this signal is high when the Port A input register is empty and ready to accept data from the peripheral device.

VII

OUTPUT LOAD CIRCUIT

Figure 2



For further details on this device, please consult the PIO MK3881 Technical Manual, included in Section IV.

ELECTRICAL SPECIFICATIONS

MK3881

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... Specified operating range
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect To Ground ..... -0.3 V to +7 V
Power Dissipation ..... .6 W

All ac parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		70*	mA	
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{LD}	Data Bus Leakage Current in Input Mode		±10	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V Port B Only

*150 mA for -4, -10, and -20 devices.

CAPACITANCE

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_Φ	Clock Capacitance	10	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

A.C. CHARACTERISTICS MK3881, MK3881-10, MK3881-20, Z80-PIO

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	3881 MIN	3881 MAX	3881-4 MIN	3881-4 MAX	UNIT
Φ	t_c	Clock Period	400	[1]	250	[1]	nsec
	$t_{W(\Phi H)}$	Clock Pulse Width, Clock High	170	2000	105	2000	nsec
	$t_{W(\Phi L)}$	Clock Pulse Width, Clock Low	170	2000	105	2000	nsec
	t_r, t_f	Clock Rise and Fall Times		30		30	nsec
	t_h	Any Hold Time for Specified Set-Up Time	0		0		nsec
C/D SEL $\overline{CE}$ ETC.	$t_{S\Phi(CS)}$	Control Signal Set-up Time to Rising Edge of Φ During Read or Write Cycle	145		145		nsec
D_0 - D_7	$t_{DR(D)}$	Data Output Delay from Falling Edge of RD		430		380	nsec
	$t_{S\Phi(D)}$	Data Set-up Time to Rising Edge of Φ During Write or $\overline{M1}$ Cycle	50		50		nsec
	$t_{DI(D)}$	Data Output Delay from Falling Edge of $\overline{IORQ}$ During $\overline{INTA}$ Cycle		340		250	nsec
	$t_{F(D)}$	Delay to Floating Bus (Output Buffer Disable Time)		160		110	nsec
IEI	$t_{S(IEI)}$	IEI Set-Up Time to Falling Edge of $\overline{IORQ}$ During $\overline{INTA}$ cycle	140		140		nsec
IEO	$t_{DH(IO)}$	IEO Delay Time from Rising Edge of IEI		210		160	nsec
	$t_{DL(IO)}$	IEO Delay Time from Falling Edge of IEI		190		130	nsec
	$t_{DM(IO)}$	IEO Delay from Falling Edge of M1 (Interrupt Occurring Just Prior to M1) See Note A.		300		190	nsec
$\overline{IORQ}$	$t_{S\Phi(IR)}$	$\overline{IORQ}$ Set-Up Time to Rising Edge of Φ During Read or Write Cycle	115		115		nsec
$\overline{M1}$	$t_{S\Phi(M1)}$	$\overline{M1}$ Set-Up Time to Rising Edge of Φ During $\overline{INTA}$ or $\overline{M1}$ Cycle. See Note B.	210		90		nsec
$\overline{RD}$	$t_{S\Phi(RD)}$	$\overline{RD}$ Set-Up Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	115		115		nsec
A_0 - A_7 B_0 - B_7	$t_{S(PD)}$	Port Data Set-Up Time to Rising Edge of $\overline{STROBE}$ (Mode 1)	260		230		nsec
	$t_{DS(PD)}$	Port Data Output Delay from Falling Edge of $\overline{STROBE}$ (Mode 2)		230		210	nsec
	$t_{F(PD)}$	Delay to Floating Port Data Bus from Rising Edge of $\overline{STROBE}$ (Mode 2)		200		180	nsec
	$t_{DI(PD)}$	Port Data Stable from Rising Edge of $\overline{IORQ}$ During $\overline{WR}$ Cycle (Mode 0)		200		180	nsec
$\overline{ASTB}$ $\overline{BSTB}$	$t_{W(ST)}$	Pulse Width, $\overline{STROBE}$	150 [4]		150 [4]		nsec nsec
$\overline{INT}$	$t_{D(IT)}$	$\overline{INT}$ Delay Time from Rising Edge of $\overline{STROBE}$		490		440	nsec
	$t_{D(IT3)}$	$\overline{INT}$ Delay Time from Data Match During Mode 3 Operation		420		380	nsec
ARDY	$t_{DH(RY)}$	Ready Response Time from Rising Edge of $\overline{IORQ}$		t_c+460		t_c+410	nsec
BRDY	$t_{DL(RY)}$	Ready Response Time from Rising Edge of $\overline{STROBE}$		t_c+ 400		t_c+ 360	nsec

VII

A. $2.5\ t_c > (N-2)t_{DL(IO)} + t_{DM(IO)} + t_{S(IEI)}$ + TTL Buffer Delay, if any.

B. $\overline{M1}$ must be active for a minimum of 2 clock periods to reset the PIO.

[1] $t_c = t_{W(\Phi H)} + t_{W(\Phi L)} + t_r + t_f$

[2] Increase $t_{DR(D)}$ by 10 nsec for each 50 pF increase in loading up to 200 pF max.

[3] Increase $t_{DI(D)}$ by 10 nsec for each 50 pF increase in loading up to 200 pF max.

[4] For Mode 2: $t_{W(ST)} > t_{S(PD)}$

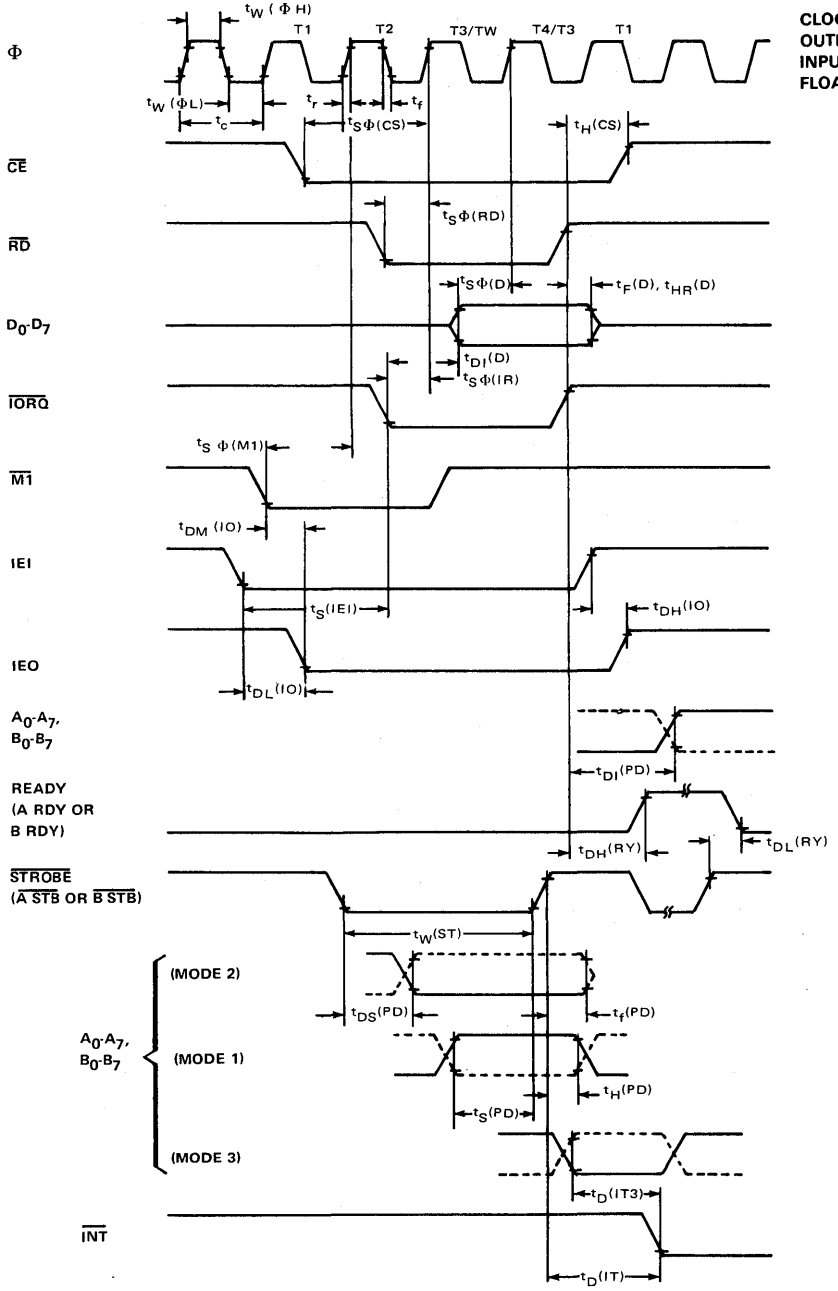
[5] Increase these values by 2 nsec for each 10 pF increase in loading up to 100 pF max.

TIMING DIAGRAM

Figure 3

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"		"0"
CLOCK	4.2 V		0.8 V
OUTPUT	2.0 V		0.8 V
INPUT	2.0 V		0.8 V
FLOAT	Δ V	=	0.5 V



ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3881N	Z80-PIO	Plastic	2.5 MHz	
MK3881P	Z80-PIO	Ceramic	2.5 MHz	
MK3881N-4	Z80A-PIO	Plastic	4.0 MHz	0° to 70°C
MK3881P-4	Z80A-PIO	Ceramic	4.0 MHz	
MK3881P-10	Z80-PIO	Ceramic	4.0 MHz	-40° to +85°C

COUNTER TIMER CIRCUIT MK3882

FEATURES

- ☐ All inputs and outputs fully TTL compatible
- ☐ Each channel may be selected to operate in either Counter Mode or Timer Mode
- ☐ Used in either mode, a CPU-readable Down Counter indicates number of counts-to-go until zero
- ☐ A Time Constant Register can automatically reload the Down Counter at Count Zero in Counter and Timer Mode
- ☐ Selectable positive or negative trigger initiates time operation in Timer Mode. The same input is monitored for event counts in Counter Mode.
- ☐ Three channels have Zero Count/Timeout outputs capable of driving Darlington transistors
- ☐ Interrupts may be programmed to occur on the zero count condition in any channel
- ☐ Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic

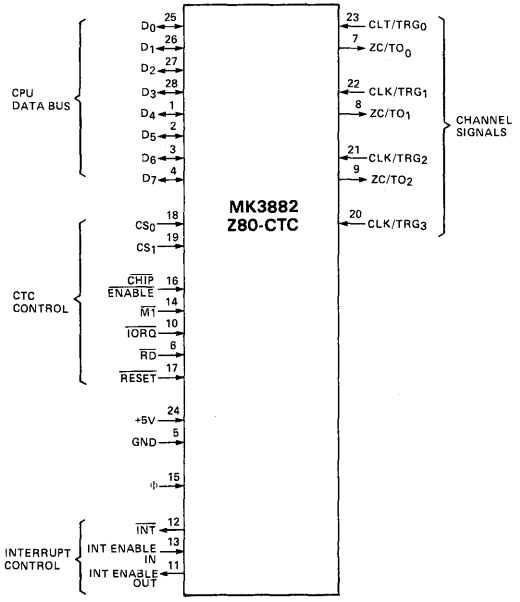
INTRODUCTION

The Z80-Counter Timer Circuit (CTC) is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z80-CPU. The CPU can configure the CTC channels to operate under various modes and conditions as required to interface with a wide range of devices. In most applications, little or no external logic is required. The Z80-CTC utilizes N-channel silicon gate depletion load technology and is packaged in a 28-pin DIP. The Z80-CTC requires only a single 5 volt supply and a one-phase 5 volt clock.

CTC PIN DESCRIPTION

A diagram of the Z80-CTC pin configuration is shown in Figure 1. This section describes the function of each pin.

Z80-CTC PIN CONFIGURATION
Figure 1



D_7-D_0 Z80-CPU Data Bus (bidirectional, tristate)
This bus is used to transfer all data and command words between the Z80-CPU and the Z80-CTC. There are 8 bits on this bus, of which D_0 is the least significant.

CS1-CS0 Channel Select (input, active high)
These pins form a 2-bit binary address code for selecting one of the four independent CTC channels for an I/O Write or Read (See truth table below.)

	CS1	CS0
Ch0	0	0
Ch1	0	1
Ch2	1	0
Ch3	1	1

$\overline{CE}$ Chip Enable (input, active low)
A low level on this pin enables the CTC to accept control words, Interrupt Vectors, or time constant data words from the Z80 Data

Bus during an I/O Write cycle, or to transmit the contents of the Down Counter to the CPU during an I/O Read cycle. In most applications this signal is decoded from the 8 least significant bits of the address bus for any of the four I/O port addresses that are mapped to the four Counter/Timer Channels.

Clock (Φ) — System Clock (input)
This single-phase clock is used by the CTC to synchronize certain signals internally.

$\overline{M1}$ — Machine Cycle One Signal from CPU (input, active low)
When $\overline{M1}$ is active and the $\overline{RD}$ signal is active, the CPU is fetching an instruction from memory. When $\overline{M1}$ is active and $\overline{IORQ}$ is active, the CPU is acknowledging an interrupt, alerting the CTC to place an Interrupt Vector on the Z80 Data Bus if it has daisy chain priority and one of its channels has requested an interrupt.

$\overline{IORQ}$ — Input/Output Request from CPU (input, active low)
The $\overline{IORQ}$ signal is used in conjunction with the $\overline{CE}$ and $\overline{RD}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus. If $\overline{IORQ}$ and $\overline{M1}$ are both true, the CPU is acknowledging an interrupt request, and the highest-priority interrupting channel will place its Interrupt Vector on the Z80 Data Bus.

$\overline{RD}$ — Read Cycle Status from the CPU (input, active low)
The $\overline{RD}$ signal is used in conjunction with the $\overline{IORQ}$ and $\overline{CE}$ signals to transfer data and Channel Control Words between the Z80-CPU and the CTC. During a CTC Write Cycle, $\overline{IORQ}$ and $\overline{CE}$ must be true and $\overline{RD}$ false. The CTC does not receive a specific write signal, instead generating its own internally from the inverse of a valid $\overline{RD}$ signal. In a CTC Read Cycle, $\overline{IORQ}$, $\overline{CE}$ and $\overline{RD}$ must be active to place the contents of the Down Counter on the Z80 Data Bus.

IEI — Interrupt Enable In (input, active high)
This signal is used to help form a system-wide interrupt daisy chain which establishes priorities when more than one peripheral device in the system has interrupting capability. A high level on this pin indicates that no other interrupting devices of higher priority are being serviced by the Z80-CPU.

IEO — Interrupt Enable Out (output, active high)
The IEO signal, in conjunction with IEI, is used to form a system-wide interrupt priority daisy chain. IEO is high only if IEI is high and the CPU is not servicing an interrupt from any CTC channel. Thus this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by the CPU.

$\overline{INT}$ — Interrupt Request (output, open drain, active low)
This signal goes true when any CTC channel which has been programmed to enable interrupts has a zero-count condition in its Down Counter.

$\overline{RESET}$ — Reset (input, active low)
This signal stops all channels from counting and resets channel interrupt enable bits in all control registers, thereby disabling CTC-generated interrupts. The ZC/TO and $\overline{INT}$ outputs go to their inactive states, IEO reflects IEI, and the CTC's data bus output drivers go to the high impedance state.

CLK/TRG3-CLK/TRG0 — External Clock/Timer Trigger (input, user-selectable active high or low)
There are four CLK/TRG pins, corresponding to the four independent CTC channels. In the Counter Mode, every active edge on this pin decrements the Down Counter. In the Timer Mode, an active edge on this pin initiates the timing function. The user may select the active edge to be either rising or falling.

ZC/TO2—ZC/TO0 — Zero Count/Timeout (output, active high)
There are three ZC/TO pins, corresponding to CTC channels 2 through 0. (Due to package pin limitations channel 3 has no ZC/TO pin.) In either Counter Mode or Timer Mode, when the Down Counter decrements to zero an active high going pulse appears at this pin.

For further details on this device, please consult the CTC MK3882 Technical Manual, included in Section IV.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... Specified operating range
Storage Temperature ..... -65°C to +150°C
Voltage On Any Pin With Respect To Ground ..... -0.3 V to +7 V
Power Dissipation ..... 0.8 W

All ac parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5 V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage (1)	V_{CC} -.6	V_{CC} +.3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -250 μA
I_{CC}	Power Supply Current		120	mA	T_C = 400 nsec**
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT} = 2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V
I_{OHD}	Darlington Drive Current	-1.5		mA	V_{OH} = 1.5 V

**T_C = 250 nsec for MK3882-4

CAPACITANCE

T_A = 25°C, f = 1 MHz

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_Φ	Clock Capacitance	20	pF	Unmeasured Pins
C_{IN}	Input Capacitance	5	pF	Returned to Ground
C_{OUT}	Output Capacitance	10	pF	

VII

A.C. CHARACTERISTICS MK3882, MK3882-10, Z80-CTC

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

SIGNAL	SYMBOL	PARAMETER	38823882-4 MIN	38823882-4 MAX	MIN	MAX	UNIT	COMMENTS
Φ	t_C	Clock Period	400	(1)	250	(1)	ns	
	t_W(ΦH)	Clock Pulse Width, Clock High	170	2000	105	2000	ns	
	t_W(ΦL)	Clock Pulse Width, Clock Low	170	2000	105	2000		
	t_r, t_f	Clock Rise and Fall Times		30		30	ns	
	t_H	Any Hold Time for Specified Setup Time	0		0		ns	
CS, $\overline{CE}$, etc.	t_SΦ(CS)	Control Signal Setup Time to Rising Edge of Φ During Read or Write Cycle	160		145		ns	
	t_DΦ(D)	Data Output Delay from Rising Edge of Φ During Read Cycle		240		200	ns	(2)
	t_SΦ(D)	Data Setup Time to Rising Edge of Φ During Write or M1 Cycle	60		50		ns	
D_0 - D_7	t_{DI}(D)	Data Output Delay from Falling Edge of $\overline{IORQ}$ During INTA Cycle		340		160	ns	(2)
	t_F(D)	Delay to Floating Bus (Output Buffer Disable Time)		230		110	ns	
IEI	t_S(IEI)	IEI Setup Time to Falling Edge of $\overline{IORQ}$ During INTA Cycle	200		140		ns	
	t_{DH}(IO)	IEO Delay Time from Rising Edge of IEI		220		160	ns	(3)
	t_{DL}(IO)	IEO Delay Time from Falling Edge of IEI		190		130	ns	(3)
IEO	t_{DM}(IO)	IEO Delay from Falling Edge of $\overline{M1}$ (Interrupt Occurring just Prior to $\overline{M1}$)		300		190	ns	(3)
$\overline{IORQ}$	t_SΦ(IR)	$\overline{IORQ}$ Setup Time to Rising Edge of Φ During Read or Write Cycle	250		115		ns	
$\overline{M1}$	t_SΦ(M1)	$\overline{M1}$ Setup Time to Rising Edge of Φ During INTA or $\overline{M1}$ Cycle	210		90		ns	
$\overline{RD}$	t_SΦ(RD)	$\overline{RD}$ Setup Time to Rising Edge of Φ During Read or $\overline{M1}$ Cycle	240		115		ns	
$\overline{INT}$	t_DΦ(IT)	$\overline{INT}$ Delay from Rising Edge of Φ		t_C(Φ) + 200		t_C(Φ) + 140		(7)
	t_C(CK)	Clock Period	2t_C(Φ)		2t_C(Φ)			(5)
	t_r, t_f	Clock and Trigger Rise and Fall Times		50		50	ns	
	t_S(CK)	Clock Setup Time to Rising Edge of Φ for Immediate Count	210		130		ns	(5)
	t_S(TR)	Trigger Setup Time to Rising Edge of Φ for Enabling of Prescaler on Following Rising Edge of Φ	210		130		ns	(6)
CLK/ TRG_{0-3}	t_W(CTH)	Clock and Trigger High Pulse Width	200		120		ns	(7)
	t_W(CTL)	Clock and Trigger Low Pulse Width	200		120		ns	(7)

A.C. CHARACTERISTICS MK3882, MK3882-10, Z80-CTC (Cont'd)

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5%, unless otherwise noted

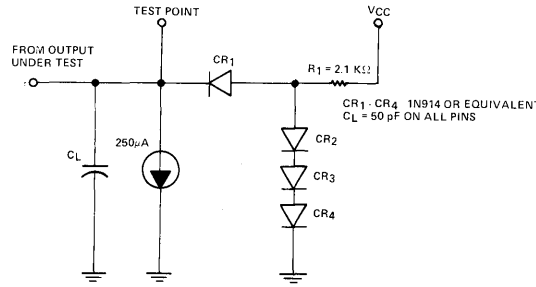
SIGNAL	SYMBOL	PARAMETER	3882 MIN	3882 MAX	3882-4 MIN	3882-4 MAX	UNIT	COMMENTS
	$t_{DH}(ZC)$	ZC/TO Delay Time from Rising Edge of Φ, ZC/TO High		190		120	ns	(7)
ZC/ TO_{0-2}	$t_{DL}(ZC)$	ZC/TO Delay Time from Falling Edge of Φ, ZC/TO Low		190		120	ns	(7)

NOTES:

1. $t_C = t_W(\Phi H) + t_W(\Phi L) + t_r + t_f$.
2. Increase delay by 10 nsec for each 50 pF increase in loading 200 pF maximum for data lines and 100 pF for control lines.
3. Increase delay by 2 nsec for each 10 pF increase in loading, 100 pF maximum.
4. $\overline{\text{RESET}}$ must be active for a minimum of 3 clock cycles.
5. Counter mode
6. Timer mode
7. Counter and Timer mode

OUTPUT LOAD CIRCUIT

Figure 2



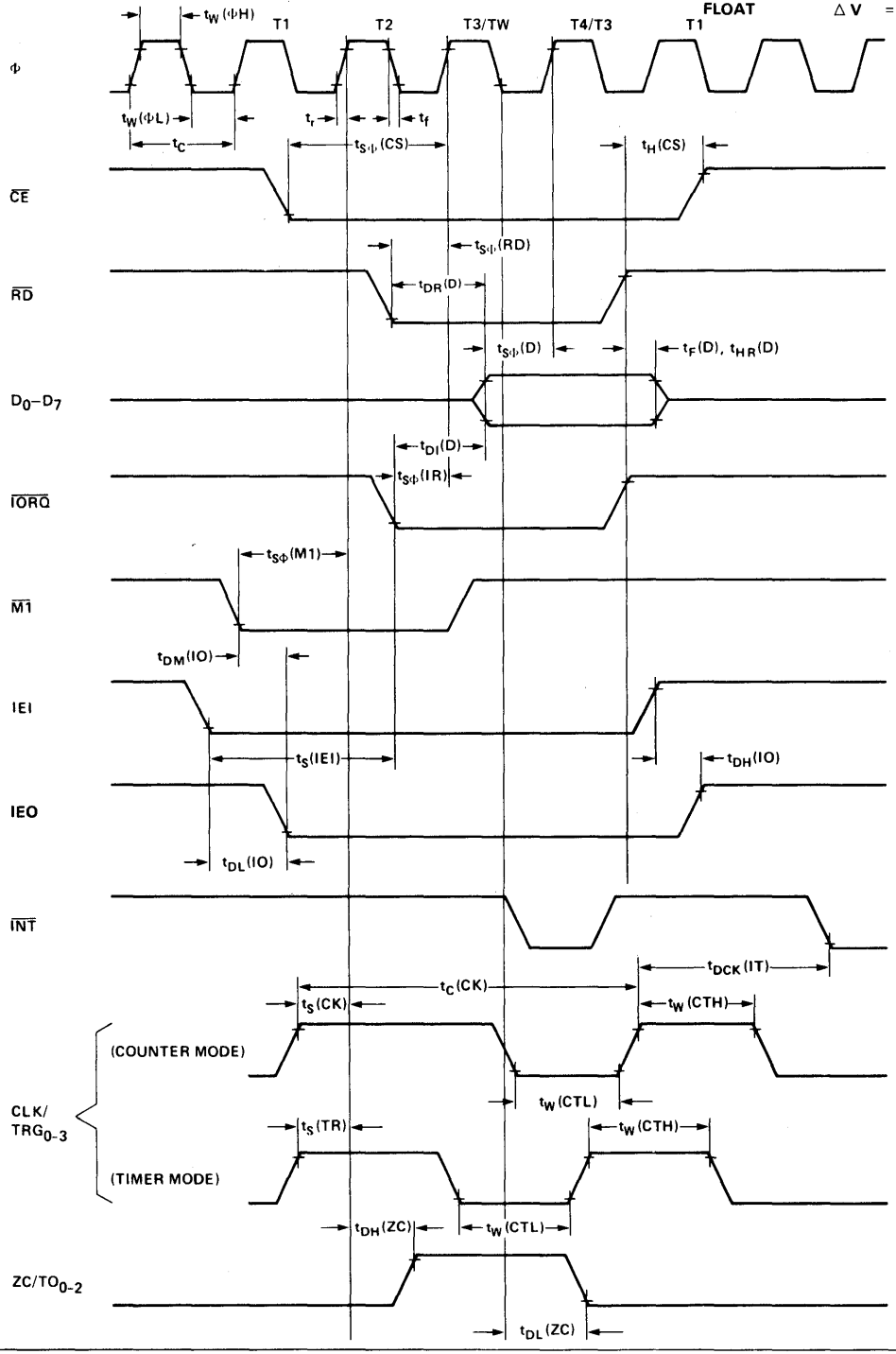
VII

TIMING DIAGRAM

Figure 3

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"		"0"
CLOCK	4.2 V		0.8 V
OUTPUT	2.0 V		0.8 V
INPUT	2.0 V		0.8 V
FLOAT	Δ V	=	0.5 V



ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3882N	Z80-CTC	Plastic	2.5 MHz	
MK3882P	Z80-CTC	Ceramic	2.5 MHz	
MK3882N-4	Z80A-CTC	Plastic	4.0 MHz	0° to 70°C
MK3882P-4	Z80A-CTC	Ceramic	4.0 MHz	
MK3882P-10	Z80-CTC	Ceramic	4.0 MHz	-40° to +85°C

DIRECT MEMORY ACCESS CONTROLLER MK3883

FEATURES

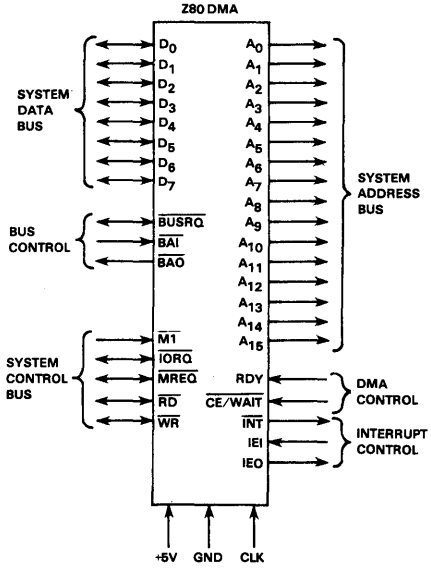
- Transfers, searches and search/transfers in byte-at-a-time, burst or continuous modes. Cycle length and edge timing can be programmed to match the speed of any port.
- Dual port addresses (source and destination) generated for memory-to-I/O, memory-to-memory, or I/O-to-I/O operations. Addresses may be fixed or automatically incremented/decremented.
- Next-operation loading without disturbing current operations via buffered starting-address registers. An entire previous sequence can be repeated automatically.
- Extensive programmability of functions. CPU can read complete channel status.
- Standard Z80 Family bus-request and prioritized interrupt-request daisy chains implemented without external logic. Sophisticated, internally modifiable interrupt vectoring.
- Direct interfacing to system buses without external logic.

GENERAL DESCRIPTION

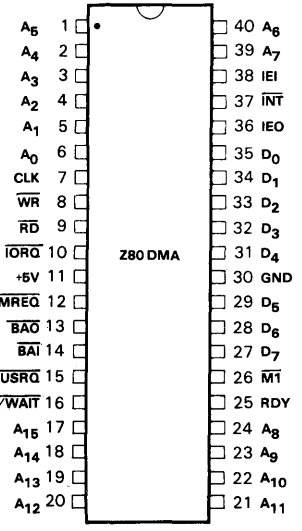
The MK3883 Z80 DMA (Direct Memory Access) is a powerful and versatile device for controlling and processing transfers of data. Its basic function of managing CPU-independent transfers between two ports is augmented by an array of features that optimize transfer speed and control with little or no external logic in systems using an 8- or 16-bit data bus and a 16-bit address bus.

VII

PIN FUNCTIONS
Figure 1



PIN ASSIGNMENTS
Figure 2



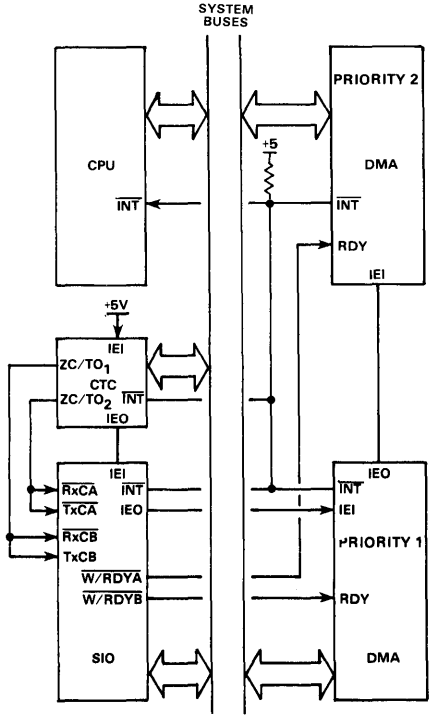
Transfers can be done between any two ports (source and destination), including memory-to-I/O, memory-to-memory, and I/O-to-I/O. Dual port addresses are automatically generated for each transaction and may be either fixed or incrementing/decrementing. In addition, bit-maskable byte searches can be performed either concurrently with transfers or as an operation in itself.

The MK3883 Z80 DMA contains direct interfacing to and independent control of system buses, as well as sophisticated bus and interrupt controls. Many programmable features, including variable cycle timing and auto-restart minimize CPU software overhead. They are especially useful in adapting this special-purpose transfer processor to a broad variety of memory, I/O and CPU environments.

The MK3883 Z80 DMA is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a single +5V power supply and the standard Z80 Family single-phase clock.

Z80 ENVIRONMENT WITH MULTIPLE DMA CONTROLLERS

Figure 3



FUNCTIONAL DESCRIPTION

Classes of Operation

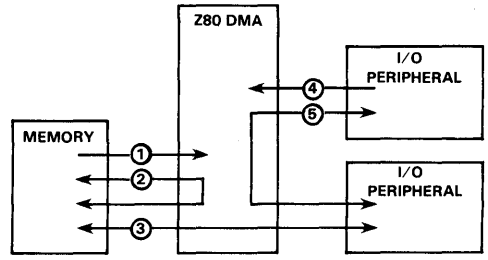
The MK3883 Z80 DMA has three basic classes of operation:

- Transfers of data between two ports (memory or I/O peripheral)
- Searches for a particular 8-bit maskable byte at a single port in memory or an I/O peripheral
- Combined transfers with simultaneous search between two ports

Figure 4 illustrates the basic functions served by these classes of operation.

BASIC FUNCTIONS OF THE Z80 DMA

Figure 4



1. Search memory
2. Transfer memory-to-memory (optional search)
3. Transfer memory-to-I/O (optional search)
4. Search I/O
5. Transfer I/O-to-I/O (optional search)

During a transfer, the DMA assumes control of the system control, address, and data buses. Data is read from one addressable port and written to the other addressable port, byte by byte. The ports may be programmed to be either system main memory or peripheral I/O devices. Thus, a block of data may be written from one peripheral to another, from one area of main memory to another, or from a peripheral to main memory and vice versa.

During a search-only operation, data is read from the source port and compared byte by byte with the DMA-internal register containing a programmable match byte. This match byte may optionally be masked so that only certain bits within the match byte are compared. Search rates up to 1.25M bytes per second can be obtained with the 2.5MHz MK3883 Z80 DMA or 2M bytes per second with the 4MHz MK3883-4 Z80 DMA.

In combined searches and transfers, data is transferred between two ports while simultaneously searching for a bit-maskable byte match.

Data transfers or searches can be programmed to stop or interrupt under various conditions. In addition, CPU-readable status bits can be programmed to reflect the condition.

Modes of Operation

The MK3883 Z80 DMA can be programmed to operate in one of three transfer and/or search modes:

- Byte-at-a-time: data operations are performed one byte at a time. Between each byte operation the system buses are released to the CPU. The buses are requested again for each succeeding byte operation.
- Burst: data operations continue until a port's Ready line to the DMA goes inactive. The DMA then stops and releases the system buses after completing its current byte operation.
- Continuous: data operations continue until the end of the programmed block of data is reached before the system buses are released. If a port's Ready line goes inactive before this occurs, the DMA simply pauses until the Ready line comes active again.

In all modes, once a byte of data is read into the DMA, the operation on the byte will be completed in an orderly fashion, regardless of the state of other signals (including a port's Ready line).

Due to the DMA's high-speed buffered method of reading data, operations on one byte are not completed until the next byte is read in. Consequently, total transfer or search block lengths must be two or more bytes, and those block lengths programmed into the DMA must be one byte less than the desired block length (count is N-1 where N is the block length).

Commands and Status

The Z80 DMA has several writeable control registers and readable status registers available to the CPU. Control bytes can be written to the DMA while the DMA is enabled or disabled, but the act of writing a control byte to the DMA disables the DMA until it is again enabled by a specific command. Status bytes can also be read at any time, but writing the Read Status command or the Read Mask command disables the DMA.

Control bytes to the DMA include those which effect immediate command actions such as enable, disable, reset, load starting-address buffers, continue, clear counters, clear status bits and the like. In addition, many mode-setting control bytes can be written, including mode and class of operation, port configuration, starting addresses, block length, address counting rule, match and match-mask byte, interrupt conditions, interrupt vector, status-affects-vector condition, pulse counting, auto restart, Ready-line and Wait-line rules, and read mask.

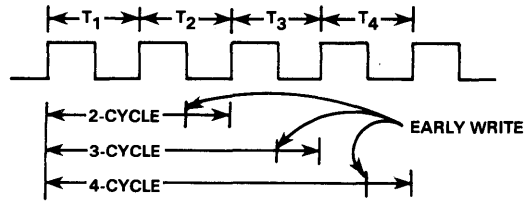
Readable status registers include a general status byte reflecting Ready-line, end-of-block, byte-match and interrupt conditions, as well as Dual-byte registers for the current byte count, Port A address and Port B address.

Variable Cycle

The Z80 DMA has the unique feature of programmable operation-cycle length. This is valuable in tailoring the DMA to the particular requirements of other system components (fast or slow) and maximizes the data-transfer rate. It also eliminates external logic for signal conditioning.

There are two aspects to the variable cycle feature. First, the entire read and write cycles (periods) associated with the source and destination ports can be independently programmed as 2, 3 or 4 T-cycles long (more if Wait cycles are used), thereby increasing or decreasing the speed with which all DMA signals change (Figure 5).

VARIABLE CYCLE LENGTH
Figure 5



Second, the four signals in each port specifically associated with transfers of data (I/O Request, Memory Request, Read and Write) can each have its active trailing edge terminated one-half T-cycle early. This adds a further dimension of flexibility and speed, allowing such things as shorter-than-normal Read or Write signals that go inactive before data starts to change.

Address Generation

Two 16-bit addresses are generated by the Z80 DMA for every transfer or search operation, one address for the source Port A and another for the destination Port B. Each address can be either variable or fixed. Variable addresses can increment or decrement from the programmed starting address. The fixed-address capability eliminates the need for separate enabling wires to I/O ports.

Port addresses are multiplexed onto the system address bus, depending on whether the DMA is reading the source port or writing to the destination port. Two readable address counters (2-bytes each) keep the current address of each port.

Auto Restart

The starting addresses of either port can be reloaded automatically at the end of a block. This option is selected by the Auto Restart control bit. The byte counter is cleared when the addresses are reloaded.

The Auto Restart feature relieves the CPU of software overhead for repetitive operations such as CRT refresh and many others. Moreover, the CPU can write different starting addresses into buffer registers during transfers causing the Auto Restart to begin at a new location.

Interrupts

The MK3883 Z80 DMA can be programmed to interrupt the CPU on four conditions:

- Interrupt on Ready (before requesting bus)
- Interrupt on Match
- Interrupt on End of Block
- Interrupt on Match at End of Block

Any of these interrupts cause an interrupt-pending status bit to be set, and each of them can optionally alter the DMA's interrupt vector. Due to the buffered constraint mentioned under "Modes of Operation," interrupts on Match at End of Block are caused by matches to the byte just prior to the last byte in the block.

The DMA shares the Z80 family's elaborate interrupt scheme, which provides fast interrupt service in real-time applications. In a Z80 CPU environment, the DMA passes its internally modifiable 8-bit interrupt vector to the CPU, which adds an additional eight bits to form the memory address of the interrupt-routine table. This table contains the address of the beginning of the interrupt routine itself.

In this process, CPU control is transferred directly to the interrupt routine, so that the next instruction executed after an interrupt acknowledge is the first instruction of the interrupt routine itself.

Pulse Generation

External devices can keep track of how many bytes have been transferred by using the DMA's pulse output, which provides a signal at 256-byte intervals. The interval sequence may be offset at the beginning by 1 to 255 bytes.

The interrupt line outputs the pulse signal in a manner that prevents misinterpretation by the CPU as an interrupt request, since it only appears when the Bus Request and Bus Acknowledge lines are both active.

PIN DESCRIPTIONS

A_0-A_{15}. System Address Bus (output, 3-state). Addresses generated by the DMA are sent to both source and destination ports (main memory or I/O peripherals) on these lines.

$\overline{BAI}$. Bus Acknowledge In (input, active Low). Signals that the system buses have been released for DMA control. In multiple-DMA configurations, the $\overline{BAI}$ pin of the highest priority DMA is normally connected to the Bus Acknowledge pin of the CPU. Lower-priority DMAs have their $\overline{BAI}$ connected to the $\overline{BAO}$ of a higher-priority DMA.

$\overline{BAO}$. Bus Acknowledge Out (output, active Low). In a multiple-DMA configuration, this pin signals that no other higher-priority DMA has requested the system busses. $\overline{BAI}$ and $\overline{BAO}$ form a daisy chain for multiple-DMA priority resolution over bus control.

$\overline{BUSRQ}$. Bus Request (bidirectional, active Low, open drain). As an output, it sends requests for control of the system address bus, data bus and control bus to the CPU. As an input when multiple DMAs are strung together in a priority daisy chain via $\overline{BAI}$ and $\overline{BAO}$, it senses when another DMA has requested the buses and causes this DMA to refrain from bus requesting until the other DMA is finished. Because it is a bidirectional pin, there cannot be any buffers between this DMA and any other DMA. It can, however, have a unidirectional into the CPU. A pull-up resistor is connected to this pin.

$\overline{CE}$/$\overline{WAIT}$. Chip Enable and Wait (input, active Low). Normally this functions only as a $\overline{CE}$ line, but it can also be programmed to serve a $\overline{WAIT}$ function. As a $\overline{CE}$ line from the CPU, it becomes active when $\overline{WR}$ and $\overline{IORQ}$ are active and the I/O port address on the system address bus is the DMA's address, thereby allowing a transfer of control or command bytes from the CPU to the DMA. As a $\overline{WAIT}$ line from memory or I/O devices, after the DMA has received a bus-request acknowledge from the CPU, it causes wait states to be inserted in the DMA's operation cycles thereby slowing the DMA to a speed that matches the memory or I/O device.

CLK. System clock (input). Standard Z80 single-phase clock at 2.5MHz (MK3883) or 4.0MHz (MK3883-4). For slower system clocks, a TTL gate with a large pullup resistor may be adequate to meet the timing and voltage level specification. For higher-speed systems, use a clock driver with an active pullup to meet the V_{IH} specification and risetime requirements. In all cases there should be a resistive pullup to the power supply of 10K ohms (max) to ensure proper power when the DMA is reset.

D_0-D_7. System Data Bus (bidirectional, 3-state). Commands from the CPU, DMA status, and data from memory or I/O peripherals are transferred on these lines.

IEI. Interrupt Enable In (input, active High). This is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this DMA. Thus, this signal blocks lower-priority devices from interrupting while a higher-priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. Interrupt Request (output, active Low, open drain). This requests a CPU interrupt. The CPU acknowledges the interrupt by pulling its $\overline{IORQ}$ output Low during an $\overline{M1}$ cycle. It is typically connected to the $\overline{INT}$ pin of the CPU with a pullup resistor and tied to all other $\overline{INT}$ pins in the system.

$\overline{IORQ}$. Input/Output Request (bidirectional, active Low, 3-state). As an input, this indicates that the lower half of the address bus holds a valid I/O port address for transfer of control or status bytes from or to the CPU, respectively; this DMA is the addressed port if its $\overline{CE}$ pin and its $\overline{WR}$ or $\overline{RD}$ pins are simultaneously active. As an output, after the DMA has taken control of the system busses, it indicates that the lower half of the address bus holds a valid port address for another I/O device involved in a DMA transfer of data. When $\overline{IORQ}$ and $\overline{M1}$ are both active simultaneously, an interrupt acknowledge is indicated.

$\overline{M1}$. Machine Cycle One (input, active Low). Indicates that the current CPU machine cycle is an instruction fetch. It is used by the DMA to decode the return-from-interrupt instruction (RETI) (ED-4D) sent by the CPU. During two-byte instruction fetches, $\overline{M1}$ is active as each opcode byte is fetched. An interrupt acknowledge is indicated when both $\overline{M1}$ and $\overline{IORQ}$ are active.

$\overline{MREQ}$. Memory Request (bidirectional, active Low, 3-state). This indicates that the address bus holds a valid address for a memory read or write operation. As an input, it indicates that control or status information from or to memory is to be transferred to the DMA, if the DMA's $\overline{CE}$ and $\overline{WR}$ or $\overline{RD}$ lines are simultaneously active. As an output, after the DMA has taken control of the system buses, it indicates a DMA transfer request from or to memory.

$\overline{RD}$. Read (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to read status bytes from the DMA's read registers. As an output, after the DMA has taken control of the system buses, it indicates a DMA-controlled read from a memory or I/O port address.

$\overline{WR}$. Write (bidirectional, active Low, 3-state). As an input, this indicates that the CPU wants to write control or command bytes to the DMA write registers. As an output, after the DMA has taken control of the system busses, it indicates a DMA-controlled write to a memory or I/O port address.

RDY. Ready (input, programmable active Low or High). This is monitored by the DMA to determine when a peripheral device associated with a DMA port is ready for a read or write operation. Depending on the mode of DMA operation (byte, burst or continuous), the RDY line indirectly controls DMA activity by causing the $\overline{BUSRQ}$ line to go Low or High.

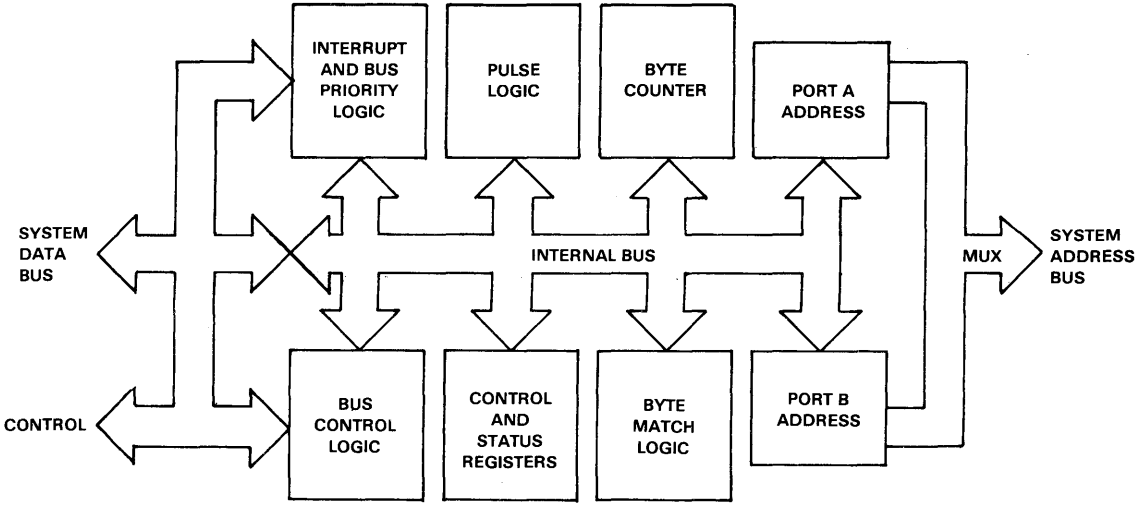
INTERNAL STRUCTURE

The internal structure of the MK3883 Z80 DMA includes driver and receiver circuitry for interfacing with an 8-bit system data bus, a 16-bit system address bus, and system control lines (Figure 6). In a Z80 CPU environment, the DMA can be tied directly to the analogous pins on the CPU (Figure 7) with no additional buffering, except for the $\overline{CE/WAIT}$ line.

The DMA's internal data bus interfaces with the system data bus and services all internal logic and registers. Addresses generated from this logic for Ports A and B (source and destination) of the DMA's single transfer channel are multiplexed onto the system address bus.

VII

BLOCK DIAGRAM
Figure 6



Specialized logic circuits in the DMA are dedicated to the various functions of external bus interfacing, internal bus control, byte matching, byte counting, periodic pulse generation, CPU interrupts, bus requests, and address generation. A set of twenty-one writeable control registers and seven readable status registers provide the means by which the CPU governs and monitors the activities of these logic circuits. All registers are eight bits wide, with double-byte information stored in adjacent registers. The two starting-address registers (two bytes each) for Ports A and B are buffered.

The 21 writeable control registers are organized into seven base-register groups, most of which have multiple registers. The base registers in each writeable group contain both control/command bits and pointer bits that can be set to address other registers within the group. The seven readable status registers have no analogous second-level registers.

The registers are designated as follows, according to their base-register groups:

WR0-WR6 - Write Register groups 0 through 6 (7 base registers plus 14 associated registers)

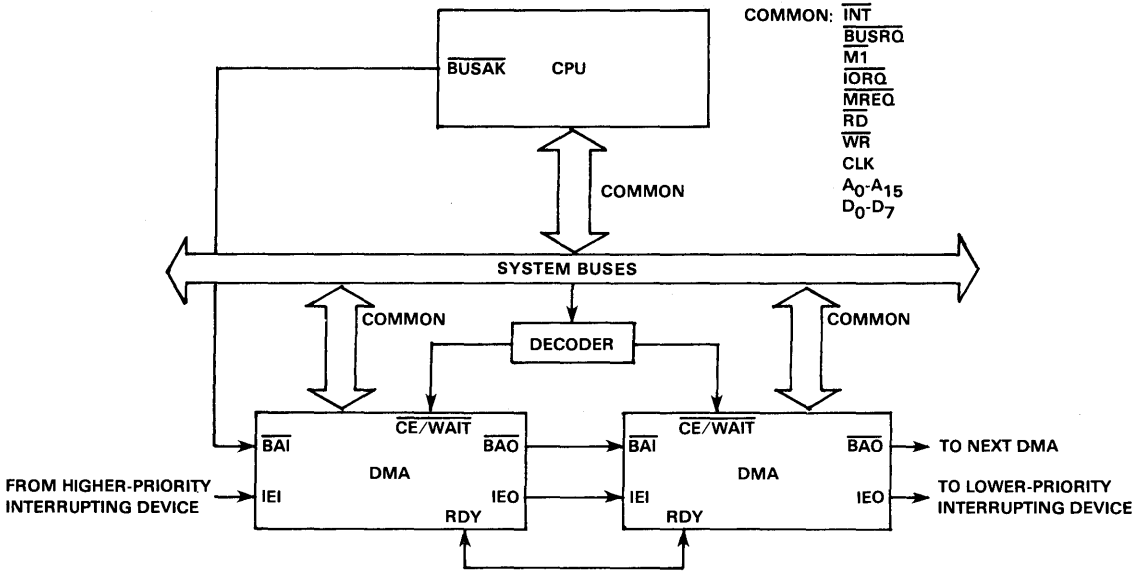
RR0-RR6 - Read Registers 0 through 6

Writing to a register within a write-register group involves first writing to the base register, with the appropriate pointer bits set, then writing to one or more of the other registers within the group. All seven of the readable status registers are accessed sequentially according to a programmable mask contained in one of the writeable registers. The section entitled "Programming" explains this in more detail.

A pipelining scheme is used for reading data in. The programmed block length is the number of bytes compared to the byte counter, which increments at the end of each cycle. In searches, data byte comparisons with the match byte are made during the read cycle of the next byte. Matches are, therefore, discovered only after the next byte is read in.

In multiple-DMA configurations, interrupt-request daisy chains are prioritized by the order in which their IEI and IEO lines are connected. The system bus, however, may not be pre-empted. Any DMA that gains access to the system buses keeps them until it is finished.

MULTIPLE-DMA INTERCONNECTION TO THE Z80 CPU
Figure 7



WRITE REGISTERS

WR0	Base register byte Port A starting address (low byte) Port A starting address (high byte) Block length (low byte) Block length (high byte)
WR1	Base register byte Port A variable-timing byte
WR2	Base register byte Port B variable-timing byte
WR3	Base register byte Mask byte Match byte
WR4	Base register byte Port B starting address (low byte) Port B starting address (high byte) Interrupt control byte Pulse control byte Interrupt vector
WR5	Base register byte
WR6	Base register byte Read mask

READ REGISTERS

RR0	Status byte
RR1	Byte counter (low byte)
RR2	Byte counter (high byte)
RR3	Port A address counter (low byte)
RR4	Port A address counter (high byte)
RR5	Port B address counter (low byte)
RR6	Port B address counter (high byte)

PROGRAMMING

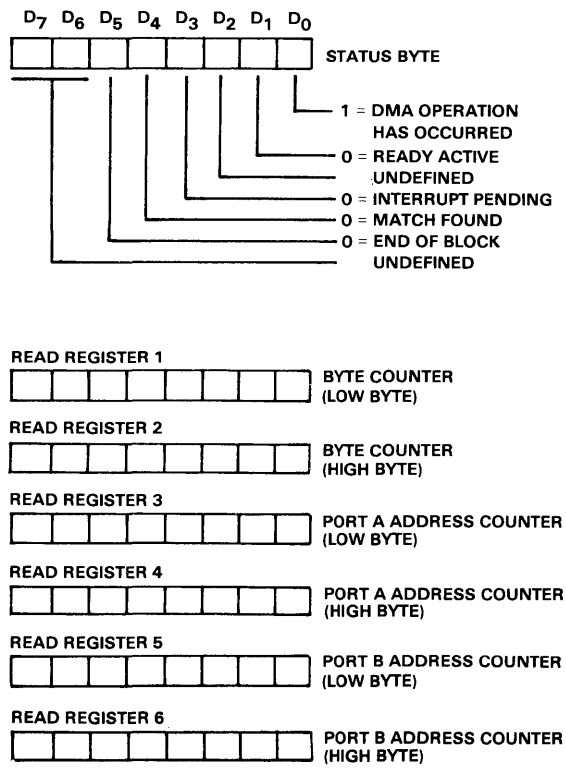
The Z80 DMA has two programmable fundamental states: (1) an enabled state, in which it can gain control of the system buses and direct the transfer of data between ports, and (2) a disabled state, in which it can initiate neither bus requests or data transfers. When the DMA is powered up or reset by any means, it is automatically placed into the disabled state. Program commands can be written to it by the CPU in either state, but this automatically puts the DMA in the disabled state, which is maintained until an enabled command is issued by the CPU. The CPU must program the DMA in advance of any data search or transfer by addressing it as an I/O port and sending a sequence of control bytes using an Output instruction (such as OTIR for the Z80 CPU).

Writing

Control or command bytes are written into one or more of the Write Register groups (WR0-WR6) by first writing to the base register byte in that group. All groups have base registers and most groups have additional associated registers. The associated registers in a group are sequentially accessed by first writing a byte to the base register containing register-group identification and pointer bits (1's) to one or more of that base register's associated registers.

READ REGISTERS

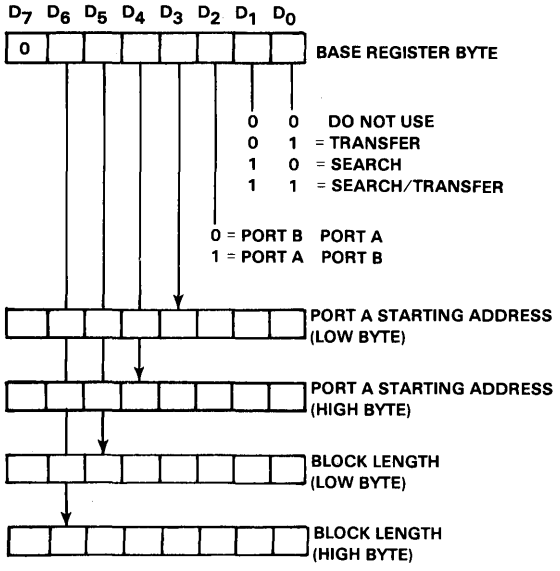
Figure 8a.



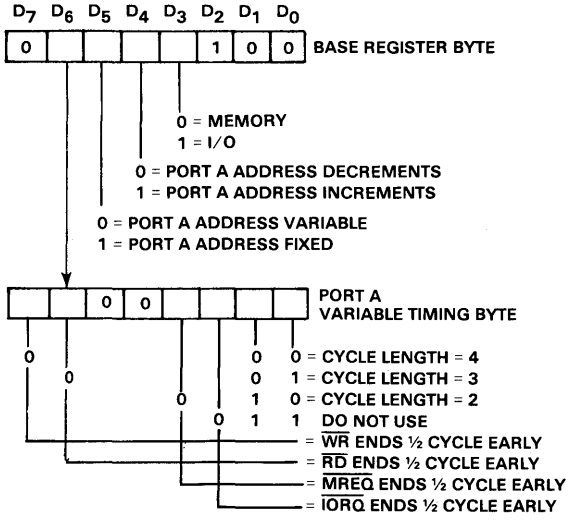
This is illustrated in Figure 8. In this figure, the sequence in which associated registers within a group can be written to is shown by the vertical position of the associated registers. For example, if a byte written to the DMA contains the bits that identify WR0 (bits D0, D1 and D7), and also contains 1's in the bit positions that point to the associated "Port A Starting Address (low byte)" and "Port A Starting Address (high byte)" then the next two bytes written to the DMA will be stored in these two registers, in that order.

WRITE REGISTERS
Figure 8b

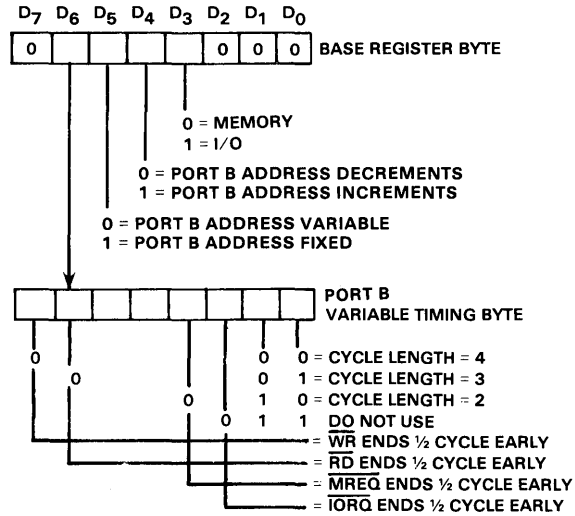
WRITE REGISTER 0



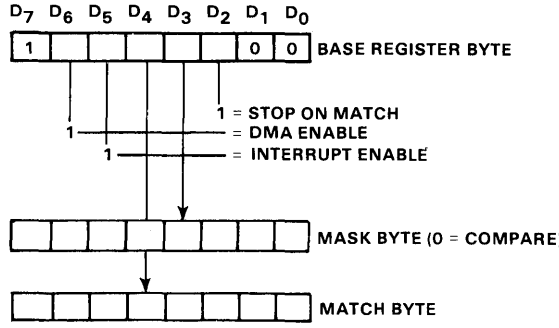
WRITE REGISTER 1



WRITE REGISTER 2



WRITE REGISTER 3



Reading

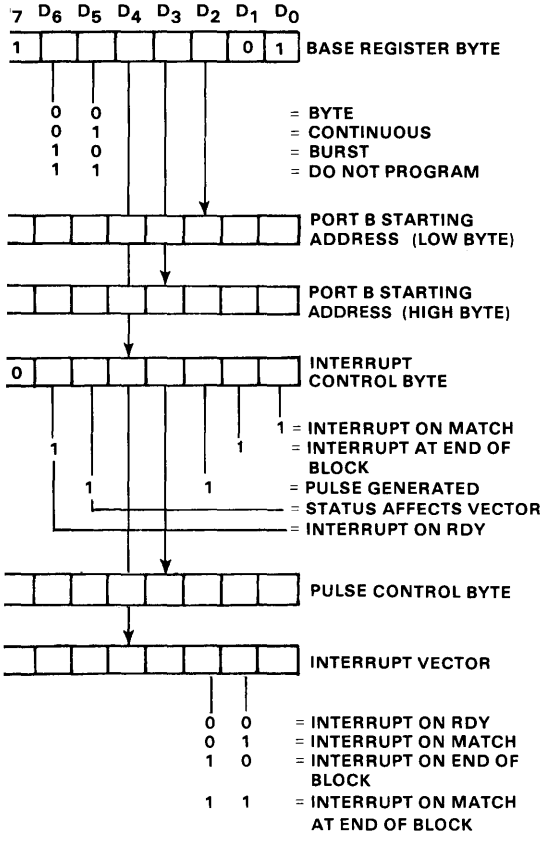
The Read Registers (RR0-RR6) are read by the CPU by addressing the DMA as an I/O port using an Input instruction (such as INIR for the Z80 CPU). The readable bytes contain DMA status, byte-counter values, and port addresses since the last DMA reset. The registers are always read in a fixed sequence beginning with RR0 and ending with RR6. However, the register read in this sequence is determined by programming the Read Mask in WR6. The sequence of reading is initialized by writing an Initiate Read Sequence or Set Read Status command to WR6. After a Reset DMA, the sequence must be initialized with the Initiate Read Sequence command or a Read Status command. The sequence of reading all registers that are not excluded by the Read Mask register must be completed before a new Initiate Read Sequence or Read Status command.

Fixed-Address Programming

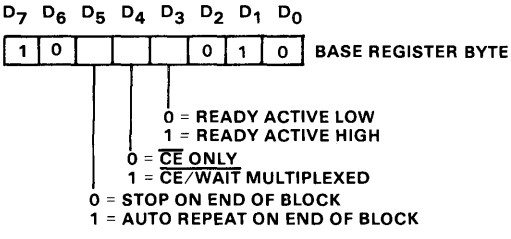
A special circumstance arises when programming a destination port to have a fixed address. The load command in WR6 only loads a fixed address to a port selected as the source, not to a port selected as the destination. Therefore, a fixed destination address must be loaded by temporarily declaring it a fixed-source

VRITE REGISTERS
igure 8b

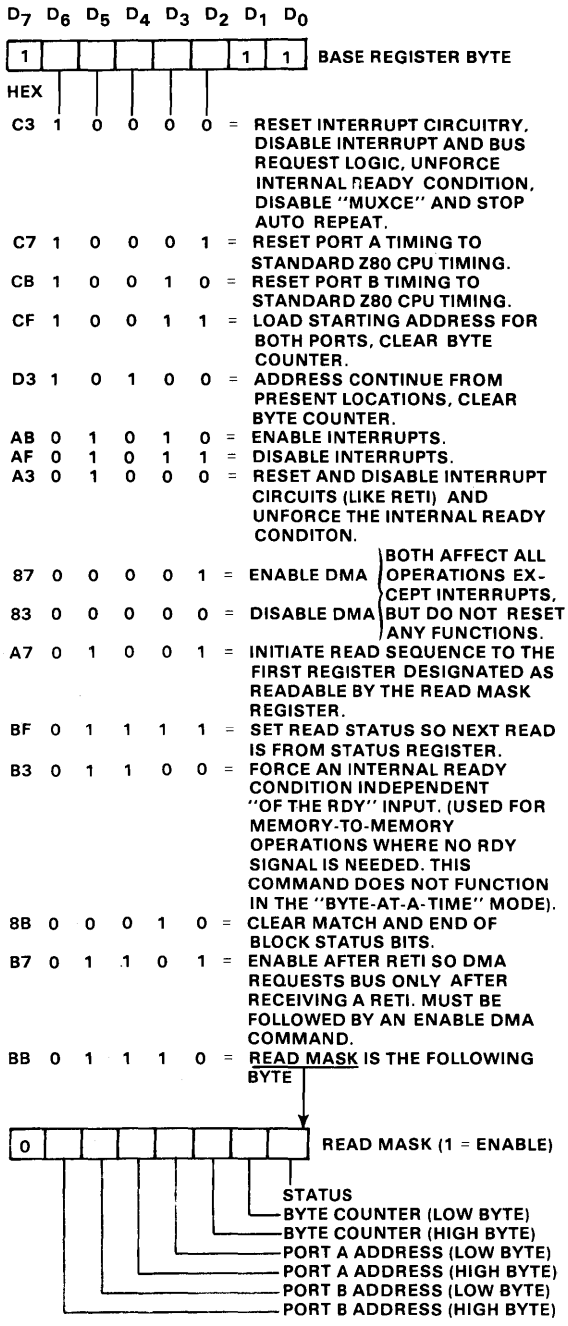
VRITE REGISTER 4



WRITE REGISTER 5



WRITE REGISTER 6



VII

SAMPLE DMA PROGRAM

Figure 9

COMMENTS	D_7	D_8	D_5	D_4	D_3	D_2	D_1	D_0	HEX
WR0 sets DMA to receive block length, Port A starting address and temporarily sets Port B as source.	0	1 Block Length Upper Follows	1 Block Length Lower Follows	1 Port A Upper Address Follows	1 Port A Lower Address Follows	0 B→A Temporary for Loading B Address	0 Transfer, No Search	1	79
Port A address (lower)	0	1	0	1	0	0	0	0	50
Port A address (upper)	0	0	0	1	0	0	0	0	10
Block length (lower)	0	0	0	0	0	0	0	0	00
Block length (upper)	0	0	0	1	0	0	0	0	10
WR1 defines Port A as peripheral with fixed address.	0	0 No Timing Follows	0 Address Changes	1 Address Increments	0 Port is Memory	1 This is Port A	0	0	14
WR2 defines Port B as peripheral with fixed address.	0	0 No Timing Follows	1 Fixed Address	0	1 Port is I/O	0 This is Port B	0	0	28
WR4 sets mode to Burst, sets DMA to expect Port B address.	1	1 Burst Mode	0	0 No Interrupt Control Byte Follows	0 No Upper Address	1 Port B Lower Address Follows	0	1	C5
Port B address (lower)	0	0	0	0	0	1	0	1	05
WR5 sets Ready active High	1	0	0 No Auto Restart	0 No Wait States	1 RDY Active High	0	1	0	8A
WR6 loads both Port addresses and resets block counter.*	1	1	0	0 Load	1	1	1	1	CF
WR0 sets Port A as source.*	0	0	0 No Address of Block Length Bytes	0	0	1 A→B	0 Transfer, No Search	1	05
WR6 reloads Port addresses and resets block counter	1	1	0	0 Load	1	1	1	1	CF
WR6 enables DMA to start operation.	1	0	0	0 Enable DMA	0	1	1	1	87

NOTE: The actual number of bytes transferred is one more than specified by the block length.
*These commands are necessary only in the case of a fixed destination address.

address and subsequently declaring the true source as such, thereby implicitly making the other a destination.

The following example illustrates the steps in this procedure, assuming that transfers are to occur from a variable-address source (Port A) to a fixed-address destination (Port B):

1. Temporarily declare Port B as source in WR0.
2. Load Port B address in WR6.
3. Declare Port A as source in WR0.
4. Load Port A address in WR6.
5. Enable DMA in WR6.

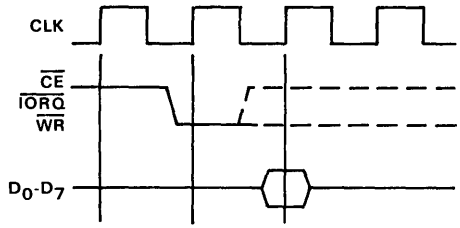
Figure 9 illustrates a program to transfer data from memory (Port A) to a peripheral device (Port B). In this example, the Port A memory starting address is 1050_H and the Port B peripheral fixed address is 05_H. Note that the data flow is 1001_H bytes—one more than specified by the block length. The table of DMA commands may be stored in consecutive memory locations and transferred to the DMA with an output instruction such as the Z80 CPU's OTIR instruction.

INACTIVE STATE TIMING (DMA as CPU Peripheral)

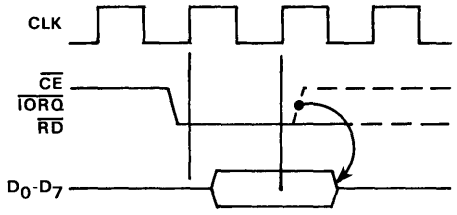
In its inactive state, the DMA is addressed by the CPU as an I/O peripheral for write and read (control and status) operations. Write timing is illustrated in Figure 10.

Reading of the DMA's status byte, byte counter or port address counters is illustrated in Figure 11. These operations require less than three T-cycles. The $\overline{CE}$, $\overline{IORQ}$ and $\overline{RD}$ lines are made active over two rising edges of CLK, and data appears on the bus approximately one T-cycle after they become active.

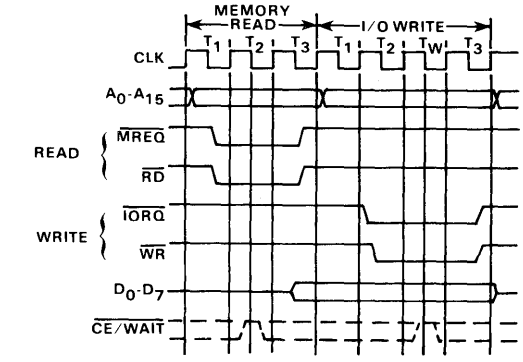
CPU-TO-DMA WRITE CYCLE
Figure 10



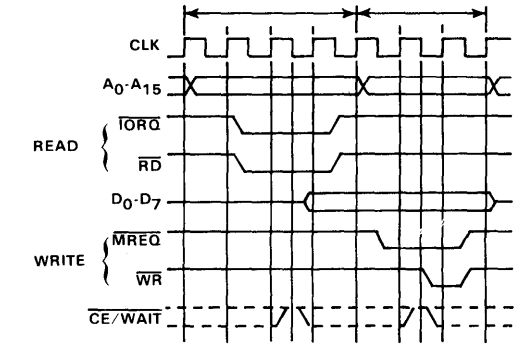
CPU-TO-DMA READ CYCLE
Figure 11



MEMORY-TO-I/O TRANSFER
Figure 12



I/O-TO-MEMORY TRANSFER
Figure 13



ACTIVE STATE TIMING (DMA as Bus Controller)

The DMA is active when it takes control of the system bus and begins transferring data.

Default Read and Write Cycles

By default, and after reset the DMA's timing of read and write operations is exactly the same as the Z80 CPU's timing of read and write cycles for memory and I/O peripherals, with one exception: during a read cycle, data is latched on the falling edge of T_3 and held on the data bus across the boundary between read and write cycles, through the end of the following write cycle.

Figure 12 illustrates the timing for memory-to-I/O port transfers and Figure 13 illustrates I/O-to-memory transfers. Memory-to-memory and I/O-to-I/O transfer timings are simply permutations of these diagrams.

The default timing uses three T-cycles for memory transactions and four T-cycles for I/O transactions, which include one automatically inserted wait cycle between T_2 and T_3. If the $\overline{CE/WAIT}$ line is programmed to act as WAIT line during the DMA's active state, it is sampled on the falling edge of T_2 for memory transactions and the falling edge of T_W for I/O transactions. If $\overline{CE/WAIT}$ is low during this time another T-cycle is added, during which the $\overline{CE/WAIT}$ line will again be sampled. The duration of transactions can thus be indefinitely extended.

Variable Cycle and Edge Timing

The Z80 DMA's default operation-cycle length for the source (read) port and destination (write) port can be independently programmed. This variable-cycle feature allows read or write cycles consisting of two, three or four T-cycles (more if Wait cycles are inserted), thereby increasing or decreasing the speed of all signals generated by the DMA. In addition, the trailing edges of the $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$ and $\overline{WR}$ signals can be independently terminated one-half cycle early. Figure 14 illustrates this.

In the variable-cycle mode, unlike default timing, $\overline{IORQ}$ comes active one-half cycle before $\overline{MREQ}$, $\overline{RD}$ and $\overline{WR}$. $\overline{CE/WAIT}$ can be used to extend only the 3 or 4 T-cycle variable cycles. It is sampled at the falling edge of T_2 for 3- or 4-cycle memory cycles, and at the falling edge of T_3 for 4-cycle I/O cycles.

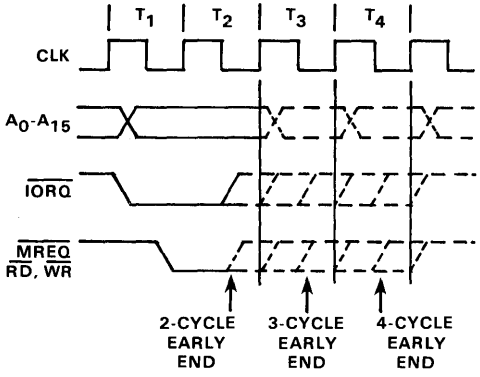
During transfers, data is latched on the clock edge causing the rising edge of $\overline{RD}$ and held until the end of the write cycle.

Bus Requests

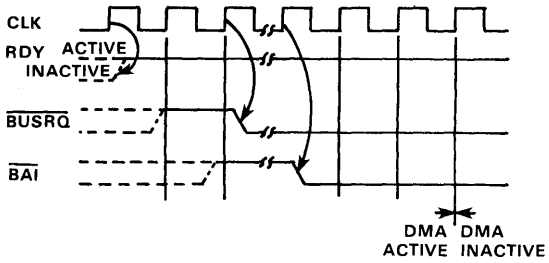
Figure 15 illustrates the bus request and acceptance timing. The RDY line, which may be programmed active

VII

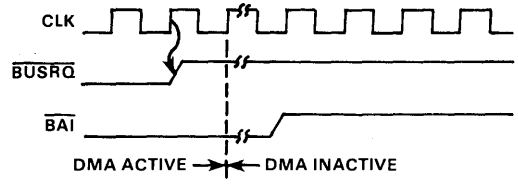
VARIABLE-CYCLE AND EDGE TIMING
Figure 14



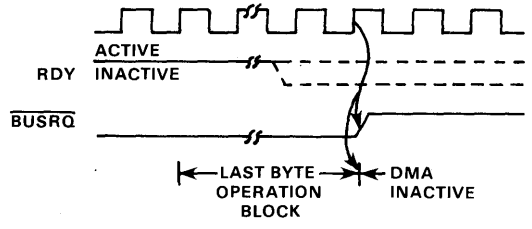
BUS REQUEST AND ACCEPTANCE
Figure 15



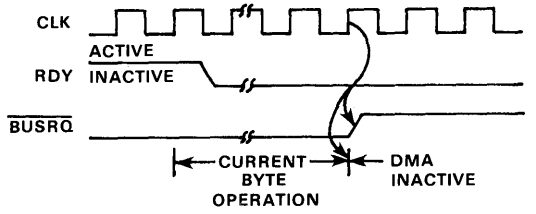
BUS RELEASE (BYTE-AT-A-TIME MODE)
Figure 16



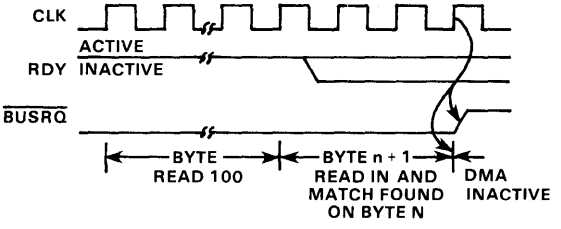
BUS RELEASE (CONTINUOUS MODE)
Figure 17



BUS RELEASE WHEN NOT READY (BURST MODE)
Figure 18



BUS RELEASE ON MATCH (BURST AND CONTINUOUS MODES)
Figure 19



High or Low, is sampled on every rising edge of CLK. If it is found to be active, and the bus is not in use by any other device, the following rising edge of CLK drives $\overline{BUSRQ}$ low. After receiving $\overline{BUSRQ}$, the CPU acknowledges on the $\overline{BAI}$ input either directly or through a multiple-DMA daisy chain. When a low is detected on $\overline{BAI}$ for two consecutive rising edges of CLK, the DMA will begin transferring data on the next rising edge of CLK.

Bus Release Byte-at-a-Time

In Byte-at-a-Time mode, $\overline{BUSRQ}$ is brought high on the rising edge of CLK prior to the end of each read cycle (search-only) or write cycle (transfer and transfer/search) as illustrated in Figure 16. This is done regardless of the state of RDY. There is no possibility of confusion when a Z80 CPU is used since the CPU cannot begin an operation until the following T-cycle. Most other CPUs are not bothered by this either, although note should be taken of it. The next bus request for the next byte will come after both $\overline{BUSRQ}$ and $\overline{BAI}$ have returned high.

Bus Release at End of Block

In Burst and Continuous modes, an end of block causes $\overline{BUSRQ}$ to go High usually on the same rising edge of CLK in which the DMA completes the transfer of the data block (Figure 17). The last byte in the block is transferred even if RDY goes inactive before completion of the last byte transfer.

Bus Release on Not Ready

In Burst Mode, when RDY goes inactive it causes $\overline{BUSRQ}$ to go High on the next rising edge of CLK after the completion of its current byte operation (Figure 18). The action on $\overline{BUSRQ}$ is thus somewhat delayed from action on the RDY line. The DMA always completes its current byte operation in an orderly fashion before releasing the bus.

By contrast, $\overline{BUSRQ}$ is not released in Continuous mode when RDY goes inactive. Instead, the DMA idles after completing the current byte operation, awaiting an active RDY again.

Bus Release on Match

If the DMA is programmed to stop on match in Burst or Continuous modes, a match causes $\overline{BUSRQ}$ to go inactive on the rising edge of CLK after the next byte following the match (Figure 19). Due to the pipelining scheme, matches are determined while the next byte is being read. Matches at End-of-Block are, therefore, actually matches to the byte immediately preceding the last byte in the block.

The RDY line can go inactive after the matching operation begins without affecting this bus-release timing.

Interrupts

Timings for interrupt acknowledge and return from interrupt are the same as timings for these in other Z80 peripherals.

Interrupt on RDY (interrupt before requesting bus) does not directly affect the $\overline{BUSRQ}$ line. Instead, the interrupt service routine must handle this by issuing the following commands to WR6:

1. Enable after Return From Interrupt (RETI) Command —Hex B7
2. Enable DMA—Hex 87
3. A RETI instruction that resets the IUS latch in the Z80 DMA

ELECTRICAL CHARACTERISTICS

VII

ABSOLUTE MAXIMUM RATINGS

Operating Ambient Temperature Under Bias ..... As Specified Under "Ordering Information"
Storage Temperature ..... -65°C to +150°C
Voltage on any pin with respect to ground ..... -0.3V to +7V
Power Dissipation 1.5W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

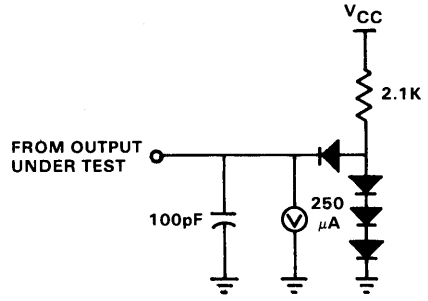
STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

- $+4.75 \leq V_{CC} \leq +5.25V$
- GND = 0V
- $0°C \leq T_A \leq +70°C$

All AC parameters assume a load capacitance of 100pF max. Timing references between two output signals assume a load difference of 50pF max.

Figure 20



DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC}-.6	5.5	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	

DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input High Voltage	2.0	5.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}=3.2mA for $\overline{BUSRQ}$ I_{OL}=2.0mA for all others
V_{OH}	Output High Voltage	2.4		V	I_{OH}=250μA
I_{CC}	Power Supply Current MK3883 MK3883-4		 150 200	 mA mA	
I_{LI}	Input Leakage Current		$\pm$ 10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode		$\pm$ 10	μA	$0 \leq V_{IN} \leq V_{CC}$

V_{CC} = 5V $\pm$ 5% unless otherwise specified, over specified temperature range.

CAPACITANCE

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
C	Clock Capacitance		35	pF	Unmeasured Pins
C_{IN}	Input Capacitance		10	pF	Returned to Ground
C_{OUT}	Output Capacitance		10	pF	

f = 1MHz, over specified temperature range

INACTIVE STATE AC CHARACTERISTICS

(See Figure 21)

NO	SYM	PARAMETER	MK3883		MK3883-4		UNIT
			MIN	MAX	MIN	MAX	
1	TcC	Clock Cycle Time	400	4000	250	4000	ns
2	TwCh	Clock Width (High)	170	2000	105	2000	ns
3	TwCl	Clock Width (Low)	170	2000	105	2000	ns
4	TrC	Clock Rise Time		30		30	ns
5	TfC	Clock Fall Time		30		30	ns
6	Th	Hold Time for Any Specified Setup Time	0		0		ns
7	TsC(Cr)	$\overline{IORQ}$, $\overline{WR}$, $\overline{CE}$ $\downarrow$ to Clock $\uparrow$ Setup	280		145		ns
8	TdDO(RDf)	$\overline{RD}$ to Data Output Delay		500		380	ns
9	TsWM(Cr)	Data In to Clock $\uparrow$ Setup ($\overline{WR}$ or $\overline{M1}$)	50		50		ns
10	TdCf(DO)	$\overline{IORQ}\downarrow$ to Data Out Delay (INTA Cycle)		340		160	ns

INACTIVE STATE AC CHARACTERISTICS (Continued)

NO	SYM	PARAMETER	MK3883		MK3883-4		UNIT
			MIN	MAX	MIN	MAX	
11	TdRD(Dz)	$\overline{RD}\uparrow$ to Data Float Delay (output buffer disable)		160		110	ns
12	TslEI(IORQ)	IEI ↓ to $\overline{IORQ}$ ↓ Setup (INTA Cycle)	140		140		ns
13	TdIEOr(IEIr)	IEI ↑ to IEO ↑ Delay		210		160	ns
14	TdIEOf(IEIf)	IEI ↓ to IEO ↓ Delay		190		130	ns
15	TdM1(IEO)	$\overline{M1}\downarrow$ to IEO↓ Delay (interrupt just prior to $\overline{M1}\downarrow$)		300		190	ns
16	TsM1f(Cr)	$\overline{M1}\downarrow$ to Clock ↑ Setup	210		90		ns
17	TsM1r(Cf)	$\overline{M1}\uparrow$ to Clock ↓ Setup	20		0		ns
18	TsRD(C)	$\overline{RD}\downarrow$ to Clock ↑ Setup ($\overline{M1}$ Cycle)	240		115		ns
19	TdI(INT)	Interrupt Cause to $\overline{INT}\downarrow$ Delay ($\overline{INT}$ generated only when DMA is inactive)		500		500	ns
20	TdBAIr (BAOr)	$\overline{BAI}\uparrow$ to $\overline{BAO}\uparrow$ Delay		200		150	ns
21	TdBAIf (BAOf)	$\overline{BAI}\downarrow$ to $\overline{BAO}\downarrow$ Delay		200		150	ns
22	TsRDY(Cr)	RDY Active to Clock ↑ Setup	150		100		ns

ACTIVE STATE AC CHARACTERISTICS
(See Figure 22)

NO	SYM	PARAMETER	MK3883		MK3883-4	
			MIN(ns)	MAX(ns)	MIN(ns)	MAX(ns)
1	TcC	Clock Cycle Time	400		250	
2	TwCh	Clock Width (High)	180	2000	110	2000
3	TwCl	Clock Width (Low)	180	2000	110	2000
4	TrC	Clock Rise Time		30		30
5	TfC	Clock Fall Time		30		30
6	TdA	Address Output Delay		145		110
7	TdC(Az)	Clock ↑ to Address Float Delay		110		90
8	TsA(MREQ)	Address to $\overline{MREQ}\downarrow$ Setup (Memory Cycle)	(2)+(5)-75		(2)+(5)-75	
9	TsA(IRW)	Address Stable to $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}\downarrow$ Setup (I/O Cycle)	(1)-80		(1)-70	
*10	TdRW(A)	$\overline{RD}$, $\overline{WR}\uparrow$ to Addr. Stable Delay	(3)+(4)-40		(3)+(4)-50	
*11	TdRW(Az)	$\overline{RD}$, $\overline{WR}\uparrow$ to Addr. Float	(3)+(4)-60		(3)+(4)-45	
12	TdCf(DO)	Clock ↓ to Data Out Delay		230		150

VII

ACTIVE STATE AC CHARACTERISTICS

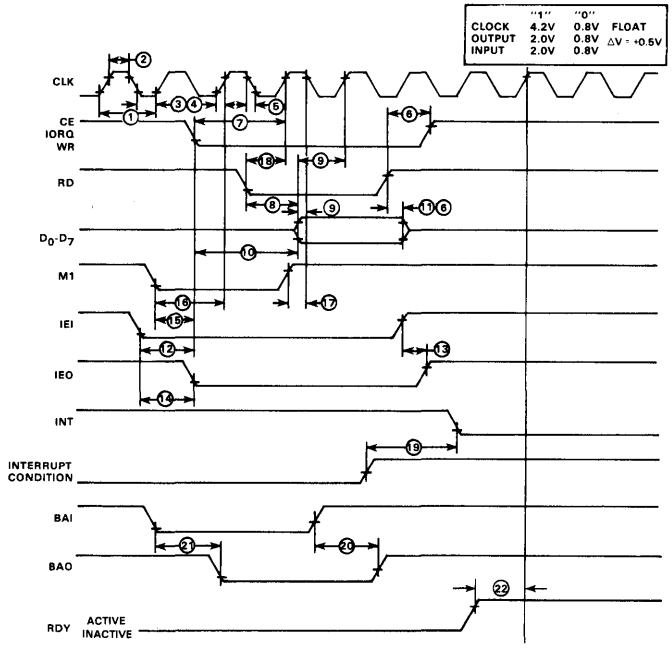
NO	SYM	PARAMETER	MK3883		MK3883-4	
			MIN(ns)	MAX(ns)	MIN(ns)	MAX(ns)
*13	TdCr(Dz)	Clock↑ to Data Float Delay (Write Cycle)		90		90
14	TsDI(Cr)	Data In to Clock↑ Setup (Read cycle when rising edge ends read)	50		35	
15	TsDI(Cf)	Data In to Clock↓ Setup (Read cycle when falling edge ends read)	60		50	
*16	TsDO(WfM)	Data Out to $\overline{WR}$↓ Setup (Memory Cycle)	(1)-210		(1)-170	
17	TsDO(WfI)	Data Out to $\overline{WR}$↓ Setup (I/O cycle)	100		100	
*18	TdWr(DO)	$\overline{WR}$↑ to Data Out Delay	(3)+(4)-80		(3)+(4)-70	
19	Th	Hold Time for Any Specified Setup Time	0		0	
*20	TdCr(Mf)	Clock↑ to $\overline{MREQ}$↓ Delay		100		85
21	TdCf(Mf)	Clock↓ to $\overline{MREQ}$↓ Delay		100		85
22	TdCr(Mr)	Clock↑ to $\overline{MREQ}$↑ Delay		100		85
23	TdCf(Mr)	Clock↓ to $\overline{MREQ}$↑ Delay		100		85
24	TwM1	$\overline{MREQ}$ Low Pulse Width	(1)-40		(1)-30	
*25	TwMh	$\overline{MREQ}$ High Pulse Width	(2)+(5)-30		(2)+(5)-20	
26	TdCr(If)	Clock↑ to $\overline{IORQ}$↓ Delay		90		75
27	TdCf(If)	Clock↓ to $\overline{IORQ}$↓ Delay		110		85
28	TdCr(Ir)	Clock↑ to $\overline{IORQ}$↑ Delay		100		85
*29	TdCf(Ir)	Clock↓ to $\overline{IORQ}$↑ Delay		110		85
30	TdCr(Rf)	Clock↑ to $\overline{RD}$↓ Delay		100		85
31	TdCf(Rf)	Clock↓ to $\overline{RD}$↓ Delay		130		95
32	TdCr(Rr)	Clock↑ to $\overline{RD}$↑ Delay		100		85
33	TdCf(Rr)	Clock↓ to $\overline{RD}$↑ Delay		110		85
34	TdCr(Wf)	Clock↑ to $\overline{WR}$↓ Delay		80		65
35	TdCf(Wf)	Clock↓ to $\overline{WR}$↓ Delay		90		80
*36	TdCr(Wr)	Clock↑ to $\overline{WR}$↑ Delay		100		80
37	TdCf(Wr)	Clock↓ to $\overline{WR}$↑ Delay		100		80
38	TwWI	$\overline{WR}$ Low Pulse Width	(1)-40		(1)-30	
39	TsWA(Cf)	$\overline{WAIT}$ to Clock↓ Setup	70		70	
40	TdCr(B)	Clock↑ to $\overline{BUSRQ}$ Delay		100		100
41	TdCr(Iz)	Clock↑ to $\overline{IORQ}$, $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ Float Delay		100		80

NOTES:

1. Numbers in parentheses are other parameter-numbers in this table; their values should be substituted in equations.
2. All equations imply DMA default (standard) timing.
3. Data must be enabled onto data bus when RD is active.
4. Asterisk(*) before parameter number means the parameter is not illustrated in the AC Timing Diagrams.

INACTIVE STATE CHARACTERISTICS

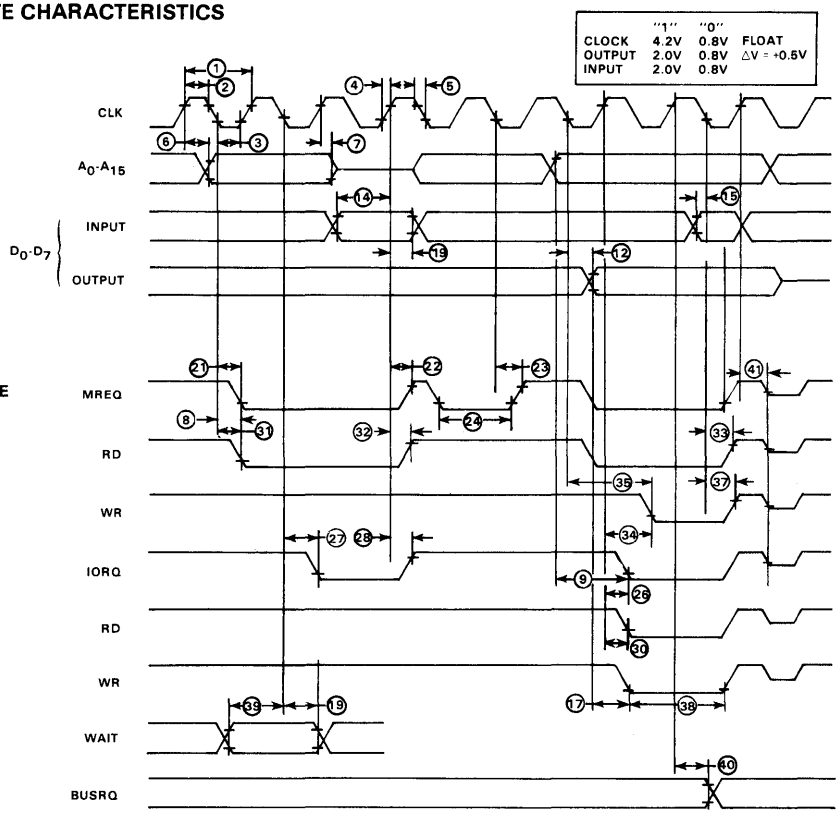
Figure 21



VII

ACTIVE STATE CHARACTERISTICS

Figure 22



ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3883N MK3883P	Z80-DMA Plastic Z80-DMA Ceramic	2.5 MHz 2.5 MHz	0°C to +70°C 0°C to +70°C
MK3883N-10 MK3883P-10	Z80-DMA Plastic Z80-DMA Ceramic	2.5 MHz 2.5 MHz	-40°C to +85°C -40°C to +85°C
MK3883N-4 MK3883P-4	Z80A-DMA Plastic Z80A-DMA Ceramic	4 MHz 4 MHz	0°C to +70°C 0°C to +70°C

SERIAL INPUT/OUTPUT CONTROLLER MK3884/5/7/SIO

FEATURES

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5MHz clock (MK3884 Z80 SIO), or 0 to 800K bits/second with a 4.0MHz clock (MK3884-4 Z80 SIO).
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/-checking, sync character and zero insertion/-deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

DESCRIPTION

The MK3884 Z80 SIO Serial Input/Output Controller is a dual-channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications.

The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on two fully-independent channels, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

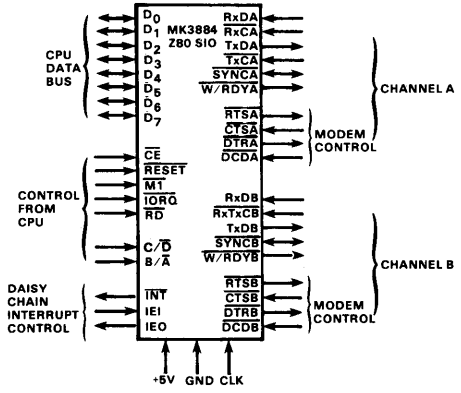
VII

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

The Z80 SIO is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a single +5V power supply and the standard Z80 family single-phase clock.

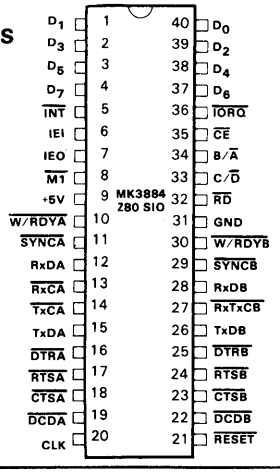
MK3884 Z80 SIO PIN FUNCTIONS

Figure 1



MK3884 Z80 SIO PIN ASSIGNMENTS

Figure 2



PIN DESCRIPTIONS

Figures 1 through 6 illustrate the three pin configurations (bonding options) available in the SIO. The constraints of a 40-pin package make it impossible to bring out the Receive Clock ($\overline{RxC}$), Transmit Clock ($\overline{TxC}$), Data Terminal Ready ($\overline{DTR}$) and Sync ($\overline{SYNC}$) signals for both channels. Therefore, either Channel B lacks a signal or two signals are bonded together in the three bonding options offered:

- MK3887 Z80 SIO lacks $\overline{SYNCB}$
- MK3885 Z80 SIO lacks $\overline{DTRB}$
- MK3884 Z80 SIO has all four signals, but $\overline{TxCB}$ and $\overline{RxCB}$ are bonded together

The pin descriptions are as follows:

B/$\overline{A}$. Channel A Or B Select (input, High selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A_0 from the CPU is often used for the selection function.

C/$\overline{D}$. Control Or Data Select (input, High selects Control). This input defines the type of information transfer performed between the CPU and the SIO. A High at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B/$\overline{A}$. A Low at C/$\overline{D}$ means that the information on the data bus is data. Address bit A_1 is often used for this function.

$\overline{CE}$. Chip Enable (Input, active Low). A Low level at this input enables the SIO to accept command or data input from the CPU during a write cycle, or to transmit data to the CPU during a read cycle.

CLK. System Clock (input). The SIO uses the standard Z80 System Clock to synchronize internal signals. This is a single-phase clock.

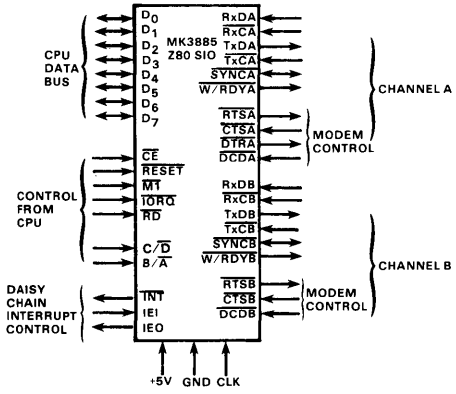
$\overline{CTSA}$, $\overline{CTSB}$. Clear To Send (inputs, active Low). When programmed as Auto Enables, a Low on these inputs enables the respective transmitter. If not programmed as Auto Enables, these inputs may be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.

D_0-D_7. System Data Bus (bidirectional, 3-state). The system data bus transfers data and commands between the CPU and the Z80 SIO. D_0 is the least significant bit.

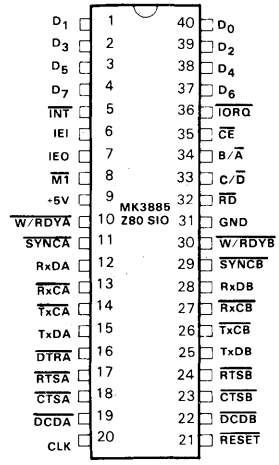
$\overline{DCDA}$, $\overline{DCDB}$. Data Carrier Detect (inputs, active Low). These pins function as receiver enables if the SIO is programmed for Auto Enables; otherwise they may be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.

$\overline{DTRA}$, $\overline{DTRB}$. Data Terminal Ready (outputs, active Low). These outputs follow the state programmed into Z80 SIO. They can also be programmed as general-purpose outputs.
In the MK3885 bonding option, $\overline{DTRB}$ is omitted.

MK3885 Z80 SIO PIN FUNCTIONS
Figure 3



MK3885 Z80 SIO PIN ASSIGNMENTS
Figure 4



IEI. Interrupt Enable In (input, active High). This signal is used with IEO to form a priority daisy chain when there is more than one interrupt-driven device. A High on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.

$\overline{INT}$. Interrupt Request (output, open drain, active Low). When the SIO is requesting an interrupt, it pulls $\overline{INT}$ Low.

$\overline{IORQ}$. Input/Output Request (input from CPU, active Low). $\overline{IORQ}$ is used in conjunction with B/$\overline{A}$, C/$\overline{D}$, $\overline{CE}$ and $\overline{RD}$ to transfer commands and data between the CPU and the SIO. When $\overline{CE}$, $\overline{RD}$ and $\overline{IORQ}$ are all active, the channel selected by B/$\overline{A}$ transfers data to the CPU (a read operation). When $\overline{CE}$ and $\overline{IORQ}$ are active, but $\overline{RD}$ is inactive, the channel selected by B/$\overline{A}$ is written to by the CPU with either data or control information as specified by C/$\overline{D}$. As mentioned previously, if $\overline{IORQ}$ and $\overline{M1}$ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

$\overline{M1}$. Machine Cycle (input from Z80 CPU, active Low). When $\overline{M1}$ is active and $\overline{RD}$ is also active, the Z80 CPU is fetching an instruction from memory; when $\overline{M1}$ is active while $\overline{IORQ}$ is active, the SIO accepts $\overline{M1}$ and $\overline{IORQ}$ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z80 CPU.

$\overline{RxCA}$, $\overline{RxCB}$. Receiver Clocks (inputs). Receive data is sampled on the rising edge of $\overline{RxC}$. The Receive Clocks may be 1, 16, 32 or 64 times the data rate in asynchronous modes. These clocks may be driven by the Z80 CTC Counter Timer Circuit for programmable baud rate generation. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).

In the MK3884 bonding option, $\overline{RxCB}$ is bonded together with $\overline{TxCB}$.

$\overline{RD}$. Read Cycle Status (input from CPU, active Low). If $\overline{RD}$ is active, a memory or I/O read operation is in progress. $\overline{RD}$ is used with B/$\overline{A}$, $\overline{CE}$ and $\overline{IORQ}$ to transfer data from the SIO to the CPU.

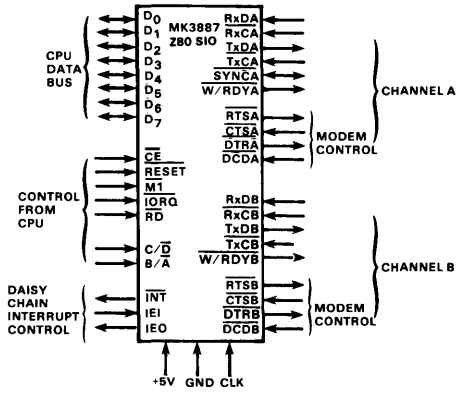
RxDA, RxDB. Receive Data (inputs, active High). Serial data at TTL levels.

$\overline{RESET}$. Reset (input, active Low). A Low $\overline{RESET}$ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls High and disables all interrupts. The control registers must be rewritten after the SIO is reset and before data is transmitted or received.

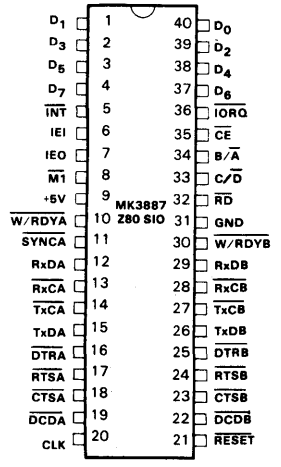
$\overline{RTSA}$, $\overline{RTSB}$. Request To Send (outputs, active Low). When the RTS bit in Write Register 5 (Figure 14) is set, the $\overline{RTS}$ output goes Low. When the $\overline{RTS}$ bit is reset in the Asynchronous mode, the output goes High after the transmitter is empty. In Synchronous modes, the $\overline{RTS}$ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

VII

MK3887 Z80 SIO PIN FUNCTIONS
Figure 5



MK3887 Z80 SIO PIN ASSIGNMENTS
Figure 6



SYNCA, SYNCB. Synchronization (inputs/outputs, active Low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to CTS and DCD. In this mode, the transitions on these lines affect the state of the Sync/-Hunt status bit in Read Register 0 (Figure 13), but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, SYNC must be driven Low on the second rising edge of RxC after that rising edge of RxC on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the SYNC input. Once SYNC is forced Low, it should be kept Low until the CPU informs the external synchronization detect logic that synchronization has been lost or a new message is about to start. Character assembly begins on the rising edge of RxC that immediately precedes the falling edge of SYNC in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock (RxC) cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the MK3887 bonding option, SYNCB is omitted.

TxCA, TxCB. Transmitter Clocks (inputs). TxD changes from the falling edge of TxC. In asynchronous modes, the Transmitter Clocks may be 1, 16, 32 or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified). Transmitter Clocks may be driven by the Z80 CTC Counter Timer Circuit for programmable baud rate generation.
In the MK3884 bonding option, TxCB is bonded together with RxCB.

TxDA, TxDB. Transmit Data (outputs, active High). Serial data at TTL levels.

W/RDYA, W/RDYB. Wait/Ready A, Wait/Ready B (outputs, open drain, when programmed for Wait function; driven High and Low when programmed for Ready function). These dual-purpose outputs may be programmed as Ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

FUNCTIONAL CAPABILITIES

The functional capabilities of the Z80 SIO can be described from two different points of view: as a data communications device, it transmits and receives serial data in a wide variety of data-communication protocols; as a Z80 family peripheral, it interacts with the Z80 CPU and other peripheral circuits, sharing the data, address and control buses, as well as being a part of the Z80 interrupt structure. As a peripheral to other microprocessors, the SIO offers valuable features such as non-vectored interrupts, polling and simple handshake capability.

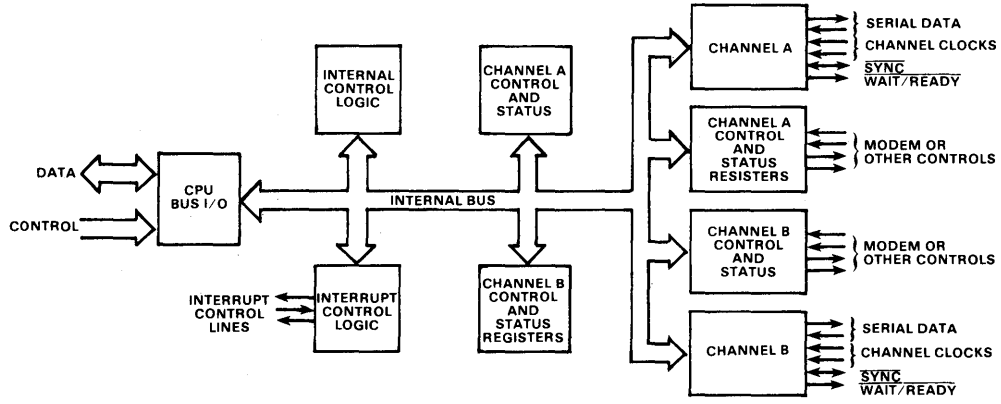
Figure 8 illustrates the conventional devices that the SIO replaces.

The first part of the following discussion covers SIO data-communication capabilities; the second part describes interactions between the CPU and the SIO.

DATA COMMUNICATION CAPABILITIES

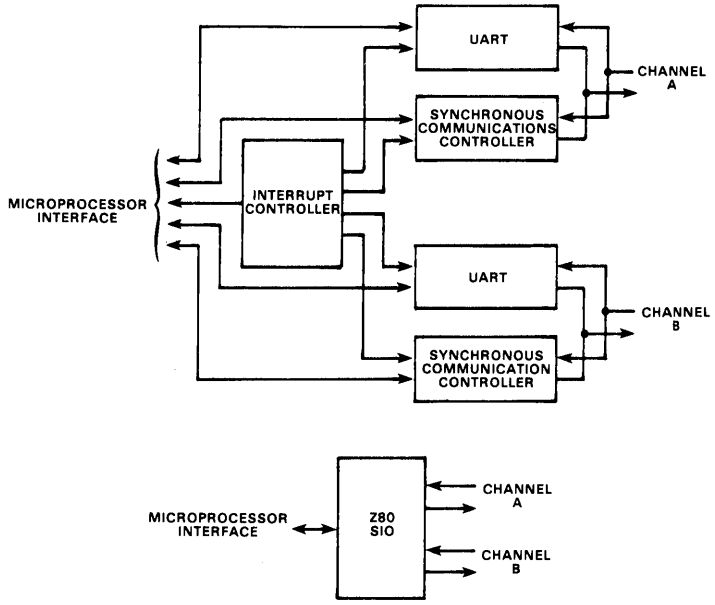
The SIO provides two independent full-duplex channels that can be programmed for use in any common asynchronous or synchronous data-communication

BLOCK DIAGRAM
Figure 7



CONVENTIONAL DEVICES REPLACED BY THE Z80 SIO

Figure 8



protocol. Figure 9 illustrates some of these protocols. The following is a short description of them. A more detailed explanation of these modes can be found in the MK3884 Z80 SIO Technical Manual.

Asynchronous Modes. Transmission and reception can be done independently on each channel with five to eight bits per character, plus optional even or odd parity. The transmitters can supply one, one-and-a-half or two stop bits per character and can provide a break output at any time. The receiver break-detection logic interrupts the CPU both at the start and end of a received break. Reception is protected from spikes by a transient spike-rejection mechanism that checks the signal one-half a bit time after a Low level is detected on the receive data input (RxDA or RxDB in Figure 5). If the Low does not persist—as in the case of a transient—the character assembly process is not started.

Framing errors and overrun errors are detected and buffered together with the partial character on which they occurred. Vectored interrupts allow fast servicing of error conditions using dedicated routines. Furthermore, a built-in checking process avoids interpreting a framing error as a new start bit: a framing error results in the addition of one-half a bit time to the point at which the search for the next start bit is begun.

The SIO does not require symmetric transmit and receive clock signals—a feature that allows it to be used with MK3882 Z80 CTC or many other clock sources. The transmitter and receiver can handle data at a rate of 1, 1/16, 1/32 or 1/64 of the clock rate supplied to the receive and transmit clock inputs. In asynchronous modes, the SYNC pin may be programmed as an input that can be used for functions such as monitoring a ring indicator.

Synchronous Modes. The SIO supports both byte-oriented and bit-oriented synchronous communication. Synchronous byte-oriented protocols can be handled in several modes that allow character synchronization with an 8-bit sync character (Monosync), any 16-bit sync pattern (Bisync) or with an external sync signal. Leading sync characters can be removed without interrupting the CPU.

Five-, six- or seven-bit sync characters are detected with 8- or 16-bit patterns in the SIO by overlapping the larger pattern across multiple in-coming sync characters, as shown in Figure 10.

CRC checking for synchronous byte-oriented modes is delayed by one character time so the CPU may disable CRC checking on specific characters. This permits implementation of protocols such as IBM Bisync.
Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. In all non-SDLC modes, the CRC generator is initialized to 0's; in SDLC modes, it is initialized to 1's. The SIO can be used for interfacing to peripherals such as hard-sectored floppy disk, but it cannot generate or check CRC for IBM-compatible soft-sectored disks. The SIO also provides a feature that automatically transmits CRC data when no other data is available for transmission. This allows very high-speed transmissions under

DMA control with no need for CPU intervention at the end of a message. When there is no data or CRC to send in synchronous modes, the transmitter inserts 8- or 16-bit sync characters regardless of the programmed character length.

The SIO supports synchronous bit-oriented protocols such as SDLC and HDLC by performing automatic flag sending, zero insertion and CRC generation. A special command can be used to abort a frame in transmission. At the end of a message the SIO automatically transmits the CRC and trailing flag when the transmit buffer becomes empty. If a transmit underrun occurs in the middle of a message, an external/status interrupt warns the CPU of this status change so that an abort may be issued. One to eight bits per character can be sent, which allows reception of a message with no prior information about the character structure in the information field of a frame.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC, and provides a synchronization signal on the SYNC pin; an interrupt can also be programmed. The receiver can be programmed to search for frames addressed by a single byte to only a specified user-selected address or to a global broadcast address. In this mode, frames that do not match either the user-selected or broadcast address are ignored. The number of address bytes can be extended under software control. For transmitting data, an interrupt on the first received character or on every character can be selected. The receiver automatically deletes all zeroes inserted by the transmitter during character assembly. It also calculates and automatically checks the CRC to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers.

The SIO can be conveniently used under DMA control to provide high-speed reception or transmission. In reception, for example, the SIO can interrupt the CPU when the first character of a message is received. The CPU then enables the DMA to transfer the message to memory. The SIO then issues an end-of-frame interrupt and the CPU can check the status of the received message. Thus, the CPU is freed for other service while the message is being received.

I/O INTERFACE CAPABILITIES

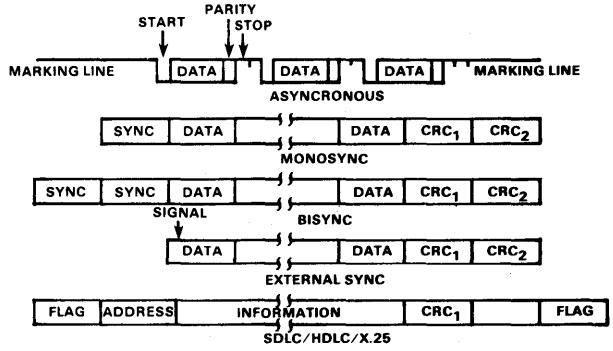
The SIO offers the choice of polling, interrupt (vectored or non-vectored) and block-transfer modes to transfer data, status and control information to and from the CPU. The block-transfer mode can also be implemented under DMA control.

Polling. Two status registers are updated at appropriate times for each function being performed (for example, CRC error-status valid at the end of a message). When the CPU is operated in a polling fashion, one of the SIO's two status registers is used to indicate whether the SIO has some data or needs some data. Depending on the contents of this register, the CPU will either write data, read data, or just go on. Two bits in the register indicate that a data transfer is needed. In addition, error and other conditions are indicated. The second status register (special receive conditions) does not have to be read in a polling sequence, until a character has been received. All interrupt modes are disabled when operating the device in a polled environment.

Interrupts. The SIO has an elaborate interrupt scheme to provide fast interrupt service in real-time applications. A control register and a status register in Channel B contain the interrupt vector. When programmed to do

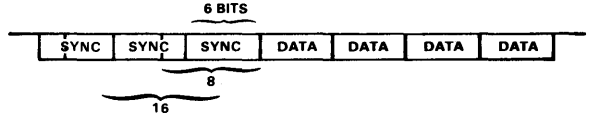
Z80 SIO PROTOCOLS

Figure 9



VARIABLE LENGTH SYNC CHARACTERS

Figure 10



so, the SIO can modify three bits of the interrupt vector in the status register so that it points directly to one of eight interrupt service routines in memory, thereby servicing conditions in both channels and eliminating most of the needs for a status-analysis routine.

Transmit interrupts, receive interrupts and external/-status interrupts are the main sources of interrupts. Each interrupt source is enabled under program control, with Channel A having a higher priority than Channel B, and with receive, transmit and external/status interrupts prioritized in that order within each channel. When the transmit interrupt is enabled, the CPU is interrupted by the transmit buffer becoming empty. (This implies that the transmitter must have had a data character written into it so it can become empty.) The receiver can interrupt the CPU in one of two ways:

- Interrupt on first received character
- Interrupt on all received characters

Interrupt-on-first-received-character is typically used with the block-transfer mode. Interrupt-on-all-received-characters has the option of modifying the interrupt vector in the event of a parity error. Both of these interrupt modes will also interrupt under special receive conditions on a character or message basis (end-of-frame interrupt in SDLC, for example). This means that the special-receive condition can cause an interrupt only if the interrupt-on-first-received--character or interrupt-on-all-received-characters mode is selected. In interrupt-on-first-received-character, an interrupt can occur from special-receive conditions (except parity error) after the first-received-character interrupt (example: receive-overrun interrupt).

The main function of the external/status interrupt is to monitor the signal transitions of the Clear To Send ($\overline{CTS}$), Data Carrier Detect ($\overline{DCD}$) and Synchronization ($\overline{SYNC}$) pins (Figures 1 through 6). In addition, an external/status interrupt is also caused by a CRC-sending condition or by the detection of a break sequence (asynchronous mode) or abort sequence (SDLC mode) in the data stream. The interrupt caused by the break/abort sequence allows the SIO to interrupt when the break/abort sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the break/-abort condition in external logic.

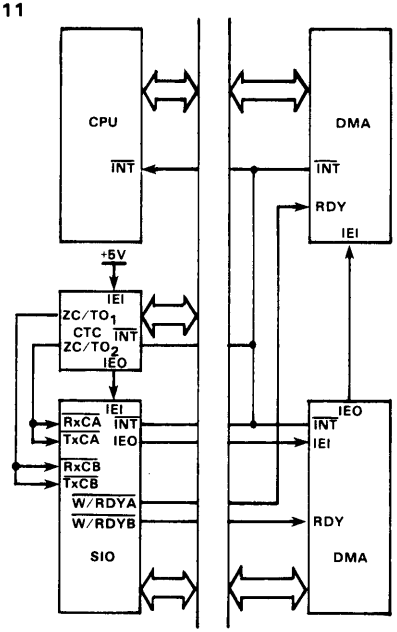
In a Z80 CPU environment (Figure 11), SIO interrupt vectoring is "automatic": the SIO passes its internally-modifiable 8-bit interrupt vector to the CPU, which adds an additional 8 bits from its interrupt-vector (I) register to form the memory address of the interrupt-routine table. This table contains the address of the beginning of the interrupt routine itself. The process entails an indirect transfer of CPU control to the interrupt routine, so that the next instruction executed after an interrupt acknowledge by the CPU is the first instruction of the interrupt routine itself.

CPU/DMA Block Transfer. The SIO's block-transfer mode accommodates both CPU block transfers and DMA controllers (Z80 DMA or other designs). The block-transfer mode uses the Wait/Ready output signal, which is selected with three bits in an internal control register. The Wait/Ready output signal can be programmed $\overline{WAIT}$ line in the CPU block-transfer mode or as a READY line in the DMA block-transfer mode.

To a DMA controller, the SIO $\overline{READY}$ output indicates that the SIO is ready to transfer data to or from memory. To the CPU, the $\overline{WAIT}$ output indicates that the SIO is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

TYPICAL Z80 ENVIRONMENT

Figure 11



ARCHITECTURE

DESCRIPTION

The internal structure of the device includes a Z80 CPU interface, internal control and interrupt logic, and two full-duplex channels. Each channel contains its own set of control and status (write and read) registers, and control and status logic that provides the interface to modems or other external devices.

The registers for each channel are designated as follows:

WR0-WR7 — Write Registers 0 through 7
RR0-RR2 — Read Registers 0 through 2

The register group includes five 8-bit control registers,

two sync-character registers and two status registers. The interrupt vector is written into an additional 8-bit register (Write Register 2) in Channel B that may be read through another 8-bit register (Read Register 2) in Channel B. The bit assignment and functional grouping of each register is configured to simplify and organize the programming process. Table 1 lists the functions assigned to each read or write register.

Read Register Functions	
RR0	Transmit/Receive buffer status, interrupt status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only)

Write Register Functions	
WR0	Register pointers, CRC initialize, initialization commands for the various modes, etc.
WR1	Transmit/Receive interrupt and data transfer mode definition.
WR2	Interrupt vector (Channel B only)
WR3	Receive parameters and control
WR4	Transmit/Receive miscellaneous parameters and modes
WR5	Transmit parameters and controls
WR6	Sync character or SDLC address field
WR7	Sync character or SDLC flag

The logic for both channels provides formats, synchronization and validation for data transferred to and from the channel interface. The modem control inputs, Clear To Send ($\overline{CTS}$) and Data Carrier Detect ($\overline{DCD}$), are monitored by the external control and status logic under program control. All external control-and-status-logic signals are general-purpose in nature and can be used for functions other than modem control.

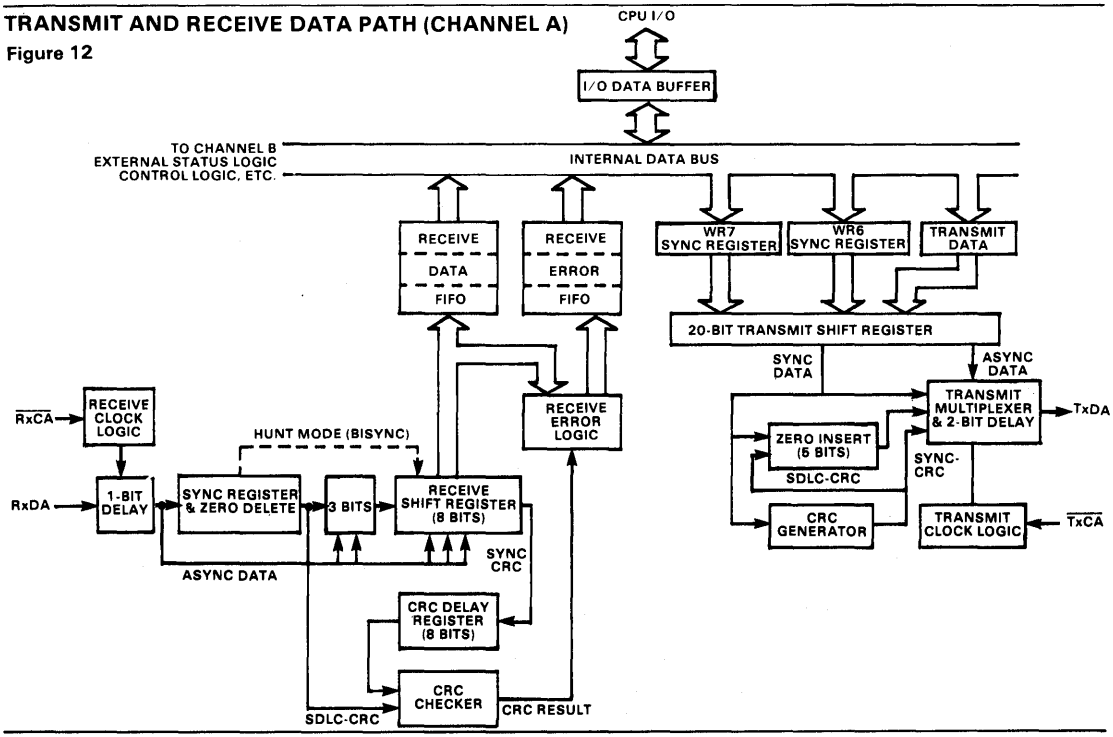
Data Path. The transmit and receive data path illustrated for Channel A in Figure 12 is identical for both channels. The receiver has three 8-bit buffer registers in a FIFO arrangement, in addition to the 8-bit receive shift register. This scheme creates additional time for the CPU to service an interrupt at the beginning of a block of high-speed data. Incoming data is routed through one of several paths (data or CRC) depending on the selected mode and—in asynchronous modes—the character length.

The transmitter has an 8-bit transmit data buffer register that is loaded from the internal data bus, and a 20-bit transmit shift register that can be loaded from the sync-character buffers or from the transmit data register. Depending on the operational mode, outgoing data is routed through one of four main paths before it is transmitted from the Transmit Data output (TxD).

The system program first issues a series of commands that initialize the basic mode of operation and then other commands that qualify conditions within the selected

TRANSMIT AND RECEIVE DATA PATH (CHANNEL A)

Figure 12



mode. For example, the asynchronous mode, character length, clock rate, number of stop bits, even or odd parity might be set first; then the interrupt mode; and finally, receiver or transmitter enable.

Both channels contain registers that must be programmed via the system program prior to operation. The channel-select input (B/$\overline{A}$) and the control/data input (C/$\overline{D}$) are the command-structure addressing controls, and are normally controlled by the CPU address bus. Figures 15 and 16 illustrate the timing relationships for programming the write registers and transferring data and status.

Read Registers. The SIO contains three read registers for Channel B and two read registers for Channel A (RR0-RR2 in Figure 13) that can be read to obtain the status information; RR2 contains the internally--modifiable interrupt vector and is only in the Channel B register set. The status information includes error conditions, interrupt vector and standard communications-interface signals.

To read the contents of a selected read register other than RR0, the system program must first write the pointer byte to WR0 in exactly the same way as a write register operation. Then, by executing a read instruction, the contents of the addressed read register can be read by the CPU.

The status bits of RR0 and RR1 are carefully grouped to simplify status monitoring. For example, when the interrupt vector indicates that a Special Receive Condition interrupt has occured, all the appropriate error bits can be read from a single register (RR1).

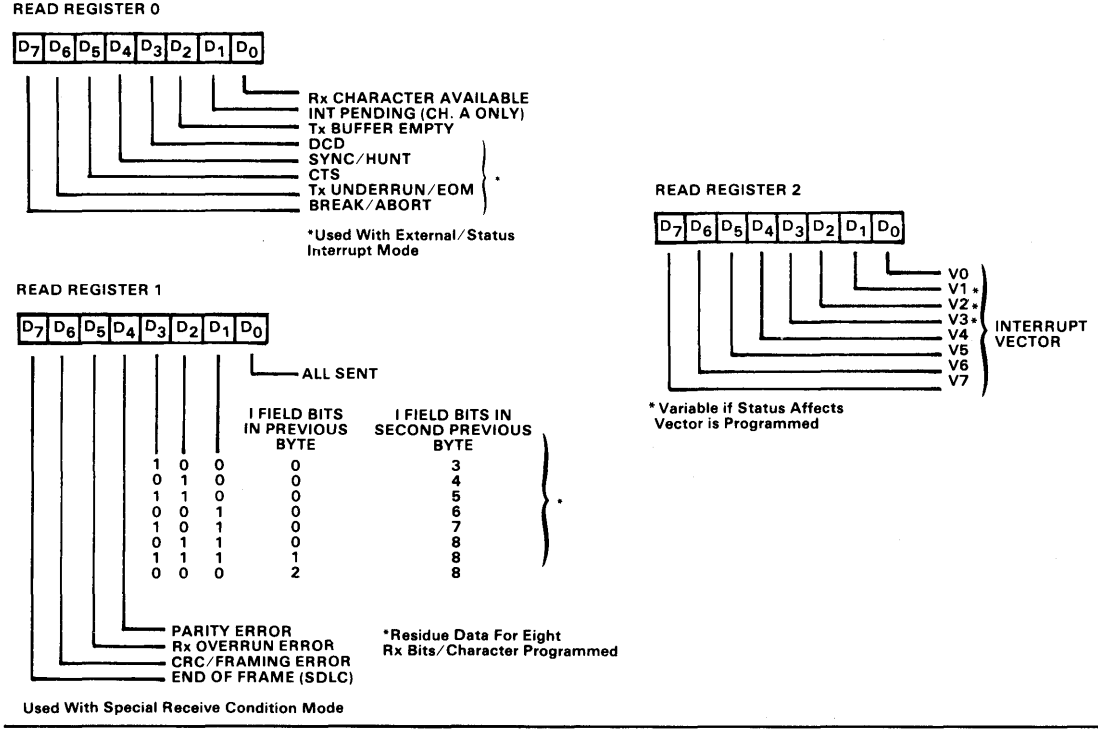
Write Registers. The SIO contains eight write registers for Channel B and seven write registers for Channel A (WR0-WR7 in Figure 14) that are programmed separately to configure the functional personality of the channels; WR2 contains the interrupt vector for both channels and is only in the Channel B register set. With the exception of WR0, programming the write registers requires two bytes. The first byte is to WR0 and contains three bits (D_0-D_2) that point to the selected register; the second byte is the actual control word that is written into the register to configure the SIO.

WR0 is a special case in that all of the basic commands can be written to it with a single byte. Reset (internal or external) initializes the pointer bits D_0-D_2 to point to WR0. This implies that a channel reset must always point to WR0.

The SIO must have the same clock as the CPU (same phase and frequency relationship, not necessarily the same driver).

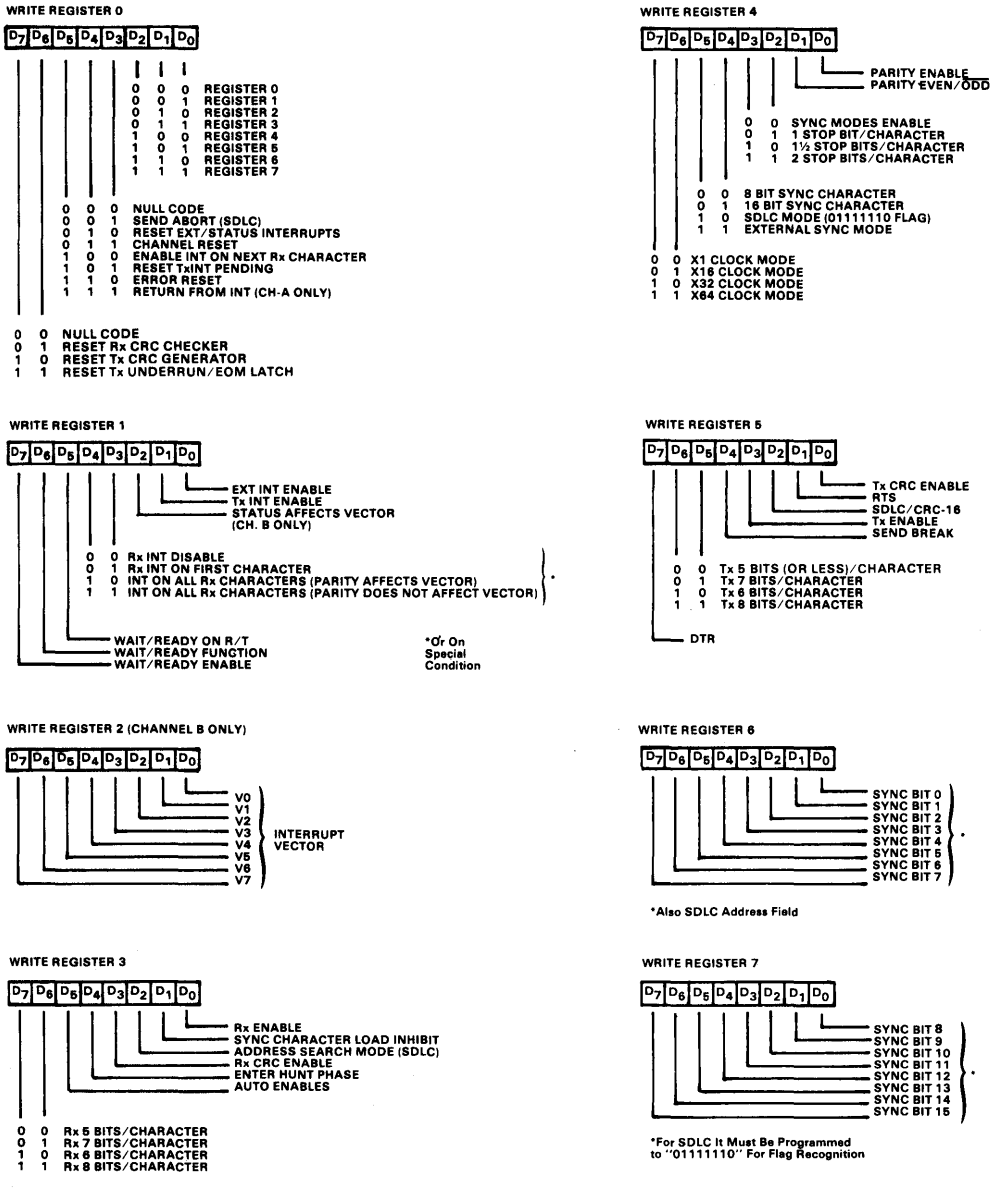
VII

READ REGISTER BIT FUNCTIONS
Figure 13



WRITE REGISTER BIT FUNCTIONS

Figure 14



Read Cycle. The timing signals generated by a Z80 CPU input instruction to read a data or status byte from the SIO are illustrated in Figure 15.

Write Cycle. Figure 16 illustrates the timing and data signals generated by a Z80 CPU output instruction to write a data or control byte into the SIO.

Interrupt-Acknowledge Cycle. After receiving an interrupt-request signal from an SIO ($\overline{INT}$ pulled Low), the Z80 CPU sends an interrupt-acknowledge sequence ($\overline{M1}$ Low, and $\overline{IORQ}$ Low a few cycles later) as in Figure 17. The SIO contains an internal daisy-chained interrupt structure for prioritizing nested interrupts for the various functions of its two channels, and this structure can be used within an external user-defined daisy chain that prioritizes several peripheral circuits.

The IEI of the highest-priority device is terminated High. A device that has an interrupt pending or under service forces its IEO Low. For devices with no interrupt pending or under service, IEO = IEI.

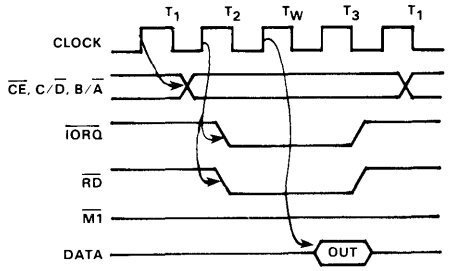
To insure stable conditions in the daisy chain, all interrupt status signals are prevented from changing while M1 is Low. When IORQ is Low, the highest priority interrupt requestor (the one with IEI High) places its interrupt vector on the data bus and sets its internal interrupt-under-service latch.

Return From Interrupt Cycle. Figure 18 illustrates the return from interrupt cycle. Normally, the Z80 CPU issues a RETI (return from interrupt) instruction at the end of an interrupt service routine. RETI is a 2-byte opcode (ED-4D) that resets the interrupt-under-service latch in the SIO to terminate the interrupt that has just been processed. This is accomplished by manipulating the daisy chain in the following way.

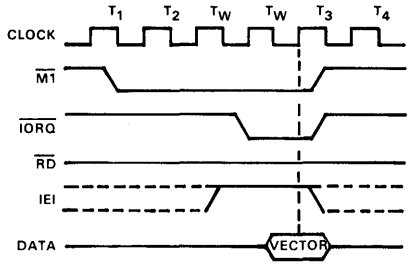
The normal daisy-chain operation can be used to detect a pending interrupt; however, it cannot distinguish between an interrupt under service and a pending unacknowledged interrupt of a higher priority. Whenever "ED" is decoded, the daisy chain is modified by forcing High the IEO of any interrupt that has not yet been acknowledged. Thus the daisy chain identifies the device presently under service as the only one with an IEI High and an IEO Low. If the next opcode byte is "4D", the interrupt-under-service latch is reset.

The ripple time of the interrupt daisy chain (both the High-to-Low and the Low-to-High transitions) limits the number of devices that can be placed in the daisy chain. Ripple time can be improved with carry-look-ahead, or by extending the interrupt-acknowledge cycle. For further information about techniques for increasing the number of daisy-chained devices, refer to the MK3880 Z80 CPU Product Specification.

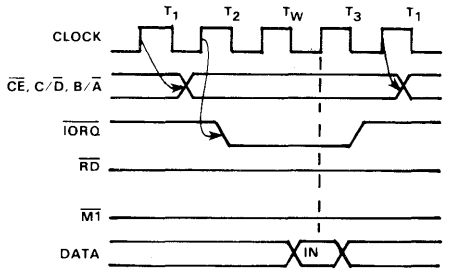
READ CYCLE
Figure 15



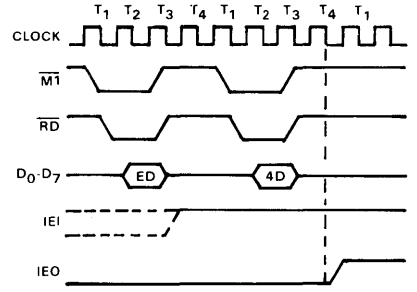
INTERRUPT ACKNOWLEDGE CYCLE
Figure 17



WRITE CYCLE
Figure 16



RETURN FROM INTERRUPT CYCLE
Figure 18



ABSOLUTE MAXIMUM RATINGS

Voltages on all inputs and outputs with respect to GND ..... -0.3V to +7.0V
Operating Ambient Temperature ..... As Specified in Ordering Information
Storage Temperature ..... -65°C to +150°C

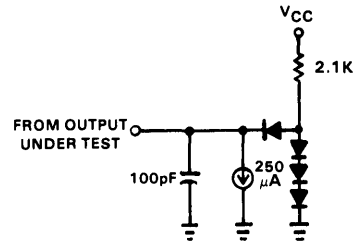
Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

- $+4.75V \leq V_{CC} \leq +5.25V$
- GND = 0V
- T_A as specified in Ordering Information

All AC parameters assume a load capacitance of 100 pF max. Timing references between two output signals assume a load difference of 50 pF max.



DC CHARACTERISTICS

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{ILC}	Clock Input Low Voltage	-0.3	+0.80	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -0.6	+5.5	V	
V_{IL}	Input Low Voltage	-0.3	+0.8	V	
V_{IH}	Input High Voltage	+2.0	+5.5	V	
V_{OL}	Output Low Voltage		+0.4	V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	+2.4		V	I_{OH} = -250 μA
I_{LI}	Input Leakage Current	-10	±10	μA	$0 < V_{IN} < V_{CC}$
I_Z	3-State Output/Data Bus Input Leakage Current	-10	+10	μA	$0 < V_{IN} < V_{CC}$
$I_{L(SY)}$	$\overline{SYNC}$ Pin Leakage Current	-40	+10	μA	$0 < V_{IN} < V_{CC}$
I_{CC}	Power Supply Current		100	mA	

Overall specified temperature and voltage range.

CAPACITANCE

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
C	Clock Capacitance		40	pF	Unmeasured pins returned to ground
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

Over specified temperature range; f = 1MHz

AC ELECTRICAL CHARACTERISTICS

See Figure 19

NUMBER	SYM	PARAMETER	MK3884		MK3884-4		UNIT
			MIN	MAX	MIN	MAX	
1	TcC	Clock Cycle Time	400	4000	250	4000	ns
2	TwCh	Clock Width (High)	170	2000	105	2000	ns
3	TfC	Clock Fall Time		30		30	ns
4	TrC	Clock Rise Time		30		30	ns
5	TwC l	Clock Width (Low)	170	2000	105	2000	ns
6	TsAD(C)	$\overline{CE}$, C/$\overline{D}$, B/$\overline{A}$ to Clock ↑ Setup Time	160		145		ns
7	TsCS(C)	$\overline{IORQ}$, $\overline{RD}$ to Clock ↑ Setup Time	240		115		ns
8	TdC(DO)	Clock ↑ to Data Out Delay		240		220	ns
9	TsDI(C)	Data In to Clock ↑ Setup (Write or M1 Cycle)	50		50		ns
10	TdRD(DOz	$\overline{RD}$ ↑ to Data Out Float Delay		230		110	ns
11	TdIO(DOI)	$\overline{IORQ}$ ↓ to Data Out Delay ($\overline{INTA}$ Cycle)		340		160	ns
12	TsM1(C)	$\overline{M1}$ to Clock ↑ Setup Time	210		90		ns
13	TsIEI(IO)	IEI to $\overline{IORQ}$ ↓ Setup Time ($\overline{INTA}$ Cycle)	200		140		ns
14	TdM1(IEO)	$\overline{M1}$ ↓ to IEO ↓ Delay (interrupt before $\overline{M1}$)		300		190	ns
15	TdIEI(IEOr)	IEI ↑ to IEO ↑ Delay (after ED decode)		150		100	ns
16	TdIEI(IEOf)	IEI ↓ to IEO ↓ Delay		150		100	ns
17	TdC(INT)	Clock ↑ to $\overline{INT}$ ↓ Delay		200		200	ns
18	TdIO (W/RWf)	$\overline{IORQ}$ ↓ or $\overline{CE}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Wait Mode)		300		210	ns
19	TdC (W/RR)	Clock ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)		120		120	ns
20	TdC (W/RWz)	Clock ↓ to $\overline{W/RDY}$ Float Delay (Wait Mode)		150		130	ns
21	Th	Any unspecified Hold when Setup is specified	0		0		ns

NOTE: Timings are referenced from minimum V_{IH} or maximum V_{IL} for inputs and from minimum V_{OH} or maximum V_{OL} for outputs.

VII

AC ELECTRICAL CHARACTERISTICS (continued)

See Figure 20

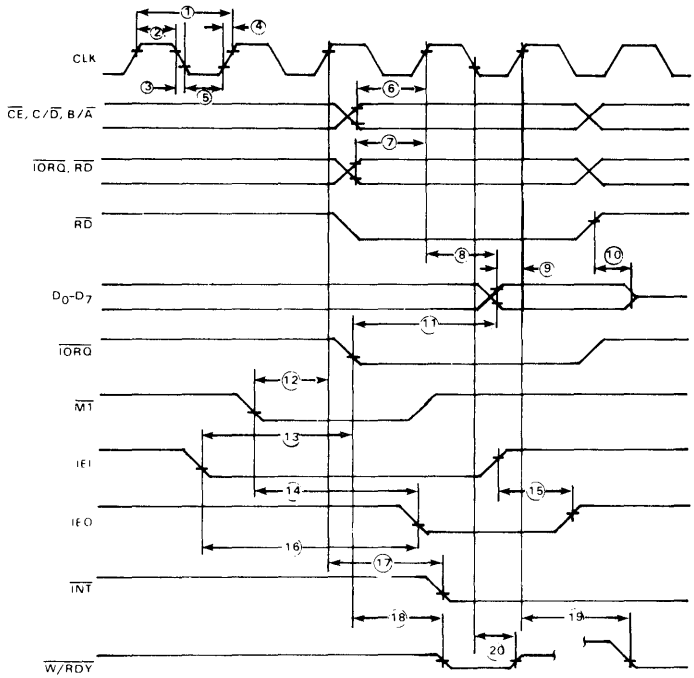
NUMBER	SYM	PARAMETER	MK3884		MK3884-4		UNIT
			MIN	MAX	MIN	MAX	
1	TwPh	Pulse Width (High)	200		200		ns
2	TwPl	Pulse Width (Low)	200		200		ns
3	TcTxC	$\overline{TxC}$ Cycle Time	400	∞	400	∞	ns
4	TwTxCl	$\overline{TxC}$ Width (Low)	180	∞	180	∞	ns
5	TwTxCh	$\overline{TxC}$ Width (High)	180	∞	180	∞	ns
6	TdTxC(TxD)	$\overline{TxC}$ ↓ to TxD Delay (x1 Mode)		400		300	ns
7	TdTxC (W/RRf)	$\overline{TxC}$ ↓ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	5	9	5	9	Clk Periods*
8	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	Clk Periods*
9	TcRxC	$\overline{RxC}$ Cycle Time	400	∞	400	∞	ns
10	TwRxCl	$\overline{RxC}$ Width (Low)	180	∞	180	∞	ns
11	TwRxCh	$\overline{RxC}$ Width (High)	180	∞	180	∞	ns
12	TsRxD(RxC)	RxD to $\overline{RxC}$ ↑ Setup Time (x1 Mode)	0		0		ns
13	ThRxD(RxC)	$\overline{RxC}$ ↑ to RxD Hold time (x1 Mode)	140		140		ns
14	TdRxC (W/RRf)	$\overline{RxC}$ ↑ to $\overline{W/RDY}$ ↓ Delay (Ready Mode)	10	13	10	13	Clk Periods*
15	TdRxC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ ↓ Delay	10	13	10	13	Clk Periods*
16	TdTxC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ ↓ Delay	5	9	5	9	Clk Periods*
17	TdRxC (SYNC)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ ↓ Delay (Output Modes)	4	7	4	7	Clk Periods*
18	TsSYNC (RxC)	$\overline{SYNC}$ ↓ to $\overline{RxC}$ ↑ Setup (External Sync Modes)	-100		-100		ns

In all modes, the System Clock rate must be at least five times the maximum data rate.
RESET must be active a minimum of one complete Clock Cycle.
*System Clock

AC ELECTRICAL CHARACTERISTICS

Figure 19

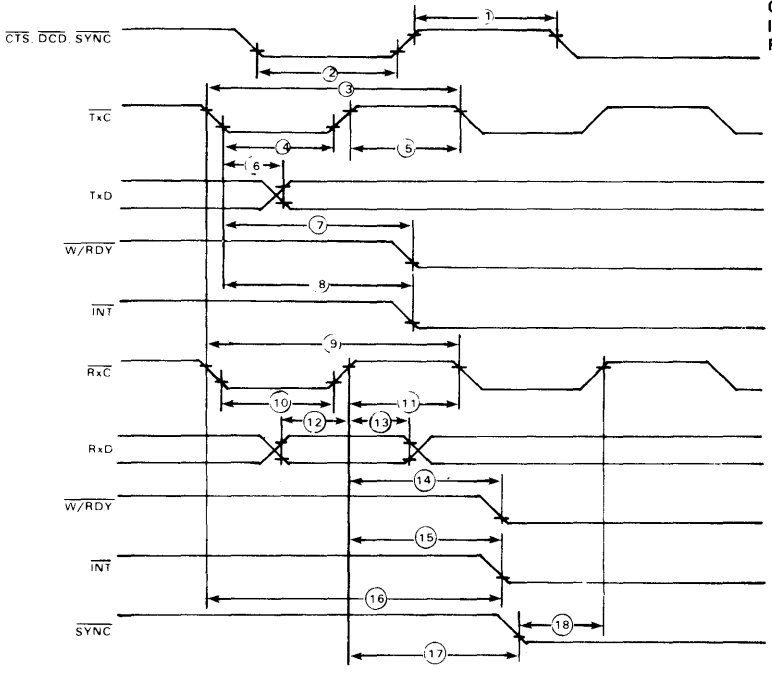
	"1"	"0"
CLOCK	V_{CC}-0.6	0.8 V
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	Δ V	±0.5 V



AC ELECTRICAL CHARACTERISTICS

Figure 20

	"1"	"0"
CLOCK	V_{CC}-0.6	0.8 V
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	Δ V	±0.5 V



VII

ORDERING INFORMATION

PART NO.	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3884N Z80-SIO	Plastic	2.5MHz	0°C to +70°C
MK3884P Z80-SIO	Ceramic	2.5MHz	0°C to +70°C
MK3884N-10 Z80-SIO	Plastic	2.5MHz	-40°C to +85°C
MK3884P-10 Z80-SIO	Ceramic	2.5MHz	-40°C to +85°C
MK3884N-4 Z80A-SIO	Plastic	4MHz	0°C to +70°C
MK3884P-4 Z80A-SIO	Ceramic	4MHz	0°C to +70°C
MK3885N Z80-SIO	Plastic	2.5MHz	0°C to +70°C
MK3885P Z80-SIO	Ceramic	2.5MHz	0°C to +70°C
MK3885N-10 Z80-SIO	Plastic	2.5MHz	-40°C to +85°C
MK3885P-10 Z80-SIO	Ceramic	2.5MHz	-40°C to +85°C
MK3885N-4 Z80A-SIO	Plastic	4MHz	0°C to +70°C
MK3885P-4 Z80A-SIO	Ceramic	4MHz	0°C to +70°C
MK3887N Z80-SIO	Plastic	2.5MHz	0°C to +70°C
MK3887P Z80-SIO	Ceramic	2.5MHz	0°C to +70°C
MK3887N-10 Z80-SIO	Plastic	2.5MHz	-40°C to +85°C
MK3887P-10 Z80-SIO	Ceramic	2.5MHz	-40°C to +85°C
MK3887N-4 Z80A-SIO	Plastic	4MHz	0°C to +70°C
MK3887P-4 Z80-SIO	Ceramic	4MHz	0°C to +70°C

NOTE: Refer to the section on pin descriptions for explanation of the differences between the MK3884, MK3885, and MK3887.

SERIAL INPUT/OUTPUT CONTROLLER MK3884/5/7/SIO/9

FEATURES

- One full-duplex channel, with separate control and status lines for modems or other devices
- Data rates of 0 to 500K bits/second in the x1 clock mode with a 2.5 MHz clock (MK3884/5/7 Z80 SIO/9), or 0 to 800K bits/second with a 4.0 MHz clock (MK3884/5/7-4 Z80 SIO/9)
- Asynchronous protocols: everything necessary for complete messages in 5, 6, 7 or 8 bits/character. Includes variable stop bits and several clock-rate multipliers; break generation and detection; parity; overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7 or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25 and others. Automatic CRC generation/-checking, sync character and zero insertion/deletion, abort generation/detection and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.
- Highly sophisticated and flexible daisy-chain interrupt vectoring for interrupts without external logic.

DESCRIPTION

The MK3884/5/7 Z80 SIO/9 Serial Input/Output Controller is a single channel data communication interface with extraordinary versatility and capability. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communication applications. Functionally, this device is identical to the MK3884 Z80 SIO, except that it operates in one channel only (Channel A).

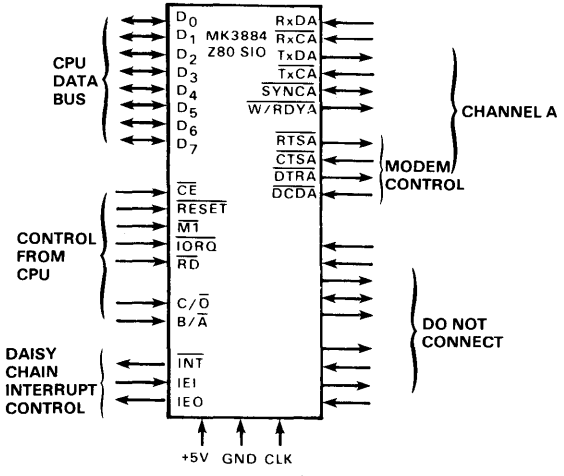
The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communication controllers combined, plus additional functions traditionally performed by the CPU. Moreover, it does this on one fully-independent channel, with an exceptionally sophisticated interrupt structure that allows very fast transfers.

Full interfacing is provided for CPU or DMA control. In addition to data communication, the circuit can handle virtually all types of serial I/O with fast (or slow) peripheral devices. While designed primarily as a member of the Z80 family, its versatility makes it well suited to many other CPUs.

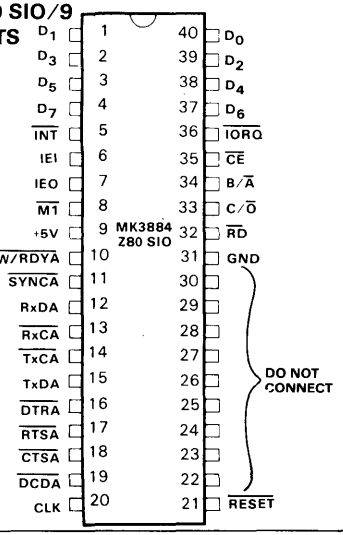
The Z80 SIO/9 is an n-channel silicon-gate depletion-load device packaged in a 40-pin plastic, or ceramic DIP. It uses a

VII

MK3884/5/7 Z80 SIO/9 PIN FUNCTIONS
Figure 1

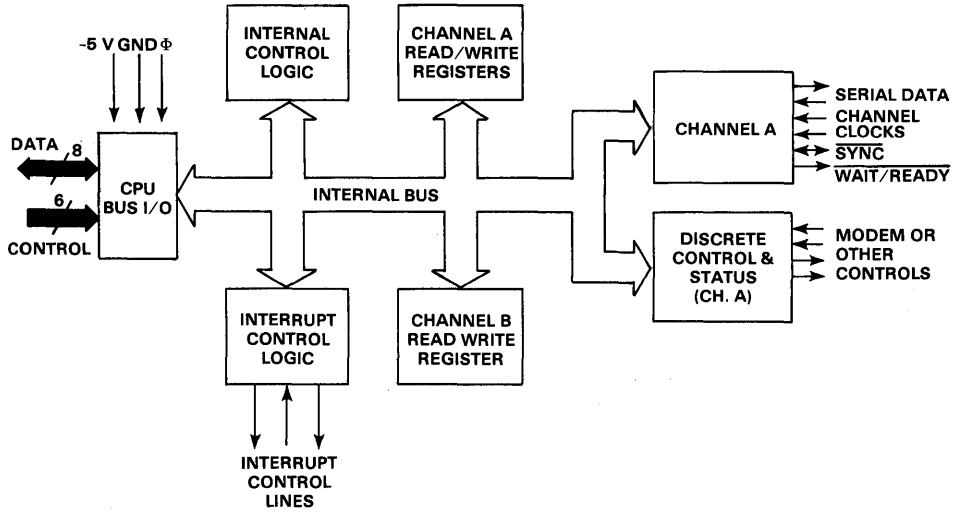


MK3884/5/7 Z80 SIO/9 PIN ASSIGNMENTS
Figure 2



Z80-SIO/9 BLOCK DIAGRAM

Figure 3



single +5V power supply and the standard Z80 family single-phase clock.

Refer to the MK3884/5/7 SIO Data Sheet and the MK3884/5/7 SIO Technical Manual for detailed functional and electrical descriptions. All functional and electrical descriptions in these publications are applicable to the SIO/9, except that Channel B cannot be used for data input or output and that pins 22 through 30 must not be connected.

Write Register 2 (Interrupt Vector) and the Status Affects Vector bit in Write Register 1 are, however, still programmed by selecting Channel B with the B/A input. All other bits in Write Register 1 or Channel B must be programmed to 0.

ORDERING INFORMATION

PART NO.	ZILOG DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3884N SIO/9 MK3884P SIO/9	Z80 SIO/9 Z80-SIO/9	Plastic Ceramic	2.5 MHz 2.5 MHz	0°C to +70°C 0°C to +70°C
MK3884N-4 SIO/9 MK3884P-4 SIO/9	Z80A-SIO/9 Z80A-SIO/9	Plastic Ceramic	4 MHz 4 MHz	0°C to +70°C 0°C to +70°C
MK3885N SIO/9 MK3885P SIO/9	Z80-SIO/9 Z80-SIO/9	Plastic Ceramic	2.5 MHz 2.5 MHz	0°C to +70°C 0°C to +70°C
MK3885N-4 SIO/9 MK3885P-4 SIO/9	Z80A-SIO/9 Z80A-SIO/9	Plastic Ceramic	4 MHz 4 MHz	0°C to +70°C 0°C to +70°C
MK3887N SIO/9 MK3887P SIO/9	Z80-SIO/9 Z80-SIO/9	Plastic Ceramic	2.5 MHz 2.5 MHz	0°C to +70°C 0°C to +70°C
MK3887N-4 SIO/9 MK3887P-4 SIO/9	Z80A-SIO/9 Z80A-SIO/9	Plastic Ceramic	4 MHz 4 MHz	0°C to +70°C 0°C to +70°C

NOTE: Refer to the section on pin descriptions for explanation of the differences between the MK3884, MK3885, and MK3887 SIO/9.

PRELIMINARY

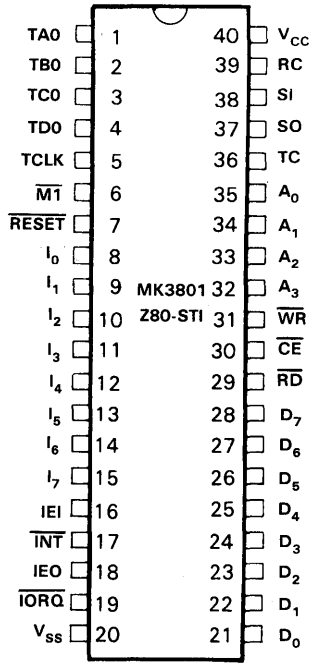
SERIAL TIMER INTERRUPT CONTROLLER MK3801

FEATURES

- ☐ Full duplex USART with programmable DMA control signals
- ☐ Two binary delay timers
- ☐ Two full feature timers with
  - Delay to interrupt mode
  - Pulse width measurement mode
  - Event counter mode
- ☐ Eight general purpose lines with
  - Full bi-directional I/O capability
  - Edge triggered interrupts on either edge
- ☐ Full control of each interrupt channel
  - Enable/disable
  - Maskable
  - Automatic end-of-interrupt mode
  - Software end-of-interrupt mode
- ☐ 2.5, 4 MHz, and 6 MHz versions available

DEVICE PINOUT

Figure 1



INTRODUCTION

The MK3801 Z80 STI (Serial Timer Interrupt) is a multifunctional peripheral device for use in Z80 microprocessor based systems. It is designed to optimize current systems by reducing chip count and system costs. By providing a USART, four timers (two binary and two full function), and eight bi-directional I/O lines with individually programmable interrupts, the MK3801 can make substantial improvement to any Z80 based system.

Control and operation of the MK3801 are provided by 24 internal registers accessible by the Z80 bus. Sixteen of these registers are directly addressable and accessible; eight are indirectly addressable. Two of the four timers provide full service features, while the other two provide delay timer features only. Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation, optional sync word recognition and stripping, and programmable DMA control handshake lines. Eight bi-directional I/O lines provide parallel I/O capability and individually programmable interrupt capability. The interrupt structure of the device is fully programmable for all interrupts, provides for interrupt vector generation, conforms to the Z80 daisy chain interrupt priority scheme, and supports automatic end of interrupt functions for the Z80.

VII

SIGNAL NAME	DESCRIPTION
V_{SS}	Ground
V_{CC}	+5 volts (± 5 percent)
$\overline{CE}$	Chip Enable (Input, active low)
$\overline{RD}$	Read Enable (Input, active low)
$\overline{WR}$	Write Enable (Input, active low)
A_0-A_3	Address Inputs. Used to address one of the internal registers during a read or write operation
D_0-D_7	Data Bus (bi-directional)
$\overline{RESET}$	Device Reset (Input, active low). When activated, all internal registers (except for Timer or USART Data registers) will be cleared, all timers stopped, USART turned off, all interruptsdisabled and all pending interrupts cleared, and all I/O lines placed in tri-state input mode.
I_0-I_7	General purpose I/O and interrupt lines
$\overline{INT}$	Interrupt Request (Output, active low, open drain)
$\overline{IORQ}$	Input/Output Request from Z80-CPU (input, active low). The IORQ signal is used in conjunction with M1 to signal the MK3801 that the CPU is acknowledging its interrupt.
IEI	Interrupt Enable In, active High
IEO	Interrupt Enable Out, active High
SO	Serial Output
SI	Serial Input
RC	Receiver Clock Input
TC	Transmit Clock Input
TAO-TDO	Timer Outputs
TCLK	Timer Clock Input
$\overline{M1}$	Z80 Machine Cycle One (Input, active low)

PIN DESCRIPTION

Figure 1 illustrates the pinout of the MK3801. The functions of these individual pins are described above.

INTERNAL ORGANIZATION

Figure 2 illustrates the MK3801 internal organization, which supports the full set of timing, communications, parallel I/O, and interrupt processing functions available in the device.

CPU BUS I/O

The CPU BUS I/O provides the means of communications between the system and the MK3801. Data, Status, and Control Registers in the MK3801 are accessed by the bus in order to establish device parameters, assert control, and transfer status and data between the system and the MK3801.

Each register in the MK3801 is addressed over the address bus in conjunction with Chip Enable ($\overline{CE}$), while data is transferred over the eight bit Data bus under control of Read ($\overline{RD}$) and Write ($\overline{WR}$) signals.

REGISTER ACCESSES

All register accesses are independent of any system clock. To read a register, both $\overline{CE}$ and $\overline{RD}$ must be active. The internal read control signal is essentially the combination of both $\overline{CE}$ and $\overline{RD}$ active; thus the read operation will begin when the later of these two signals goes active and will end when the first signal goes inactive. The address bus must be stable prior to the start of the operation and must remain stable until the end of the operation. Unless a read operation or an interrupt acknowledge cycle is in progress, the data bus (D_0-D_7) will remain in the tri-state condition.

To write a register, both $\overline{CE}$ and $\overline{WR}$ must be active. The address must be stable prior to the start of the operation and must remain stable until the end of the operation. The data must be stable prior to the end of the operation and must remain stable until the end of the operation. The data presented on the bus will be latched into the register shortly after either $\overline{WR}$ or $\overline{CE}$ goes inactive.

INTERNAL REGISTERS

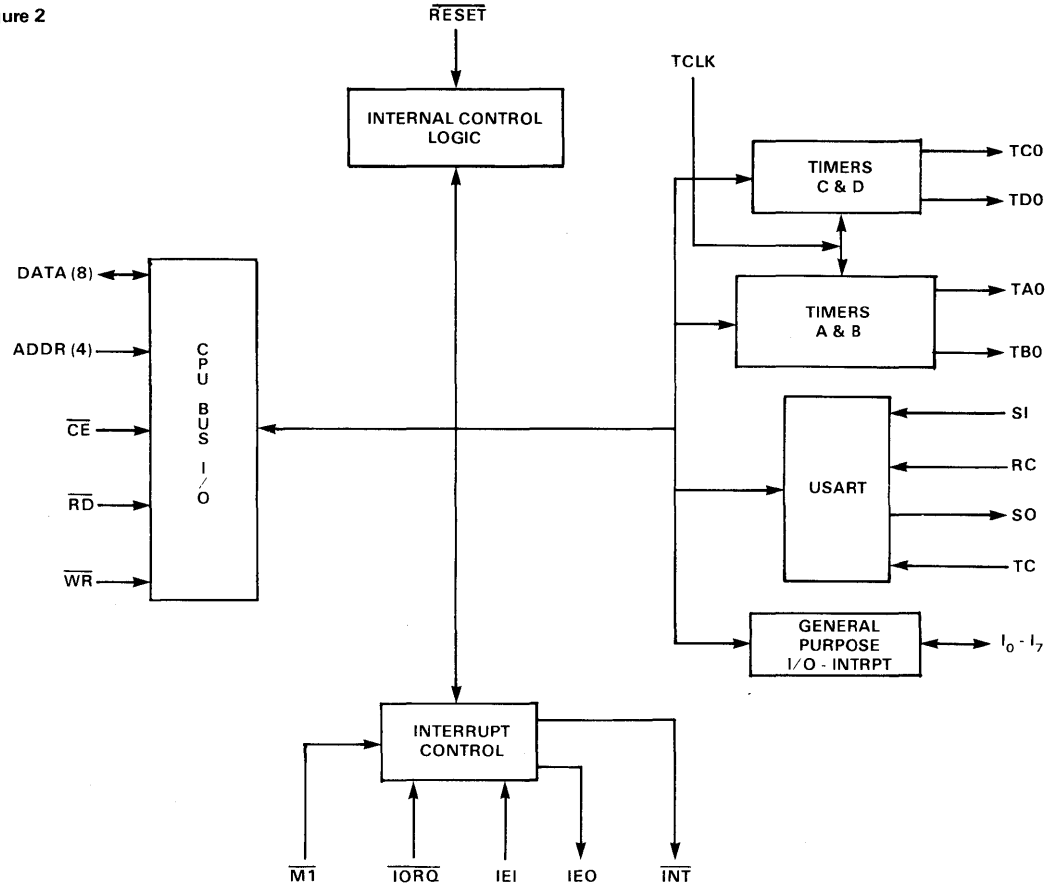
There are 24 internal registers used to control the operation of the STI. Sixteen of these registers are directly addressable and accessible. Eight registers are indirectly addressable via the Pointer/Vector Register and accessible via the Indirect Data Register.

DIRECTLY ADDRESSABLE REGISTERS

The Directly Addressable Registers are accessed by placing the address of the desired register on the address lines (A_0-A_3) during a write or read cycle. Figure 3 lists the Directly Addressable Registers.

INTERNAL ORGANIZATION

Figure 2



DIRECTLY ACCESSIBLE REGISTERS

Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
0	IDR	Indirect Data Register
1	GPIP	General Purpose I/O-Interrupt
2	IPRB	Interrupt Pending Register B
3	IPRA	Interrupt Pending Register A
4	ISRB	Interrupt in-Service Register B
5	ISRA	Interrupt in-Service Register A
6	IMRB	Interrupt Mask Register B
7	IMRA	Interrupt Mask Register A
8	PVR	Pointer/Vector Register
9	TABCR	Timers A and B Control Register

VII

DIRECTLY ACCESSIBLE REGISTERS (Continued)
Figure 3

ADDRESS	ABBREVIATION	REGISTER NAME
A	TBDR	Timer B Data Register
B	TADR	Timer A Data Register
C	UCR	USART Control Register
D	RSR	Receiver Status Register
E	TSR	Transmitter Status Register
F	UDR	USART Data Register

INDIRECTLY ADDRESSABLE REGISTERS
Figure 4

INDIRECT ADDRESS	ABBREVIATION	REGISTER NAME
0	SCR	Sync Character Register
1	TDDR	Timer D Data Register
2	TCDR	Timer C Data Register
3	AER	Active Edge Register
4	IERB	Interrupt Enable Register B
5	IERA	Interrupt Enable Register A
6	DDR	Data Direction Register
7	TCDCR	Timers C and D Control Register

INDIRECTLY ADDRESSABLE REGISTERS

Indirectly Addressable Registers are addressed by placing the indirect address in bits IA0-IA2 of the Pointer/Vector Register, as defined in Figure 5. Data may be written to or read from the register indicated by these Indirect Register Address bits by a write or read access of the Indirect Data Register (selected when A_0-A_3 are all zero). The indirect address bits of the Pointer/Vector Register will remain unchanged after an indirect access. Repeated accesses of the Indirect Data Register will access the same indirect register as long as the indirect address in the Pointer/Vector Register remains unchanged. The Indirectly Addressable Registers are listed in Figure 4.

INTERRUPT VECTOR DEFINITION

Each individual function in the MK3801 is provided with a unique interrupt vector that is presented to the system during the interrupt acknowledge cycle. The interrupt vector returned during interrupt acknowledge is formed as shown in Figure 6. There are 16 vector addresses generated internally by the MK3801, one for each of the 16 interrupt channels. The three most significant bits of these vector addresses correspond to the three most significant bits of the Pointer/Vector Register shown in Figure 5. The least significant bit of each vector address is always 0, thus producing even vector addresses. The remaining 4 bits (IV_1 through IV_4) identify each of the 16 interrupt channels individually. The lowest priority channel responds with 0000 for IV_4-IV_1 respectively. The next higher priority channel responds with 0001, and so on in binary order, with the highest priority channel responding with 1111. Figure 7 lists each of the 16 interrupt channels in order of descending priority.

INTERRUPT CONTROL REGISTERS

The Interrupt Control Registers provide control of interrupt processing for all I/O facilities of the MK3801. These registers allow the programmer to enable or disable any or all of the 16 interrupts, provide masking for any interrupts, and access to the pending or in-service status of the interrupts. Optional End-of-Interrupt modes are available under software control. The format of each of the Interrupt Control Registers is presented in Figure 8.

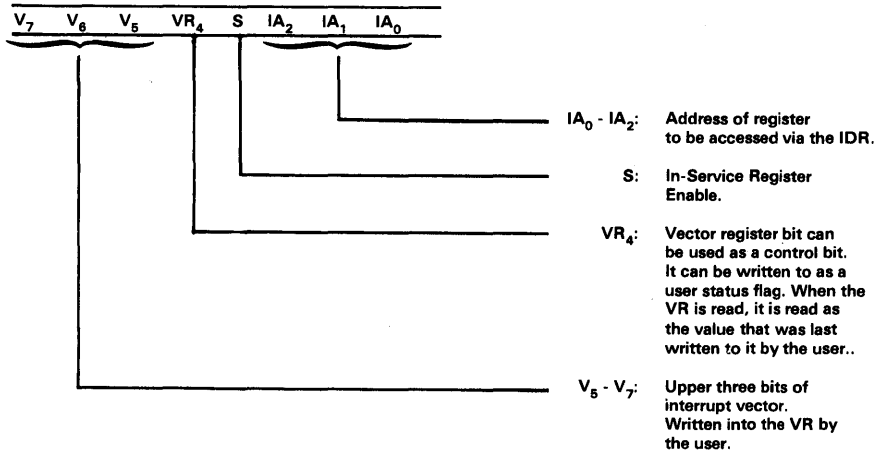
INTERRUPT OPERATION

The Interrupt Enable Registers enable or disable the setting of an interrupt in the Interrupt Pending Registers. A 0 in a bit of the Interrupt Enable Registers disables the interrupt for the associated channel while a 1 enables the interrupt.

Once an interrupt is enabled, the occurrence of an interrupting condition on that channel will cause the

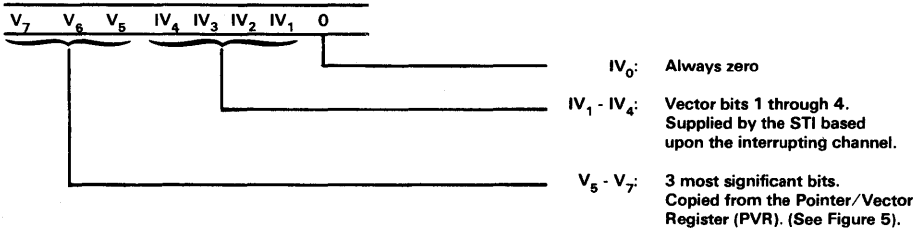
POINTER/VECTOR REGISTER (PVR) Port 08

Figure 5



INTERRUPT VECTOR

Figure 6



VII

corresponding bit in the Interrupt Pending Register to be set. This indicates that an interrupt is pending in the MK3801.

Pending interrupts are presented to the Z80 CPU in order of priority (see Figure 1) unless they have been masked off. This is done by clearing the bit in the Interrupt Mask Register corresponding to the channel whose interrupt is to be masked. The channel's interrupt will remain pending until the mask bit for that channel is set, at which time the interrupt for that channel will be processsed in order of priority.

When an interrupt vector is generated for a pending interrupt and passed to the Z80 CPU, the bit in the Interrupt Pending Register, associated with the channel generating the interrupt, will be cleared. At this time, no history of the interrupt remains in the MK3801.

In order to retain historical evidence of an interrupt being serviced by the Z80, the In-Service Register may be enabled by setting the S-bit in the Pointer/Vector Register (see Figure 5). If the In-Service Register is enabled, the bit of the In-Service Register corresponding to the interrupting channel will be set when the interrupt vector is passed to the Z80. At the same time, the Interrupt Pending bit will be cleared since the interrupt is now in service. The In-Service bit will be cleared on execution of a Return-from-Interrupt (H'ED4D') instruction. The In-Service Registers are directly addressable, and the In-Service bit for any interrupt may be cleared by writing to the In-Service Register if the Return-from-Interrupt instruction is not used.

INTERRUPT CONTROL REGISTER DEFINITIONS

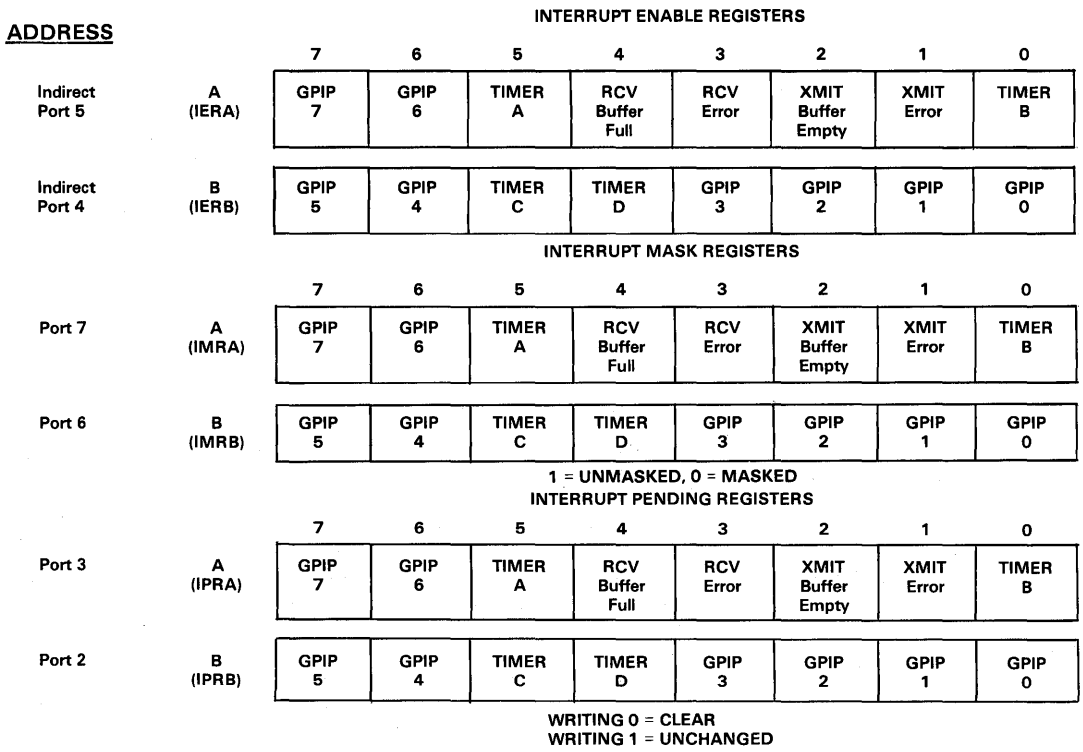
Figure 7

There are sixteen interrupt channels on the STI arranged in the following priority:

PRIORITY	CHANNEL	DESCRIPTION	ALTERNATE USAGE
HIGHEST	1111	General Purpose Interrupt 7 (I_7)	
	1110	General Purpose Interrupt 6 (I_6)	
	1101	Timer A	
	1100	Receive Buffer Full	
	1011	Receive Error	
	1010	Transmit Buffer Empty	
	1001	Transmit Error	
	1000	Timer B	
	0111	General Purpose Interrupt 5 (I_5)	
	0110	General Purpose Interrupt 4 (I_4)	TA (PW-Event)
	0101	Timer C	
	0100	Timer D	
	0011	General Purpose Interrupt 3 (I_3)	TB (PW-Event)
	0010	General Purpose Interrupt 2 (I_2)	
	0001	General Purpose Interrupt 1 (I_1)	DMA (TR)TX
LOWEST	0000	General Purpose Interrupt 0 (I_0)	DMA (RR)REC

INTERRUPT CONTROL REGISTERS

Figure 8



INTERRUPT CONTROL REGISTERS (Continued)

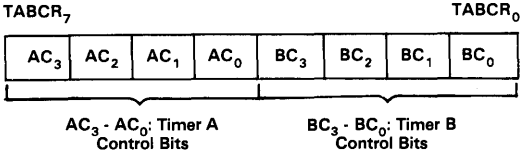
Figure 8

INTERRUPT SERVICE REGISTERS

ADDRESS		7	6	5	4	3	2	1	0
Port 5	A (ISRA)	GPIP 7	GPIP 6	TIMER A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	TIMER B
Port 4	B (ISRB)	GPIP 5	GPIP 4	TIMER C	TIMER D	GPIP 3	GPIP 2	GPIP 1	GPIP 0

TIMER A and B CONTROL REGISTER (TABCR) Port 9

Figure 9



The four control bits are used to select the timer mode and prescale value, as follows:

CONTROL BIT DEFINITION

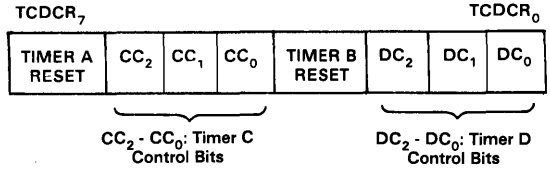
C_3	C_2	C_1	C_0	
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, ÷4 Prescale
0	0	1	0	Delay Mode, ÷10 Prescale
0	0	1	1	Delay Mode, ÷16 Prescale
0	1	0	0	Delay Mode, ÷50 Prescale
0	1	0	1	Delay Mode, ÷64 Prescale
0	1	1	0	Delay Mode, ÷100 Prescale
0	1	1	1	Delay Mode, ÷200 Prescale
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, ÷4 Prescale
1	0	1	0	Pulse Width Mode, ÷10 Prescale
1	0	1	1	Pulse Width Mode, ÷16 Prescale
1	1	0	0	Pulse Width Mode, ÷50 Prescale
1	1	0	1	Pulse Width Mode, ÷64 Prescale
1	1	1	0	Pulse Width Mode, ÷100 Prescale
1	1	1	1	Pulse Width Mode, ÷200 Prescale

TIMER A DATA REGISTER AND TIMER B DATA REGISTER (TADR, TBDR) Port B & Port A

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

TIMER C and D CONTROL REGISTER (TCDCR) Indirect Port 7

Figure 10



Three control bits are used to control each timer, as defined below:

CONTROL BIT DEFINITION

C_2	C_1	C_0	
0	0	0	Timer Stopped
0	0	1	Delay Mode, ÷4 Prescale
0	1	0	Delay Mode, ÷10 Prescale
0	1	1	Delay Mode, ÷16 Prescale
1	0	0	Delay Mode, ÷50 Prescale
1	0	1	Delay Mode, ÷64 Prescale
1	1	0	Delay Mode, ÷100 Prescale
1	1	1	Delay Mode, ÷200 Prescale

TIMER C DATA REGISTER and TIMER D DATA REGISTER (TCDR, TDDR) Indirect, Port 2 and Indirect Port 1

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

VII

TIMERS

Four timers are available on the MK3801. Two provide full service features including delay timer operation, event counter operation, pulse width measurement operation, and pulse generation. The two other timers provide delay timer features only, and may be used for baud rate generators for use with the USART.

All timers are prescaler/counter timers, with a common independent clock input, and are not required to be operated from the system clock. In addition, all timers have a time-out output function that toggles each time the timer times out.

TIMER CONTROL REGISTERS

The 4 timers (A,B,C, and D) are programmed via 2 control registers and 4 timer data registers. Timers A and B are controlled by a single register (TABCR) and two timer data registers (TADR,TBDR). Timers C and D are controlled by a second control register (TCDCR) and two timer data

registers (TCDR, TDDR). Bits in the control registers allow the selection of operational mode, prescale, and control, while the data registers are used to read the timer or write the time constant register. General Purpose I/O Interrupt pins 3 (TB) and 4 (TA) are used for timer B and A inputs in event and pulse width modes. Figure 9 illustrates the Control and Data Register for timers A and B, while Figure 10 illustrates the Control and Data registers for timers C and D.

USART

Serial Communication is provided by the USART, which is capable of either asynchronous or synchronous operation. Variable word width and start/stop bit configurations are available under software control for asynchronous operation. For synchronous operation, a Sync Word is provided to establish synchronization during receive operations. The Sync Word will also be repeatedly transmitted when no other data is available for transmission. Operational modes exist to allow stripping of all Sync Words received in synchronous operation, and to allow the operation of DMA control handshake lines by the USART through General Purpose I/O Port lines 0 and 1. Separate receive and transmit clocks are available, and separate receive and transmit status and data bytes allow independent operation of the transmit and receive sections.

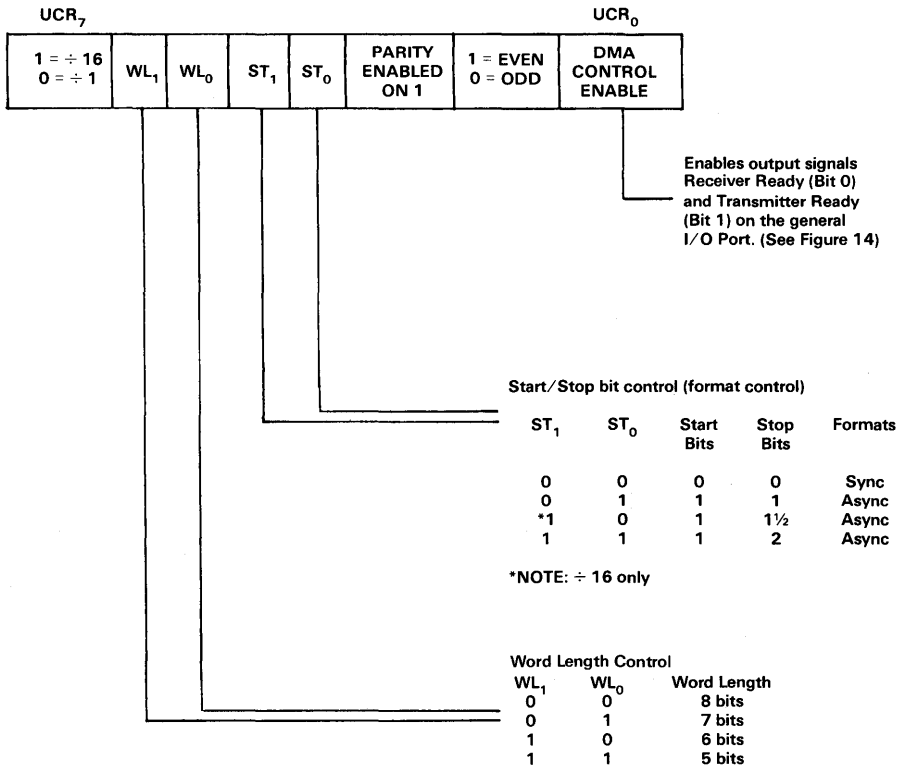
USART CONTROL REGISTERS

The USART is provided with 3 control/status registers and a data register. The programmer may specify operational parameters for the USART via the Control Register, as shown in Figure 11. Status of both the Receiver and Transmitter sections is accessed by means of the 2 Status Registers, as shown in Figure 12. Data written to the Data Register is passed to the transmitter, while reading the data register will access data received by the USART. The USART Data Register form is illustrated in Figure 13.

ERROR CONDITIONS

Error conditions in the USART are determined by monitoring the Receive Status Register (Port D) and the Transmitter Status Register (Port E). These error conditions are only valid for each word boundary and are not latched. When executing block transfers of data, it is necessary to save any errors so that they can be checked at the end of a block. In order to save error conditions during data transfer, the STI interrupt controller may be used by enabling error

USART CONTROL REGISTER (UCR) Port C
Figure 11



RECEIVER STATUS REGISTER (RSR) Port D

Figure 12

RSR_7							RSR_0
BUFFER FULL	OVERRUN ERROR	PARITY ERROR	FRAME ERROR	FOUND/$\overline{\text{SEARCH}}$ OR BREAK DETECT	MATCH/CHARACTER IN PROGRESS	SYNC STRIP ENABLE	RECEIVER ENABLE

TRANSMITTER STATUS REGISTER (TSR) Port E

TSR_7							TSR_0
BUFFER EMPTY	UNDERRUN ERROR	AUTO TURNAROUND	END OF TRANSMISSION	BREAK	HIGH	LOW	TRANSMITTER ENABLE

H	L	Serial Output State
0	0	Hi-Z
0	1	Low ("0")
1	0	High
1	1	Loop*

*Connects transmitter output to receiver input. In loopback mode, transmitter goes high when disabled. Also connects clocks with TC given priority.

USART DATA REGISTER (UDR) Port F

Figure 13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

GENERAL PURPOSE I/O CONTROL REGISTERS

Figure 14

ACTIVE EDGE CONTROL REGISTER (AER) Indirect Port 3

1 = RISING
0 = FALLING

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

DATA DIRECTION REGISTER (DDR) Indirect Port 6

1 = OUTPUT
0 = INPUT

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1	GPIP 0

GENERAL PURPOSE I/O DATA REGISTER (GPIP) Port 1

GPIP 7	GPIP 6	GPIP 5	GPIP 4	GPIP 3	GPIP 2	GPIP 1 (TR)	GPIP 0 (RR)
			TIMER A INPUT	TIMER B INPUT			

interrupts (Port 5, Indirect) for the desired channel (Receive error or Transmit error) and by masking these bits off (Port 7). Once the transfer is complete, the Interrupt Pending Register (Port 3) can be polled to determine the presence of a pending error interrupt, and therefore an error.

GENERAL PURPOSE I/O - INTERRUPT PORT

The General Purpose I/O - Interrupt Port provides eight I/O lines that may be operated either as inputs or outputs under software control. In addition, each line may generate an interrupt on either a positive going edge or a negative going edge of the input signal.

Two of the lines in this port provide auxiliary input functions for the timers in the pulse width measurement mode and the event counter mode. Two others serve as auxiliary output lines for the USART, one indicating the Receive Buffer Full condition (RR) and the other indicating the Transmitter Buffer Empty condition (TR). These may be used as handshake signals for a DMA controller or other external control circuitry.

GENERAL PURPOSE I/O CONTROL REGISTERS

The General Purpose I/O and Interrupt Port has 2 control registers. One allows the programmer to specify the Active Edge for each bit that will trigger the interrupt associated with that bit. The other register specifies the Data Direction (input and output) associated with each bit. The third register is the actual data I/O register used to input or output data to the port. When the USART is programmed to use DMA signals, this overrides the GPIP data and the DDR. The General Purpose I/O Control and Data Registers are illustrated in Figure 14.

MK3801 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -25°C to + 100°C
Storage Temperature ..... -65°C to + 150°C
Voltage on Any Pin with Respect to Ground ..... -.3 V to + 7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITION
V_{IH}	Input High Voltage	2.0	V_{CC} + 3	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -120 μA
V_{OL}	Output Low voltage		0.4	V	I_{OL} = 2.0 mA
I_{LL}	Power Supply Current		180	mA	Outputs Open
I_{LI}	Input Leakage Current		±10	μA	V_{IN} = 0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float		10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float		-10	μA	V_{OUT} = 0.4 V

All voltages are referenced to ground.

CAPACITANCE

T_A = 25°C, f = 1 MHz unmeasured pins returned to ground.

SYM	PARAMETER	MAX	UNIT	TEST CONDITION
C_{IN}	Input Capacitance	10	pf	Unmeasured pins returned to ground
C_{OUT}	Tri-state Output Capacitance	10	pf	

A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise noted.

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
A_0-A_3	T_{SAR} & T_{SAW}	Address setup time prior to falling edge of $\overline{CEWR}$ or $\overline{CERD}$	80		30		15		ns	
	T_{HAR} & T_{HAW}	Address hold time after rising edge of $\overline{CEWR}$ or $\overline{CERD}$	0		0		0		ns	
$\overline{CEWR}$	T_{WL}	$\overline{CEWR}$ pulse width low (write cycle)	360		205		175		ns	Note 1
	T_{WW}	$\overline{CEWR}$ high time between write cycles	580		400		300		ns	
	T_{WRD}	$\overline{CEWR}$ high to $\overline{CERD}$ low	580		400		300		ns	
$\overline{CERD}$	T_{RDL}	$\overline{CERD}$ pulse width low (read cycle)	400		250		215		ns	Note 1
	T_{RR}	$\overline{CERD}$ high time between read cycles	300		200		190		ns	
	T_{M1RD}	Rising $\overline{M1RD}$ to falling $\overline{M1RD}$	225		165		95		ns	
	T_{RDW}	$\overline{CERD}$ high to $\overline{CEWR}$ low	125		100		75			
$\overline{M1}$	T_{SM1}	$\overline{M1}$ setup time prior to falling $\overline{IORQ}$ during interrupt acknowledge	800		500		350		ns	
$\overline{IORQ}$	T_{IOL}	$\overline{IORQ}$ low time	300		185		170		ns	
IEI	T_{SIEI}	Setup to falling $\overline{IORQ}$ during interrupt acknowledge	140		80		65		ns	
	T_{SRD}	Setup prior to end of 4D read on RETI	100		50		40		ns	
D_0-D_7	T_{SDM1}	Data valid prior to rising $\overline{RD}$ ($\overline{M1}$ cycle)	65		50		45		ns	Load 100 pf +
	T_{HDM1}	Data hold time after rising $\overline{RD}$ ($\overline{M1}$ cycle)	0		0		0		ns	1 TTL load
	T_{DRD}	Data output delay from $\overline{CERD}$		400		250		215	ns	
	T_{SDW}	Data setup time to rising edge of $\overline{CEWR}$	350		280		175		ns	
	T_{HDW}	Data hold time from rising edge of $\overline{CEWR}$	0		0		0		ns	
	T_{DDI}	Data output delay from falling $\overline{IORQ}$ during interrupt acknowledge		300		185		170	ns	

VII

A.C. CHARACTERISTICS (Continued)

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
	T_{DHVZ}	Data hold time following M1 IORQ during interrupt acknowledge cycle.	0		0		0		ns	
	T_{DDZ}	Delay to float		150		100		80	ns	
I_0-I_7	T_{IPW}	Minimum active pulse width	200		100		90		ns	
	T_{ICY}	Minimum time between active edges	200		100		90		ns	
	T_{DIW}	Data valid from rising CEWR		600		500		400	ns	Load 100 pf + 1 TTL
RR	T_{DRR}	Delay from rising RC		710		590		545	ns	1 TTL
TR	T_{DTR}	Delay from rising TC		800		645		590	ns	
TAO-TDO	T_{DTW}	Timer output low from rising edge of CEWR (A & B) (Reset T_{OUT})		600		500		400	ns	Load 100 pf +
	T_{DTI}	T_{OUT} valid from Internal timeout		2 t_{CLK} +400		2 t_{CLK} +300		2 t_{CLK} +250	ns	1 TTL load
TCLK	T_{tCLKL}	Low time	130		95		75		ns	
	T_{tCLKH}	High time	130		95		75		ns	
	T_{tCKC}	Cycle time	300	2500	200	2500	165	2500	ns	
RESET	T_{RSL}	Low time for part reset	3		2		1.6		μs	
IEO	T_{DIEOH}	IEO delay from rising edge of IEI		200		130		100	ns	Load 100 pf +
	T_{DIEOL}	IEO delay from falling edge of IEI		200		130		100	ns	1 TTL load
	T_{DIEOM}	IEO delay from falling edge of M1 (interrupt occurring just prior to M1)		270		190		110	ns	
	T_{DIEOA}	Delay to rising IEO from rising IORQ during interrupt acknowledge		1000		800		600	ns	
	T_{DIEOR}	Delay to rising IEO from rising edge of RD during ED fetch of RETI		500		400		300	ns	
INT	T_{DRCI}	Time delay from Receive Clock to interrupt from rising or falling edge of RC		910		760		680	ns	

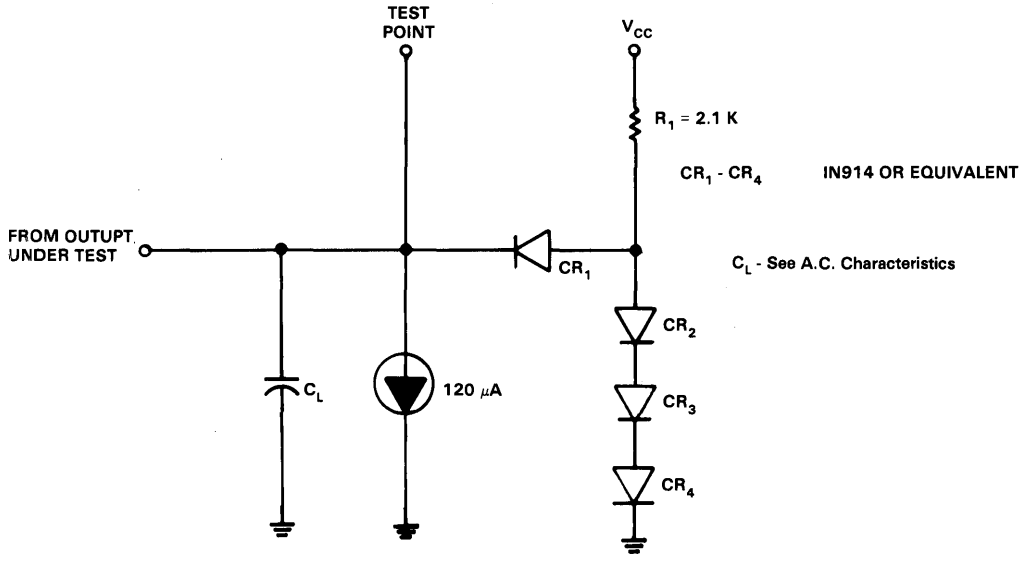
A.C. CHARACTERISTICS (Continued)

SIGNAL	SYMBOL	PARAMETER	MK3801-0		MK3801-4		MK3801-6		UNIT	CONDITION
			MIN	MAX	MIN	MAX	MIN	MAX		
	T_{DTCI}	Time delay from Transmit Clock to interrupt from rising or falling edge of TC		1460		980		690	ns	
SI	T_{SSI}	Serial in set up time to rising edge of RC (Divide by one only)	80		80		55		ns	
	T_{HSI}	Data hold time from rising edge of RC (Divide by one only)	400		350		300		ns	
SO ÷ 1	T_{DSO}	Data valid from falling edge of TC		420		390		345	ns	100 pf + 1 TTL load
SO ÷ 16	T_{DSO}	Data valid from falling edge of TC		520		490		445	ns	100 pf + 1 TTL load
TC	T_{TCL}	Low time	650		500		400		ns	
	T_{TCH}	High time	650		500		400		ns	
	T_{TCCY}	Cycle time	1.5		1.05		.85		μs	
RC	T_{RCL}	Low time	650		500		400		ns	
	T_{RCH}	High time	650		500		400		ns	
	T_{RCCY}	Cycle time	1.5		1.05		.85		μs	

NOTE:
1. One wait state must be inseted when used as a 6 MHz memory mapped device.
2. All A.C. measurements are referenced to V_{IL} max., V_{IH} min., V_{08} (0.8V), or (2.0 V).

OUTPUT LOAD CIRCUIT

Figure 15



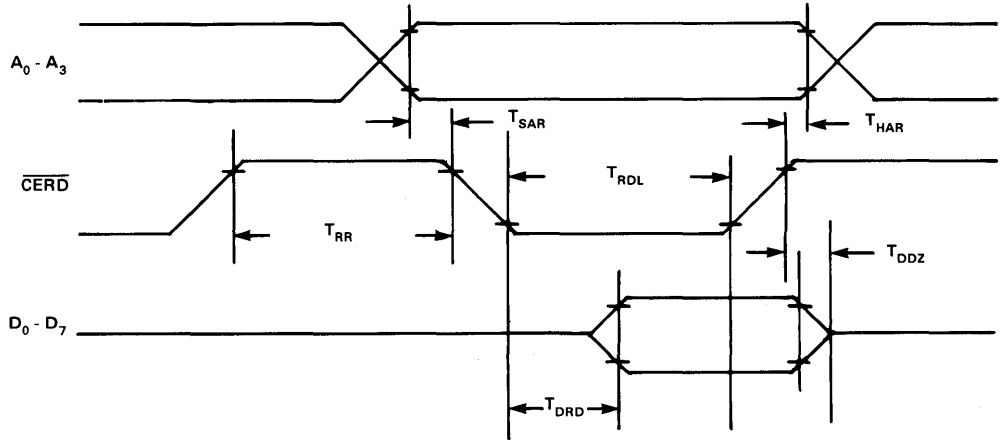
TIMING DIAGRAMS

Figure 16

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"		"0"
OUTPUT	2.0 V		0.8 V
INPUT	2.0 V		0.8 V
FLOAT	Δ V	=	0.5 V

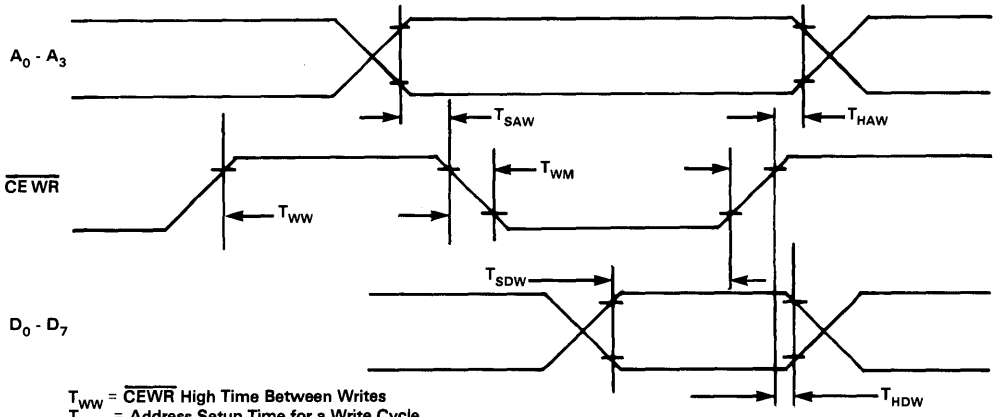
READ CYCLE



T_{SAR} = Address Setup Time for a Read Cycle
T_{DRD} = Data Output Delay from $\overline{CERD}$
T_{DDZ} = Time to Tri-State Following a Read Cycle
T_{HAR} = Required Address Hold Time Following a Read Cycle

WRITE CYCLE

Figure 17

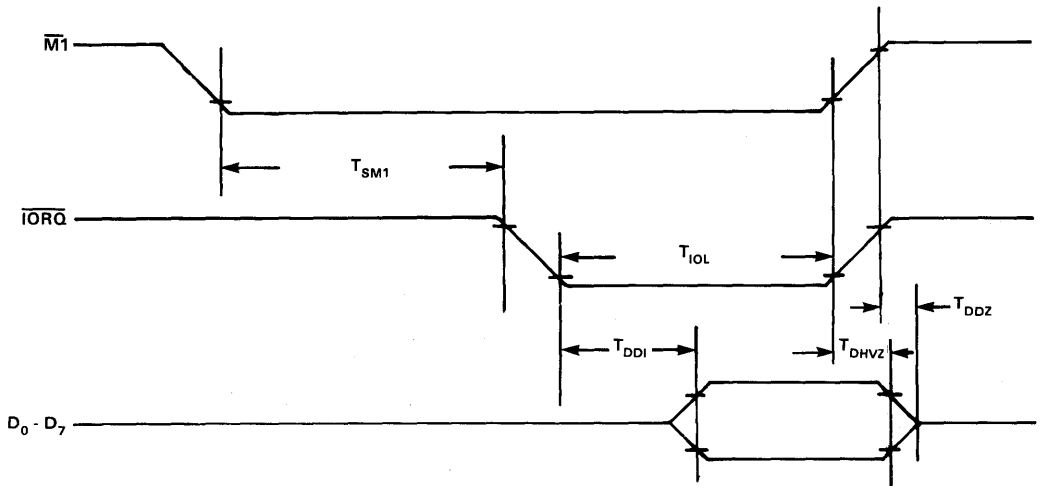


T_{WW} = $\overline{CEWR}$ High Time Between Writes
T_{SAW} = Address Setup Time for a Write Cycle
T_{SDW} = Data Setup Time Prior to the End of a Write Cycle
T_{HDW} = Required Data Hold Time Following a Write Cycle
T_{HAW} = Required Address Hold Time Following a Write Cycle
T_{WM} = $\overline{CEWR}$ pulse width low

VII

INTERRUPT ACKNOWLEDGE CYCLE

Figure 18



T_{IOL} = $\overline{IORQ}$ Pulse Width Low
T_{SMI} = $\overline{M1}$ Setup Time prior to $\overline{IORQ}$ For an Acknowledge cycle
T_{DDI} = Access Time for Vector
T_{DDZ} = Time to Tri-State Following a Vector
T_{DHVZ} = Data hold time following $\overline{M1}$ $\overline{IORQ}$ during interrupt acknowledge cycle

TIMER A.C. CHARACTERISTICS

Definitions:

Error = Indicated Time Value - Actual Time Value

tpsc = t_{CLK} x Prescale Value

Internal Timer Mode

V_{CC} + .:

Single Interval Error (free running) (Note 2) ..... ± 100 ns
Cumulative Internal Error 0
Error Between Two Timer Reads ..... ± (tpsc + 4 t_{CLK})
Start Timer to Stop Timer Error ..... 2 t_{CLK} + 100 ns to −(tpsc + 6t_{CLK} + 100 ns)
Start Timer to Read Timer Error ..... 0 to −(tpsc + 6 t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (Note 3) ..... −2 t_{CLK} to −(4t_{CLK} +800 ns)

Pulse Width Measurement Mode

Measurement Accuracy (Note 1) ..... 2 t_{CLK} to −(tpsc + 4t_{CLK})
Minimum Pulse Width ..... 4t_{CLK}

Event Counter Mode

Minimum Active Time of I_3, I_4 ..... 4t_{CLK}
Minimum Inactive Time of I_3, I_4 ..... 4t_{CLK}

NOTES:
1. Error may be cumulative if repetitively performed.
2. Error with respect to T_{OUT} or INT if note 3 is true.
3. Assuming it is possible for the timer to make an interrupt request immediately.

ORDERING INFORMATION

PART NO.	DESIGNATOR	PACKAGE TYPE	MAX CLOCK FREQUENCY	TEMPERATURE RANGE
MK3801N-0	Z80-STI	Plastic	2.5 MHz	0 to 70°C
MK3801N-4	Z80-STI	Plastic	4.0 MHz	0 to 70°C
MK3801N-6	Z80-STI	Plastic	6.0 MHz	0 to 70°C

1984/1985 MICROELECTRONIC DATA BOOK

3870 FAMILY
SELECTION GUIDE

	MEMORY					I/O	PKG.	ADDRESS RANGE		MISC.
ROM DEVICES	ROM x 8	SCRATCHPAD RAM x 8	EXECUTABLE RAM x 8	PARALLEL I/O LINES	SERIAL I/O	PACKAGE SIZE	ADDRESS REGISTERS SIZE	USABLE ADDRESS RANGE (Note 1)	STANDBY RAM OPTION	OTHER
2870/10	1K	64	0	20	No	28	12 bits	1K	No	
3870/10	1K	64	0	32	No	40	12 Bits	1K	No	
3870/20	2K	64	0	32	No	40	11 Bits 12 Bits	2K	No	(Note 2)
38C70/20	2K	64	0	32	No	40	16 Bits	2K	Halt Mode	CMOS
3870/30	3K	64	0	32	No	40	12 Bits	3K	No	
3870/40	4K	64	0	32	No	40	12 Bits	4K	No	
3870/42	4032	64	64	32	No	40	12 Bits	4K	No	
3873/22	2K	64	64	29	Yes	40	12 Bits	2K + 64	No	Baud rate generator
3875/42	4032	64	64	30	No	40	12 Bits	4K	Yes	
P-PROM DEVICES										Address external Memory (EPROM) through socket on top of 40 pin package
97300	0	64	64	29	Yes	40	12 Bits	4K	No	(38P73)
97310	0	64	64	29	Yes	40	12 Bits	4K	No	(38P73)
97400	0	64	64	32	No	40	12 Bits	4K	No	(38P70)
97403	0	64	64	30	No	40	12 Bits	4K	Yes	(38P75)
97410	0	64	64	32	No	40	12 Bits	4K	No	(38P70)
97500	0	64	64	32	No	40	16 Bits	8K +64	No	(38P70)
97501	0	64	64	32	No	40	16 Bits	8K +64	No	(38P70)
97502	0	64	64	32	No	40	16 Bits	64K	No	(38P70)

NOTES:

1. Usable address range is the amount of memory that can effectively be addressed. This may be less than the full range of the address registers either because the amount of on-chip memory is less than the possible address range or, in the case of P-PROM devices, all address bits are not externally available.
2. The original 3870 device (3870/20) has 11 bit address registers. A version is now available with 12 bit address registers.

VIII

MK3870 AND MK38P70

MK3870 FEATURES

- ☐ Available with 1K, 2K, or 4K bytes of mask programmable ROM memory
- ☐ 64 bytes scratchpad RAM
- ☐ Available with 64 bytes executable RAM
- ☐ 32 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary timer
  Interval timer mode
  Pulse width measurement mode
  Event counter mode
- ☐ External interrupt input
- ☐ Crystal, LC, RC, or external time base options
- ☐ Low power (275 mW typ.)
- ☐ Single +5 volt supply

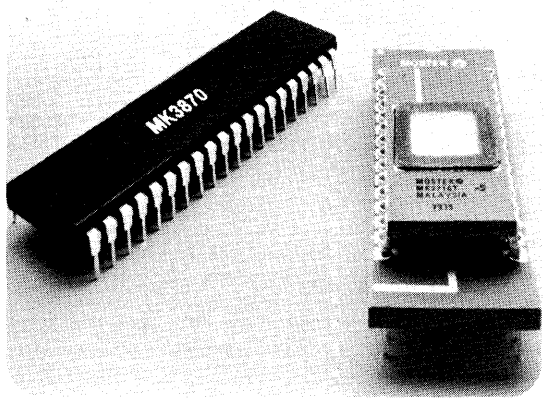
MK38P70 FEATURES

- ☐ EPROM version of MK3870
- ☐ Piggyback PROM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3870
- ☐ In-Socket emulation of MK3870

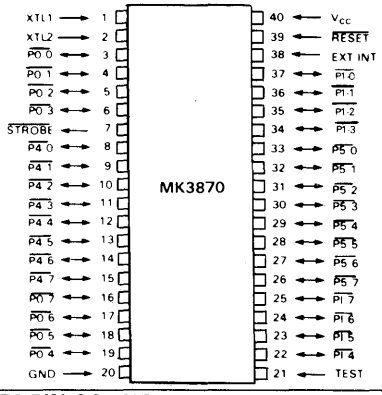
GENERAL DESCRIPTION

The MK3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. The MK3870 can execute a set of more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK3870 features 1-4K bytes of ROM and optional additional executable RAM depending on the specific part type designated by a slash number suffix. The MK3870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 32 bits of I/O.

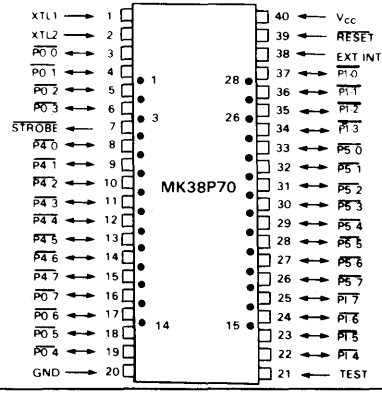
The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the



MK3870 PIN CONNECTIONS

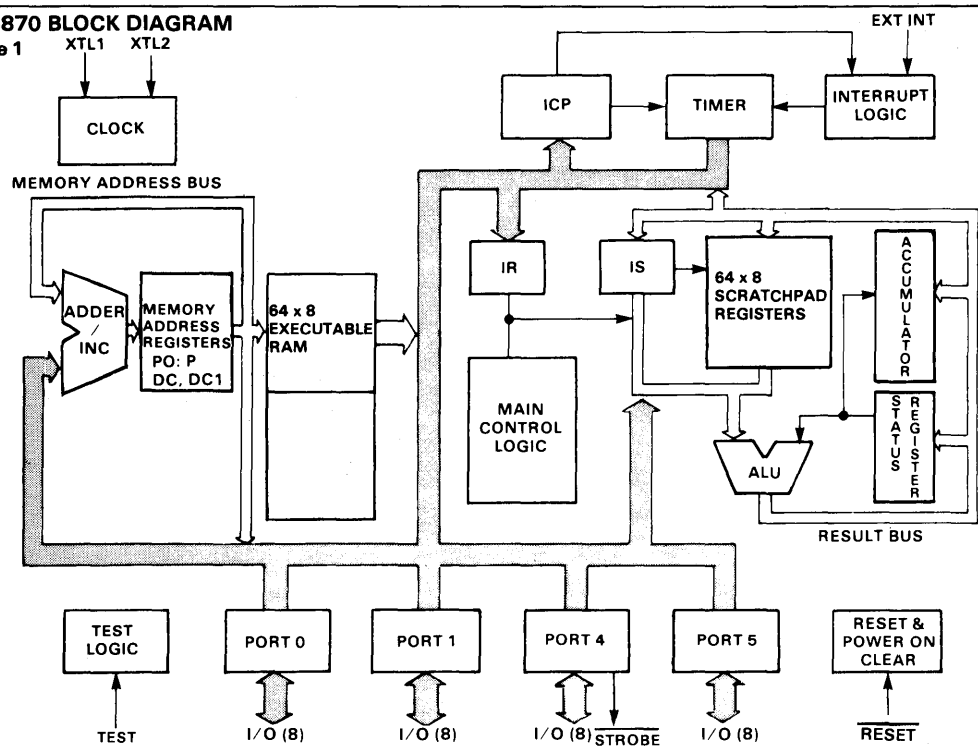


MK38P70 PIN CONNECTIONS



VIII

MK3870 BLOCK DIAGRAM
Figure 1



event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources for the MK3870 and MK38P70: Crystal, LC, RC, or external clock. In addition, the user can specify either a ±10% power supply tolerance or a ±5% power supply tolerance.

The MK38P70 microcomputer is the PROM based version of the MK3870. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P70 retains exactly the same pinout and architectural features as other members of the 3870 family. The MK38P70 is discussed in more detail in a later section.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$ -- $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ -- $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ -- $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ -- $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$-- $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$--$\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$--$\overline{P5\text{-}7}$ are 32 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ may be used to externally reset the MK3870. When pulled low the MK3870 will reset. When then allowed to go high the MK3870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK3870. The MK38P70 will operate with any of the four configurations.

TEST is an input, used only in testing the MK3870. For normal circuit function this pin may be left unconnected, but

it is recommended that TEST be grounded. On MK38P70 devices, the TEST must be grounded.

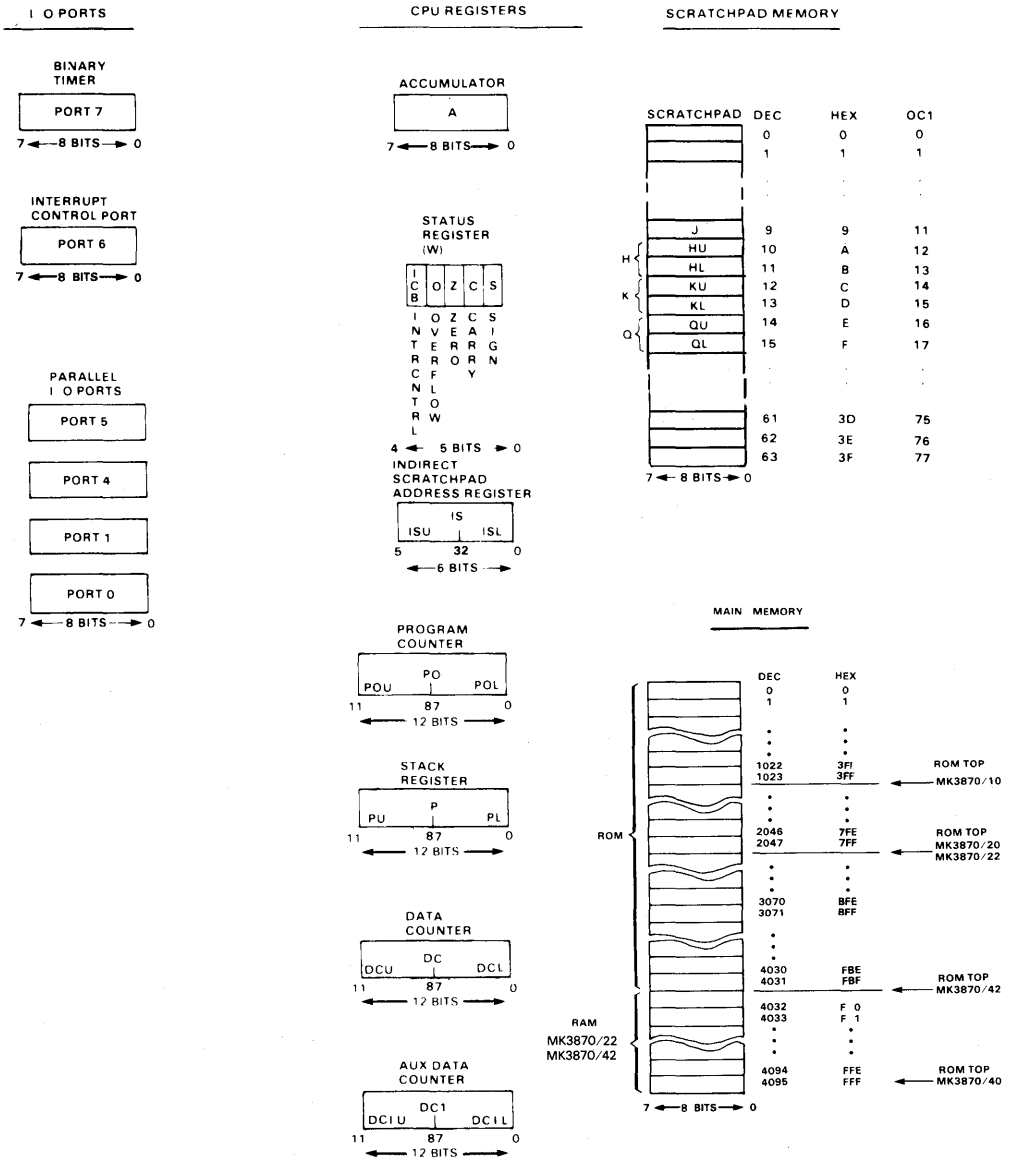
V_{CC} is the power supply input (single +5v).

MK3870 ARCHITECTURE

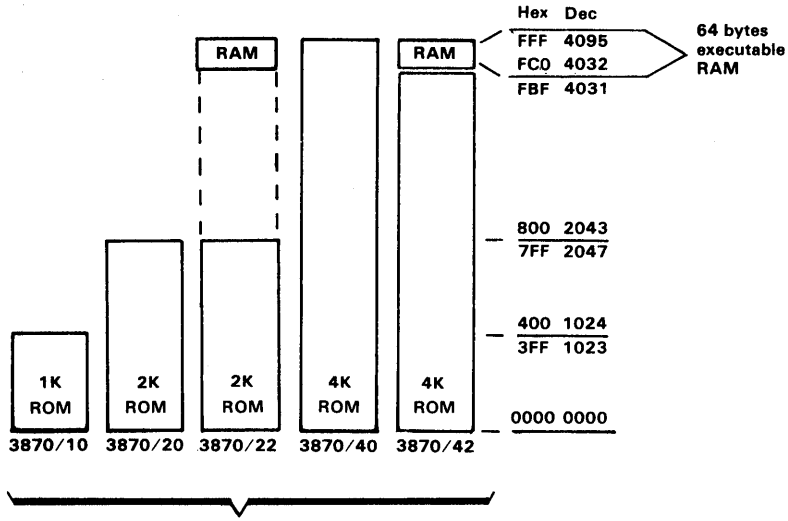
The basic functional elements of the MK3870 are shown in Figure 1. A programming model is shown in Figure 2. The architecture is common to all members of the 3870 family. All 3870 devices are instruction set compatible and differ only in amount and type of ROM, RAM, and I/O. The unique features of the MK3870 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to all 3870 family devices.

MK3870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



MK3870 MAIN MEMORY
SIZES AND TYPES BY SLASH NUMBERS
Figure 3



All devices contain 64 bytes of scratchpad RAM.

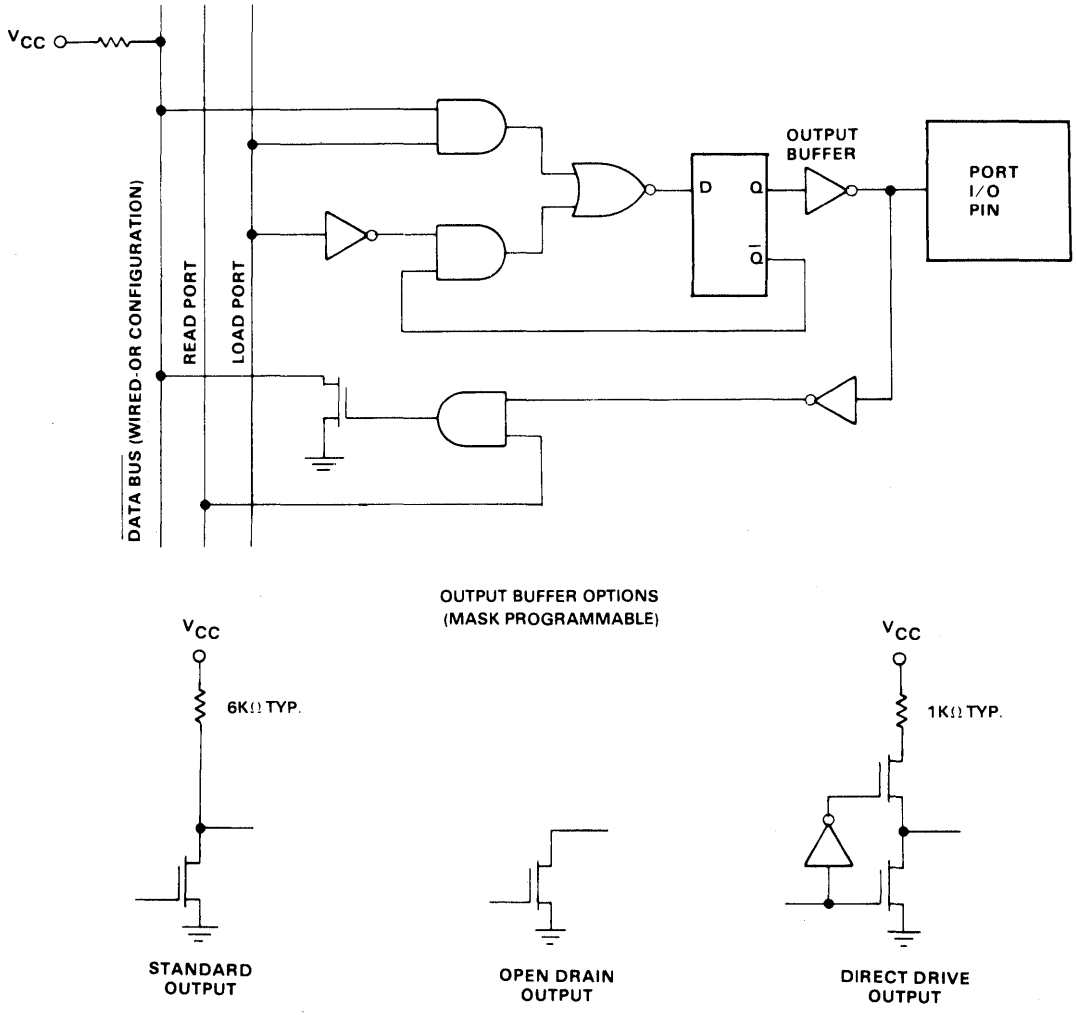
NOTE: Data derived from addressing any locations other than those within a part's specified ROM space or RAM space (if any) are not tested nor are the data guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK3870/10	64 bytes	12 bits	1024 bytes	0 bytes
MK3870/20*	64 bytes	12 bits	2048 bytes	0 bytes
MK3870/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3870/40	64 bytes	12 bits	4096 bytes	0 bytes
MK3870/42	64 bytes	12 bits	4032 bytes	64 bytes

*The MK3870/20 is equivalent to the original 3870 device in memory size; however, the original 3870 had an 11-bit Address Register. The original 3870 with 11-bit Address Register is available where required. Consult the section describing ROM Code Ordering Information for additional information.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



VIII

Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable).

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P70.

MK3870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the XDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

The graph in Figure 3 shows the amounts of ROM and executable RAM for every available slash number in the MK3870 pin configuration.

EXECUTABLE RAM

The upper bytes of the address space in some of the MK3870 devices are RAM memory. As with the ROM memory, the RAM may be addressed by the PO and the DC address registers. The executable RAM may be addressed by all MK3870 instructions which address Main Memory. Additionally, the MK3870 may execute an instruction sequence which resides in the executable RAM. Note this cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory.

I/O PORTS

The MK3870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may also be used as an input strobe to Port 4 after completing the input operation.

MK38P70 GENERAL DESCRIPTION

The MK38P70 is the EPROM version of the MK3870. It retains an identical pinout with the MK3870, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P70 is housed in two packages which incorporate a 28 or 24-pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P70 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P70 eliminates the need for emulator board products. In addition, several MK38P70s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3870s. The compact size of the MK38P70/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P70 can be used as the actual production device.

Most of the material which has been presented for the MK3870 in this document applies to the MK38P70. This includes the description of the pin configuration, architecture, programming model, and I/O ports. Additional information is presented in the following sections.

MK38P70 MAIN MEMORY

There are two basic versions of the MK38P70. These are the 97400 series and the 97500 series. The 97400 series parts have twelve bit address capability thus a total 4K memory map like the MK3870 ROM devices. The 97500 series has 16 bit address capability. The 97400 series accepts 24 pin EPROMs, and the 97500 series accepts 28 pin EPROMs.

As can be seen from Figure 6, both the 97400 series and the 97500 series contain on-chip RAM in the upper portion of their memory maps and no on-chip ROM. Instead of on-chip ROM, address and data lines are brought out to the 28 pin socket located directly on top of the 40 pin package so that external memory devices (principally EPROMs) are addressed.

By using an external EPROM, the 38P70 may be used to emulate the 3870 ROM devices. The 97400 series can directly emulate the following devices.

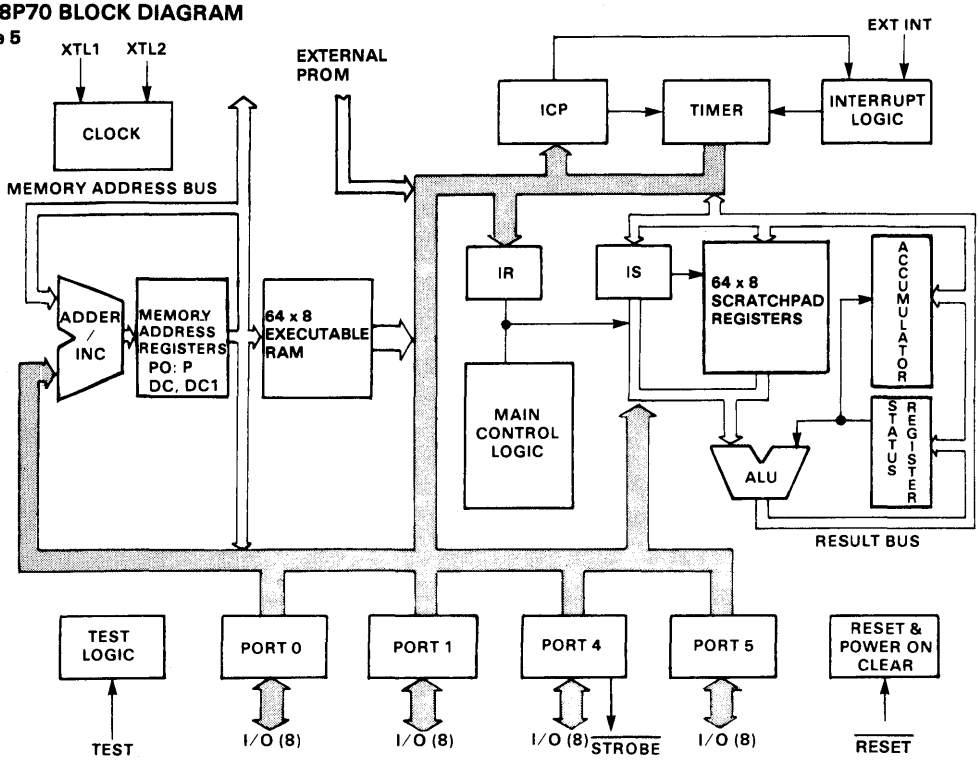
MK3870/10
MK3870/20
MK3870/22
MK3870/42

The MK3870/40 cannot be emulated exactly by the 97400 series because the 97400 devices have the 64 bytes of RAM in the upper memory map while the 3870/40 provides ROM memory in this address space.

Besides the difference in the size of the address registers, 97500 series can also emulate many of the 3870 ROM devices. This difference in address capability should not cause any functional difference as long as normal programming practice is used. That is, as long as address roll-over or automatic truncation is not used. One such usage would be an end around branch (branching forward

MK38P70 BLOCK DIAGRAM

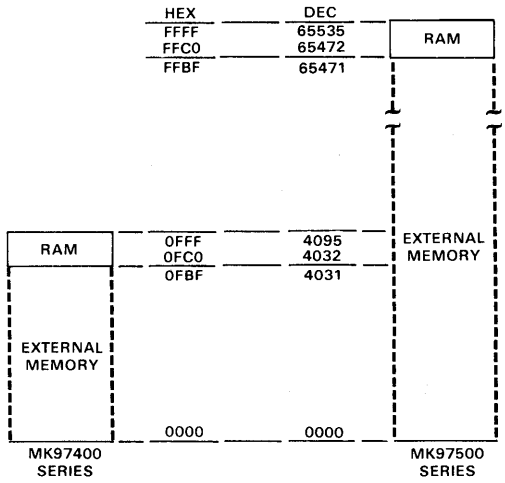
Figure 5



VIII

MK38P70 MAIN MEMORY MAP

Figure 6



MK38P70 TYPE	SCRATCHPAD RAM SIZE (DECIMAL)	ADDRESS REGISTER SIZE	EXTERNALLY ADDRESSABLE MEMORY SIZE	INTERNAL EXECUTABLE RAM SIZE
97400 Series	64 bytes	12 bits	4032 bytes	64 bytes
97500 Series	64 bytes	16 bits	65472 bytes	64 bytes

MK38P70 devices have no internal ROM memory.

at upper memory to get to lower memory). Another case would be in using automatic truncation of data loaded into the 12 bit address registers on the ROM devices. For example, to access some particular location (03FF hex for example) via the data counter, one could load that address into DC using the DCI instruction. The instruction

DCI '73FF'

would cause 3FF to be loaded into the DC of the 3870 ROM device because the upper bits of the DC (bits 12-15) do not exist. If that instruction was followed by the LM instruction, the data stored at location 3FF would be obtained. The 97500 series devices would not truncate the 73FF address to 3FF. As previously stated, this type of programming is generally not done and thus the 97500 devices can be used to emulate the following devices directly.

MK3870/10
MK3870/20
MK3870/40

The 97500 series can also be used to emulate the remainder of the 3870 devices as long as one accounts for the difference in the location of the RAM memory. In the 97500 devices, RAM is located at FFC0 through FFFF. While in 3870 devices this RAM (when it exists) is located at 0FC0 through 0FFF. When this minor difference is accounted for, the 97500 series will also emulate the following devices.

MK3870/22
MK3870/42

MK38P70 EPROM SOCKET

A 28 or 24 pin socket is located on top of the 40 pin package, depending on the specific device. A 28 pin top socket array was used so that the same package could be used for all 38P70 devices but could accommodate both 24 pin and 28 pin. Due to pin-out differences between various common memory devices, several different versions of the MK38P70 are provided with differing signals connected to particular pins on the socket. Figure 7 shows the various options available. When 24 pin memories are used, they are inserted so that pin 1 of the memory device is plugged into pin 3 of the array (the 24 pin memory is lower justified in the 28 pin array).

MK38P70 I/O PORTS

For custom 3870 ROM codes, the user is given a bit by bit selection of I/O options on I/O ports 4 and 5. Additionally, the user has the option of selecting whether or not either $\overline{\text{RESET}}$ or EXT INT has an internal pull-up resistor. This flexibility allows about 172 million possible variations in I/O port and $\overline{\text{RESET}}$ and EXT INT configurations. Obviously, it is not practical to offer this variety in an "off the shelf" product like the 38P70. Thus a few variations are offered which still give some flexibility to the designer. The available I/O options are also shown in Figure 7.

28 PIN SOCKET SIGNALS

The 40 package pins are the identical signals that are provided with the MK3870 ROM devices. In addition to these 40 inputs and outputs, various other signals are implemented on the 38P70 die which are available for connection to the top socket. Depending upon the particular version, some subset of these signals are connected to the 28 or 24 pin socket. These signals are described below.

A_0 - A_{11} (97400 Series)
A_0 - A_{15} (97500 Series)

These are the address buses. They are always outputs and a new address will appear on this bus during each machine cycle. Normally this is the address of op-codes or operands, but there are machine cycles wherein no op-code or operand is required by the CPU. During these cycles, an address is still provided but the data that may be read from that address is not used.

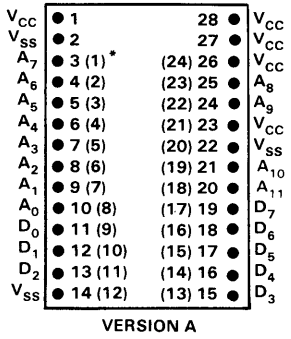
D_0 - D_7 (97400 and 97500 Series)

This is the bi-directional data bus for the external memory. Normally these lines are high impedance inputs. During op-code or operand reads, they receive data from the external memory and conduct it onto the internal 38P70 data bus. During those cycles wherein the operation is strictly internal to the 38P70, they remain hi-z inputs. Data may be presented to the 38P70 by an external memory device but it is not conducted onto the internal data bus. This includes machine cycles wherein op-codes or operands are read from the internal executable RAM. During the operand write machine cycle that occurs in the ST (store) instruction, they become push-pull outputs to conduct data to be written out to the external memory. However, if data is written to the internal executable RAM, this transaction is strictly internal and thus the data bus lines remain in their hi-z state. It, therefore, depends upon the address as to whether this bus becomes an active output bus or remains high impedance. If the address of the operand is not within the internal executable RAM space when a ST instruction is executed, D_0 - D_7 will become active outputs at the appropriate time, or else they will remain in the hi-z state. The 97400 devices do not provide a RD (read) control signal, nor is this signal provided on all versions of the 97500 series. Thus if a ST is executed with the operand address being that of external memory, that memory may access data and drive it onto D_0 - D_7 while the 38P70 is also driving data onto D_0 -D_7 and a bus conflict will result. This condition should be avoided; thus the user should note whether or not his external memory will drive D_0 - D_7 in this event. If it will drive D_0 - D_7, an ST with that operand address should be avoided. In general, one would not normally execute a write to a memory location where there is ROM or EPROM memory instead of RAM. However, some 3870 users have

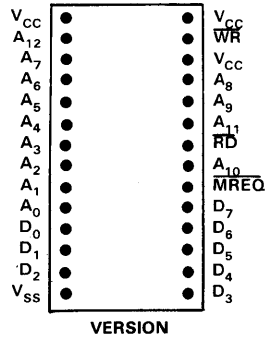
MK38P70 VERSIONS

Figure 7

DEVICE	PORT 4 I/O TYPE	PORT 5 I/O TYPE	SUPPORTS THESE MEMORY DEVICES	TOP 28 PIN SOCKET ARRAY WIRING VERSION
MK97400	TTL	TTL	2716, 2516, 2532, 2758 MK34000 ROM	A
MK97410	Open Drain	Open Drain	2716, 2516, 2532, 2758 MK34000 ROM	A
MK97501	TTL	TTL	2764, 2732, MK37000 ROM MK34000 ROM	B
MK97521	TTL	Open Drain	2764, 2732, MK37000 ROM MK34000 ROM	B



VERSION A



VERSION B

***NOTE:** On Version A packages, sockets are provided in only 24 of the 28 possible locations for a 24 pin EPROM.

VIII

found the ST instruction useful even in devices like the 3870/20 which have no executable RAM. In this case it causes the data counter to increment (to perhaps totalize some event) but otherwise does nothing as one cannot write the internal ROM. No internal conflicts will occur if one attempts to write a 3870 ROM location. Most 97500 versions place a $\overline{RD}$ (read, active low) signal on the top socket pin which matches the $\overline{OE}$ (output enable, active low) input on most memories. Since $\overline{RD}$ will remain high during an operand write, the external memory would not have its data outputs enabled and no conflict will occur.

$\overline{MREQ}$ (97500 Series Only)

This is an active low output which occurs during each machine cycle. It goes high at the start of each cycle then goes low for the remainder of the cycle.

$\overline{RD}$ (97500 Series Only)

This is the active low read output which goes high at the start of each cycle then goes low if data (op-codes or operands) are to be read from external memory. During cycles wherein a strictly internal operation occurs, $\overline{RD}$ will remain high. It will also remain high during an operand write cycle.

$\overline{WR}$ (97500 Series Only)

This is the active low write control output. It is normally high but will go low then return high during an operand write if the address is not that of internal executable RAM.

$\overline{FETCH}$ (97500 Series Only)

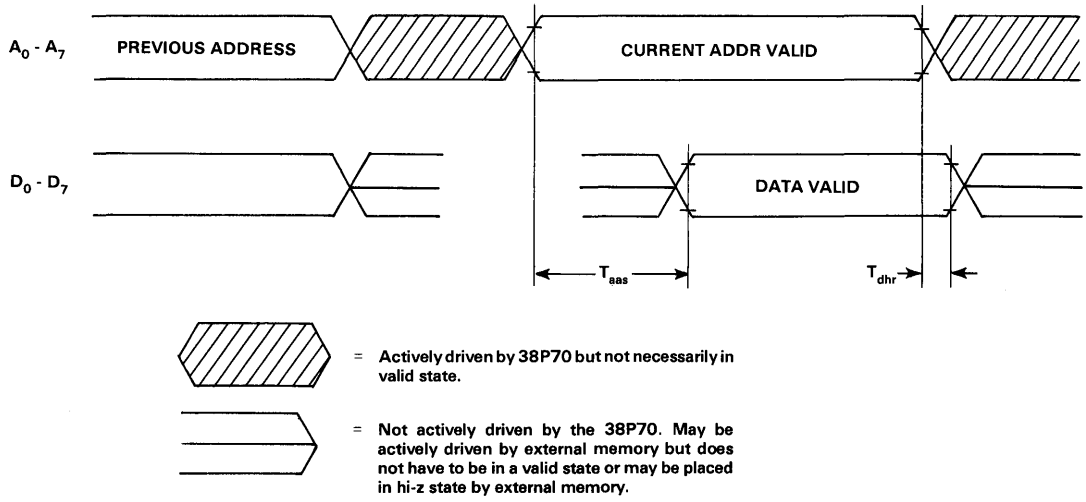
This is the active low fetch status signal which signals that an op-code fetch occurred during that cycle. It is generated for use of the 97500 as a development system component.

It will go low during all op-code fetches whether from internal or external memory.

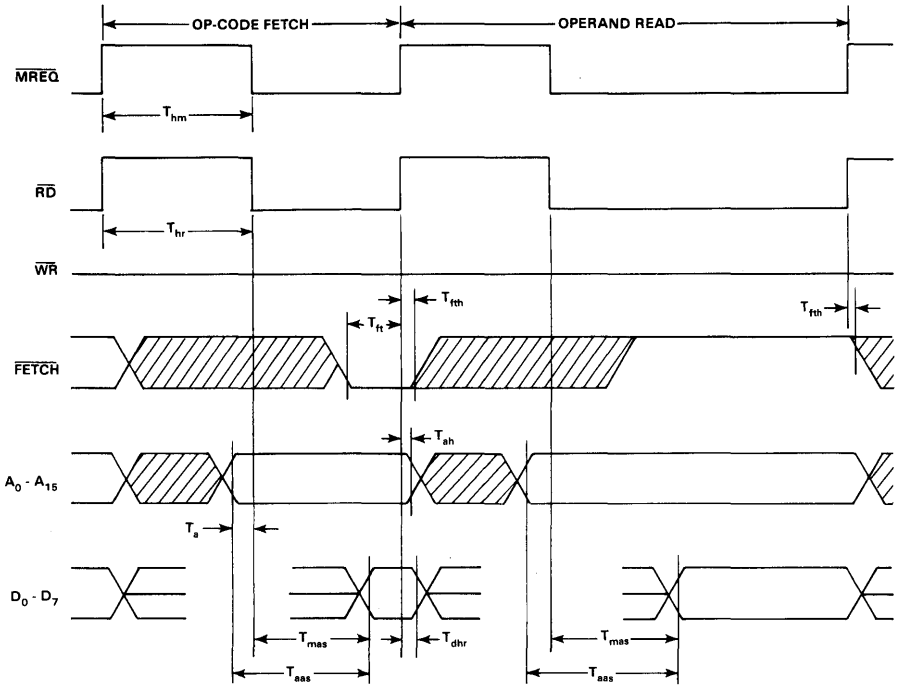
38P70 EXTERNAL MEMORY TIMING

The following Figures show the relative waveforms for the signals used to interface with external memory. The timing parameters are labeled. Their values are given in the A.C. Characteristics section of the Electrical Specifications.

97400 SERIES TIMING
Read Cycle
Figure 8



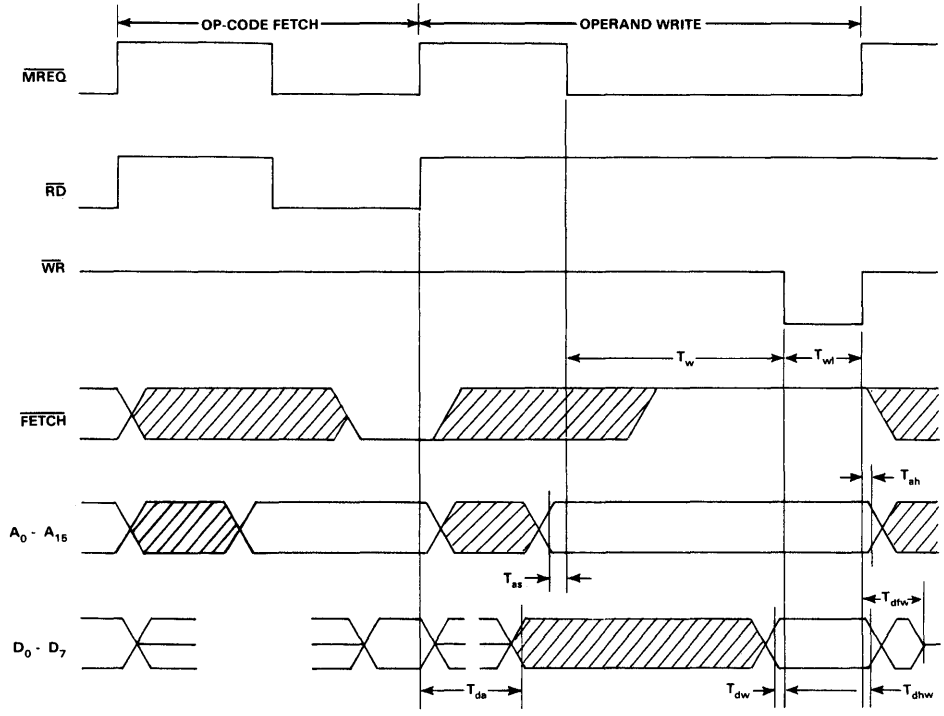
97500 SERIES TIMING
Figure 9



A. OP-CODE AND OPERAND READ FROM EXTERNAL MEMORY

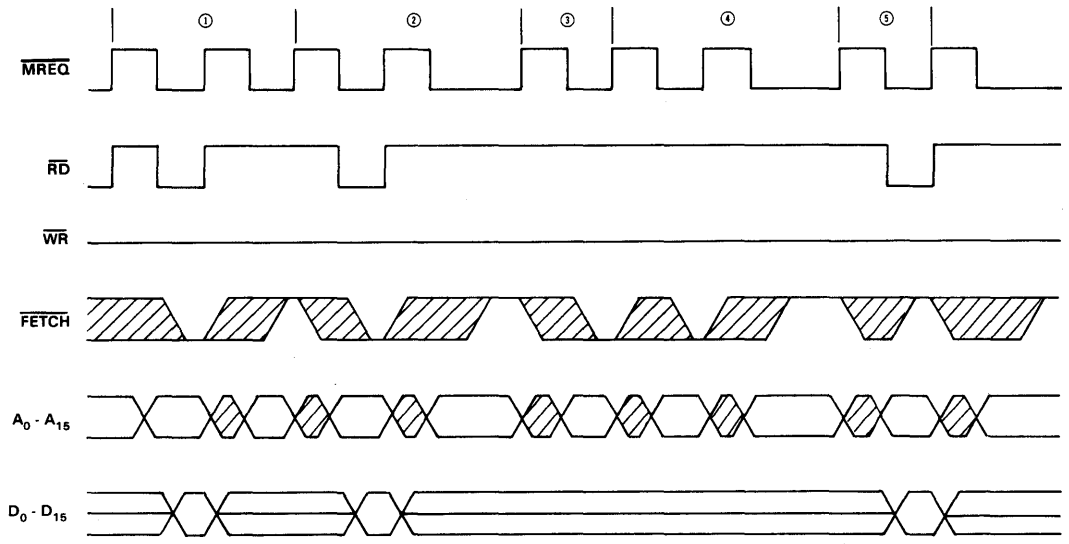
VIII

Figure 9



B. OPERAND WRITE TO EXTERNAL MEMORY

Figure 9



C. EXAMPLES OF VARIOUS CYCLES

① Op-code fetch from external memory followed by an internal cycle (short cycle).
② Op-code fetch from external memory followed by an internal cycle (long cycle) such as an operand read or write internal executable RAM.
③ Op-code fetch from internal executable RAM.
④ Op-code fetch from internal executable RAM followed by a internal cycle (long cycle) such as an operand read or write of internal executable RAM.
⑤ First cycle of an interrupt acknowledge. Had an interrupt not occurred, this would have been an op-code fetch. If it would have been an external op-code fetch, $\overline{RD}$ will still go low but $\overline{FETCH}$ will not indicate a fetch cycle. Externally this would appear to be an operand read except that it occurs in a short cycle and all real operand reads occur in a long cycle.

3870 TIME BASE OPTIONS

The 3870 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 3870 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3870 must be specified at the time when mask ROM devices are ordered. However, the MK38P70 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26 pF capacitor between XTL 1 and GND and an internal 26 pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproduction from system to system is unsurpassed. The 3870 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 11 lists the required crystal parameters for use with the 3870. The Crystal Mode time base configuration is shown in Figure 10.

Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3870, if a single crystal is to provide the time base for more than just a single 3870.

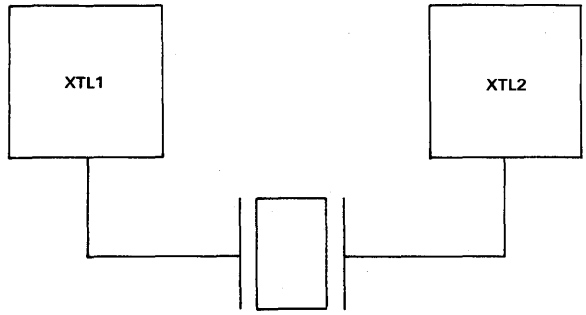
While a ceramic resonator may work with the 3870 crystal oscillator, it was designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3870 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 12. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3870, C_{XTL}, and the stray

CRYSTAL MODE CONNECTION

Figure 10



CRYSTAL PARAMETERS

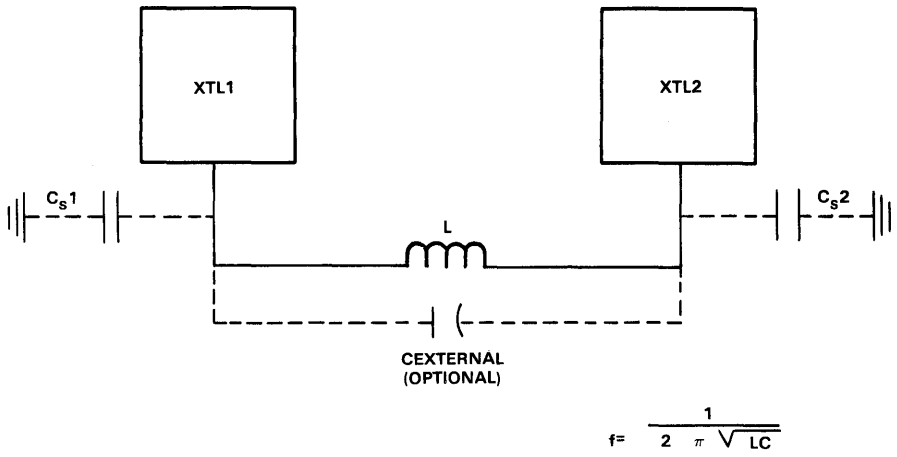
Figure 11

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

LC MODE CONNECTION
Figure 12



capacitances, C_{S1} and C_{S2}. C_{XTL} is the capacitance looking into the internal two port network at XTL1 and XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3870 at XTL1 and XTL2 and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3870.

RC CLOCK CONFIGURATION

The time base for the 3870 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 13. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy, Mostek recommends the use of the Crystal or LC time base configuration. Figure 14 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3870 devices are also shown in the diagram.

The designer must select the RC product such that a frequency of less than 2 MHz is not possible, taking into account the maximum possible RC product and using the minimum curve shown in Figure 14 below. Also, the RC product must not allow a frequency of more than 4 MHz, taking into account the minimum possible R and C and using the Maximum curve shown below. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit owing to switching speed and level at constant temperature and V_{CC} = + or - 5 percent.

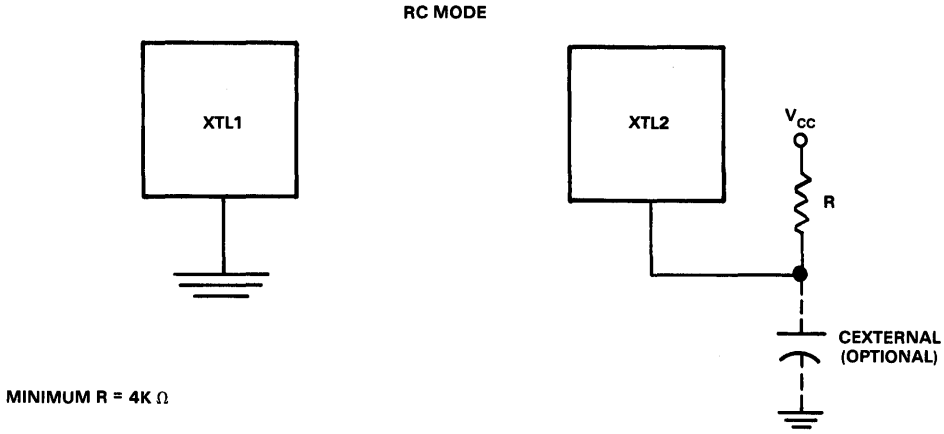
Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, -05	+6 percent to - 9 percent
387X-10, -15	+9 percent to -12 percent

VIII

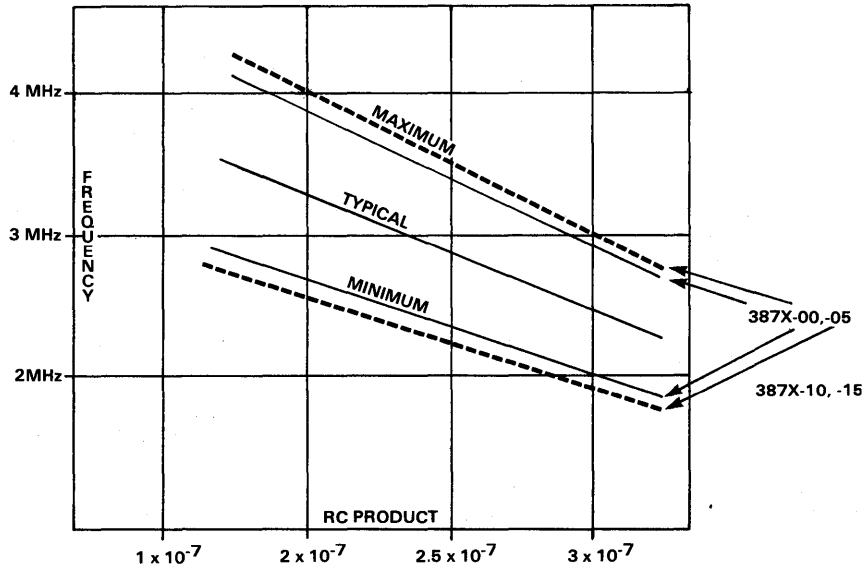
RC MODE CONNECTION
Figure 13



MINIMUM R = 4K Ω

C = 26.5 pF ± 2.6pF + Cexternal

FREQUENCY VS. RC
Figure 14



Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

Typical RC = (R typ) (C external typ + $\frac{\{C_{XTL} \text{ max} + C_{XTL} \text{ min}\}}{2}$)

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Negative Freq. Variation due to RC Components = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$

Total frequency variation due to all factors:

387X-00, -05
= +18 percent plus positive frequency variation due to RC components

387X-10, -15
= +21 percent plus positive frequency variation due to RC components

= -18 percent minus negative frequency variation due to RC components

= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

387X-00, -05
= + 13 percent

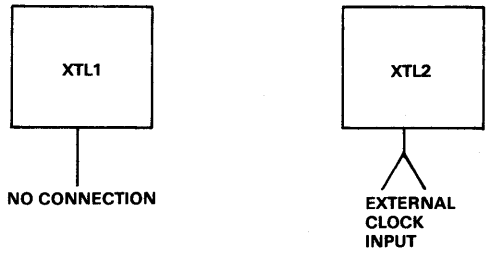
387X-10, -15
= + 16 percent

EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 15. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3870 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION
Figure 15



VIII

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temprature T_A
— 00	+5V ± 10%	0°C - 70°C
— 05	+5V ± 5%	0°C - 70°C
— 10	+5V ± 10%	-40°C - +85°C
— 15	+5V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to +13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O power dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_O	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_O$		$2t_O$			
WRITE	t_W	Internal WRITE Clock period	$4t\Phi$ $6t\Phi$		$4t\Phi$ $6t\Phi$			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	$3t\Phi$ -1000	$3t\Phi$ +250	$3t\Phi$ -1200	$3t\Phi$ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	$8t\Phi$ -250	$12t\Phi$ +250	$8t\Phi$ -300	$12t\Phi$ +300	ns	$\overline{STROBE}$ load= 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	$6t\Phi$ +750		$6t\Phi$ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +0.1		power supply rise time +.15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	$6t\Phi$ +750		$6t\Phi$ +1000		ns	To trigger interrupt
			$2t\Phi$		$2t\Phi$		ns	To trigger timer

AC CHARACTERISTICS FOR MK38P70 Signals brought to top 28 pin socket.
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)
97400 Series (See Note 3)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}	External memory required access time from A_0-A_{11} stable	3tΦ -850		3tΦ -850		ns	C_L A_0-A_{11} = 50 pF

97500 Series (See Note 3)

SIGNAL	SYMBOL	PARAMETER	-00, -05		-10, -15		UNITS	CONDITION
			MIN	MAX	MIN	MAX		
$\overline{MREQ}$	T_{hm}	$\overline{MREQ}$ high time	2tΦ -100		2tΦ -100		ns	Load = 50 pF + 1 TTL load
$\overline{RD}$	T_{hr}	$\overline{RD}$ high time	2tΦ -100		2tΦ -100		ns	Load = 50 pF + 1 TTL load
$\overline{WR}$	T_w	$\overline{WR}$ low from $\overline{MREQ}$ low	3 to -200	3 to +100	3 to -200	3 to +100	ns	Load = 50 pF + 1 TTL load
	T_{wl}	$\overline{WR}$ low time	to -100	to +100	to -100	to +100	ns	
$\overline{FETCH}$	T_{ft}	$\overline{FETCH}$ stable prior to rising $\overline{MREQ}$	650	650	650	650	ns	Load = 50 pF + 1 TTL Load
	T_{fh}	$\overline{FETCH}$ hold time after $\overline{MREQ}$ high	20		20		ns	Load = 20 pF
A_0 - A_{15}	T_a	Address stable prior to $\overline{RD}$ or $\overline{MREQ}$ falling	tΦ -400		tΦ -400		ns	Load = 50 pF + 1 TTL load
	T_{ah}	Address hold time after $\overline{MREQ}$, $\overline{RD}$, or $\overline{WR}$ high	15		15		ns	Load = 20 pF
D_0 - D_7	T_{aas}	External memory required access time from	3tΦ -850		3tΦ -850		ns	
	T_{mas}	External memory required access time from $\overline{MREQ}$ or $\overline{RD}$ low	2tΦ -450		2tΦ -450		ns	
	T_{dhr}	Required data hold time after $\overline{MREQ}$ rising	0		0		ns	
	T_{da}	Data bus active after $\overline{MREQ}$ or $\overline{RD}$ high	tΦ		tΦ			
	T_{dw}	Data stable prior to $\overline{WR}$ falling	5tΦ -2250		5tΦ -2250		ns	Load = 50 pF + 1 TTL load
	T_{dhr}	Data hold after $\overline{WR}$ high	15		15		ns	Load = 20 pF
	T_{dfw}	Data bus delay to float after $\overline{MREQ}$ rising		200		200	ns	

VIII

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS
T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100 mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		85		110	mA	MK3870/10 Outputs Open
			85		110	mA	MK3870/20 Outputs Open
			94		125	mA	MK3870/22 Outputs Open
			100		130	mA	MK3870/40 Outputs Open
			100		130	mA	MK3870/42 Outputs Open
			125		150	mA	MK38P70/X02 No EPROM, Outputs Open

DC CHARACTERISTICS (cont.)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
P_D	Power Dissipation		400		525	mW	MK3870/10 Outputs Open
			400		525	mW	MK3870/20 Outputs Open
			440		575	mW	MK3870/22 Outputs Open
			475		620	mW	MK3870/40 Outputs Open
			475		620	mW	MK3870/42 Outputs Open
			600		750	mW	MK38P70/X02 No EPROM, Outputs Open

VIII

DC CHARACTERISTICS (cont.)

T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	-.3	.8	-.3	7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	$V_{IN}=0.4V$
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	$V_{IN}=13.2V$ $V_{IN}=0.0V$
I_{OH}	Output high current pins with standard pull-up resistor	-100		-89		μA	$V_{OH}=2.4V$
		-30		-25		μA	$V_{OH}=3.9V$
I_{OHDD}	Output high current, direct drive pins	-100 -1.5	 -8.5	-80 -1.3	 -11	μA mA mA	$V_{OH}=2.4V$ $V_{OH}=1.5V$ $V_{OH}=0.7V$
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	V_{OH} = 2.4V
I_{OL}	Output low current	1.8		1.65		mA	$V_{OL}=0.4V$
I_{OLS}	$\overline{STROBE}$ Output Low current	5.0		4.5		mA	$V_{OL}=0.4V$

DC CHARACTERISTICS FOR MK38P70

Signals brought to top 25 pin socket
T_A, V_{CC} within specified range
I/O Power Dissipation ≤ 100 mW (Note 2)

97400, 97500 Series

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITION
V_{IH}	Input high level (D_0 - D_7)	2.0	V_{CC} +.3	2.1	V_{CC} +.3	V	D_0 - D_7 in Hi-z input mode
V_{IL}	Input low level (D_0 - D_7)	V_{SS} -.3	.8	V_{SS} -.3	.7	V	
I_L	Input Leakage (D_0 - D_7)		±10		±15	μA	
V_{OH}	Output high level (all outputs and D_0-D_7 in output mode)	2.4		2.4		V	
V_{OL}	Output low level (all outputs and D_0-D_7 in output mode)		.4		.4	V	
I_{OH}	Output source current (all outputs and D_0-D_7 in output mode)	-100		-90		μA	V_{OH} = 2.4 V
I_{OL}	Output sink current (all outputs and D_0-D_7 in output mode)	1.8		1.65		mA	V_{OL} = .4 V
R_{CC}	Package resistance from device pin 40 to top socket V_{CC} pin(s)					Ω	Pin 28, 27, or 26 when V_{CC}
						Ω	Pin 1 if V_{CC}
						Ω	Pin 23 if V_{CC}
R_{SS}	Package resistance from device pin 20 to top socket V_{SS} pin(s)					Ω	Pin 14 when V_{SS}
						Ω	Pin 2 or 22 when V_{SS}
I_{CC}	Supply current available from top socket V_{CC} pin(s)		-185		-185	mA	ΣI pin 28. 27, 26 when V_{CC}
			-20		-20	mA	Pin 1 if V_{CC}
			-10		-10	mA	Pin 23 if V_{CC}
I_{SS}	Supply current available from top socket V_{SS} pin(s)		190		190	mA	Pin 14 if V_{SS}
			2		2	mA	Pin 2 if V_{SS}
			2		2	mA	Pin 22 if V_{SS}

NOTES:

1. $\overline{\text{RESET}}$ and EXT INT have internal Schmit triggers giving minimum .2 V hysteresis.
2. Power dissipation for I/O pins is calcualted by $\Sigma(V_{CC} - V_{IL})(|I_{IL}|) = \Sigma(V_{CC}-V_{OH})(|I_{OH}|) = \Sigma(V_{OH})(I_{OL})$
3. AC timing for external memory signals on 38P70 are measured from either the .8 or 2.0 volt points as applicable. High means at or above 2.0 volts. Low means at or below .8 volts. Stable means high or low as appropriate. Rising means signal is no longer below .8 volts. Falling means signal is no longer above 2.0 volts. Hold times on outputs assume full rated load on reference signal and 20 pf load on specified signal. For 97400 series, only applicable specification is Taas as no other signals are available to reference to other than A_0-A_{11}.

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0

Error between two Timer reads (Note 2) ..... ± (tpsc + tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... + tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... -5tΦ to - (tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -8tΦ
Load Timer to stop Timer error (Note 1) ..... + tΦ to - (tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... -5t ± to - (tpsc + 8t ±)
Load Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -9tΦ

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) ..... + tΦ to -(tpsc + 2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

Event Counter Mode:

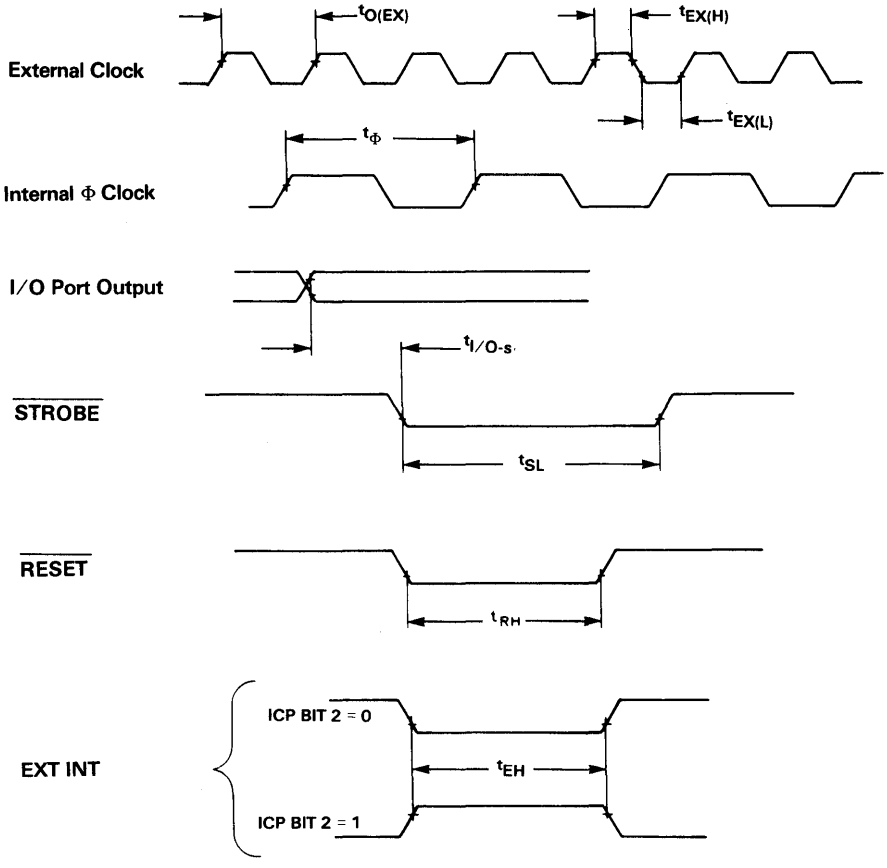
Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

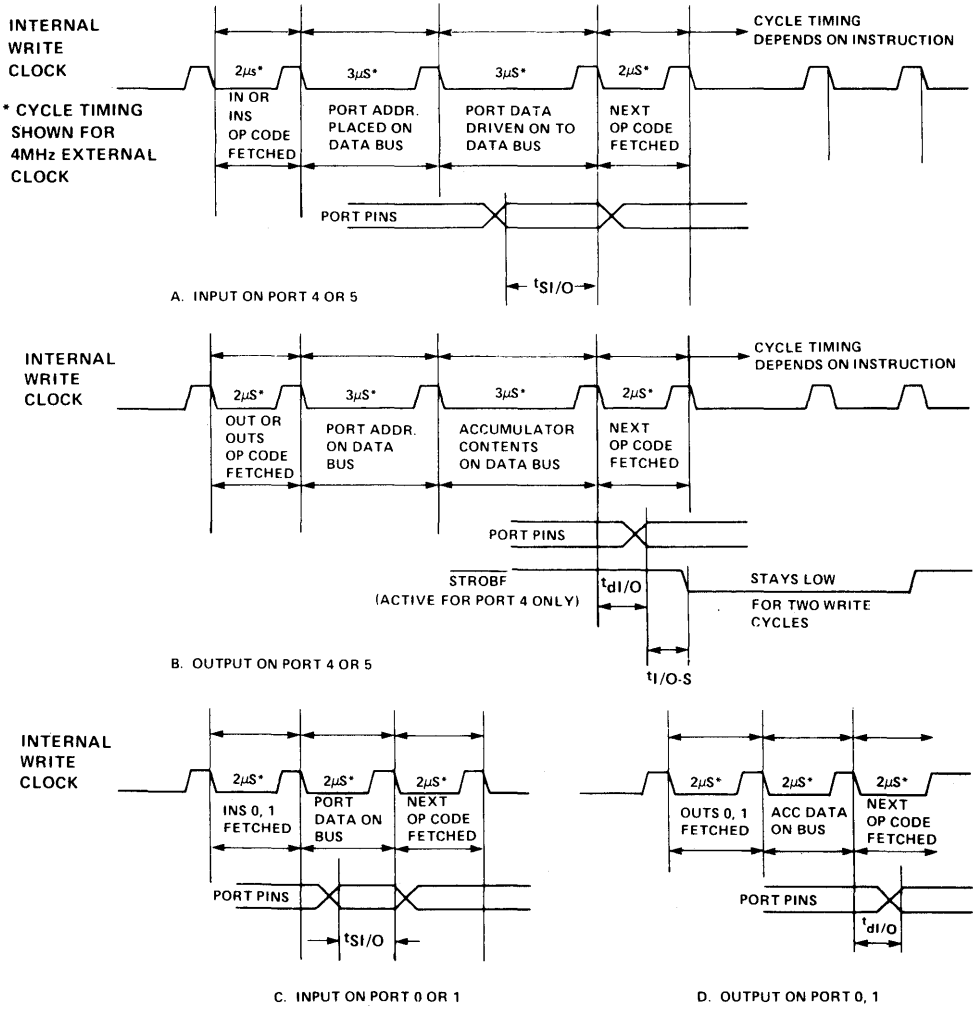
AC TIMING DIAGRAM

Figure 16



Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

INPUT/OUTPUT AC TIMING
Figure 17

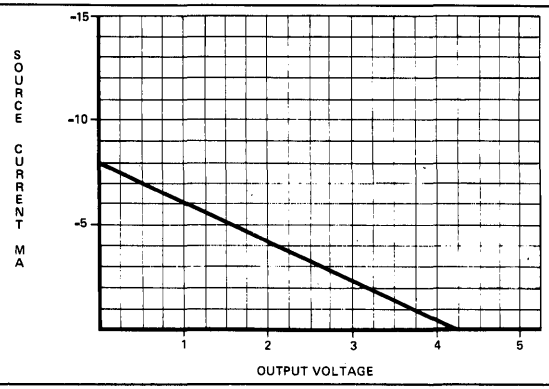


VIII

STROBE SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

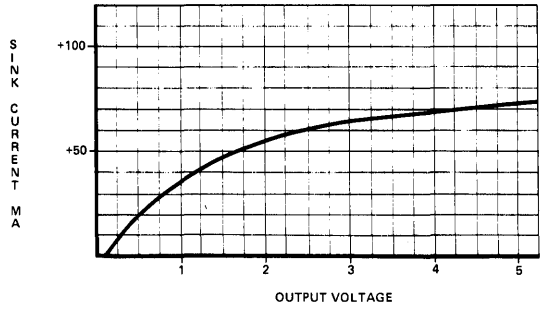
Figure 18



STROBE SINK CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

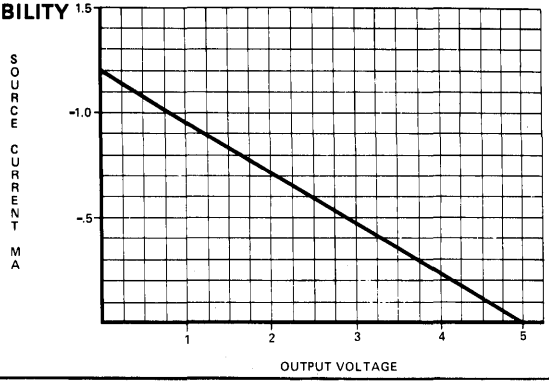
Figure 19



STANDARD I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

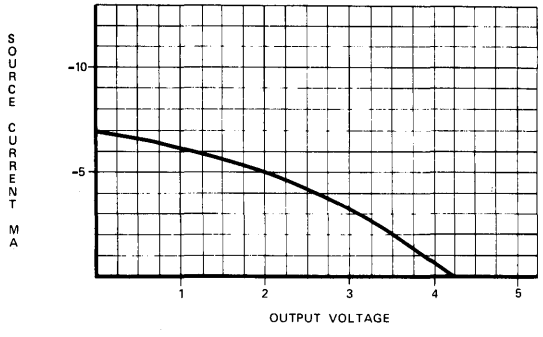
Figure 20



DIRECT DRIVE I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

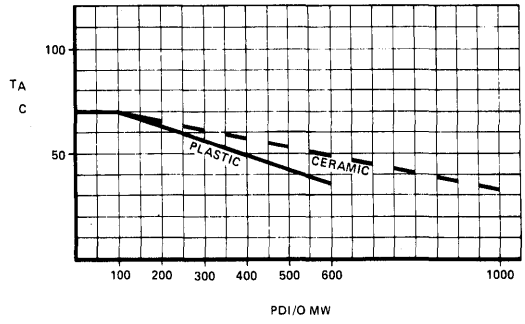
Figure 21



I/O PORT SINK CAPABILITY

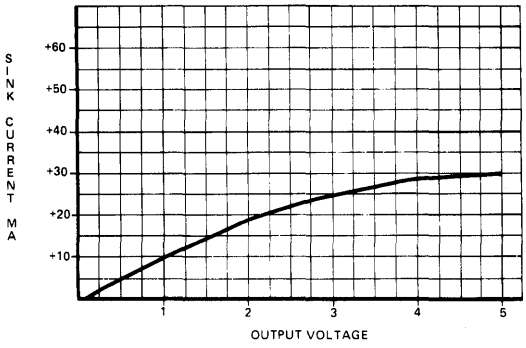
(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

Figure 22



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 23



VIII

ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number. Note: the specific device order number will be used to differentiate between the MK3870/20 with 12-bit Address Registers and the original 3870 with 11-bit Address Register, as mentioned in an earlier section.

GENERIC PART NUMBER

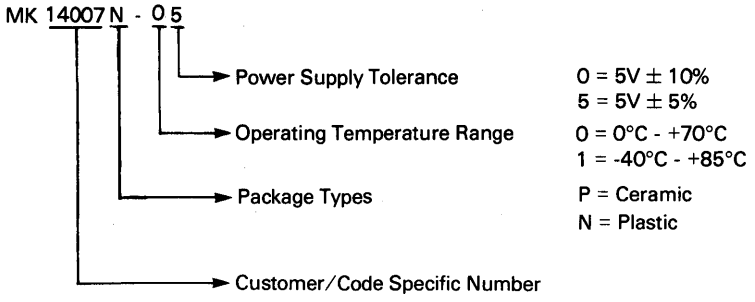
An example of the generic part number is shown below.

MK 3870 /2 2 P- 1 0

Power Supply Tolerance	0 = 5V ± 10% 5 = 5V ± 5%
Operating Temperature Range	0 = 0°C - +70°C 1 = -40°C - +85°C
Package type	P = Ceramic N = Plastic
Executable RAM Designator	0 = None 2 = 64 bytes
ROM Designator	1 = 1K Bytes 2 = 2K bytes 4 = 4K Bytes
Basic Device Type	

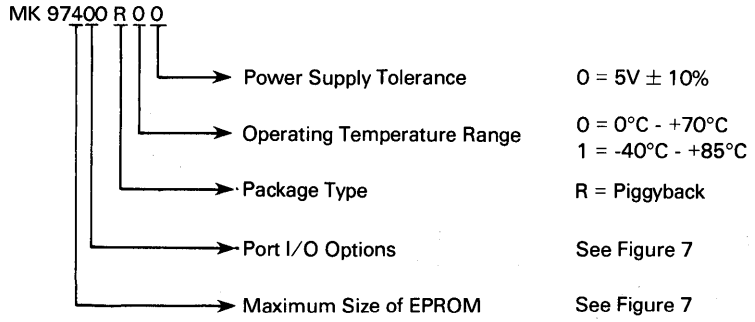
DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

Examples of a 38P70 device order number is shown below.



3870 SINGLE CHIP MICRO FAMILY
MK2870

MK2870 FEATURES

- 28-pin version of the industry standard MK3870 single chip microcomputer
- Available with 1K bytes of mask programmable ROM memory
- 64 bytes scratchpad RAM
- 20 bits TTL compatible I/O
- Programmable binary timer
  Interval timer mode
  Pulse width measurement mode
  Event counter mode
- External interrupt input
- Crystal, LC, RC, or external time base options
- Low power (275 mW typ.)
- Single +5 volt supply

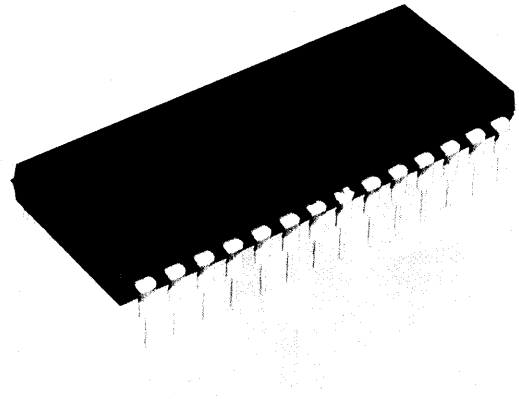
GENERAL DESCRIPTION

The MK2870 is the 28-pin version of the industry standard Mostek MK3870 single chip microcomputer. It is offered as a low cost device which can be used in those applications that do not require the entire I/O capability of the 40 pin MK3870. The compact 28-pin package makes the MK2870 ideally suited for applications where PC board space is a premium.

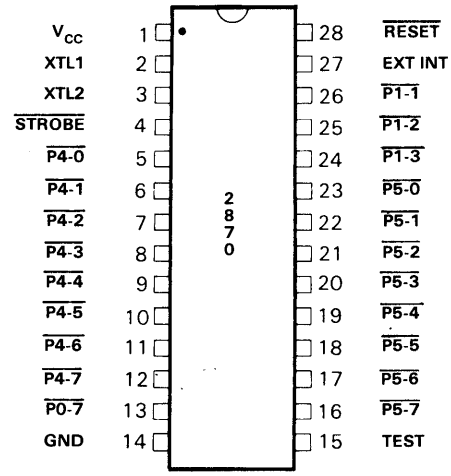
The MK2870 can execute more than 70 instructions, and is completely software compatible with the rest of the devices in the 3870 family. The MK2870 features 1K bytes of ROM. The MK2870 also features 64 bytes of scratchpad RAM, a programmable binary timer, and 20 bits of I/O.

The programmable binary timer operates by itself in the interval timer mode or in conjunction with the external interrupt input in the pulse width measurement and the event counter modes of operation. Two sources of vectored, prioritized interrupt are provided with the binary timer and the external interrupt input. The user has the option of specifying one of four clock sources for the MK2870:

MK2870
Figure 1



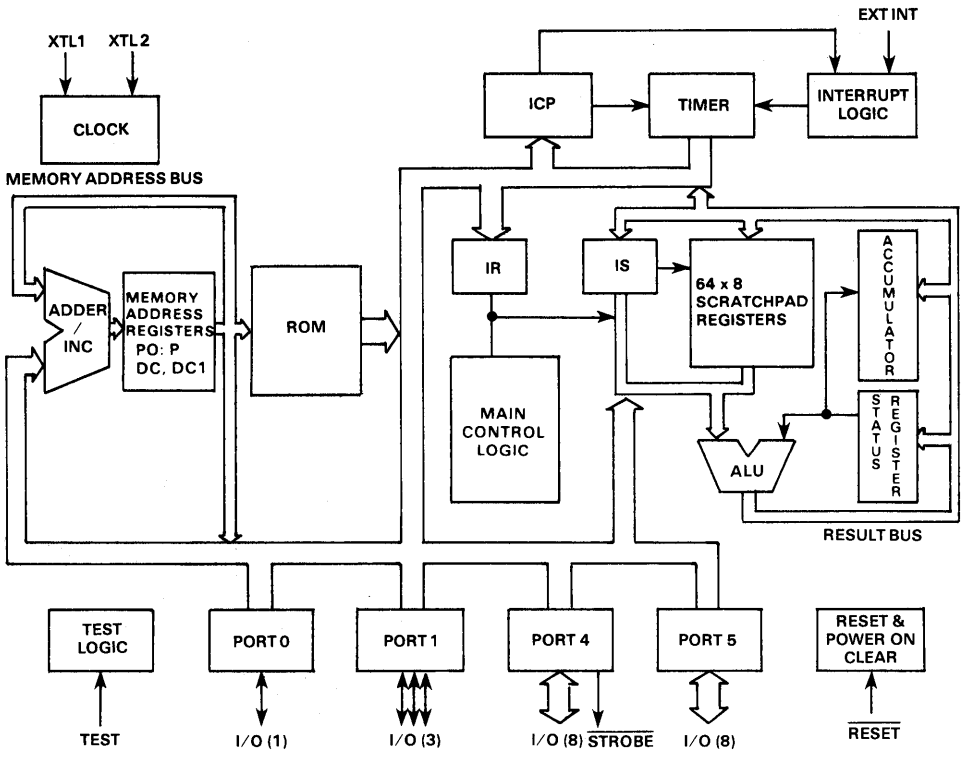
MK2870 PIN CONNECTIONS
Figure 2



VIII

MK2870 BLOCK DIAGRAM

Figure 3



Crystal, LC, RC, or external clock. In addition, the user can specify either a ±10% power supply tolerance or a ±5% power supply tolerance.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}7}$	I/O Port 0 Bit 7	Bidirectional
$\overline{P1\text{-}1}$ -- $\overline{P1\text{-}3}$	I/O Port 1 Bits 1-3	Bidirectional
$\overline{P4\text{-}0}$ -- $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ -- $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}7}$, $\overline{P1\text{-}1}$--$\overline{P1\text{-}3}$, $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$--$\overline{P5\text{-}7}$ are 20 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$--$\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ may be used to externally reset the MK2870. When pulled low the MK2870 will reset. When then allowed to go high the MK2870 will begin program execution at program location H '000'.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering a mask ROM MK2870.

TEST is an input, used only in testing the MK2870. For normal circuit functionality this pin may be left unconnected, but it is recommended that TEST be grounded.

V_{CC} is the power supply input (single +5 V).

MK2870 ARCHITECTURE

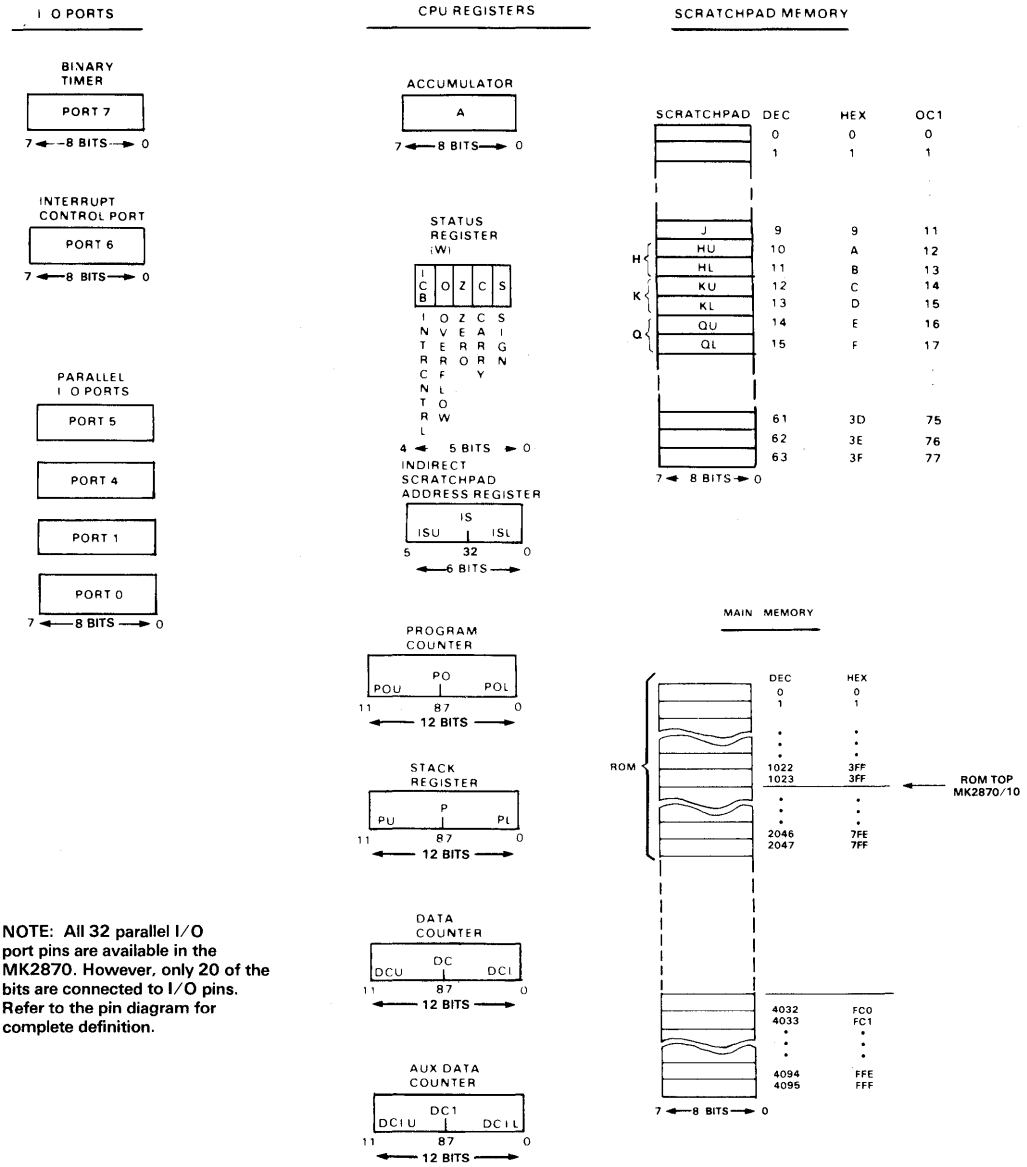
The basic functional elements of the MK2870 are shown in Figure 3. A programming model is shown in Figure 4. The MK2870 is instruction set compatible. The unique features of the MK2870 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features.

MK2870 MAIN MEMORY

There are four address registers used to access main memory. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions or immediate operands. The Stack Register is used to save the contents of the Program Counter during an interrupt or subroutine call. Thus, the Stack Register

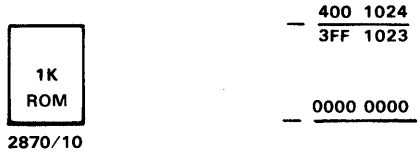
MK2870 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 4



NOTE: All 32 parallel I/O port pins are available in the MK2870. However, only 20 of the bits are connected to I/O pins. Refer to the pin diagram for complete definition.

MK2870 MAIN MEMORY SIZE AND TYPE
Figure 5



This device contains 64 bytes of scratchpad RAM.

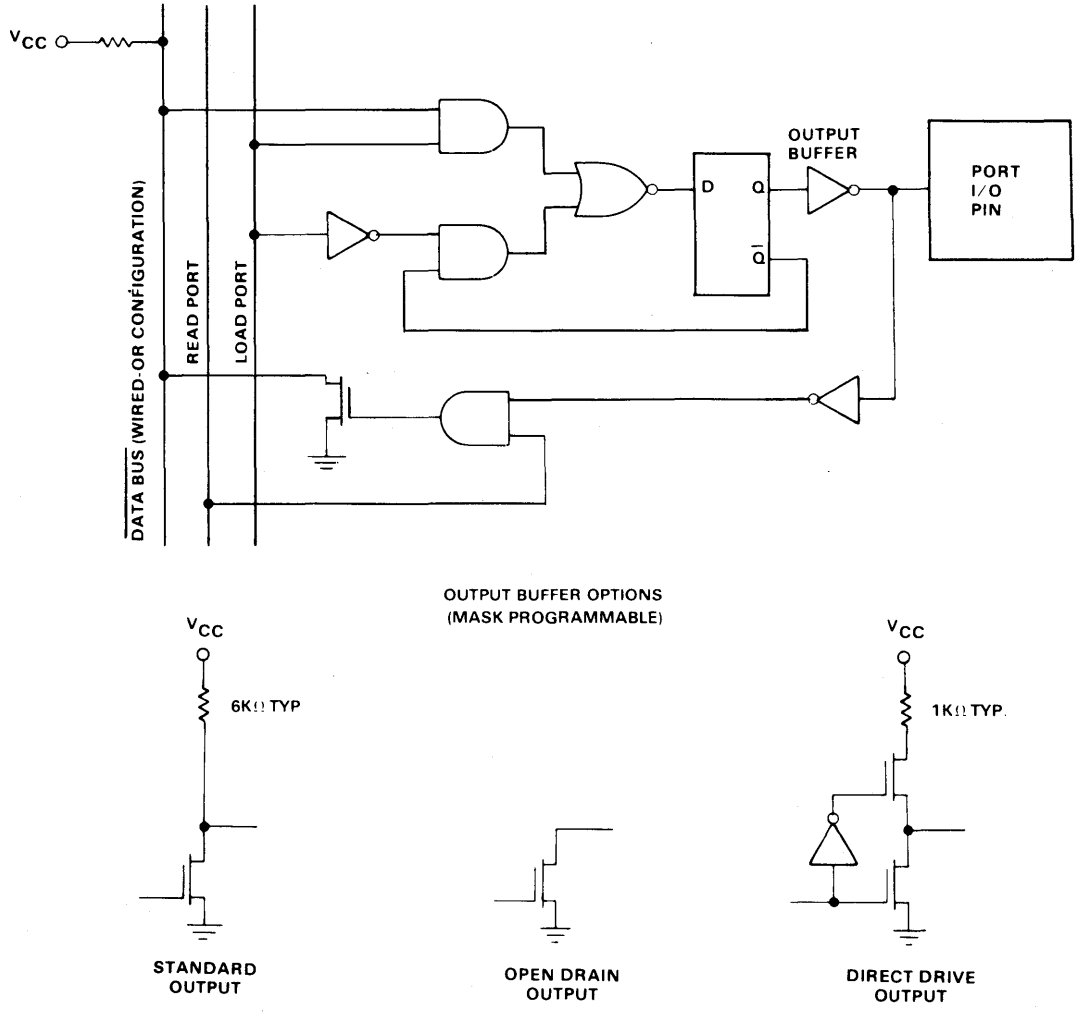
NOTE:

Data derived from addressing any locations other than those within a part's specified ROM space or RAM space (if any) is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size (Decimal)
MK2870/10	64 bytes	12 bits	1024 bytes	0 bytes

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 6



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6K Ω (typical) pull-up or may have no pull-up (mask programmable).

When Direct Drive option is selected, it should be used as an Output only (not as an input).

contains the return address at which processing is to resume upon completion of the subroutine or interrupt routine. The Data Counter is used to address data tables. This register is auto-incrementing. Of the two data counters, only Data Counter (DC), can access the ROM. However, the SDC instruction allows the Data Counter and Auxiliary Data Counter to be exchanged.

Figure 5 shows the amounts of ROM and executable RAM in the MK2870/10 pin configuration.

I/O PORTS

The MK2870 provides four, 8 bit bidirectional Input/Output ports. These are ports 0, 1, 4, 5. However, only 20 of the bits are connected to I/O pins. The remaining bits are storage elements. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pin are covered in the 3870 Family Technical Manual. The schematic of an I/O pin and available output drive options are shown in Figure 6.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK2870 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may also be used as an input strobe to Port 4 after completing the input operation.

To use a port pin as an input, the large transistor which pulls the pin to V_{SS} must be turned off. This is accomplished by writing a '0' to that bit of the port. This applies to Ports 0, 1, 4, and 5 only.

MK2870 TIME BASE OPTIONS

The MK2870 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the MK2870 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK2870 must be specified at the time when mask ROM devices are ordered.

The specifications for the four configurations are given in the following text. There is an internal capacitor between XTL 1 and GND and an internal capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all clock modes the external time base frequency is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

The use of a crystal as the time base is highly recommended as the frequency stability and reproducability from system to system is unsurpassed. The MK2870 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 8 lists the required crystal parameters for use with the MK2870. The Crystal Mode time base configuration is shown in Figure 7.

Through careful buffering of the XTL 1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and the waveform from that oscillator be buffered and supplied to all devices, including the MK2870, in the event that a single crystal is to provide the time base for more than just a single MK2870.

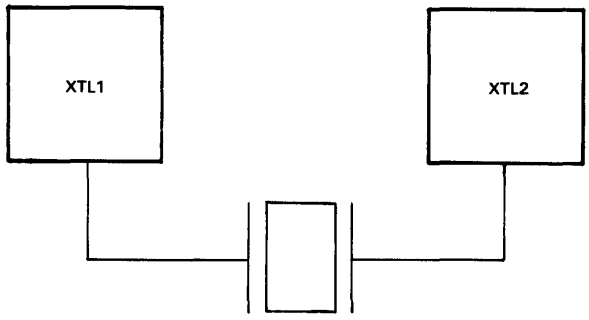
While a ceramic resonator may work with the MK2870 crystal oscillator, it was not designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the MK2870 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 9. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must be a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the MK2870 C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the capacitance looking into the internal two port network at XTL 1 and XTL 2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL 1 to ground and from XTL 2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

CRYSTAL MODE CONNECTION

Figure 7



NOTE: Lead lengths from the crystal to the 2870 pins should be kept reasonably short to reduce stray capacitance load.

CRYSTAL PARAMETERS

Figure 8

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_s) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

*This holder may not be available at frequencies near the lower end of this range.

VIII

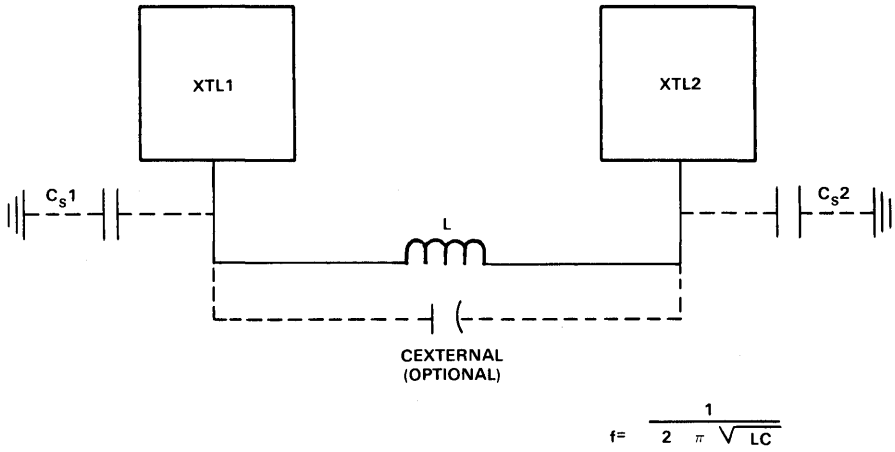
Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the MK2870 at XTL 1 and XTL 2 and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the MK2870.

RC CLOCK CONFIGURATION

The time base for the MK2870 may be provided from an RC network tied to the XTL 2 pin, when XTL 1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 10. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy Mostek recommends the use of the Crystal or LC time base configuration. Figure 11 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of MK2870 devices are also shown in the diagram.

LC MODE CONNECTION

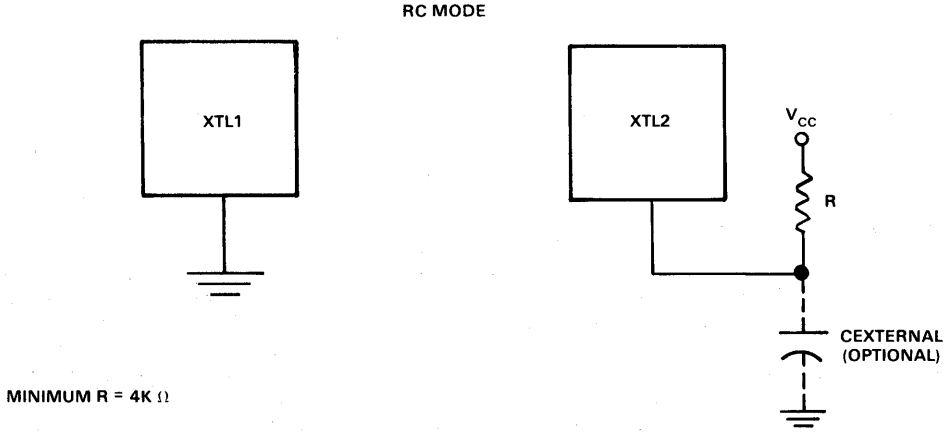
Figure 9



NOTE: The LC options uses the same mask option as the crystal option.

RC MODE CONNECTION

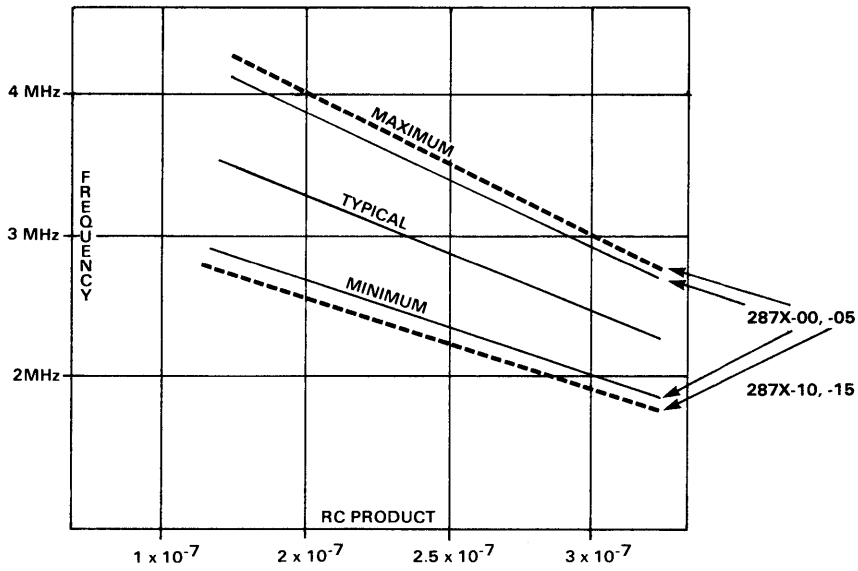
Figure 10



MINIMUM R = 4K Ω

C = 26.5 pF ± 2.6pF + Cexternal

FREQUENCY VS. RC
Figure 11



VIII

The designer must select the RC product such that a frequency of less than 2 MHz is not possible taking into account the maximum possible RC product and using the minimum curve shown in Figure 11. Also, the RC product must not allow a frequency of more than 4 MHz taking into account the minimum possible R and C and using the Maximum curve shown below. Temperature induced variations in the external components should be considered in calculating the RC Product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or -5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5 V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
287X-00, -05	+6 percent to - 9 percent
287X-10, -15	+9 percent to -12 percent

Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

Typical RC = (R typ) (C external typ + $\{\frac{C_{XTL} \text{ max} + C_{XTL} \text{ min}}{2}\}$)

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Netative Freq. Variation due to RC Components = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$

Total frequency variation due to all factors:

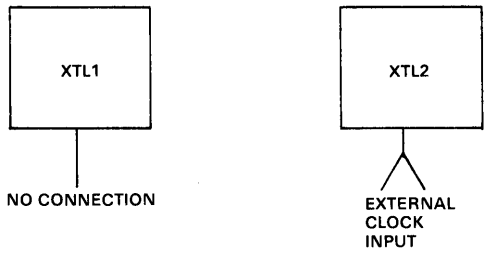
287X-00, -05	287X-10, -15
+18 percent plus positive frequency variation due to RC components	= +21 percent plus positive frequency variation due to RC components
= -18 percent minus negative frequency variation due to RC components	= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5 V V_{CC}, 25 C

287X-00, -05	287X-10, -15
= + 13 percent	= +16 percent

EXTERNAL MODE CONNECTION

Figure 12



EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 12. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section for input capacitance.

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
— 00	+5 V ±10%	0°C - 70°C
— 05	+5 V ± 5%	0°C - 70°C
— 10	+5 V ± 10%	-40°C - +85°C
— 15	+5 V ± 5%	-40°C - +85°C

See Ordering Information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0 V to +7 V	-1.0 V to + 7 C
Voltage on TEST with Respect to Ground	-1.0 V to +9 V	-1.0 V to +9 V
Voltage on Open Drain Pins With Respect to Ground	-1.0 V to +13.5 V	-1.0 V to +13.5 V
Power Dissipation	1.5 W	1.5 W
Power Dissipation by any one I/O pin	60 mW	60 mW
Power Dissipation by all I/O pins	600 mW	600 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O power dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	NOTES
XTL 1 XTL 2	t_o $t_{ex(H)}$ $t_{ex(L)}$	Time Base Period, all clock modes External clock pulse width high External clock pulse width low	250 90 100	500 400 400	250 100 110	500 390 390	ns ns ns	4 MHz - 2 MHz
Φ	t_Φ	Internal Φ clock	$2t_0$		$2t_0$			
WRITE	t_w	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50 pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50 pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load = 50 pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time + 0.1		power supply rise time + .15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

VIII

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100 mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	DEVICE
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		85		110	mA	MK2870/10 Outputs Open
P_D	Power Dissipation		400		525	mW	MK2870/10 Outputs Open
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard pull-up
		2.0	13.2	2.0	13.2	V	Open drain (1)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	Standard pull-up
		2.0	13.2	2.2	13.2	V	No Pull-up
V_{IL}	Input low level	-.3	.8	-.3	.7	V	(1)
I_{IL}	Input low current, all pins with standard pull-up resistor		-1.6		-1.9	mA	V_{IN} = 0.4 V
I_L	Input leakage current, open drain pins, and inputs with no pull-up resistor		+10 -5		+18 -8	μA μA	V_{OH} = 13.2 V V_{IN} = 0.0 V
I_{OH}	Output high current pins with standard pull-up resistor	-100 -30		-89 -25		μA μA	V_{OH} = 2.4 V V_{OH} = 3.9 V

DC CHARACTERISTICS (cont.)

T_A, V_{CC} within specified operating range, I/O power dissipation ≥ 100 mW (Note 2)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITIONS
I_{OHDD}	Output high current, direct drive pins	-100 -1.5	 -8.5	-80 -1.3	 -11	μA mA mA	V_{OH} = 2.4 V V_{OH} = 1.5 V V_{OH} = 0.7 V
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	V_{OH} = 2.4 V
I_{OL}	Output low current	1.8		1.65		mA	V_{OL} = 0.4 V
I_{OLS}	$\overline{STROBE}$ Output Low current	5.0		4.5		mA	V_{OL} = 0.4 V

TIMER AC CHARACTERISTICS

Definitions:
Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ±(tpsc + tΦ)
Start Timer to stop Timer error (Notes 1, 4) ..... +tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2) ..... -5t Φ to - (tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -8 tΦ
Load Timer to stop Timer error (Note 1) ..... + tΦ to - (tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2) ..... -5tΦ ± to - (tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3) ..... -2tΦ to -9tΦ

Pulse Width Measurement Mode:

Measurement accuracy (Note 4) ..... + tΦ to - (tpsc + 2tΦ)
Minimum pulse width of EXT INT pin 2tΦ

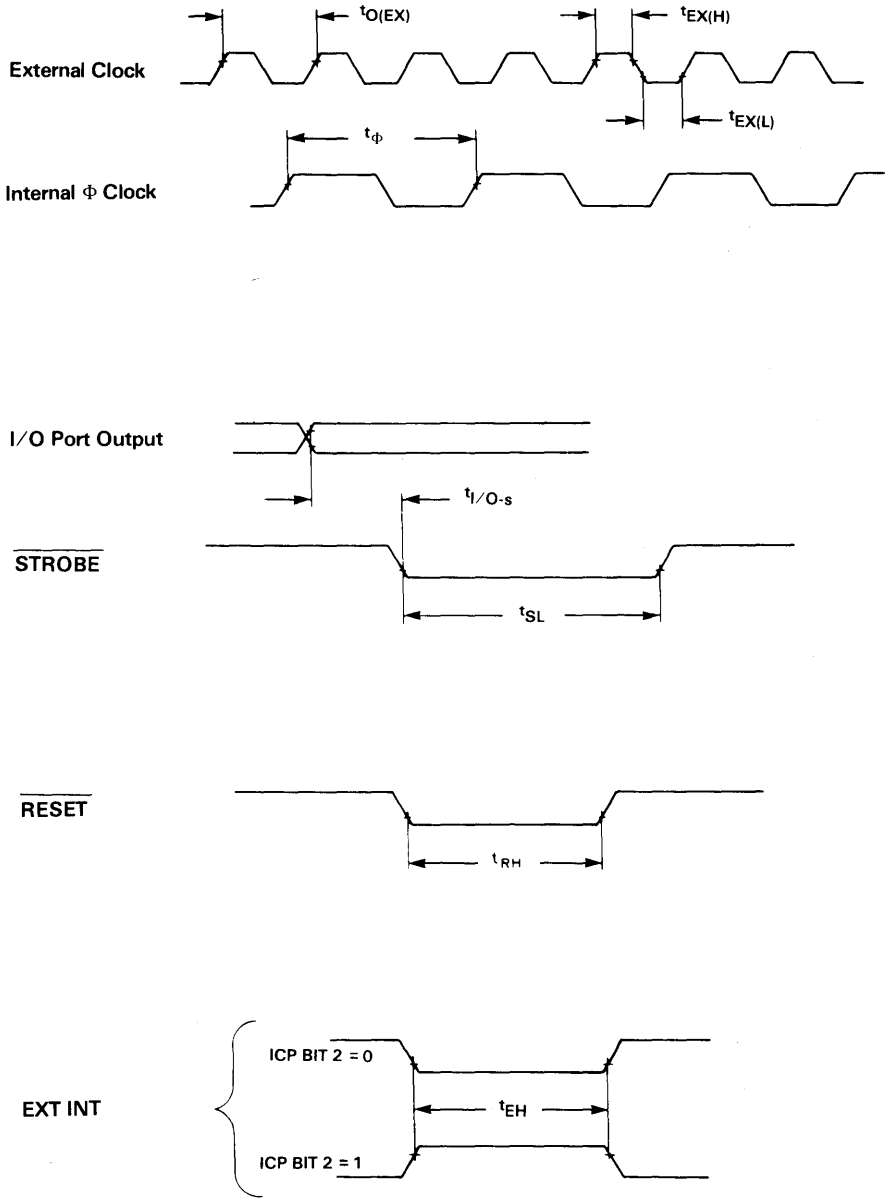
Event Counter Mode:

Minimum active time of EXT INT pin 2tΦ
Minimum inactive time of EXT INT pin 2tΦ

NOTES:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

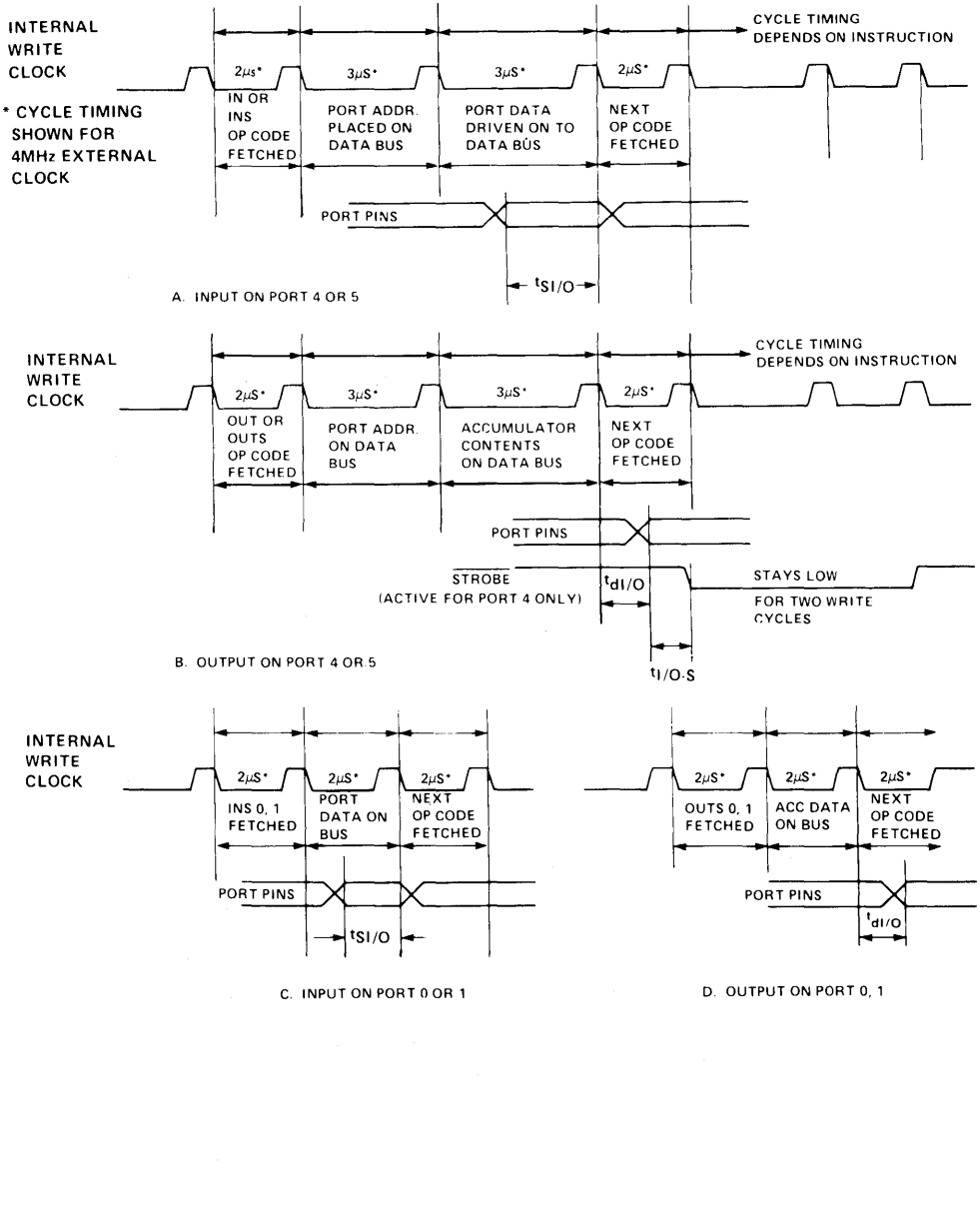
AC TIMING DIAGRAM
Figure 13



Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

INPUT/OUTPUT AC TIMING

Figure 14

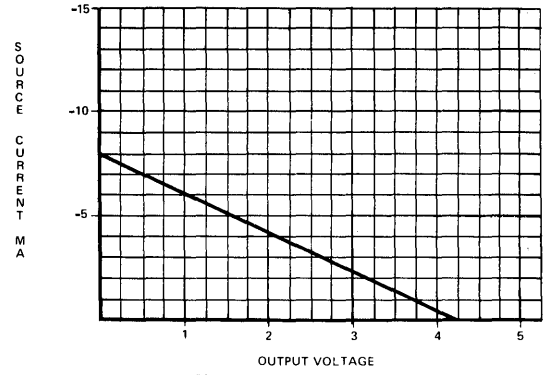


VIII

STROBE SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

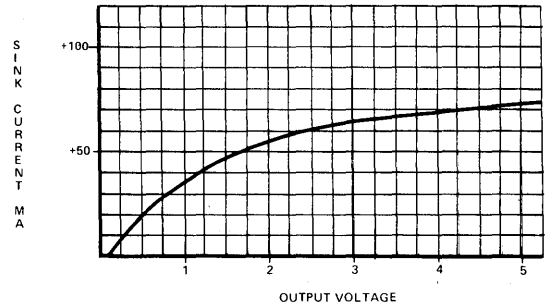
Figure 15



STROBE SINK CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

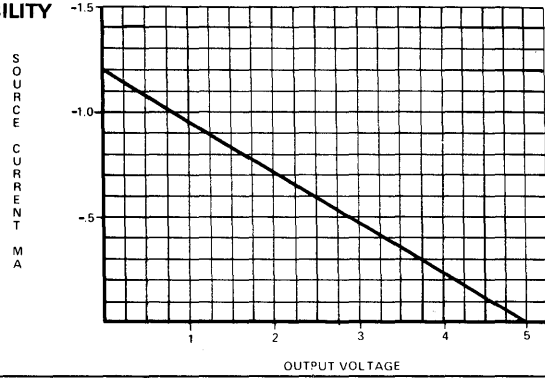
Figure 16



STANDARD I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

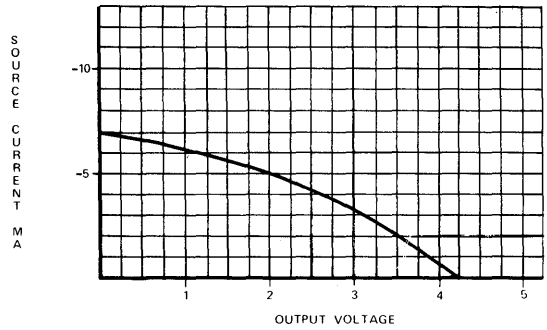
Figure 17



DIRECT DRIVE I/O PORT SOURCE CAPABILITY

(TYPICAL AT V_{CC} = 5 V, T_A = 25°C)

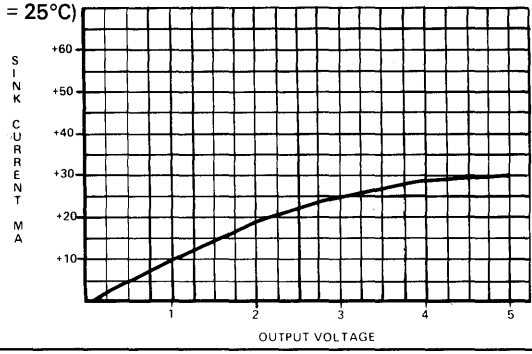
Figure 18



I/O PORT SINK CAPABILITY

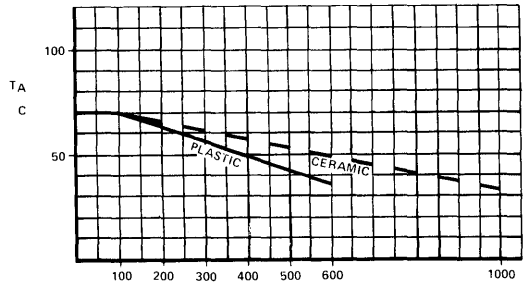
(TYPICAL AT V_{CC} = 5 V, $T_{A'}$ = 25°C)

Figure 19



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 20



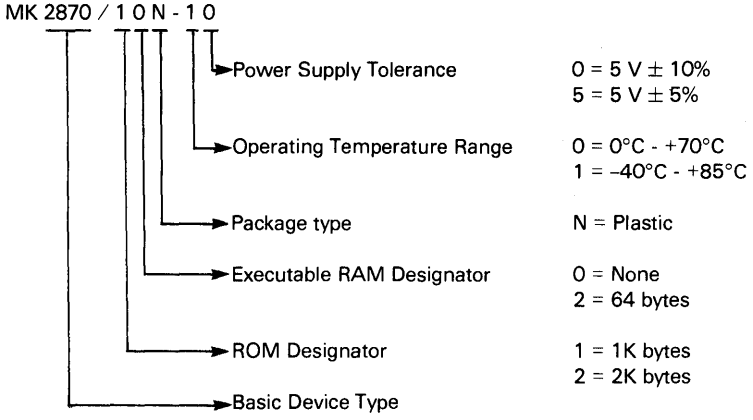
VIII

ORDERING INFORMATION

There are two types of part numbers for the 2870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

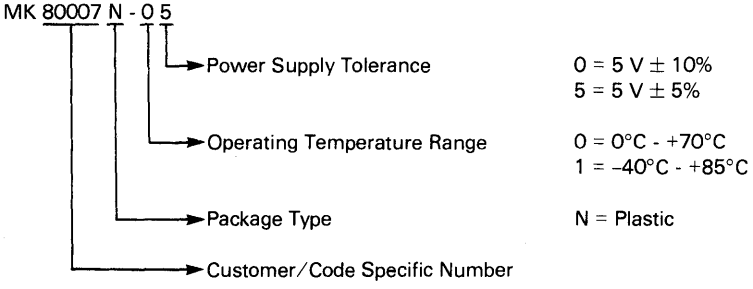
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

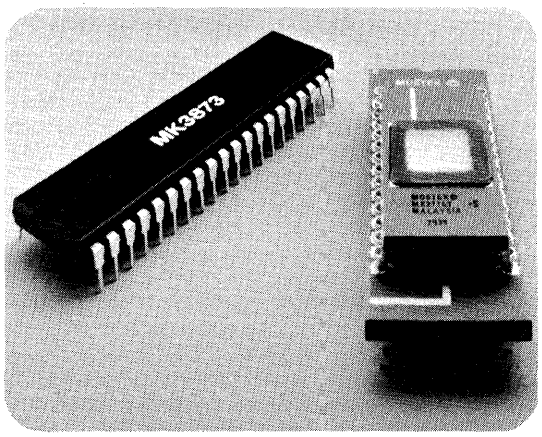
3870 SINGLE CHIP MICRO FAMILY
MK3873 AND MK38P73

MK3873 FEATURES

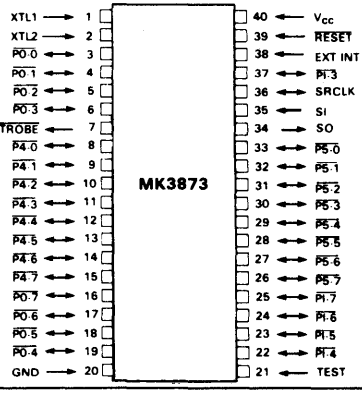
- ☐ Available with 1K byte mask programmable ROM
- ☐ Software compatible with 3870 instruction set
- ☐ 64 byte scratchpad RAM
- ☐ Available with 64 byte Executable RAM
- ☐ 29 bits (4 ports) TTL compatible parallel I/O
- ☐ Serial Input/Output port
  - External or Internal Serial Port Clock
  - Transmit and Receive registers double buffered
  - Internal Baud rate generator
  - Synchronous or Asynchronous serial I/O
  - Data rates to 9600 bits per second (ASYNC)
  - I/O pins dedicated as SERIAL IN, SERIAL OUT, and SERIAL CLOCK
  - Variable duty cycle waveform generation
- ☐ Vectored interrupts
- ☐ Programmable binary timer
  - Internal timer mode
  - Pulse width measurement mode
  - Event counter mode
- ☐ External Interrupt
- ☐ Crystal, LC, RC or external time base options available
- ☐ Low power (325 mW typ.)
- ☐ Single +5V power supply
- ☐ Pinout compatible with the 3870 Family members

MK38P73 FEATURES

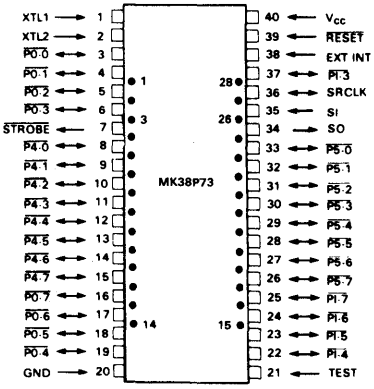
- ☐ EPROM version of MK3873
- ☐ Piggyback PROM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3873
- ☐ In-Socket emulation of MK3873



MK3873 PIN CONNECTIONS



MK38P73 PIN CONNECTIONS



VIII

GENERAL DESCRIPTION

The MK3873 single chip microcomputer introduces a major addition to the 3870 microcomputer family, a serial input/output port. This serial port is capable of either synchronous or asynchronous serial data transfers. The heart of the serial port is a 16-bit Shift Register that is double-buffered on transmit and receive. The Shift Register clock source can be either the internal baud rate generator or an external clock. An end-of-word vectored interrupt is generated in either transmit or receive mode so that the CPU overhead is only at the word rate and not at the serial bit rate. This serial channel can be used to provide a low-cost data channel for communicating between 3873 microcomputers or between a 3873 and another host computer. The serial port is also very flexible so that it could be used for other purposes such as an interface to external serial logic or serial memory devices.

The MK3873 retains commonality with the 3870 family of single chip microcomputers. It has 2048 bytes of mask ROM for program storage, and 64 bytes of scratchpad random-access memory. Certain versions also include up to 64 bytes of Executable RAM. Also, the 3870's sophisticated programmable binary timer is included and provides for system flexibility by operating in 3 different modes. The MK3873 has a large number of parallel I/O lines available to the user. Twenty nine pins of the MK3873 are dedicated to parallel I/O. In addition, three pins are dedicated to the serial I/O port. These pins provide input, output, and clock for the serial port. The serial clock pin can be driven externally or programmed to provide a 50% duty cycle TTL compatible serial clock. No additional CPU instructions are necessary for use with the serial port. Thus, the MK3873 is instruction set compatible with the rest of the 3870 family.

The MK38P73 microcomputer is the PROM based version of the MK3873 single-chip microcomputer. The MK38P73 is called the Piggyback PROM (P-PROM)™ microcomputer because of a new packaging concept. This concept allows a 24 or 28 pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can then be removed and reprogrammed as required with a standard PROM programmer. The MK38P73 retains exactly the same pinout and architectural features as other members of the MK3873 Family. The MK38P73 is discussed in more detail in a later section of this document.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}0}$ - $\overline{P0\text{-}7}$, $\overline{P1\text{-}3}$ - $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$, $\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ are 29 bidirectional I/O lines which can either be used as TTL compatible inputs or latch outputs.

SI - SERIAL IN is a TTL compatible Schmitt Trigger input pin for either serial synchronous or asynchronous data.

SO - SERIAL OUT is an output line for either serial synchronous or asynchronous data.

SRCLK is the clock for the serial port operations. It can be configured by software to be an input or output depending upon whether an internal baud rate or external clock is desired. It has a Schmitt trigger input and can be used to drive up to 3 TTL loads.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin which is normally high provides a single low pulse after valid data is present on the $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ pins during an output instruction. $\overline{STROBE}$ can be used to drive up to 3 TTL loads.

$\overline{RESET}$ may be used to externally reset the MK3873. When pulled low the MK3873 will reset. When allowed to go high the MK3873 will begin program execution at program location H'000'.

PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}0}$, $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}3}$ - $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
SI	Serial Input	Input
SO	Serial Output	Output
SRCLK	Serial Clock	Bidirectional
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

EXT INT is the external interrupt input. Its active state is software programmable as described in the 3870 Family Technical Manual. This input is also used in conjunction with the timer for pulse width measurement and event counting.

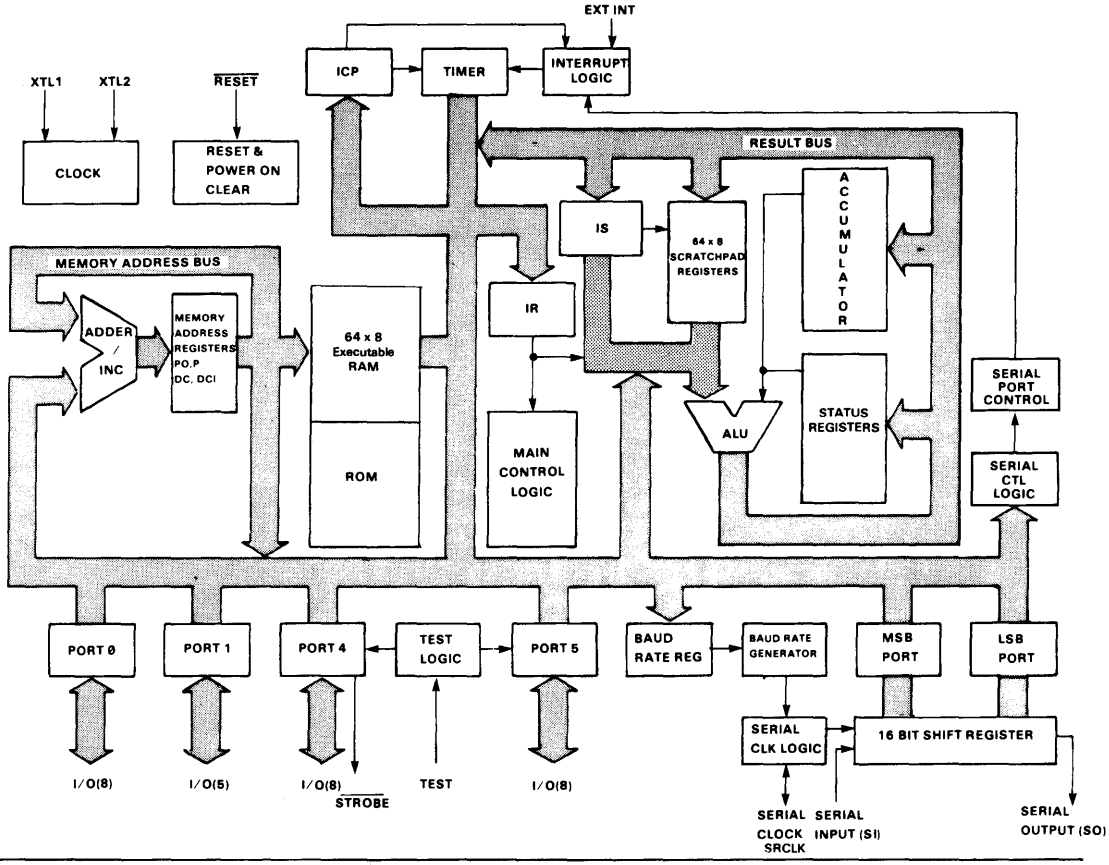
XTL 1 and XTL 2 are the time base inputs (2 MHz to 4 MHz) to which a crystal, LC network, RC network, or an external single-phase clock may be connected. The time base mode must be specified when submitting an order for a mask ROM MK3873. The MK38P73 will operate with any of the four configurations.

MK3873 ARCHITECTURE

The architecture of the MK3873 is identical to that of the rest of the devices in the 3870 family, with the exception of the serial port logic. The serial port logic is shown in the block diagram of the MK3873 (Figure 1). Addressing of the serial port logic is accomplished through I/O instructions. Operation and programming of the serial port is thoroughly discusssed below. A programming-model of the MK3873 is shown in Figure 2. For a more complete discussion of the 3870 family architecture, the user is referred to the 3870 Family Technical Manual.

MK3873 BLOCK DIAGRAM

Figure 1



MAIN MEMORY

The main memory section on the MK3873 consists of a combination of ROM and executable RAM.

There are four registers associated with the main memory section. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC), and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions during program execution. P is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine. The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data counters, only DC can access memory directly. However, the XDC instruction allows DC and DC1 to be exchanged.

The length of the PO, P, DC, and DC1 registers for the MK3873/22 device is listed in the table shown in Figure 3. The graph and table in Figure 3 also shows the amounts of ROM and executable RAM.

EXECUTABLE RAM

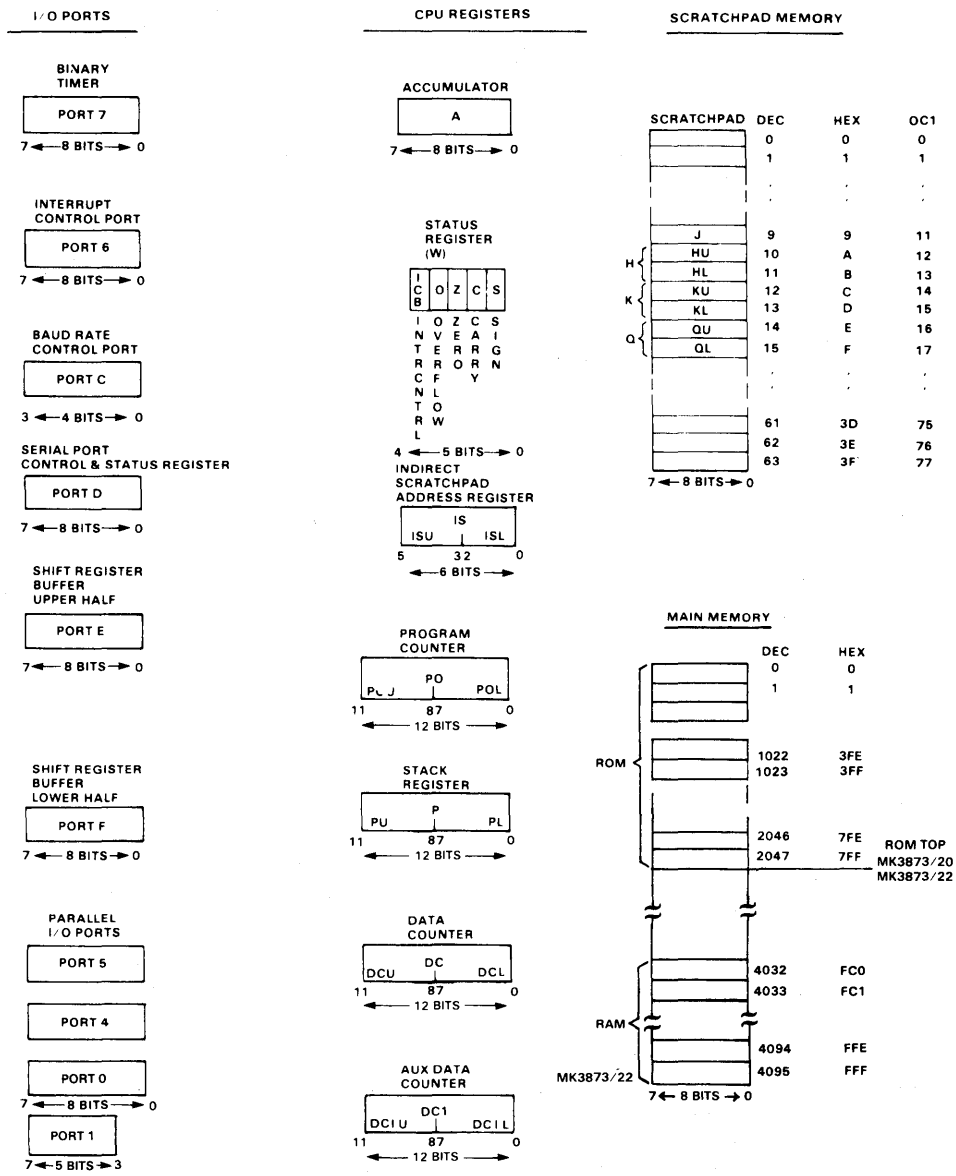
The upper bytes of the total address space in certain MK3873 devices is RAM memory. As with the ROM memory the RAM may be addressed by the PO and DC address registers. The executable RAM may be accessed by all 3870 instructions which address main memory indirectly through the Data Counter (DC) register. Additionally, the MK3873 may execute an instruction sequence which resides in the Executable RAM. Note that this cannot be done with the scratchpad RAM memory, which is the reason the term "Executable RAM" is given to this additional memory.

I/O PORTS

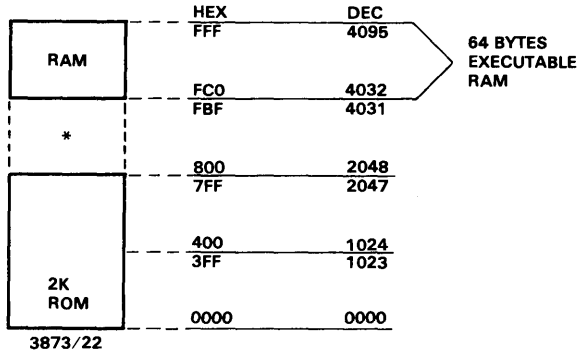
On the MK3873, 29 lines are provided for bidirectional, parallel I/O. These lines are addressable as four parallel I/O ports at locations 0, 1, 4, and 5. Note that Ports 0, 4, and 5 are 8 bits wide, while Port 1 contains only 5 bits of I/O in bit positions 3, 4, 5, 6, and 7. Bits 0-2 on Port 1 are not available for use as I/O port pins or as storage elements. The remaining three pins are used to provide the serial I/O

MK3873 PROGRAMMABLE REGISTERS, PORTS, AND MEMORY MAP

Figure 2



MK3873 MAIN MEMORY SIZE AND TYPE
Figure 3



This device contains 64 bytes of Scratchpad RAM.

*Data derived from addressing these intermediate locations is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size PØ, P, DC, DC1	ROM Size (Decimal)	Executable RAM Size
MK3873/22	64 bytes	12 bits	2048 bytes	64 bytes

VIII

function. A conceptual schematic of a bidirectional I/O port pin and available output drive options are shown in Figure 4.

As in all other 3870 family devices, an output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3873 has just completed an output of new data to port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. STROBE may also be used as an input strobe by doing a dummy output of H '00' to port 4 after completing the input operation.

SERIAL I/O OPERATION

The Serial Input/Output Port consists of a serial Shift Register, baud rate generator and control logic as shown in Figure 1. Together these elements provide the MK3873 with a half duplex asynchronous, or a full duplex synchronous, variable bit length serial port. Data is shifted into or out of the shift register at a rate determined by the internal baud rate generator or external clock. An end-of-word interrupt is generated in transmit or receive mode so that the CPU overhead is only at the word rate and not the serial bit rate.

SHIFT CLOCK

The internal clock is used to clock data transfers into and out of the 16 bit Shift Register. It is also used as an input to an internal counter which keeps track of the number of bits which have been shifted into or out of the Shift Register. Input data is sampled on the SERIAL INPUT, (SI), line on the rising edge of the SHIFT clock and is clocked into the most significant bit of the shift register. Output data is gated to the SERIAL OUTPUT line on the falling edge of the internal SHIFT clock.

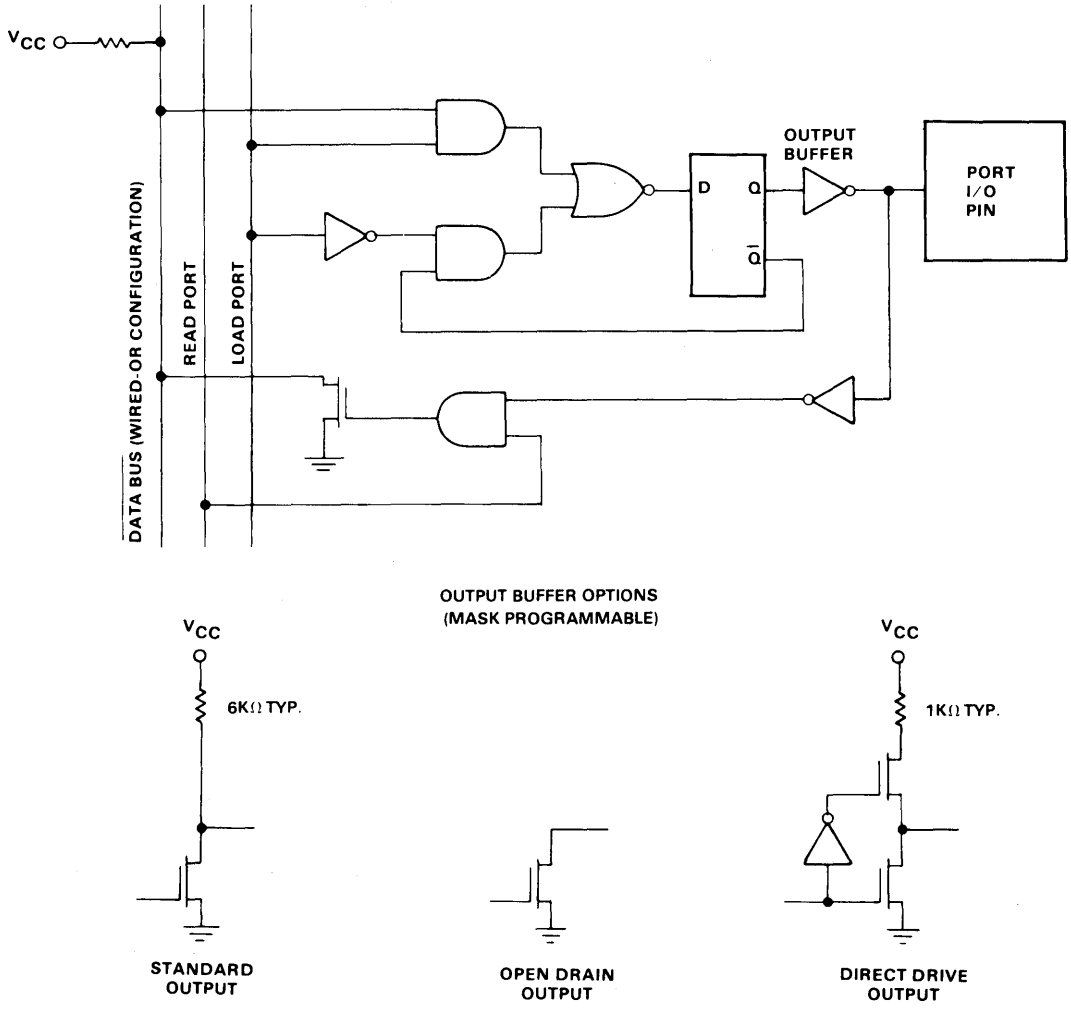
The clock is derived from the SRCLK pulse. The SRCLK pulse may be generated from the internal baud rate generator or it may be programmed as an input. The internal SHIFT clock operates at the same frequency as the SRCLK pulse when the Sync mode is selected, and at a rate which is divided by 16 (÷16) from the SRCLK pulse when the Async mode is selected.

SHIFT REGISTER

The Serial Port Shift Register is a 16-bit serial to parallel, parallel to serial shift register. This register is addressed and double-buffered by ports E and F as shown in Figure 5A.

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable). These two inputs have Schmitt trigger inputs with a minimum of 0.2 volts of hysteresis.

Serial In is a Schmitt trigger input with a minimum of 0.2V hysterisis.

Serial Out (SO) is the Standard Output type.

SRCLK output is capable of driving 3 TTL loads.

PORT D SERIAL PORT CONTROL REGISTER

The Serial Port Control register is write only and is addressed as Port D. The bit assignment is pictured in Figure 5C. The function of each bit is described below.

N2, N1, N0 - WORD LENGTH SELECT

These bits select one of the eight possible word lengths which are available with the MK3873 serial port. The serial port will shift the programmed number of bits through the Shift Register. If the Transmit mode is selected, data will be shifted out of the least significant bit (SR0) of the Shift Register to the Serial Out line (SO) while data is simultaneosly sampled at the Serial Input (SI) line and shifted into the most significant bit (SR15) of the Shift Register. When the Receive mode is selected, data will be sampled at SI and shifted in, but the SO line will be disabled such that it remains in a marking condition (Logic "1"). After the programmed number of bits have been shifted, the serial port logic will generate an end-of-word condition. This end-of-word condition will cause an interrupt if the serial port INTERRUPT ENABLE bit has been set.

It should be noted that the word values have been chosen so that the MK3873 can be programmed to send and receive a wide variety of asynchronous serial codes with various combinations of start and stop bits. Shown in Figure 6 is a table which gives the word length.

Values which would be programmed into the MK3873 Serial Port Register for Baudot, ASCII and 8 bit binary codes in an asynchronous word format are shown in the table of Figure 6. Shown in the table are word length values for various combinations of data bits, start and stop bits, and parity. It can be seen that the MK3873 serial port can accommodate many different word lengths of asynchronous or synchronous data.

SERIAL PORT REGISTERS

Figure 5A

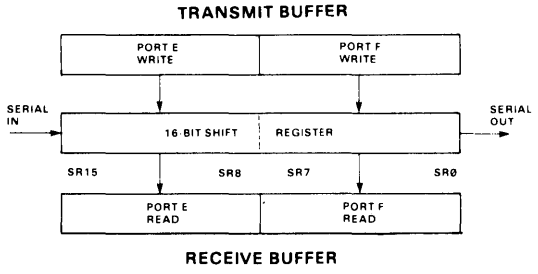


Figure 5B

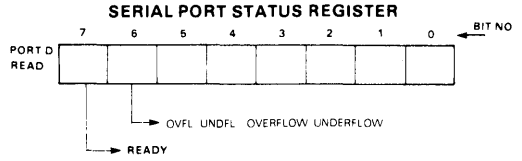
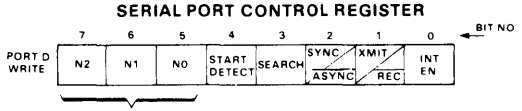


Figure 5C



WORD LENGTH SELECT

N2	N1	N0	WORD LENGTH
0	0	0	4 Bits
0	0	1	7 Bits
0	1	0	8 Bits
0	1	1	9 Bits
1	0	0	10 Bits
1	0	1	11 Bits
1	1	0	12 Bits
1	1	1	16 Bits

VIII

ASYNCHRONOUS WORD LENGTHS

Figure 6

DATA WORD	# OF BITS	START BITS	STOP BITS	PARITY	WORD LENGTH (BITS)
BAUDOT	5	1	1	No	7
	5	1	2	No	8
	5	1	1	Yes	8
	5	1	2	Yes	9
ASCI I	7	1	1	No	9
	7	1	2	No	10
	7	1	1	Yes	10
	7	1	2	Yes	11
8 Bit Binary	8	1	1	No	10
	8	1	2	No	11
	8	1	1	Yes	11
	8	1	2	Yes	12

START DETECT

When the START DETECT bit is enabled the serial port will not shift data through the Shift Register until a valid start bit is detected at the SI input pin. The Start Detect mode is operative only when the Async mode has been selected by programming bit 2 of the Serial Port Control Register to a logic "0". By selecting the Async mode, the internal SHIFT clock frequency is divided by 16 from the clock frequency at the SRCLK pin. (Recall that SRCLK can be an input or an output depending on whether the internal baud rate generator or the external clock is selected). When the START DETECT bit is set, the serial port logic looks for a high to low transition on the SI input. Until this transition occurs, the internal SHIFT clock is held low and no data is shifted in through the shift register. Once the transition is sensed, the SI input will be sampled on every SRCLK pulse for seven clock periods. If the logic level remains at zero on the SI input for each of the seven clock periods, the serial port logic will begin shifting data into the Shift Register on the eighth SRCLK pulse. Data will be shifted in at the ÷16 or SHIFT clock rate until the number of bits which have been programmed into the word length select have been shifted in. Once the programmed number of bits have been shifted in, the start detect circuitry will be rearmed and will begin searching for the next high-to-low transition on SI. This operation is pictured in the example shown in Figure 7.

When the START DETECT bit is disabled, data is continuously shifted through the Shift Register. An end-of-word condition will be generated each time the programmed number of bits has been shifted into or out of the Shift Register. A serial port interrupt will be generated when the end of word condition occurs if it has been enabled.

SEARCH

The SEARCH bit is enabled by programming it to a logic "1". When enabled, the SEARCH bit causes the serial port logic to generate an interrupt at every bit time if the serial port interrupt has been enabled. This interrupt will occur regardless of whether the Transmit or Receive mode has been selected and whether the Synchronous or Asynchronous mode has been selected. The Search mode is usually used for recognition of a sync character in synchronous serial data transmission. The MK3873 serial port does not automatically detect sync characters.

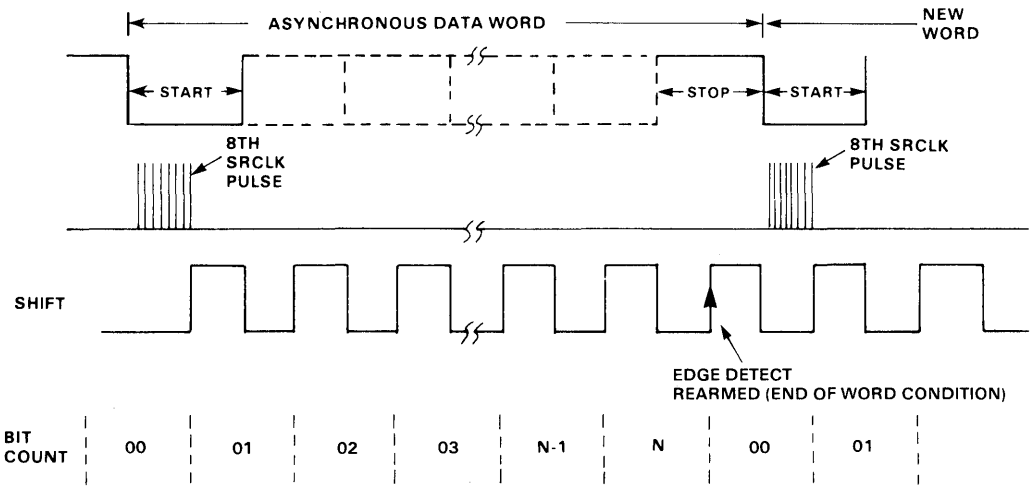
SYNC/ASYNC

The SYNC/$\overline{\text{ASYNC}}$ bit is used to select either the Synchronous mode of operation or the Asynchronous mode of operation. In the Synchronous mode of operation data is shifted through the Shift Register at a rate which is ÷1 the rate of SRCLK. When the Synchronous mode is selected, the start bit detect circuitry cannot be enabled, even if the START DETECT bit is programmed to a "1". In the Asynchronous mode (SYNC/$\overline{\text{ASYNC}}$ = 0) the internal SHIFT clock operates at a rate which is ÷16 the rate of SRCLK.

XMIT/$\overline{\text{REC}}$

The XMIT/$\overline{\text{REC}}$ bit is used to select either the Transmit or Receive modes of operation. When programmed to a "1" XMIT is selected and the serial port will shift data on the SO line as well as shift data into the SI input. Transmitted data will be enabled on the SO output on the falling edge of the internal SHIFT clock. When the Receive mode is selected (by programming XMIT/$\overline{\text{REC}}$ = 0), data will be clocked into the Shift Register on the rising edge of SHIFT, as it is when the

MK3873 SERIAL PORT START BIT DETECTION
Figure 7



where N is the word length value selected by programming bits N2-N0 in the serial port control register

Transmit mode is enabled, but data will be disabled from being shifted out on Serial Out. Serial Out will be held at a marking, or logic "1", condition.

SERIAL PORT INTERRUPT ENABLE

By programming this bit to a "1", the serial port interrupt will be enabled. A serial port interrupt may then occur when an end-of-word condition is generated. Program control will be vectored to one of two locations upon a serial port interrupt, depending on the way the XMIT/$\overline{\text{REC}}$ bit has been programmed. If the Transmit mode has been selected by programming XMIT/$\overline{\text{REC}}$ bit to a "1", then program control will be vectored to location E0 (Hex). For the Receive mode (XMIT/$\overline{\text{REC}}$ = 0) program control will be vectored to 60 (Hex) when the serial port interrupt occurs. With the addition of the Serial Port Interrupt, the MK3873 has three sources of interrupt. If these three interrupts were to occur simultaneously, priority between them would be such that they would be serviced in the following order:

1) Serial Port
2) Timer
3) External Interrupt

STATUS REGISTER

Reading port D of the MK3873 by performing an Input or Input Short (IN or INS) instruction will load the contents of the Serial Port Status Register into the Accumulator. The two bits which make up the Status Register are shown in Figure 5B. The operation of these two bits is described below:

READY - The meaning of the READY flag depends on whether the Transmit or Receive mode is selected. When the Transmit mode has been selected, the READY flag is set when a Transmit Buffer empty condition occurs. This means that any previous data which may have been loaded into the Transmit Buffer register pair has been transferred into the Shift Register. Loading either byte of the Transmit Buffer will clear the READY flag until the time that the Transmit Buffer register pair is loaded into the Shift Register during an end-of-word condition

In the Receive mode (XMIT/$\overline{\text{REC}}$ = 0), the READY flag is used to indicate a Receive Buffer full condition. This means that a word of the programmed length has been shifted in and has been loaded into the receive buffer register pair. Reading one of the ports E or F which make up the receive buffer register pair will clear the READY flag. The READY flag will remain a 0 until the next word is completely shifted in and loaded into the receive buffer.

OVFL/UNDFL is like the READY flag; the meaning of OVFL/UNDFL depends on the programming of the XMIT/$\overline{\text{REC}}$ bit in the Serial Port Control Register. When the Transmit mode has been selected OVFL/UNDFL is used to indicate a transmitter underflow condition.

A transmitter underflow condition can occur as follows: Assume that the Transmit mode is selected. Suppose that a word is loaded into the Transmit Buffer register. The serial port logic will load the contents of the Transmit Buffer into the Shift Register and will begin to shift the word out on the SO pin. When the contents of the Transmit Buffer are loaded into the Shift Register, the serial port logic will signal the Transmit Buffer empty condition by setting the READY flag to a "1". When the word in the Shift Register is completely shifted out, an end-of-word condition will be generated. The serial port logic will then check to see if new data has been loaded into the Transmit Buffer. If it has not, the OVFL/UNDFL flag will be set, indicating that the serial port logic has run out of data to send. The OVFL/UNDFL flag can be used to signal an error condition to the firmware, or it can be used to signal that all data has been cleared out of the Shift Register for the purposes of line turnaround.

The OVFL/UNDFL flag which, in this case, represents a transmitter underflow condition, is reset by reading the Status Register.

When the Receive mode is programmed, OVFL/UNDFL is used to signal that the Receive Buffer has overflowed. This overflow condition can occur as follows: Suppose that a serial word is shifted in, generating an end-of-word condition. The serial port logic will load the contents of the Shift Register into the Receive Buffer, and will set the READY flag to a "1" to indicate that the Receive Buffer is full. When the next word being received is completely shifted in, generating the next end-of-word condition, the serial port logic will check to see if the Receive Buffer has been read by examining the state of the READY flag. If the READY flag = 0, then the previous word has already been read from the Receive Buffer by the software and the serial port logic will load the current word into the Receive Buffer and will again set the READY flag. If the READY flag = 1, then the previous word has not been read from the Receive Buffer. The serial port logic will load the new word into the Receive Buffer, destroying the previous word. This action is signalled by the serial port logic setting the OVFL/UNDFL to a "1" signalling a receive buffer overflow condition. In this case reading the status register also clears the OVFL/UNDFL flag.

BAUD RATE CONTROL REGISTER

Port C is designated as the Baud Rate Control register. Four bits, 0-3, are used to select nine different internal baud rates or an external clock. When an internal baud rate is programmed, the SRCLK output is generated at a frequency which is divided from the MK3873's time base frequency. The SRCLK frequency can be calculated by dividing the time base frequency by the divide factor shown in Figure 8 for the bit pattern which is programmed into bits C3-C0. Also shown in Figure 7 is the programming of bits C3-C0 to obtain a set of standard baud rates when a 3.6864MHz crystal is used as a time base.

BAUD RATE CONTROL PORT
PORT C WRITE ONLY
Figure 8

PORT C WRITE 7 6 5 4	3	2	1	0	Bit No.	SRCLK Divide Factor	Shift Clock Rate (@ 3.6864 MHz time base SYNC	ASYNC
X	X	X	X	C3	C2	C1	C0			
				1	0	1	1	÷24	153.6 kbs	9600 bps
				1	0	1	0	÷48	76.8 kbs	4800 bps
				1	0	0	1	÷96	38.4 kbs	2400 bps
				1	0	0	0	÷192	19.2 kbs	1200 bps
				0	1	1	1	÷384	9600 bps	600 bps
				0	1	1	0	÷768	4800 bps	300 bps
				0	1	0	1	÷1536	2400 bps	150 bps
				0	1	0	0	÷2096	1758.8 bps	110 bps
				0	0	1	1	÷3072	1200 bps	75 bps
				0	0	0	0	External Clock Mode		

When any of the internal baud rates are selected, pin 36 becomes an output port pin. This pin is capable of driving three standard TTL inputs and provides a square wave output from the frequency selected in port C. The SYNC/$\overline{\text{ASYNC}}$ bit in the Serial I/O Control register has no effect on the output clock rate. The output will always be ÷1 directly from the baud rate generator.

If all zeros are loaded into this port, the External Clock mode is selected. Pin 36 becomes an input. Any TTL compatible square wave input can be used to generate the clock for the serial port.

TRANSMIT AND RECEIVE BUFFERS

The Receive Buffer registers are two eight bit registers which are addressed as ports E and F (Hex) and are read only. The Receive Buffer registers may be read at any time. The Transmit Buffer registers are also two 8-bit registers which are write only and addressed as ports E and F (Hex).

In the Receive mode, the contents of the 16 bit Shift Register are transferred to the Receive Buffer Register pair when a complete word has been shifted in. Bits SR15-SR8 of the Shift Register are loaded into bits 7-0 of port E while bits SR7-SR0 are loaded into bits 7-0 of Port F.

When entering the Transmit mode, the first data transfer from the Transmit Buffer to the 16 bit Shift Register won't occur until a 1 word time delay after entering Transmit Mode.

In the Receive mode, no transfers between the Transmit Buffer and the 16 bit Shift Register can occur.

The serial port does not automatically right justify incoming data, nor does it insert or strip start and stop bits from an asynchronous data word. Therefore, it is usually necessary to right justify incoming data read from the Receive Buffer registers in software through shift instructions, as well as strip start and stop bits if an asynchronous data format is being used. Likewise, in transmitting an asynchronous data word, it is usually necessary to insert start and stop bits in software into the 16 bit word which is to be loaded in two halves into the Transmit Buffer register.

RESET

The reset circuit on the MK3873 is used to initialize the device to a known condition either during the course of program execution or on a power on condition. This section discusses the effect of $\overline{\text{RESET}}$ on the serial port logic. A more complete description of $\overline{\text{RESET}}$ may be found in the 3870 Family Technical Manual.

Upon reset, both the serial port control register (port D) and the Baud Rate Control register (port C) are loaded with zeroes. This action sets the serial port control logic in the following state:

N2, N1, N0 (word length) = 4 bits
START DETECT disabled
SEARCH disabled
Asynchronous Receive mode
Serial port interrupt disabled
External Clock mode (SRCLK = 1).
Ports E and F are undefined

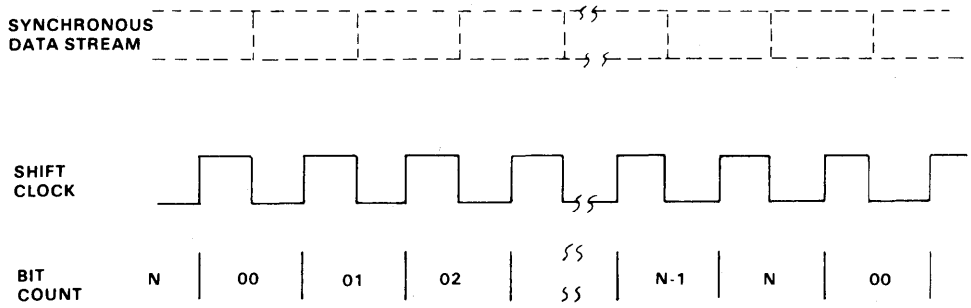
After the first control word is written to the Serial Port Control Register which selects an internal clock mode, the SRCLK will become an output and will remain high for one-half of a clock period as programmed into port C. It will then go low and produce a clock output waveform with the selected frequency.

ASYNCHRONOUS RECEIVE OPERATION

Figure 7 illustrates the timing for an example using the serial port in the Asynchronous mode. When operating in this mode, the Serial Port Control Register should be programmed for receive (XMIT/$\overline{\text{REC}}$ = 0) and the START DETECT bit should be enabled. Also, the Async mode should be selected, which allows the start detect circuitry to operate and sets the internal SHIFT clock at a rate which is divided by 16 (÷16) from the SRCLK rate. Upon selecting the Async mode and the START DETECT bit, the internal SHIFT clock is held low until a negative transition occurs on the SI pin. After a valid edge has been detected (see the START DETECT bit operation section) the SHIFT clock will go high and data will be shifted in at the middle of each bit time. When the programmed number of bits have been shifted in, an end-of-word condition is generated and a serial port receive interrupt will occur if it has been enabled.

After the falling edge of SHIFT following the end-of-word interrupt, the start detect circuitry will be enabled in preparation for the next word. Thus, if a start bit is present immediately following the time when the start detect circuitry is enabled, SHIFT Clock will again go high approximately one bit-time after the rising edge of SHIFT which clocked in the last bit of the preceeding word and caused the end-of-word interrupt. In other words, SHIFT

SYNCHRONOUS TRANSMIT OR RECEIVE TIMING
Figure 9



can go high again on the eighth SRCLK pulse as soon as the start detect circuitry is rearmed.

The Shift Register may be read before the next end-of-word condition; otherwise, a receiver overrun error will occur. For a 9600 bps data rate, this would require reading the Receive Buffer within N x 104 μs from the time that the end-of-word condition is generated, where N is the number of bits in the data word.

The example in Figure 7 shows the timing required for asynchronous data reception from a device such as a teletype. Within this data stream are start, data and stop bits. A typical format requires 1 start bit, 8 data bits and 2 stop bits for a total of 11 bits. All of these bits will be residing in the 16 bit Shift Register when the end-of-word interrupt is generated. It is, therefore, necessary to strip the start and stop bits from the data.

SYNCHRONOUS RECEIVE OPERATION

For synchronous operation, the START DETECT bit should not be enabled and the XMIT/$\overline{\text{REC}}$ bit should be programmed to a zero. Also the Sync mode should be enabled so that the internal SHIFT clock is divided by 1, or is equivalent to, SRCLK. Once a control word is written to port D specifying START DETECT = 0, Receive mode, and Sync mode, then the Serial Port will continuously shift data into the MSB of the upper half of the Shift Register at the SRCLK rate and will generate an end-of-word condition when the programmed number of bits have been shifted in.

An illustration of synchronous receive timing is shown in Figure 9. This diagram is a synchronous receive sequence for a word which is N bits in length, where N corresponds to the number of bits which have been programmed into the Serial Port Control Register. Note the relationship of SHIFT clock, the synchronous data stream, and the bit count. Since the START DETECT bit is not enabled, the serial port logic will continuously shift data in and generate end-of-word conditions at regular intervals. When the end-of-word condition occurs, a serial port receive interrupt occurs if it has been enabled, and the contents of the Shift Register will be loaded into the Receive Buffer. The serial port logic will set the READY flag in the Serial Port Status Register, indicating that the receive buffer is full. Since the serial port is double-buffered on receive, the program has entire word time to read the Receive Buffer. At 9600 bps this corresponds to a word time of N x 104μs, where N is the number of bits in a word.

Note that if a new control word is written to port D during the time that a serial word is shifted in, the bit count will be reset.

When using the Synchronous Receive mode on the MK3873, it is usually necessary to establish word synchronization in the data stream. The SEARCH bit, when enabled, causes the serial port logic to interrupt on each rising edge of SHIFT so that the data stream can be examined on a bit by bit basis. When the last bit of a sync word is found, the Search mode can be disabled and the serial port logic will shift in data and interrupt at the word rate.

ASYNCHRONOUS TRANSMIT OPERATION

The Asynchronous Transmit mode of operation is initiated by setting the XMIT/$\overline{\text{REC}}$ bit to a "1", and by programming the SYNC/$\overline{\text{ASYNC}}$ bit to a "0". Also, there must be an SRCLK pulse by selecting an internal or external source for SRCLK by programming port C. Upon setting XMIT/$\overline{\text{REC}}$ to a "1", there will be a 1 word length delay prior to the actual transfer of the first word from the Transmit Buffer to the 16 bit Shift Register. Serial data will then be shifted to the right on each rising edge of the internal SHIFT clock, and each new bit in the data stream will be enabled onto the SERIAL OUTPUT pin (SO) at the time of the falling edge of the

VIII

internal SHIFT clock.

As mentioned, one word time delay is generated between the time that the Transmit mode is initiated by programming XMIT/$\overline{\text{REC}}$ = 1 and the time that the contents of the Transmit Buffer are transferred into the Shift Register. This word time delay is generated internally to the MK3873 by counting the number of SHIFT clock pulses which correspond to the number of bits programmed into the word length select section of the Serial Port Control Register (N2, N1, N0). Therefore, the word time delay is equivalent to the time it takes to shift a complete serial data word out of the Shift Register. The same word time delay will result if data had been loaded prior to programming the XMIT/$\overline{\text{REC}}$ bit to a "1". As mentioned in the "START DETECT" bit description, the internal SHIFT clock is disabled when this bit is programmed to a "1". Since the serial port logic counts SHIFT clock pulses to generate the word time delay, the Transmit Buffer contents will never be transferred to the Shift Register and shifted out when the START DETECT bit is enabled. Also, the Transmit Buffer contents cannot be loaded into the Shift Register when XMIT/$\overline{\text{REC}}$ bit = 0.

When the initial serial data word has been transferred into the Shift Register, the READY flag is set in the Serial Port Status Register which is used to indicate the Transmit Buffer is empty. A transmit interrupt will be generated if the INTERRUPT ENABLE bit has been set in the Serial Port Control Register, and program control will be vectored to location E0 (hex). When operating the serial port in a polled environment with the serial port interrupt disabled, the READY bit can be used as a flag which indicates that new data may be loaded into the Transmit Buffer. In an interrupt driven software configuration, new data may be loaded into the Transmit Buffer at the beginning of the serial port interrupt service routine.

During the operation of the Transmit Mode the SERIAL INPUT pin (SI) is sampled and shifted into the Shift Register. However, since the START DETECT bit must be disabled during a transmit sequence, there is no way of establishing bit synchronization on any incoming serial data. Therefore, in the Asynchronous mode, the serial port can only be used in a half-duplex configuration.

After a block of data has been sent, it is sometimes useful for the program to know when the last serial word has been shifted out of the shift register. This is especially useful when operating the MK3873 with a bidirectional half-duplex transmission line. Once the block of serial data has been completely shifted out of the port, then it is usually desirable to reverse the direction of the line so that data may be received.

One way of determining when the last word has been shifted out of the Shift Register is through the use of the OVFL/UNDFL status bit in the Serial Port Status Register. The sequence would take place as follows: The program loads the Transmit Buffer with the last serial data word which is to be sent out either when the "READY" bit is set or during a transmit interrupt service routine. Loading the Transmit Buffer clears the READY flag. At the next end-of-word condition, the last serial data word is transferred from the Transmit Buffer into the Shift Register, which sets the READY flag once again. At this point the program would not load any more data into the Transmit Buffer and the READY flag will remain set. When the last word is completely shifted out of the Shift Register, the serial port logic will check to see if any new data has been loaded into the Transmit Buffer register pair. When it determines that there is no new data in the Transmit Buffer, the serial port logic will set the OVFL/UNDFL bit in the serial port status register and will return the SERIAL OUTPUT pin (SO) to a marking condition (logic "1"). The SERIAL OUTPUT pin (SO) is always returned to a marking condition on transmitter underflow when the ASYNC mode is selected. Since the OVFL/UNDFL bit is set when the last serial data word has completely been sent out, it can be used as a signal to indicate the end of transmission and that the direction of the transmission line may be set for receive.

SYNCHRONOUS TRANSMIT OPERATION

The Synchronous Transmit mode of operation is selected by programming bit 2 (XMIT/$\overline{\text{REC}}$) of the Serial Port Control register to a "1" and setting the SYNC/$\overline{\text{ASYNC}}$ bit to a "1".

Figure 9 illustrates serial output timing relationships in the Synchronous mode. Data is shifted to the right on each rising edge of the internal SHIFT clock. Output data is not enabled to the SERIAL OUTPUT pin (SO) until the falling edge of the SHIFT clock. In a 16 bit data word, SR0, the least significant bit of the Shift Register is shifted out first, and SR15, the most significant bit of the Shift Register, is shifted out last. While the Shift Register contents are being output on a bit by bit basis, data is simultaneously shifted in to the Shift Register through the SI pin.

As discussed in the "ASYNCHRONOUS TRANSMIT OPERATION" section, a word time delay is generated between the time that data is written to the Transmit Buffer and the time that the contents of the Transmit Buffer are loaded into the Shift Register once the XMIT/$\overline{\text{REC}}$ bit has been programmed to a one (1).

Another way of loading the initial data word into the Transmit Buffer requires the word synchronization having been achieved through recognition of a received sync character. Recall that in the Transmit mode, data is sampled at SI and shifted into the Shift Register at the same time that data is shifted out through SO. Upon power up or reset, a control word may be written to Port D which specifies Transmit and Synchronous modes. Word synchronization can then be achieved through the use of the SEARCH bit as described in the section which covers Synchronous Receive mode. Once word synchronization is achieved, the SEARCH bit is disabled and the serial port shifts in data and generates an end-of-word condition at the word rate.

Each time the end of word condition is reached, receive data

is transferred from the shift register into the Receive Buffer. At the same time, data is transferred from the Transmit Buffer into the Shift Register.

Therefore, in the Synchronous Transmit mode, the serial port may be used in a full duplex mode if word synchronization is established. At each end of word condition, output data is transferred to the Shift Register from the Transmit Buffer. At the same time, an incoming data word is transferred from the Shift register to the Receive Buffer register pair. In this case, the End-of-Word transmit routine would be used for sending data by loading the Transmit Buffer register, and for receiving data by reading the Receive Buffer register. Note that once word synchronization is established, an amount of time which is equal to one word time is available following the end-of-word interrupt for loading data into the Transmit Buffer.

The serial port operates differently in the Transmit mode for Synchronous operation than it does for Asynchronous operation. In the Asynchronous mode, after a word has been shifted out, the SO line is returned to a marking condition if no new data has been loaded into the Transmit Buffer.

In the Synchronous mode, after a word has been shifted out, the contents of the Transmit Buffer are loaded into the Shift Register regardless of whether or not new data was loaded into the Transmit Buffer. If new data was not loaded since the last time the transmit buffer was read, the OVFL/UNDFL flag is set which signals a transmitter underflow condition. This feature of always reloading the Shift Register with the contents of the Transmit Buffer when an end-of-word condition occurs allows a sync word to be continuously generated without CPU intervention when the transmitter is idle. This feature also allows variable duty cycle, variable frequency waveforms to be generated on the Serial Output line.

MK3873 CLOCKS

The time base network used with the MK3873 may be one of the four different types listed below.

Crystal
LC
RC
External Clock

The type of network which is to be used with the MK3873 is to be specified at the time when mask ROM MK3873 devices are ordered. The time base specification for each of the four modes are covered in the 3870 Family Technical Manual.

MK38P73 GENERAL DESCRIPTION

The MK38P73 is the EPROM version of the MK3873. It retains an identical pinout with the MK3873. The MK38P73 is housed in the "R" package which incorporates a 28 pin socket located directly on top of the package.

The MK38P73 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3870 devices. Thus, the MK38P73 eliminates the need for emulator board products. In addition, several MK38P73s can be used in prototype systems in order to test design concepts in field service before committing to high-volume production with mask ROM MK3873s. The compact size of the MK38P73/EPROM combination allows the packaging of such prototype systems to be the same as that used in production.

Finally, in low-volume applications the MK38P73 can be used as the actual production device.

Most of the material which has been presented for the MK3873 applies to the MK38P73. The MK38P73 has the same architecture and pinout as the MK3873. Additional information is presented in the following sections.

MK38P73 MAIN MEMORY

As can be seen from the block diagram in Figure 10, the MK38P73 contains no on-chip ROM. The memory address and data lines are brought out to the 28 pin socket located directly on top of the 40 pin package. The MK38P73 will address up to 4096 bytes of external EPROM memory.

There is one memory version of the MK38P73, and it is designated as the MK38P73/02. The MK38P73/02 contains 64 bytes of on-chip executable RAM. The MK38P73/02 can emulate the mask ROM MK3873/22 device.

Addressing of main memory on the MK38P73 is accomplished in the same way as it is for the MK3873. See Figure 12 for Main Memory addresses and for address register size in the MK38P73.

MK38P73 EPROM SOCKET

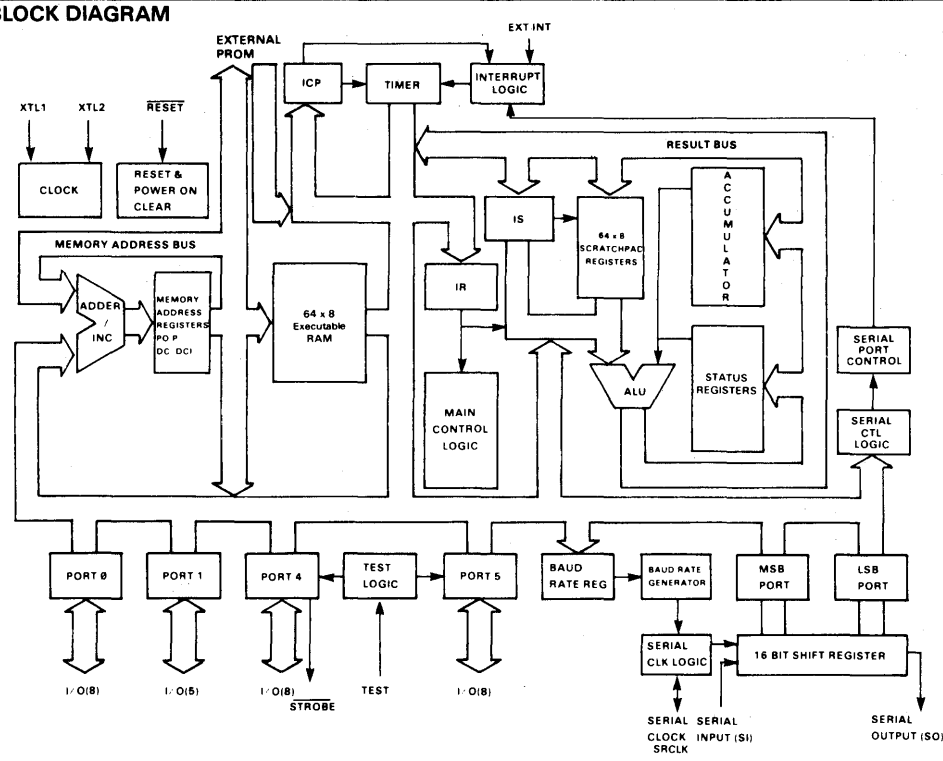
A 28 pin EPROM socket is located on top of the MK38P73 "R" package. The socket and compatible EPROM memories is shown in Figure 11. When 24 pin memories are used in the 28 pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket. (The memory should be lower justified in the 28 pin socket.)

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P73.

Initially, the MK38P73 that is compatible with the MK2716 is available. The MK38P73 designed to accommodate the 28-

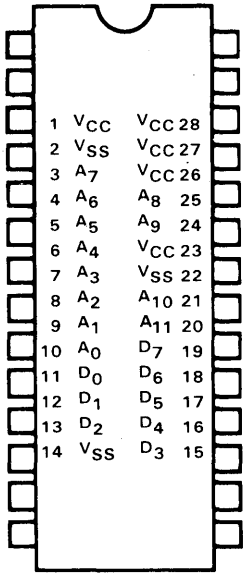
MK38P73 BLOCK DIAGRAM

Figure 10



MK38P73 "R" PACKAGE PINOUT

Figure 11



MK97310 (Open Drain)
Compatible Memories
2758
MK2716
2516 2532

pin memory devices will be available at a later date.

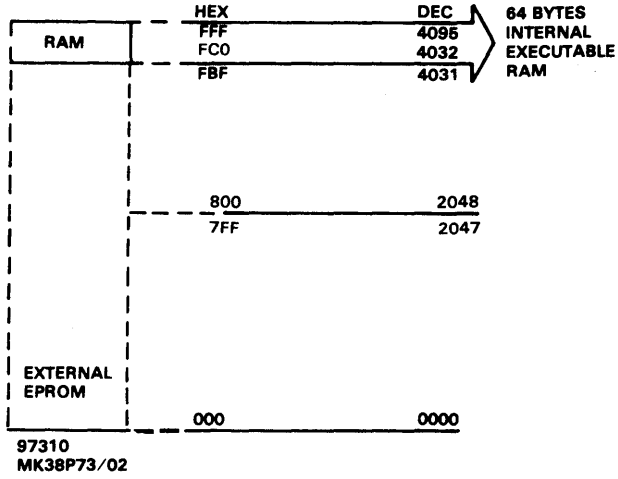
MK38P73 I/O PORTS

The MK38P73 is offered with open drain type output buffers on Ports 4 and 5. This open drain version is provided so that user-selected open drain port pins on the mask ROM MK38P73 can be emulated prior to ordering those mask ROM parts. Figure 11 lists the part ordering number for an MK38P73/02.

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P73 is shown in Figure 13. The Φ clock signal is derived internally in the MK38P73 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P73 which corresponds to a machine cycle during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is

MK38P73 MAIN MEMORY MAP
Figure 12



Device	Scratchpad RAM Size (Decimal)	Address Register Size PØ, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P73/02 97300, 97310	64 bytes	12 bits	Ø bytes	64 bytes

VIII

the cycle which is pictured in the timing diagram. After a delay from the falling edge of the WRITE clock, the address lines A_{11} - A_0 become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P73 is shown as t_{aas}, or the time when address is stable until data must be valid on the data bus lines.

An equation for calculating available memory access time along with some calculated access times based on the listed time base frequencies is also shown in Figure 13.

MK38P73 CLOCKS

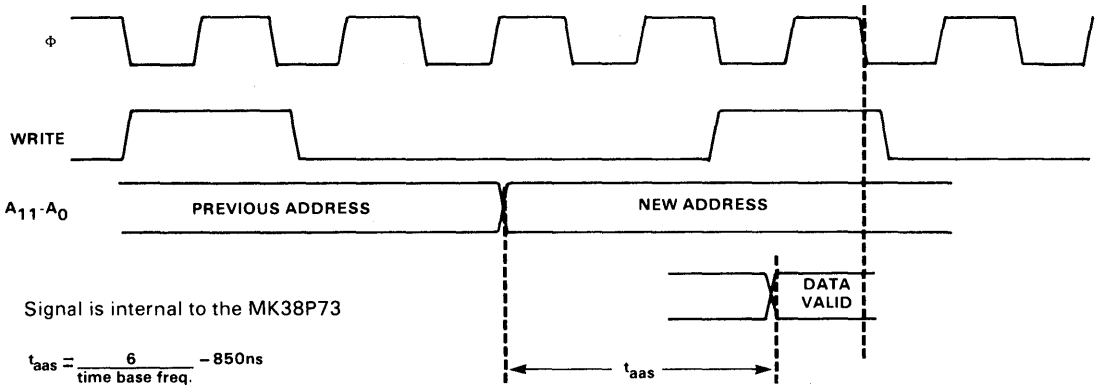
The MK38P73 has the ability to operate with any one of the following time base configurations.

Crystal
LC
RC
External Clock

This capability has been provided in the MK38P73 so that it can emulate a mask ROM MK3873 operating in any of the possible clock configurations.

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P73

Figure 13



Signal is internal to the MK38P73

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850\text{ns}$$

(FROM ADDRESS STABLE)

	4MHz	3.58MHz	3MHz	2.5MHz	2MHz
ACCESS TIME	650ns	825ns	1.15μs	1.55μs	2.15μs

OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
—00	+5V ± 10%	0° - 70°C
—05	+5V ± 5%	0°C - 70°C
—10	+5V ± 10%	-40°C - +85°C
—15	+5V ± 5%	-40°C - +85°C

ABSOLUTE MAXIMUM RATINGS*

	-00,-05	-10,-15
Temperature Under Bias	-20°C to +85°C	-50°C to +100°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins With Respect to Ground	-1.0V to +13.5V	-1.0V to + 13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin[2]	60mW	60mW
Power Dissipation by all I/O pins[2]	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_O$		$2t_O$			
WRITE	t_W	Internal WRITE Clock period	4tΦ 6tΦ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50pF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	12tΦ +300	ns	$\overline{STROBE}$ load = 50pF+3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time -0.1		power supply rise time -0.15		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

VIII

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O, $\overline{RESET}$, EXT INT, TEST		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

AC CHARACTERISTICS FOR SERIAL I/O PINS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SIGNAL	SYM	PARAMETER	-00, -05		-10, -15		UNIT	CONDITIONS
			MIN	MAX	MIN	MAX		
SRCLK	$t_{C(SRCLK)}$	Serial Clock Period in External Clock Mode	3.3	∞	∞		μs	
	$t_{W(SRCLKH)}$	Serial Clock Pulse Width, High. External Clock Mode	1.3	∞		∞	μs	
	$t_{W(SRCLKL)}$	Serial Clock Pulse Width, Low. External Clock Mode	1.3	∞		∞	μs	
	$t_{r(SRCLK)}$	Serial Clock Rise Time Internal Clock Mode	60		60		ns	0.8V -2.0V C_L = 100pf
	$t_{f(SRCLK)}$	Serial Clock Fall Time Internal Clock Mode	30		30		ns	2.4V -0.4V C_L = 100pf
SI	$t_{S(SI)}$	Setup Time To Rising Edge of SRCLK (SYNC Mode)	0		0		ns	
	$t_{H(SI)}$	Hold Time From Rising Edge of SRCLK (SYNC Mode)	1500		1500		ns	
SO	$t_{D(SO)}$	Data Output Delay From Falling Edge of SRCLK (SYNC Mode)	1190		1190		ns	

AC CHARACTERISTICS FOR MK38P73

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100mW (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11}-A_{01} stable until data must be valid at D_7-D_0	650				ns	Φ = 2.0MHz

*See Table in Figure 13.

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O power dissipation ≤ 100mW

SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNIT	DEVICE
I_{CC}	Average Power Supply Current		103		138	mA	MK3873/12 Outputs Open
			138		165	mA	MK38P73/02 No EPROM, Outputs Open
P_D	Power Dissipation		485		645	mW	MK3873/22 Outputs Open
			646		775	mW	MK38P73/02 No EPROM, Outputs Open

VIII

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	I/O input high level	2.0	5.8	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	2.0	13.2	V	open drain (1)
V_{IHR}	Input high level, $\overline{RESET}$	2.0	5.8	2.2	5.8	V	standard pull-up (1)
		2.0	13.2	2.2	13.2	V	No pull-up
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	5.8	V	standard pull-up (1)
		2.0	13.2	2.2	13.2	V	No pull-up
V_{IL}	I/O ports, $\overline{RESET}$[1], EXT INT[1] input low level	-.3	.8	-.3	0.7	V	(1)
I_{IL}	Input low current, standard pull-up pins		-1.6		-1.9	mA	$V_{IN}=0.4V$
I_L	Input leakage current, open drain pins $\overline{RESET}$ and EXT INT inputs With no pull-up resistor		+10 -5		+18 -8	μA μA	$V_{IN}=13.2V$ $V_{IN}=0.0V$
I_{OH}	Output high current, standard	-100		-89		μA	$V_{OH}=2.4V$
	pull-up pins	-30		-25		μA	$V_{OH}=3.9V$
I_{OHDD}	Output high current,	-100		-80		μA	$V_{OH}=2.4V$
	direct drive pins	-1.5	-8.5	-1.3	-11	mA mA	$V_{OH}=1.5V$ $V_{OH}=0.7V$
I_{OL}	Output low current, I/O ports	1.8		1.65		mA	$V_{OL}=0.4V$
I_{OHS}	$\overline{STROBE}$ Output High current	-300		-270		μA	$V_{OL}=2.4V$
I_{OLS}	$\overline{STROBE}$ output low current	5.0		4.5		mA	$V_{OL}=0.4V$

DC CHARACTERISTICS FOR MK38P73

(Signals brought out at socket)

T_A, V_{CC} within specifiec operating range, I/O Power Dissipation ≤ 100mW. (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
I_{CCE}	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.7	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100 -30		-90 -25		μA μA	V_{OH}=2.4V V_{OH}=3.9V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

DC CHARACTERISTICS FOR SERIAL PORT I/O PINS

T_A, V_{CC} within specified operating range

I/O Power Dissipation ≤ 100mW (Note 2)

SYM	PARAMETER	-00, -05		-10, -15		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
V_{IHS}	Input High for SI, SRCLK	2.0	5.8	2.0	5.8	V	
V_{ILS}	Input Low level for SI, SRCLK	-.3	.8	-.3	0.7	V	
I_{ILS}	Input low current for SI, SRCLK		-1.6		-1.9	mA	V_{IL} = 0.4V
I_{OHSO}	Output High Current SO	-100 -30		-90 -25		μA μA	V_{OH} = 2.4V V_{OL} = 3.9V
I_{OLSO}	Output Low Current SO	1.8		1.65		mA	V_{OL} = 0.4V
I_{OHSRC}	Output High Current SRCLK	-300		-270		μA	V_{OH} = 2.4V
I_{OLSRC}	Output Low Current	5.0		4.5		mA	V_{OL} = 0.4V

1. $\overline{\text{RESET}}$ and EXT INT have internal Schmit triggers giving minimum .2V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL})(|I_{IL}|) + \Sigma (V_{CC} - V_{OH})(|I_{OH}|) + \Sigma (V_{OL})(|I_{OL}|)$

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

tpsc = t Φ x Prescale Value

Interval Timer Mode:

Single interval error, free running (Note 3) ..... ±6tΦ
Cumulative interval error, free running (Note 3) 0
Error between two Timer reads (Note 2) ..... ± (tpsc + tΦ
Start Timer to stop Timer error (Notes 1,4) ..... +tΦ to —(tpsc +tΦ)
Start Timer to read Timer error (Notes 1,2) ..... —5tΦ to —(tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1,3) ..... —2tΦ to —8tΦ)
Load Timer to stop Timer error (Note 1) ..... +tΦ to —(tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1,2) ..... —5tΦ to —(tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1,3) ..... —2tΦ to —9tΦ)

VIII

Pulse Width Measurement Mode:

Measurement accuracy (Note 4)	+t Φ to —(tpsc +2t Φ)
Minimum pulse width of EXT INT pin	2tΦ

Event Counter Mode:

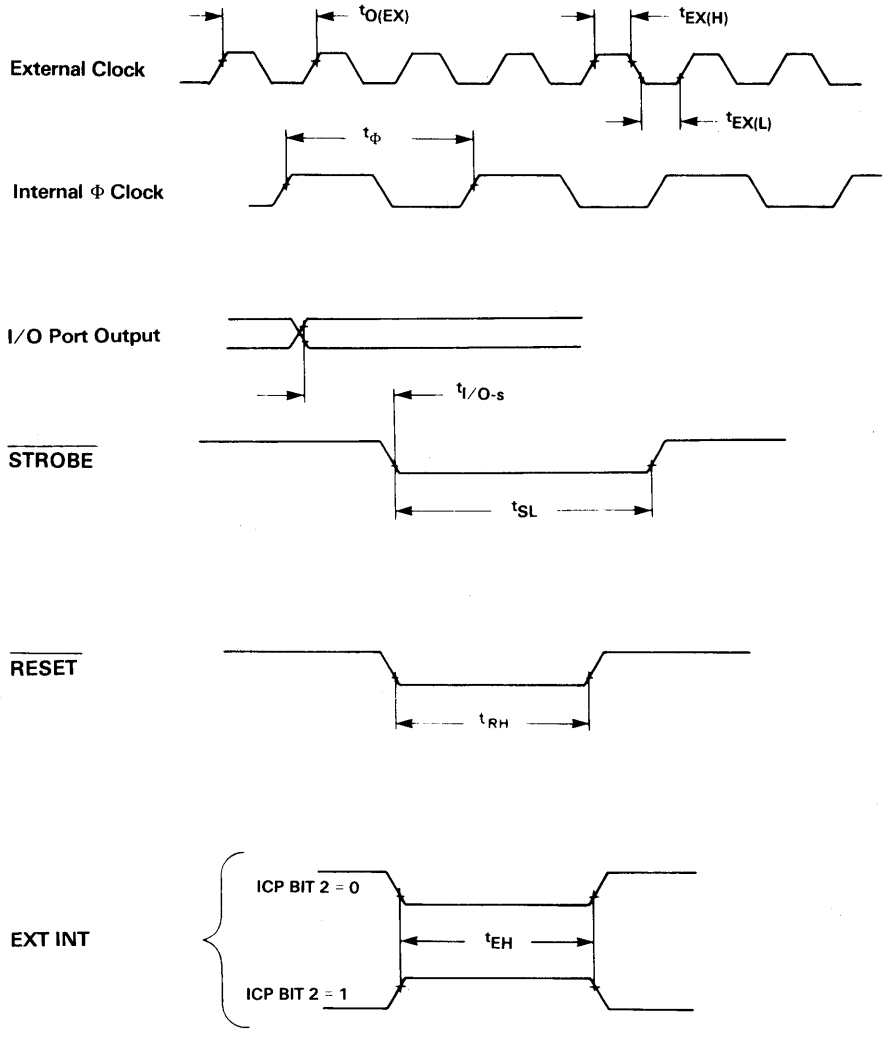
Minimum active time of EXT INT pin	2tΦ
Minimum inactive time of EXT INT pin	2tΦ

Notes:

1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

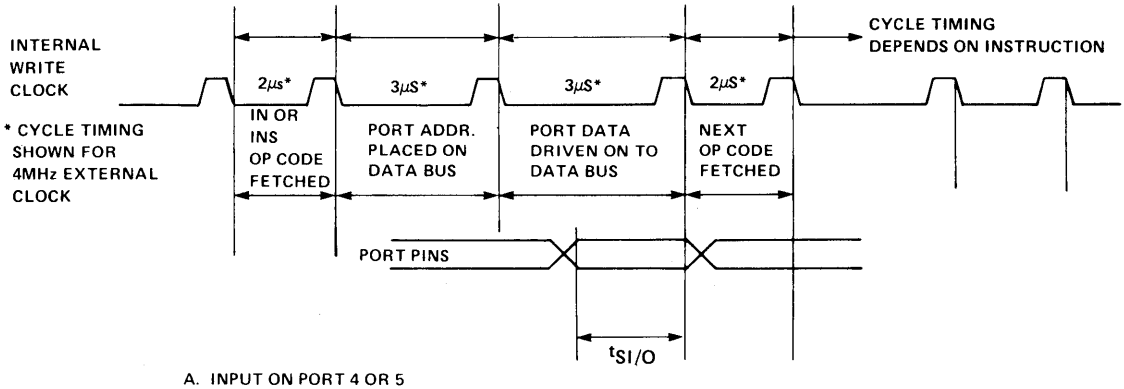
AC TIMING DIAGRAM

Figure 14

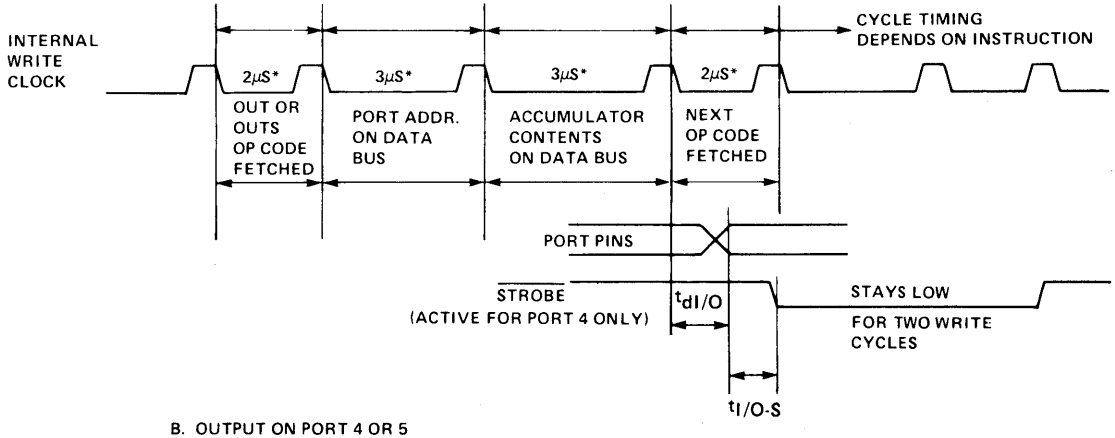


Note: All measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} max., or V_{OH} min.

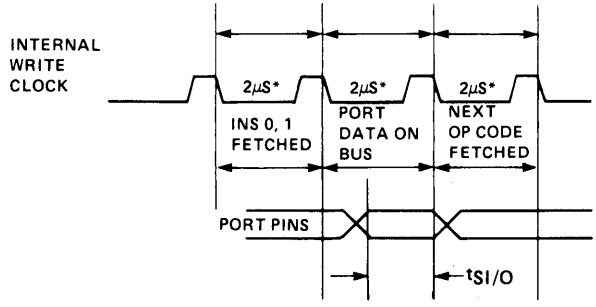
INPUT/OUTPUT AC TIMING
Figure 15



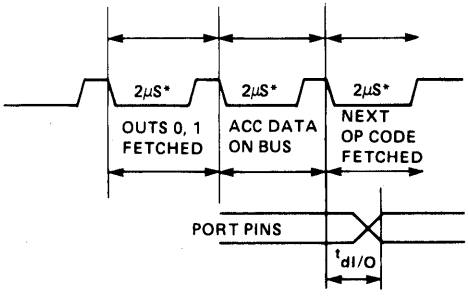
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5



C. INPUT ON PORT 0 OR 1

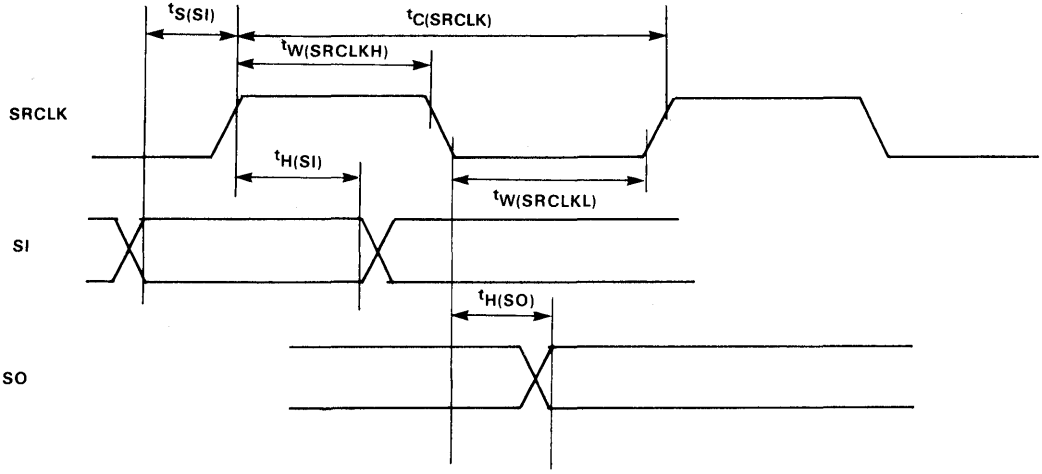


D. OUTPUT ON PORT 0, 1

VIII

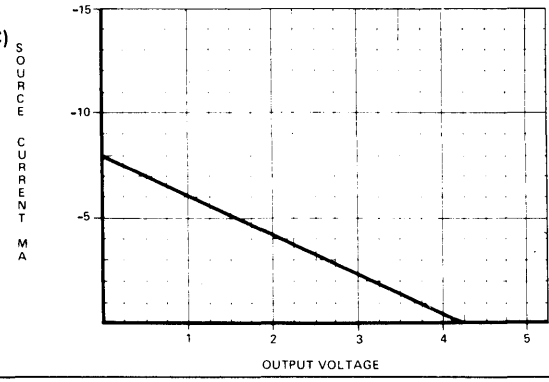
AC TIMING DIAGRAM FOR SERIAL I/O PINS.

Figure 16



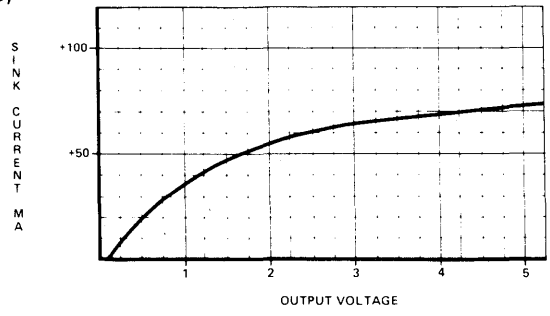
STROBE SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 17

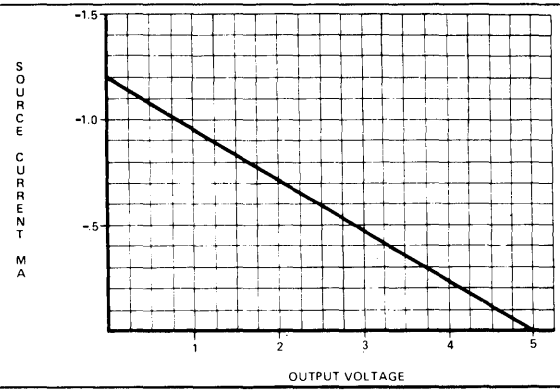


STROBE SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

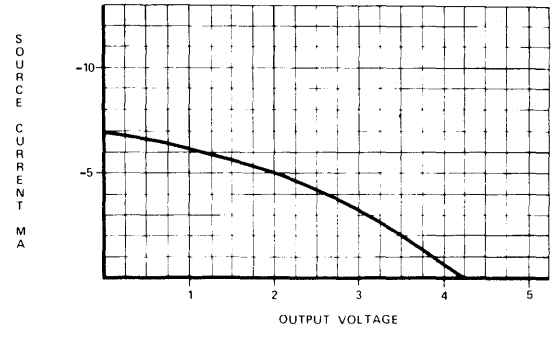
Figure 18



STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 19

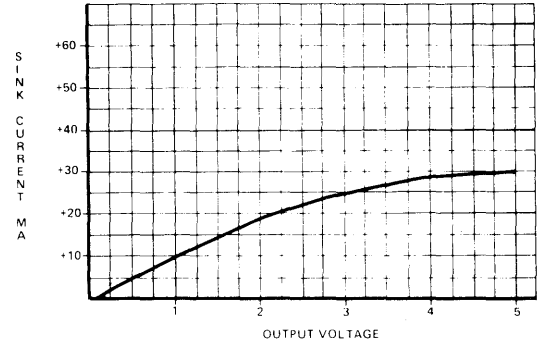


DIRECT DRIVE I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 20

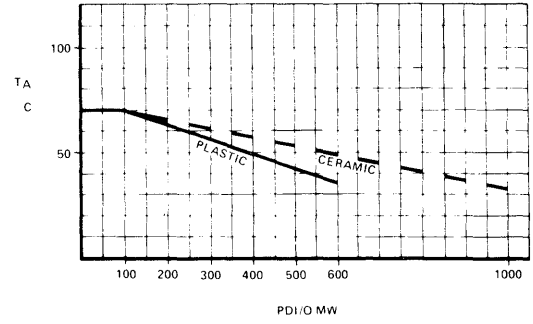


VIII

I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 21



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION
Figure 22

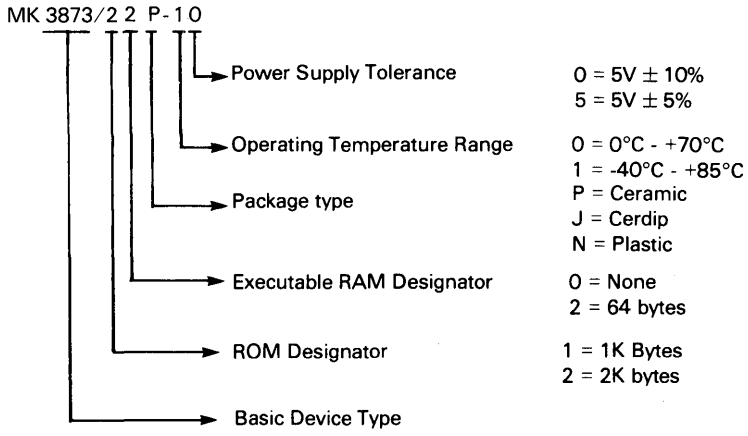


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and Executable RAM, the desired package type, temperature range, and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

GENERIC PART NUMBER

An example of the generic part number is shown below.

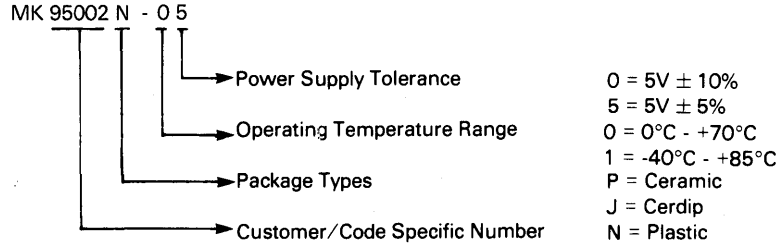


An example of the generic part number for the PPROM device is shown below.

MK38P73/02 R-05

DEVICE ORDER NUMBER

An example of the device order number is shown below.



The Customer/Code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirements of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

3870 SINGLE CHIP MICRO FAMILY
MK3875 AND MK38P75

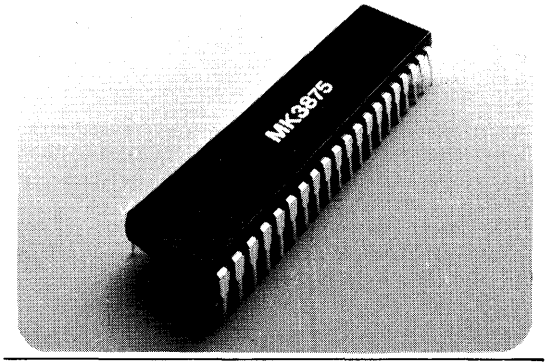
MK3875 FEATURES

- ☐ Available with 2K or 4K bytes of mask programmable ROM memory.
- ☐ 64 bytes scratchpad RAM
- ☐ 64 bytes of Executable RAM
- ☐ Standby feature for low power data retention of executable RAM including:
  Low standby power
  Low standby supply voltage
  No external components required to trickle charge battery.
- ☐ Software compatible with 3870 family
- ☐ 30 bits (4 ports) TTL compatible I/O
- ☐ Programmable binary Timer
  Interval Timer Mode
  Pulse Width Measurement Mode
  Event Counter Mode
- ☐ External Interrupt Input
- ☐ Crystal, LC, RC, or external time base options available
- ☐ Low power under normal operation (285 mW typ.)
- ☐ +5 volt main power supply
- ☐ Pinout compatible with 3870 family

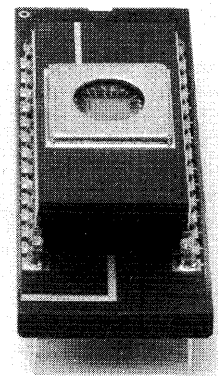
MK38P75 FEATURES

- ☐ EPROM version of MK3875
- ☐ Piggyback RPOM (P-PROM)™ package
- ☐ Accepts 24 pin or 28 pin EPROM memories
- ☐ Identical pinout as MK3875
- ☐ In-socket emulation of MK3875

MK3875

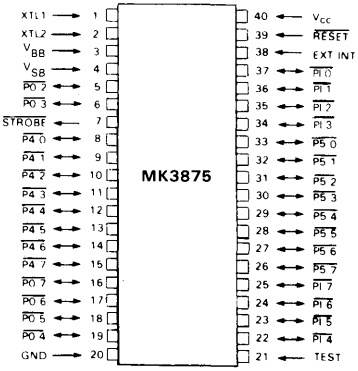


MK38P75

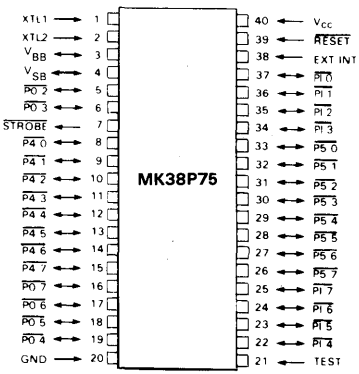


VIII

PIN CONNECTIONS
MK3875



PIN CONNECTIONS
MK38P75



PIN NAME	DESCRIPTION	TYPE
$\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$	I/O Port 0	Bidirectional
$\overline{P1\text{-}0}$ - $\overline{P1\text{-}7}$	I/O Port 1	Bidirectional
$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$	I/O Port 4	Bidirectional
$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$	I/O Port 5	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line	Input
XTL 1, XTL 2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input
V_{SB}	Standby Power	Input
V_{BB}	Substrate Decoupling	Input

GENERAL DESCRIPTION

The MK3875 Single Chip Microcomputer offers a Low Power Standby mode of operation as an addition to the 3870 Family. The Low Power Standby feature provides a means of retaining data in the executable RAM on the MK3875 while the main power supply line (V_{CC}) is at 0 volts and the rest of the MK3875 microcomputer is shut down. The executable RAM is powered from an auxiliary power supply input (V_{SB}) while operating in the Lower Power Standby mode. When V_{SB} is maintained at or above its minimum level, data is retained in the executable RAM memory with a very low power dissipation.

The MK3875 retains commonality with the rest of the industry standard 3870 family of single chip microcomputers. It has the same central processing unit, oscillator and clock circuits, and 64 byte scratchpad memory array. Also, the 3870's sophisticated programmable binary timer is included which provides three different operating modes. Two pins on the MK3875 are dedicated to the Low Power Standby mode and are designated as V_{SB} and V_{BB}. The $\overline{RESET}$ line serves to reset the MK3875 and place it in a protected state so that the contents of the Executable RAM will remain unchanged when V_{CC} is being powered down to 0 volts. All other pins on the MK3875 are identical in function to corresponding pins on the MK3870, so that pin compatibility is maintained. The MK3875 executes the entire 3870 instruction set.

The MK38P75 microcomputer is the PROM based version of the MK3875. It is called the piggyback PROM (P-PROM)™ because of its packaging concept. This concept allows a standard 24-pin or 28-pin EPROM to be mounted directly on top of the microcomputer itself. The EPROM can be removed and reprogrammed as required with a standard PROM programmer. The MK38P75 retains the pinout and architectural features as other members of the 3870 family. The MK38P75 is discussed in more detail in a later section.

FUNCTIONAL PIN DESCRIPTION

$\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$, $\overline{P1\text{-}0}$ - $\overline{P1\text{-}7}$, $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$, and $\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ are 30 lines which can be individually used as either TTL compatible inputs or as latched outputs.

$\overline{STROBE}$ is a ready strobe associated with I/O Port 4. This pin, which is normally high, provides a single low pulse after valid data are present on the $\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ pins during an output instruction.

$\overline{RESET}$ - may be used to externally reset the MK3875. When pulled low, the Mk3875 will reset. When allowed to go high the MK3875 will begin program execution at program location H '000'. Additionally, when $\overline{RESET}$ is brought low all accesses of the executable RAM are prevented and the RAM is placed in a protected state for powering down V_{CC} without loss of data.

EXT INT is the external interrupt input. Its active state is software programmable. This input is also used in conjunction with the timer for pulse width measurement and event counting.

XTL 1 and XTL 2 are the time base inputs to which a crystal (2 to 4 MHz), LC network, RC network, or an external single-phase clock may be connected. The time base network must be specified when ordering an MK3875.

TEST is an input used only in testing the MK3875. For normal circuit function this pin may be left unconnected but it is recommended that TEST be grounded.

V_{CC} is the power supply input +5 V.

V_{SB} is the RAM standby power supply input.

V_{BB} is the substrate decoupling pin. A .01 micro-Farad capacitor is required which is tied between V_{BB} and GND.

MK3875 ARCHITECTURE

The basic functional elements of the mask ROM MK3875 single chip microcomputer are shown in the block diagram in Figure 1. A programming model is shown in Figure 2. Much of the Mk3875 architecture is identical with the rest of the devices in the 3870 family. The significant features of the MK3875 are discussed in the following sections. The user is referred to the 3870 Family Technical Manual for a thorough discussion of the architecture, instruction set, and other features which are common to the 3870 family.

MAIN MEMORY

The main memory section on the MK3875 consists of a combination of ROM and executable RAM.

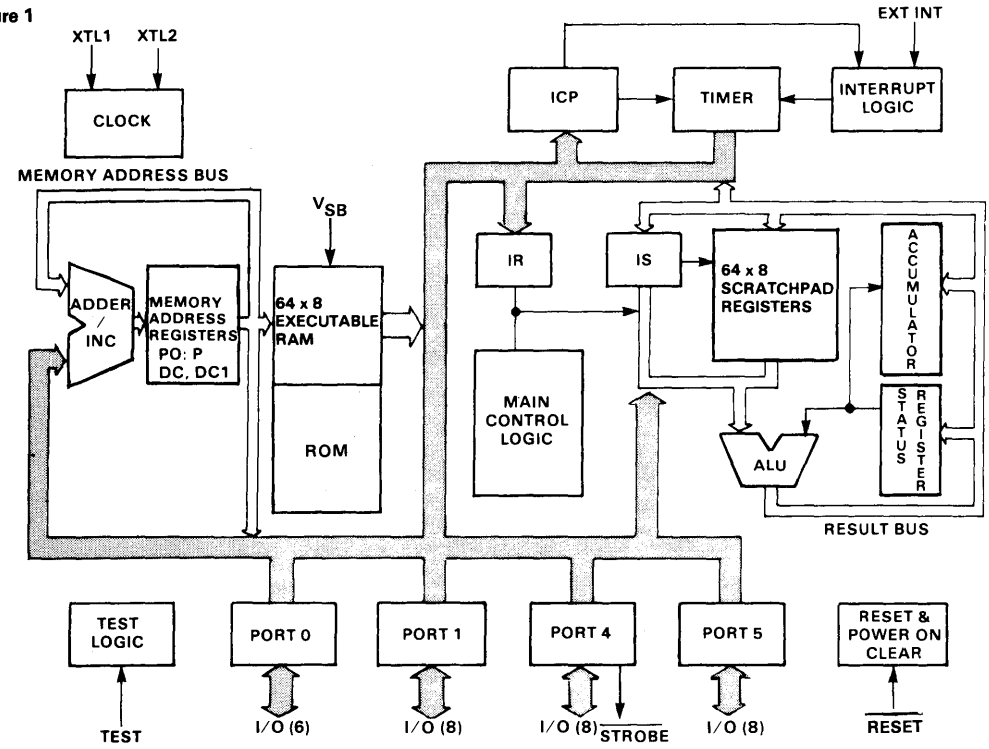
There are four registers associated with the main memory section. These are the Program Counter (PO), the Stack Register (P), the Data Counter (DC) and the Auxiliary Data Counter (DC1). The Program Counter is used to address instructions during program execution. P is used to save the contents of PO during an interrupt or subroutine call. Thus, P contains the return address at which processing is to resume upon completion of the subroutine or the interrupt routine.

The Data Counter (DC) is used to address data tables. This register is auto-incrementing. Of the two data counters only DC can access the memory. However, the XDC instruction allows DC and DC1 to be exchanged.

The length of the PO, P, DC, and DC1 registers for all MK3875 devices is 12 bits. Figure 3 shows the amounts of

MK3875 BLOCK DIAGRAM

Figure 1



ROM and Executable RAM for each device in the MK3875 family.

EXECUTABLE RAM

The upper bytes of the total address space in all MK3875 devices are RAM memory. As with the ROM memory, the RAM may be addressed by the PO and DC address registers. The executable RAM may be accessed by all 3870 instructions which address main memory indirectly through the Data Counter (DC) register. Additionally, the MK3875 may execute an instruction sequence which resides in the executable RAM. Note that this sequence cannot be done with the scratchpad RAM memory, which is the reason the term "executable RAM" is given to this additional memory. The contents of the executable RAM memory are preserved when the Low Power Standby mode is in operation.

I/O PORTS

The MK3875 provides 30 bits of bidirectional parallel I/O. These lines are addressed as Ports 0, 1, 4 and 5. In addition, the Interrupt Control Port is addressed as Port 6 and the binary timer is addressed as Port 7. The programming of Ports 6 and 7 and the bidirectional I/O pins are covered in the 3870 Family Technical Manual.

Since two pins are dedicated to serve the Standby Power mode (V_{SB}), port 0 has only the upper 6 bits, $\overline{P0\text{-}2}$ - $\overline{P0\text{-}7}$, available for use as general purpose I/O pins. Ports 1, 4, and 5 are all a full 8 bits wide.

The schematic of an I/O pin and available output drive options are shown in Figure 4.

An output ready strobe is associated with Port 4. This flag may be used to signal a peripheral device that the MK3875 has just completed an output of new data to Port 4. The strobe provides a single low pulse shortly after the output operation is completely finished, so either edge may be used to signal the peripheral. $\overline{\text{STROBE}}$ may be used as an input strobe simply by doing a dummy output of H '00' to Port 4 after completing the input operation.

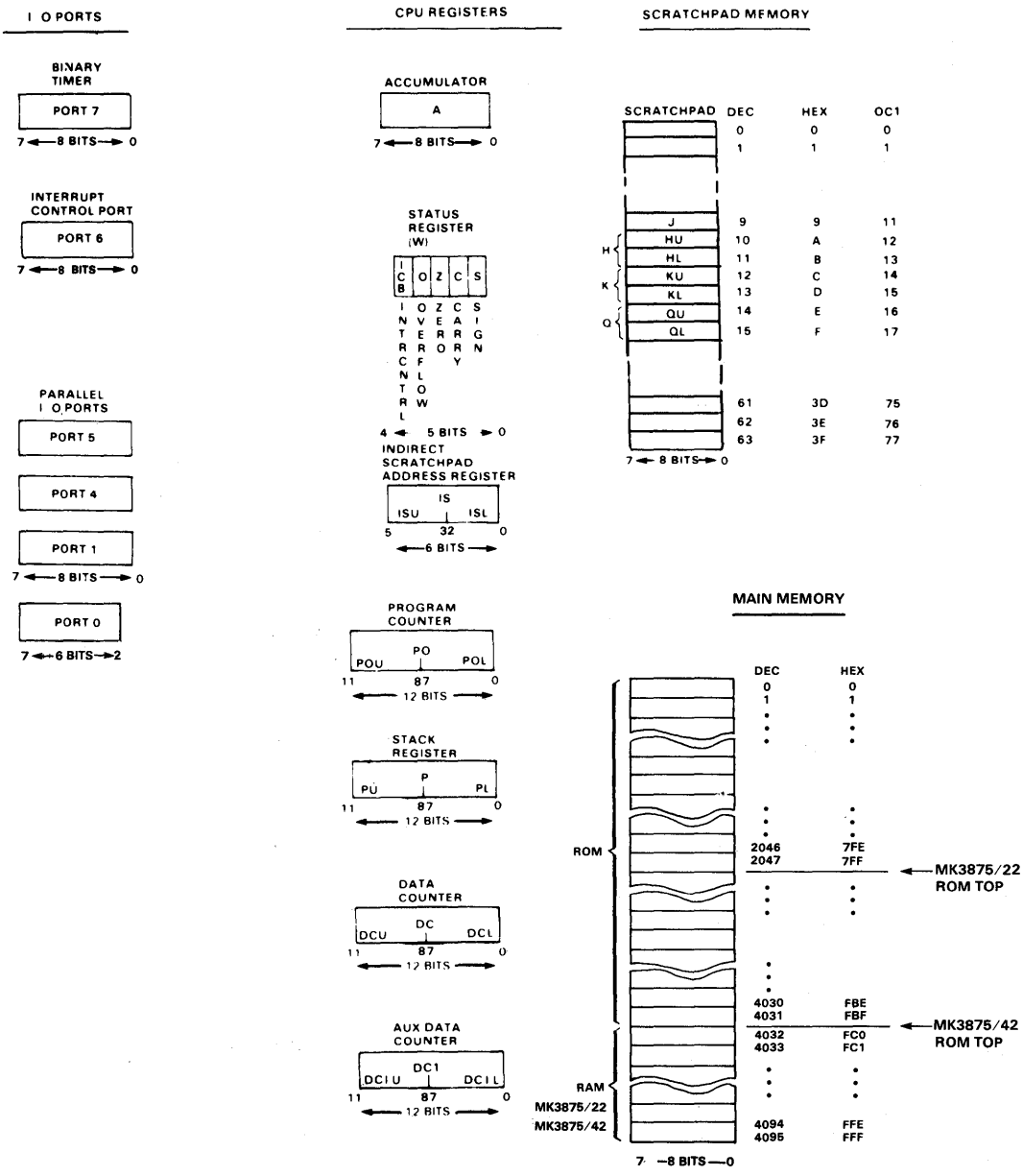
STANDBY POWER MODE

On the MK3875, the contents of the on-chip executable RAM can be saved when the Standby Power mode is operative. The Standby Power mode allows the MK3875's main power supply to drop all way down to 0 volts while the on-chip executable RAM is powered from the auxiliary low power supply input, V_{SB}. Thus, key variables may be maintained within the MK3875 executable RAM during the time that the rest of the microcomputer is powered down.

On the MK3875, two of the pins which are used as bidirectional port pins on the MK3870 are used for the Standby Power feature. Port 0, Bit 0 (PO-0), remains readable and writeable although it is not connected to a package pin. The logic level being applied to the auxiliary

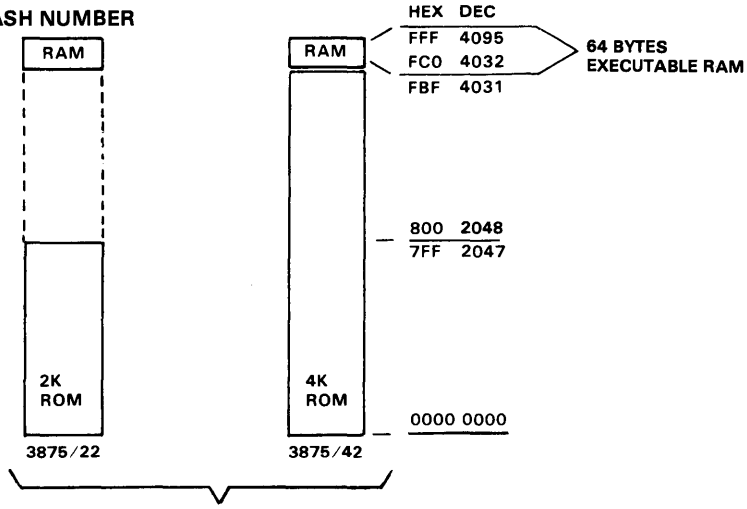
3875 PROGRAMMABLE REGISTERS, PORTS AND MEMORY MAP

Figure 2



MK3875 MAIN MEMORY SIZES AND TYPES BY SLASH NUMBER

Figure 3



All devices contain 64 bytes of scratchpad RAM

Data derived from addressing any locations other than within the specified ROM or RAM space is not tested nor is it guaranteed. Users should refrain from entering this area of the memory map.

Device	Scratchpad RAM Size (Decimal)	Address Register Size (P0,P,DC,DC1)	ROM Size (Decimal)	Executable RAM Size
MK3875/22	64 bytes	12 bits	2048 bytes	64 bytes
MK3875/42	64 bytes	12 bits	4032 bytes	64 bytes

VIII

power supply input (V_{SB}) can be read at Port 0, Bit 1 ($\overline{PO\text{-}1}$). Writing to $\overline{PO\text{-}1}$ has no effect.

A capacitor (.01 microfarads) must be connected between pin 3 (V_{BB}) and ground. V_{BB} is bonded directly to the substrate of the MK3875. The purpose of the capacitor is to decouple noise on the substrate of the circuit when V_{CC} is switched on and off.

It is recommended that Nickel Cadmium batteries (typical voltage of 3 series cells = 3.6V) be used for standby power, since the MK3875 can automatically trickle charge the three NiCads. If more than three cells in series are used, the charging circuit must be provided outside the MK3875.

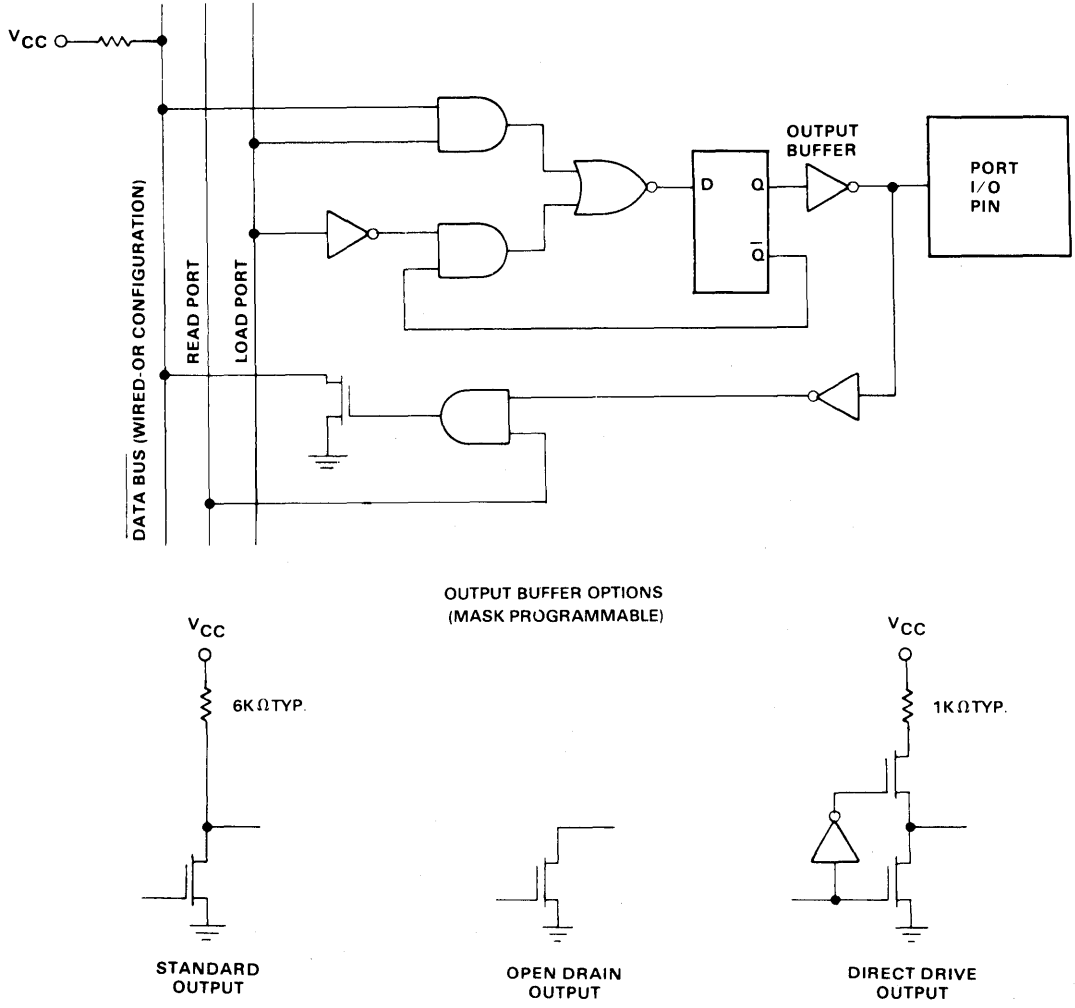
Whenever $\overline{RESET}$ is brought low, the executable RAM is placed in a protected state. Also the RAM is switched from V_{CC} power to the V_{SB} power. When powering down, it may be desirable to interrupt the MK3875 when an impending power down condition is detected, so that the necessary data can be saved before V_{CC} falls below the minimum level. After the save is completed, $\overline{RESET}$ can fall, which prevents any further access of the RAM. The timing for this power down sequence is illustrated in Figure 5A.

A second power down sequence is illustrated in Figure 5B, and may be used if a special save data routine is not needed. The EXT INT line need not be used. Note that for both cases shown in Figures 5A and 5B, $\overline{RESET}$ must be low before V_{CC} drops below the minimum specified operating voltage for the MK3875. This is to ensure that the contents of the executable RAM are not altered during the power down sequence.

There may be a set of variables stored in the RAM memory which is continually updated during the tme when the MK3875 is in its normal operating mode. If a particular variable occupies more than one byte of RAM, there can be a problem if a reset occurs in response to an impending power down condition during the time that the multi-byte variable was being modified. If such a reset occurs, then only part of the variable may contain the updated value, while the rest contains the old value. An example of this case would be when a double precision (2 byte) binary number is being saved in the executable RAM. Suppose that a new value of the number has been calculated in the program, and that this new value is to replace the old value contained in the executable RAM; note that a reset could occur just after the program wrote one byte of the new value

I/O PIN CONCEPTUAL DIAGRAM WITH OUTPUT BUFFER OPTIONS

Figure 4



Ports 0 and 1 are Standard Output type only.

Ports 4 and 5 may both be any of the three output options (mask programmable bit by bit)

The $\overline{\text{STROBE}}$ output is always configured similar to a Direct Drive Output except that it is capable of driving 3 TTL loads.

$\overline{\text{RESET}}$ and EXT INT may have standard 6KΩ (typical) pull-up or may have no pull-up (mask programmable). These two inputs have Schmitt trigger inputs with a minimum of 0.2 volts of hysteresis.

$\overline{\text{RESET}}$ and EXT INT do not have internal pull up on the MK38P75.

into the RAM. When power is restored following the Standby Power mode, the double precision variable would contain an erroneous value.

This problem can be avoided if the external interrupt is used to signal the MK3875 of an impending power down condition. The user's system should be designed so that the MK3875 can properly save all variables between the time that the external interrupt occurs and $\overline{\text{RESET}}$ falls. If multi-byte variables must be saved during the Standby Power mode and it is not desirable to use the external interrupt in the manner described above, then each byte of a multi-byte variable may be kept with an associated flag. The method of updating a two byte variable would be as follows:

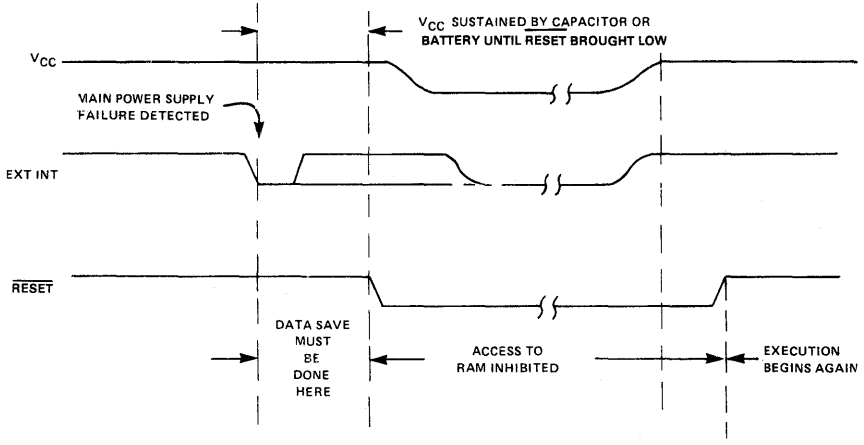
- Clear Flag Word 1
- Update Byte 1
- Set Flag Word 1
- Clear Flag Word 2
- Update Byte 2
- Set Flag Word 2

Now if $\overline{\text{RESET}}$ goes low during the update of a byte of a variable, the flag word associated with that byte of data will be reset. Any byte of the variable where the flag word is "set" is a good byte of data. While this method significantly encumbers the data storage process, it eliminates the need for a power fail interrupt which both reduces external circuitry and leaves the external interrupt pin completely free for other use.

Often it is necessary to distinguish between an initial power-on condition wherein there is no valid data stored in the RAM (or where V_{SB} has dropped below the minimum required stand-by level) and a re-application of power wherein valid RAM data has been maintained during the power outage. One method of distinguishing between these two conditions is to reserve several memory locations for key words and checksums. When V_{CC} is applied and processor operation begins, these locations can be checked for proper contents. However, this method may not be perfectly accurate as those locations holding key codes may be maintained even though V_{SB} drops below its minimum required level while other RAM locations may lose data, or they could power up with the exact data required to match the key codes. Also a checksum may be matched on occasion even though RAM data has been corrupted. The accuracy of this method is improved by increasing the number of memory locations used and the variety of key codes and or checksums used.

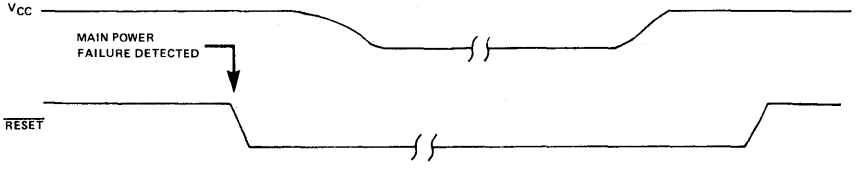
SAVE ROUTINE REQUIRED, $V_{SB} > 3.2$ VOLTS

Figure 5a



NO SAVE ROUTINE REQUIRED, $V_{SB} > 3.2$ VOLTS

Figure 5b

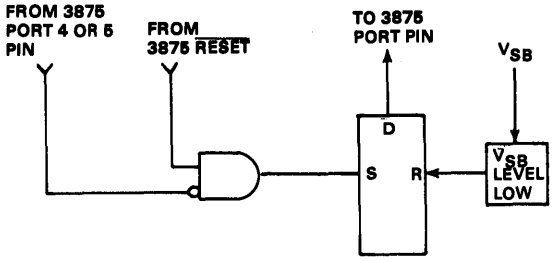


A more reliable method is the external V_{SB} flip-flop. The flip-flop is designed to power up in a known first state and hold that first state until forced into a second state. As long as V_{SB} is above the minimum operating level, the flip-flop can hold the second state, but, if V_{SB} drops below the minimum level, the flip-flop will flip back to the first state. Thus when power is initially applied or if V_{SB} drops below the minimum level during a V_{CC} outage, the flip-flop will be in the first state. The flip-flop output can be read through a port pin by the processor when processor operation begins to determine whether the RAM data is valid (second state) or invalid (first state). If the flip-flop is found to be in the first state it can be forced to the second state by the processor. If it holds the second state, V_{SB} is above the minimum level (batteries are charged).

A conceptual diagram is shown in Figure 6.

CONCEPTUAL DIAGRAM

Figure 6



MK38P75 GENERAL DESCRIPTION

The MK38P75 is the EPROM version of the MK3875. It retains an identical pinout with the MK3875, which is documented in the section of this data sheet entitled "FUNCTIONAL PIN DESCRIPTION". The MK38P75 is housed in the "R" package which incorporates a 28-pin socket located directly on top of the package. A number of standard EPROMs may be plugged into this socket.

The MK38P75 can act as an emulator for the purpose of verification of user code prior to the ordering of mask ROM MK3875 devices. Thus, the MK38P75 eliminates the need for emulator board products. In addition, several MK38P75s can be used in prototype systems in order to test design concepts in field service before commiting to high-volume production with mask ROM MK3875s. The compact size of the MK38P75/EPROM combination allows the packaging of such prototype systems to be the same as that used in production. Finally, in low-volume applications, the MK38P75 can be used as the actual production device.

Most of the material which has been presented for the MK3875 in this document applies to the MK38P75. This includes the description of the pin configuration, architecture, and programming mode. Additional information is presented in the following sections.

MK38P75 I/O PORTS

The MK38P75 is offered with two types of output buffer options on Ports 4 and 5. These are the open drain output buffer and the standard output buffer which are pictured in Figure 4. The open drain version of the MK38P75 is provided so that user-selected open drain port pins on the MK3875 can be emulated prior to ordering those mask ROM devices. Figure 9 lists which version(s) of the MK38P75 has open drain output buffers and which has standard output buffers in parentheses following the specified MK38P75 part ordering number (MK9XXXX).

MK38P75 MAIN MEMORY

As can be seen from the block diagram in Figure 7, the MK38P75 contains executable RAM in the main memory map. The MK38P75 contains no on-chip ROM. Instead, the memory address lines are brought out to the 28-pin socket located directly on top of the 40-pin package, so the external ERPOM memory is addressed as main memory.

There is one memory version of the MK38P75 and it is designated as the MK38P75/02. The MK38P75/02 contains 64 bytes of on-chip executable RAM. The MK38P75/02 can emulate the following devices.

MK3875/22
MK3875/42

The MK38P75/02 cannot exactly emulate the MK3875/40 because of the 64 bytes of executable RAM in the upper ROM space of the MK3875/40.

Addressing of main memory on the MK38P75 is accomplished in the same way as it is for the MK3875. See Figure 8 for main memory addresses and for address register size in the MK38P75.

MK38P75 EPROM SOCKET

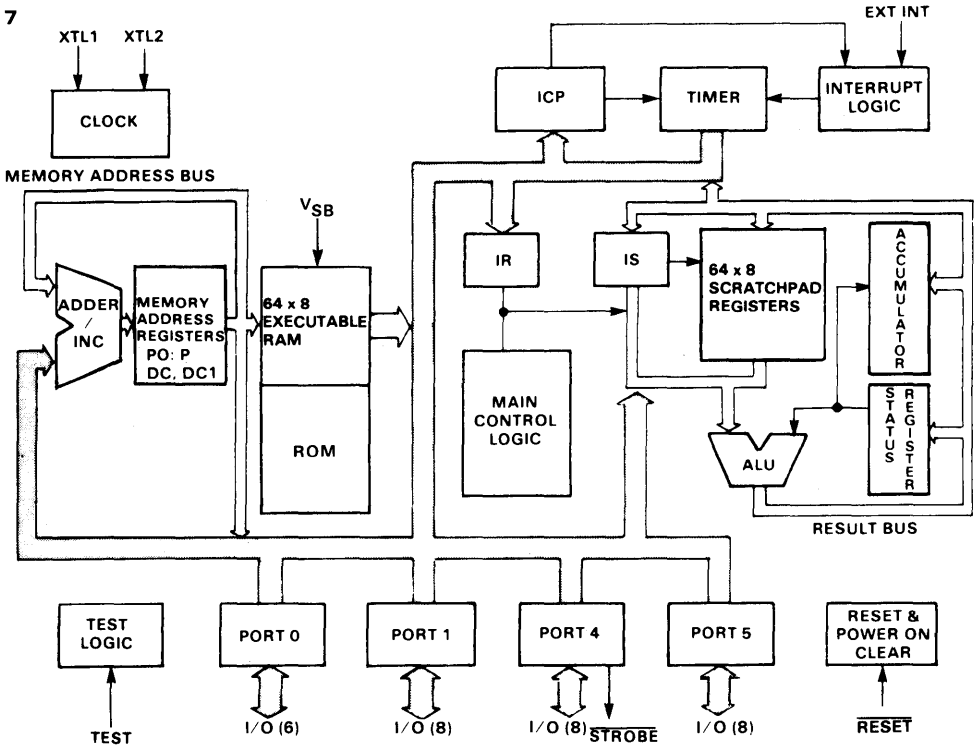
A 28-pin ERPOM socket is located on top of the MK38P75 "R" package. The socket and compatible ERPOM memories are shown in Figure 9. When 24-pin memories are used in the 28-pin socket, they should be inserted so that pin 1 of the memory device is plugged into pin 3 of the socket (the 24-pin memory should be lower justified in the 28-pin socket).

The 28-pin socket has been provided to allow use of both 24-pin and 28-pin memory devices. Minor pin-out differences in the memory devices must be accommodated by providing different versions of the MK38P75.

Initially, the MK38P75 that is compatible with the MK2716 is available. The MK38P75 designed to accommodate the 28-pin memory devices will be available at a later date.

MK38P75 BLOCK DIAGRAM

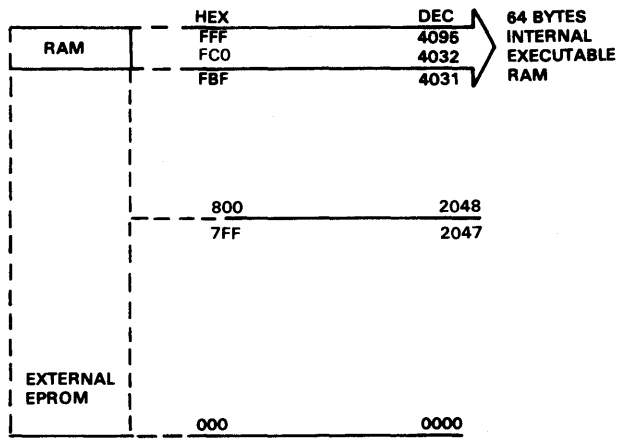
Figure 7



VIII

MK38P75 MAIN MEMORY MAP

Figure 8

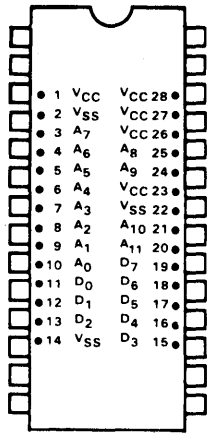


MK38P75/02

Device	Scratchpad RAM Size (Decimal)	Address Register Size P0, P, DC, DC1)	ROM Size (Decimal)	Executable RAM Size
MK38P75/02 97403	64 bytes	12 bits	0 bytes	64 bytes

MK38P75 "R" PACKAGE SOCKET PINOUT

Figure 9



MK97413 (Open Drain Outputs) Compatible Memories
2758
MK2716
2516
2532

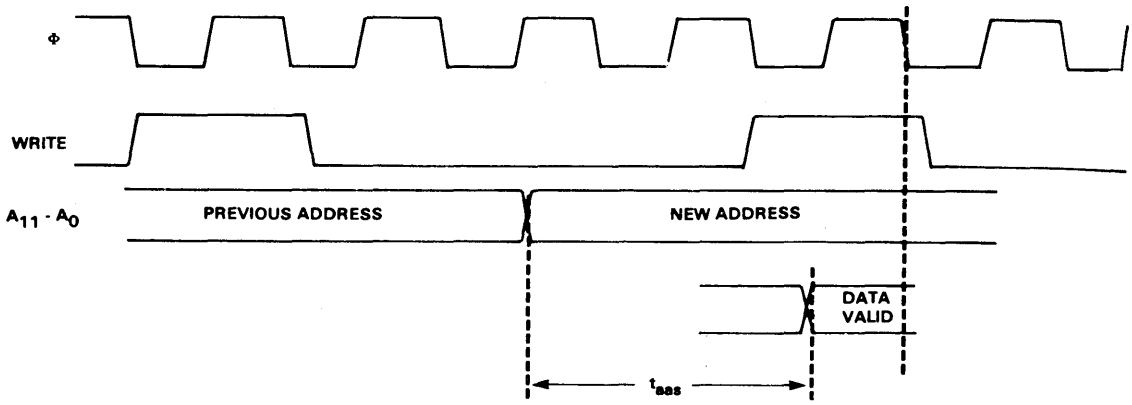
MK97403 (Standard Outputs) Compatible Memories
2758
MK2716
2516
2532

MEMORY ACCESS TIMING

A timing diagram depicting the memory access timing of the MK38P75 is shown in the next table. The Φ clock signal is derived internally in the MK38P75 by dividing the time base frequency by two and is used to establish all timing frequencies. The WRITE signal is another internal signal to the MK38P75 which corresponds to a machine cycle, during which time a memory access may be performed. Each machine cycle is either 4 Φ clock periods or 6 Φ clock periods long. These machine cycles are termed short cycles and long cycles, respectively. The worst case memory cycle is the short cycle, during which time an op code fetch is performed. This is the cycle which is pictured in the timing diagram. After a delay from the falling edge of the WRITE clock, the address lines become stable. Data must be valid at the data out lines of the PROM for a setup time prior to the next falling edge of the WRITE pulse. The total access time available for the MK38P75 version is shown as t_{aas} or the time when address is stable until data must be valid on the data bus lines. The equation for calculating available memory access time along with some calculated access times based on the listed time base frequencies is shown in the following table.

MEMORY ACCESS SHORT CYCLE OP CODE FETCH MK38P75

Figure 10



Φ Signal is internal to the MK38P75

$$t_{aas} = \frac{6}{\text{time base freq.}} - 850 \text{ ns}$$

(FROM ADDRESS STABLE)

	4 MHz	3.5 MHz	3 MHz	2.5 MHz	2 MHz
ACCESS TIME	650 ns	825 ns	1.15 μs	1.55 μs	2.15 μs

3875 TIME BASE OPTIONS

The 3875 contains an on-chip oscillator circuit which provides an internal clock. The frequency of the oscillator circuit is set from the external time base network. The time base for the 3875 may originate from one of four sources:

1) Crystal
2) LC Network
3) RC Network
4) External Clock

The type of network which is to be used with the mask ROM MK3875 must be specified at the time when mask ROM devices are ordered. However, the MK38P75 may operate with any of the four configurations so that it may emulate any configuration used with a mask ROM device.

The specifications for the four configurations are given in the following text. There is an internal 26 pF capacitor between XTL 1 and GND and an internal 26 pF capacitor between XTL 2 and GND. Thus, external capacitors are not necessarily required. In all external clock modes the external time base frequently is divided by two to form the internal PHI clock.

CRYSTAL SELECTION

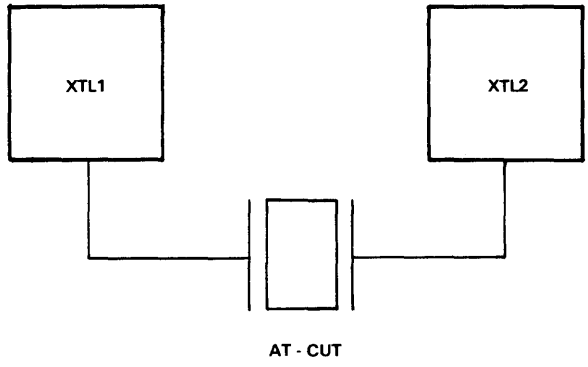
The use of a crystal as the time base is highly recommended as the frequency stability and reproducability from system to system is unsurpassed. The 3875 has an internal divide by two to allow the use of inexpensive and widely available TV Color Burst Crystals (3.58 MHz). Figure 12 lists the required crystal parameters for use with the 3875. The Crystal Mode time base configuration is shown in Figure 11.

Through careful buffering of the XTL1 pin it may be possible to amplify this waveform and distribute it to other devices. However, Mostek recommends that a separate active device (such as a 7400 series TTL gate) be used to oscillate the crystal and that the waveform from that oscillator be buffered and supplied to all devices, including the 3875, in the event that a single crystal is to provide the time base for more than just a single 3875.

While a ceramic resonator may work with the 3875 crystal oscillator, it was not designed specifically to support the use of this component. Thus, Mostek does not support the use of a ceramic resonator either through proper testing, parametric specification, or applications support.

VIII

CRYSTAL MODE CONNECTION
Figure 11



CRYSTAL PARAMETERS

Figure 12

a) Parallel resonance, fundamental mode AT-Cut
b) Shunt capacitance (C_0) = 7 pf max.
c) Series resistance (R_S) = See table
d) Holder = See table below.

Frequency	Series Resistance	Holder
f = 2-2.7 MHz	Rs = 300 ohms max	HC-6 HC-33
f = 2.8-4 MHz	Rs = 150 ohms max	HC-6 HC-18* HC-25* HC-33

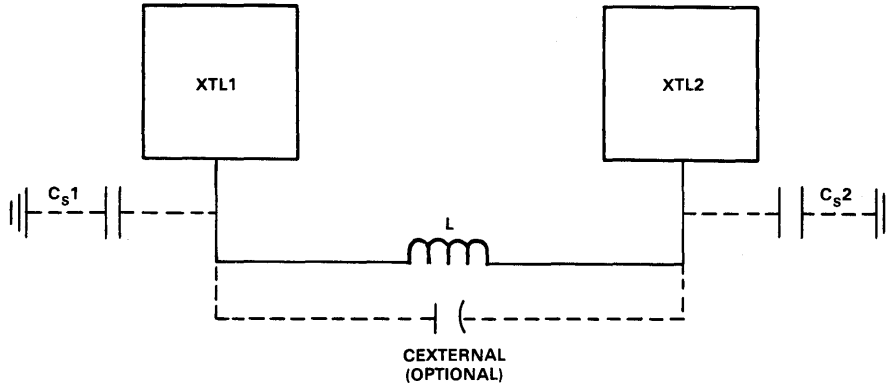
*This holder may not be available at frequencies near the lower end of this range.

LC NETWORK

The LC time base configuration can be used to provide a less expensive time base for the 3875 than can be provided with a crystal. However, the LC configuration is much less accurate than is the crystal configuration. The LC time base configuration is shown in Figure 13. Also shown in the figure are the specified parameters for the LC components, along with the formula for calculating the resulting time base frequency. The minimum value of the inductor which is required for proper operation of the LC time base network is 0.1 millihenries. The inductor must have a Q factor which is no less than 40. The value of C is derived from C external, the internal capacitance of the 3875, C_{XTL}, and the stray capacitances, C_{S1} and C_{S2}. C_{XTL} is the at XTL1 and capacitance looking into the internal two port network XTL2. C_{XTL} is listed under the "Capacitance" section of the Electrical Specifications. C_{S1} and C_{S2} are stray capacitances from XTL1 to ground and from XTL2 to ground, respectively. C external should also include the stray shunt capacitance across the inductor. This is typically in the 3 to 5 pf range and significant error can result if it is not included in the frequency calculation.

LC MODE CONNECTION

Figure 13

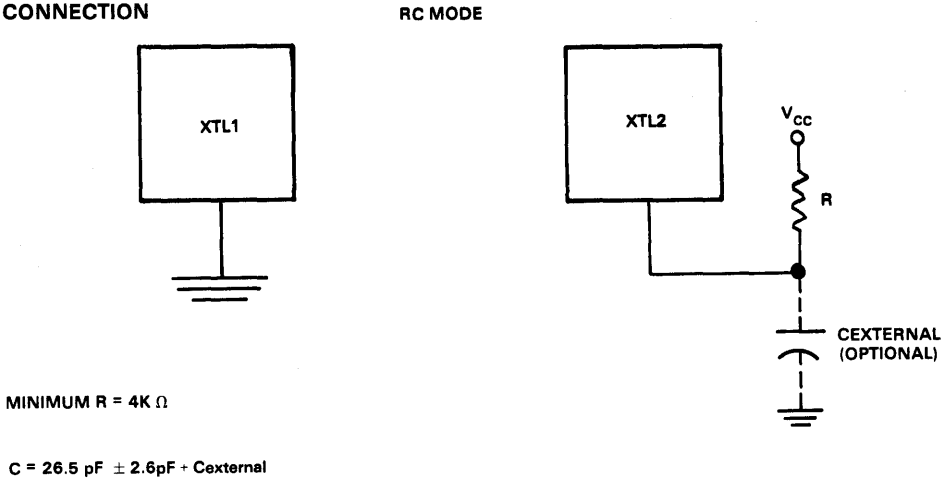


Variation in time base frequency with the LC network can arise from one of four sources: 1) Variation in the value of the inductor. 2) Variation in the value of the external capacitor. 3) Variation in the value of the internal capacitance of the 3875 at XTL1 and XTL2, and 4) Variation in the amount of stray capacitance which exists in the circuit. Therefore, the actual frequency which is generated by the LC circuit is within a range of possible frequencies, where the range of frequencies is determined by the worst case variation in circuit parameters. The designer must select component values such that the range of possible frequencies with the LC mode does not go outside of the specified operating frequency range for the 3875.

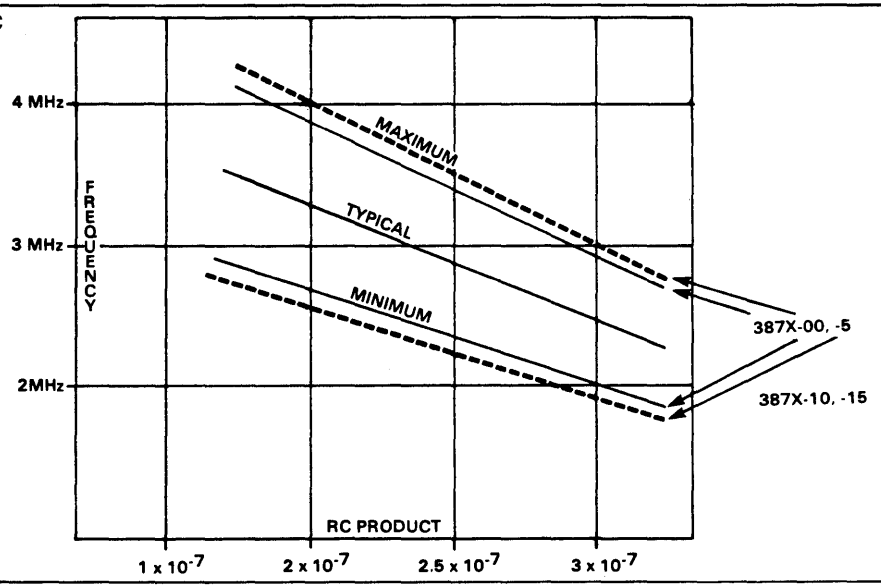
RC CLOCK CONFIGURATION

The time base for the 3875 may be provided from an RC network tied to the XTL2 pin, when XTL1 is grounded. A schematic picturing the RC clock configuration is shown in Figure 14. The RC time base configuration is intended to provide an inexpensive time base source for applications in which timing is not critical. Some users have elected to tune each unit using a variable resistor or external capacitor thus reducing the variation in frequency. However, for increased time base accuracy Mostek recommends the use of the Crystal or LC time base configuration. Figure 15 illustrates a curve which gives the resulting operating frequency for a particular RC value. The x-axis represents the product of the value of the resistor times the value of the capacitor. Note that three curves are actually shown. The curve in the middle represents the nominal frequency obtained for a given value of RC. A maximum curve and a minimum curve for different types of 3875 devices are also shown in the diagram.

RC MODE CONNECTION
Figure 14



FREQUENCY VS. RC
Figure 15



VIII

The designer must select the RC product such that a frequency of less than 2 MHz is not possible taking into account the maximum possible RC product and using the minimum curve shown in Figure 15. Also, the RC product must not allow a frequency of more than 4 MHz taking into account the minimum possible R and C and using the Maximum curve shown. Temperature induced variations in the external components should be considered in calculating the RC product.

Frequency variation from unit to unit due to switching speed and level at constant temperature and V_{CC} = + or - 5 percent.

Frequency variation due to V_{CC} with all other parameters constant with respect to +5V = +7 percent to -4 percent on all devices.

Frequency variation due to temperature with respect to 25 C (all other parameters constant) is as follows:

PART #	VARIATION
387X-00, -05	+6 percent to - 9 percent
387X-10, -15	+9 percent to -12 percent

Variations in frequency due to variations in RC components may be calculated as follows:

Maximum RC = (R max) (C external max + C_{XTL} max)

Minimum RC = (R min) (C external min + C_{XTL} min)

$$\text{Typical RC} = (\text{R typ})\left(\text{C external typ} + \frac{\{C_{XTL}\ \text{max} + C_{XTL}\ \text{min}\}}{2}\right)$$

Positive Freq. Variation = $\frac{\text{RC typical - RC minimum}}{\text{RC typical}}$

Negative Freq. Variation due to RC Components = $\frac{\text{RC maximum - RC typical}}{\text{RC typical}}$

Total frequency variation due to all factors:

387X-00, -05	387X-10, -15
= +18 percent plus positive frequency variation due to RC components	= +21 percent plus positive frequency variation due to RC components
= -18 percent minus negative frequency variation due to RC components	= -21 percent minus negative frequency variation due to RC components

Total frequency variation due to V_{CC} and temperature of a unit tuned to frequency at +5V V_{CC}, 25 C

387X-00, -05	387X-10, -15
= + 13 percent	= + 16 percent

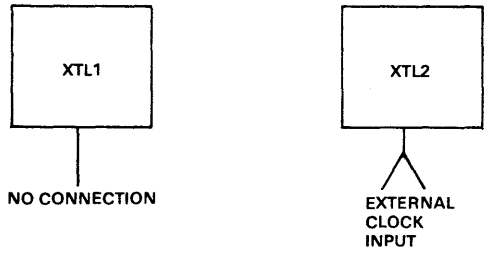
EXTERNAL CLOCK CONFIGURATION

The connection for the external clock time base configuration is shown in Figure 16. Refer to the DC Characteristics section for proper input levels and current requirements.

Refer to the Capacitance section of the appropriate 3875 Family device data sheet for input capacitance.

EXTERNAL MODE CONNECTION

Figure 16



OPERATING VOLTAGES AND TEMPERATURES

Dash Number Suffix	Operating Voltage V_{CC}	Operating Temperature T_A
- 00	+5V ± 10%	0°C - 70°C
- 05	+5V ± 5%	0°C - 70°C
- 10	+5V ± 10%	-40°C - +85°C
- 15	+5V ± 5%	-40°C - +85°C

See order information for explanation of part numbers.

ABSOLUTE MAXIMUM RATINGS*

	-00, -05	-10, -15
Temperature Under Bias	-20°C +85°C	-50°C to 100°C
Storage Temperature	-65°C +150°C	-65°C to +150°C
Voltage on any Pin With Respect to Ground (Except open drain pins and TEST)	-1.0V to +7V	-1.0V to +7V
Voltage on TEST with Respect to Ground	-1.0V to +9V	-1.0V to +9V
Voltage on Open Drain Pins with Respect to Ground	-1.0V to +13.5V	-1.0V to 13.5V
Power Dissipation	1.5W	1.5W
Power Dissipation by any one I/O pin	60mW	60mW
Power Dissipation by all I/O pins	600mW	600mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating and conditions for extended periods may affect device reliability.

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation < 100mW (Note 4)

SIGNAL	SYM	PARAMETER	-00,-05 MIN	-00,-05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	250	500	ns	4MHz-2MHz
	$t_{ex(H)}$	External clock pulse width high	90	400	100	390	ns	
	$t_{ex(L)}$	External clock pulse width low	100	400	110	390	ns	
Φ	t_Φ	Internal Φ clock	$2t_O$		$2t_O$			
WRITE	t_W	Internal WRITE Clock period	4 t Φ 6 t Φ		4tΦ 6tΦ			Short Cycle Long Cycle
I/O	$t_{dI/O}$	Output delay from internal WRITE clock	0	1000	0	1200	ns	50pF plus one TTL load
	$t_{sI/O}$	Input setup time to internal WRITE clock	1000		1200		ns	
$\overline{STROBE}$	$t_{I/O-s}$	Output valid to $\overline{STROBE}$ delay	3tΦ -1000	3tΦ +250	3tΦ -1200	3tΦ +300	ns	I/O load = 50fF + 1 TTL load
	t_{sL}	$\overline{STROBE}$ low time	8tΦ -250	12tΦ +250	8tΦ -300	125Φ +300	ns	$\overline{STROBE}$ load = 50pF + 3TTL loads
$\overline{RESET}$	t_{RH}	$\overline{RESET}$ hold time, low	6tΦ +750		6tΦ +1000		ns	
	t_{RPOC}	$\overline{RESET}$ hold time, low for power clear	power supply rise time +5.0		power supply rise time +5.5		ms	
EXT INT	t_{EH}	EXT INT hold time in active and inactive state	6tΦ +750		6tΦ +1000		ns	To trigger interrupt
			2tΦ		2tΦ		ns	To trigger timer

VIII

AC CHARACTERISTICS FOR MK38P75

(Signals brought out at socket)
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW. (Note 2)

SYMBOL	PARAMETER	-00, -05		-10, -15		UNIT	CONDITION
		MIN	MAX	MIN	MAX		
t_{aas}*	Access time from Address A_{11}-A_0 stable until data must be valid at D_7-D_0	650		650		ns	Φ = 2.0 MHz

*See Table in Figure 10

CAPACITANCE

T_A = 25°C All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O $\overline{\text{RESET}}$, EXT INT, TEST		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

DC CHARACTERISTICS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100mW (Note 4)

SYM	PARAMETER	-00,-05		-10,-15		UNIT	NOTES
		MIN	MAX	MIN	MAX		
I_{CC}	Average Power Supply Current		94		125	mA	Outputs Open (5)
P_D	Average Power Dissipation		440		575	mW	Outputs Open (6)
V_{IHEX}	External Clock input high level	2.4	5.8	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	-.3	.6	V	
I_{IHEX}	External Clock input high current		100		130	μA	$V_{IHEX}=V_{CC}$
I_{ILEX}	External Clock input low current		-100		-130	μA	$V_{ILEX}=V_{SS}$
$V_{IHI/O}$	Input high level, I/O pins	2.0	5.8	2.0	5.8	V	Standard Pull-Up (1,2)
		2.0	13.2	2.0	13.2	V	Open Drain (1,3)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	2.2	5.8	V	Standard Pull-Up(1, 2)
		2.0	13.2	2.2	13.2	V	No Pull-Up (1,3)
V_{IHEI}	Input high level, EXT INT	2.0	5.8	2.2	3.8	V	Standard Pull-Up(1, 2)
		2.0	13.2	2.2	13.2	V	No Pull-Up (1,3)
V_{IL}	I/O ports, $\overline{\text{RESET}}$, EXT INT input low level	-.3	.8	-.3	.7	V	
V_{ILRPT}	$\overline{\text{RESET}}$ input low level to protect RAM during loss at V_{CC}	-.3	.4	-.3	.4	V	
I_{IL}	Input low current, standard pull-up pins		-1.6		-1.9	mA	V_{IN}=0.4V (2)

DC CHARACTERISTICS (Continued)

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 4)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	NOTES
I_L	Input leakage current, open drain pins Reset and EXT INT inputs With no pull-up resistor		+10 -5		+18 -8	μA μA	V_{IN}=13.2V V_{IN}=0.0V (3)
I_{OH}	Output high current, standard	-100		-89		μA	V_{OH}=2.4V
	Pull-Up pins	-30		-25		μA	V_{OH}=3.9V
I_{OHDD}	Output high current	-100		-80		μA	V_{OH}=2.4V
	Direct Drive pins	-1.5		-1.3		mA	V_{OH}=1.5V
			-8.5		-11	mA	V_{OH}=0.7V
I_{OL}	Output low current, I/O ports	1.8		1.65		mA	V_{OL}=0.4V
I_{OHS}	STROBE Output High current	-300		-270		μA	V_{OL}=2.4V
I_{OLS}	STROBE output low current	5.0		4.5		mA	V_{OL}=0.4V

DC CHARACTERISTICS FOR STANDBY POWER PINS

V_{CC}, T_A within operating range I/O Power Dissipation ≤ 100 mW (Note 4)

SYMBOL	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10,-15 MIN	-10,-15 MAX	UNIT	NOTES
V_{SB}	Standby V_{CC} for RAM	3.2	V_{CC} MAX	3.2	V_{CC} MAX	V	
I_{SB}	Standby Current		6		7.5	mA	V_{SB} = V_{SB} MAX
			3.7		5.0	mA	V_{SB} = V_{SB} MIN
I_{CHARGE}	Trickle charge available on V_{SB} with V_{CC} in operating range.	-.8		-.7		mA	V_{SB} = 3.8V
			-15		-19	mA	V_{SB} = 3.2V

DC CHARACTERISTICS FOR MK38P75

(Signals brought out at socket)
T_A, V_{CC} within specified operating range, I/O power dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	-00, -05 MIN	-00, -05 MAX	-10, -15 MIN	-10, -15 MAX	UNIT	CONDITION
I_{CCE}	Power Supply Current for EPROM		-185		-185	mA	
V_{IL}	Input Low Level Data bus in	-0.3	0.8	-0.3	0.8	V	
V_{IH}	Input High Level Data bus in	2.0	5.8	2.0	5.8	V	
I_{OH}	Output High Current	-100		-90		μA	V_{OH}=2.4 V
		-30		-25		μA	V_{OH}=3.9 V
I_{OL}	Output Low Current	1.8		1.65		mA	V_{OL}=0.4 V
I_{IL}	Input Leakage Current		10		10	μA	Data Bus in Float

VIII

1. $\overline{\text{RESET}}$ and ET INT have internal Schmit triggers giving minimum .2V hysteresis.
2. $\overline{\text{RESET}}$ and EXT INT prgrammed with standard pull-up
3. $\overline{\text{RESET}}$ or EXT INT programmed without standard pull-up
4. Power dissipation for I/O pins is calculated by $\Sigma (V_{CC} - V_{IL}) (|I_{IL}|) + \Sigma (V_{CC} - V_{OH}) (|I_{OH}|) + \Sigma (V_{OL}) (I_{OL})$
5. I_{CC} exclusive of I_{charge}.
6. P_D exclusive of battery charging power. Battery charging power dissipated inside the MK3875 $(V_{CC} - V_{SB}) (I_{charge})$.

TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value - actual time value

tpsc = tΦ x Prescale Value

Interval Timer Mode

Single interval error, free running (Note 3)	±6tΦ
Cumulative interval error, free running (Note 3)	0
Error between two Timer reads (Note 2)	±(tpsc + tΦ)
Start timer to stop Timer error (Notes 1, 4)	+tΦ to - (tpsc + tΦ)
Start Timer to read Timer error (Notes 1, 2)	-5tΦ to -(tpsc + 7tΦ)
Start Timer to interrupt request error (Notes 1, 3)	-2tΦ to -8tΦ
Load Timer to stop Timer error (Note 1)	+tΦ to -(tpsc + 2tΦ)
Load Timer to read Timer error (Notes 1, 2)	-5tΦ to -(tpsc + 8tΦ)
Load Timer to interrupt request error (Notes 1, 3)	-2tΦ to -9tΦ

Pulse Width Measurement Mode

Measurement accuracy (Note 4)	+t Φ to -(tpsc +2t Φ
Minimum pulse width of EXT INT pin	2t Φ

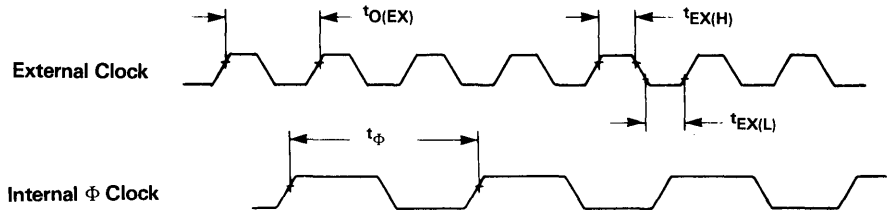
Event Counter Mode

Minimum active time of EXT INT pin	2t Φ
Minimum inactive time of EXT INT pin	2t Φ

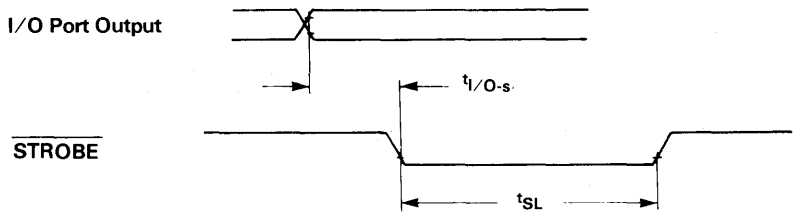
Notes:

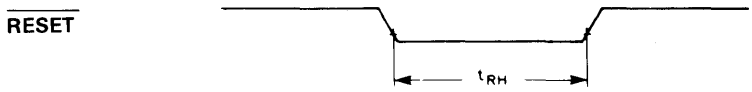
1. All times which entail loading, starting, or stopping the Timer are referenced from the end of the last machine cycle of the OUT or OUTS instruction.
2. All times which entail reading the Timer are referenced from the end of the last machine cycle of the IN or INS instruction.
3. All times which entail the generation of an interrupt request are referenced from the start of the machine cycle in which the appropriate interrupt request latch is set. Additional time may elapse if the interrupt request occurs during a privileged or multicycle instruction.
4. Error may be cumulative if operation is repetitively performed.

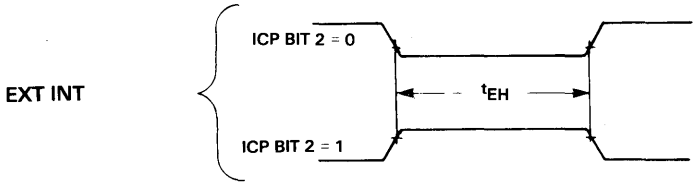
AC TIMING DIAGRAM
Figure 17



Input capacitance; I/O, $\overline{\text{RESET}}$, EXT INT,





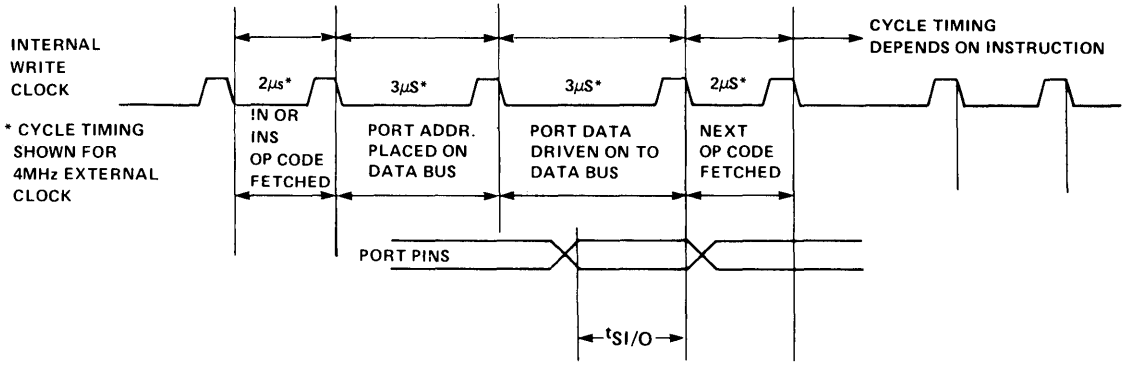


Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v).

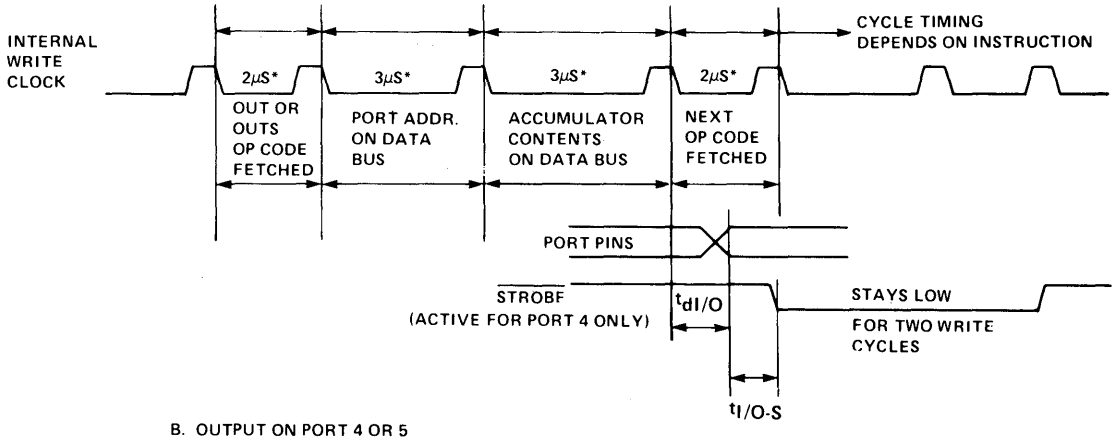
VIII

INPUT/OUTPUT AC TIMING

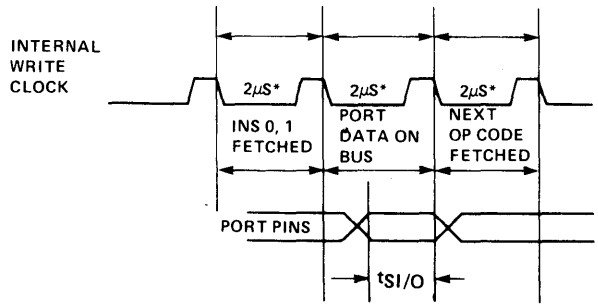
Figure 18



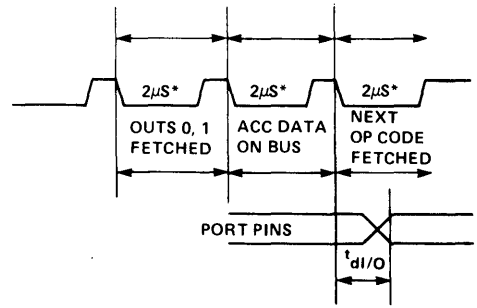
A. INPUT ON PORT 4 OR 5



B. OUTPUT ON PORT 4 OR 5



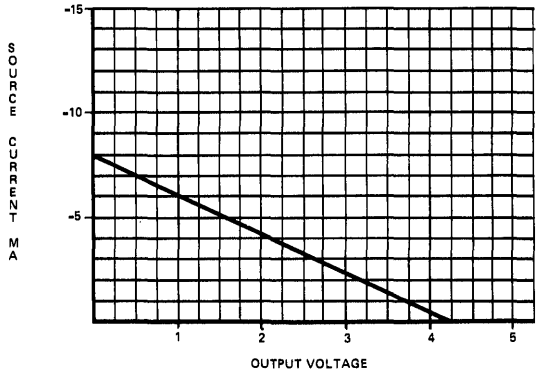
C. INPUT ON PORT 0 OR 1



D. OUTPUT ON PORT 0, 1

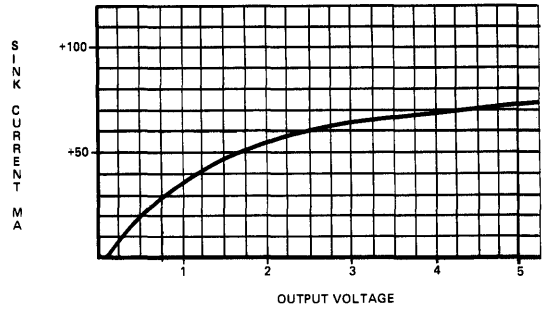
STROBE SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 19



STROBE SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

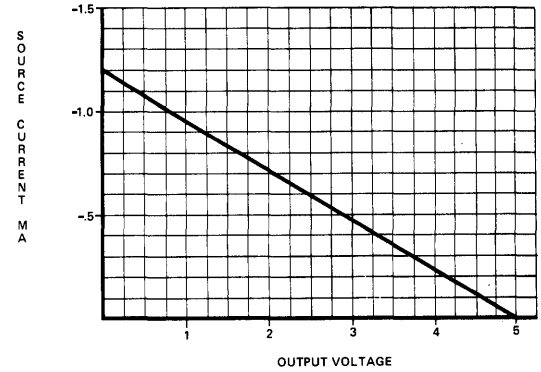
Figure 20



VIII

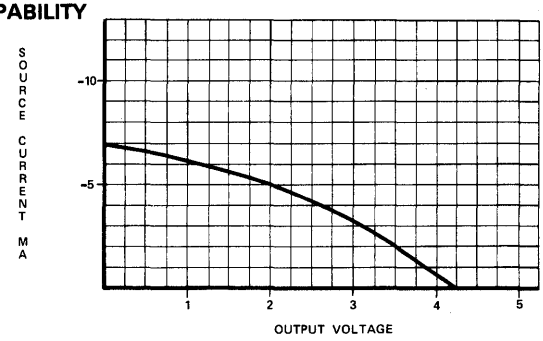
STANDARD I/O PORT SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 21



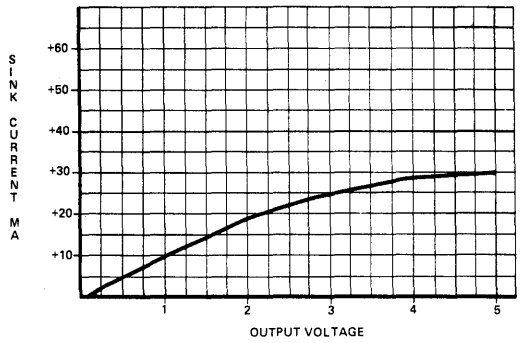
DIRECT DRIVE I/O PORT SOURCE CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 22



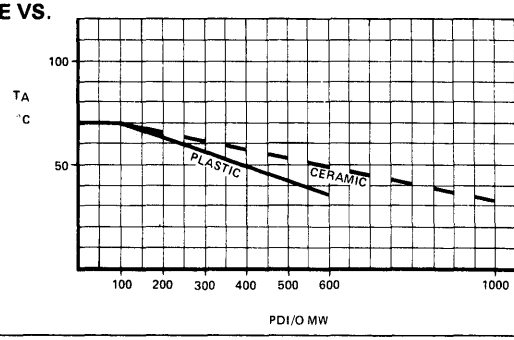
I/O PORT SINK CAPABILITY (TYPICAL AT V_{CC} = 5V, T_A = 25°C)

Figure 23



MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 24

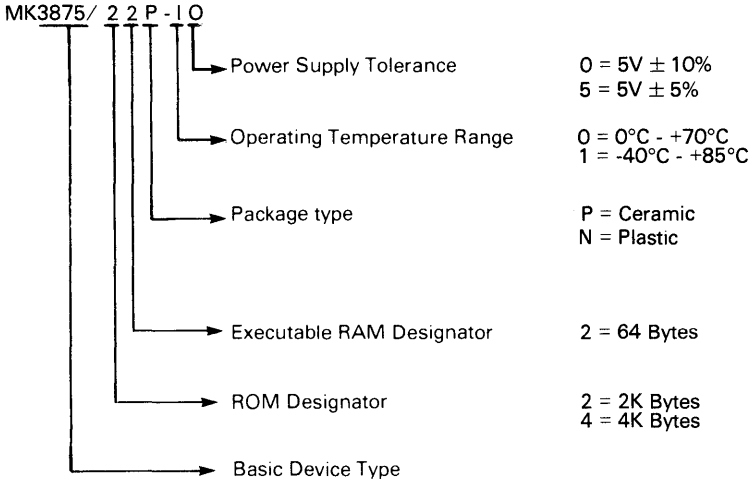


ORDERING INFORMATION

There are two types of part numbers for the 3870 family of devices. The generic part number describes the basic device type, the amount of ROM and executable RAM, the desired package type, temperature range and power supply tolerance. For each customer specific code, additional information defining I/O options and oscillator options will be combined with the information described in the generic part number to define a customer/code specific device order number.

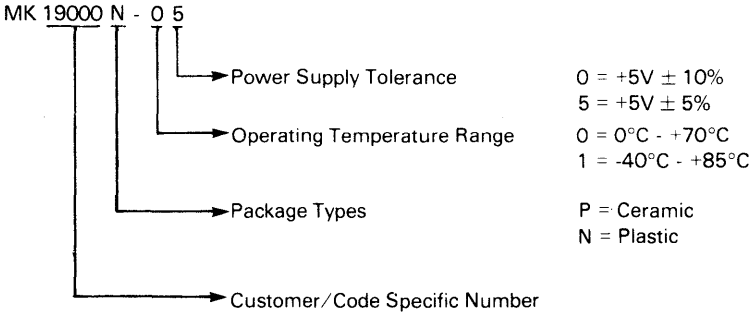
GENERIC PART NUMBER

An example of the generic part number is shown below.



DEVICE ORDER NUMBER

An example of the device order number is shown below.



The customer/code specific number defines the ROM bit pattern, I/O configuration, oscillator type, and generic part type to be used to satisfy the requirement of a particular customer purchase order. For further information on the ordering of mask ROM devices, the customer should refer to the 3870 Family Technical Manual.

VIII

1984/1985 MICROELECTRONIC DATA BOOK

PRELIMINARY

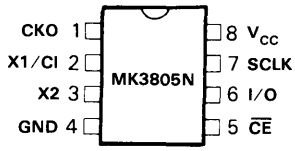
CMOS MICROCOMPUTER CLOCK/RAM MK3805N

FEATURES

- Real-time clock counts seconds, minutes, hours, date of the month, day of the week, month, and year. Every 4th year, February has 29 days.
- Serial I/O for minimum pin count (8 pins)
- 24 x 8 RAM for scratchpad data storage
- Simple Microcomputer interface
- High speed shift clock independent of crystal oscillator frequency
- Single byte or multiple byte (Burst Mode) data transfer capability for read or write of clock or RAM data.
- TTL Compatible (V_{CC} = 5V)
- Low-power CMOS

PIN OUT

Figure 1



PIN DESCRIPTION

Table 1

PIN 3805N	NAME	DESCRIPTION
1	CKO	Buffered System Clock Output
2	X1/C1	Crystal or External Clock Input
3	X2	Crystal Input
4	GND	Power Supply Pin
5	$\overline{CE}$	Chip Enable for Serial I/O Transfer
6	I/O	Data Input/Output Pin
7	SCLK	Shift Clock for Serial I/O Transfer
8	V_{CC}	Power Supply Pin

IX

GENERAL DESCRIPTION

Many microprocessor applications require a real-time clock and/or memory that can be battery powered with very low power drain. The MK3805N is specifically designed for these applications. The device contains a real-time clock/calendar, 24 bytes of static RAM, an on-chip oscillator, and it communicates with the microprocessor via a simple serial interface. The MK3805N is fabricated using CMOS technology, thus ensuring very low power consumption.

The real-time clock/calendar provides seconds, minutes, hours, day, date, month, and year information to the microprocessor. The end of the month date is automatically adjusted for months with less than 31 days, including correction for leap year every 4 years. The clock operates in either the 24 hour or 12 hour format with an AM/PM indicator.

The on-chip oscillator provides a real-time clock source for the clock/calendar. It incorporates a programmable divider so that a wide variety of crystal frequencies can be accommodated. The oscillator also has an output available that can be connected to the microprocessor clock input. A separately programmable divider provides several different output frequencies for any given crystal frequency. This feature can eliminate having to use a separate crystal or external oscillator for the microprocessor, thereby reducing system cost.

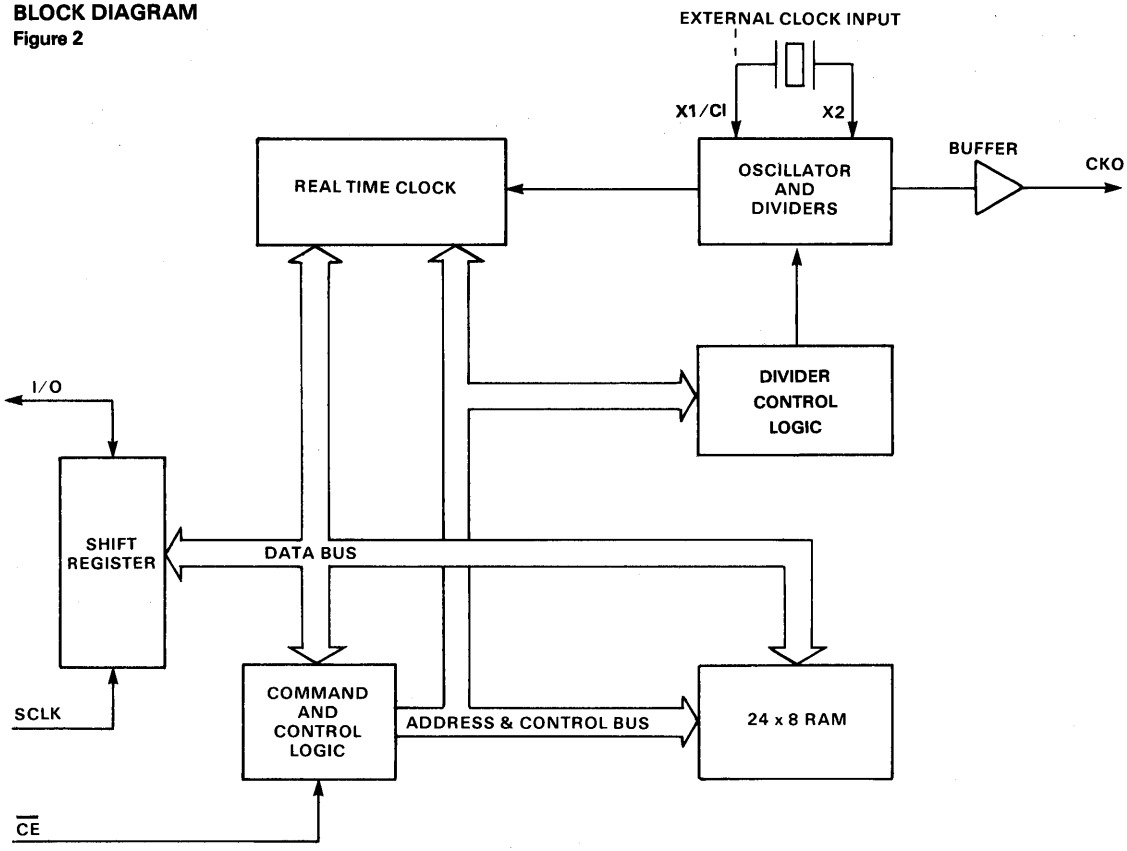
Interfacing the CLOCK/RAM with a microprocessor is greatly simplified using synchronous serial communication. Only 3 lines are required to communicate with the CLOCK/RAM: (1) $\overline{CE}$ (chip enable), (2) I/O (data line) and (3) SCLK (shift register clock). Data can be transferred to and from the CLOCK/RAM one byte at a time or in a burst of up to 24 bytes.

TECHNICAL DESCRIPTION

Figure 2 is a block diagram of the CLOCK/RAM chip. Its main elements are the oscillator and divider circuit, divider control logic, the real-time clock/calendar, static RAM, the serial shift register, and the command and control logic.

The shift register is used to communicate with the outside world. Data on the I/O line is either input or output on each shift register clock pulse when the chip is enabled. If the chip is in the input mode, the data on the I/O line is input to the shift register on the rising edge of SCLK. If in the output

BLOCK DIAGRAM
Figure 2



mode, data is shifted out onto the I/O line on the falling edge of SCLK.

The command and control logic receives the first byte input by the shift register after $\overline{CE}$ goes active. This byte must be the command byte and will direct further operations within the CLOCK/RAM. The command specifies whether subsequent transfers will be data input or data output, and which register or RAM location will be involved.

A control register provides programmable control of the divider for the internal clock signal, the external clock signal, the crystal type and mode, and the write protect function.

The real-time clock/calendar is accessed via seven dynamic registers. These registers are seconds, minutes, hours, day, date, month, and year. Certain bits within these registers also control a run/stop function, 12/24 hour format, and indicate AM or PM (12 hour mode only). These registers can be accessed sequentially in Burst Mode, or randomly in a single byte transfer.

The static RAM is organized as 24 bytes of 8-bits each. They can be accessed either sequentially in burst mode, or randomly in a single byte transfer.

POWER UP

A time base on the crystal input pins is necessary for correct power up. This time base can be provided by a crystal or it can be derived from another generated clock source. It should be noted that a delay exists between power up and the correct power up state of the clock and control registers.

DATA TRANSFER

Data Transfer is accomplished under control of the $\overline{CE}$ and SCLK inputs by an external microcomputer. Each transfer consists of a single byte ADDRESS/COMMAND input followed by a single byte or multiple byte (if Burst Mode is specified) data input or output, as specified by the ADDRESS/COMMAND byte. The serial data transfer occurs with LSB first, MSB last format.

ADDRESS/COMMAND BYTE

The ADDRESS/COMMAND Byte is shown below:

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A4	A3	A2	A1	A0	Rd / $\overline{W}$

As defined, the MSB (bit 7) must be a logical 1; bit 6 specifies a Clock/Calendar/Control register if logical 0 or a RAM register if logical 1; bits 1-5 specify the designated register(s) to be input or output; and the LSB (bit 0) specifies a WRITE operation (input) if logical 0 or READ operation (output) if logical 1.

BURST MODE

Burst Mode may be specified for either the Clock/Calendar/Control registers or for the RAM registers by addressing location 31 Decimal (ADDRESS/COMMAND bits 1-5 = logical 1). As before, bit 6 specifies Clock or RAM and bit 0 specifies read or write.

There is no data storage capability at location 31 in either the Clock/Calendar/Control registers or the RAM registers.

SCLK and $\overline{CE}$ CONTROL

All data transfers are initiated by $\overline{CE}$ going low. After $\overline{CE}$ goes low, the next 8 SCLK cycles input an ADDRESS/COMMAND byte of the proper format. An SCLK cycle is the sequence of a positive edge followed by a negative edge. For data inputs, the data must be valid during the SCLK cycle. If bit 7 is not a logical 1, indicating a valid CLOCK/RAM ADDRESS/COMMAND, the ADDRESS/COMMAND byte is ignored as are all SCLK cycles until $\overline{CE}$ goes high and returns low to initiate a new ADDRESS/COMMAND transfer. See Figure 3.

ADDRESS/COMMAND bits and DATA bits are input on the rising edge of SCLK, and DATA bits are output on the falling edge of SCLK.

A data transfer terminates if $\overline{CE}$ goes high, and the transfer must be reinitiated by the proper ADDRESS/ COMMAND when $\overline{CE}$ again goes low. The data I/O pin is high impedance when $\overline{CE}$ is high.

DATA INPUT

Following the 8 SCLK cycles that input the WRITE Mode ADDRESS/COMMAND byte (bit 0 = logical 0), a DATA byte is input on the rising edge of the next 8 SCLK cycles (per byte, if Burst Mode is specified). Additional SCLK cycles are ignored should they inadvertently occur.

DATA OUTPUT

Following the 8 SCLK cycles that input the READ Mode ADDRESS/COMMAND byte (bit 0 = logical 1), a DATA byte is output on the falling edge of the next 8 SCLK cycles (per byte, if Burst Mode is specified). Note that the first data bit to be transmitted from the CLOCK/RAM occurs on the falling edge of the last bit of the command byte. Additional SCLK cycles retransmit the data byte(s) should they inadvertently occur, so long as $\overline{CE}$ remains low. This operation permits continuous Burst Read Mode capability.

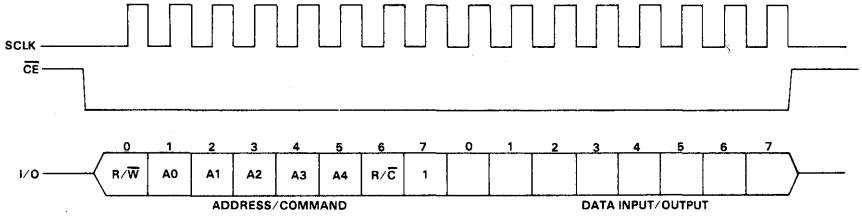
DATA TRANSFER SUMMARY

A data transfer summary is shown in Figure 3.

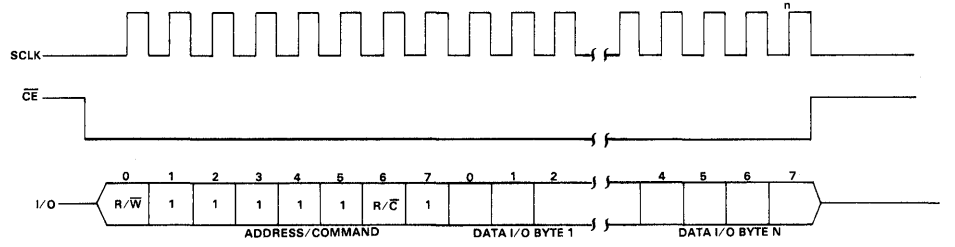
DATA TRANSFER SUMMARY

Figure 3

I. SINGLE BYTE TRANSFER



II. BURST MODE TRANSFER



NOTES

1) Data input sampled while SCLK is high
2) Data output changes on falling edge of clock
3) Rising edge of $\overline{CE}$ terminates operation and resets address/command

FUNCTION	BYTE N	SCLK n
CLOCK	8	72
RAM	24	200

IX

REGISTER DEFINITION

CLOCK/CALENDAR

The Clock/Calendar is contained in 7 writeable/readable registers, as defined below.

Address	Function	Range (BCD)
0	Seconds+Clock Halt Flag	00-59
1	Minutes	00-59
2	Hours/AM-PM/12-24 Mode	00-23 or 01-12
3	Date	01-28,29, 30,31
4	Month	01-12
5	Day	01-07
6	Year	00-99

Data contained in the Clock/Calendar registers is in binary coded decimal format (BCD).

CLOCK HALT FLAG

Bit 7 of the Seconds Register is defined as the Clock Halt Flag. Bit 7 = logical 1 inhibits the 1 Hz input to the Clock/Calendar. Bit 7 is set to logical 1 on power-up to prevent counting, and it may be set high or low by writing to the seconds register under normal operation of the device.

AM-PM/12-24 MODE

Bit 7 of the Hours Register is defined as the 12 or 24 hour mode select bit. When high, the 12 hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

TEST MODE BITS

Bit 7 of the Date Register and Bit 7 of the Day Register are Test Mode Bits utilized in testing the MK3805N. These bits should be logic 0 for normal operation.

CONTROL REGISTER

The Control Register specifies the crystal mode/frequency to be used, the system clock output frequency, and the WRITE PROTECT Mode for data protection. The Control Register is located at address 7 in the Clock/Calendar/Control address space.

7	6	5	4	3	2	1	0
WP	C1	C0	X4	X3	X2	X1	X0

CRYSTAL DIVIDER MODE

X4 and X3 specify the Crystal frequency divider mode selected.

X4	X3	Xtal Mode	Primary Frequencies
0	0	Binary	2^{22}, 2^{21}, 2^{20} Hz
0	1	Microprocessor	8, 5, 4, 2.5, 2, 1.25, 1 MHz
1	0	Baud Rate	7.3728, 3.6864, 1.8432 MHz
1	1	Color Burst	3.5795 MHz

CRYSTAL DIVIDER PRESCALER

X2, X1, and X0 specify a particular prescaler divider selection necessary to generate a 1 Hz frequency for the Clock/Calendar. Refer to Table 2 for complete definition.

SYSTEM CLOCK OUTPUT

C1 and C0 designate the system clock output frequency selected. The options are X, X/2, X/4, and ~2 kHz. When in the Binary Mode and C1, C0 = '1', the output frequency is 2048 Hz. In any other mode the output frequency is ~2048 Hz. Refer to Table 3 for complete definition.

WRITE PROTECT

Bit 7 of the Control Register is the WRITE PROTECT Flag. Bit 7 is set to logical 1 on power-up, and it may be set high or low by writing to the Control Register. When high, the WRITE PROTECT Flag prevents a write operation to any internal register, including the other bits of the Control Register. Further, logic is included such that the WRITE PROTECT bit may be reset to a logic 0 by a Write operation without altering the other bits of the Control Register.

CLOCK/CALENDAR/CONTROL BURST MODE

Address 31 Decimal of the Clock/Calendar/Control Address space specifies Burst Mode operation. In this mode, the 7 Clock/Calendar Registers and the Control Register may be consecutively read or written. Addresses above address 7 (Control Register) are non-existent; only addresses 0-7 are accessible.

RAM

The static RAM is contained in 24 writeable/readable registers, addressed consecutively in the RAM address space beginning at location 0.

RAM BURST MODE

Address 31 Decimal of the RAM address space specifies Burst Mode operation. In this mode, the 24 RAM registers may be consecutively read or written. Addresses above the maximum RAM address location are non-existent and are not accessible.

REGISTER SUMMARY

A Register, Data Format summary is shown in Figure 4.

MICROCOMPUTER CLOCK/RAM ADDRESS/COMMAND REGISTER, DATA FORMAT SUMMARY

Figure 4

I. ADDRESS/COMMAND FORMAT

7	6	5	4	3	2	1	0
1	RAM / $\overline{CK}$	A_4	A_3	A_2	A_1	A_0	RD / $\overline{W}$

II. REGISTER ADDRESS

A. CLOCK

	7	6	5	4	3	2	1	0	REGISTER DEFINITION	7	4	3	0	POWER ON RESET
SEC	1	0	0	0	0	0	0	RD / $\overline{W}$	00-59	CH	10 SEC		SEC	80
MIN	1	0	0	0	0	0	1	RD / $\overline{W}$	00-59	0	10 MIN		MIN	00
HR	1	0	0	0	0	1	0	RD / $\overline{W}$	01-12 00-23	12/24	0	10 A/P	HR	00
DATE	1	0	0	0	0	1	1	RD / $\overline{W}$	01-28/29 01-30 01-31	T_1	0	10 DATE	DATE	01
MONTH	1	0	0	0	1	0	0	RD / $\overline{W}$	01-12	0	0	0	10 M / MONTH	01
DAY	1	0	0	0	1	0	1	RD / $\overline{W}$	01-07	T_2	0	0	0 / 0 DAY	01
YEAR	1	0	0	0	1	1	0	RD / $\overline{W}$	0-99	10 YEAR			YEAR	00
CONTROL	1	0	0	0	1	1	1	RD / $\overline{W}$		WP	C_1	C_0	X_4	X_3	X_2	X_1	X_0	A0
CLOCK BURST	1	0	1	1	1	1	1	RD / $\overline{W}$										

B. RAM

RAM 0	1	1	0	0	0	0	0	RD / $\overline{W}$	RAM DATA 0									XX
RAM 23	1	1	1	0	1	1	1	RD / $\overline{W}$	RAM DATA 23									XX
RAM BURST	1	1	1	1	1	1	1	RD / $\overline{W}$										

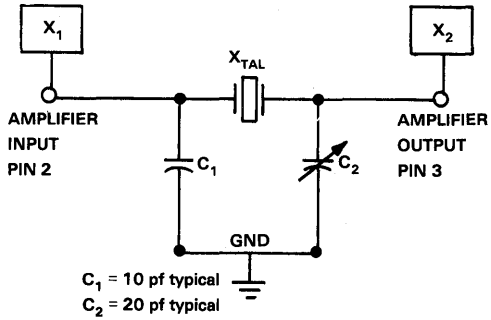
IX

CRYSTAL SELECTION

The wide frequency range of crystals that can be chosen for the Clock/RAM offers the user a large degree of flexibility. To aid in the selection of a suitable crystal, the following suggestions should be considered by the user. First, the MK3805 offers an output pin that will provide a system clock signal at either the crystal frequency, ½ the crystal frequency, or ¼ the crystal frequency. A system that requires a 4MHz clock initially may operate with an 8 MHz clock in the future. By applying an 8 MHz crystal to the Clock/RAM, a software change could provide the faster clock. Second, it is well known that, for a CMOS part, power dissipation will increase in direct proportion with frequency. Using a 1 MHz crystal and programming the CKO pin for 2048 Hz will cause the MK3805 to draw a minimum of power. (See Figures 9 and 10). The crystal connection is shown in Figure 5. If a generated clock signal is to be used as a time base, the connection is to Pin 2 (CKI) with Pin 3 left floating.

CRYSTAL CONNECTION

Figure 5



If it is desirable to "tune" the oscillator to a precise frequency, C_2 may be a variable capacitor.

C_2 should be in the range of $C_1 \geq C_2 \geq 2C_1$.

For low frequency operation (1 MHz) $C_1 \sim 10 - 20$ pf

For a high frequency operation (8 MHz) $C_1 \sim 5 - 10$ pf.

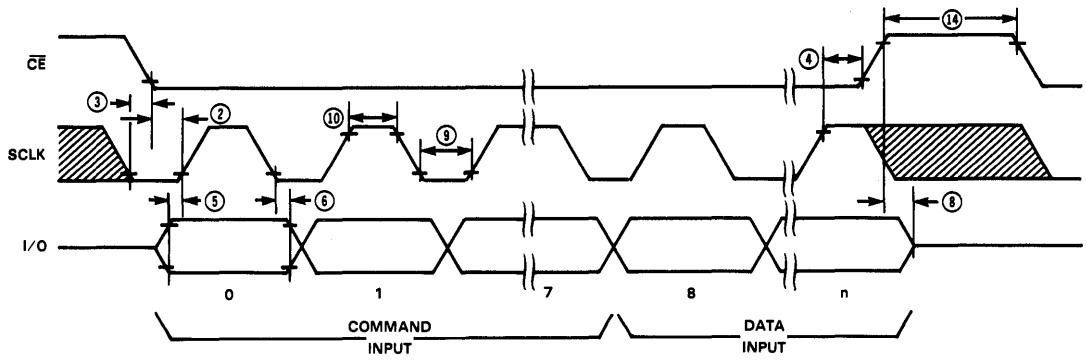
SUMMARY OF CRYSTAL SPECIFICATIONS

Figure 6

Frequency Range	Specification
1 MHz — 8.4 MHz	Parallel resonance Fundamental mode C_L = 20 pf to 40 pf AT cut

INPUT TIMING DIAGRAM

Figure 7



WRITE DATA TRANSFER (n Bits)

CRYSTAL FREQUENCY SELECTION

Table 2

Crystal Frequency Divider Mode	X4	X3	X2	X1	X0	f_{XTAL} (MHz) Crystal Frequency	Comments
Binary Mode	0	0	0	0	0	8.388608	Power on condition
	0	0	0	0	1	8.388608	
	0	0	0	1	0	4.194304	
	0	0	0	1	1	4.194304	
	0	0	1	0	0	2.097152	
	0	0	1	0	1	2.097152	
	0	0	1	1	0	1.048576	
	0	0	1	1	1	Reserved	
Microprocessor Mode	0	1	0	0	0	8.000000	
	0	1	0	0	1	5.000000	
	0	1	0	1	0	4.000000	
	0	1	0	1	1	2.500000	
	0	1	1	0	0	2.000000	
	0	1	1	0	1	1.250000	
	0	1	1	1	0	1.000000	
	0	1	1	1	1	Reserved	
Baud Rate Mode	1	0	0	0	0	7.372800	
	1	0	0	0	1	7.372800	
	1	0	0	1	0	3.686400	
	1	0	0	1	1	3.686400	
	1	0	1	0	0	1.843200	
	1	0	1	0	1	1.843200	
	1	0	1	1	0	0.921600	
	1	0	1	1	1	Reserved	
Color Burst Mode	1	1	0	0	0	7.159040	
	1	1	0	0	1	7.159040	
	1	1	0	1	0	3.579520	
	1	1	0	1	1	3.579520	
	1	1	1	0	0	1.789760	
	1	1	1	0	1	1.789760	
	1	1	1	1	0	0.894880	
	1	1	1	1	1	Reserved	

CLOCK OUTPUT SELECTION

Table 3

C1	C0	CKO Output Frequency	Comments
0	0	f_{XTAL}	
0	1	$f_{XTAL} \div 2$	Power on condition
1	0	$f_{XTAL} \div 4$	
1	1	= 2048 Hz	Frequency applies for use with Binary Mode only. Other operating modes produce a CKO signal approximately equal to 2000 Hz.

ELECTRICAL SPECIFICATIONS MK3805N-03

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} relative to GND ..... -0.5 V to + 12.0 V
Voltage on any pin ..... -0.5 V to + V_{CC} + .5
Temperature under bias ..... -50°C + 95°C
Storage Temperature ..... -55°C to +125°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC OPERATING CONDITIONS

$0°C \leq T_A \leq +70°C$

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.5	V	1
V_{SB}	RAM Retention Standby	3.5		V	1,7

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
I_{CC1}	Power Supply Current		6.0	mA	2
I_{CC2}	Power Supply Current		10.0	mA	3
I_{CC3}	Power Supply Current		2.0	mA	4
I_{CC4}	Power Supply Current		600	μA	5
I_{LI}	Input Leakage Current, SCLK and $\overline{CE}$	-1.0	1.0	μA	6
I_{LO}	Output Leakage Current, I/O Pin	-10.0	10.0	μA	6
V_{IH}	Logic "1" Voltage, All Inputs except X1	2.2		V	1
V_{IL}	Logic "0" Voltage, All Inputs		0.8	V	1
V_{IHX1}	Logic "1" Voltage, X_1 Input	3.9			8
$V_{I/OH}$	Output Logic "1" Voltage, I/O pin	2.4		V	1(I_{OH}=-100μA)
$V_{I/OL}$	Output Logic "0" Voltage, I/O pin		0.4	V	1(I_{OL}= 3.8 mA)
V_{CKH}	Output Logic "1" Voltage, CKO pin	2.4		V	1(I_{OH} = 1.0 mA)
V_{CKL}	Output Logic "0" Voltage, CKO pin		0.4	V	1(I_{OL} = 5.0 mA)

NOTES:
1. All voltages referenced to GND.
2. Crystal/Clock Input frequency = 8.4 MHz, f_{CKO} = 4.2 MHz with 30 pf load.
3. Crystal/Clock input frequency = 8.4 MHz, f_{CKO} = 8.4 MHz with 100 pf load.
4. Crystal/Clock input frequency = 8.4 MHz, f_{CKO} = 2084 Hz with 30 pf load.
5. Crystal/Clock Input frequency = 1 MHz, f_{CKO} = 2048 Hz with a 30 pf load.
6. Measured with V_{CC} = 5.0 V, $0 \leq V_I \leq 5.0$ V, outputs in high impedance state.
7. Applied to pin 8 to retain data in RAM during a power fault.
8. V_{IHX1} spec. applies only to the external clock input configuration.

CAPACITANCE

T_A = 25°C

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITION
C_I	Capacitance on Input Pin	10	pF	Note 1
$C_{I/O}$	Capacitance on I/O pin	12	pF	Note 1
C_X	Capacitance on X1/C1 and X2	12	pF	Note 1

NOTE:
1. Measured as $C = \frac{I\Delta t}{\Delta V}$ with V = 3 V, and unmeasured pins grounded.

AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq +70°C$, $V_{CC} = 5V \pm 10\%$

NUM	SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTES
1	f_X	Crystal frequency	800	8400	kHz	
2	t_{CSS}	$\overline{CE}$ to SCLK↑ set up time	1.0		μs	1,6
3	t_{SCS}	SCLK low set up time to $\overline{CE}$ ↓	40		ns	1,6
4	t_{SCH}	SCLK↑ to $\overline{CE}$↑ hold time	1.0		μs	1,5,6
5	t_{DSS}	Input Data to SCLK↑ set up time	400		ns	1,6
6	t_{SDH}	Input Data from SCLK↓ hold time	200		ns	1,6
7	t_{SDD}	Output Data from SCLK↓ delay time		600	ns	1,2,3,6
8	t_{CDZ}	$\overline{CE}$↑ to I/O high impedance		500	ns	1,2,3,6
9	t_{SWL}	SCLK low time	1.95	∞	μs	
10	t_{SWH}	SCLK high time	1.95	∞	μs	
11	f_{SCLK}	SCLK frequency	DC	250	kHz	
12	t_{SR}, t_{SF}	SCLK Rise and Fall Time		1	μs	4,6
13	t_{CR}, t_{CF}	CKO Rise and Fall Time		50	ns	4,6
14	t_{CWH}	$\overline{CE}$ high time	2.0		μs	

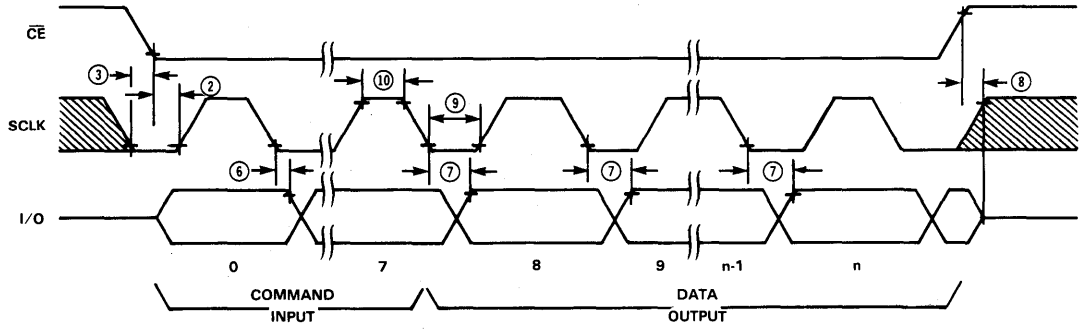
NOTES:

1. Measured at $V_{IH} = 2.0V$ or $V_{IL} = 0.8V$ and 50 ns rise and fall times on inputs.
2. Measured at $V_{OH} = 2.4V$ and $V_{OL} = 0.4V$.
3. Load Capacitance = 100 pF
4. t_r and t_f measured from 0.8V to 2.2 V
5. t_{SCH} must follow the last rising edge of S_{CLK} during a write cycle in order to allow time to complete a write to the internal register.
6. All voltages referenced to ground.

IX

OUTPUT TIMING DIAGRAM

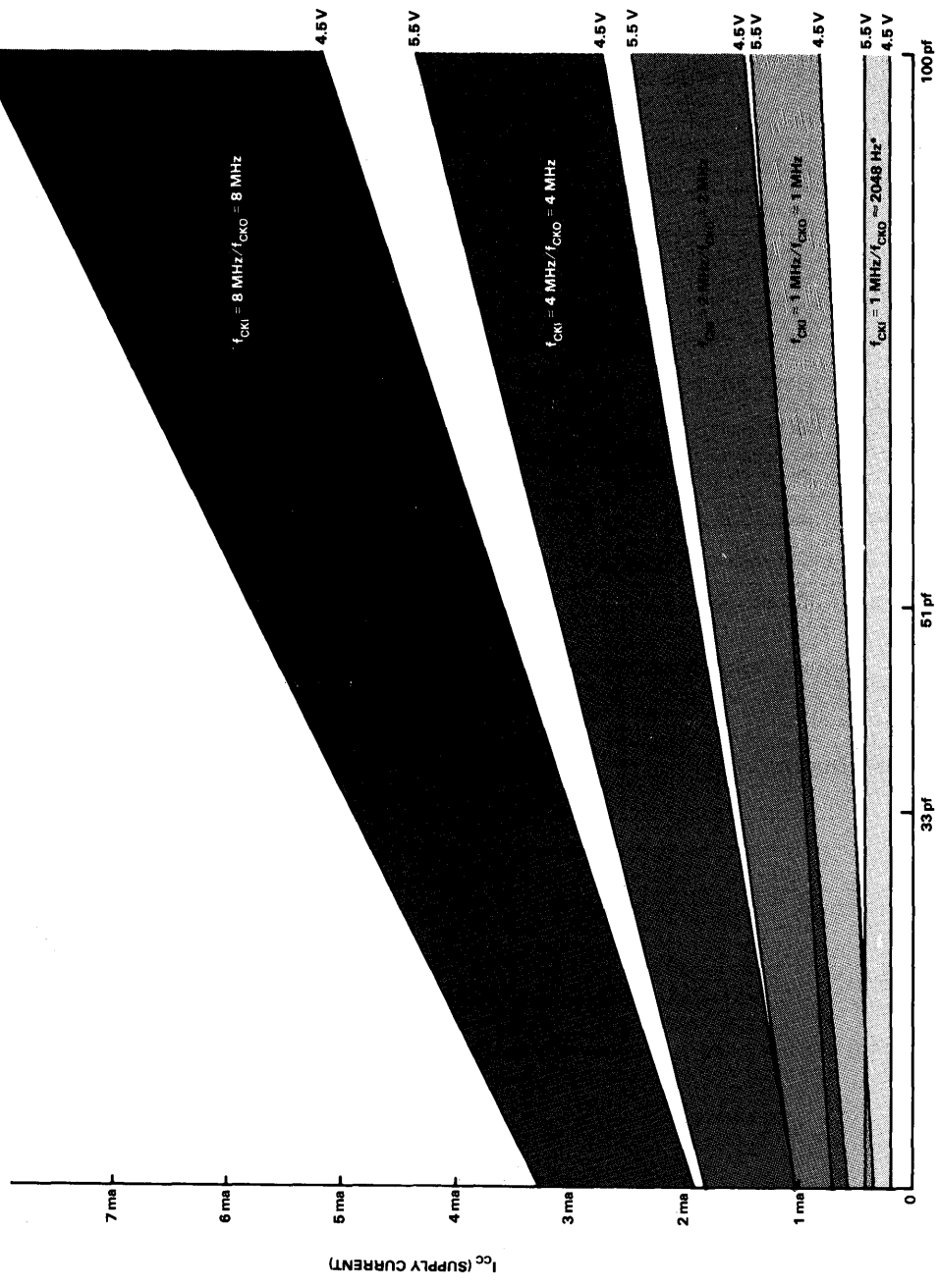
Figure 8



READ DATA TRANSFER (n Bits)

TYPICAL SUPPLY CURRENT FOR DIVIDE-BY-ONE MODE CRYSTAL OPERATION, T_A = 25°C

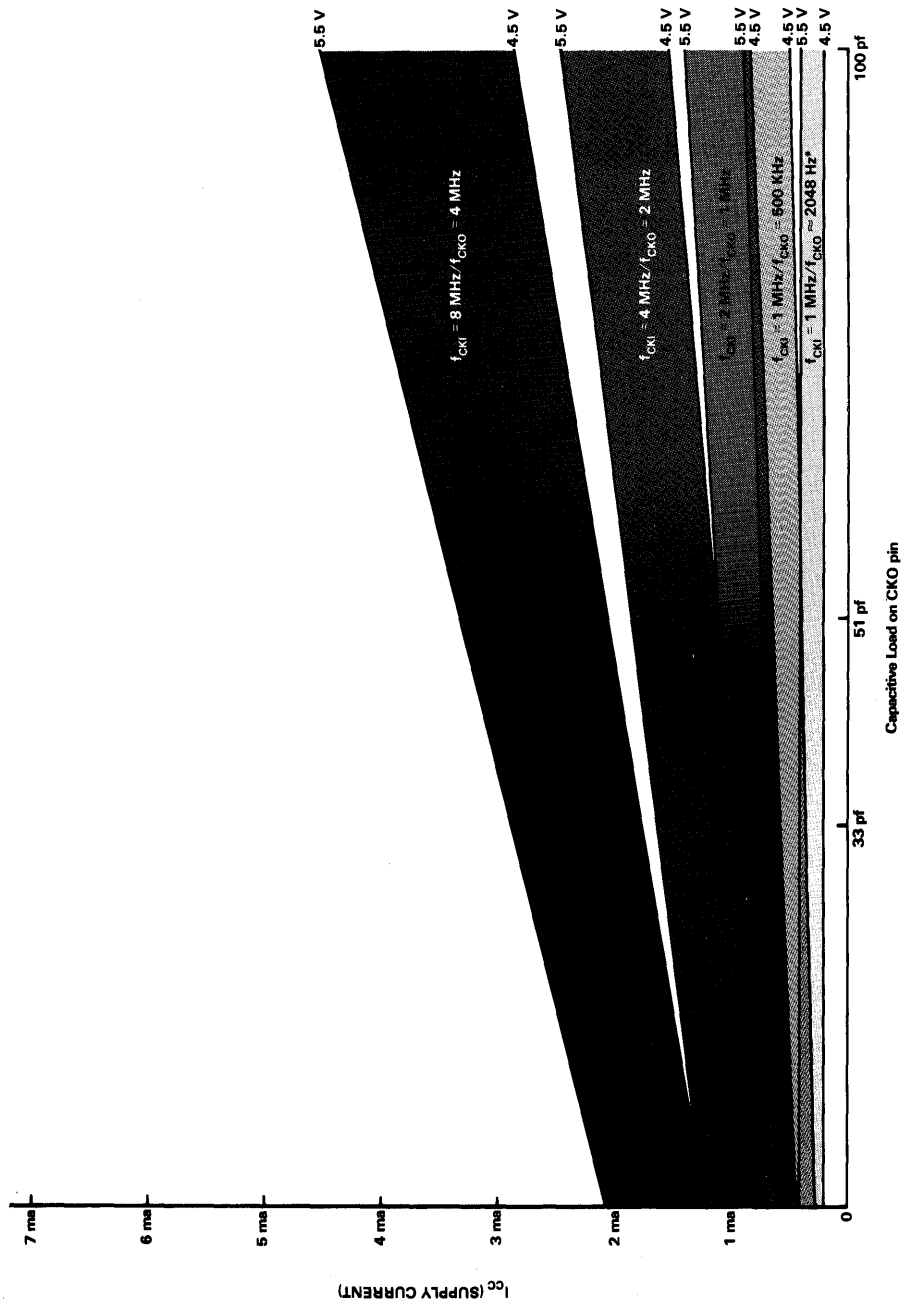
Figure 9



* This curve applies to the operating case where clock output selection is programmed for C1 = 1, CO = 1, and is included for comparison purposes to other operating modes.

TYPICAL SUPPLY CURRENT FOR DIVIDE-BY-TWO MODE CRYSTAL OPERATION, $T_A = 25°C$

Figure 10

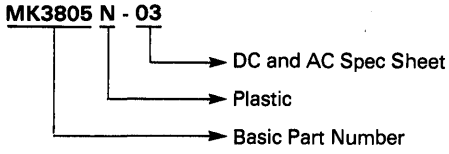


* This curve applies to the operating case where clock output selection is programmed for C1 = 1, C0 = 1, and is included for comparison purposes to other operating modes.

IX

ORDERING INFORMATION

Device Order Number	VCC	Temp	Package
MK3805N-03	5 V ± 10%	0 - 70°C	Plastic

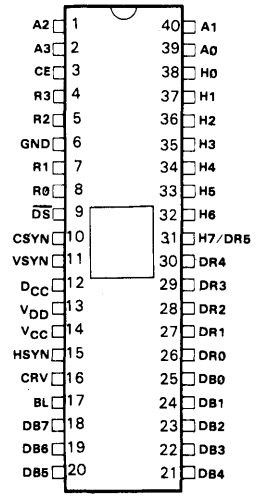


MK3807
PROGRAMMABLE CRT VIDEO CONTROL UNIT (VCU)

FEATURES

- Fully Programmable Display Format
  - Characters per data row (1-200)
  - Data rows per frame (6-64)
  - Raster scans per data row (1-16)
- Programmable Monitor Sync Format
  - Raster Scans/Frame (256-1023)
  - "Front Porch"
  - Sync Width
  - "Back Porch"
  - Interlace/Non-Interlace
  - Vertical Blanking
- Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Blanking
  - Cursor coincidence
- Programmed via:
  - Processor data bus
  - External PROM
- Standard or Non-Standard CRT Monitor Compatible
- Refresh Rate: 60 Hz
- Scrolling
  - Single Line
  - Multi-Line
- Cursor Position Registers
- Programmable Character Format
- Programmable Vertical Data Positioning
- Balanced Beam Current Interlace
- Graphics Compatible
- Split-Screen Applications
  - Horizontal
  - Vertical
- Interlace or Non-Interlace operation

PIN CONFIGURATION



- TTL Compatibility
- BUS Oriented: Compatible with most microprocessors
- Second source to SMC CRT 5037
- N-Channel Silicon Gate Technology

GENERAL DESCRIPTION

The Programmable CRT Video Control Unit (VCU) Chip is a user programmable 40-pin n channel MOS/LSI device containing the logic functions required to generate all the timing signals for the presentation and formatting of interlaced and non-interlaced video data on a standard or non-standard CRT monitor. The MK3807 VCU is a second source to SMC CRT 5037.

With the exception of the dot counter, which may be clocked at a video frequency above 25 MHz and is therefore not recommended for MOS implementation, all frame formatting, such as horizontal, vertical, and composite sync, characters per data row, data rows per frame, and raster scans per data row and per frame, are totally user programmable. The data row counter has been designed to facilitate scrolling. Refer to Table 1 for description of pin functions.

Programming is accomplished by loading seven 8-bit control registers directly off an 8-bit bidirectional data bus. Four register address lines and a chip enable line provide complete microprocessor compatibility for program controlled set up. The device can be "self loaded" via an external PROM tied on the data bus as described in the OPERATION section.

Figure 1 shows a block diagram of the internal functional components of the VCU.

The MK3807 (VCU) may be programmed for an odd or even number of scan lines per data row in both interlaced and non-interlaced modes.

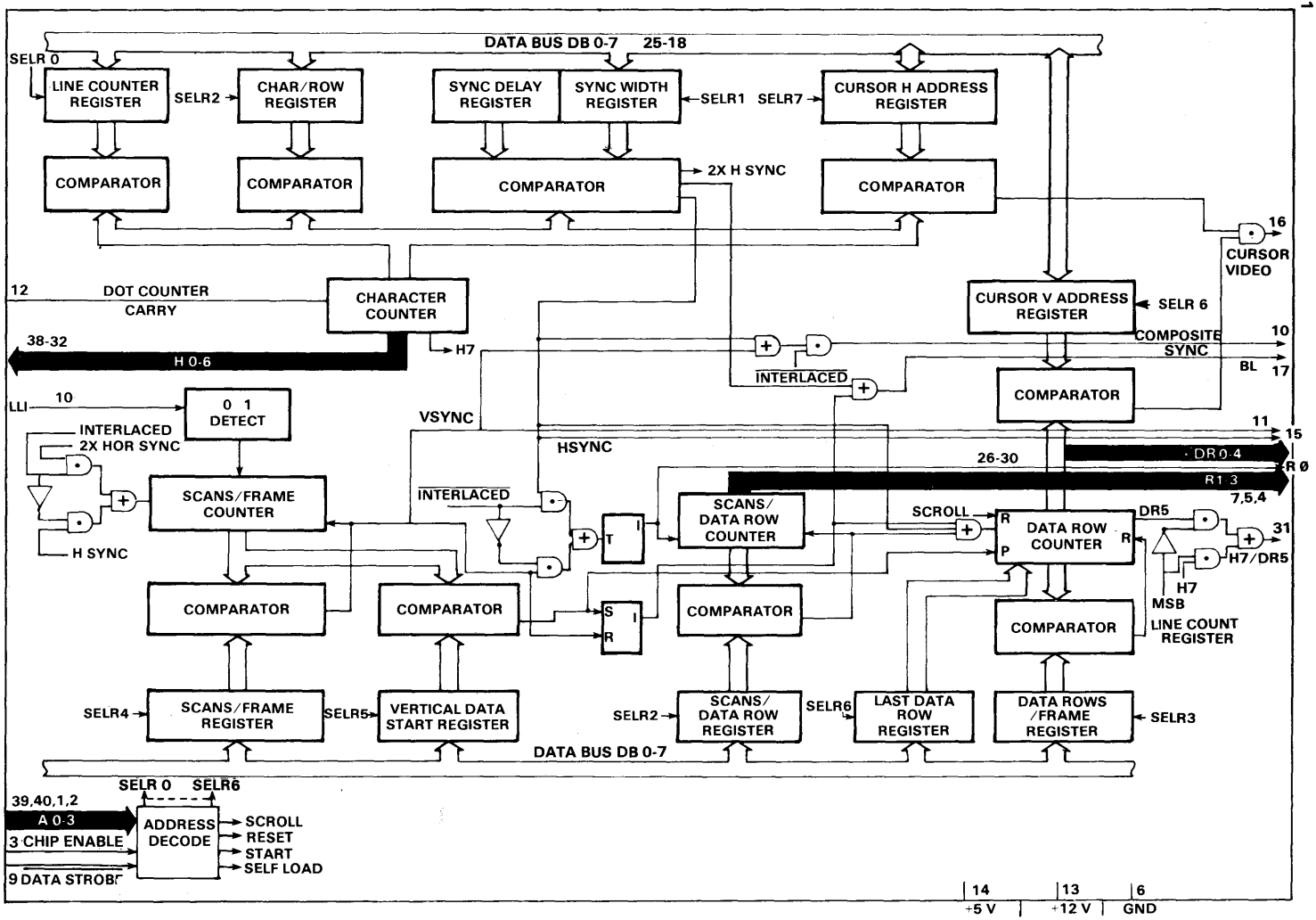
In addition to the seven control registers, two additional registers are provided to store the cursor character and data row addresses for generation of the cursor video signal. The contents of these two registers can also be read out onto the bus for update by the program.

DESCRIPTION OF PIN FUNCTIONS

Table 1

Pin No.	Symbol	Name	Input/ Output	Function
25-18	DB0-7	Data Bus	I/O	Data bus. Input bus for control words from microprocessor or PROM. Bi-directional bus for cursor address.
3	CE	Chip Enable	I	Signals chip that it is being addressed.
39,40,1,2	A0-3	Register Address	I	Register address bits for selecting one of seven control registers or either of the cursor address registers.
9	$\overline{DS}$	Data Strobe	I	Strobes DB0-7 into the appropriate register or outputs the cursor character address or cursor line address onto the data bus.
12	DCC	Dot Counter Carry	I	Carry from off-chip dot counter establishing basic character clock rate. Character clock.
38-32	H0-6	Character Counter Outputs	O	Character counter outputs.
7,5,4	R1-3	Scan Counter Outputs	O	Three most significant bits of the Scan Counter; row select inputs to character generator.
31	H7/DR5	H7/DR5	O	Pin definition is user programmable. Output is MSB of Character Counter if horizontal line counter (REG.0) is $\geq$ 128; otherwise output is MSB Of Data Row Counter.
8	R0	Scan Counter LSB	O	Least significant bit of the scan counter. In the interlaced mode with an even number of scans per data row, R0 will toggle at the field rate; for an odd number of scans per data row in the interlaced mode, R0 will toggle at the data row rate.
26-30	DR0-4	Data Row Counter Outputs	O	Data Row counter outputs.
17	BL	Blank	O	Defines non-active portion of horizontal and vertical scans.
15	HSYN	Horizontal Sync	O	Initiates horizontal retrace.
11	VSYN	Vertical Sync	O	Initiates vertical retrace.
10	CSYN	Composite Sync Output	O	Composite sync is provided on the MK3807. This output is active in non-interlaced mode only. Provides a true RS-170 composite sync wave form.
16	CRV	Cursor Video	O	Defines cursor location in data field.
14	V_{CC}	Power Supply	PS	+5 volt Power Supply
13	V_{DD}	Power Supply	PS	+12 volt Power Supply

BLOCK DIAGRAM
Figure 1



OPERATION

The design philosophy employed was to allow the MK3807 Programmable CRT Video Control Unit (VCU) to interface effectively with either a microprocessor based or hardwire logic system. The device is programmed by the user in one of two ways: via the processor data bus as part of the system initialization routine, or during power up via a PROM tied on the data bus and addressed directly by the Row Select outputs of the chip (See Figure 2). Seven 8-bit words are required to program the chip fully. Bit assignments for these words are shown in Tables 2, 3 and 4. The information contained in these seven words consists of the following:

Horizontal Formatting:	
Characters/Data Row	A 3 bit code providing 8 mask programmable character lengths from 20 to 132. The standard device will be masked for the following character lengths; 20, 32, 40, 64, 72, 80, 96, and 132.
Horizontal Sync Delay	3 bits assigned providing up to 8 character times for generation of "front porch".
Horizontal Sync Width	4 bits assigned providing up to 16 character times for generation of horizontal sync width.
Horizontal Line Count	8 bits assigned providing up to 256 character times for total horizontal formatting.
Skew Bits	A 2 bit code providing from a 0 to 2 character skew (delay) between the horizontal address counter and the blank and sync (horizontal, vertical, composite) signals to allow for retiming of video data prior to generation of composite video signal. The Cursor Video signal is also skewed as a function of this code.
Vertical Formatting:	
Interlaced/Non-interlaced	This bit provides for data presentation with odd/even field formatting for interlaced systems. It modifies the vertical timing counters as described below. A logic 1 establishes the interlace mode.
Scans/Frame	8 bits assigned, defined according to the following equations: Let X = value of 8 assigned bits. 1) in interlaced mode—scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (00000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields. Range = 513 to 1023 scans/frame, odd counts only. 2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011). Range = 256 to 766 scans/frame, even counts only. In either mode, vertical sync width is fixed at three horizontal scans (≡3H).
Vertical Data Start	8 bits defining the number of raster scans from the leading edge of vertical sync until the start of display data. At this raster scan the data row counter is set to the data row address at the top of the page.
Data Rows/Frame	6 bits assigned providing up to 64 data rows per frame.
Last Data Row	6 bits to allow up or down scrolling via a preload defining the count of the last displayed data row.
Scans/Data Row	4 bits assigned providing up to 16 scan lines per data row.

ADDITIONAL FEATURES

MK3807 VCU Initialization:

Under microprocessor control—The device can be reset under system or program control by presenting a 1010 address on A3-0. The device will remain reset at the top of the even field page until a start command is executed by presenting a 1110 address on A3-0.

Via "Self Loading"—In a non-processor environment, the self loading sequence is effected by presenting and holding the 1111 address on A3-0, and is initiated by the receipt of the strobe pulse ($\overline{DS}$). The 1111 address should be maintained long enough to ensure that all seven registers have been loaded (in most applications under one millisecond). The timing sequence will begin one line scan after the 1111 address is removed. In processor based systems, self loading is initiated by presenting the 0111 address to the device. Self loading is terminated by presenting the start command to the device which also initiates the timing chain.

Scrolling—In addition to the Register 6 storage of the last displayed data row a "scroll" command (address 1011) presented to the device will increment the first displayed data row count to facilitate up scrolling in certain applications.

CONTROL REGISTERS PROGRAMMING CHART
Table 2

Horizontal Line Count: Total Characters/Line = N + 1, N = 0 to 255 (DB0 = LSB)

Characters/Data Row:

DB2	DB1	DB0		
0	0	0	= 20	Active Characters/Data Row
0	0	1	= 32	
0	1	0	= 40	
0	1	1	= 64	
1	0	0	= 72	
1	0	1	= 80	
1	1	0	= 96	
1	1	1	= 132	

Horizontal Sync Delay: = N, from 1 to 7 character times (DB0 = LSB, N = 0 Disallowed)

Horizontal Sync Width: = N, from 1 to 15 character times (DB3 = LSB, N = 0 Disallowed)

Skew Bits

DB7	DB8	Sync/Blank Delay	Cursor Delay (Character Times)
0	0	0	0
1	0	1	0
0	1	2	1
1	1	2	2

Scans/Frame

8 bits assigned, defined according to the following equations:
Let X = value of 8 assigned bits. DB0 = LSB)
1) in interlaced mode— scans/frame = 2X + 513. Therefore for 525 scans, program X = 6 (0000110). Vertical sync will occur precisely every 262.5 scans, thereby producing two interlaced fields.
Range = 513 to 1023 scans/frame, odd counts only.
2) in non-interlaced mode—scans/frame = 2X + 256. Therefore for 262 scans, program X = 3 (00000011).
Range = 256 to 766 scans/frame, even counts only.
In either mode, vertical sync width is fixed at three horizontal scans (= 3H)

Vertical Data Start: N = number of raster lines delay after leading edge of vertical sync of vertical start position. (DB0 = LSB)

Data Rows/Frame: Number of data rows = N + 1, N = 0 to 63 (DB0 = LSB)

Last Data Row: N = Address of last displayed data row, N = 0 to 63, ie; for 24 data rows, program N = 23. (DB0 = LSB)

Mode: Register 1, DB7 = 1 established Interlace

Scans/Data Row:

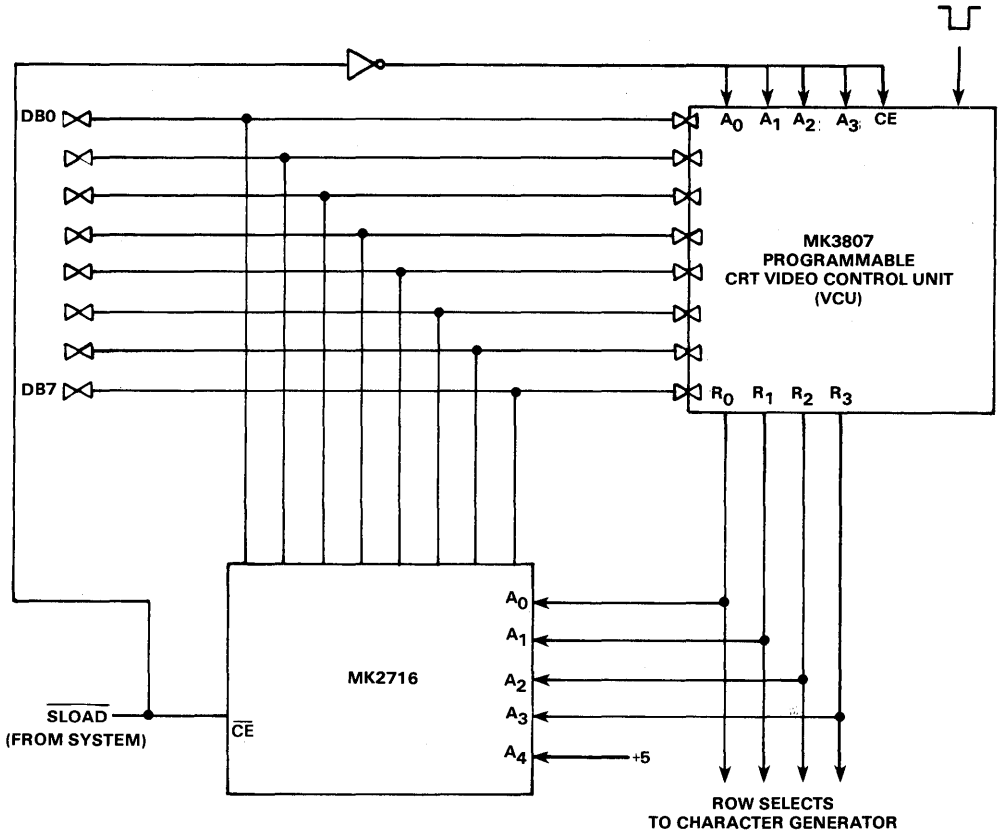
Interlace Mode

Scans per data Row = N + 2. N = 0 to 14, odd or even counts.

Non-Interlace Mode

Scans per Data Row = N + 1, odd or even count, N = 0 to 15.

SELF LOADING SCHEME
Figure 2



OPTIONAL START-UP SEQUENCE

When employing microprocessor controlled loading of the MK3807 VCU's registers, the following sequence of instruction may be used optionally:

ADDRESS	COMMAND
1 1 1 0	Start Timing Chain
1 0 1 0	Reset
0 0 0 0	Load Register 0
.	.
.	.
.	.
0 1 1 0	Load Register 6
1 1 1 0	Start Timing Chain

The sequence of START RESET LOAD START is necessary to ensure proper initialization of the registers.

This sequence is not required if register loading is via either of the Self Load modes.

REGISTER SELECTS/COMMAND CODES

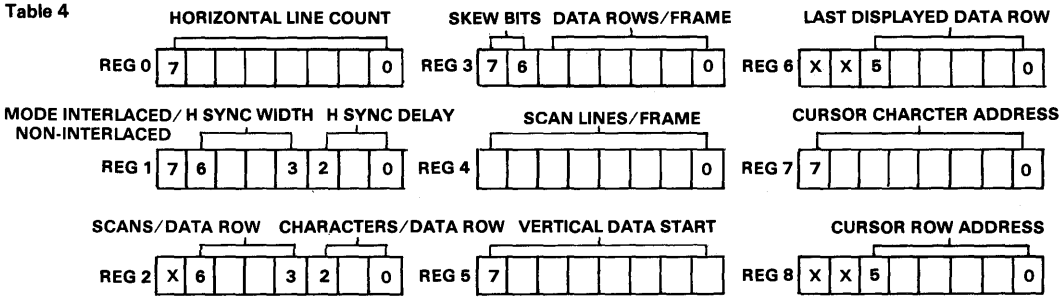
Table 3

A3	A2	A1	A0	Select/Command	Description
0	0	0	0	Load Control Register 0	See Table 4
0	0	0	1	Load Control Register 1	
0	0	1	0	Load Control Register 2	
0	0	1	1	Load Control Register 3	
0	1	0	0	Load Control Register 4	
0	1	0	1	Load Control Register 5	
0	1	1	0	Load Control Register 6	
0	1	1	1	Processor Initiated Self Load	Command from processor instructing MK3807 VCU to enter Self Load Mode (via external PROM)
1	0	0	0	Read Cursor Line Address	
1	0	0	1	Read Cursor Character Address	
1	0	1	0	Reset	Resets timing chain to top left of page. Reset is latched on chip by $\overline{DS}$ and counters are held until released by start command.
1	0	1	1	Up Scroll	Increments address of first displayed data row on page, i.e.; prior to receipt of scroll command—top line = 0, bottom line = 23. After receipt of Scroll Command—top line = 1, bottom line = 0.
1	1	0	0	Load Cursor Character Address[1]	
1	1	0	1	Load Cursor Line Address[1]	
1	1	1	0	Start Timing Chain	Receipt of this command after a Reset or Processor Self Load command will release the timing chain approximately one scan line later. In applications requiring synchronous operation of more than one VCU the dot counter carry should be held low during the $\overline{DS}$ for this command.
1	1	1	1	Non-Processor Self Load	Device will begin self load via PROM when $\overline{DS}$ goes low. The 1111 command should be maintained on A3-0 long enough to guarantee self load. (Scan counter should cycle through at least once). Self load is automatically terminated and timing chain initiated when the all "1's" condition is removed, independent of $\overline{DS}$. For synchronous operation of more than one VCU, the Dot Counter Carry should be held low when the command is removed.

NOTE 1: During Self-Load, the Cursor Character Address Register (REG 7) and the Cursor Row Address Register (REG 8) are enabled during states 0111 and 1000 of the R3-R0 Scan Counter outputs respectively. Therefore, Cursor data in the PROM should be stored at these addresses.

BIT ASSIGNMENT CHART

Table 4



IX

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to + 70°C
Storage Temperature Range ..... -55°C to + 150°C
Lead Temperature (soldering, 10 sec.) ..... + 325°C
Positive Voltage on any Pin, with respect to ground ..... + 18.0 V
Negative Voltage on any Pin, with respect to ground ..... -0.3 V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

DC CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, unless otherwise noted)

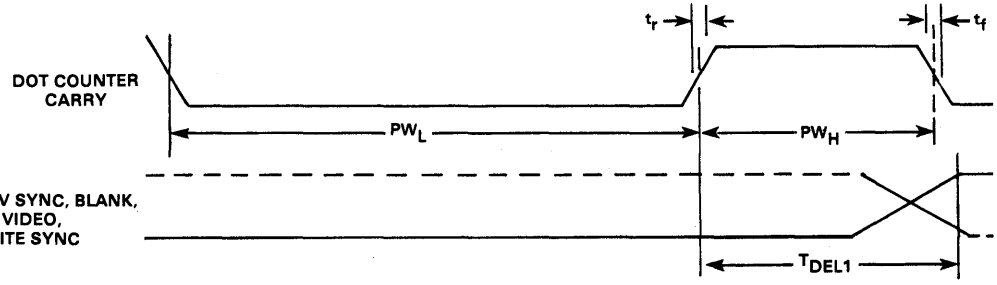
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
INPUT VOLTAGE LEVELS					
Low Level, V_{IL}			0.8	V	
High Level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low Level - V_{OL} for R0-3			0.4	V	I_{OL}=3.2 ma
Low Level - V_{OL}, all others			0.4	V	I_{OL}=1.6 ma
High Level - V_{OH} for R0-3, DB0-7	2.4				I_{OH}=80μa
High Level - V_{OH} all others	2.4				I_{OH}=40μa
INPUT CURRENT					
Low Level, I_{IL} (Address, CE only)			250	μA	V_{IN}=0.4 V
Leakage, I_{IL} (All inputs except Address, CE)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data Bus, C_{IN}		10	15	pF	
$\overline{DS}$, Clock, C_{IN}		25	40	pF	
All other, C_{IN}		10	15	pF	
DATA BUS LEAKAGE in INPUT MODE					
I_{DB}			10	μA	$0.4 \leq V_{IN} \leq 5.25$ V
POWER SUPPLY CURRENT					
I_{CC}		80	100	mA	
I_{DD}		40	70	mA	

AC CHARACTERISTICS
(T_A = 70°C)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DOT COUNTER CARRY					
frequency	0.5		4.0	MHz	Figure 3
PW_H	35			ns	Figure 3
PW_L	215			ns	Figure 3
t_r, t_f		10	50	ns	Figure 3
DATA STROBE					
PW_{DS}	150ns		10μs		Figure 4
ADDRESS, CHIP ENABLE					
Set-up time	125			ns	Figure 4
Hold time	50			ns	Figure 4
DATA BUS - LOADING					
Set-up time	125			ns	Figure 4
Hold time	75			ns	Figure 4
DATA BUS - READING					
T_{DEL2}			125	ns	Figure 4, CL =50pF
T_{DEL4}	5		60	ns	Figure 4, CL =50pF
OUTPUTS, H0-7, HS, VS, BL, CRV					
CE-T_{DEL1}			125	ns	Figure 3, CL =20pF
OUTPUTS: R0-3, DR0-5					
T_{DEL3}	*		750	ns	Figure 5, CL =20pF

IX

AC TIMING DIAGRAMS
VIDEO TIMING
Figure 3



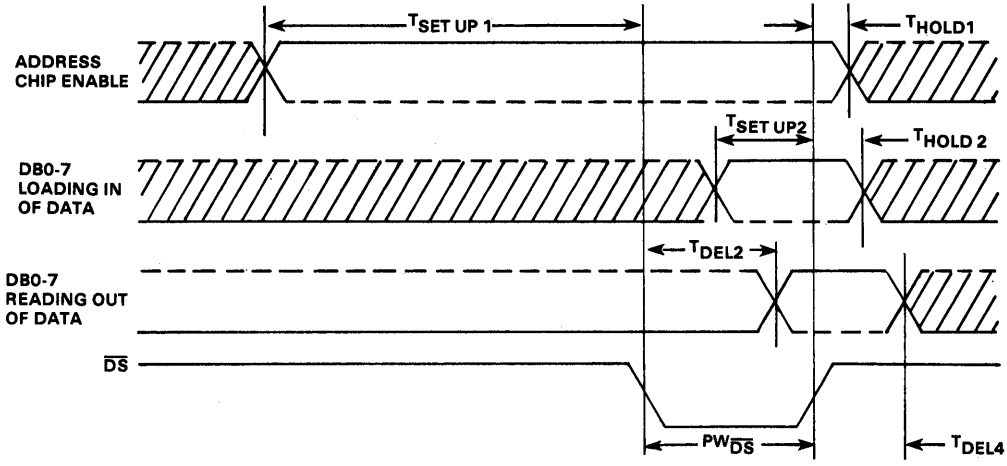
RESTRICTIONS

1. Only one pin is available for strobing data into the device via the data bus. The cursor X and Y coordinates are loaded into the chip by presenting one set of addresses and are output by presenting a different set of addresses. Therefore, the standard WRITE and READ control signals from most microprocessors must be "NORed" externally present a single strobe ($\overline{DS}$) signal to the device.

2. In interlaced mode, the total number of character slots assigned to the horizontal scan must be even to ensure that vertical sync occurs precisely between horizontal sync pulses.

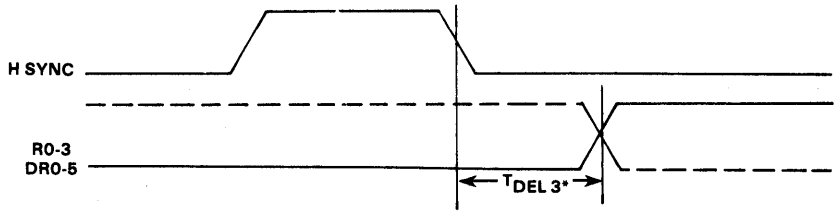
LOAD/READ TIMING

Figure 4



SCAN AND DATA ROW COUNTER TIMING

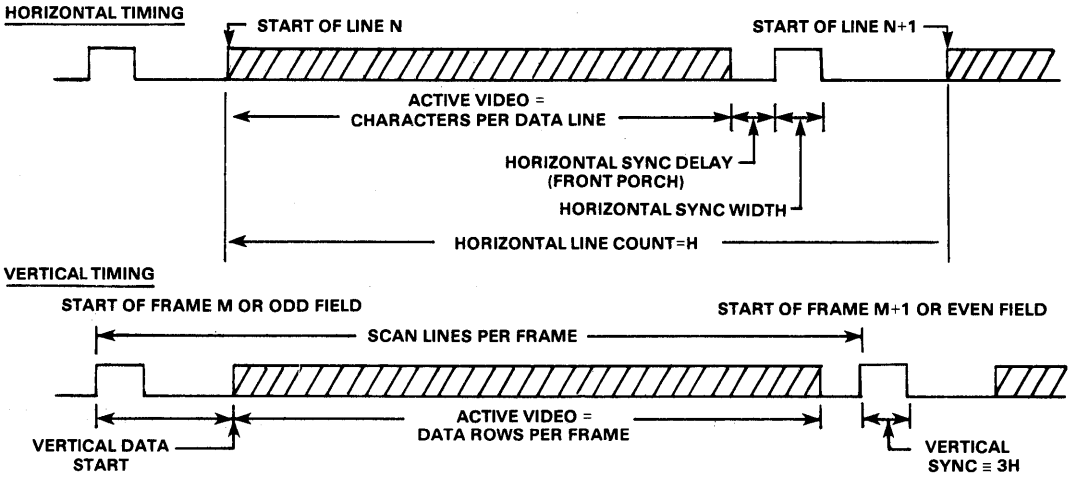
Figure 5



*R0-3 and DR0-5 may change prior to the falling edge of H sync

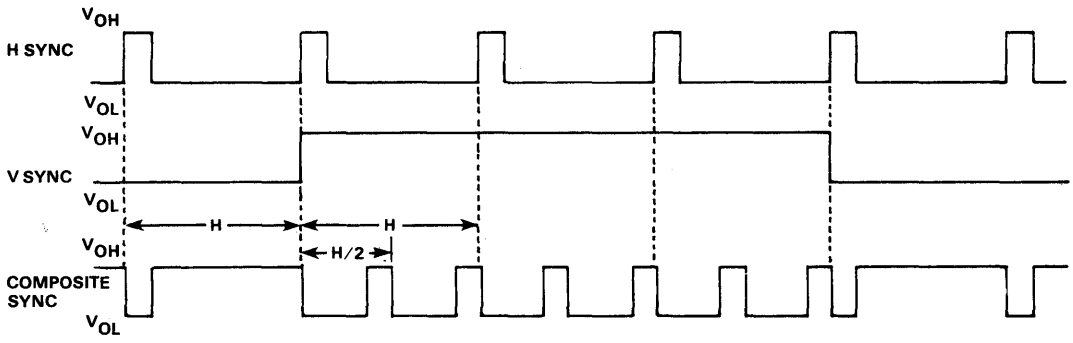
GENERAL TIMING

Figure 6



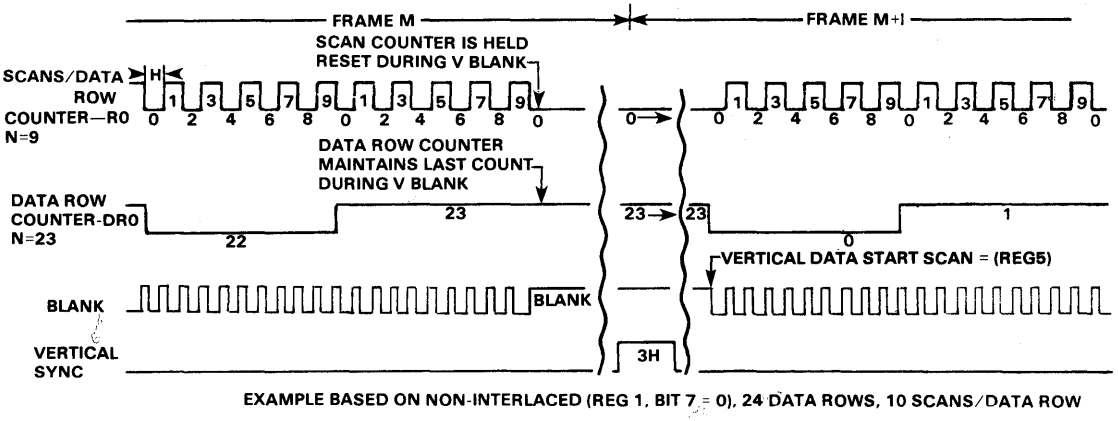
COMPOSITE SYNC TIMING

Figure 7



VERTICAL SYNC TIMING

Figure 8



EXAMPLE BASED ON NON-INTERLACED (REG 1, BIT 7 = 0), 24 DATA ROWS, 10 SCANS/DATA ROW

IX

1984/1985 MICROELECTRONIC DATA BOOK

PRELIMINARY

SERIAL CONTROL UNIT SCU20

FEATURES

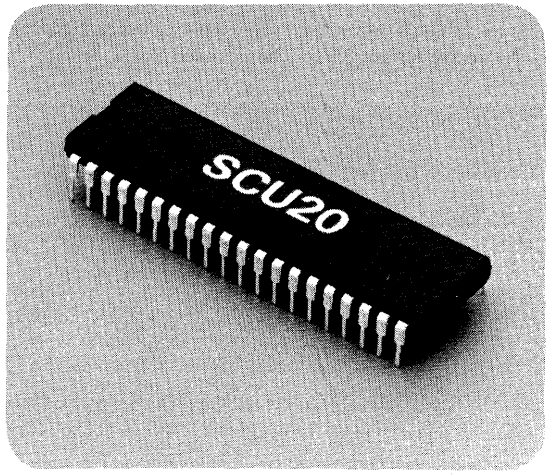
- Provides programmable remote I/O functions, real time operational capabilities, and standardized network communications on a 40 pin chip.
- Performs preprogrammed functions on command, including:
  - Byte input and output
  - Bit input and output
  - Set, clear, and toggle selected pins
  - Data access from real time functions
- Performs real time preprogrammed functions, including:
  - Data log on external interrupt, timer, or host control, up to 63 bytes of data
  - Five Event Counters driven from external interrupt, timer or host control
- Up to 24 programmable I/O pins
- Allows user to network up to 255 SCUs on a single communications channel
- Asynchronous serial data transmission
- Selectable Baud rate (300, 1200, 2400, or 9600 Baud)
- Secure, Error resistant data link protocol
- Requires single +5 volt supply
- Low power (275mW typ)

INTRODUCTION

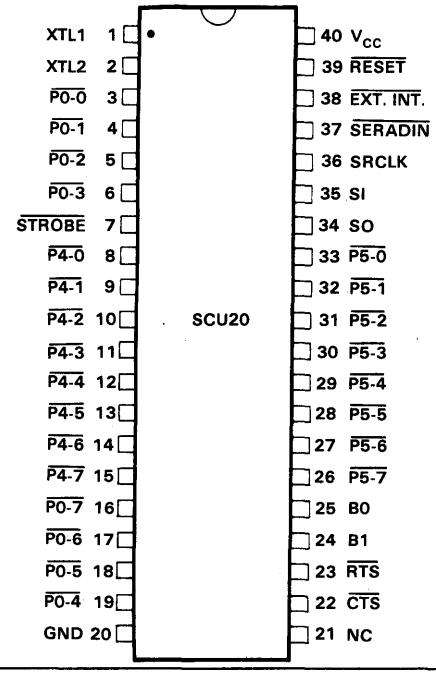
The SCU20 serial control unit is a preprogrammed MK3873 single chip microcomputer. It is a general purpose remote control/data acquisition unit, with 38 preprogrammed functions available to the user.

Communications with the SCU20 take place over an asynchronous half duplex communications channel at 300, 1200, 2400, or 9600 Baud. The communications protocol is efficient and error resistant, and yet easy to implement on the host system.

SCU20
Figure 1



SCU20 PINOUT
Figure 2



X

The SCU20 can be used for both monitoring and control systems where remote intelligence is required. It can be configured to provide many different input/output and data acquisition functions through its 24 I/O pins. Such intelligent functions as Data Log and Event Counters allow many different applications that will not burden the host system with constant update requirements.

FUNCTIONAL PIN DESCRIPTION

The SCU20 is housed in a plastic 40 pin dual in-line package.

Figure 2 shows the location of each pin on the SCU20. The following describes the function of each pin.

SCU20 PINOUT DEFINITION

XTL1, XTL2 - Time base inputs for 3.6864 MHz crystal.

$\overline{P0\text{-}0}$ - $\overline{P0\text{-}7}$ - SCU20 port 0 (Bidirectional, active low). SCU20 address input or general purpose data port (see SCU20 Address section).

$\overline{STROBE}$ - Data available strobe for port 4 (output active low).

$\overline{P4\text{-}0}$ - $\overline{P4\text{-}7}$ - SCU20 port 4 (Bidirectional, active low). General purpose data port.

$\overline{P5\text{-}0}$ - $\overline{P5\text{-}7}$ - SCU20 port 5 (Bidirectional, active low). General purpose data port.

SRCLK - Clock signal generated by internal Baud rate generator.

SI - Serial input. Receives serial asynchronous data from the host.

SO - Serial output. Transmits serial asynchronous data to the host.

$\overline{RTS}$ - Request to send (output, active low).

$\overline{CTS}$ - Clear to send (input, active low).

$\overline{RESET}$ - External reset (input, active low).

$\overline{EXT.\ INT.}$ - External interrupt (input, active low).

$\overline{SERADIN}$ - Serial address input/address mode (input, active low. See SCU20 Address section).

B0, B1 - Baud rate select.

V_{CC} - Power supply, 5 volts.

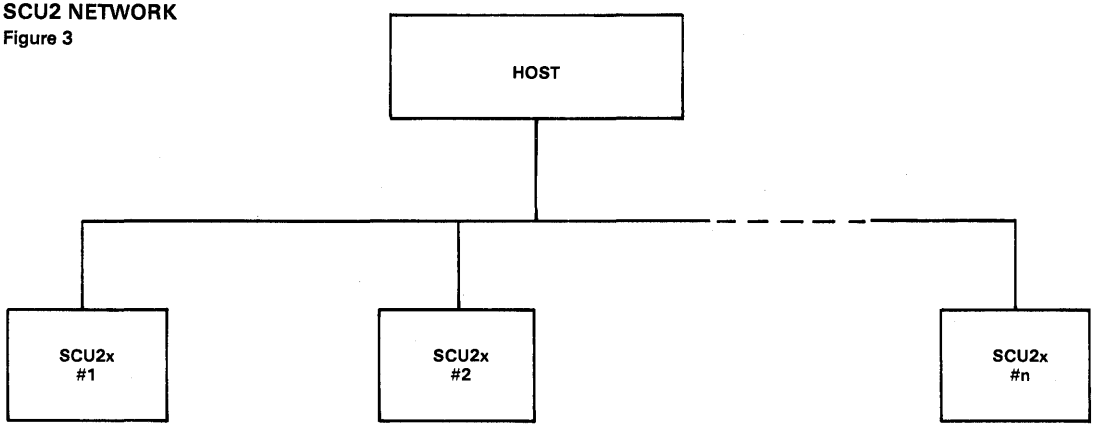
GND - Power supply ground.

SCU2 NETWORK

The SCU2 Network is a serial linked network of devices in the SCU2 family. All communications are via a common serial link using the SCU2 family communications protocol. In this way, a distributed control facility may be easily implemented from standard parts, and controlled by the host computer via the serial link.

Figure 3 illustrates the SCU2 Network.

SCU2 NETWORK
Figure 3



Each SCU2x in the network has an individual address to which it will respond. All SCU2x devices in the network are slave processors to the host, and are unable to initiate communications except in response to the host.

When the system is initialized, all SCU2x devices are in the listen mode, and are performing no functions. The host will issue an inquiry command to each device. Once all devices have been queried, the host will issue commands to each device to set up the particular operational parameters required of it. When this has been done, the host may then use the devices to control equipment, measure values, etc., by issuing commands and receiving responses.

Unless issuing a response, the SCU2x is always in the listen mode. If a command has been sent to an SCU2x, a response is expected within a specific time period. If none is forthcoming, it means that the command transmitted was not successfully received by the device. In this case, the host must take steps either to notify the operator or to retransmit the command.

If a system error occurs in the host, it may suspend operation of the entire network by transmitting the network reset command which causes all devices to be reset. This is the only command that does not require a specific SCU2x address as part of the command. It uses the system reset address which is recognized by each device.

SCU20 ADDRESS

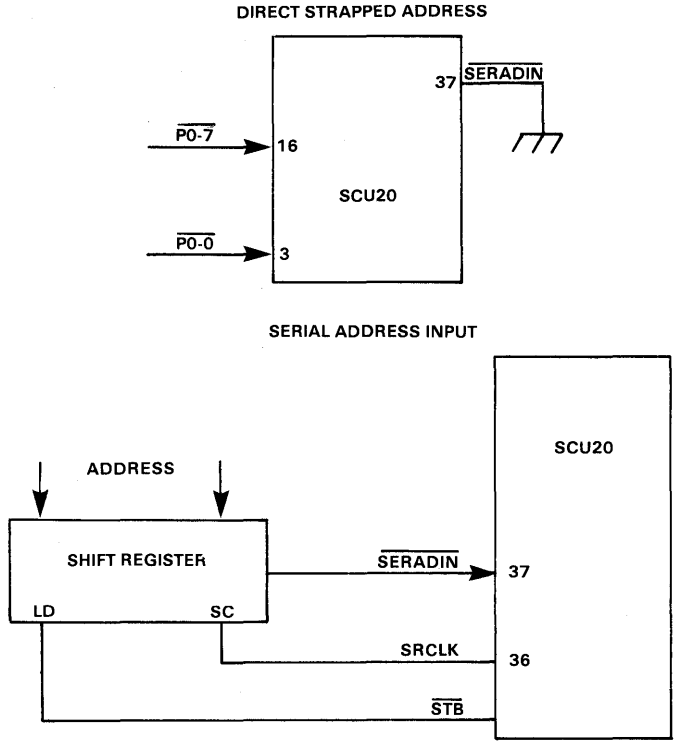
The address to which the SCU20 responds may be established in one of two ways.

The first mode is the Direct Strapped Address mode, and is enabled by tying the $\overline{\text{SERADIN}}$ pin directly to ground. In this mode, the SCU20 address is strapped at port 0. Because of this, port 0 is not available as a general purpose I/O port.

The second mode is the Serial Address Input mode. The $\overline{\text{SERADIN}}$ pin is used to input the address as a serial 8-bit stream from a shift register. SRCLK is used as a shift clock for this operation. The $\overline{\text{STROBE}}$ signal is used at initialization time to cause the address to be loaded into the shift register before shifting begins. In the Serial Address mode, port 0 becomes available for use as a general purpose data I/O port.

Figure 4 illustrates both methods of establishing the SCU20 address.

SCU20 ADDRESS ESTABLISHMENT
Figure 4



X

SCU20 COMMUNICATIONS

The SCU20 communicates with the host computer over a half duplex asynchronous serial link. The communications protocol is simple, yet error resistant.

The general form of the communication message is as follows:

HDR	ADDR	CMD	DATA	DATA	• • • •	LRC

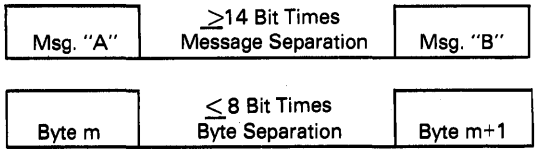
HDR - Message header. Hex '01' indicates a command message from the host; Hex '02' indicates a response from the SCU20.

ADDR - SCU20 Address. Indicates which SCU20 the message is for, or originates from.

CMD - Command. Indicates the function to be performed.

DATA - Any data that may be required by the particular command.

LRC - Linear Redundancy Check.



Messages are to be transmitted in block mode, with a message separation of at least 14 bit times. Interbyte separations should be no more than 8 bit times within a message.

A message from the host to the SCU20 will generate a response if there is no transmission error. If any transmission error is detected, no response will be made.

Possible transmission errors are LRC errors, parity errors, interbyte separation errors, or intermessage separation errors.

BAUD RATE SELECTION

The serial Baud rate is selected by a strapped option on the SCU20. Those options are listed below:

BAUD RATE	B0 (Pin 25)	B1 (Pin 24)
300	Low	Low
1200	Low	High
2400	High	Low
9600	High	High

MODEM SIGNALS

$\overline{RTS}$ and $\overline{CTS}$ are provided to facilitate handshaking with modems. Just prior to responding to a valid command, $\overline{RTS}$ will go to logic 1, indicating that the SCU20 is ready to send data back to the host. $\overline{CTS}$ is an input to the SCU20 that is tested after $\overline{RTS}$ goes active to determine if the SCU20 may begin transmitting data.

PARALLEL I/O PORTS

The SCU20 has a minimum of 2 parallel I/O ports and a maximum of 3 available for general use, depending on the address selection mode chosen. For each of these ports, there exist 2 registers that control and modify the I/O to and from the ports. These are the Data Direction Register (DDR) and the Mask Register(MR).

The Data Direction Register defines the usage of each pin in the port. If a bit is set to 0, then the corresponding pin is used as input. If a bit is set to 1, then the corresponding pin is used as an output. When a port is read, all bits are sampled for input whether or not they are marked for input. When a port is written to, however, only those pins declared as output will be modified.

The Mask Register provides a data mask that may be applied to the input data before transmission to the master. The mask is established once and may be used repeatedly before being changed by establishing a new mask value. If a pin is to be available upon read, the corresponding bit in the mask register is set to 1, while a pin that is to be masked out will have its mask bit set to 0.

SCU20 PREPROGRAMMED FUNCTIONS

The SCU20 has a variety of preprogrammed functions available to the user. Each of these functions addresses a different general area of application such that the SCU20 is truly a general purpose device.

PORT COMMANDS

There are several commands which allow the host to manipulate the 8-bit general purpose I/O ports. The host may load data into any one or all of the ports, may read any or all of the ports with or without a mask, may read with a new mask, or may read using the last defined mask. When data is loaded, the resulting port state is returned in the response message.

LOGIC COMMANDS

In addition to performing data I/O with the ports, the host may perform logical operations with the ports and data from the host. These commands allow the host to AND, OR, or Exclusive OR (XOR) data with any or all of the ports, and output the result to the ports. The resultant output is returned in the command response message.

BIT COMMANDS

These commands allow the host to SET, CLEAR, TEST, or TOGGLE bits in the ports by specifying bit number (0 - 24). Any pin that is declared as an input will not be changed.

EVENT COUNTERS

There are 5 Event Counters defined in SCU20. They are 16 bit up counters, and are driven by the timer, the external interrupt, or by host command. They may be used as simple event counters, or may be used in conjunction with the Data Log, and Pulse functions.

DATA LOG

The Data Log function allows the user to command the SCU20 to log data from the ports specified in the command, and store the data in the on-board RAM. Up to 63 bytes of data may be accumulated in the log, and may be captured on external interrupt, timer, or host command through use of an Event Counter.

Data from the Log is transmitted back to the host in a single read command burst.

CONTROL COMMANDS

There are several commands to control the SCU20 as well as the entire SCU2 network. These commands provide the host with the ability to query each individual SCU2x on the network for its type, the last message it sent, and for detailed error codes. In addition, there are commands that allow the host to reset an individual device, or to cause the entire SCU2 network to reset with a single command.

ERROR PROCESSING

The SCU20 does not provide a "negative acknowledge" response to command stream errors. Those errors are parity errors, LRC errors, unidentifiable commands, overrun, or violation of the separation specifications as described earlier.

In some cases, the SCU20 will provide error response to functional errors in commands that have been recognized. This response will be either a "NAK0" or a "NAK3" as specified for the command. "NAK0" is the hex value H'FB', and "NAK3" is the hex value H'FE'.

H'2'	ADDR	H'FB' or H'FE'	LRC

SCU20 COMMANDS

Figure 5 gives a complete list of the commands and functions available to the SCU20. For a full description of these commands and their use, refer to the SCU20 Operations Manual.

SCU20 COMMANDS
Figure 5

FUNCTION	COMMAND CODES	# DATA BYTES (CMD)	# DATA BYTES (RESP)	ERR COD RET
** PORT COMMANDS **				
Load Data Direction Registers	1E	3	0	-
Load Port (0, 4, 5)	00,01,02	1	1	-
Load All Ports	03	3	3	-
Read Port (0, 4, 5)	04,05,06	0	1	-
Read All Ports	07	0	3	-
Read Port Masked, Mask Provided	08,09,0A	1	1	-
Read All Ports, Masks Provided	0B	3	3	-
Read Port using Previous Mask	0C,0D,0E	0	1	-
Read All Ports using Previous Masks	0F	0	3	-

**** PORT LOGIC COMMANDS ****				
AND Data to Port	10,11,12	1	1	-
AND Data to All Ports	13	3	3	-
OR Data to Port	14,15,16	1	1	-
OR Data to All Ports	17	3	3	-
XOR Data to Port	18,19,1A	1	1	-
XOR Data to All Ports	1B	3	3	-
**** BIT COMMANDS ****				
Set Bit in Port	1F	1	0	-
Clear Bit in Port	20	1	0	-
Toggle Bit in Port	21	1	1	-
Test Bit in Port	22	1	1	-
**** EVENT COUNTERS ****				
Start Event Counter	80	1	0	-
Read Event Counter	81	1	2	NAK0
Clear Event Counter	82	1	0	NAK0
Stop Event Counter	83	1	0	NAK0
Step Event Counter	84	1	0	NAK0
**** DATA LOG COMMANDS ****				
Start Data Log	85	3	0	NAK0
Stop and Read Data Log	86	0	var.	-
Read Data Log Count	87	0	1	-
**** SCU CONTROL COMMANDS ****				
Enquiry	1C	0	var.	NAK3
Return SCU Type	1D	0	1	-
Read Error Code	F7	0	1	-
Reset SCU20 (data byte must be H'AA')	F9	1	0	-
General Reset (SCU2 Network)	FF	0	-	-

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -20°C to +85°C
Storage Temperature ..... -65°C to +150°C
Voltage on any Pin With Respect to Ground
(Except open drain pins and TEST) ..... -1.0 V to +7 V
Voltage on TEST with Respect to Ground ..... -1.0 V to + 9 V
Voltage on Open Drain Pins With Respect to Ground ..... -1.0 V to +13.5 V
Power Dissipation ..... 1.5 W
Power Dissipation by any one I/O pin[2] ..... 60 mW
Power Dissipation by all I/O pins[2] ..... 600 mW

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING VOLTAGES AND TEMPERATURES

Operating Voltage V_{CC} ..... +5 V ± 10%
Operating Temperature T_A ..... 0° - 70°C

AC CHARACTERISTICS

T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	NOTES
XTL1 XTL2	t_o	Time Base Period, all clock modes	250	500	ns	4 MHz - 2 MHz 3.6864 required for
	$t_{ex(H)}$	External clock pulse width high	90	400	ns	standard baud
	$t_{ex(L)}$	External clock pulse width low	100	400	ns	frequencies
Φ	t_Φ	Internal Φ clock	$2t_0$			
$\overline{\text{STROBE}}$	$t_{I/O-s}$	output valid to $\overline{\text{STROBE}}$ delay	3tΦ -1000	3tΦ +250	ns	I/O load = 50 pF + 1 TTL load
	t_{sL}	$\overline{\text{STROBE}}$ low time	8tΦ -250	12tΦ +250	ns	$\overline{\text{STROBE}}$ load = 50 pF + 3TTL loads
$\overline{\text{RESET}}$	t_{RH}	$\overline{\text{RESET}}$ hold time, low	6tΦ +750		ns	
	t_{RPOC}	$\overline{\text{RESET}}$ hold time, low for power clear	power supply rise time +0.1		ms	
$\overline{\text{EXT INT}}$	t_{EH}	$\overline{\text{EXT INT}}$ hold time in active and inactive state	6tΦ +750		ns	To trigger interrupt

X

CAPACITANCE
T_A = 25°C
All Part Numbers

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
C_{IN}	Input capacitance; I/O, $\overline{\text{RESET}}$, $\overline{\text{EXT INT}}$		10	pF	unmeasured pins grounded
C_{XTL}	Input capacitance; XTL1, XTL2	23.5	29.5	pF	

AC CHARACTERISTICS FOR SERIAL I/O PINS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SIGNAL	SYM	PARAMETER	MIN	MAX	UNIT	CONDITIONS
SRCLK	$t_{r(SRCLK)}$	Serial Clock Rise Time	60		ns	0.8 V - 2.0 V C_L = 100 pf
	$t_{f(SRCLK)}$	Serial Clock Fall Time	30		ns	2.4 V - 0.4 V C_L = 100 pf

DC CHARACTERISTICS
T_A, V_{CC} within specified operating range.
I/O Power Dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	MIN	MAX	UNIT	DEVICE
I_{CC}	Average Power Supply Current		103	mA	SCU20 Outputs Open
P_D	Power Dissipation		485	mW	SCU20 Outputs Open

DC CHARACTERISTICS
T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 2)

SYM	PARAMETER	MIN	MAX	UNIT	CONDITIONS
V_{IHEX}	External Clock input high level	2.4	5.8	V	
V_{ILEX}	External Clock input low level	-.3	.6	V	
I_{IHEX}	External Clock input high current		100	μA	$V_{IHEX} = V_{CC}$
I_{ILEX}	External Clock input low current		-100	μA	$V_{ILEX} = V_{SS}$
$V_{IHI/O}$	I/O input high level	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	open drain (1)
V_{IHR}	Input high level, $\overline{\text{RESET}}$	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	No pull-up
V_{IHEI}	Input high level, $\overline{\text{EXT INT}}$	2.0	5.8	V	standard pull-up (1)
		2.0	13.2	V	No pull-up
V_{IL}	I/O ports, $\overline{\text{RESET}}$[1], $\overline{\text{EXT INT}}$[1] input low level	-.3	.8	V	(1)
I_{IL}	Input low current, I/O ports and $\overline{\text{EXT IN}}$		-1.6	mA	$V_{IN} = 0.4$ V
I_L	Input leakage current, $\overline{\text{RESET}}$ input		+10 -5	μA μA	$V_{IN} = 13.2$ V $V_{IN} = 0.0$V
I_{OH}	Output high current, I/O ports	-100		μA	$V_{OH} = 2.4$ V
		-30		μA	$V_{OH} = 3.9$ V
I_{OL}	Output low current, I/O ports	1.8		mA	$V_{OL} = 0.4$ V
I_{OHS}	$\overline{\text{STROBE}}$ Output High current	-300		μA	$V_{OL} = 2.4$ V
I_{OLS}	$\overline{\text{STROBE}}$ output low current	5.0		mA	$V_{OL} = 0.4$ V

X

DC CHARACTERISTICS FOR SERIAL PORT I/O PINS

T_A, V_{CC} within specified operating range
I/O Power Dissipation ≤ 100 mW (Note 2)

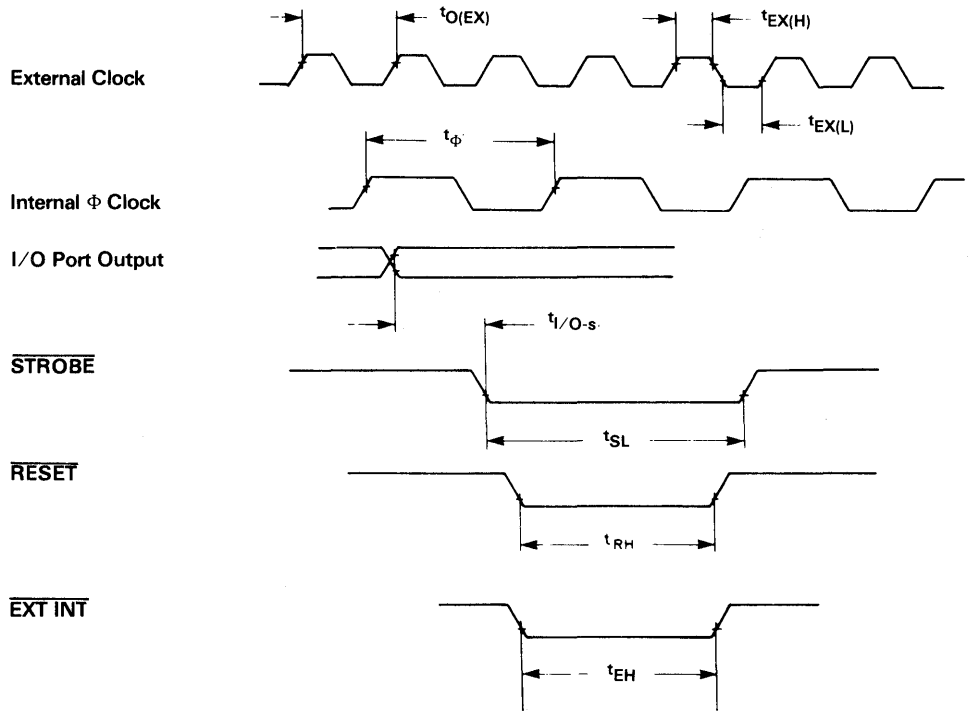
SYM	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
V_{IHS}	Input High for SI	2.0	5.8	V	
V_{ILS}	Input Low level for SI	-.3	.8	V	
I_{ILS}	Input low current for SI		-1.6	mA	V_{IL} = 0.4 V
I_{OHSO}	Output High Current SO	-100 -30		μA μA	V_{OH} = 2.4 V V_{OL} = 3.9 V
I_{OLSO}	Output Low Current SO	1.8		mA	V_{OL} = 0.4 V
I_{OHSRC}	Output High Current, SRCLK	-300		μA	V_{OH} = 2.4 V
I_{OLSRC}	Output Low Current, SRCLK	5.0		mA	V_{OL} = 0.4 V

NOTES

1. RESET and EXT INT have internal Schmitt triggers giving minimum .2 V hysteresis.
2. Power dissipation for I/O pins is calculated by $\Sigma(V_{CC} - V_{IL})(I_{IL}) + \Sigma(V_{CC} - V_{OH})(I_{OH}) + \Sigma(V_{OL})(I_{OL})$

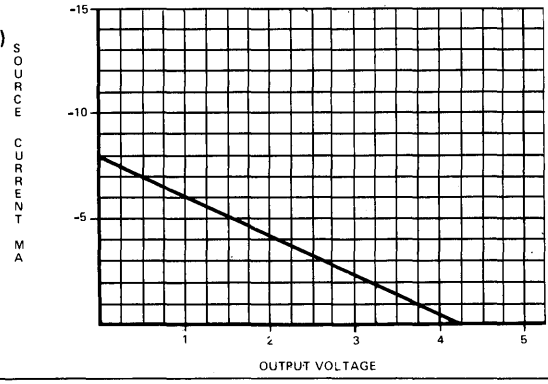
AC TIMING DIAGRAM

Figure 6

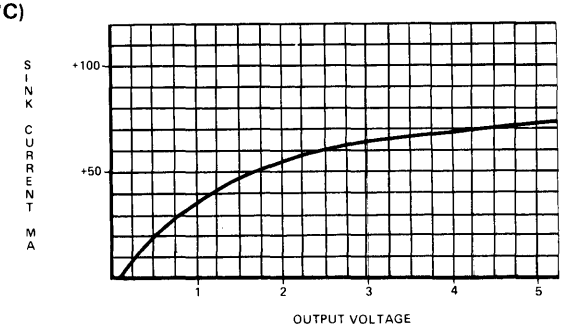


Note: All AC measurements are referenced to V_{IL} max., V_{IH} min., V_{OL} (.8v), or V_{OH} (2.0v)

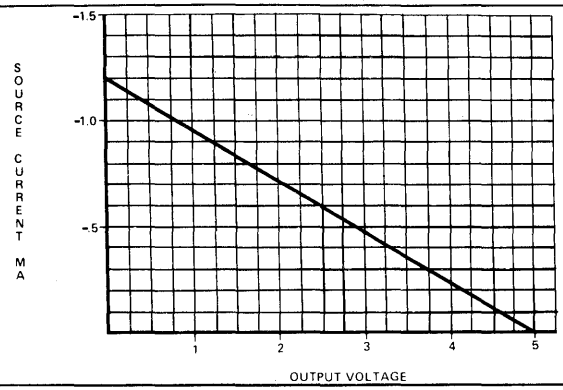
STROBE SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 7



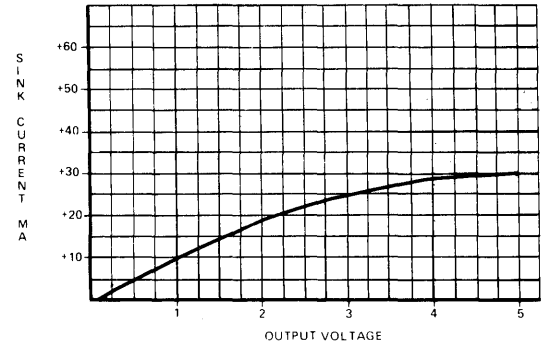
STROBE SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 8



STANDARD I/O PORT SOURCE CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 9



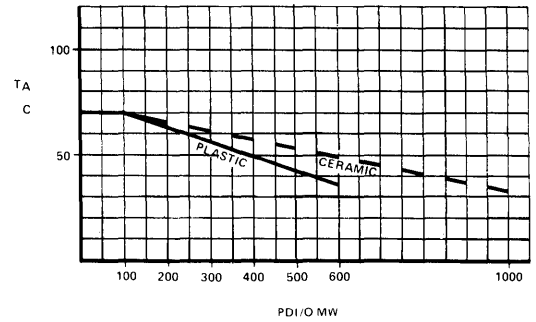
I/O PORT SINK CAPABILITY
(TYPICAL AT V_{CC} = 5V, T_A = 25°C)
Figure 10



X

MAXIMUM OPERATING TEMPERATURE VS. I/O POWER DISSIPATION

Figure 11



ORDERING INFORMATION

An example of the device order number is shown below.

MK 95103 N - 1 0

Power Supply Tolerance	0 = 5 V ±10% 5 = 5 V ± 5%
Operating Temperature Range	0 = 0°C - +70°C 1 = -40°C - +85°C
Package Types	P = Ceramic N = Plastic
Basic Device Type	

1984/1985 MICROELECTRONIC DATA BOOK

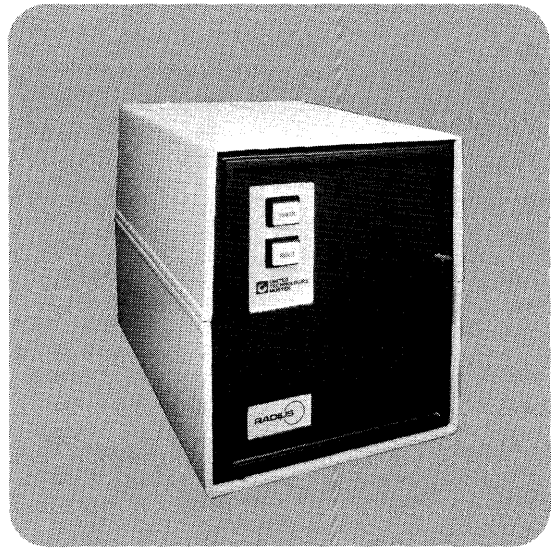
RADIUS™ REMOTE DEVELOPMENT STATION

FEATURES

- ☐ Microcomputer development with host computer
  - Software development on the host
  - Download to RADIUS
  - Hardware debug and software integration on RADIUS
- ☐ Utilizes standard Mostek SDE series AIM modules
- ☐ Host software available
  - Preconfigured for selected hosts
  - Reconfigurable for other hosts
- ☐ Upload/download performed with error tolerant protocol
- ☐ Emulation possible while disconnected from the host
- ☐ Serial I/O Baud rate up to 9600
- ☐ Supports optional local line printer and PROM programmer
- ☐ Self-diagnostic test

RADIUS

Figure 1



INTRODUCTION

Mostek RADIUS - Remote Access Development and Integration µcomputer System - is a state-of-the-art microcomputer development system, designed specifically to be used in a host computer environment. RADIUS provides software development capability via the host computer and hardware development and software integration using the advanced in-circuit-emulation capability of Mostek AIM modules.

RADIUS is installed between the user's CRT terminal and the host computer via an ASCII RS-232 serial interface. See Figure 2. It can be operated in any of three modes: Transparent, Local or Utility.

In Transparent Mode, the user can:

- Perform any function that can be performed on the host computer. RADIUS becomes completely transparent to the user.

In Local Mode, the user can:

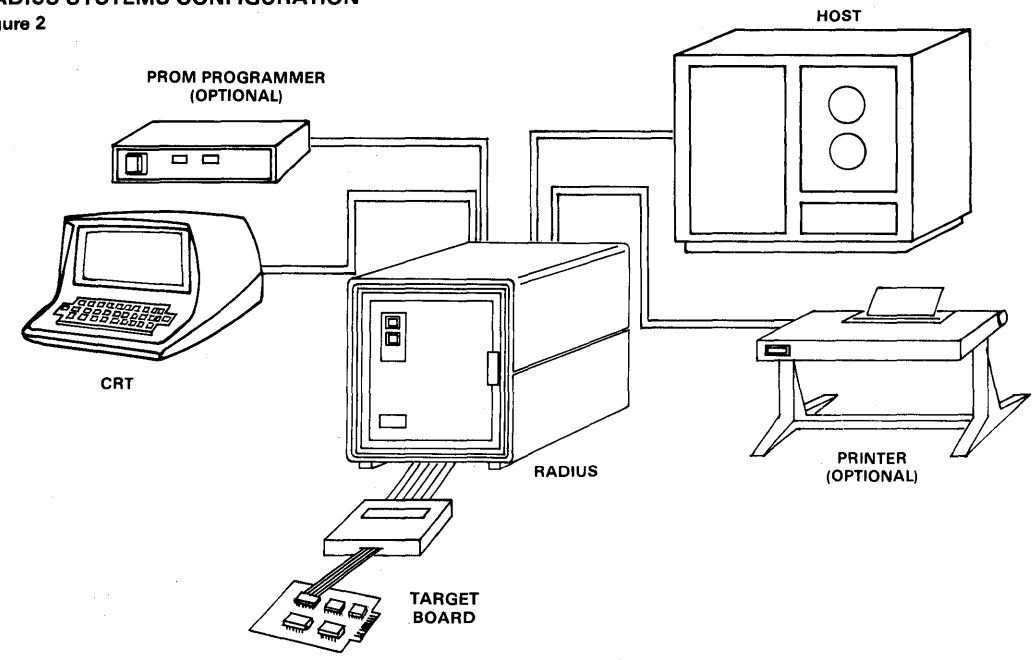
- Set optional Baud rates and special RADIUS control characters
- Perform self diagnostics on RADIUS

In Utility Mode, the user can:

- Run the host components of the RADIUS Utility Packages (i.e. AIM-Z80BE, AIM-7XE, Line Printer Utility, PROM Programmer Utility, etc.).
- Perform hardware debug and software integration.

RADIUS has no mass storage. Instead it uses the mass storage capabilities of the host. Once the user's target program is downloaded, the user has the option of disconnecting the RADIUS from the host. This allows the user to save connect time and long distance charges.

RADIUS SYSTEMS CONFIGURATION
Figure 2



RADIUS can be configured in a single-user environment or in a multi-user environment, in which several RADIUS units are connected to an appropriate host and operated simultaneously, performing entirely separate jobs. This configuration supports the development of multiple microprocessor/microcomputer systems. See Figure 3.

DEVELOPMENT SYSTEM

RADIUS is a cost effective microcomputer development tool. It consists of an integrated cabinet, power supply, I/O panel, and a Z80 based processor module with four serial I/O ports.

RADIUS is supplied with a host communications software package configured for several popular mini/microcomputer systems. (See ordering information.) A user rehostable version is available for other host computers. Additional preconfigured versions of the RADIUS host software will be provided in the future.

RADIUS HARDWARE FEATURES

RADIUS consists of a structural foam cabinet, a Z80 based RADIUS processor board, and a power supply board. The user can add AIM-68000, AIM-Z80BE, or AIM-7XE modules to RADIUS to perform the full range of real time in-circuit emulation needed for hardware development and software integration. Future AIM products will be completely supported on RADIUS.

The cabinet is divided into two compartments: the power supply compartment on the left and the processing compartment on the right. The processing compartment can house up to five boards: a RADIUS processor board, two-card AIM module set, and two slots for future expansion.

The RADIUS processor board contains:

- Z80 CPU
- 64 Kbyte internal systems memory
- Four SIO ports;
  - one dedicated to user terminal, one to the host computer, and two for optional printer and PROM programmer
  - RADIUS supports 11 standard Baud rates from 50 to 9600 Baud

RADIUS SOFTWARE FEATURES

- Local mode to set options on RADIUS and to perform local diagnostics
- Most link parameters set at host configuration time
- Full AIM command set available
- AIM packages can run command files from the host
- AIM packages can log all terminal output to the host
- Progress of download/upload indicated on CRT
- Protocol re-transmits messages upon line error
- Self-explanatory error messages
- Translators to convert INTELHEX, TEKHEX, Motorola S-Record, and F8HEX object formats to Mostek HEX
- Local PROM programming (optional)
- Local printing (optional)
- Self diagnostic test

RADIUS local mode provides the following commands:

- HELP
- PORT
- MEMORY
- OPTIONS
- DIAGNOSE
- QUIT

SPECIFICATIONS

The power supply board has single phase AC input at 47 Hz to 63 Hz for the following voltage ranges:

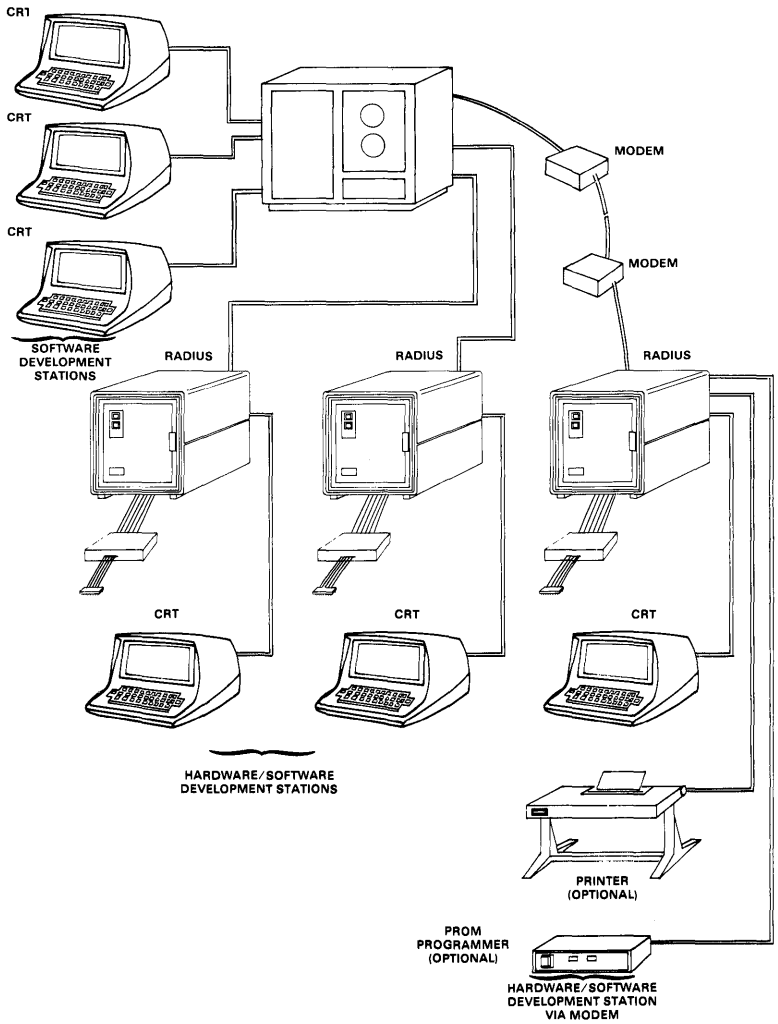
- 95 V to 132 V
- 190 V to 264 V

The approximate dimensions are:

- Width: 9.2"
- Height: 10.8"
- Depth: 12.6"

RADIUS INSTALLATION IN A MULTI-USER ENVIRONMENT

Figure 3



ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

AIM-68000

FEATURES

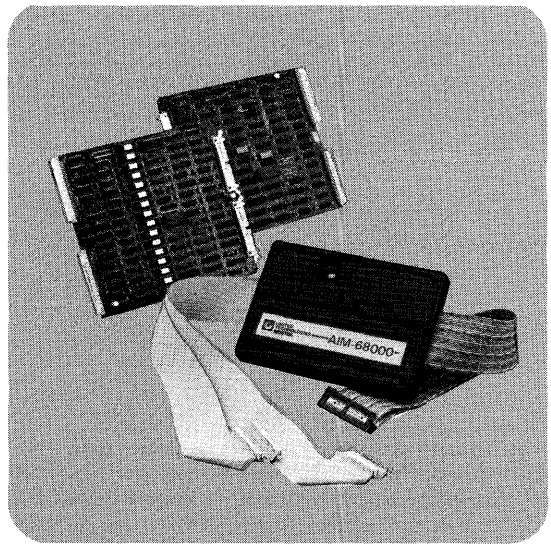
- In-circuit emulation for the MK68000 processor
- Real-time execution to 10 MHz with no wait states
- Direct interface to Mostek's RADIUS Station and MATRIX Development System
- 16K words of Emulation Memory mappable in 2K word blocks on 2K address boundaries; Illegal "Write-to-Memory" Detection provided
- "Stand-alone" Mode allows Software Debug with no Target System
- Flexible breakpoints: Hardware, Software, and Timer
- Single Step execution with Break on Register Contents
- Instruction trace memory for tracing Instruction Execution History ("Soft Trace")
- Exception Handler Routines provided
- Symbolic Addressing Capabilities
- Batch Mode and User Activity Logging provided
- Extensive HELP facility
- Disassembly of Instructions in memory
- English oriented Command Structure

GENERAL DESCRIPTION

AIM-68000 is an advanced development tool which provides debug assistance for both hardware and software via in-circuit emulation of the MK68000 microprocessor. All CPU signals are active during user program execution. No memory wait states are required.

The user friendly command structure consists of English-like commands. A structured HELP facility and the ability to enter keywords allow easy system familiarization. As the user becomes more familiar with the system, commands may be abbreviated. A BATCH facility with PAUSE allows a list of commands on the host to be executed. This feature is useful for test environments and lengthy program setups.

AIM-68000
Figure 1



Single Step capability allows the user to execute instructions one at a time and examine registers to see the exact effect of each instruction. The Single Step function operates in either ROM or RAM.

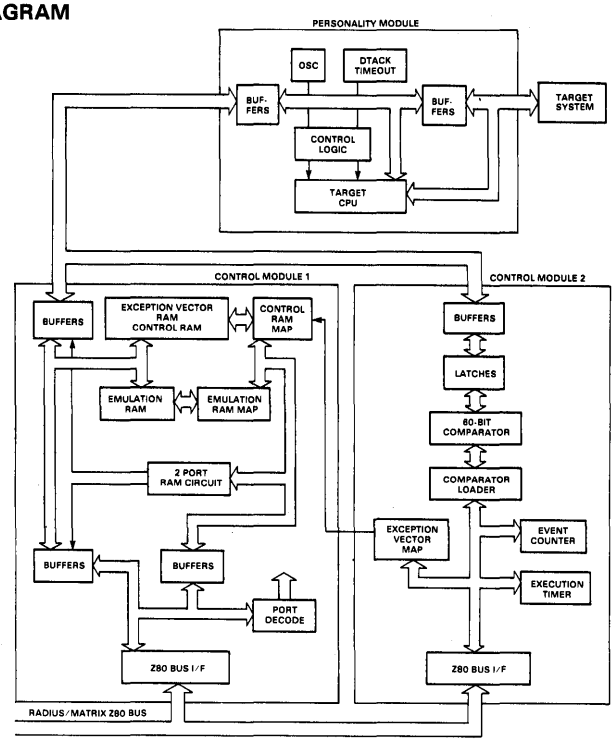
Up to 16K words of Emulation RAM can be used to emulate user Target ROM or RAM. This memory may also be used while the emulator operates in Stand-alone mode, allowing software development prior to hardware availability.

AIM-68000 breakpoint conditions allow 8 software breakpoints, one hardware breakpoint, and one timer breakpoint to be set.

The Hardware Breakpoint detect circuitry allows user program execution to proceed until a specified bus condition occurs. The Breakpoint consists of address, data, function codes, and an external "ARM" bit which allows the Hardware Breakpoint to be slaved to an external TTL input. Any of the Breakpoint condition bits may be designated as a "don't care" bit by setting the "match bits" option. An Event Count and Timer Breakpoint further enhance the Hardware Breakpoint facility.

A software Trace Buffer allows the storage of register

AIM68000 BLOCK DIAGRAM
Figure 2



contents and processor status during single step or Invisible Trace. Invisible Trace allows single stepping to proceed with no information displayed at the user's console. A powerful additional feature of the software trace is the Register Content Breakpoint Function which forces stepping to stop upon the occurrence of a specified set of register conditions. The Trace Buffer may be Reviewed after stepping terminates.

BLOCK DIAGRAM DESCRIPTION

The AIM-68000 emulator consists of two boards, Control 1, Control 2, and a Personality Module. The two control boards are attached to the personality module which contains the MK68000 CPU and plugs into the Target system CPU socket directly. Switch options in the personality module allow the user to operate AIM-68000 in a Stand-alone mode.

Control Board 1 contains the Emulation Memory, the Emulation Memory Map, Control RAM, the Control RAM Map, and the two port memory access circuitry. In addition, the Write Violation Detect circuitry is located on Control Board 1.

Control Board 2 contains circuitry for the Hardware Breakpoint, Timer Breakpoint, the Exception Vector Map, and Keyboard Escape.

The Personality Module contains an on board 10 MHz clock generator, the DTACK timeout hardware, and a number of buffers and associated steering logic.

USING AIM-68000

When AIM-68000 is attached to the user Target System, it effectively becomes part of the user's system. It is important to understand the implications of this addition. The considerations may be grouped into four areas. They are:

1. System (i.e., Emulation) Memory
2. Control Memory
3. Exception Vector Memory
4. MK68000 CPU Control Signals

SYSTEM MEMORY

System Memory may be mapped into or out of the user's memory space via the MAP command. If a block of memory is mapped as System resident, the memory will appear in the user's memory map. AIM-68000 provides a DTACK signal to the MK68000 CPU for those areas which are mapped as System and the memory cycles terminate with no wait states.

CONTROL MEMORY

Control Memory: AIM-68000 requires 1K words of the user's memory space. The default location for this memory is 24000H; however, it may be relocated via the INIT

command to reside anywhere in the MK68000 memory space. Control Memory is a two-port memory which may be accessed both by the MK68000 and the development system's Z80 CPU. The user software must not access the 1K word area of Control Memory.

The MK68000 executes in control memory whenever user software is not being executed. Execution in control memory may include the insertion of several wait states in a memory cycle; however, all user software is executed in real time with no wait states up to 10 MHz.

EXCEPTION VECTOR MEMORY

Exception Vector Memory is located at addresses 0-0FFH. Each exception Vector may be mapped as System or Target resident. If a vector is mapped as System Resident, AIM-68000 will provide the DTACK signal for the MK68000 CPU.

The RESET, NMI, and ILLEGAL INSTRUCTION vectors are special cases and are used to perform emulator functions. They operate as follows:

RESET: Is mapped as System Resident upon Initialization (INIT Command). Immediately after initialization, this vector is mapped as Target resident. It may not be remapped as system resident.

NMI: NMI is a shared Level 7 Autovector interrupt used by both AIM-68000 and the user. It may be mapped as either System or Target resident. If it is mapped as System resident, the response to a Level 7 Autovector Interrupt will be a message displayed on the user console. The user NMI vector is read from the Target system prior to execution. The user must not alter the Level 7 Autovector during program execution.

ILLEGAL INSTRUCTION: Illegal Instruction is the vector used by AIM-68000 to generate the Software Breakpoint. It may be mapped as either System or Target resident. The user Illegal Instruction vector is read from the target system prior to the start of execution. The user must not alter the vector during program execution.

Since the actual exception vectors fetched by the MK68000 are not always the vectors in Target memory, the user should not attempt to run memory verification programs on the Exception Vector Table.

MK68000 CPU CONTROL SIGNALS

All address lines, address strobe, and data strobes are presented to the Target System at the CPU socket for all memory accesses, whether they are for Target or AIM-68000 system resident memory. Data is presented on the data lines only during memory write cycles. MK68000 signal delay information is provided in the Specifications section.

AIM-68000 SOFTWARE

AIM68K is the software which operates the AIM-68000 emulator in either the RADIUS or MATRIX development system. In the RADIUS environment, Target software programs are generated and assembled on the host computer. The hex object module is downloaded into AIM-68000 and/or Target memory via the GET command.

The AIM68K software for use with the RADIUS station is available on several different formats for a variety of host computers. The software will be supplied on a flexible diskette for use in the MATRIX Development System.

COMMAND SUMMARY

The user commands for AIM68K are summarized in Table 1. Each command may also be entered in an abbreviated form. Keywords are allowed in the command syntax to promote rapid user familiarization.

AIM-68000 USER COMMANDS

Table 1

COMMAND	DESCRIPTION
ACCESS	Define memory accesses as word or byte
BASE	Set or Display Memory Offset
BATCH	Submit a Batch File
BREAK	Set or Display a Breakpoint
	Hardware Breakpoint
	Event Count for Hardware Breakpoint
	Trigger for Hardware Breakpoint
	Mask for Hardware Breakpoint
	Software Breakpoint (RAM only)
	Timer Breakpoint
	Register Contents Breakpoint (for use with STEP or GO command)
CLEAR	Clear one or more Breakpoints
COPY	Copy a block of memory to another area
DELETE	Delete a symbol
DISASSEMBLE	Disassemble instructions in memory
DUMP	Dump memory to a file
EXECUTE	Begin user program execution
FILL	Fill memory with a data pattern
GET	Load user program or mapping configuration
GO	Invisible Single Step with Trace
HELP	Display command syntax and description
	Structured to provide two levels of information for commands
HEXADECIMAL	Evaluate a hexadecimal expression
INITIALIZE	Initialize AIM-68000; Relocate Control Memory
LOCATE	Locate a pattern of data in memory
LOG	Log user activity to a host file
MAP	Map emulation memory into target memory space
MEMORY	Display and/or update memory
QUIT	Terminate AIM-68000 operation
RAMTEST	Test RAM memory; continuous test option
REGISTER	Examine or modify register contents
REVIEW	Examine the Software Trace buffer
SELECT	Choose registers or symbols for Step and Trace Display
SET	Set Exception Vector Map
SYMBOL	Enter or display symbols in table
STEP	Single Step with Software Trace
TRANSPARENT	Communicate with the host transparently
VERIFY	Verify memory against other memory

Note that the ACCESS command limits emulator accesses to word wide or byte wide operations only. A write only option for the MEMORY command allows the user to set up programmable peripheral devices manually.

SPECIFICATIONS

Target Operating Frequency	1.0 to 10 MHz
Standalone Operating Frequency	10 MHz
Operating Temperature Range	0° - 40°C
Target Power Requirement	None

Signals from the MK68000 have the following maximum delays:

Signal	Delay
A1-23	0 ns
/AS	0 ns
/BERR	40 ns
/BR	22 ns
/BG	0 ns
/BGACK	0 ns
CLK*	8 ns
D0-D15 t_{CLDO}**	145 ns @ 10 MHz 135 ns @ 8 MHz 100 ns @ 6 MHz
/LDS,/UDS	0 ns
/DTACK	14 ns
E	0 ns
FC2-0	0 ns
/HALT	0 ns
IPL2-0	40 ns
R/W	0 ns
/RESET	0 ns
/VMA	0 ns
/VPA	20 ns

* Skew from the Target CLK to the MK68000 CLK input.

** On a write cycle, DATA valid at the Target after the falling edge of S2, t_{CLDO} max.

ORDERING INFORMATION

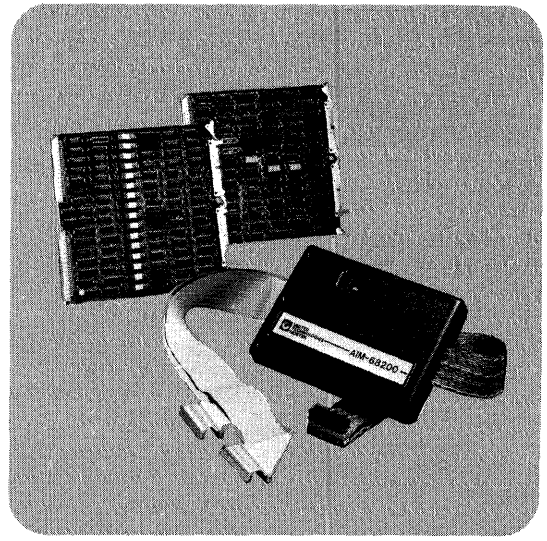
For information on ordering AIM-68000 hardware and the appropriate AIM68K software, refer to the Development Products Ordering Guide.

AIM-68200

FEATURES

- In-Circuit Emulation for the MK68200 family of microcomputers
- Real-time execution to 4 MHz, with no wait states
- Direct interface to Mostek's RADIUS Station and MATRIX Development System
- 16K words of Emulation Memory mappable in 2K word blocks on 2K address boundaries. Illegal "Write-to-Memory" Detection provided
- Stand-alone Mode allows Software Debug with no Target System
- Flexible breakpoints: Hardware, Software, and Timer
- Single-step execution
- Interrupt Handler Routines provided
- Symbolic Addressing Capabilities
- Batch Mode and User Activity Logging provided
- Extensive HELP facility
- Disassembly of Instructions in memory
- English oriented Command Structure

AIM-68200
Figure 1



GENERAL DESCRIPTION

AIM-68200 is an advanced development tool that provides debug assistance, for both hardware and software, via in-circuit emulation of the MK68200 family of microcomputers. All signals are active during user program execution. No memory wait states are required.

The user friendly command structure consists of commands similar to English. A structured HELP facility and the ability to enter keywords allow easy system familiarization. As the user becomes more familiar with the system, commands may be abbreviated. A BATCH facility with PAUSE allows a list of commands on the host to be executed. This feature is useful for test environments and lengthy program setups.

Single-step capability allows the user to execute instructions one at a time and examine registers to see the exact effect of each instruction. The Single-step function operates in either ROM or RAM.

Up to 16K words of Emulation RAM can be used to emulate user Target ROM or RAM. This memory may also be used while the emulator operates in Stand-alone Mode, allowing software development prior to hardware availability.

AIM-68200 breakpoint conditions allow eight software breakpoints, one hardware breakpoint, and one timer breakpoint to be set.

The hardware breakpoint detect circuitry allows user program execution to proceed until a specified bus condition occurs. The breakpoint consists of address, data, and an external "ARM" bit that allows the hardware breakpoint to be slaved to an external TTL input. Any of the breakpoint

condition bits may be designated as a "don't care" bit by setting the "match bits" option. An event count and timer breakpoint further enhance the hardware breakpoint facility.

BLOCK DIAGRAM DESCRIPTION

The AIM-68200 emulator consists of two boards, Control 1, Control 2, and a Personality Module. The two control boards are attached to the Personality Module, which contains the MK68200, and plugs directly into the target system's socket. Switch options in the Personality Module allow the user to operate AIM-68200 in a Stand-alone Mode.

Control Board 1 contains the Emulation Memory, Emulation Memory Map, Control RAM, the Control RAM Map, and two port memory access circuitry. In addition, the Write Violation Detect circuitry is located on Control Board 1.

Control Board 2 contains circuitry for the Hardware Breakpoint, Timer Breakpoint, Interrupt Vector Map, and Keyboard Escape.

The Personality Module contains an on board 4 MHz clock generator, DTACK timeout hardware, and a number of buffers and associated steering logic.

USING AIM-68200

When AIM-68200 is attached to the user's Target System, it effectively becomes part of the user's system. It is important to understand the implications of this addition. The considerations may be grouped into the following three areas:

1. System (i.e., Emulation) Memory.
2. Interrupt Vector Memory.
3. MK68200 Control Signals.

SYSTEM MEMORY

System Memory may be mapped into or out of the user's memory space via the MAP command. If a block of memory is mapped as System resident, the memory will appear in the user's memory map. AIM-68200 provides a DTACK signal to the MK68200 for those areas that are mapped as System, and the memory cycles terminate with no wait states.

INTERRUPT VECTOR MEMORY

Interrupt Vector Memory is located at addresses 0-1FH. Each Interrupt Vector may be mapped as System or Target resident. If a vector is mapped as System resident, AIM-68200 will provide the DTACK signal for the MK68200.

The RESET and NMI Vectors are special cases and are used to perform emulator functions. They operate as follows:

RESET: Mapped as system resident upon RESET (via the INIT Command or executed as part of the software power-up sequence). Immediately after initialization, this vector is mapped as target resident. It may not be re-mapped as system resident.

NMI: Shared by both AIM-68200 and the user. It may be mapped as either System or Target resident. If it is mapped as System resident, the response to an NMI will be a message displayed on the user console. The user NMI Vector is read from the Target system prior to execution. The user must not alter the NMI Vector during program execution.

Since the actual Interrupt Vectors fetched by the MK68200 are not always the vectors in Target Memory, the user should not attempt to run memory verification programs on the Interrupt Vector Table.

MK68200 CONTROL SIGNALS

In any expanded mode, all address/data lines and address strobe are presented to the Target system at the MK68200 socket for all memory accesses, whether they are for Target or AIM-68200 System resident memory. Data strobe(s) will be presented only if the memory access is to Target memory. Data is presented on the data lines only during memory write cycles. MK68200 signal delay information is provided in the Specification section.

AIM-68200 SOFTWARE

AIM-68200 is the software that operates the AIM-68200 emulator in either the RADIUS or MATRIX development system. In the RADIUS environment, Target software programs are generated and assembled on the host computer. The hex object module is downloaded into System and/or Target memory via the GET command.

The AIM-68200 software for use with the RADIUS station is available in several different formats for a variety of host computers. The software will be supplied on a flexible diskette for the MATRIX development system.

COMMAND SUMMARY

The user commands for AIM-68200 are summarized in Table 1. Each command may also be entered in an abbreviated form. Keywords are allowed in the command syntax to promote rapid user familiarization.

AIM-68200 USER COMMANDS

Table 1

COMMAND	DESCRIPTION
ACCESS*	Define memory accesses as word or byte
BASE	Set or Display Memory Offset
BATCH	Submit a Batch File
BREAK	Set or Display a Breakpoint
	Hardware Breakpoint
	Event Count for Hardware Breakpoint
	Trigger for Hardware Breakpoint
	Mask for Hardware Breakpoint
	Mode for Hardware Breakpoint
	Segment for Hardware Breakpoint
	Software Breakpoint (RAM only)
	Timer Breakpoint
CLEAR	Clear one or more Breakpoints
COPY	Copy a block of memory to another area
DELETE	Delete a symbol
DISASSEMBLE	Disassemble instructions in memory
DUMP	Dump target memory to a file
EXECUTE	Begin user program execution
FILL	Fill target memory with a data pattern
GET	Load user program or mapping configuration
HELP	Display command syntax and description
	Structured to provide two levels of information for commands
HEXADECIMAL	Evaluate a hexadecimal expression
INIT	Initialize AIM-68200; Relocate Control Memory
LOCATE	Locate a pattern of data in memory
LOG	Log user activity to a host file
MAP	Map emulation memory into target memory space
MEMORY	Display and/or update memory
MODE	Display or select mode of operation
PORT	Display or write to port
QUIT	Terminate AIM-68200 operation
RAMTEST	Test RAM memory; continuous test option
REGISTER	Examine or modify register contents
SEGMENT	Display or select segment
STEP	Single Step with Software Trace
SYMBOL	Enter or display symbols in table
TRANSPARENT	Communicate with the host transparently
VECTOR	Display or set Interrupt Vector Map
VERIFY	Verify memory against other memory

*Note: The ACCESS command limits emulator accesses to word wide or byte wide operations only. A write only option for the MEMORY command allows the user to manually set up programmable peripheral devices.

XI

SPECIFICATIONS

Target Operating Frequency:

1.0 to 4.0 MHz

Operating Temperature Range:

0° - 40°C

Stand-alone Operating Frequency:

4 MHz

Target Power Requirement:

None

MAXIMUM DELAYS OF SIGNALS FROM/TO THE MK68200

SIGNAL	NON-EXP	GP-EXP	UPC-EXP
$\overline{DS}$,$\overline{LDS}$,$\overline{UDS}$	—	33 ns	33 ns
$\overline{NMI}$	56 ns	56 ns	56 ns
$\overline{RESET}$	30 ns	30 ns	30 ns
STRH	20 ns	20 ns*	20 ns*

* 0 ns if system's mode logic is switched out.

EXTRA LOADING OF SIGNALS INTO THE MK68200

SIGNAL	NON-EXP	GP-EXP	UPC-EXP
AD15-AD0	20 μA/ -0.4 mA	20 μA/ -0.4 mA	20 μA/ -0.4 mA
$\overline{BUSOUT}$,$\overline{BR}$	—	20 μA/ -0.6 mA	—
$\overline{BUSIN}$,$\overline{BG}$	—	20 μA/ -0.6 mA	20 μA/ -0.6 mA
$\overline{BGACK}$	—	—	20 μA/** -0.6 mA
CLKOUT	20 μA/ -0.4 mA	20 μA/ -0.4 mA	20 μA/ -0.4 mA
MODE	20 μA/ -0.4 mA	20 μA/ -0.4 mA	20 μA/ -0.4 mA
$\overline{AS}$	55μA***	55μA***	55μA***

* Delay to MK68200 from fall of $\overline{NMI}$. A second $\overline{NMI}$ from the target may not be asserted for approximately 6.5 ms after the first $\overline{NMI}$ is asserted.

** Pulled high with 100K resistor UPC only

*** Pulled high with 100K resistor

DIFFERENT LOADING OF SIGNALS INTO THE MK68200

SIGNAL	NON-EXP	GP-EXP	UPC-EXP
STRH		20 μA/ -0.4 mA*	

*Same as MK68200 if system's mode logic is switched out.

ORDERING INFORMATION

For information on ordering AIM-68200 hardware and the appropriate AIM-68200 software, refer to the Development Systems Products Ordering Guide, located in the Computer Products Data Book under Development Systems.

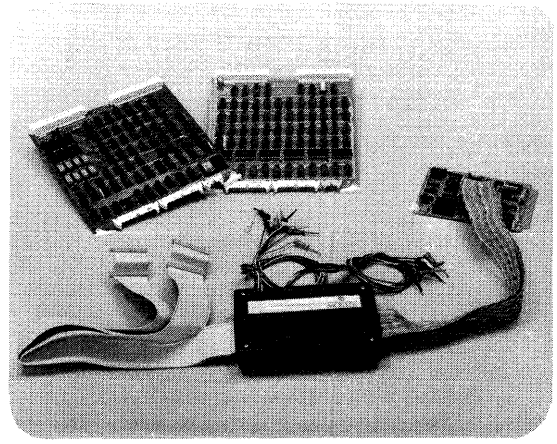
AIM-Z80BE APPLICATION INTERFACE MODULE

FEATURES

- Direct interface to Mostek's RADIUS Development Station and MATRIX-80/SDS Development System
- In-circuit emulation of the Z80 microprocessor
- Real-time execution (to 6 MHz with no wait states)
- Flexible breakpoints (one hardware, eight software, and one timer)
- Single-step execution
- 16 K bytes of emulation RAM
- Memory mappable into target or AIM system memory in 256 byte blocks
- Illegal write-to-memory detection
- Non-existent memory mapping and access detection
- Forty-eight-channel-by-1024-words history memory for tracing bus events
- T-state timer to measure execution time
- English-oriented command structure
- Disassembly of instructions
- System configuration parameters can be saved for future use

AIM-Z80BE PRODUCTS

Figure 1



GENERAL DESCRIPTION

AIM-Z80BE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit-emulation of the Z80 microprocessor. Use of the AIM-Z80BE is transparent to the user's final system configuration (referred to as the "target"). No memory space or user ports are used, and all signals, including $\overline{\text{RESET}}$ $\overline{\text{INT}}$, and NMI are functional during emulation. No memory wait states are required.

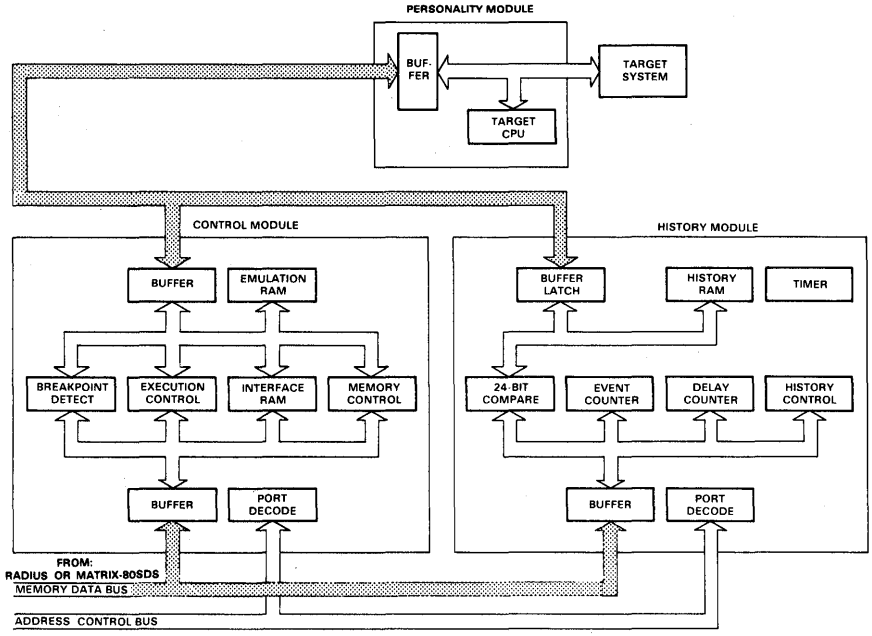
Single-step circuitry allows the user to execute target instructions one at a time to see the exact effect of each instruction. Single step is functional in both ROM and RAM. Up to 16K bytes of contiguous emulation RAM can be used to emulate the target microprocessor RAM or ROM. Thus, debugging can begin before the user system is completely configured with memory.

Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate execution. All CPU status information and register contents can be displayed for the user and saved for later continuation of execution or single-stepping. Real-time execution may be terminated by the user at any time. EVENT and DELAY counters associated with the hardware breakpoint give added flexibility for viewing the exact point of interest in the user's program.

A forty-eight channel history memory records up to 1024 bus transactions. The address bus, data bus, control signals, and 18 external probes may be logged into the history memory and later displayed by the user.

AIM-Z80BE BLOCK DIAGRAM

Figure 2



BLOCK DIAGRAM DESCRIPTION

The Z80 emulation system is composed of two boards, the Control Module and the History Module, as shown in Figure 2. These boards are attached to a Personality Module which contains the target CPU and plugs directly into the target system CPU socket. Address, data, and control signals are buffered by the Personality Module and cabled to the Control and History Module installed in the development system.

The Control Module has the circuitry for detecting the breakpoint condition(s) and forces program execution to begin in a separate System Interface RAM. The System Interface RAM is loaded with an interface program and is shadowed into the target memory space. This control program makes the target CPU a slave to the development system. When the user desires to resume execution of his program, the control program activates the execution control circuit and execution resumes at the desired address. The Control Module contains 16 K bytes of emulation RAM, which may be mapped into any address space required by the target system. Alternatively, if the user's system has memory available, he may use that as his target memory instead of the memory on the Control Module.

The History Module has a 24-bit comparator circuit, an EVENT counter, and a DELAY counter to detect a hardware breakpoint condition. The 48-channel-by-1024-word history RAM is controlled by the History Control Circuit.

The Timer Circuit is used to count target processor clocks for logging elapsed time and generating the timer breakpoint.

USING THE AIM-Z80BE

The Control and History Modules of AIM-Z80BE are installed directly into the development system. To complete the emulation system the Personality Module is used as a buffer interface between the first two boards and the target system's Z80 CPU socket.

The program which controls the AIM-Z80BE emulator system is AIMZ80. After execution of AIMZ80 is started, the program takes control of the AIM-Z80BE emulation system. The user can then initialize the target system and use the AIMZ80 commands to load, test, and debug the target program.

AIMZ80 SOFTWARE

AIMZ80 is the software which operates the AIM-Z80BE emulation system in the RADIUS Development Station or MATRIX Development System. Target system programs may be developed on a Mostek disk system by use of the appropriate assembler. Programs may be developed for RADIUS cross products supplied by Mostek or other vendors. The AIM software is supplied on a variety of media for use with Mostek disk-based development systems and with different host systems for RADIUS. The commands available in AIMZ80 are summarized below. Each command also has a "short form" which allows abbreviated input with fewer keystrokes.

BATCH	Read AIM commands from a file
BREAK	Display and set breakpoints (8 software, 1 hardware, and 1 timer breakpoint)
CLEAR	Clear one breakpoint or all breakpoints
COPY	Copy one block of memory to another block
DISABLE	Disable target CPU interrupts
DISASSEMBLE	Display and/or update instructions
DUMP	Dump a block of memory to a file
	Dump the memory map to a file
ENABLE	Enable target CPU interrupts
EXECUTE	Start or continue execution of the target program
FILL	Fill memory with a data byte
GET	Load a target program into memory
	Load the target memory map from a file
HEXADECIMAL	Perform hexadecimal arithmetic
HELP	Display a menu of commands for the user
HISTORY	Set history logging options
INIT	Reinitialize target handshake
LOCATE	Locate a pattern in a memory block
LOG	Log all console output to a file
MAP	Map the block of memory as target supplied, AIM system supplied, or non-existent, and write protected or not write protected
MEMORY	Display and/or update memory
OFFSET	Set an offset value for relative module debugging
PORT	Display and update a port on the target CPU
	Output a value to a port without reading it
QUIT	Return to the resident operating system
RAMTEST	Perform a test on the target RAM
REGISTER	Display and/or update the target CPU registers
STATUS	Display the current status of the AIM system
STEP	Perform a single or multi-step execution
TRACE	Display the contents of the history RAM
TRANSPARENT	Allows the RADIUS user to temporarily access the host
VERIFY	Verify the contents of a block of memory with another block or with a file.

SPECIFICATIONS

Target operating frequency: 500 kHz to 6 MHz (MK78204)

Target interface: all signals meet the specifications for the Z80 with the following exceptions:

1. The output low voltage is 0.5 V max at 1.8 mA for the ADDRESS, DATA, IORQ, RFSH, HALT, and BUSAK signals.
2. The input low current is 400 microamps max for the PHI clock, RESET, INT, NMI, and DATA signals.
3. The input high current is 20 microamps for the PHI clock, RESET, INT, NMI, and DATA signals.
4. The signals M1, MREQ, RD, and WR have a maximum of 25 nanoseconds added propagation delay.
5. The input signals RESET, INT, and NMI have a maximum of 45 nanoseconds propagation delay.

Target system power requirements: +5 V ± 5% @ 600 milliamps (maximum)

System compatibility: RADIUS, MATRIX-80/SDS,

Operating temperature range; 0 to +50 degrees C

ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

AIM-7XE APPLICATION INTERFACE MODULE

FEATURES

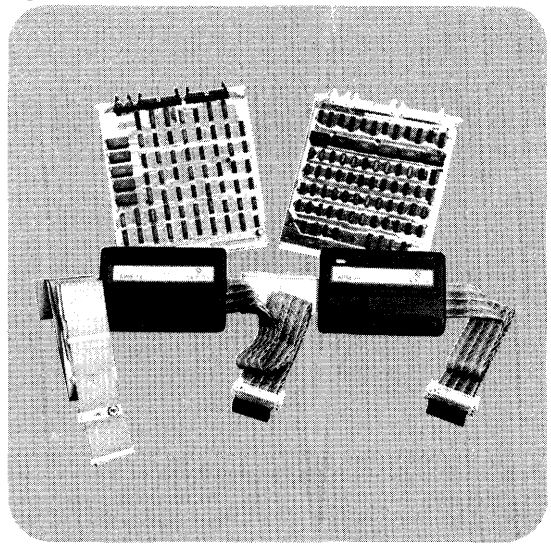
- Direct interface to Mostek's RADIUS Development Station and MATRIX-80/SDS Development System
- In-circuit emulation of all MK3870 and MK3873 family microprocessors (does not include piggy-back parts)
- Real-time execution (to 4 MHz with no wait states)
- Flexible breakpoints (one hardware, eight software, and one timer breakpoint) and any number of manually-inserted breakpoints
- Single-step execution
- 4 K bytes of emulation RAM
- Option of on-board oscillator or user clock
- Illegal write-to-memory detection
- Forty-eight-channel-by-1024-words history memory for tracing bus events
- Event counter and delay counter for monitoring bus events
- T-state timer to measure execution time
- English-oriented command structure
- Disassembly of instructions

GENERAL DESCRIPTION

AIM-7XE is an advanced development tool which provides debug assistance for both software and hardware via in-circuit-emulation of the MK3870 and MK3873 family of microprocessors. Use of the AIM-7XE is completely transparent to the user's final system configuration (referred to as the "target"). No memory space or user ports are used, and all signals, including /RESET and /EXT INT, are functional during emulation. No memory wait states are required.

Single-step circuitry allows the user to execute target instructions one at a time to see the exact effect of each instruction. 4 K bytes of emulation RAM are used to emulate the target microprocessor ROM.

AIM-7XE
Figure 1



Breakpoint-detect circuitry allows real-time execution to proceed to any desired point in the user's program and then terminate execution.

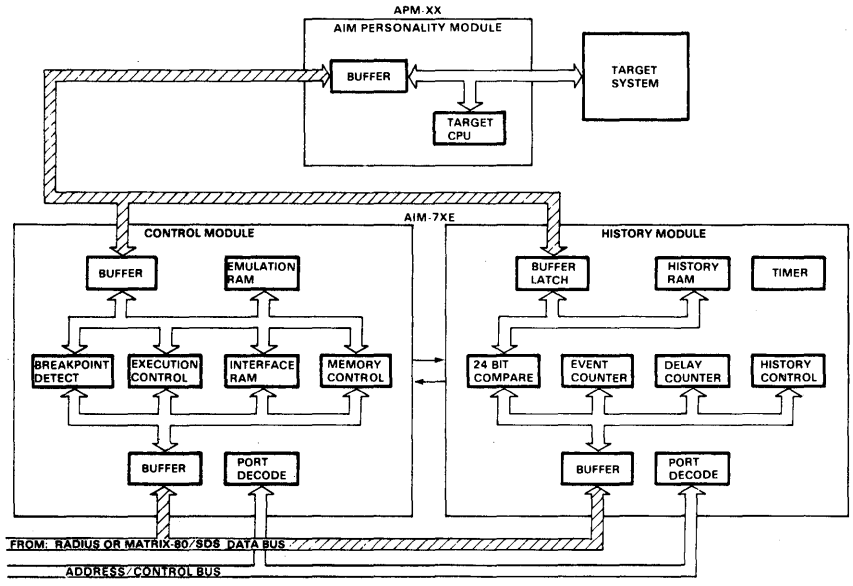
All CPU status information and registers can be displayed for the user and saved for later continuation of execution or single-stepping. Real-time execution may be terminated by the user, at any time. EVENT and DELAY counters associated with the hardware breakpoint give added flexibility for viewing the exact point of interest in the user's program.

A forty-eight channel history memory records up to 1024 bus transactions. The address bus, data bus, ports 0, 1, and either port 4, 5, or 8 external probes may be logged into the history memory and later displayed by the user.

BLOCK DIAGRAM DESCRIPTION

The MK3870 Family emulation system is composed of both the AIM-7XE system and personality modules. AIM-7XE consists of two boards, the Control Module and the History Module, as shown in Figure 2. These boards are attached by cables to the Personality Module which contains the target

AIM-7XE BLOCK DIAGRAM
Figure 2



CPU and plugs directly into the target system CPU socket. Address, data, and control signals are buffered by the Personality Module.

The Control Module has the circuitry for detecting the breakpoint condition(s) and forces program execution to begin in the System Interface RAM. The System Interface RAM is loaded with an interface program and is shadowed into the target memory space. This control program makes the target CPU a slave to the development system. When the user desires to resume execution of his program, the control program activates the execution control circuit and execution resumes at the desired address.

The History Board has a 24-bit comparator circuit, an EVENT counter, and a DELAY counter to detect a hardware breakpoint condition. The 48-channel-by-1024-word history RAM is controlled by the History control circuit. The Timer circuit is used to count target processor clocks for logging elapsed time and generating the timer breakpoint.

USING THE AIM-7XE

The Control and History Modules of the AIM-7XE are installed directly into the Mostek development system. To complete the emulation system a Personality Module is required. This module is a buffer interface between the first two boards and the target system's CPU socket. Note that a complete user target system is not required to do software debugging. Only the AIM-7XE boards and a Personality Module are needed.

The program which controls the AIM-7XE emulator system is named AIM7X. After execution of AIM7X is started, the program takes control of the AIM-7XE emulation system. The user can then initialize the target system and use the AIM7X commands to load, test, and debug the target program.

AIM7X SOFTWARE

AIM7X is the software which operates the AIM-7XE emulation system in the Mostek RADIUS Development Station or MATRIX Development System. Target system programs may be developed on a Mostek disk system for RADIUS™ using cross products supplied by Mostek or other vendors. The AIM7X software is available on a diskette for Mostek disk-based systems and on a variety of media for different host systems for use with RADIUS™. The commands available in AIM7X are summarized below. Each command also has a "short form" which allows abbreviated input with fewer keystrokes.

BATCH	Read AIM commands from a file
BREAK	Display and set breakpoints (8 software, 1 hardware, and 1 timer breakpoint)
CLEAR	Clear one breakpoint or all breakpoints
COPY	Copy one block of memory to another block
DISABLE	Disable target CPU interrupts
DISASSEMBLE	Display and/or update instructions
DUMP	Dump a block of memory to a file
ENABLE	Enable target CPU interrupts
EXECUTE	Start or continue execution of the target program
FILL	Fill memory with a data byte
GET	Load a target program file into memory
HEXADECIMAL	Perform hexadecimal arithmetic
HELP	Display a menu of commands for the user
HISTORY	Set history logging options
INIT	Reinitialize target handshake
LOCATE	Locate a pattern in a memory block
LOG	Log all console output to a file
MEMORY	Display and/or update memory
OFFSET	Set an offset value for relative module debugging
PORT	Display and update a port on the target CPU
QUIT	Return to the resident operating system
RAMTEST	Perform a test on the target RAM
REGISTER	Display and/or update the target CPU registers
STATUS	Display the current status of the AIM system
STEP	Perform a single or multi-step execution
TRACE	Display the contents of the history RAM
TRANSPARENT	Allows the RADIUS user to temporarily access the host
VERIFY	Verify the contents of a block of memory with another block or a file

SPECIFICATIONS

Target operating frequency: 1 to 4 MHz

Target interface: All signals meet the specifications of the MK3870 family except that the XLT2 input will not accept a user crystal. It requires a TTL clock input.

System compatibility: RADIUS, MATRIX-80/SDS

Operating temperature range: 0 to +50°C

ORDERING INFORMATION

For detailed ordering information refer to the Development System Products Ordering Guide.

PRELIMINARY

EPP-1 MK78229 EPROM PROGRAMMER

FEATURES

- Provides EPROM programming capability for RADIUS
- May be adapted for use with other computers
- Communicates with host via half-duplex RS232 or TTL serial link
- Programs, reads, and verifies most +5 V EPROMs available today
- 4 Selectable Baud rates: 300, 1200, 2400, 9600
- Emulates a subset of DATA I/O's System 19 command set
- Includes wall mount transformer power supply
- 8K x 8 bits of on-board RAM
- 28 pin zero-insertion-force socket for 24 and 28 pin EPROMs
- LED indicators for "programming" and "power on".
- High level commands for ease of use with RADIUS

EPP-1
Figure 1

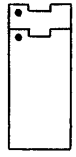
GENERAL DESCRIPTION

The EPP-1 is a microcomputer controlled MOS EPROM programmer capable of programming most MOS EPROMs currently available. It can be upgraded by adding a bipolar PROM to allow programming of new EPROMs when they become available.

The EPP-1 is designed to be used with the RADIUS remote development station. The software for the RADIUS allows use of all the commands supported by EPP-1 and additional higher level commands for ease of use by the operator.

Communication with the host computer is via a serial link which can be RS232 or TTL compatible. Baud rates are selectable to 300, 1200, 2400 or 9600 Baud. The unit is powered by a wall mount transformer which provides unregulated DC voltages to the programmer.

LED indicators are provided to show when the power is on and when an EPROM is being programmed. A 28 pin zero-insertion-force socket is supplied for use with 24 and 28 pin EPROMs. 24 pin EPROMs are inserted with pin 1 of the EPROM in pin 3 of the 28 pin socket as shown below.



I/O COMMANDS

W	Set Address Offset	Sets the specified offset to be subtracted from all incoming addresses and added to all outgoing addresses.
I	Input	Input data from computer to RAM.
O	Output	Output data from RAM to computer.
C	Compare	Compare RAM data with data from computer.

EDITING COMMANDS

\	RAM-RAM Block Move	Initiates transfer of data from one block RAM to another. Block limits must first be set.

PROGRAMMER RESPONSES

>+RETURN + LINE FEED	Prompt character. Informs the computer that the EPROM programmer has successfully executed a command.
F+RETURN + LINE FEED	Fail character. Informs the computer that the EPROM programmer has failed to execute the last-entered command.
?+RETURN + LINE FEED	Question mark. Informs the computer that the EPROM programmer does not understand a command.

TECHNICAL SPECIFICATIONS

Dimensions

7.8 in (19.8 cm) x 10.8 in. (27.4 cm)
2.0 in. (5.1 cm) maximum thickness

ELECTRICAL SPECIFICATIONS

Serial Communication Link

RS232 or TTL compatible

Operating Temperature

20°C to 40°C

Power Supply Requirements

115 V AC @ 200 ma

SOFTWARE

The high level commands supported by the RADIUS software for EPP-1 are:

COMMAND	DESCRIPTION
BATCH 'filename'	Accept command input from a Host file
BIT	Illegal bit test on EPROM
BLANK	Check if EPROM is blank
COMPARE 'filename'	Compare data from Host to EPROM Programmer
DEVICE xxxx	Select the device address to be used for programming, verifying, or loading device data
DIRECT	Allows direct entry of commands to the EPROM programmer via the console. May be terminated with control-C.
FAMILY [xxxx]	Select/display the family/pinout
HELP [Command name]	Display a HELP description of all commands or of a specific command
INPUT 'filename'	Input data from Host to EPROM programmer
LOAD	Load EPROM data from the EPROM into RAM
LOG 'filename'	Log console activity to a Host file
MEMORY xxxx [xxxx]	Display or update EPROM programmer RAM
MOVE xxxx xxxx xxxx	Move a block of data in RAM
OFFSET xxxx	Select an offset to be added to input addresses and subtracted from output addresses
OUTPUT xxxx xxxx 'filename'	Output data from EPROM programmer to Host
*(pause [msg])	Pause while in batch mode; message can be displayed.
PROGRAM	Program EPROM device with data in RAM
QUIT	Exit the utility; return EPROM programmer to keyboard control
RAM xxxx	Select RAM address to be used for data transfer
SHUFFLE xxxx	Merge 2 blocks of RAM; complement of SPLIT
SIZE xxxx	Select the hex number of bytes to be transferred; must be selected after RAM command
SPLIT xxxx	Split even/odd numbered bytes into 2 blocks; complement of SHUFFLE
SUM	Calculate check-sum of programmer RAM
SWAP	Swap nibbles in every byte in RAM
TRANSPARENT	Allows RADIUS development system transparent communication to Host
VERIFY	Verify EPROM device with data in RAM

EPROMs SUPPORTED

The following EPROMs may be programmed by the EPP-1.

MANUFACTURER	PART #	SIZE	FAMILY/PINOUT CONFIGURATION #
ADVANCED MICRO DEVICES	4716	2K x 8	1923
ELECTRONIC ARRAYS	2716	2K x 8	1923
FUJITSU	8516 (2716)	2K x 8	1923
HITACHI	46532	4K x 8	1925
HITACHI	46732	4K x 8	1924
INTEL	2758	1K x 8	1922
INTEL	2716	2K x 8	1923
INTEL	2732	4K x 8	1924
INTEL	2764	8K x 8	3533
MITSUBISHI	2716	2K x 8	1923
MOSTEK	2716	2K x 8	1923
MOTOROLA	MCM2716	2K x 8	1923
MOTOROLA	2532	4K x 8	1925
MOTOROLA	68764	8K x 8	6424
NATIONAL SEMICONDUCTOR	2716	2K x 8	1923
NATIONAL SEMICONDUCTOR	2532	4K x 8	1925
NATIONAL SEMICONDUCTOR	2732	4K x 8	1924
NIPPON ELECTRIC	2716	2K x 8	1923
OKI	2716	2K x 8	1923
TEXAS INSTRUMENTS	2508	1K x 8	1922
TEXAS INSTRUMENTS	2516	2K x 8	1923
TEXAS INSTRUMENTS	2532	4K x 8	1925
TEXAS INSTRUMENTS	2564	8K x 8	3130
TOSHIBA	323	2K x 8	1923

EPP-1 DIRECT COMMAND SUMMARY

CONTROL COMMANDS

RETURN		Execute a command
ESC		Abort a command

UTILITY COMMANDS

G	Software Configuration number	This command returns a 4-digit hex number representing the software configuration of the programmer.
(HHHH)<	Set Begin RAM	BLOCK LIMIT L1. Defines first RAM address (in HEX) to be used for data transfers. Also functions as the RAM source address in the RAM-RAM Block Move command.
(HHHH);	Set Block Size	BLOCK LIMIT L2. Sets number of bytes (in HEX) to be transferred. Must be set after the Set Begin RAM command is used.
(HHHH):	Set Begin Device	BLOCK LIMIT L3. Sets the first device address (in HEX) to be used in data transfers. Also functions as the destination address in the RAM-RAM Block Move Command.
S	Sum-Check	Causes programmer to calculate the check-sum of RAM data and output it to the computer.
F	Error-Status Inquiry	EPROM programmer returns a 32 bit error code.
X	Error-Code	EPROM programmer outputs Error Codes stored in scratchpad RAM and then clears them from memory.
H	No operation	This is a null command and always returns a prompt character (>).

DEVICE COMMANDS

T	Illegal Bit Test	Test for illegal bit in a device.
B	Blank Check	Check that no bits are programmed in a device.
[	Family and Pinout	EPROM programmer sends a 4-digit number (FFPP) where FF is the family code and PP is the pinout in effect.
(FFPP)@	Select Family and Pinout	A 2-digit family code (FF) and pinout code (PP) specifies programming of a particular device.
R	Respond	Programmer indicates status and outputs device word limit, byte size, and programming pulse polarity.
L	Load	Load device data into RAM.
P	Program	Program RAM data into device.
V	Verify	Verify device against RAM.

ORDERING INFORMATION

Designator	Description	Part No.
EPP-1	EPROM PROGRAMMER w/wall mount transformer (US)	MK78229-0
EPP-1	EPROM PROGRAMMER w/in line transformer (international)	MK78299-1
	EPP-1 Technical Manual	4420379

VME MATRIX 68K MICROCOMPUTER SYSTEM MK75102

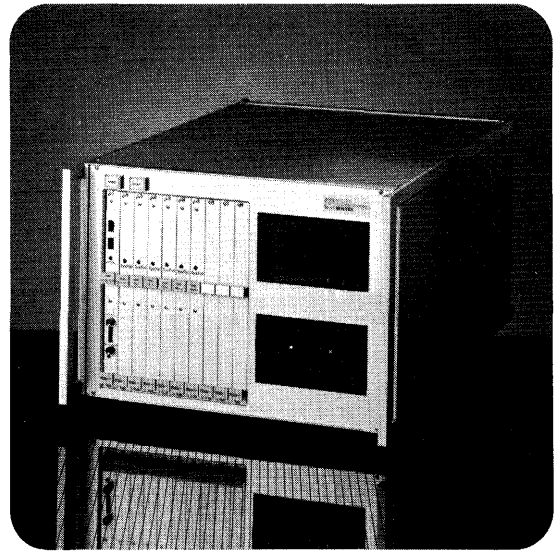
FEATURES

- ☐ VMEbus compatible
- ☐ 68000 Processor and 68451 Memory Management Unit on CPU board
- ☐ 512K byte dynamic RAM with byte parity and longword (32 bit) capability
- ☐ 128K byte additional dual-ported dynamic RAM on CPU board
- ☐ 36M byte (unformatted) 5¼ inch Winchester disc
- ☐ 1M byte (unformatted) 5¼ inch floppy disc
- ☐ Real time calendar clock
- ☐ Parallel (Centronics compatible) output port
- ☐ UNIPLUS+ (UNIX SYSTEM III plus Berkley 4.1 enhancements) * O/S
  - Single processor
  - Multiuser (5 MAX)
- ☐ BOOT68K MONITOR (firmware)
  - Initialization
  - Bootstep loading
  - Serial host down loading
  - Diagnostics
  - Transparent mode
  - Console interface
- ☐ 68000 ASSEMBLER
- ☐ C COMPILER
- ☐ DIAGNOSTIC PACKAGE
- ☐ 3 Spare VMEbus slots for expansion, backplane 32 bit data paths
- ☐ FCC Approved

*NOTE:
UNIX is a trademark of BELL LABORATORIES.
UNIPLUS+ is a trademark of UNISOFT SYSTEMS.

VME MATRIX 68K SYSTEM

Figure 1



MATRIX 68K DESCRIPTION

The MATRIX 68K is a multiuser, VMEbus based, UNIX system designed around the powerful 68000 microprocessor. The MATRIX 68K has seven VMEbus compatible cards (see Figure 2), 36M byte of Winchester hard disk storage and 1M byte of floppy storage. The system also has five serial ports, one parallel printer port (Centronics compatible) and 640K byte of main memory (512K byte on the DRAM and 128K byte on the MMCPU). All of this is packaged in an enclosure measuring 12.25 inches high x 17.75 inches wide x 26 inches deep, containing a ten slot double-VME motherboard (fully capable of 32-bit data transfers), Mostek I/O Panels and a power supply available in either 115 or 230 volt AC versions.

The software provides the ability to efficiently develop software for VMEbus applications. The MATRIX68K software includes the UniPlus+ (UNIX System III) Operating System, 68000 Assembler, C Compiler and a Mostek system diagnostic package. The system firmware, BOOT 68K, initializes the system, controls bootstrap loading and has a number of convenient utilities.

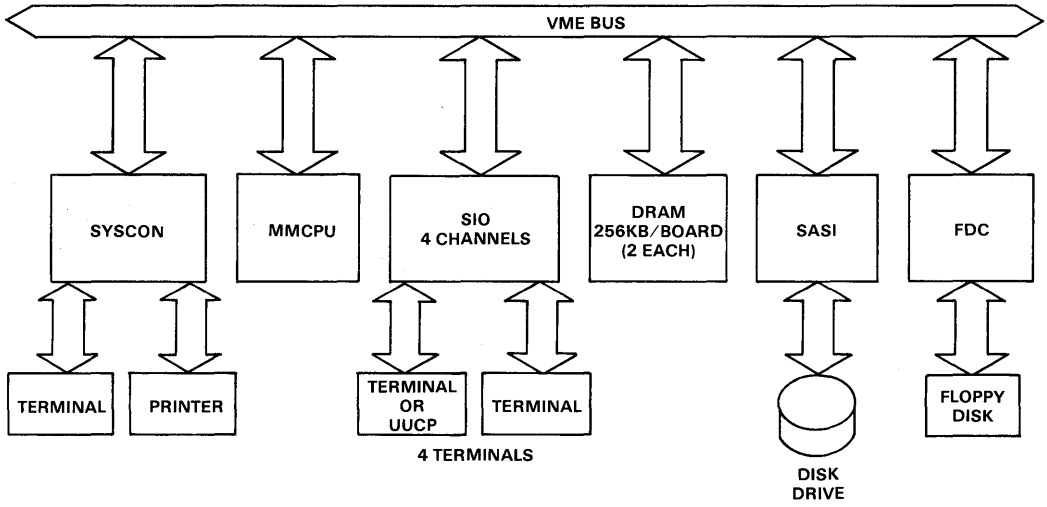
OPTIONAL SOFTWARE PACKAGES

The following software packages are available as additions to the basic software described above:

- FORTRAN COMPILER
- PASCAL COMPILER
- MOSTEK MACRO ASSEMBLER/LINKER 68000
- RECONFIGURATION OPTION

MATRIX 68K BLOCK DIAGRAM

Figure 2



MATRIX™-80/SDS MICROCOMPUTER DEVELOPMENT SYSTEM

INTRODUCTION

The Mostek MATRIX™ is a complete state-of-the-art, floppy disk-based computer. Not only does it provide all the necessary tools for software development, but it provides complete hardware/software debug through Mostek's AIM™ series of in-circuit emulation cards for the 68000, Z80, and the 3870 family of single-chip microcomputers. The MATRIX has at its heart the powerful OEM-80E (Single Board Computer), the RAM-80BE (RAM I/O add-on board), and the FLP-80E (floppy disk controller board). Because these boards and software are available separately to OEM users, the MATRIX serves as an excellent test bed for developing systems applications.

The disk-based system eliminates the need for other mass storage media and provides ease of interface to any peripheral normally used with computers. The file-based structure for storage and retrieval consolidates the data base and provides a reliable portable media to speed and facilitate software development.

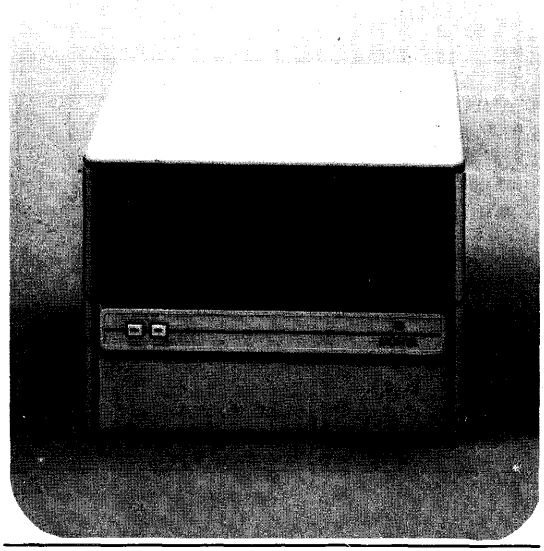
Development System Features

The MATRIX is an excellent integration of both hardware and software development tools for use throughout the complete system design and development phase. Debug can then proceed inside the MATRIX domain using its resources as if they were in the final system. Using combinations of the Monitor, Designer's Debugging Tool, execution time breakpoints, and single step/multistep operation along with a formatted memory dump, provides control for attacking those tough problems. The use of the Mostek AIM™ options provides extended debug with versatile hardware breakpoints on memory or port locations, a buffered in-circuit emulation cable for extending the software debug into its own natural hardware environment.

Package System Features

From a system standpoint, the MATRIX has been designed to be the basis of an end-product, such as a small business/industrial computer. Other hardware options are available, with even more to be added. Expansion of the disk drive units to a total of four single-sided or double-sided units provides up to two megabytes of storage. This computer uses the third-generation Z80 processor supported with the power of a complete family of peripheral chips. Through the use of its 158 instructions, including

MATRIX™-80/SDS
Figure 1



16-bit arithmetic, bit manipulation, advanced block moves and interrupt handling, almost any application from communication concentrators to general purpose accounting systems is made easy.

OEM Features

The hardware and software basis for the MATRIX is also available separately to the OEM purchaser. Through a software licensing agreement, all Mostek software can be utilized on these OEM series of cards.

MATRIX RESIDENT FIRMWARE (DDT-80)

The Designer's Debugging Tool consists of commands for facilitating an otherwise difficult debugging process. The MATRIX allows rapid source changes through the editor and assembler. This is followed by DDT operations which close the loop on the debug cycle. The DDT commands include:

Memory	- display, update, or tabulate memory
Port	- display, update or tabulate I/O ports
Execute	- execute user's program
Hexadecimal	- performs 16 bit add/sub
Copy	- copy one block to another

MATRIX SYSTEM SPECIFICATIONS

- Z80 CPU
- 4K-byte PROM bootstrap and Z80 debugger
- 60K bytes user RAM (56K contiguous)
- 8 x 8 bit I/O ports (4 x PIO) with user-definable drivers/receivers
- Serial port, RS 232 and 20 mA current loop
- 4 channel counter/timer (CTC)
- 2 single-density, single-sided disk drives; 250K bytes per floppy disk
- 3 positions for AIM modules, Serial Interface, etc.
- PROM programmer I/O port. Programmer itself is optional.
- Bus compatible with Mostek SDE series of OEM boards

HARDWARE DESCRIPTION OEM-80E
CPU Module

The OEM-80E provides the essential CPU power of the system. While using the Z80 as the central processing unit, the OEM-80E is provided with other Z80 family peripheral chip support. Two Z80 PIO's give 4 completely programmable 8 bit parallel I/O ports with handshake from which the standard system peripherals are interfaced. Also on the card is the Z80-CTC counter timer circuit which has 3 free flexible channels to perform critical counting and timing functions. Along with 16K of RAM, the OEM-80E provides 5 ROM/PROM sockets which can be utilized for 10/20K of ROM or 5/10K PROM. Four sockets contain the firmware. The remaining socket can be strapped for other ROM/PROM elements.

RAM-80BE

The RAM-80BE adds additional memory with Mostek's MK4116 16K dynamic memory along with more I/O. These two fully programmable 8-bit I/O ports with handshake provide additional I/O expansion as system RAM memory needs to grow. Standard system configuration is 48K bytes for a system total of 60K bytes user RAM (56K contiguous).

FLP-80E

Integral to the MATRIX system is the floppy disk controller. The FLP-80E is a complete IBM 3740 single-density/ double-sided controller for up to 4 drives. The controller has 128 bytes of FIFO buffer resulting in a completely interruptable disk system.

OPTIONAL MODULES COMPATIBLE WITH MATRIX

AIM-68000 (10 MHz max. clock rate)

The AIM-68000 is an advanced development tool which provides project debug capabilities for both hardware and software via in-circuit emulation of the MK68000 Microprocessor. Real-time emulation is provided up to 10 MHz operation. Flexible breakpoints and Single-Step emulation with Invisible Break on Register Contents are provided. Symbolic addressing and an extensive HELP Facility ease the use of AIM-68000.

AIM-Z80BE (6.0 MHz max. clock rate)

The AIM-Z80BE is an improved Z80 In-Circuit-Emulation module usable at Z80-CPU clock rates of up to 6MHz. The AIM-Z80BE is a two processor solution to In-Circuit Emulation which utilizes a Z80-CPU in the buffer box for accurate emulation at high clock rates with minimum restrictions on the target system. The AIM-Z80BE provides real time emulation (no WAIT states) while providing full access to RESET, NMI and INT control lines. Eight single byte software breakpoints (in RAM) are provided as well as one hardware trap (RAM or ROM). The emulation RAM on the AIM-Z80BE is mappable into the target system in 256 byte increments. A 1024 word x 48 bit history memory is triggerable by the hardware intercept and can be read back to the terminal to provide a formated display of the Z80-CPU address, data, and control busses during the execution of the program under test. Several trigger options are available to condition the loading of the history memory.

AIM-7XE

The AIM-7XE module provides debug and in-circuit emulation capabilities for the 3870 series microcomputers on the MATRIX. Multiple-breakpoint capability and single-step operation allow the designer complete control over the execution of the 3870 Series microcomputer.

Register, Port display, and modification capability provide information needed to find system "bugs." All I/O is in the user's system and is connected to AIM-7X by a 40-pin interface cable.

The debugging operation is controlled by a mnemonic debugger which controls the interaction between the Z80 host computer and the 3870 slave. It includes a history module for the last 1024 CPU cycles and also supports all 3870 family circuits.

DCC-80E

The DCC-80E multi-channel serial controller board was developed as a general purpose four port serial I/O card. DCC-80E can be user configured to interconnect computer systems and will support SDLC and BYSINC protocols.

Assembly and linking are done using cross products supplied by Mostek or other vendors.

MECHANICAL SPECIFICATIONS

Overall Dimensions:

CPU subsystem	- 8" High x 21" wide x 22" deep (20.3 cm x 53.3 cm x 55.8 cm)
Disk Subsystem	- 8" High x 21" wide x 22" deep (20.3 cm x 53.3 cm x 55.8 cm)

Humidity: up to 90% relative, noncondensing.

Material: Structural Foam (Noryl)

Weight: CPU Subsystem 25 lbs (11.3 Kg)
Disk Subsystem 50 lbs (22.7 Kg)

Fan Capacity: 115 CFM

Card Cage: Six slots DIN 41612 type connectors

Operating Temperature: +10°C to +35°C

ELECTRICAL SPECIFICATIONS

INPUT 100/115/230 volts AC ± 10%
50 Hz (MK78189) or 60 Hz (MK78188)

OUTPUT

CPU subsystem	+5 VDC at 12A max.
	+12 VDC at 1.7A max.
	-12 VDC at 1.7A max.
Disk subsystem	+5 VDC at 3.0A max.
	-5 VDC at 0.5A max.
	+24 VDC at 3.4A max.

ORDERING INFORMATION

See Development System Products ordering guide.

PERIPHERALS AND CABLES

NAME	DESCRIPTION	PART NO.
PPG-8/16	Programmer for 2708, 2758 and 2716 PROM Includes interfacing cables to MATRIX.	MK79081-1
SD-WW	Wire wrap card compatible with MATRIX.	MK79063
SD-EXT	Extender card compatible with MATRIX.	MK79062
LP-CABLE	Interface cable from MATRIX Microcomputer to Centronics 306 or 702 printer	MK79089
PPG-CABLE	Interface cables from MATRIX to PPG-8/16 PROM programmer (MK79081).	MK79090

EVAL-70
3870 EVALUATION SYSTEM

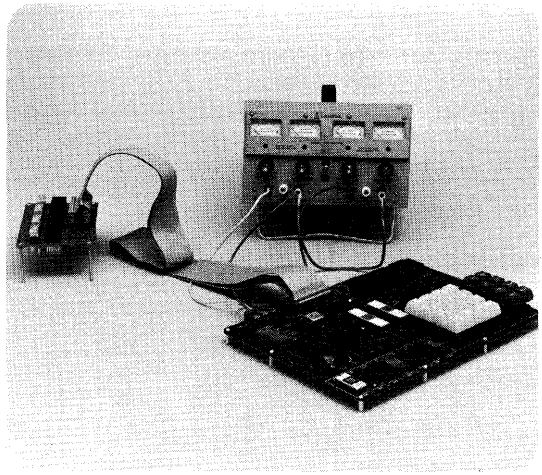
FEATURES

- An ideal hardware and/or software design aid for the MK38P70 and MK3870 family of Single-Chip Microcomputers
- Includes a 2K byte firmware monitor
- Keypad for command and data entry
- 7-segment address and data display
- Programming socket for MK2716/2758's
- Crystal controlled system clock
- 2K bytes of MK4118 static RAM (up to 4K optional)
- Sockets for up to 4K bytes of MK2716 PROM's
- Flexible memory map strapping options
- Current loop or RS-232 serial loader optional (110-300-1200 baud)
- 3 general purpose timer/counters
- 3 general purpose external interrupts
- Easy to use - requires only two supplies for normal operation (+5, +12)
- Ideal for evaluation of MK3870 family single-chip microcomputers
- Full in-circuit emulation of MK3870 single-chip microcomputer family.

DESCRIPTION

EVAL-70 is a single board computer with on-board keypad, address and data displays, and 2716 PROM programmer. EVAL-70 is designed to be an easy-to-use introduction to the industry standard MK3870 family of single-chip computers. Programs can be written and debugged in RAM using the powerful DDT-70 operating system. The 40 pin AIM cable can be used to perform real-time emulation of the MK3870 family of devices. After debugging, programs can be loaded into MK2716's for final circuit checkout (and emulation).

EVAL-70
Figure 1



USING EVAL-70

The photograph above shows how EVAL-70 is used as a program development tool. Only an external power supply is required for operation of EVAL-70; the built-in keyboard and display offer all the functions needed to design, develop, and debug programs for the MK3870 family of single-chip microcomputers at the machine code level.

COMMAND SUMMARY

DM:	Display memory: allows memory to be displayed and (RAM) updated.
DR:	Display registers: allows the user's register values to be displayed and updated.
DP:	Display ports: allows the contents of ports 0 thru F to be displayed and updated
HX:	Hex calculator: allows hexadecimal arithmetic calculations to be performed (add and subtract)
GO:	causes execution of a user program at a specified address

BK: Breakpoint: allows a breakpoint to be set or reset

ST: Step: causes single-step execution of a user program at a specified address

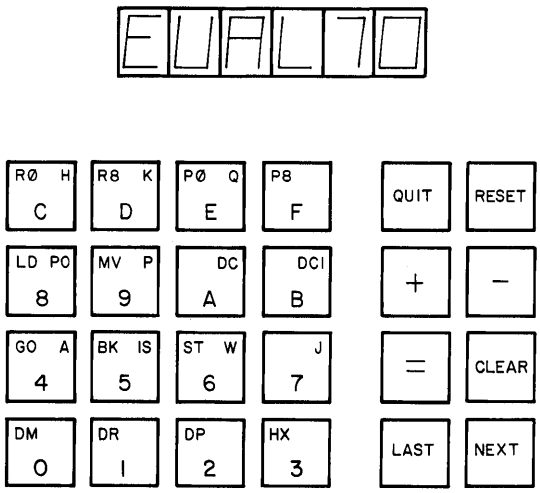
LD: Load: initiates the serial loader (optional)

MV: Move: allows a block of memory to be moved or copied from one space to another

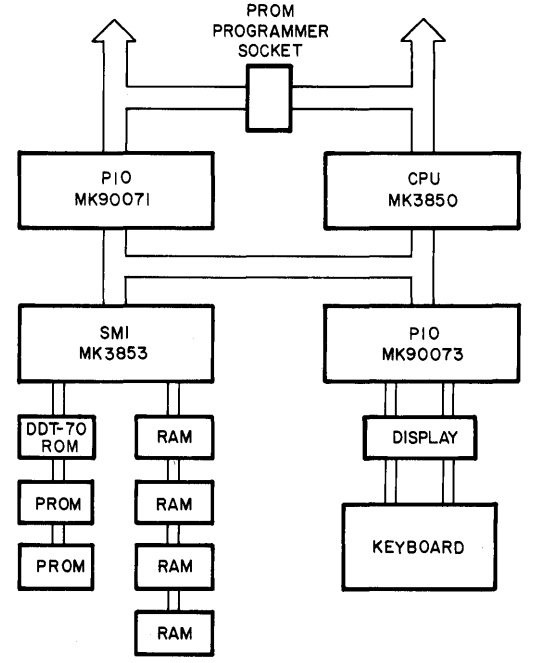
RO, R8: Read PROM: causes the PROM programmer socket to be read into address space 00-7FF or 800-F7F

PO, P8: Program PROM: causes the contents of address space 000-7FF or 800-F7F to be programmed into the PROM programmer socket

EVAL-70 KEYBOARD DRAWING



BLOCK DIAGRAM



BLOCK DIAGRAM

EVAL-70 uses several members of the F8 multichip family. A MK3850 Central Processing Unit (CPU) provides the ALU, registers, system control and two 8-bit ports. A MK90071 Peripheral Input Output chip (PIO) provides two more 8-bit ports plus a flexible timer/interrupt control block. These four ports are connected to the AIM cable connector for in-circuit emulation of the MK3870 family devices, and also to the PROM programmer socket. An additional PIO (MK90073) interfaces the LED display and keyboard. A MK3853 Static Memory Interface chip (SMI) interfaces the operating system ROM, up to two 2K PROMs and up to four 1K RAMs. A switch option allows either the 4K of PROM or the 4K of RAM to appear at address 0000H, with the other 4K appearing at 1000H. The operating system ROM may be up to 8K (currently 2K) starting at 8000H. A switch option allows reset to either 0000H or to the 8000H ROM.

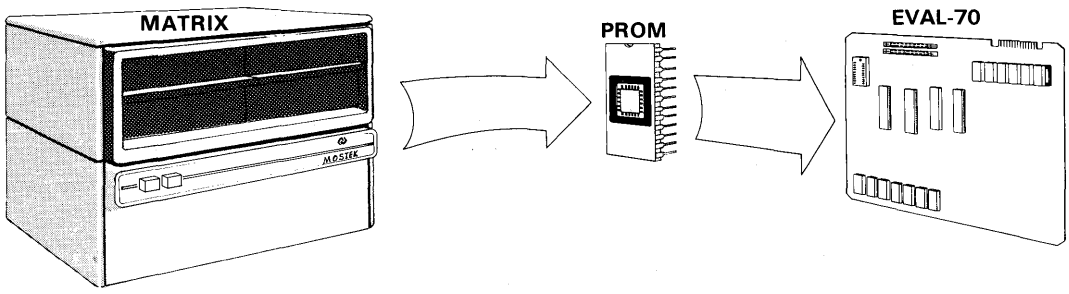
USING EVAL-70 WITH LARGER SYSTEMS

Although the EVAL-70 operating system (DDT-70) was designed to make program machine code entry simple and quick, many users will find it more efficient to assemble their programs on a larger computer and then download to EVAL-70.

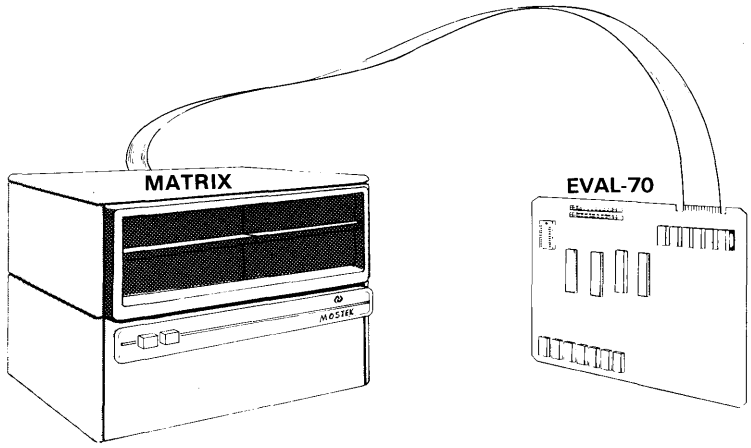
The download to EVAL-70 may be accomplished in either of two ways:

1) A PROM may be programmed on the Development System, and then read into RAM by the EVAL-70 for debugging.
2) A direct connection may be made between a serial port on the Development System and the serial loader port on EVAL-70. An optional serial loader program is provided in the EVAL-70 Operations Manual.

DEVELOPMENT SYSTEM

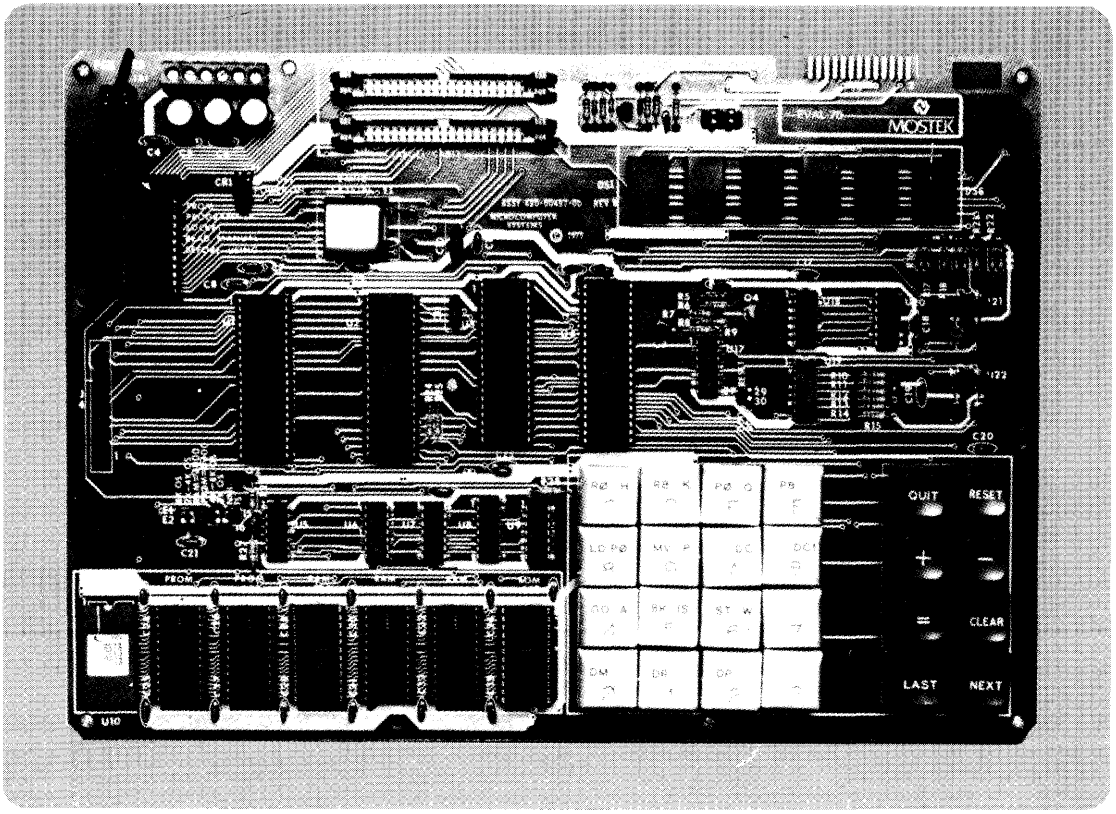


DEVELOPMENT SYSTEM



XI

EVAL-70 BOARD



SPECIFICATIONS

Operating Temperature: 0°C - 50°C

Power Supplies Required: +5VDC ±5% 1.0A max
+12VDC ±5% 0.1A max
+25VDC ±5% 0.1A max

Board Size: 8.5 in. (21.6 cm) x 12 in. (30.5cm) x 2 in. (5cm)

Connectors and Cables: 40 pin in-circuit-emulation cable is provided.

ORDERING INFORMATION

See Development System Products ordering guide.

FLEXIBLE DISK OPERATING SYSTEM - **M/OS-80**

USER FEATURES

- Virtual CP/M™ compatibility gives the user many available programs to choose from.
- Additional utilities and systems commands provide increased capability and functionality to the user.
- Provided on standard media for use with Mostek standard systems and MD Series boards for short system integration time.

INTRODUCTION

M/OS-80 is a CP/M™ compatible, floppy disk operating system for the MD or SD series of microcomputer board systems. It offers a comprehensive solution to a wide variety of system design problems. The software is provided on an 8-inch single-sided, single-density floppy diskette which can be booted on Mostek disk-development systems or user-configured systems (see "Hardware Required" paragraph). M/OS-80 can be altered for different input/output hardware configurations by using the MOSGEN Utility (sold separately).

Several powerful utilities are provided with M/OS-80. These programs give the user a broad base of support and will improve design efficiency. These include:

Editior (Edit)
Designer's Development Tool (Debugger)
Transfer Utility (XFER)
File/Disk Dumps (DSKDUMP)
Print Utility (PRINT)
Print Spooler (SPOOL)
Several System Utilities

Because of M/OS-80's CP/M compatibility, a large number of pre-written programs are available. M/OS-80 is designed to run programs written for other CP/M-compatible operating systems, such as CDOS™, I/OS™, and SDOS™, provided these programs conform to the standards described by Digital Research in versions 1.4 through 2.2. Virtually all compilers and interpreters now sold for use on CP/M (versions 1.4 -2.2) will work. For those Mostek customers who are currently running FLP-80DOS, M/OS-80 provides a direct migration path to CP/M compatibility without any changes to the system hardware.

SYSTEM FEATURES

M/OS-80 is a more sophisticated and powerful floppy disk operating system than any other micro-operating system available. It provides the user with a unique, but invisible, library structure. By assigning one system disk as a Master Library disk, the system can free the user to place all application-related files on another disk while still having the utility of the various system programs on-line.

Unlike other operating systems, M/OS-80 provides the user with comprehensive error messages. In most cases, methods of recovery are displayed and the operator is given several options from which to choose.

HARDWARE REQUIRED

M/OS-80 is currently supplied in three versions. V3 is designed to run on Mostek's MATRIX systems and on systems built with MD Series boards. An MD Series system must contain the following boards:

Item	Hardware Required
Processor	MDX-CPU1 or MDX-CPU2
Console Interface	MDX-EPROM/UART or MDX-SIO
Printer Interface	MDX-PIO or MDX-SIO
Floppy Interface	MDX-FLP1 or MDX FLP2
Memory	(2) MDX-DRAM with 64K of RAM

The V5 system is for use with a Mostek Phantom PROM system configuration. The following boards are required:

Item	Hardware Required
Processor	MDX-CPU3 or MDX-CPU4
Floppy Interface	MDX-FLP2
Memory	(2) MDX-DRAM with 64K of RAM (required only for MDX-CPU4)

The V6 system is for use with a Mostek Phantom hard-disk system. The following boards are required:

XI

CP/M is a Trademark of Digital Research, Inc.
CDOS is a Trademark of Cromemco, Inc.
SDOS is a Trademark of SD Systems, Inc.
I/OS is a Trademark of Infosoft Systems, Inc.

Item	Hardware Required
Processor	MDX-CPU3 or MDX-CPU4
Floppy Interface	MDX-FLP2
Memory	(2) MDX-DRAM with 64K of RAM (required only for MDX-CPU4)
Hard Disk Interface	MDX-SASI1 & MDX-SASI2

With either the V3, V5 or V6, M/OS-80 requires 64K bytes of RAM for operation. Four bootstrap PROMs are supplied with V3, and one bootstrap PROM is supplied with V5 or V6. The system initially must have at least one 8-inch, single-sided, single-density floppy disk drive in order to boot-up M/OS-80. Up-to-four disk drives are supported. The V6 configuration can also boot-up from hard disk.

Table 1 details the peripheral and CPU configurations required for the M/OS-80 versions.

M/OS-80 CONFIGURATION SUMMARY
Table 1

PERIPHERALS	CPU1	CPU2	CPU3	CPU4*
UART Console	V3	V3	N/A	N/A
SIO Console	V3	V3	N/A	N/A
STI Console	N/A	N/A	V5/6	V5/6
SIO Line Printer	V3**	V3**	V5**/6	V5**/6
PIO Line Printer	V3	V3	N/A	N/A
STI Line Printer	N/A	N/A	V5/6	V5/6
FLP1	V3	V3	N/A	N/A
FLP2	V3***	V3***	V5/6	V5/6
SASI	*	*	V6	V6

N/A Not Applicable.
* Future Design.
** SIO line printer configuration is supplied as alternate on systems disk.
*** Single-density only.

NOTE:
1. MOSGEN Utility may be purchased to configure systems for different peripherals and smaller sizes of RAM. See the MOSGEN Data Sheet for more information.

EDIT - Text Editor

The ASCII EDITor file provided with M/OS-80 provides a text editor for users who do not have access to a screen-editor. The editor allows creation and modification of the text files by several easy-to-use commands. EDIT features include:

Find a text string
Change a text string
Find a line
Insert new text
Delete a line(s) or character(s)
Put a block of text into another file
Get a block of text from another file
View text on the console screen
Print text on the line printer
Create a set of commands which can be executed as a macro

XFER — Transfer Utility

The XFER program is a general-file transfer utility. It allows for the moving of files from disks or devices to other (or the same) disks or devices. The XFER features include:

Transfer an ASCII file
Compare two files without moving
Filter out illegal ASCII characters
Conditionally transfer a file (user prompted)
Transfer a Read-Only file
Expand tabs
Verify files after moving
Print HEX address of comparison failure
Transfer only old files
Transfer only new files

DSKDUMP - Disk Dump

The DSKDUMP program allows reading or modifying of a file, the disk data area, or the disk directory. Each block requested is read into a 128-byte buffer, then displayed. The blocks are numbered sequentially. Any block can be selected, displayed, modified, and written back to the disk.

PRINT - Print Utility

The PRINT utility formats ASCII files to the CRT or printer with automatic headings, tabbing and pagination. User-specified options include page width and length, page headings, date printed of the top of each page, and page formatting.

SPOOL - Print Spooler

The SPOOL file system feature is used to output a file from the printer to a system list device while the system continues with other functions. Any ASCII file may be spool-printed, and direct printer activity is prevented while a spool-print is active.

Other System Utilities

M/OS-80 provides several other system utilities to permit a user the highest degree of flexibility in the manipulation of the files and programs created and used with the system. Some of these utilities include: programs to format disks, change disk labels, examine directories, and to diagnose disk problems. A PROM programming utility is also included that interfaces with Mostek's PPG 8/16.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NO.
M/OS-80 V3	One diskette containing all M/OS-80 programs in binary, four bootstrap PROMs, and one Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreeement (enclosed) with purchase order.	MK71010C-81
M/OS-80 V5	One diskette containing all M/OS-80 programs in binary, one bootstrap PROM, and one Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreement (enclosed) with purchase order.	MK71011C-81
M/OS-80 V6	One diskette containing all M/OS-80 programs in binary, one PROM for booting from floppy or hard disk, and an Operations Manual. (See Table 1 for hardware configuration requirements.) Requires the signed Software License Agreement (enclosed) with purchase order.	MK71012C-81
M/OS-80 Operations Manual	Detailed description of the operation and use of the M/OS-80 software package.	4420064
MOSGEN	System generation utilities and device drivers, data sheet	4420268
M80/L80 BASIC-80 BASCOM FORTRAN-80	Microsoft language packages, data sheet	4420309
AIM-Z80	In-circuit-emulation for Z80, data sheet	4420245

MICROSOFT M80/L80 - MK71002
MICROSOFT BASIC-80 - MK71003
MICROSOFT BASCOM - MK71004
MICROSOFT FORTRAN-80 - MK71005

FEATURES

- M/OS-80 development aids for Z80 microcomputer
- CP/M™ compatible
- Macro assembler
- Relocating linking loader
- BASIC interpreter and compiler
- FORTRAN compiler
- Common relocatable object format-link modules in different languages

INTRODUCTION

A series of Microsoft program development tools are now available from Mostek. They offer a comprehensive solution to a wide variety of system and application design problems. The software is provided on 8-inch single-sided single-density floppy diskettes and operates under M/OS-80.

M80/L80

M80 is a relocatable macro assembler for Z80 microcomputer systems, incorporating almost all "big computer" assembler features without sacrificing speed or memory space. The M80/L80 package is comprised of the M80 assembler, L80 linking loader, and a cross reference utility.

BASIC-80

BASIC-80 is the most extensive implementation of BASIC available for the Z80 microprocessor. In three years of use, it has become the world standard for microcomputer BASICs, meeting the requirements for the ANSI subset standard for BASIC, and supporting many unique features rarely found in other BASICs.

BASCOM

Microsoft's BASIC compiler (BASCOM) is a powerful new tool for programming BASIC applications or microcomputer system software. The single-pass compiler produces extremely efficient, optimized machine code that is in standard Microsoft relocatable binary format. Execution speed is typically 3-10 times faster than interpreter BASICs. The M80/L80 assembler/linker package is included with BASCOM.

FORTRAN-80

Microsoft's FORTRAN-80 package provides new capabilities for users of Z80 microcomputer systems. FORTRAN-80 is comparable to FORTRAN compilers on large mainframes and minicomputers. All of ANSI standard FORTRAN X3.9-1966 is included except the COMPLEX data type. Therefore, users may take advantage of the many application programs already written in FORTRAN. The M80/L80 assembler/linker package is included with FORTRAN-80.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
M80/L80	Relocating macro assembler/linker on diskette, with operations manual	MK71002C-80
BASIC-80	BASIC interpreter on diskette, with operations manual	MK71003C-80
BASCOM	BASIC compiler on diskette with operations manual (includes M80/L80)	MK71004C-80
FORTRAN-80	FORTRAN compiler on diskette, with operations manual (includes M80/L80)	MK71005C-80
M/OS-80	CP/M™ compatible disk operating system data sheet	4420271

ASM-68000 STRUCTURED MACRO CROSS ASSEMBLER LNK-68000 RELOCATING LINKAGE EDITOR FOR DEC™ PDP-11™, VAX™, OR VME-MATRIX 68K

BENEFITS

ASM-68000 is one of the most powerful tools available for assembly language programming of the MK68000 microprocessor.

The assembly language is standard and virtually compatible with the Motorola definition.

The package is easy to install on any DEC™ PDP-11™, VAX™, or VME-Matrix 68K™ computer system.

Coupled with RADIUS™ and AIM-68000™ for debugging/in-circuit-emulation, the ASM-68000 package offers the user complete software development capability.

FEATURES

- ☐ Absolute or relocatable code generation
- ☐ Uses Motorola standard asembly language mnemonics and addressing modes and directives for macros and conditional assembly
- ☐ Provides enhanced macro and conditional assembly capability
- ☐ Provides structured control statements for efficient programming:

IF-THEN-ELSE	REPEAT-UNTIL
FOR-ENDF	WHILE-ENDW
LOOP-ENDL	EXIT

- ☐ Provides for complex expression evaluation
- ☐ Produces a complete assembly listing including symbol table and cross reference listing
- ☐ Provides a listing formatting option which will automatically align source statement fields and indent structured statements
- ☐ Package includes the Relocating Linkage Editor

GENERAL DESCRIPTION

Mostek's ASM-68000 Structured Macro Cross Assembler is used to translate source statements written in the MK68000 assembly language into relocatable object code (68000 machine language). The assembler assigns storage locations to instructions and data and performs auxiliary assembler actions designated by the user. The LNK-68000 Relocating Linkage Editor, supplied with the package, combines relocatable object code modules into an absolute load module ready to be debugged. Debugging can be completed using Mostek's RADIUS Remote Development Station and AIM-68000 in-circuit-emulator. The package is designed to be run on a host minicomputer such as the DEC PDP-11 family, the DEC VAX (running in compatiblity mode) or the VME-Matrix 68K microcomputer system. The ASM-68000/LNK-68000 package is supplied on magnetic tape or floppy diskette.

ASM-68000

The ASM-68000 provides the programmer with the means to translate standard MK68000 assembly language source statements into relocatable object code for subsequent input to the LNK-68000 Linkage Editor. The assembler generates a complete printed listing containing the source language input, assembled object code, and additional information, such as error messages, which are useful to the programmer. In addition, a symbol table and cross reference table can be requested to provide additional information.

Assembly is a five-phase process: the macro phase, structured phase, symbol definition phase, code generation phase, and cross reference listing phase. The macro phase reads in the user-specified input file and processes the macro, conditional, and include directives (if any). The structured phase translates the user-specified control structures into their corresponding executable instruction sequences. The symbol definition phase creates a symbol table, associating user-defined labels with values and addresses. In the code generation phase, the translation from source language to machine language takes place, using the symbol table. As each source line is processed in turn, the assembler generates appropriate object code and the assembly listing. The cross reference phase outputs the symbol table to the listing file. If the cross reference option is requested, the cross references are written out with the symbol table.

All standard mnemonics are accepted for instructions and operands, assembler directives, symbolic names, operators and expressions, macros, and conditional assembly

directives. All of the Motorola defined syntax is allowed. In addition, the assembler provides enhanced macro and conditional facilities, and a set of powerful structured statements.

The assembler produces a relocatable object module in Mostek relocatable format which contains information to allow LNK-68000 to combine modules and assign memory addresses. This offers many advantages to the user: reassembly is not required when the locations of subroutines are changed; the object module is substantially smaller than the source program; relocation is faster than reassembly; and relocation is handled automatically by the Linkage Editor.

The ASM-68000 completely checks the syntax of the user program and generates messages in the listing when errors are found. The messages are explicit, and they detail the source of the error. The user guide supplied with the assembler describes how to correct the error.

OPTIONS

The Assembler allows the following options to be selected by the user:

[NO]OBJECT - Selects or deselects the object output
[NO]LIST - Selects or deselects the listing output
[NO]MACRO - Selects or deselects the listing of macro expansions
[NO]CROSS REFERENCE - Selects or deselects the cross reference/listing
[NO]STRUCTURE - Selects or deselects listing of the code generated by structured control statements
[NO]FORMAT - Selects or deselects formatting of the source listing
[NO]MOTOROLA - Selects Mostek - or Motorola - format input souce

LANGUAGE

All standard MK68000 assembly language mnemonics and addressing modes are allowed. Symbols may be any number of characters, the first eight of which are significant. The first character of a symbol may be upper or lower case letters or a period. Additional characters may be upper or lower case letters, numbers, dollar sign, period, or underscore.

Numbers may be specified as octal (preceded with @), binary (preceded with %), decimal, or hexadecimal (preceded with $). ASCII strings are included in apostrophes. Expression operators include arithmetic (+ - * /), shift (<< >>), and logical (& for AND, ! for OR).

DIRECTIVES

Assembler directives for controlling operation of the assembler include the following:

Program assembly control:

ORG	- Absolute origin
SECTION	- Relocatable program section
OFFSET	- Defines offsets
END	- Program end
EQU	- Assigns permanent value
SET	- Assigns temporary value
REG	- Defines register list
DC	- Defines constants
DS	- Defines storage
DCB	- Defines constant block

Listing output control:

PAGE	- Ejects listing page
[NO]LIST	- Enables or disables the listing
[NO]FORMAT	- Enables or disables formatting of listing
SPC n	- Skips n lines
LLEN n	- Sets line length on listing
TTL string	- Specifies title for listing
OPT	- Specifies assembler options
FAIL	- Generates error condition

Linkage Editor control:

IDNT	- Generates identification record for LNK-68000
XDEF	- External symbol definition
XREF	- External symbol reference

Macro and conditional assembly directives:

MACRO	- Macro definition
ENDM	- End of macro definition
MEXIT	- Terminates macro expansion
IFC	- Conditional assembly
ENDC	- End of conditional assembly
INCLUDE	- Inserts code from another source file

Macro functions:

/ARG(n)	- Returns string of the nth macro argument
/NARG	- Returns number of parameters in a macro call
/NEXP	- Expands to decimal number representing the expansion number of the macro
/QUAL	- Expands to the qualifier name of the macro call

STRUCTURED CONTROL STATEMENTS

The ASM-68000 accepts structured control statements which provide for higher-level constructs. These statements make a program more readable and improve programming efficiency without compromising the desirable

aspects of programming in assembly language. Several formats of the structured statements are available and are described below:

IF-THEN-ENDI	- If, then, end if structure
IF-THEN-ELSE-ENDI	- If, then, else, end if structure
IF-THEN-ELSEIF-ELSE-ENDI	- If, then else if, else, end if structure
FOR-BY-DO-ENDF	- FOR structure
FOR-DOWNTO-BY-DO-ENDF	- FOR DOWNTO structure
LOOP-ENDL	- Looping structure
EXIT	- Exit a FOR, LOOP, REPEAT, or WHILE loop
REPEAT-UNTIL	- REPEAT structure
WHILE-DO-ENDW	- WHILE structure

Expressions used in the above statements allow testing of condition codes in the Condition Code Register of the 68000, comparing of simple operands such as used in a compare instruction, and checking of compound expressions which make use of logical AND and OR operations. The comparison operators include:

minus	carry set	overflow set	equal
less than	less than or =	lower	lower or same
always true	plus	carry clear	overflow clear
not equal	greater than	greater than	higher
higher or same	never true	or equal	

LNK-68000

The LNK-68000 Relocating Linkage Editor accepts object modules generated by ASM-68000 and combines them into an absolute load module ready for subsequent debugging. The linker can be directed to generate the absolute load module in either Mostek HEX format or Motorola S-record format, which are not currently compatible with the UNIX operating system.

The user can specify up to four "segments" of memory. For example, ROM code can be contained in a segment separate from RAM data. Up to 16 relocatable sections, plus absolute and named common sections (limited only by available memory) may be allocated among the segments. Comprehensive listing output options are provided, including a load map, externally defined symbols, undefined symbols, multiply defined symbols, segment lengths, and error counts. A library feature enables the user to load only the modules needed from library files. Extensive control of LNK-68000 is provided interactively at link time, including section order, address assignment, resolution of undefined references, and generation of listings.

OPTIONS

The LNK-68000 provides a number of user selection options:

- A - Accepts user commands from the command input device
- B - Forces each relocatable section to start on a page boundary
- H - Lists header information in each object module to the listing file
- I - Lists the command line and all user commands to the listing file
- M - Lists the load map
- S - Allocates segments which do not have a user-specified starting address sequentially
- U - Lists any unresolved references at the end of pass 1 on the console
- X - Lists the external symbol definitions to the listing file

The LNK-68000 generates syntax error messages, fatal messages, and warning messages for the user. These messages detail the source of the error. The user manual supplied with the Linkage Editor describes how to correct the error.

USER COMMANDS

Any sequence of commands may be placed in a separate user command file and executed by the Linkage Editor upon request. The following user commands are provided:

INPUT	- Extends (or replaces) the input file name capability of the command line
ABORT	- Causes an immediate, orderly halt to all processing
END	- Signals the end of the user commands
DEFINE	- Assigns an absolute value to a symbol specified in XREF directive in the program
ENTRY	- Indicates the beginning execution address of the load module being produced
SEGMENT	- Defines a memory management unit segment for the load module
START	- Defines the starting address at which a particular section(s) will be stored
LIST	- Directs all listings to the listing device
LISTM	- Produces an immediate listing of the current load map
LISTU	- Produces an immediate listing of all currently unresolved external references
LISTX	- Produces an immediate listing of the current external symbol definitions

OPERATING ENVIRONMENT

The ASM-68000 package is supplied in two forms: 1) the DOS-11 formatted, 9-track, 800BPI magnetic tape in compiled object form, ready to link and run on DEC PDP-11

computers under RSX-11M or on DEC VAX computers under VMS in compatibility mode and 2): one double-sided, double density 5¼-inch floppy diskette in executable object format, ready to install on the VME-Matrix 68K system under UniPlus+™ Operating System (UNIX™ System III). Command files for automated installation are provided. Complete instructions are included with the package.

Debugging can be completed by using Mostek's RADIUS Remote Development Station and the AIM-68000 in-circuit-emulator. See the appropriate data sheet for more information.

UniPlus+ is a trademark of Unisoft System Incorporated.
UNIX is a trademark of Bell Laboratories and signifies software derived from UNIX System III under license from AT&T.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
ASM-68000	MK68000 Structured Macro Coss Assembler, with manuals, includes LNK-68000, for RSX11M or VAX in compatibility mode.	MK71020C-33
RADIUS	RADIUS Remote Development Station Data Sheet	4420194
AIM-68000	MK68000 Application Interface Module Data Sheet	4420316
ASM/LNK 68000	MK68000 Structured Macro Cross Assembler, with manuals. Includes the LNK-68000, for VME-Matrix 68K/UniPlus+.	MK71020C-56
ASM-68000	Manual only	4420297
LNK-68000	Manual only	4420299
VME-Matrix 68K	VME based developmental system. Uses the UniPlus+ version of UNIX. It comes equipped with a 36 MB Winchester Drive, 2 1-MB 5¼-inch floppy disk, and a 640K bytes of memory.	MK75102

ASM-68200 STRUCTURED MACRO CROSS ASSEMBLER LNK-68200 RELOCATING LINKAGE EDITOR

BENEFITS

ASM-68200 is a powerful state-of-the-art tool used in the assembly language programming of the MK68200 microcomputer.

The assembly language contains macro statements and structured control statements which are similar to those found in higher level languages. These features can improve program readability and programming efficiency.

The package is easy to install and runs on any DEC™ PDP-11™ under RSX-11M™, VAX™ under VMS™ in compatibility mode, or VME-MATRIX 68K™ system under the UniPlus+™ operating system which is a UNIX™ system III port.

ASM-68200 is coupled with RADIUS™ and AIM-68200™ for debugging and in-circuit-emulation. The ASM-68200 package offers the user complete software development capability.

FEATURES

- ☐ Generates absolute or relocatable code
- ☐ Assembles the MK68200 standard instruction mnemonics and directives
- ☐ Provides enhanced macro and conditional assembly capability
- ☐ Provides structured control statements for efficient programming:

IF-THEN-ELSE	REPEAT-UNTIL
FOR-ENDF	WHILE-ENDW
LOOP-ENDL	EXIT

- ☐ Provides for complex expression evaluation
- ☐ Produces a complete assembly listing including a symbol cross reference listing
- ☐ Provides a listing formatting option which will automatically align source statement fields and indent structured statements
- ☐ The package includes the Relocating Linkage Editor

DESCRIPTION

Mostek's ASM-68200 Structured Macro Cross Assembler is used to translate source statements, written in the MK68200 assembly language, into relocatable object code (68200 machine language). The assembler assigns storage locations to instructions and data, and it performs auxiliary assembler actions designated by the user. The LNK-68200 Relocating Linkage Editor, supplied with the package, combines relocatable object code modules into an absolute load module, which is ready to be debugged. Debugging can be completed using Mostek's RADIUS Remote Development Station and AIM-68200 in-circuit-emulator. The package runs on a host minicomputer such as the DEC PDP-11 family, the DEC VAX, or microcomputer such as the VME-MATRIX 68K/UniPlus+. The ASM-68200/LNK-68200 package is supplied on magnetic tape or floppy diskette.

ASM-68200

The ASM-68200 provides the programmer with the means to translate standard MK68200 assembly language source statements into relocatable object code for subsequent input to the LNK-68200 Linkage Editor. The assembler generates a complete printed listing containing the source language input, assembled object code, and additional information, such as error messages that are useful to the programmer. In addition, a symbol cross reference table can be requested to provide additional information.

Assembly is a five-phase process that includes a macro phase, a structured phase, a symbol definition phase, a code generation phase, and an optional cross reference listing phase. The macro phase reads in the user-specified input file and processes the macro, conditional, and include any directives. The structured phase translates the user-specified control structures into their corresponding executable instruction sequences. The symbol definition phase creates a symbol table, associating user-defined labels with values and addresses. In the code generation phase, the translation from source language to machine language takes place using the symbol table. As each source line is processed, in turn, the assembler generates the appropriate object code and the assembly listing. The cross reference phase outputs a symbol table with cross references to the listing file.

The assembler produces a relocatable object module in Mostek relocatable format, which contains information to allow LNK-68200 to combine modules and assign memory addresses. This offers advantages to the user. A program may be partitioned into a number of small modules that may be assembled separately and linked together. Individual

*DEC, PDP-11, RSX, VAX, and VMS are trademarks of Digital Equipment Corporation.

program sections may be relocated in memory without reassembly, and general purpose object libraries may be created and searched at link time.

The LNK-68200 generates syntax error messages, fatal messages, and warning messages for the user. These messages detail the source of the error; and the user manual, supplied with the Linkage Editor, describes how to correct the error.

OPTIONS

The Assembler allows the following options to be selected by the user:

[NO]OBJECT	- Selects or deselects the object output.
[NO]LIST	- Selects or deselects the listing output.
[NO]MACRO	- Selects or deselects the listing of macro expansions.
[NO]CROSS REFERENCE	- Selects or deselects the cross reference listing.
[NO]STRUCTURE	- Selects or deselects listing of the code generated by structured control statements.
[NO]FORMAT	- Selects or deselects formatting of the source listing.

LANGUAGE

A program consists of sequences of assembly language source statements. Source statements may include executable instructions, assembler directives, macro statements, structured statements, or comment statements. Each source statement has an overall format that is some combination of the following fields:

1. LABEL
2. OPERATION
3. OPERAND
4. COMMENT

User-defined symbols include macro names and labels, which may be referenced in the operand field. The first character of a user-defined symbol must be a letter, and the remaining characters can be composed of letters, digits, or an underscore. User-defined symbols may be of any length, but only the first eight characters are significant.

Expressions in the operand field may include arithmetic operators (+ - * /), shift operators (<< >>), and logical operators (& for AND, ! for OR). Numbers may be specified as octal (preceded with @), binary (preceded with %), decimal, or hexadecimal (preceded with $). ASCII strings are included in apostrophes.

DIRECTIVES

Assembler directives for controlling operations of the assembler include the following:

Program assembly control:

ORG	- Absolute origin
SECTION	- Relocatable program section
OFFSET	- Defines offsets
END	- Program end
EQU	- Assigns permanent value
SET	- Assigns temporary value
REG	- Defines register list
DC	- Defines constants
DS	- Defines storage
DUP	- Duplicates constant block

Listing output control:

PAGE	- Ejects listing page
[NO]LIST	- Enables or Disables the listing
[NO]FORMAT	- Enables or Disables formatting of listing
SPC n	- Skips n lines
LLEN n	- Sets line length on listing
TTL string	- Specifies title for listing
OPT	- Specifies assembler options
FAIL	- Generates error condition

Linkage Editor control:

IDNT	- Generates identification record for LNK-68200
XDEF	- External symbol definition
XREF	- External symbol reference

Macro and conditional assembly directives:

MACRO	- Macro definition
ENDM	- End of macro definition
MEXIT	- Terminates macro expansion
IFC	- Conditional assembly
ENDC	- End of conditional assembly
INCLUDE	- Inserts code from another source file

Macro functions:

/ARG(n)	- Returns string of the nth macro argument
/NARG	- Returns number of parameters in a macro call
/NEXP	- Expands to decimal number representing the expansion number of the macro
/QUAL	- Expands to the qualifier name of the macro call

STRUCTURED CONTROL STATEMENTS

The ASM-68200 accepts structured control statements that provide for higher-level constructs. These statements make a program more readable and improve programming efficiency without compromising the desirable aspects of programming in assembly language. Several formats of the

structured statements are available and are described below:

IF-THEN-ENDI	- If, then, end if structure
IF-THEN-ELSE-ENDI	- If, then, else, end if structure
IF-THEN-ELSEIF-ELSE-ENDI	- If, then, else if, else, end if structure
FOR-TO-DO-ENDF	- FOR structure
FOR-DOWNTO-DO-ENDF	- FOR DOWNTO structure
LOOP-ENDL	- Looping structure.
REPEAT-UNTIL	- REPEAT structure
WHILE-DO-ENDW	- WHILE structure
EXIT	- Exit a FOR, LOOP, REPEAT, or WHILE loop

Expressions used in the above structured statements allow testing of condition codes in the Status Register of the 68200 and comparison of simple operands, such as those used in the compare instruction. Compound expressions, which make use of logical AND and OR operations, are also supported. The following statements illustrate the use of the REPEAT-UNTIL construct and a compound expression:

```
REPEAT
    MOVE (A0)+, (A1)+
UNTIL A0 <GT> #1000 OR (A0) <EQ> #0
```

LNK-68200

The LNK-68200 Relocating Linkage Editor accepts object modules generated by ASM-68200 and combines them into an absolute load module ready for subsequent debugging. The load module can be generated in either Mostek HEX format or Motorola S-record format.

The user can specify up to four "segments" of memory. For example, ROM code can be contained in a segment separate from RAM data. Up to 16 relocatable sections, plus absolute and named common sections (limited only by available memory), may be allocated among the segments. Comprehensive listing output options are provided including a load map, externally defined symbols, undefined symbols, multiply defined symbols, segment lengths, and error counts. A library feature enables the user to load only the modules needed from library files. Extensive control of LNK-68200 is provided interactively at link time including section order, address assignment, resolution of undefined references, and generation of listings.

OPTIONS

The LNK-68200 provides a number of user selectable options:

- A - Accepts user commands from the command input device.
- B - Forces each relocatable section to start on a page boundary.
- H - Lists header information in each object module to the listing file.
- I - Lists the command line and all user commands to the listing file.
- L - Specifies an object library to be searched if there are any unresolved references.
- M - Lists the load map.
- Q - Selects load module format of S-record or Hex.
- S - Allocates segments that do not have a user-specified starting address sequentially.
- U - Lists any unresolved references at the end of pass 1 on the console.
- X - Lists table of externally defined symbols to the listing file.

The LNK-68200 generates syntax error messages, fatal messages, and warning messages for the user. These messages detail the source of the error; and the user manual, supplied with the Linkage Editor, describes how to correct the error.

USER COMMANDS

Any sequence of commands may be placed in a separate user command file and executed by the Linkage Editor upon request. The following user commands are provided:

INPUT	- Extends (or replaces) the input file name capability of the command line.
ABORT	- Causes an immediate, orderly halt to all processing.
END	- Signals the end of the user commands.
DEFINE	- Assigns an absolute value to a symbol specified in XREF directive in the program.
ENTRY	- Indicates the beginning execution address of the load module being produced.
SEGMENT	- Defines segment attributes and the relocatable section numbers (0-15) to be included in the segment.
START	- Defines the starting address at which a particular section(s) will be stored.
LIST	- Directs all listings to the listing device.
LISTM	- Produces an immediate listing of the current load map.
LISTU	- Produces an immediate listing of all currently unresolved external references.
LISTX	- Produces an immediate listing of the table of externally defined symbols.
LIBRARY	- Specifies an object library to be searched if there are any unresolved references.

OPERATING ENVIRONMENT

The ASM/LNK68200 software package is supplied in 2 forms:

1. DOS-11 formatted, 9 track, 800BPI magnetic tape in compiled object form, ready to link and run on DEC PDP-11 computers under RSX-11M and VAX computers under VMS in compatibility mode;

2. double-density, double-sided 5¼ inch floppy diskette in executable object form, ready to install on VME-MATRIX68K microcomputers under UniPlus+ (UNIX System III).

Each package contains command files for automated installation as well as complete installation instructions and reference manuals.

Debugging can be completed by using Mostek's RADIUS Remote Development Station and the AIM-68200 in-circuit emulator. See the appropriate data sheet for more information.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
ASM-68200	MK68200 Structured Macro Cross Assembler includes LNK-68200 for use under RSX-11M or VAX in compatibility mode. Includes manuals.	MK71030C-33
ASM-68200	MK68200 Structured Macro Cross Assembler includes LNK-68200 for use on VME-MATRIX68K/UniPlus+ microcomputer system. Includes manuals.	MK71030C-56
	ASM-68200 User's Guide. Manual only.	4420357
	LNK-68200 User's Guide. Manual only.	4420397
	MK68200 Principles of Operation. Manual only.	4420399
RADIUS	RADIUS Remote Development Station Data Sheet	4420194
AIM-68200	MK68200 Application Interface Module Data Sheet	4420396

CRASM-70 3870 CROSS-ASSEMBLER

FEATURES

- ☐ Assembles standard 3870 and F8 source
- ☐ Produces absolute load module in F8HEX format
- ☐ Runs under M/OS-80 on any Mostek disk system
- ☐ Produces complete assembly listing to disk or printer
- ☐ Produces symbol reference table

DESCRIPTION

The Mostek 3870 Cross Assembler (CRASM-70) runs under the M/OS-80 operating system, and assembles standard 3870/F8 assembly language. The output is an absolute object file (load module) in F8HEX format. A conversion utility is provided to convert F8HEX files to Mostek Hex for use with the AIM-7X in-circuit-emulator system. The Mostek MATRIX-80/SDS disk development system can be used for stand-alone assembly and debug capability, with the AIM-7X plugged directly into the system. The assembler object module may also be downloaded from a M/OS-80-based system to a Mostek RADIUS development system containing an AIM-7X.

CRASM-70 produces an assembly listing which can be directed to a disk file or directly to the M/OS-80 LST: list device (printer). The listing shows program address, machine code, and line number for each statement, along with each source program statement. Any errors which are found in the source program are indicated in the listing. A symbol reference table is printed at the end of the listing. Up to 500 symbols may be used in the source program.

CRASM-70 is supplied on a standard 8-inch single-sided single-density CP/M-compatible diskette, precompiled, ready to run under M/OS-80.

ORDERING INFORMATION

DESIGNATOR	DESCRIPTION	PART NUMBER
CRASM-70	3870/F8 Cross Assembler, runs under M/OS-80, on 8" SSSD diskette, with manual	MK71007C-80
CRASM-70	Documentation package for above	MK71007D
RADIUS	Remote Development Station data sheet	4420194
AIM-7XE	Application Interface Module data sheet	4420246

RADIUS - Remote Development Station

RADIUS is a hardware/software development station that connects to a host computer. When you order a RADIUS, you must specify the operating voltage characteristics. The host software must be ordered separately (as described in the next section).

DESCRIPTION	ORDER
RADIUS for 60 Hz, 115 VAC Operation	MK78213
RADIUS for 50 Hz, 230 VAC Operation	MK78214

RADIUS HOST SOFTWARE

RADIUS host software is provided on a variety of media depending on host environment. When you order please specify one of the following.

DESCRIPTION	ORDER
M/OS Version - implemented for M/OS-80 and CP/M supplied on single-sided, single-density, 8-inch floppy diskette.	MK78224-11
RSX Version - implemented for RSX-11M V3.2 supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI. Host must have a FORTRAN IV (ANSI-66) compiler.	MK78224-33
VMS Version - implemeted for VMS V2.3 supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI. Host must have a FORTRAN IV (ANSI-66) compiler.	MK78224-34
Rehostable Version - supplied in source form. Host must have a FORTRAN IV (ANSI-66) compiler. Supplied on ASCII 9-track magnetic tape, 800 BPI, blocked in 80-character records.	MK78224-45
MATRIX UNIX version-implemented for UNIX on the MATRIX 68K. Supplied on a double sided, double density 5 ¼ inch floppy diskette.	MK78224-56

MATRIX is a stand-alone, floppy disk based development system. It is supplied with M/OS V3.01, the M80 assembler, and the L80 linker. When you order a MATRIX, you must specify the operating voltage characteristics:

DESCRIPTION	ORDER
MATRIX for 60 Hz, 115 VAC operation	MK78188
MATRIX for 50 Hz, 230 VAC operation	MK78189

AIM-7XE (Application Interface Module for 387X)

AIM-7XE is the in-circuit-emulator for the 387X family. It will function in both RADIUS and MATRIX. When AIM-7XE is ordered, a personality module must also be ordered. This personality module provides emulation for the 3870 or 3873 family.

In addition, the AIM-7X software must be ordered separately (as described in next section).

DESCRIPTION	ORDER
AIM-7XE - control board and history board for 387X families.	MK79094
APM-70 - personality module for 3870 family	MK79093
APM-73 - personality module for 3873 family	MK79092

AIM-7X (Software for AIM 7XE)

The following software configurations are available for use with AIM 7XE. Please specify one of the following when ordering.

DESCRIPTION	ORDER
Unix Version - configured for use with the MATRIX 68K. Supplied on a double sided double density 5 ¼ inch floppy diskette.	MK78225-50
M/OS-80 Version - configured for use with M/OS-80 and CP/M host and RADIUS. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78225-10
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI.	MK78225-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78225-40
M/OS-80 Version - configured for use with MATRIX. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78225-11

AIM-Z80AE/AIM-Z80BE (Application Interface Modules for Z80)

AIM-Z80AE and AIM-Z80BE are the in-circuit-emulators for the Z80. They will function in both RADIUS and MATRIX. When either of the two is ordered, the AIM-Z80 software must be ordered separately (as described in the next section).

DESCRIPTION	ORDER
AIM-Z80AE - In-circuit-emulator for 2.5 and 4 MHz Z80. Provides 32K emulation RAM	MK78181-4
AIM-Z80BE - In-circuit-emulator for 2.5, 4, and 6 MHz Z80. Provides 16K emulation RAM	MK78204

AIM-Z80 (Software for AIM-Z80AE/AIM-Z80BE)

The following software configurations are available for use with AIM-Z80AE or AIM-Z80BE. Please specify one of the following when ordering.

DESCRIPTION	ORDER
Unix Version - configured for use with the MATRIX 68K. Supplied on a double sided double density 5 ¼ inch floppy diskette.	MK78226-50
M/OS-80 Version - configured for use with M/OS-80 and CP/M host and RADIUS. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78226-10
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track Magnetic tape, 800 BPI.	MK78226-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78226-40
M/OS-80 Version - configured for use with MATRIX. Supplied on single-sided, single-density, 8-inch floppy diskette.	MK78226-11

AIM-68000 (Application Interface Module for 68000)

AIM-68000 is the in-circuit-emulator for the 68000. It will function in both RADIUS and MATRIX. When AIM-68000 is ordered, the AIM-68000 software must be ordered separately (as described in the next section).

DESCRIPTION	ORDER
AIM-68000 - In-ciruit-emulator for up to 10 MHz 68000. Includes two (2) control boards and a buffer box/cable assembly.	MK78228

AIM-68000 (Software for AIM-68000)

The following software configurations are available for use with AIM-68000. Please specify one of the following when ordering.

DESCRIPTION	ORDER
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI.	MK78232-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78232-40
M/OS 80 Resident Version-configured for use with the MATRIX Development System.	MK78232-11
M/OS 80 Hosted Version-configured for down loading from MATRIX to RADIUS.	MK78232-10
UNIX - Version - configured for use with the MATRIX 68K.	MK78232-50

EVAL-70

EVAL-70 is a 3870 family evaluation system. It includes an in-circuit-emulation cable.

DESCRIPTION	ORDER
EVAL-70	MK79086

ASM/LNK 68000

ASM/LNK is the assembler and linker for the 68000. The following software configurations are available on ASM/LNK 68000.

DESCRIPTION	ORDER
68000 structured Macro Cross Assembler and linker for use on DEC PDP-11 systems running RSX-11M or DEC VAX Systems running in compatibility mode under VMS.	MK71020C-33
68000 structured Macro Cross Assembler and linker for use on MATRIX-68K with UNIX operating system.	MK71020C-56
68000 Cross Assembler and linker for use on 8080/Z80 Systems using the M/OS-80 or CP/M Operating System for use with Mostek development system equipment.	MK78238C-11

AIM-68200 (Application Interface Module For 68200)

AIM-68200-In-circuit-emulator for the 68200. It will function in both RADIUS and MATRIX. When AIM-68200 is ordered, the AIM-68200 software must be ordered separtely (as described in the next section).

DESCRIPTION	ORDER
AIM-68200-In-Circuit-emulator for up to a 6 MHz 68200. Includes two (2) control boards and a buffer box/cable assembly.	MK78235

AIM-68200 (Software For AIM-68200)

The following software configurations are available for use with AIM-68200. Please specify one of the following when ordering.

DESCRIPTION	ORDER
RSX and VMS Version - configured for use with RSX-11M V3.2 and VMS V2.3 host and RADIUS. Supplied on DEC DOS-11 format 9-track magnetic tape, 800 BPI.	MK78234-30
ASCII Version - configured for use with general host and RADIUS. Supplied on ASCII 9-track magnetic tape, 800 BPI.	MK78234-40
M/OS 80 Resident Version - configured for use with the MATRIX Development System.	MK78234-11
M/OS 80 Hosted Version - configured for down loading from MATRIX to RADIUS.	MK78234-10
UNIX Version - configured for use with the MATRIX 68K.	MK78234-50

EPP-1 (EPROM Programmer)

EPP-1 is a programmer for use with RADIUS.

DESCRIPTION	ORDER
EPP-1 EPROM programmer	MK78229-0

EPP-1 (SOFTWARE FOR EPP-1)

DESCRIPTION	ORDER
PROM programmer utility for EPP-1 (Data I/O)	MK78236

ASM/LNK 68200

ASM/LNK 68200 is the assembler and linker for the 68200. The following software configurations are available on ASM/LNK 68200.

DESCRIPTION	ORDER
68200 structured Macro Cross Assembler and Linker for use on DEC PDP-11 systems running RSX-11M or DEC VAX system running in compatibility mode under VMS.	MK71030C-33
68200 Structured Macro Cross Assembler for use on MATRIX 68K with UNIX operating system.	MK71030C-56
68200 Cross Assembler and Linker for use on 8080/Z80 systems using the M/OS-80 or CP/M operating system.	MK71039C-11

CRASM-70

CRASM-70 is the cross assembler that runs under MO/S-80 operating svstem, and assembles standard 3870/F8 assembly language.

DESCRIPTION	ORDER
Cross Assembler for 3870/F8 runs on MATRIX.	MK71007C-80

1984/1985 MICROELECTRONIC DATA BOOK

INTEGRATED TONE DIALER MK5087(N/P/J)

FEATURES

- Pin-for-pin compatible with MK5085 with improved performance
- Direct telephone-line operation with no external power supply
- Auxiliary switching functions on chip
- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- On-chip regulation of dual-and single-tone amplitudes
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Multiple key entry pin-selectable to either single tone or no tone

DESCRIPTION

The MK5087 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II* family of integrated tone dialers, the MK5087 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

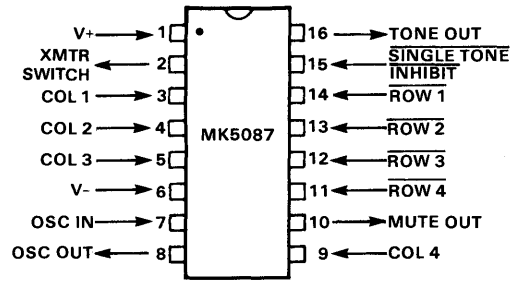
The MK5087 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, auxiliary switching functions, single-contact keyboard inputs, and Single Tone Inhibit option.

Keyboard entries to the TONE II* family of integrated tone dialers cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sine wave and requires little or no filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low and high-group signals. Frequency stability of this type of tone generator is such that no frequency adjustment is needed to meet standard DTMF specifications.

* Trademark of Mostek Corporation

PIN CONNECTIONS

Figure 1



Pin connections are shown in Figure 1 and a block diagram is shown in Figure 2.

XII

FUNCTIONAL DESCRIPTION

V+, Pin 1

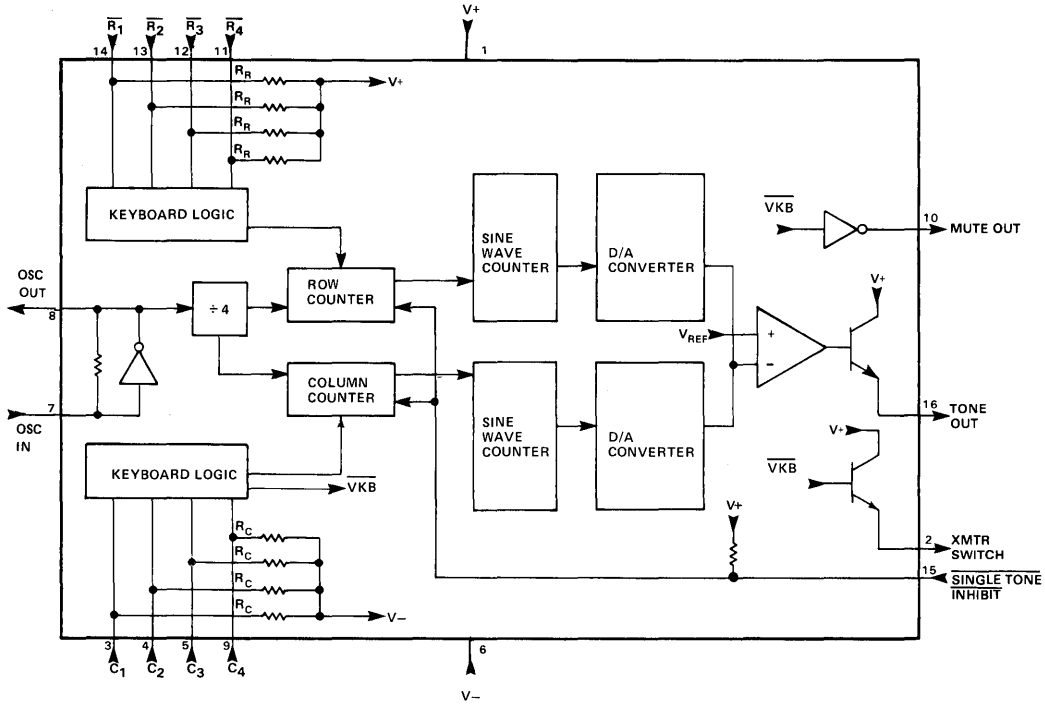
Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 3.5 and 10.0 volts, measured relative to V- (Pin 6).

XMTR SWITCH, Pin 2

Pin 2 is connected to the emitter of an on-chip bipolar transistor whose collector is connected to V+. With no keyboard input this transistor is turned on and pulls Pin 2 up to within V_{BE} of the V+ supply. When a keyboard entry is sensed, this output goes open circuit (high impedance). The XMTR Switch output switches regardless of the state of the Single Tone Inhibit input.

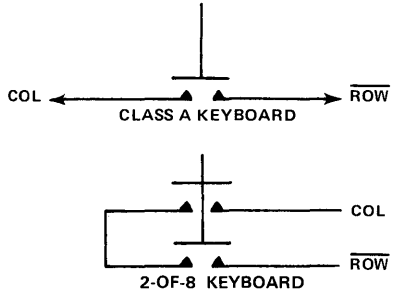
MK5087 BLOCK DIAGRAM

Figure 2



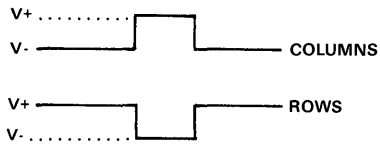
KEYBOARD CONFIGURATIONS

Figure 3



ELECTRONIC INPUT

Figure 4



$\overline{ROW}$-COL INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5087 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 3 shows how to connect to the two keyboard types and Figure 4 shows waveforms for electronic input. The inputs are static, i.e. there is no noise generation as occurs with scanned or dynamic inputs.

The internal structure of the MK5087 inputs is shown in Figure 5. R_R and R_C pull in opposite directions and hold their associated input sensing circuit turned off. When one or more row or column inputs are tied together, however, the input sensing circuits sense the "½ Level" and deliver a logic signal to the internal circuitry of the MK5087 and cause the proper tone or tones to be generated.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when one or more buttons in the same row or column is pushed. Activation of diagonal buttons will result in no tones being generated.

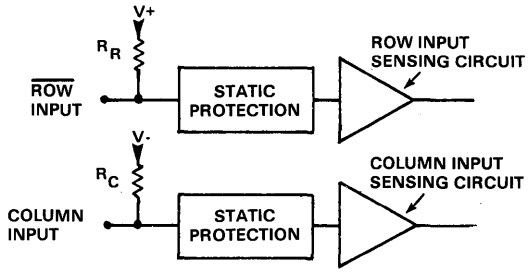
When the inputs to the MK5087 are electronically activated, per Figure 4, input to a single row and column will result in that dual-tone digit's being generated. Input to a

single column will result in that column tone being generated. Input to multiple columns will result in no tone being generated.

Activation of a single row is not sensed by the internal circuitry of the MK5087. If a single-row tone is desired, two columns must be activated along with the desired row.

ROW AND COLUMN INPUTS

Figure 5



V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5087 contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1. The oscillator is disabled whenever a keyboard input is not sensed.

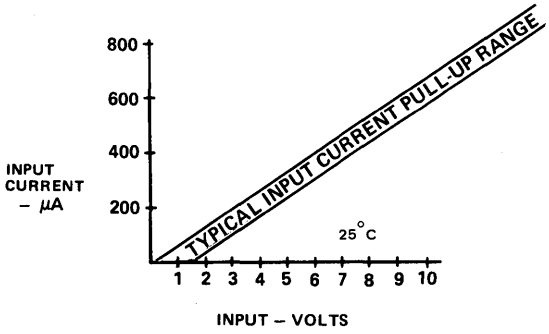
Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

MUTE OUT, Pin 10

The Mute output is a conventional CMOS gate that pulls to V- with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The Mute output switches regardless of the state of the $\overline{\text{Single Tone Inhibit}}$ input.

INPUT CURRENT VS. INPUT VOLTAGE

Graph 1



OUTPUT FREQUENCY DEVIATION

Table 1

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
ROW	f_1	697	701.3	+0.62	
	f_2	770	771.4	+0.19	LOW GROUP
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
COL	f_5	1209	1215.9	+0.57	
	f_6	1336	1331.7	-0.32	HIGH GROUP
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull-up to the V+ supply and, when left floating or tied to V+, single or dual tones may be generated as described in the paragraph under row-column inputs. When forced to the V- supply, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

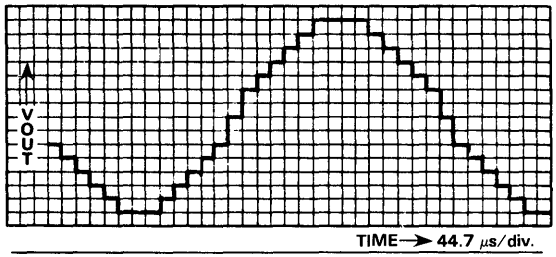
TONE OUT, Pin 16

The output pin is connected internally in the MK5087 to the emitter of an npn transistor whose collector is tied to V+. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together.

The level of a dual-tone output is the sum of the levels of a single-row and a single-column output. This level is controlled by an on-chip reference which is not sensitive to variations in the supply voltage.

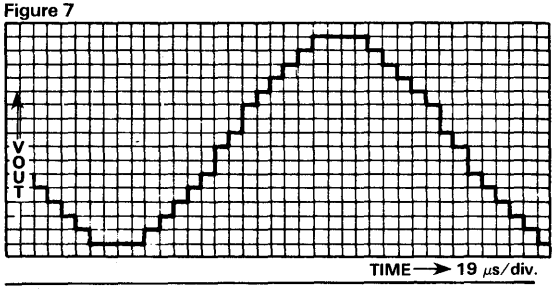
ROW 2 TONE OUTPUT

Figure 6



COLUMN 4 TONE OUTPUT

Figure 7



OUTPUT WAVEFORM

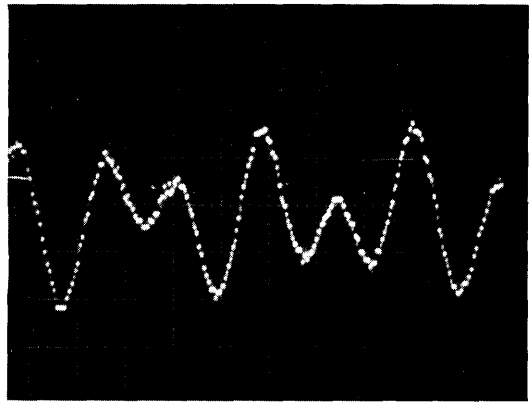
The row and column output waveforms are shown in Figures 6 and 7. These waveforms are digitally-synthesized using on-chip D-to-A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 9% or less.

The on-chip operational amplifier of the MK5087 mixes the row and column tones to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically all harmonic and intermodulation distortion components will be -30 dB when referenced to the strongest fundamental (column tone).

A commonly quoted method of dual-tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals. For the MK5087 dual-tone waveform, THD is -20 dB maximum.

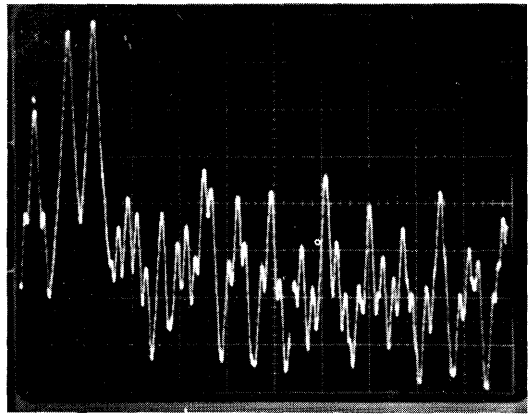
TYPICAL DUAL-TONE WAVEFORM (ROW 1, COL. 1)

Figure 8



SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 8 (Vert-10 dB/div., Horizontal-1 kHz/div.)

Figure 9



A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK5087 dual-tone spectrum will show all individual harmonic and IMD components are typically at least -30 dB with respect to the column tone.

Figures 8 and 9 show a typical dual-tone waveform and its spectral analysis.

TYPICAL APPLICATION

Figure 11 shows an application of the MK5087 in a standard telephone set that uses the standard 2500-type network. The tone levels and loop compensation that result from this application meet the requirements of the U.S. telephone systems.

ABSOLUTE MAXIMUM RATINGS*

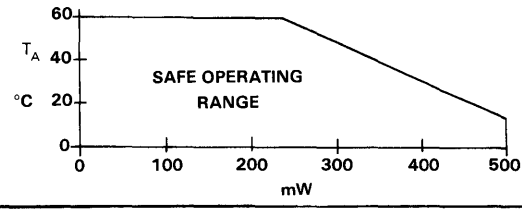
DC Supply Voltage V+ ..... 10.5 Volts
Any Input Relative to V+ ..... +0.30 Volts
Any Input Relative to V- ..... -0.30 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE

Figure 10



ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(-30°C ≤ T_A ≤ 60°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	3.5		10.0	V	1
V_{IL}	Input Voltage Low - "0"	V-		30% of V+	V	1, 11
V_{IH}	Input Voltage High - "1"	70% of V+		V+	V	1, 12
$R_{IP\overline{STI}}$	Input Pull-up Resistance, $\overline{STI}$	20		100	kΩ	3

AC CHARACTERISTICS

(-30°C ≤ T_A ≤ 60°C; 3.0 V ≤ V+ ≤ 10.0 V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I_{SSB}	Supply Current-Standby (Pin 6, V+ = 3.5 V) (Pin 6, V+ = 10.0 V)		 0.25 0.50	 100 200	 μA μA	 2,7 2,7
I_{SO}	Supply Current-Operating (V+ = 3.5 V) (V+ = 10.0 V)		 1.0 5.0	 2.0 15.0	 mA mA	 2,6,8,9 2,6,8,9
I_{OHX}	Output Drive, XMTR Switch-No Entry (V+ = 3.5 V, V_{OHX} = 2.5 V) (V+ = 10.0 V, V_{OHX} = 8.0 V)	 -15 -40	 -25 -100		 mA mA	
I_{OLX}	Output Drive, XMTR Switch-Valid Entry (V+ = 10.0 V, Output = 0.0 V)		0.1	10.0	μA	
I_{OHM}	Output Drive, MUTE - Valid Entry (V+ = 3.5 V, V_{OH} = 3.0 V) (V+ = 10.0 V, V_{OH} = 9.5 V)		 0.5 1.0	 2.0 4.0	 mA mA	
I_{OLM}	Output Drive, MUTE - No Entry (V+ = 3.5 V, V_{OL} = 0.5 V) (V+ = 10.0 V, V_{OL} = 0.5 V)		 0.5 1.0	 2.0 4.0	 mA mA	
Input Current Rows and Columns - SEE GRAPH 1						

AC CHARACTERISTICS (Continued)

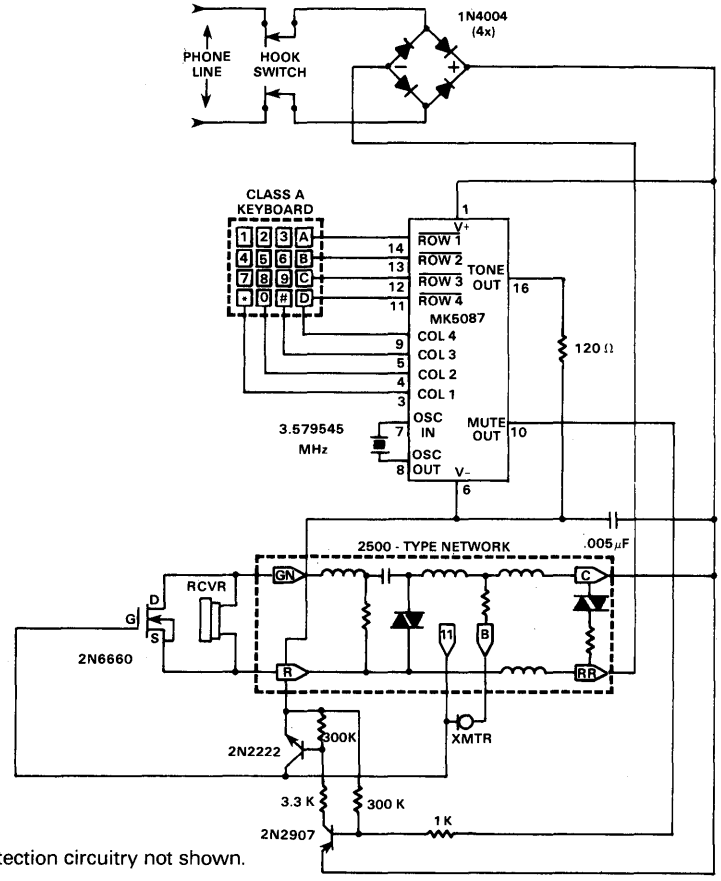
SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{NKD}	Tone Output-No Key Down			-80	dBm	
t_{RISE}	Tone Output Rise Time		3.0	5.0	ms	5,9
V_{OUT}	Tone Output Voltage Row Tone (R_L = 1K, 620 Ω, 330 Ω) Col Tone (R_L = 1K, 620 Ω, 330 Ω)	 317 396	 400 500	 504 630	 mVRMS mVRMS	 1,3,6 1,3,6
PE_{HB}	Pre-Emphasis, High Band	1.0	2.0	3.0	dB	
DIS	Output Distortion			-20	dB	4,10

NOTES:

1. All voltages referenced to V-.
2. All outputs unloaded.
3. T_A = 25°C.
4. Any row plus any column at V+ ≥ 4 volts.
5. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of the final magnitude of either frequency.
6. True RMS Readings
7. Current Out Of Pin 6 No Key Depressed.
8. Current Out Of Pin 6 One Key Depressed.
9. Crystal parameters $R_S \leq 100\ \Omega$, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, C_L = 18 pF.
10. Output Distortion measured in terms of total out-of-band power relative to the sum of Row and Column fundamental power.
11. Column inputs require a voltage low (0) of 10% of V+ (max).
12. $\overline{\text{Row}}$ inputs require a voltage high (1) of 90% of V+ (min).

TYPICAL APPLICATION IN 2500-TYPE TELEPHONE

Figure 11



NOTE: Transient protection circuitry not shown.

INTEGRATED TONE DIALER MK5089(N/P/J)

FEATURES

- Minimum external parts count
- High-accuracy tones
- Digital divider logic, resistive ladder network, and CMOS operational amplifier on single chip
- Uses inexpensive 3.579545 MHz television color-burst crystal
- Multiple key entry pin selectable to either single tone or no tone
- Interfaces easily in electronic or μP dialing applications
- $\overline{\text{Tone Disable}}$ inhibits tone generation without defeating the $\overline{\text{Any Key Down}}$ output

DESCRIPTION

The MK5089 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. A member of the TONE II* family of integrated tone dialers, the MK5089 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies which are mixed to provide tones suitable for Dual-Tone Multi-Frequency (DTMF) telephone dialing.

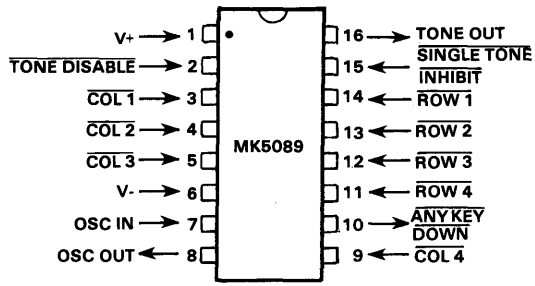
The MK5089 was designed specifically for integrated tone dialer applications that require the following: fixed supply operation, a negative-true keyboard input, $\overline{\text{Tone Disable}}$ input, stable output tone level, and an $\overline{\text{Any Key Down}}$ output that is open circuit when no keyboard buttons are pushed and pulls to the V– supply when a button is pushed.

Keyboard entries to the TONE II* family of integrated tone dialers cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator. D-to-A conversion is accomplished on-chip by a conventional R-2R ladder network. The tone output is a stairstep approximation to a sine wave and requires little filtering for low-distortion applications. The same operational amplifier that accomplishes the current-to-voltage transformation necessary for the D-to-A converter also mixes the low- and high-group signals. Frequency stability of this type of tone generation is such that no frequency adjustment is needed to meet standard DTMF specifications.

*Trademark of Mostek Corporation

PIN CONNECTIONS

Figure 1



Pin connections are shown in Figure 1 and a block diagram is shown in Figure 2.

FUNCTIONAL DESCRIPTION

V+, Pin 1

Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 3.0 and 10.0 volts, measured relative to V– (Pin 6).

$\overline{\text{TONE DISABLE}}$, Pin 2

The $\overline{\text{Tone Disable}}$ input is used to defeat tone generation when the keyboard is used for other functions besides DTMF signaling. It has a pull-up to the V+ supply and, when tied to the V– supply, tones are inhibited. All other chip functions operate normally.

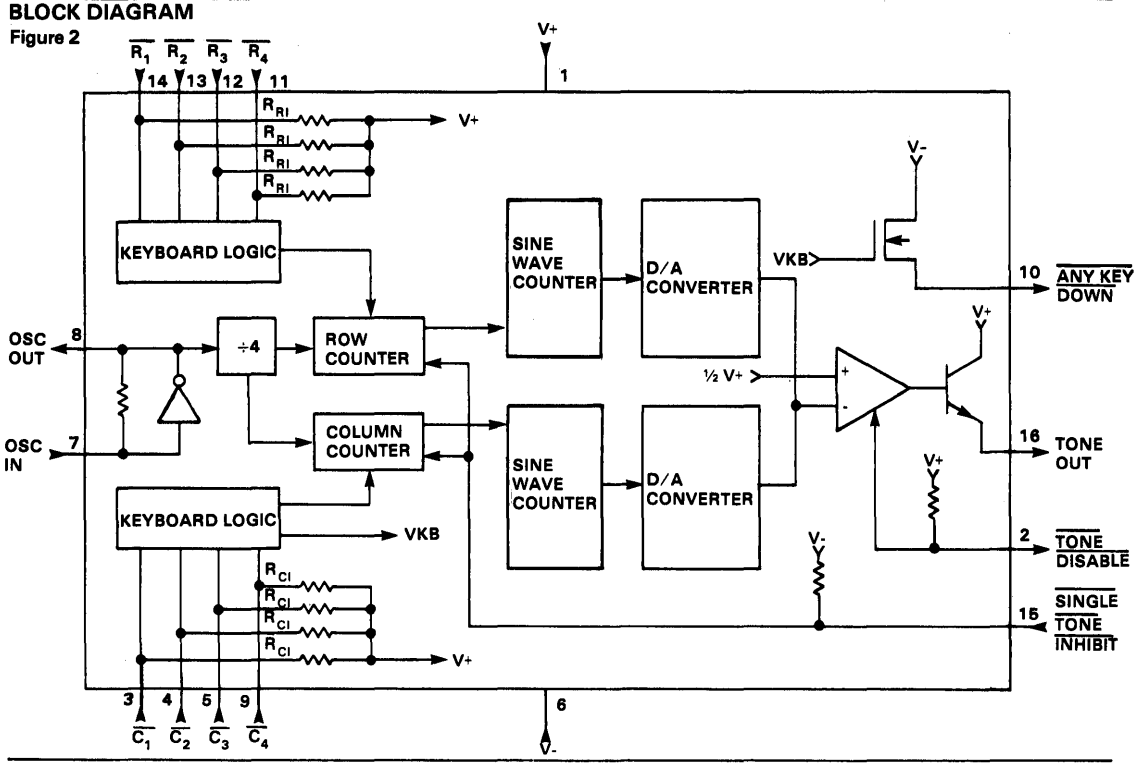
$\overline{\text{ROW}}$-$\overline{\text{COLUMN}}$ INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

With $\overline{\text{Single Tone Inhibit}}$ at V+, connection of V– to a single column will cause the generation of that column tone. Connection of V– to more than one column will result in no

XII

BLOCK DIAGRAM

Figure 2



FUNCTIONAL DESCRIPTION (Continued)

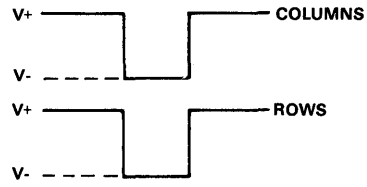
tones being generated. The application of V– to only a row pin or pins has no effect on the circuit. There must always be at least one column connected to V– for row tones to be generated. If a single-row tone is desired, it may be generated by tying any two column pins and the desired row pin to V–. Dual tones will be generated if a single-row pin and a single-column pin are connected to V–. When $\overline{\text{Single Tone Inhibit}}$ is tied to V–, only dual tones will be generated.

Each keyboard input is standard CMOS with a pull-up resistor to the V+ supply. These inputs may be controlled by a keyboard or electronic means. Open-collector TTL or standard CMOS (operated off same supply as the MK5089) may be used for electronic control. Refer to Figures 3 and 4.

The switch contacts used in the keyboards may be void of precious metals, due to the CMOS network's ability to recognize resistance up to 1 kΩ as a valid key closure.

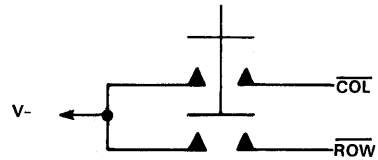
ELECTRONIC INPUT

Figure 3



2-OF-8 KEYBOARD

Figure 4



V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5089 contains an on-board inverter with sufficient loop-gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 1. The oscillator is disabled whenever a keyboard input is not sensed.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION

Table 1

	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard
Row f_1	697	701.3	+0.62
Row f_2	770	771.4	+0.19
Row f_3	852	857.2	+0.61
Row f_4	941	935.1	-0.63
Col f_5	1209	1215.9	+0.57
Col f_6	1336	1331.7	-0.32 **High Group**
Col f_7	1477	1471.9	-0.35
Col f_8	1633	1645.0	+0.73

$\overline{\text{ANY KEY DOWN}}$, Pin 10

The $\overline{\text{Any Key Down}}$ output is used for electronic control of receiver and/or transmitter switching and other desired functions. It switches to the V- supply when a keyboard button is pushed, and is open-circuited when not. The $\overline{\text{AKD}}$ output switches regardless of the $\overline{\text{Tone Disable}}$ and $\overline{\text{Single Tone Inhibit}}$ inputs.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull down to the V- supply and when floating or tied to V-, any input situation that would normally result in a single tone will now result in no tone, with all other chip functions operating normally.

When forced to the V+ supply, single or dual tones may be generated as described in the paragraph under Row-Column Inputs.

TONE OUT, Pin 16

The tone output pin is connected internally in the MK5089 to the emitter of an npn transistor whose collector is tied to V+. The input to this transistor is the on-chip operational amplifier which mixes the row and column tones together and provides output level regulation.

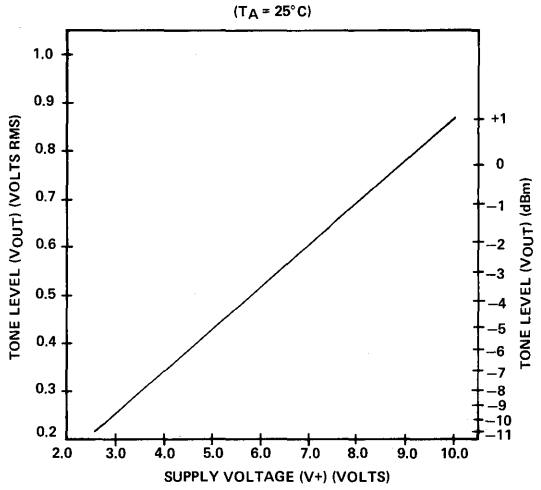
The output tone level of the MK5089 is a function of supply voltage. Figure 5 is a plot of the typical output level of a single-tone output vs. supply voltage. The level of a dual-tone output is the sum of the levels of a single-row and a single-column output.

The row and column output waveforms are shown in Figures 6 and 7. These waveforms are digitally-synthesized using on-chip D-to-A converters. Distortion measurement of these unfiltered waveforms will show a typical distortion of 7% or less.

The on-chip operation amplifier of the MK5089 mixes the row and column tones to result in a dual-tone waveform. Spectral analysis of this waveform will show that typically

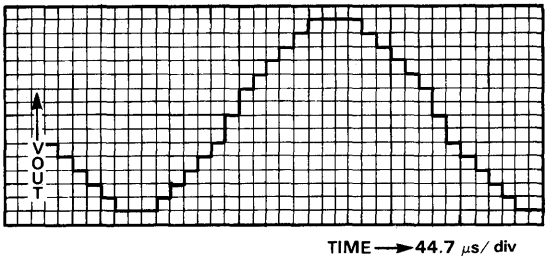
TYPICAL SINGLE-ROW LEVEL VS. SUPPLY VOLTAGE

Figure 5



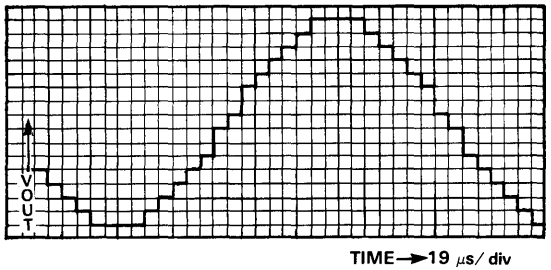
ROW 2 TONE OUTPUT

Figure 6



COLUMN 4 TONE OUTPUT

Figure 7



all harmonic and intermodulation distortion components will be -30 dB down when referenced to the strongest fundamental (column tone).

A commonly-quoted method of dual-tone distortion measurement is the comparison of total power in the unwanted components (i.e. intermodulation and harmonic components) with the total power in the two fundamentals.

XII

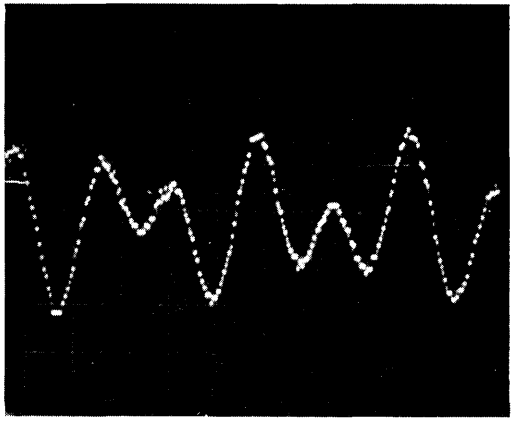
For the MK5089 dual-tone waveform, THD is -20 dB maximum.

A simpler measurement may be made directly from the screen of a spectrum analyzer by relating any component to one of the fundamentals. The MK5089 dual-tone spectrum will show all individual harmonic and IMD components are typically at least 30 dB down with respect to the column tone.

Figures 8 and 9 show a typical dual-tone waveform and its spectral analysis.

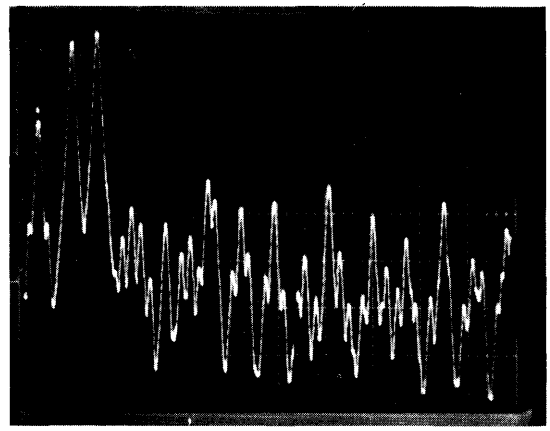
TYPICAL DUAL-TONE WAVEFORM (ROW 1, COL. 1)

Figure 8



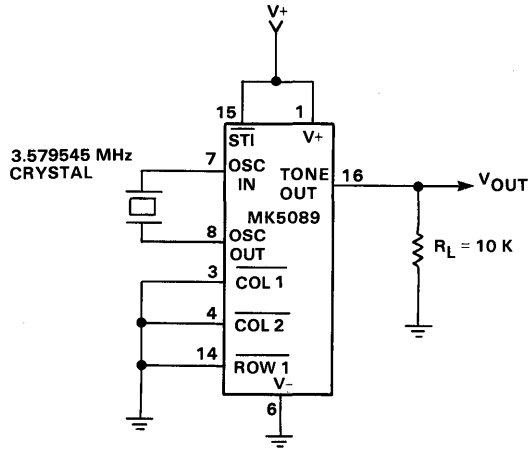
SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 8 (Vert-10 dB/div, Horizontal-1kHz/div)

Figure 9



TONE LEVEL TEST CIRCUIT

Figure 10



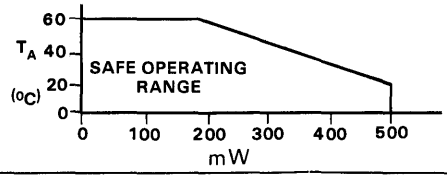
NOTE: Keyboard connections shown are for Row tone level test. Only $\overline{\text{Col 1}}$ (Pin 3) should be connected to V- for Column tone level test.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ ..... 10.5 Volts
Any Input Relative to V+ ..... +0.30 Volts
Any Input Relative to V– ..... –0.30 Volts
Operating Temperature ..... –30°C to +60°C
Storage Temperature ..... –55°C to +85°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(–30°C ≤ T_A ≤ 60°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Supply Voltage	3.0		10.0	V	
V_{IL}	Input "0"	V–		30% of V+	V	
V_{IH}	Input "1"	70% of V+		V+	V	
R_I	Input Pull-Up Resistor	20		100	kΩ	

AC CHARACTERISTICS

(–30°C ≤ T_A ≤ 60°C; 3.0 V ≤ V+ ≤ 10.0 V)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{OUT}	Tone Output (R_{LOAD} = 10 K)	–10		–7	dBm	1,7
PE_{HB}	Pre-Emphasis, High Band	2.4	2.7	3	dB	
DIS	Output Distortion			–20	dB	2,6
t_{RISE}	Rise Time		2.8	5.0	ms	3
$I_{\overline{AKD}}$	$\overline{\text{Any Key Down}}$ Sink Current to V–	500			μA @5 V	
$I_{\overline{AKDO}}$	$\overline{\text{AKD}}$ Off-Leakage			2.0	μA@5 V	
I_{SO}	Supply Current-Operating			2.0	mA@3.5 V	5
I_{SST}	Supply Current-Standby			200	μA@10.0 V	4
V_{NKD}	Tone Output - No Key Down (R_{LOAD} = 10 kΩ)			–80	dBm	

NOTES

1. Single-tone, low-group. Any V+ between 3.4 and 3.6 V. 0dBm = .775 V.
2. Any dual-tone. Any V+ between 3.4 and 10.0 V. See Figure 10 and Figure 11.
3. Time from a valid keystroke with no bounce to allow the waveform to go from min. to 90% of the final magnitude of either frequency. Crystal parameters: R_S ≤ 100 Ω, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz ± 0.02%, C_L = 18 pF.
4. Stand-by condition is defined as no keys activated, $\overline{TD}$ = Logical 1, $\overline{\text{Single Tone Inhibit}}$ = Logical 0.
5. One key depressed only. Outputs unloaded.
6. Output Distortion measured in terms of total out-of-band power relative to the sum of Row and Column fundamental power.
7. For 3.4 V ≤ V+ ≤ 10.0 V, Tone Output is typically [0.0855 (V+) ± 1 dB] mV_{rms}. Refer to Figures 5 and 10.

XII

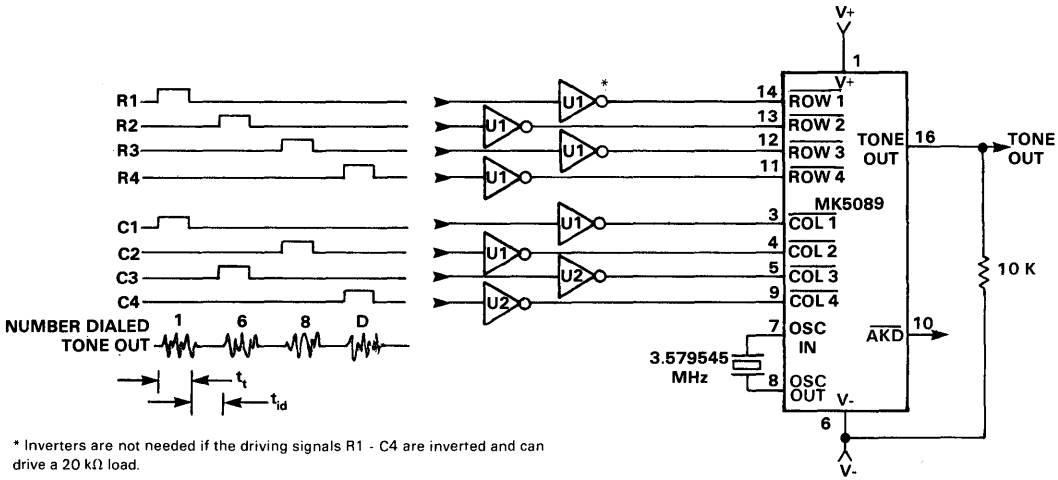
TYPICAL APPLICATION

The MK5089 row and column inputs must be pulled low for a valid key entry. The MK5089 has internal pull-up resistors for both the rows and columns. Therefore, the MK5089 keyboard inputs may be driven by CMOS, TTL, and TTL open-collector logic without the requirement for external pull-up resistors. Thus, the MK5089 can be easily used in electronic or μP dialing applications, as shown in Figure 11.

V+ and V- on the MK5089 should be typically connected to the supply used for the electronic drive circuitry. However, care must be taken to ensure that V+ does not exceed the specified 10 volt maximum. The logic levels present at the MK5089 inputs must meet the criteria specified under the Absolute Maximum Ratings and Electrical Characteristics.

TYPICAL APPLICATION

Figure 11



* Inverters are not needed if the driving signals R1 - C4 are inverted and can drive a 20 kΩ load.

NOTE:

U1 and U2 are hex inverters (TTL - 7404, 74LS04; TTL open-collector - 7405, 74LS05; CMOS - 4049)

$t_t \geq 50$ ms and 45 ms $\leq t_{id} \leq 3$ s to meet Bell Specifications PUB 47001, section 4.3

t_t = tone duration time

t_{id} = interdigit time

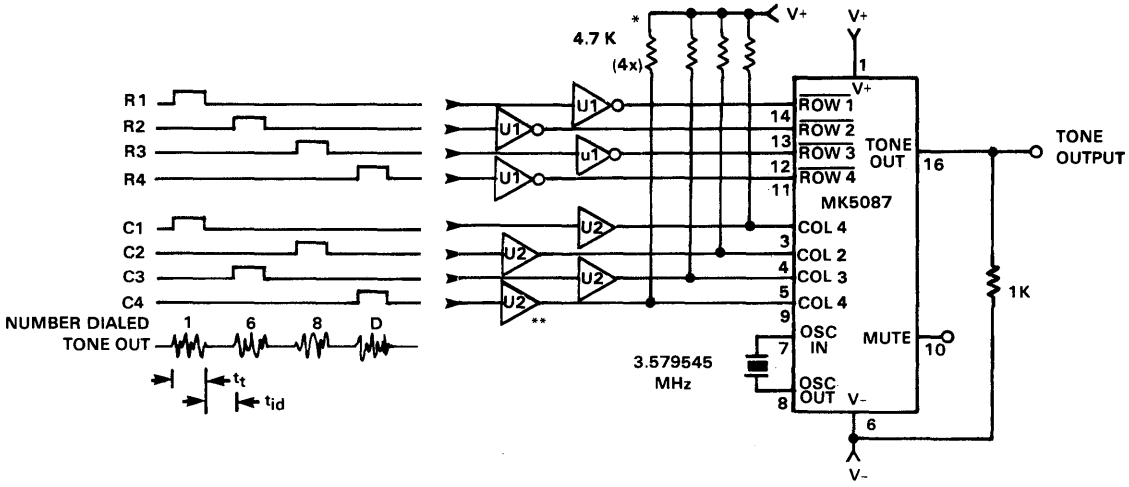
APPLICATION BRIEF

MK5087/89 ELECTRONIC DRIVE

The purpose of this application brief is to provide information as to the various means by which the MK5087 and MK5089 keyboard inputs may be electronically driven.

The MK5087 keyboard inputs can be driven by both CMOS and TTL logic. With the MK5087, the row inputs must be pulled low for a valid key entry. Since the MK5087 has internal pull-up resistors on the rows and pull-down resistors on the columns, external pull-ups are only needed when driving the column inputs with TTL open-collector logic. The circuit diagram in Figure 1 shows the interface for electronically driving the MK5087.

Figure 1



* Only needed when using TTL open-collector logic

** Inverters and buffers are not needed if the driving signals R1 - R4 are inverted and R1 - C4 can drive a 4.7 kΩ load.

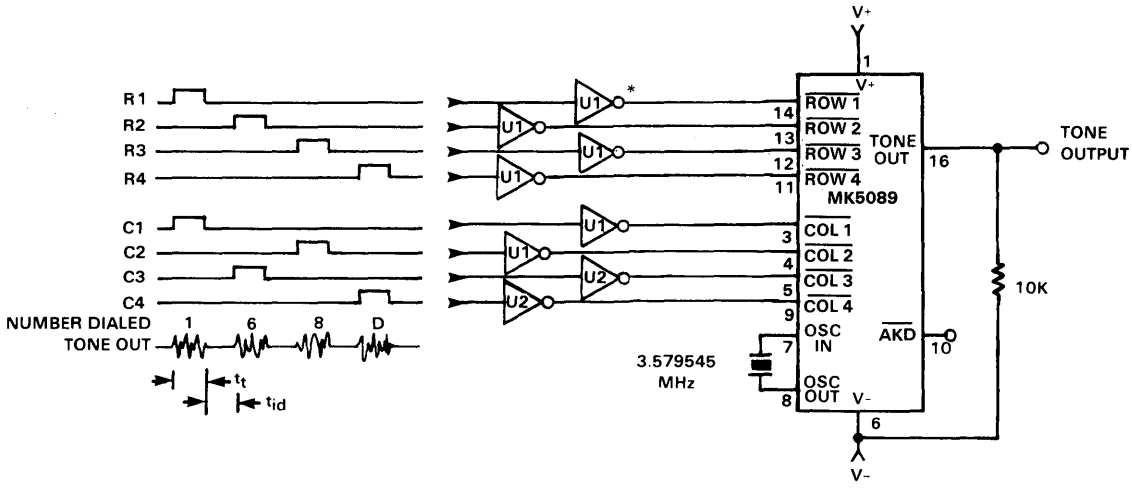
NOTE:

U1 is a hex inverter (TTL - 7404, 74LS04; TTL open-collector - 7405, 74LS05; CMOS - 4049)
U2 is a hex buffer (TTL open-collector - 7407, 74LS07, 7417, 74LS17; CMOS - 4050)
$t_t \geq 50$ ms and 45 ms $\geq t_{id} \geq 3$ s to meet Bell Specifications PUB 47001, section 4.3
t_t = tone duration time
t_{id} = interdigit time

XII

The MK5089 row and column inputs must be pulled low for a valid key entry. The MK5089 has internal pull-up resistors for both the rows and columns. Therefore, the MK5089 keyboard inputs may be driven by CMOS, TTL, and TTL open-collector logic without the requirement for external pull-up resistors. The interface for electronically driving the MK5089 is shown in Figure 2.

Figure 2



* Inverters are not needed if the driving signals R1 - C4 are inverted and can drive a 20 kΩ load.

NOTE:

U1 and U2 are hex inverters (TTL - 7404, 74LS04; TTL open-collector - 7405, 74LS05; CMOS - 4049)
$t_t \geq 50$ ms and 45 ms $\geq t_{id} \geq 3$ s to meet Bell Specifications PUB 47001, section 4.3
t_t = tone duration time
t_{id} = interdigit time

V+ and V- on the MK5087 and MK5089 should be typically connected to the supply used for the electronic drive circuitry. However, care must be taken to ensure that V+ does not exceed the 10 volt maximum as specified in the MK5087 and MK5089 data sheets. The logic levels present at the MK5087 and MK5089 inputs must meet the criteria specified in the respective data sheets and repeated in Table 1. The high logic level must not exceed V+ and the low logic level must not be more negative than V-.

LOGIC LEVEL REQUIREMENTS

Table 1

	MK5087	MK5089
Column High	≥ .7 V+	≥ .7 V+
Column Low	≤ .1 V+	≤ .3 V+
Row High	≥ .9 V+	≥ .7 V+
Row Low	≤ .3 V+	≤ .3 V+

PRELIMINARY

INTEGRATED TONE DIALER MK5380(N/P/J)

FEATURES

- Low standby power
- Minimum external parts count
- Uses inexpensive 3.579545 MHz television color-burst crystal to provide high-accuracy tones
- Improved loop compensation
- Distortion lower than industry standards
- Low voltage operation - 2.5 volts
- Uses low-cost calculator-type keyboard (Form A contact) or standard 2-of-8 keyboard
- Auxiliary switching functions on chip
- Multiple key entry pin-selectable to either single tone or no tone

DESCRIPTION

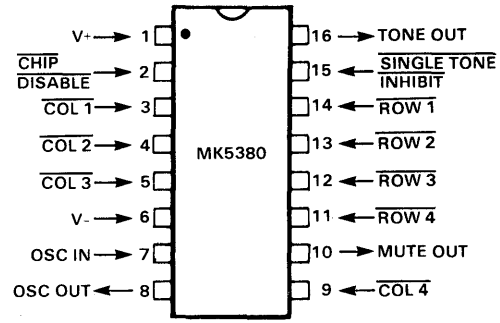
The MK5380 is a monolithic, integrated circuit fabricated using Mostek's Silicon Gate CMOS process. A member of the Tone III* family of integrated tone dialers, the MK5380 uses an inexpensive crystal reference to provide eight different audio sinusoidal frequencies, which are mixed to provide tones suitable for Dual-Tone-Multi-Frequency (DTMF) telephone dialing.

The MK5380 was designed specifically for integrated tone-dialer applications that require the following: wide-supply operation with regulated output, scanned keyboard inputs, auxiliary switching functions, and a Chip Disable input.

Keyboard entries to the MK5380 integrated tone dialer cause the selection of the proper divide ratio to obtain the required two audio frequencies from the 3.579545 MHz reference oscillator.

PIN CONNECTIONS

Figure 1



D-to-A conversion for synthesis of the tones is accomplished on chip by a sinusoidally tapped resistor tree.

Pin connections are shown in Figure 1 and a block diagram of the MK5380 is shown in Figure 2.

FUNCTIONAL DESCRIPTION

V+, Pin 1

Pin 1 is the positive supply pin. The voltage on Pin 1 should be between 2.5 and 10.0 volts, measured relative to V- (Pin 6).

CHIP DISABLE, Pin 2

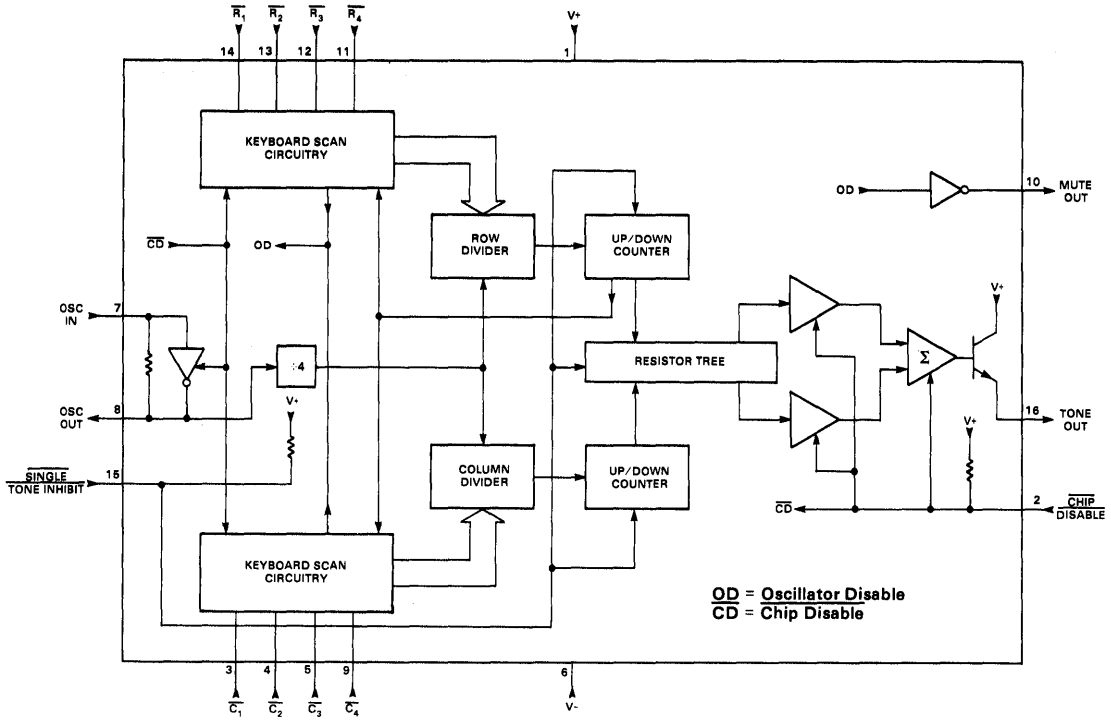
When the Chip Disable input is connected to the V- supply, tone generation will be inhibited, the keyboard inputs will go to a high impedance state, and the amplifiers and oscillator will be powered down. The Chip Disable input has a pull-up resistor to the V+ supply and when floating or tied to V+, the MK5380 will operate normally.

XII

*Trademark of Mostek Corporation

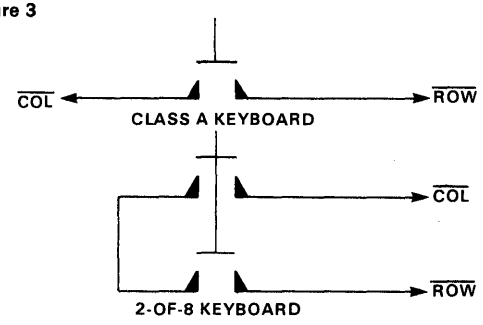
MK5380 BLOCK DIAGRAM

Figure 2



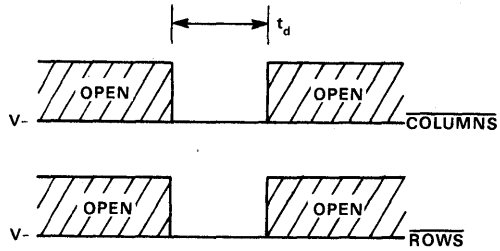
KEYBOARD CONFIGURATION

Figure 3



ELECTRONIC INPUT

Figure 4



NOTE: t_d is minimum tone duration plus oscillator start up time (t_{RISE})

FUNCTIONAL DESCRIPTION (Continued)

COL-ROW INPUTS, Pins 3, 4, 5, 9, 11, 12, 13, 14

The MK5380 features inputs compatible with the standard 2-of-8 keyboard, the inexpensive single-contact (Form A) keyboard, and electronic input. Figure 3 shows how to connect to the two keyboard types and Figure 4 shows waveforms for electronic input.

The internal structure of the MK5380 Row and Column inputs is shown in Figure 5. These inputs are designed to sense a connection between Row and Column, or an electronic input as shown in Figure 4. Table 1 is a functional truth table for these inputs. Note that at least one Row and one Column input must be active to generate a valid output.

When operating with a keyboard, normal operation is for dual-tone generation when any single button is pushed, and single-tone operation when more than one button in the same row or column is pushed. Activation of two or more diagonal buttons will result in no tones being generated.

V-, Pin 6

Pin 6 is the power supply return pin and it is the measurement reference for V+ (Pin 1).

FUNCTIONAL TRUTH TABLE

Table 1

ACTIVE LOW INPUTS		
$\overline{\text{ROW}}$	$\overline{\text{COLUMN}}$	OUTPUT
One	One	Dual Tone
Two or More	One	Column Tone
One	Two or More	Row Tone
Two or More	Two or More	No Tone

NOTE: $\overline{\text{STI}}$ is floating.
$\overline{\text{CD}}$ is floating.

OSC IN, Pin 7; OSC OUT, Pin 8

The MK5380 contains an on-board inverter with sufficient loop gain to provide oscillation when working with a low-cost television color-burst crystal. The inverter's input is Osc In (Pin 7) and output is Osc Out (Pin 8). The circuit is designed to work with a crystal cut to 3.579545 MHz to give the frequencies in Table 2. The oscillator is disabled whenever a keyboard input is not sensed.

Any crystal frequency deviation from 3.579545 MHz will be reflected in the tone output frequency. Most crystals do not vary more than ± .02%.

OUTPUT FREQUENCY DEVIATION

Table 2

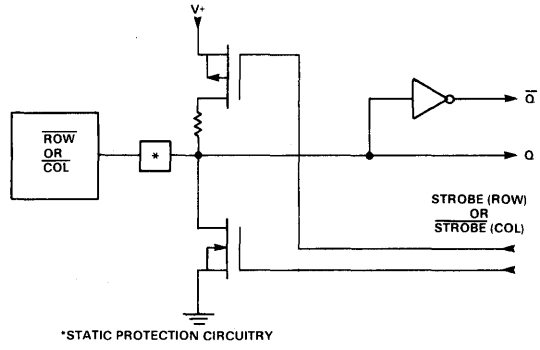
	Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
$\overline{\text{ROW}}$ f_1	697	699.1	+0.31	Low Group
f_2	770	766.2	-0.49	
f_3	852	847.4	-0.54	
f_4	941	948.0	+0.74	
$\overline{\text{COL}}$ f_5	1209	1215.9	+0.57	High Group
f_6	1336	1331.7	-0.32	
f_7	1477	1471.9	-0.35	
f_8	1633	1645.0	+0.73	

MUTE OUT, Pin 10

The Mute output is a conventional CMOS inverter that pulls to V– with no keyboard input and pulls to the V+ supply when a keyboard entry is sensed. This output is used to control auxiliary switching functions that are required to actuate upon keyboard input. The Mute Output switches regardless of the state of the $\overline{\text{Single Tone Inhibit}}$ input. Mute output is not affected by keyboard inputs when $\overline{\text{CD}}$ is tied to V–.

$\overline{\text{ROW}}$ AND $\overline{\text{COLUMN}}$ INPUTS

Figure 5



*STATIC PROTECTION CIRCUITRY

NOTE: $\overline{\text{Chip Disable}}$ is floating.
When $\overline{\text{CD}}$ is tied to V–, $\overline{\text{Row}}$ and $\overline{\text{Column}}$ inputs go to a high impedance state.

$\overline{\text{SINGLE TONE INHIBIT}}$, Pin 15

The $\overline{\text{Single Tone Inhibit}}$ input is used to inhibit the generation of other than dual tones. It has a pull-up to the V+ supply and, when floating, single or dual tones may be generated as described in the paragraph under $\overline{\text{Row}}$-Column inputs.

When forced to the V– supply, any time two or more rows (or columns) are activated, no tone will result.

TONE OUT, Pin 16

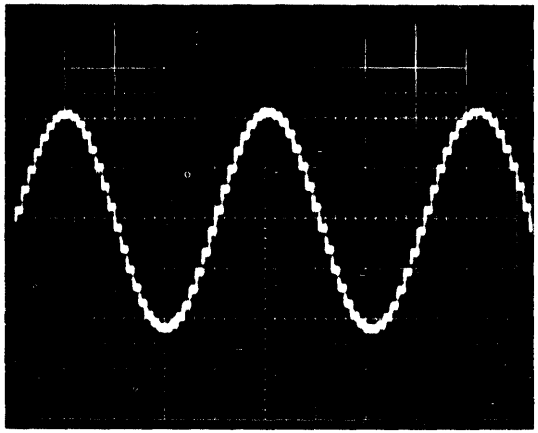
The Tone output pin is connected internally in the MK5380 to the emitter of an npn transistor whose collector is tied to V+. The base of this transistor is the output of the on-chip operational amplifier which mixes the row and column tones together.

The level of a dual tone output is the sum of the levels of a single row and a single column output. This level is controlled by an on-chip reference which is not sensitive to variations in the supply voltage.

A typical single-tone sine wave output is shown in Figure 6. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

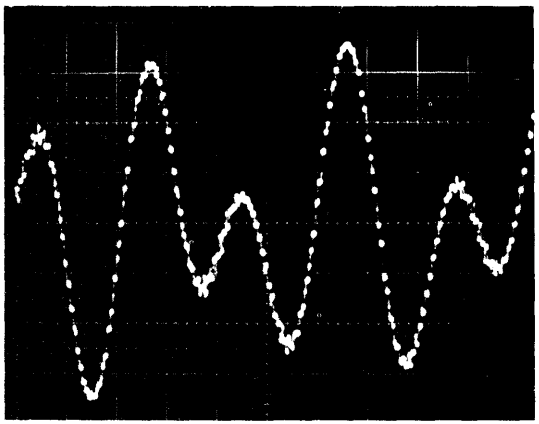
A simple measurement of distortion may be made directly from the screen of a spectrum analyzer by comparing any component to one of the fundamentals.

TYPICAL SINE WAVE OUTPUT - SINGLE TONE
Figure 6

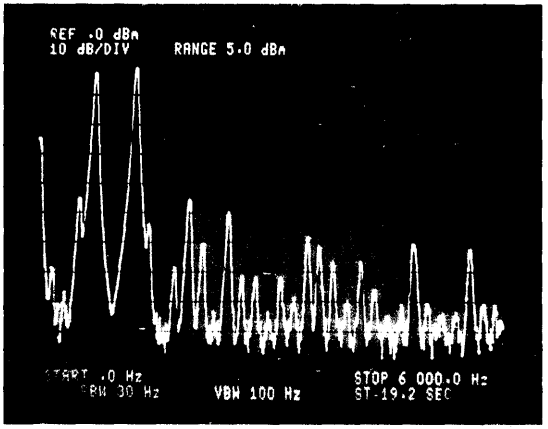


Figures 7 and 8 show a typical dual-tone waveform and its spectral analysis.

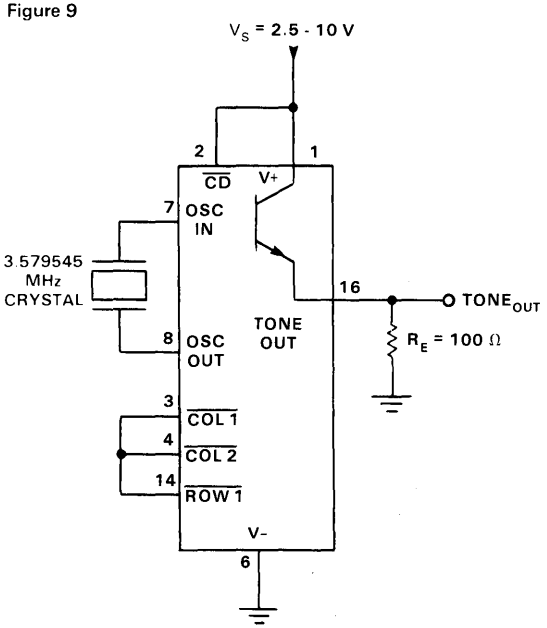
TYPICAL DUAL-TONE WAVEFORM (Row 1, Col 1)
Figure 7



SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 7 (Vert-10 dB/div. Horizontal - 600 Hz/div.)
Figure 8



TONE LEVEL TEST CIRCUIT
Figure 9



NOTE: The above circuit connections are for a Row 1 single tone test. For a Col 1 single-tone test, connect Row 1 (Pin 14) and Row 2 (Pin 13) to Col 1 (Pin 3).

ABSOLUTE MAXIMUM RATINGS*

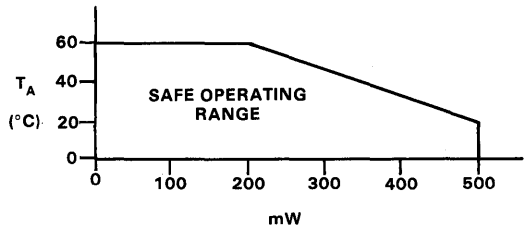
DC Supply Voltage V+ ..... 10.5 volts
Any Input Relative to V+ ..... +0.30 volts
Any Input Relative to V– ..... –0.30 volts
Operating Temperature ..... –30°C to +60°C
Storage Temperature ..... –55°C to +125°C
Maximum Circuit Power Dissipation ..... 500 mW @ 25°C (see derating curve below)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CHARACTERISTICS

POWER DISSIPATION DERATING CURVE

Figure 10



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS

(–30°C ≤ T_A ≤ 60°C)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.5		10.0	V	1, 2
V_{IL}	Input Voltage Low - "0"	V–		30% of V+	V	1
V_{IH}	Input Voltage High - "1"	70% of V+		V+	V	1
R_{IP}	Input Pull-Up Resistance, $\overline{STI}$, $\overline{CD}$	20		125	kΩ	
I_{SSB}	Supply Current - Standby and $\overline{CD}$ floating or tied to V+. (TA = 25°C)		0.1	2.0	μA	3,4,6
			2.0	10.0		3,4,7
I_{SO}	Supply Current - Operating ($\overline{CD}$ floating or tied to V+)		1.0	2.0	mA	3,5,6
			5.0	10		3,5,7
R_{KPU}	Keyboard Pull-Up Resistance $\overline{CD}$ tied to V+		100		kΩ	8
	$\overline{CD}$ tied to V–		10		MΩ	
R_{KPD}	Keyboard Pull-Down Resistance $\overline{CD}$ tied to V+		4.0		kΩ	8
	$\overline{CD}$ tied to V–		10		MΩ	
I_{OLM}	Output Drive, MUTE - No Entry	0.5	2.0		mA	9
		1.0	4.0			10
I_{OHM}	Output Drive, MUTE - Valid Entry	0.5	2.0		mA	11
		1.0	4.0			12

XII

AC CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$; $2.5\ V \leq V+ \leq 10.0\ V$)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{RISE}	Tone Output Rise Time			5.0	ms	13,14
$TONE_{NKD}$	Tone Output-No Key Down or $\overline{CD}$ tied to V–			-80	dBm (600 Ω)	
$TONE_{OUT}$	Tone Output Voltage	200	245	330	mV_{rms}	15, 16, 17
	(Key Down and $\overline{CD}$ floating or tied to V+)		155		mV_{rms}	15,18,19
PE_{HB}	Pre-Emphasis, High Band		2.0		dB	16
DIS	Output Distortion		5.0	10.0	%	16
f_{KBS}	Keyboard Scan Frequency	699		948	Hz	8

NOTES

1. All voltages referenced to V– (Pin 6).
2. 2.5 V minimum instantaneous in loop applications.
3. All outputs unloaded.
4. Current out of Pin 6, no key depressed.
5. Current out of Pin 6, one key depressed.
6. V+ = 2.5 V.
7. V+ = 10.0 V.
8. When $\overline{Row}$ or $\overline{Column}$ inputs are sensed, the keyboard inputs are alternately strobed. When a $\overline{Row}$ is strobed, the $\overline{Row}$ pull-down and $\overline{Column}$ pull-up resistances are enabled. This strobing alternates in the frequency range of 699 to 948 Hz depending on which row is selected. When no inputs exist, either a $\overline{Row}$ or a $\overline{Column}$ input will be statically sensed.
9. V+ = 2.5 V, V_{OLM} = 0.5 V.
10. V+ = 10.0 V, V_{OLM} = 0.5 V.
11. V+ = 2.5 V, V_{OHM} = 2.0 V.
12. V+ = 10.0 V, V_{OHM} = 9.5 V.
13. Time from a valid keystroke with no bounce to allow wave to go from minimum to 90% of final magnitude of either frequency.
14. Crystal parameters: $R_S \leq 100\ \Omega$, L_M = 96 mH, C_M = 0.02 pF, C_h = 5 pF, f = 3.579545 MHz, C_L = 18 pF.
15. Single-tone, low-group $T_A = 25°C$.
16. $2.5\ V \leq V+ \leq 10.0\ V$, $R_E = 100\ \Omega$ (See Figure 9).
17. $TONE_{OUT}$ measured at Pin 16 (See Figure 9).
18. $TONE_{OUT}$ (measured at Pin 16 in loop applications) = 155 mV_{rms} (typical). $R_E = 100\ \Omega$. (See Figure 11).
19. The tone level, when used in a subscriber set, is a function of the output resistor R_E and the telephone ac resistance (R_L). The low-group single-tone output amplitude is a function of R_E and R_L by the relationship:

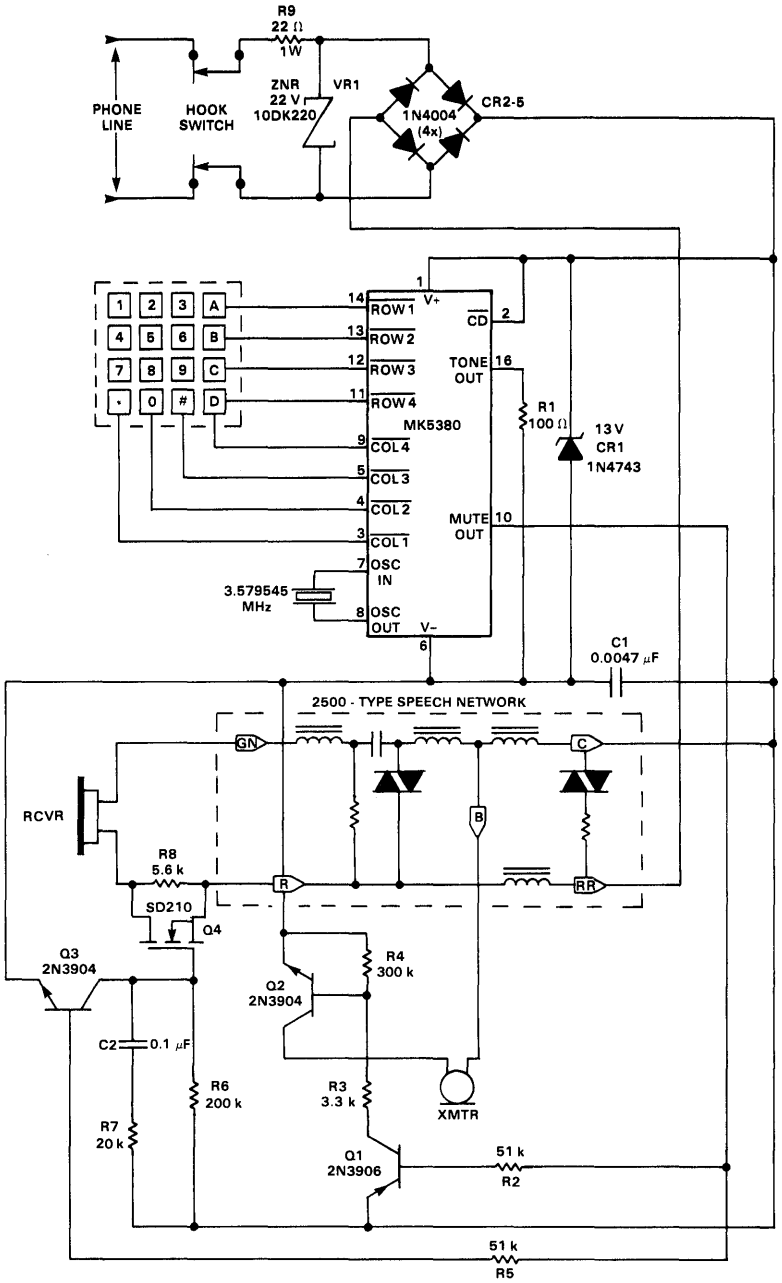
$$\frac{V_o}{TONE_{OUT}} = \frac{1}{0.2 + \frac{R_E}{R_L}}$$

where V_o is the tone output amplitude at the phone line, and R_L is the equivalent ac impedance in shunt with the tone generator (R_L typically varies with loop current). R_E is the resistor value from $TONE_{OUT}$ to V–. In a 2500-Type application R_L will typically vary from 200 to 500 Ω. Thus, at the phone line tone output levels will range from 200 to 400 mV_{rms}, depending on loop current.

TYPICAL APPLICATION

Figure 11 shows an application of the MK5380 in a standard telephone set that uses the standard 2500-Type Speech Network.

TYPICAL APPLICATION IN 2500-TYPE TELEPHONE
Figure 11



APPLICATION NOTE

MK5175/MK5380 PULSE/TONE SWITCHABLE APPLICATION

In addition to its use in applications which are exclusively Tone or Pulse, the MK5175 repertory dialer can be used in conjunction with the MK5380 tone dialer to form a switchable Pulse/Tone Repertory Dialer. Attached is a schematic drawing detailing how the MK5175/5380 application is to interface to the telephone line. Also included in this description are some suggestions for alternate circuit configurations.

OSCILLATOR CONSIDERATIONS

In this application, switiching from one mode to another requires a single DPDT switch. One pole of the switch determines the elements used by the oscillator, while the other sets the MK5175 in the proper mode of operation. In the Pulse mode, the MK5175 uses a 455KHz ceramic resonator (operating anti-resonantly at 480KHz) as its frequency reference, to give a very accurate 10pps (pulses per second) outpulsing rate. In the Tone mode, the MK5175 uses an RC oscillator whose frequency is determined by the values of C3 and R7. Using standard values of 220pF and 470Kohms, the oscillator frequency will nominally be 8KHz, which results in a signalling rate of 5tps (tones per second). This signalling rate may be changed by varying the value of R7, but in this circuit C3 should not be varied significantly because of its use in both modes. Resistor R7 however, is effectively removed from the circuit when in the Pulse mode because diode D5 is reverse biased. This portion of the application is where many designers of a Pulse/Tone circuit will have problems because of improper switching between the two oscillator circuits.

OSCILLATOR & POWER CONSIDERATIONS

As can be seen, both the MK5175 and MK5380 are continuously powered from either the line (off-hook) or from the battery (on-hook). The typical standby current for the combination is less than 2.0 microamps at 2.5 volts at room temperature. When operating in the Pulse mode, the MK5380 is disabled ($\overline{CD}$ of the MK5380 is pulled low by the Mode switch through diode D4). However, because of the internal 100Kohm pull-up resistor on $\overline{CD}$ of the MK5380 causing an increase in current when $\overline{CD}$ is pulled low, the circuit has been designed to revert to Tone mode when on-hook. This is accomplished using hookswitch B (SPDT) to connect the MK5175 Mode input (and HKS, pin 15) to the positive supply. Note than when going on-hook with the DPDT Mode switch in the Pulse configuration, the ceramic resonator will remain connected even though hookswitch B has placed the MK5175 in the Tone mode. Thus, the RC oscillator must be able to function even in this case, and therefore capacitor C2 was added to counteract the loading effect of the ceramic resonator. The RC oscillator will run approximately 30% slower in the on-hook pulse mode, but the only impact of such a frequency variation will be to increase the required minimum key entry time from 32ms to about 40ms.

STANDBY POWER CONSIDERATIONS

As was previously noted, the circuit reverts to the Tone mode when on-hook, in order to reduce standby current to a minimum. Also note that the Tone Out load resistor R1 is connected to hookswitch B so that excess current cannot be drawn through R1 when on hook. It is **not recommended** that the MK5380 be powered down when on hook. Doing this will not only violate the input specifications for the MK5380, but will also cause the circuit to draw excess current.

PULSE MODE OPERATION

In the Pulse mode, the Mode switch selects the ceramic resonator as the frequency reference and connects the MK5175 Mode input and MK5380 $\overline{CD}$ input to V−. Thus, the MK5380 is disabled, its keyboard inputs go to a high impedance state, and the MK5175 operates as a standard repertory pulse dialer. With the MK5380 disabled, its Mute output will stay low, thus allowing muting transistors Q3 & Q4 to stay on until $\overline{Mute}$ of the MK5175 goes low to cause muting of the transmitter and receiver. The MK5175 will pulse the line through transistors Q5 & Q6, controlled by the open drain $\overline{Pulse}$ output. Constant current regulator Q1 is used to limit the current to the repertory dialer during pulsing, in order to achieve the >50Kohm break impedance specification required by the telephone company. In the Tone mode however, Q1 is bypassed to allow the MK5380 to directly modulate the telephone line with the DTMF signal.

TONE MODE OPERATION

In the Tone mode, the Mode switch selects the RC oscillator as the frequency reference and connects the MK5175 Mode input to the positive supply, thus

bypassing Q1. In this mode, pin 16 ($\overline{\text{Pulse}}$/13-key) of the MK5175 is pulled high placing the MK5175 in the 12-key Tone mode, and causing pulsing transistors Q5 & Q6 to always be turned on (thus keeping the speech network always connected to the line, as in a standard tone application). Diode D6 prevents current drain on the battery by the telephone line or the speech network. Diode D1 prevents charging of the battery and allows the tone dialer to modulate the line (else the battery will act as a large capacitor dampening the DTMF tones). It should be noted that clipping of the DTMF signal will occur if the minimum instantaneous modulated voltage level drops below the battery voltage minus the series diode drop (2.5 volts in this case).

When **off hook** in the Tone mode, the MK5175 features a bidirectional keyboard scheme that will passively monitor key inputs while the MK5380 scans the keyboard and generates the corresponding tones. When the MK5175 senses a * or # key has been entered, it will disable the MK5380 (MK5175 $\overline{\text{DD}}$, pin 10, will pull MK5380 $\overline{\text{CD}}$, pin 2, low) before the tone can be generated. Thus the * and # keys can be used to control the MK5175 without their tones being generated. The * or # tones may be generated by entering them twice (consecutively), however they cannot be stored in memory for later redial.

When **on hook** in the Tone mode, the MK5175 leaves the MK5380 enabled ($\overline{\text{CD}}$ high) so excess standby current is not drawn through the $\overline{\text{CD}}$ pull-up resistor. In order to avoid keyboard contention, the MK5175, when on hook, passively monitors the keyboard until the MK5380 completes one full keyboard scan cycle and then disables it (the MK5380 keyboard inputs go to a high impedance state when the chip is disabled) and continues scanning the keyboard until the key is released. When on hook, the MK5380 remains disabled only while a key is depressed, thus operating as efficiently as possible. It is very important to realize that **the MK5175 will only operate with a tone dialer that has an active low keyboard scanning scheme, whose inputs will go to a high impedance state** when the chip is disabled. To our knowledge, the MK5380 and MK5389 are the only tone dialers with these features.

ALTERNATE CIRCUIT SUGGESTIONS

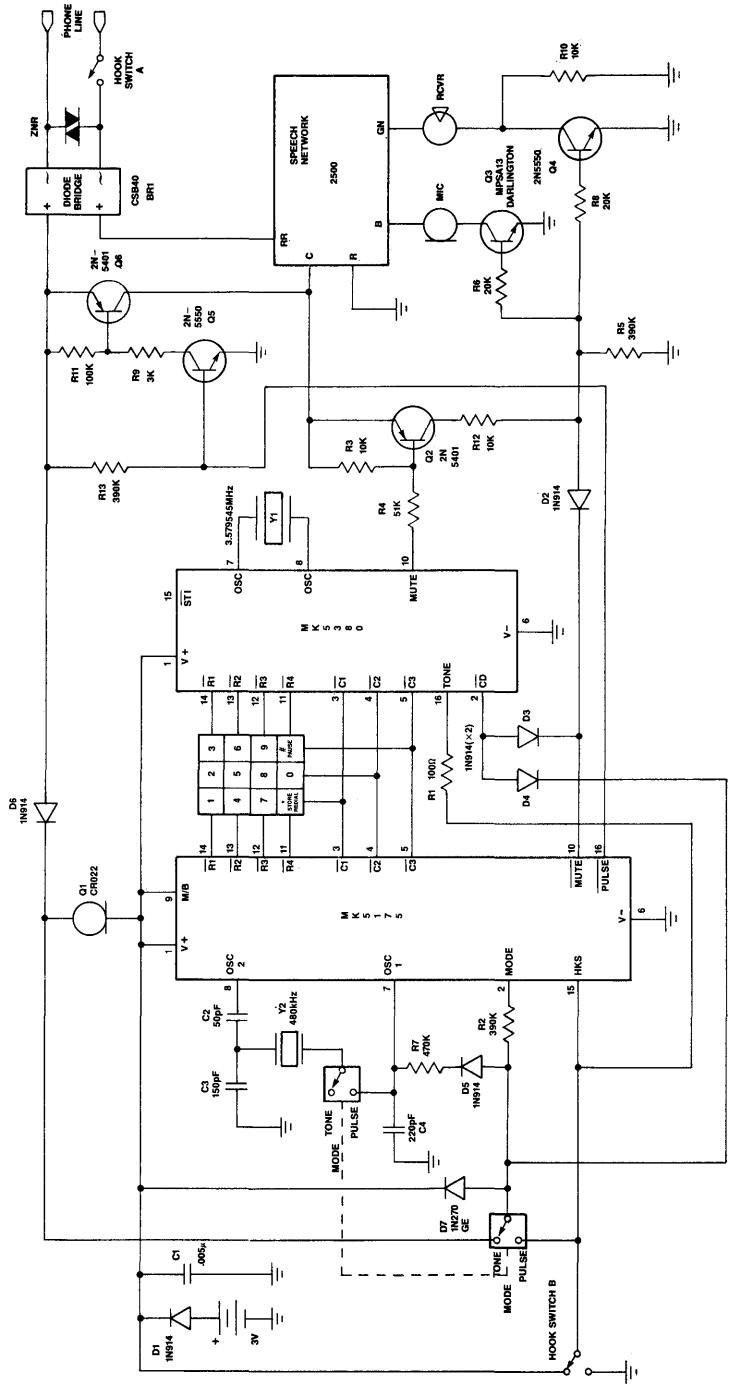
The battery and series diode D1 may be eliminated and replaced with a low leakage capacitor (1000 to 10,000μF) and a series resistor Rs (5 to 10K). This capacitor would be charged directly from the line (through Rs) when off hook, and trickle charged (through a 10Mohm resistor to the postive side of the bridge) when on hook. In such an application it would be advantageous to do memory storage when off hook. Adding another switch labeled PROG/DIAL in series with HKS, pin 15, (PROG= HKS to V+, Dial= HKS to V−) would enable this function. Thus numbers could be programmed into memory while off hook, thereby eliminating the unwanted current drain of key entry operations while on hook. It is important to note that **if a battery is not used, the telephone will eventually lose memory** if disconnected from the phone line or if another phone on the same line remains off-hook for a prolonged period of time.

The constant current regulator Q1 may also be eliminated, but care should be taken to minimize the voltage transients on the dialers when pulsing and to guarantee supply current during break. Placing a 10.5V zener diode and a 68uF capacitor across the supply pins of the dialers should take care of this problem. With Q1 removed, the anode of diode D6 should be connected to the collector of transistor Q6 and a jumper should be put in place of Q1.

CONCLUSIONS

This application is quite suitable for users requiring rotary (Pulse) dialing to reach a long distance service such as MCI or SPRINT, and then switching to Tone mode to dial the long distance number into the MCI or SPRINT system. The application will also operate quite well as a standard Tone or Pulse 10-number repertory dialer. The circuit however, has a problem when dialing in the Tone mode and switching to the Pulse Mode without a hookswitch transition in between. This is due to the fact that during Tone mode manual dialing, the MK5175 passively monitors the keyboard and stores each digit into the LND (Last Number Dialed) buffer while the MK5380 generates the tones on the line. If the circuit is then switched to pulse mode (prior to a hookswitch transition), the MK5175 will outpulse the information just entered into its LND buffer.

MK5175/5380 TONE/PULSE APPLICATION
Figure 1



XII

APPLICATION BRIEF

INTEGRATED DIALER COMPARISON-TONE II vs TONE III

The purpose of this Application Brief is to define the major differences between Mostek's Tone II* and Tone III* series of integrated tone dialers.

The Tone III series was developed as an improvement over Tone II. The minimum operating dc voltage of Tone III has been reduced and loop compensation of the tones generated has been improved. Distortion has also been reduced due to a scheme in which DTMF tones are synthesized using a sinusoidally tapped resistor tree.

The Tone III family of integrated tone dialers is fabricated using Mostek's Silicon Gate CMOS process. Tone III devices use a scanned keyboard scheme with which various keyboard types or electronic input may be used. Tone III dialers also have a Chip Disable feature which causes tone generation to be inhibited, the keyboard inputs to go to a high-impedance state, and the amplifiers and oscillator to be powered down.

The following is a comparison of the major differences between the MK5087 and MK5089 (Tone II), and the MK5380 (Tone III) and MK5389 (Tone III).

KEYBOARD TYPE

- ☐ MK5087 - Class A; 2-of-7 or 2-of-8 (K/B common floating)
- ☐ MK5089 - 2-of-7 or 2-of-8 (K/B common tied to V-)
- ☐ MK5380/5389 - Class A; 2-of-7 or 2-of-8 (K/B common floating or tied to V-)

AUXILIARY FUNCTIONS

- ☐ Pin 2
  - MK5087 - Bipolar XMTR SW (no key = 1; key input = open)
  - MK5089 - Tone Disable
  - MK5380/5389 - Chip Disable
- ☐ Pin 10
  - MK5087/5380 - CMOS MUTE SW (no key = 0; key input = 1)
  - MK5089/5389-N-Chnl MUTE SW ($\overline{AKD}$) (no key = open; key input = 0)

DC OPERATING VOLTAGE

- ☐ MK5087 - 3.5 to 10.0 V
- ☐ MK5089 - 3.0 to 10.0 V
- ☐ MK5380/5389 - 2.5 to 10.0 V

TONE OUTPUT

- ☐ MK5089 - Low Group: [.0855 $V_{DD} \pm 1$ dB] V_{rms} into 10 kΩ load
  High Group: 2.7 dB above low group
- ☐ MK5389 - Low Group: [0.0778 $V_{DD} \pm 1$ dB] V_{rms}
  High Group: 2.7 dB above low group

The following are designed to deliver U.S. telephone system tone levels in a telephone. On a fixed supply the levels will be:

- ☐ MK5087 - Low Group: 317-504 mV_{rms} into 1 kΩ load
  High Group: 2.0 dB above low group
- ☐ MK5380 - Low Group: 245 mV_{rms} typically (see notes 1 and 2)
  High Group: 2.0 dB above low group

TYPICAL APPLICATIONS

- ☐ MK5087 (Uses fixed supply or modulating supply in telephone)
  - Telephone tone-dialer applications
- ☐ MK5089 (Uses fixed or regulated supply in telephone)
  - Electronic or μP-dialing applications
  - European telephone applications
- ☐ MK5380 (Uses fixed supply or modulating supply in telephone)
  - Telephone tone-dialer applications
  - Electronic or μP-dialing applications
  - Interfaces to MK5175/7 repertory dialers
- ☐ MK5389 (Uses fixed or regulated supply in telephone)
  - European telephone applications
  - Electronic or μP-dialing applications
  - Interfaces to MK5175/7 repertory dialers

XII

*Trademark of Mostek Corporation

NOTES:

1. $TONE_{OUT}$ (measured at Pin 16 in loop applications) = 155 mV_{rms} (typical). R_E = 100 Ω.
2. In loop applications, the low-group single-tone output amplitude is a function of R_E and R_L by the relationship:

$$\frac{V_o}{TONE_{OUT}} = \frac{1}{0.2 + \frac{R_E}{R_L}}$$

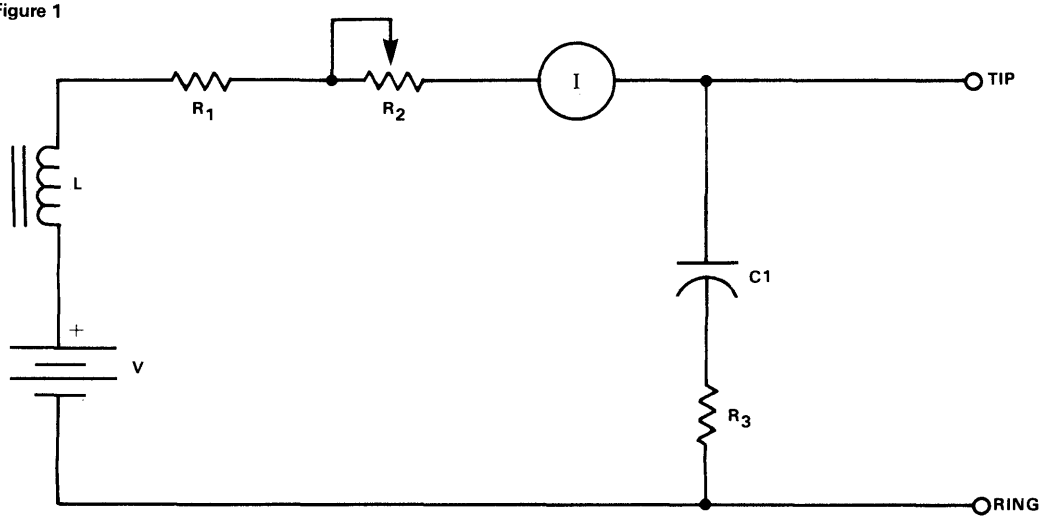
where V_o is the tone output amplitude at the phone line and R_L is the equivalent ac impedance in shunt with the tone generator (R_L typically varies with loop current). R_E is the resistor value from $TONE_{OUT}$ to V-. In a 2500-Type application R_L will typically vary from 200 to 500 Ω. Thus, at the phone line, tone output levels will range from 200 to 400 mV_{rms}, depending on loop current.

APPLICATION BRIEF

LOOP SIMULATOR

The following is a simple circuit which can be used to simulate a telephone loop for most testing purposes. Potentiometer R2 may be varied to provide various loop currents simulating different loop lengths. Normal loop currents range between 20 and 80 mA. Resistor R1 is used to limit the loop current to a maximum of approximately 120 mA (Tip and Ring short-circuited). An ammeter, I, is used to measure the loop current and capacitor C1 and resistor R3 are used to simulate the 600 Ω impedance of the telephone line. Inductor L provides a high impedance in series with the power supply so that the impedance across Tip and Ring is effectively 600 Ω.

Figure 1



V = 48 V (power supply or battery)

R1 = 250 Ω (5 Watts)

R2 = 2 kΩ (2 Watts)

R3 = 600 Ω ±1% (¼ Watt)

I = Ammeter (100 mA full scale)

C1 = 500 μF, -10%, +50%, (50 V)

L ≥ 10 H up to 150 mA dc
($R_L \approx 150\ \Omega$)

XII

1984/1985 MICROELECTRONIC DATA BOOK

INTEGRATED PULSE DIALER WITH REDIAL
MK50981(N)-05

FEATURES

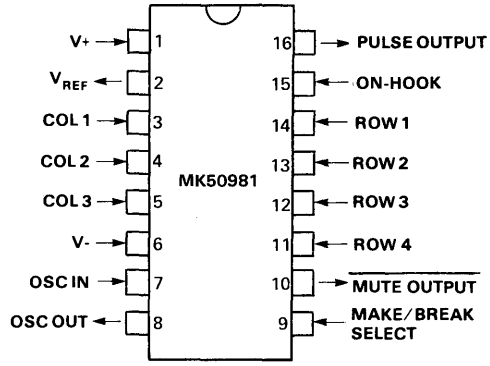
- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses either a standard 2-of-7 matrix keyboard with pos. true common or the inexpensive Form A-type keyboard
- Ceramic resonator used as frequency reference for accuracy
- Make/Break ratio pin-selectable
- Redial with either a * or # input

DESCRIPTION

The MK50981 is a monolithic CMOS integrated circuit, which converts keyboard inputs into pulse signal outputs, simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signaling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

The MK50981 is in either the on-hook or off-hook mode, as determined by the input to the pin designated "On-Hook/Test." In order to accept any key inputs, the MK50981 must be in the off-hook state. Upon sensing a key input, the normally static oscillator is enabled, and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory stores up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except * or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has a FIFO (first-in-first-out) type architecture, and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

PIN CONNECTIONS



The MK50981 also features the redial function. Any 17-digit number sequence may be redialed with a * or # key input, providing that the circuit enters the on-hook mode for a finite time.

Functions of the individual pins are described below.

V+, Pin 1

This is the positive supply input to the part; it is measured relative to V- (Pin 6). The voltage on this pin must be regulated to less than 6 volts, using either the on-chip reference circuitry or an external form of regulation.

V_{REF}, Pin 2

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters, which define the minimum operating voltage of each part. In a typical application, the V_{REF} pin is simply tied to V- (Pin 6). The internal circuit, with its associated I-V characteristic, is shown in Figure 1.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to 60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation 25°C 500mW
Maximum Voltage on any Pin ..... (V+) + 0.3; (V–) –0.3 Volts

*Stresses above these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or at any other condition above those indicated in the operational sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS AT 25°C

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.5	4	6.0	V	
I_{MR}	Memory Retention Current		0.7		μA	1
I_{OP}	DC Operating Current		100		μA	2
V_{REF}	Magnitude of (V+ - V_{REF}) I_{SUPPLY} = 150μA		2.5		V	
I_M	Mute Sink Current: V+ = 2.5V, Vo = 0.5V		2.0		mA	
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V		4.0		mA	

NOTES

Typical values are to be used as a design aid and are not subject to production testing.

1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook mode.
2. Current required for proper circuit function. Off-Hook Mode. Valid key input, V_{REF} tied to V–.

AC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
f_{OSC}	Oscillator Frequency (antiresonant mode)		480		kHz	1
P_R	Pulse Rate		10.0		pps	
t_B	Break Time: Pin 9 tied to V+/ tied to V-		61.0/67.0		ms	
t_{IDP}	Interdigital Pause		800		ms	

NOTES

"Typical" values are exact values with a nominal 480 kHz frequency reference (except for oscillator start-up time).

1. Ceramic resonator should have the following equivalent values: $R < 20\Omega$, $R_A \geq 70k\Omega$. $Co \leq 500pF$.

KEYBOARD INPUTS, Pins 3, 4, 5, 11, 12, 13, 14

The MK50981 incorporates an innovative keyboard scheme that allows use of either the standard 2-of-7 keyboard with positive common or the inexpensive single-contact (Form A) keyboard, as shown in Figure 2.

A valid key entry is defined by either a single row being connected to a single column, or V+ being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high, and no keyboard inputs are accepted. When Off Hook, the keyboard is completely static, until the initial valid key input is sensed. The oscillator is then enabled, and the row and columns are alternately scanned (pulled high, then low) to verify that the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

V-, Pin 6

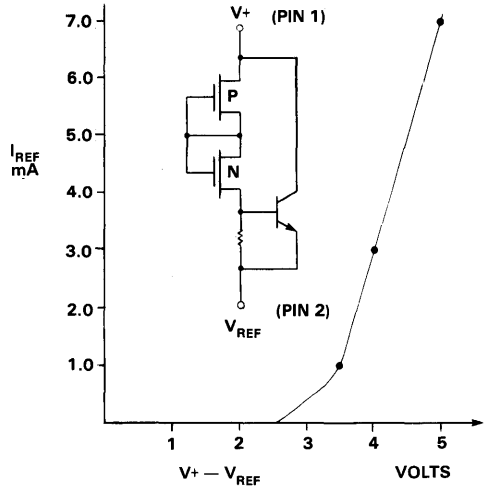
This pin is the negative supply pin input.

OSCILLATOR IN, OUT, Pin 7, 8

The MK50981 contains an on-chip inverter with sufficient gain to provide oscillation when working with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the timing specification section. These values will insure proper oscillator operation in the specified voltage range.

TYPICAL I—V CHARACTERISTICS

Figure 1



The MK50981 may be driven externally with a 480kHz signal on Pin 7.

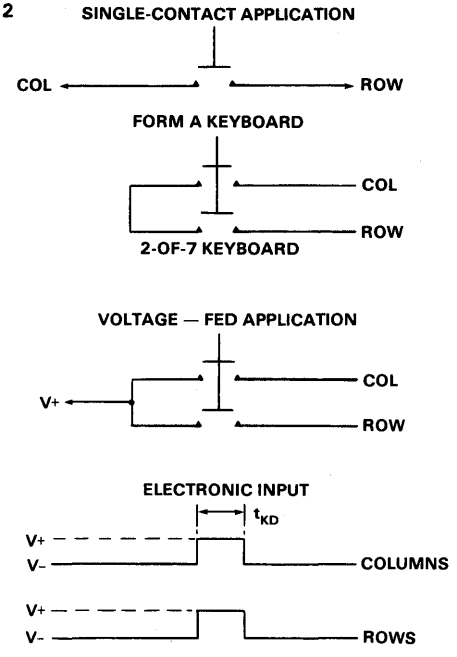
MAKE/BREAK SELECT, Pin 9

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. Table 1 indicates the two popular ratios from which the user can choose.

XIII

KEYBOARD CONFIGURATION

Figure 2



ON-HOOK/TEST, Pin 15

The "Test" or "On-Hook" input of the MK50981 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V- input sets it in the Off-Hook or Normal Mode.

When Off-Hook, the MK50981 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50981 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, if the first key entry is either * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

MAKE/BREAK RATIO SELECTION

Table 1

Input To Make/Break Pin	Pulse Output	
	Make	Break
V+ (Pin 1)	39%	61%
V- (Pin 6)	33%	67%

$\overline{\text{MUTE}}$ OUTPUT, Pin 10

The $\overline{\text{Mute}}$ Output consists of an open-drain, N-channel transistor. It provides the logic necessary to mute the receiver, while the telephone line is being pulsed.

PULSE OUTPUT, Pin 16

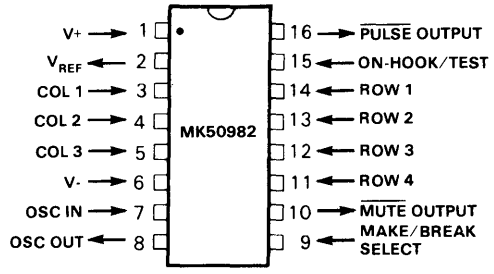
The Pulse output is an open-drain, N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break, pulse rate, and interdigital pause timings.

INTEGRATED PULSE DIALER WITH REDIAL MK50982(N)

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses standard 2-of-7 matrix with pos. true common or the inexpensive Form A-type keyboard
- Ceramic resonator used as frequency reference for guaranteed accuracy
- Make/Break ratio pin-selectable
- Redial with either * or #
- Provision for rapid testing
- On-chip voltage regulator
- Power-Up-Clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50982 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs, one to pulse the telephone line and one to mute the receiver, are provided to implement the pulse dialer function. Accurate timing is accomplished by using a ceramic resonator as the frequency reference for the on-chip oscillator.

The MK50982 is in either the on-hook or off-hook mode as determined by the input to the pin designated, "On-Hook/Test." In order to accept any key inputs, the MK50982 must be in the off-hook state.

Refer to Figure 1 for a block diagram. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except* or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has FIFO-(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50982 also features the redial function. Any 17-digit number sequence may be redialed with an* or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test Pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50982. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may be entered in normal fashion.

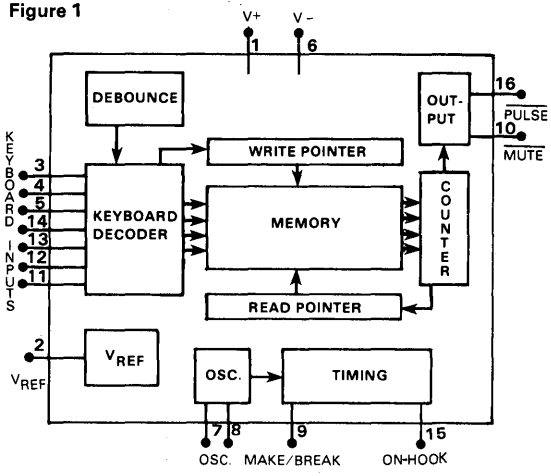
FUNCTIONAL DESCRIPTION

V+, Pin 1

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

BLOCK DIAGRAM

Figure 1

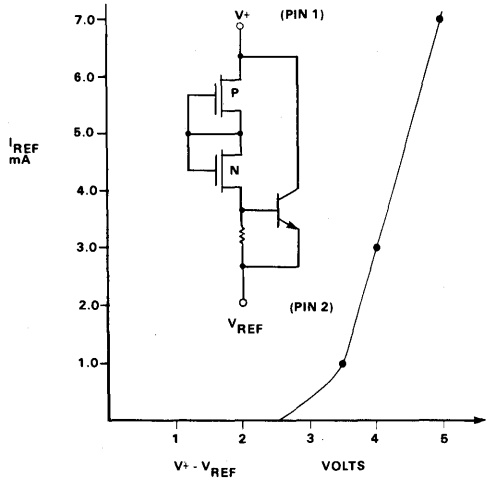


V_{REF}, Pin 2

The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 5, the V_{REF} pin is simply tied to V-(Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 2.

TYPICAL I-V CHARACTERISTICS

Figure 2



V-, Pin 6

This is the negative supply pin to which V_{REF} is normally tied (see V_{REF} paragraph).

KEYBOARD INPUTS, Pins 3, 4, 5, 11, 12, 13, 14

The MK50982 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 3.

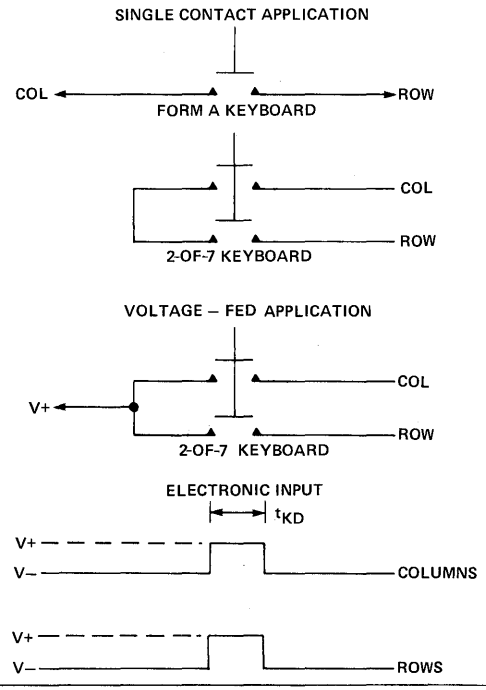
A valid key entry is defined by either a single row being connected to a single column or V+ being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted, thus preventing any accidental key contacts from causing excessive current flow.

When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the row and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

KEYBOARD CONFIGURATION

Figure 3



OSCILLATOR IN, OUT, Pins 7, 8

The MK50982 contains an on-chip inverter with sufficient gain to provide oscillation when used with a low-cost 480kHz ceramic resonator (anti-resonant mode). In addition to the resonator, two external capacitors are required. Suggested equivalent values for the resonator are given in the timing specification section. These values will insure proper oscillator operation in the specified voltage range. The MK50982 may be driven externally with a 480kHz signal on Pin 7.

MAKE/BREAK SELECT, Pin 9

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. Table 1 indicates the two popular ratios from which the user can choose.

MAKE/BREAK RATIO SELECTION
Table 1

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V+ (Pin 1)	39%	61%
V- (Pin 6)	33%	67%

$\overline{\text{MUTE}}$ OUTPUT, Pin 10

The $\overline{\text{Mute}}$ output consists of an open-drain N-channel transistor. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output is shown in the application diagram in Figure 5. Figure 6 shows the timing characteristics of the $\overline{\text{Mute}}$ output.

ON-HOOK/TEST, Pin 15

The "Test" or "On-Hook" input of the MK50982 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode, while a V- input sets it in the Off-Hook or Normal Mode. Any digits to be tested in the "On-Hook/Test" mode must be entered while "Off-Hook."

When Off-Hook, the MK50982 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50982 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, if the first key entry is either * or #, the number sequence stored on-chip will be outpulsed. Any other valid entries will clear the memory and outpulse the new number sequence.

$\overline{\text{PULSE}}$ OUTPUT, Pin 16

The $\overline{\text{Pulse}}$ output is an open-drain N-Channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by controlling the loop current through the network. The timing characteristics of the $\overline{\text{Pulse}}$ output are shown in Figure 6.

TEST CIRCUIT

A test circuit is shown in Figure 4. This circuit can be used to demonstrate the basic operation of the MK50982.

TYPICAL APPLICATION

The schematic diagram in Figure 5 shows one method which can be used to interface the pulse dialer with the telephone line. In the approach shown, the pulse dialer circuitry is in series with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50982 ($\geq$ 150 μA). The current source shown is constructed with two components, Q2 and R1. The current is regulated by the negative feedback provided by R1 to the gate of Q2. Several other implementations can be considered, such as a constant current diode, or a configuration using bipolar transistors.

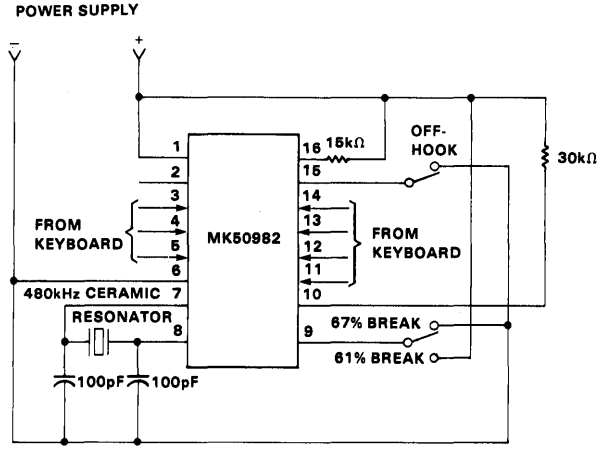
The purpose of transistor Q1 is to take the place of an additional hookswitch contact. When S1 closes, Q1 is turned on and On-Hook (pin 15) is pulled to V-. This sets the MK50982 in the normal mode, ready to accept key inputs.

When going On-Hook, S1 is opened, causing Q1 to be turned off. An on-chip resistor pulls pin 15 to V+ and the current source is disabled. The purpose of D1 is to limit any reverse current flow through the current source. A large-value resistor, R3, allows a small amount of current to maintain the memory on MK50982.

To return Off-Hook, S1 is closed, causing Q1 to be turned on thus tying the On-Hook pin to V-. The $\overline{\text{Pulse}}$ and $\overline{\text{Mute}}$ outputs drive external transistors to perform the outpulsing function. The receiver is connected through transistor Q6 to the speech network. $\overline{\text{Mute}}$ causes the transistor to be held on until outpulsing begins. When $\overline{\text{Mute}}$ switches low, the receiver is removed from the speech network. The pops caused by breaking the line are then isolated from the receiver. The $\overline{\text{Pulse}}$ output drives transistors Q3 and Q5 to make and break the line until the digit has been completely outpulsed. $\overline{\text{Mute}}$ then switches high, returning the receiver to the speech network.

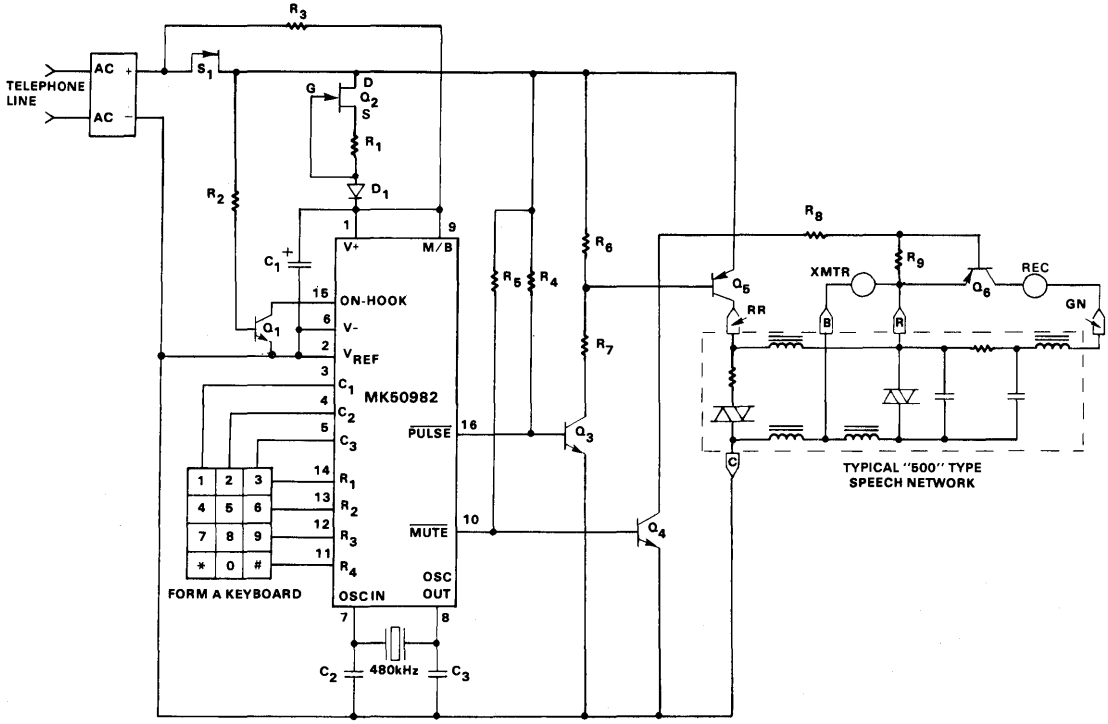
TEST CIRCUIT

Figure 4



TYPICAL APPLICATION

Figure 5



Q1, 3, 4 = 2N5550
Q5, 6 = 2N5401
Q2 = 2N3822

D1 = 1N914
C1 = 20μF (low leakage)
C2, 3 = 100pF ± 20%

R1 = 8kΩ
R2 = 500kΩ
R3 = 22MΩ

R4, 5 = 390kΩ
R6, 9 = 100kΩ
R7, 8 = 3kΩ

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation (25°C) 500mW
Maximum Voltage on any Pin ..... (V+) +0.3; (V-) -0.3 Volts

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($-30°C \leq T_A \leq 60°C$)

DC CHARACTERISTICS

SYM	PARAMETER: SPECIFIC CONDITIONS	MIN	TYP*	MAX	UNITS
V+	DC Supply Voltage	2.5		6.0	V
I_{MR}	Memory Retention Current: Note 1		0.7	2.5	μA
I_{OP}	DC Operating Current: Note 2		100	150	μA
V_{REF}	Magnitude of (V+ - V_{REF}): I_{SUPPLY} = 150 μA	1.5	2.5	3.5	V
I_M	Mute Sink Current: V+ = 2.5, V_O = 0.5V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	"0" Logic Level	V-		20% of V+	V
K_{IH}	"1" Logic Level	80% of V+		V+	V
K_{RU}	Keyboard Pull-Up Resistance: Note 3		4.0		kΩ
K_{RD}	Keyboard Pull-Down Resistance: Note 3		100		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

NOTES
*Typical values are to be used as a design aid and are not subject to production testing.
1. Current necessary for memory to be maintained. All outputs unloaded.On-Hook mode.
2. Current required for proper circuit function. Off-Hook mode, Valid Key input, V_{REF} tied to V-
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

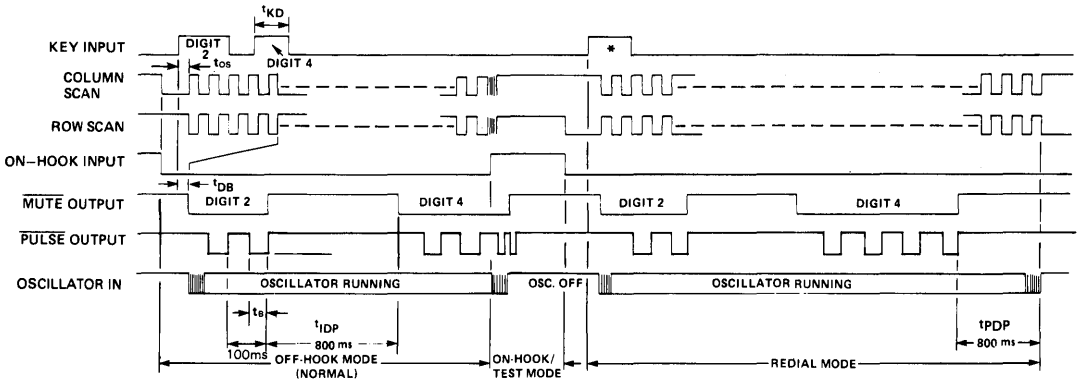
AC CHARACTERISTICS* (The timing Relationships are shown in Figure 6)

SYM	PARAMETER: SPECIFIC CONDITIONS	MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency (antiresonant mode): Note 1		480		kHz
t_{DB}	Keyboard Debounce Time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_{OS}	Oscillator Start-Up Time		6.0		ms
P_R	Pulse Rate		10.0		pps
t_B	Break Time: Pin 9 Tied to V+/Tied to V-		61.0/67.0		ms
t_{IDP}	Interdigital Pause		800		ms

NOTES:
*Typical values are exact with a nominal 480 kHz frequence reference (except for oscillator start-up time).

Ceramic resonator should have the following equivalent values R <20Ω, $R_A \geq$ 70k Ω, Co ≤ 500pF.

TIMING CHARACTERISTICS
Figure 6

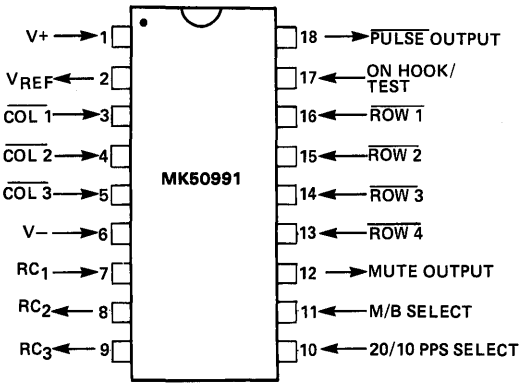


INTEGRATED PULSE DIALER WITH REDIAL MK50991(N)

FEATURES

- Direct telephone-line operation
- CMOS technology is used for low-voltage, low-power operation
- Uses either a standard 2-of-7 matrix keyboard or the inexpensive Form A-type keyboard
- Inexpensive RC oscillator used as frequency reference
- Redial with either a * or # input
- Make/Break ratio and pulse rate are pin-selectable
- Provision for rapid testing
- On-chip voltage regulator
- Power-up-clear circuitry

PIN CONNECTIONS



DESCRIPTION

The MK50991 is a monolithic CMOS integrated circuit which converts keyboard inputs into pulse signal outputs simulating a rotary telephone dial. It is designed to operate directly from the telephone line and can be interfaced properly to meet telephone specifications in systems utilizing loop-disconnect signalling. Two outputs are provided to implement the pulse dialer function, one to pulse the line and another to mute the receiver. The mute output can be interfaced with a bistable latching relay in applications with this requirement.

The MK50991 is in either the on-hook or off-hook mode as determined by the input to the pin designated "On-Hook/Test." In order to accept any key inputs, the MK50991 must be in the off-hook state. Upon sensing a key input, the normally static oscillator is enabled and the row and column inputs are alternately strobed to verify that the keyboard input is valid. The decoded input is then entered into an on-chip memory. The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit (except * or #) clears the memory buffer and starts the outpulsing sequence. As additional digits are entered, they are stored in the memory and outpulsed in turn. The memory has a FIFO—(first-in-first-out) type architecture and more than 17 digits may be dialed in any number sequence. The limitation is that there can never be more than 17 digits remaining to be outpulsed.

The MK50991 also features the redial function. Any 17-digit number sequence may be redialed with a * or # key input, providing that the circuit enters the on-hook mode for a finite time, t_{OH} (refer to discussion on the On-Hook/Test pin).

An on-chip "Power-Up-Clear" circuit insures reliable operation of the MK50991. If the supply to the circuit should become insufficient to retain data in the memory (see electrical specifications), a "Power-Up-Clear" will occur upon regaining a proper supply level. This function will prevent the "Redial" or spontaneous outpulsing of incorrect data. A new number sequence may then be entered in normal fashion.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation 25°C 500mW
Maximum Voltage on any Pin ..... (V+) + 0.3; (V-) - 0.3 Volts

*Stresses above these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	PARAMETER	MIN	TYP*	MAX	UNITS
V+	DC Operating Voltage	2.5		6.0	Volts
I_{MR}	Memory Retention Current: (Note 1)		0.7	2.5	μA
I_{OP}	DC Operating Current: (Note 2)		100	150	μA
V_{REF}	Magnitude of (V+ - V_{REF}): $I_{supply} = 150\mu A$	1.5	2.5	3.5	Volts
I_{ML}	Mute Sink Current: V+ = 2.5V, Vo = 0.5V	0.5	2.0		mA
I_{MH}	Mute Source Current: V+ = 2.5V, Vo = 2.0V	0.5	2.0		mA
I_P	Pulse Sink Current: V+ = 2.5V, Vo = 0.5V	1.0	4.0		mA
I_{LKG}	Mute and Pulse Leakage: V+ = 6.0V, Vo = 6.0V		0.001	1.0	μA
R_{KI}	Keyboard Contact Resistance			1.0	kΩ
C_{KI}	Keyboard Capacitance			30	pF
K_{IL}	Keyboard "0" Logic Level	V-		20% of V+	Volts
K_{IH}	Keyboard "1" Logic Level	80% of V+		V+	Volts
K_{RU}	Keyboard Pull-Up Resistance: (Note 3)		100		kΩ
K_{RD}	Keyboard Pull-Down Resistance: (Note 3)		4.0		kΩ
R_{OH}	On-Hook Pull-Up Resistance		100		kΩ

NOTES:

*Typical values are to be used as a design aid and are not subject to production testing.

1. Current necessary for memory to be maintained. All outputs unloaded. On-Hook mode. V_{REF} tied to V-.
2. Current required for proper circuit function. Off-Hook Mode. Valid key input, V_{REF} tied to V-.
3. Keyboard to be scanned at 500Hz when oscillator enabled. Row and Column to alternately pull high and low.

AC CHARACTERISTICS
(The Timing Relationships are shown in Figure 4)

SYM	PARAMETER	MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency (Note 1)		4.0		kHz
Δf_{OSC1}	Frequency Stability: 2.5 to 3.5V (Note 2)		± 4		%
Δf_{OSC2}	Frequency Stability: 3.5 to 6.0V (Note 2)		± 4		%
Δf_{OSC3}	Frequency Stability: 150→500 μA (Note 3)		± 3		%
P_R	Pulse Rate: Pin 10 tied to V+/V-		20/10		pps
t_{DB}	Keyboard Debounce Time		10		ms
t_{KD}	Time for Valid Key Entry	40			ms
t_B	Break Time: Pin 9 tied to V+/ tied to V-		66.0/60.0		ms
t_{IDP}, t_{PDP}	Interdigital Pause, Predigital Pause (Note 4)		800+ t_M		ms
t_{MO}	Mute Overlap of Pulse		5		ms

NOTES:

"Typical" values are exact assuming a 4kHz frequency reference.

1. A change in the frequency will result in a proportional change in all circuit timing.
2. For stated voltages, the given "typical" Δf_{OSC} holds from part to part over the stated operating temperature range.
3. Using V_{REF} in conjunction with a current source results in the given "typical" Δf_{OSC} from part to part over the stated operating temperature and current.
4. Time from last break to next break, t_M = 100ms-t_B = make time.

Functions of the individual pins are described below:

V+, Pin 1

This is the positive supply input to the part and is measured relative to V- (pin 6). The voltage on this pin must be regulated to less than 6 volts using either the on-chip reference circuitry or an external form of regulation.

V_{REF}, Pin 2

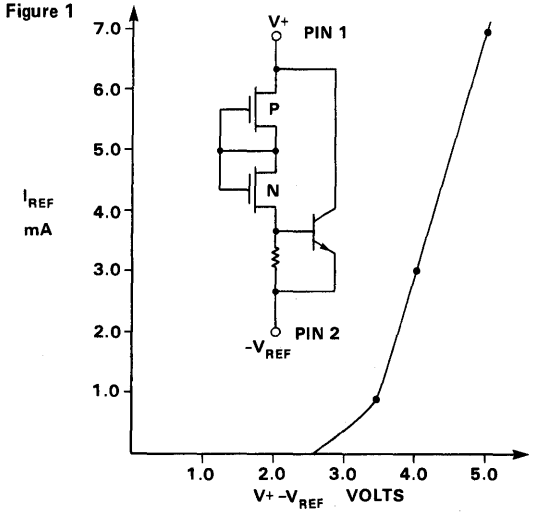
The V_{REF} output provides a negative reference voltage relative to the V+ supply. Its magnitude is a function of the internal parameters which define the minimum operating voltage of each part. In a typical application, as shown in Figure 5, the V_{REF} pin is simply tied to V-(Pin 6). The internal circuit with its associated I-V characteristic is shown in Figure 1.

KEYBOARD INPUTS, Pins 3, 4, 5, 13, 14, 15, 16

The MK50991 incorporates an innovative keyboard

V_{REF} TYPICAL I–V CHARACTERISTICS

Figure 1



XIII

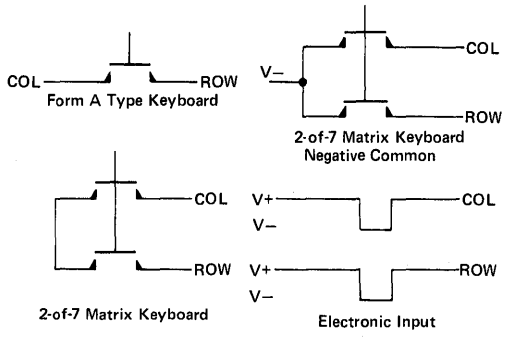
scheme that allows either the standard 2-of-7 keyboard with positive common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column or V- being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. The input must remain valid continuously for 10 ms of debounce time to be accepted.

KEYBOARD CONFIGURATIONS

Figure 2



RC OSCILLATOR, Pins 7, 8, 9

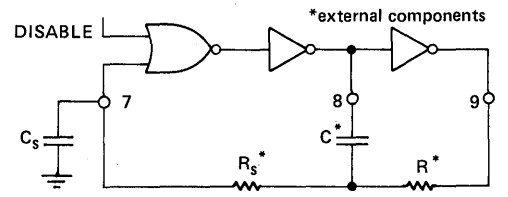
The MK50991 contains on-chip inverters to provide an oscillator which will operate with a minimum of external components. Figure 3 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 10. The oscillator period is given by:

$$T = RC \left[1.386 + \frac{3.5KCs}{C} - \frac{2K}{K+1} \ln \left(\frac{K}{1.5K + 0.5} \right) \right]$$

where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with the capacitance minimized.

OSCILLATOR CONFIGURATION

Figure 3



20/10 PPS SELECT, Pin 10

Tying this input to either V+ (Pin 1) or V- (Pin 6) will select a pulse rate of either 20 or 10 pps respectively.

MAKE/BREAK SELECT, Pin 11

The Make/Break ratio may be selected by connecting the pin to either the V+ or V- supply. The table below indicates the two popular ratios from which the user can choose.

MAKE/BREAK RATIO SELECTION

Table 1

INPUT TO MAKE/BREAK PIN	PULSE OUTPUT	
	MAKE	BREAK
V+ (Pin 1)	34%	66%
V– (Pin 6)	40%	60%

MUTE OUTPUT, Pin 12

The Mute output consists of a complementary pair of CMOS transistors. It provides the logic necessary to be interfaced with a bistable latching relay to Mute the speech network. Upon coming off-hook, a negative transition on Mute will insure the speech network is properly connected to the telephone line. When outpulsing begins, a positive transition will switch the relay, continuously muting the network until the entire number sequence entered is outpulsed. Figure 4 shows, in detail, the timing diagram of the Mute Output.

ON-HOOK/TEST, Pin 17

The "Test" or "On-Hook" input of the MK50991 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode while a V- input sets it in the Off-Hook or Normal Mode.

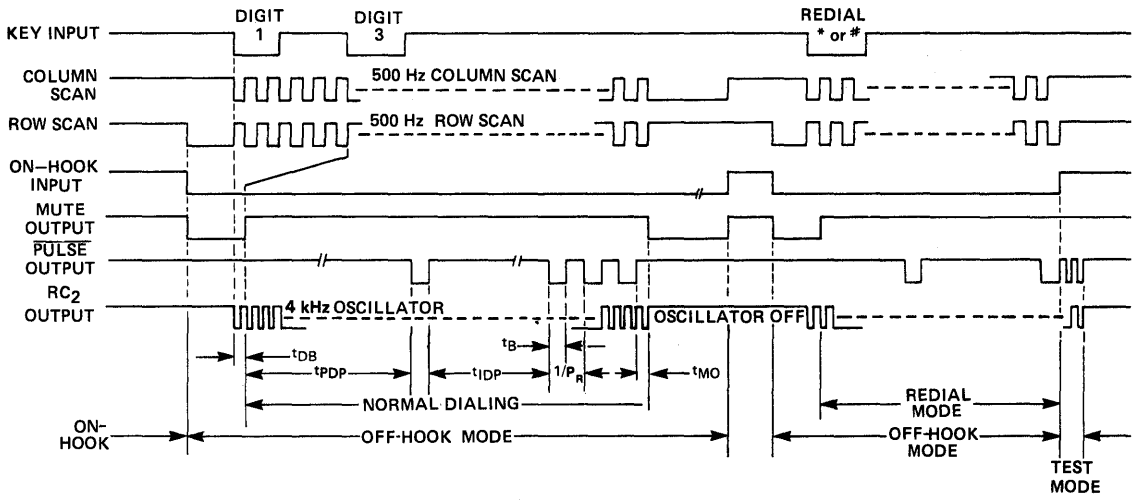
When Off-Hook, the MK50991 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50991 to On-Hook while it is outpulsing causes the remainingdigits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transistion on the Mute Output will insure the speech network is connected to the line. If the first key entry is either a * or #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

TIMING CHARACTERISTICS

Figure 4



PULSE OUTPUT, Pin 18

The Pulse Output consists of an open-drain N-channel transistor. This output provides the logic necessary to pulse the telephone line with the correct Make/Break, pulse rate, and interdigital pause timings. The timing characteristic of the Pulse Output is shown in Figure 4 above.

TYPICAL APPLICATION

The schematic diagram in Figure 5 shows one method which can be used to interface the MK50991 with the telephone line. In this approach, the speech network is connected directly to the telephone line through a metallic relay contact. The pulse signalling circuitry is in parallel with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK50991 (>150μA). Transistor Q_2 provides the source current to the device. The magnitude of this current is determined by the voltage on R_1 due to the forward-biased diodes D_1 and D_2. Transistor Q_1 provides a regulated bias current to the diodes as well as Q_2.

When in the On-Hook mode, S_1 and S_2 are open. The current source is disabled in this manner and only a small amount of current, supplied through R_3, is needed to maintain data in the memory. The relay is open, thereby disconnecting the speech network from the telephone line.

When coming Off-Hook, switches S1 and S2 close, connecting the On-Hook input to V–. Immediately the output of Mute switches low. This transition pulses the relay through Q_5 and Q_6, latching it in the closed position. The speech network is now attached directly to the telephone line for normal conversation. Diode D3 will hold the pulsing Darlington composed of transistors Q_3 and Q_4 off.

Upon receiving a valid key entry, Mute switches high. This transition pulses the relay to its open state, thereby muting the network. The loop current is still passed through the Darlington pair, Q_3 and Q_4, for a predigital pause time of approximately 840ms. (t_{PDP}). Break is accomplished when the Pulse output switches low, cutting the Darlington off. During break, current flow is limited to the current source and the Pulse pullup resistor R_4, insuring a high impedence in this interval. Pulsing of the complete digit continues in this manner. Each digit in the number sequence dialed is separated by standard interdigital pauses (t_{IDP}).

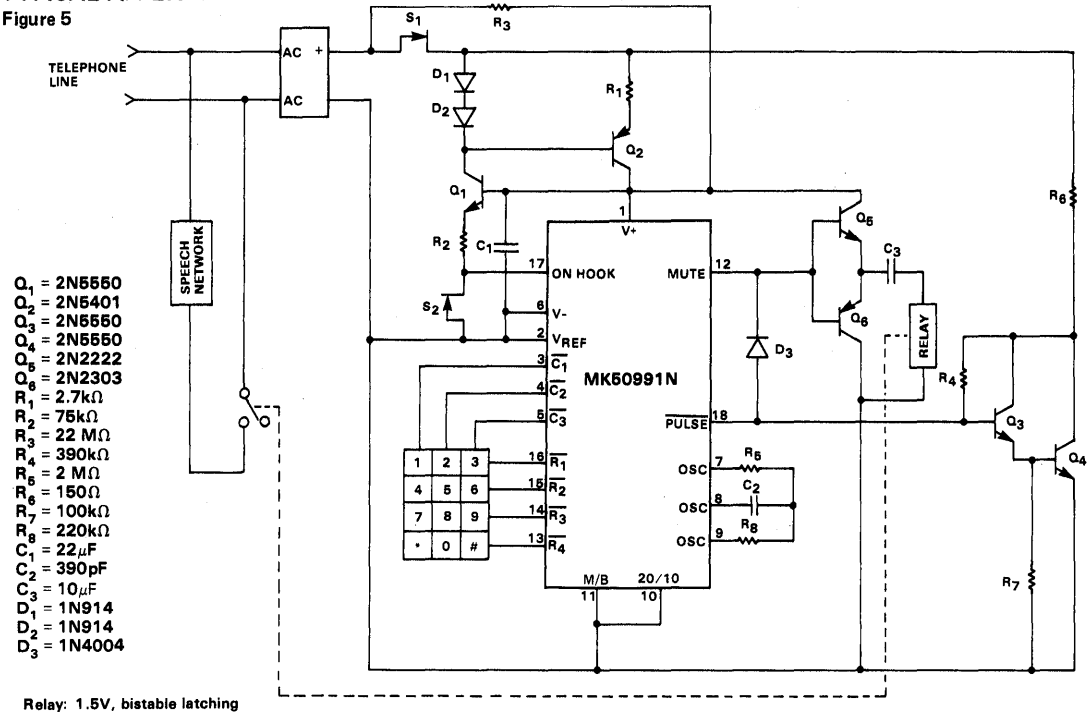
After the final digit is outpulsed, the Mute Output returns low and the speech network is connected back to the telephone line through the relay contact for normal conversation. Returning On-Hook causes Mute to switch high, removing the network from the line.

Applications which do not require operation with a bistable relay may use our MK50981 pulse dialer to better advantage.

XIII

TYPICAL APPLICATION

Figure 5

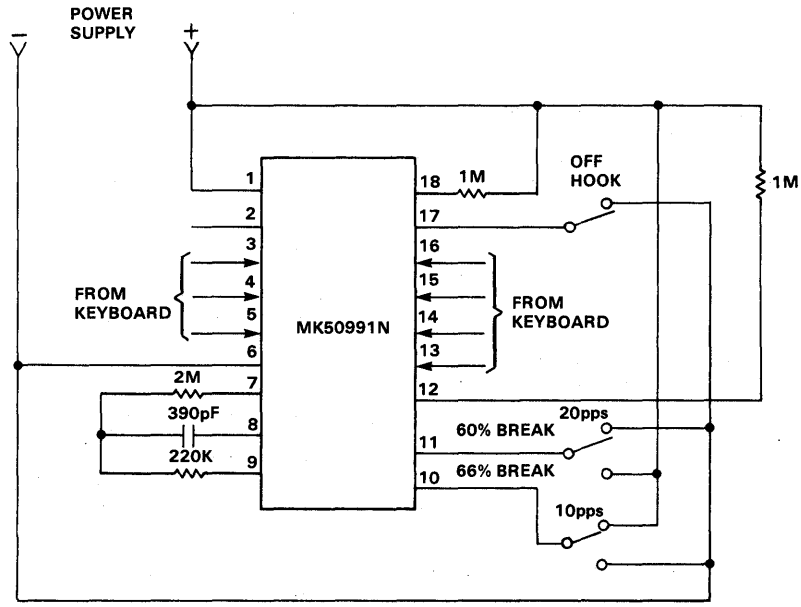


Q_1 = 2N5550
Q_2 = 2N5401
Q_3 = 2N5550
Q_4 = 2N5550
Q_5 = 2N2222
Q_6 = 2N2303
R_1 = 2.7kΩ
R_2 = 75kΩ
R_3 = 22 MΩ
R_4 = 390kΩ
R_5 = 2 MΩ
R_6 = 150Ω
R_7 = 100kΩ
R_8 = 220kΩ
C_1 = 22μF
C_2 = 390pF
C_3 = 10μF
D_1 = 1N914
D_2 = 1N914
D_3 = 1N4004

Relay: 1.5V, bistable latching

TEST CIRCUIT

Figure 6

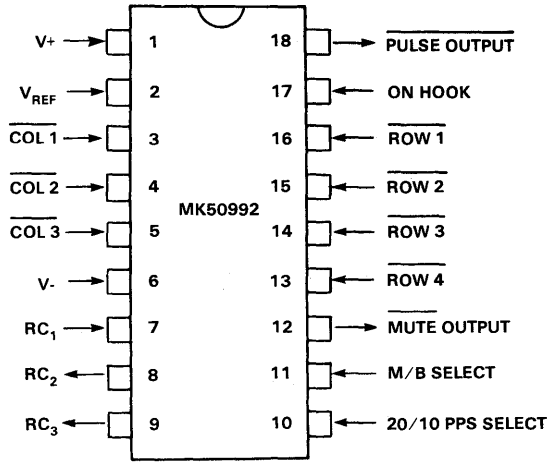


INTEGRATED PULSE DIALER WITH REDIAL
MK50992(N)-05

FEATURES

- Direct Telephone Line Operation
- Uses standard 2-of-7 matrix with negative true common or the inexpensive Form A-type keyboard
- CMOS Technology for Low-Voltage, Low-Power Operation
- Supply Voltage Range 2.5 to 6 volts
- MAKE/BREAK Ratio Pin-Selectable
- Redial with # or *
- Continuous Mute
- Inexpensive RC Oscillator

PIN CONNECTIONS



DESCRIPTION

The MK50992 is a monolithic, CMOS integrated circuit, which uses an inexpensive RC oscillator for its frequency reference and provides all the features required for implementing a pulse dialer with redial. It operates directly off the telephone line supply and converts 2-of-7 keyboard inputs into pulse signals, simulating a rotary telephone dial. When not outpulsing, the MK50992 consumes only micro-amperes of current.

When off-hook, the MK50992 senses a key down condition, verifies that only one key is depressed, and then enters the key's code into an on-chip memory.

The memory will store up to 17 digits and allows keystrokes to be entered at rates comparable to tone dialing telephones. Entering the first digit starts a predigital pause counter and clears the memory buffer. At the end of the predigital pause, outpulsing begins. As digits are entered during the outpulsing period, they will also be stored in the memory. Outpulsing will continue until all entered digits have been dialed. The first 17 digits entered will be stored in the on-chip redial memory and can be redialed by pressing either # or *, provided that the receiver has gone on-hook.

When on-hook, key inputs will not be recognized because the oscillator is disabled. This oscillator inhibit prevents the circuit from drawing excessive current when on-hook.

Functions of the individual pins are described below.

V+ (Pin 1)

This is the positive supply pin. The voltage on this pin is measured relative to V- and is supplied from a 150 μA current source. This voltage must be regulated to less than 6.0 volts.

V_{REF} (Pin 2)

The V_{REF} output provides a reference voltage that tracks internal parameters of the MK50992. V_{REF} provides a negative voltage reference to the V+ supply. Its magnitude will be approximately 0.6 volt greater than the minimum operating voltage of each particular MK50992.

The typical application would be to connect the V_{REF} pin to the V-pin (Pin 6). The supply to the V+ pin (Pin 1) should then be regulated to 150 μA (Iop max). With this amount of supply current, operation of the MK50992 is guaranteed.

The typical internal circuit of the V_{REF} function is shown in Figure 1, with its associated I-V characteristic.

XIII

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 6.2 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +150°C
Maximum Power Dissipation @ 25°C 500mW
Maximum Voltage on any Pin Relative to V- ..... -0.3 Volts
Maximum Voltage on any Pin Relative to V+ ..... +0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these, or at any other condition above those indicated in the operation sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS AT 25°C

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	DC Supply Voltage	2.5	4.0	6.0	V	
R_{KI} C_{KI}	Key Input (R1 - 4R, C1 - C3) Contact Resistance Keyboard Capacitance				kΩ pF	
K_{IRU}	Keyboard Pull-Up Resistance		100		kΩ	
K_{IRD}	Keyboard Pull-Down Resistance		4.0		kΩ	
I_M	Mute Sink Current @ V_O = 0.5V, V+ = 2.5V		2.0		μA	
I_P	Pulse Output Sink Current @ V_O = 0.5V, V+ = 2.5V		4.0		mA	
I_{MR}	Memory Retention Current		0.7		μA	7
I_{OP}	Operating Current		100		μA	1
I_{LKG}	Mute or Pulse Off Leakage V+ = 6.0V V_O = 6.0V		.001		μA	
I_{REF}	V_{REF} Output Source Current (V_{REF} = -6.0V REF to V+)		7		mA	

AC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_{OSC}	Oscillator Frequency		4		kHz	4
t_{OS}	Oscillator Start-Up Time (V+ = 2.5V)		1		ms	2
t_{MO}	Mute Valid After Last Outpulse		5		ms	3,6
Pr	Pulse Output Pulse Rate		10		pps	5
t_{PDP}	Pre-Digital pause		800		ms	3,6
t_{IDP}	Inter-Digital Pause		800		ms	3,6

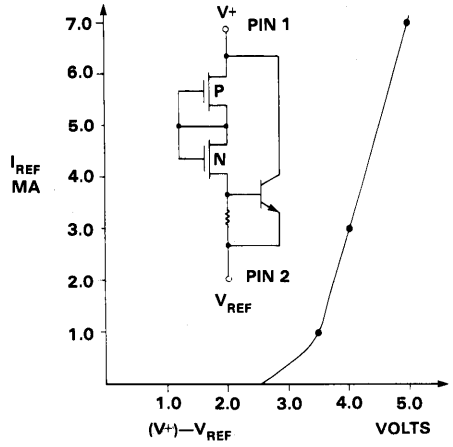
NOTES:

Typical values are to be used as a design aid and are not subject to production testing.

1. Output and V_{REF} unloaded.
2. Debounce plus oscillator startup time ≤ 40ms.
3. These times are directly proportional to the oscillator frequency.
4. R_S = 2MΩ, R = 220KΩ, C = 390pF. See oscillator paragraph.
5. If pin 10 is tied to V+, the Pulse Output Pulse Rate will be 20pps.
6. If the 20pps option is selected, the times will be half of these shown.
7. Current is necessary for memory to be maintained. All outputs are unlaoded.

V_{REF} TYPICAL I-V CHARACTERISTICS

Figure 1



TEST/ON-HOOK (Pin 17)

The "Test" or "On-Hook" input of the MK50992 has a 100kΩ pull-up to the positive supply. A V+ input or allowing the pin to float sets the circuit in its On-Hook or test mode while a V- input sets it in the Off-Hook or Normal Mode.

When Off-Hook, the MK50992 will accept key inputs and outpulse the digits in normal fashion. Upon completion of the last digit, the oscillator is disabled and the circuit stands by for additional inputs.

Switching the MK50992 to On-Hook while it is outpulsing causes the remaining digits to be outpulsed at 100 x the normal rate (M/B ratio is then 50/50). This feature provides a means of rapidly testing the device and is also an efficient method by which the circuitry is reset. When the outpulsing in this mode, which can take up to 300ms, is completed, the circuit is deactivated and will require only the current necessary to sustain the memory and Power-Up-Clear detect circuitry (refer to the electrical specifications).

Upon returning Off-Hook, a negative transition on the Mute Output will insure the speech network is connected to the line. If the first key entry is either a * or a #, the number sequence stored on-chip will be outpulsed. Any other valid key entries will clear the memory and outpulse the new number sequence.

KEYBOARD INPUTS (Pins 3, 4, 5, 13, 14, 15, 16)

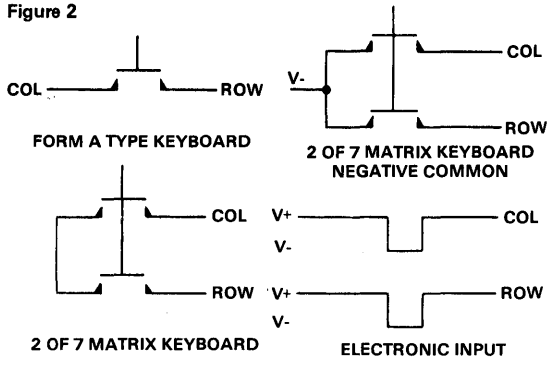
The MK50992 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single contact (Form A) keyboard to be used.

A valid key entry is defined by either a single row being connected to a single column, or V- being simultaneously presented to both a single row and column.

When in the On-Hook mode, the row and column inputs are held high, and no keyboard inputs are accepted. When Off-Hook, the keyboard is completely static until the initial valid key input is sensed. The oscillator is then enabled, and the rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. The input must remain valid continuously for 10ms of debounce time to be accepted.

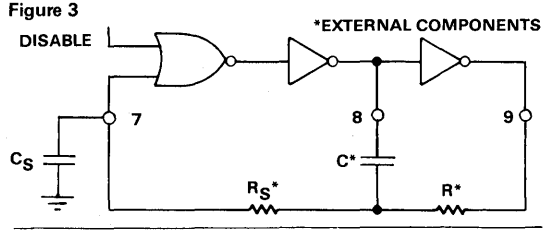
KEYBOARD CONFIGURATIONS

Figure 2



OSCILLATOR CONFIGURATION

Figure 3



OSCILLATOR (Pins 7, 8, 9)

The MK50992 contains on-chip inverters to provide an oscillator that will operate with a minimum of external components. Figure 3 shows the on-chip configuration with the necessary external components. Optimum stability occurs with the ratio $K = R_S/R$ equal to 10. The oscillator period is given by:

$$T=RC[1.386+(3.5KCs)/C-(2K/(K+1-))\ln (K/(1.5K+0.5))]$$

where C_S is the stray capacitance on Pin 7. Accuracy and stability will be enhanced with this capacitance minimized.

V- (Pin 6)

This is the negative supply pin and is normally tied to V_{REF} (see V_{REF} paragraph).

20/10 PPS (Pin 10)

Tying this pin to V- will select an Output Pulse Rate of 10pps. Tying the pin to V+ will select an Output Pulse Rate of 20pps.

MAKE/BREAK (Pin 11)

The MAKE/BREAK pin controls the MAKE/BREAK ratio of the pulse output. The MAKE/BREAK ratio is controlled by connecting V+ or V- to this pin, as shown in the following table.

MAKE/BREAK RATIO SELECTION

Table 1

Input To Make/Break Pin	Pulse Output	
	Make	Break
V+ (Pin 1)	34%	66%
V- (Pin 6)	40%	60%

$\overline{\text{MUTE}}$ OUTPUT (Pin 12)

The $\overline{\text{Mute}}$ output is an open-drain, N-channel transistor designed to drive an external bipolar transistor. This circuitry is usually used to mute the receiver during outpulsing.

The MK50992 $\overline{\text{Mute}}$ output turns on (pulls to the V- supply) at the beginning of the predigital pause and turns off (goes to an open circuit) following the last break. The delay, from the end of the last break until the $\overline{\text{Mute}}$ output turns off, is mute overlap and is specified as t_{MO}.

$\overline{\text{PULSE}}$ OUTPUT (Pin 18)

The $\overline{\text{Pulse}}$ output is an open drain, N-channel transistor designed to drive an external bipolar transistor. These transistors would normally be used to pulse the telephone line by disconnecting and connecting the network.

The MK50992 $\overline{\text{Pulse}}$ output is an open circuit during make and pulls to the V- supply during break.

Outpulsing starts with a make before break.

APPLICATION BRIEF

PULSE DIALER COMPARISON

The purpose of this Application Brief is to define the major differences between Mostek's pulse dialers.

The first Mostek pulse dialers were the MK5098 and the MK5099. Later, the MK50981 and MK50991 were developed to meet other requirements which the MK5098 and MK5099 did not meet. However, these are not direct replacements for the MK5098 and MK5099. Therefore, the improved MK50982 and MK50992 were designed to directly replace the MK5098 and MK5099, respectively. All of Mostek's pulse dialers, except the MK5098, have the last-number-redial feature.

The following is a comparison of all of the major differences between Mostek pulse dialers.

KEYBOARD TYPE

- MK5098/981/982 - Class A or 2-of-7 (K/B common floating or tied to V+)
- MK5099 - 2-of-7 (K/B common tied to V–)
- MK50991/992 - Class A or 2-of-7 (K/B common floating or tied to V–)

MEMORY RETENTION CURRENT

- MK5098 - Does not have last-number redial: $I_{SS} \leq 15$ μA at 2.5 V
- MK5099 - ≤ 20 μA at 2.5 V
- MK50981/982/991/992 - 0.7 μA typical and 2.5 μA maximum

OSCILLATOR

- MK5098/981/982 - 480 kHz Ceramic Resonator (anti-resonant mode) plus two 100 pF capacitors
- MK5099/991/992 - RC Oscillator consisting of 2 resistors and one capacitor

PIN-SELECTABLE OPTIONS

- Make/Break Ratio

  MK5098/981/982 - Pin 9 tied to V+ = 39%/61%
  Pin 9 tied to V– = 33%/67%

  MK5099 - Pin 11 tied to V+ = 39%/61%
  Pin 11 tied to V– = 33%/67%

  MK50991/992 - Pin 11 tied to V+ = 34%/66%
  Pin 11 tied to V– = 40%/60%

- Pulse Rate
  MK5098/981/982 - 10 pps
  MK5099/991/992 - Pin 10 tied to V+ = 20 pps
  Pin 10 tied to V– = 10 pps

OUTPUT LOGIC LEVELS

- Pulse

  MK5098/982/99/991/992 - $\overline{\text{Pulse}}$ output (active low, 0 - true output level)

  MK50981 - Pulse output (active high, 1 - true output level)

- Mute

  MK5098/981/982/99/992 - $\overline{\text{Mute}}$ output (active low, 0 - true output level)

  MK50991 - Mute output (active high, 1 - true output level)

TYPICAL APPLICATION

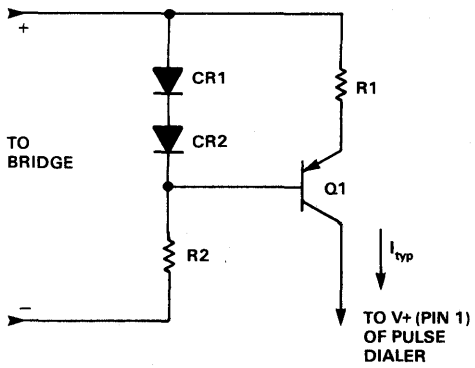
- MK5098/982/99/992 - The mute and pulse outputs of these pulse dialers have logic levels and timing characteristics such that they are easily used in applications requiring pulsing in series with the speech network.
- MK50981/991 - The mute and pulse outputs of these pulse dialers have logic levels and timing characteristics that make them more suitable for use in applications requiring pulsing in parallel with the speech network. The mute output of the MK50991 provides the logic necessary for interface with a bistable latching relay to mute the speech network.

The purpose of this application brief is to discuss the use of constant current sources in pulse-dialer application circuits. Current sources serve two important purposes in pulse-dialer applications. First, they provide a relatively constant current to the pulse dialer so that it may operate consistently during pulsing. Secondly, constant current sources help maintain the high break impedance that is required by U.S. telephone specifications for loop disconnect dialers.

There are various configurations of current sources which can be used to achieve these goals. In this application brief, three different configurations will be examined. All of these current sources are interchangeable.

One of the most commonly used configurations consists of two diodes, one transistor, and two resistors. This configuration is used in the MK50992 typical application. A schematic of this current source is shown in Figure 1.

Figure 1



The operation of this type of current source is as follows. Diodes CR1 and CR2 ensure that the base of transistor Q1 is biased at two diode drops below the voltage at the positive side of the bridge. Resistor R2 provides bias current for diodes CR1 and CR2 and transistor Q1. R2 must be carefully selected to bias CR1 and CR2 past the knee of the current-voltage curve, yet still satisfy break impedance requirements. The emitter-to-base voltage of Q1 is approximately equal to one diode drop ($V_{CR} \approx 0.4$ - 0.7 V). Therefore, the voltage drop across R1 is also approximately equal to one diode drop. The current through Q1 is determined by the value of R1 according to the equation:

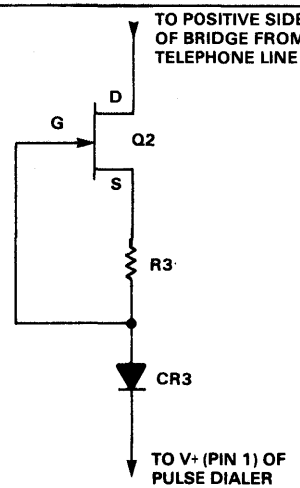
$$I_{typ} \approx \frac{V_{CR1}}{R1}$$

For a typical pulse-dialer application, the following components are recommended:

Q1 = 2N5401
CR1 = CR2 = 1N914
R1 = 1.5 kΩ
R2 = 560 kΩ

Another frequently used current source configuration consists of an N-channel JFET, one resistor, and one diode. This configuration is used in the MK50982 typical application circuit and is shown in Figure 2.

Figure 2



With this type of configuration, the value of resistor R3 and the characteristics of transistor Q2 determine the amount of current that flows to the pulse dialer. As current through R3 increases, the voltage across it (which corresponds to V_{GS} of the FET) also increases, thus regulating the amount of current that flows through Q2.

Diode CR3 is used to block reverse-current flow through the current source to the pulse dialer.

XIII

For a typical pulse-dialer application, the recommended components are:

Q2 = 2N3822
R3 = 12 kΩ
CR3 = 1N914

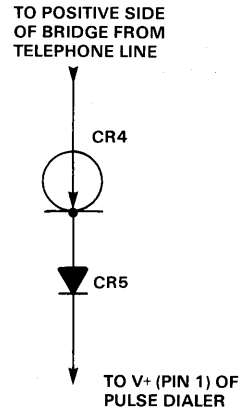
This current source scheme can also be constructed using different types of FETs. The position of R3 will depend upon the type of FET selected.

This type of current source has two main disadvantages over the type shown in Figure 1. The first disadvantage is cost. The FET selected must have a V_{DS} high enough to withstand open-circuit, telephone-line voltage (100 V max), and will be more expensive than a comparable bipolar transistor. The second disadvantage is poor stability. The current that flows through Q2 will vary with changes in the V_P (pinch-off voltage) of the FET. Careful selection of the FET used for Q2 and the tolerance of R3 will decrease the variability of this current source.

A third type of current source in common use is the constant current or regulator diode. This type of current source configuration is shown in Figure 3.

The constant current diode is composed of a transistor similar to the one shown in Figure 2, but with a built-in resistor and feedback loop. These constant current diodes operate according to the same principles as the current source shown in Figure 2.

Figure 3



For this type of current source configuration, the recommended silicon diode (CR5) is a 1N914. A germanium diode, such as the 1N270, may be used for CR3 and CR5 in Figures 2 and 3 respectively if a smaller voltage drop across the current source is desired. This will enable the pulse dialer to operate with a slightly lower voltage present at the telephone line. The constant current diode (CR4) can be any commercially available regulator diode such as the Siliconix CR022, the Siliconix J522, or the Teledyne TCR500. Any constant current diode can be used as long as it provides the minimum current required for operation of the selected Mostek dialer.

1984/1985 MICROELECTRONIC DATA BOOK

PRELIMINARY

TEN-NUMBER REPERTORY DIALER MK5175(N)

FEATURES

- Silicon Gate CMOS process for low-voltage (2.0 V to 10.0 V) and low-power operation
- Stores ten 16-digit telephone numbers
- Line operation off-hook, battery operation on-hook
- Stand-alone Pulse dialer
- Interfaces with Mostek's Tone dialers
- PABX pause key input
- Last-number-dialed memory
- Last number dialed may be transferred to any one of nine other locations
- Make/break ratio is pin-selectable in the Pulse mode
- Uses either the inexpensive Form A-type keyboard or the standard 2-of-7 matrix keyboard with common V– (Tone mode may use SPST switch control key in 13-key mode to avoid redundancies in key entries)
- Power up circuit initializes RAM and logic

DESCRIPTION

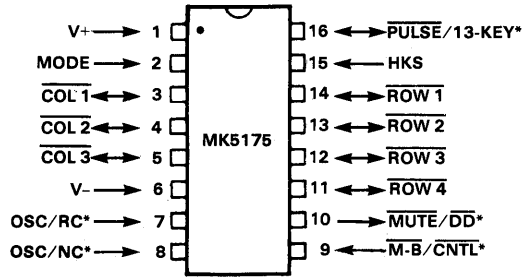
The MK5175 is a monolithic integrated ten-number repertory dialer manufactured using Mostek's Silicon Gate CMOS process. The circuit accepts keyboard inputs and provides the Pulse and Mute logic levels required for loop-disconnect signaling. For DTMF signaling, the MK5175 may be interfaced with one of Mostek's new Tone dialers with low external parts count.

The dialer will function in either Tone or Pulse mode, dependent upon the logic level presented to Pin 2, the "Mode Select" pin. The interpretation of several inputs and outputs is dependent upon the mode selected.

In the Pulse mode, the time base for the circuit is a ceramic resonator which is low-cost, yet provides an accurate reference. In the Tone mode, a single-pin RC oscillator provides the frequency reference for the circuit. This provides the least expensive means to adequately control the tone output rate. The block diagram in Figure 2 illustrates the general internal structure of the MK5175.

PIN CONNECTIONS

Figure 1



*Dual pin designations correspond to the pulse/tone modes, respectively

An on-chip RAM is capable of storing ten 16-digit telephone numbers including the last number dialed. When used in a PABX system, a pause (# key) may be stored in the number sequence. The repertory dialer will recognize this pause when automatically dialing and stop until any key input is received, except the * or the CNTL keys.

The MK5175 repertory dialer uses a standardized pinout scheme, shown in Figure 1, common to all Mostek Tone and Pulse dialers. This will facilitate the design of a family of telephone products using common PC boards and circuit components.

FUNCTIONAL DESCRIPTION

V+, Pin 1

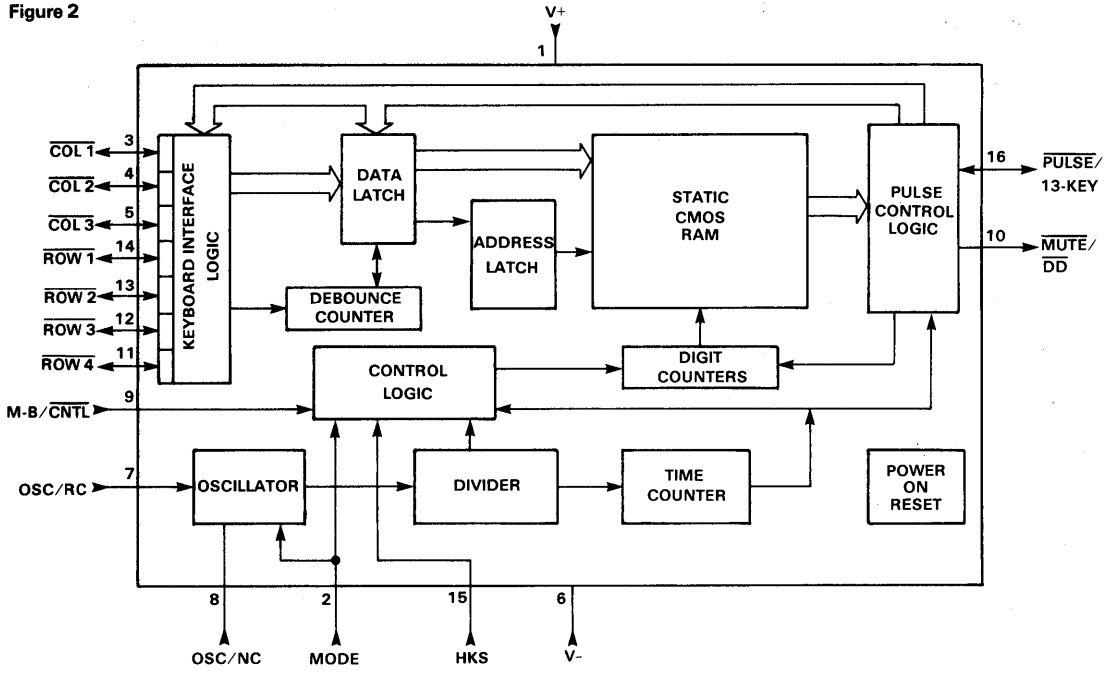
Pin 1 is the positive supply input to the part and is measured relative to V– (Pin 6). The voltage on this pin should not exceed 10 V. On-chip zener diodes will provide protection from supply transients in most applications.

MODE, Pin 2

The MK5175 will function in either Tone or Pulse mode, dependent upon the logic level presented to Pin 2. For Pulse mode operation, this pin must be tied to V– (Pin 6). For Tone mode, it should be tied to V+ (Pin 1). The interpretation of Pins 7, 8, 9, 10, and 16 are dependent upon the mode selected.

MK5175 BLOCK DIAGRAM

Figure 2



KEYBOARD INPUTS, Pins 3, 4, 5, 11, 12, 13, 14

The MK5175 incorporates an innovative keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 3.

A valid key entry is defined by either a single row being connected to a single column or V– being simultaneously presented to both a single row and column.

In the Tone mode, the MK5175 features a bidirectional keyboard scheme. In this scheme, as the MK5175 passively monitors the key inputs (using the scan provided by the tone dialer), they are debounced, decoded, and stored in the on-chip LND (Last Number Dialed) buffer. This does not affect the normal functioning of the tone generator, which begins signaling immediately. The repertory dialer will disable the tone generator and scan the keyboard whenever a command key entry is detected, as shown in Figure 5. The MK5175 simulates key closures so that a tone dialer will perform the repertory tone-dialing function.

In the Pulse mode, the MK5175 keyboard inputs are totally static until an initial valid key input is sensed. The oscillator is then enabled and the rows and columns are alternately scanned (pulled high, then low) to verify the input is valid. Keyboard bounce is ignored for 32 ms after the initial key down is detected. A key input is accepted if it is valid after this initial debounce time. This scheme allows any valid key input to be recognized in less than 40 ms after the initial key closure.

V–, Pin 6

Pin 6 is the power supply return pin and is the measurement reference for V+ (Pin 1).

OSCILLATOR, Pins 7, 8

In the Tone mode, only a resistor and a capacitor are needed to provide the frequency reference for the MK5175. The resistor should be connected from Pin 7 (Osc/RC) to V+ (Pin 1) and the capacitor from Pin 7 to V– (Pin 6). Pin 8 (Osc/NC) should be left open or connected to V+. A nominal frequency of 8 kHz will provide a tone rate of 100 ms on and 100 ms off (f_{OSCT} = 1/1.25 RC). This tone rate is directly proportional to the oscillator frequency.

In the Pulse mode, an accurate frequency reference is obtained using an on-chip inverter with sufficient gain to provide oscillation when used with a low-cost 480 kHz ceramic resonator (antiresonant mode). In addition to the resonator, two external capacitors are required, as shown in Figure 6.

M-B/$\overline{\text{CNTL}}$, Pin 9

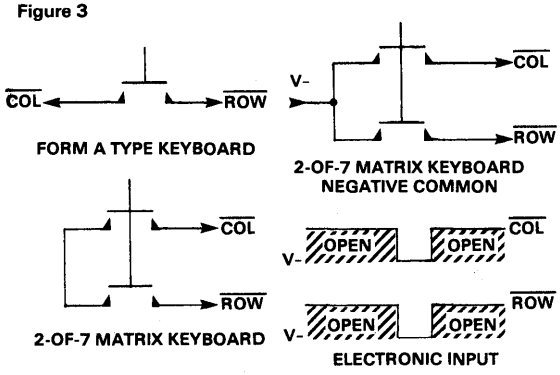
In the 13-key Tone mode, Pin 9 can be used as a $\overline{\text{Control}}$

input by connecting a control key (n.o. SPST switch) from this pin to V- (Pin 6). This feature allows the * and # key entries to be interpreted simply as DTMF signals. When not used as a key input, this pin should be connected to V+ (Pin 1). (See 13-Key Tone Mode)

In the Pulse mode, the make/break ratio may be selected by connecting this pin to either the V+ or V- supply. Table 1 indicates the two popular ratios from which the user can choose.

KEYBOARD CONFIGURATIONS

Figure 3



MAKE/BREAK RATIO SELECTION

Table 1

Input to Make/Break Pin	Pulse Output	
	MAKE	BREAK
V+ (Pin 1)	40%	60%
V- (Pin 6)	32%	68%

MUTE/DD, Pin 10

Pin 10 is the output of an open-drain N-channel transistor.

In the Tone mode, Pin 10 is used to provide the tone dialer with a Dialer-Disable signal. This signal is used to inhibit the generation of tones by pulling to V- when command entries are being made.

In the Pulse mode, Pin 10 is the Mute output. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output is shown in the application diagram in Figure 6. Figure 4 shows the timing characteristics of the Mute output.

HKS, Pin 15

Pin 15 is the hook switch input pin. Pin 15 requires an external pull-up resistor to the positive supply. A V+ input sets the circuit in its on-hook mode, while a V- input sets it in the off-hook or dialing mode.

PULSE/13-KEY, Pin 16

In the Tone mode, a V+ level at Pin 16 sets the MK5175 in a mode in which a control key (n.o. SPST) connected from CNTL (Pin 9) to V- is used to initiate control functions. With Pin 16 tied to V-, the MK5175 is set in the 12-key mode and the * and # keys are used in control functions.

In the Pulse mode, Pin 16 is the Pulse output. It consists of an open-drain N-channel transistor designed to drive an external transistor. These transistors are typically used to pulse the telephone line by controlling the loop current through the network, as shown in Figure 6. The timing characteristics of the Pulse output are shown in Figure 4.

STANDARD 12-KEY OPERATION

During normal dialing, each digit is stored in the LND (Last Number Dialed) buffer, location 0. The telephone number dialed can be left in this temporary LND buffer for later use or it can be copied into any of the other nine permanent memory locations.

STORAGE

Telephone numbers to be automatically dialed by the MK5175 may be entered into the LND buffer while either on-hook or off-hook. However, the MK5175 must be in the on-hook mode for a number to be copied into a permanent memory location. A number may be copied and stored by entering the key sequence * *, followed by the address (1-9) of the memory location in which the number is to be stored. This operation requires 300 ms before going off-hook or reinitiating the store function and does not change the data in the LND buffer. Information present in the LND buffer when new data is entered is replaced and cannot be recalled.

AUTOMATIC DIALING

The automatic dialing function is implemented by going off-hook and entering a *, followed by the address (1-9) of the desired telephone number. Dialing will begin with the release of the address key and can be interrupted by initiating a new redial command. The LND buffer will contain the information last entered. A key sequence of * 0 will cause the last number entered to be redialed. More than one number sequence may be automatically dialed from memory without returning on-hook.

PAUSE/CONTINUE COMMAND

The MK5175 has a feature which allows an indefinite pause to be programmed into the first 15 digits of a number sequence by entering a # key at the point in the sequence where a pause is desired. When the number is automatically dialed, the circuit will stop dialing when the pause is encountered. Any key entry, except for a * key, will cause the MK5175 to continue dialing the remainder of the number. If more than one pause was originally

programmed into the number sequence, a corresponding number of continue commands must be made in order for the number to be completely dialed.

The continue input will not be recognized until one IDP period following the signalling of the digit preceeding the pause. This is approximately 800 ms in Pulse mode and 100 ms in Tone mode.

NORMAL DIALING

When dialing manually in the Pulse mode, the key entry rate may exceed the dialing rate. The memory has a FIFO (first-in-first-out) architecture and any length number sequence may be dialed as long as the key entered is not more than 16 entries ahead of the digit being outpulsed.

In order to dial a * or # DTMF signal when in the 12-key Tone mode, the * or # key must be depressed twice consecutively. This will cause the MK5175 to enable the tone dialer to generate the corresponding tone. However, the MK5175 will not store a * or # as a DTMF signaling digit.

Examples:

1. On-Hook, enter 323-1000
   Then enter * * 5
   323-1000 is stored in location 5
   •
   •
   •
   Come off-hook
   Enter * 5
   323-1000 is automatically dialed

2. Off-Hook, dial 42 (PBX access code)
   While waiting for dial tone, enter #
   Dial 1-214-323-1000
   Busy/Hang up
   Enter * * 3
   (Number is stored in location 3)
   •
   •
   •
   Come off-hook
   Enter * 3
   42 is dialed
   Wait for dial tone
   Enter 3 (continue command)
   1-214-323-1000 is dialed

13-KEY TONE MODE

An extra feature available on the MK5175 is the ability to use the entire keyboard for normal signaling such that when any key is depressed once, including * and #, the proper DTMF signal is generated. This feature is activated by connecting Pin 16 to V+. In order to utilize this function, an extra control key (n.o. SPST) connected from Pin 9 (M-B/$\overline{\text{CNTL}}$) to V- is required.

All digit entries, except * and #, are stored in the LND buffer, as they are entered, whether off-hook or on-hook. However,the MK5175 must be in the on-hook mode for a number to be copied from the LND buffer into a permanent memory location. A number may be copied and stored into a permanent memory location by entering the key sequence C N (where C is the control key and N is the location, 1-9, in which the number is to be stored). An indefinite pause may be programmed into a number by entering a C # key sequence at the point desired.

In order to automatically dial a number in memory, the key sequence C N must be entered after going off-hook, where N is the address of the number to be dialed. Last-number redial is accomplished by dialing C 0. If a pause has been programmed into the number to be automatically dialed, the number will be dialed up to the point where a pause is encountered. Any key entry (except the C key) will cause the MK5175 to continue dialing the remainder of the number. If more than one pause was programmed into the number, a corresponding number of continue commands must be made in order for the number to be completely redialed.

Examples:

1. On-hook, enter 555-2525
   Enter C 5 (C is a control key)
   555-2525 is stored in location 5
   •
   •
   •
   Come off-hook
   Enter C 5
   555-2525 is automatically dialed

2. Off-hook, dial 9 (PBX access code)
   Enter C # (a pause is programmed in, with no tones emitted)
   Once dial tone is established
   Dial 1-214-323-1000
   Busy/Hang up
   Enter C 2
   (Number is stored in location 2)
   •
   •
   •
   Come off-hook
   Enter C 2
   9 is dialed
   Establish dial tone
   Enter 2 (continue command)
   1-214-323-1000 is dialed

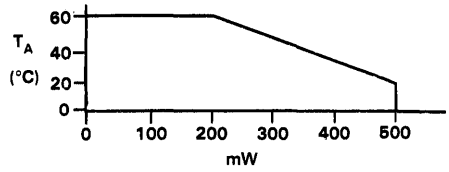
ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 10.5 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +85°C
Maximum Power Dissipation (25°C) ..... 500 mW
Maximum Voltage on any Pin ..... (V+) +0.3; (V-) -0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V+	DC Supply Voltage	2.0		10.0	V	
I_{SB}	DC Standby Current V+ = 2.5 V		1.0	2.0	μA	1
I_{OP}	DC Operating Current (Tone Mode) V+ = 2.5 V		50	100	μA	2
I_{OP}	DC Operating Current (Pulse Mode) V+ = 2.5 V		100	200	μA	2
I_{ML}	Mute Sink Current: V+ = 2.0 V, Vo = 0.5 V	0.5	2.0		mA	
I_P	Pulse Sink Current: V+ = 2.0 V, Vo = 0.5 V	1.0	4.0		mA	
I_{LKG}	Mute and Pulse Leakage: V+ = 10.0 V, Vo = 10.0 V		0.001	1.0	μA	
R_{KI}	Keyboard Contact Resistance			1.0	kΩ	
C_{KI}	Keyboard Capacitance			30	pF	
K_{IL}	"0" Logic Level	V-		20% of V+	V	
K_{IH}	"1" Logic Level	80% of V+		V+	V	
K_{RU}	Keyboard Pull-Up Resistance		100		kΩ	3
K_{RD}	Keyboard Pull-Down Resistance		0.5		kΩ	3
R_{CNTL}	CNTL Pull-Up Resistance		100		kΩ	

*Typical values are to be used as a design aid and are not subject to production testing.

NOTES:

1. All outputs unloaded. On-hook mode.
2. Current required for proper circuit function with a valid key input, off-hook or on-hook.
3. Keyboard to be scanned at 250 Hz when oscillator enabled Row and Column to alternately pull high and low.

AC CHARACTERISTICS (The timing Relationships are shown in Figures 4 and 5)

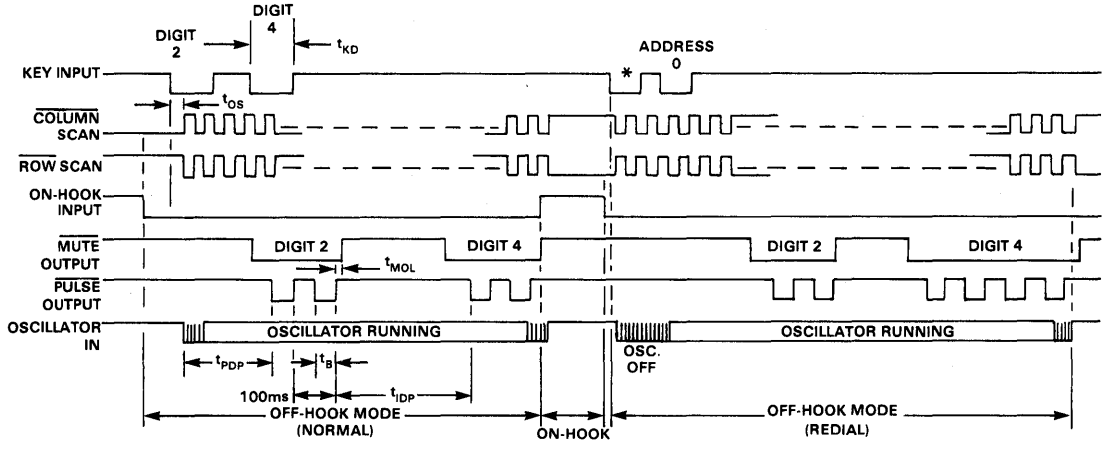
SYM	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
f_{OSCP}	Oscillator Frequency (antiresonant mode) (Pulse Mode)		480		kHz	1
t_{DB}	Keyboard Debounce Time		32		ms	2
t_{KD}	Valid Key Down Time	40			ms	
t_{OS}	Oscillator Start-Up Time			8.0	ms	
P_R	Pulse Rate (Pulse Mode)		10.0		pps	
t_B	Break Time: Pin 9 Tied to V+/Tied to V- (Pulse Mode)		60/68		ms	
t_{IDP}	Interdigital Pause (Pulse Mode)		840		ms	
f_{OSCT}	Oscillator Frequency (Tone Mode)		8.0		kHz	3
T_R	Tone Out Rate		$f_{OSCT}/1600$		tones/sec	3
t_{ROLL}	Rollover Overlap Time	4			ms	4
t_{MOL}	$\overline{\text{Mute}}$ Overlap Time		2		ms	
t_{PDP}	Predigital Pause		170		ms	

*Typical values are to be used as a design aid and are not subject to production testing.

NOTES:
1. Ceramic resonator should have the following equivalent values: $R < 20\ \Omega$, $R_A \geq 70\ k\Omega$, $Co \leq 500$ pF.
2. A key entry must be present after 32 ms to be valid (oscillator on).
3. $f_{OSCT} = 1/1.25\ R2C1$, nominal $f_{OSCT} = 8$ kHz, $200\ pF \leq C1 \leq 550$ pF.
4. Rollover is the period of time keyboard inputs must be invalid for successive entries to be recognized.

TIMING CHARACTERISTICS PULSE MODE

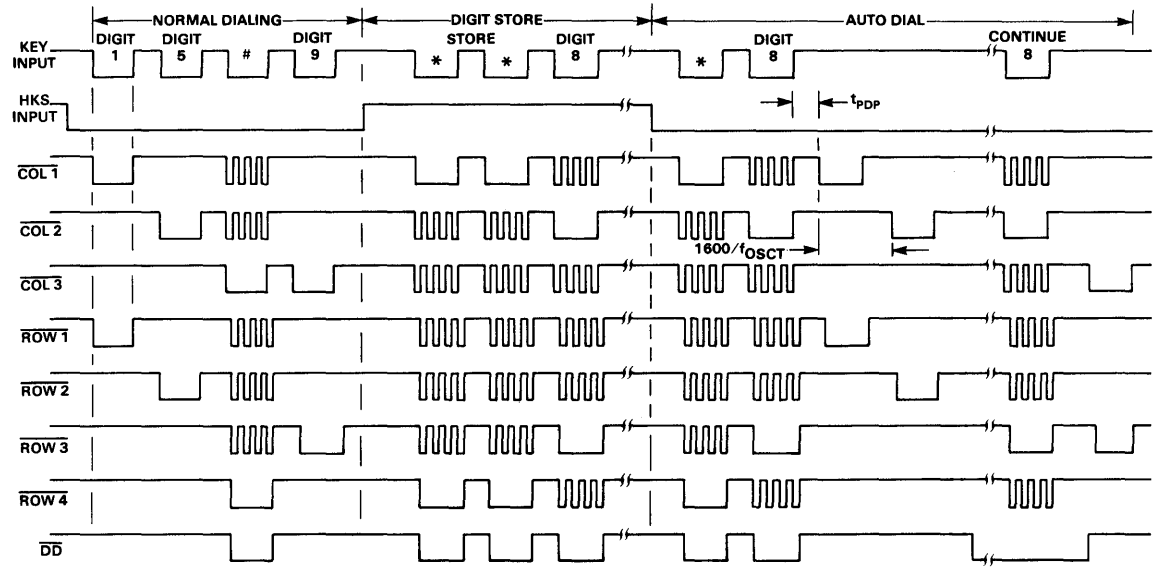
Figure 4



NOTE:
After the first key entry there is typically 100 ms prior to the time $\overline{\text{Mute}}$ becomes active.

TIMING CHARACTERISTICS TONE MODE (12 KEY)

Figure 5



NOTES:

1. Keyboard inputs are high impedance when not low or scanning.
2. Rows and columns are alternately pulled high and low for scanning.
3. After the address key is released there is typically 100 ms (t_{PDP}) before Row and Col information becomes active.

TYPICAL APPLICATIONS

REPERTORY PULSE DIALER

The schematic diagrams in Figures 6 and 7 show two methods which can be used to interface the MK5175 with the telephone line. In the approaches shown, the MK5175 is in the Pulse-dialer mode; the pulsing circuitry is shown in series (see Figure 6) and in parallel (see Figure 7) with the speech network.

A current source of some type is desired to present a high impedance to the telephone line while guaranteeing sufficient current to power the MK5175 while off-hook and dialing. The current source is constructed using current-regulator diode CR1 and diode D9. Other implementations, such as the the alternate current source shown in Figures 6 and 7, may be considered.

A diode bridge is used to insure the proper voltage polarity for the MK5175, and hook switch S1 is used to connect the circuit to the telephone line. VR1 provides transient protection for the circuit. Hook switch S2 is used to provide the logic necessary at Pin 15 to set the MK5175 in its off-hook mode.

Pin 2 (Mode) is connected to V- to set the MK5175 in the Pulse dialer mode. In this mode, Pins 7 and 8 are defined as the oscillator pins and Pins 9, 10, and 16 are defined as M-B, Mute, and Pulse, respectively.

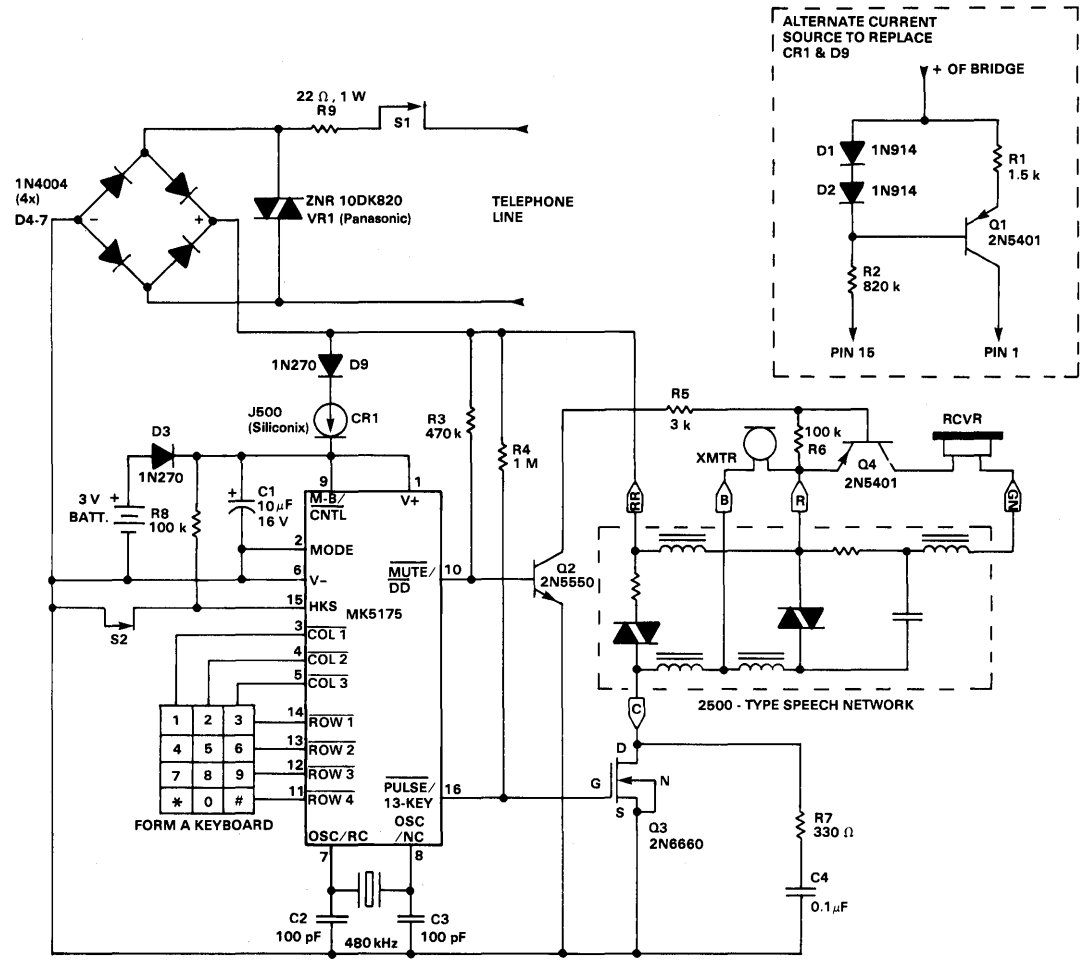
The Pulse and Mute outputs drive external transistors to perform the outpulsing function. In Figure 6 the receiver is connected to the speech network through transistor Q4. Mute causes the transistor to be held on until outpulsing begins. When Mute switches low, the receiver is removed from the network. The transients caused by breaking the line are then isolated from the receiver. The Pulse output drives transistor Q3 to make and break the line until the digit has been completely outpulsed. Mute then switches high, returning the receiver to the speech network.

In Figure 7 the speech network is connected to the telphone line through transistor Q3. Mute causes the transistor (Q3) to be held on until outpulsing begins. When Mute switches low, the speech network is removed from the telephone line, and the loop current is then maintained through resistors R5 (since diode D10 no longer holds transistors Q4 and Q5 off) until outpulsing begins. The Pulse output drives transistors Q4 and Q5 to make and break the line until the digit has been completely outpulsed.

A 3-V battery has been included in the circuits to provide power to the MK5175 to retain the numbers stored in memory and to provide the power necessary for the on-hook entry and/or storage of numbers. If the battery were to fail or be removed, the circuit would still function as a regular Pulse dialer with no memory.

TYPICAL APPLICATION PULSE MODE (SERIES PULSING)

Figure 6



NOTE:
Memory retention cannot be guaranteed if battery is not used.

REPERTORY TONE DIALER

In the application shown in Figure 8, tone mode operation of the MK5175 is selected by connecting Mode (Pin 2) to V+ (Pin 1). In the tone mode, only resistor R2 and capacitor C1 are needed to provide for the frequency reference for MK5175. The oscillator frequency is given by the following equation:

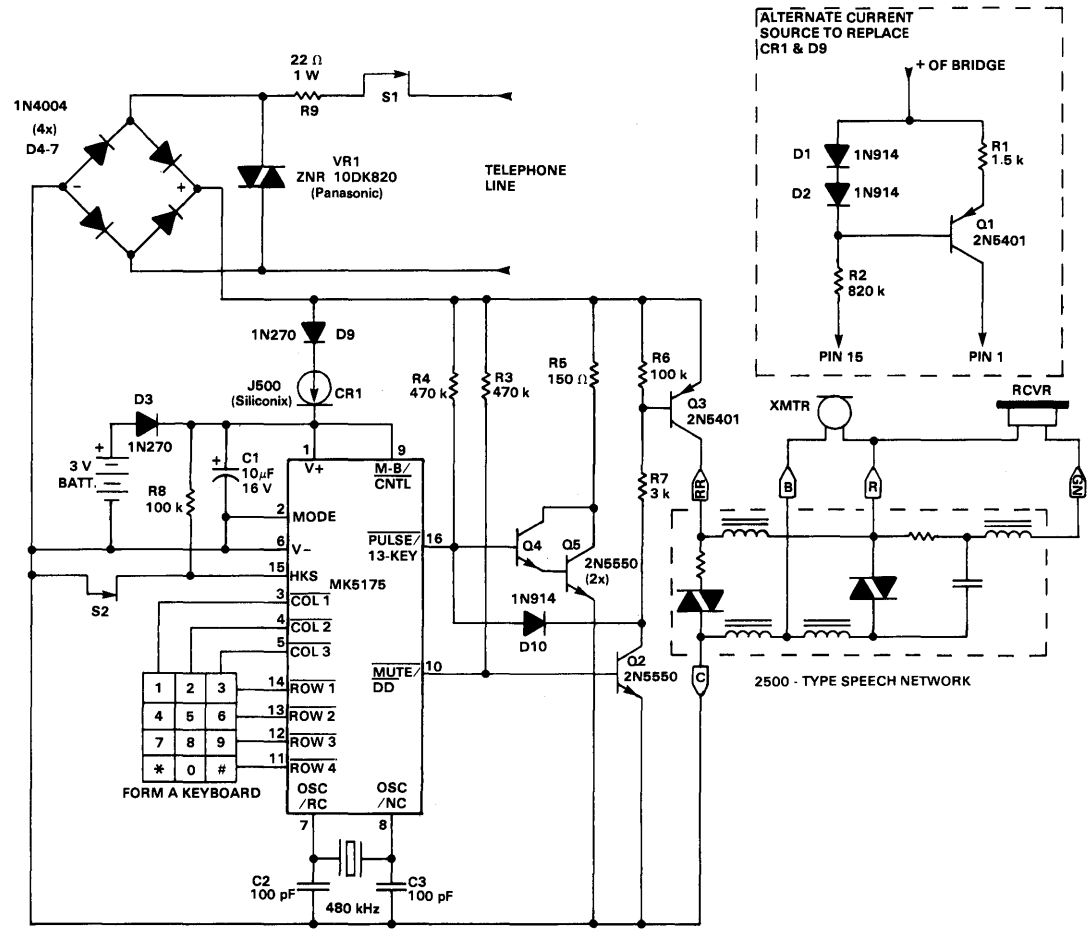
$$f_{OSCT} = 1/1.25\ R2\ C1$$

A nominal frequency of 8 kHz will provide a tone rate of 100 ms on and 100 ms off, when automatically dialing a number. This tone rate is directly proportional to the oscillator frequency.

In the tone mode, the MK5175 provides the user with the option of selecting whether the * and # keys or a 13th key (a control key) is used to initiate control functions. In this application, $\overline{\text{Pulse}}$/13-Key (Pin 16) is connected to V-(Pin 6), thus selecting the 12-key mode. Therefore, the * and # keys are used in control functions and must be depressed twice consecutively in order for their corresponding DTMF tones to be produced by the MK5380.

In the circuit shown in Figure 8, the MK5175 and MK5380 are powered directly from the telephone line. A 3 V battery provides power for on-hook operation and memory retention. (Without a battery, the circuit will function as a non-repertory dialer).

TYPICAL APPLICATION PULSE MODE (PARALLEL PULSING)
Figure 7



NOTE:
Memory retention cannot be guaranteed if battery is not used.

The MK5175, in the tone mode, features a bidirectional keyboard scheme that passively monitors key inputs and simulates key closures so that a tone dialer will perform the repertory tone-dialing function. Thus, the MK5175 and MK5380 keyboard inputs are connected together and share the same keyboard. The repertory dialer disables the tone dialer ($\overline{\text{Mute/DD}}$ (Pin 10 of the MK5175) pulls $\overline{\text{Chip Disable}}$ (Pin 2 of the MK5380) low) and scans the keyboard whenever a command entry is detected. To prevent the keyboard input circuitry of the MK5380 from interfering with the scanning process of the MK5175, the chip disable feature of the MK5380 was designed to place the MK5380 keyboard inputs in a high-impedance state when $\overline{\text{Chip Disable}}$ (Pin 2) is pulled low.

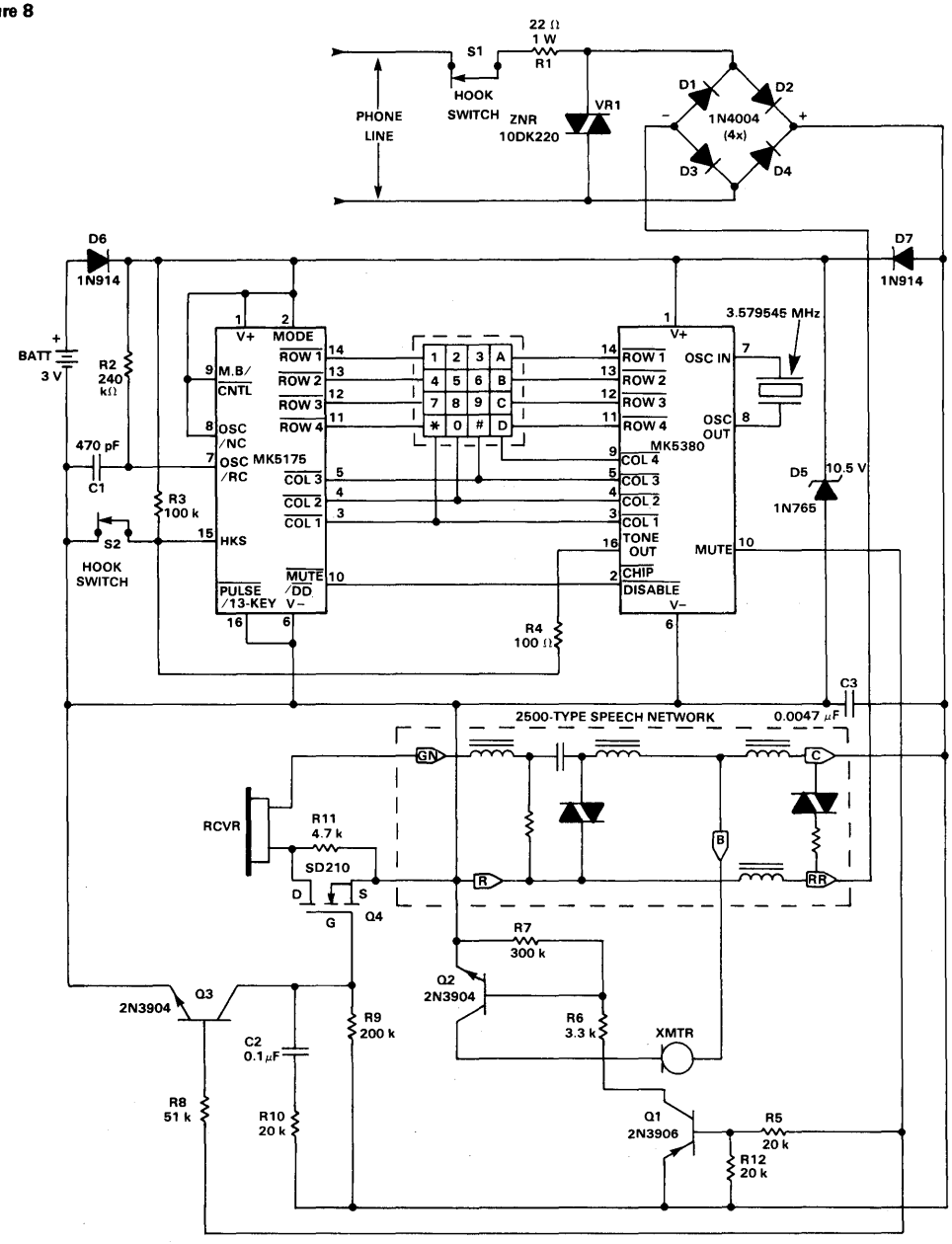
During keyboard entries to the MK5380 (from the keyboard, or the MK5175), the MK5380 Mute output (Pin 10) switches high, activating the switching circuitry (composed of transistors Q1-Q4, resistors R5-R11, and capacitor C2) to mute the receiver and disconnect the transmitter. The receiver is muted so that only a low level DTMF signal is provided to the user. The transmitter is disconnected to increase the dc resistance of the speech network to allow

for tone generation and to eliminate distortion of the DTMF signal due to noise present at the transmitter. The MK5380 produces tones on the telephone line by modulating the loop current through resistor R4 which is connected from Tone Out (Pin 16) to V- (Pin 6).

A diode bridge, composed of D1-D4, is used to protect the circuit from telephone line polarity reversals. A ZNR (VR1), a resistor (R1), a zener diode (D5), and a standard 2500-type speech network provide overvoltage and line-surge protection.

TYPICAL APPLICATION TONE MODE (12 KEY)

Figure 8



NOTE:
Memory retention cannot be guaranteed if battery is not used.

PRELIMINARY

TEN NUMBER REPERTORY DIALER WITH PACIFIER TONE MK5177(N), MK5176(N)

FEATURES

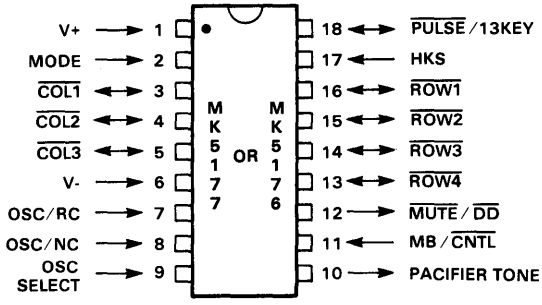
- Silicon Gate CMOS process for low-voltage (2 to 10 V) and low-power operation
- Low memory-retention current of 300 nA typical
- Auto-dials ten 16-digit numbers including Last Number Dialed (LND)
- Pacifier Tone Output
- Oscillator Selectable in pulse mode (RC or ceramic resonator)
- Stand-alone pulse dialer
- Interfaces with Mostek's tone dialers
- PABX pause key input
- Last number dialed memory
- Last number dialed may be copied into any one of nine other locations.
- Make/Break ratio is pin selectable in pulse mode
- Uses either the inexpensive Form-A type keyboard or the standard 2-of-7 matrix keyboard with common V-
- Optional use of 13th key input to control repertory functions in tone mode

DESCRIPTION

The MK5177 and MK5176 are monolithic, integrated, ten-number repertory dialers manufactured using Mostek's Silicon Gate CMOS process. The circuit accepts keyboard inputs and provides the pulse and mute logic levels required for loop-disconnect signaling. In addition, the MK5177/6 interfaces with the MK5380 or MK5389 tone generator circuits for DTMF signaling. The MK5177 is functionally similar to the MK5175 except for pins 9 and 10, which provide the additional features of Oscillator Select and Pacifier Tone Output. The MK5176 is the same as the MK5177, but has continuous mute timing on its Mute output (see Figure 5b).

PIN CONNECTION

Figure 1



Pin 2, the "Mode Select" input determines whether signaling will be pulse or tone. The interpretation of several inputs and outputs is dependent upon the mode selected.

In the pulse mode, the time base for the circuit is selectable between a ceramic resonator and an RC oscillator. In Tone mode, the circuit can use only the RC oscillator.

An on-chip RAM is capable of storing ten 16-digit telephone numbers, including the last number dialed. When used in a PABX system, a pause (# key) may be stored in the number sequence. The repertory dialer will recognize this pause when automatically dialing and stop until another key input is received.

The MK5177/6 repertory dialer uses a standardized pinout, shown in Figure 1, common to other Mostek tone and pulse dialers. This facilitates the design of a family of telephone products using common PC boards and circuit components. The block diagram in Figure 2 illustrates the general internal structure of the MK5177/6.

FUNCTIONAL DESCRIPTION

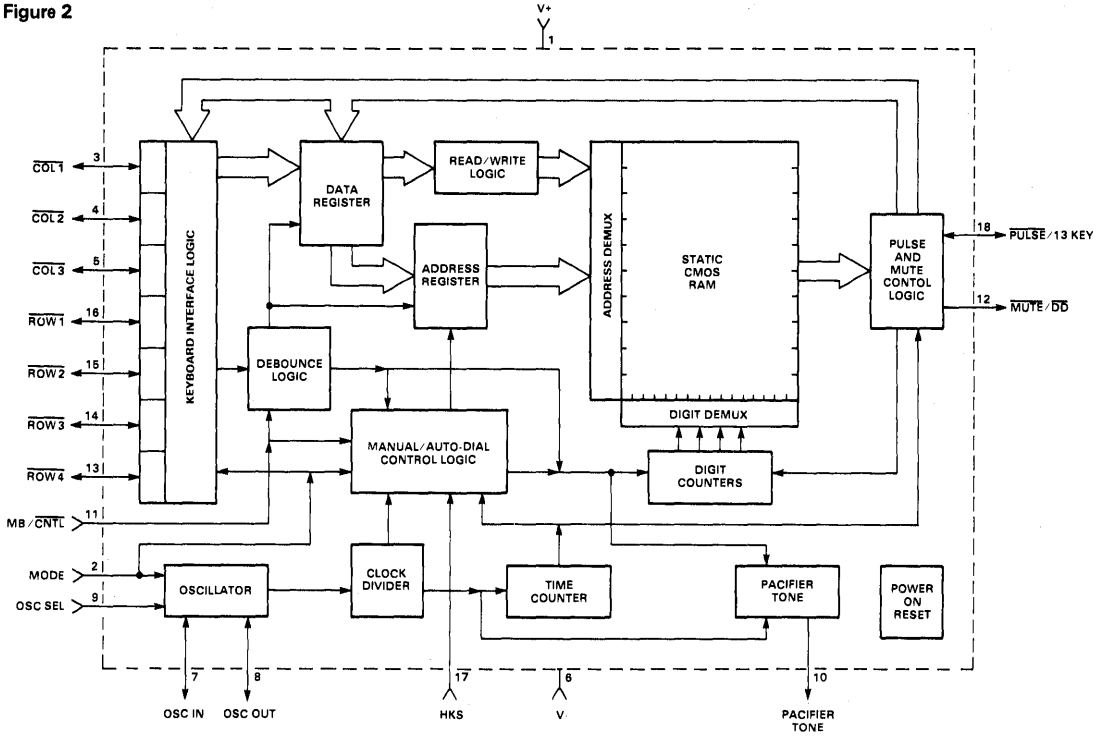
V+, Pin 1

Pin 1 is the positive supply input to the part and is measured relative to V- (Pin 6). The voltage on this pin should not exceed 10 volts. A low voltage detect circuit will perform a power-up initialization whenever the supply voltage at this pin falls below a level necessary to guarantee proper circuit operation.

XIV

MK5177/6 BLOCK DIAGRAM

Figure 2



MODE, Pin 2

The MK5177/6 will function in either tone or pulse mode, dependent upon the logic level presented to pin 2. For pulse mode operation, this pin must be tied to V- (pin 6). For tone mode, it should be tied to V+ (pin 1). The interpretation of pins 7, 8, 11, 12, and 18 is dependent upon the mode selected.

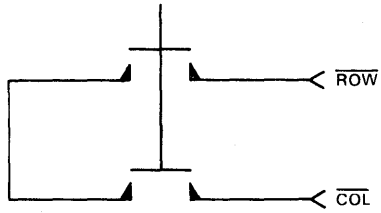
KEYBOARD INPUTS, Pins 3, 4, 5, 13, 14, 15, 16

The MK5177/6 incorporates a keyboard scheme that allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (Form A) keyboard to be used, as shown in Figure 3.

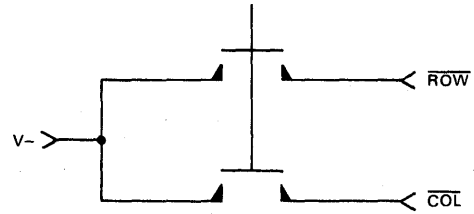
KEYBOARD CONFIGURATIONS

Figure 3

FORM A TYPE OF KEYBOARD



2 OF 7 MATRIX KEYBOARD



2-7 MATRIX KEYBOARD
NEGATIVE TRUE COMMON

A valid key entry is defined by either a single row being connected to a single column or by V- being simultaneously presented to both a single row and column.

In the tone mode, the MK5177/6 features a bidirectional keyboard scheme. As the MK5177/6 passively monitors the key inputs (using the scan provided by the tone dialer), they are debounced, decoded, and stored in the on-chip LND (Last Number Dialed) buffer. The keyboard inputs in tone mode normally have high impedance, allowing the tone chip to scan the keyboard lines and begin signaling immediately upon detecting a key entry. A command key entry disables the tone chip, and scanning is then controlled by the repertory dialer until the key is released. In tone mode, auto-dialing is performed by the MK5177/6, which simulates key-contact closures. The tone generator accepts these inputs as valid keyboard information and generates the proper DTMF frequencies.

In the pulse mode, the MK5177/6 keyboard inputs are static until an initial valid key input is sensed. The oscillator is then enabled, and the rows and columns are alternately scanned (pulled high, then low) to verify that the input is valid. Keyboard bounce is ignored for 32 ms after the initial key down is detected. A key input is accepted if it is valid after this initial debounce time. This scheme guarantees any valid key input to be recognized in less than 40 ms after the initial key closure.

V-, Pin 6

Pin 6 is the power supply return pin and is the reference for all input levels and the V+ supply (pin 1).

OSCILLATOR, Pins 7 and 8

The RC oscillator (Figure 4a) requires a resistor and capacitor to provide the frequency reference for the MK5177/6. The resistor should be connected from Pin 7 (Osc/RC) to pin 1 (V+) and the capacitor from Pin 7 to Pin 6 (V-). Pin 8 should be connected to V+ for normal operation. The nominal frequency for standard operation is 8 kHz. This provides for a tone rate of 100 ms on and 100 ms off and a pulse rate of 10 pps. The frequency of oscillation is approximated by the equation:

$$F_{OSC} = 1/(1.45\ RC).$$

The value suggested for the capacitor (C) should be 410 pF or lower, and resistor (R) may be adjusted for the desired signaling rate. 10 PPS and 5 TPS operation is achieved by selecting a 390 pF capacitor and a 220K Ohm resistor.

A more accurate and constant frequency reference in pulse mode is obtained using a 480 kHz ceramic resonator, as shown in Figure 4b. The ceramic resonator is connected in parallel with an on-chip inverter. Two external capacitors to ground also are required.

OSCILLATOR SELECT, Pin 9

This pin determines the mode of oscillation used by the repertory dialer when in pulse mode. The ceramic resonator is chosen by tying this pin to Pin 1 (V+). The RC oscillator is chosen by tying this pin to Pin 6 (V-).

In tone mode, this input must be tied either high or low; however, it will not affect the mode of oscillation, which is always RC. The timing of the repertory dialer is independent of the tone chip that uses a 3.5795 MHz crystal as its frequency reference.

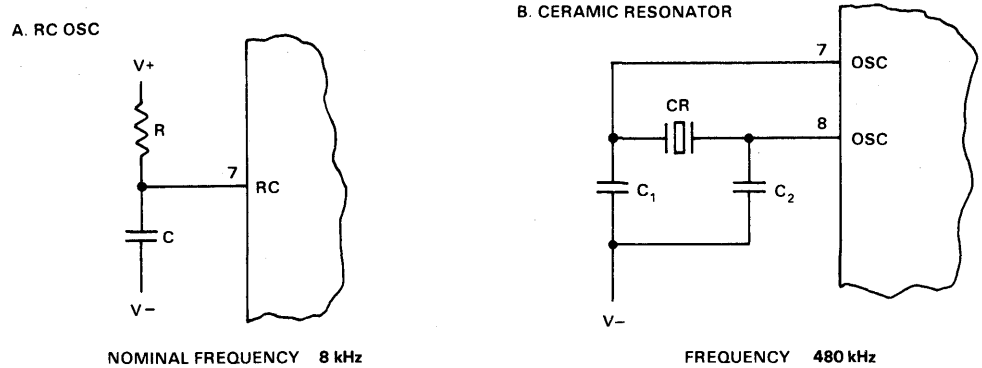
PACIFIER TONE, Pin 10

The pacifier tone consists of a burst of a 500-Hz square wave. The burst is initiated with the acceptance of a valid key input (following the debounce time) and terminates after 28 ms or with the release of the key, whichever comes first. The output has high impedance when not active.

MB/$\overline{\text{CNTL}}$, Pin 11

The level on pin 18 determines the control-key inputs required to implement the repertory-dialer function. In the

OSCILLATOR CONFIGURATIONS
Figure 4



XIV

13-key tone mode, pin 11 can be used to control the repertory-dialer functions of the phone with a momentary SPST switch to the negative supply connected to this input. This feature allows the basic keyboard to operate the same as in a standard telephone, and only the closure of the 13th key will initiate a repertory dialer function. The "*" and "#" key inputs will be accepted as normal DTMF inputs (however, they will not be stored in the LND buffer). In 12 key mode, this pin should be connected to the positive supply (V+).

In pulse mode, the make/break ratio may be selected by connecting this pin to either the V+ or V- supply. Table 1 indicates the two ratios available.

Table 1

MB Input	%Break	%Make
V+	60	40
V-	68	32

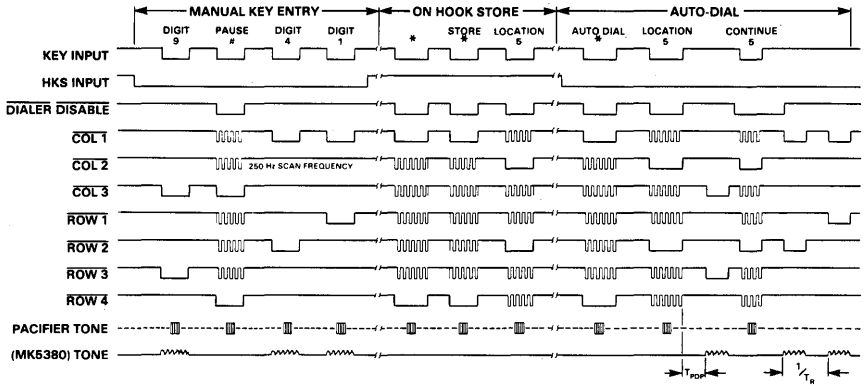
$\overline{\text{MUTE}}$/$\overline{\text{DIALER DISABLE}}$, Pin 12

Pin 12 is the output of an open-drain, N-channel transistor. In the tone mode, it is used to provide the tone dialer with a $\overline{\text{Dialer Disable}}$ signal which inhibits the generation of tones during command key entries. The timing characteristics in tone mode are shown in Figure 5a.

In the pulse mode, pin 12 is the $\overline{\text{Mute}}$ output. It provides the logic necessary to mute the receiver while the telephone line is being pulsed. A typical method of interfacing this output is shown in the application diagram in Figure 8. Figure 5b shows the timing characteristics of the Mute output for both the MK5177 and MK5176. The continuous

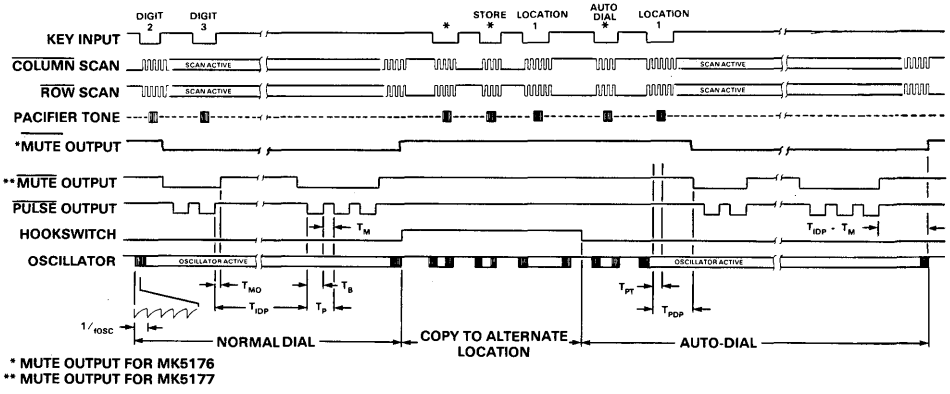
TONE MODE TIMING

Figure 5a



PULSE MODE TIMING

Figure 5b



* MUTE OUTPUT FOR MK5176
** MUTE OUTPUT FOR MK5177

Mute timing provided by the MK5176 is particularly useful in applications sensitive to noise generated during dialing, such as in cordless telephones.

HKS, Pin 17

The HKS (hook switch) input determines how the repertory dialer will handle key entries. When in the off-hook state (pin tied to V-), signaling is enabled, and all entries will be stored in the LND buffer. A control-key input in this state initiates the AUTO-DIAL function.

In the on-hook state (pin 17 tied to V+), the dialer stores key information in the LND buffer as they are entered but will not pulse out or allow the DTMF generator to tone. A control-key input is interpreted as a STORE command, causing the information present in the LND buffer to be copied into the indicated location.

A hook-switch transition terminates all dialer operations immediately and initializes all counters and latches. The dialer is then ready to accept a key entry which will be stored over previous data in the LND buffer.

$\overline{\text{PULSE}}$/13KEY, Pin 18

In the tone mode, a V+ level at pin 18 allows the MK5177/6 to accept inputs from a control key (n.o. SPST) connected from CNTL (Pin 11) to V-. It is used to initiate all repertory functions. This is referred to as 13-key tone mode. With Pin 18 tied to V-, the MK5177/6 is set in the 12-key tone mode, and the "*" and "#" keys are used in control functions. Pulse mode defaults to 12-key mode. Both 12- and 13-key tone modes are discussed in more detail in the Operations section of this data sheet.

In the pulse mode, Pin 18 is the $\overline{\text{Pulse}}$ output. It consists of an open-drain, N-channel transistor and provides the necessary timing for make, break, interdigital delay, and pulse rate to meet dialer specifications worldwide. The timing charcteristics of the Pulse output are shown in Figure 5b.

GENERAL OPERATION

During normal dialing, each digit is stored in the LND (Last Number Dialed) buffer, location 0. The telephone number dialed can be left in this temporary LND buffer for later use, or it can be copied into any of the other nine permanent memory locations (1-9).

The wrap-around feature of the buffer allows more than 16 digits to be dialed. Entries following the sixteenth input will be stored beginning with the first buffer location, replacing the information originally stored there. Any number of digits may be entered and dialed correctly. In pulse mode, the user should not get more than 15 entries ahead of the digit being pulsed.

Keys entered while auto-dialing in pulse mode will be ignored and not affect the number dialed. In tone mode, if a key is entered while auto-dialing, it will interfere with the keyboard outputs generated by the MK5177/6. The key entry is detected and auto-dialing is interrupted until the key is released. The keyboard entry generates a DTMF signal if valid.

The MK5177/6 repertory dialer will not store either a "*" or "#" entry in the buffer but will allow the tone generator to signal these digits as described below.

12-KEY OPERATION

NORMAL DIALING

In pulse mode, digits 0-9 will result in the pulsing of that digit at the standard rate of 10 pps. If the RC oscillator is utilized, this rate can be varied, achieving a pulse rate of up to 20 pps. The "*" and "#" keys enable the repertory functions listed below.

In tone-mode operation, digits 0-9 cause the generation of respective DTMF signal. In order to tone a "*" or "#" key, it must be entered twice. The second entry will generate the desired DTMF tone, although it will not be stored in memory.

STORAGE

Telephone numbers may be entered into the LND buffer while either on-hook or off-hook. However, the MK5177/6 must be in the on-hook mode for a number to be copied into a permanent memory location. The LND is copied by entering the key sequence "**", followed by the address (1-9) of the desired memory location. This operation requires 300 ms before going off-hook or initiating another store, and does not change the data in the LND buffer. Information present in the LND buffer when new data are entered is replaced and cannot be recalled.

The storage operation may be performed with the telephone off-hook. It requires the addition of an additional switch (Figure 7), providing an excellent "scratchpad memory". Numbers may be entered and copied without signaling the line, making use of line current rather than battery current. Scratchpad memory is useful whenever the user has a need to record a telephone number.

AUTOMATIC DIALING

The automatic dialing function is implemented by going off-hook and entering a "*", followed by the address (1-9) of the desired telephone number. Dialing will begin with the release of the address key and can be interrupted by initiating a new redial command or with a transition on the HKS pin. The LND buffer will contain the information last entered. A key sequence of "*" 0 will cause the last number entered to be redialed. More than one number sequence may be automatically dialed from memory without returning on-hook.

PAUSE/CONTINUE ENTRIES

The MK5177/6 has a feature that allows an indefinite pause to be programmed into the first 15 digits of a number sequence by entering a "#" key at the point in the sequence where a pause is desired. As the number is automatically dialed, the circuit will stop dialing when the pause is encountered. Any key entry, except for a "*" key, will cause the MK5177/6 to continue dialing the remainder of the number. If more than one pause was originally programmed into the number sequence, a corresponding number of "continue" commands must be made in order for the number to be completely dialed.

The "continue" input will not be recognized until one IDP period following the signaling of the digit preceding the pause. This is approximately 940 ms in pulse mode and 100 ms in tone mode.

13-KEY MODE OPERATION

NORMAL DIALING

An additional mode of operation (tone mode only) is the ability to use the entire keyboard for normal signaling such that when any key is depressed once, including "*" or "#", the proper DTMF signal is generated. This feature is activated by connecting Pin 18 to V+. The repertory-dialer functions are then initiated by an extra control key (n.o. SPST) connected from Pin 11 (MB/CNTL) to V-. This key will be referred to as "C".

STORAGE

The information in the LND buffer may be "copied" or stored into one of the nine permanent memory locations when the input to HKS is high. The control sequence for this function is C-N. The information will be copied, yet the LND buffer information will be left intact.

AUTOMATIC DIALING

Information stored in any of 10 memory locations may be autodialed by entering C-N when the input to HKS (pin 17) is low. Autodialing may be initiated immediately following a hookswitch transition or manual key entries, or after the completion of a previous auto-dial number.

PAUSE/CONTINUE

An indefinite pause may be inserted into the number sequence with a C-# entry. This feature is quite useful when dialing through a PABX. When a number sequence with a pause is autodialed, signaling will stop when the pause is reached and will continue only when a valid key input is detected.

EXAMPLES

I. Pulse and 12-Key Tone Mode

CALL FRIEND AT MOSTEK,
i) Off-hook, dial 42 (PBX access code), and # (PAUSE)
ii) Dial 1-214-466-1000.
ii) CALL COMPLETED, PARTY NOT IN.
iii) On-hook, enter * * 3 (stores number into permanent memory location 3)
SOME TIME LATER . . . AUTO-DIAL LOCATION 3.
iv) Off-hook, enter * 3, receive dial tone, enter 3 to continue.
NUMBER IS AUTO-DIALED, PARTY ANSWERS.

II. 13-Key Tone Mode

CALL "INFORMATION" TO GET THE NUMBER FOR MOSTEK'S MARKETING DEPARTMENT.
i) Off-hook dial 1-214-555-1212,
SET TELEPHONE TO "SCRATCHPAD"
ii) Enter 1-214-466-1241; the information is stored in the LND buffer.
HIT THE HOOKSWITCH; AUTO-DIAL MOSTEK
iii) Enter C-O, autodial of the LND buffer begins.
CALL COMPLETED, ORDER SOME MK5177 REPERTORY DIALERS FOR YOUR NEW TELEPHONE DESIGN.

FUNCTIONAL SUMMARY
Table 2

FUNCTION	13-KEY TONE	12-KEY TONE	PULSE
Store in permanent memory	▲ C N	▲ * * N	▲ * * N
Redial from memory	▼ C N	▼ * N	▼ * N
Enter PABX Pause	C #	#	#
Redial Last Number	▼ C O	▼ * O	▼ * O
Tone *	▼ *	▼ * *	-
Tone #	▼ #	▼ # #	-
C is a control-key entry			
N is a digit entry (0-9)			

▲ indicates HKS input is high
▼ indicates HKS input is low

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage, V+ ..... 10.5 Volts
Operating Temperature ..... -30°C to +60°C
Storage Temperature ..... -55°C to +125°C
Maximum Power Dissipation (25 C) ..... 500 mW
Maximum Voltage on Any Pin ..... (V+) +0.3, (V-) -0.3

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

SYM	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V+	DC Operating Voltage	2.0		10.0	Volts	1
I_{OP}	Operating Current (Tone)		50	100	μA	2
I_{OP}	Operating Current (Pulse)		100	200	μA	2
I_{SB}	Standby Current (V+ = 2.5 V)		1.0	2.0	μA	3
I_{MR}	Memory-Retention Current		0.3	1.0	μA	1
V_{MR}	Memory-Retention Voltage	1.5	1.3		V	1
I_{ML}	Mute-Sink Current	0.5	2.0		mA	4
I_P	Pulse-Sink Current	1.0	4.0		mA	4
I_{PT}	Pacifier Tone Source/Sink	200	500		μA	4
I_{LKG}	Mute And Pulse Leakage		.001	1.0	μA	5
R_{KI}	Key Contact Resistance			1.0	k-Ohms	6
C_{KI}	Keyboard Capacitance			30	pF	6
K_{IL}	"0" Logic Level	V–		0.2 V+	Volts	
K_{IH}	"1" Logic Level	0.8 V+		V+	Volts	
K_{RU}	Keyboard Pullup		100		k-Ohms	7
K_{RD}	Keyboard Pulldown		1.0		k-Ohms	7
R_{CNT}	CNT Pullup (pin 11)		100		k-Ohms	8

NOTES:
1. The memory will be retained at a lower voltage level than that required for circuit operation. If either I_{MR} or V_{MR} is maintained, the memory contents will not be cleared.
2. Operating current with a valid key input at 2.5 volts.
3. Standby current on-hook or off-hook with all inputs unloaded.
4. For V+ = 2.5, Sink V_O = 0.5 Volts, Source V_O = 2.0 volts.
5. Leakage with V+, V_O = 10.0 Volts
6. Keyboard contact resistance and parasitic capacitance, maximum values.
7. Keyboard I/O pins will scan 250 Hz with oscillator-enabled pulse mode and during $\overline{DD}$ in tone mode.
8. Tone mode only.

OPERATING CHARACTERISTICS (cont)

AC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
F_{CR}	Oscillator (Cer. Res.)		480		kHz	1
F_{RC}	Oscillator (RC)		8	16	kHz	2
$\triangle F_{RC}$	Oscillator Stability	-3%		+3%		3
T_{DB}	Debounce Time		32		ms	4
T_{KD}	Valid Key-Down Time	40			ms	
T_{OS}	Oscillator Start-Up Time			8	ms	
T_{ROL}	Key-Rollover OVLP Time	4			ms	5
P_R	Pulse Rate		10		PPS	
T_B	Break Time (pin 11 V+/V-)		60/68		ms	
T_{IDP}	Interdigital Pause Time		940		ms	
T_{PDP}	Predigital Pause Time		170		ms	6
T_{MOL}	Mute Overlap Time		2		ms	
T_R	Tone Rate		5		TPS	
T_{PT}	Pacifier-Tone-Burst Time		28		ms	7
F_{PT}	Pacifier-Tone Frequency		500		Hz	8

NOTES:
1. Ceramic Resonator should have the following equivalent values: R < 20 Ohms, R_A > 70k Ohms, C_O < 500 pF.
2. The RC values chosen determine frequency. The nominal frequency is 8 kHz. To accelerate dialing, the frequency may be increased to twice the nominal value. This would double signaling rate and halve most timing specifications.
3. Voltage range of 2.5 to 6.0 volts, over temperature, and unit-to-unit variations.
4. Key entry must be present after 32 ms to be valid.
5. Rollover is the time key inputs must be invalid for successive entries to be recognized.
6. Time from initial key input till first break or tone output.
7. Tone burst will terminate if key released before 28 ms.
8. This is a square-wave output.

*Typical values are not subject to production testing; typical timing values assume a nominal frequency reference of 8 KHz.

TYPICAL APPLICATIONS

PULSE/TONE SWITCHABLE APPLICATION

This application circuit, shown in Figure 6, allows the user to switch between tone and pulse modes with the use of a single SPDT switch. Standby current for the MK5177/6/MK5380 pair will typically be less than 1.5 μA when on-hook, during which time the circuit will be in tone mode. When on-hook, there is no real difference in functionality between tone and pulse mode. Current is supplied by the battery when on-hook and by the line when off-hook. Diode D6 serves to prevent current flow from the battery to the network or to the line. Diode D1 prevents charging of the battery and clipping of the generated tones. In tone-mode operation, the MK5380 should never be forcibly disabled or removed from the circuit, since initial detection of any key input depends upon the scan circuitry of the tone chip.

In pulse-mode operation, the MK5177/6/MK5380 pair is isolated from the line and pulsing transients by constant current diode Q1. The tone generator is always disabled in pulse mode (except for the on-hook state). In tone mode, Q1 is bypassed allowing the DTMF tone generator to modulate the line directly. The time base for the repertory dialer is an RC oscillator circuit using R8 and C2, and the frequency reference for the tone generator is supplied by a 3.5795 MHz crystal.

Common circuitry is used to mute the transmitter and receiver in both modes of operation. $\overline{\text{Mute}}$ (MK5177/6) removes the transmitter and receiver in pulse mode by cutting off Q3 and Q4 through D2. With these elements removed, pulsing is accomplished by switching Q6 on (MAKE) and off (BREAK). Pulsing through the network in this way is termed "series pulsing". $\overline{\text{Mute}}$ (MK5380) operates similarly in the tone mode; the CMOS logic level is

inverted through Q2, which provides base drive for Q3 and Q4. During $\overline{\text{Mute}}$, Q2 is off, thereby cutting off Q3 and Q4.

Also shown is a piezo resonator that is driven directly by the pacifier-tone output (MK5177/6). This resonator may be dedicated to the repertory dialer or shared with the ringer circuitry for increased economy.

TONE-ONLY APPLICATION

The tone-only application (Figure 7) is much like the switchable application (Figure 6), but since it is tone-only, it uses a minimum number of external components. It consists primarily of a standard tone-application circuit with some additional supply considerations.

The MK5177/6 repertory dialer shares the keyboard with the MK5380 and controls the activity of the tone chip through the keyboard and Dialer Disable. When on-hook, the load resistor on the tone output is connected to the supply to eliminate any sudden current flow from on-hook key entries.

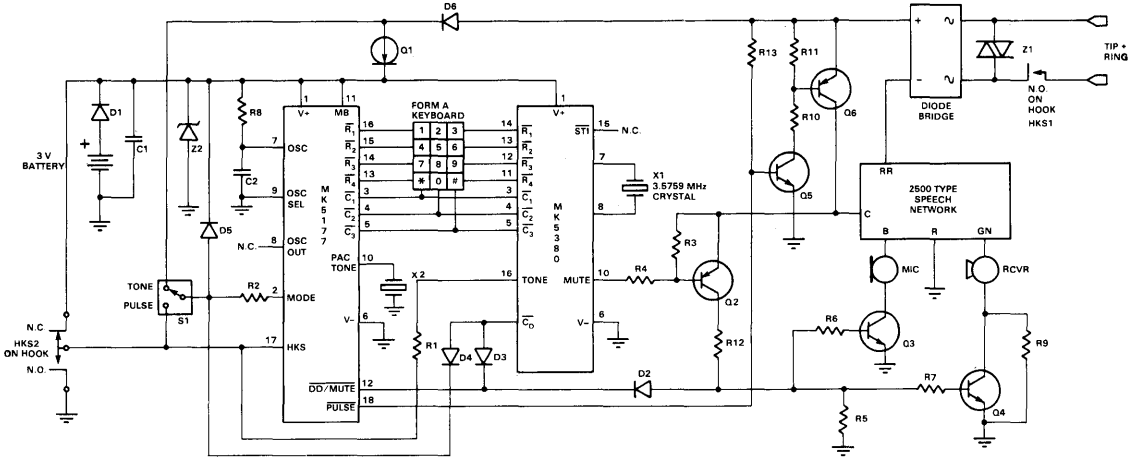
PULSE-ONLY

The application of the MK5177/6 repertory dialer in a pulse-only circuit is identical to that of the MK5175 (shown in the MK5175 data sheet), except for the ability of the MK5177/6 to use an RC oscillator. The RC oscillator not only costs less but provides a means to accelerate the signaling rate from 10 pps to 20 pps.

The application shown in Figure 8 uses parallel pulsing and illustrates how storage can be accomplished off-hook with the addition of a single programming switch. When switched to a program mode while off-hook, pulse signaling is inhibited, but numbers may be entered into the LND buffer and then stored into any of the nine permanent memory locations, providing a versatile "scratchpad" feature.

TONE - PULSE SWITCHABLE

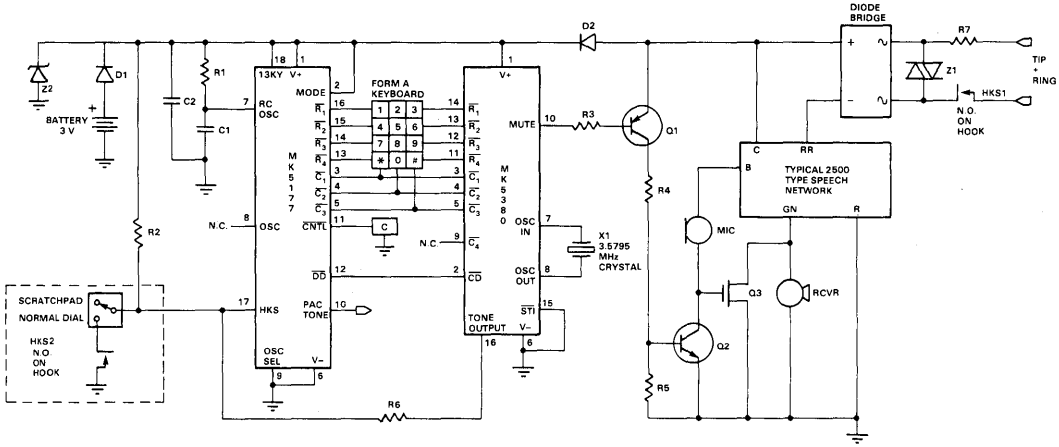
Figure 6



R1	100	R9	10K	D1-6	1N914
R2	390K	R10	10K	Q1	J500/CR022
R3	10K	R11	100K	Q2	2N5401
R4	51K	R12	10K	Q3	2N5550
R5	390K	R13	390K	Q4	2N5550
R6	20K	C1	.005 μF	Q5	2N5550
R7	20K	C2	390 pF	Q6	2N5550
R8	220K	Z1	10K220	Z2	1N753
				X2	Piezo Resonator

MK5177/6/MK5380 TONE MODE APPLICATION CIRCUIT

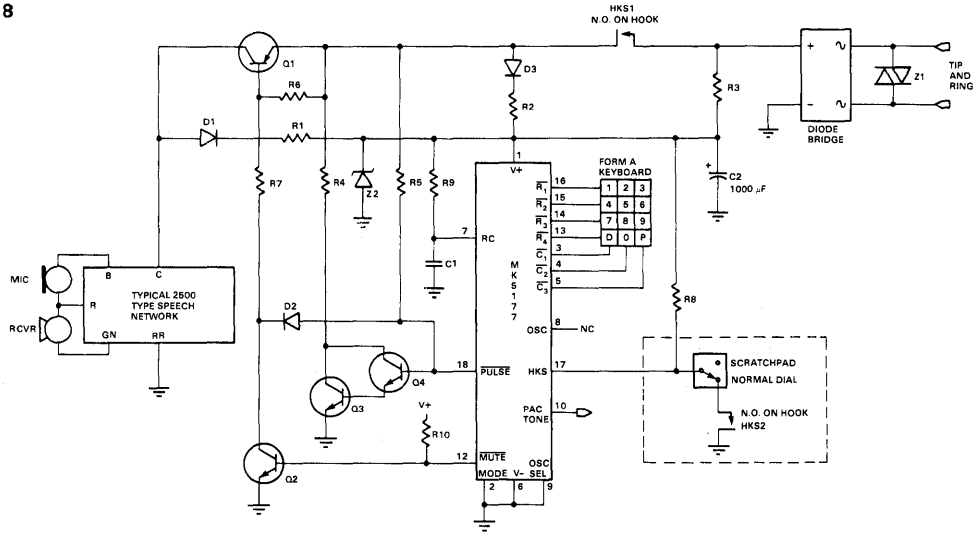
Figure 7



R1	220K	C1	390 pF	Z1	10K220
R2	390K	C2	.005 μF	Z2	1N753
R3	10K	D1	1N914		
R4	3.3K	D2	1N914		
R5	390K	Q1	2N5401		
R6	100	Q2	2N5550		
R7	22	Q3	2N6660		

MK5177/6 PARALLEL PULSE MODE — NO BATTERY

Figure 8



R1	10K	R9	220K	Q1	2N5401
R2	200K	R10	240K	Q2	2N5550
R3	2.2 M	C1	390 pF	Q3	2N5550
R4	150	C2	1000 μF	Q4	2N5550
R5	470K	D1-3	1N914		
R6	100K	Z1	10K820		
R7	3K	Z2	1N753		
R8	390K				

TARGET SPECIFICATION

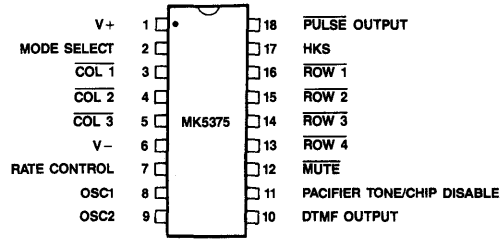
TEN-NUMBER REPERTORY TONE/PULSE DIALER MK5375

FEATURES

- ☐ CMOS Technology provides low-voltage operation
- ☐ Converts push-button inputs to both DTMF and loop-disconnect signals
- ☐ Stores ten 16-digit telephone numbers, including last number dialed
- ☐ Pacifier tone and PBX pause
- ☐ Last-number-dialed (LND) privacy
- ☐ Manual and auto-dialed digits may be cascaded
- ☐ Ability to store and dial both "*" and "#" DTMF signals
- ☐ Variable dialing rate
- ☐ On-chip power-up-clear guarantees data integrity

PIN CONNECTION

Figure 1



DESCRIPTION

The MK5375 is a monolithic, integrated circuit manufactured using Mostek's proprietary Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. It also allows for the storage of ten telephone numbers, including as many as 16 digits each, in on-chip memory.

The MK5375 accepts rapid keypad inputs (up to 25 key entries per second) and buffers these inputs in the FIFO (First-In-First-Out) LND (Last-Number-Dialed) register. Each digit entry is accompanied by a pacifier tone, which is activated after the digit has been debounced, decoded, and properly stored. Signaling occurs at a rate determined by externally connected components, allowing the dialing rate to be adjusted for any system.

The flexibility of the dialer makes possible a variety of applications, such as "scratchpad" number storage. In "scratchpad" applications, the MK5375 inhibits signaling during entry, without interrupting a conversation.

Privacy is also an important feature. The MK5375 allows the LND (Last-Number-Dialed) buffer to be cleared following a call, without affecting data stored in other permanent memory locations. The memory in the permanent locations may be easily protected from inadvertent key entries with the addition of a simple "memory lock" switch to the application.

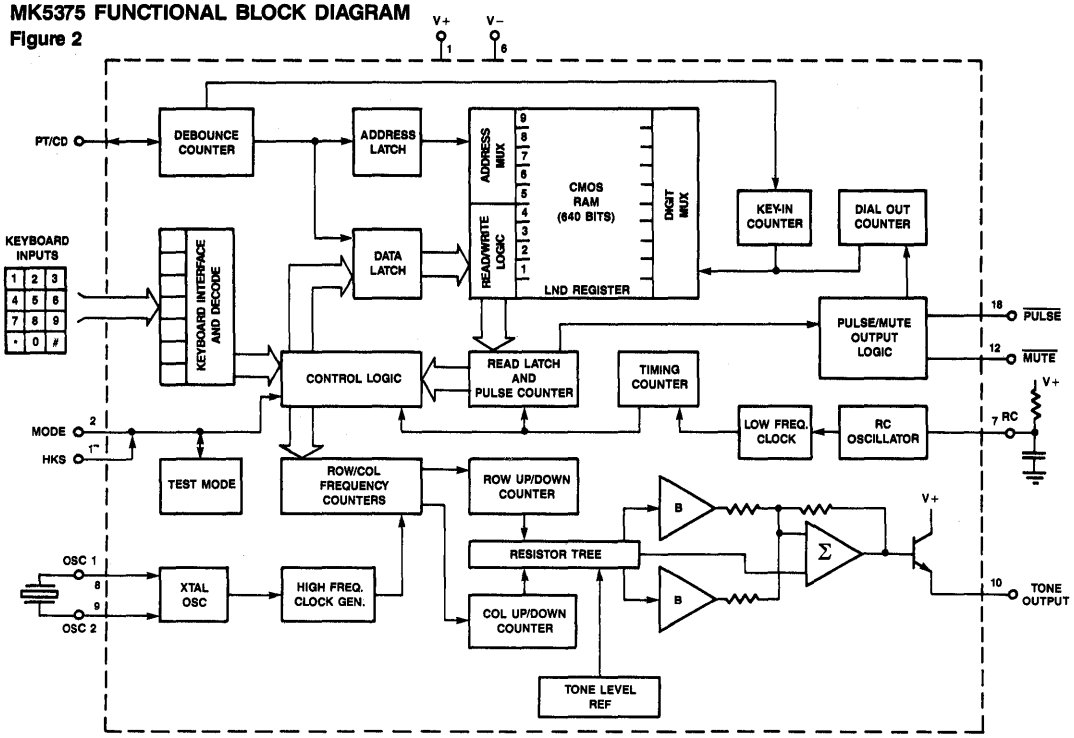
All of these options plus additional features are discussed in more detail in the following sections. The first section contains a brief detailed description of each pin function. The second section describes the device operation. This is followed by the DC and AC Electrical Specifications, and a few application suggestions.

FUNCTIONAL PIN DESCRIPTION

V+
(Pin 1)

Pin 1 is the positive supply for the circuit and must meet the maximum and minimum voltage requirements as stated in the electrical specifications.

MK5375 FUNCTIONAL BLOCK DIAGRAM
Figure 2



MODE SELECT
(Pin 2)

In normal operations, Pin 2 determines the signaling mode used; a logic level 1 (V+) selects Tone Mode operation, while a logic level 0 (V−) selects Pulse Mode operation. This input must be tied to one of the supplies to guarantee proper dialing. This pin can also be used to force the device into a test mode; this mode of operation is not suitable for normal dialing.

KEYBOARD INPUT: $\overline{COL1}$, $\overline{COL2}$, $\overline{COL3}$, $\overline{ROW4}$, $\overline{ROW3}$, $\overline{ROW2}$, $\overline{ROW1}$
(Pins 3,4,5,13,14,15,16)

The MK5375 keypad interface allows either the standard 2-of-7 keyboard with negative common or the inexpensive single-contact (FORM-A) keyboard to be used (Figure 3). A valid key entry is defined by either a single Row being connected to a single Column or by V− being presented to both a single Row and Column. In standby mode either all the rows will be a logic 1 (V+) and all the columns will be a logic 0 (V−), or vice versa.

The keyboard interface logic detects when an input is pulled low and enables the RC (Rate Control) oscillator and keypad scan. Scanning consists of alternately strobing the rows and columns high through on-chip pullups. After both valid row and column key closures have been detected, the debounce counter is enabled. Breaks in contact continuity (bouncing contacts, etc.) are ignored for a debounce period (T_{db}) of 32 ms. At this time the keypad is sampled, and if both row and column information is valid, this information is buffered into the LND location.

RATE CONTROL
(Pin 7)

The Rate Control input is a single-pin RC oscillator. An external resistor and capacitor determine the rate at which signaling occurs in both Tone and Pulse modes. An 8 kHz oscillation provides the nominal signaling rates of 10 PPS (Pulses per second) in Pulse Mode and 5 TPS (Tones per second) in Tone Mode; the Tone duty cycle is 98 ms on, 102 ms off. The RC values on this input can be adjusted to a maximum oscillation frequency of 16 kHz resulting in an effective Pulse rate of 20 PPS and a Tone rate of 10 TPS.

The frequency of oscillation is approximated by the following equation:

$$Fosc = 1/(1.49RC). \quad (1.0)$$

The value suggested for the capacitor (C) should be a maximum of 410 pF to guarantee the accuracy of the oscillator. The resistor is then selected for the desired signaling rate. Nominal frequency (8 kHz) is achieved with component values of 390 pF and 220 kohms. Parasites must be taken into account.

OSCIN, OSCOUT (Pins 8,9)

Pins 8 and 9 are the input and output, respectively, of an on-chip inverter with sufficient loop gain to oscillate when used in conjunction with a low-cost television color-burst crystal. The nominal crystal frequency is 3.579545 MHz, and any deviaton from this standard is directly reflected in the Tone Output frequencies.

This oscillator is under direct control of the repertory dialer and is enabled only when a tone signal is to be transmitted. During all other times it remains off, and the input has high impedance. The input OSCIN may be driven by an external source.

DTMF OUTPUT (Pin 10)

The DTMF Output pin is connected internally to the emitter of an NPN transistor, which has its collector tied to V+, as shown on the functional block diagram (Figure 2). The base of this transistor is the output of an on-chip operational amplifier that mixes the Row and Column Tones together.

The level of the DTMF Output is the sum of a single row frequency and a single column frequency. A typical single-tone sine wave is shown in Figure 4. This waveform is synthesized using a resistor tree with sinusoidally weighted taps.

The tone level of the MK5375 is a function of the supply voltage. The voltage to the device may be regulated to achieve the desired tone level, which is related to the supply by either of the following equations:

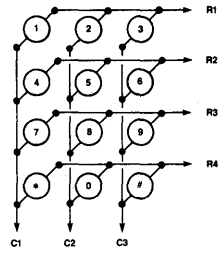
$$T(O) = 20 \text{ LOG } [(0.078V+)/0.775] \text{ dBm.} \quad (2.0)$$
$$T(O) = 0.085(V+) \text{ VRMS.} \quad (2.1)$$

PACIFIER TONE OUTPUT / CHIP DISABLE (Pin 11)

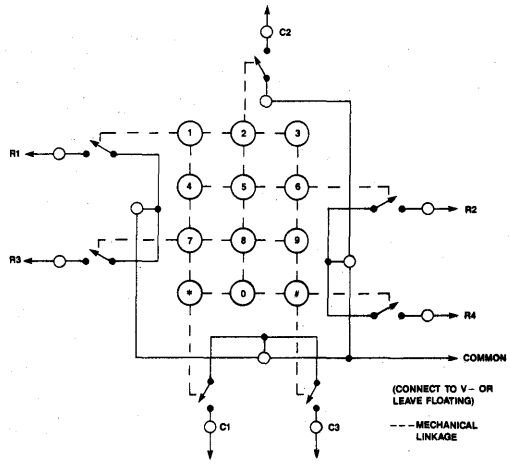
This pin normally has high impedance. Upon acceptance of a valid key input, and after the 32 ms debounce time, a 500 Hz square-wave will be output on this pin. The square-wave terminates after a maximum of 30 ms or when the valid key is no longer present. The purpose of this pacifier tone is to provide to the user audible feedback that a valid key has been entered. This feature is useful particularly for on-hook storage and pulse-mode signaling.

KEYPAD SCHEMATICS
Figure 3

3A. Calculator-Type Keypad

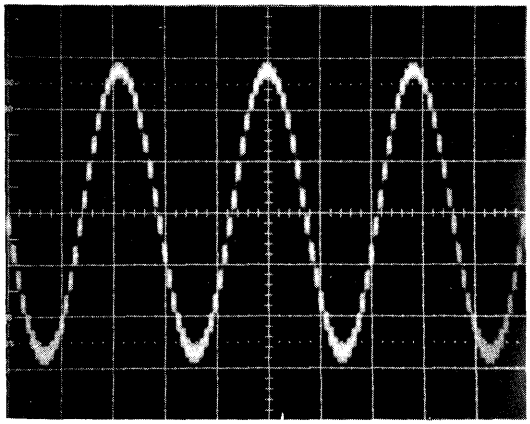


3B. Standard Telephone-Type Keypad

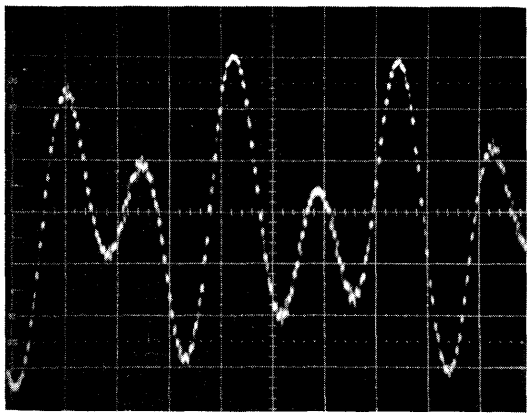


XIV

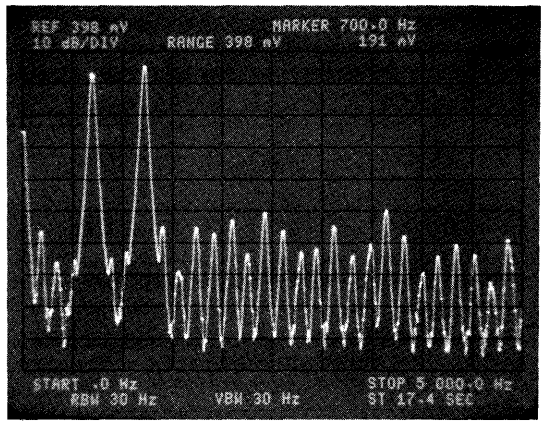
TYPICAL SINE WAVE OUTPUT - SINGLE TONE
Figure 4A



TYPICAL DUAL-TONE WAVEFORM (Row 1, Col 1)
Figure 4B



SPECTRAL ANALYSIS OF WAVEFORM IN FIG. 7
(Vert-10 dB/div. Horizontal - 600 Hz/div.)
Figure 4C



OUTPUT FREQUENCY
Table 1

KEY INPUT		STANDARD FREQUENCY	ACTUAL FREQUENCY	% DEVIATION
ROW	1	697	699.1	+0.31
	2	770	766.2	−0.49
	3	852	847.4	−0.54
	4	941	948.0	+0.74
COL	1	1209	1215.9	+0.57
	2	1336	1331.7	−0.32
	3	1477	1471.9	−0.35

The pacifier tone is not enabled when manually dialing in tone mode. This eliminates any confusion between the audible DTMF feedback and the pacifier tone, and prevents distortion of the DTMF signal by any of the pacifier tone frequency components. In both cases, the tone confirms that the key has been properly entered and accepted; whereas, without the tone, the user will not know if the keys have been properly entered.

IMPORTANT: This pin also serves as a chip-disable pin. Pulling this input high through a resistor will disable the keypad (high impedance) and initialize all counters and flip-flops (memory remains undisturbed). Pulling the input low through the same resistor enables the circuit. For the device to function properly, the resistor to V− (Pin 6) is required.

This feature is useful in several applications, as described in the application notes section.

MUTE OUTPUT
(Pin 12)

This pin is the Mute output for both Tone and Pulse modes of operation. The timing is dependent upon which mode is being used. The output consists of an open-drain, N-channel device. During standby, the output has high impedance and generally requires an external pullup resistor to the positive supply.

In Tone Mode, the Mute output is used to remove the transmitter and the receiver from the network during DTMF signaling. The output will mute continuously while auto-dialing and during manual DTMF signaling until each digit entered has been signaled.

In Pulse Mode of operation, the Mute output is used to remove the receiver or even the entire network from the line. These timing relationships are shown in Figure 5.

HKS INPUT
(Pin 17)

This pin is a high-impedance input and must be switched high for on-hook operation or low for off-hook operation. A transition on this input will cause the on-chip logic to initialize, terminating any operation in progress at the time. Signaling is inhibited while on-hook, but key inputs will be accepted and stored in the LND register. The information stored in the LND register may be copied into an alternate location only while on-hook. A logic level may be presented to this input, independent of the position of the hook-switch, allowing on-hook operations, such as storage, to be performed off-hook.

PULSE
(Pin 18)

This is an output driven by an open-drain, N-channel device. In Pulse Mode operation, the timing at this output meets Bell Telephone and EIA specifications for loop-disconnect signaling. The Make/Break ratio is set to 40/60 on the standard MK5375. The pulse rate is determined by the RC values selected for the Rate Control, Pin 7. Note: The standard make/break ratio may not be suitable if the Pulse dialing rate is accelerated.

DEVICE OPERATION

The MK5375 can be used in low-priced phones with basic 3×4 matrix keypads. The block diagram in Figure 2 shows the data and control signal flow between the various functional blocks. The keypad entries are decoded, debounced, and if valid, they are stored into the LND (Last-Number-Dialed) buffer, which acts much like a FIFO (First-In-First-Out) register. Each subsequent entry is stacked in the buffer. Typically, the dialing sequence begins 172 ms after the first digit is accepted in Pulse Mode operation and 132 ms in Tone Mode operation. Each digit buffered into the RAM is dialed out with a 98 ms burst of DTMF and an inter-signal time of 102 ms.

Buffering the data into the RAM prior to signaling is an important feature of the repertory dialer. It allows for the use of less expensive keypads, since the user cannot enter the digits too quickly for the system, and the pacifier tone can be used to provide audible feedback following each key entry not generating a DTMF signal. It also guarantees that the data stored in the RAM matches exactly the digits actually dialed.

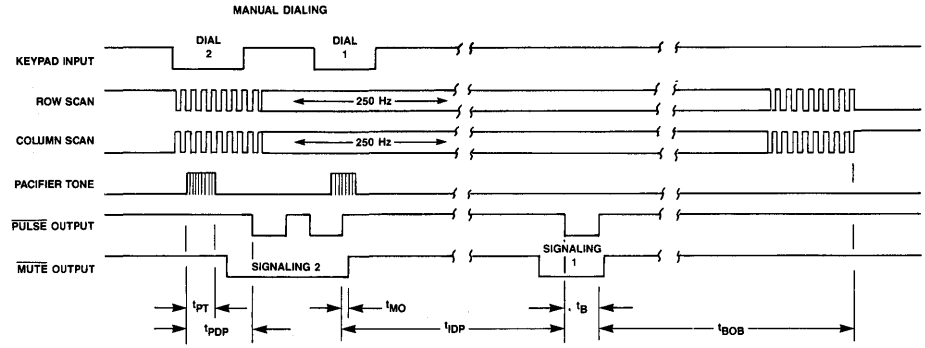
Manual dialing and auto-dialing can be executed in any order, consecutively or cascaded. The dialer must complete auto-dialing the previous entry before another key is entered. Digits should not be entered while the device is auto-dialing. Most digits would be ignored unless preceded by a control key; in which case, an error in dialing may occur.

KEYPAD CONFIGURATION
Figure 6

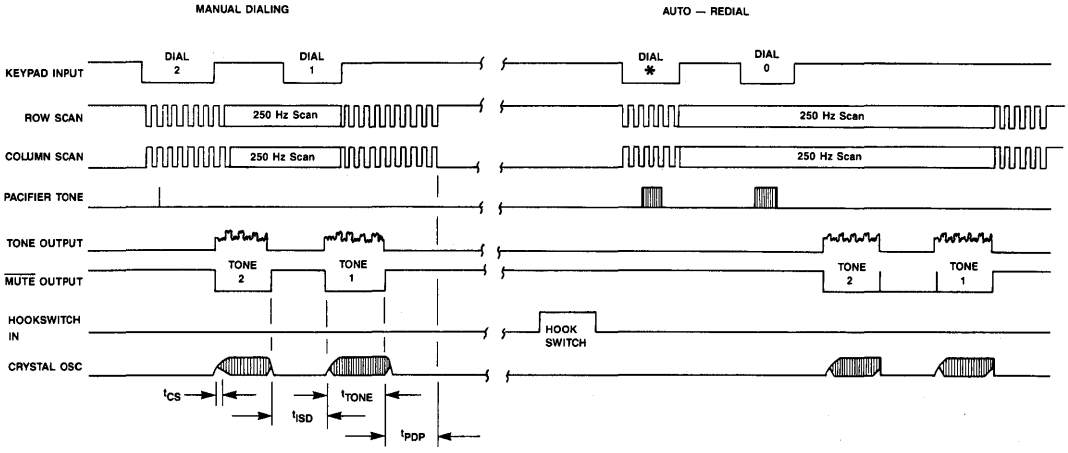
1	2	3
4	5	6
7	8	9
*	0	#

STORE DIAL LND PAUSE

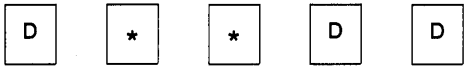
MK5375 TIMING DIAGRAM — PULSE MODE
OFF-HOOK OPERATION
Figure 5A



MK5375 TIMING DIAGRAM — TONE MODE
Figure 5B



NORMAL DIALING

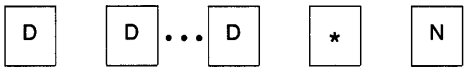


The "*" (STAR) key is used as the modifier to control repertory functions. All numeric keys will signal normally unless preceded by a modifier. To signal either a "*" or "#", these keys must be entered twice in succession. The first entry is not signaled or stored.

LND PRIVACY

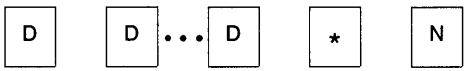
A single "*" input prior to going on-hook or prior to coming off-hook will erase the information stored in the LND buffer.

AUTO DIALING (Off-Hook)



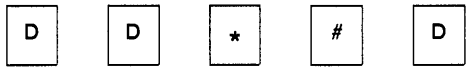
The key sequence "*", followed by any digit, will autodial the number sequence stored in the designated address location while off-hook.

STORAGE (On-Hook)



D is any data (telephone numbers) being entered or dialed. N is the address (memory location) in which numbers are stored. The number sequence stored in the LND buffer can be transferred to one of the other nine permanent locations with the simple sequence "*" followed by the address. New digits may be written into the LND buffer while on-hook. To enter either a "*" or "#" signal the digit must be entered twice in succession.

PABX PAUSE (Off-Hook and On-Hook)



An indefinite pause is stored in a number sequence by entering the "*" key modifier, followed by a "#" key input. When the number sequence is redialed, the dialer will pause when it encounters the "#" entry. A key input will cause it to continue.

PULSE DIALING

Most of the Pulse key operations are the same as they were in Tone Mode; PABX Pause is the only exception. In Pulse Mode, the pause may be stored as in tone mode, "* #", or with a single "#" input. Two "#" inputs will store two pauses.

The "*" key exercises the control function; two "*" inputs will be the same as a single input (multiple inputs are not accepted.)

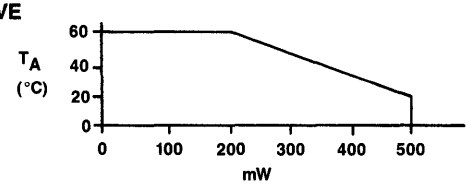
ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ . . . . . 6.5 Volts
Operating Temperature . . . . . −30°C to +60°C
Storage Temperature . . . . . −55°C to +85°C
Maximum Power Dissipation (25°C) . . . . . 500 mW
Maximum Voltage on any Pin . . . . . (V+) + 0.3; (V−) − 0.3 Volts

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

POWER DISSIPATION DERATING CURVE



DERATE AT 9 mW/°C WHEN SOLDERED INTO PC BOARD.

ELECTRICAL SPECIFICATIONS

DC CHARACTERISTICS

$-30°C \leq T_A \leq 60°C$

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
V+	DC Operating Voltage	2.5		6.0	V	
I_{SB}	Standby Current		0.3	1.0	μA	1
V_{MR}	Memory Retention Voltage	1.5	1.3		V	2
I_{MR}	Memory Retention Current	750	200		nA	2
I_T	Operating Current (Tone)		0.5	1.0	mA	3
I_P	Operating Current (Pulse)		50	150	μA	3
I_{ML}	Mute Output Sink Current	1.0	3.0		mA	4
I_{PL}	Pulse Output Sink Current	1.0	3.0		mA	4
I_{PC}	Pacifier Tone Sink/Source	250	500		μA	5
K_{RU}	Keypad Pullup Resistance		100		kOHMS	
K_{RD}	Keypad Pulldown Resistance		500		OHMS	

NOTES:

(All specifications are for 2.5 volt operation, unless otherwise stated. Typical values are representative values at room temperature and are not tested or guaranteed parameters.)

1. All inputs unloaded, Quiescent Mode (Oscillator off)
2. Meeting these minimum supply requirements will guarantee the retention of data stored in memory.
3. All outputs unloaded, single key input
4. V_{OUT}=0.5 Volts
5. Sink current for V_{OUT}=0.5; source current for V_{OUT}=2.0 VOLTS

AC CHARACTERISTICS -- KEYPAD INPUTS, PACIFIER TONE

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
T_{KD}	Keypad Debounce Time		32		mSEC	1
F_{KS}	Keypad Scan Frequency		250		Hz	1
T_{RL}	Two Key Rollover Time		4		mSEC	1
F_{PT}	Frequency Pacifier Tone		500		Hz	1
T_{PT}	Pacifier Tone		30		mSEC	1
F_{RC}	Frequency RC Oscillator	−5.0	±2.5	+5.0	%	2

NOTES:

1. Times based upon 8 kHz RC input for Rate Control
2. Deviation of oscillator frequency takes into account all voltage (2.5 to 6.0 volts), temperature (−30° to +60°C), and unit-to-unit variations. The tolerance of the external RC components or parasitic capacitance is not included.

AC CHARACTERISTICS -- TONE MODE

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
T_{NK}	Tone Output No Key Down			−80	dBm	1
T_O	Tone Output	−13 173	−12 194	−11 218	dBm mV (RMS)	1
PE	Pre-emphasis, High Band		2.7		dB	1
V_{DC}	Average DC Bias Tone Out		1.7		VOLTS	
DIS	Output Distortion		5.0	8.0	%	1
TR	Tone Signaling Rate		5	10	1/SEC	2
PSD	Pre-signal Delay		132		mSEC	2
ISD	Inter-signal Delay		100		mSEC	2

NOTES:
1. Load = 10 kΩ
2. These values are directly related to the RC input to Pin 7, nominally 8 kHz.

AC CHARACTERISTICS -- PULSE MODE OPERATION

SYM	CHARACTERISTIC	MIN	TYP	MAX	UNIT	NOTES
P_R	Pulse Rate		10		PPS	1
PDP	Predigital Pause		172		mSEC	1
IDP	Interdigital Pause		940		mSEC	1
T_{MO}	Mute Overlap Time		2		mSEC	1

NOTES:
1. Typical times assume nominal RC input frequency of 8 kHz. An increase in frequency results in an equal decrease in time values and an equal increase in rate values.

APPLICATION CIRCUIT

The MK5375 integrated circuit provides the ability to convert keypad inputs into either DTMF or loop-disconnect signals compatible with most telephone systems. Both modes of signaling utilize loop currents to transmit the desired signaling information to the central office.

The circuit schematic in Figure 7 illustrates a typical implementation of the MK5375 dialer IC along with the necessary components required to interface with the telephone line in a tone/pulse application.

In loop-disconnect signaling, each digit dialed consists of a series of momentary interruptions of loop current called "breaks" (i.e., a digit "1" consists of a single break, a digit "2" consists of two breaks, and so on. The Pulse output is dedicated to loop-disconnect signaling and controls the flow of loop current through the speech network switching transistors, Q4 and Q5. The Mute output, through transistors Q2 and Q3, removes the receiver and transmitter to eliminate loud pops in the receiver caused by switching current through the network. The Pulse and Mute output signals, as shown in Figure 5A, consist of make, break, and interdigital time intervals.

DTMF signaling requires that the loop current be modulated, producing an analog signal on the telephone line. Transistor Q1 modulates the loop current by amplifying the DTMF signal coupled to its base from the Tone Output. The Mute output removes the receiver and transmitter by switching transistors Q2 and Q3. This eliminates any interference with the DTMF signal from the transmitter and cuts down on the amplitude of the DTMF tone heard at the receiver. The timing diagram in Figure 5B illustrates the time relationship between key entries, Tone Output, and -Mute-Output.

The voltage regulator circuit comprising resistor R2, zener diode Z2, and transistor Q6 serves several purposes. In tone mode operation, it provides the regulated supply voltage to the MK5375 which determines the DTMF signal amplitude at the Tone Output. Varying the supply voltage will vary the DTMF output signal. In pulse mode, it helps provide some isolation from the transients caused by switching the speech network in and out.

During normal off-hook dialing, the MK5375 operates

using current from the telephone line. On-hook number storage and memory retention current are supplied by the battery shown in Figure 7. Transistor Q6 prevents the flow of battery current to the speech network.

The rate at which dialing occurs is determined by the values chosen for resistor R1 and capacitor C1. These values can be predetermined using equation (1.0) described above. The 3.5795 MHz crystal is used as a reference for synthesizing the DTMF signals and is activated only for the short periods during which these tones are being generated.

The application circuit schematic in Figure 8 gives an example of the various features which can be utilized with the addition of several switches. The example also shows that multiple devices may be used to increase the effective storage capability of the telephone design.

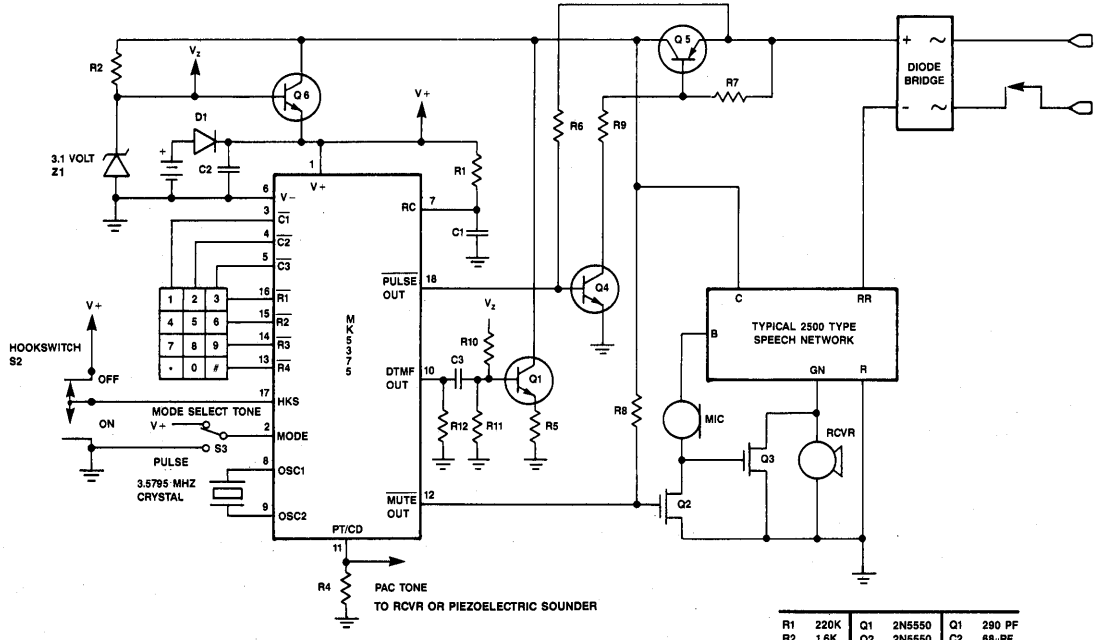
Much of the circuitry used to modulate and pulse the line, mute the speech network, and regulate the supply voltage is unchanged from the basic tone/pulse switchable telephone described above.

The two devices in Figure 8 are hooked up in parallel with one another except for their oscillator pins and the Chip Disable inputs. A DPDT switch is used to select between the two dialers through the Chip Disable pin; one device is activated while the other is put on standby.

Some applications may include a memory lock switch to prevent any of the data stored to be changed inadvertently. This memory lock switch can take the form of a locking key switch, which would allow only the person with the key to alter data stored in memory.

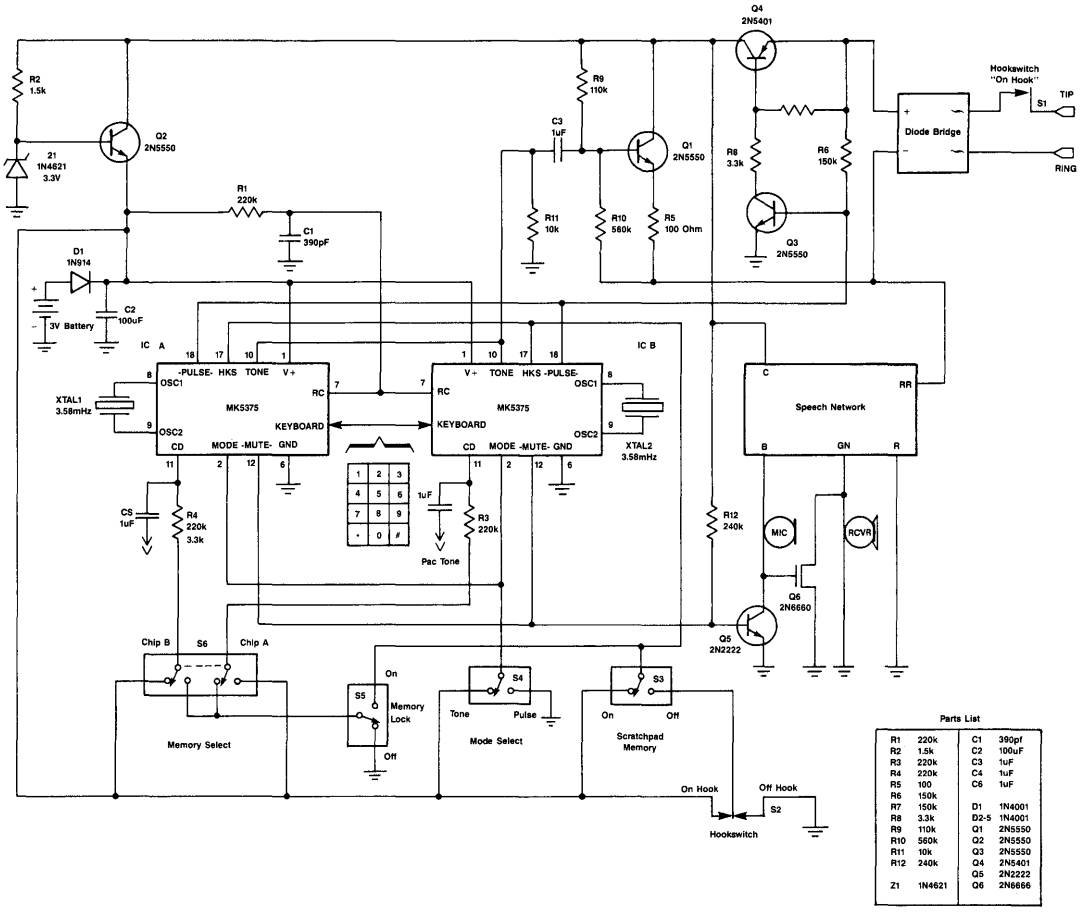
A scratchpad feature may be implemented to allow off-hook programming of the memory while inhibiting dialing. A switch is added in series with the telephone hookswitch to allow the dialer to be forced into its on-hook key entry mode while the telephone set is off-hook.

MK5375 CIRCUIT SCHEMATIC
Figure 7



R1	220K	Q1	2N5550	Q1	290 PF
R2	1.6K	Q2	2N5550	C2	68μPF
		Q2	2N6660	C3	1μF
R4	220K	Q3	2N6800	BATTERY 3 VOLT CELL	
R5	1000	Q5	2N5401	BRIDGE	
R6	160K	Q6	2N5550		
R7	150K	D1	1N914		
R8	240K	Z1	1N4619		
R9	3.3K				
R10	110K				
R11	560K				
R12	10K				

MK5375 APPLICATION CIRCUIT SCHEMATIC
Figure 8



Parts List

R1	220k	C1	390pf
R2	1.5k	C2	100uF
R3	220k	C3	1uF
R4	220k	C4	1uF
R5	100	C6	1uF
R6	150k		
R7	150k	D1	1N4001
R8	3.3k	D2-5	1N4001
R9	110k	Q1	2N5550
R10	560k	Q2	2N5550
R11	10k	Q3	2N5550
R12	240k	Q4	2N5401
		Q5	2N2222
Z1	1N4621	Q6	2N6666

XIV

ADVANCE INFORMATION

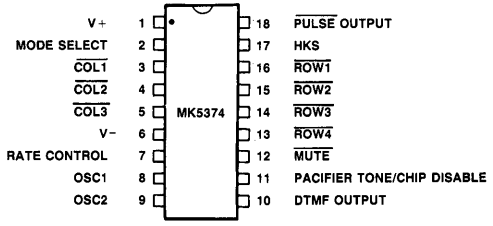
10 NUMBER REPERTORY TONE/ PULSE DIALER MK5374/MK5376

FEATURES

- ☐ Converts push-button inputs to both DTMF and pulse signals
- ☐ Stores ten 16-digit telephone numbers including last number dialed
- ☐ Pacifier tone and PBX pause
- ☐ Last number dialed (LND) privacy
- ☐ Manual and auto-dialed digits may be cascaded
- ☐ Ability to store and dial both * and # DTMF signals

PIN CONNECTION

Figure 1

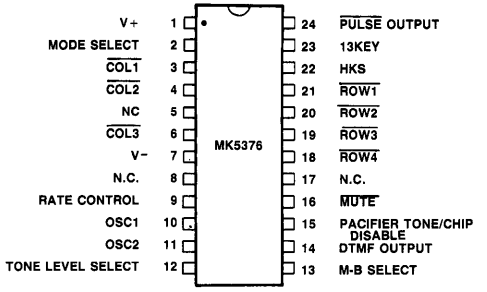


DESCRIPTION

The MK5374 is a monolithic, integrated circuit manufactured using Mostek's Silicon Gate CMOS process. This circuit provides the necessary signals for either DTMF or loop disconnect dialing. Ten telephone numbers of up to 16 digits each may be stored in the on-chip RAM. Manual and auto-dialed numbers may be cascaded in any order.

PIN CONNECTION

Figure 2



Additional functions available are a Pacifier Tone output, PABX pause, external control of the signaling rate, and total functional control with either a standard 3x4 matrix keypad (FORM-A) or a 2 of 7 keyboard. A 13th key option, available only on the MK5376, allows control of the dialer's repertory features. The telephone keypad then functions for signaling purposes only, independent of the repertory functions. This feature is important for users unfamiliar with the MK5376 special features.

The dialer's flexibility provides for many applications, for example, off-hook programming, the use of additional chips in parallel for 10, 20, and 30 number repertory phones, and permanent memory protection.

The dialer is available in two standard package sizes, an 18-pin (MK5374) and a 24-pin (MK5376) version. The MK5376 adds more flexibility to the basic MK5374 repertory dialer, making it suitable for a broader range of applications. The extra pins allow control of the tone level, choosing between a supply-independent tone level and one that is supply dependent. In addition, the 13th key mode available in the M-B (Make/Break) Ratio is user selectable.

ADVANCE INFORMATION

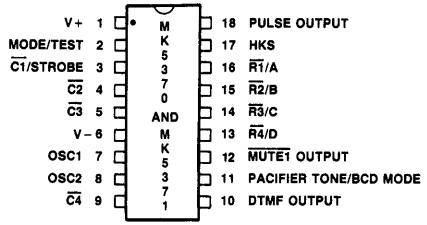
SINGLE NUMBER PULSE TONE SWITCHABLE DIALER MK5370/MK5371/MK5372

FEATURES

- ☐ Stand-alone DTMF and pulse signaling
- ☐ Softswitch automatically switches signaling mode
- ☐ Recall of last number dialed (up to 28 digits long)
- ☐ Flash key input initiates timed hook flash
- ☐ Microprocessor interface (BCD inputs) for smart telephones
- ☐ Timed PABX pause
- ☐ 10/20 PPS select option
- ☐ Form-A and 2-of-8 keyboard interface
- ☐ Pacifier tone
- ☐ Powered from telephone line, low operating voltage for long loop applications

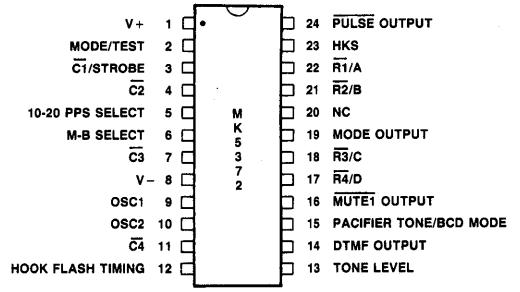
PIN CONNECTION

Figure 1



PIN CONNECTION

Figure 2



DESCRIPTION

The MK5371 is a monolithic, integrated circuit manufactured under Mostek's Silicon Gate CMOS process. This circuit provides necessary signals for either DTMF or loop disconnect (Pulse) signaling. The MK5371 buffers up to 28 digits into memory that can be later redialed with a single key input. This memory capacity is sufficient for local, long distance, overseas, and even computerized long-haul networks. Users can store all 12 signaling keys and access several unique special functions with single key entries. These functions include: Last Number Dialed (LND), Softswitch (Mode), Flash, and Pause. Figure 3 shows the keypad configuration.

KEYPAD CONFIGURATION

Figure 3

1	2	3	FLASH
4	5	6	MODE
7	8	9	PAUSE
*	0	#	LND

XIV

The LND key input automatically redials the last number dialed. The device ignores additional key entries during autodialing.

The Mode key simplifies the process of alternating dialing modes. This input automatically toggles the immediate dialing mode. The function is also stored in memory. During auto-redial, the signaling mode is toggled each time the Mode code appears in the digit sequence. The signaling mode always defaults to the mode selected (hardwire or switch) at Pin 2 (MODE/TEST). Switching modes through Pin 2 toggles the immediate dialing mode and changes the default, but it is not stored in memory.

Two features simplify PABX dialing. The PAUSE key stores a timed pause in the number sequence. Redial is then delayed until an outside line can be accessed or some other activity occurs before normal signaling resumes. The FLASH key simulates a hook flash to transfer calls or to activate other special features provided by the PABX or a central office. The MK5370/MK5371 ensures exact timing for the hook flash.

In addition to interfacing with standard keypads, the MK5370/MK5371 also accepts parallel BCD inputs. This feature simplifies interfacing a microprocessor-based design to the telephone line. The MK5371 buffers 28 bytes of information, including special functions.

All features are provided in an 18-pin package and also a more versatile 24-pin version, the MK5372. It includes RC programmable hook-flash timing, selectable tone levels, and the addition of both Make-Break (M-B) and 10-20 PPS select in Pulse Mode. The MK5370 is an 18-pin package that provides a continuous Mute output while signaling in Pulse Mode and a supply-independent tone level.

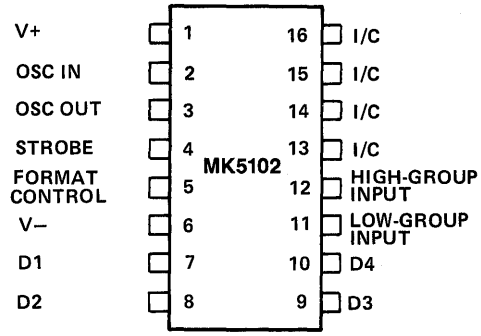
1984/1985 MICROELECTRONIC DATA BOOK

INTEGRATED TONE DECODER MK5102(N/P/J)

FEATURES

- ☐ Detects all 16 standard DTMF digits
- ☐ Requires minimum external parts count for minimum system cost
- ☐ Uses inexpensive 3.579545 MHz crystal for reference
- ☐ Digital counter detection with period averaging insures minimum false response
- ☐ 16-pin package for high system density
- ☐ Single supply 5 Volts ± 10%
- ☐ Output in either 4-bit binary code or dual 2-bit row/column code
- ☐ Latched outputs

MK5102 PIN OUT



DESCRIPTION

The MK5102 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television colorburst crystal for reference, the MK5102 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5102 ideal for applications requiring minimum size and external parts count.

The MK5102 detects the high and low group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 33 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5102 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP Package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V–) ..... +6.0 Volts
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... –55°C to 100°C
Maximum Circuit Power Dissipation ..... 300 mW
Voltage on any pin, with respect to V– ..... –0.3 Volt
Voltage on any pin, with respect to V+ ..... +0.3 Volt

*Operation Above Absolute Maximum Ratings May Damage The Device

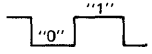
ELECTRICAL CHARACTERISTICS

$0° C \leq T_A \leq 70° C$ V– = 0 Volts

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V– = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	50% Duty Cycle Square Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE D1, D2, D3, D4 OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)–1		V+	Volts @ 0.1 mA	
FORMAT CONTROL Input	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+)–0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		33			ms	4
Interdigit Interval		35			ms	4
Signal to Noise Ratio		18			dB	3
Supply Current @ 5.5V	Inputs and Outputs Unloaded		5	10	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low leakage .05 μF capacitor.
2. No coupling capacitor is needed if the DTMF square wave meets the following criteria:



   a. Logic "0" level = 1 Volt (max)
   b. Logic "1" level = 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
   $SN = 20 \log \frac{SA}{NA}$
   where SA = RMS Amplitude of single tone being detected.
   NA = RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.

OSCILLATOR

The MK5102 contains an on-board inverter with sufficient gain to provide oscillation when working with a low cost television "color burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins D1 through D4. This three-state input selects a 4-Bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

FORMAT CONTROL (Continued)

The following table describes the two output codes.

Table 1

Digit	4-Bit Binary D1	D2	D3	D4	Dual 2-Bit Row/Column Row D1	D2	Column D3	D4
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 1 shows the relationship between the data output code shown in Table 1 and the standard DTMF keyboard.

DTMF DIALING MATRIX

Figure 1

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

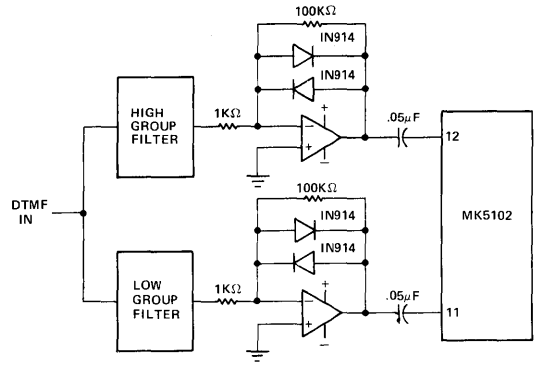
DETECTION FREQUENCY

Table 2

Low Group f_o	High Group f_o
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

SUGGESTED INPUT LIMITER CIRCUIT

Figure 2



OUTPUTS D1 THRU D4 (PINS 7 THRU 10)

Outputs D1 thru D4 are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

D1 thru D4 are the data out lines. The output data can be in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with D1 and D2 indicating the row selected, and D3 and D4 indicating the column selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

I/C (PINS 13 THRU 16)

Pins 13 thru 16 are internally connected and are intended to be left floating.

STROBE (Pin 4)

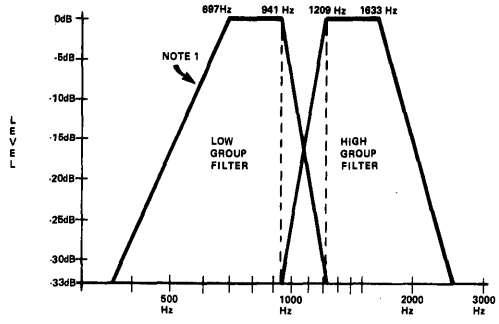
The STROBE output goes to a "1" when 33 milliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at D1-D4 are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

LOW-GROUP INPUT (Pin 11) and HIGH-GROUP INPUT (Pin 12)

The low- and high-group inputs are comparators that can detect capacitively-coupled square-wave signals as small as 0.9 volts peak-to-peak. The circuitry driving these inputs would typically use back-to-back silicon diodes as symmetrical limiters to regulate this level.

These inputs are biased to the midpoint of the supply with a resistive divider. Nominal input impedance is 100K Ω.

INPUT BAND SPLIT REQUIREMENTS



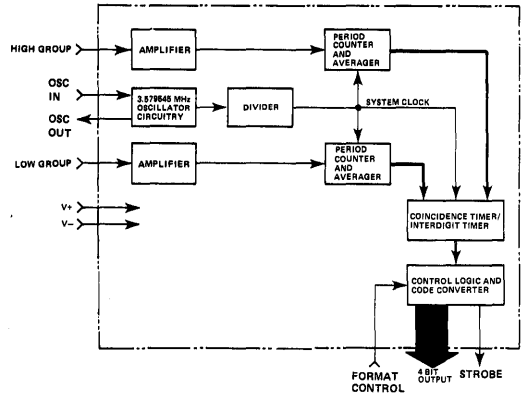
RELATIVE INPUT LEVEL VS FREQUENCY

NOTES:

1. Dial tone notch filter adequate to maintain S/N ratio of $\geqslant$ 18dB in above pass bands.

2. Filter response described above will normally result in operation to 6dB of twist with 18dB S/N.

MK5102 BLOCK DIAGRAM



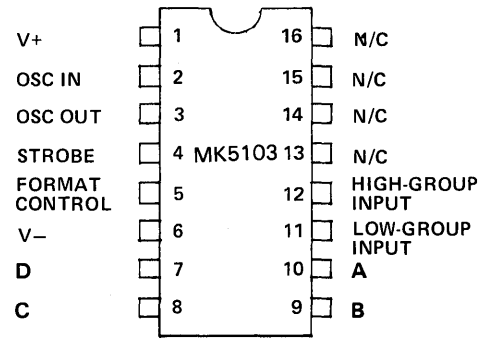
INTEGRATED TONE DECODER MK5103(N/P/J)

FEATURES

- Detects all 16 standard DTMF digits
- Requires minimum external parts count for minimum system cost
- Uses inexpensive 3.579545 MHz crystal for reference
- Digital counter detection with period averaging insures minimum false response
- 16-pin package for high system density
- Single supply: 5 volts ±10%
- Output in either 4-bit binary code or dual 2-bit row/column code
- Will operate at 14dB S/N ratio under worst-case signal conditions
- Latched outputs

PIN CONNECTIONS

Figure 1



DESCRIPTION

The MK5103 is a monolithic integrated circuit fabricated using the complementary-symmetry MOS (CMOS) process. Using an inexpensive 3.579545 MHz television color-burst crystal for reference, the MK5103 detects and decodes the 8 standard DTMF frequencies used in telephone dialing. The requirement of only a single supply and its construction in a 16-pin package make the MK5103 ideal for applications requiring minimum size and external parts count.

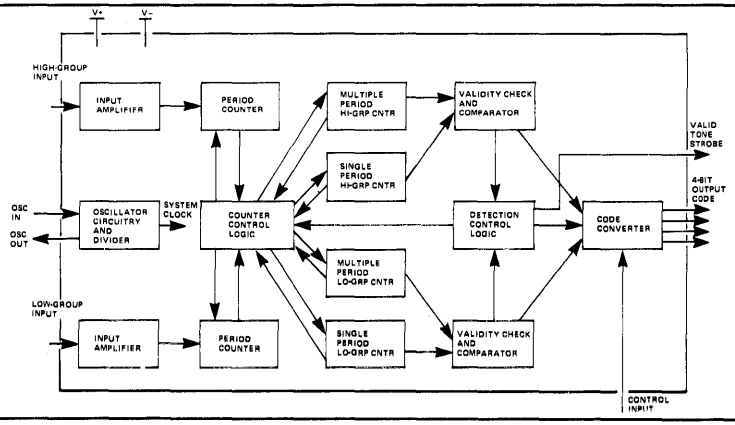
The MK5103 detects the high- and low-group DTMF tones after band splitting using a digital counting method. The zero crossings of the incoming tones are counted over several periods and the results averaged over a longer period. When a minimum of 30 milliseconds of a valid DTMF digit is detected, the proper data is latched into the outputs and the output strobe goes high. When a valid digit is no longer detected, the strobe will return low and the data will remain latched into the outputs. Minimum interdigit time is 35 milliseconds.

The MK5103 is designed to interface with the MK5099 Integrated Pulse Dialer with only one additional DIP package. These two parts working together form a DTMF-to-Pulse converter that meets the recognized telephone standards.

A block diagram of the MK5103 is shown in Figure 2. Functions of the individual pins are described beginning on page 2.

BLOCK DIAGRAM

Figure 2



XV

ABSOLUTE MAXIMUM RATINGS*

DC Supply Voltage V+ (Referenced to V-) ..... +6.0 Volts
Operating Temperature ..... 0°C to 70°C
Storage Temperature ..... -55°C to 100°C
Maximum Circuit Power Dissipation 300mW
Voltage on any pin, with respect to V- ..... -0.3 Volt
Voltage on any pin, with respect to V+ ..... +0.3 Volt

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

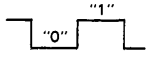
ELECTRICAL CHARACTERISTICS

$0°C \leq T_A \leq 70°C$ V- = **0 Volts**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (V+)	(V- = 0)	4.5		5.5	Volts	
Lo Group & Hi Group Inputs	47% - 53% Duty Cycle Rectangular Wave	0.9		V+	Volts Peak-to-Peak	1,2
STROBE, A, B, C, D OUTPUTS	"0" Level	0.0		0.4	Volt @ 1.6 mA	
	"1" Level	(V+)-1		V+	Volts @ 0.1 mA	
FORMAT CONTROL INPUT	"0" Level	0.0		0.5	Volt @ 700μA	
	"1" Level	(V+)-0.5		V+	Volt @ 700μA	
Frequency Detect Band Width		± 2.0	± 2.5	± 2.9	% of f_o	
Tone Coincidence Duration		30			ms	4
Interdigit Interval		35			ms	4
Signal-to-Noise Ratio		14			dB	3,5
Supply Current @ 5.5V	Inputs and Outputs Unloaded		2	5	mA	

NOTES:

1. Due to internal biasing, this input must be capacitively coupled with a low-leakage 0.05 μF capacitor.
2. No coupling capacitor is needed if the DTMF rectangular wave meets the following criteria:



A. Logic "0" level = 1 Volt (max)
B. Logic "1" level = 4 Volts (min)

3. Signal-To-Noise Ratio is defined as:
$SN = 20 \log \frac{SA}{NA}$
where SA = RMS Amplitude of single tone being detected.
NA = RMS white noise in the band from 300Hz to 3.4KHz.
4. Tone coincidence duration and interdigit interval measured at High- and Low-group inputs. Filter and/or limiter or comparator characteristics will affect the overall detect time.
5. Signal-To-Noise Ratio with 33db Filter Separation.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The MK5103 contains an on-board inverter with sufficient gain to provide oscillation when working with a low-cost television "color-burst" crystal. The inverter input is OSC IN (pin 2) and output is OSC OUT (pin 3). The circuit is designed to work with a crystal cut to 3.579545 MHz to give detection of the standard DTMF frequencies.

FORMAT CONTROL (PIN 5)

The Control pin is used to control the output format of Pins 7 through 10. This three-state input selects a 4-bit Binary Code, a Dual 2-Bit Row/Column code, or high-impedance output for use with bus-structured circuitry. This three-state input is controlled as follows:

FORMAT CONTROL FUNCTIONS
Table 1

FORMAT CONTROL INPUT	OUTPUT DATA FORMAT
V-	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

The following table describes the two output codes.

Table 2

Digit	4-Bit Binary D	C	B	A	Dual 2-Bit Row D	C	Column B	A
1	0	0	0	1	0	1	0	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	1	1
4	0	1	0	0	1	0	0	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	1	0	1	1
7	0	1	1	1	1	1	0	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	1	1	1	1
0	1	0	1	0	0	0	1	0
*	1	0	1	1	0	0	0	1
#	1	1	0	0	0	0	1	1
A	1	1	0	1	0	1	0	0
B	1	1	1	0	1	0	0	0
C	1	1	1	1	1	1	0	0
D	0	0	0	0	0	0	0	0

Figure 3 shows the relationship between the data output code shown in Table 2 and the standard DTMF keyboard.

DTMF DIALING MATRIX
Figure 3

	Col 1	Col 2	Col 3	Col 4
Row 1	1	2	3	A
Row 2	4	5	6	B
Row 3	7	8	9	C
Row 4	*	0	#	D

Note: Column 4 is for special applications and is not normally used in telephone dialing.

Table 3 shows the detection frequency associated with each row or column:

DETECTION FREQUENCY
Table 3

Low Group fo	High Group fo
Row 1 = 697 Hz	Column 1 = 1209 Hz
Row 2 = 770 Hz	Column 2 = 1336 Hz
Row 3 = 852 Hz	Column 3 = 1477 Hz
Row 4 = 941 Hz	Column 4 = 1633 Hz

OUTPUTS A THRU D (PINS 7 THRU 10)

Outputs A thru D are CMOS push-pull when enabled and open-circuited (high impedance) when disabled by the format control pin.

A thru D are the data out lines. The output data can be in in two formats as described in the section about the format control pin (pin 5).

The Dual 2-Bit Row/Column code decodes with A and B indicating the column selected, and C and D indicating the row selected.

The two output codes allow the user to obtain either 1-of-16 or 2-of-8 output data by using only a single additional package.

N/C (PINS 13 THRU 16)

Pins 13 thru 16 are not internally connected and may be used as tie points.

STROBE (PIN 4)

The STROBE output goes to a "1" when 30 milliseconds of a valid DTMF signal is detected and remains at a "1" until an interdigit interval has been detected. The data at A-D are already valid when STROBE goes to a "1" and will remain unchanged until the next DTMF digit is detected.

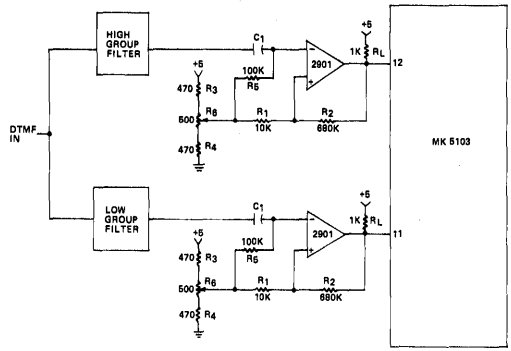
LOW-GROUP INPUT (PIN 11) AND HIGH-GROUP INPUT (PIN 12)

The circuitry driving these inputs, as shown in Figure 4, should be squaring circuits which use resistive dividers to set the output duty cycle to 50%. The squaring circuit shown was designed to provide hysteresis and allow the circuit to respond to signal levels of -28dBm or greater, where -28dBm corresponds to a peak-to-peak voltage of 87.1mV. Any squaring circuit providing a 47% - 53% duty cycle over the receiver and dynamic range is sufficient.

The high-group and low-group signals are provided by the high-group filter and the low-group filter, as shown in Figure 4. These filters have the response characteristics shown in Figure 5 and are used to separate the DTMF signal into its high-group and low-group components.

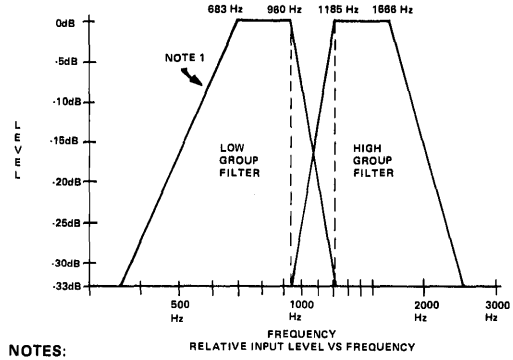
SUGGESTED INPUT LIMITER CIRCUIT

Figure 4



INPUT BAND SEPARATION FILTER

Figure 5



NOTES:

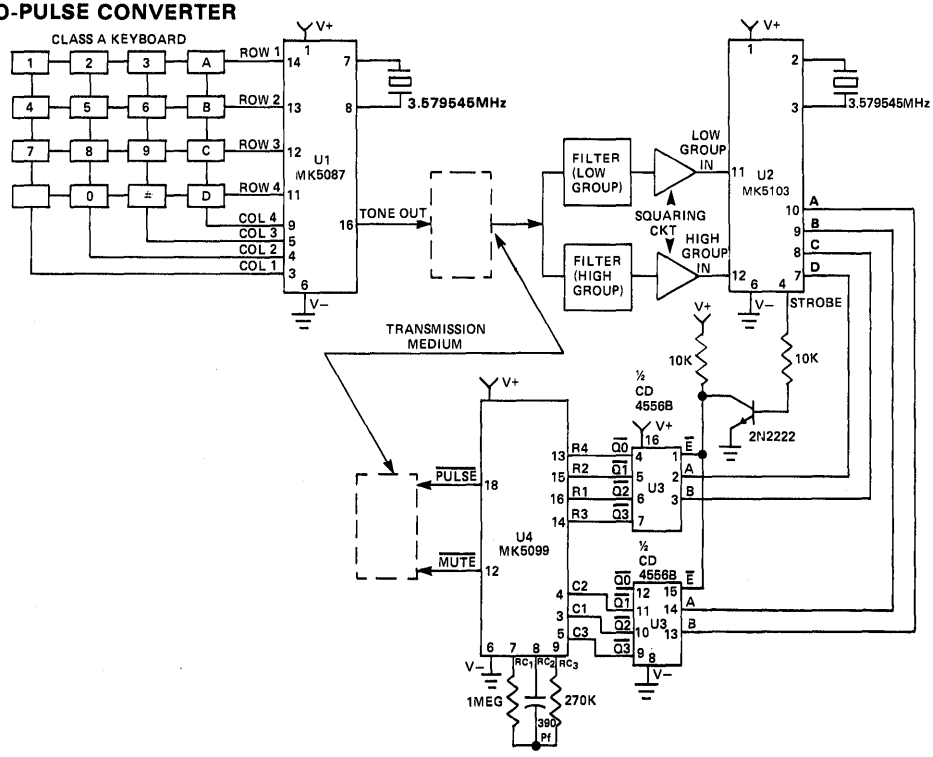
APPLICATIONS

Two possible applications of the MK5103 are shown in Figure 6 and Figure 7. The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 6. On this circuit, the MK5103N-5, CD4556 and MK5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK5103N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

For simple remote-control applications, the circuit of Figure 7 is useful. After a valid tone is detected, strobe will go high and one of the 16 outputs on the binary-to-1-of-16 encoder will go true. Thus, a DTMF transmitter and 16-key keyboard can be used to control 1 of 16 functions in a DTMF receiver.

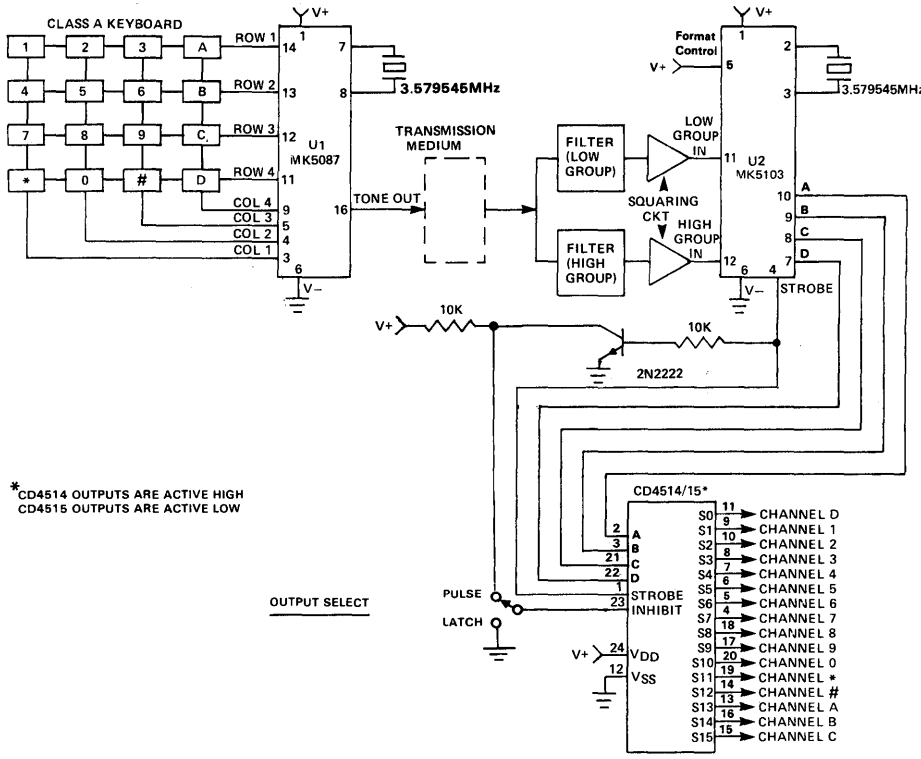
TONE-TO-PULSE CONVERTER

Figure 6



16-CHANNEL REMOTE CONTROL

Figure 7



XV

APPLICATION BRIEF

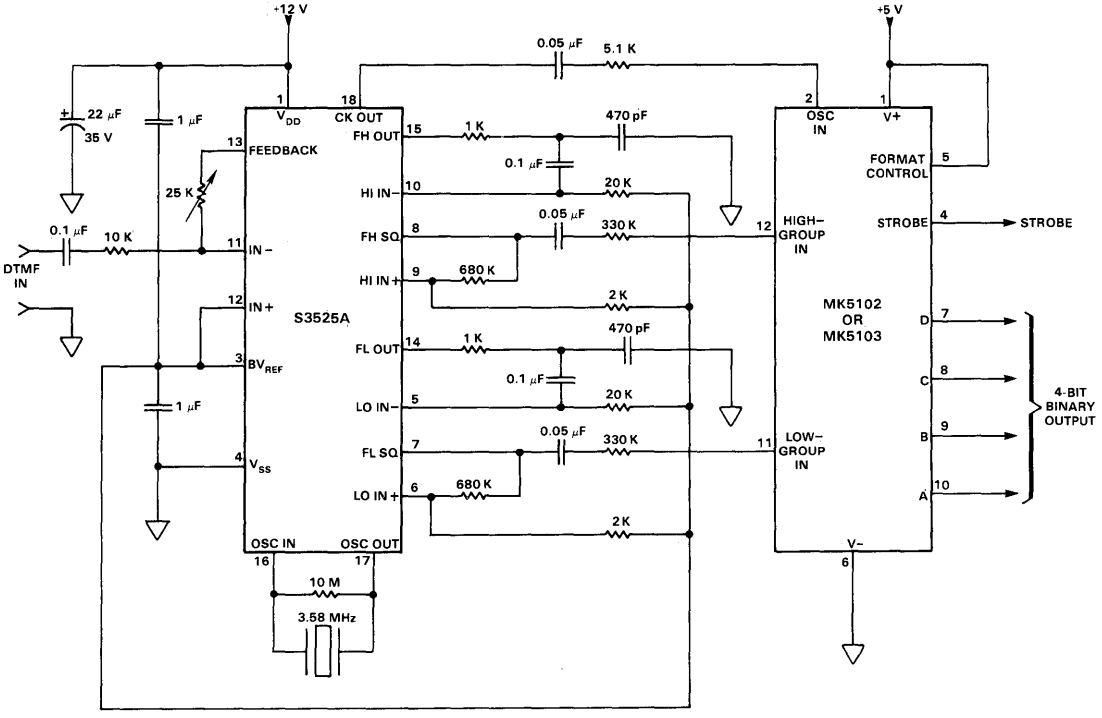
MK5102/S3525A DTMF RECEIVER SYSTEM

An inexpensive DTMF receiver system with a low parts count may be constructed using the Mostek MK5102 or MK5103 Tone Decoder with the AMI S3525A Bandsplit Filter. The S3525A is an 18-pin monolithic CMOS switched-capacitor filter. It uses a 3.58 MHz crystal as a time base and has a buffered clock output to drive the oscillator of the MK5102/3. The S3525A also has on-chip comparators which can be used to construct adjustable squaring circuits.

Using the circuit shown in Figure 1, the duty cycle of the signals provided to the MK5102 should be within the 50 ± 1% range which is required for reliable operation. (Since the MK5103 requires a 50 ± 3% duty cycle, the input signals will be well within its range.) With the potentiometer adjusted so that the filter has unity gain, the results listed in Tables 1, 2, and 3 should be obtained. Tables 1 and 2 show the Mitel test tape (CM7291) results for the DTMF receiver system using the S3525A and the MK5102 or MK5103, respectively. Table 3 shows the Minimum Tone Coincidence Duration for the system using the MK5102 and MK5103 at various input levels.

The operation of the circuit shown in Figure 1 has been verified at temperatures of 0°C, 25°C, and 70°C. However, Tables 1, 2, and 3 show only the data for circuit operation at 25°C.

MK5102/S3525A DTMF RECEIVER SYSTEM
Figure 1



XV

MK5102 WITH AMI S3525A MITEL TAPE (CM7291) TEST RESULTS

Table 1

TEST #	RESULTS
2a, b	BW = 4.6% of fo
2c, d	BW = 4.9% of fo
2e, f	BW = 4.7% of fo
2g, h	BW = 5.0% of fo
2i, j	BW = 4.8% of fo
2k, l	BW = 4.7% of fo
2m, n	BW = 4.8% of fo
2o, p	BW = 4.7% of fo
3	160 decodes
4	Acceptable Amplitude Ratio = 18.2 dB
5	Dynamic Range = 32 dB
6	Guard Time = 34.8 ms
7	99.0% Successful Decode at S/N Ratio of 12 dB
8	1 Hit on Talk-Off Test

MK5103 WITH AMI S3525A MITEL TAPE (CM7291) TEST RESULTS

Table 2

TEST #	RESULTS
2a, b	BW = 5.0% of fo
2c, d	BW = 5.1% of fo
2e, f	BW = 4.9% of fo
2g, h	BW = 5.2% of fo
2i, j	BW = 5.1% of fo
2k, l	BW = 5.0% of fo
2m, n	BW = 5.2% of fo
2o, p	BW = 5.1% of fo
3	160 decodes
4	Acceptable Amplitude Ratio = 19.1 dB
5	Dynamic Range = 32 dB
6	Guard Time = 32.5 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	1 Hit on Talk-Off Test

MK5102/3 WITH AMI S3525A MINIMUM TONE COINCIDENCE DURATION

Table 3

Input Level dBm (600 Ω)	MK5102 Decode Time	MK5103 Decode Time
-28 dBm	43.4 ms	38.9 ms
-25 dBm	37.4 ms	34.7 ms
-20 dBm	37.0 ms	34.7 ms
-10 dBm	36.3 ms	28.8 ms
0 dBm	37.3 ms	28.8 ms
+6 dBm	36.5 ms	28.9 ms

NOTES:

1. More information regarding the S3525A is available from:
   American Microsystems Inc.
   3800 Homestead Rd.
   Santa Clara, CA 95051
   Telephone: (408) 246-0330
   TWX: 910-338-0018
2. More information regarding the MK5102 and MK5103 is available from:
   Mostek Telecom Dept.
   1215 W. Crosby Rd.
   Carrollton, Texas 75006
   Telephone: (214) 323-1000
3. The AMI S3525A used in this evaluation was a typical part. Slightly different results may be obtained depending upon the particular S3525A used.

APPLICATION BRIEF

DTMF RECEIVER SYSTEM

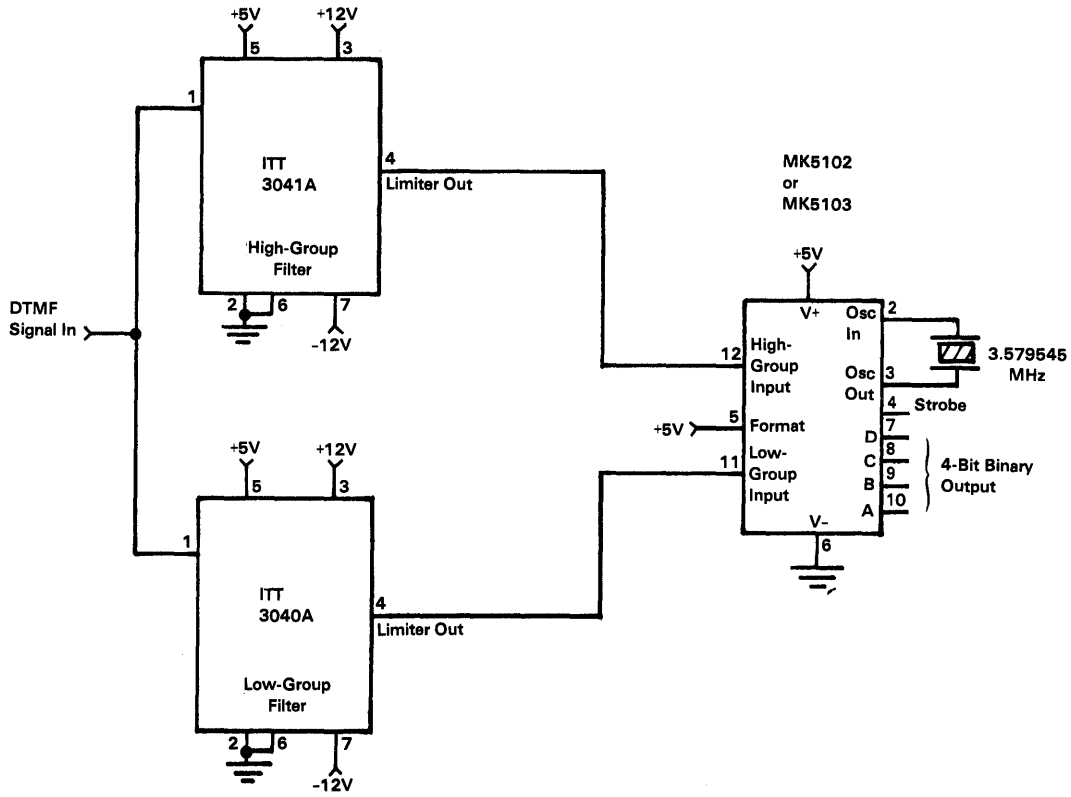
A DTMF receiver system with a low parts count may be constructed using the MK5102 or MK5103 tone decoder and the ITT 3040A and ITT 3041A hybrid filter[1]. The ITT 3040A and ITT 3041A filters have on-chip limiters so that external squaring circuits are not needed. An alternate design allowing precise adjustment of external squaring circuits is described in another Mostek Application Note[2]. Tables 1 and 2 show the MITEL (CM7290) tape results using the ITT 3040A/41A with the MK5102 and MK5103, respectively.

NOTES:

(1) ITT 3040A and ITT 3041A filters with limiters may be obtained from:
ITT North Microsystems Division
700 Hillsboro Plaza
Deerfield Beach, Florida 33441
Telephone: 305-421-8450
TWX: 510-953-7523

(2) MK5102N-5 DTMF Decoder Application Note, "Design Considerations for a DTMF Receiver System" is available from:
Mostek • Telecom Dept.
1215 W. Crosby Rd.
Carrollton, Texas 75006
Telephone: 214-323-6000

Figure 1



XV

MK5102 with ITT 3040A and ITT 3041A
MITEL TAPE (CM7290) TEST RESULTS
Table 1

TEST #	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 4.8 % of fo
2e, f	BW = 5.4 % of fo
2g, h	BW = 4.9 % of fo
2i, j	BW = 5.3 % of fo
2k, l	BW = 5.4 % of fo
2m, n	BW = 5.6 % of fo
2o, p	BW = 4.9 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 19.7 dB
5	Dynamic Range = 25 dB
6	Guard Time = 32.9 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	3 Hits on Talk-Off Test

MK5103 with ITT 3040A and ITT 3041A
MITEL TAPE (CM7290) TEST RESULTS
Table 2

TEST #	RESULTS
2a, b	BW = 5.3 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.4 % of fo
2i, j	BW = 5.6 % of fo
2k, l	BW = 5.3 % of fo
2m, n	BW = 5.4 % of fo
2o, p	BW = 5.6 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 19.9 dB
5	Dynamic Range = 30 dB
6	Guard Time = 23.3 ms
7	99.9% Successful Decode at S/N Ratio of 12 dB
8	9 Hits on Talk-Off Test

MK5102(N)-5 DTMF DECODER APPLICATION NOTE

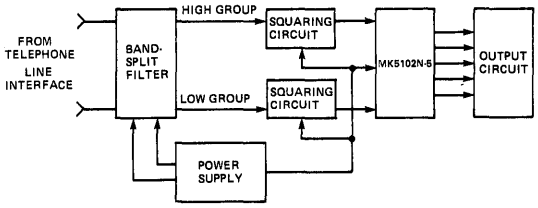
This application note will describe all of the requirements for building a high-quality DTMF receiver using the MK5102N-5 and hybrid filters. The following topics will be discussed:

1. Power supply requirements
2. Band separation filter requirements
3. Squaring circuit requirements
4. Squaring circuit-to-decoder coupling requirements
5. Receiver testing
6. Output formatting
7. Other system considerations

Since the MK5102N-5 is intended to be a portion of a tone receiver SYSTEM, SYSTEM requirements must be met before a satisfactory decoder can be constructed. A block diagram of a typical system is shown in Figure 1. Each portion of the block diagram is discussed in succeeding paragraphs.

TYPICAL DTMF RECEIVER

Figure 1



POWER SUPPLY REQUIREMENTS

For proper operation of the MK5102N-5, the V+ power supply must be between 4.5 VDC and 5.5 VDC, with V- grounded. A power supply decoupling capacitor (typically .1uF) should be connected between V+ and V- to insure that no high-frequency noise is present on the V+ supply. Typically, a 1-volt peak-to-peak signal may be applied to V+ and the MK5102N-5 will function properly.

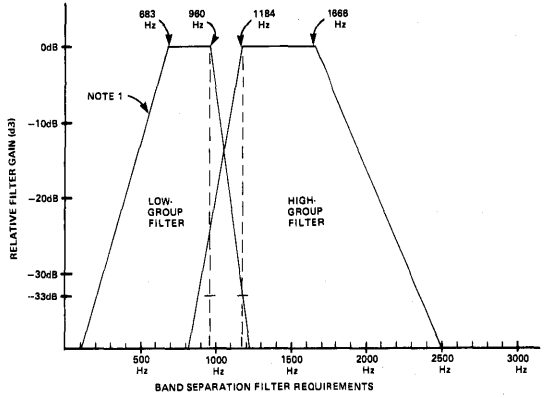
FILTER REQUIREMENTS

For proper operation of the MK5102N-5, an external band separation filter must be provided to split the DTMF signal into its high-group and low-group components. However, the band separation requirements are not as stringent for the MK5102N-5 as they are for competing designs. As shown in figure 2, the MK5102N-5 requires a band separation of only 33dB in an average application. The 33dB requirement allows for a S/N ratio of 18dB, 6dB of twist, and a detection bandwidth of at least ± 2%. A reduction of twist margin or S/N requirements will result in a corresponding lower requirement for band separation. For example, if there is not a requirement for twist margin, the band separation can be reduced to 27dB. In a system with no noise and no twist, the band separation can be 22dB.

The plot shown in Figure 2 depicts corner frequencies of 683Hz, 960Hz, 1184Hz and 1666Hz. These represent a 2% deviation from the DTMF frequencies of 697Hz, 941Hz, 1209Hz and 1633Hz, respectively. This deviation is necessary because of the requirement that a DTMF receiver must detect frequencies which are 2% higher or lower than the nominal DTMF frequency. Table 1 lists the 8 DTMF frequencies and the corresponding frequencies which a DTMF decoder is required to detect.

BAND SEPARATION FILTER REQUIREMENTS

Figure 2



NOTES:

1. Dial tone notch filter must maintain S/N ratio ≥ 18dB
2. Filter response shown will allow operation to 6dB of twist with 18dB S/N.

XV

TABLE I

8 STANDARD DTMF FREQUENCIES AND CORRESPONDING UPPER AND LOWER REQUIRED DETECTION FREQUENCIES

DTMF FREQUENCY (HZ)	LOWER DETECTION FREQUENCY LIMIT (HZ)	UPPER DETECTION FREQUENCY LIMIT (HZ)
697	683	711
770	755	786
852	834	869
941	922	960
1209	1184	1233
1336	1309	1363
1477	1447	1507
1633	1600	1666

DETECTION ALGORITHM

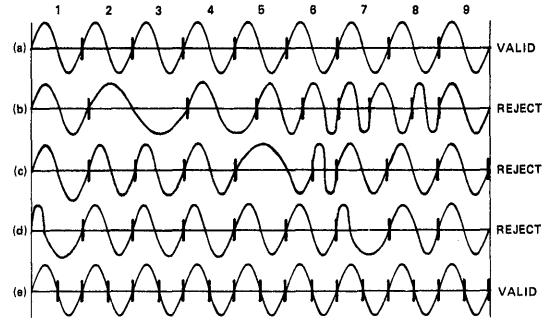
The detection approach used in the MK5102N-5 utilizes zero-crossing detection and digital period-counting. To increase the rejection of random noise and the residue from out-of-band components, an averaging scheme is used. Figure 3(a) shows nine cycles of a symmetrical sine wave. If zero-crossings were the only detection criteria, and if the average period-count obtained over nine periods were acceptable, then the signal in Figure 3(a) represents a valid tone. The jitter of the zero-crossings is integrated out by the nine-period average. However, based on the simple nine-period average, the signal shown in Figure 3(b) would be accepted as a valid tone. To improve rejection of this speech-type waveform, the nine-period detection time can be broken into three period-averaged sub-groups as indicated by the dashed lines in Figure 3(b). By combining the nine-period average and the sub-group average criteria, 200 false hits are obtained on 30 minutes of a standard speech tape. Figure 3(c) represents a type of waveform that would produce a hit based on the nine-period and sub-group average algorithm. To improve rejection of this waveform, requirements must be placed on every single period in addition to the nine-period average and the sub-group average. However, the waveform of Figure 3(d) will be detected using only these three criteria. Therefore an additional requirement must be placed on each half-period of the waveform. Figure 3(e) shows the only type of signal which will be accepted by a detection algorithm which requires the following:

1. Valid nine-period average
2. Three valid sub-group averages
3. Valid single-period
4. Valid half-period

Using these four criteria, the number of hits on a standard speech tape can be reduced to less than six.

POSSIBLE INPUT WAVEFORMS

Figure 3

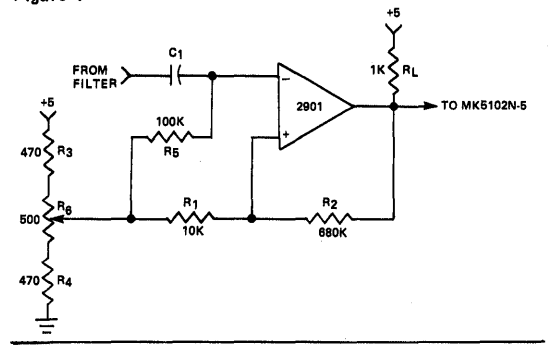


INPUT SQUARING CIRCUITS

As described above, to minimize the number of false hits, a detection algorithm must place stringent requirements on each half-period of the input waveform (high group or low group). To successfully meet these requirements, the duty cycle of the input waveform must be between 49% and 51%. The input squaring circuit must therefore provide an output which accurately tracks the input without adversely affecting the duty cycle. Such a circuit, an inverting comparator with hysteresis, is illustrated in Figure 4.

INPUT SQUARING CIRCUIT

Figure 4



C_1 is used to ac couple the filter output to the squaring circuit so that DC bias present at the filter output will not affect the performance of the squaring circuit. R_3, R_4, and R_6 establish a bias level at about 2.5 Volts, and R_5 is used to provide the same bias level at the inverting input of the comparator used in the squaring circuit. The maximum input bias current for the LM2901 is 500nA, so the DC bias level at the inverting input is effectively the same as the voltage at the wiper of R_6. R_6 must be adjusted so that, for an input signal level of -28dBm, the output duty cycle will be 50%. This adjustment compensates for

the input offset voltage of the LM2901. R_L is the pullup resistor for the open-collector output of the comparator. R_1 and R_2 set the hysteresis level. Their values are determined by the following approximate relationships:

$$V_{UT} = 2.5 + \frac{(2.5)(R_1)}{(R_1 + R_2 + R_L)}$$

where V_{UT} is the upper threshold

$$V_{LT} = \frac{(2.5 - V_{OL})(R_2)}{(R_1 + R_2)}$$

where V_{LT} is the lower threshold and V_{OL} is the output saturation voltage

In both cases, any variation due to the current in R_5 is ignored.

For central office applications, the tone receiver system must operate over an input signal level range of -26dBm to +6dBm. The squaring circuit, therefore, must respond to signal levels of -26dBm or greater but is not required to respond to lower signal levels.

To allow for signal attenuation through the band separation filter, the squaring circuit should be set to respond to signal levels of -28dBm or greater. The -28dBm cutoff point corresponds to a peak-to-peak voltage of 87.1mV. For a 50% duty-cycle output waveform, V_{UT} should be set 43.5mV above and V_{LT} should be set 43.5mV below the DC bias point. The passive components for the squaring circuit are then selected as follows:

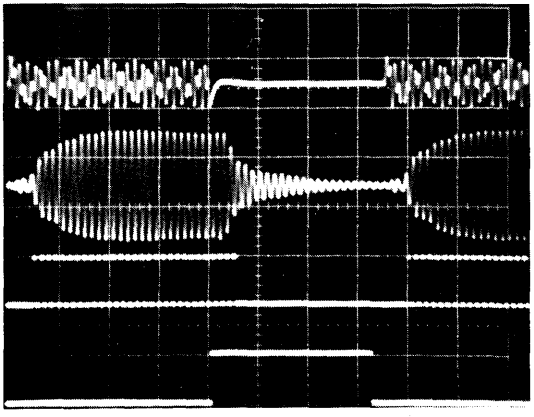
$R_L = 1k\Omega$	Chosen value.
$R_2 = 680k\Omega$	Chosen value.
$R_1 = 12k\Omega$	Calculated value.
$R_3 = R_4 = 470\Omega$	Chosen value for DC bias.
$R_5 = 100k\Omega$	Chosen value. Tradeoff effect on DC bias vs. drop across R_5 due to 2901 input bias current.
$C_1 = 1\mu F$	Chosen value. Must be low impedance over frequency range of 683Hz to 1666Hz.

To achieve proper operation at low signal levels, R_1 must be 10kΩ. The discrepancy between the calculated value and the actual required value results from component tolerances.

Since many commercially-available filters exhibit a ringing characteristic at their output, as shown in Figure 5 and Figure 6, additional circuitry is required to detect the beginning of ringing and squelch the output of the squaring circuit. The required circuitry, an envelope detector, is shown in Figure 7. The detector consists of two precision rectifiers, two sample-and-hold circuits, and a comparator. C_3 is used to couple the low-group filter output to the envelope detector. Z1a, D_1, C_1, R_2, and R_3 then rectify the incoming signal and store a peak value. The $R_2/R_3/C_1$ time constant is set for 20ms so that the voltage at the inverting input of Z_2 will represent ½ the peak value of the incoming signal. Z1b, D_2, R_1 and C_2 also rectify the incoming signal and store a peak value, but the time constant is set for 1.4ms so that the voltage at the non-inverting input of Z_2 will represent the instantaneous peak value of the incoming waveform. As long as the instantaneous value is greater than ½ of the peak value, the comparator output will be high. However, as soon as the instantaneous value decreases to less than ½ the peak value (this will occur as ringing begins), the comparator output will go low and inhibit the output of the squaring circuit. It is necessary to provide only one envelope detector since the MK5102N-5 will treat the absence of a valid low-group/high-group tone combination as interdigit time.

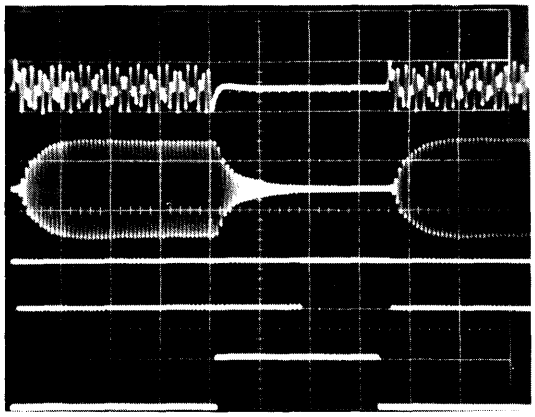
LOW-GROUP FILTER RESPONSE (3044)

Figure 5



HIGH–GROUP FILTER RESPONSE (3045)

Figure 6



EACH TIME DIVISION = 10 ms

DTMF INPUT TO FILTER (5V/DIV.)

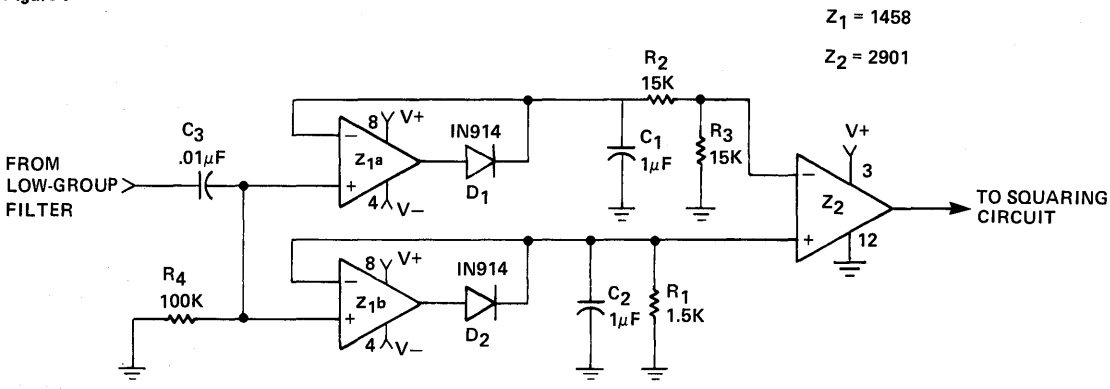
LOW-GROUP
FILTER OUTPUT (IV/DIV.)

SQUARING CIRCUIT
OUTPUT (5V/DIV.)

STROBE FROM MK5102N-5
(5V/DIV.)

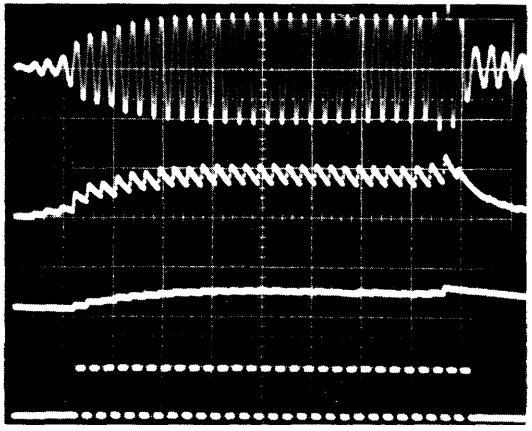
ENVELOPE DECAY DETECTOR

Figure 7



ENVELOPE DETECTOR OPERATION

Figure 8



LOW-GROUP
FILTER OUTPUT (IV/DIV.)

INSTANTANEOUS PEAK
DETECTOR (IV/DIV.)

AVERAGE PEAK
DETECTOR (IV/DIV.)

LOW-GROUP INPUT
TO 5102N-5 (5V/DIV.)

SQUARING CIRCUIT-TO-DECODER COUPLING

The output of the squaring circuit may be tied directly to the MK5102N-5 if it meets the following requirements:

Logic 1 ≥ 4 volts
Logic 0 ≤ 1 volt

A squaring circuit with an output that does not meet these requirements must be capacitively coupled to the MK5102N-5 with a 0.05μF capacitor. The value of the coupling capacitor is critical because of the impedance of the bias circuit at the high-group or low-group input. As shown in Figure 9, the sudden appearance of a tone burst causes the DC bias point to shift upward. Until the DC bias returns to its normal level, the input comparator will not switch and the input signal will be ignored, causing an increase in the dual-tone detection time. Using a 0.05μF capacitor will minimize the effect of this DC level shift. The peak-to-peak value of the coupled signal must be greater than .9 volts but less than V+ volts.

OUTPUT SIGNALS

D1, D2, D3, and D4 are the data output lines. The output format present on these pins is determined by the format control (pin 5) as shown in Table 2.

FORMAT CONTROL FUNCTIONS
TABLE 2

Format Control Input	Data Output Format
V–	High Impedance
V+	4-Bit Binary
Floating	Dual 2-Bit Row/Column

SHIFT IN DC BIAS LEVEL CAUSED BY APPLICATION OF TONE BURST
Figure 9

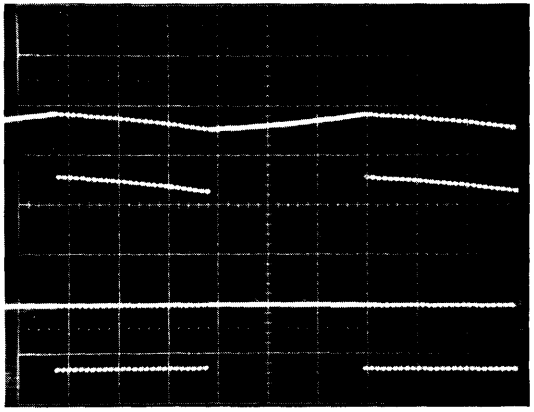


Table 3 describes the two output codes available.

TABLE 3

OUTPUT FORMAT

			4-Bit Binary				Dual 2-Bit Row/Column			
							Row		Column	
Key	Row	Col.	D1	D2	D3	D4	D1	D2	D3	D4
1	1	1	0	0	0	1	0	1	0	1
2	1	2	0	0	1	0	0	1	1	0
3	1	3	0	0	1	1	0	1	1	1
4	2	1	0	1	0	0	1	0	0	1
5	2	2	0	1	0	1	1	0	1	0
6	2	3	0	1	1	0	1	0	1	1
7	3	1	0	1	1	1	1	1	0	1
8	3	2	1	0	0	0	1	1	1	0
9	3	3	1	0	0	1	1	1	1	1
0	4	2	1	0	1	0	0	0	1	0
*	4	1	1	0	1	1	0	0	0	1
#	4	3	1	1	0	0	0	0	1	1
A	1	4	1	1	0	1	0	1	0	0
B	2	4	1	1	1	0	1	0	0	0
C	3	4	1	1	1	1	1	1	0	0
D	4	4	0	0	0	0	0	0	0	0

When all detection criteria are present, the MK-5102N-5 will latch the proper data into its outputs and strobe will go high. After an interdigit time has been detected, strobe will go low, but the data will remain on D1 through D4.

The dual 2-bit row/column code is useful when interfacing a key-to-pulse converter, as shown in Figure 10. On this circuit, the MK5102N-5, CD4556 and MK 5099 combine to form a tone-to-pulse converter, which allows the use of DTMF telephones in rotary exchanges. The DTMF tones are detected by the MK 5102N-5, which then generates the corresponding row/column code. Each CD4556 then uses this 2-bit code to select 1 of 4 active-low outputs. The MK5099 then interprets these signals as a valid key closure and generates a corresponding series of pulses.

TEST CIRCUIT FOR CERMETEK AND NORTH ELECTRIC FILTERS

Figure 13

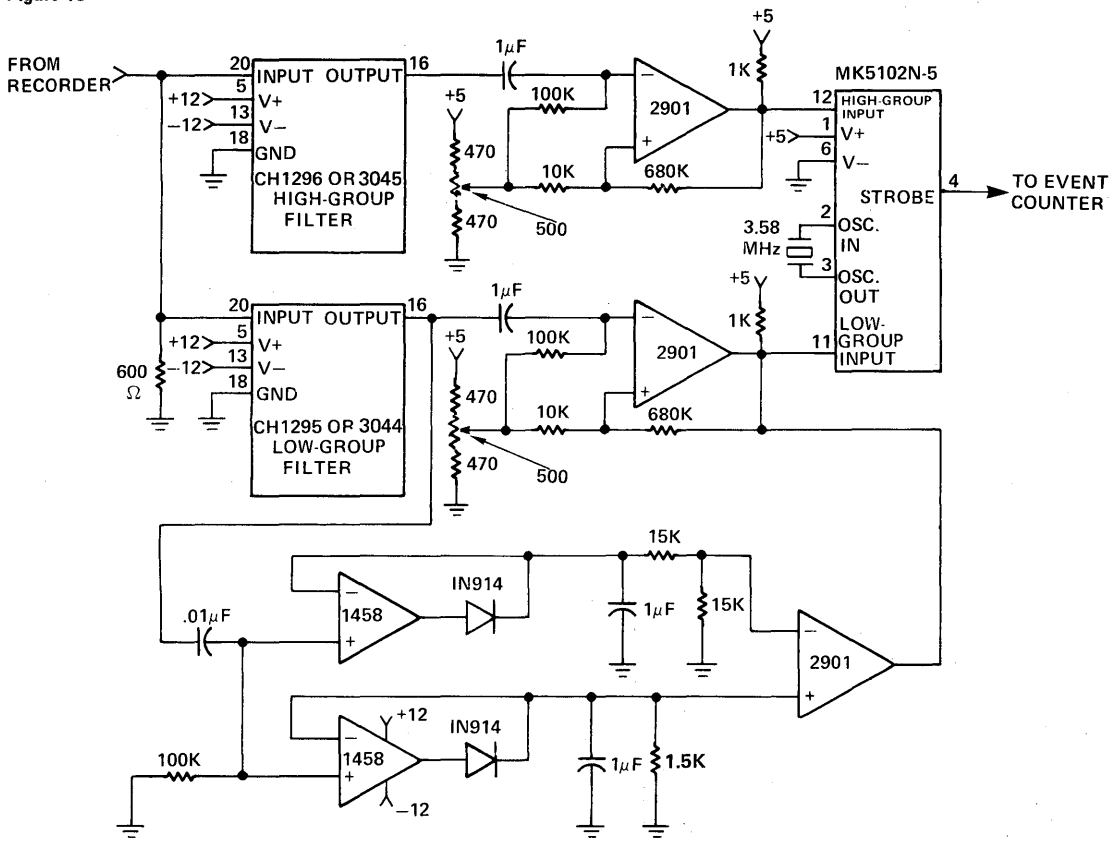


TABLE 4
MITEL TAPE TEST RESULTS FOR NORTH ELECTRIC FILTERS

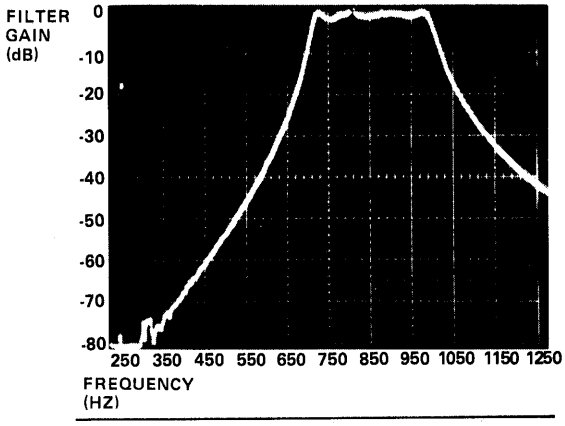
TEST#	RESULTS
2a, b	BW = 4.7 % of fo
2c, d	BW = 5.2 % of fo
2e, f	BW = 5.1 % of fo
2g, h	BW = 5.1 % of fo
2i, j	BW = 5.1 % of fo
2k, l	BW = 4.9 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	159 decodes
4	Acceptable Amplitude Ratio = 13.1dB
5	Dynamic Range = 31.33 dB
6	Guard Time = 34.23 ms
7	99.8 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

TABLE 5
MITEL TAPE TEST RESULTS FOR CERMETEK FILTERS

TEST#	RESULTS
2a, b	BW = 5.6 % of fo
2c, d	BW = 5.7 % of fo
2e, f	BW = 5.0 % of fo
2g, h	BW = 5.3 % of fo
2i, j	BW = 5.2 % of fo
2k, l	BW = 5.0 % of fo
2m, n	BW = 5.5 % of fo
2o, p	BW = 5.0 % of fo
3	158 decodes
4	Acceptable Amplitude Ratio = 12.6dB
5	Dynamic Range = 31.67 dB
6	Guard Time = 33.4 ms
7	98.33 % Successful Decode at N/S Ratio of -12dbV
8	3 Hits on Talk-Off Test

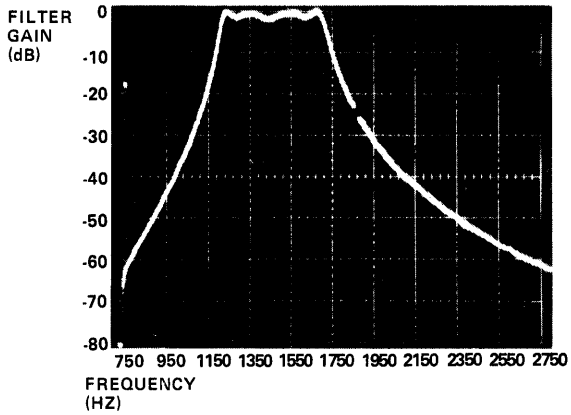
SPECTRAL RESPONSE OF CH1295 LOW-GROUP FILTER

Figure 14



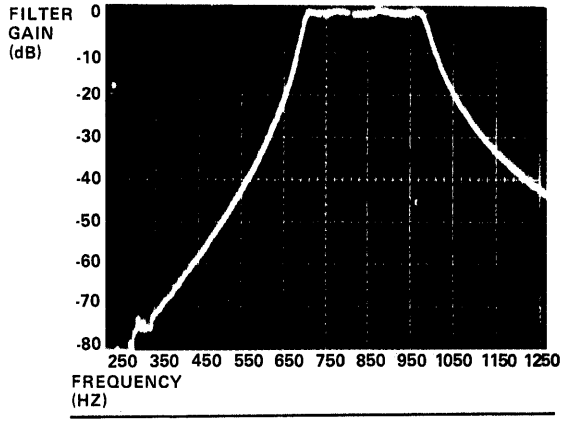
SPECTRAL RESPONSE OF CH1296 HIGH-GROUP FILTER

Figure 15



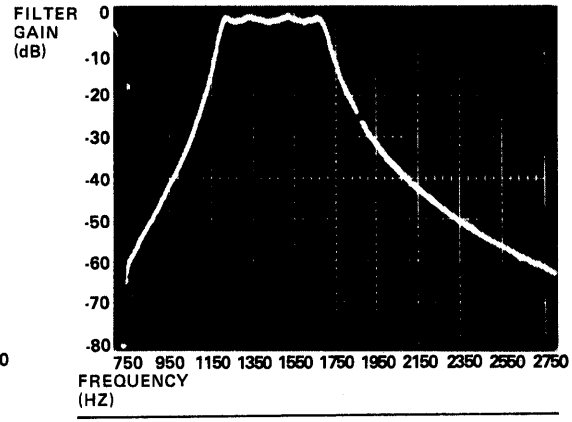
SPECTRAL RESPONSE OF 3044 LOW-GROUP FILTER

Figure 16



SPECTRAL RESPONSE OF 3045 HIGH-GROUP FILTER

Figure 17



OTHER SYSTEM CONSIDERATIONS

System noise will affect the operation of the MK5102N-5 by causing the detection bandwidth to shrink. The instantaneous value of the low-group or high-group waveform is represented by the following approximate relationship, $a = a_T \sin w_T t + a_N \sin w_N t$, where a is the instantaneous amplitude of the overall waveform, a_T is the amplitude of the high-group or low-group component, and a_N is the amplitude of the noise. If the highly-simplified noise term ($a_N \sin w_N t$) were removed, then the remaining term would represent a pure sine wave and the zero crossings of the waveform would be repeatable from cycle to cycle. All detection criteria would be present and the DTMF tone would be detected within a ± 2.0% to ± 2.9% bandwidth. However, adding the noise term introduces instantaneous amplitude variations which will effectively alter the duty cycle of the sine wave by causing the zero crossing points to jitter. If 0.5% jitter is caused by system noise, detection bandwidth will be decreased by .5%. Therefore, as the system noise level increases, the detection bandwidth will decrease.

As noted in the Filter Requirements paragraph, the 33dB band separation requirement allows for a S/N ratio of 18dB, with 6dB of twist, which means that the algorithm in the MK5102N-5 has been set up to provide a ± 2% minimum detection bandwidth in the presence of noise which is 18dB below the signal level and in the presence of high-group and low-group signals with an amplitude difference of 6dB.

SUMMARY

The MK5102N-5 provides a high-performance solution for DTMF detection at a lower cost than competing approaches. Band separation requirements for the MK5102N-5 are not as stringent as for competing designs, and, as was seen in the test results of Table 4 and Table 5, the MK5102N-5 provides excellent talk-off rejection. When used in conjunction with either the Cermetek or the North Electric filters, the MK5102N-5 will give the user a high-quality DTMF receiver which may be used in myriad applications.

1984/1985 MICROELECTRONIC DATA BOOK

μ-255 LAW COMPANDING CODEC MK5116(J/N)

FEATURES

- ☐ ±5-Volt Power Supplies
- ☐ Low Power Dissipation - 30mW (Typ)
- ☐ Follows the μ-255 Companding Law
- ☐ Synchronous or Asynchronous Operation
- ☐ On-chip sample and hold
- ☐ On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- ☐ Single 16-Pin Package
- ☐ Minimal External Circuity Required
- ☐ Serial Data Output of 64kb/s—2.1 Mb/s at 8kHz Sampling Rate
- ☐ Separate Analog and Digital Grounding Pins Reduce System Noise Problems

DESCRIPTION

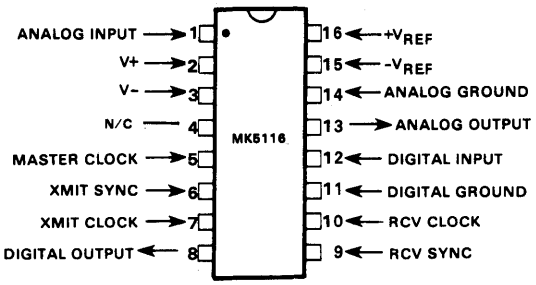
The MK5116 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occurring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

The pin configuration of the MK5116 is shown in Figure 1.

PIN CONNECTIONS

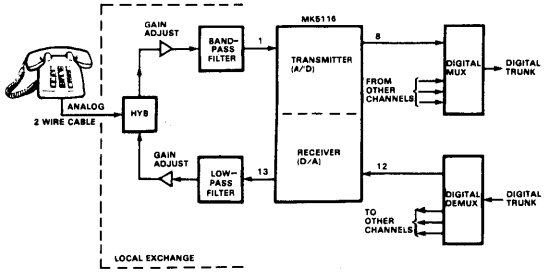
Figure 1



A block diagram of a PCM system using the MK5116 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM

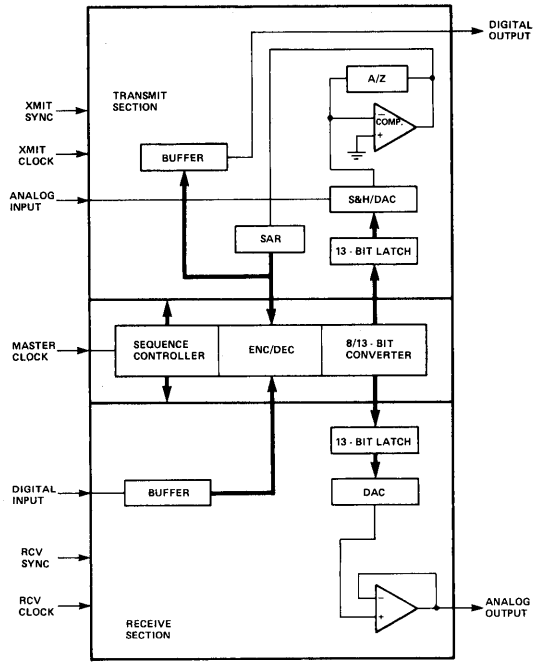
Figure 2



XVI

FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5116 BLOCK DIAGRAM
Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5116. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (refer to Figure 4). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 9.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV SYNC, RCV CLOCK, XMIT SYNC, or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated, and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC may remain high longer than 8 XMIT CLOCK cycles, but must go low for at least 1 master clock before the transmission of the next digital word (refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5116 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (refer to the Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

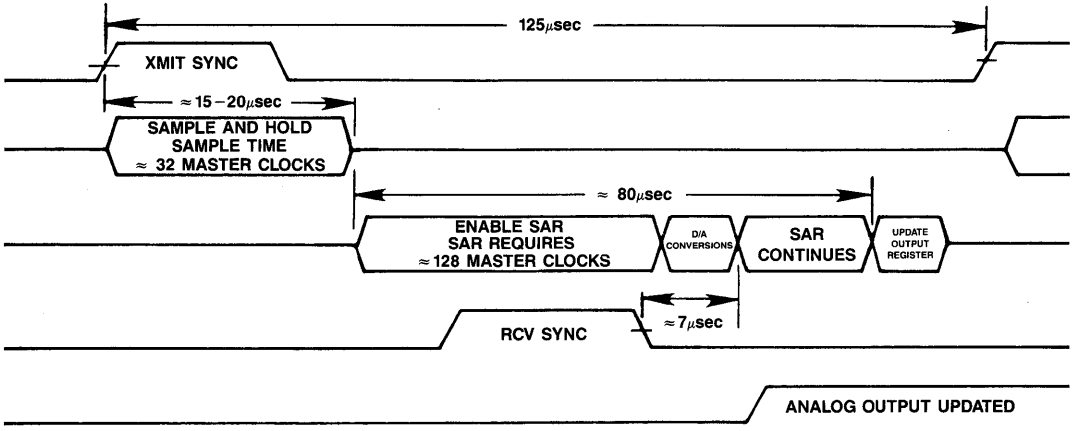
RVC SYNC, Pin 9 (Refer to Figure 11 for the Timing Diagram)

This input is synchronized with RCV CLOCK, and serial data is clocked in by RCV CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV CLOCK periods. The conversion from digital to analog starts after the negative edge of the RCV SYNC pulse (refer to Figure 4). The negative edge of RCV SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (refer to Figure 13).

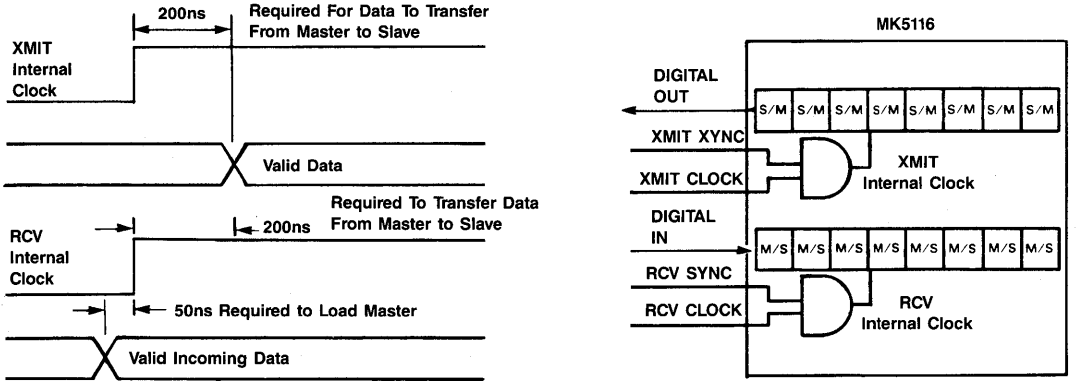
RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5116 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV SYNC occurs after the first rising edge of RCV CLOCK, RCV SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up

A/D, D/A CONVERSION TIMING
Figure 4



DATA INPUT/OUTPUT TIMING
Figure 5



and hold times for the first clock pulse should be measured from the positive edge of RCV SYNC.

DIGITAL OUTPUT, Pin 8

The MK5116 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.
Each Chord has a specific value; and the Step Bits, 16 in each Chord, specify the displacement from that value (refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL INPUT, Pin 12

The MK5116 input register accepts the 8-bit sample of an analog value and loads it under control of RCV SYNC and RCV CLOCK. The timing diagram is shown in Figure 11. When RCV SYNC goes high, the MK5116 uses RCV

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	000	0.0mV	0.613mV
2.	001	10.11mV	1.226mV
3.	010	30.3mV	2.45mV
4.	011	70.8mV	4.90mV
5.	100	151.7mV	9.81mV
6.	101	313mV	19.61mV
7.	110	637mV	39.2mV
8.	111	1.284V	78.4mV

EXAMPLE:

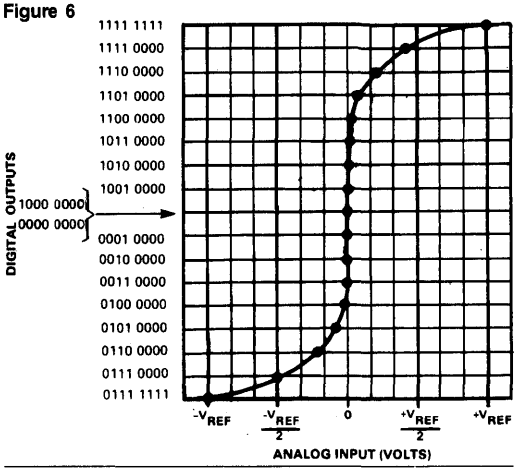
1 011 0010 = + 70.8mV + (2×4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

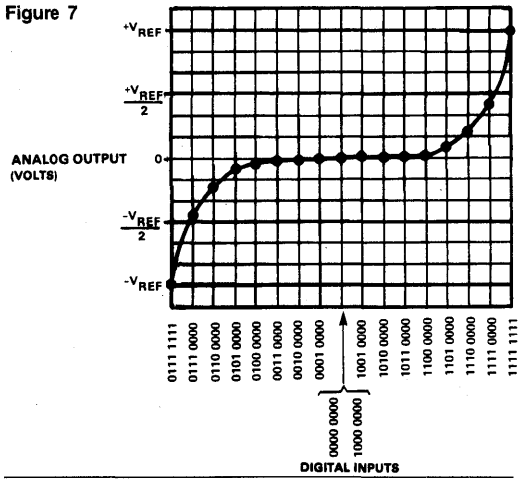
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



CLOCK to clock the serial data into its input register. RCV SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (μ-Law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV CLOCK FREQUENCIES

XMIT/RCV SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master-clock period (min.) before the next digital word is transmitted. RCV SYNC is required to be at a logic "0" state for 17 master-clock periods (min.) before the next digital word is received (refer to Figures 12 and 13).

OFFSET NULL

The offset-null feature of the MK5116 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset-adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because the resultant DC error ($V_{OFFSET0}$) will have no effect, since the output is intended to be AC-coupled to the external filter. The sign is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5116. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5116. The Digital Output of the CODEC is tied back to the Digital Input, and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5116 are connected as follows:

(1) RCV SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

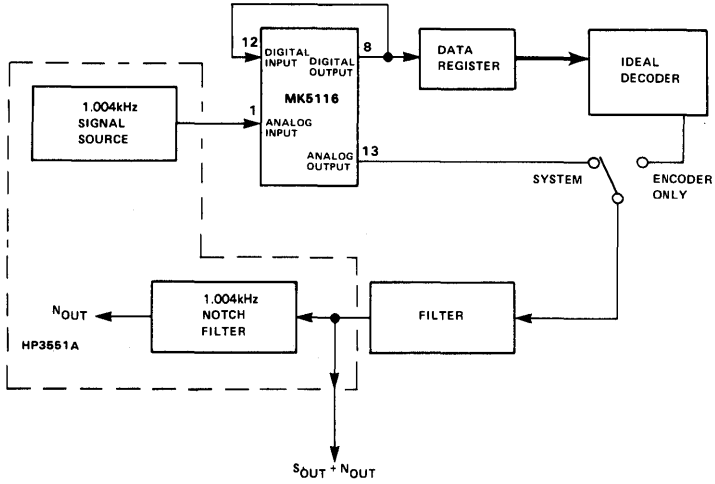
When all the above requirements are met, the setup of

Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5116 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK, and MASTER CLOCK should be separated from RCV CLOCK. XMIT and RCV SYNCS are also separated.

Some experimental results obtained with the MK5116 are shown in Figure 14 and Figure 15. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5116 exceeds the requirements for Signal-to-Distortion ratio (Figure 14) and for Gain Tracking (Figure 15).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ . . . . . +6V
DC Supply Voltage, V− . . . . . −6V
Ambient Operating Temperature, T_A . . . . . 0°C to 70°C
Storage Temperature . . . . . −55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input . . . . . $-0.5V \leq V_{IN} \leq V+$
Analog Input . . . . . $V- \leq V_{IN} \leq V+$
$+V_{REF}$ . . . . . $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ . . . . . $V- \leq -V_{REF} \leq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damages to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

ELECTRICAL OPERATING CHARACTERISITCS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V−	Negative Supply Voltage	−5.25	−5.0	−4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	−2.625	−2.5	−2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V− = −5.0V, $+V_{REF}$ = 2.5V, $-V_{REF}$ = −2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/1}$	Analog Input Offset Voltage		±1	±8	mV	2
R_{OUTA}	Analog Output Resistance		1	10	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/0}$	Analog Output Offset Voltage		+20	±850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		±0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Master and RCV Clock Input, RCV Sync Input		±0.1	±10	μA	3
I_{INHIGH_X}	Logic Input High Current (V_{In} = 2.4V) TX Clock, TX Sync		−.25	−0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		±0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I−	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	XMIT, RCV Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of PW_{CLK}	ns	
t_{RS}, t_{FS}	Sync Rise, Fall Time (XMIT, RCV)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT RCV)		$\frac{8}{F_X(F_R)}$		μs	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{PS}	Sync Pulse Period (XMIT, RCV)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC} (t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4
t_{SRC}	RVC Sync-to-RCV Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV Data Set-Up Time	50			ns	7
t_{RDH}	RCV Data Hold Time	200			ns	7
t_{RCS}	RCV Clock-to-RCV Sync Delay	200			ns	
t_{RSS}	RCV Sync Set-Up Time	200			ns	7
t_{SAO}	RCV Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW−	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

AC CHARACTERISTICS (Refer to Figures 14 and 15)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
GT_X	Gain Tracking Transmit	−.2 −.4 −1.25	0.0 ±0.1 ±0.2	+.2 +.4 +1.25	dB dB dB	Analog Input=+3 to −37dBm0 Analog Input=−37 to −50dBm0 Analog Input =−50 to −55dBm0 Relative to 0 dBm0
GT_R	Gain Tracking Receive	−.2 −.4 −1.25	0.0 ±0.1 ±0.2	±.2 +.4 +1.25	dB dB dB	Input Level=+3 to −37dBm0 Input Level=−37 to −50dBm0 Input Level=−50 to −55dBm0 Relative to 0 dBm0
GT_{E-E}	Gain Tracking End to End	−.4 −.8 −2.50	0.0 ±0.1 ±0.2	+.4 +.8 +2.50	dB dB dB	Analog Input=+3 to −37dBm0 Analog Input=−37 to −50dBm0 Analog Input=−50 to −55dBm0 Relative to 0 dBm0
SD_X	Signal to Distortion Transmit	37 31 26			dB dB dB	Analog Input=0 to −30dBm0 Analog Input= −40dBm0 Analog Input= −45dBm0
SD_R	Signal to Distortion Receive	37 31 26			dB dB dB	Input Level=0 to −30dBm0 Input Level= −40dBm0 Input Level= −45dBm0

AC CHARACTERISTICS (Refer to Figures 14 and 15)

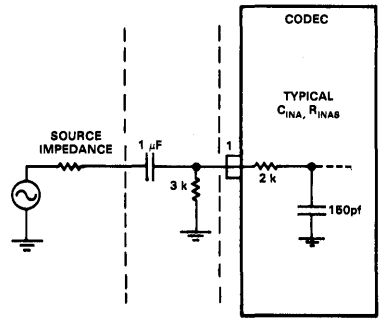
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
SD_{E-E}	Signal to Distortion End to End	35 29 24			dB dB dB	Analog Input=0 to −30 dBm0 Analog Input= −40 dBm0 Analog Input= −45 dBm0
N_X	Idle Channel Noise Transmit			17	dBnc0	Analog Input=0 Volts
N_R	Idle Channel Noise Receive			0	dBnc0	Digital Input=0 Code
N_{E-E}	Idle Channel Noise End to End			18	dBnc0	Analog Input=0 Volts Digital Output to Digital Input
CT_{RX}	Crosstalk Receive to Transmit			−80	dB	Analog In= −50 dBm0 at 2600 H_Z Digital Input= 0 dBm0 at 1008 H_Z digital
CT_{XR}	Crosstalk Transmit to Receive			−80	dB	Analog In=0 dBm0 at 1008 H_Z Digital Input=0 Code
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input-related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 9.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with I_{OH} = 100μA, I_{OL} = 500μA.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

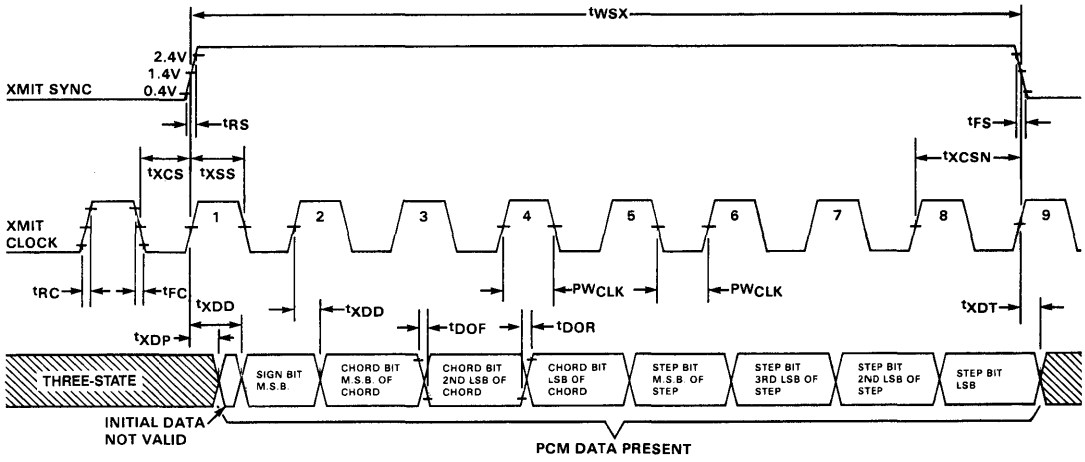
RECOMMENDED ANALOG INPUT CIRCUIT

Figure 9



TRANSMITTER SECTION TIMING

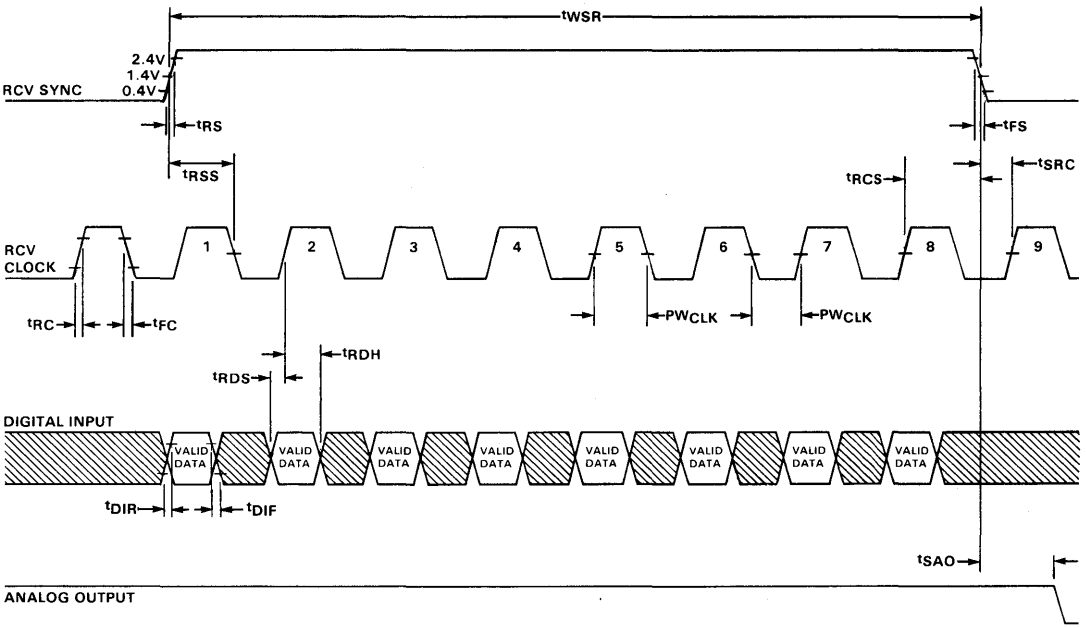
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

Figure 11

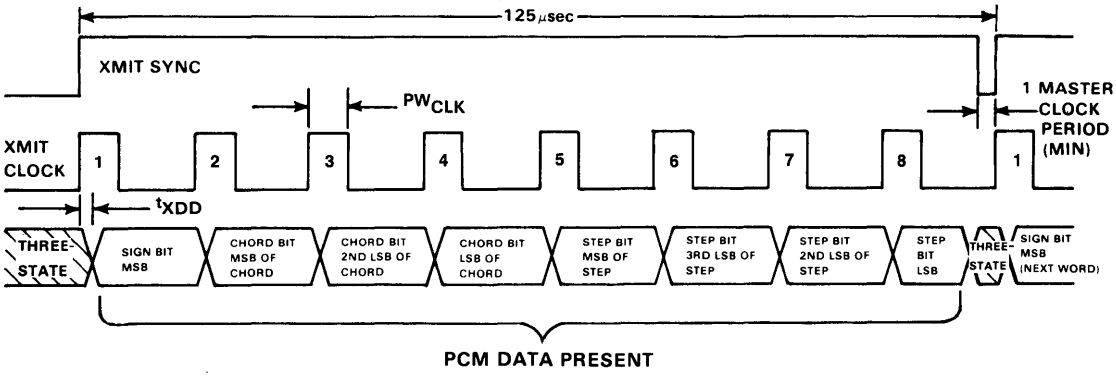


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

XVI

64kHz OPERATION, TRANSMITTER SECTION TIMING

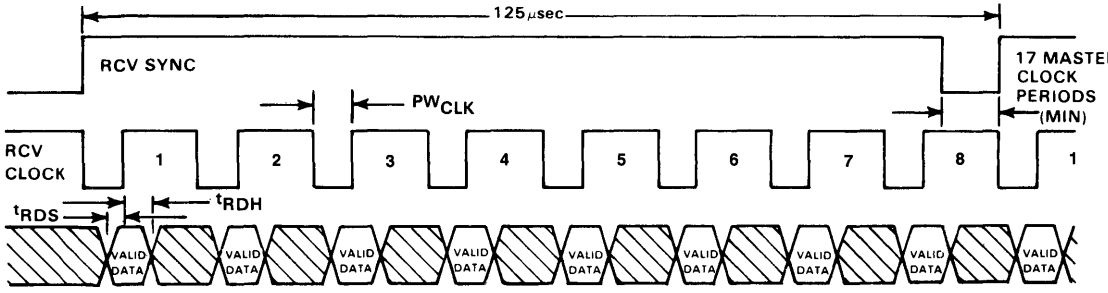
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, RECEIVER SECTION TIMING

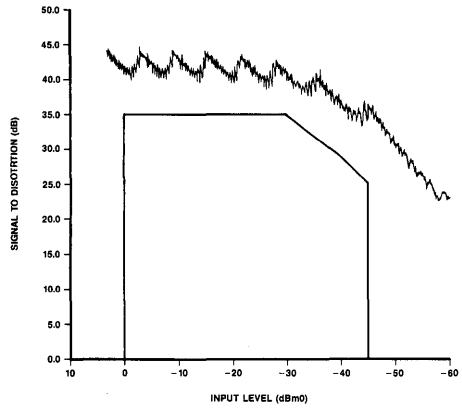
Figure 13



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

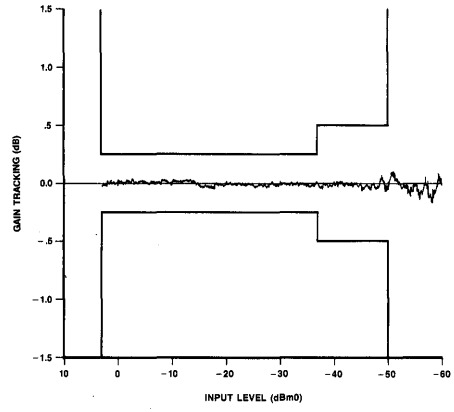
MK5116 SINGLE-ENDED SIGNAL TO DISTORTION

Figure 14



MK5116 SINGLE-ENDED GAIN TRACKING

Figure 15



μ-255 LAW COMPANDING CODEC MK5151(J/P)

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- **Follows the μ-255 Companding Law**
- Zero Code Suppression and Sign-Magnitude Data Format
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 24-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s - 2.1Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

DESCRIPTION

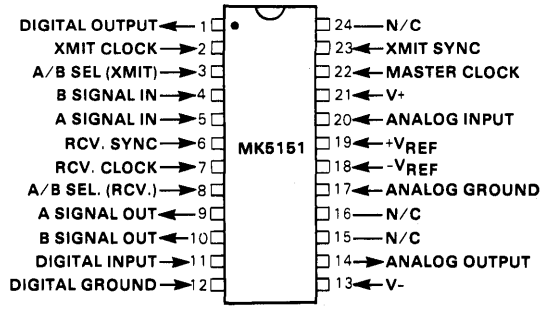
The MK5151 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the μ-255 companding law and (2) a digital-to-analog converter which also conforms to the μ-255 law.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in telephone digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

The pin configuration of the MK5151 is shown in Figure 1.

PIN CONNECTIONS

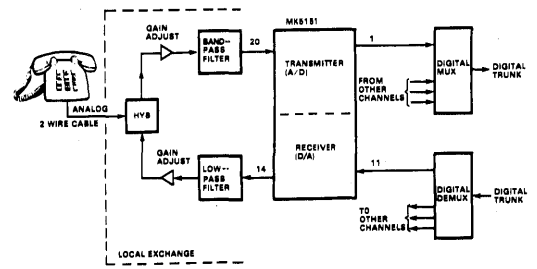
Figure 1



A block diagram of a PCM system using the MK5151 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM

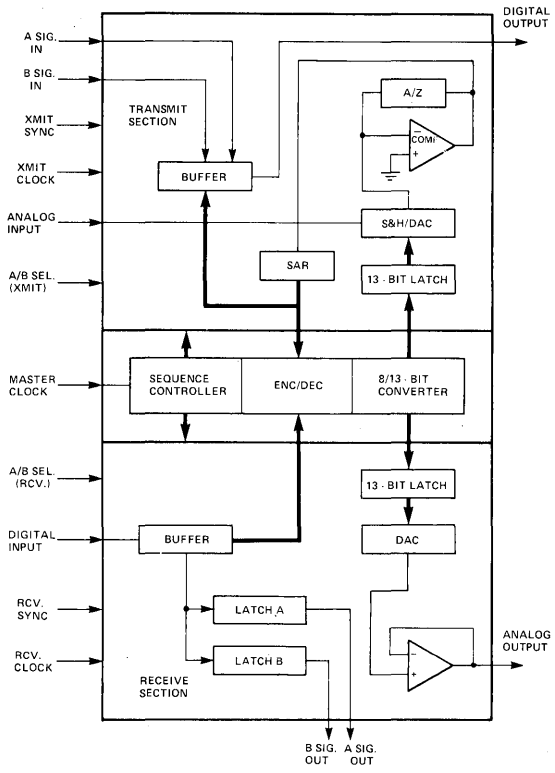
Figure 2



XVI

FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5151 BLOCK DIAGRAM
Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 19 and 18

These inputs provide the conversion references for the digital-to-analog converters in the MK5151. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 20

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 11.

MASTER CLOCK, Pin 22

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 23 (Refer to Figure 12 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word. (Refer to Figure 14).

XMIT CLOCK, Pin 2 (Refer to Figure 12 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5151 is unloaded at the clock rate present on this pin. Clock rates of 64kHz - 2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 6 (Refer to Figure 13 for the timing diagram)

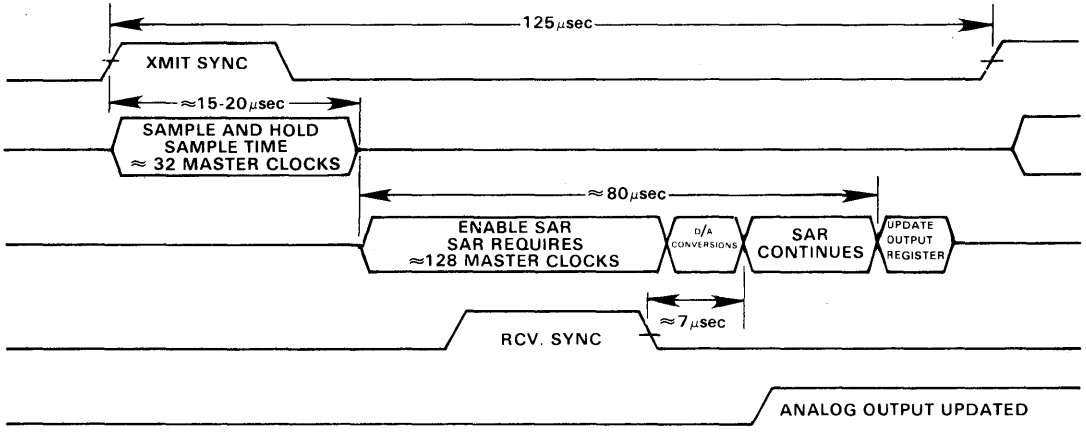
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 15).

RCV CLOCK, Pin 7 (Refer to Figure 13 for Timing Diagram)

The on-chip 8-bit shift register for the MK5151 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this

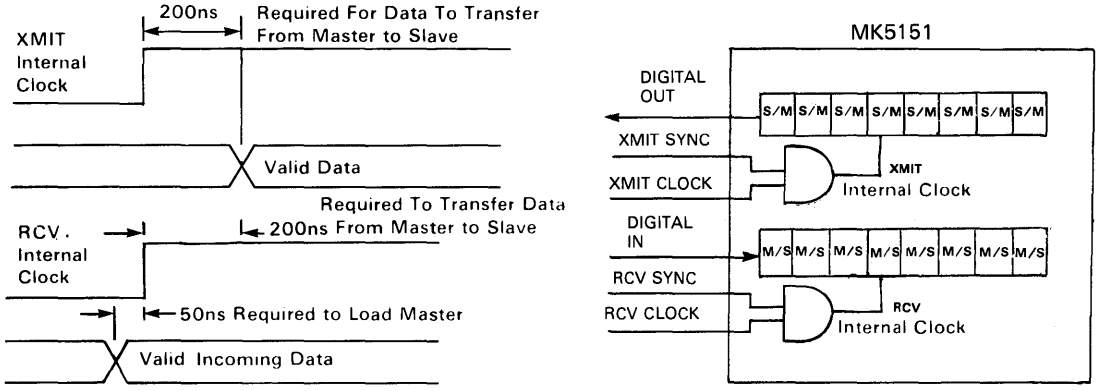
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 1

The MK5151 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first Chord, the Step Bit has a value of 0.6mV. In the second Chord, the Step Bit has a value of 1.2mV. This doubling of the step value continues for each of the six successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the μ-255 law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (μ-law Encoder) is shown in Figure 6.

DIGITAL OUTPUT CODE μ-LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	111	0.0mV	0.613mV
2.	110	10.11mV	1.226mV
3.	101	30.3mV	2.45mV
4.	100	70.8mV	4.90mV
5.	011	151.7mV	9.81mV
6.	010	313mV	19.61mV
7.	001	637mV	39.2mV
8.	000	1.284V	78.4mV

EXAMPLE:

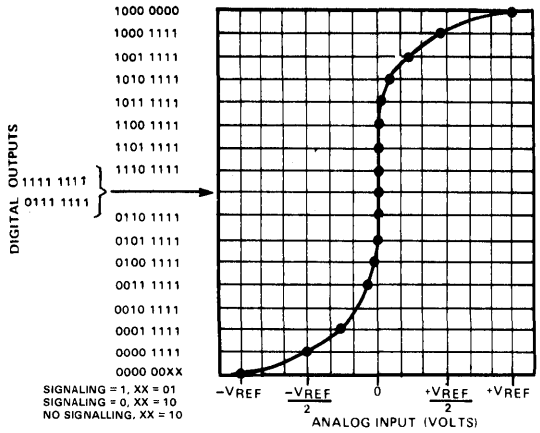
1 100 1101 = +70.8mV + (2 x 4.90mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

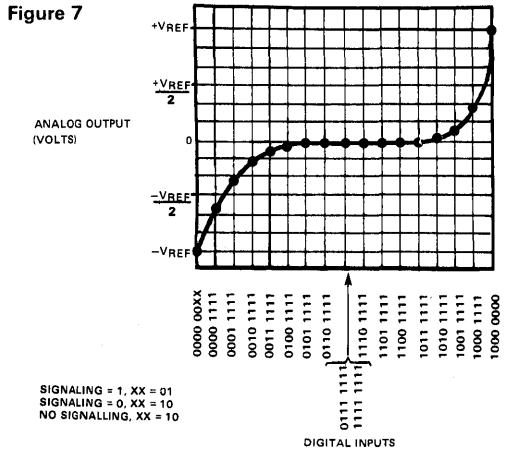
A/D CONVERTER (μ-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (μ-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



DIGITAL INPUT, Pin 11

The MK5151 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 13. When RCV. SYNC goes high, the MK5151 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the SERIAL OUTPUT. The transfer characteristic of the D/A converter (μ-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 14

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal. When the 8th bit of the word is a signalling bit, it is assigned a value of ½ step. This results in a lower system quantization error rate than would result if the bit were arbitarily set to 0 (no step) or 1 (full step).

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 14 and 15).

A/B SIGNAL IN, Pins 4 and 5

These two pins allow insertion of signalling information into the transmitted data stream. The inserted information occurs as the 8th bit (LSB) in the transmitted word. A positive transition occuring on A/B SEL (XMIT) selects A SIGNAL IN while a negative transition selects B SIGNAL IN.

A/B SIGNAL OUT, Pins 9 and 10

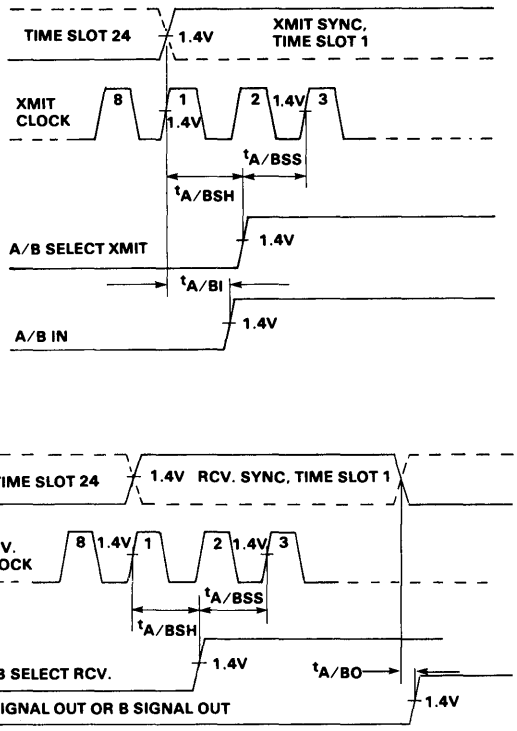
These two pins are provided to output received signalling information. A positive transition on A/B SEL (RCV.) routes the signal bit to A SIGNAL OUT while a negative transition routes the signal bit (bit 8) to B SIGNAL OUT. Refer to Figure 8.

A/B SEL (XMIT), Pin 3

This input selects either A SIGNAL IN or B SIGNAL IN as described in the A/B SIGNAL IN paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

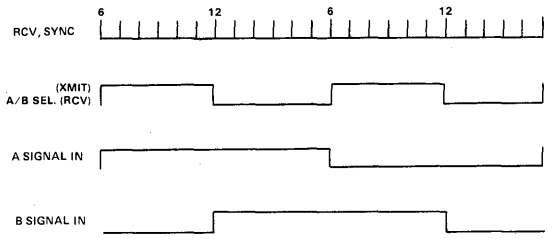
A/B SELECT TIMING

Figure 8



SIGNALLING TIMING REQUIREMENTS FOR PERFORMANCE EVALUATION

Figure 9



A/B SEL (RCV.), Pin 8

This input routes the signalling bit, bit 8, either to A SIGNAL OUT or to B SIGNAL OUT as described in the A/B SIGNAL OUT paragraph above, and should be changed only at the start of the 6th and 12th frames as shown in Figure 9.

OFFSET NULL

The offset null feature of the MK5151 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 10 can be used to evaluate the performance of the MK5151. An analog signal provided by the HP3551A Transmission Test Set is connected to the Analog Input (Pin 20) of the MK5151. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3551A. Remaining pins of the MK5151 are connected as follows:

(1) A/B SEL. (RCV.) is tied to A/B SEL. (XMIT).
(2) RCV. SYNC is tied to XMIT SYNC.
(3) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 MASTER CLOCK periods

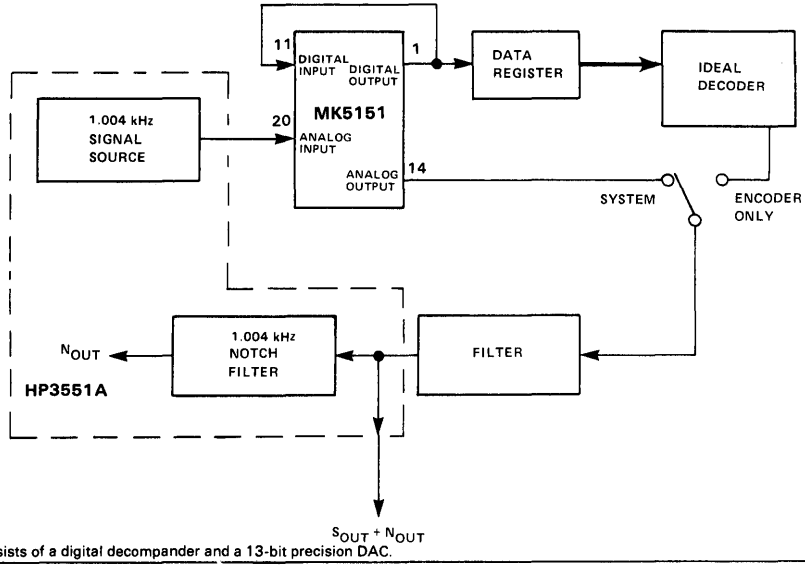
Additional timing signals are shown in Figure 9.

When all the above requirements are met, the setup of Figure 10 permits the measurement of synchronous system performance over a wide range of analog inputs. The data register and ideal decoder provide a means of checking the encoder portion of the MK5151 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also.

Some experimental results obtained with the MK5151 are shown in Figure 16 and Figure 17. In each case, both the measured results and the corresponding D3 Channel Bank specifications are shown. The MK5151 exceeds the requirements for Signal-to-Distortion ratio (Figure 17) and for Gain Tracking (Figure 16).

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 10



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... –6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... –55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq +V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq 0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS

POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	–5.25	–5.0	–4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	–2.625	–2.5	–2.375	V	1

TEST CONDITIONS: V+ = 5.0 V, V- = -5.0 V, + V_{REF} = 2.5 V, -V_{REF} = -2.5 V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2

DC CHARACTERISTICS CONTINUED

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	±8	mV	2
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
$V_{OFFSET/O}$	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Logic Output Low Voltage Digital Output, A/B Signal Out			0.4	V	4
$V_{OUTHIGH}$	Logic Output High Voltage Digital Output, A/B Signal Out	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I-	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 12 and Figure 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	1.544	2.1	MHz	
F_R, F_X	Receive, Transmit Clock Frequency	0.064	1.544	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}	Clock Rise Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS},t_{FS}	Sync Fall, Rise Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR}, t_{DIF}	Digital Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50%of t_{FC} (t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4

AC CHARACTERISTICS CONTINUED (Refer to Figure 12 and 13)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	7
t_{RDH}	RCV. Data Hold Time	200			ns	7
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	7
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
$t_{A/BI}$	A/B Signalling Input Setup Time			200	ns	
$t_{A/BSH}$	A/B Select Hold Time	200			ns	
$t_{A/BSS}$	A/B Select Setup Time	400			ns	
$t_{A/BO}$	A/B Signalling Output Delay		200	400	ns	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW–	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

SYSTEM CHARACTERISTICS (Refer to Figures 16 and 17)

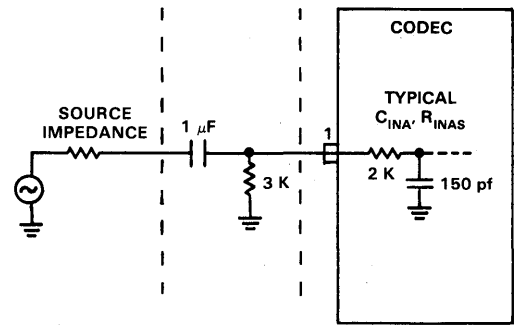
SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		10	18	dBrnc0	Analog Input=0 Volts Note 2
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

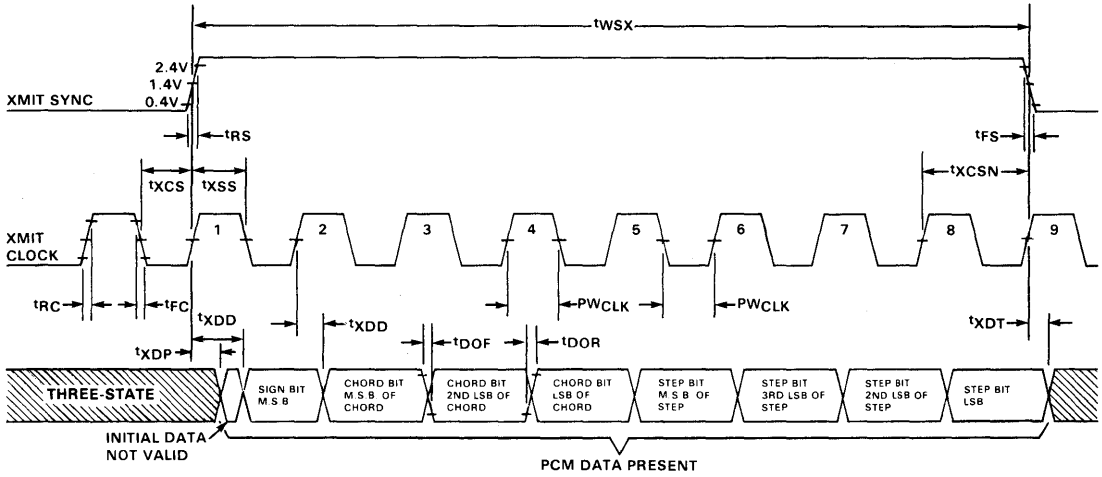
1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 11.
3. When a transistion from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with I_{OH} = -100μA, I_{OL} = 500μA.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping CLOCK and SYNC.
7. The first bit of data is loaded when the Sync and Clock are both "1" during bit time 1 as shown on RCV timing diagram.

RECOMMENDED ANALOG INPUT CIRCUIT

Figure 11

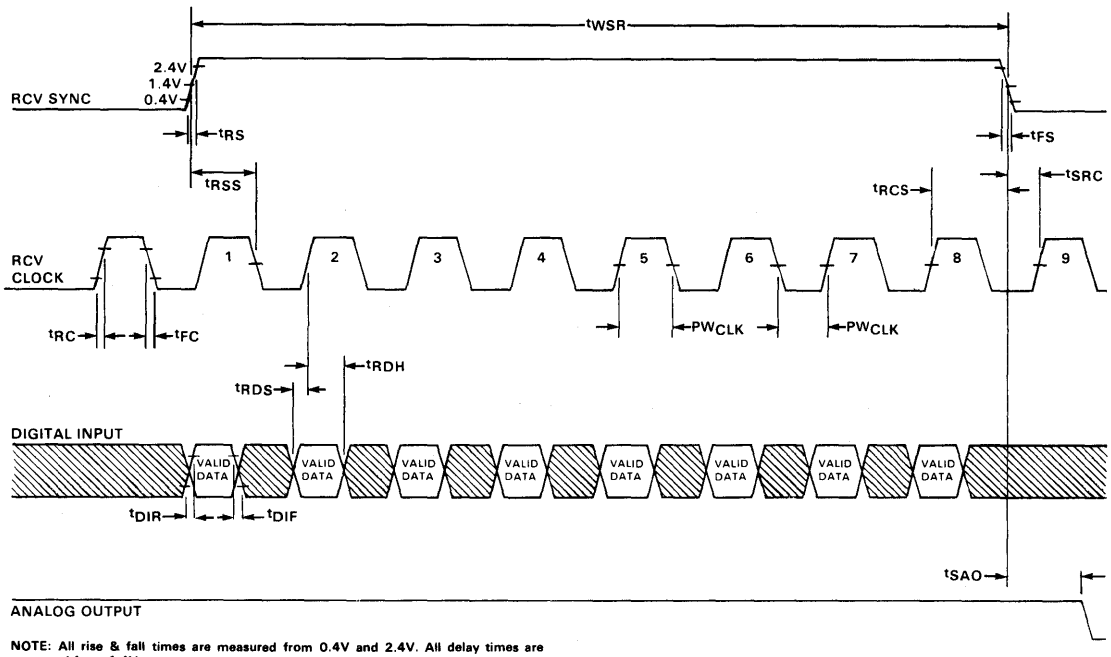


TRANSMITTER SECTION TIMING
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V.
All delay times are measured from 1.4V.

RECEIVER SECTION TIMING
Figure 13

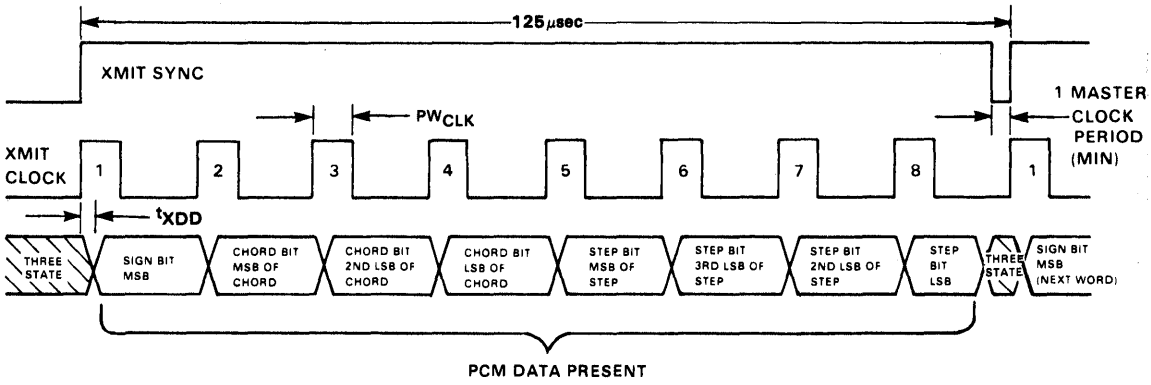


NOTE: All rise & fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

XVI

64kHz OPERATION, TRANSMITTER SECTION TIMING

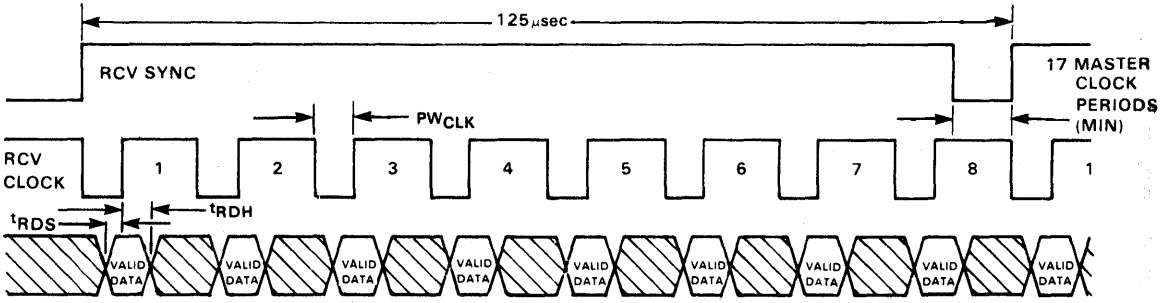
Figure 14



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

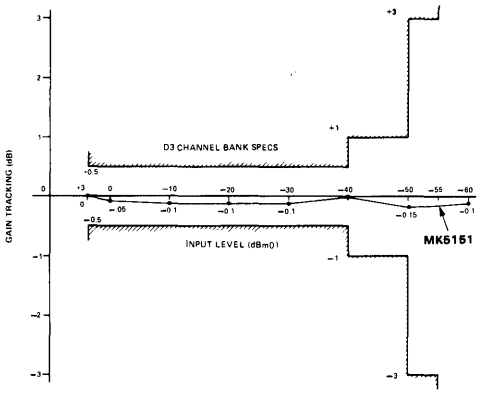
64kHz OPERATION, RECEIVER SECTION TIMING

Figure 15

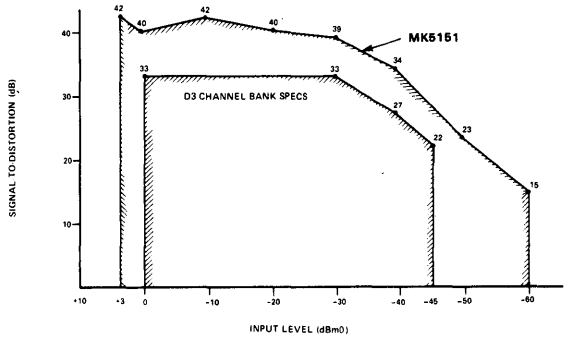


NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

MK5151 GAIN TRACKING PERFORMANCE
Figure 16



MK5151 S/D RATIO VS. INPUT LEVEL
Figure 17



XVI

A-LAW COMPANDING CODEC MK5156(J/P)

FEATURES

- ±5-Volt Power Supplies
- Low Power Dissipation - 30mW (Typ)
- Follows the A-Law Companding Code
- Includes CCITT Recommended Even-Order-Bit Inversion
- Synchronous or Asynchronous Operation
- On-Chip Sample and Hold
- On-Chip Offset Null Circuit Eliminates Long-Term Drift Errors and Need for Trimming
- Single 16-Pin Package
- Minimal External Circuitry Required
- Serial Data Output of 64kb/s-2.1 Mb/s at 8kHz Sampling Rate
- Separate Analog and Digital Grounding Pins Reduce System Noise Problems

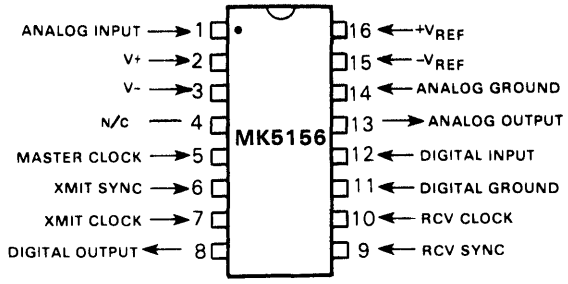
DESCRIPTION

The MK5156 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristic conforming to the A-law companding code and (2) a digital-to-analog converter which also conforms to the A-law code.

These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in digital switching and transmission systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64kb/s-2.1 Mb/s rate with analog signal sampling occuring at an 8kHz rate. A sync pulse input is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line.

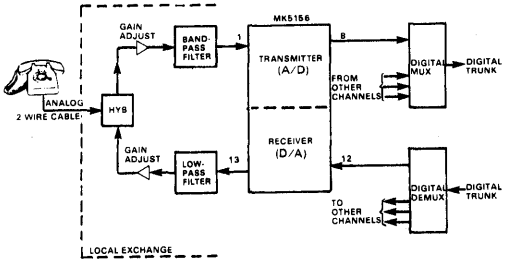
The pin configuration of the MK5156 is shown in Figure 1.

PIN CONNECTIONS
Figure 1



A block diagram of a PCM system using the MK5156 is shown in Figure 2.

PCM SYSTEM BLOCK DIAGRAM
Figure 2

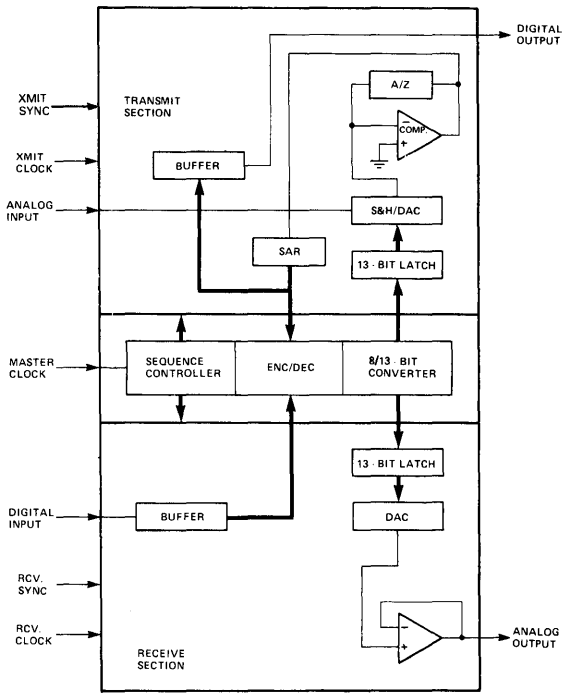


XVI

FUNCTIONAL DESCRIPTION: (Refer to Figure 3 for a Block Diagram)

MK5156 BLOCK DIAGRAM

Figure 3



POSITIVE AND NEGATIVE REFERENCE VOLTAGES ($+V_{REF}$ and $-V_{REF}$) Pins 16 and 15

These inputs provide the conversion references for the digital-to-analog converters in the MK5156. $+V_{REF}$ and $-V_{REF}$ must maintain 100ppM/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

ANALOG INPUT, Pin 1

Voice-frequency analog signals which are bandwidth-limited to 4kHz are input at this pin. Typically, they are then sampled at an 8kHz rate (Refer to Figure 4.). The analog input must remain between $+V_{REF}$ and $-V_{REF}$ for accurate conversion. The recommended input interface circuit is shown in Figure 9.

MASTER CLOCK, Pin 5

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV. SYNC, RCV. CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

XMIT SYNC, Pin 6 (Refer to Figure 10 for the Timing Diagram)

This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word. (Refer to Figure 12).

XMIT CLOCK, Pin 7 (Refer to Figure 10 for the Timing Diagram)

The on-chip 8-bit output shift register of the MK5156 is unloaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 5). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

RCV. SYNC, Pin 9 (Refer to Figure 11 for the Timing Diagram)

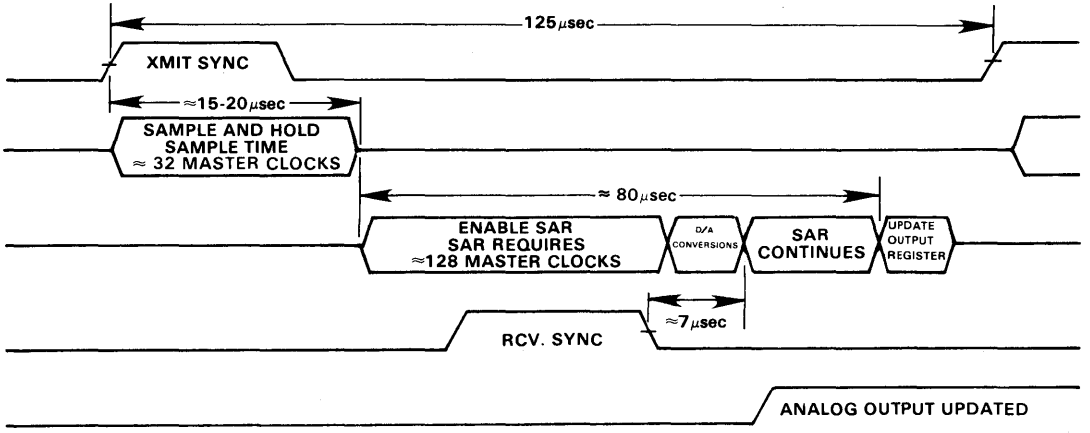
This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 4). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 13).

RCV CLOCK, Pin 10 (Refer to Figure 11 for Timing Diagram)

The on-chip 8-bit shift register for the MK5156 is loaded at the clock rate present on this pin. Clock rates of 64kHz-2.1MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 5). This set up time, t_{RDS}, allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time, t_{RDH}, is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In

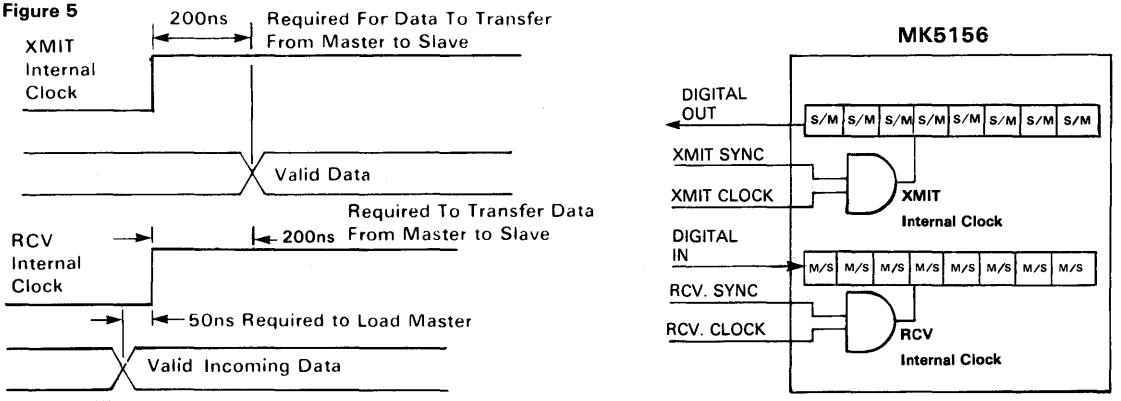
A/D, D/A CONVERSION TIMING

Figure 4



DATA INPUT/OUTPUT TIMING

Figure 5



this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

DIGITAL OUTPUT, Pin 8

The MK5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2mV. In the third Chord, the Step Bit has a value of 2.4mV. This doubling of the step value continues for each of the five successive Chords.

Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 6.

DIGITAL INPUT, Pin 12

The MK5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 11. When RCV. SYNC goes high, the MK5156 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The

DIGITAL OUTPUT CODE: A LAW

Table 1

	Chord Code	Chord Value	Step Value
1.	101	0.0mV	1.221mV
2.	100	20.1mV	1.221mV
3.	111	40.3mV	2.44mV
4.	110	80.6mV	4.88mV
5.	001	161.1mV	9.77mV
6.	000	332mV	19.53mV
7.	011	645mV	39.1mV
8.	010	1.289V	78.1mV

EXAMPLE:

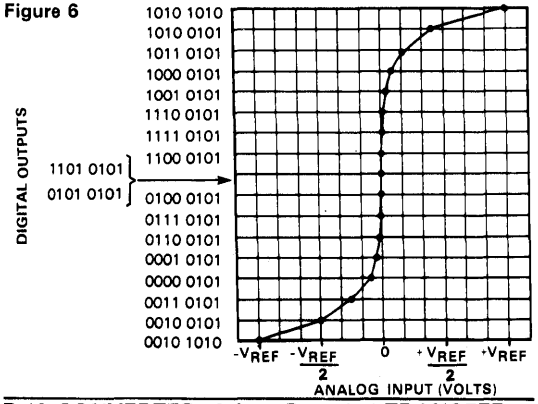
1 110 0111= +80.6mV+ (2 x 4.88mV)

Sign Bit Chord Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

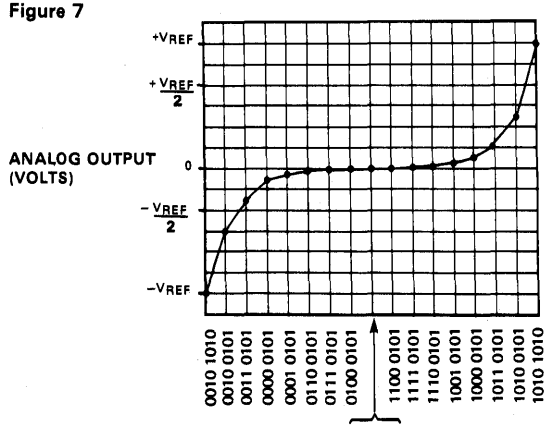
A/D CONVERTER (A-Law Encoder) TRANSFER CHARACTERISTIC

Figure 6



D/A CONVERTER (A-Law Decoder) TRANSFER CHARACTERISTIC

Figure 7



transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 7.

ANALOG OUTPUT, Pin 13

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with sinx/x correction to recreate the sampled voice signal.

OPERATION OF CODEC WITH 64kHz XMIT/RCV. CLOCK FREQUENCIES

XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figures 12 and 13).

OFFSET NULL

The offset null feature of the MK5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ($V_{OFFSET/O}$) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

PERFORMANCE EVALUATION

The equipment connections shown in Figure 8 can be used to evaluate the performance of the MK5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the MK5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the MK5156 are connected as follows:

(1) RCV. SYNC is tied to XMIT SYNC
(2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.

The following timing signals are required:

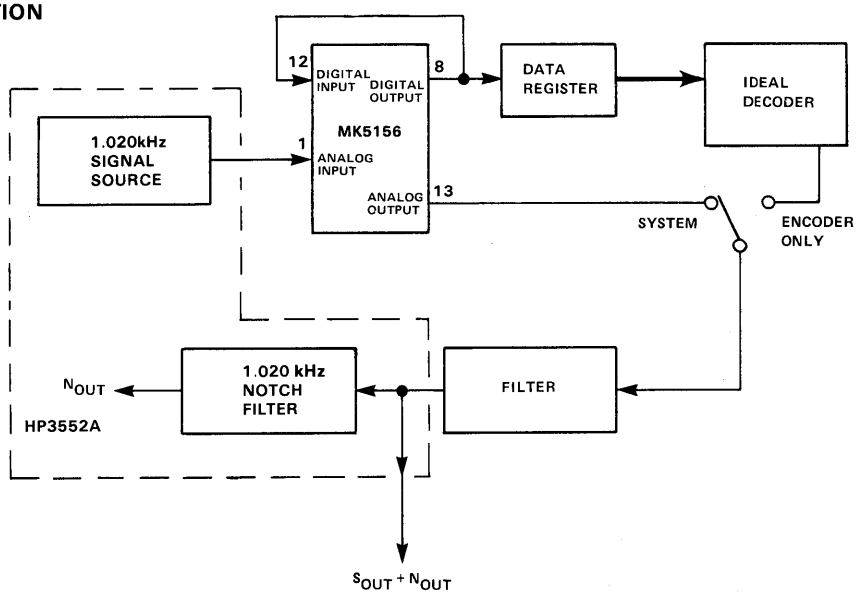
(1) MASTER CLOCK = 1.536 MHz
(2) XMIT SYNC repetition rate = 8kHz
(3) XMIT SYNC width = 8 XMIT CLOCK periods

When all the above requirements are met, the setup of Figure 8 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the MK5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the MK5156 are shown in Figures 14 and 15.

SYSTEM CHARACTERISTICS TEST CONFIGURATION

Figure 8



NOTE: The ideal decoder consists of a digital decompander and a 13-bit precision DAC.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage, V+ ..... +6V
DC Supply Voltage, V– ..... -6V
Ambient Operating Temperature, T_A ..... 0°C to 70°C
Storage Temperature ..... –55°C to +125°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB) 500mW
Digital Input ..... $-0.5V \leq V_{IN} \leq V+$
Analog Input ..... $V- \leq V_{IN} \leq V+$
$+V_{REF}$ ..... $-0.5V \leq +V_{REF} \leq V+$
$-V_{REF}$ ..... $V- \leq -V_{REF} \leq +0.5V$

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL OPERATING CHARACTERISTICS
POWER SUPPLY REQUIREMENTS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V–	Negative Supply Voltage	–5.25	–5.0	–4.75	V	
$+V_{REF}$	Positive Reference Voltage	2.375	2.5	2.625	V	1
$-V_{REF}$	Negative Reference Voltage	–2.625	–2.5	–2.375	V	1

TEST CONDITIONS: V+ = 5.0V, V- = -5.0V, + V_{REF} = 2.5V, -V_{REF} = -2.5V, T_A = 0°C to 70°C

DC CHARACTERISTICS

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
R_{INAS}	Analog Input Resistance During Sampling		2		kΩ	2
R_{INANS}	Analog Input Resistance Non-Sampling		100		MΩ	
C_{INA}	Analog Input Capacitance		150	250	pF	2
$V_{OFFSET/I}$	Analog Input Offset Voltage		±1	± 8	mV	2
R_{OUTA}	Analog Output Resistance		20	50	Ω	
I_{OUTA}	Analog Output Current	0.25	0.5		mA	
($V_{OFFSET/O}$)	Analog Output Offset Voltage		-200	± 850	mV	
I_{INLOW}	Logic Input Low Current (V_{IN} = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	±10	μA	3
I_{INHIGH}	Logic Input High Current (V_{IN} = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C_{DO}	Digital Output Capacitance		8	12	pF	
I_{DOL}	Digital Output Leakage Current		± 0.1	±10	μA	
V_{OUTLOW}	Digital Output Low Voltage			0.4	V	4
$V_{OUTHIGH}$	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	5
I-	Negative Supply Current		2	6	mA	5
I_{REF+}	Positive Reference Current		4	20	μA	
I_{REF-}	Negative Reference Current		4	20	μA	

AC CHARACTERISTICS (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
F_M	Master Clock Frequency	1.5	2.048	2.1	MHz	
F_R, F_X	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
PW_{CLK}	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
t_{RC}, t_{FC}	Clock Rise, Fall Time (MASTER, XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{RS},t_{FS}	Sync Rise, Fall Time (XMIT, RCV.)			25% of PW_{CLK}	ns	
t_{DIR},t_{DIF}	Data Input Rise, Fall Time			25% of PW_{CLK}	ns	
t_{WSX}, t_{WSR}	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		μs	
t_{PS}	Sync Pulse Period (XMIT, RCV.)		125		μs	
t_{XCS}	XMIT Clock-to-XMIT Sync Delay	50% of t_{FC}(t_{RS})			ns	6
t_{XCSN}	XMIT Clock-to-XMIT Sync (Negative Edge) Delay	200			ns	

AC CHARACTERISTICS CONTINUED (Refer to Figure 10 and Figure 11)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
t_{XSS}	XMIT Sync Set-Up Time	200			ns	
t_{XDD}	XMIT Data Delay	0		200	ns	4
t_{XDP}	XMIT Data Present	0		200	ns	4
t_{XDT}	XMIT Data Three State			150	ns	4
t_{DOF}	Digital Output Fall Time		50	100	ns	4
t_{DOR}	Digital Output Rise Time		50	100	ns	4
t_{SRC}	RCV. Sync-to-RCV. Clock Delay	50% of t_{RC} (t_{FS})			ns	6
t_{RDS}	RCV. Data Set-Up Time	50			ns	7
t_{RDH}	RCV. Data Hold Time	200			ns	7
t_{RCS}	RCV. Clock-to-RCV. Sync Delay	200			ns	
t_{RSS}	RCV. Sync Set-Up Time	200			ns	7
t_{SAO}	RCV. Sync-to-Analog Output Delay		7		μs	
SLEW+	Analog Output Positive Slew Rate		1		V/μs	
SLEW-	Analog Output Negative Slew Rate		1		V/μs	
DROOP	Analog Output Droop Rate		25		μV/μs	

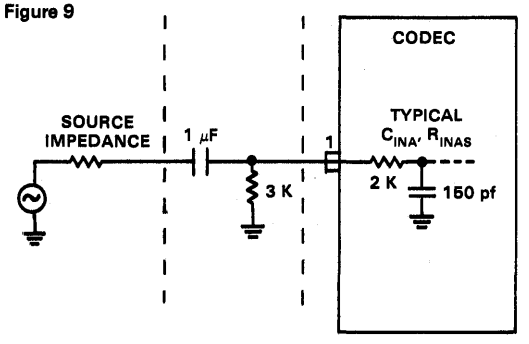
SYSTEM CHARACTERISTICS (Refer to Figures 14 and 15)

SYM	PARAMETER	MIN	TYP	MAX	UNITS	TEST COND.
S/D	Signal-to-Distortion Ratio	35 29 24	39 34 29		dB dB dB	Analog Input=0 to -30dBm0 Analog Input=-40dBm0 Analog Input=-45dm0
GT	Gain Tracking	-0.4 -0.8 -2.5	±0.1 ±0.1 ±0.2	+0.4 +0.8 +2.5	dB dB dB	Analog Input=+3 to -37dBm0 Analog Input=-37 to -50dBm0 Analog Input=-50 to -55dBm0
N_{IC}	Idle Channel Noise		-80	-68	dBm0p	Analog Input=0 Volts; note 2.
TLP	Transmission Level Point		+4		dB	600Ω

NOTES:

1. $+V_{REF}$ and $-V_{REF}$ must be matched within ± 1% in order to meet system requirements.
2. Sampling is accomplished by charging an internal capacitor; therefore, the designer should avoid excessive source impedance. Input related device characteristics are derived using the Recommended Analog Input Circuit. See Figure 9.
3. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving 30pF with I_{OH} = -100 μA, I_{OL} = 500 μA.
5. Results in 30 mW typical power dissipation (clocks applied) under normal operating conditions.
6. This delay is necessary to avoid overlapping Clock and Sync.
7. The first bit of data is loaded when Sync and Clock are both "1" during bit time 1 as shown on RCV. timing diagram.

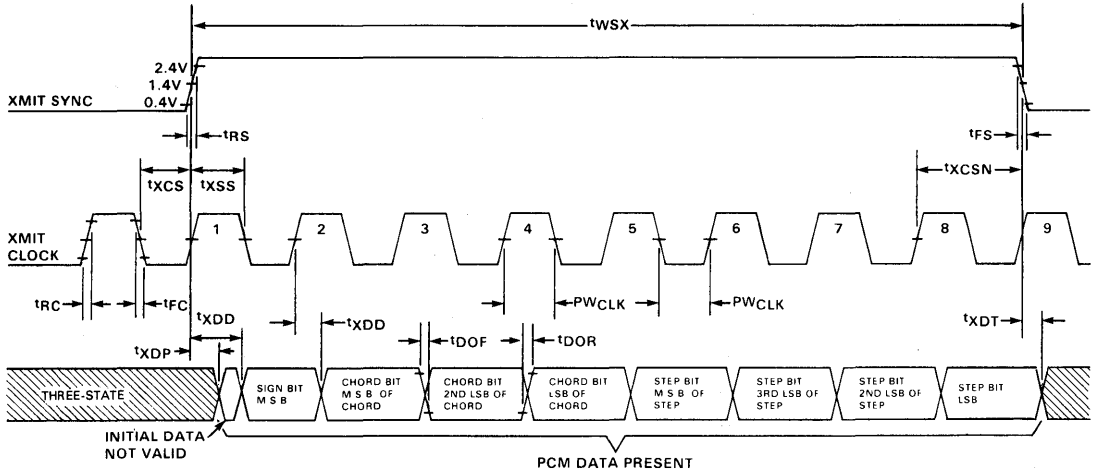
RECOMMENDED ANALOG INPUT CIRCUIT
Figure 9



XVI

TRANSMITTER SECTION TIMING

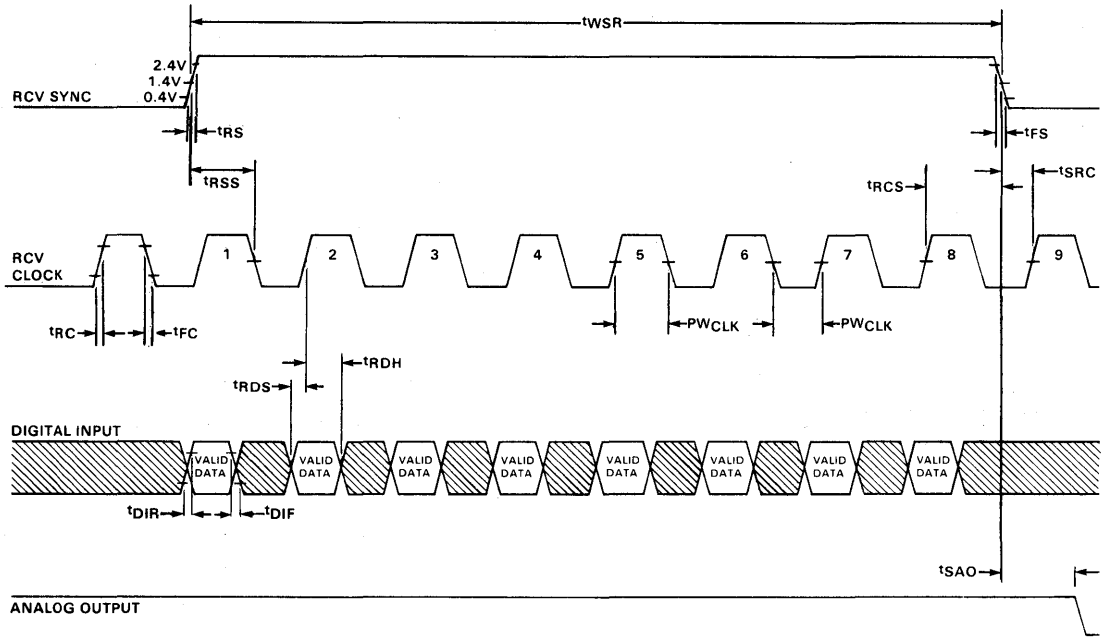
Figure 10



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

RECEIVER SECTION TIMING

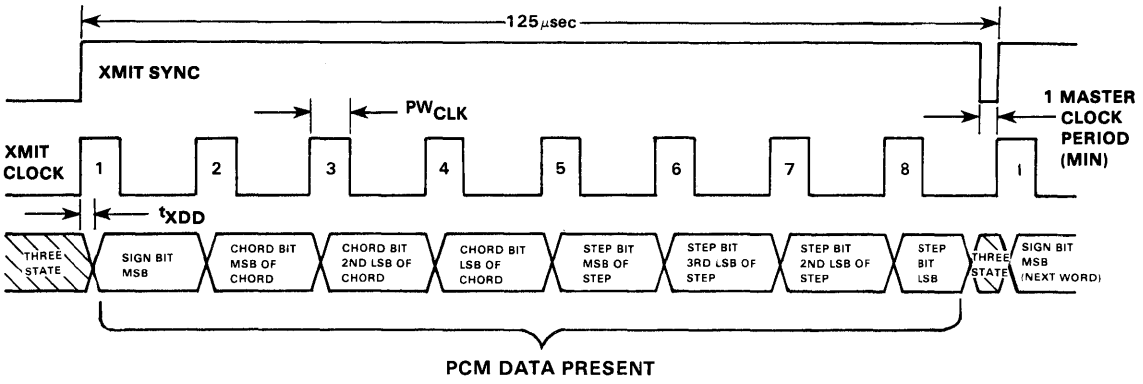
Section 11



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, TRANSMITTER SECTION TIMING

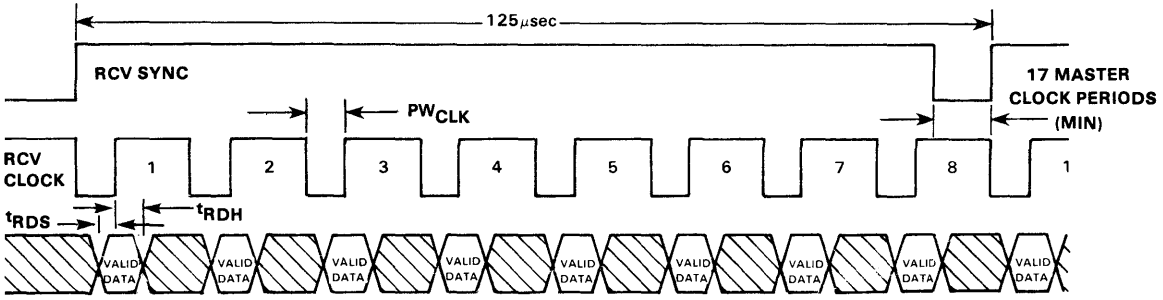
Figure 12



NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

64kHz OPERATION, RECEIVER SECTION TIMING

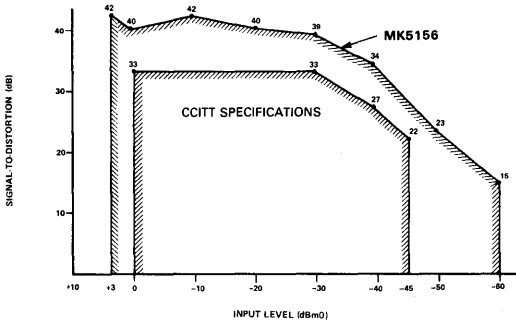
Figure 13



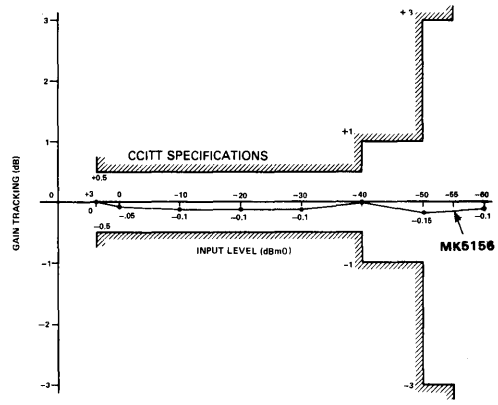
NOTE: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

XVI

MK5156 S/D RATIO VS. INPUT LEVEL
Figure 14



M5156 GAIN TRACKING PERFORMANCE
Figure 15



ADVANCE INFORMATION

COMPANDING CODEC WITH FILTERS MK5316(J)

FEATURES

- ☐ Per-channel, single-chip CODEC with filters
- ☐ AT&T D3/D4 and CCITT compatible
- ☐ Pin-programmable μ-law/power-down
- ☐ On-chip voltage references
- ☐ ±5 volt power supplies, ±5%
- ☐ Low power dissipation
  - 40 mW operating (typ)
  - .5 μW power down (typ)
- ☐ TTL/CMOS-compatible digital inputs and outputs
- ☐ Gain adjust available at the transmit and receive filter stages
- ☐ Synchronous or asynchronous operation
- ☐ Serial data rate from 64 kb/s to 4.096 Mb/s
- ☐ Separate internal analog and digital grounds reduce system noise problems
- ☐ Single 16-pin package
- ☐ Minimal external component count

DESCRIPTION

The MK5316 is a monolithic device containing a companding CODEC and PCM filters on a single chip. This device has been designed to meet the needs of the telecommunications industry for per-channel, voice-frequency CODECs and PCM filters. Both the transmit and receive sections have been incorporated into a single package with negligible loss of crosstalk immunity. Typical device applications are PBX systems, central offices, channel banks, and other telephone digital switching and transmission systems.

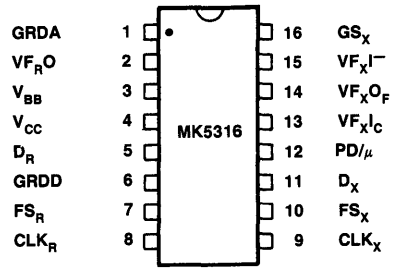
The MK5316 transmit section is composed of an input amplifier, a band-pass filter, and a compressing A/D converter. The operational amplifier output is available for use in an inverting gain configuration at the transmit stage. By disabling the amplifier, this output can be used as a noninverting high-impedance input to the band-pass filter. The band-pass, switched-capacitor filter provides rejection of the 50-60 Hz power line frequency and the band-limiting required for an 8 kHz sampling system. The A/D converter transforms the band-limited, voice-frequency signals into 8-bit words using one of two selectable companding laws. The encoded data is transmitted in a serial format under the control of a data clock and a frame synchronization input.

The receive section of the MK5316 is composed of an expanding D/A converter and a low-pass filter. The D/A converter receives 8-bit words in a serial format under control of a data clock and a frame synchronization input. The low-pass, switched-capacitor filter smooths the voltage steps of the D/A converter and provides compensation for the sinx/x decoder response. The receive filter output may then be adjusted to system levels by use of a voltage divider network.

Pin connections for the MK5316 are shown in Figure 1.

PIN CONNECTIONS

Figure 1



XVI

ADVANCE INFORMATION

COMPANDING CODEC WITH FILTERS MK5320(J)

FEATURES

- ☐ Per-channel, single-chip CODEC with filters and receive power amplifiers
- ☐ AT&T D3/D4 and CCITT compatible
- ☐ Pin-programmable μ-law/A-law/power-down
- ☐ On-chip voltage references
- ☐ $\pm$5 volt power supplies, $\pm$5%
- ☐ Low power dissipation
  - 40 mW typical without power amplifiers
  - .5 μW typical in power down mode
- ☐ TTL/CMOS-compatible digital inputs and outputs
- ☐ Gain adjust available at the transmit and receive filter stages
- ☐ Synchronous or asynchronous operation
- ☐ Serial data rate from 64 kb/s to 4.096 Mb/s
- ☐ Separate internal analog and digital grounds reduce system noise problems
- ☐ Single 20-pin 300-mil package
- ☐ Minimal external component count

DESCRIPTION

The MK5320 is a monolithic silicon-gate CMOS device containing a companding CODEC, PCM filters, and receive power amplifiers on a single chip. This device has been designed to meet the needs of the telecommunications industry for per-channel, voice-frequency CODECs and PCM filters. Both the transmit and receive sections have been incorporated into a single package with negligible loss of crosstalk immunity. Typical device applications are PBX systems, central offices, channel banks, and other telephone digital switching and transmission systems.

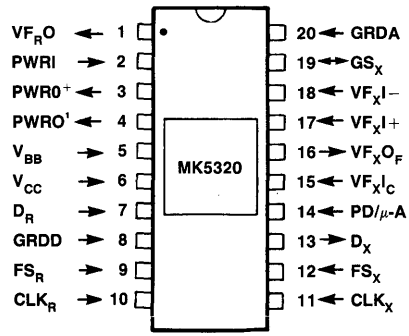
The MK5320 transmit section is composed of an input amplifier, a band-pass filter, and a compressing A/D converter. The operational amplifier output is available for use in a gain configuration at the transmit stage. By disabling the amplifier, this output can be used as a noninverting high-impedance input to the band-pass filter. The band-pass, switched-capacitor filter provides rejection of the 50-60 Hz power line frequency and the band-limiting required for an 8 kHz sampling system. The A/D converter transforms the band-limited, voice-frequency signals into 8-bit words using one of two selectable companding laws. The encoded data is transmitted in a serial format under the control of a data clock and a frame synchronization input.

The receive section of the MK5320 is composed of an expanding D/A converter, a low pass filter, and a differential power amplifier pair. The D/A converter receives 8-bit words in a serial format under control of a data clock and a frame synchronization input. The low-pass, switched-capacitor filter smooths the voltage steps of the D/A converter and provides compensation for the sinx/x decoder response. The receive filter output may then be adjusted to system levels by use of a voltage divider network. The differential power amplifier pair is available for use in applications requiring low-impedance drive capability.

Pin connections for the MK5320 are shown in Figure 1.

PIN CONNECTIONS

Figure 1



XVI

ADVANCE INFORMATION

COMPANDING CODEC WITH FILTERS MK5356(J)

FEATURES

- ☐ Per-channel, single-chip CODEC with filters
- ☐ CCITT compatible
- ☐ Pin-programmable A-law/power-down
- ☐ On-chip voltage references
- ☐ ±5 volt power supplies, ±5%
- ☐ Low power dissipation
  - 40 mW operating (typ)
  - .5 μW power down (typ)
- ☐ TTL/CMOS-compatible digital inputs and outputs
- ☐ Gain adjust available at the transmit and receive filter stages
- ☐ Synchronous or asynchronous operation
- ☐ Serial data rate from 64 kb/s to 4.096 Mb/s
- ☐ Separate internal analog and digital grounds reduce system noise problems
- ☐ Single 16-pin package
- ☐ Minimal external component count

DESCRIPTION

The MK5356 is a monolithic device containing a companding CODEC and PCM filters on a single chip. This device has been designed to meet the needs of the telecommunications industry for per-channel, voice-frequency CODECs and PCM filters. Both the transmit and receive sections have been incorporated into a single package with negligible loss of crosstalk immunity. Typical device applications are PBX systems, central offices, channel banks, and other telephone digital switching and transmission systems.

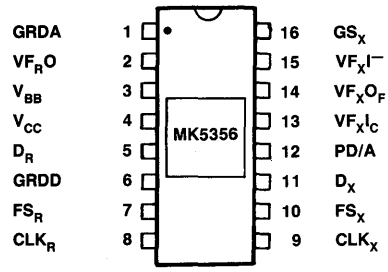
The MK5356 transmit section is composed of an input amplifier, a band-pass filter, and a compressing A/D converter. The operational amplifier output is available for use in an inverting gain configuration at the transmit stage. By disabling the amplifier, this output can be used as a noninverting high-impedance input to the band-pass filter. The band-pass, switched-capacitor filter provides rejection of the 50-60 Hz power line frequency and the band-limiting required for an 8 kHz sampling system. The A/D converter transforms the band-limited, voice-frequency signals into 8-bit words using A-law companding. The encoded data is transmitted in a serial format under the control of a data clock and a frame synchronization input.

The receive section of the MK5356 is composed of an expanding D/A converter and a low pass filter. The D/A converter receives 8-bit words in a serial format under control of a data clock and a frame synchronization input. The low-pass, switched-capacitor filter smooths the voltage steps of the D/A converter and provides compensation for the sinx/x decoder response. The receive filter output may then be adjusted to system levels by use of a voltage divider network.

Pin connections for the MK5356 are shown in Figure 1.

PIN CONNECTIONS

Figure 1



XVI

ADVANCE INFORMATION

COMPANDING CODEC WITH FILTERS MK5326(J)

FEATURES

- ☐ Per-channel, single-chip CODEC with filters and receive power amplifiers
- ☐ CCITT compatible
- ☐ Pin-programmable A-law/power-down
- ☐ On-chip voltage references
- ☐ ±5 volt power supplies, ±5%
- ☐ Low power dissipation
  - 40 mW typical without power amplifiers
  - .5 μW typical in power down mode
- ☐ TTL/CMOS-compatible digital inputs and outputs
- ☐ Gain adjust available at the transmit and receive filter stages
- ☐ Synchronous or asynchronous operation
- ☐ Serial data rate from 64 kb/s to 4.096 Mb/s
- ☐ Separate internal analog and digital grounds reduce system noise problems
- ☐ Single 20-pin 300-mil package
- ☐ Minimal external component count

DESCRIPTION

The MK5326 is a monolithic silicon-gate CMOS device containing a companding CODEC, PCM filters, and receive power amplifiers on a single chip. This device has been designed to meet the needs of the telecommunications industry for per-channel, voice-frequency CODECs and PCM filters. Both the transmit and receive sections have been incorporated into a single package with negligible loss of crosstalk immunity. Typical device applications are PBX systems, central offices, channel banks, and other telephone digital switching and transmission systems.

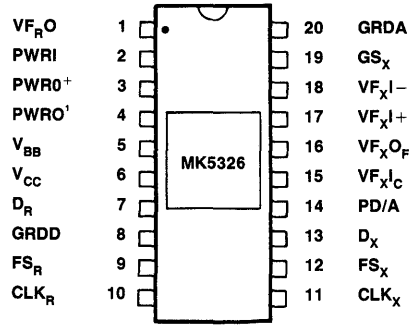
The MK5326 transmit section is composed of an input amplifier, a band-pass filter, and a compressing A/D converter. The operational amplifier output is available for use in a gain configuration at the transmit stage. By disabling the amplifier, this output can be used as a noninverting high-impedance input to the band-pass filter. The band-pass, switched-capacitor filter provides rejection of the 50-60 Hz power line frequency and the band-limiting required for an 8 kHz sampling system. The A/D converter transforms the band-limited, voice-frequency signals into 8-bit words using A-law companding. The encoded data is transmitted in a serial format under the control of a data clock and a frame synchronization input.

The receive section of the MK5326 is composed of an expanding D/A converter, a low pass filter, and a differential power amplifier pair. The D/A converter receives 8-bit words in a serial format under control of a data clock and a frame synchronization input. The low-pass, switched-capacitor filter smooths the voltage steps of the D/A converter and provides compensation for the sinx/x decoder response. The receive filter output may then be adjusted to system levels by use of a voltage divider network. The differential power amplifier pair is available for use in applications requiring low-impedance drive capability.

Pin connections for the MK5326 are shown in Figure 1.

PIN CONNECTIONS

Figure 1



XVI

INTEGRATED PCM CODEC TECHNOLOGY UPDATE

INTRODUCTION

A general trend towards the conversion of voice signals to digital information is currently occurring. TDM PCM is the most popular form of digital transmission.

Today there are several important applications for this TDM scheme:

1. A high speed digital data link between central offices to pass many conversations over one pair of wires.
2. The electronic connection of two different circuit paths.
3. Concentrators

Traditionally this connection had been done by electromechanical crossreed switches. Very low "on" resistance, low crosstalk, and immunity from the large ringing or transient voltages were required. Since the electromechanical technique was deemed to be of lower reliability, an all electronic approach was desired. Electronic cross point switches were designed and built, but because the electrical requirements mentioned above are extremely difficult to meet, the results were not entirely satisfying.

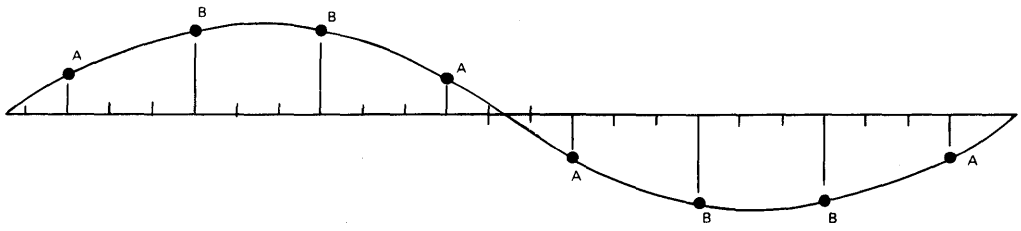
The digital approach obviates the analog switch problem by first performing an A to D conversion, then assigning a time slot for each voice channel. For the D3 channel bank, 24 channels of digital data of 8 bits per word are transmitted in a serial bit stream at 1.544 Mbits/sec. Each voice channel is sampled at an 8kHz rate so this signal must be bandlimited to less than 4kHz in order to prevent undesirable aliasing.

Figure 1 shows how a 1kHz input signal is sampled every 125 μsec. At each of these sampling times, the analog information is converted into an eight-bit digital word that is later sent out in serial format at the 1.544 Mbits/sec rate.

Figure 2 shows how the 24 voice channels are time division multiplexed onto one wire (for simplicity only simplex operation is shown).

Channel 1 analog information is first bandlimited to less than 4kHz, then sampled and converted to a companded digital code. This 8 bit word is serially transmitted to a multiplexer where digital information from all the other channels are assimalated. The final bit stream of 1.544mbit/sec is sent to the demultiplexer where the appropriate alphanumeric channel is connected to numeric channel. This control (selection) is done by the main computer or processor. One may see that any numeric channel could be connected to any alphanumeric channel by means of a different time slot assignment. This completes the switching in a completely digital manner.

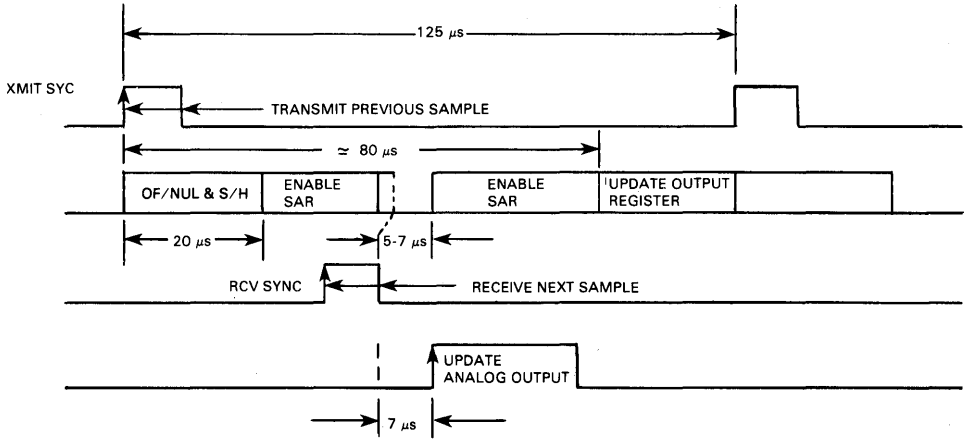
8kHz SAMPLING SYSTEM
Figure 1



XVI

A/D AND D/A CONVERSION TIMING

Figure 4



process is completed, the output of the SAR is loaded into the output buffer. The data is transmitted serially at the output clock rate during the period the XMIT SYNC is high. During the signalling frame, signalling information (SigA/SigB) is inserted into the output bit stream in place of the 8th data bit as selected by the A/B select (SMIT) input.

CIRCUIT DESCRIPTION

The system timing is controlled by the sequence controller which operates at master clock rate of 1.5 - 2.1 MHz. All necessary signals, e.g. and S&H, SAR clock Encode/Decode control, etc; are generated in this section. To insure proper encode operation, decode interrupt is allowed only when the internal SAR clock is low thus resulting in a variable (5-7 μs) decode interrupt interval.

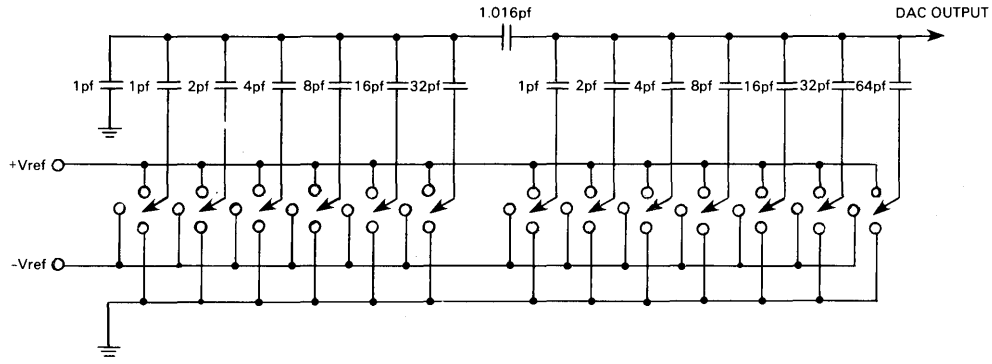
The 8 to 13 bit converter gives a one-to-one translation between 8 bit companded code at its input to a 13 bit linear code at its output thus allowing the use of a linear DAC in the digital-to-analog conversion process.

The 13-bit linear DAC operates on the charge distribution principal of a binary weighted capacitor ladder.

As shown in Figure 5, the capacitor ladder has two sections of 7 bits (7 most significant bits) and 6 bits (6 least significant bits) connected by a 64:1 capacitor divider. The equivalent circuit of the two sections can be drawn as shown in Figure 6.

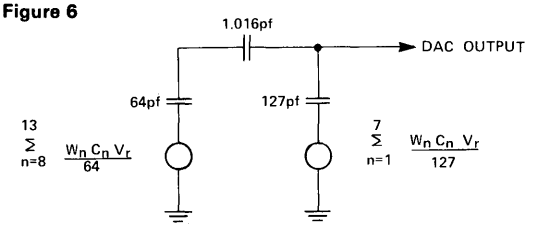
CAPACITOR LADDER

Figure 5



CAPACITOR LADDER EQUIVALENT CIRCUIT

Figure 6



WHERE W_n = 0 or 1 for the n th bit.
C_n = n th bit capacitor.
V_r = Reference Voltage ($+V_{ref}$ or $-V_{ref}$)

The output of the DAC can be written as:

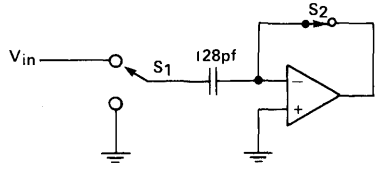
$$V_{DAC} = \frac{V_r}{128}\left[\sum_{n=1}^{7} W_n C_n + \sum_{n=8}^{13} W_n (C_n/64)\right]$$

which is equivalent to the output of a 13 bit DAC with an equivalent output capacitance of 128pF.

In the encode section this equivalent capacitor of 128pF is also employed to perform the additional function of offset-null and sample-hold as shown in Figure 7.

OFFSET NULL/SAMPLE HOLD

Figure 7



Initially S_1 is connected to V_{in} and S_2 is closed. The op. amp. is operating as a unity gain follower and its offset voltage (V_{off}), along with the analog input voltage, is stored on the capacitor.

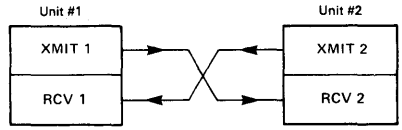
Then switch S_2 is opened and S_1 is switched to analog ground. The voltage at the inverting input of the op-amp is now V_{off}-V_{in}. Thus when the amplifier operates with S_2 open it acts as a comparator with effectively zero offset and $-V_{in}$ applied on its inverting input. The other end of the capacitor can now be operated as a DAC. Thus the capacitor ladder performs all the necessary functions of offset-null sample-hold as well as a DAC in the encode section of the chip.

EXPERIMENTAL RESULTS

The set up of Figure 8 was used to evaluate the chip performance.

CHIP PERFORMANCE

Figure 8

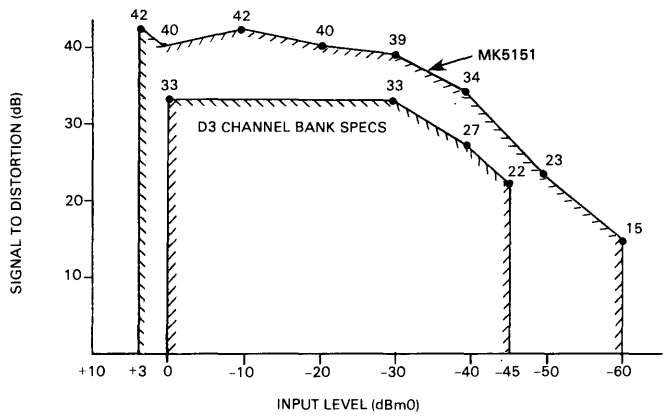


The MK5151 CODEC performance exceeds the AT&T D3 channel bank specifications. Figure 9 shows the signal-to-quantizing distortion as a function of input level.

Idle channel noise of 13-14dBrnC0 is better than the D3 spec by 9-10dB. Gain tracking is shown in Figure 10.

SIGNAL-TO-NOISE RATIO

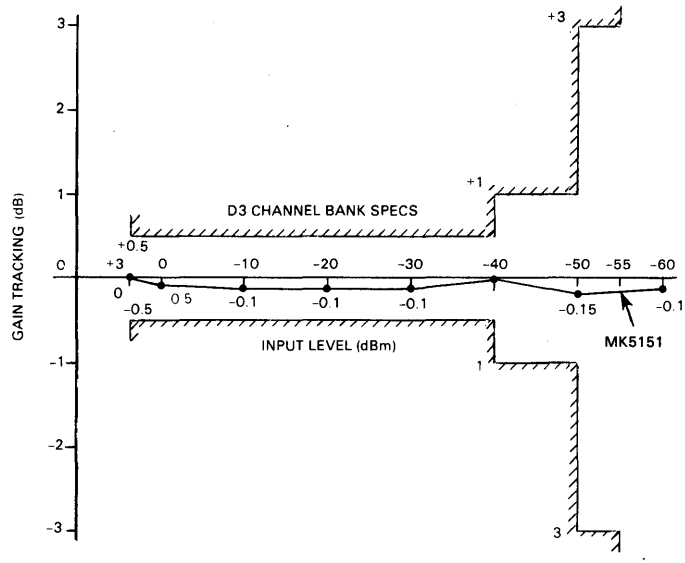
Figure 9



XVI

GAIN TRACKING

Figure 10



Operating power measured at room temperature typically is 30mW. This is low enough that a stand-by mode is not deemed necessary. The European A-law version of the CODEC is also available and is simply a metal mask variation of this product. Chip size is 170 x 184 mils.

1984/1985 MICROELECTRONIC DATA BOOK

PRELIMINARY

LOCAL AREA NETWORK CONTROLLER FOR ETHERNET MK68590

FEATURES

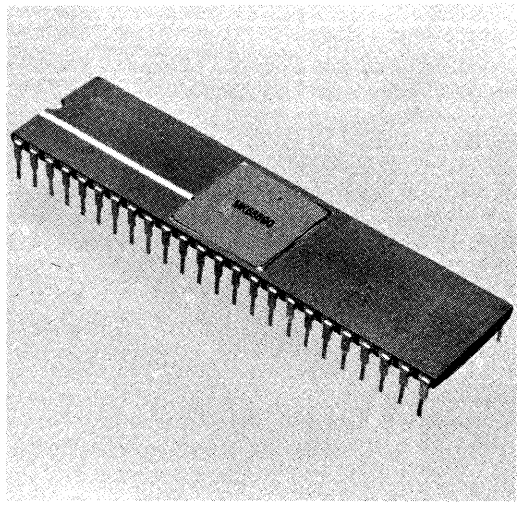
- ☐ 100% compatible Ethernet serial port
- ☐ Data packets moved by block transfers over a processor bus (on-board DMA controller 24-bit linear address space)
- ☐ Buffer management
- ☐ Packet framing
- ☐ Preamble and CRC insertion
- ☐ Preamble stripping and CRC checking
- ☐ General 16-bit microprocessor bus interface compatible with popular processors (68000, 8086, Z800[illegible] LSI-11)
- ☐ Cable fault detection
- ☐ Multicast logical address filtration
- ☐ Collision handling and retry
- ☐ Scaled N-channel MOS VLSI technology
- ☐ 48-pin DIP
- ☐ Single 5-volt power supply
- ☐ Single phase TTL level clock
- ☐ All inputs and outputs TTL compatible
- ☐ Completely compatible with companion Serial Interface Adapter (SIA) chip. (MK68591)

DESCRIPTION

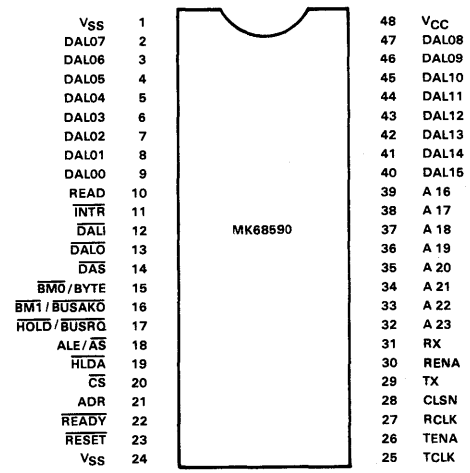
The MK68590-LANCE™ (Local Area Network Controller for Ethernet) is a 48-pin VLSI device designed to simplify greatly the interfacing of a microcomputer or a minicomputer to an Ethernet Local Area Network. This chip operates in a local environment that includes a closely coupled memory and microprocessor. The LANCE uses scaled N-channel MOS technology and is compatible with several microprocessors.

LANCE is a trademark of Mostek Corporation.

MK68590
Figure 1



LANCE PIN ASSIGNMENT
Figure 2



PIN DESCRIPTION

DAL00-DAL15
(Data/Address Bus)
Input/Output Tri-State. The time multiplexed Address/Data bus. These lines will be driven as a Bus Master and as a Bus Slave.

READ
Input/Output Tri-State. Indicates the type of operation to be performed in the current bus cycle. When it is a Bus Master, LANCE drives this signal.

LANCE as Bus Slave:
High - The chip places data on the DAL lines.
Low - The chip takes data off the DAL lines.
LANCE as Bus Master:
High - The chip takes data off the DAL lines.
Low - The chip places data on the DAL lines.

INTR
(Interrupt)
Output Open Drain. When enabled, an attention signal that indicates the occurrence of one or more of the following events: a message reception or transmission has completed or an error has occurred during the transaction; the initialization procedure has completed; or a memory error has been encountered. Programming register (CSR0) enables INTR.

DALI
(Data/Address Line In)
Output Tri-State. An external bus transceiver control line. When LANCE is a Bus Master and reads from the DAL lines, DALI is asserted.

DALO
(Data/Address Line Out)
Output Tri-State. An external bus transceiver control line. When LANCE is a Bus Master and drives the DAL lines, DALO is asserted.

DAS
(Data/Strobe)
Input/Output Tri-State. Defines the data portion of the bus transaction. DAS is driven only as a Bus Master.

BM0, BM1 or BYTE, BUSAKO
(Byte Mask)
Output Tri-State. Pins 15 and 16 are programmable through bit (00) of CSR3 (known as BCON). Asserting RESET clears CSR3.

If BCON = 0
PIN 16 = BM 1 (Output Tri-State)
PIN 15 = BM 0 (Output Tri-State)

BM0, BM1 Byte Mask. Indicates the byte(s) of a bus transaction to read or written. The BM lines are ignored as a Bus Slave and assume word transfers only. The LANCE drives the BM lines only when it is a Bus Master. Byte selection occurs as follows:

BM1	BM0	
LOW	LOW	Whole Word
LOW	HIGH	Byte of DAL 08 - DAL 15
HIGH	LOW	Byte of DAL 04 - DAL 07
HIGH	HIGH	None

If BCON = 1
PIN 16 = BUSAKO (Output)
PIN 15 = BYTE (Output Tri-State)

Byte. An alternate byte selection line. Byte selection occurs when the BYTE and DAL (00) lines are latched during the address portion of the bus transaction. BYTE, BM0 and BM1 are ignored as Bus Slaves. There are two modes of ordering bytes depending on bit (02) of CSR3, (known as BSWP). This programmable ordering of upper and lower bytes when using BYTE and DAL (00) as selection signals is required to make the ordering compatible with various 16-bit microprocessors.

BSWP = 0		BSWP = 1		
BYTE	DAL(00)	BYTE	DAL(00)	
LOW	LOW	LOW	LOW	WHOLE WORD
LOW	HIGH	LOW	HIGH	ILLEGAL CONDITION
HIGH	HIGH	HIGH	LOW	UPPER BYTE
HIGH	LOW	HIGH	HIGH	LOWER BYTE

BUSAKO. The DMA daisy chain output.

HOLD/BUSRQ
(Bus Hold Request)
Input/Output Open Drain. LANCE asserts this signal when it requires access to memory. HOLD is held LOW for the entire bus transaction. This bit is programmable through bit (00) of CSR3 (known as BCON). In the daisy chain DMA mode (BCON = 1) BUSRQ is asserted only if BUSRQ is inactive prior to assertion. Bit (00) of CSR3 is cleared when RESET is asserted.

CSR3(00) BCON = 0
PIN 17 = HOLD (Output Open Drain)
CSR3(00) BCON = 1
PIN 17 = BUSRQ (Output Open Drain)
BUSRQ will be asserted only if PIN 17 is high prior to assertion.

ALE/AS
(Address Latch Enable)
Output Tri-State. Used to demultiplex the DAL lines and define the address portion of the bus cycle. This I/O pin is programmable through bit (01) of CSR3. As ALE, the signal transitions from a HIGH to a LOW at the end of

the address portion of the bus transaction and remains LOW during the entire data portion of the transaction. As $\overline{AS}$, the signal transitions from a LOW to a HIGH at the end of the address portion of the bus transaction and remains HIGH throughout the entire data portion of the transaction. The LANCE drives the ALE/$\overline{AS}$ line only as a Bus Master.

CSR3(01) ACON = 0
PIN 31 = ALE
CSR3(01) ACON = 1
PIN 31 = AS

$\overline{HLDA}$
(Bus Hold Acknowledge)
Input. A response to $\overline{HOLD}$ indicating that the LANCE is the Bus Master. $\overline{HLDA}$ stops its response when $\overline{HOLD}$ ends its assertion.

$\overline{CS}$
(Chip Select)
Input. When asserted, $\overline{CS}$ indicates LANCE is the slave device of the data transfer. $\overline{CS}$ must be valid throughout the data portion of the bus cycle.

ADR
(Register Address Port Select)
Input. When $\overline{CS}$ is asserted, ADR indicates which of the two register ports is selected. ADR must be valid throughout the data portion of the bus cycle.

ADR	PORT
LOW	Register Data Port
HIGH	Register Address Port

$\overline{READY}$
Input/Output Open Drain. When the LANCE is a bus master, $\overline{READY}$ is an asynchronous acknowledgement from external memory that will complete the data transfer. As a bus slave, the chip asserts $\overline{READY}$ when it has put data on the bus, or is about to take data off the bus. $\overline{READY}$ is a response to $\overline{DAS}$. $\overline{READY}$ negates after $\overline{DAS}$ negates. Note: If $\overline{DAS}$ or $\overline{CS}$ deassert prior to the assertion of $\overline{READY}$, $\overline{READY}$ cannot assert.

$\overline{RESET}$
Input. Bus reset signal. Causes LANCE to cease operation, and enter an idle state.

TLCK
(Transmit Clock)
Input. Normally a free-running 10 MHz clock. (Crystal-controlled within .01% accuracy.)

TENA
(Transmit Enable)
Output. Transmit Output Stream Enable. A level asserted with the transmit output bit stream, TX, to enable the external transmit logic.

RCLK
(Receive Clock)
Input. Normally a 10MHz square wave synchronized to the Receive data and only present while receiving an input bit stream.

CLSN
(Collision)
Input. A logical input that indicates that a collision is occurring on the channel.

TX
(Transmit)
Output. Transmit Output Bit Stream.

RENA
(Receive Enable)
Input. A logical input that indicates the presence of data on the channel.

RX
(Receive)
Input. Receive Input Bit Stream.

A16-A23
(High-Order Address Bus)
Output Tri-State. The additional address bits necessary to extend the DAL lines to produce a 24-bit address. These lines will be driven as a Bus Master only.

VCC
Power supply pin. +5 VDC ±5%

VSS
Ground. 0 VDC

FUNCTIONAL CAPABILITIES

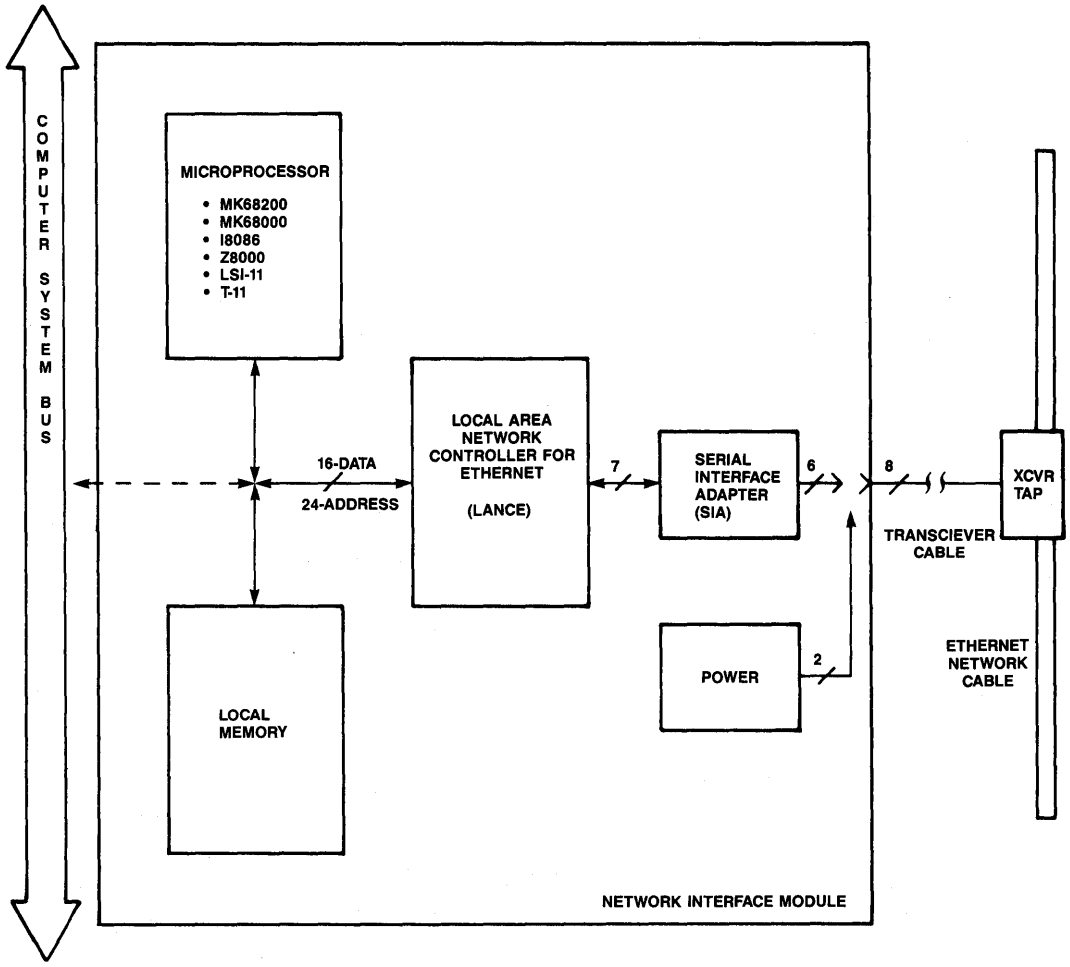
The Local Area Network Controller for Ethernet (LANCE) interfaces to a microprocessor bus characterized by time multiplexed address and data lines. Typically, data transfers are 16 bits wide but byte transfers occur if the buffer memory address boundaries are odd. The address bus is 24 bits wide.

The Ethernet packet format consists of 64-bit preamble, a 48-bit destination address, a 48-bit source address, a 16-bit type field, and from a 46 to 1500 byte data field terminated with a 32-bit CRC. The packets' variable widths accommodate both short status, command and terminal traffic packets, and long data packets to printers and disks (1024 byte disk sectors, for example). Packets are spaced a minimum of 9.6 μsec apart to allow one node enough time to receive back-to-back packets.

The LANCE operates in a minimal configuration that requires close coupling between local memory and a processor. The local memory provides packet buffering for the chip and serves as a communication link between

the chip and the processor. During initialization, the control processor loads the starting address of the initialization block plus the operating mode of the chip via two control registers into LANCE. The host processor talks directly to LANCE only during this initial phase. All further communications are handled via a DMA machine under microword control contained within LANCE. Figure 3 shows a block diagram of the LANCE and SIA device used to create an Ethernet interface for a computer system.

ETHERNET LOCAL AREA NETWORK SYSTEM BLOCK DIAGRAM
Figure 3



FUNCTIONAL DESCRIPTION

SERIAL DATA HANDLING

LANCE provides the Ethernet interface as follows. In the transmit mode (since there is only one transmission path, Ethernet is a half duplex system), the LANCE reads data from a transmit buffer by using Direct Memory Access (DMA) and appends the preamble, sync pattern (two ones after alternating ones and zeros in the preamble), and calculates and appends the complement of the 32-bit CRC. In the receive mode, the destination address, source address, type, data, and CRC fields are transferred to memory via DMA cycles. The CRC is calculated as data and transmitted CRC is received. At the end of the packet, if this calculated CRC does not agree with a constant, an error bit is set and an interrupt is generated to the microprocessor. In the receive mode, LANCE accepts packets under four modes of operation. The first mode is a full comparison of the 48-bit destination address in the packet with the node address that was programmed into the LANCE during an initialization cycle. There are two types of logical addresses. One is a group type mask where the 48-bit address in the packet is put through a hash filter in order to map the 48-bit physical addresses into 1 of 64 logical groups. This mode can be useful if sending packets to all of one type of a device simultaneously on the network. (i.e., send a packet to all file servers or all printer servers). The second logical address is a multicast address where all nodes on the network receive the packet. The last receive mode of operation is the so called "promiscuous mode" in which a node will accept all packets on the coax regardless of their destination address.

COLLISION DETECTION AND IMPLEMENTATION

The Ethernet CSMA/CD network access algorithm is implemented completely within the LANCE. In addition to listening for a clear network cable before transmitting, Ethernet handles collisions in a predetermined way. Should two transmitters attempt to seize the network cable at the same time, they will collide, and the data on the network cable will be garbled. LANCE is constantly monitoring the CLSN (Collision) pin. This signal is generated by the transceiver when the signal level on the network cable indicates the presence of signals from two or more transmitters. If LANCE is transmitting when CLSN is asserted, it will continue to transmit the preamble, (normally collisions will occur while the preamble is being transmitted) then will "jam" the network for 32 bit times (3.2 microseconds). This jamming ensures that all nodes have enough time to detect the collision. The transmitting nodes then delay a random amount of time according to the "truncated binary backoff" algorithm defined in the Ethernet specification to minimize the probability of the colliding nodes having multiple collisions with each other. After 16 abortive attempts to transmit a packet, LANCE will report a RTRY error due to excessive collisions and step over the transmitter buffer. During reception, the detection of a collision causes that reception to be aborted. Depending on when the collision occurred, LANCE will treat this packet as an error packet if the packet has an address mismatch, as a runt packet (a packet that has less than 64 bytes), or as a legal length packet with a CRC error.

Extensive error reporting is provided by the LANCE through a microprocessor interrupt and error bits in a status register. The following are the significant error conditions: CRC error on received data; transmitter on longer than 1518 bytes; missed packet error (meaning a packet on the network cable was missed because there were no empty buffers in memory), and memory error, in which the memory did not respond (handshake) to a memory cycle request.

BUFFER MANAGEMENT

A key feature of the LANCE and its DMA channel is the flexibility and speed of communication between the LANCE and the host microprocessor through common memory locations. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings, as shown in Figure 4. Separate descriptor rings describe either transmit or receive operations. Up to 128 tasks may be queued on a descriptor ring for execution by the LANCE. Each entry in a descriptor ring holds a pointer to a data memory buffer and an entry for the data buffer length. Data buffers can be chained or cascaded to handle a long packet in multiple data buffer areas. The LANCE searches the descriptor rings to determine the next empty buffer. This enables it to chain buffers together or to handle back-to-back packets. As each buffer is filled, an "own" bit is reset, signaling the host processor to empty this buffer.

MICROPROCESSOR INTERFACE

The parallel interface of the LANCE has been designed to be "friendly" or easy to interface to many popular 16-bit microprocessors. These microprocessors include the following: MK68000, Z8000, 8086, LSI-11, T-11, and MK68200. (The MK68200 is a 16-bit single chip microcomputer being sampled by Mostek with an architecture modeled after the MK68000). The LANCE has a wide 24-bit linear address space when it is in the Bus Master Mode, allowing it to DMA directly into the entire address space of the above microprocessors. The LANCE uses no segmentation or paging methods and as such the addressing is closest to MK68000 addressing. However, it is compatible with the others. When the LANCE is a Bus Master, a programmable mode of operation allows byte addressing either by employing a Byte/Word control signal, much like that used on the 8086 or the Z8000, or by using an Upper Data Strobe/Lower Data Strobe much like that used on the MK68000, LSI-11 and MK68200 microprocessors. A programmable polarity on

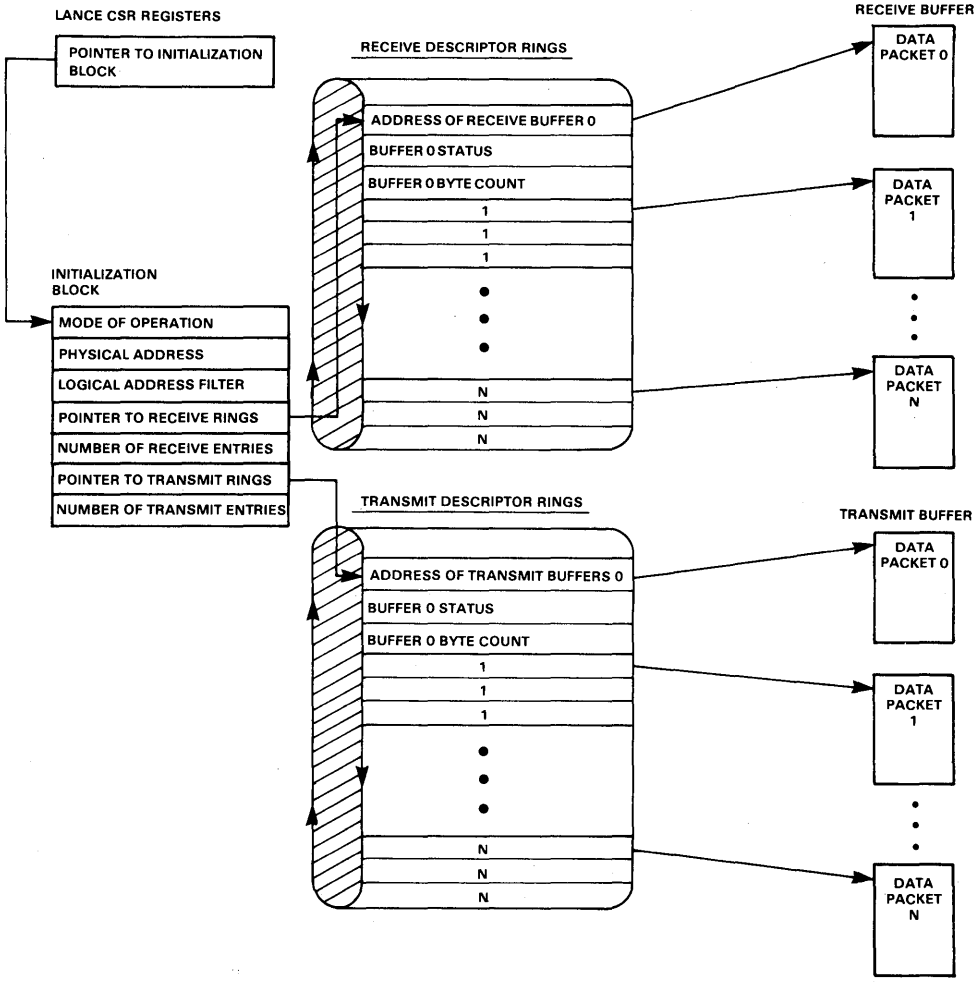
the Address Strobe signal eliminates the need for external logic. LANCE interfaces with multiplexed and demultiplexed data busses and features control signals for address/data bus transceivers.

After the initialization routine, packet reception and transmission, transmitter timeout error, a missed packet, and memory error, LANCE generates interrupts to the microprocessor.

The cause of the interrupt is ascertained by reading CSR0. Bit (06) of CSR0, INEA, enables or disables interrupts to the microprocessor. In a polling mode, BIT (07) of CSR0 is sampled to determine when an interrupt causing condition occurred.

LANCE MEMORY MANAGEMENT

Figure 4



LANCE INTERFACE DESCRIPTION

ALE, $\overline{DAS}$ and $\overline{READY}$ time all data transfers from the LANCE in the Bus Master mode. The automatic adjustment of the LANCE cycle by the $\overline{READY}$ signal allows synchronization with variable cycle time memory due either to memory refresh or to dual port access. Bus cycles are a minimum of 600 ns long and can be increased in 100 ns increments.

READ SEQUENCE

At the beginning of a read cycle, valid addresses are placed on DAL00-DAL15 and A16-A21. The BYTE Mask signals ($\overline{BM0}$ and $\overline{BM1}$) become valid at the beginning of this cycle as does READ, indicating the type of cycle. The trailing edge of ALE or $\overline{AS}$ strobes the addresses A0-A15 into the external latches. Approximately 100 ns later, DAL00-DAL15 go into a tri-state mode. There is a 50 ns delay to allow for transceiver turnaround, then $\overline{DAS}$ falls low to signal the beginning of the data portion of the cycle. At this point in the cycle, the LANCE stalls waiting for the memory device to assert $\overline{READY}$. Upon assertion of $\overline{READY}$, $\overline{DAS}$ makes a transition from a zero to a one, latching memory data. ($\overline{DAS}$ is low for a minimum of 200 ns).

The bus transceiver controls, $\overline{DALI}$ and $\overline{DALO}$, control the bus transceivers. $\overline{DALI}$ signals to strobe data toward the LANCE and $\overline{DALO}$ signals to strobe data or addresses away from the LANCE. During a read cycle, $\overline{DALO}$ goes inactive before $\overline{DALI}$ goes active to avoid "spiking" of bus transceivers.

WRITE SEQUENCE

The write cycle begins exactly like a read cycle with the READ line remaining inactive. After ALE or $\overline{AS}$ pulse, the DAL00-DAL15 change from addresses to data. $\overline{DAS}$ goes active when the DAL00-DAL15 are stable. This data remains valid on the bus until the memory device asserts $\overline{READY}$. At this point, $\overline{DAS}$ goes inactive, latching data into the memory device. Data is held for 75 ns after the negation of $\overline{DAS}$.

LANCE INTERFACE DESCRIPTION — BUS SLAVE MODE

The LANCE enters the Bus Slave Mode whenever $\overline{CS}$ becomes active. This mode must be entered whenever writing or reading the four status control registers (CSR0, CSR1, CSR2, and CSR3) and the register address pointer (RAP). RAP and CSR0 may be read or written to at any time, but the LANCE must be stopped for CSR1, CSR2, and CSR3 to be written to.

MK68590 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . −25°C to +100°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin with Respect to Ground . . . . . −7 V to +7 V
Power Dissipation . . . . . 2.0 W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0°C to 70°C, V_{CC} = +5 V ± 5% unless otherwise specified.

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}		−0.5	+0.8	V
V_{IH}		+2.0	V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2 mA		+0.5	V
V_{OH}	@ I_{OH} = −0.4 mA	+2.4		V
I_{IL}	@ V_{in} = 0.4 to V_{CC}		±10	μA

CAPACITANCE

F=1 MHz

SYMBOL	PARAMETER	MIN	MAX	UNITS
C_{IN}			10	pf
C_{OUT}			10	pf
C_{IO}			20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
1	TCLK	T_{TCT}	TCLK period		99		101
2	TCLK	T_{TCL}	TCLK low time		45		55
3	TCLK	T_{TCH}	TCLK high time		45		55
4	TCLK	T_{TCR}	Rise time of TCLK		0		8
5	TCLK	T_{TCF}	Fall time of TCLK		0		8
6	TENA	T_{TEP}	TENA propagation delay after the rising edge of TCLK	CL = 50 pf			95
7	TENA	T_{TEH}	TENA hold time after the rising edge of TCLK	CL = 50 pf	5		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
8	TX	T_{TDP}	TX data propagation delay after the rising edge of TCLK	CL=50 pf			95
9	TX	T_{TDH}	TX data hold time after the rising edge of TCLK	CL=50 pf	5		
10	RCLK	T_{RCT}	RCLK period		85		118
11	RCLK	T_{RCH}	RCLK high time		38		
12	RCLK	T_{RCL}	RCLK low time		38		
13	RCLK	T_{RCR}	Rise time of RCLK		0		8
14	RCLK	T_{RCF}	Fall time of RCLK		0		8
15	RX	T_{RDR}	RX data rise time		0		8
16	RX	T_{RDF}	RX data fall time		0		8
17	RX	T_{RDH}	RX data hold time (RCLK to RX data change)		5		
18	RX	T_{RDS}	RX data setup time (RX data stable to the rising edge of RCLK)		60		
19	RENA	T_{DPL}	RENA low time		120		
20	CLSN	T_{CPH}	CLSN high time		80		
21	A/DAL	T_{DOFF}	Bus master driver disable after rising edge of $\overline{HOLD}$		0		50
22	A/DAL	T_{DON}	Bus master driver enable after falling edge of $\overline{HLDA}$		0		150
23	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus master)		0		
24	$\overline{RESET}$	T_{RW}	RESET pulse width low		200		
25	A/DAL	T_{CYCLE}	Read/write, address/data cycle time		600		
26	A	T_{XAS}	Address setup time to the falling edge of ALE		75		
27	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		35		
28	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
29	DAL	T_{AH}	Address hold time after the falling edge of ALE		35		
30	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master read)		50		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

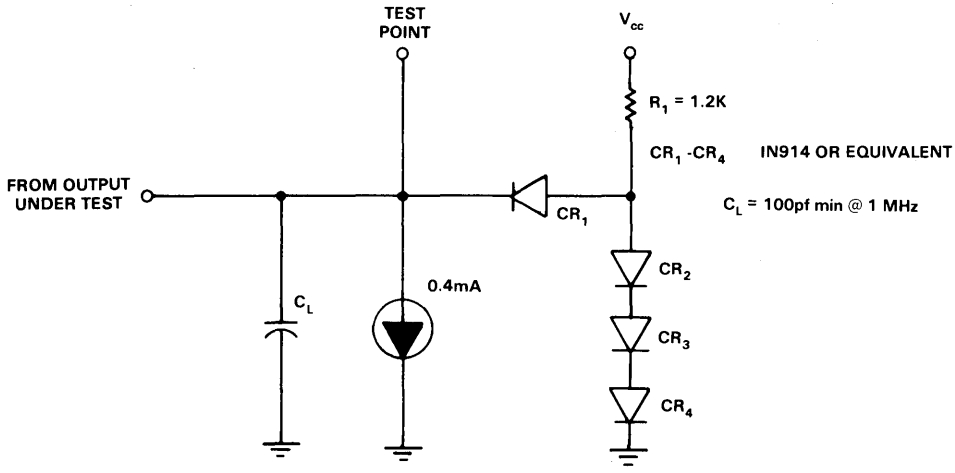
#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
31	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
32	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus master write)		0		
33	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus master write)		200		
34	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		35		
35	DAL	T_{SDO1}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 0,3, RAP)		400	
36	DAL	T_{SDO2}	Data driver delay after the falling edge of $\overline{DAS}$ (Bus slave read)	(CSR 1,2)		1200	
37	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)		0		35
38	DAL	T_{SWDH}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
39	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
40	ALE	T_{ALEW}	ALE width high		130		
41	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
42	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
43	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		
44	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (BUS master read)		35		
45	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	Taryd= 300 ns	100		250
46	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		35		
47	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus master read)		135		
48	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
49	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		55		
50	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus master read)		110		
51	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
52	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus master write)		35		

AC TIMING SPECIFICATIONS (CONTINUED)
T_A = 0°C to 70°C, V_{CC} = +5 V± 5% unless otherwise specified.

#	SIGNAL	SYMBOL	PARAMETER	TEST CONDITIONS	MIN ns	TYP ns	MAX ns
53	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
54	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
55	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
56	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
57	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600 ns)				80
58	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
59	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus master)		0		
60	$\overline{READY}$	T_{SRO1}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 0, 3, RAP)		600	
61	$\overline{READY}$	T_{SRO2}	$\overline{READY}$ driver turn on after the falling edge of $\overline{DAS}$ (Bus slave)	(CSR 1,2)		1400	
62	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		35
63	READ	T_{SRH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
64	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		

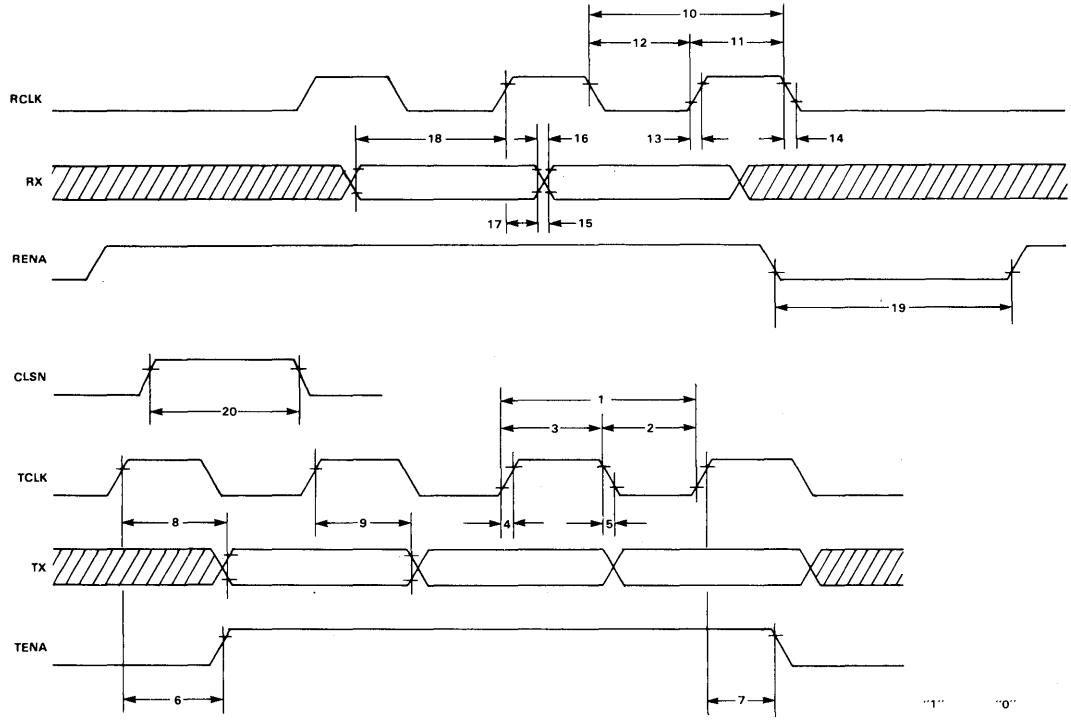
OUTPUT LOAD DIAGRAM

Figure 5



SERIAL LINK TIMING DIAGRAM - SIA INTERFACE SIGNALS

Figure 6

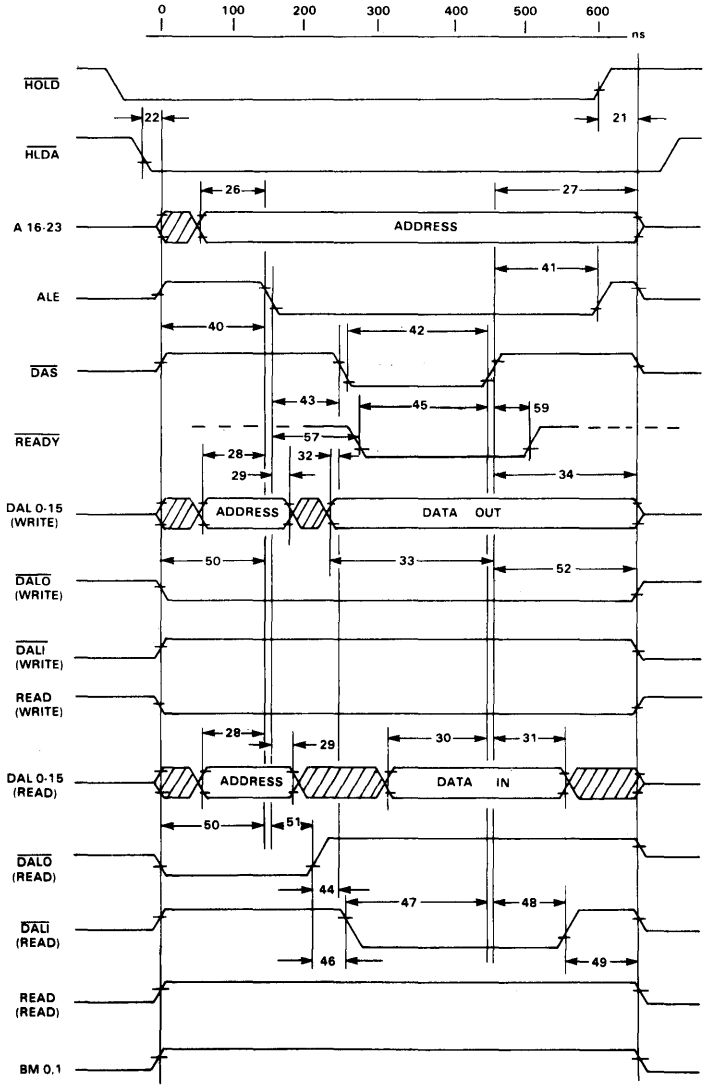


Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8V
FLOAT	V	0.5 V

LANCE BUS MASTER TIMING DIAGRAM

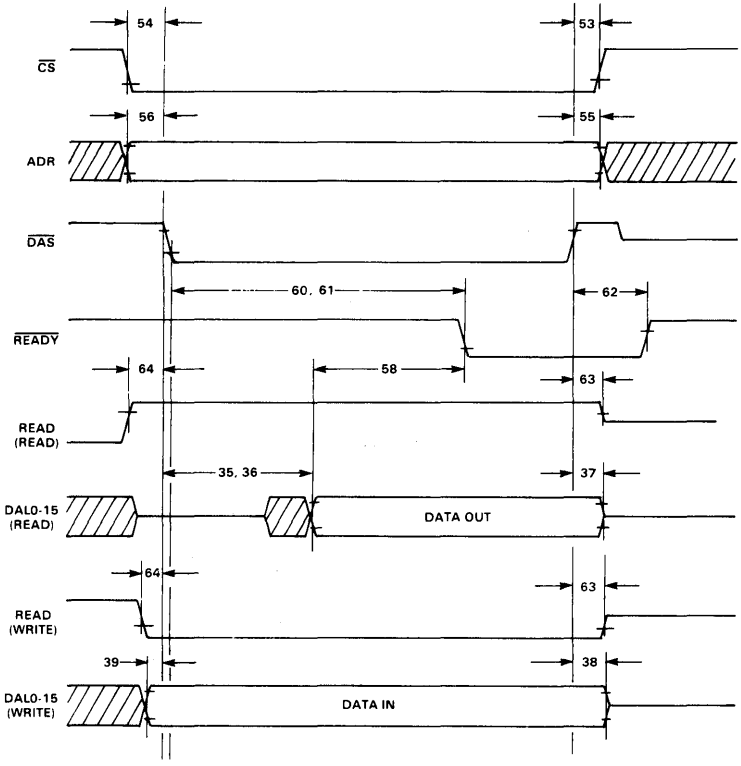
Figure 7



NOTE: The Bus Master cycle time will increase from a minimum of 600 ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

LANCE BUS SLAVE TIMING DIAGRAM

Figure 8



ADVANCE INFORMATION

SERIAL INTERFACE ADAPTER (SIA) MK68591

FEATURES

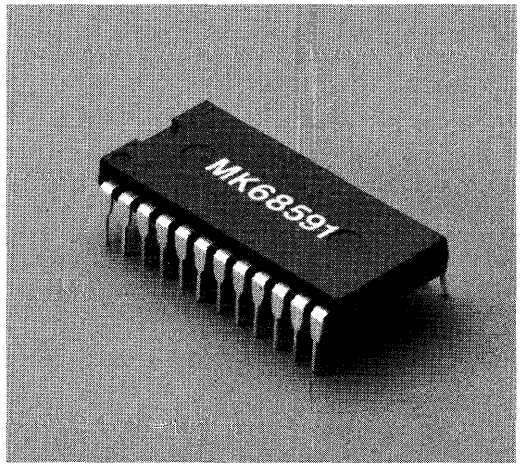
- ☐ Compatible with Ethernet
- ☐ Crystal controlled Manchester Encoder
- ☐ Manchester Decoder acquires clock and data within six-bit times with an accuracy of ±3ns.
- ☐ Guaranteed carrier detection and collision detection threshold limits
  - — Carrier/collision detected for greater than −300mV
  - — No carrier/collision for less than −175mV
- ☐ Input signal conditioning rejects transient noise
  - — Transients <10ns for collision detector inputs
  - — Transients <16ns for carrier detector inputs
- ☐ Receiver decodes Manchester data with up to ±20ns clock jitter (at 10MHz)
- ☐ TTL compatible host interface
- ☐ Transmit accuracy ±0.01% (without adjustments)

GENERAL DESCRIPTION

The MK68591 Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with Ethernet specifications. In an Ethernet application, the MK68591 interfaces the MK68590 Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable, acquires clock and data within 6 bit-times and decodes Manchester data up to ± 20ns phase jitter at 10MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize any false start conditions.

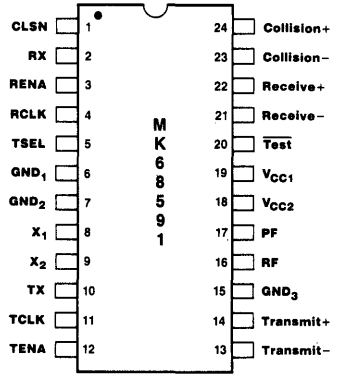
SIA ADAPTOR

Figure 1



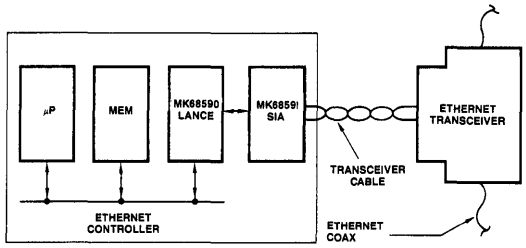
PIN ASSIGNMENT

Figure 2



TYPICAL ETHERNET NODE

Figure 3



Mostek Corporation, 1215 West Crosby Rd.
Carrollton, Texas 75006 USA; (214) 466-6000
In Europe, Contact: Mostek Brussels
270-272 Avenue de Tervuren (BTE21)
B-1150 Brussels, Belgium; Telephone: 762.18.80

PRINTED IN USA July 1984
Publication No. 4420479