## LSI <br> Databook <br> Seventh Edition



## LSI DATABOOK <br> SEVENTH EDITION

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## Introduction

This book has been prepared to give the user a concise list of all LSI Products offered by Monolithic Memories. It is divided by products into sections on Military Products Division, PROMs, PLE ${ }^{\text {Tm }}$ devices, PAL $^{\circledR}$ devices, HAL ${ }^{\circledR} /$ ZHAL devices, System Building Blocks/HMSI ${ }^{\text {Tm }}$, FIFOs, Memory Support, Arithmetic Elements and Logic, Multipliers, 8-Bit Interface, Double-Density PLUS Interface, (CMOS products included), Logic Cell Array, ECL10KH products and a General Information Section which has definition of Terms and Waveforms. Each section has been designed to allow the user the most useable format for the products described. Cross reference and selection guides are given where applicable. FIFO, PAL devices, System Building Blocks $/ \mathrm{HMSI}^{\text {m }}$, Multipliers, 8 -Bit Interface, DoubleDensity PLUS Interface and ECL10KH data sheets are shown in detail for each product. Advance information Sheets are included to inform you of soon-to-be released products. This LSI databook was formatted with you, the user, in mind.

For more information, contact the local Monolithic Memories sales representative or franchised distributor. In section 19 of this book Monolithic Memories Sales Reps and Franchised Distributors are listed, for your convenience.

Products listed in the Advance Information section were due for imminent release at the time of printing. Please contact Monolithic Memories for current availability and full parametric specifications.

## Prices

All prices are in U.S. dollars and are subject to change without notice.

## Terms

70\%/30 days, 30\%/45 days from date of invoice, FOB Sunnyvale, California.

## Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of $\$ 1000$ ( $\$ 100$ per line item) except for the following:
HAL* Circuits-A Non-Recurring Engineering (NRE) charge is made to cover mask and test vector generation. This charge may be amortized over the initial production commitment. Minimum production commitments and NRE charges are as follows:

|  | MIN. | MIN. QTY <br> NER DELY |
| :--- | :--- | :--- | :--- |
| 20 and 24 pin HAL |  |  |
| devices: |  |  |

ProPAL" Circuits - ProPAL circuits are programmed PAL devices which are functionally tested by Monolithic Memories prior to shipment. The NRE charge covers setup and test vector generation costs and may be amortized over the initial production commitment quantities. A nominal per unit programming and testing charge is also made and varies according to device type. NREs and minimum order requirements for ProPAL circuits are as follows:

|  | NRE | MIN. | MIN. QTY <br> ANNUAL QTY |
| :--- | ---: | ---: | ---: |
| PER DELY |  |  |  |

## General

Unless otherwise specified, the standard packages are " J " or " $N$ " packages. In some instances the " $D$ " package is the only package available. Other non-standard packages and military Level 883B devices not listed may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

## In-House PROM Programming Guidelines

1) Minimum Order Size.
$1 / 4 \mathrm{~K}-8 \mathrm{~K} \quad 5 \mathrm{~K} \mathrm{pcs} / \mathrm{yr} /$ pattern
$500 \mathrm{pcs} /$ shipment
16K-32K $2.5 \mathrm{~K} \mathrm{pcs} / \mathrm{yr} /$ pattern 250 pcs/shipment
2) Lead Time: Initial code acceptance six weeks. Standard lead time plus two weeks after code acceptance.
3) Cancellations: 60 Days
4) Schedule Change: 30 Days
5) Price Adder:

A nominal per unit programming and testing charge is made and varies according to device type. Price includes ink marking with customer pattern number.
6) Inputs: Truth Table, Paper Tape, Disk, Master; a combination of two inputs are required. If only one input is supplied, a sample lot must be signed off by the customer.

## Commercial/Industrial/Military Codes

The letter codes "C," "I," and " $M$ " are used to denote commercial, industrial, and military device limits as follows:

$$
\begin{aligned}
\text { Commercial }-T_{A} & =0^{\circ} \mathrm{C} \text { to }+75^{\circ} \mathrm{C} \\
V_{C C} & =5 \mathrm{~V} \pm 5 \% \\
\text { Industrial }-T_{A} & =-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C} \\
V_{C C} & =5 \mathrm{~V} \pm 10 \% \\
\text { Military }-T_{A} & =-55^{\circ} \mathrm{C} \text { to }+125^{\circ} \mathrm{C} \\
V_{C C} & =5 \mathrm{~V} \pm 10 \%
\end{aligned}
$$

## Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

## PACKAGE CODE

J Ceramic dual-in-line
JS Ceramic dual-in-line SKINNYDIP©
$N \quad$ Plastic dual-in-line
NS Plastic dual-in-line SKINNYDIP*
NL Molded leaded chip carrier
D $\quad$ Side brazed ceramic dual-in-line
F Flat Pack-Bottom Brazed
L Leadless-Ceramic chip carrier
$T \quad$ Inverted " $D$ " package
P Pin Grid Array
W Cerpack
See "Part Numbering Systems" for complete part descriptions.
DIP Package Width Configuration

|  | 300 mil | 600 mil | 900 mil |
| :---: | :---: | :---: | :---: |
| $16,18,20$ pin | $\mathrm{N}, \mathrm{J}$ |  |  |
| 24 pin | $\mathrm{NS}, \mathrm{JS}$ | $\mathrm{N}, \mathrm{J}$ |  |
| $28,40,48,52 \mathrm{pin}$ |  | $\mathrm{N}, \mathrm{J}$ |  |
| 64 pin |  |  | $D$ |

## Screening Options

| PROCESS LEVEL | PART <br> MARKING |
| :--- | :---: |
| MIL-STD-883 |  |
| Method 5004 and 5005 | $883 B$ |
| Level B | (Suffix) |

## PAL® <br> Programmable Array Logic Circuits

PAL 16 L 8 B - 4 C N STD H01234

```
FAMILY TYPE
    PAL = Programmable Array Logic
    PAL10H = ECL 10KH Programmable Array Logic
    HAL = Hard Array Logic
    ZHAL = Zero-power Hard Array Logic
```

NUMBER OF ARRAY INPUTS
OUTPUT CELL
L = Active Low
$\mathrm{H}=$ Active High
C = Complementary
$\mathbf{P}=$ Programmable Polarity
RP = Registered Programmable Polarity
$\mathbf{S}=$ Shared
RS $=$ Registered Shared
$\mathbf{X}=$ Exclusive-OR
$A=A r l t h m e t i c$
VX = Varied Exclusive-OR
RA $=$ Registered Asynchronous
G = Latched
NUMBER OF OUTPUTS
SPEED
Blank = Standard
A = High Speed
B = Very High Speed
$=$ Very High Speed
$=$ Ultra High Speed
POWER
Blank $=$ Standard
$-2=1 / 2$ Power
$-4=1 / 4$ Power
OPERATING CONDITIONS
C = Commercial
C
I
= Industrial
I $=$ Industria
$\mathbf{M}=$ Military
PACKAGE
N = Piastic DIP
J = Ceramic DIP
NS = Plastic SKINNYDIP
JS = Ceramic SKINNYDIP
NL = Plastic Leaded Chip Carrier
$P=P i n$ Grid Array
L = Leadless Chip Carrier
W = Cerpack
F = Flat Pack
PROCESSING
STD = Standard
$\mathbf{X X X X}=0$ Other
BIT PATTERN NUMBER

PLE ${ }^{\text {TM }}$
Programmable Logic Element


## High Performance PROMs



FIFOs


## Memory Support/Arithmetic/ HSMI/ <br> Double-Density PLUST™ Interface



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## Monolithic Memories

## Terms and Conditions of Sale

## General Provisions

1. ACCEPTANCE THE TERMS OF SALE CONTAINED HEREIN APPLY TO ALL QUOTATIONS MADE AND PURCHASE ORDERS ENTERED INTO BY THE SELLER. SOME OF THE TERMS SET OUT HERE MAY DIFFER FROM THOSE IN BUYER'S PURCHASE ORDER AND SOME MAY BE NEW. THIS ACCEPTANCE IS CONDITIONAL ON BUYER'S ASSENT TO THE TERMS SET OUT HERE IN LIEU OF THOSE IN BUYER'S PURCHASE ORDER. SELLER'S FAILURE TO OBJECT TO PROVISIONS CONTAINED IN ANY COMMUNICATION FROM BUYER SHALL NOT BE DEEMED A WAIVER OF THE PROVISIONS OF THIS ACCEPTANCE. ANY CHANGES IN THE TERMS CONTAINED HEREIN MUST SPECIFICALLY BE AGREED TO IN WRITING BUY AN OFFICER OF THE SELLER BEFORE BECOMING BINDING ON EITHER THE SELLER OR THE BUYER. All orders or contracts must be approved and accepted by the Seller at its home office. These terms shall be applicable whether or not they are attached to or enclosed with the products to be sold hereunder.
2. TAXES Unless otherwise specifically provided herein, the amount of any present or future sales, revenue, excise or other tax applicable to the products covered by this order or the manufacture of sale thereof, shall be added to the purchase price and shall be paid by the Buyer, or in lieu thereof the Buyer shall provide the Seller with a tax exemption certificate acceptable to the taxing authorities. In the event Seller is required to pay any such tax, fee, or charge, at the time of sale or thereafter, the Buyer shall reimburse Seller therefore.
3. RELEASE Prices apply only if the quantity hereunder is released within twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order; otherwise, Seller's standard prices in effect at the time of release date shall apply to the quantity shipped, and Buyer shall be invoiced for the difference in price, if any.
4. FOB POINT Shipments of goods within and outside the U.S. shall be delivered FOB Seller's plant, and title and liability for loss or damage thereto shall pass to Buyer upon Seller's tender of delivery of the goods to a carrier for shipment to Buyer, and any loss or damage thereafter shall not relieve Buyer of any obligation hereunder. Buyer shall reimburse Seller for taxes and any other expenses incurred or licenses or clearance required at port of entry and destination. Seller may deliver the goods in installments. Unless otherwise agreed, all items shall be packaged and packed in accordance with Seller's normal practices.
5. DELIVERY All shipping dates are estimates only and are dependent upon prompt receipt of all necessary information from Buyer. Shipments may be made in installments. Seller shall be excused from performance and shall not be liable for any delay in delivery or for nondelivery, in whole or in part, caused by the occurrence of any contingency beyond the reasonable control of Seller, including but not limited to, war (whether or not an actual declaration thereof is made), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof affecting the terms of this contract or otherwise, judicial action, labor dispute, accident, defaults of suppliers, fire, explosion, flood, storm or other acts of God, shortage of labor, fuel, raw material or machinery or technical or yield failures where Seller has exercised ordinary care in the prevention thereof. If any such contingency occurs, Seller may at its sole discretion allocate production and delivery among Seller's customers.
6. PAYMENT TERMS (a) Unless otherwise agreed, payment terms are $70 \%$ thirty (30) days; $30 \%$ forty-five (45) days after date of invoice. No discounts are authorized. Shipments, deliveries, and performance of work shall at all times be subject to the approval of the Seller's credit department and the Seller may at any time decline to make any shipments or deliveries or perform any work except upon receipt of payment or upon terms and condition or security satisfactory to such department.
(b) If in the judgment of the Seller, the financial condition of the Buyer at any time does not justify continuation of production or shipment on the terms of payment originally specified, the Seller may require full or partial payment in advance and, in the event of the bankruptcy or insolvency of the Buyer or in the event any proceeding is brought by or against the Buyer under the bankruptcy or insolvency laws, the Seller shall be entitled to cancel any order then outstanding and shall receive reimbursement for its cancellation charges.
(c) Each shipment shall be considered a separate and independent transaction, and payment therefore shall be made accordingly. If shipments are delayed by the Buyer, payments shall become due on the date when the Seller is prepared to make shipment. If the work covered by the purchase order is delayed by the Buyer, payments shall be made based on the purchase price and the percentage of completion. Products held for the Buyer shall be at the risk and expense of the Buyer.
7. INSPECTION Unless otherwise specified and agreed upon, the material to be furnished under this order shall be subject to the Seller's standard inspection at the place of manufacture. If it has been agreed upon and specified in this order that Buyer is to inspect or provide for inspection at place of manufacture such inspection shall be so conducted as to not interfere unreasonably with Seller's operations and consequent approval or rejection shall be made before shipment of the materials. Notwithstanding the foregoing, if, upon receipt of such material by Buyer, the same shall appear not to conform to the contract, the Buyer shall immediately notify the Seller of such conditions and afford the Seller a reasonable opportunity to inspect the material. No material shall be returned without Seller's consent. Seller's Return Material Authorization form must accompany such returned material.
8. LIMITED WARRANTY AND LIMITED REMEDY The Seller warrants that the products to be delivered under this purchase order will be free from defects in material and workmanship under normal use and service. Seller's obligations under this Warranty are limited to replacing or repairing or giving credit for, at its option, at its factory, any of said products which shall, within one (1) year after shipment, be returned to the Seller's factory of origin, transportation charges prepaid, and which are, after examination, disclosed to the Seller's satisfaction to be thus defective. THIS WARRANTY is EXPRESSED IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON THE SELLER'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR THE SELLER ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID ARTICLES. This Warranty shall not apply to any of such products which shall have been repaired or altered, except by the Seller, or which shall have been subjected to misuse, negligence, or accident. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by Seller.

It is understood that if this order calls for the delivery of semiconductor devices which are not furnished and fully encapsulated, that no warranty, statutory, expressed or implied, including the implied warranty of merchantability and fitness for a particular purpose, shall apply. All such devices are sold as-is, where-is.
9. PATENT INDEMNIFICATION Buyer shall hold Seller harmless from and defend Seller against any cost, expenses, damages or liabilities arising from Seller's compliance with Buyer's designs or specifications. Except as set forth above, the Seller agrees to protect and hold harmless the Buyer from any and all claims, demands, proceedings, actions, liabilities and costs resulting from any alleged infringement of patents in the United States owned by third parties by Products purchased by Buyer from Seller, provided the Buyer gives to Seller prompt notice of any such claim made against the Buyer and authorizes the Seller to settle or defend any such claim, demand, proceeding or action and assists the Seller in so doing (at the Seller's expense) upon request by the Seller. Should, as a result of any such claim, demand, proceeding or action, the Buyer be enjoined from selling or using the product, the Seller shall either (1) procure for the Buyer the right to use or sell the product; (2) modify the product so that it becomes noninfringing; (3) upon return of the product provide to the Buyer a noninfringing product meeting the same functional specifications as the product; or (4) authorize the return of the product to the Seller and upon its receipt refund to the Buyer the cost of the product plus transportation charges. The foregoing states the entire liability of the Seller for infringement of the patents of third parties and, in particular, the Seller has no obligation to indemnify the buyer for infringement of patents resulting from combinations of the product with other products whether or not supplied by the Seller. THIS PROVISION IS STATED IN LIEU OF ANY OTHER EXPRESSED, IMPLIED, OR STATUTORY WARRANTY AGAINST INFRINGEMENT AND SHALL BE THE SOLE AND EXCLUSIVE REMEDY FOR PATENT INFRINGEMENT OF ANY KIND.
10. DAMAGE LIMITATION INDEPENDENTLY OF ANY OTHER LIMITATION HEREOF AND REGARDLESS OF WHETHER THE PURPOSE OF SUCH LIMITATION IS SERVED, IT IS AGREED THAT IN NO EVENT SHALL SELLER BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES OF ANY KIND UNDER THIS ORDER.
11. SALE CONVEYS NO LICENSE Seller's products are offered for sale and are sold by Seller subject in every case to the condition that such sale does not convey any license, expressly or by implication, estoppel or otherwise, under any patent claim with respect to which Seller can grant licenses covering a completed equipment, or any assembly, circuit, combination, method or process in which any such products are used as components (notwithstanding the fact that such products may have been designed for use in or may only be useful in, such patented

## Monolithic Memories

## Terms and Conditions of Sale

## General Provisions

equipment, assembly, circuit, combination, method or process and that such products may have been purchased and sold for such use). Seller expressly reserves all its rights under such patent claims.
12. RETURNS AND ADJUSTMENTS Products may only be returned with prior written approval of Seller. Adjustments for defective products are subject to Seller's concurrence that the alleged defects exist, to Selier's satisfaction, after suitable inspection and test by Seller. Adjustments may include credit or replacement at the option of the Seller.
13. TERMINATION AND CANCELLATION (a) Buyer may terminate this contract in whole or, from time to time, in part upon written notice to Selier. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of goods actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for prorated expenses and anticipated profits.
(b) Unless otherwise specified on the face hereof, all quantities must be released no more than twelve (12) months and shipments scheduled no more than eighteen (18) months from the date of Seller's receipt of Buyer's order, otherwise this contract may be cancelled by Seller and Buyer shall be liable for termination charges as provided herein.
14. NONWAIVER OF DEFAULT In the event of any default by Buyer, Seller may decline to make further shipments. If Seller elects to continue to make shipments, Seller's action shall not constitute remedies for any such default.
15. APPLICABLE LAW The validity, performance and construction of this contract shall be governed by the laws of the State of California.
16. U.S. GOVERNMENT CONTRACTS if Buyer's original purchase order indicates by contract number, that it is placed under a government contract, only the following provisions of the current Federal Acquisition Regulations are applicable in accordance with the terms thereof, with an appropriate substitution of parties, as the case may be-i.e., "Contracting Officer" shall mean "Buyer," "Contractor" shall mean "Seller," and the "Contract" shall mean this order.
52.202-1. Definitions: 52:232-11, Extras; 52.212-9, Variation in Quantity; 52.23223, Assignment of Claims; 52.228-2, Additional Bond Security; 52.225-11, Certain Communist Areas; 52.222-4, Contract Work Hours and Safety Standards Act -Overtime Compensation; 52.222-20, Walsh-Healy Public Contracts Act; 52.2225, Equal Opportunity; Officials Not to Benefit; 52.203-5, Covenant Against Contin-
gent Fees; 52.249-1, Termination for Convenience of the Government (Fixed Price) (Short Form) (only to the extent that Buyer's contract is terminated for the convenience of the government); 52.2-1, Contractor Inspection Requirements; 52.227-1, Authorization and Consent; 52.227-2, Notice and Assistance Regarding Patent and Copyright Information; 52.247-1, Commercial Bills of Lading Notations; 52.223-35, Affirmative Action for Special Disabled and Vietnam Era Veterans; 52.222-1, Notice to the Government of Labor Disputes; 52.215-1, Examination of Records by Comptroller General; 52.220-3, Utilization of Labor Surplus Area Concerns.
17. ASSIGNMENT This contract shall be binding upon and inure to the benefit of the parties and the successors and assigns of the entire business and good will of either Seller or Buyer, or of that part of the business of either used in the performance of this contract, but shall not be otherwise assignable.
18. MODIFICATION This contract constitutes the entire agreement between the parties relating to the sale of goods described on the face hereof, and no addition to or modification of any provision upon the face or reverse of this contract shall be binding upon Seller unless made in writing and signed by a duly authorized representative of Seller located in Santa Clara, California. Buyer hereby acknowledges that he has not entered into this agreement in reliance upon any warranty or representation by any person or entity except for the warranties or representations specifically set forth herein.
19. GENERAL The Seller represents that with respect to the production of the articles and/or the performance of the services covered by this order, it will fully comply with all requirements of the Fair Labor Standards Act of 1938, as amended.
20. PROPERTY RIGHTS AND TOOLING The design, development or manufacture by Seller of a product for a specific customer shall not be deemed to produce a work made for hire and shall not give to the customer any copyright interest in the product or any interest in all or any portion of the mask works relating to the product. All such rights shall remain the property of Seller. Notwithstanding the foregoing, Seller will provide a custom product (e.g., personalized gate array, cell library or full custom) utilizing a logic design supplied by a customer exclusively to that customer absent written agreement to the contrary with the customer.
21. VARIATION IN QUANTITY If this order calls for a product not listed in Seller's current catalog, or for a product which is specially programmed for Buyer, it is agreed that Seller may ship a quantity which is five percent ( $5 \%$ ) more or less than the ordered quantity and that such quantity shipped will be accepted and paid for in full satisfaction of each party's obligation hereunder for the quantity ordered.

## Quality System

The quality system at Monolithic Memories is based on MIL-Q-9858, "Quality Program Requirements," MIL-I-45208, "Inspection System Requirements," and MIL-M-38510, Appendix A, "Product Assurance Program." Mil-M-38510 plays a significant role in structuring Monolithic Memories' Quality Program as specified herein.
Monolithic Memories has facilities certified by DESC, Defense Electronics Supply Center, to qualify and manufacture Class B Schottky Bipolar PROMS and Programmable Array Logic devices, in accordance with the requirements of MIL-M-38510. This certification included a successful audit of our quality system to the stringent requirements of Appendix A of MIL-M-38510 which defines a Product Assurance Program tailored for integrated circuit manufacturers by DESC. This same quality system has also met the strict requirements of both "controlled" and "captive" line programs connected with our special Hi-Rel programs.
The quality accent at Monolithic Memories is on process control as reflected in the use of many monitors and audits rather than gate inspection. This philosophy is consistent with building in quality and reliability rather than attempting to screen for it.

## Process Control

Monolithic Memories manufacturing process uses advanced techniques to reduce random defects and produce consistent optimum quality. Typical techniques employed are:

- Redundant Masking
- Pellicalized Masks
- Direct Step on Wafer Processing

These processes although more costly, result in significant quality and reliability improvements. During the initial production stages of new designs and periodically thereafter, engineering characterizes the design process compatibility by careful sample selection of lots reflecting process variable extremes.

## Product Reliability Programs

Monolithic Memories has an ongoing reliability program for military and commercial products, each utilizing the appropriate test methods of MIL-STD-883. This program provides for a consistent database in the following areas:

- Product/Process Reliability Data
- Qualification of Raw Materials
- Customer Quality Conformance
- Reliability verification of state of the art design and production techniques.


## Quality Monitors

MMI constantly monitors product quality and reliability through the following ongoing programs:

- Reliability assessments of all products, processes and packages.
- Inprocess and Final product quality measurements.
- Process and product quality feedback at all key manufacturing points.
- Positive corrective action and verification.


## Screening

Much of the assembly and processing is performed offshore at facilities owned by or qualified by MMI. These facilities are routinely monitored by Monolithic Memories personnel to our quality system requirements.
Standard Commercial product receives the following screens and monitors to insure the highest possible quality.

- Precap Inspection

MIL-Standard 883 Level B

- Temperature Cycle
- Constant Acceleration
- Fine and Gross Leak

Ongoing daily monitor to confirm the AQL levels are met or exceeded.

- Final Electrical Test
- Visual and Mechanical Inspection
The standard product AQL levels which Monolithic Memories guarantees are listed in the table on this page.


## Quality Assurance (AQL) Levels

| TEST | AQL <br> TEMPERANCE |
| :--- | :---: |
| Hermeticity (includes fine and gross) | .1 |
| Electrical |  |
| DC at $25^{\circ} \mathrm{C}$ | .065 |
| Functional at $25^{\circ} \mathrm{C}$ | .065 |
| AC at $25^{\circ} \mathrm{C}$ | .25 |
| DC at Temperature Extremes | .25 |
| Functional at Temperature Extremes | .25 |
| AC at Temperature Extremes | .25 |



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| FIFO | $\varepsilon$ |
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## Introduction

In August, 1982 Monolithic Memories Inc. formed a Military Products Division. Although Monolithic Memories has participated in the defense market for some time, we feel that by focusing on this very demanding customer base with a totally dedicated resource, we can provide aerospace and military systems manufacturers with a new industry standard of service and responsiveness.

Monolithic Memories offers devices to a full complement of military screening levels:

Monolithic Memories Inc. Level S
JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc Mil-Temp Product
In addition, we welcome the opportunity to review and quote to customer source control drawings. Our spec Review group is measured to a 2 week turn-around time on drawing reviews, so our customers will receive a timely response on our ability to meet custom requirements.

Monolithic Memories is Certified by the Defense Electronics Supply Center to assemble and test JAN 38510 Class B devices at its Sunnyvale, California.
Offshore Assembly facilities for Mil-Std-883 Class B devices are located in Penang, Malaysia.

## Standard Processing Flows

Monolithic Memories Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.
Standard processing flows which the Military Products Division currently operates to include:

Monolithic Memories Inc. Modified Level S JAN 38510 Class B
DESC Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc. Mil-Temp Product
In addition, these flows are expanded to provide for factory programming on PAL circuits and PROMS, when required by our customers.
Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost - no price adders for custom processing.
- Improved lead time - no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

It is the policy of Monolithic Memories to always operate to the most current revision of Mil-Std-883.


## Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"
Mil-Q-9858, "Quality Program Requirements"
Mil-I-45208, "Inspection System Requirements"
Monolithic Memories facilities in Sunnyvale are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Schottky Bipolar PROMs and PAL circuits in accordance with Mil-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of Mil-M-38510. Monolithic Memories has also demonstrated compliance with the strict requirements of both controlled and captive lines connected with special Military programs.

## Quality Assurance

Following 100\% screening, the Military Products Division samples all products processed in conformance with MIL-STD-883 Class B to the following LTPD levels:

| Test | LTPD |
| :--- | ---: |
| DC $25^{\circ} \mathrm{C}$ | 2 |
| DC $+125^{\circ} \mathrm{C}$ | 3 |
| DC $-55^{\circ} \mathrm{C}$ | 5 |
| Functional at $25^{\circ} \mathrm{C}$ | 2 |
| Functional at Temperature Extremes | 5 |
| AC $25^{\circ} \mathrm{C}$ | 2 |
| $\mathrm{AC}+125^{\circ} \mathrm{C}$ | 3 |
| $\mathrm{AC}-55^{\circ} \mathrm{C}$ | 5 |

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of Mil-Std-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to $A C$ tests, testing is performed utilizing MIL-M-38510 Slash Sheet sample plans.

Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that Monolithic Memories' Reliability Department, as a minimum, conduct full qualification testing per Method 5005 of Mil-Std883. Once qualified, each package type (from each assembly line) and device (by technology group as delineated in Mil-M38510 ) are incorporated into Monolithic Memories Quality Conformance Inspection program which utilizes the requirements of Mil-M-38510.
When Military Programs do not require that QCI data be run on the specific lot shipped, Monolithic Memories Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and desctruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following generic data is available:

## Group B-Package related tests

- QCI is performed every 6 weeks of manufacture on each package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly integrity.

Group C-Product/Process related tests

- QCI is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and parametric performance for each product technology.


## Product Qualification/ Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with Mil-Std-883, Method 5005.

## Prices

All prices are in U.S. dollars and are subject to change without notice.

## Minimum Order Requirements

For all orders placed in the factory there is a minimum order requirement of $\$ 1000$ ( $\$ 250$ per line item) except for the following:
HAL ${ }^{*}$ Circuits -The $\$ 3-4$ K N.R.E. and mask charge can be amortized over the initial production commitment. The minimum initial production commitment is 5 K units within one year; the minimum quantity per line item release is 2 K .
ProPAL Circuits-When purchased, the initial phase of HAL Circuit, there is no additional N.R.E. and there is a nominal adder for programming and testing. The minimum quantity per release is 500 units. When purchased without a follow-on the $\$ 1-2 K$ N.R.E. can be amortized over a minimum initial production commitment of $\$ 2500$ units.
There will be a minimum of $\$ 250$ and $\$ 50$ per line item for drop-ship orders.

## Terms

$70 \% / 30$ days, $30 \% / 45$ days from date of invoice, FOB Sunnyvale, California.

## Commercial Code

The letter code " $C$ " is used to denote commercial device limits as follows:
Commercial $-\mathrm{TA}=0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$

$$
V C C=5 V \pm 5 \%
$$

## General

Unless otherwise specified the standard packages are " J " or " $N$ " packages. In some instances the " $D$ " package is the only package available. Other non-standard packages may be available. Contact a sales representative of Monolithic Memories. Non-standard devices are considered nonreturnable by distribution to Monolithic Memories.

## Package Codes

All devices ordered must include a package code as a suffix to the part number. The package code definitions are shown below.

| PACKAGE CODE | DESCRIPTION |
| :---: | :---: |
| $J$ | Ceramic dual-in-line* |
| JS | Ceramic dual-in-line* |
| N | Plastic dual-in-line* |
| NS | Plastic dual-in-line* |
| NL | Molded Leadless Chip Carrier |

## JAN Program

Monolithic Memories is certified by the Defense Electronics Supply Center to fabricate wafers in our 4-inch fab lines and to assemble and test MIL-M-38510 Class B PROMs and PAL circuits in our Sunnyvale facilities. Monolithic Memories has, in addition, been awarded full laboratory suitability to conduct all qualification and conformance testing in accordance with MIL-STD-883, Method 5005.
Selected devices will be further qualified in leadless chip carriers.

Long term QPL I plans include FIFO's Double-Density PLUS Interface, New PAL Families as they are introduced, and Registered/Standard PROMs.
Our goal in the Military Products Division is to support the JAN38510 Program with a continual flow of new highperformance, Advanced Technology Products.
Monolithic Memories Products for which slash sheet specifications currently exist are listed in the "M38510 Slash Sheet Cross Reference to Generic Part Number."

Listings are based on QPL-38510-65, dated October 1985 M38510 (Part I Qualified Devices) Slash Sheet Cross Reference to Generic Part Number

| M38510 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 10 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  |  |
| 206 |  | $53 S 441$ |  |  |  |  |  |  |  |  |
| 209 |  |  |  |  |  |  |  | $53 S 841$ |  |  |
| 503 | $10 H 8$ | $12 H 6$ | 14 H 4 |  |  | 10 L 8 | 12 L 6 | 14 L 4 |  |  |
| 504 | 16 L8A | 16R8A | 16R6A | 16R4A |  |  |  |  |  |  |

Near future QPL I plans include:
PAL16L8A-2
PAL16R8A-2
PAL16R6A-2
PAL16R4A-2
PAL20L8A
PAL20R8A
PAL20R6A
PAL20R4A

## DESC Drawing Program

Monolithic Memories is an active participant in the DESC Drawing Program. For contracts invoking MIL-STD-454 we offer our full PAL product line to DESC Drawings 81035 and 81036. Monolithic Memories is also approved to supply the 32K PROM to DESC Drawing 82008. The idea behind the DESC Drawing Program is to standardize MIL-STD-883B microcircuits where fully qualified JAN product is not available. The advantage to the user is that DESC Drawings are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.
Since semiconductor demand is on the rise, and lead times will be a major concern, DESC Drawings should always be considered to improve availability over source control draw-
ings. It is standard practice at Monolithic Memories to convert our 883B processing to DESC Drawings for all products which we are approved to supply. Monolithic Memories Inc. then dual marks devices with both the DESC Drawing Number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and distributor channels.

The following cross reference will allow you to determine the appropriate DESC Drawing part numbers for each PAL product and the 32K PROM. Future DESC print activity will include new PAL products and registered PROMs. Monolithic Memories will work with DESC to continually generate new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

## DESC Drawing/Generic Part Type Cross Reference

| DESC DRAWING PART NO.: 81035 | 01 | R | X* |
| :---: | :---: | :---: | :---: |
| DRAWING | DEVICE TYPE | CASE OUTLINE | LEAD FINISH |

PAL DEVICES

| DESC DRAWING | GENERIC PART NUMBER | REPLACEMENT JAN SPECIFICATION PART NUMBER |
| :---: | :---: | :---: |
| 8103501RA* | PAL10H8MJ883B | M38510/50301BRX |
| 81035012C | PAL10H8ML883B | M38510/50301B2X |
| 8103501 YC | PAL10H8MF883B | M38510/50301BYX |
| 8103502RA | PAL12H6MJ883B | M38510/50302BRX |
| 81035022C | PAL12H6ML883B | M38510/50302B2X |
| 8103502YC | PAL12H6MF883B | M38510/50302BYX |
| 8103503RA | PAL14H4MJ883B | M38510/50303BRX |
| 81035032C | PAL14H4ML883B | M38510/50303B2X |
| 8103503YC | PAL14H4MF883B | M38510/50303BYX |
| 8103504RA | PAL16H2MJ883B | M38510/50304BRX |
| 81035042C | PAL16H2ML883B | M38510/50304B2X |
| 8103504YC | PAL16H2MF883B | M38510/50304BYX |
| 8103505RA | PAL16C1MJ883B | M38510/50305BRX |
| 81035052C | PAL16C1ML883B | M38510/50305B2C |
| 8103505YC | PAL16C1MF883B | M38510/50305BYX |
| 8103506RA | PAL10L8MJ883B | M38510/50306BRX |
| 81035062C | PAL10L8ML883B | M38510/50306B2X |
| 8103506YC | PAL10L8MF883B | M38510/50306BYX |
| 8103507RA | PAL12L6MJ883B | M38510/50307BRX |
| 81035072C | PAL12L6ML883B | M38510/50307B2X |
| 8103507YC | PAL12L6MF883B | M38510/50307BYX |
| 8103508RA | PAL14L4MJ883B | M38510/50308BRX |
| 81035082C | PAL14L4ML883B | M38510/50308B2X |
| 8103508YC | PAL14L4MF883B | M38510/50308BYX |
| 8103509RA | PAL16L2MJ883B | M38510/50309BRX |
| 81035092C | PAL16L2ML883B | M38510/50309B2X |
| 8103509YC | PAL16L2MF883B | M38510/50309BYX |
| *Lead Finishes <br> A = Solder Dip <br> C = Gold Plate |  |  |



DESC Drawing/Generic Part Type Cross Reference continued

| DESC DRAWING |  | GENERIC PART NUMBER | REPLACEMENT JAN SPECIFICATION PART NUMBER |
| :---: | :---: | :---: | :---: |
| 8103607RA |  | PAL16L8AMJ883B ${ }^{1}$ | M38510/50401BRX |
| 81036072C |  | PAL16L8AML883B | M38510/50401B2X |
| 8103607SA |  | PAL16L8AMW883B | M38510/50401BYX |
| 8103608RA |  | PAL16R8AMJ883B ${ }^{1}$ | M38510/50402BRX |
| 81036082C |  | PAL16R8AML883B | M38510/50402B2X |
| 8103608SA |  | PAL16R8AMW883B | M38510/50402BYX |
| 8103609RA |  | PAL16R6AMJ883B ${ }^{1}$ | M38510/50403BRX |
| 81036092C |  | PAL16R6AML883B | M38510/50403B2X |
| 8103609SA |  | PAL16R6AMW883B | M38510/50403BYX |
| 8103610RA |  | PAL16R4AMJ883B ${ }^{1}$ | M38510/50404BRX |
| 81036102C |  | PAL16R4AML883B | M38510/50404B2X |
| 8103610SA |  | PAL16R4AMW883B | M38510/50404BYX |
| 8103611RA |  | **PAL16L8A-2MJ883B | M38510/50407BRX |
| 81036112C |  | **PAL16L8A-2ML883B | M38510/50407B2X |
| 8103611SC |  | PAL16L8A-2MF883B | - - - - |
| 8103612RA |  | **PAL16R8A-2MJ883B | M38510/50408BRX |
| 81036122C |  | **PAL16R8A-2ML883B | M38510/50408B2X |
| $8103612 \text { SC }$ | $\underset{\sim}{4}$ | PAL16R8A-2MF883B | $-\quad-\quad-$ |
| 8103613RA |  | **PAL16R6A-2MJ883B | M38510/50409BRX |
| 81036132C |  | **PAL16R6A-2ML883B | M38510/50409B2X |
| 8103613SC |  | PAL16R6A-2MF883B | $-\quad-\quad-$ |
| 8103614RA |  | **PAL16R4A-2MJ883B | M38510/50410BRX |
| 81036142C |  | **PAL16R4A-2ML883B | M38510/50410B2X |
| $8103614 \mathrm{SC}$ |  | PAL16R4A-2MF883B |  |
| 8412901LA |  | PAL20L8AMJS883B | M38510/50501BJX |
| $84129013 \mathrm{C}$ |  | PAL20L8AML883B | M38510/50501B3X |
| $8412901 \mathrm{KA}$ |  | PAL20L8AMW883B |  |
| 8412902LA |  | PAL20R8AMJS883B | M38510/50502BJX |
| $84129023 C$ |  | PAL20R8AML883B | M38510/50502B3X |
| $8412902 \mathrm{KA}$ |  | PAL20R8AMW883B | - - - |
| 8412903LA |  | PAL20R6AMJS883B | M38510/50503BJX |
| 84129033C |  | PAL20R6AML883B | M38510/50503B3X |
| 8412903KA |  | PAL20R6AMW883B | - - - |
| 8412904LA |  | PAL20R4AMJS883B | M38510/50504BJX |
| 84129043C |  | PAL20R4AML883B | M38510/50504B3X |
| 8412904KA |  | PAL20R4AMW883B | - - |
| 8412905LA |  | PAL20L10AMJS883B | - - - |
| 84129053C |  | PAL20L10AML883B | - - - |
| 8412906LA |  | PAL20X8AMJS883B | - - - |
| 84129063C |  | PAL20X8AML883B | - - - |
| 8412907LA |  | PAL20X10AMJS883B | - - - |
| 84129073C |  | PAL20X10AML883B | - |

[^0]

DESC Drawing/Generic Part Type Cross Reference continued

| DESC DRAWING | GENERIC PART NUMBER | REPLACEMENT JAN SPECIFICATION PART NUMBER |
| :---: | :---: | :---: |
| 8412908LA | PAL20X4AMJ883B | - |
| 84129083C | PAL20X4AML883B | - - - |
| 8506501RA | **PAL16L8A-4MJ883B | - - - |
| 85065012C | **PAL16L8A-4ML883B | - - - |
| 8506501SC | **PAL16L8A-4MF883B | - - - |
| 8506502RA | **PAL16R8A-4MJ883B | - - - |
| 85065022C | **PAL16R8A-4ML883B | - - - |
| 8506502SC | **PAL16R8A-4MF883B | - - - |
| 8506503RA | **PAL16R6A-4MJ883B | - - - |
| 85065032C | **PAL16R6A-4ML883B | - - - |
| 8506503SC | **PAL16R6A-4MF883B | - - - |
| 8506504RA | **PAL16R4A-4MJ883B | - - - |
| 85065042C | **PAL16R4A-4ML883B | - - - |
| 8506504SC | **PAL16R4A-4MF883B | - - - |
| 8515501RA ${ }^{1}$ | PAL16L8BPJ883B | - - - |
| 85155012C ${ }^{1}$ | PAL16L8BPL883B | - - - |
| 8515502RA ${ }^{1}$ | PAL16R8BPJ883B | - - - |
| 85155022C ${ }^{1}$ | PAL16R8BPL883B | - - - |
| 8515503RA ${ }^{1}$ | PAL16R6BPJ883B | - - - |
| 85155032C ${ }^{1}$ | PAL16R6BPL883B | - - - |
| 8515504RA ${ }^{1}$ | PAL16R4BPJ883B | - - - |
| 85155042C ${ }^{1}$ | PAL16R4BPL883B | - - - |
| 8515505RA ${ }^{1}$ | PAL16L8BM-2J883B | - - - |
| 85155052C ${ }^{1}$ | PAL16L8BM-2L883B | - - - |
| 8515506RA ${ }^{1}$ | PAL16R8BM-2J883B | - |
| 85155062C ${ }^{1}$ | PAL16R8BM-2L883B | - - - |
| 8515507RA ${ }^{1}$ | PAL16R6BM-2J883B | - |
| 85155072C ${ }^{1}$ | PAL16R6BM-2L883B | - - - |
| 8515508RA ${ }^{1}$ | PAL16R4BM-2J883B | - - - |
| 85155082C ${ }^{1}$ | PAL16R4BM-2L883B | - - - |
| PROM: 82008B1JA | 53S3281MJ883B | M38510/21102BJX |
| 82008B13C | 53S3281ML883B | M38510/21102B3X |
| 82008B2JA | 53S3281AJ883B | - - - |
| 82008B23C | 53S3281AL883B | - - - |

**Converting from " $A$ " to " $B$ " PAL in fourth quarter 1986. ${ }^{1}$ DESC Print 85155 to be released approx. 6/86

## Group D-In-depth package related tests

- QCI is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.


## Generic Data:

Monolithic Memories Generic Data Program is based on MIL-M-38510, which allows for shipments based on 26 weeks of coverage for Group C Testing and 36 weeks of coverage for Group D Testing.
Should circumstances arise where generic coverage to MIL-M-38510 is not possible, Monolithic Memories reserves the right to ship product based on 52 weeks of generic Group C and/or D coverage per MIL-M-883 Revision C.

## Manufacturing and Screening Locations

JAN Products, Monolithic Memories Modified Level " S ," and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified assembly line in Sunnyvale, California.
Mil-Std-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by Monolithic Memories Quality Department, as well as by many of our customers, to manufacture Mil-Std-883 Class B product. Conformance to Mil-Std-883 requirements is routinely monitored through audits at the Penang facility, as well as incoming inspections in Sunnyvale. Manufacturing capabilities for each Monolithic Memories facility are highlighted on the chart below.

## Manufacturing Capabilities

|  | Sunnyvale | Penang |
| :--- | :---: | :---: |
| Assembly | X | X |
| Precap Inspection | X | X |
| Environmental Testing | X | X |
| Electrical Pre-Test | X | X |
| Burn-In | X | X |
| Post Burn-In Electricals | X | X |
| Group A Testing | X | X |
| Mark | X | X |
| Factory Programming (when applicable) | X |  |
| Qualification and Quality | X |  |
| Conformance Testing |  |  |

To identify the assembly location of each military device, the Country of origin is marked on all products prior to shipment. Products assembled in our stateside facility in Sunnyvale, California, will have "USA" marked on the topside of the device. The exception to this is JAN 38510 product, which is marked to the Mil-M-38510 requirements only.
Offshore built product, which is manufactured in Penang, Malaysia, will have "Malaysia" or "Malay" marked on the bottom side of the device.
Marking Example:


ESD Designator

## Process Audits

Process Audits are performed in accordance with Mil-M38510, Appendix A, paragraph 20.1.3.9, self audits by the Quality Assurance Department.

## AC Testing

Although Monolithic Memories offers a large selection of programmable products, it must be pointed out that AC Testing cannot be performed on many of our product types without their being programmed. For those devices which must be programmed prior to AC Tests and are ordered unprogrammed, Monolithic Memories must "guarantee" their AC Performance.
Newer devices in the PROM/PLE and PAL families do allow preprogram $A C$ testability at $25^{\circ} \mathrm{C}$.
Since the guaranteeing of parameters can be a serious concern for the Military user, we have outlined several approaches to address the AC screening issue.

1. Monolithic Memories can pull a Sample from a lot using our own Standard patterns (designed to blow in excess of 50 percent of the fuses) and perform AC testing.
a) PAL/PROM products processed to DESC prints include programmability samples and AC testing at $25^{\circ} \mathrm{C}$.
b) PROM/PLE AC testing can be performed at $25^{\circ} \mathrm{C}$, $-55^{\circ} \mathrm{C}, 125^{\circ} \mathrm{C}$ temperatures.
2. Monolithic Memories can program PROM/PLE's using custom patterns submitted by the customer. AC can then be done with the following options:
a) Sample AC at $25^{\circ} \mathrm{C}$
b) Sample AC at $25^{\circ} \mathrm{C},-55^{\circ} \mathrm{C}, 125^{\circ} \mathrm{C}$
c) $100 \% \mathrm{AC}$ at $25^{\circ} \mathrm{C}$
d) $100 \% \mathrm{AC}$ at $25^{\circ} \mathrm{C},-55^{\circ} \mathrm{C}$ and $125^{\circ} \mathrm{C}$

## Note: For PALs contact the factory

On PAL products where custom programming is performed and $A C$ testing is required, additional vector generation and fault coverage analysis is required, as well as AC program generation and checkout.
To give you an idea of delivery differences for the options discussed above, general lead times are as follows:

- Unprogrammed:

Cerdip, 4-6 weeks
Cerpack/Flat pack, 8-12 weeks
Leadless chip carrier, 6-12 weeks
(consult monthly leadtime guide for individual part types).

- Unprogrammed product using our standard pattern to verify AC at room temperature on sample basis (option 1). Add 2 weeks to standard delivery.
- Programmed product using customer programs with sample AC (option $2 a$ and $b$ ). Contact factory for delivery. Delivery quoted will be after receipt of customer design package.
- $100 \%$ AC testing at $25^{\circ} \mathrm{C}$-Standard Monolithic Memories pattern or customer pattern, (option c). Contact factory.
Remember, for ProPALs, customer must provide design package including Boolean Equations, "Seed" function test sequence, package stipulation and AC test vectors, when required. Delivery quotes for this type of product begin after receipt of this data from the customer.


## VIL/VIH Parametric Information

$\mathrm{V}_{\mathrm{IL}}$ and $\mathrm{V}_{\mathrm{IH}}$ parameters are, in effect, input conditions of D.C. and Functional output tests and are not directly tested. $\mathrm{V}_{\mathrm{IL}}$ is specified at $\leq 0.8 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{IH}}$ is specified at $\geq 2.0 \mathrm{~V}$.

## ElectroStatic Discharge

The Military Products Division of Monolithic Memories has fully implemented static control procedures throughout its facilities in Penang, Malayasia and Sunnyvale, California.
All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.
All product is moved throughout our facilities and shipped to customers in static shielded containers.
In addition, MPD distributors must demonstrate that they meet the same stringent standards governing ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by MPD's Quality Assurance Department.
An ESD identifier is marked on all products in front of the date code, and all shipping containers are labeled with an ESD Caution Message. These procedures have been implemented, and will continually be reviewed, to ensure that our customers receive only the highest quality product from the Military Products Division.

## Package Information Leadless Chip Carrier/Pin Grid Array

Monolithic Memories' Military Products Division offers, with few exceptions, our entire product line in square, ceramic leadless chip carriers.
8-BIT INTERFACE

- 20 square LCC

PROM CIRCUITS (Programmable Read Only Memories)

- 20 square LCC
- 28 square LCC

PLE CIRCUITS (Programmable Logic Elements)

- 20 square LCC
- 28 square LCC

PAL/HAL* CIRCUITS (Programmable Array Logic)

- 20 square LCC
- 28 square LCC
- 44 square LCC

HMSI CIRCUITS (High-Complexity
Medium Scale Integration)

- 28 square LCC

FIFO CIRCUITS (First-In-First-Out Memories)

- 20 square LCC

DOUBLE-DENSITY INTERFACE CIRCUITS

- 20 square LCC
- 28 square LCC

MULTIPLIER CIRCUITS

- 44 square LCC
*HALs are the mask-programmable versions of PAL.


# Military Ordering Information 

## PAL/PROM/PLE Programming Inputs:

A. Two masters (programmed device) and checksum
B. Master and truthtable (or product terms for PAL)
C. Master and magnetic tape (VAX compatible)
D. Master and floppy disk (VAX compatible)
E. PALASM/PLEASM IBM compatible floppies, vAX compatible magnetic tape or floppies
F. Master only (least preferred)

NOTES:

If options A, B, C, D or E are submitted, Monolithic Memories may require customer approval of prototypes before proceeding with programming.

## Military Ordering Information

## Minimum Order Guidelines:

- Standard (unprogrammed/non-programmable) product Mil-Std-883, Class B
DESC Print Devices
JAN Devices
Requires a $\$ 1000.00$ ( $\$ 250$ per line item) per order
- Source Control Drawings (unprogrammed/ non-programmable) product
Requires a $\$ 1000.00$ ( $\$ 250$ per line item) per order
- ProPAL32R16
\$5K per pattern
500 units min per pattern
200 units min per request date per pattern
- HAL20RA10 \& 24RS Family
\$5K per pattern*
2500 units min per pattern
1000 units min per request date per pattern
- HAL20/24
\$3K per combinatorial pattern
\$4K per sequential pattern
2500 units min per pattern
1000 units min per request date per pattern
*Applicable to 20RA10 only. Assumes customers provide a set of test vectors, verifiable to $90 \%$ fault grading for all HAL devices.

If option F is submitted, Monolithic Memories will require customer approval of factory generated prototypes before proceeding.

## Military Ordering Information

## Cancellation Policy:

HAL (Mask Programmable Devices)

- 60 days firm.
- 90 days uncancellable.
- 61-90 days can be rescheduled once up to 60 days out.
- Any line item shortage of less than $5 \%$ can be rescheduled for next delivery date (or cancelled).
ProPAL/ProPROM/ProPLE (Programmed Devices)
- 30 days firm.
- 60 days uncancellable.
- 31-60 days can be rescheduled once up to 60 days out.
- Any line item shortage of less than $5 \%$ can be rescheduled for next delivery date (or cancelled).


## Terms:

70\%/30 Days, 30\%/45 Days from date of invoice, F.O.B. Sunnyvale, California.

## PAL® <br> Programmable Array Logic Circuits



High Performance PROMs


## PLE ${ }^{\text {m }}$

## Programmable Logic Element



## FIFO



Power Strobe


## DESC Drawing Numbering System




## JAN Part Numbering System




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PROM Performance Analysis

## (Maximum Commercial Limits)



## PROM Performance Analysis <br> (Maximum Commercial Limits)



[^1]
# High Performance 32x8 PROM TiW PROM Family 

## Features/Benefits

- 15-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $98 \%$ programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs.


## Applications

- Programmable logic element (PLE $\left.{ }^{\text {ru }}\right) 5$ inputs, 8 outputs, 32 product terms
- Address decoder
- Priority encoder


## Description

The 53/63S080, 53/63S081 and 63S081A feature low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high-state. Special onchip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The 53/63S080, 53/63S081 and 63S081A are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 1/4 K | $32 \times 8$ | TS | $\begin{gathered} 16 \\ (20) \end{gathered}$ | $\begin{gathered} \mathrm{N}, \mathrm{~J}, \mathrm{~W} \\ (\mathrm{NL}),(\mathrm{L}) \end{gathered}$ | Enhanced | 63S081A | - |
|  |  | TS |  |  | Standard | 63 S081 | 53S081 |
|  |  | OC |  |  |  | 635080 | 53S080 |

## Pin Configurations



## Block Diagram



Plastic Chip Carrier

Absolute Maximum Ratings
Supply voltage $V_{C C}$
Operating
-0.5 V to 7 V
Input voltage -1.5 V to 7 V Programming

Input current
-30 mA to +5 mA
Off-state output voltage .................................................................... 0.5 V to 5.5 V
Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYM | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{1 C}$ | Input clamp voltage | $V_{C C}=$ MIN | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| 1 IL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| $\mathrm{I}_{\mathrm{IH}}$ | High-level input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }} \mathrm{MAX}$ |  |  |  | 40 | $\mu \mathrm{A}$ |
|  | Low-level output voltage | $V{ }^{\text {O }}=$ MIN | A | Com |  |  | 0.45 | V |
| $\mathrm{V}_{\text {OL }}$ | Low-level output volage | $V_{C C}=$ Min | OL $=16 \mathrm{ma}$ | Mil |  |  | 0.5 | $\checkmark$ |
|  | High-level output voltage* | V | Com ${ }^{1} \mathrm{OH}=$ |  | 2.4 |  |  | V |
| OH | High-level output voitage | $C C=M 1 N$ | Mil $\mathrm{I}_{\mathrm{OH}}=-2$ |  | 2.4 |  |  | V |
| IOZL | Off-state output current* | $V_{C C O}=$ MAX | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  | $V_{C C}$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
|  |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
| ' | Open collector output current | C | $\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}$ |  |  |  | 100 |  |
| Ios | Output short-circuit current*** | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. | uts grounded. | its open. |  | 90 | 125 | mA |

## Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | taA $_{\text {An }}(\mathbf{n s})$ADDRESS ACCESS TIME |  | $t_{\text {EA }}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S081A | 9 | 15 | 9 | 20 | ns |
|  | 63S080, 63S081 | 9 | 25 | 9 | 20 |  |
| MILITARY | 53S080, 53S081 | 9 | 35 | 9 | 30 |  |

[^2]
## Features/Benefits

- 30-ns maximum access time
- Reliable titanium-tungsten fuses (TIW) guarantee greater than 98\% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs


## Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {M }}$ ) with 8 inputs, 4 outputs, and 256 product terms


## Description

The 53/63S140 and 53/63S141/A are $256 \times 4$ bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The $53 / 63$ S 140 and $53 / 63$ S141/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 1 K | 256x4 | TS | $\begin{gathered} 16 \\ (20) \end{gathered}$ | $\begin{aligned} & \mathrm{N}, \mathrm{~J}, \mathrm{~W}, \\ & (\mathrm{NL}),(\mathrm{L}) \end{aligned}$ | Enhanced | 63S141A | 53S141A |
|  |  | TS |  |  | Standard | 635141 | $53 S 141$ |
|  |  | OC |  |  |  | 635140 | $53 S 140$ |

## Pin Configurations



Plastic Chip Carrier

## Block Diagram



## Absolute Maximum Ratings

Operating
Programming

12 V
Input voltage .................................................................................. . 1.5 V to 7 V
Input current . ............................................................................ -30 mA to +5 mA

Storage temperature
$-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY <br> COMMERCIAL |  |  | UNIT |
| :--- | :--- | :--- | :--- | :--- | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | MIN NOM MAX | MIN NOM MAX |  |  |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature | 4.5 | 5 | 5.5 | 4.75 |

## Electrical Characteristics Over Operating Conditions



Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $\begin{gathered} \text { tAA }_{\text {AA }} \text { (ns) } \\ \text { ADDRES ACCESS TIME } \end{gathered}$ |  | $t_{\text {EA }}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S141A | 20 | 30 | 10 | 20 | ns |
|  | 63S140, 635141 | 20 | 45 | 10 | 25 |  |
| MILITARY | 53S141A | 20 | 40 | 10 | 30 |  |
|  | 53S140, 53S141 | 20 | 55 | 10 | 30 |  |

[^3]
# High Performance 512x4 PROM Ti-W PROM Family 

## Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $98 \%$ programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs


## Applications

- Microprogram control store
- Microrocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE ${ }^{\top 4}$ ) with 9 inputs, 4 outputs, 512 product terms


## Description

The 53/63S240 and 53/63S241/A are $512 \times 4$ bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titaniumtungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The $53 / 63 S 240$ and $53 / 63 S 241 /$ A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic Ti-W PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 2 K | $512 \times 4$ | TS | $\begin{gathered} 16 \\ (20) \end{gathered}$ | $\begin{gathered} \mathrm{N}, \mathrm{~J}, \mathrm{~W}, \\ (\mathrm{NL}),(\mathrm{L}) \end{gathered}$ | Enhanced | 63S241A | 53S241A |
|  |  | TS |  |  | Standard | 63 S 241 | 53S241 |
|  |  | OC |  |  |  | 63S240 | 53S240 |

## Pin Configurations




Plastic Chip Carrier

## Block Diagram



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | NOM | MAX |  |  |  |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | $V$ |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  | 2 |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $V_{C C}=$ MIN $\quad I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| 1 IL | Low-level input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX} \quad \mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| 1 H | High-level input current | $V_{C C}=M A X$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}^{\mathrm{OL}}=16 \mathrm{~mA}$ | Com |  | 0.45 | V |
|  |  |  |  | Mil |  | 0.5 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage* | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Com ${ }^{\mathrm{OH}}=-3.2 \mathrm{~mA}$ |  | 2.4 |  | V |
|  |  |  | Mil $\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}$ |  |  |  |  |
| ${ }^{1} \mathrm{OZL}$ | Off-state output current* | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 | $\mu \mathrm{A}$ |
| $\mathrm{I}^{\mathrm{OZH}}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 |  |
| ${ }^{\text {I CEX }}$ | Open collector output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  | $\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}$ |  |  | 100 |  |
| 10 S | Output short-circuit current** | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 | -90 | mA |
| ICC | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. All inputs grounded. All outputs open. |  |  | 80 | 130 | mA |

Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $t_{A A}(n s)$ ADDRESS ACCESS TIME |  | $t_{E A}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63 S 241 A | 25 | 35 | 12 | 20 | ns |
|  | 63S240, 63S241 | 25 | 45 | 12 | 25 |  |
| MILITARY | 53S241A | 25 | 45 | 12 | 30 |  |
|  | 53S240, 53S241 | 25 | 55 | 12 | 30 |  |

[^4]
## Features/Benefits

- 28-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98\% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs


## Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {tM }}$ ) with 8 inputs, 8 outputs, and 256 product terms


## Description

The $53 / 63 \mathrm{~S} 280$ and $53 / 63$ S281/A are $256 \times 8$ bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The 53/63S280 and 53/63S281/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NIMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 2 K | 256x8 | TS | 20 | N,J,W NL, L | Enhanced | 63S281A | 53S281A |
|  |  | TS |  |  | Standard | 635281 | 53 S 281 |
|  |  | OC |  |  |  | 635280 | 53S288 |

## Pin Configurations



Block Diagram


## Absolute Maximum Ratings

Operating
Programming
Supply voltage $V_{C C}$. -0.5 V to 7 V .12 V
Input voltage ............................................................................ 1.5 V to 7 V
Input current ..................................................................... -30 mA to +5 mA

Storage temperature ..................................................................... $65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| TA | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## DC Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{1 C}$ | Input clamp voltage | $V_{C C}=M I N$ | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| 1 H | High-level input current | $V_{C C}=M A X$ | $V_{1}=V_{C C} M A$ |  |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  |  | Com |  |  | 0.45 |  |
| ${ }^{\text {OL }}$ | utput | $V_{C C}=M 1 N$ | $\mathrm{OL}=16 \mathrm{~mA}$ | Mil |  |  | 0.5 | $\checkmark$ |
| $\mathrm{V}_{\mathrm{OH}}$ | * | $V_{C C}=\mathrm{MIN}$ | Com $\mathrm{IOH}=$ |  | 24 |  |  | V |
| $\mathrm{OH}^{\text {O }}$ |  | $V_{C C}=M 1 N$ | Mil $\mathrm{I}_{\mathrm{OH}}=-2$ |  |  |  |  |  |
| ${ }^{1} \mathrm{OZL}$ | Off-state output current* |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 |  |
| ${ }^{1} \mathrm{OZH}$ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| ICEX | Open collector output current | $V_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 | A |
| CEX | Open collector output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current*** | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{\text {c Cc }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. | uts grounded. A | s open. |  | 90 | 140 | mA |

## Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $t_{A A}$ (ns) <br> ADDRESS ACCESS TIME |  | $t_{\text {EA }}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S281A | 21 | 28 | 18 | 25 | ns |
|  | 63S280, 63S281 | 21 | 45 | 18 | 25 |  |
| MILITARY | 53S281A | 21 | 40 | 18 | 30 |  |
|  | 53S280, 53S281 | 21 | 50 | 18 | 30 |  |

## Features/Benefits

- Replaces 24-pin 256x8 NiCr PROM (6336)
- Upward pinout-compatible with higher density PROMs
- 45-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $\mathbf{9 9 \%}$ programming yields
- Low voltage generic programming
- PNP inputs for low input current
- Three-state outputs with four enable pins


## Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter


## Description

The 63 S 285 is a $256 \times 8$ bipolar PROM featuring low-current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range.

## Programming

The $63 S 285$ PROM is programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  | PACKAGE |  | OUTPUT | PERFORMANCE | PART NUMBER |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE |  |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ |
| $2 K$ | $256 \times 8$ | 24 | N,J | TS | Standard | $63 S 285$ |

## Pin Configuration



## Part Numbering System



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL |  | PARAMETER | COMMERCIAL <br> MIN NOM MAX |
| :--- | :--- | ---: | ---: |
| VCC | Supply voltage | 4.75 | 5 |
| $T_{A}$ | Operating free-air temperature | 0 | V |

## DC Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN TYP $\dagger$ MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VIL | Low-level input voltage | Guaranteed input logical low voltage for all inputs $\dagger \dagger$ |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage | Guaranteed input logical high voltage for all inputs $\dagger \dagger$ |  | 2 | $V$ |
| $V_{1 C}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{I}}=-18 \mathrm{~mA}$ | -1.5 | $V$ |
| IIL | Low-level input current | $V_{C C}=$ MAX | $V_{1}=0.4 \mathrm{~V}$ | -0.25 | mA |
| 1 H | High-level input current | $V_{C C}=M A X$ | $V_{1}=V_{C C} M A X$ | 40 | $\mu \mathrm{A}$ |
| VOL | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOL}=16 \mathrm{~mA}$ | 0.45 | V |
| VOH | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOH}=-3.2 \mathrm{~mA}$ | 2.4 | V |
| IOZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ | -40 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ | 40 |  |
| los | Output short-circuit current* | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 -90 | mA |
| ICC | Supply current | $\mathrm{V}_{\mathrm{CC}}=$ MAX. All inputs grounded. All outputs open. |  | 115160 | mA |

Switching Characteristics over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | tAA (ns) ADDRESS ACCESS TIME |  | tEA AND tER (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S285 | 26 | 45 | 18 | 30 | ns |

[^5]
## High Performance 1024x4 PROM TiW PROM Family

## 53/63S440 53/63S441 53/63S441A

## Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than 98\% programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs


## Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable logic element (PLE $\left.{ }^{\text {TM }}\right) 10$ inputs, 4 outputs, 1024 product terms


## Description

The 53/63S440 and 53/63S441/A are $1024 \times 4$ bipolar PROMs featuring low input current PNP inputs, full Schottky clamping with open collector or three-state outputs. The titaniumtungsten fuses store a logical low and are programmed to the high-state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The 53/63S440 and 53/63S441/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 4 K | 1024×4 | TS | $\begin{gathered} 18 \\ (20) \end{gathered}$ | $\binom{\mathrm{N}, \mathrm{~J}, \mathrm{~W},}{(\mathrm{NL}),(\mathrm{L})}$ | Enhanced | 63S441A | 53S441A |
|  |  | TS |  |  | Standard | $63 S 441$ | 53 S 441 |
|  |  | OC |  |  |  | $63 S 440$ | $53 S 440$ |

## Pin Configuration



Block Diagram



## Absolute Maximum Ratings

Operating
Programming

Input voltage ................................................................................. 1.5 V to 7 V
Input current .......................................................................... . -30 mA to +5 mA
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ......... -0.5 V to 5.5 V


Operating Conditions

| SYMBOL | PARAMETER | MILITARY <br> COMMERCIAL |  |  | UNIT |
| :--- | :--- | ---: | ---: | ---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating free-air temperature | -55 | 125 | 0 | 5.25 |

## Electrical Characteristics over Operating Conditions



Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $t_{A A}$ (ns) ADDRESS ACCESS TIME |  | $t_{E A}$ AND tER (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S441A | 24 | 35 | 16 | 25 | ns |
|  | 63S440, 63S441 | 24 | 45 | 16 | 25 |  |
| MILITARY | 53S441A | 24 | 50 | 16 | 30 |  |
|  | 53S440, 53S441 | 24 | 55 | 16 | 30 |  |

[^6]
# High Performance $512 \times 8$ PROM TiW PROM Family 

## Features/Benefits

- 30 ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $98 \%$ programming yields
- Low voltage generic programming
- PNP inputs for low input current
- Open collector or three-state outputs


## Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {w }}$ ) with 9 inputs, 8 outputs, and 512 product terms


## Description

The $53 / 63 S 480$ and $53 / 63 S 481 / \mathrm{A}$ are $512 \times 8$ bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and open collector or three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The 53/63S480 and 53/63S481/A PROMs are programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 4 K | $512 \times 8$ | TS | 20 | N,J,F, <br> NL,L | Enhanced | 63S481A | 53S481A |
|  |  | TS |  |  | Standard | 63 S481 | 535481 |
|  |  | OC |  |  |  | 635480 | 535480 |

## Pin Configurations



Block Diagram


## Absolute Maximum Ratings


Input voltage .................................................................................. 1.5 V to 7 V
Input current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 30 mA to +5 mA
Off-state output voltage ................................................................... -0.5 V to 5.5 V
Storage temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

DC Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| ILL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| IH | High-level input current | $V_{C C}=M A X$ | $V_{1}=V_{C C} M A$ |  |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  |  | Com |  |  | 0.45 |  |
| ${ }^{\text {OL }}$ | Low-level output voltage | $V_{C C}=M I N$ | $\mathrm{l}^{\mathrm{OL}}=16 \mathrm{~mA}$ | Mil |  |  | 0.5 | V |
| V | High-level output voltage* |  | Com ${ }^{1} \mathrm{OH}=-$ |  | 2.4 |  |  | V |
| ${ }^{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=M 1 N$ | Mil ${ }^{\prime} \mathrm{OH}=-2$ |  | 2.4 |  |  | V |
| IOZL | Off-state output current* | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | $\mu$ |
| $\mathrm{IOZH}^{\prime}$ |  | $V_{C C}$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
|  | Open collector |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
| ' | Open collector | C | $\mathrm{V}_{\mathrm{O}}=5.5 \mathrm{~V}$ |  |  |  | 100 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current*** | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{\text {ICC }}$ | Supply current | $V_{C C}=M A X$. | uts grounded. | ts open |  | 104 | 155 | mA |

Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | ${ }^{t_{A A}}$ (ns) <br> ADDRESS ACCESS TIME |  | $t_{E A}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S481A | 22 | 30 | 18 | 25 | ns |
|  | 63S480, 635481 | 22 | 45 | 18 | 25 |  |
| MILITARY | 53S481A | 22 | 40 | 18 | 30 |  |
|  | 53S480, 53S481 | 22 | 50 | 18 | 35 |  |

[^7]
## Features/Benefits

- Upward pinout-compatible with higher density PROMs
- 45-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $99 \%$ programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Three-state outputs with four ANDed enable pins
- Saves space with 24 -pin SKINNYDIP® package


## Applications

- Microprogram control store
- Microprocessor program store
- Character generator
- Code converter
- Look-up table


## Description

The $53 S 485$ and $63 S 485$ are $512 \times 8$ bipolar PROMs featuring low current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The 535485 and $63 S 485$ PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  | OUTPUT | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION |  | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 4K | $512 \times 8$ | TS | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{aligned} & \text { NS,JS,N,J,W, } \\ & \text { (NL),(L) } \end{aligned}$ | Standard | $63 S 485$ | $53 S 485$ |

## Pin Configurations



## Absolute Maximum Ratings

| Supply voltage VCC | V to 7 V | 2 V |
| :---: | :---: | :---: |
| Input voltage | -1.5 V to 7 V | 7 V |
| Input current | -30 mA to +5 mA |  |
| Off-state output voltage | -0.5 V to 5.5 V | 12 V |
| Storage temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |  |

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY <br> COMMERCIAL |  |  | UNIT |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $V_{C C}$ | Supply voltage | MIN NOM MAX | MIN NOM | MAX |  |
| $T_{A}$ | Operating free-air temperature | 4.5 | 5 | 5.5 | 4.75 |

## DC Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage | Guaranteed input logical low voltage for all inputs |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage | Guaranteed input logical high voltage for all inputs |  |  | 2 |  |  | V |
| V IC | Input clamp voltage | $V_{C C}=$ MIN | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current | $V_{C C}=$ MAX | $V_{1}=V_{C C} M A X$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| VOL | Low-level output voltage | $V_{C C}=\mathrm{MIN}$ | $1 \mathrm{OL}=16 \mathrm{~mA}$ | Com |  |  | 0.45 | V |
|  |  |  |  | Mil |  |  | 0.5 |  |
| VOH | High-level output voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{Com} 1 \mathrm{OH}=-3.2 \mathrm{~mA}$ |  | 2.4 |  |  | V |
|  |  |  | Mil $\mathrm{IOH}^{\prime}=-2 \mathrm{~mA}$ |  |  |  |  |  |
| IOZL | Off-state output current | $V_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
| los** | Output short-circuit current** | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ICC | Supply current | $\mathrm{V}_{C C}=$ MAX. All inputs grounded. All outputs open. |  |  |  | 115 | 160 | mA |

## Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | tAA (ns) <br> ADDRESS ACCESS TIME |  | teA AND ter ( ns ) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63 S485 | 26 | 45 | 18 | 30 | ns |
| MILITARY | 53S485 | 26 | 55 | 18 | 35 |  |

[^8]
# High Performance 2048x4 PROM TiW PROM Family 

## 53/63S841 53/63S841A

## Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $98 \%$ programming yields
- Low-voltage generic programming
- PNP inputs for low input current


## Applications

- Microprogram control store
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ ) with 11 inputs, 4 outputs and 2048 product terms per output


## Description

The 53/63S841 and 53/63S841A are 2048×4 bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special onchip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The $53 / 63 S 841$ and $53 / 63$ S841A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 8 K | 2048×4 | TS | $\begin{gathered} 18 \\ (20)^{*} \end{gathered}$ | $\begin{array}{\|c\|} \hline \mathrm{N}, \mathrm{~J}, \mathrm{~W}, \\ (\mathrm{NL}),(\mathrm{L}) \end{array}$ | Enhanced | 63S841A | 53S841A |
|  |  |  |  |  | Standard | 635841 | 53S841 |

* Available in either a 20 or 28 terminal ceramic Leadless Chip Carrier.


## Pin Configurations



Block Diagram


## Absolute Maximum Ratings

Operating
-0.5 V to 7 V
-1.5 V to 7 V
-30 mA to +5 mA
Input voltage

Storage temperature
$-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

|  | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $V_{\text {CC }}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| TA | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  | V |
| $\mathrm{V}_{\mathrm{IC}}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\mathrm{I}_{\mathrm{IL}}$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current | $V_{C C}=M A X$ | $V_{1}=V_{C C} M A X$ |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  |  | Com |  | 0.45 |  |
| O | Low-level output voltage | $V_{C C}=M / N$ | L | Mil |  | 0.5 | $\checkmark$ |
| V OH | vel output voltage | $V_{C C}=\mathrm{MIN}$ | Com ${ }^{\circ} \mathrm{OH}=$ |  | 2.4 |  | V |
| $\mathrm{V}_{\mathrm{OH}}$ | , output voltage | $V_{C C}-M / N$ | Mil $\mathrm{IOH}^{=-2}$ |  |  |  |  |
| ${ }^{\mathrm{O}} \mathrm{OZL}$ | Off-state output curre | V | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 | A |
| $\mathrm{I}^{\mathrm{OZH}}$ | Off-state output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current* | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 | -90 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. | uts grounded. A | ts open. | 110 | 150 | mA |

Switching Characteristics over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $t_{A A}$ ( $n s$ ) <br> ADDRESS ACCESS TIME |  | $t_{E A}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S841A | 30 | 35 | 12 | 25 | ns |
|  | 635841 | 30 | 50 | 12 | 25 |  |
| MILITARY | 53S841A | 30 | 50 | 12 | 30 |  |
|  | 53S841 | 30 | 55 | 12 | 30 |  |

[^9]
## High Performance 1024x8 PROM TiW PROM Family

## 53/63S881 53/63S881A

## Features/Benefits

- 30-ns maximum access time
- Reliable titanium-tungsten fuses (TiW) guarantee greater than $99 \%$ programming yields
- Low-voltage generic programming
- PNP inputs for low input current
- Three-state outputs
- 24-pin SKINNYDIP® or 600-mil DIP package


## Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ ) with 10 inputs,

8 outputs and 1024 product terms

## Selection Guide

| MEMORY |  | OUTPUT | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION |  | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 8K | 1024×8 | TS | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{gathered} \text { NS,JS,N,J,W, } \\ \text { (NL),(L) } \end{gathered}$ | Enhanced | 635881A | 53S881A |
|  |  |  |  |  | Standard | 635881 | 535881 |

## Pin Configurations



## Description

The 53/63S881 and 53/63S881A are $1024 \times 8$ bipolar PROMs featuring low input current PNP inputs, full Schottky clamping, and three-state outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The 53/63S881 and 53/63S881A PROMs are programmed with the same programming algorithm as all other Monolithic Memories generic TiW PROMs. For details contact the factory.

## Absolute Maximum Ratings

| Absolute Maximum Ratings | Operating | Programming |
| :---: | :---: | :---: |
| Supply voltage $\mathrm{V}_{\mathrm{CC}}$ | -0.5 V to 7 V | ... 12 V |
| Input voltage | -1.5 V to 7 V | 7 V |
| Input current | -30 mA to +5 mA |  |
| Off-state output voltage | -0.5 V to 5.5 V | 12 V |
| Storage temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |  |

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY <br> MIN NOM |  |  | COMMERCIAL <br> MIN |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $V_{\text {CC }}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 |
| $T_{A}$ | Operating free-air temperature | -55 | 5.25 | V |  |

## DC Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage | Guaranteed input logical low voltage for all inputs |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage | Guaranteed input logical high voltage for all inputs |  |  | 2 |  |  | V |
| $V_{\text {I }} \mathrm{C}$ | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| ${ }^{1 / H}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{v}_{1}=\mathrm{V}_{\mathrm{CC}} M A$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOL}^{\prime}=16 \mathrm{~mA}$ | Com |  |  | 0.45 | V |
|  |  |  |  | Mil |  |  | 0.5 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Com ${ }^{\mathrm{OH}}{ }^{\text {a }}=-3.2 \mathrm{~mA}$ |  | 2.4 |  |  | V |
|  |  |  | $\mathrm{Mil} \mathrm{I}^{\mathrm{OH}}=-2 \mathrm{~mA}$ |  |  |  |  |  |
| 'OZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
| Ios | Output short-circuit current* | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=$ MAX. All inputs grounded. All outputs open. |  |  |  | 92 | 160 | mA |

## Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $t_{A A}(n s)$ <br> ADDRESS ACCESS TIME |  | $t_{\text {EA AND }}$ ter ( $^{\mathrm{ns})}$ ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 635881 A | 26 | 30 | 18 | 25 | ns |
|  | 635881 | 26 | 45 | 18 | 30 |  |
| MILITARY | 53S881A | 26 | 45 | 18 | 30 |  |
|  | 535881 | 26 | 55 | 18 | 35 |  |

[^10]
## High Performance 4096x4 PROM TiW PROM Family

## 53/63S1641 53/63S1641A

## Features/Benefits

- 35-ns maximum access time
- Reliable titanium-tungsten fuses (TiW)
- Low-voltage generic programming
- PNP inputs for low input current


## Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ ) 12 inputs, 4 outputs, 4096 product terms


## Description

The 53/63S1641 features low input current PNP inputs, full Schottky clamping and three-state outputs. The titaniumtungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The $53 / 63 S 1641$ PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT |  |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 16 K | $4 \mathrm{~K} \times 4$ | TS | $\begin{aligned} & \mathrm{N}, \mathrm{~J}, \\ & \mathrm{NL} \end{aligned}$ | Enhanced | 63S1641A | 53S1641A |
|  |  |  |  | Standard | $63 S 1641$ | $53 S 1641$ |

## Pin Configuration



## Block Diagram



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | NOM | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| TA | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  |  |  | 2 |  | V |
| $V_{1 C}$ | Input clamp voltage | $V_{C C}=M I N$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=\mathrm{V}_{\mathrm{CC}} \mathrm{M}$ |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  |  | Com |  | 0.45 |  |
| O | Low-level output voltage | V | ${ }^{\prime} \mathrm{OL}=16 \mathrm{~mA}$ | Mil |  | 0.5 | $\checkmark$ |
| V | High-level output voltage | $V_{C O}=\mathrm{MIN}$ | Com ${ }^{1} \mathrm{OH}=$ |  | 24 |  | V |
| OH | High-level output volage | $V_{C C}=\mathrm{MIN}$ | Mil ${ }^{\text {OH }}=$ |  |  |  |  |
| ${ }^{\prime} \mathrm{OZL}$ |  |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 | A |
| ${ }^{1} \mathrm{OZH}$ |  | $V_{C C}$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 | $\mu \mathrm{A}$ |
| ${ }^{\text {I OS }}$ | Output short-circuit current* | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 | -90 | mA |
| ${ }^{\text {ICC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. | uts grounded. | ts open. | 130 | 175 | mA |

## Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TIME | $\begin{gathered} \text { taA }_{\text {AA }} \text { (ns) } \\ \text { ADDRS } \end{gathered}$ |  | $t_{\text {EA AND }}$ ter $^{(n s)}$ ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S1641A | 28 | 35 | 12 | 25 | ns |
|  | 6351641 | 28 | 50 | 12 | 25 |  |
| MILITARY | 53S1641A | 28 | 50 | 12 | 30 |  |
|  | 5351641 | 28 | 65 | 12 | 30 |  |

[^11]
# High Performance 2048x8 PROM TiW PROM Family 

## 53/63S1681 53/63S1681A

## Features/Benefits

- 35-ns maximum access time
- 16384-bit memory
- Reliable titanium-tungsten fuses (TiW)
- Available in space saving SKINNYDIP® package


## Applications

## - Microprogram control stores

- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ ) 11 inputs, 8 outputs, 2048 product terms


## Description

The $53 / 63$ S1681 is a high-speed $2 \mathrm{~K} \times 8$ PROM which uses industry standard package and pin out. In addition, the device is available in the 24 -pin ( 0.3 in.) SKINNYDIP®.

The family features low current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The $53 / 63 S 1681$ PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  | OUTPUT | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION |  | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 16K | 2048×8 | TS | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{gathered} \mathrm{N}, \mathrm{NS}, \mathrm{~J}, \mathrm{JS}, \mathrm{~W}, \\ (\mathrm{NL}),(\mathrm{L}) \end{gathered}$ | Enhanced | 63S1681A | 53S1681A |
|  |  |  |  |  | Standard | 6351681 | $53 S 1681$ |

## Pin Configurations



Block Diagram



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY <br> MIN NOM MAX |  |  | COMMERCIAL <br> MIN NOM MAX |
| :--- | :--- | :--- | ---: | ---: | :---: |
| $V_{\text {CC }}$ | UnNIT |  |  |  |  |
| $T_{A}$ | Operating free air temperature | 4.5 | 5 | 5.5 | 4.75 |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $V_{1 H}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| V IC | Input clamp voltage | $V_{C C}=M I N$ | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| ${ }_{1} \mathrm{H}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }}$ MAX |  |  |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{I}^{\mathrm{OL}}=16 \mathrm{~mA}$ | Com |  |  | 0.45 | V |
|  |  |  |  | Mil |  |  | 0.5 |  |
| $\mathrm{VOH}^{\text {O }}$ | High-level output voltage | $V_{C C}=M I N$ | Com $\mathrm{IOH}=-3.2 \mathrm{~mA}$ |  | 2.4 |  |  | V |
|  |  |  | Mil ${ }^{\text {OH }}=-2 \mathrm{~mA}$ |  |  |  |  |  |
| ${ }^{\text {O }} \mathrm{OL}$ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
| IOS | Output short-circuit current* | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $V_{C C}=$ MAX. All inputs grounded. All outputs open. |  |  |  | 135 | 185 | mA |

## Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE | $\begin{gathered} \text { taA }_{\text {AA }}(\mathrm{ns}) \\ \text { ADDRESS ACCESS TIME } \end{gathered}$ |  | $t_{\text {EA }}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S1681A | 27 | 35 | 18 | 25 | ns |
|  | 6351681 | 27 | 50 | 18 | 30 |  |
| MILITARY | 53S1681A | 27 | 50 | 18 | 30 |  |
|  | 5351681 | 27 | 60 | 18 | 35 |  |

[^12]
# High Performance 4096x8 PROM TiW PROM Family 

## Features/Benefits

- 35-ns maximum access time
- 32768-bit memory
- Reliable titanium-tungsten fuses (TiW)
- PNP inputs for low input current


## Applications

- Microprogram control stores
- Microprocessor program store
- Look-up table
- Character generator
- Code converter
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ ) with 12 inputs, 8 outputs and 4096 product terms


## Description

The $53 / 63 S 3281$ is a high-speed $4 \mathrm{~K} \times 8$ PROM which uses industry standard pin out.
The family features low-current PNP inputs, full Schottky clamping and three-state outputs. The Titanium-Tungsten fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide preprogramming testing which assure high programming yields and high reliability.
The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

## Programming

The $53 / 63 S 3281$ PROM is programmed with the same programming algorithm as all other Monolithic Memories' generic TiW PROMs. For details contact the factory.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OUTPUT | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 32 K | 4096x8 | TS | $\begin{gathered} 24 \\ (28)^{\star} \end{gathered}$ | $\begin{gathered} \mathrm{N}, \mathrm{~J}, \mathrm{~W}, \\ (\mathrm{NL}),(\mathrm{L}) \end{gathered}$ | Enhanced | 6353281A | 53S3281A |
|  |  |  |  |  | Standard | 6353281 | 5353281 |

## Pin Configurations

## Absolute Maximum Ratings

Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | COMMERCIAL |  | MIN NOM MAX | UNIT |  |
| $V_{\text {CC }}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 |
| $T_{A}$ | Operating free-air temperature | -55 | 125 | 0 | 5.25 |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $\mathrm{V}_{1 \mathrm{C}}$ | Input clamp voltage | $V_{C C}=$ MIN | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| ${ }_{1 / H}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }}$ MAX |  |  |  | 40 | $\mu \mathrm{A}$ |
| VOL | Low-level output voltage |  | $1 \mathrm{~L}=16 \mathrm{~mA}$ | Com |  |  | 0.45 | V |
| VOL | Low-level output voltage | $V_{C C}=M /{ }^{\text {d }}$ | OL $=16 \mathrm{~mA}$ | Mil |  |  | 0.5 | $v$ |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=\mathrm{MIN}$ | Com ${ }^{1} \mathrm{OH}=$ |  | 2.4 |  |  | V |
| VOH | High-level output voltage | $V_{C C}-M N$ | Mil ${ }^{1} \mathrm{OH}=-2$ |  | 2.4 |  |  | $\checkmark$ |
| IOZL | ent | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ | , | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 |  |
| Ios | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. | uts grounded. Al | ts open. |  | 150 | 190 | mA |

Switching Characteristics Over Operating Conditions (See standard test load)

| OPERATING CONDITIONS | DEVICE TYPE |  |  | $t_{\text {EA }}$ AND ter (ns) ENABLE ACCESS TIME RECOVERY TIME |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | TYP $\dagger$ | MAX | TYP $\dagger$ | MAX |  |
| COMMERCIAL | 63S3281A | 26 | 35 | 18 | 30 | ns |
|  | 6353281 | 26 | 45 | 18 | 30 |  |
| MILITARY | 53S3281B | 26 | 40 | 18 | 35 |  |
|  | 53S3281A | 26 | 50 | 18 | 35 |  |
|  | 53S3281 | 26 | 60 | 18 | 35 |  |



53/63S081 63S081A
Typical TAA vs Temperature


53/63S141/A
Typical TAA vs Temperature


53/63S240 53/63S241/A

Typical TAA vs Temperature


Typical Icc vs Temperature


Typical Icc vs Temperature


## 53/63S280 53/63S281/A

Typical ICC vs Temperature


## 53/63S285

Typical ICC vs Temperature


Typical TAA vs Temperature


Typical TAA vs Temperature


53/63S440

Typical ICc vs Temperature


53/63S480
Typical ICC vs Temperature


## 53/63S441A

Typical TAA vs Temperature


## 53/63S481A

Typical TAA vs Temperature


## 53/63S485 53/63S485A

## Typical ICC vs Temperature



53/63S841
Typical ICC vs Temperature


Typical TAA vs Temperature


53/63S841A
Typical TAA vs Temperature



53/63S881 53/635881A
Typical TAA vs Temperature

## 53/63S1641 53/63S1641A

Typical Icc vs Temperature


Typical TAA vs Temperature


53/63S1681 53/63S1681A

## Typical Icc vs Temperature



53/63S3281 53/63S3281A

## Typical ICC vs Temperature <br> <br> e

 <br> <br> e}

## Typical TAA vs Temperature



Typical TAA vs Temperature


## Switching Test Load



## Definition of Waveforms



Notes: 1. Input pulse amplitude 0 V to 3.0 V .
2. Input rise and fall times $2-5 \mathrm{~ns}$ from 0.8 V to 2.0 V .
3. Input access measured at the 1.5 V level.
4. $t_{A A}$ is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ and measured at 1.5 V output level.
5. For open collector devices, $t_{E A}$ and $t_{E R}$ are measured at the 1.5 V output level with $\mathrm{S}_{1}$ closed and $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedence to " 1 " test, and closed for high impedance to " 0 " test.
${ }^{\mathrm{t} E R}$ is tested with $\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

[^13]
# High Performance $512 \times 8$ 

## Features/Benefits

- Versatile synchronous and asynchronous enables
- Asynchronous preset and clear
- Edge-triggered "D" registers
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- On-chip register simplifies system timing
- Faster cycle times
- 16 mA IOL output drive capability
- Reliable titanium-tungsten fuses (TI W), with programming yields typically greater than $98 \%$


## Applications

- Microprogram control store
- State sequencers/state machines
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE ${ }^{\text {™ }}$ )

9 Inputs, 8 Registered Outputs, 512 product terms

## Description

The 53/63RA481 and 53/63RA481A are $512 \times 8$ Registered PROMs with on-chip " $D$ " type registers, versatile output enable control through synchronous and asynchronous three-state enable inputs, and asynchronous preset and clear.

Data is transferred into the output registers on the rising edge of the clock. The data will appear at the outputs provided that both the asynchronous ( $\bar{E}$ ) and synchronous ( $\overline{\mathrm{ES}}$ ) enables are Low. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made more flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting Eto a High or if $\overline{E S}$ is High when the rising clock edge occurs. When $V_{C C}$ power is first applied, the synchronous enable flip-flop will be in the set condition causing the outputs to be in the highimpedance state.

The output registers will be set to all Highs when preset is Low independent of the state of clock. The output registers will be reset to all Lows when clear is Low independent of the state of clock. Note that preset and clear are exclusive operations and cannot occur simultaneously.

## Selection Guide

| MEMORY |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 4 K | $512 \times 8$ | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{gathered} \mathrm{NS}, \mathrm{JS}, \\ \mathrm{~W}, \\ (\mathrm{NL}),(\mathrm{L}) \end{gathered}$ | Enhanced | 63RA481A | 53RA481A |
|  |  |  |  | Standard | 63RA481 | 53RA481 |

## Block Diagram



## Pin Configurations




Plastic Chip Carrier

## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | TYP $\dagger$ | COMMERCIAL |  |  |  | MILITARY |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 63RA481A |  | 63RA481 |  | 53RA481A |  | 53RA481 |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 5.0 | 4.75 | 5.25 | 4.75 | 5.25 | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature | 25 | 0 | 75 |  | 75 | -55 | 125 | -55 | 125 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of clock (High or Low) | 10 | 20 |  | 20 |  | 20 |  | 20 |  | ns |
| $t_{\text {prw }}$ | Width of preset or clear | 10 | 20 |  | 20 |  | 20 |  | 20 |  | ns |
| ${ }^{\text {t }}$ crw | (Low) to Output (High or Low) |  |  |  |  |  |  |  |  |  |  |
| ${ }_{\text {t }}^{\text {prr }}$ | Recovery from preset or clear | 11 | 20 |  | 20 |  | 25 |  | 25 |  | ns |
| ${ }_{\text {c }}^{\text {clir }}$ | (Low) to clock High |  |  |  |  |  |  |  |  |  |  |
| $t_{s}(A)$ | Setup time from address to clock | 22 | 30 |  | 35 |  | 35 |  | 45 |  | ns |
| $\mathrm{t}_{s}(\overline{\mathrm{ES}})$ | Setup time from $\overline{\mathrm{ES}}$ to clock | 7 | 10 |  | 10 |  | 15 |  | 15 |  | ns |
| $t_{h}(A)$ | Hold time from address to clock | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $t_{h}(\overline{E S})$ | Hold time from $\overline{E S}$ to clock | -3 | 5 |  | 5 |  | 5 |  | 5 |  | ns |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2.0 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ | * |  | -1.2 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| 1 H | High-level input current | $V_{C C}=M A X$ | $v_{1}=v_{C C}$ | \% |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{IOL}=16 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=$ MIN | Com ${ }^{\text {OH }}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
|  |  |  | Mil $\mathrm{IOH}=-2 \mathrm{~mA}$ |  |  |  |  |
| IOZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 | $\mu \mathrm{A}$ |
| O OH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 |  |
| IOS | Output short-circuit current* | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $V_{C C}=M A X$. | All inputs TTL. All outputs open. |  | 130 | 180 | mA |

[^14]Switching Characteristics Over Operating Conditions and using Standard Test Load

| SYMBOL | PARAMETER | TYP+ | COMMERCIAL |  |  |  | MILITARY |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 63RA481A |  | 63RA481 |  | 53RA481A |  | 53RA481 |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\text {t CLK }}$ | Clock to output Delay | 11 |  | 15 |  | 20 |  | 20 |  | 25 | ns |
| $t_{\text {teSA }}$ | Clock to output access time (ES) | 14 |  | 25 |  | 30 |  | 30 |  | 35 | ns |
| ${ }^{\text {t }}$ ESR | Clock to output recovery time ( $\overline{\mathrm{ES}}$ ) | 14 |  | 25 |  | 30 |  | 30 |  | 35 | ns |
| ${ }^{\text {t }}$ EA | Enable to output access time ( $\overline{\mathrm{E}})$ | 10 |  | 20 |  | 30 |  | 25 |  | 35 | ns |
| $\mathrm{t}_{\mathrm{ER}}$ | Disable to output recovery time ( $\overline{\mathrm{E}})$ | 10 |  | 20 |  | 30 |  | 25 |  | 35 | ns |
| ${ }^{\text {t }}$ PR | Preset to output delay ( $\overline{\mathrm{PR}}$ ) | 15 |  | 25 |  | 25 |  | 25 |  | 30 | ns |
| ${ }^{t}$ CLR | Clear to output delay ( $\overline{\mathrm{CLR}}$ ) | 18 |  | 25 |  | 30 |  | 35 |  | 40 | ns |

$\dagger$ Typicals at $5.0 \vee \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

## Function Table

| $\overline{\mathrm{E}}$ | ES | CLK | $\overline{\mathbf{P R}}$ | $\overline{C L R}$ | A8-A 0 | Q7-Q0 | Operation |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| H | X | X | X | X | X | Z | High-Impedance |
| X | H | 1 | X | X | X | Z | High-Impedance |
| L | L | X | L | H | X | H | Preset |
| L | L | X | H | L | X | L | Clear |
| L | L | X | L | L | X |  | Ilegal Operation |
| L | L | 1 | H | H | A | Data | Memory Access |

## Definition of Waveforms



# High Performance 1024x8 

## Features/Benefits

- Edge triggered "D" registers
- Synchronous and asynchronous enables
- Versatile 1:16 initialization words
- 8-Bit-wide in 24-pin SKINNYDIP® package for high board density
- Simplifies system timing
- Faster cycle times
- $16 \mathrm{~mA} \mathrm{I}_{\mathrm{OL}}$ output drive capability
- Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than $\mathbf{9 8 \%}$


## Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE ${ }^{\text {rw }}$ )

10 Inputs, 8 Registered Outputs, 1024 product terms

## Description

The 53/63RS881 and 53/63RS881A are $1 \mathrm{Kx8}$ PROMs with onchip " $D$ " type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start up sequencing through programmable initialization.
Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous (E) and synchronous (ES) enables are low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\bar{E}$ to a high or if $\overline{E S}$ is high when the rising clock edge occurs. When $\mathrm{V}_{\mathrm{C}}$ p power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin low, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). The unprogrammed state of $\overline{I S}$ words are low, presenting a CLEAR with IS pin low. With all $\bar{I}$ column words (A3-A0) programmed to the same pattern, the $\overline{\mathrm{I}}$ function will be independent of both row and column addressing and may be used as a single pin control. With all IS words programmed high a PRESET function is performed.

## Selection Guide

| MEMORY |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 8 K | 1024x8 | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{gathered} \mathrm{NS}, \mathrm{JS}, \\ \mathrm{~J}, \mathrm{~W}, \\ \text { (NL),(L) } \end{gathered}$ | Enhanced | 63RS881A | 53RS881A |
|  |  |  |  | Standard | 63RS881 | 53RS881 |

## Block Diagram



## Pin Configurations




## Absolute Maximum Ratings

$\qquad$


Storage temperature $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | TYP $\dagger$ | MILITARY |  |  |  | COMMERCIAL |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 53RS881A |  | 53RS881 |  | 63RS881A |  | 63RS881 |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $t_{w}$ | Width of clock (high or low) | 10 | 20 |  | 20 |  | 20 |  | 20 |  | ns |
| $\mathrm{t}_{5}(\mathrm{~A})$ | Setup time from address to clock | 25 | 40 |  | 45 |  | 30 |  | 35 |  | ns |
| $\left.\mathrm{t}_{\mathrm{S}} \overline{\mathrm{ES}}\right)$ | Setup time from $\overline{\mathrm{ES}}$ to clock | 8 | 15 |  | 15 |  | 15 |  | 15 |  | ns |
| $\mathrm{t}_{\mathrm{s}} \overline{(\mathrm{IS})}$ | Setup time from $\overline{\bar{S}}$ to clock | 20 | 30 |  | 35 |  | 25 |  | 30 |  | ns |
| th(A) | Hold time address to clock | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $t_{\text {L }}(\overline{\mathrm{ES}})$ | Hold time ( $\overline{\mathrm{ES}}$ ) | -3 | 5 |  | 5 |  | 5 |  | 5 |  | ns |
| th( $\overline{\mathrm{IS}}$ ) | Hold time ( $\overline{\mathrm{IS}}$ ) | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.75 | 5.25 | 4.75 | 5.25 | V |
| TA | Operating free-air temperature | 25 | -55 | 125 | -55 | 125 | 0 | 75 | 0 | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2.0 |  |  | V |
| V IC | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ | - |  | -1.2 | V |
| 1 LL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| ${ }_{1 / \mathrm{H}}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }} \mathrm{MAX}$ |  |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Com $\mathrm{IOH}^{\prime}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
|  |  |  | Mil ${ }^{\text {OH }}=-2 \mathrm{~mA}$ |  |  |  |  |
| ${ }^{1} \mathrm{OZL}$ |  |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 |  |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 |  |
| IOS | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ICC | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$. | ts TTL. All outputs open. |  | 130 | 180 | mA |

[^15]
## Switching Characteristics over Operating Conditions and using Standard Test Load



## Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V .
2. Input rise and fall times $2-5 \mathrm{~ns}$ from 0.8 V to 2.0 V .
3. Input access measured at the 1.5 V level.
4. $t_{A A}$ is tested with switch $S_{1}$ closed. $C_{L}=30 \mathrm{pF}$ and measured at 1.5 V output level.
5. $\mathrm{t}_{\text {EA }}$ and $\mathrm{t}_{\text {EA }}$ are measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test and closed for high impedance to " 0 " test.
${ }^{t_{E R}}$ and $t_{E A}$ are measured. $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{O H}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Features/Benefits

- Synchronous output enable
- Edge-triggered " $D$ " registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® for high board density
- Simplifies system timing
- Faster cycle times
- $16 \mathrm{~mA} \mathrm{I}_{\mathrm{OL}}$ output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than $\mathbf{9 8 \%}$


## Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ ) 11 Inputs, 8 Registered Outputs, 2048 product terms


## Description

The 53/63RA1681 and 53/63RA1681A are $2 \mathrm{~K} \times 8$ PROMs with on-chip "D"-type registers. Output enable control through an asynchronous enable input and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous enable $(\bar{E})$ is low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing.
Memory expansion and data control is made flexible with asynchronous enable inputs. Outputs may be set to the high impedance state at any time by setting $\bar{E}$ to a HIGH.
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin LOW, one of the 16 column words (A3-A0) will be set in the output registers independent of the row addresses (A9-A4). With all IS column words (A3-A0) programmed to the same pattern, the $\overline{I S}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{I S}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{\mathrm{IS}}$ words are LOW, presenting a CLEAR with $\overline{\mathrm{I}}$ pin LOW.

## Selection Guide

| MEMORY |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 16 K | 2048×8 | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{gathered} \hline \mathrm{NS}, \mathrm{JS}, \\ \mathrm{~W}, \\ \mathrm{NL}),(\mathrm{L}) \end{gathered}$ | Enhanced | 63RA1681A | 53RA1681A |
|  |  |  |  | Standard | 63RA1681 | 53RA1681 |

## Block Diagram



## Pin Configurations




Plastic Chip Carrier

## 53/63RA1681 53/63RA1681A

## Absolute Maximum Ratings

Operating

Input voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -1.5 V to 7 V
Input current. ........................................................................... -30 mA to +5 mA
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to 5.5 V


Programming

## Operating Conditions

| SYMBOL | PARAMETER | TYP $\dagger$ | MILITARY |  |  |  | COMMERCIAL |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 53RA1681A |  | 53RA1681 |  | 63RA1681A |  | 63RA1681 |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $t_{w}$ | Width of clock (high or low) | 10 | 20 |  | 20 |  | 20 |  | 20 |  | ns |
| $\mathrm{t}_{\mathrm{S}}(\mathrm{A})$ | Setup time from address to clock | 28 | 40 |  | 45 |  | 35 |  | 40 |  | ns |
| $\mathrm{t}_{\mathbf{S}(\mathrm{IS}}$ ) | Setup time from $\overline{\bar{S}}$ to clock | 20 | 30 |  | 35 |  | 25 |  | 30 |  | ns |
| th(A) | Hold time address to clock | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $\operatorname{th}(\overline{\mathrm{S}})$ | Hold time (İS) | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.75 | 5.25 | 4.75 | 5.25 | V |
| TA | Operating free-air temperature | 25 | -55 | 125 | -55 | 125 | 0 | 75 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2.0 |  |  | V |
| VIC | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.2 | V |
| ILL | Low-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High-level input current | $V_{C C}=$ MAX | $V_{1}=V_{C C} M A X$ |  |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{l}_{\mathrm{OL}}=16 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{C C}=\mathrm{MIN}$ | Com $\mathrm{IOH}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
|  |  |  | Mil $\mathrm{O}_{\mathrm{OH}}=-2 \mathrm{~mA}$ |  |  |  |  |
| IOZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 | $\mu \mathrm{A}$ |
| ${ }^{\text {O }} \mathrm{OH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 |  |
| Ios | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=$ MAX. All inputs TTL. All outputs open. |  |  | 140 | 185 | mA |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ Typicals at $5.0 \vee \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$


## Switching Characteristics Over Operating Conditions and using Standard Test Load


$\dagger$ Typicals at 5.0 V VCC and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

## Definition of Waveforms



Notes: 1. Input pulse amplitute 0 V to 3.0 V .
2. Input rise and fall times $2-5 \mathrm{~ns}$ from 0.8 V to 2.0 V .
3. Input access measured at the 1.5 V level.
4. Switch $\mathrm{S}_{1}$ is closed. $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ and outputs measured at 1.5 V output level for all tests except teA and terR
5. tEA and TESA are measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
$t_{E R}$ and $t_{E S R}$ are tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $V_{O H}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## 2048x8

 Registered PROM
## Features/Benefits

- Synchronous output enable
- Edge-triggered "D" registers
- Versatile 1:16 user programmable initialization words
- 8-bit-wide in 24-pin SKINNYDIP® ${ }^{\circledR}$ for high board density
- Simplifies system timing
- Faster cycle times
- 16 mA IOL output drive capability
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98\%


## Applications

- Microprogram control store
- State sequencers
- Next address generation
- Mapping PROM
- Programmable Logic Element (PLE ${ }^{\text {TM }}$ )

11 Inputs, 8 Registered Outputs, 2048 product terms

## Description

The 53/63RS1681 and 53/63RS1681A are $2 \mathrm{~K} \times 8$ PROMs with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.
Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous (ES) enable is LOW, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.
Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting $\overline{E S}$ HIGH before the rising clock edge occurs. When $V_{C C}$ power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.
The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin LOW, one of the 16 column words (A3-AO) will be set in the output registers independent of the row addresses (A10-A4). With all IS column words (A3-A0) programmed to the same pattern, the $\overline{\text { IS }}$ function will be independent of both row and column addressing and may be used as a single pin control. With all IS words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{\mathrm{I}}$ words are LOW, presenting a CLEAR with $\overline{\mathrm{S}}$ pin LOW.

## Selection Guide

| MEMORY |  | PACKAGE |  | PERFORMANCE | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE |  | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 16 K | $2048 \times 8$ | $\begin{gathered} 24 \\ (28) \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { NS, JS, } \\ \text { W, } \\ (N L),(L) \end{array}$ | Enhanced | 63RS1681A | 53RS1681A |
|  |  |  |  | Standard | 63RS1681 | 53RS1681 |

## Block Diagram



## Pin Configurations




Plastic Chip Carrier

## Absolute Maximum Ratings

Operating
Programming
Supply voltage $V_{C C}$ -0.5 V to 7 V 12 V
input voltage $\ldots-1.5 \mathrm{~V}$ to 7 V
Input current . . ............................................................................... mA to +5 mA
-0.5 V to 5.5 V
.7 V
Off-state output voltage
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | TYP $\dagger$ | MILITARY |  |  |  | COMMERCIAL |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 53RS1681A |  | 53RS1681 |  | 63RS1681A |  | 63RS1681 |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $t_{\text {w }}$ | Width of clock (high or low) | 10 | 20 |  | 20 |  | 20 |  | 20 |  | ns |
| $t_{s}(A)$ | Setup time from address to clock | 28 | 40 |  | 45 |  | 35 |  | 40 |  | ns |
| $\left.\mathrm{t}_{\mathrm{s}} \overline{\mathrm{ES}}\right)$ | Setup time from ES to clock | 7 | 15 |  | 15 |  | 15 |  | 15 |  | ns |
| $\mathrm{t}_{\mathrm{s}} \overline{(\mathrm{IS})}$ | Setup time from $\overline{\bar{S}}$ to clock | 20 | 30 |  | 35 |  | 25 |  | 30 |  | ns |
| $\operatorname{th}(\mathrm{A})$ | Hold time address to clock | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $\operatorname{th}(\overline{\mathrm{ES}})$ | Hold time (ES) | -3 | 5 |  | 5 |  | 5 |  | 5 |  | ns |
| th(IS) | Hold time (IS) | -5 | 0 |  | 0 |  | 0 |  | 0 |  | ns |
| $V_{C C}$ | Supply voltage | 5 | 4.5 | 5.5 | 4.5 | 5.5 | 4.75 | 5.25 | 4.75 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | 25 | -55 | 125 | -55 | 125 | 0 | 75 | 0 | 75 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  | 6 | 2.0 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | 1. |  |  | -1.2 | V |
| 1 L | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0,25 | mA |
| ${ }_{1 / H}$ | High-level input current | $V_{C C}=M A X$ | $V_{1}=V_{\text {CC }}$ MAX |  |  | 40 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=M I N$ | Com ${ }^{\circ} \mathrm{OH}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
|  |  |  | Mil ${ }^{\mathrm{OH}}$ = $=-2 \mathrm{~mA}$ |  |  |  |  |
| IOZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -40 | $\mu \mathrm{A}$ |
| 1 OZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 |  |
| Ios | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ${ }^{\text {I Cc }}$ | Supply current | $\mathrm{V}_{C C}=$ MAX. All inputs TTL. All outputs open. |  |  | 140 | 185 | mA |

[^16]
## Switching Characteristics Over Operating Conditions and using Standard Test Load



[^17]
## Definition of Waveforms



Notes: 1. Input pulse amplitute 0 V to 3.0 V .
2. Input rise and fall times $2-5 \mathrm{~ns}$ from 0.8 V to 2.0 V .
3. Input access measured at the 1.5 V level.
4. Switch $S_{1}$ is closed. $C_{L}=30 \mathrm{pF}$ and outputs measured at 1.5 V output level for all tests except $t_{E S A}$ and $t_{E S R}$.
5. tEA and LESA are measured at the 1.5 V output level with $C_{L}=30 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
tER and $t_{E S R}$ are tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Switching Test Load



## Definition of Timing Diagrams



CENTER LINE IS HIGH IMPEDANCE STATE


WILL BE STEADY

## Schematic of Inputs and Outputs


(53DA1643 Only)


## Switching Test Load



## Definition of Timing Diagrams



## Schematic of Inputs and Outputs



## Features/Benefits

- Programmable asynchronous output initialization
- Three-state outputs with two enables
- Provides system diagnostic testing with system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® package saves space
- 24-mA output drive capability
- Replaces embedded diagnostic code
- Guaranteed programming yields of greater than 98\%


## Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing


## Description

The $53 / 63 D A 441$ and $53 / 63 D A 442$ are $1 \mathrm{Kx4}$ PROMs with registered outputs, programmable asynchronous initialization, three-state outputs with two enables and a shadow register for diagnostic capabilities.

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus.

During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and paraliel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

When exercised, the initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This features is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

The distinguishing feature between the 53/63DA441 and 53/ 63DA442 is on the output enable structure. The 53/63DA441 has two asynchronous output enables, $\overline{\mathrm{E} 1}$ and $\overline{\mathrm{E} 2}$. Outputs will be enabled when both E1 and E2 are LOW. The 53/63DA442 has one asynchronous output enable $\bar{E}$ and one synchronous output enable $\overline{\mathrm{ES}}$. Outputs will be enabled if $\overline{\mathrm{ES}}$ is LOW during the last rising edge of CLK and $\bar{E}$ is LOW.

## Selection Guide

| MEMORY |  |  | PACKAGE |  | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | OPTIONS | PINS | TYPE | MILITARY | COMMERCIAL |
| 4 K | 1024x4 | Two asynchronous enables | $\begin{aligned} & 24 \\ & (28) \end{aligned}$ | $\begin{aligned} & \text { NS,JS,W, } \\ & \text { (NL),(L) } \end{aligned}$ | 53DA441 | 63DA441 |
|  |  | One synchronous enable, one asynchronous enable |  |  | 53DA442 | 63DA442 |

## Block Diagrams



## Logic Symbols




Plastic Chip Carrier

## Function Table

| INPUTS |  |  |  | OUTPUTS |  |  | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | SDI | CLK | DCLK | Q3-Q0 | S3-S0 | SDO |  |
| L | X | 1 | * | $\mathrm{Qn} \leftarrow \mathrm{PROM}$ | HOLD | S3 | Load output register from PROM array |
| L | X | * | $\uparrow$ | HOLD | $\begin{aligned} & S n \leftarrow S n-1 \\ & S 0 \leftarrow S D I \end{aligned}$ | S3 | Shift shadow register data |
| L | X | 1 | $\uparrow$ | $\mathrm{Qn}^{-}-\mathrm{PROM}$ | $\begin{aligned} & S n \leftarrow S n-1 \\ & S 0 \leftarrow S D I \end{aligned}$ | S3 | Load output register from PROM array while shifting shadow register data |
| H | $X$ | 1 | * | Qn - Sn | HOLD | SDI | Load output register from shadow register |
| H | L | * | $\dagger$ | HOLD | $\mathrm{Sn} \leftarrow \mathrm{Qn}$ | SDI | Load shadow register from output bus |
| H | H | * | 1 | HOLD | HOLD | SDI | No operation $\dagger$ |

* Clock must be steady or falling.
$\dagger$ Reserved operation for SN54/74S818 8-Bit Diagnostic Register.


## Definition of Signals

MODE $\quad$ The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.

SDI The Serial Data In pin is the input to the leastsignificant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.

CLK The clock pin loads the output register on the rising edge of CLK.
DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 Qn represents the data outputs of the output register. During a shadow register load with outputs enabled, these pins are the internal data inputs to the shadow register. With the outputs three-stated, these pins are external data inputs to the shadow register.
S3-S0 Sn represents the internal shadow register outputs.
An represents the address inputs to the PROM array.
$\overline{\mathrm{E}}, \overline{\mathrm{E}}, \overline{\mathrm{E}} \quad$ These Output Enable pin(s) operate independent of CLK. For'D441, outputs are enabled if, and only if, both E1 and E2 are LOW. For D442, outputs are enabled only when ES is LOW at the last rising edge of CLK and $\overline{\mathrm{E}}$ is LOW.
ES $\quad$ Synchronous Output Enable for 'DA442 only. Outputs are enabled only when ES is LOW at the last rising edge of CLK and $\bar{E}$ is LOW.
The asynchronous output register initialization input pin operates independent of CLK. When II is LOW, the output register is loaded with a userprogrammable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction system reset or interrupt.

## Logic Diagram

53/63DA441
1024x4 Diagnostic PROM with Asynchronous Initialization and Asynchronous Enables


## Logic Diagram

53/63DA442
$1024 \times 4$ Diagnostic PROM with Asynchronous Initialization and Both Asynchronous and Synchronous Enables


## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{T}$ A | Operating free-air temperature | -55 | 25 | 125 | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of CLK (HIGH or LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $t_{\text {su }}$ | Setup time from address to CLK | 45 | 25 |  | 35 | 25 |  | ns |
| $t_{\text {h }}$ | Hold time for CLK | 0 | -15 |  | 0 | -15 |  | ns |
| ${ }_{\text {wd }}$ | Width of DCLK (HIGH or LOW) | 35 | 15 |  | 25 | 15 |  | ns |
| $\mathrm{t}_{\text {sud }}$ | Setup time from control inputs (SDI, MODE) to CLK, DCLK | 50 | 20 |  | 40 | 20 |  | ns |
| $t_{\text {hd }}$ | Hold time for DCLK | 0 | -5 |  | 0 | -5 |  | ns |
| $\mathrm{t}_{\mathrm{s}}(\overline{\mathrm{ES}})$ | Setup time from ES to CLK ('DA442 only) | 20 | 10 |  | 15 | 10 |  | ns |
| $t_{h}(\overline{\text { ES }})$ | Hold time (ES) ('DA442 only) | 5 | 0 |  | 5 | 0 |  | ns |
| $\mathrm{tiw}_{\text {iw }}$ | Initialization pulse width (LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {ir }}$ | Initialization recovery time | 45 | 30 |  | 40 | 30 |  | ns |

## Electrical Characteristics Over Operating Conditions



[^18]
## Switching Characteristics Over Operating Conditions and Using Standard Test Load

| SYMBOL | PARAMETER | MILITARY |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN TYP $\dagger$ | MAX |  | TYP $\dagger$ |  |  |
| ${ }^{\text {t CLK }}$ | CLK to output | 11 | 25 |  | 11 | 18 | ns |
| $\mathrm{t}_{\mathrm{ER}}$ | Disable time | 14 | 30 |  | 14 | 25 | ns |
| $t_{E A}$ | Enable time | 16 | 30 |  | 16 | 25 | ns |
| $t_{\text {MAXD }}$ | Maximum diagnostic clock frequency | $7 \quad 20$ |  | 10 | 20 |  | MHz |
| ${ }^{\text {t }}$ S | DCLK to SDO delay (MODE $=$ LOW $)$ | 17 | 35 |  | 17 | 30. | ns |
| ${ }^{\text {t SS }}$ | SDI to SDO delay ( $\mathrm{MODE}=\mathrm{HIGH}$ ) | 16 | 30 |  | 16 | 25 | ns |
| ${ }^{\text {tMS }}$ | MODE to SDO delay | 14 | 30 |  | 14 | 25 | ns |
| ${ }^{1} 1 Q$ | Initialization to output delay | 22 | 35 |  | 22 | 30 | ns |
| teSR | CLK to output disable time ('DA442 only) | 22 | 35 |  | 22 | 30 | ns |
| ${ }^{\text {t }}$ ESA | CLK to output enable time ('DA442 only) | 15 | 35 |  | 15 | 30 | ns |

$\dagger$ Typicals at $5.0 \vee \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C}_{\mathrm{A}}$.

## Definition of Waveforms



Normal PROM Operation (Mode $=$ LOW)
(for both 53/63DA441 and 53/63DA442 with outputs enabled)


Normal PROM Operation $($ Mode $=$ LOW $)$
(for 53/63DA442 only with $\overline{\mathrm{I}}=\mathrm{HIGH}$ )


SYSTEM CONTROL


SYSTEM OBSERVATION

## Features/Benefits

- Asynchronous output enable
- Programmable asynchronous output initialization
- Provides system diagnostic testing with system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered " $D$ " registers simplifies system timing
- Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- Reliable titanium-tungsten fuses (TiW), with programming yields typically greater than 98\%
- 24-mA output drive capability
- Replaces embedded diagnostic code


## Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing


## Description

The 53/63DA841 is a $2 \mathrm{~K} \times 4$ PROM with registered three-state outputs, programmable asynchronous initialization and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be par-allel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the register with a userprogrammable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt.

## Selection Guide

| MEMORY |  | PACKAGE |  | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 8 K | 2048x4 | $\begin{gathered} 24 \\ (28) \end{gathered}$ |  | 63DA841 | 53DA841 |

## Block Diagram



## Pin Configurations



Plastic Chip Carrier

## Function Table

| INPUTS |  |  |  | OUTPUTS |  |  | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | SDI | CLK | DCLK | Q3-Q0 | S3-50 | SDO |  |
| L | X | $\dagger$ | * | Qn - PROM | HOLD | S3 | Load output register from PROM array |
| L | X | * | 1 | HOLD | $\begin{aligned} & \mathrm{Sn}-\mathrm{Sn}-1 \\ & \mathrm{SO}-\mathrm{SDI} \end{aligned}$ | S3 | Shift shadow register data |
| L | X | $\dagger$ | 1 | Qn - PROM | $\begin{aligned} & S n-S n-1 \\ & S 0-S D I \end{aligned}$ | S3 | Load output register from PROM array while shifting shadow register data |
| H | X | $\dagger$ | * | $\mathrm{Qn}-\mathrm{Sn}$ | HOLD | SDI | Load output register from shadow register |
| H | L | * | 1 | HOLD | $\mathrm{Sn}-\mathrm{Qn}$ | SDI | Load shadow register from output bus |
| H | H | * | 1 | HOLD | HOLD | SDI | No operation $\dagger$ |

* Clock must be steady or falling.
$\dagger$ Reserved operation for SN54/74S818 8-Bit Diagnostic Register.


## Definition of Signals

The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.
The Serial Data in pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDl is also a control input to the shadow register when it is not in the shift mode.
The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

The clock pin loads the output register on the rising edge of CLK.

DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

A10-A0 An represents the address inputs to the PROM array.

The Output Enable pin operates independent of CLK. When $\bar{E}$ is LOW the outputs are enabled. When $\bar{E}$ is HIGH, the outputs are in the highimpedance state.
Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

Sn represents the internal shadow register outputs.

The asynchronous output register initialization input pin operates independent of CLK. When I is LOW, the output register is loaded with a userprogrammable initialization word. Programmable initialization is a super-set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

## Logic Diagram

$2048 \times 4$ Diagnostic PROM
with Asynchronous Enable
and Output Initialization


## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY MIN TYP ${ }^{\dagger}$ MAX |  |  | COMMERCIAL MIN TYP ${ }^{\text {C MAX }}$ |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 | 25 | 125 | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of CLK (HIGH or LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $t_{\text {su }}$ | Set up time from address to CLK | 45 | 27 |  | 40 | 27 |  | ns |
| $t_{h}$ | Hold time for CLK | 0 | -15 |  | 0 | -15 |  | ns |
| ${ }^{\text {wd }}$ | Width of DCLK (HIGH or LOW) | 45 | 15 |  | 40 | 15 |  | ns |
| $\mathrm{t}_{\text {sud }}$ | Set up time from control inputs (SDI, MODE) to CLK, DCLK | 50 | 20 |  | 45 | 20 |  | ns |
| thd | Hold time for DCLK | 0 | -5 |  | 0 | -5 |  | ns |
| $\mathrm{t}_{\text {iw }}$ | Initialization pulse width (LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $t_{\text {ir }}$ | Initialization recovery time | 45 | 30 |  | 40 | 30 |  | ns |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2.0 |  |  | V |
| VIC | Input clamp voltage | $V_{C C}=M I N$ | $1 .=-18 \mathrm{~mA}$ |  |  | -1.2 | V |
| IL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| $\mathrm{IIH}^{\prime}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=\mathrm{V}_{\text {CC }}$ MAX |  |  | 40 | $\mu \mathrm{A}$ |
| V OL | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Com $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  | 0.5 | V |
|  |  |  | Mil ${ }_{\mathrm{OL}}=16 \mathrm{~mA}$ |  |  |  |  |
| V OH | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Com $/ \mathrm{OH}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
|  |  |  | Mil ${ }^{\text {OH }}=-2 \mathrm{~mA}$ |  |  |  |  |
| ${ }^{1} \mathrm{OZL}$ |  |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ | e output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 40 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ${ }^{\text {ICC }}$ | Supply current | $V_{C C}=M A X$ | ts TTL. All outputs open. |  | 140 | 185 | mA |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

Switching Characteristics Over Operating Conditions and Using Standard Test Load

$\dagger$ Typical at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

## Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)


## SYSTEM CONTROL



# 4096x4 Diagnostic Registered PROM Asynchronous Enable 

## Features/Benefits

- Asynchronous output enable
- Provides system diagnostic testing for system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered " $D$ " registers simplifies system timing
- Casadable for wide control words used in microprogramming
- 24-pin SKINNYDIP ${ }^{\circledR}$ saves space
- 24-mA output drive capability
- Replaces embedded diagnostic code


## Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing


## Description

The 53/63D1641 is a $4 K \times 4$ PROM with registered three-state outputs and a shadow register for diagnostic capabilities.

Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register, is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. When the output drivers are disabled, the shadow register receives its parallel data from the output bus. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and paral-lel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independent of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming.

## Selection Guide

| MEMORY |  | PACKAGE |  | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE | $0^{\circ} \mathbf{C}$ to $+\mathbf{7 5}{ }^{\circ} \mathbf{C}$ | $-\mathbf{5 5}{ }^{\circ} \mathbf{C}$ to $+125^{\circ} \mathbf{C}$ |
| 16 K | $4096 \times 4$ | 24 | NS,JS, <br> W, <br> (NL),(L) | $63 D 1641$ | $53 D 1641$ |

## Block Diagram



## Pin Configurations




Plastic Chip Carrier

## Function Table

| INPUTS |  |  |  | OUTPUTS |  |  | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | SDI | CLK | DCLK | Q3-Q0 | S3-S0 | SDO |  |
| L | X | $\dagger$ | * | Qn $\leftarrow$ PROM | HOLD | S3 | Load output register from PROM array |
| L | X | * | $\uparrow$ | HOLD | $\begin{aligned} & S n-S n-1 \\ & S 0-S D I \end{aligned}$ | S3 | Shift shadow register data |
| L | X | $\uparrow$ | $\uparrow$ | Qn - PROM | $\begin{aligned} & S n-S n-1 \\ & S 0-S D I \end{aligned}$ | S3 | Load output register from PROM array while shifting shadow register data |
| H | X | $\uparrow$ | * | $\mathrm{Qn} \leftarrow \mathrm{Sn}$ | HOLD | SDI | Load output register from shadow register |
| H | L | * | $\dagger$ | HOLD | $\mathrm{Sn}-\mathrm{Qn}$ | SDI | Load shadow register from output bus |
| H | H | * | $\uparrow$ | HOLD | HOLD | SDI | No operation $\dagger$ |

* Clock must be steady or falling.
$\dagger$ Reserved operation for SN54/74S818 8-Bit Diagnostic Register.


## Definition of Signals

The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output bus. With MODE and SDI both HIGH, the shadow register holds its present data.
The Serial Data In pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode. most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

CLK The CLOCK pin loads the output register on the rising edge of CLK.

DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 Qn represents the data outputs of the output register. During a shadow register load with outputs enabled these pins are the internal data inputs to the shadow register. With the outputs three-stated these pins are external data inputs to the shadow register.

S3-S0 Sn represents the internal shadow register outputs.

A11-A0 An represents the address inputs to the PROM array.
$\bar{E}$
The Output Enable pin operates independent of CLK. When $\bar{E}$ is LOW the outputs are enabled. When $\bar{E}$ is HIGH, the outputs are in the high impedance state.

## Logic Diagram



## Absolute Maximum Ratings

## Operating

Programming
$\qquad$
Input voltage .................................................................................... . 1.5 V to 7 V
Input Current ....................................................................... -30 mA to +5 mA

Storage temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ..... $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP ${ }^{\dagger}$ | MAX | MIN | TYP ${ }^{\dagger}$ | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature | -55 | 25 | 125 | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of CLK (HIGH or LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Set up time from address to CLK | 45 | 25 |  | 40 | 25 |  | ns |
| $t_{h}$ | Hold time for CLK | 0 | -15 |  | 0 | -15 |  | ns |
| $\mathrm{t}_{\text {wd }}$ | Width of DCLK (HIGH or LOW) | 45 | 15 |  | 40 | 15 |  | ns |
| $t_{\text {sud }}$ | Set up time from control inputs (SDI, MODE) to CLK, DCLK | 50 | 20 |  | 45 | 20 |  | ns |
| $t_{\text {h }}$ d | Hold time for DCLK | 0 | -5 |  | 0 | -5 |  | ns |

Electrical Characteristics Over Operating Conditions


[^19]Switching Characteristics Over Operating Conditions and Using Standard Test Load

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | TYP ${ }^{\dagger}$ | MAX | MIN |  | MAX |  |
| ${ }^{\text {t CLK }}$ | CLK to output |  | 11 | 25 |  | 11 | 20 | ns |
| ${ }^{\text {E ER }}$ | Disable time |  | 16 | 30 |  | 16 | 25 | ns |
| ${ }^{\text {t }}$ EA | Enable time |  | 16 | 30 |  | 16 | 25 | ns |
| ${ }_{\text {f MAXD }}$ | Maximum diagnostic clock frequency | 7 | 18 |  | 10 | 18 |  | MHz |
| ${ }^{\text {t }}$ DS | DCLK to SDO delay (MODE = LOW) |  | 17 | 35 |  | 17 | 30 | ns |
| ${ }^{\text {t }}$ SS | SDI to SDO delay (MODE $=$ HIGH ) |  | 16 | 30 |  | 16 | 25 | ns |
| ${ }^{\text {tMS }}$ | MODE to SDO delay |  | 14 | 30 |  | 14 | 25 | ns |

$\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

## Definition of Waveforms



NORMAL PROM OPERATION (MODE = LOW)


## SYSTEM CONTROL



SYSTEM OBSERVATION

## Features/Benefits

- Programmable asynchronous output initialization
- Provides system diagnostic testing with system controllability and observability
- Shadow register eliminates shifting hazards
- Edge-triggered "D" registers simplifies system timing
- Cascadable for wide control words used in microprogramming
- 24-pin SKINNYDIP® saves space
- 24-mA output drive capability
- Replaces embedded diagnostic code


## Applications

- Microprogram control store with built-in system diagnostic testing
- Serial character generator
- Serial code converter
- Parallel in/serial out memory
- Cost-effective board testing


## Description

The 53/63DA1643 is a $4 K \times 4$ PROM with registered outputs, programmable asynchronous initialization, and a shadow register for diagnostic capabilities. Shadow register diagnostics allow observation and control of the system without introducing intermediate illegal states. The output register, which can receive parallel data from either the PROM array or the shadow register is loaded on the rising edge of CLK. The shadow register, which can receive parallel data from the output register or serial data from SDI, is loaded on the rising edge of DCLK. During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through SDO, allowing observation of the system. Similarly, diagnostic data can be serially shifted into the shadow register through SDI, and parallel-loaded into the output register, allowing control and test scanning to be imposed on the system. Since the output register and the shadow register are loaded by different input signals, they can be operated independently of one another. In addition, diagnostic PROMs can be cascaded to construct wide control words used in microprogramming. When exercised, the Initialization input loads the output register with a user-programmable initialization word, independent of the state of CLK. This feature is a superset of preset and clear functions, and can be used to generate an arbitrary microinstruction for system reset or interrupt

## Selection Guide

| MEMORY |  | PACKAGE |  | PART NUMBER |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SIZE | ORGANIZATION | PINS | TYPE | $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| 16 K | $4096 \times 4$ | 24 | NS,JS, |  |  |

## Block Diagram



## Pin Configurations




Plastic Chip Carrier

Function Table

| INPUTS |  |  |  | OUTPUTS |  |  | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | SDI | CLK | DCLK | Q3-Q0 | S3-S0 | SDO |  |
| L | X | $\dagger$ | * | Qn - PROM | HOLD | S3 | Load output register from PROM array |
| L | X | * | $\uparrow$ | HOLD | $\begin{aligned} & S n \leftarrow S n-1 \\ & S 0 \leftarrow S D I \end{aligned}$ | S3 | Shift shadow register data |
| L | X | $\dagger$ | 1 | Qn - PROM | $\begin{aligned} & S n-S n-1 \\ & S 0-S D 1 \end{aligned}$ | S3 | Load output register from PROM array while shifting shadow register data |
| H | X | $\dagger$ | * | $\mathrm{Qn}-\mathrm{Sn}$ | HOLD | SDI | Load output register from shadow register |
| H | L | * | $\uparrow$ | HOLD | $\mathrm{Sn} \leftarrow \mathrm{Qn}$ | SDI | Load shadow register from output bus |
| H | H | * | 1 | HOLD | HOLD | SDI | No operation $\dagger$ |

* Clock must be steady or falling.
$\dagger$ Reserved operation for SN54/74S818 8-Bit Diagnostic Register.


## Definition of Signals

MODE

SDI

SDO

The MODE pin controls the output register multiplexer and the shadow register. When MODE is LOW, the output register receives data from the PROM array and the shadow register is configured as a shift register with SDI as its input. When MODE is HIGH, the output register receives data from the shadow register. The shadow register is controlled by SDI as well as MODE. With MODE HIGH and SDI LOW, the shadow register receives parallel data from the output register. With MODE and SDI both HIGH, the shadow register holds its present data.
The Serial Data in pin is the input to the least significant bit of the shadow register when operating in the shift mode. SDI is also a control input to the shadow register when it is not in the shift mode.
The Serial Data Out pin is the output from the most significant bit of the shadow register when operating in the shift mode. When the shadow register is not in the shift mode, SDO displays the logic level present at SDI, decreasing serial shift time for cascaded diagnostic PROMs.

DCLK The diagnostic clock pin loads or shifts the shadow register on the rising edge of DCLK.

Q3-Q0 Qn represents the data outputs of the output register. During a shadow register load these pins are the internal data inputs to the shadow register.

S3-S0 $\quad$ Sn represents the internal shadow register outputs.

A11-A0 An represents the address inputs to the PROM array.
$T \quad$ The asynchronous output register initialization input pin operates independent of CLK. When I is LOW, the output register is loaded with a user programmable initialization word. Programmable initialization is a super set of preset and clear functions, and can be used to generate any microinstruction for system reset or interrupt.

## Logic Diagram


Absolute Maximum Ratings
Operating
-0.5 V to 7 V
12 V
Input voltage12 VStorage temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY MIN TYP ${ }^{\dagger}$ MAX |  |  | COMMERCIAL MIN TYP ${ }^{+}$MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 | 25 | 125 | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of CLK (HIGH or LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Set up time from address to CLK | 45 | 25 |  | 40 | 25 |  | ns |
| $t_{h}$ | Hold time for CLK | 0 | -15 |  | 0 | -15 |  | ns |
| $\mathrm{t}_{\mathrm{wd}}$ | Width of DCLK (HIGH or LOW) | 45 | 15 |  | 40 | 15 |  | ns |
| ${ }^{\text {t }}$ sud | Set up time from control inputs (SDI, MODE) to CLK, DCLK | 50 | 20 |  | 45 | 20 |  | ns |
| thd | Hold time for DCLK | 0 | -5 |  | 0 | -5 |  | ns |
| $t_{\text {iw }}$ | Initialization pulse width (LOW) | 25 | 10 |  | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {ir }}$ | Initialization recovery time | 45 | 25 |  | 40 | 25 |  | ns |

## Electrical Characteristics Over Operating Conditions



[^20]
## Switching Characteristics Over Operating Conditions and Using Standard Test Load

| SYMBOL | PARAMETER | MILITARY MIN TYP ${ }^{\dagger}$ MAX |  | COMMERCIAL MIN TYP ${ }^{\dagger}$ MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t CLK }}$ | CLK to output | 11 | 25 |  | 11 | 20 | ns |
| ${ }^{1}$ IQ | Initialization to output delay | 23 | 40 |  | 23 | 35 | ns |
| $\mathrm{f}_{\text {MAXD }}$ | Maximum diagnostic clock frequency | $7 \quad 18$ |  | 10 | 18 |  | MHz |
| ${ }^{\text {t }}$ DS | DCLK to SDO delay (MODE = LOW) | 17 | 35 |  | 17 | 30 | ns |
| tss | SDI to SDO delay (MODE $=$ HIGH) | 16 | 30 |  | 16 | 25 | ns |
| $t_{M S}$ | MODE to SDO delay | 14 | 30 |  | 14 | 25 | ns |

$\dagger$ Typicals at 5.0 V VCC and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

## Definition of Waveforms



## Definition of Waveforms



## SYSTEM CONTROL



## SYSTEM OBSERVATION

## Monolithic Memories PROM Programmer Reference Chart

| Source and Location | Data I/O Corp. <br> 10525 Willows Rd. N.E. <br> P.O. Box 97046 <br> Redmond <br> WA 98073-9746 | Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039 | Stag Microsystems Inc. 528-5 Weddell Dr. <br> Sunnyvale <br> CA 94089 | Digelec Inc. <br> 1602 Lawrence Ave. <br> Suite 113 <br> Ocean <br> NJ 07712 | Varix Corp. 1210 E. Campbell Rd. Suite 100 Richardson TX 75081 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Programmer Model(s) | Model 19/29A/29B | Model MPP-80S | Model PPX <br> Model PPZ | UP803 | OMNI |
| MMI Generic Bipolar PROM Personality Module | UniPak Rev 10 UniPak II Rev 07 (Not all PROMs are supported by earlier UniPak revisions) | MOD16 | Zm 2000 | FAM Mod. No. 12 |  |
| Socket Adapter(s) and Device Code |  |  |  |  |  |
| 635080/81 | $\begin{aligned} & \text { F18 P02 } \\ & \text { Model 22A - } \\ & \text { Adapter 351A-064 } \end{aligned}$ | SA3 | AM110-2 <br> Code 21 | DA No. 2 Pinout 1A Switch Pos. 0-7 (63S080) <br> Switch Pos. 0-6 (63S081) | $\begin{aligned} & 63 S 080 \\ & 63 S 081 \end{aligned}$ |
| 63S140/41 | F18 P01 <br> Model 22A - <br> Adapter 351A-064 | SA4-2 | AM130-2 Code 21 | DA No. 1 Pinout 1B Switch Pos. 0-7 (63S140) <br> Switch Pos. 0-6 (63S141) | $\begin{aligned} & 63 S 140 \\ & 63 S 141 \end{aligned}$ |
| 63S240/41 | F18 P03 <br> Model 22A - <br> Adapter 351A-064 | SA4-1 | AM130-3 Code 21 | DA No. 1 Pinout 1D Switch Pos. 2-15 (63S240) <br> Switch Pos. 2-14 (63S241) | $\begin{aligned} & \hline 63 S 240 \\ & 63 S 241 \end{aligned}$ |
| 63S280/81 | $\begin{aligned} & \text { F18 P08 } \\ & \text { Model 22A - } \\ & \text { Adapter 351A-064 } \end{aligned}$ | SA6-1 | Code 21 | $\dagger$ | $\begin{aligned} & 63 \mathrm{~S} 280 \\ & 63 \mathrm{~S} 281 \end{aligned}$ |
| 63S440/41 | F18 P05 <br> Model 22A - <br> Adapter 351A-064 | SA4 | AM140-2 <br> Code 21 | DA No. 3 Pinout 1E Switch Pos. 0-7 (63S440) <br> Switch Pos. 0-6 (63S441) | $\begin{aligned} & 63 S 440 \\ & 63 S 441 \end{aligned}$ |
| 63S480/81 | F18 P09 <br> Model 22A - <br> Adapter 351A-064 | SA6 | Code 21 | $\dagger$ | $\begin{aligned} & 63 S 480 \\ & 63 S 481 \end{aligned}$ |
| 63RA481 | FEC P65 <br> Model 22A - <br> Adapter 351A-074 | SA31-2 | Code 21 | Pinout 1H <br> Switch Pos. 5-14 | 63RA481 |
| 63DA441/42 | FAA PAC <br> Adapter 351A-073 | $\dagger$ | $\dagger$ | $\dagger$ | $\dagger$ |
| 635841 | F18 P06 <br> Model 22A - <br> Adapter 351A-064 | SA4-4 | AM 140-3 Code 21 | DA No. 3 Pinout 1L Switch Pos. 5-15 (63S840) <br> Switch Pos. 5-14 (63S841) | 635841 |
| 63RS881 | F18 P86 <br> Model 22A - <br> Adapter 351A-074 <br> ( 300 mil pkg ) | $\dagger$ | Code 21 | DA No. 64 Switch Pos. 0-12 | 63RS881 |

[^21]
## Monolithic Memories PROM Programmer Reference Chart

| Source and Location | Data I/O Corp. 10525 Willows Rd. N.E. P.O. Box 97046 Redmond WA 98073-9746 | Kontron Electronics Inc. 1230 Charleston Rd. Mountain View CA 94039 | Stag Microsystems Inc. 528-5 Weddell Dr. Sunnyvale CA 94089 | Digelec Inc. <br> 1602 Lawrence Ave. <br> Suite 113 <br> Ocean <br> NJ 07712 | Varix Corp. <br> 1210 E. Campbell Rd. <br> Suite 100 <br> Richardson <br> TX 75081 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Programmer Model(s) | Model 19/29A/29B | Model MPP-80S | Model PPX <br> Model PPZ | UP803 | OMNI |
| MMI Generic <br> Bipolar PROM Personality Module | UniPak Rev 10 UniPak II Rev 07 (Not all PROMs are supported by earlier UniPak revisions) | MOD16 | Zm 2000 | FAM Mod. No. 12 |  |
| Socket Adapter(s) and Device Code |  |  |  |  |  |
| 63DA841 | FAA PAD <br> Adapter 351A-073 | $\dagger$ | $\dagger$ | $\dagger$ | $\dagger$ |
| 6351641 | F18 P53 <br> Model 22A - <br> Adapter 351A-064 | SA20 | AM 120-6 <br> Code 21 | DA No. 70 <br> Switch Pos. 4-12 | 6351641 |
| 6351681 | F18 P21 | SA5-4 | AM 100-5 Code 21 | DA No. 7 | 63 S1681 |
| $\begin{aligned} & \text { 63RA1681 } \\ & \text { 63RS1681 } \end{aligned}$ | F18 PA3 | $\dagger$ | Code 21 | DA No. 64 | 63RA1681 63RS1681 |
| 63D1641 | FB2 P80 Adapter 351A-073 | $\dagger$ | Code 21 | $\dagger$ | 63D1641 |
| 63DA1643 | FAA P87 Adapter 351A-073 | $\dagger$ | $\dagger$ | $\dagger$ | $\dagger$ |
| 6353281 | F18 P63 | $\dagger$ | Code 21 | DA No. 64 Pinout 47 Switch Pos. 0-4 | 6353281 |

$\dagger$ Contact manufacturer for availability and programming information.


## Table of Contents

## PLE DEVICES

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PLE to PROM Cross Reference


[^22]
## Programmable Logic Element PLE ${ }^{\text {TM }}$ Circuit Family

## Features/Benefits

- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- Expedites and simplifies prototyping and board layout
- Saves space with 0.3-inch SKINNYDIP® packages (except PLE 12P8)
- Programmed on standard PROM programmers
- Test and simulation made simple with PLEASM ${ }^{\text {TM }}$ software
- Low-current PNP inputs
- Three-state outputs
- Reliable TiW fuses guarantee $\mathbf{> 9 8 \%}$ programming yield


## Ordering Information



PLE = Programmable Logic Element
NUMBER OF INPUTS -
OUTPUT TYPE
$\mathbf{P}=$ Non Registered
R = Registered
RA $=$ Registered
Asynchronous Enable
RS = Registered Synchronous Enable

NUMBER OF OUTPUTS $\qquad$
PROCESSING
STD = Standard
XXXX $=$ Mil-Std-883, Class B
PACKAGE TYPE
$\mathrm{N}=$ Plastic DIP
NS = Plastic SKINNYDIP
J = Ceramic DIP
JS = Ceramic SKINNYDIP
F = Ceramic Solder Seal Flat Pack
L = Leadless Chip Carrier
NL = Plastic Leaded Chip
Carrier
W = Cerpack
TEMPERATURE CODE
$\mathrm{C}=0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$
$\mathrm{M}=-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$

Blank = Standard
A = Enhanced

## PLE Circuit Selection Guide

| PART NUMBER | INPUTS | OUTPUTS | PRODUCT TERMS | OUTPUT REGISTERS | $\begin{aligned} & \text { tpD (ns) } \\ & \text { MAX }^{*} \end{aligned}$ |
| :---: | :---: | :---: | :---: | :---: | :---: |
| PLE5P8 | 5 | 8 | 32 |  | 25 |
| PLE5P8A | 5 | 8 | 32 |  | 15 |
| PLE8P4 | 8 | 4 | 256 |  | 30 |
| PLE8P8 | 8 | 8 | 256 |  | 28 |
| PLE9P4 | 9 | 4 | 512 |  | 35 |
| PLE9P8 | 9 | 8 | 512 |  | 30 |
| PLE10P4 | 10 | 4 | 1024 |  | 35 |
| PLE10P8 | 10 | 8 | 1024 |  | 30 |
| PLE11P4 | 11 | 4 | 2048 |  | 35 |
| PLE11P8 | 11 | 8 | 2048 |  | 35 |
| PLE12P4 | 12 | 4 | 4096 |  | 35 |
| PLE12P8 | 12 | 8 | 4096 |  | 35 |
| PLE9R8 | 9 | 8 | 512 | 8 | 15 |
| PLE10R8 | 10 | 8 | 1024 | -8 | 15 |
| PLE11RA8 | 11 | 8 | 2048 | 8 | 15 |
| PLE11RS8 | 11 | 8 | 2048 | 8 | 15 |

* Clock to output time for registered outputs.

Note: Commercial limits specified.

## PLE Family

## PLE Means Programmable Logic Element

Joining the world of IdeaLogic ${ }^{\text {TM }}$ is a new generation of Highspeed PROMs which the designer can use as Programmable Logic Elements. The combination of PLE circuits as logic elements with PAL devices can greatly enhance system speed while providing almost unlimited design freedom.
Basically, PLE circuits are ideal when a large number of product terms is required. On the other hand, a PAL device is best suited for situations when many inputs are needed.
The PLE circuit transfer function is the familiar OR of products, Like the PAL device, the PAE circuit has a single array of fusible links. Unlike the PAL device, the PLE circuits have a programmable OR array driven by a fixed AND array (the PAL device is a programmed AND array driving a fixed OR array).

## PRODUCT TERM AND INPUT LINES

|  | PLE | PAL |
| :--- | :---: | :---: |
| Product Terms | 32 to 4096 | 1 to 16 |
| Input Lines | 5 to 12 | 6 to 64 |

The PLE family features common electrical parameters and programming algorithm, low-current PNP inputs, full Schottky clamping and three-state outputs.
The entire PLE family is programmed on conventional PROM programmers with the appropriate personality cards and socket adapters.

## Registered PLE Circuits

The registered PLE circuits have on-chip " $D$ " type registers, versatile output enable control through synchronous and asynchronous enable inputs, and flexible start-up sequencing through programmable initialization.
Data is transferred into the output registers on the rising edge of the clock. Provided that the asynchronous ( $\overline{\mathrm{E}}$ ) and synchronous (ES) enables are Low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Data control is made flexible with synchronous and asynchronous enable inputs. Outputs may be set to the high-impedance state at any time by setting $\bar{E}$ to a High or if $\overline{E S}$ is High when the rising clock edge occurs. When $\mathrm{V}_{\mathrm{CC}}$ power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high-impedance state.
A flexible initialization feature allows start-up and time-out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE (IS) pin Low, one of the 16 initialize words, addressed through pins $5,6,7$ and 8 will be set in the output registers independent of all other input pins. The unprogrammed state of $\overline{\mathrm{S}}$ words are Low, presenting a CLEAR with $\overline{\mathrm{I}}$ pin Low. With all $\overline{\mathrm{I}}$ column words (A3-AO) programmed to the same pattern, the $\overline{\mathrm{S}}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{\mathrm{S}}$ words programmed High a PRESET function is performed.

The PLE9R8 has asynchronous PRESET and CLEAR functions. With the chip enabled, a Low on the $\overline{P R}$ input will cause all outputs to be set to the High state. When the CLR input is set Low the output registers are reset and all outputs will be set to the Low state. The $\overline{P R}$ and $\overline{C L R}$ functions are common to all output registers and independent of all other data input states.

|  | AND | OR | OUTPUT OPTIONS |
| :---: | :---: | :---: | :---: |
| PLE | Fixed | Prog | TS, Registered Outputs, <br> Fusible Polarity |
| FPLA | Prog | Prog | TS, OC, Fusible Polarity |
| FPGA | Prog | Prog | TS, OC, Fusible Polarity |
| FPLS | Prog | Prog | TS, Registered Feedback I/O |
| PAL | Prog | Fixed | TS, Registered Feedback I/O <br> Fusible Polarity |

## PLEASM ${ }^{\text {w }}$ Software

## Software that makes programmable logic easy.

Monolithic Memories has developed a software tool to assist in designing and programming PROMs as PLE circuits. This package called "PLEASM" (PLE Assembler) is available for several computers including the VAX/VMS and IBM PC/DOS. PLEASM

PLE (PROM)

software converts design equation (Boolean and arithmetic) into truth tables and formats compatible with PROM programmers. A simulator is also provided to test a design using a Function Table before actually programming the PLE circuit.
PLEASM software may be requested through the Monolithic Memories IdeaLogic Exchange.


Note: $-=$ Hardwired connection
$X=$ Programmable fuse with a diode

## Logic Symbols



PLE10P8



## Logic Symbols




* Initialize Pin


## Absolute Maximum Ratings

Operating
-0.5 V to 7 V
Programming
Supply voltage $\mathrm{V}_{\mathrm{CC}}$.
Input voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -1.5 V to 7 V $\qquad$
Off-state output voltage . ........................................................................... . 0.5 V to 5.5 V
Storage temperature
$-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| S | PARAMETER | COMMERCIAL |  |  | MILITARY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.75 | 5 | 5.25 | 4.5 | 5 | 5.5 | $\checkmark$ |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | 0 | 25 | 75 | -55 | 25 | 125 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\text {CC }}=$ MIN | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  |  | -0.25 | mA |
| $\mathrm{I}_{\mathrm{IH}}$ | High-level input current | $\mathrm{V}_{\text {CC }}=\mathrm{MAX}$ | $\mathrm{V}_{1}=\mathrm{V}_{\mathrm{CC}}$ |  |  |  | 40 | $\mu \mathrm{A}$ |
|  |  |  |  | Com |  |  | 0.45 |  |
| O | Low-level output voltage | ${ }^{\text {CC }}$ | OL | Mil |  |  | 0.5 | V |
|  | High-level output voltage |  | Com ${ }^{\circ} \mathrm{OH}=-$ |  | 2.4 |  |  | V |
|  | High-level output voltage |  | Mil $\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}$ |  | 2.4 |  |  | $\checkmark$ |
| ${ }^{1} \mathrm{OZL}$ | Off-state output current | $V_{C O}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -40 | A |
| l OZH | Ofr-state output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 40 | $\mu \mathrm{A}$ |
| IOS | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
|  |  |  | 5P8 |  |  | 90 | 125 |  |
|  | 4 a |  | 5P8A |  |  | 90 | 125 |  |
|  |  |  | 8P4 |  |  | 80 | 130 |  |
|  |  |  | 8P8 |  |  | 90 | 140 |  |
|  |  |  | 9P4 |  |  | 80 | 130 |  |
|  |  | $V_{C C}=M A X$ All inputs | 9P8 |  |  | 104 | 155 |  |
|  |  | grounded; | 10P4 |  |  | 95 | 140 |  |
| ${ }^{1} \mathrm{CC}$ | Supply current |  | 10P8 |  |  | 92 | 160 | mA |
|  |  |  | 11P4 |  |  | 110 | 150 |  |
|  |  |  | 11 P 8 |  |  | 135 | 185 |  |
|  |  |  | 12 P 4 |  |  | 130 | 175 |  |
|  |  |  | 12P8 |  |  | 150 | 190 |  |
|  |  |  | $9 \mathrm{R8}$ |  |  | 130 | 180 |  |
|  |  | $V_{C C}=M A X$ | 10R8 |  |  | 130 | 180 |  |
|  |  | all outputs open | 11RA8 |  |  | 140 | 185 |  |
|  |  |  | 11RS8 |  |  | 140 | 185 |  |

[^23]
## Switching Characteristics Over Commercial Operating Conditions

| DEVICE TYPE | $t_{P D}$ ( ns ) PROPAGATION DELAY MAX | ${ }^{\text {t }}$ PZX AND ${ }^{\text {tpXZ }}$ (ns) INPUT TO OUTPUT ENABLE/DISABLE TIME MAX |
| :---: | :---: | :---: |
| 5P8AC | 15 | 20 |
| 5P8C | 25 | 20 |
| 8P4C | 30 | 20 |
| 8P8C | 28 | 25 |
| 9P4C | 35 | 20 |
| $9 P 8 \mathrm{C}$ | 30 | 25 |
| 10P4C | 35 | 25 |
| 10P8C | 30 | 25 |
| 11P4C | 35 | 25 |
| 11P8C | 35 | 25 |
| 12P4C | 35 | 25 |
| 12P8C | 35 | 30 |

## Switching Characteristics Over Military Operating Conditions

| DEVICE TYPE | $t^{\mathrm{PD}}$ ( ns ) PROPAGATION DELAY MAX | $t_{\text {tPZX AND tpXZ (ns) }}$ INPUT TO OUTPUT ENABLE/DISABLE TIME MAX |
| :---: | :---: | :---: |
| 5P8M | 35 | 30 |
| 8P4M | 40 | 30 |
| 8P8M | 40 | 30 |
| 9P4M | 45 | 30 |
| 9P8M | 40 | 30 |
| 10P4M | 50 | 30 |
| 10P8M | 45 | 30 |
| 11P4M | 50 | 30 |
| 11P8M | 50 | 30 |
| 12P4M | 50 | 30 |
| 12P8M | 40 | 35 |

## Operating Conditions

| SYMBOL | PARAMETER | COMMERCIAL |  |  | MILITARY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP* | MAX | MIN | TYP* | MAX |  |
| ${ }_{\text {t }}$ w | Width of clock (High or Low) | 20 | 10 |  | 20 | 10 |  | ns |
| $t_{\text {tprw }}$ | Width of preset or clear (Low) to Output (High or Low) | 20 | 10 |  | 20 | 10 |  | ns |
| ${ }^{\text {clirw }}$ |  |  |  |  |  |  |  |  |
| tprr | Recovery from preset or clear (Low) to clock High | 20 | 11 |  | 25 | 11 |  | ns |
| ${ }^{\text {c }}$ crir |  |  |  |  |  |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time from input to clock | 30 | 22 |  | 35 | 22 |  | ns |
| $\left.\mathrm{t}_{\mathrm{s}} \overline{(\mathrm{ES}}\right)$ | Setup time from $\overline{\mathrm{ES}}$ to clock | 10 | 7 |  | 15 | 7 |  | ns |
| $t_{\text {h }}$ | Hold time from input to clock | 0 | -5 |  | 0 | -5 |  | ns |
| $t_{h} \overline{(E S)}$ | Hold time from ES to clock | 5 | -3 |  | 5 | -3 |  | ns |

## Switching Characteristics Over Operating Conditions and using Standard Test Load

| SYMBOL | PARAMETER | COMMERCIAL <br> MIN TYP* MAX |  | MILITARY |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t CLK }}$ | Clock to output delay | 11 | 15 | 11 | 20 | ns |
| ${ }^{\text {t }}$ PR | Preset to output delay | 15 | 25 | 15 | 25 | ns |
| ${ }^{t}$ CLR | Clear to output delay | 18 | 25 | 18 | 35 | ns |
| ${ }^{\text {tPZX }}$ (CLK) | Clock to output enable time | 14. | 25 | 14 | 30 | ns |
| $t_{\text {PXZ }}$ (CLK) | Clock to output disable time | 14 | 25 | 14 | 30 | ns |
| ${ }^{\text {tPZ }}$ PX | Input to output enable time | 10 | 20 | 10 | 25 | ns |
| tPXZ | Input to output disable time | 10 | 20 | 10 | 25 | ns |

[^24]
## Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V .
2. Input rise and fall times $2-5$ ns from 0.8 V to 2.0 V .
3. Input access measured at the 1.5 V level.
4. Switch $S_{1}$ is closed. $C_{L}=30 \mathrm{pF}$ and outputs measured at 1.5 V level for all tests except $t_{P X Z}$ and $t_{P Z X}$.
5. tPZX and $t_{P Z X(C L K)}$ are measured at the 1.5 V output level with $C_{L}=30 \mathrm{pF} . S_{1}$ is open for high impedance to " 1 " test and closed for high impedance to " 0 " test.
$t_{P X Z}$ and $t_{P X Z(C L K)}$ are tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}^{-}} 0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

Operating Conditions

| SYMBOL | PARAMETER | COMMERCIAL |  | MILITARY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP* MAX | MIN | TYP* | MAX |  |
| ${ }^{\text {tw }}$ | Width of clock (High or Low) | 20 | 10 | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Setup time from input to clock (10R8) | 30 | 25 | 40 | 25 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Setup time from input to clock (11RA8, 11RS8) | 35 | 28 | 40 | 28 |  | ns |
| $\mathrm{t}_{\mathrm{s}}(\overline{\mathrm{ES}})$ | Setup time from $\overline{E S}$ to clock (except 11RA8) | 15 | 7 | 15 | 8 |  | ns |
| $t_{s}(\bar{S})$ | Setup time from $\overline{\text { S }}$ to clock | 25 | 20 | 30 | 20 |  | ns |
| th | Hold time input to clock | 0 | -5 | 0 | -5 |  | ns |
| $t_{h}(\overline{E S})$ | Hold time (ES) (except 11RA8) | 5 | -3 | 5 | -3 |  | ns |
| $t_{h}(\overline{\text { I }}$ ) | Hold time ( $\overline{\mathrm{IS}}$ ) | 0 | -5 | 0 | -5 |  | ns |

## Switching Characteristics Over Operating Conditions and using Standard Test Load

| SYMBOL | PARAMETER | COMMERCIAL MIN TYP* MAX |  | MILITARY |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{t} \mathrm{CLK}$ | Clock to output delay | 10 | 15 | 10 | 20 | ns |
| $t_{\text {PZX }}$ (CLK) | Clock to output enable time (except 11RA8) | 17 | 25 | 18 | 30 | ns |
| $t_{\text {t X } ~}^{\text {( }}$ (CLK) | Clock to output disable time (except 11RA8) | 17 | 25 | 18 | 30 | ns |
| $t_{P Z X}$ | Input to output enable time (except 11RS8) | 17 | 25 | 17 | 30 | ns |
| ${ }^{\text {t P X }}$ \% | Input to output disable time (except 11RS8) | 17 | 25 | 17 | 30 | ns |

${ }^{*}$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

## Definition of Waveforms



NOTES: 1. Input pulse amplitude 0 V to 3.0 V .
2. Input rise and fall times $2-5 \mathrm{~ns}$ from 0.8 V to 2.0 V .
3. Input access measured at the 1.5 V level.
4. Switch $\mathrm{S}_{1}$ is closed. $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ and outputs measured at 1.5 V level for all tests except $\mathrm{t}_{\mathrm{P}} \mathrm{ZX}$ and tpXZ
5. $\operatorname{tPZX}$ and $\mathrm{tPZX}^{\prime} C L K$ ) are measured at the 1.5 V output level with $C_{L}=30 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test and closed for high impedance to " 0 " test.
$t_{P X Z}$ and $t_{P X Z(C L K)}$ are tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test. measured at $V_{\mathrm{OH}}-05 \mathrm{~V}$ output level:
$\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

Switching Test Load


## Definition of Waveforms



NOTES: Apply to electrical and switching characteristics.
Typical at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.
Measurements are absolute voltages with respect to the ground pin on the device and includes all overshoots due to system and/or tester noise. In all PLE devices unused inputs must be tied to either ground or $V_{C C}$. The series resistor required for unused inputs on standard TTL is NOT required for PLE devices, thus using less parts.

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

For commercial operating range $R_{1}=200 \Omega, R_{2}=390 \Omega$. For military operating range $R_{1}=300 \Omega, R_{2}=600 \Omega$.

1. Input pulse amplitude 0 V to 3.0 V .
2. Input rise and fall times $2-5$ ns from 0.8 to 2.0 V .
3. Input access measured at the 1.5 V level.
4. Data delay is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ and measured at 1.5 V output level.
5. tpZX is measured at the 1.5 V ouput level with $C_{L}=30 \mathrm{pF} \mathrm{S} \mathrm{S}_{1}$ is open for high-impedance to " 1 " test and closed for high-impedance to " 0 " test. ${ }^{\text {t PX Z }}$ is measured $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high-impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high-impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Block Diagrams

PLE5P8/A


## PLE8P8



PLE8P4


PLE9P4


## Block Diagrams

PLE9P8


## PLE10P8



PLE10P4


PLE11P4


## Block Diagrams

## PLE11P8



PLE12P4


## PLE12P8



Block Diagrams

PLE9R8


PLE11RA8


PLE10R8


PLE11RS8


[^25]
## Monolithic Memories PLE Programmer Reference Chart

| SOURCE AND <br> LOCATION | Data I/O Corp. <br> 10525 Willows Rd. N.E. <br> P.O. Box 97046 <br> Redmond <br> WA 98073-9746 | Kontron Electronics Inc. 1230 Charleston Rd. <br> Mountain View CA 94039-7230 | Stag Microsystems Inc. 528-5 Weddell Dr. <br> Sunnyvale CA 94089 | Digelec Inc. <br> 1602 Lawrence Ave. <br> Suite 113 <br> Ocean <br> NJ 07712 | Varix Corp. <br> 1210 E. Campbell Rd. <br> Suite 100 <br> Richardson <br> TX 75081 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| Programmer Model(s) | Model 19/29A/29B Model 22 | Model MMP-80S | Model PPX <br> Model PPZ | UP803 | OMNI |
| MMI Generic Bipolar PLE Personality Module | UniPak Rev 10 UniPak II Rev 07 (Not all PLE devices are supported by earlier UniPak revisions) | MOD16 | Zm 2000 | FAM Mod. No. 12 |  |
| Socket Adapter(s) and Device Code |  |  |  |  |  |
| PLE5P8/ PLE5P8A | F18 P02 <br> Model 22A- <br> Adapter 351A-064 | SA3 | AM110-2 <br> Code 21 | DA No. 2 Pinout 1A Switch Pos. 0-6 | $63 S 081$ |
| PLE8P4 | F18 P01 <br> Model 22A- <br> Adapter 351A-064 | SA4-2 | AM130-2 <br> Code 21 | DA No. 1 Pinout 1B Switch Pos. 0-6 | 63 S141 |
| PLE9P4 | F18 P03 <br> Model 22A- <br> Adapter 351A-064 | SA4-1 | AM130-3 <br> Code 21 | DA No. 1 Pinout $1 D$ Switch Pos. 2-14 | 63 S 241 |
| PLE8P8 | F18 P08 <br> Model 22A- <br> Adapter 351A-064 | SA6-1 | Code 21 | $\dagger$ | 635281 |
| PLE10P4 | F18 P05 <br> Model 22A- <br> Adapter 351A-064 | SA4 | AM140-2 <br> Code 21 | DA No. 3 Pinout 1E Switch Pos. 0-6 | $63 S 441$ |
| PLE9P8 | F18 P08 <br> Model 22A- <br> Adapter 351A-064 | SA6 | Code 21 | $\dagger$ | $63 S 481$ |
| PLE9R8 | FEC P65 <br> Model 22A- <br> Adapter 351A-074 | SA31-2 | Code 21 | Pinout 1H <br> Switch Pos. 5-14 | 63RA481 |
| PLE11P4 | F18 P06 <br> Model 22A- <br> Adapter 351A-064 | SA4-4 | AM140-3 <br> Code 21 | DA No. 3 Pinout 1L Switch 5-14 | 635841 |
| PLE10R8 | F18 P86 <br> Model 22A- <br> Adapter 351A-074 <br> ( 300 mil pkg ) | $\dagger$ | Code 21 | DA No. $64{ }^{\dagger}$ Switch Pos. 0-12 | 63RS881 |
| PLE12P4 | F18 P53 <br> Model 22A- <br> Adapter 351A-064 | SA20 | AM120-6 <br> Code 21 | DA No. 70 Switch Pos. 4-12 | 6351641 |
| PLE11RA8 PLE11RS8 | F18 PA3 | $\dagger$ | Code 21 | DA No. 64 | 63RA1681 63RS1681 |
| PLE11P8 | F18P21 | SA5-4 | AM100-5 <br> Code 21 | DA No. 7 | 6351681 |
| PLE12P8 | F18P63 | $\dagger$ | Code 21 | DA No. 64 Pinout 47 Switch Pos. 0-4 | 6353281 |

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## The PAL® Device Concept

Monolithic Memories'family of PAL devices gives designers a powerful tool with unique capabilities for use in new and existing logic designs. The PAL device saves time and money by solving many of the system partitioning and interface problems brought about by increases in semiconductor device technology.

Rapid advances in large scale integration technology have led to larger and larger standard logic functions; single I.C.s now perform functions that formerly required complete circuit cards. While LSI offers many advantages, advances have been made at the expense of device flexibility. Most LSI devices still require large numbers of SSI/MSI devices for interfacing with user systems. Designers are still forced to turn to random logic for many applications.

The designer is confronted with another problem when a product is designed. Often the function is well defined and could derive significant benefits from fabrication as an integrated circuit. However, the design cycle for a custom circuit is long and the costs can be very high. This makes the risk significant enough to deter most users. The technology to support maximum flexibility combined with fast turnaround on custom logic has simply not been available. Monolithic Memories offers the programmable solution.

The PAL device family offers a fresh approach to using fuse programmable logic. PAL circuits are a conceptually unified group of devices which combine programmable flexibility with high speed and an extensive selection of interface options. PAL devices can lower inventory, cut design cycles and provide high complexity with maximum flexibility. These features, combined with lower package count and high reliability, truly make the PAL device a circuit designer's best friend.

## The PAL Device-Teaching Old PROMs New Tricks



Monolithic Memories developed the modern PROM and introduced many of the architectures and techniques now regarded as industry standards. As the world's largest PROM manufacturer, Monolithic Memories has the proven technology and high volume production capability required to manufacture and support the PAL device.
The PAL device is an extension of the fusible link technology pioneered by Monolithic Memories for use in bipolar PROMs. The fusible link PROM first gave the digital systems designer the power to "write on silicon". In a few seconds he was able to transform a blank PROM from a general purpose device into one containing a custom algorithm, microprogram, or Boolean transfer function. This opened up new horizons for the use of PROMs in computer control stores, character generators, data storage tables and many other applications. The wide acceptance of this technology is clearly demonstrated by today's multi-million dollar PROM market.
The key to the PROM's success is that it allows the designer to customize the chip quickly and easily to fit his unique requirements. The PAL device extends this programmable flexibility by utilizing proven fusible link technology to implement logic functions. By using PAL circuits the designer can quickly and effectively implement custom logic varying in complexity from random gates to complex arithmetic functions.

## ANDs and ORs

The PAL device implements the familiar sum-of-products logic by using a programmable AND array whose output terms feed a fixed OR array. Since the sum-of-products form can express any Boolean transfer function, the PAL circuit uses are only limited by the number of terms available in the AND - OR arrays. PAL devices come in different sizes to allow for effective logic optimization.

Figure 1 shows the basic PAL device structure for a two-input, one-output logic segment. The general logic equation for this segment is:

$$
\begin{aligned}
\text { Output }= & \left(l_{1}+\overline{f_{1}}\right)\left(\overline{I_{1}}+\overline{f_{2}}\right)\left(l_{2}+\overline{f_{3}}\right)\left(\overline{l_{2}}+\overline{f_{4}}\right)+ \\
& \left(l_{1}+\overline{f_{5}}\right)\left(\overline{l_{1}}+\overline{f_{6}}\right)\left(l_{2}+\overline{f_{7}}\right)\left(\overline{l_{2}}+\overline{f_{8}}\right)
\end{aligned}
$$

where the "f" terms represent the state of the fusible links in the PAL device AND array. An unblown link represents a logic 1. Thus:

$$
\text { fuse blown, } f=0
$$

An unprogrammed PAL device has all fuses intact.


Figure 1

## PAL Device Notation

Logic equations, while convenient for small functions, rapidly become cumbersome in large systems. To reduce possible confusion, complex logic networks are generally defined by logic diagrams and truth tables. Figure 2 shows the logic convention adopted to keep PAL device logic easy to understand and use, in the figure, an " $x$ " represents an intact fuse used to perform the logic AND function. (Note: the input terms on the common line with the $x$ 's are not connected together.) The logic symbology shown in Figure 2 has been informally adopted by integrated circuit manufacturers because it clearly establishes a one-toone correspondence between the chip layout and the logic diagram. It also allows the logic diagram and truth table to be combined into a compact and easy to read form, thereby serving as a convenient shorthand for PAL circuits. The two-input, oneoutput example from Figure 1, redrawn using the new logic convention, is shown in Figure 3.


Figure 2


Figure 3
As a simple PAL device example, consider the implementation of the transfer function:

$$
\text { Output }=1_{1} \bar{I}_{2}+\overline{1}_{1} 1_{2}
$$

The normal combinatorial logic diagram for this function is shown in Figure 4, with the PAL device logic equivalent shown in Figure 5.


Figure 4


Figure 5

Using this logic convention it is now possible to compare the PAL device structure to the structure of the more familiar PROM and PLA. The basic logic structure of a PROM consists of a fixed AND array whose outputs feed a programmable OR array (Figure 6). PROMs are low-cost, easy to program, and available in a variety of sizes and organizations. They are most commonly

PROM 16 Words $\times 4$ Bits


Figure 6
used to store computer programs and data. In these applications the fixed input is a computer memory address; the output is the contents of that memory location.

The basic logic structure of the PLA consists of a programmable AND array whose outputs feed a programmable OR array (Figure 7). Since the designer has complete control over all inputs and outputs, the PLA provides the ultimate flexibility for implementing logic functions. They are used in a wide variety of applications. However, this generality can make PLAs expensive, quite formidable to understand, and costly to program.

The basic logic structure of the PAL device, as mentioned earlier, consists of a programmable AND array whose outputs feed a fixed OR array (Figure 8). The PAL device combines much of the flexibility of the PLA with the low cost and easy programmability of the PROM. Table 1 summarizes the characteristics of the PROM, PLA, and PAL device logic families.

FPLA
4 In• 4 Out•16 Products


Figure 7

PAL Device 4 In•4 Out-16 Products


Figure 8

|  | AND | OR | OUTPUT OPTIONS |
| :--- | :--- | :--- | :--- |
| PROM | Fixed | Prog | TS,OC |
| FPLA | Prog | Prog | TS, OC, Prog. Polarity |
| FPGA | Prog | None | TS, OC, Prog. Polarity |
| FPLS | Prog | Prog | TS, Registered Feedback, I/O |
| PAL Device | Prog | Fixed | TS, Registered Feedback, I/O <br> Prog. Polarity |

## PAL Device Circuits For Every Task

The members of the PAL device family and their characteristics are summarized in the PAL device menu. They are designed to cover the spectrum of logic functions at reduced cost and lower package count. This allows the designer to select the PAL device that best fits his application. PAL device units come in the following basic configurations:

## Logic Arrays

PAL device logic arrays are available in sizes from $6 \times 16$ ( 6 input terms, 16 output terms) to $64 \times 32$, with both active high and active low output configurations available (ref. PAL device menu). This wide variety of input/output formats allows the PAL device to replace many different sized blocks of combinatorial logic with single packages.


Figure 9

## Programmable I/O

A feature of the high-end members of the PAL device family is programmable input/output. This allows the product terms to directly control the outputs of the PAL device (Figure 10). One product term is used to enable the three-state buffer, which in turn gates the summation term to the output pin. The output is
also fed back into the PAL device array as an input. Thus the PAL device drives the I/O pin when the three-state gate is enabled; the I/O pin is an input to the PAL device array when the three-state gate is disabled. This feature can be used to allocate available pins for $1 / O$ functions or to provide bi-directional output pins for operations such as shifting and rotating serial data.

INPUTS, FEEDBACK AND I/O


Figure 10

## Registered Outputs with Feedback

Another feature of the high end members of the PAL device family is registered data outputs with registered feedback. Each product term is stored into a D-type output flip-flop on the rising edge of the system clock (Figure 11). The Q output of the flip-flop can then be gated to the output pin by enabling the active low three-state buffer.

In addition to being available for transmission, the Q output is fed back into the PAL device array as an input term. This feedback allows the PAL device to "remember" the previous state, and it can alter its function based upon that state. This allows the designer to configure the PAL device as a state sequencer which can be programmed to execute such elementary functions as count up, count down, skip, shift, and branch. These functions can be executed by the registered PAL device at rates of up to 40 MHz .


Figure 11
of the features of the Registered PAL devices are included in the XOR PAL unit. The XOR function provides an easy implementation of the HOLD operation used in counters and other state sequencers.

## XOR PAL Devices

These PAL devices feature an exclusive-OR (XOR) function. The sum of products is segmented into two sums which are then exclusive ORed at the input of the D-type flip-flop (Figure 12). All


Figure 12

## Arithmetic Gated Feedback

The arithmetic functions (add, subtract, greater than, and less than) are implemented by addition of gated feedback to the features of the XOR PAL device. The XOR at the input of the D-type flip-flop allows carrys from previous operations to be XORed with two variable sums generated by the PAL device array. The flip-flop Q output is fed back to be gated with input
terms A (Figure 13). This gated feedback provides any one of the sixteen possible Boolean combinations which are mapped in the Karnaugh map (Figure 15). Figure 14 shows how the PAL device array can be programmed to perform these sixteen operations. These features provide for versatile operations on two variables and facilitate the parallel generation of carrys necessary for fast arithmetic operations.


Figure 13



Figure 15

Figure 14

## PAL Device Introduction

## Programmable Output Polarity

The outputs can be programmed either active-low or activehigh. This is represented by the exclusive-or gates shown in Figure 13, PAL20RA10 Logic Diagram. When the output polarity fuse is blown, the lower input to the exclusive-or gate is high, so the output is active-high. Similarly, when the output polarity fuse is intact, the output is active-low. The programmable output polarity feature allows the user a higher degree of flexibility when writing equations.

## Programmable Clock

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others. (See Figure 16)

## Programmable Set and Reset

Two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1. If the reset product line is high, the register output becomes a logic 0 . The operation of the programmable set and reset overrides the clock. (See Figure 16)

## Individually Programmable Register Bypass

If both the set and reset product lines are high, the sum-ofproducts bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode. (See Figure 16)


Figure 16

## Product Term Sharing

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair, each product term can be used by either output; but, since product term sharing is
exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL assemblers configure product terms automatically.


Figure 17

## PAL Device Programming

PAL devices can be programmed in most standard PROM programmers with the addition of a PAL device personality card. For details on programming equipment, see the PAL Device Programmer Reference Guide in this databook.

## PALASM (PAL Device Assembler)

PALASM is the software used to define, simulate, build, and test PAL device units. PALASM accepts the PAL device Design Specification as an input file. It verifies the design against an optional function table and generates the fuse plot which is used to program the PAL devices. PALASM is available upon request for many computers.

## HAL (Hard Array Logic) Device

The HAL device family is the mask programmed version of a PAL device. The HAL device is to a PAL device just as a ROM is to a PROM. A standard wafer is fabricated as far as the metal mask. Then a custom metal mask is used to fabricate aluminum
links for a HAL device instead of the programmable TiW fuses used in a PAL device.

## PAL Device Technology

PAL circuits are manufactured using the proven TTL Schottky bipolar TiW fuse process to make fusible-link PROMs. An NPN emitter follower array forms the programmable AND array. PNP inputs provide high impedance inputs ( 0.25 mA max) to the array. All outputs are standard TTL drivers with internal active pull-up transistors.

## PAL Device Data Security

The circuitry used for programming and logic verification can be used at any time to determine the logic pattern stored in the PAL device array. For security, the PAL device has a "last fuse" which can be blown to disable the verification logic. This provides a significant deterrent to potential copiers, and it can be used to protect proprietary designs.

[^27]
## PAL Device Part Numbers

The PAL device part number is unique in that the part number code also defines the part's logic operation. The PAL device numbering system is shown in Figure 17. For example, a PAL 14 L4CN would be a 14 -input term, 4 -output term, active-low PAL device with a commercial temperature range packaged in a 20-pin plastic DIP.
The electronic dice game is simply constructed using a free running oscillator whose output is used to drive two asyn-
chronous modulo six counters. When the user "rolls" the dice (presses a button), the current state of the counters is decoded and latched into a display resembling the pattern seen on an ordinary pair of dice.
A conventional logic diagram for the dice game is shown in Figure 16. It is implemented using standard TTL, SSI and MSI parts, with a total I.C. count of eight: six quad gate packages and two quad D-latches. Looks like a nice clean logic design, right? Wrong!!


Figure 16


## PAL Device Logic Symbols

The logic symbols for each of the individual PAL devices gives a concise functional description of the PAL device logic function. This symbol makes a convenient reference when selecting the PAL device that best fits a specific application. Figure 18 shows the logic symbol for a PAL10H8 array.


Figure 18

## A PAL Device Example

As an example of how the PAL device enables the designer to reduce costs and simplify logic design, consider the design of a simple, high-volume consumer product: an electronic dice game. This type of product will be produced in extremely high volume, so it is essential that every possible production cost be minimized.

## PAL Device Goes to the Casino

A brief examination of Figure 16 reveals two basic facts: first, the circuit contains mostly simple, combinatorial logic, and second, it uses a clocked state transition sequence. Remembering that the PAL device family contains ample provision for these features, the PAL device catalog is consulted. The PAL16R8 has all the required functions, and the entire logic content of the circuit can be programmed into a single PAL device shown in Figure 19.
In this example, the PAL device effected an eight-to-one package count reduction and a significant cost savings. This is typical of the power and cost-effective performance that the PAL device family brings to logic design.


Figure 19

## Advantages of Using PAL Devices



The PAL device has a unique place in the world of logic design. Not only does it offer many advantages over conventional logic, it also provides many features not found anywhere else. Among the benefits of the PAL device family:

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by at least 4 to 1.
- Expedites and simplifies prototyping and board layout.
- Saves space with 20-pin and 24-pin SKINNYDIP packages, and surface-mount PLCC packages.
- High speed: 15 ns maximum propagation delay, on B series.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Special feature eliminates possibility of copying by competitors.
All of these features combine together to lower product development costs and increase product cost effectiveness. The bottom line is that PAL devices save money.


## Direct Logic Replacement



In both new and existing designs, the PAL device can be used to replace various logic functions. This allows the designer to optimize a circuit in many ways never before possible. The PAL device is particularly effective when used to provide interfaces required by many LSI functions. The combination of PAL device flexibility and LSI function density makes a powerful team.

## Design Flexibility

The PAL device offers the systems logic designer a whole new world of options. Until now, the decision on logic system implementation was usually between SSI/MSI logic functions on one hand and microprocessors on the other. In many cases the function required is too awkward to implement the first way and too simple to justify the second. Now the PAL device offers the designer high functional density, high speed, and low cost. Even better, PAL devices come in a variety of sizes and functions, thereby further increasing the designer's options.

## Space Efficiency



By allowing designers to replace many simple logic functions with single packages, the PAL device allows more compact P.C. board layouts. The PAL device space-saving 20-pin and 24-pin SKINNYDIP packages help to reduce board area further while simplifying board layout and fabrication. this means that many multi-card systems can now be reduced to one or two cards, and that can make the difference between a profitable success or an expensive disaster.

## Smaller Inventory

The PAL device family can be used to replace up to $90 \%$ of the conventional TTL family. This considerably lowers both shelving and inventory cataloging requirements. In addition, small custom modifications to the standard functions are easy for PAL device users, but not so easy for standard TTL users.


## High Speed



The PAL device family runs faster than or equal to the best of bipolar logic circuits. This makes the PAL device the ideal choice for most logical operations or control sequence which requires a medium complexity and high speed. Also, in many microcomputer systems, the PAL device can be used to handle high-speed data interfaces that are not feasible for the microprocessor alone. This can be used to significantly extend the capabilities of the low-cost, low-speed NMOS microprocessors into areas formerly requiring high-cost bipolar microprocessors.

## Easy Programming

The members of the PAL device family can be quickly and easily programmed using standard PROM programmers. This allows designers to use PAL devices with a minimum investment in special equipment. Many types of programmable logic, such as the FPLA, require an expensive, dedicated programmer.

## Secure Data



The PAL device verification logic can be completely disabled by blowing out a special "last link". This prevents the unauthorized copying of valuable data, and makes the PAL device perfect for use in any application where data integrity must be carefully guarded.

## Summary

The PAL device family of logic devices offers logic designers new options in the implementation of sequential and combinatorial logic designs. The family is fast, compact, flexible, and easy to use in both new and existing designs. It promises to reduce costs in most areas of design and production with a corresponding increase in product profitability.

## A Great Performer!




PAL16R6 Logic Symbols


PAL16R6 Logic Diagram


PAL16R6 Metalization

# PAL® (Programmable Array Logic) Devices HAL® (Hard Array Logic) Devices 

## Features/Benefits

- Reduces SSI/MSI chip count greater than 5 to 1
- Saves space with SKINNYDIP® packages
- Reduces IC inventories substantially
- Expedites and simplifies prototyping and board layout
- PALASM®2 silicon compiler provides easy design entry
- Security fuse reduces possibility of copying by competitors


## Description

The PAL device family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.
The HAL device family utilizes standard Low-Power Schottky TTL process and automated mask pattern generation directly from logic equations to provide a semi-custom gate array for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.
The PAL device lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.
The PAL/HAL device transfer function is the familiar sum of products. Like the PROM, the PAL device has a single array of fusible links. Unlike the PROM, the PAL device is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array).

In addition the PAL/HAL device provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability
- Exclusive-OR gates

Unused input pins should be tied directly to $V_{C C}$ or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. PAL/HAL device Logic Diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets. PALASM software automatically generates a similar diagram, called the fuse plot.
The entire PAL device family is programmed using inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL device is programmed and verified, two additonal fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.
To design a HAL, the user first programs and debugs a PAL device using PALASM and the "PAL DEVICE DESIGN SPECIFICATION" standard format. This specification is submitted to Monolithic Memories where it is computer-processed and assigned a bit pattern number, e.g., H01234.
Monolithic Memories will provide a PAL device sample for customer qualification. The user then submits a purchase order for a HAL of the specified bit pattern number, e.g., HAL18L4 H01234. For details on ordering HAL devices, please refer to the brochure, ProPAL, HAL, and ZHAL Devices: The Logical Solutions for Volume Programmable Logic, available from Monolithic Memories.

[^28]
## Register Bypass (MegaPAL Devices)

Outputs within a bank must either be all registered or all combinatorial. Whether or not a bank of registers is bypassed depends on how the outputs are defined in the equations. A colon followed by an equal sign [:=] specifies a registered output with feedback which is updated after the low-to-high transition of the clock. An equal sign [=] defines a combinatorial output which bypasses the register. Registers are bypassed in banks of eight. Bypassing a bank of registers eliminates the feedback lines for those outputs.

## Output Polarity

Output polarity is defined by comparison of the pin list and the equations. If the logic sense of a specific output in the pin list is different from the logic sense of that output as defined by its equation, the output is inverted or active low polarity. If the logic sense of a specific output in the pin list is the same as the logic sense of that output as defined by its equation, the output is active high polarity. Note that the P, RA, RS, and MegaPAL devices have programmable output polarity.

## Product Term Sharing <br> (RS, MegaPAL Devices)

The basic configuration is sixteen product terms shared between two output cells. For a typical output pair; each product term can be used by either output; but, since product term sharing is exclusive, a product term can be used by only one output, not both. If equations call for an output pair to use the same product term, two product terms are generated, one for each output. This should be taken into account when writing equations. PAL device assemblers configure product terms automatically.

## Product Term Editing

A unique feature of product term sharing is the ability to edit the design after the device has been programmed. Without this feature, a new PAL device had to be programmed if the user needed to change his design. Product term editing allows the user to delete an unwanted product term and reprogram a previously unused product term to the desired fuse pattern. This feature is made possible by the product term sharing architecture. Since each product term can be routed to either output in a given pair by selecting one of two steering fuses, it is possible to blow both of the steering fuses thereby completely disabling that product term. Once disabled, that product term is powered down, saving typically 0.25 mA . The desired change may now be programmed into one of the previously unused product terms corresponding to that output pair. Additional edits can be made as long as there are unused product terms for the output in question.

## PRESET Feature (PAL64R32 only)

Register banks of eight may be PRESET to all highs on the outputs by setting the PRESET pin (PS) to a Low level. Note from the Logic Diagram that when the state of an output is High, the state of the register is Low due to the inverting tri-state buffer.

## TTL-Level Preload Features (RA, MegaPAL Devices)

Preload pins have been added to enable the testability of each state in state-machine design. Typically, for a modulo-n counter or a state machine there are many unreachable states for the registers. These states, and the logic which controls them are untestable without a way to "set-in" the desired starting state of the registers. In addition, long test sequences are sometimes needed to test a state machine simply to reach those starting states which are legal. Since complete logic verification is needed to ensure the proper exit from "illegal" or unused states, a way to enter these states must be provided. The ability to preload a given bank of registers is provided in this device.
To use the preload feature, several steps must be followed. First, a high level on an assertive-low output enable pin disables the outputs for that bank of registers. Next, the data to be loaded is presented at the output pins. This data is then loaded into the register by placing a low level on the PRELOAD pin. PRELOAD is asynchronous with respect to the clock.


## Programmable Set and Reset (RA Family only)

In each SMAC, two product lines are dedicated to asynchronous set and reset. If the set product line is high, the register output becomes a logic 1 . If the reset product line is high, the register output becomes a logic 0 . The operation of the programmable set and reset overrides the clock. Note that set and reset are in reference to the register, independent of polarity.

## Individually Programmable Register Bypass (RA Family only)

If both the set and reset product lines are high, the sum-ofproducts bypasses the register and appears immediately at the output, thus making the output combinatorial. This allows each output to be configured in the registered or combinatorial mode.

## Programmable Clock (RA Family only)

One of the product lines in each group is connected to the clock. This provides the user with the additional flexibility of a programmable clock, so each output can be clocked independently of all the others.

Monolithic Memories PAL® Device Menu

| FAMILY | PART NUMBER | PACKAGE | DESCRIPTION |  |  | MAXIMUM |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | INPUTS | OUTPUTS |  | $\begin{gathered} \mathbf{t}^{\mathbf{P}}{ }^{\text {ns }}{ }^{*} \end{gathered}$ | $\begin{gathered} \mathrm{ICC} \\ \mathrm{~mA} \end{gathered}$ |
|  |  |  |  | COMBINATORIAL | REGISTERED |  |  |
| Small 20 Combinatorial | PAL10H8 <br> PAL12H6 <br> PAL14H4 <br> PAL16H2 <br> PAL16C1 <br> PAL10L8 <br> PAL12L6 <br> PAL14L4 <br> PAL16L2 | $\begin{gathered} \text { 20N, J, NL, } \\ F, L \end{gathered}$ | $\begin{aligned} & \hline 10 \\ & 12 \\ & 14 \\ & 16 \\ & 16 \\ & 10 \\ & 12 \\ & 14 \\ & 16 \end{aligned}$ | 8 6 4 2 2 8 6 4 2 | $\begin{aligned} & \text { - } \\ & \text { - } \\ & \text { - } \\ & \text { - } \\ & - \end{aligned}$ | $\begin{aligned} & 35 \\ & 35 \\ & 35 \\ & 35 \\ & 40 \\ & 35 \\ & 35 \\ & 35 \\ & 35 \end{aligned}$ | 90 |
| Small 20－2 Combinatorial | PAL10H8－2 <br> PAL12H6－2 <br> PAL14H4－2 <br> PAL16H2－2 <br> PAL16C1－2 <br> PAL10L8－2 <br> PAL12L6－2 <br> PAL14L4－2 <br> PAL16L2－2 | $\begin{gathered} 20 \mathrm{~N}, \mathrm{~J}, \mathrm{NL}, \\ F, \mathrm{~L} \end{gathered}$ | $\begin{aligned} & 10 \\ & 12 \\ & 14 \\ & 16 \\ & 16 \\ & 10 \\ & 12 \\ & 14 \\ & 16 \end{aligned}$ | $\begin{aligned} & \hline 8 \\ & 6 \\ & 4 \\ & 2 \\ & 2 \\ & 8 \\ & 6 \\ & 4 \\ & 2 \end{aligned}$ | $\begin{aligned} & \text { 二 } \\ & \text { 二 } \\ & \text { 二 } \\ & \text { — } \\ & \hline \end{aligned}$ | 60 | 45 |
| Medium 20 Standard | PAL16L8 <br> PAL16R8 <br> PAL16R6 <br> PAL16R4 | 20N，J，NL | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & 8 \\ & \hline 2 \\ & 4 \end{aligned}$ | $\begin{aligned} & 8 \\ & 6 \\ & 4 \end{aligned}$ | 35 | 180 |
| Medium 20A Standard | PAL16L8A <br> PAL16R8A <br> PAL16R6A <br> PAL16R4A | $\begin{gathered} \text { 20N, J, NL, } \\ \text { W, L } \end{gathered}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & \overline{8} \\ & 6 \\ & 4 \end{aligned}$ | 25 | 180 |
| Medium 20A－2 Standard | PAL16L8A－2 <br> PAL16R8A－2 <br> PAL16R6A－2 <br> PAL16R4A－2 | $\underset{F, L}{20 N, J, ~ N L, ~}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 2 \\ & 4 \end{aligned}$ | $\begin{aligned} & 8 \\ & 6 \\ & 4 \end{aligned}$ | 35 | 90 |
| Medium 20A－4 Standard | PAL16L8A－4 <br> PAL16R8A－4 <br> PAL16R6A－4 <br> PAL16R4A－4 | $\begin{gathered} 20 \mathrm{~N}, \mathrm{~J}, \mathrm{NL}, \\ \mathrm{~F}, \mathrm{~L} \end{gathered}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & \overline{8} \\ & 6 \\ & 4 \\ & \hline \end{aligned}$ | 55 | 50 |
| Medium 20B Standard | PAL16L8B <br> PAL16R8B <br> PAL16R6B <br> PAL16R4B | $\begin{gathered} 20 \mathrm{~N}, \mathrm{~J}, \mathrm{NL}, \\ \mathrm{~W}, \mathrm{~L} \end{gathered}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & - \\ & 6 \\ & 6 \\ & 4 \end{aligned}$ | 15 | 180 |
| Medium 20B－2 Standard | PAL16L8B－2 <br> PAL16R8B－2 <br> PAL16R6B－2 <br> PAL16R4B－2 | $\begin{gathered} \text { 20N, J, NL, } \\ \text { W, L } \end{gathered}$ | $\begin{aligned} & \hline 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & \overline{8} \\ & 6 \\ & 4 \end{aligned}$ | 25 | 90 |
| Medium 20B－4 Standard | PAL16L8B－4 <br> PAL16R8B－4 <br> PAL16R6B－4 <br> PAL16R4B－4 | $\begin{gathered} 20 \mathrm{~N}, \mathrm{~J}, \mathrm{NL}, \\ \mathrm{~W}, \mathrm{~L} \end{gathered}$ | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & 8 \\ & \hline 2 \\ & 4 \end{aligned}$ | $\begin{aligned} & 8 \\ & 6 \\ & 4 \end{aligned}$ | 35 | 55 |
| Medium 20AP Programmable Polarity | PAL16P8A <br> PAL16RP8A <br> PAL16RP6A <br> PAL16RP4A | 20N，J，NL | $\begin{aligned} & 16 \\ & 16 \\ & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & -8 \\ & 6 \\ & 4 \\ & \hline \end{aligned}$ | 25／30＊＊ | 180 |
| Large 20 Arithmetic | PAL16X4 <br> PAL16A4 | $\begin{gathered} 20 \mathrm{~N}, \mathrm{~J}, \mathrm{NL}, \\ \mathrm{~F}, \mathrm{~L} \end{gathered}$ | $\begin{aligned} & 16 \\ & 16 \end{aligned}$ | $\begin{aligned} & 4 \\ & 4 \end{aligned}$ | $\begin{aligned} & 4 \\ & 4 \end{aligned}$ | 40 | $\begin{aligned} & 225 \\ & 240 \end{aligned}$ |
| Large 20RA Asynchronous | PAL16RA8 | 20N，J，NL | 16 | － | 8 | 30／35＊＊ | 170 |
| ＊Minimum commerc <br> ＊＊Polarity fuse progra | su for devices with all r ed（active High）． | stered outputs | $N=$ Plastic DIP <br> NS＝Plastic SKINNYDIP <br> $J=$ Ceramic DIP <br> JS＝Ceramic SKINNYDIP |  | $\begin{aligned} \text { NL } & =\text { Plastic Leaded Chip Carrier (PLCC) } \\ P & =\text { Pin Grid Array } \\ L & =\text { Leadless Chip Carrier (LCC) } \\ W & =\text { Cerpack } \\ F & =\text { Ceramic Solder Seal Flat Pack } \end{aligned}$ |  |  |

## Monolithic Memories PAL Device Menu

## PAL Circuit Series 24

| FAMILY | PART NUMBER | PACKAGE | DESCRIPTION |  |  | MAXIMUM |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | INPUTS | OUTPUTS |  | $\begin{gathered} \text { tPD* } \\ \text { ns } \end{gathered}$ | ICC mA |
|  |  |  |  | COMBINATORIAL | REGISTERED |  |  |
| Small 24 Combinatorial | PAL12L10 <br> PAL14L8 <br> PAL16L6 <br> PAL18L4 <br> PAL20L2 <br> PAL20C1 | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | $\begin{aligned} & 10 \\ & 14 \\ & 16 \\ & 18 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & 10 \\ & 8 \\ & 6 \\ & 4 \\ & 2 \\ & 2 \end{aligned}$ | $\begin{aligned} & \overline{-} \\ & \overline{-} \\ & \hline \end{aligned}$ | 40 | 100 |
| Small 24A Decoder | PAL6L16A <br> PAL8L14A | $\begin{aligned} & \text { 24NS,JS, } \\ & \text { 28NL } \end{aligned}$ | $\begin{aligned} & 6 \\ & 8 \end{aligned}$ | $\begin{aligned} & 16 \\ & 14 \end{aligned}$ | - | 25 | 90 |
| Medium 24A Standard | PAL20L8A PAL20R8A PAL20R6A PAL20R4A | 24NS, JS, W, 28NL, 28L | $\begin{aligned} & 20 \\ & 20 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & \overline{8} \\ & 6 \\ & 4 \end{aligned}$ | 25 | 210 |
| Medium 24A-2 <br> Standard | PAL20L8A-2 <br> PAL20R8A-2 <br> PAL20R6A-2 <br> PAL20R4A-2 | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & \hline 4 \end{aligned}$ | $\begin{aligned} & 8 \\ & 6 \\ & 4 \end{aligned}$ | 35 | 105 |
| Medium 24B Standard | PAL20L8B <br> PAL20R8B <br> PAL20R6B <br> PAL20R4B | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & \frac{8}{2} \\ & 4 \end{aligned}$ | $\begin{aligned} & -8 \\ & 6 \\ & 4 \\ & \hline \end{aligned}$ | 15 | 210 |
| Medium 24X <br> Exclusive OR | PAL20L10 <br> PAL20X10 <br> PAL20X8 <br> PAL20X4 | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \\ & 20 \\ & 20 \end{aligned}$ | $\begin{aligned} & \frac{10}{2} \\ & 4 \end{aligned}$ | $\begin{gathered} \overline{10} \\ 8 \\ 4 \end{gathered}$ | 50 | $\begin{aligned} & 165 \\ & 180 \\ & 180 \\ & 180 \end{aligned}$ |
| Medium 24XA Exclusive OR | PAL20L10A <br> PAL20X10A <br> PAL20X8A <br> PAL20X4A | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \\ & 20 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{aligned} & \frac{10}{2} \\ & 6 \end{aligned}$ | $\begin{gathered} 10 \\ 8 \\ 8 \end{gathered}$ | 30 | $\begin{aligned} & 165 \\ & 180 \\ & 180 \\ & 180 \end{aligned}$ |
| Large 24RS Shared Product Terms | PAL20S10 <br> PAL20RS10 <br> PAL20RS8 <br> PAL20RS4 | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | $\begin{aligned} & 20 \\ & 20 \\ & 20 \\ & 20 \\ & \hline \end{aligned}$ | $\begin{aligned} & \frac{10}{2} \\ & 6 \end{aligned}$ | $\begin{gathered} 10 \\ 8 \\ 4 \end{gathered}$ | $\begin{gathered} 35 / 40^{* *} \\ 35 \\ 35 / 40^{* *} \\ 35 / 40^{* *} \end{gathered}$ | $\begin{aligned} & 240 \\ & 240 \\ & 240 \\ & 240 \end{aligned}$ |
| Large 24RA Asynchronous | PAL20RA10 | $\begin{aligned} & \text { 24NS, JS, W, } \\ & \text { 28NL, 28L } \end{aligned}$ | 20 | - | 10 | 30/35** | 200 |

## PAL Circuit Series MegaPAL'm

| FAMILY | PART NUMBER | PACKAGE | DESCRIPTION |  | MAXIMUM |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | INPUTS | REGISTERED OUTPUTS | $\begin{gathered} \text { tPD* } \\ \text { ns } \end{gathered}$ | ICC mA |
| 1500 Gates | PAL32R16 | 40N, J, 44NL, 44L | 32 | 16 | 40/45** | 280 |
| 5000 Gates | PAL64R32 | 88P, 84L | 64 | 32 | 50/55** | 640 |

[^29]
## fMAX Parameters

The parameter $\mathrm{f}_{\text {MAX }}$ is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, $f_{\text {MAX }}$ for the B-speed devices is specified to address two major classes of synchronous designs.

The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is
employed (Figure 1). Under these conditions, the frequency of operation is limited by the greater of the data setup time ( $\mathrm{t}_{\mathrm{su}}$ ) or the minimum clock period (twhigh + tw low). This parameter is designated fMAX (no feedback).
For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feeback paths (Figure2). Under these conditions, fMAX is defined as the reciprocal of ( $\mathrm{t}_{\text {su }}+\mathrm{t}_{\mathrm{CLK}}$ ) and is designated fMAX (feedback).


Figure 1. No Feedback


Figure 2. Feedback


16L8/B/B-2/B-4
A/A-2/A-4



16R8/B/B-2/B-4 A/A-2/A-4


16R6/B/B-2/B-4
A/A-2/A-4


16R4/B/B-2/B-4 A/A-2/A-4


16X4


16A4




10H8/-2


10L8/-2


16H2/-2


12H6/-2


12L6/-2


16L2/-2

$16 R 8 / B / B-2 / B-4$
$A / A-2 / A-4$


14H4/-2


14L4/-2


16C1/-2






12 L 10


14L8


16L6





20R4A/A-2/B


20RA10


## 20-Pin PAL/HAL Devices-PLCC



20RS4


6L16A


8L14A



64R32


Plastic Chip Carrier

32R16



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{T}$ A | Operating free-air temperature | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{T} \mathrm{C}$ | Operating case temperature |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions



## Switching Characteristics

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{t} \mathrm{PD}$ | Input or feedback to output | Except 16C1 |  | $\begin{aligned} & R 1=560 \Omega \\ & R 2=1.1 \mathrm{k} \Omega \end{aligned}$ |  | 25 | 45 |  | 25 | 35 | ns |
|  |  | 16C1 |  |  | 25 | 45 |  | 25 | 40 |  |  |

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP | MaX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}}{ }^{*}$ | High-level input voltage |  |  |  | 2 |  |  | $v$ |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -0.8 | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.02 | -0.25 | mA |
| $\mathrm{IIH}^{\text {d }}$ | High-level input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $V_{1}=2.4 \mathrm{~V}$ |  |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{I}_{\mathrm{OL}}=4 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
|  |  |  | Com | $\mathrm{I}^{\mathrm{OL}}=4 \mathrm{~mA}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{I}^{\mathrm{OH}}=-1 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
|  |  |  | Com | $\mathrm{I}^{\mathrm{OH}}=-1 \mathrm{~mA}$ |  |  |  |  |
| Ios | Output short-circuit current ** | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| Icc | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  |  | 30 | 45 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST | MILITARY | COMMERCIAL <br> COM | UNIT |
| :--- | :---: | :---: | :---: | :---: | :---: |
| tPD | Input or feedback to output | $R 1=1.12 \mathrm{k} \Omega$ |  | 45 | 80 |

## Standard PAL/HAL Devices Series 20 <br> 16L8, 16R8, 16R6, 16R4, 16X4, 16A4

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY 16X4/A4 ONLY MIN TYP MAX |  |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VCC | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {tw }}$ | Width of clock | Low | 25 | 10 |  | 25 | 10 |  | ns |
|  |  | High | 25 | 10 |  | 25 | 10 |  |  |
| $\mathrm{t}_{\text {su }}$ | Set up time from input or feedback to clock | 16R8, 16R6, 16R4 | 45 | 25 |  | 35 | 25 |  | ns |
|  |  | 16X4, 16A4 | 55 | 30 |  | 45 | 30 |  |  |
| th | Hold time |  | 0 | -15 |  | 0 | -15 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TC | Operating case temperature |  |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics



## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MILITARY 16X4/A4 ONLY MIN TYP MAX |  |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPD | Input or feedback to output | 16R6, 16R4, 16L8 | $\begin{aligned} & \mathrm{R}_{1}=200 \Omega \\ & \mathrm{R}_{2}=390 \Omega \end{aligned}$ |  |  |  |  | 25 | 35 | ns |
|  |  | 16X4, 16A4 |  |  | 30 | 45 |  | 30 | 40 |  |
| tCLK | Clock to output or feedback |  |  |  | 15 | 25 |  | 15 | 25 | ns |
| tPZX | Pin 11 to output enable except 16L8 |  |  |  | 15 | 25 |  | 15 | 25 | ns |
| tPXZ | Pin 11 to outpu | le except 16L8 |  |  | 15 | 25 |  | 15 | 25 | ns |
|  | Input to | 16R6, 16R4, 16L8 |  |  |  |  |  | 25 | 35 |  |
| tPZX | output enable | 16X4, 16A4 |  |  | 30 | 45 |  | 30 | 40 | ns |
| tPX | Input to | 16R6, 16R4, 16L8 |  |  |  |  |  | 25 | 35 |  |
| tPX | output disable | 16X4, 16A4 |  |  | 30 | 45 |  | 30 | 40 | ns |
|  | Maximum | 16R8, 16R6, 16R4 |  |  |  |  | 16 | 25 |  | Mz |
| MAX | frequency | 16X4, 16A4 |  | 12 | 22 |  | 14 | 22 |  | Mz |

## Fast PAL/HAL Devices Series 20A 16L8A, 16R8A, 16R6A, 16R4A

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {w }}$ w | Width of clock | Low | 20 | 10 |  | 15 | 10 |  | ns |
|  |  | High | 20 | 10 |  | 15 | 10 |  |  |
| $\mathrm{t}_{\mathrm{su}}$ | Set up time from input or feedback to clock | 16R8A, 16R6A, 16R4A | 30 | 15 |  | 25 | 15 |  | ns |
| $t_{h}$ | Hold time |  | 0 | -10 |  | 0 | -10 |  | ns |
| ${ }^{\text {T }}$ A | Operating free-air temperature |  | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\top} \mathrm{C}$ | Operating case temperature |  |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions



## Switching Characteristics Over Operating Conditions

|  | PARAMETER |  | TEST | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {t PD }}$ | Input or feedback to output | 16R6A, 16R4A, 16L8A | $\begin{aligned} & R_{1}=200 \Omega \\ & R_{2}=390 \Omega \end{aligned}$ |  | 15 | 30 |  | 15 | 25 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  | 10 | 20 |  | 10 | 15 | ns |
| ${ }_{\text {tPZX }}$ | Pin 11 to output enable except 16L8A |  |  |  | 10 | 25 |  | 10 | 20 | ns |
| ${ }_{\text {tPXZ }}$ | Pin 11 to output disable except 16L8A |  |  |  | 11 | 25 |  | 11 | 20 | ns |
| ${ }^{\text {t P P }}$ | Input to output enable | 16R6A, 16R4A, 16L8A |  |  | 10 | 30 |  | 10 | 25 | ns |
| ${ }^{\text {t P X }}$ \% | Input to output disable | 16R6A, 16R4A, 16L8A |  |  | 13 | 30 |  | 13 | 25 | ns |
| $f_{\text {MAX }}$ | Maximum frequency | 16R8A, 16R6A, 16R4A |  | 20 | 40 |  | 28.5 | 40 |  | MHz |

## Operating Conditions



Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}{ }^{*}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -0.8 | -1.5 | V |
| IL | Low-level input current $\dagger$ | $V_{\text {CC }}=$ MAX | $V_{1}=0.4 \mathrm{~V}$ |  |  | -0.02 | -0.25 | mA |
| IIH | High-level input current $\dagger$ | $V_{C C}=$ MAX | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{I}^{\mathrm{OL}}=12 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
|  |  |  | Com | $\mathrm{I}^{\mathrm{OL}}=24 \mathrm{~mA}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | ${ }^{\prime} \mathrm{OH}=-2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
|  |  |  | Com | ${ }^{\prime} \mathrm{OH}=-3.2 \mathrm{~mA}$ |  |  |  |  |
| 'OZL | Off-state output current $\dagger$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current ** | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| Icc | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  |  | 60 | 90 | mA |

## Switching Characteristics Over Operating Conditions

|  | PARAMETER |  | TEST | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {t PD }}$ | Input or feedback to output | 16L8A-2 16R6A-2 16R4A-2 | $\mathrm{R}_{1}=200 \Omega$ |  | 25 | 50 |  | 25 | 35 | ns |
| tCLK | Clock to output or feedback |  |  |  | 15 | 25 |  | 15 | 25 | ns |
| tPXZ/ZX | Pin 11 to output disable/enable except 16L8A-2 |  |  |  | 15 | 25 |  | 15 | 25 | ns |
| $t^{\prime}$ PZX | Input to output enable | 16L8A-2 16R6A-2 16R4A-2 | $\mathrm{R}_{2}=390 \Omega$ |  | 25 | 45 |  | 25 | 35 | ns |
| ${ }^{\text {t PXZ }}$ | Input to output disable | 16L8A-2 16R6A-2 16R4A-2 |  |  | 25 | 45 |  | 25 | 35 | ns |
| $f_{\text {max }}$ | Maximum frequency | 16R8A-2 16R6A-2 16R4A-2 |  | 14 | 25 |  | 16 | 25 |  | MHz |

## Quarter Power Series 20A-4

16L8A-4, 16R8A-4, 16R6A-4, 16R4A-4

## Operating Conditions

| SYMBOL | PARAMETER |  |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {tw }}$ | Width of clock |  | Low | 40 | 20 |  | 30 | 20 |  | ns |
|  |  |  | High | 40 | 20 |  | 30 | 20 |  |  |
| ${ }^{\text {t }}$ su | Set up time from input or feedback to clock | 16R8A-4 16R6A-4 16R4A-4 |  | 90 | 45 |  | 60 | 45 |  | ns |
| $t_{h}$ | Hold time |  |  | 0 | -15 |  | 0 | -15 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions


## Switching Characteristics Over Operating Conditions

|  | PARAMETER |  | TEST | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| L |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{t} P D$ | Input or feedback to output | 16R6A-4 16R4A-4 16L8A-4 |  | $\begin{aligned} & R_{1}=800 \Omega \\ & R_{2}=1.56 \mathrm{k} \Omega \end{aligned}$ |  | 35 | 75 |  | 35 | 55 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  | 20 | 45 |  | 20 | 35 | ns |
| ${ }^{\text {t PXX } / Z X}$ | Pin 11 tooutputdisable/enable-except 16L8A-4 |  |  |  | 15 | 40 |  | 15 | 30 | ns |
| ${ }^{\text {t P Z X }}$ | Input to output enable | 16R6A-4 16R4A-4 16L8A-4 |  |  | 30 | 65 |  | 30 | 50 | ns |
| ${ }^{1} \mathrm{PXZ}$ | Input to output disable | 16R6A-4 16R4A-4 16L8A-4 |  |  | 30 | 65 |  | 30 | 50 | ns |
| ${ }^{\text {f MAX }}$ | Maximum frequency | 16R8A-4 16R6A-4 16R4A-4 | 8 |  | 18. |  | 111 | 18 |  | MHz |

## PAL Series 20B Very High Speed Programmable Array Logic

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MMER <br> TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $t_{w}$ | Width of clock | Low | 10 | 6 |  | ns |
|  |  | High | 10 | 5 |  |  |
| ${ }^{\text {tsu }}$ | Setup time from input or feedback to clock | 16R8B 16R6B 16R4B | 15 | 10 |  | ns |
| $t_{n}$ | Hold time |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{\text {* }}$ | High-level input voltage |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| ILI $\dagger$ | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| ${ }_{1 / 4}{ }^{\dagger}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | ${ }^{\prime} \mathrm{OL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| ${ }^{\text {l OZL }}$ + | Off-state output current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}{ }^{\dagger}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| 'Os** | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | -30 | -70 | -130 | mA |
| ICC | Supply current | $V_{C C}=M A X$ |  |  | 120 | 180 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | $\begin{gathered} \text { AMER } \\ \text { TVD } \end{gathered}$ | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{\text {PD }}$ | 16L8B, 16R4B, 16R6B input or feedback to output |  | $\begin{aligned} & \text { Commercial } \\ & \mathrm{R}_{1}=200 \Omega \\ & \mathrm{R}_{2}=360 \Omega \end{aligned}$ |  | 12 | 15 | ns |
| ${ }^{\text {t CLIK }}$ | Clock to output or feedback except 16L8B |  |  |  | 8 | 12 | ns |
| $t_{\text {P }}$ | Pin 11 to output enable except 16L8B |  |  |  | 10 | 15 | ns |
| $t_{P X Z}$ | Pin 11 to output disable except 16L8B |  |  |  | 10 | 15 | ns |
| $t_{P Z X}$ | Input to output enable | 16R6B, 16R4B, and 16L8B |  |  | 12 | 22 | ns |
| ${ }^{\text {tPXZ }}$ | Input to output disable | 16R6B, 16R4B, and 16L8B |  |  | 12 | 20 | ns |
| ${ }_{\text {f MAX }}$ | 16R8B, 16R6B, 16R4B <br> Maximum frequency | Feedback |  | 37 | 45 |  |  |
|  |  | No feedback |  | 50 | 55 |  | MHz |

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MMER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {t }}$ w | Width of clock | Low | 15 | 10 |  | ns |
|  |  | High | 15 | 10 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time from input or feedback to clock | $\begin{aligned} & \text { 16R8B-2 } \\ & \text { 16R6B-2 } \\ & \text { 16R4B-2 } \end{aligned}$ | 25 | 15 |  | ns |
| $t_{h}$ | Hold time |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | COMMERCIAL <br> MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{*}$ | High-level input voltage |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | $V$ |
| $\mathrm{ILI}^{\dagger}$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| ${ }_{1 / 4}{ }^{\dagger}$ | High-level input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| VOL | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $1 \mathrm{OL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOH}^{\prime}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| ${ }^{\text {O OZL }}{ }^{\dagger}$ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}{ }^{\dagger}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| 'OS** | Output short-circuit current | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | $-100$ | -250 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $V_{C C}=M A X$ |  |  | 60 | 90 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{P D}$ | Input or feedback to output 16L8B-2, 16R4B-2, and 16R6B-2 | $\begin{aligned} & \text { Commercial } \\ & R_{1}=200 \Omega \\ & R_{2}=390 \Omega \end{aligned}$ |  | 17 | 25 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback except 16L8B-2 |  |  | 10 | 15 | ns |
| ${ }_{\text {t }}$ PZX | Pin 11 to output enable except 16L8B-2 |  |  | 10 | 20 | ns |
| $t_{\text {PXZ }}$ | Pin 11 to output disable except 16L8B-2 |  |  | 11 | 20 | ns |
| tPZX | Input to output enable 16R6B-2, 16R4B-2, and 16L8B-2 |  |  | 10 | 25 | ns |
| ${ }_{\text {t PXZ }}$ | Input to output disable 16R6B-2, 16R4B-2, and 16L8B-2 |  |  | 13 | 25 | ns |
| $\mathrm{f}_{\text {MAX }}$ | Maximum frequency 16R8B-2, 16R6B-2, and 16R4B-2 |  | 28.5 | 40 |  | MHz |

Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MMER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| ${ }^{t}$ w | Width of clock | Low | 25 | 10 |  | ns |
|  |  | High | 25 | 10 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time from input or feedback to clock | 16R8B-4 16R6B-4 16R4B-4 | 35 | 25 |  | ns |
| $t_{\text {h }}$ | Hold time |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}^{*}}{ }^{\text {( }}$ | High-level input voltage |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{C C}=\mathrm{MIN}$ | I $=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| $\mathrm{ILI}^{\dagger}$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| $\mathrm{IIH}^{\dagger}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{l}_{\mathrm{OL}}=8 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{l}_{\mathrm{OH}}=-1 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| ${ }^{\text {O OZL }}{ }^{\dagger}$ |  |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| $\mathrm{IOZH}^{+}$ | Off-state output current | x | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| los** | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -100 | -250 | mA |
| ${ }^{\text {ICC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 30 | 55 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{\text {PD }}$ | Input or feedback to output 16L8B-4, 16R4B-4, and 16R6B-4 | $\begin{aligned} & R_{1}=800 \Omega \\ & R_{2}=1.56 \mathrm{~K} \Omega \end{aligned}$ |  | 25 | 35 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback except 16L8B-4 |  |  | 15 | 25 | ns |
| ${ }_{\text {t }}^{\text {P }}$ X X | Pin 11 to output enable except 16L8B-4 |  |  | 15 | 25 | ns |
| tPXZ | Pin 11 to output disable except 16L8B-4 |  |  | 15 | 25 | ns |
| tPZX | Input to output enable 16R6B-4, 16R4B-4, and 16L8B-4 |  |  | 25 | 35 | ns |
| $t_{P X Z}$ | Input to output disable 16R6B-4, 16R4B-4, and 16L8B-4 |  |  | 25 | 35 | ns |
| ${ }^{\text {f MAX }}$ | Maximum frequency 16R8B-4, 16R6B-4, and 16R4B-4 |  | 16 | 25 |  | MHz |

## PAL Devices Series 20PA with Programmable Output Polarity

## Operating Conditions

| SYMBOL | PARAMETER |  |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  | 4.75 | 5 | 5.25 | V |
| $t_{w}$ | Width of clock | Low |  | 20 | 14 |  | ns |
|  |  | High |  | 10 | 6 |  |  |
| $t_{\text {su }}$ | Setup time from input or feedback to clock | $\begin{aligned} & \text { 16RP8A } \\ & \text { 16RP6A } \\ & \text { 16RP4A } \end{aligned}$ | Polarity fuse intact | 25 | 15 |  | ns |
|  |  |  | Polarity fuse blown | 30 | 20 |  |  |
| th | Hold time |  |  | 0 | -10 |  | ns |
| TA | Operating free-air temperature |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TC | Operating case temperature |  |  |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{\text {* }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 H^{*}}$ | High-level input voltage |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{C C}=\mathrm{MIN}$ | II $=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| IIL $\dagger$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| ${ }_{1 H}{ }^{+}$ | High-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| VOL | Low-level output voltage | $V_{C C}=M I N$ | $1 \mathrm{OL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{C C}=\mathrm{MIN}$ | $1 \mathrm{OH}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| lozlt | Off-state output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{\text {IOZHt }}$ | Or-state output current | C MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| Ios** | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ICC | Supply current | $\mathrm{V}_{C C}=\mathrm{MAX}$ |  |  | 120 | 180 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPD | Input or feedback to output 16P8A, 16RP6A, 16RP4A | Polarity fuse intact | $\begin{aligned} & \mathrm{R}_{1}=200 \Omega \\ & \mathrm{R}_{2}=390 \mathrm{~K} \Omega \end{aligned}$ |  | 15 | 25 |  |
|  |  | Polarity fuse blown |  |  | 20 | 30 | ns |
| tclk | Clock to output or feedback |  |  |  | 10 | 15 | ns |
| tpzX | Pin 11 to output enable except 16P8A |  |  |  | 10 | 20 | ns |
| tpXZ | Pin 11 to output disable except 16P8A |  |  |  | 11 | 20 | ns |
| tpZX | Input to output enable | 16RP6A, 16RP4A, and 16P8A |  |  | 10 | 25 | ns |
| tPXZ | Input to output disable | 16RP6A, 16RP4A, and 16P8A |  |  | 13 | 25 | ns |
| fMAX | Maximum frequency 16RP8A, 16RP6A, 16RP4A | Polarity fuse intact |  | 28.5 | 40 |  | MHz |
|  |  | Polarity fuse blown |  | 25 | 33 |  |  |

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $t_{w}$ | Width of clock |  | 20 | 13 |  | ns |
| $t_{\text {wp }}$ | Preload pulse width |  | 35 | 15 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Setup time for input or feedback to clock |  | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {sup }}$ | Preload setup time |  | 25 | 5 |  | ns |
| th | Hold time | Polarity fuse intact | 10 | -2 |  | ns |
|  |  | Polarity fuse blown | 0 | -6 |  | ns |
| thp | Preload hold time |  | 25 | 5 |  | ns |
| TA | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TC | Operating case temperature |  |  |  |  | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}}$ | High-level input voltage |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | II $=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| ILL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| IIH | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOL}=8 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | $\mathrm{IOH}^{\prime}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| IOZ | Off-state output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} / \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ | -100 |  | 100 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current | $V_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ICC | Supply current | $V_{C C}=\mathrm{MAX}$ |  |  | 135 | 170 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPD | Input or feedback to output | Polarity fuse intact | $\begin{aligned} & R_{1}=560 \Omega \\ & R_{2}=1.1 \mathrm{~K} \Omega \end{aligned}$ |  | 20 | 30 | ns |
|  |  | Polarity fuse blown |  |  | 25 | 35 |  |
| tCLK | Clock to output or feedback |  |  | 10 | 17 | 30 | ns |
| ts | Input to asynchronous set |  |  |  | 22 | 35 | ns |
| tR | Input to asynchronous reset |  |  |  | 27 | 40 | ns |
| tpzX | Pin 11 to output enable |  |  |  | 10 | 20 | ns |
| tPXZ | Pin 11 to output disable |  |  |  | 10 | 20 | ns |
| tpZX | Input to output enable |  |  |  | 18 | 30 | ns |
| tPXZ | Input to output disable |  |  |  | 15 | 30 | ns |
| fMAX | Maximum frequency |  |  | 20 | 35 |  | MHz |

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  | MIN | TYP | MAX | MIN | TYP |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{1 L}{ }^{*}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $V_{1 H}{ }^{*}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $V_{C C}=M 1 N$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  | -0.8 | -1.5 | V |
| If | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  | -0.02 | -0.25 | mA |
| IIH | High-level input current | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $V_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=M I N$ | MIL | $\mathrm{I}^{\text {OL }}=8 \mathrm{~mA}$ |  | 0.3 | 0.5 | v |
|  |  |  | COM | ${ }^{\prime} \mathrm{OL}=8 \mathrm{~mA}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | MIL | ${ }^{\prime} \mathrm{OH}=-2 m A$ | 2.4 | 2.8 |  | V |
|  |  |  | COM | $\mathrm{I}^{\mathrm{OH}}=-3.2 \mathrm{~mA}$ |  |  |  |  |
| Ios | Output short-circuit current** | $V_{C C}=5 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | $-130$ | mA |
| Icc | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | $\cdots$ |  | 60 | 100 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {tPD }}$ | Input or feedback to output | $\begin{aligned} & \mathrm{R} 1=560 \Omega \\ & \mathrm{R} 2=1.1 \mathrm{k} \Omega \end{aligned}$ |  | 25 | 45 |  | 25 | 40 | ns |

## Operating Conditions

| SYMBOL | PARAMETER | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITION | MIN TYP MAX |
| :--- | :--- | :--- | ---: | :---: | UNIT

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPD }}$ | Input to output propagation delay | $\begin{aligned} & \mathrm{R} 1=560 \Omega \\ & \mathrm{R} 2=1.1 \mathrm{~K} \Omega \end{aligned}$ |  | 15 | 25 | ns |

Fast Series 24A
20L8A, 20R8A, 20R6A, 20R4A
Operating Conditions

| SYMBOL |  | ETER |  | LITAR |  | CO | MERCI |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
|  | Width of clock | Low | 20 | 7 |  | 15 | 7 |  | ns |
| ${ }^{\text {w }}$ | Widh of clock | High | 20 | 7 |  | 15 | 7 |  | ns |
| ${ }^{\text {t }} \mathrm{su}$ | Set up time from input or feedback to clock | 20R8A 20R6A 20R4A | 30 | 15 |  |  | 15 |  | ns |
| $t_{h}$ | Hold time |  | 0 | -10 |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{T}$ C | Operating case temperature |  | 125 |  |  |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  | \% | 0.8 | V |
| $\mathrm{V}_{1 H}{ }^{*}$ | High-level input voltage | Na, |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $V_{C C}=\mathrm{MIN} \quad \quad I_{1}=-18 \mathrm{~mA}$ |  |  |  | -0.8 | -1.5 | V |
| IIL | Low-level input current $\dagger$ | $\mathrm{V}_{\text {CC }}=\mathrm{MAX} \quad \mathrm{V}_{1}=0.4$ |  |  |  | -0.02 | -0.25 | mA |
| 1 IH | High-level input current $\dagger$ | $V_{C C}=M A X$ |  |  |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X \quad V_{1}$ |  |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{I}^{\mathrm{OL}}=12 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
|  |  |  | Com | $\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=\mathrm{MIN}$ | Mil | ${ }^{1} \mathrm{OH}=-2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
|  |  |  | Com | ${ }^{\prime} \mathrm{OH}=-3.2 \mathrm{~mA}$ |  |  |  |  |
| ${ }^{\prime} \mathrm{OZL}$ | Off-state output current $\dagger$ | $V_{C C}=M A X$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| 'os | Output short-circuit current** | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=\mathrm{OV}$ | -30 | -90 | -130 | mA |
| ${ }^{1} \mathrm{Cc}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  |  | 160 | 210 | mA |

## Switching Characteristics Over Operating Conditions

|  | PARAMETER |  | TEST | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | CONDITIONS | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {t }}$ PD | Input or feedback to output | 20R6A 20R4A 20L8A | $\begin{aligned} & R_{1}=200 \Omega \\ & R_{2}=390 \Omega \end{aligned}$ |  | 15 | 30 |  | 15 | 25 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  | 10 | 20 |  | 10 | 15 | ns |
| ${ }^{\text {tPZX }}$ | Pin 13 to output enable except 20L8A |  |  |  | 10 | 25 |  | 10 | 20 | ns |
| ${ }_{\text {tPXZ }}$ | Pin 13 to output disable except 20L8A |  |  |  | 11 | 25 |  | 11 | 20 | ns |
| ${ }^{\text {t P }}$ (X | Input to output enable | 20R6A 20R4A 20L8A |  |  | 10 | 30 |  | 10 | 25 | ns |
| ${ }^{\text {t P X }}$ \% | Input to output disable | 20R6A 20R4A 20L8A |  |  | 13 | 30 |  | 13 | 25 | ns |
| ${ }^{\text {f M }}$ M ${ }^{\text {P }}$ | Maximum frequency | 20R8A 20R6A 20R4A |  | 20 | 40 |  | 28.5 | 40 |  | MHz |

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $t_{w}$ | Width of clock | Low | 25 | 10 |  | ns |
|  |  | High | 25 | 10 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time from input or feedback to clock | 20R8A-2, 20R6A-2, 20R4A-2 | 35 | 25 |  | ns |
| th | Hold time |  | 0 | -15 |  | ns |
| TA | Operating free-air temperature |  | 0 | - 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{\text {* }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 H^{*}}$ | High-level input voltage |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{VCC}_{\text {c }}=\mathrm{MIN}$ | If $=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| I/L $\dagger$ | Low-level input current | $V_{C C}=$ MAX | $V_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| ${ }_{1 / H \dagger}{ }^{+}$ | High-level input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| VOL | Low-level output voltage | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | $1 \mathrm{OL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOH}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| lozl $\dagger$ | state output current | $V_{C C C}=\mathrm{MAX}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{\text {IOZH }}{ }^{\text {+ }}$ | State output current | VCC MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| los** | Output short-circuit current | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ICC | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 80 | 105 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY <br> MIN TYP MAX |  |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t P }}$ | Input or feedback to output 20L8A-2 20R6A-2 20R4A-2 | $\begin{aligned} & \text { Commercial } \\ & R_{1}=200 \Omega \\ & \mathrm{R}_{2}=390 \Omega \end{aligned}$ |  | 25 | 50 |  | 25 | 35 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback except 20L8A-2 |  |  | 15 | 25 |  | 15 | 25 | ns |
| ${ }^{\text {t } P X Z Z Z X ~}$ | Pin 13 to output disable/enable except 20L8A-2 |  |  | 15 | 25 |  | 15 | 25 | ns |
| ${ }^{\text {P P Z }}$ X | Input to output enable 20L8A-2 20R6A-2 20R4A-2 |  |  | 25 | 45 |  | 25 | 35 | ns |
| ${ }^{\text {tPXZ }}$ | Input to output disable 20L8A-2 20R6A-2 20R4A-2 |  |  | 25 | 45 |  | 25 | 35 | ns |
| ${ }^{\text {f MAX }}$ | Maximum frequency 20R8A-2 20R6A-2 20R4A-2 |  | 14 | 19 |  | 16 | 19 |  | MHz |

## PAL Device Series 24B Very High Speed Programmable Array Logic

Operating Conditions


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{IL}}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{*}$ | High-level input voltage |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $1 .=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| IIL $\dagger$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| $\mathrm{IIH}^{\dagger}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{OL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOH}^{\prime}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| ${ }^{\text {l OZL }}{ }^{\dagger}$ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{\mathrm{O}} \mathrm{OHH}{ }^{\dagger}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| 'OS** | Output short-circuit current | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $V_{C C}=M A X$ |  |  | 140 | 210 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPD }}$ | Input or feedback to output 20L8B, 20R6B, 20R4B |  | Commercial$\begin{aligned} & R_{1}=200 \Omega \\ & R_{2}=390 \Omega \end{aligned}$ |  | 12 | 15 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback except 20L8B |  |  |  | 8 | 12 | ns |
| $t_{\text {PZX }}$ | Pin 13 to output enable except 20L8B |  |  |  | 10 | 15 | ns |
| $t_{P X Z}$ | Pin 13 to output disable except 20L8B |  |  |  | 8 | 12 | ns |
| ${ }^{\text {tPZX }}$ | Input to output enable 20R6B, 20R4B, 20L8B |  |  |  | 12 | 18 | ns |
| ${ }^{\text {t P X }}$ Z | Input to output disable 20R6B, 20R4B, 20L8B |  |  |  | 12 | 15 | ns |
| $f_{\text {MAX }}$ | Maximum frequency 20R8B, 20R6B, 20R4B | Feedback |  | 37 | 40 |  |  |
|  |  | No feedback |  | 45 | 50 |  | $z$ |

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $t_{w}$ | Width of clock | Low | 40 | 20 |  | 35 | 20 |  | ns |
|  |  | High | 30 | 10 |  | 25 | 10 |  |  |
| ${ }^{\text {tsu }}$ | Set up time from input or feedback to clock | 20X10, 20X8, 20X4 | 60 | 38 |  | 50 | 38 |  | ns |
| $t_{h}$ | Hold time |  | 0 | -15 |  | 0 | -15 |  | ns |
| $T_{\text {A }}$ | Operating free-air temperature |  | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{T} \mathrm{C}$ | Operating case temperature |  |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions



## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {t }}$ PD | Input or feedback to output 20X8, 20X4, 20LID | $\begin{aligned} & \mathrm{R}_{1}=200 \Omega \\ & \mathrm{R}_{2}=390 \Omega \end{aligned}$ |  | 35 | 60 |  | 35 | 50 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback except 20L10 |  |  | 20 | 35 |  | 20 | 30 | ns |
| ${ }^{\text {t PXZ }}$ /ZX | Pin 13 to output disable/enable except 20L10 |  |  | 20 | 45 |  | 20 | 35 | ns |
| ${ }^{\text {t P }}$ ( ${ }^{\text {P }}$ | Input to output enable except 20X10 |  |  | 35 | 55 |  | 35 | 45 | ns |
| ${ }^{\text {t PXZ }}$ | Input to output disable except 20X10 |  |  | 35 | 55 |  | 35 | 45 | ns |
| $\mathrm{f}_{\text {MAX }}$ | Maximum frequency 20X10, 20X8, 20X4 |  | 10.5 | 16 |  | 12.5 | 16 |  | MHz |

PAL Device Series 24XA

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MMER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $t_{w}$ | Width of clock | Low | 25 | 15 |  | ns |
|  |  | High | 15 | 7 |  |  |
| $t_{\text {su }}$ | Setup time from input or feedback to clock | $\begin{aligned} & 20 \times 10 \mathrm{~A} \\ & 20 \times 8 \mathrm{~A} \\ & 20 \times 4 \mathrm{~A} \end{aligned}$ | 30 | 20 |  | ns |
| $t_{h}$ | Hold time |  | 0 | -15 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{H}}{ }^{*}$ | High-level input voltage |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{C C}=\mathrm{MIN}$ | II $=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| $I_{\text {IL }} \dagger$ | Low-level input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| ${ }_{1 H}{ }^{\text {¢ }}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}^{\mathrm{OH}}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| ${ }^{\text {OZZL }}{ }^{\text {+ }}$ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{v}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}{ }^{\dagger}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| OOS* | Output short-circuit current | $\mathrm{V}_{C C}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| 1 CC | Supply current | $V_{C C}=M A X$ | 20×10A, 20X8A, 20×4A |  | 140 | 180 | mA |
|  |  |  | 20L10A |  | 115 | 165 |  |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | $\begin{aligned} & \text { MMER } \\ & \text { TYP } \end{aligned}$ | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t PD }}$ | Input or feedback to output 20L10A, 20X8A, and 20X4A |  | Commercial$R_{1}=200 \Omega$$R_{2}=360 \Omega$ |  | 23 | 30 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  | 10 | 15 | ns |
| ${ }_{\text {t }}^{\text {PZX }}$ | Pin 13 to output enable except 20L10A |  |  |  | 11 | 20 | ns |
| tPXZ | Pin 13 to output disable except 20L10A |  |  |  | 10 | 20 | ns |
| ${ }^{\text {t P } ~} \mathrm{XX}$ | Input to output enable | 20X8A, 20X4A, and 20L10A |  |  | 19 | 30 | ns |
| ${ }_{\text {tPXZ }}$ | Input to output disable | 20X8A, 20X4A, and 20L10A |  |  | 15 | 30 | ns |
| $f_{\text {MAX }}$ | Maximum frequency | 20X10A, 20X8A, and 20X4A |  | 22.2 | 32 |  | MHz |

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
|  | Width of clock | Low | 20 | 10 |  | 15 | 10 |  | ns |
| ${ }^{\text {w }}$ w | Width of clock | High | 20 | 10 |  | 15 | 10 |  | ns |
| ${ }^{\text {tsu }}$ | Setup time from input or feedback to clock | 20RS10 20RS8 20RS4 |  | 25 |  |  | 25 |  | ns |
| $t_{h}$ | Hold time |  | $0 \quad-10$ |  |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {T }}$ C | Operating case temperature |  |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{\text {* }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}{ }^{*}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  | -0.8 | -1.5 | V |
| $\mathrm{I}_{\text {IL }}{ }^{\dagger}$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.02 | -0.25 | mA |
| ${ }_{1 H}{ }^{+}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{I}^{\mathrm{OL}}=12 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
|  |  |  | Com | $\mathrm{I}^{\mathrm{OLL}}=24 \mathrm{~mA}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{I}^{\mathrm{OH}}=-2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
|  |  |  | Com | $\mathrm{I}_{\mathrm{OH}}=-3.2 \mathrm{~mA}$ |  |  |  |  |
| ${ }^{\text {OZLL }}{ }^{\dagger}$ | Off-state output current | $V_{C C}=M A X$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}{ }^{\dagger}$ |  |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~mA}$ |  |  | 100 |  |
| los** | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $V_{C C}=M A X$ |  |  |  | 175 | 240 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP | MAX |  | TYP | MAX |  |
| ${ }^{\text {t PD }}$ | Input or feedback to output 20S10, 20RS8, 20RS4 | Polarity fuse intact | $\begin{aligned} & \text { Commercial } \\ & R_{1}=200 \Omega \\ & R_{2}=390 \mathrm{~K} \Omega \end{aligned}$ |  | 25 | 40 |  | 25 | 35 |  |
|  |  | Polarity fuse blown |  |  | 30 | 45 |  | 30 | 40 |  |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  | 12 | 20 |  | 12 | 17 | ns |
| ${ }^{\text {tPZX }}$ | Pin 13 to output enable except 20S10 |  |  |  | 10 | 25 |  | 10 | 20 | ns |
| tPXZ | Pin 13 to output disable except 20510 |  |  |  | 11 | 25 |  | 11 | 20 | ns |
| ${ }^{\text {t }}$ PZX | Input to output enable | $\begin{aligned} & \text { 20S10, 20RS8, } \\ & \text { 20RS4 } \end{aligned}$ |  |  | 25 | - 35 |  | 25 | 35 | ns |
| tPXZ | Input to output disable | $\begin{aligned} & \text { 20S10, 20RS8 } \\ & \text { 20RP4 } \end{aligned}$ | Military$\begin{aligned} & R_{1}=390 \Omega \\ & R_{2}=750 \Omega \end{aligned}$ |  | 13 | 30 |  | 13 | 25 | ns |
| $\mathrm{f}_{\text {MAX }}$ | Maximum frequency | 20RS10, 20RS8, 20RS4 |  | 18 | 28 |  | 20 | 28 |  | MHz |

## PAL20RA10

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {t }}$ w | Width of clock | Low | 25 | 13 |  | 20 | 13 |  | ns |
|  |  | High | 25 | 13 |  | 20 | 13 |  |  |
| $t_{\text {wp }}$ | Preload pulse width |  | 45 | 15 |  | 35 | 15 |  | ns |
| $t_{\text {su }}$ | Setup time for input or feedback to clock |  | 25 | 10 |  | 20 | 10 |  | ns |
| $\mathrm{t}_{\text {sup }}$ | Preload setup time |  | 30 | 5 |  | 25 | 5 |  | ns |
| $t_{\text {h }}$ | Hold time | Polarity fuse intact | 10 | -2 |  | 10 | -2 |  | ns |
|  |  | Polarity fuse blown | 0 | -6 |  | 0 | -6 |  |  |
| thp | Preload hold time |  | 30 | 5 |  | 25 | 5 |  | ns |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature |  | -55 |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{T} \mathrm{C}$ | Operating case temperature |  |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{\text {* }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}{ }^{*}$ | High-level input voltage |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | V |
| IL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| $\mathrm{I}_{\mathrm{IH}}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{IOL}^{\text {OL }}=8 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=$ MIN | $\mathrm{I}_{\mathrm{OH}}$ : Mil-2 mA Com-3.2 mA | 2.4 | 2.8 |  | V |
| l OZ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V} / \mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ | -100 |  | 100 | $\mu \mathrm{A}$ |
| los** | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 155 | 200 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MILITARY MIN TYP MAX |  |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{t} \mathrm{PD}$ | Input or feedback to output | Polarity fuse intact | $\begin{gathered} R_{1}=560 \Omega \\ R_{2}=1.1 \mathrm{~K} \Omega \end{gathered}$ |  | 20 | 35 |  | 20 | 30 | ns |
|  |  | Polarity fuse blown |  |  | 25 | 40 |  | 25 | 35 |  |
| ${ }^{\mathrm{t}} \mathrm{CLK}$ | Clock to output or feedback |  |  | 10 | 17 | 35 | 10 | 17 | 30 | ns |
| ${ }^{\text {ts }}$ | Input to asynchronous set |  |  |  | 22 | 40 |  | 22 | 35 | ns |
| $\mathrm{t}_{\mathrm{R}}$ | Input to asynchronous reset |  |  |  | 27 | 45 |  | 27 | 40 | ns |
| ${ }^{\text {t P } ~} \mathrm{PX}$ | Pin 13 to output enable |  |  |  | 10 | 25 |  | 10 | 20 | ns |
| ${ }^{\text {t PXX }}$ | Pin 13 to output disable |  |  |  | 10 | 25 |  | 10 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PZX}$ | Input to output enable |  |  |  | 18 | 35 |  | 18 | 30 | ns |
| ${ }^{\text {t PXZ }}$ | Input to output disable |  |  |  | 15 | 35 |  | 15 | 30 | ns |
| ${ }^{\text {f MAX }}$ | Maximum frequency |  |  | 16 | 35 |  | 20 | 35 |  | MHz |

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {t }}$ w | Width of clock | Low | 25 |  |  | 20 |  |  | ns |
|  |  | High | 25 |  |  | 20 |  |  |  |
| $t_{\text {wp }}$ | Preload pulse width |  | 45 |  |  | 35 |  |  | ns |
| ${ }^{\text {tsu }}$ | Setup time for input to clock | Polarity fuse intact | 50 |  |  | 40 |  |  | ns |
|  |  | Polarity fuse blown | 50 |  |  | 40 |  |  |  |
| $\mathrm{t}_{\text {sup }}$ | Preload setup time |  | 30 |  |  | 25 |  |  | ns |
| $t_{\text {h }}$ | Hold time |  | 0 | -10 |  | 0 | -10 |  | ns |
| thp | Preload hold time |  | 10 |  |  | 5 |  |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 3 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{T} \mathrm{C}$ | Operating case temperature |  |  |  | 125 |  |  |  | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | $\underset{\operatorname{MIN}}{\text { MI }}$ | LITARY <br> TYP MAX | $\begin{aligned} & \text { COM } \\ & \text { MIN } \end{aligned}$ | IMERCIAL TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t }}$ PD | Input to output | Polarity fuse intact | $\begin{gathered} \mathrm{R}_{1}=560 \Omega \\ \mathrm{R}_{2}=1.1 \mathrm{~K} \Omega \end{gathered}$ |  | 50 |  | 40 | s |
|  |  | Polarity fuse blown |  |  | 55 |  | 45 |  |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  | 30 |  | 25 | ns |
| $t_{\text {t }}$ | Output enable |  |  |  | 25 |  | 20 | ns |
| $t_{P X Z}$ | Output disable |  |  |  | 25 |  | 20 | ns |
| ${ }^{\text {f MAX }}$ | Maximum frequency |  |  | 14 |  | 16 |  | MHz |

## PAL64R32

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MMER <br> TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {w }}$ w | Width of clock | Low | 20 |  |  | ns |
|  |  | High | 20 |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time from input to clock | Polarity fuse intact | 40 |  |  | ns |
|  |  | Polarity fuse blown | 40 |  |  |  |
| $t_{h}$ | Hold time |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| $T_{C}$ | Operating case temperature |  |  |  |  | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{VIL}^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{*}$ | High-level input voltage |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{C C}=\mathrm{MIN}$ | I $=-18 \mathrm{~mA}$ |  | -0.8 | -1.5 | $V$ |
| $\mathrm{I}_{1 /}$ | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| $\mathrm{I}_{1 \mathrm{H}}$ | High-level input current | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=\mathrm{MIN}$ | $\mathrm{l}_{\mathrm{OL}}=8 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOH}^{\prime}=-0.4 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| IOZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| OSA* | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \quad \mathrm{~V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -10 | -40 | -60 | mA |
| 1 CC | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 400 | 640 | mA |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MER TYP | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPD }}$ | Input to output | Polarity fuse intact | $\begin{aligned} & R_{1}=560 \Omega \\ & R_{2}=1.1 \mathrm{k} \Omega \end{aligned}$ |  |  | 50 | ns |
|  |  | Polarity fuse blown |  |  |  | 55 |  |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback |  |  |  |  | 22 | ns |
| ${ }^{\text {tPZX }}$ | Output enable |  |  |  |  | 30 | ns |
| tpXZ | Output disable |  |  |  |  | 30 | ns |
| ${ }^{\text {tPRH }}$ | Preset to output |  |  |  |  | 35 | ns |
| $\mathrm{f}_{\mathrm{MAX}}$ | Maximum frequency |  |  | 16 | 20 |  | MHz |

## PAL64R32

## Testing Conditions



## Output Register PRELOAD

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for PRELOAD is as follows:

## Series 20PA

1. Raise $\mathrm{V}_{\mathrm{CC}}$ to 4.5 V .
2. Disable output registers by setting pin 11 to $\mathrm{V}_{\mathrm{IH}}$.
3. Apply $\mathrm{V}_{\mathrm{IL}} N_{\mathrm{IH}}$ to all registered output pins.
4. Pulse pin 8 to $V_{p}$, then back to 0 V .
5. Remove $\mathrm{V}_{\mathrm{IL}} N_{\mathrm{IH}}$ from all output registers.
6. Lower pin 11 to $\mathrm{V}_{\mathrm{IL}}$ to enable the output registers.
7. Verify for $\mathrm{V}_{\mathrm{OL}} N_{\mathrm{OH}}$ at all registered output pins.

## Series 24RS/24XA

1. Raise $\mathrm{V}_{\mathrm{CC}}$ to 4.5 V .
2. Disable output registers by setting pin 13 to $\mathrm{V}_{\mathrm{IH}}$.
3. Apply $\mathrm{V}_{\mathrm{IL}} N_{I H}$ to all registered output pins.
4. Pulse pin 10 to $V_{p}$, then back to 0 V .
5. Remove $\mathrm{V}_{\mathrm{IL}} / \mathrm{V}_{\mathrm{IH}}$ from all output registers.
6. Lower pin 13 to $V_{I L}$ to enable the output registers.
7. Verify for $\mathrm{V}_{\mathrm{OL}} / \mathrm{N}_{\mathrm{OH}}$ at all registered output pins.

## Power-Up RESET

All devices with this PRELOAD feature also have power-up RESET. All registers power up to a logic high for predictable system initialization.


PIN 13


## Switching Waveforms



Notes: 1. Input pulse amplitude 0 V to 3.0 V ,
2. Input access measured at the 1.5 V level.




$16 C 1$





$16 L 8$



16R6


16R4


16P8


16RP8


16RP6


PAL/HAL Devices Logic Diagram

16RP4

$16 \times 4$







2012




## Logic Diagram

6L16A


## Logic Diagram


$20 L 8$


20R8




20 L 10



$20 \times 4$




## 20RS8



PAL/HAL Devices Logic Diagram

20RS4



## 32R16




## 20-Pin Device Family

## Data I/O Corporation

10525 Willows Road N.E.
PO Box 97046
Redmond, WA 98073-9746
(800) 247-5700


Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL™ Device Families

 Data I/O

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.
${ }^{1}$ Not supported on Model 19

## 20-Pin Device Family Digelec

1602 Lawrence Ave.
Suite 113
Ocean, NJ 07712
System UP803
(201) 493-2420


Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL"' Device Families

## Digelec



Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 20-Pin Device Family

 Kontron1230 Charleston Road
Mountain View, CA 94039-7230
(415) 965-7020

System MPP-80S
System EPP-80

| Series | Part Number | UPM-B Rev. |
| :---: | :---: | :---: |
| Small 20/-2 Combinatorial | PAL10H8/-2 | 1.44 |
|  | PAL10L8/-2 |  |
|  | PAL12H6/-2 |  |
|  | PAL12L6/-2 |  |
|  | PAL14H4/-2 |  |
|  | PAL14L4/-2 |  |
|  | PAL16H2/-2 |  |
|  | PAL16L2/-2 |  |
|  | PAL16C1/-2 |  |
| Medium 20/ PAL16L8/A/-2/-4/B-2/-4 |  |  |
| $\begin{aligned} & \text { 20A/20A-2/4/ } \\ & 20 B-2 /-4 \\ & \text { Standard } \end{aligned}$ | PAL16R8/A/-2/-4/B-2/-4 |  |
|  | PAL16R6/A/-2/-4/B-2/-4 |  |
|  | PAL16R4/A/-2/-4/B-2/-4 |  |
| - | - |  |
| Medium20B/D | PAL16L8B/D |  |
|  | PAL16R8B/D |  |
|  | PAL16R6B/D |  |
|  | PAL16R4B/D |  |
|  |  |  |
| Medium 20BP <br> Standard | PAL16L8BP | Under Development |
|  | PAL16R8BP |  |
|  | PAL16R6BP |  |
|  | PAL16R4BP |  |
|  |  |  |
| Medium 20PA Programmable Polarity | PAL16P8A | $1.44$ |
|  | PAL16RP8A |  |
|  | PAL16RP6A |  |
|  | PAL16RP4A |  |
| Large 20 Arithmetic | PAL16X4 |  |
|  | PAL16A4 |  |
| - . . . |  |  |
| Large 20RA Asynchronous | PAL16RA8 | 1.47 |

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL"' Device Families

## Kontron



| Large 24A <br> Registered XOR | PAL22RX8A |  |
| :---: | :---: | :---: |


| Large 24/A <br> Varied XOR | PAL32VX10/A | 1.48 |
| :---: | :---: | :---: |
| Large 24RA Asynchronous | PAL20RA10 | 1.44 |
| ECL <br> Combinatorial | PAL10H20P8 | 1.47 |
| MegaPALTM Devices | PAL32R16 | Under Development |

Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## PAL ${ }^{\circledR}$ Device Programmer Reference Guide

## 20-Pin Device Family

 MicroprossParc d'activite des Pres
5, rue Denis-Papin
59650 Villeneuve-d'Ascq
Tel 20479040

| Series | Part Number | Rev. |
| :---: | :---: | :---: |
| Small 20/-2 Combinatorial | PAL10H8/-2 | 3.5 |
|  | PAL10L8/-2 |  |
|  | PAL12H6/-2 |  |
|  | PAL12L6/-2 |  |
|  | PAL14H4/-2 |  |
|  | PAL14L4/-2 |  |
|  | PAL16H2/-2 |  |
|  | PAL16L2/-2 |  |
|  | PAL16C1/-2 |  |
|  |  |  |
|  |  |  |
| $\begin{aligned} & \text { Medium 20/ } \\ & \text { 20A/20A-2/4/ } \\ & 20 B-2 /-4 \\ & \text { Standard } \end{aligned}$ | PAL16R8/A/-2/-4/B-2/-4 |  |
|  | PAL16R6/A/-2/-4/B-2/-4 |  |
|  | PAL16R4/A/-2/-4/B-2/-4 |  |
| Medium 20B/D | PAL16L8B/D |  |
|  | PAL16R8B/D |  |
|  | PAL16R6B/D |  |
|  | PAL16R4B/D |  |
|  | M |  |
| Medium 20BP <br> Standard | PAL16L8BP | Under Development |
|  | PAL16R8BP |  |
|  | PAL16R6BP |  |
|  | PAL16R4BP |  |
|  |  |  |
| Medium 20PA <br> Programmable Polarity | PAL16P8A | 3.5 |
|  | PAL16RP8A |  |
|  | PAL16RP6A |  |
|  | PAL16RP4A |  |
| Large 20 Arithmetic | PAL16X4 |  |
|  | PAL16A4 |  |
|  |  |  |
| Large 20RA Asynchronous | PAL16RA8 | Under Development |

Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL™ Device Families

Micropross


| Small 24A | PAL6L16A |  |
| :---: | :--- | :--- |
| Decoder | PAL8L14A | Under Development |



Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## PAL® Device Programmer Reference Guide

## 20-Pin Device Family

## Promac

Adams MacDonald Enterprises, Inc.
2999 Monterey/Salinas Highway
Monterey, CA 93940
Promac P3
(408) 373-3607

Programmer

| Series | Part Number | Software Rev. | S1/S2 |
| :---: | :---: | :---: | :---: |
| Small 20/-2 Combinatorial | PAL10H8/-2 | 3.0 | 0/1 |
|  | PAL10L8/-2 |  | 0/6 |
|  | PAL12H6/-2 |  | 0/2 |
|  | PAL12L6/-2 |  | $0 / 7$ |
|  | PAL14H4/-2 |  | 0/3 |
|  | PAL14L4/-2 |  | 0/8 |
|  | PAL16H2/-2 |  | 0/4 |
|  | PAL16L2/-2 |  | 0/9 |
|  | PAL16C1/-2 |  | 0/5 |
| $\begin{gathered} \text { Medium } 20 / \\ 20 \mathrm{~A} / 20 \mathrm{~A}-2 / 4 / \\ 20 \mathrm{~B}-2 /-4 \\ \text { Standard } \\ \hline \end{gathered}$ | PAL16L8/A/-2/-4/B-2/-4 |  | 0/10 |
|  | PAL16R8/A/-2/-4/B-2/-4 |  | 0/11 |
|  | PAL16R6/A/-2/-4/B-2/-4 |  | 0/12 |
|  | PAL16R4/A/-2/-4/B-2/-4 |  | 0/13 |
|  | . . . . . . . . |  | . |
| Medium 20B/D | PAL16L8B/D |  | 5/0 |
|  | PAL16R8B/D |  | 5/1 |
|  | PAL16R6B/D |  | 5/2 |
|  | PAL16R4B/D |  | 5/3 |
|  |  | [ | - |
| Medium | PAL16L8BP | Under Development |  |
| 20BP | PAL16R8BP |  |  |
| Standard | PAL16R6BP |  |  |
|  | PAL16R4BP |  |  |
|  |  |  |  |
| Medium 20PA <br> Programmable <br> Polarity | PAL16P8A | 3.0 | 1/0 |
|  | PAL16RP8A |  | 1/3 |
|  | PAL16RP6A |  | 1/2 |
|  | PAL16RP4A |  | 1/1 |
|  |  |  | - |
| Large 20 Arithmetic | PAL16X4 |  | 0/14 |
|  | PAL16A4 |  | 0/15 |
|  | . . . |  |  |
| Large 20RA Asynchronous | PAL16RA8 |  | 1/12 |

Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL"' Device Families

## Promac

| Series | Part Number | Software Rev. | S1/S2 |
| :---: | :---: | :---: | :---: |
|  | PAL12L10 | 3.0 | 2/2 |
|  | PAL14L8 | 3.0 | 2/3 |
| Small 24 | PAL16L6 |  | $2 / 4$ |
| Combinatorial | PAL18L4 |  | $2 / 5$ |
|  | PAL20L2 |  | 2/6 |
|  | PAL20C1 |  | 2/1 |
| Small 24A | PAL6L16A |  | 3/11 |
| Decoder | PAL8L14A |  | 3/10 |
|  | PAL20L8A/-2/B |  | 2/8 |
| Medium 24A/ | PAL20R8A/-2/B |  | 2/9 |
| 24A-2/B | PAL20R6A-2/B |  | 2/10 |
| Standard | PAL20R4Al-2/B |  | 2/11 |
|  | PAL20L10 |  | $2 / 7$ |
| Medium 24X | PAL20X10 |  | 2/12 |
| Exclusive-OR | PAL20X8 |  | 2/13 |
|  | PAL20X4 |  | 2/14 |
|  | PAL20L10A |  | $2 / 7$ |
| Medium 24XA | PAL20X10A |  | 2/15 |
| Exclusive-OR | PAL20X8A |  | 3/0 |
|  | PAL20X4A |  | 3/1 |
|  | PAL20S10 |  | 3/5 |
| Large 24RS | PAL20RS10 |  | 3/6 |
| Shared | PAL20RS8 |  | 3/7 |
| Product Terms | PAL20RS4 |  | 3/8 |
| Large 24A Registered XOR | PAL22RX8A |  |  |
| Large 24/A Varied XOR | PAL32VX10/A |  |  |
| Large 24RA Asynchronous | PAL20RA10 |  | 3.4 |
| ECL <br> Combinatorial | PAL10H20P8 | $\downarrow$ |  |
| MegaPALTM <br> Devices | PAL32R16 | Under Development |  |
|  | PAL64R32 |  |  |

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 20-Pin Device Family

## Stag Microsystems

528-5 Weddell Drive Sunnyvale, CA 94089<br>(408) 745-1991

$$
\begin{aligned}
& \text { ZL30 } \\
& \text { PPZ }
\end{aligned}
$$




Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL"' Device Families

## Stag Microsystems



Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 20-Pin Device Family

## Storey Systems

3201 North Hwy. 67
Suite H
Mesquite, TX 75150
(214) 270-4135

| Series | Part Number | Rev. |
| :---: | :---: | :---: |
| Small 20/-2 Combinatorial | PAL10H8/-2 | 2.0 |
|  | PAL10L8/-2 |  |
|  | PAL12H6/-2 | $\checkmark$ |
|  | PAL12L6/-2 |  |
|  | PAL14H4/-2 |  |
|  | PAL14L4/-2 |  |
|  | PAL16H2/-2 |  |
|  | PAL16L2/-2 |  |
|  | PAL16C1/-2 |  |
| $\begin{gathered} \text { Medium } 20 / \\ 20 \mathrm{~A} / 20 \mathrm{~A}-2 / 4 / \\ 20 \mathrm{~B}-2 /-4 \\ \text { Standard } \\ \hline \end{gathered}$ | PAL16L8/A/-2/-4/B-2/-4 |  |
|  | PAL16R8/A/-2/-4/B-2/-4 |  |
|  | PAL16R6/A/-2/-4/B-2/-4 |  |
|  | PAL16R4/A/-2/-4/B-2/-4 |  |
|  | M.......... |  |
| Medium 20B/D | PAL16L8B/D | $4.0$ |
|  | PAL16R8B/D |  |
|  | PAL16R6B/D |  |
|  | PAL16R4B/D |  |
|  |  |  |
| $\begin{aligned} & \text { Medium } \\ & 20 B P \end{aligned}$ <br> Standard | PAL16L8BP | Under Development |
|  | PAL16R8BP |  |
|  | PAL16R6BP |  |
|  | PAL16R4BP |  |
|  |  |  |
| Medium 20PA <br> Programmable Polarity | PAL16P8A | $4.0$ |
|  | PAL16RP8A |  |
|  | PAL16RP6A |  |
|  | PAL16RP4A |  |
|  |  |  |
| Large 20 Arithmetic | PAL16X4 | 2.0 |
|  | PAL16A4 |  |
|  |  |  |
| Large 20RA Asynchronous | PAL16RA8 | 4.04 |

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL"' Device Families

Storey Systems

| Series | Part Number | Rev. |
| :---: | :---: | :---: |
| Small 24 <br> Combinatorial | PAL12L10 | 2.0 |
|  | PAL14L8 |  |
|  | PAL16L6 |  |
|  | PAL18L4 |  |
|  | PAL20L2 |  |
|  | PAL20C1 |  |


| Small 24A Decoder | PAL6L16A | Under Development |
| :---: | :---: | :---: |
|  | PAL8L14A |  |
| Medium 24A/ $24 A-2 / B$ <br> Standard | PAL20L8A/-2/B | 2.0 |
|  | PAL20R8A/-2/B |  |
|  | PAL20R6A/-2/B |  |
|  | PAL20R4A/-2/B |  |
| Medium 24X <br> Exclusive-OR | PAL20L10 | $\downarrow$ |
|  | PAL20X10 |  |
|  | PAL20X8 |  |
|  | PAL20X4 |  |
| Medium 24XA <br> Exclusive-OR | PAL20L10A |  |
|  | PAL20X10A | Under Developmen |
|  | PAL20X8A |  |
|  | PAL20X4A |  |
| Large 24RS Shared Product Terms | PAL20S10 |  |
|  | PAL20RS10 |  |
|  | PAL20RS8 |  |
|  | PAL20RS4 |  |


| Large 24A Registered XOR | PAL22RX8A |  |
| :---: | :---: | :---: |
| Large 24/A Varied XOR | PAL32VX10/A |  |
| Large 24RA Asynchronous | PAL20RA10 | 4.04 |
| ECL <br> Combinatorial | PAL10H20P8 |  |
| MegaPAL ${ }^{\text {TM }}$ Devices | PAL32R16 <br> PAL64R32 | Under Development |

Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 20-Pin Device Family

## Structured Design

1700 Wyatt Drive
Suite 7
Santa Clara, CA 95054
(408) $988-0725$


Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL™ Device Families

## Structured Design

| Series | Part Number | SD 20/24 | SD 1000 |
| :---: | :---: | :---: | :---: |
| Small 24 <br> Combinatorial | PAL12L10 | $\left.\right\|_{1} ^{1.6}$ | 1.05 |
|  | PAL14L8 |  |  |
|  | PAL16L6 |  |  |
|  | PAL18L4 |  |  |
|  | PAL20L2 |  |  |
|  | PAL20C1 |  |  |


| Small 24A <br> Decoder | PAL6L16A |  | Under Development |
| :---: | :--- | :--- | :--- |
|  | PAL8L14A |  |  |


| $\begin{gathered} \text { Medium 24A/ } \\ \text { 24A-2/B } \\ \text { Standard } \end{gathered}$ | PAL20L8A/-2/B | 1.6 | 1 |
| :---: | :---: | :---: | :---: |
|  | PAL20R8A/-2/B |  |  |
|  | PAL20R6A/-2/B |  |  |
|  | PAL20R4A/-2/B |  |  |
|  | PAL20L10 |  |  |
| Medium 24X | PAL20X10 |  |  |
| Exclusive-OR | PAL20X8 |  |  |
|  | PAL20X4 |  |  |
|  | PAL20L10A |  |  |
| Medium 24XA | PAL20X10A |  |  |
| Exclusive-OR | PAL20X8A |  |  |
|  | PAL20X4A |  |  |


| Large 24RS Shared Product Terms | PAL20S10 | Under Development |
| :---: | :---: | :---: |
|  | PAL20RS10 |  |
|  | PAL20RS8 |  |
|  | PAL20RS4 |  |
| Large 24A Registered XOR | PAL22RX8A |  |
| Large 24/A Varied XOR | PAL32VX10/A |  |
| Large 24RA Asynchronous | PAL20RA10 |  |
| ECL <br> Combinatorial | PAL10H20P8 |  |
| MegaPAL ${ }^{\text {TM }}$ | PAL32R16 |  |
| Devices | PAL64R32 |  |

Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 20-Pin Device Family

## Valley Data Sciences

Charleston Business Park
2426 Charleston Road
Mountain View, CA 94043
(415) 968-2900


Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL™ Device Families

## Valley Data Sciences

| Series | Part Number | Rev. |
| :---: | :---: | :---: |
| Small 24 Combinatorial | PAL12L10 | 1.03 |
|  | PAL14L8 |  |
|  | PAL16L6 |  |
|  | PAL18L4 |  |
|  | PAL20L2 |  |
|  | PAL20C1 |  |


| Small 24A <br> Decoder | PAL6L16A | Under Development |
| :---: | :--- | :---: | :---: |
|  | PAL8L14A |  |


| $\begin{gathered} \text { Medium 24A/ } \\ 24 A-2 / B \\ \text { Standard } \end{gathered}$ | PAL20L8A/-2/B | 1.03 |
| :---: | :---: | :---: |
|  | PAL20R8A/-2/B |  |
|  | PAL20R6A/-2/B |  |
|  | PAL20R4Al-2/B |  |
| Medium 24X <br> Exclusive-OR | PAL20L10 |  |
|  | PAL20X10 |  |
|  | PAL20X8 |  |
|  | PAL20X4 |  |
| Medium 24XA <br> Exclusive-OR | PAL20L10A |  |
|  | PAL20X10A |  |
|  | PAL20X8A |  |
|  | PAL20X4A |  |
| Large 24RS Shared Product Terms | PAL20S10 |  |
|  | PAL20RS10 |  |
|  | PAL20RS8 |  |
|  | PAL20RS4 |  |
| Large 24A Registered XOR | PAL22RX8A |  |
| Large 24/A PAL32VX10/A |  |  |
| Large 24RA Asynchronous | PAL20RA10 |  |
| ECL Combinatorial | PAL10H20P8 |  |
| MegaPAL ${ }^{\text {TM }}$ Devices | PAL32R16 | 1.04 + 1.1 Adapter |
|  | PAL64R32 | Under Development |

Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

## PAL® Device Programmer Reference Guide

## 20-Pin Device Family

## Varix

1210 E. Campbell Road Richardson, TX 75081
(214) 437-0777

OMNI
Programmer


| Medium <br> 20BP <br> Standard | PAL16L8BP |  |
| :---: | :--- | :--- |
|  | PAL16R8BP |  |
|  | PAL16R6BP |  |
|  | PAL16R4BP |  |


| Medium 20PA <br> Programmable Polarity | PAL16P8A | 3.18 |
| :---: | :---: | :---: |
|  | PAL16RP8A |  |
|  | PAL16RP6A |  |
|  | PAL16RP4A |  |
| Large 20 Arithmetic | PAL16X4 |  |
|  | PAL16A4 |  |
| Large 20RA Asynchronous | PAL16RA8 | Under Development |

Note: The software and hardware revisions listed are the earliest revisions that support these products. Later software and hardware revisions can also be assumed to support these products.

## 24-Pin and MegaPAL™ Device Families

## Varix



Note: The software and hardware revisions listed are the earliest revisions that support these products.
Later software and hardware revisions can also be assumed to support these products.

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# ProPAL ${ }^{\text {M }}$, HAL ${ }^{\circledR}$, and ZHAL ${ }^{\text {TM }}$ Devices: The Logical Solutions for Volume Programmable Logic 

So you have discovered the convenience and flexibility of designing with PAL® devices from Monolithic Memories. You have implemented a design using PAL devices, and taken that design into production. Now may be the time to consider ways of reducing the efforts you put into programming, testing, and marking large volumes of PAL devices. Wouldn't it be more convenient if you could be relieved of the duties and costs of volume programming and testing and still reap the benefits afforded by programmable logic?
Or perhaps you are considering a semicustom product, but you're a little nervous about going to a gate array. Wouldn't it be preferable if you could find a semicustom product which allows easy, inexpensive prototyping, provides fast prototype turnaround, comes fully tested, can have a custom marking, has low NRE charges, provides design flexibility, and has an assured second source?
Well, Monolithic Memories, the inventor of the PAL device, offers the logical solutions. ProPAL, HAL, and ZHAL devices make the transition from user-programmed devices to customized production-ready devices easy and risk free.


## ProPAL Devices

ProPAL (Programmed PAL) devices are simply PAL devices that Monolithic Memories programs and tests for you. You receive a fully functional unit without having to do the programming and testing. But you still have the flexibility to handle design changes easily.


## HAL Devices

HAL (Hard Array Logic) devices are to PAL devices as ROMs are to PROMs. Instead of fuses in the logic array, your pattern is
implemented using metal links that are masked in during wafer fabrication. So your need to program devices is eliminated. And because the devices have their functionality masked in, Monolithic Memories can provide full functional testing before shipping the product. You can place the devices in your boards with a minimum of handling and the highest level of confidence.
Monolithic Memories offers a HAL device for every PAL device. Any PAL device design you program can be implemented in a HAL version, allowing you to move smoothly into volume production.


## ZHAL Devices

Monolithic Memories now provides a third alternative for the programmable logic user: new Zero-Standby-Power CMOS HAL devices.

For the first time there are HAL devices which can implement any pattern from the Series 20 and Series 24 PAL devices with the greatly reduced power consumption only CMOS can offer.
For high complexity designs reaching into the thousands of gates, Zero Power MegaHAL ${ }^{\text {™ }}$ devices provide the natural semicustom VLSI alternative to gate arrays. The MegaPAL ${ }^{\text {m }}$ devices provide the flexibility and fast design turn-around you need for prototyping. Once you are ready for production, the CMOS MegaHAL devices provide the same functionality with Zero Power.
All of the ZHAL devices are fully HC/HCT compatible, making them easy to use in TTL and CMOS environments.

## Should You Use a PAL, ProPAL, or HAL Device?

PAL devices offer the flexibility and convenience needed for prototyping your innovative designs. They provide a means for designing an efficient system by integrating functions and saving you board space. For flexible production, it makes sense to program and test your own PAL devices. This is especially true if you need low volumes per pattern. You always have the option of making last minute design tweaks as you fine tune your system design.

Once your production volumes reach a moderate volume of a few thousand devices per year for each pattern, you may wish to dedicate your production resources to newer designs, instead of programming and testing production volumes. Yet in order to be able to make quick design updates, you might not want to commit to a HAL mask. ProPAL devices provide the ideal solution by eliminating programming and testing needs while retaining enough flexibility to accommodate design changes.
When you feel that your design has stabilized and your volume has ramped up to several thousand devices per year, a HAL device becomes the most cost effective way to purchase our programmable logic. By shifting the burdens to Monolithic Memories, who can handle large volumes easily, you can concentrate your energies on more productive projects.

## How Does MMI Do This?

Monolithic Memories takes your proven PAL device design and either arranges to program ProPAL devices in volume, or generates a custom mask for a HAL or ZHAL device. And all without the normal risks inherent in purchasing a semicustom product. Why? Because:

- You can prototype your system and initiate production using standard Monolithic Memories PAL devices. You don't have to worry about making a mistake that could put your design schedule in jeopardy.
- The nominal Non-Recurring Engineering (NRE) charges for ProPAL and HAL devices are far lower than those normally required for a semicustom circuit. And they can even be amortized over your first production quantity.

- You save on the costs of programming devices. This will also shorten your production cycle, since you can plug the devices into the socket with no additional processing.
- All of the devices are tested for full functionality before they leave Monolithic Memories. You save on the costs of testing and generating test programs.
- Monolithic Memories is geared towards providing volumes of high quality devices. No one knows how to test programmable logic as well as Monolithic Memories. Between the thorough, efficient testing and marking capabilities and the option to provide burn-in for extra reliability, you can obtain a higher quality device that if you did the programming and testing yourself.
- MMI can provide custom marking. This saves you the added expense of stripping the mark from standard devices and then remarking them with your own mark.
- HAL devices are secure by design. If you prefer ProPAL devices, they can also be secured for you at the factory.
- ProPAL device lead time is only 1 to 2 weeks longer than that of unprogrammed PAL devices.
- HAL device turn-around time is a mere 6 to 8 weeks or less from acceptance of your design package to receipt of first units.
- If you find yourself with an unexpected demand, you need not turn away business for lack of HAL device stock. You can always use ProPAL devices to make up for any temporary shortfall.


## How Can You Take Advantage of This?

The following are some guidelines which you can use to help convert your designs to ProPAL, HAL or ZHAL devices.

## 1. Send in Your Design

You will need to provide your logic equations from either PALASM ${ }^{\circledR}$ PALASM 2 or ABEL ${ }^{\text {TM }}$ on magnetic media*.
When Monolithic Memories generates vectors for use in functionally testing your pattern, "seed" vectors are helpful in providing the foundation upon which the final test vectors will be based.
A master PAL device containing your design is needed for Monolithic Memories to verify that the pattern you submitted has been correctly processed. If you cannot provide a Monolithic Memories master PAL device, Monolithic Memories will accept your design inputs and provide ProPAL samples for your approval.
For your convenience, a checklist is included to help you prepare all of the necessary materials to be submitted to Monolithic Memories. This will also help Monolithic Memories process your design, resulting in smoother and faster turn-around. Copies of this form are available from your Sales Representative, or you can simply copy the attached form.

## 2. MMI Will Verify the Design

Upon receiving your design package, Monolithic Memories will enter your design into their computer and verify that there are no format or syntax problems. A fuse map will be generated, and sample ProPAL devices programmed.
If any questions are encountered at this stage, they will be resolved with you before any further processing takes place.

## 3. MMI Will Check the Samples

If you have approved immediate production of your devices, Monolithic Memories will make a fuse for fuse comparison between the samples and the master device you provide. If there are no discrepancies, test generation will be started immediately (or upon receipt of your purchase order).
If you prefer to see programmed sample ProPAL devices prior to initiating production, Monolithic Memories can provide them for your approval before proceeding further. Sample approval is also needed when no master devices are provided or when a discrepancy is found during verification.

## 4. MMI Will Generate Test Vectors

A functional test sequence is generated using TGEN ${ }^{\text {Tw }}$, a proprietary software package. Any seed vectors you provide will be used to help initiate test generation. TGEN will check for hazards and race conditions, monitor fault coverage and systematically add vectors until test coverage goals are met.
Monolithic Memories has a test quality standard that sets as a minimum goal $90 \%$ coverage of all stuck-at faults. Lower coverage patterns can sometimes be processed as HAL devices, or it is possible to handle them as ProPAL devices only, but your approval will be needed. If acceptable coverage cannot be obtained, ways of increasing the testability of the design may have to be considered before Monolithic Memories can process the pattern.
For more detail on exactly how the test coverage is determined, refer to the article "PAL Design Function and Test Vectors" in the Monolithic Memories Programmable Logic Handbook.
When suitable test coverage is obtained, as is normally the case, there is no need for you to be involved with vector generation. If, however, you wish to approve the test vectors before production units are generated, the vectors will be made available to you.

## 5. MMI Will Generate Production Units

After an acceptable test sequence has been generated, Monolithic Memories will generate the appropriate HAL or ZHAL mask and build the devices. Or, in the case of a ProPAL device, Monolithic Memories will arrange to program and test blank units.

[^30]
## Having Your Devices Marked

The standard Monolithic Memories mark consists of the device type, the package type, the date code, and the Monolithic Memories logo.
If you wish, you can have the standard marking replaced by a custom marking. The logo and date code are standard, but any other markings can be as you desire. The character and line limitations for the most common packages are in Table 1.
If the package you want is not listed, your local representative can help you determine the guidelines you need.

## Whom to Contact

When you are ready to put the power of the Monolithic Memories factory to work for you, just contact your local Monolithic Memories sales representative. And let Monolithic Memories take care of your production programming, testing, and marking needs.

Table 1.

| PLASTIC | 20 pin $(300 \mathrm{mil})$ | 2 lines $/ 13$ characters per line |
| :--- | :--- | :--- |
|  | 24 pin $(300 \mathrm{mil})$ | 2 lines $/ 17$ characters per line |
| CERDIP | 20 pin $(300 \mathrm{mil})$ | 2 lines $/ 16$ characters per line |
|  | 24 pin $(300 \mathrm{mil})$ | 2 lines $/ 17$ characters per line |
| PLCC | 20 lead | 4 lines $/ 11$ characters per line |
|  | 28 lead | 5 lines $/ 12$ characters per line |



# Zero Power CMOS Hard Array Logic ZHAL" ${ }^{\text {20 }}$ 20A Series 

Patent Pending

## Features/Benefits

- Zero standby power
- 25-ns maximum propagation delay
- HC and HCT compatible
- Space saving PLCC available
- Low power alternative for Small and Medium 20-pin PAL® devices, including 16L8/16R8/16R6/16R4


## Description

The Zero Power Hard Array Logic (ZHAL) devices are ideal in low-power applications that require high-speed operation. These attributes are achieved through the use of Monolithic Memories' advanced high-speed CMOS process. Now system designers have the option of using a ZHAL device that matches fast PAL device speeds, but with the added advantage of zero standby power. These features are ideal for power-critical areas such as portable digital equipment or lap-top computers.
This family of ZHAL devices utilizes a unique architecture that is designed for a high degree of flexibility in implementing most patterns of the listed 20-pin PAL/HAL® devices. Prototyping can be done using standard PAL devices before converting to ZHAL circuits for production. ZHAL devices are fabricated by Monolithic Memories with custom metallization masks defined by a user-supplied HAL Design Specification.

The procedures for designing with Monolithic Memories' ZHAL devices are shown in the flow chart on page 8. The ZHAL20 option in the PALASM ${ }^{\oplus} 2$ CAD package will confirm whether a design specification will fit within the ZHAL20 architecture. For more information on the ZHAL20 software, refer to the PALASM 2 User Manual. For more information on the ZHAL device generation flow, see the Monolithic Memories brochure "ProPAL"', HAL®, and ZHAL Devices."
For evaluation of the ZHAL2OA circuit, sample patterns are available. See page 6 for details.

## Ordering Information

| PART NUMBER | PACKAGE | ARRAY | OUTPUTS |  |
| :---: | :---: | :---: | :---: | :---: |
|  |  |  | COMB | REG |
| ZHAL10H8A |  | 10 | 8 | - |
| ZHAL12H6A |  | 12 | 6 | - |
| ZHAL14H4A |  | 14 | 4 | - |
| ZHAL16H2A |  | 16 | 2 | - |
| ZHAL16C1A |  | N, NL | 16 | 2 |
| ZHAL10L8A |  | 10 | 8 | - |
| ZHAL12L6A |  | 12 | 6 | - |
| ZHAL14L4A |  | 14 | 4 | - |
| ZHAL16L2A |  | 16 | 2 | - |
| ZHAL16L8A |  | 16 | 8 | - |
| ZHAL16R8A |  | 16 | - | 8 |
| ZHAL16R6A |  | NL | 16 | 2 |
| ZHAL16R4A |  | 16 | 4 | 4 |
| ZHAL16P8A |  | 16 | 8 | - |
| ZHAL16RP8A |  | 16 | - | 8 |
| ZHAL16RP6A | N, NL | 16 | 2 | 6 |
| ZHAL16RP4A |  | 16 | 4 | 4 |





## Operating Conditions

| SYMBOL | PARAMETER |  |  | USTR | IAL |  | MMER | $\overline{S I A L}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| ${ }^{\text {tw }}$ | Width of clock | 16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A | 15 | 10 |  | 15 | 10 |  | ns |
| ${ }^{\text {tsu }}$ | Setup time from input or feedback to clock |  | 20 | 13 |  | 20 | 13 |  | ns |
| $t_{\text {h }}$ | Hold time |  | 0 | -10 |  | 0 | -10 |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -40 | 25 | 85 | 0 | 25 | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions



## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS (See Test Load) |  | $\begin{aligned} & \text { USTF } \\ & \text { TYP } \end{aligned}$ | AL MAX |  | $\begin{aligned} & \text { AMER } \\ & \text { TYP } \end{aligned}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPD }}$ | Input or feedback to output 10H8A, 12H6A, 14H4A, 16H2A, 16C1A, 10L8A, 12L6A, 14L4A 16L2A, 16L8A, 16R6A, 16R4A, 16P8A, 16RP6A, 16RP8A |  | $\begin{aligned} & R_{\mathrm{L}}=1 \mathrm{~K} \Omega \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | 15 | 25 |  | 15 | 25 | ns |
| ${ }^{\text {t CLK }}$ | Clock to output or feedback 16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A |  |  |  | 10 | 15 |  | 10 | 15 | ns |
| ${ }^{\text {t }}$ PZX | Input to output enable | 16L8A, 16R4A, 16R6A, 16P8A, 16RP4A, 16RP6A |  |  | 12 | 25 |  | 12 | 25 | ns |
| ${ }^{t} P X Z^{6}$ | Input to output disable |  |  |  | 14 | 25 |  | 14 | 25 | ns |
| $\begin{aligned} & \mathrm{t}_{\mathrm{P} X Z} \\ & \mathrm{t}_{\mathrm{P} Z X} \end{aligned}$ | Pin 11 to output disable/enable | 16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A |  |  | 12 | 15 |  | 12 | 15 | ns |
| ${ }_{\text {f MAX }}$ | Maximum frequency |  |  | 28.5 | 40 |  | 28.5 | 40 |  | MHz |

Notes: Apply to electrical and switching characteristics.

1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Pin 8 (PRELOAD pin). Applies to all devices whether registered or non-registered. 3. JEDEC standard no. 7 for high-speed CMOS devices.
3. Disable output pins $=\mathrm{V}_{\mathrm{CC}}$ or GND . 5. Add 3 mA per additional 1.0 MHz of operation over $1 \mathrm{MHz} . \quad 6 . \quad \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$.

## Absolute Maximum Ratings

Supply voltage, $\mathrm{V}_{\mathrm{CC}}$ ..... -0.5 V to 7 V
DC input voltage, $\mathrm{V}_{\mathrm{I}}$ ..... -0.5 V to $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$
DC output voltage, $\mathrm{V}_{\mathrm{O}}$ ..... -0.5 V to $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$
DC output source/sink current per output pin, IO ..... $\pm 35 \mathrm{~mA}$
DC VCC or ground current, ICC or IGND ..... $\pm 100 \mathrm{~mA}$
Input diode current, IIK:
$V_{1}<0$ ..... $-20 \mathrm{~mA}$
$V_{1}>V_{C C}$ ..... $+20 \mathrm{~mA}$
Output diode current, loK:
$\mathrm{V}_{\mathrm{O}}<0$ ..... $-20 \mathrm{~mA}$
$\mathrm{V}_{\mathrm{O}}>\mathrm{V}_{\mathrm{CC}}$ ..... $+20 \mathrm{~mA}$
Storage temperature ..... $-65^{\circ} \mathrm{C}$ to $150^{\circ} \mathrm{C}$

## Switching Test Load



Notes: 1. CL includes probe and jig capacitance.
2. When measuring ${ }^{t_{P L Z}}$ and ${ }^{{ }_{P P L}}, S 1$ is tied to $V_{C C}$. When measuring $t_{\mathrm{PHZ}}$ and $\mathrm{t}_{\mathrm{PZH}}, \mathrm{S} 1$ is tied to ground. ${ }^{t} P Z X$ is measured with $C_{L}=50 \mathrm{pF}$. $\mathrm{t}_{\mathrm{PXZ}}$ is measured with $\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$. When measuring propagation delay times of 3-state outputs, S 1 is open, i.e., not connected to $V_{C C}$ or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

## Output Register PRELOAD $\dagger$

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of state sequencer designs by allowing direct setting of output states for improved test coverage. The procedure for PRELOAD is as follows:

1. Raise $V_{C C}$ to 4.5 V .
2. Disable output registers by setting pin 11 to $\mathrm{V}_{\mathrm{IH}}$. Set pin 1 to 0 V .
3. Apply $\mathrm{V}_{\mathrm{iL}} / \mathrm{V}_{\mathrm{IH}}$ to all registered output pins.
4. Pulse pin 8 to $\mathrm{V}_{\mathrm{p}}(12 \mathrm{~V})$, then back to 0 V .
5. Remove $\mathrm{V}_{\mathrm{IL}} / \mathrm{V}_{\mathrm{IH}}$ from all registered output pins.
6. Lower pin 11 to $V_{I L}$ to enable the output registers.
7. Verify for $\mathrm{V}_{\mathrm{OL}} / \mathrm{V}_{\mathrm{OH}}$ at all registered output pins.
$\dagger$ Note: Only applies to parts with output registers.
Typical $\mathrm{t}_{\text {sup }}=50 \mathrm{~ns}$
$\mathrm{t}_{\mathrm{wp}}=100 \mathrm{~ns}$
thp $=50 \mathrm{~ns}$
$I_{H}=30 \mu \mathrm{~A}(\operatorname{Pin} 8)$

Enable/Disable Delay


## Schematic of Inputs and Outputs



## Features/Benefits

- Demonstrates all features of ZHAL20A product
- 4-bit up/down counter with reset
- 3-bit shifter
- 25-ns maximum propagation delay
- Zero standby power


## Description

The ZHAL20A Evaluation Pattern is provided as an example of the features and characteristics of the ZHAL20A Series products.
This design consists of two functionally independent patterns: a 4 -bit up/down counter and a 3-bit shifter. The 4-bit counter can count up or count down and has reset capability. These features are controlled by two control signals: UP and CNTRSET (Count Reset). When UP is high, the counter counts up. When UP is low, the counter counts down. CNTRSET overrides the count function and resets the counter to all ones, synchronous with the clock.
The 3-bit shifter shifts data bits by 0,1 or 2 positions. The three bits of the shifter are enabled when EN (enable) is high, and are disabled (high-Z) when EN is low.
The PALASM ${ }^{\circledR 2}$ 2 software file and simulation results are shown on the next page. Below are the function tables that summarize the functions of the counter and the shifter.

## Counter Function Table

| $\overline{\mathbf{O E}}$ | UP | CNTRSET | CLK | Q3-Q0 | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :--- |
| H | X | X | X | Z | High-Z |
| L | H | L | † | Q plus 1 | Increment |
| L | L | L | † | Q minus 1 | Decrement |
| L | X | H | † | High | Reset |

$\mathrm{H}=\mathrm{HIGH}$ voltage level
$L=$ LOW voltage level
$\mathrm{X}=$ Don't care
$Z=$ High impedance (off) state
1 = LOW-to-HIGH clock transition

## Logic Symbol



## Shifter Function Table

| EN | 11 | 10 | Y2 | Y1 | Y0 | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| L | X | X | Z | Z | Z | High-Z |
| $H$ | L | L | $\overline{\mathrm{D} 2}$ | $\overline{\mathrm{D} 1}$ | $\overline{\mathrm{D} 0}$ | No operation |
| $H$ | L | H | $\overline{\mathrm{D} 0}$ | $\overline{\mathrm{D} 2}$ | $\overline{\mathrm{D} 1}$ | Shift by one |
| $H$ | $H$ | L | $\overline{\mathrm{D} 1}$ | $\overline{\mathrm{D} 0}$ | $\overline{\mathrm{D} 2}$ | Shift by two |

## PALASM Design Specification



## Simulation Results

PALASM SIMULATION HISTORY LISTING
ZZZ

|  |  |  | cgcgcgegeg |  |
| :---: | :---: | :---: | :---: | :---: |
| CLK | LLLLHLLHLL | HLLHLHLHLH | LHLHLHLHLH | LHLHLHLHL |
| IO | XXLLLLLLLLH | HHLLLLLLLL | LLLLLLLLLLL | LL |
| Il | XXLLLLLLLLL | LLHHHHHHHH | HHHHHHHHHH | HHHHHHHH |
| DO | XXLLLLLLLLH | HHLLLLLLLL | LLLLLLLLLL | LLLLLLLLL |
| D1 | XXLLLLLLLLL | LLHHHHHHHH | нНННННННН | HH |
| D2 | XXLLLLLLLLH | HHLLLLLLLL | LLLLLL | LLLLLLLLL |
| EN | LLHHHHHHHH | нНнНнHHHHH | HHHHHHHHHH | HHHHHH |
| UP | XXXXXXHHHH | HHHHHHHHHH | HHHHHHHHHH | HHHHHHHHH |
| CNTRSET | XXHHHHLLLL | LLLLLLLLLL | LLLLLLLLLL | LLLLLLLLL |
| GND | LLLLLLLLLL | LLLLLLLLL | LLLL | L |
| /OE | HHLLLLLLLLL | LLLLLLLL | LLLL | LLLLLLLI |
| Y2 | XZHHHHHHHL | LLLLLLLLLL | LLLLLLLLL | LLL |
| Q1 | ZZXXXHHHLL | LLLLHHHHLL | LLHHHHLLLL | HHHHLLL |
| Q2 | Z2XXXHHHLL | LLLLLLLLHH | HHHHHHLLLL | LLLLHHHHH |
| Q3 | ZZXXXHHHLL | LLLLLLLLLL | LLLLLLHHHH | HHHHHHHHH |
| Q0 | ZZXXXHHHLL | LHHHLLHHLL | HHLLHHLLHH | LLHHLIHHL |
| Y1 | XZHHHHHHHL | LLHHHHHHHH | HHHHHHHHH | HH |
| Yo | XZHHHHHHH | HHHHHHH |  |  |
| Vcc |  |  |  |  |

## Simulation File

SIMULATION
TRACE_ON CLK IO I1 DO D1 D2 EN UP CNTRSET /OE Y2 Q1 Q2 Q3 QO Y1 Yo SETF/CLK /OE/EN

SETF OE EN /II /IO /D2 /D1 /DO Y2 Y1 YO CNTRSET CLOCKF CLK

CHECK Q3 Q2 Q1 QO
SETF /II /IO /D2 /D1 /DO Y2 Y1 YO /CNTRSET UP CLOCKF CLK

CHECK /Q3 /Q2 /Q1/QO
SETF /I1 IO D2 /D1 DO /Y2 /Y1 YO
CLOCKF CLK
CHECK /Q3 /Q2 /Q1 QO
SETF II /IO /D2 D1 /DO /Y2 Y1 YO
CLOCKF CLK
CHECK /Q3 /Q2 Q1/QO
SETF OE /CNTRSET UP
CLOCKF CLK
CHECK /Q3 /Q2 Q1 QO
SETF OE /CNTRSET UP CLOCKF CLK
CHECK /Q3 Q2/Q1/Q0
SETF OE /CNTRSET UP
CLOCKF CLK CLOCKF CLK
CHECK /Q3 Q2 /Q1 QO
SETF OE/CNTRSET UP CLOCKF CLK
CHECK /Q3 Q2 Q1 /QO
SETF OE/CNTRSET UP CLOCKF CLK
CHECK /Q3 Q2 Q1 QO
SETF OE/CNTRSET UP CLOCKF CLK
CHECK Q3 /Q2/Q1/QO
SETF OE /CNTRSET UP CLOCKF CLK
CHECK Q3 /Q2 /Q1 QO
SETF OE/CNTRSET UP CLOCKF CLK
CHECK Q3 /Q2 Q1/QO
SETF OE /CNTRSET UP CLOCKF CLK

CHECK Q3/Q2 Q1 QO
SETF OE /CNTRSET UPं CLOCKF CLK
CHECK Q3 Q2/Q1/Q0
SETF OE/CNTRSET UP CLOCKF CLK
CHECK Q3 Q2/Q1 QO
SETF OE/CNTRSET UP CLOCKF CLK

CHECK Q3 Q2 Q1/QO
TRACE_OFF

## ZHAL 20A Device Generation Flow




Please complete this form for each pattern submitted to Monolithic Memories, and include it in your design package.
Submitted by: $\qquad$ Date:
Title: $\qquad$


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## System Building Blocks/HMSI Selection Guide

| FUNCTION | PART NUMBER |
| :--- | :--- |
| 8-Bit Counter | SN54/74LS461A |
| 8-Bit Up/Down Counter | SN54/74LS469A |
| 10-Bit Counter | SN54/74LS491A |
| 16:1 Mux | SN54/74LS450 |
| Dual 8:1 Mux | SN54/74LS451 |
| Quad 4:1 Mux | SN54/74LS453 |
| Increment and Skip Counter | 671492 |
| 2-Digit BCD Counter | 671493 |
| 8-Bit Priority Encoder <br> with Register | $5 / 671494$ |

## 8-Bit Counter SN54/74LS461A

## Features/Benefits

- 8-bit counter for microprogram-counter, DMA-controller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8-bit increments


## Description

The 'LS461A is an 8-bit synchronous counter with parallel load, clear, and hold capability. Two function select inputs (IO, I1) provide one of four operations which occur synchronously on the rising edge of the clock (CK).
The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The CLEAR operation resets the output register to all LOWs. The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ( $\overline{\mathrm{Cl}}=\mathrm{LOW})$, otherwise the operation is a HOLD. The carry-out $(\overline{\mathrm{CO}})$ is TRUE $(\overline{\mathrm{CO}}=$ LOW $)$ when the output register $\left(Q_{7}-Q_{0}\right)$ is all HIGHs, otherwise FALSE $(\overline{\mathrm{CO}}=\mathrm{HIGH})$.
The data output pins are enabled when $\overline{\mathrm{OE}}$ is LOW, and disabled (HI-Z) when $\overline{\mathrm{OE}}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.
Two or more'LS461A 8-bit counters may be cascaded to provide larger counters. The operation codes were chosen such that when 11 is HIGH, 10 may be used to select between LOAD and INCREMENT as in a program counter (JUMP/INCREMENT).

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN54LS461A | JS, W, 28L | Mil |
| SN74LS461A | NS, JS | Com |

## Logic Symbol



## Function Table

| $\overline{\mathbf{O E}}$ | CK | I1 | IO | CI | D7-D0 | Q7-Q0 | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| H | ${ }^{*}$ | * $^{*}$ | ${ }^{*}$ | ${ }^{*}$ | ${ }^{*}$ | Z | HI-Z |
| L |  | L | L | L | X | X | L |
| CLEAR |  |  |  |  |  |  |  |
| L | 1 | L | H | X | X | Q | HOLD |
| L |  |  | H | L | X | H | H |
| D | X | Q | HOAD |  |  |  |  |
| H |  | H | H | L | X | Q plus 1 | INCREMENT |

* When $\overline{\mathrm{OE}}$ is HIGH, the three-state outputs are disabled to the high-impedance states; however, sequential operation of the counter is not affected.


## Logic Diagram

8-Bit Counter


## Absolute Maximum Ratings


Input voltage ..................................................................................................................... 5.5 V


Operating Conditions

| SYMBOL | PARAMETER |  |  | ILITA |  |  | MMER | IAL | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP $\dagger$ | MAX | MIN | TYP $\dagger$ | MAX | UNIT |
| VCC | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| TA | Operating free-air temperature |  | -55 |  | 125* | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of clock | Low | 35 | 15 |  | 25 | 15 |  | ns |
|  |  | High | 20 | 7 |  | 15 | 7 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time |  | 40 | 20 |  | 30 | 20 |  |  |
| th | Hold time |  | 0 | -15 |  | 0 | -15 |  | ns |

* Case temperature


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{* *}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{* *}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | I $=-18$ |  |  | -0.8 | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4$ |  |  | -0.02 | 0.25 | mA |
| IIH | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4$ |  |  |  | 25 | $\mu \mathrm{A}$ |
| $1 /$ | Maximum input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=5.5$ |  |  |  | 1 | mA |
|  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Mil | $\mathrm{IOL}=12 \mathrm{~mA}$ |  |  |  |  |
| VoL | w-level output voltag | $V_{I H}=2 \mathrm{~V}$ | Com | $\mathrm{IOL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | $\checkmark$ |
|  |  | $V_{C C}=\mathrm{MIN}$ | Mil | $\mathrm{IOH}=-2 \mathrm{~mA}$ |  |  |  |  |
| V OH | High-level output voltage | $\begin{aligned} & V_{I L}=0.8 \\ & V_{1 H}=2 \mathrm{~V} \\ & \hline \end{aligned}$ | Com | $\mathrm{IOH}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| IOZL |  | $V_{C C}=M A X$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu$ |
| IOZH | Off-state output current | $V_{I H}=2 \mathrm{~V}$ |  | $\mathrm{VO}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| los | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ICC | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  |  | 140 | 180 | mA |

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$* * V_{I L}$ and $V_{I H}$ parameters are, in effect, input conditions of $D . C$. and functional output $\dagger$ All typical values are at $V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}$ tests are not directly tested. $\mathrm{V}_{\mathrm{IL}}$ is specified at $\leq 0.8 \mathrm{~V}$ and $\mathrm{V}_{I H}$ is specified at $\geq 2.0 \mathrm{~V}$.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MILITARY <br> MIN TYP $\dagger$ MAX |  |  | COMMERCIAL MIN TYP $\dagger$ MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{f}_{\mathrm{MAX}}$ | Maximum clock frequency* | Commercial$\mathrm{R}_{1}=200 \Omega$ | 16.6 |  |  | 25 |  |  | MHz |
| tpD | Cl to CO delay |  |  | 15 | 35 |  | 15 | 25 | ns |
| tCLK | Clock to Q | $\mathrm{R}_{2}=390 \Omega$ |  | 10 | 25 |  | 10 | 15 | ns |
| tPD | Clock to CO | Military |  | 25 | 60 |  | 25 | 40 | ns |
| tpZX | Output enable delay | $\mathrm{R}_{1}=390 \Omega$ |  | 11 | 25 |  | 11 | 20 | ns |
| tPXZ | Output disable delay | $\mathrm{R}_{2}=750 \Omega$ |  | 10 | 25 |  | 10 | 20 | ns |

${ }^{{ }^{f}}{ }_{\text {MAX }}$ is derived from: $1 /$ MAX $\left[\left(t_{\text {su }}+t_{h}\right), t_{w}\right.$ (Low) ${ }^{+t_{w}}$ (High), $\left.t_{C L K}\right]$.

Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation

OUTPUT


Notes: 1

1. ${ }^{\text {tPD }}$ is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level
2. $t_{P Z X}$ is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
3. tpXZ is tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{VOL}^{+}+0.5 \mathrm{~V}$ output level.

## Application

16-Bit Counter


# 8-Bit Up/Down Counter SN54/74LS469A 

## Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMAcontroller and general-purpose counting applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading
- Expandable in 8 -bit increments


## Description

The 'LS469A is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs $\overline{(L D}, \overline{U D}, \overline{\mathrm{CBI}})$ provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D7-D0) into the output register (Q7-Q0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ( $\overline{\mathrm{CBI}}=\mathrm{LOW}$ ), and the up/down control line ( $\overline{\mathrm{UD}}$ ) is LOW, otherwise the operation is a HOLD. The carry-out ( $\overline{\mathrm{CBO}})$ is TRUE ( $\overline{\mathrm{CBO}}=\mathrm{LOW}$ ) when the output register (Q7-Q0) is all HIGHs, otherwise FALSE $(\overline{\mathrm{CBO}}=\mathrm{HIGH})$. The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ( $\overline{\mathrm{CBI}}=1.0 \mathrm{~W}$ ), and the up/down control line ( $\overline{\mathrm{UD}}$ ) is HIGH, otherwise the operation is a HOLD. The borrow-out $(\overline{\mathrm{CBO}})$ is TRUE $(\overline{\mathrm{CBO}}=\mathrm{LOW})$ when the output register (Q7-QO) is all LOWs, otherwise FALSE $(\overline{\mathrm{CBO}}=\mathrm{HIGH})$.
The data output pins are enabled when $\overline{O E}$ is LOW, and disabled (HI-Z) when $\overline{\mathrm{OE}}$ is HIGH . The output drivers will sink the 24 mA required for many bus-interface standards. Two or more'LS469A 8 -bit up/down counters may be cascaded to provide larger counters.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN54LS469A | JS, W, 28L | Mil |
| SN74LS469A | NS, JS | Com |

## Logic Symbol



## Function Table

| $\overline{\text { OE }}$ | CK | $\overline{\text { LD }}$ | $\overline{\text { UD }}$ | CBI | D7-D0 | Q7-Q0 | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| H | * | * | * | * | * | Z | HI-Z* |
| L | $\dagger$ | L | X | X | D | D | LOAD |
| L | 1 | H | L | H | X | Q | HOLD |
| L | 1 | H | L | L | X | Q plus 1 | INCREMENT |
| L | 1 | H | H | H | X | Q | HOLD |
| L | 1 | H | H | L | X | Q minus 1 | DECREMENT |

* When $\overline{O E}$ is HIGH, the three-state outputs are disabled to the high-impedance state; however, sequential operation of the counter is not affected.

Logic Diagram


## Absolute Maximum Ratings

| Supply voltage $V_{C C}$ | 7.0 V |
| :---: | :---: |
| Input voltage | 5.5 V |
| Off-state output voltage | 5.5 V |
| Storage temperature | $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$ |
| Operating Conditions |  |


| SYMBOL | PARAMETER |  |  | LITAR |  |  | MMER | =IAL | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP $\dagger$ | MAX | MIN | TYP $\dagger$ | MAX | UNT |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 125* | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{\text {w }}$ | Width of clock | Low | 35 | 15 |  | 25 | 15 |  | ns |
|  |  | High | 20 | 7 |  | 15 | 7 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time |  | 40 | 20 |  |  | 20 |  | ns |
| th | Hold time |  | 0 | -15 |  | 0 | -15 |  |  |

* Case temperature


## Electrical Characteristics over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}{ }^{* *}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{VIH}^{* *}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | I $=-18$ |  |  | -0.8 | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=0.4$ |  |  | -0.02 | 0.25 | mA |
| 1 H | High-level input current | $V_{C C}=M A X$ | $V_{1}=2.4$ |  |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=$ MAX | $V_{1}=5.5$ |  |  |  | 1 | mA |
|  |  | $V_{C C}=$ MIN | Mil | $\mathrm{IOL}=12 \mathrm{~mA}$ |  |  |  |  |
|  |  | $V_{I H}=2 \mathrm{~V}$ | Com | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  |  |  |
|  |  | $\mathrm{VCC}=\mathrm{MIN}$ | Mil | $1 \mathrm{OH}=-2 \mathrm{~mA}$ |  |  |  |  |
| VOH | High-level output voltage | $\begin{aligned} & V_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | Com | $\mathrm{IOH}=-3.2 \mathrm{~mA}$ | 2.4 | 2.8 |  | V |
| IOZL |  | $V_{C C}=$ MAX |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 |  |
| IOZH |  | $V_{I H}=2 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 |  |
| IOS | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -70 | -130 | mA |
| ICC | Supply current | $V_{C C}=$ MAX |  |  |  | 140 | 180 | mA |

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
${ }^{*} V_{I L}$ and $V_{I H}$ parameters are, in effect, input conditions of D.C. and functional output $\dagger$ All typical values are at $V_{C C}=5 \mathrm{~V}, T_{A}=25^{\circ} \mathrm{C}$. tests are not directly tested. $\mathrm{V}_{\mathrm{IL}}$ is specified at $\leq 0.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{IH}}$ is specified at $\geq 2.0 \mathrm{~V}$.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MILITARY |  | COMMERCIAL |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN TYP $\dagger$ | MAX | MIN TYP $\dagger$ |  |  |
| $\mathrm{f}_{\mathrm{MAX}}$ | Maximum clock frequency* | Commercial$\mathrm{R}_{1}=200 \Omega$ | 16.6 |  | 25 |  | MHz |
| tPD | Cl to CO delay |  | 15 | 35 | 15 | 25 | ns |
| tCLK | Clock to Q | $\mathrm{R}_{2}=390 \Omega$ | 10 | 25 | 10 | 15 | ns |
| tpD | Clock to CO | Military | 25 | 60 | 25 | 40 | ns |
| tpZX | Output enable delay | $\mathrm{R}_{1}=390 \Omega$ | 11 | 25 | 11 | 20 | ns |
| tPXZ | Output disable delay | $\mathrm{R}_{2}=750 \Omega$ | 10 | 25 | 10 | 20 | ns |

${ }^{{ }^{f}}{ }_{\text {MAX }}$ is derived from: $1 /$ MAX $\left[\left(t_{s u}+t_{h}\right), t_{w}(\right.$ Low $) ~+t_{w}$ (High),$\left.t_{\text {CLK }}\right]$.

## Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation


Notes:

1. tPD is tested with switch $S_{1}$ closed. $C_{L}=50 \mathrm{pF}$ and measured at 1.5 V output level
2. $\mathrm{t}_{\mathrm{PZX}}$ is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to" 1 " test, and closed for high impedance to " 0 " test.
3. ${ }^{\mathrm{t}} \mathrm{PXZ}$ is tested with $\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}{ }^{-0.5} \mathrm{~V}$ output level: $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Application

16-Bit Up/Down Counter

BUS OUT ENABLE

COUNT ENABLE

$$
\begin{array}{r}
\frac{C K}{L D} \\
\text { POL } \\
\text { 16-BIT } \\
\text { DATA BUS }
\end{array}
$$

IN



## 10-Bit Counter <br> SN54/74LS491A

## Features/Benefits

- CRT vertical and horizontal timing generation
- Bus-structured pinout
- 24-pin SKINNYDIP® ${ }^{\circledR}$ saves space
- Three-state outputs drive bus lines
- Low-current PNP inputs reduce loading


## Ordering Information

tion adds one to the output of the register when the count up input is asserted ( $\overline{U P}=$ LOW). The COUNT DOWN operation subtracts one from the output register when the count up input is not asserted $(\overline{U P}=\mathrm{HIGH})$. SET overrides both LOAD and COUNT, LOAD overrides COUNT, and COUNT is conditional on CARRY IN.
The data output pins are enabled when $\overline{\mathrm{OE}}$ is LOW, and disabled ( $\mathrm{HI}-\mathrm{Z}$ ) when $\overline{\mathrm{OE}}$ is HIGH . The $24-\mathrm{mA}$ IOL outputs are suitable for driving RAM/PROM address lines in video graphics systems.

## Logic Symbol



| PART <br> NUMBER | TEMP | PACKAGE | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| SN54LS491A | Mil | $\mathrm{JS}, \mathrm{W}, \mathrm{L}(28)$ | 10.5 MHz Counter |
| SN74LS491A | Com | NS,JS,NL(28) | 25 MHz Counter |



Function Table

| $\overline{\text { OE }}$ | CK | SET | LD | $\overline{\text { CNT }}$ | $\overline{\text { CIN }}$ | $\overline{\mathrm{UP}}$ | D9-D0 | Q9-Q0 | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| H | * | * | * | * | * | * | * | Z | HI-Z* |
| L | $\dagger$ | H | X | X | X | X | X | H | SET all HIGH |
| L | 1 | L | L | X | X | X | D | D | LOAD D |
| L | $\dagger$ | L | H | H | X | $x$ | $x$ | Q | HOLD |
| L | $\dagger$ | L | H | L | H | X | X | Q | HOLD |
| L | $\dagger$ | L | H | L | L | L | X | Q plus 1 | COUNT UP |
| L | $\dagger$ | L | H | L | L | H | X | Qminus 1 | COUNT DN |

* When $\overline{\mathrm{OE}}$ is HIGH, the three-state outputs are disabled to the high-inpedance states; however, sequential operation of the counter is not affected.


## Description

The 'LS491/A is a 10-bit up/down counter with set, load and hold capabilities for two LSB, two MSB and six middle bits that are HIGH or LOW as a group. Five control inputs (SET, $\overline{\mathrm{LD}}$, $\overline{\mathrm{CNT}}, \overline{\mathrm{CIN}}$ and $\overline{\mathrm{UP}}$ ) provide one of five operations which occur synchronously on the rising edge of the clock (CK).
The SET operation sets the output register (Q9-Q0) to all HIGHs. The LOAD operation loads the inputs (D9-D0) into the register. When COUNT or CARRY IN are not asserted ( $\overline{\mathrm{CNT}}=$ HIGH or $\overline{\mathrm{CIN}}=\mathrm{HIGH}$ ), the HOLD operation holds the previous value regardless of clock transitions. The COUNT UP opera-

## Logic Diagram



## Absolute Maximum Ratings


Input voltage ............................................................................................................................. 5.5 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V


## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | COMMERCIAL TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of clock | High | 15 | 7 |  | ns |
|  |  | Low | 25 | 15 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time |  | 30 | 20 |  | ns |
| $t_{\text {h }}$ | Hold time |  | 0 | -15 |  | ns |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}{ }^{\text {* }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{\text {* }}$ | High-level input voltage |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| ILL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | 0.25 | mA |
| $\mathrm{I}_{\mathrm{H}}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=\mathrm{MIN} \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $1 \mathrm{OH}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
| IOZL | -state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{\text {I OZH }}$ | Off-state output current | $V_{I H}=2 V$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 | $\mu \mathrm{A}$ |
| 'Os** | Output short-circuit current | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 |  | -130 | mA |
| ${ }^{\text {cce }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 120 | 180 | mA |

* $V_{I L}$ ad $V_{I H}$ parameters are. in effect. input conditions of D.C. and Functional output tests and are not directly tested. $V_{I L}$ is specified at 0.8 V , and $\mathrm{V}_{I H}$ is specified at 20 V .
** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
$\dagger$ All typical values are set at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} . \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load) | MILITARY MIN TYP $\dagger$ MAX |  |  | COMMERCIAL MIN TYP $\dagger$ MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum counting frequency** | Commercial <br> $R_{1}=200 \Omega$ <br> $R_{2}=390 \Omega$ <br> Mil <br> $R_{1}=390 \Omega$ <br> $R_{2}=750 \Omega$ | 15.3 |  |  | 25 |  |  | MHz |
| ${ }^{\text {t CLK }}$ | Clock to Q |  |  | 10 | 25 |  | 10 | 15 | ns |
| ${ }^{\text {tPZX }}$ | Output enable delay |  |  | 11 | 25 |  | 11 | 20 | ns |
| ${ }_{\text {t P X }}$ | Output disable delay |  |  | 10 | 25 |  | 10 | 20 | ns |

** ${ }_{\mathrm{f}}^{\mathrm{MAX}}$ is derived from: $1 / \mathrm{MAX}\left[\left(\mathrm{t}_{\mathrm{su}}+\mathrm{t}_{\mathrm{h}}\right), \mathrm{t}_{\mathrm{w}}(\mathrm{High})+\mathrm{t}_{\mathrm{w}}\right.$ (Low), $\left.\mathrm{t}_{\text {CLK }}\right]$.
Test Load


[^31]Noles 1. tpD is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level
2. tPZX is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}} 50 \mathrm{pF} \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test
3. tPXZ is tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level: $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Application

## Video Horizontal Timing and Blanking



## Timing Analysis:

Path 1 - Outputs of 74LS491A setting up at PAL16R4A
${ }^{t}{ }^{\text {PD }}$ CK-Q/74LS491A ${ }^{+t} U_{P A L 16 R 4 A}=15 n s+25 n s=40 n s$
Path 2 - Outputs of PAL16R4A setting up at 74LS491A inputs

$$
{ }^{{ }^{P} D_{C K-Q / P A L 16 A ~}}+{ }^{+} \mathrm{SU}_{74 L S 491 A}=25 \mathrm{~ns}+30 \mathrm{~ns}=55 \mathrm{~ns}
$$

Accordingly, the worst-case timing of the two paths is $55-\mathrm{ns}$, which results in a maximum video dot clock frequency of 18.18 MHz . Strict interpretation of the 60 Hz field rate NTSC Standard suggests that up to $52.1 \mu \mathrm{sec}$ of time is available for active-raster-line duration. In practice however, most CRT monitors
overscan the screen to correct horizontal sweep nonlinearities. As a consequence, the horizontal blanking time is increased, and the active video time decreased, typically to about $40 \mu \mathrm{sec}$. For the application circuit shown above, over 512 dots (pixels) for one line can be displayed:

$$
\frac{40 \mu \mathrm{sec} \text { per line }}{55 \mathrm{~ns} \text { per pixel per line }}=727 \text { pixels }
$$

Normally, at least a 10 -bit counter is required to provide a video timing chain for such resolutions. The 74LS491A combined with a high-speed PAL® (PAL16R4A) is capable of generating a complete set of video timing signals. Note that in the application circuit, the maximum horizontal count [HMAX ( $n-1$ )] is decoded one clock early, due to the 1 -level pipelining used to obtain circuit speed.

## 16:1 Mux

SN54/74LS450

## Features/Benefits

- 24-pin SKINNYDIP® ${ }^{\circledR}$ saves space
- Similar to SN5/74150
- Low-current PNP inputs reduce loading


## Ordering Information

| PART NUMBER | PACKAGE |  | TEMPERATURE |
| :---: | :---: | :---: | :---: |
| SN54LS450 | JS, W | 28 L | IMil |
| SN74LS450 | NS, JS |  | Com |

## Logic Symbol



## Function Table

| $\begin{aligned} & \text { INPUT } \\ & \text { SELECT } \end{aligned}$ |  |  |  | OUTPUT <br> W Y |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| D | C | B | A |  |  |
| L | L | L | L | EO | E0 |
| L | L | L | H | $\overline{\mathrm{E} 1}$ | E1 |
| L | L | H | L | E2 | E2 |
| L | L | H | H | E3 | E3 |
| L | H | L | L | E4 | E4 |
| L | H | L | H | $\overline{\text { E5 }}$ | E5 |
| L | H | H | L | $\overline{\mathrm{E} 6}$ | E6 |
| L | H | H | H | E7 | E7 |
| H | L | L | L | $\overline{\mathrm{E}}$ | E8 |
| H | L | L | H | E9 | E9 |
| H | L | H | L | $\overline{\mathrm{E} 10}$ | E10 |
| H | L | H | H | $\overline{\mathrm{E} 11}$ | E11 |
| H | H | L | L | E12 | E12 |
| H | H | L | H | $\overline{\mathrm{E} 13}$ | E13 |
| H | H | H | L | E14 | E14 |
| H | H | H | H | E15 | E15 |

## Logic Diagram

16:1 Mux


## Absolute Maximum Ratings


Input voltage ............................................................................................................................ 5.5 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V
Storage temperature ....................................................................................................... $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125* | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

* Case temperature.


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | TYP $\dagger$ MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  | 2 |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| ${ }_{1}$ IL | Low-level input current | $\mathrm{V}_{\mathrm{CC}}=$ MAX | $=0.4 \mathrm{~V}$ |  |  | 0.25 | mA |
| ${ }_{1} \mathrm{H}$ | High-level input current | $V_{C C}=$ MAX | $=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=$ MAX | $=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=\mathrm{MIN} \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ |  | ${ }^{\prime} \mathrm{OL}=8 \mathrm{~mA}$ |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =\mathrm{MIN} \\ \mathrm{~V}_{\mathrm{IL}} & =0.8 \mathrm{~V} \end{aligned}$ |  | ${ }^{1} \mathrm{OH}=-2 \mathrm{~mA}$ | 2.4 |  | V |
| ${ }^{\mathrm{OH}}$ | High-level output | $V_{I H}=2 V$ | Com | $\mathrm{I}^{\mathrm{OH}}=-3.2 \mathrm{~mA}$ |  |  |  |
| Ios | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 | -130 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $V_{C C}=$ MAX |  |  |  | $60 \quad 100$ | mA |

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ All typicals values are at $\underline{V}_{C O}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY | COMMERCIAL | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | (See Test Load) | MIN TYP MAX | MIN TYP | MAX |  |

## Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation

${ }^{\text {tPD }}$ is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level

2. tpZX is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
3. ${ }^{t} P \times Z$ is tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level: $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Application

Test Condition Mux


## Dual 8:1 Mux SN54/74LS451

## Features/Benefits

- 24-pin SKINNYDIP® ${ }^{\text {® }}$ saves space
- Twice the density of SN5/741S151
- Low-current PNP inputs reduce loading


## Description

The Dual 8:1 Mux selects one of eight inputs, D0 through D7, specified by three binary select inputs, $A, B$ and $C$. The true data is output on Y when strobed by S . Propagation delays are the same for inputs, addresses and strobes and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totempole drive standard.

## Logic Symbol

## Function Table

| INPUTS |  |  |  | OUTPUTS |
| :---: | :---: | :---: | :---: | :---: |
| SELECT |  | STROBE | Y |  |
| C | B | A |  |  |
| X | X | X | H | H |
| L | L | L | L | D0 |
| L | L | H | L | D1 |
| L | H | L | L | D2 |
| L | H | H | L | D3 |
| H | L | L | L | D4 |
| H | L | H | L | D5 |
| H | H | L | L | D6 |
| H | H | H | L | D7 |

## Ordering Information

| PART NUMBER | PACKAGE |  | TEMPERATURE |
| :---: | :---: | :---: | :---: |
| SN54LS451 | JS, W | 28 L | Mil |
| SN74LS451 | NS, JS |  | Com |



Logic Diagram
Dual 8:1 Mux


## Absolute Maximum Ratings

Supply voltage $\mathrm{V}_{\mathrm{C}}$. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 7.0 V
Input voitage ................................................................................................................................... 5.5 V

Storage temperature . .................................................................................................... $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

\left.| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  | UNIT |
| :--- | :--- | ---: | ---: | ---: | ---: | ---: | :---: | :---: |
|  |  | MIN | NOM MAX | MIN | NOM | MAX |  |  |$\right]$

* Case temperature.


## Electrical Characteristics Over Operating Conditions



* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ All typicals values are at ${ }^{\circ} \mathrm{CC}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.


## Switching Characteristics Over Operating Conditions



## Test Load

* The "Test Point" is driven by the outputs under test, and observed by instrumentation



Notes: 1. ${ }^{\text {t }}$ PD is tested with switch $\mathrm{S}_{1}$ closed $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level
2. ${ }^{\mathrm{t}} \mathrm{PZX}$ is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test. and closed for high impedance to " 0 " test.
3. tPXZ is tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+05 \mathrm{~V}$ output level.

Application
4-Bit Wide 8:1 Bus Multiplexer


## Quad 4:1 Mux SN54/74LS453

## Features/Benefits

- 24-pin SKINNYDIP® ${ }^{\circledR}$ saves space
- Twice the density of SN5/74LS153
- Low-current PNP inputs reduce loading


## Description

The Quad 4:1 Mux selects one of four inputs, C 0 through C 3 , specified by two binary select inputs, $A$ and $B$. The true data is output on Y. Propagation delays are the same for inputs and addresses and are specified for 50 pF loading. Outputs conform to the standard 8 mA LS totem-pole drive standard.

## Ordering Information

| PART NUMBER | PACKAGE |  | TEMPERATURE |
| :---: | :---: | :---: | :---: |
| SN54LS453 | JS, W | 28 L | Mil |
| SN74LS453 | NS, JS |  | Com |

## Logic Symbol



Logic Diagram
Quad 4:1 Mux

Absolute Maximum Ratings
Supply voltage $\mathrm{V}_{\mathrm{CC}}$ ..... 7.0 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | NOM | MAX | MIN | NOM | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125* | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

* Case temperature.

Electrical Characteristics Over Operating Conditions


* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ All typicals values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.


## Switching Characteristics over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load) | MILITARY | COMMERCIAL | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $C_{L}=50 \mathrm{pF}$ | TYP MAX | MIN TYP | MAX |

## Test Load



## Application



## Increment and Skip Counter 671492

## Features/Benefits

- Octal counter for microprogram counters, DMA controllers, and general purpose counting applications
- Bus-structured pinout
- 24-pin SKINNYDIP® saves space
- Low current PNP inputs reduce loading
- Expandable in multiples of 8 -bits
- Increment by two function can be used as a microprogrammed SKIP or Short BRANCH, resulting in simplified microprogrammed control structures


## Description

The Increment and Skip Counter (ISC) is an 8-bit cascadable synchronous counter with the ability to be incremented by one or two on the rising edge of the clock line CK. All of the control inputs are synchronous with respect to CK.
The LD input initializes the counter with data setup at the D7-D0 inputs. When the LD pin is HIGH prior to the rising edge of CK, data present at the inputs will be stored. If LD is LOW prior to clocking, a HOLD operation will take place. The LD pin, though synchronous with CK, operates independently of the count increment control SKIP. When $\overline{\text { SKIP }}$ is HIGH, the counter is instructed to count by one upon clocking. Alternately, when $\overline{\text { SKIP }}$ is LOW the counter will increment by two. To enable counting, the Count Input line $\overline{\mathrm{Cl}}$ is required to be LOW. In many applications of the ISC, the $\overline{\mathrm{CI}}$ input can be used as a count enable/disable control node.
During the increment by one operation, the Count Output signal $\overline{\mathrm{CO}}$ is LOW when the count becomes hexadecimal FF. Similarly, $\overline{\mathrm{CO}}$ is LOW for a count of hexadecimal FE during the increment by two operation. At all other times, $\overline{\mathrm{CO}}$ is HIGH. Accordingly, the $\overline{\mathrm{CO}}$ output can be connected to the $\overline{\mathrm{Cl}}$ input of a succeeding counter to expand in multiples of 8 -bits. $\overline{C O}$ is not affected by $\overline{\mathrm{OE}}$. The outputs Q7-Q0 are enabled when the output enable control $\overline{\mathrm{OE}}$ is LOW. Otherwise, when $\overline{\mathrm{OE}}$ is HIGH, the outputs are three-stated. Q7-Q0 are fully buffered, and have 24 mA sink current capability, which is required of many bus interface standards.

## Block Diagram



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 671492 | NS, JS | Commercial |

## Function Table

| $\overline{\mathbf{O E}}$ | $\mathbf{C K}$ | LD | $\overline{\mathbf{S K I P}}$ | $\overline{\mathbf{C I}}$ | D7-DO | Q7-Q0 | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| H | $*$ | $*$ | $*$ | $*$ | $*$ | $*$ | HI-Z |
| L |  | H | X | X | D | D | Load |
| L |  | L | X | H | X | Q0 | Hold |
| L |  | L | H | L | X | Q0 +1 | Incr +1 |
| L |  | L | L | L | X | Q0 +2 | Incr +2 |

* When $\overline{O E}$ is HIGH, Q7-Q0 are disabled to the high-impedance state; however, sequential operation of the counter is not affected


## Pin Configuration



## Absolute Maximum Ratings

Supply voltage $V_{\text {CC }}$. ....................................................................................................................... 7 V

Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .... . 5.5 V


## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Clock width | Low | 35 |  | * | ns |
|  |  | High | 25 |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time |  | 50 |  |  | ns |
| $t_{h}$ | Hold time |  | 0 | -15 |  | ns |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | COMMERCIAL TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{\text {* }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}{ }^{*}$ | High-level input voltage |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | 1 | -1.5 | $V$ |
| $I_{\text {IL }}$ | Low-level input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| $I_{1 H}$ | High-level input current | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=\mathrm{MIN} \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\mathrm{I}^{\mathrm{OL}}=24 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOH}^{\prime}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
| lozl | Off-state output current | $\begin{aligned} & V_{C C}=M A X \\ & V_{1 L}=0.8 V \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 |  |
| 'OS** | Output short-circuit current** | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -30 |  | -130 | mA |
| ${ }^{\text {CC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 120 | 180 | mA |

[^32]
## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See test load) | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency | Commercial$\begin{aligned} & C_{L}=50 \mathrm{pF} \\ & R_{1}=200 \Omega \\ & R_{2}=390 \Omega \end{aligned}$ | 12.5 |  | \% | MHz |
| tPD3 | Cl to CO delay |  |  | 35 | 50 | ns |
| ${ }^{\text {tPD1 }}$ | Clock to Q |  |  | 20 | 30 | ns |
| tpD2 | Clock to CO |  |  | 55 | 80 | ns |
| ${ }^{\text {tPZ }}$ X | Output enable delay |  |  | 35 | 45 | ns |
| tpxz | Output disable delay |  |  | 35 | 45 | ns |

## Standard Test Load



Notes: 1. $t_{P D}$ is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level.
2. tpZX is measured at the 1.5 V output level with $C_{L}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
3. tpXZ is tested with $\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$. $\mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Load Timing



## Timing During Operation



## Carry In To Carry Out Timing



## Application

The Increment and Skip Counter (ISC) is useful as a microprogram counter for a Micro-Programmed Control Unit (MCU). A block diagram of a general-purpose MCU is shown in Figure 1. The ISC, being the central element, provides addresses for microprogram memory. This memory is typically built with bipolar PROMs (such as the 63RS88 shown). However, MOS EPROMs and EEPROMs can be used for greater density and lower cost, if speed is not particularly an important application requirement.
As shown in Figure 1, the Interrupt Request Lines position the microprogram Start Address through a priority encoder and a small ( $32 \times 8$ ) PROM. The priority encoder serves to reduce as many as eight Interrupt Request Lines down to a 3-bit binaryweighted field used as the address for the mapping PROM. Since only three of the five PROM addresses are used, an optional 2-bit field can be applied to the PROM for diagnostics, or for task context switching. The Start Address, in conjunction with the Branch Address field, are connected to the Next Address multiplexer. Hence the Next Address multiplexer can select either of the two sources for branch address. The Start Address, essentially a forced branch operation, is used when an interrupt operation is requested externally to the MCU; whereas the 8 -bit Branch Address Field, which can have up to 256 words of microinstruction memory, is utilized for specific conditional branches.
The Control Field bits represent the control lines to the hardware that the MCU controls. These bit fields can either be encoded or
unencoded. In most microprogrammed systems, the bit fields are usually unencoded and connected directly to the specific device under control. However, a performance compromise can be achieved if all or a portion of the Control Field is encoded. The advantage of this technique is that more functions can be controlled. The trade-off is in conserving the number of microinstruction bits allocated to the Control Field, versus the number of possible controlled functions. The two techniques are termed Horizontal and Vertical microprogramming. Horizontal refers to fully parallel operation of the bit fields; whereas, Vertical implies some form of bit field encoding.
The Conditional Control Field selects from among various condition codes that can cause microprogram branch operations. Two kinds of branch operations can be performed in this MCU. The conventional branching described previously uses the ISC LD line to allow the Branch Address to be loaded. Loading new data in the ISC effectively causes the microprogram to branch to the next instruction set by the Branch Address. The Skip facility can be used to quickly test several conditions, then finally take a conventional branch upon exiting all of the tests. If a test is not passed, then a single increment occurs. The microinstruction sequence can then branch to another part of the program, rather than complete the remaining tests. This conditional control structure makes complex test operations more manageable because the test operations can be unified by +2 offset caused by a skip. This contrasts to the longer branch operation, which required precomputing all of the target address in the microprogram for every exit a loop has.

## 671492 Increment and Skip Counter

Application: General Purpose Microprogram Control Unit


## 2-Digit BCD Counter 671493

## Features/Benefits

- Drive numeric displays
- Expansion in 2-digit increments
- 24-pin SKINNYDIP® saves space
- Bus structured pinout
- Low current PNP inputs reduce loading
- Three-state output drive bus lines


## Description

The 2-digit BCD (Binary Coded Decimal) Counter is a synchronous counter with complementary count enables (CE1, CE2), parallel load ( $\overline{\mathrm{LD}}$ ), and carry out ( $\overline{\mathrm{CO}}$ ). Three control inputs ( $\overline{\mathrm{LD}}$, $\overline{C E 1}, C E 2$ ) provide one of three operations which occur synchronously on the rising edge of the clock (CK).
The load operation loads the inputs (D1 and D2) into the output register (Q1 and Q2) when load is LOW. Note that the load line overrides the increment.
When $\overline{L D}$ is not active, the counter will increment in a Binary-Coded-Decimal sequence if both count enables are asserted $\overline{C E 1}=\mathrm{L}$ and CE2 $=\mathrm{H}$ ), otherwise it holds.

Two or more BCD Counters can be cascaded to implement larger BCD counters by connecting carry out ( $\overline{\mathrm{CO}})$ of the first stage to count enable (CE1) of the second stage. This signal is not affected by $\overline{\mathrm{OE}}$.
Parallel loading allows programmability of the BCD Counter and numeric indicator.
This BCD Counter is ideal in an industrial control application where an event counter is needed to drive numeric displays. The device can receive one count enable in the form of strobes from a motor or other device. The second count enable can receive the period signal. With connections in this manner, the counter counts events during a period. The device will provide two active high BCD outputs (Q1 and Q2) to drive two numeric indicators, which feature an on-board decoder/driver.

## Block Diagram



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 671493 | NS, JS | Com |

Function Table

| $\overline{O E}$ | CK | LD | CE1 | CE2 | D1A-D1D/ D2A-D2D | $\begin{array}{\|l\|} \text { Q1A-Q1D/ } \\ \text { Q2A-Q2D } \end{array}$ | OPERATION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| H | * | * | * | * | * | Z | HI-Z* |
| L | 1 | L | X | X | D | D | Load |
| L | 1 | H | H | X | X | Q | Hold (CE1=H) |
| L | 1 | H | X | L | X | Q | Hold (CE2=L) |
| L | 1 | H | L | H | X | Q plus 1 | Increment |

* When $\overline{\mathrm{OE}}$ is HIGH, Q1 and Q2 are disabled to the high-impedance state; however, sequential operation of the counter is not affected.


## Pin Configuration



## Absolute Maximum Ratings

$\qquad$
$\qquad$
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V


## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | $\begin{aligned} & \text { AMER } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {tw}}$ | Clock width | Low | 35 |  |  | ns |
|  |  | High | 25 |  |  | ns |
| $\mathrm{t}_{\text {su }}$ | Setup time |  | 50 |  |  | ns |
| $t_{h}$ | Hold time |  | 0 | -15 |  | ns |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | COMMERCIAL TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 H^{*}}$ | High-level input voltage |  |  | 2 |  |  | V |
| $V_{1 C}$ | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| I/L | Low-level input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.25 | mA |
| ${ }_{1 / H}$ | High-level input current | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $V_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voitage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{I}^{\mathrm{OL}}=24 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | ${ }^{\mathrm{OH}}{ }^{\text {a }}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
| IOZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | A |
| $\mathrm{I}_{\mathrm{OZH}}$ | Of | $\begin{aligned} & V_{I L}=0.8 \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 |  |
| los** | Output short-circuit current** | $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | $-30$ |  | -130 | mA |
| $l_{\text {ICC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 120 | 180 | mA |

${ }^{*} V_{I L}$ and $V_{I H}$ are, in effect, input conditions of output tests and are not, themselves, directly tested. As conditions of tests, $V_{I L} \leq 0.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{IH}} \geq 2.0 \mathrm{~V}$.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ Typicals at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See test load) | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency | Commercial$\begin{aligned} & C_{\mathrm{L}}=50 \mathrm{pF} \\ & \mathrm{R}_{1}=200 \Omega \\ & \mathrm{R}_{2}=390 \Omega \end{aligned}$ | 12.5 |  |  | MHz |
| tpD1 | Clock to Q |  |  | 20 | 30 | ns |
| $\mathrm{t}_{\mathrm{PD} 2}$ | Clock to CO |  |  | 55 | 80 | ns |
| ${ }^{\text {t }}$ ZX | Output enable delay |  |  | 35 | 45 | ns |
| tPXZ | Output disable delay |  |  | 35 | 45 | ns |

## Standard Test Load



Notes: 1. ${ }^{\text {t }}$ PD is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level.
2. tpZX is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
3. tpXZ is tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for " 1 " to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Output Timing



## Input Timing



## Application: LED Displays

The Event Counter can be implemented using the 2-Digit BCD Counters. The 2-Digit BCD Counters control the display for three pairs of LED displays. The 2-Digit BCD Counters count the events.
The displays are controlled by the output enable. These counters display the count in 10s, 100s and 1000s respectively. These simply count the occurrence of an external event.

## 671493 2-Digit BCD Counter

## Application: Event Counter



# 8-Bit Priority Encoder with Register 

## Features/Benefits

- Encodes eight data lines in priority
- Output enable capability
- Three-state outputs drive bus lines


## Description

The 8-Bit Registered Priority Encoder accepts data from eight inputs (17-10) and provides a binary representation on the three outputs (Q2-Q0). A priority is assigned to each input (with 10 having the highest priority line, and 17 the lowest), so that when two or more inputs are simultaneously active, the input with the highest priority is loaded into the output registers. Pin 14 serves as the interrupt flag ( $\overline{\mathrm{FLAG}}$ ) and goes LOW when there is an interrupt present and remains HIGH when there is not interrupt present. The Priority Encoder registers are updated on the rising edge of the clock. The device also features four priority interrupt enable lines: E1, E2, $\overline{E 3}, \bar{E} 4$, which enable or disable the $\overline{F L A G}$ output. These enable lines have no effect on the priority outputs Q2-Q0. All outputs are HIGH-Z when the output control line $(\overline{\mathrm{OE}})$ is HIGH , and $\overline{\mathrm{OE}}$ operates independently of all other inputs.

## Block Diagram



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 671494 | $\mathrm{~N}, \mathrm{~J}$ | Com |

## Function Table

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | CLK | $\overline{\mathrm{OE}}$ | FLAG* | Q2 | Q1 | Q0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| L | X | X | X | X | X | X | H | 1 | L | L | H | H | H |
| L | X | X | X | X | X | H | L | 1 | L | L | H | H | L |
| L | X | X | X | X | H | L | L | 1 | L | L | H | L | H |
| L | X | X | X | H | L | L | L | 1 | L | L | H | L | L |
| L | X | X | H | L | L | L | L | 1 | L | L | L | H | H |
| L | X | H | L | L | L | L | L | 1 | L | L | L | H | L |
| L | H | L | L | L | L | L | L | 1 | L | L | L | L | H |
| H | L | L | L | L | L | L | L | 1 | L | L | L | L | L |
| L | L | L | L | L | L | L | L | 1 | L | H | H | H | H |
| X | X | X | X | X | X | X | X | X | H | Z | Z | Z | Z |

* Presumes E1, E2 $=\mathrm{HIGH}$ and $\overline{\mathrm{E} 3}, \overline{\mathrm{E} 4}=$ LOW. If the states of these four lines are different, the $\overline{\text { FLAG }}$ output will be disabled (HIGH), regardless of 10-17.


## Pin Configuration

## Absolute Maximum Ratings


Input voltage ........................................................................................................................... 7 . 7 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V


## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TC | Operating case temperature |  |  |  |  | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {w }}$ w | Clock width | Low | 25 | 10 |  | ns |
|  |  | High | 25 | 10 |  | ns |
| $\mathrm{t}_{\text {su }}$ | Setup time |  | 35 | 15 |  | ns |
| th | Hold time |  | 0 |  |  | ns |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | COMMERCIAL TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}^{*}}$ | High-level input voltage |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  | -0.73 | -1.5 | V |
| IIL | Low-level input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.02 | -0.25 | mA |
| $\mathrm{IIH}^{1}$ | High-level input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| 11 | Maximum input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| VOL | Low-level output voltage | $\begin{aligned} & V_{C C}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | ${ }^{\prime} \mathrm{OL}=24 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| VOH | High-level output voltage | $\begin{aligned} & V_{C C}=\mathrm{MIN} \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ | ${ }^{\prime} \mathrm{OH}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
| IOZL | Off-state output current | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MAX} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 100 |  |
| IOS | Output short-circuit current** | $V_{C C}=M A X \quad V_{O}=0 \mathrm{~V}$ |  | -30 | -70 | -130 | mA |
| ICC | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$, Outputs open |  |  | 120 | 180 | mA |

* $V_{I L}$ and $V_{I H}$ are, in effect, input conditions of $D C$ and functional output tests and are not directly tested.
$V_{I L}$ is specified at $\leq 0.8 \mathrm{~V}$ and $\mathrm{V}_{I H}$ is specified $\geq 2.0 \mathrm{~V}$.
** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ Typicals at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency | Commercial$\begin{aligned} & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\ & \mathrm{R}_{1}=200 \Omega \\ & \mathrm{R}_{2}=390 \Omega \end{aligned}$ | 16 | 25 |  | MHz |
| ${ }^{\text {tPLH }}$ | Clock to output delay |  |  | 15 | 25 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 15 | 25 |  |
| ${ }^{\text {t PRL }}$ | Output enable delay |  |  | 15 | 25 | ns |
| ${ }^{\text {tPZH }}$ |  |  |  | 15 | 25 |  |
| ${ }^{\text {PPLZ }}$ | Output disable delay |  |  | 15 | 25 | ns |
| ${ }_{\text {tPHZ }}$ |  |  |  | 15 | 25 |  |

## Standard Test Load



Notes: 1. tPD is tested with switch $\mathrm{S}_{1}$ closed. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$ and measured at 1.5 V output level.
2. tPZX is measured at the 1.5 V output level with $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} . \mathrm{S}_{1}$ is open for high impedance to " 1 " test, and closed for high impedance to " 0 " test.
3. tpXZ is tested with $C_{L}=5 \mathrm{pF} . \mathrm{S}_{1}$ is open for "1" to high impedance test, measured at $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ output level; $\mathrm{S}_{1}$ is closed for " 0 " to high impedance test measured at $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ output level.

## Output Timing



## Input Timing



## Application: DMA and Interrupt Arbitration

The Priority Encoder with Register has several applications in systems requiring arbitration among several competing request lines. In order to obtain a sufficiently quick response in a real time system, access to resources must be ordered, or weighted by priority of importance. For example, a computer and its peripherals may use a number of interrupt request lines for service requests. In some applications, a normal interrupt request is processed too slowly, and a faster means of receiving or sending data is required. In this situation, direct access to system memory could be required, and a DMA Controller used to perform the operations in cooperation with the host computer. Disk Drives commonly use this technique; if more than one drive is in a system, a flexible means of arbitrating DMA requests would be required.
Figure 1 details how a Priority Encoder can be used to construct a Priority Interrupt Controller. Note that in this application, the inputs can either be DMA or Interrupt requests to the Host Computer. In fact, two circuits can be combined in one system to accommodate both types of requests. The expansion possibilities of Figure 1 will be covered after the basic operation of the circuit is explained.
The Interrupt Controller consists of the Priority Encoder, an Interrupt Latch, an Interrupt Level Register, a Comparator, FlipFlop and a single gate. For many applications the Comparator, Flip-Flop and gate could be realized in a PAL device, but are
shown as separate elements for clarity. The Interrupt Latch can be a common 74LS373, or if additional speed is required, a 74 S 373 can be used.

The registers of a Priority Encoder are clocked at a constant rate by the I-CLK signal, which means that any of the interrupt request lines 17-10 passed on by the interrupt latch are continously sampled by l-CLK. The purpose of the interrupt latch is to freeze, or lock out, all interrupt requests once a validated interrupt is sent to the system.
An interrupt is validated by the 3-bit comparator shown in Figure 1, and by the Priority Encoder flag signal. A prestored Mask Value from the Interrupt Level Register is compared with the current value of Q2-Q0, and if the priority code is greater, and if FLAG is LOW, the system is informed that an interrupt is needed. FLAG normally goes low when any of the 17-10 lines are asserted High, if simultaneously all of the Priority Encoder enables (E1, E2, E3 and E4) are asserted.

Because of the fact that in a typical system interrupts can occur at irregular intervals, the Interrupt Controller must be capable of synchronizing to the cycle timing of the host machine. The on-chip registers of the Priority Encoder make possible this synchronization activity. The FLAG signal in combination with the host system timing, and the Interrupt Latch allows the host positive control over the Interrupt Controller.

## 5/671494 Priority Encoder with Register

## Application: Priority Interrupt Controller Application



## SiBER <br> (Single Burst Error Recovery IC)

673480

## Features/Benefits

- 15 MHz data rate
- Selectable CRC or ECC polynomials
- Standard 16-bit CRC-CCITT polynomial detects errors
- Computer-generated 32-bit ECC polynomial exceeds the performance of Fire code polynomials
- Double-burst error detection and single-burst error correction with ECC polynomial
- Programmable correction span of 5,8 or 11 bits
- Hardware or software correction modes
- Separate receiver and transmitter ports
- HOLD pin for idle operation
- Maximum of 1024 bytes of data
- Inverted checkbits and selective initialization to a HIGH state improve reliability


## Description

The SiBER (Single Burst Error Recovery) is a LSI error detection and correction circuit used to insure data integrity between two serial ports. An industry standard 16-bit CRC polynomial and a 32-bit computer-generated ECC polynomial are both implemented on this chip. Both polynomials have error detection capabilities, but only the ECC polynomial is used for error correction. The ECC polynomial has a maximum correction span of 11 bits in series and a maximum record length of 1024

## Pin Configuration



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 673480 | J | Com |

bytes of data. The 16-bit CRC polynomial is the industry standard CCITT polynomial:

$$
x^{16}+x^{12}+x^{5}+1
$$

The 32-bit computer-generated ECC polynomial is selected for its error detection span, and the high probability of detecting short double-burst errors:

$$
x^{32}+x^{28}+x^{26}+x^{19}+x^{17}+x^{10}+x^{6}+x^{2}+1
$$

The SiBER implements the transmit, receive, search, and correct algorithms, which are basically serial division operations. By simply asserting the appropriate control signals, spelled out in the "modes of operation" section of this data sheet, the user can:

1) Append checkbits to the data under transmission.
2) Generate the syndrome from received data.
3) Correct erroneous data bits with the information embedded in the syndrome.
Selective inversion of checkbits and selective initialization of the internal registers to an all-one-state insure randomness in the encoded checkbits and, consequently, improve reliability.
Typical applications of the SiBER include mass storage environments and data communication channels.

## Block Diagram



## SiBER Pin Description

| PIN NUMBER | SYMBOL | PIN NAME | FUNCTION |
| :---: | :---: | :---: | :---: |
| 1, 12 | GND | Ground | Electrical Ground |
| 2 | $\overline{\text { INIT }}$ | Initialize | An active LOW asynchronous input pulse is used to reset all internal registers and output flags before transmitting or receiving any data. |
| 3 | HOLD | Hold | Raising this input HIGH puts the device in idle operation by holding its present state. The data present on SIT is sent to SOT. A LOW presented on this pin resumes normal operation. |
| 4 | SIC | Serial Input Correction | During hardware correction, the buffered data is presented to this input one bit at a time in reverse order. If the data bit is erroneous it is corrected and placed on SOT. See block diagram for data flow. |
| 5 | SIT | Serial Input Transmitter | During the transmit mode, data to be transmitted is presented to this input in a serial fashion. |
| 6 | SOT | Serial Output Transmitter | Four different types of data are shifted out on this output (see block diagram). Data on SIR appears on this pin during receive mode; corrected data appears during hardware correction, error syndrome appears during software correction; and error pattern appears during hardware/software correction. |
| 7, 18 | $V_{C C}$ | VCC | +5 volt supply. |
| 8,9 | $\mathrm{CS}_{0}, \mathrm{CS}_{1}$ | Correction Span Select | Correction spans that can be selected by specifying $\mathrm{CS}_{0}$ and $\mathrm{CS}_{1}$ are: a 5 -bit correction span ( $\mathrm{CS}_{0}=\mathrm{LOW}, \mathrm{CS}_{1}=\mathrm{LOW}$ ), an 8 -bit correction span ( CS $_{0}=$ LOW, CS $_{1}=$ HIGH) , and an 11-bit correction span (CS $0=$ $\left.\mathrm{HIGH}, \mathrm{CS}_{1}=\mathrm{HIGH}\right)$. The fourth state $\left(\mathrm{CS}_{0}=\mathrm{HIGH}, \mathrm{CS}_{1}=\mathrm{LOW}\right)$ is restricted and must never be entered. It is used by the factory during manufacturing to test the device for enhanced quality assurance and guaranteed functionality. |
| 10 | CRC/ECC | $\begin{aligned} & \mathrm{CRC} / \overline{\mathrm{ECC}} \\ & \text { Select } \end{aligned}$ | This input control line is used to select the desired polynomial. The 32-bit computer-generated ECC polynomial is selected when CRC/ECC is LOW and the 16 -bit standard CRC-CCITT polynomial when CRC/ECC is HIGH. |
| 11 | CLKIN | Clock Input | This is the clock input, and the rising edge is used to strobe the data during the transmit, receive, and correction modes of operation. |
| 13 | CLKOUT | Clock Output | The Clock output is a delayed clock input. It is generally used for synchronization of all output signals from the SiBER. |
| 14 | PATT | Pattern Flag | This output is set HIGH (and remains set until initialized) when the error pattern is found by the SiBER. |
| 15 | ERRFLG | Error Flag | This output is set HIGH (and remains set until initialized) when the syndrome is nonzero. A nonzero syndrome at the end of the receive cycle means that the data read is in error. |
| 16 | EOC | End of Correction | This output is set HIGH (and remains set until initialized) eleven clock cycles after the pattern flag is set. |
| 17 | $\overline{\text { TEST }}$ | $\overline{\text { Test }}$ | This input must be tied to $V_{C C}$ for normal operation. This pin is used by the factory during manufacturing to test the device for enhanced quality assurance and guaranteed functionality. |
| 19 | SOR | Serial Output Receiver | Two different types of data are shifted out on this output (see block diagram). During the transmit mode, the data presented on SIT appears on this pin when TGS is HIGH, and checkbits appear when TGS is pulled LOW. |
| 20 | SIR | Serial Input Receiver | During the receive mode, data is presented to this input in a serial fashion. |
| 21 | CGS | Correction Generate or Shift | This input controls the device during the search and correct modes. The four options are: (1) Shift the syndrome when CGS is LOW immediately after a receive operation, (2) generate the error pattern when CGS is HIGH and the output PATT is LOW, (3) shift the error pattern when CGS is LOWered and the output PATT is HIGH, and (4) correct the burst of erroneous data when CGS is HIGH and PATT is HIGH. |
| 22 | RGS | Receive Generate or Shift | This input controls the device during the receive mode. When RGS=HIGH the syndrome is being generated. On the HIGH-to LOW transition of RGS, the error condition is latched; the error flag is set if the syndrome is nonzero and the SiBER enters correction mode. |
| 23 | TGS | Transmit Generate or Shift | This input controls the device during the transmit mode. The two options are to generate checkbits (TGS $=$ HIGH) and to shift checkbits (TGS = LOW). |
| 24 | $\mathrm{R} / \mathrm{T}$ | $\frac{\text { Receivel }}{\text { Transmit }}$ | This input pin controls the mode of operation. A LOW enables the transmit mode, and a HIGH enables the receive mode. |

## Modes of Operation

Prior to performing any operation, the appropriate correction span and polynomial type must be selected. The settings of the
control signals for each of the four options are summarized below:

| SIGNALS |  | DESCRIPTION |  |
| :---: | :---: | :---: | :--- |
| CRC/ECC | CSO | CS1 |  |
| 0 | 0 | 0 | 5-bit correction span, <br> ECC polynomial |
| 0 | 0 | 1 | 8-bit correction span, <br> ECC polynomial |
| 0 | 1 | 1 | 11-bit correction span, <br> ECC polynomial |
| 1 | X | X | No correction, CRC polynomial <br> generation |
| X | 1 | 0 | Illegal state. It is only used <br> by the factory for testing <br> the devices. |

" X " Designates "Don't Care".

The four different modes of operation are tabulated below. Note that the CRC polynomial cannot go into the search/correct
mode, but the other modes and functions are common to both the CRC and ECC polynomials.

| MODE | CONTROL SIGNALS |  |  |  | DATA PATH |  | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | R/T | TGS | RGS | CGS | IN | OUT |  |
| TRANSMIT | 0 | 1 | X | X | SIT | SOR | Generate checkbits from the data placed on SIT. This data appears on SOR. |
|  | 0 | 0 | X | X | X | SOR | Shift the checkbits serially on SOR. |
| RECEIVE | 1 | X | 1 | X | SIR | SOT | The data on SIR appears on SOT. Simultaneously, the syndrome is generated in the 32-bit feedback shift register. |
|  | 1 | X | 1 | X | X | X | Set the error flag if the syndrome is nonzero. |
| SEARCH <br> (ERRFLG $=\mathrm{H}$, <br> PATT = L) | 1 | X | 0 | 1 | X | X | Search for the error pattern. |
|  | 1 | X | 0 | 0 | X | SOT | Shift the syndrome serially on SOT. (software correction) |
| CORRECT (ERRFLG $=\mathrm{H}$, PATT = H) | 1 | X | 0 | 1 | SIC | SOT | Data placed on SIC is corrected and placed on SOT. (hardware correction) ${ }^{1}$ |
|  | 1 | X | 0 | 0 | X | SOT | Shift the error pattern. (software/hardware correction) |

NOTE: 1. In this mode, data placed on SIC is transmitted to SOT. This feature allows the user to implement a read-modify-write operation on buffered data without paying attention to the pattern flag PATT.

## Transmit Mode

In this mode, the SiBER generates the unique checkbits for the data being transmitted. These checkbits are appended to the end of the data stream. To initialize the device INIT is asserted while $R / \bar{T}$ is LOW. The internal registers and the output flags are reset and the device is in the transmit mode. If TGS is LOW the SiBER will remain initialized until TGS is pulled HIGH. This feature is implemented to allow relaxed initialization timing. Once TGS is

HIGH the device starts to generate checkbits for the data present on SIT. The data on SIT also appears on the SOR output. When the last data bit is transmitted, LOWer TGS and the 32 checkbits for the ECC polynomial or the 16 checkbits for the CRC polynomial are serially shifted out on SOR. Figure 1 shows the data flow during the transmit mode. TGS must remain low for at least 32 clock cycles for the ECC polynomial or 16 clock cycles for the CRC polynomial to allow all the checkbits to be shifted out.


Figure 1. Data Flow During the Transmit Mode

## Receive Mode

In this mode, data and checkbits are read from the SIR pin and the SiBER generates a syndrome. To initialize the device $\overline{\mathrm{NIT}}$ is asserted while $\mathrm{R} / \overline{\mathrm{T}}$ is HIGH . The internal registers and the output flags are reset and the device is in the receive mode. If RGS is LOW the SiBER will remain initialized until RGS is pulled HIGH. The feature is implemented to allow relaxed initialization timing. Once RGS is HIGH, the device starts to generate the syndrome for the data present on SIR. The data on SIR also appears on the

SOT output. When the last data bit, which is really the last checkbit that was appended to the block of data, is presented on SIR, the error flag ERRFLG is latched on the HIGH-to-LOW transition of RGS; the error flag is set for the case of a non-zero syndrome. When the syndrome is non-zero (ERRFLG = HIGH) and the ECC polynomial is asserted, then the search mode is invoked. The state of the control pin CGS determines the operation performed. The correction cycle is not invoked when the CRC polynomial is asserted. Figure 2 shows the data flow during the receive mode.


Figure 2. Data Flow During the Receive Mode

## Search/Correct Mode

The search/correct mode is used to find the error pattern required to correct the erroneous data record that has just been received. The error pattern can be found by shifting the 32-bit syndrome (left by the receive operation) backwards until a correctable pattern is found, or the search is exhausted by clocking beyond the length of the data record (which indicates the error is uncorrectable). Note that the search/correct mode pertains only to ECC operations and not to CRC operations.
When an error occurs, and correction of the error is desired, there are three methods of finding the error and correcting it, as follows:

1) Pass the syndrome on to the host processor for software correction.
2) Perform a correction pattern search inside the SiBER and pass the error pattern on to the host processor for correction (hardware/software correction).
3) Pass the data record to be corrected through the SiBER (in reverse order) while the SiBER performs the pattern search AND corrects the data record 'on the fly' as it passes through the SiBER chip.
Typically, after the last bit of the ECC field of the data record being read is clocked into the SiBER, RGS is deactivated and HOLD is activated. One clock later, the ERRFLG signal will reflect the final state of the ECC/CRC shift register. It is at this time the system must decide whether to perform a correction or not. Typically, in magnetic media implementations, the system may perform one or more retries on the data record before attempting the correction (some systems will retry until subsequent received ECC fields or syndromes generated by receive operations, are found to be identical).

The Syndrome can be clocked out of the SiBER by simply deactivating the HOLD signal, allowing the syndrome to be shifted out of the SiBER on the SOT line. If the SiBER is to be used to perform all or part of the correction function (as in method 2 or 3 ), the CGS signal is activated and the HOLD signal is deactivated and the search operation begins.
The first clock cycle of the search operation is used to prepare the syndrome for reverse polynomial shifting. From then on, the SiBER looks for error burst patterns to appear in the ECC shift register. The exact type of pattern searched for is dependent on the correction span selection input signals, CSO and CS1 (5-, 8-, or 11-bit maximum burst lengths). When an error pattern that fits the qualifications of the correction span inputs is found in the proper position of the ECC shift register, the PATT signal is activated by the SiBER . If method 2 is being used, then the error pattern is shifted out of the SiBER (by lowering the CSG input) when the PATT signal has become active (the HOLD signal can be used to aid in controlling the transition between searching and error pattern shifting, for system timing constraints). Note: the error pattern being shifted out of the SiBER will be generated in the reverse order with respect to the original data received. It may also be noted that the error pattern extracted will be CS bits long (where CS represents the selected correction span) regardless of the actual error burst length. When an error burst whose length is less than the correction span selected is found, the first N bits of the error pattern from the SiBER will be zeros (where N = correction span - actual error burst length). For example, if a single-bit error burst occurs and correction is performed with an 8 -bit correction span selected, then when the error pattern is found, the first seven bits of the error pattern out of the SiBER will be zeros, and the eighth bit will be a one.


Figure 3. Data Flow During the Search/Correct Mode for Method 1 and Method 2. The Error Syndrome or Pattern is Shifted Out on SOT

Once the pattern is found, the number of clock cycles required to find it, NCC, is used to calculate the position of the error. The calculation is made with respect to the end of the data record including the 32-bit ECC field. The calculation is as follows: $E D=$ NCC -1 (where ED is the Error Displacement in bits, NCC is the Number of Clock Cycles required to find the pattern, and 1 for the search preparation). Therefore, if the pattern is found in one clock, the error displacement, ED, will be zero, indicating the error pattern was found at the end of the ECC field of the data record.
Since the ECC field is used only for error detection and correction, many systems do not store this field if dedicated hardware is used for correction. Therefore the Error Displacement equation can be modified to calculate the distance with respect to the end of the data field, instead of the ECC field. The calculation would then be: ED = NCC-33. Note that the Error Displacement can, in this case, be a negative number. This simply indicates that the error burst is partially, if not entirely, contained in the ECC field. Careful consideration for boundary conditions are required in these cases.
The maximum number of clock cycles, MNC, to find a correctable error pattern with the SiBER is calculated as: $\mathrm{MNC}=\mathrm{DL}+33-$ CS (where DL is the number of bits in the data field, and CS the selected correction span), which corresponds to an error burst at the beginning of the data field. The search operation should be terminated if the PATT signal has not been activated within the number of clock cycles calculated in the above equation for MNC. If the error pattern cannot be found within MNC clock cycles, then the error is considered uncorrectable and no further action can be taken.
Method 3 is implemented with the SiBER by retransmitting the data record through the SiBER during the pattern search. Note: The data record is transmitted in reverse order with respect to the receive operation, during the search/correct operation.

When the SiBER finds the error pattern, the data being presented at the SIC input is XORed with the error pattern and retransmitted, via the SOT output, as corrected data. During other periods of the search/correct operation, the data presented at the SIC input is retransmitted to the SOT output, unchanged.
After a receive operation with an error condition present, the SiBER starts the search/correct operation, just as described for method 2, by asserting the CGS input line. For proper positioning of the retransmitted data with respect to the error pattern to be found, the SiBER must be clocked once (if the data record retransmission includes the 32-bit ECC field) or thirty-three times (if the data record retransmission does not include the 32-bit ECC field) before data bits are presented at the SIC input and captured at the SOT output.
If the PATT output does not become active within MNC clock cycles, as calculated above, then the error is uncorrectable.

## Example:

Data Field $=512$ bytes $=4096$ bits Correction Span $=11$ bits
MNC $=(4096+33-11)=4118$ clock cycles
Therefore, with this format, all correctable error patterns must be found within 4118 clock cycles from when the search/correct operation began, otherwise the error is uncorrectable.
If a search operation finds the error pattern in 1787 clock cycles, then the 11-bit error burst starts (in reverse order) 1786 bits from the end of the ECC field or 1754 bits from the end of the data field: This can be recalculated for forward displacement as (4096-1754-11) bits $=2331$ bits from the beginning of, or starting with bit 4 of the 292nd byte, of the data field. Figure 4 shows the position of the error pattern in the data field.


Figure 4. Example


Figure 5. Data Flow During Search/Correct Mode for Method 3. Data on SIC is Corrected and Placed on SOT

## Multiple Burst Errors

When there is an error, the error flag ERRFLG goes HIGH. If this error is within the correcting capability of the code, then PATT goes HIGH when the error pattern is found. If there is a multiple error of two or more bursts and the capability of the code is
exceeded, then the pattern flag PATT remains LOW during the search mode. The SiBER is recommended for detecting and correcting bursts of errors in 1 K bytes of data or a total of 8 K bits in a serial stream. It can be used for even larger streams, but the probability of miscorrection is increased.


Figure 6. Clock and Hold Timing

## Absolute Maximum Ratings

Supply Voltage $V_{C C}$ ..... 7 V
Input Voltage ..... 7 V
Off-state output Voltage ..... 5.5 V
Storage temperature $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VCC | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| tIPW | Initialization Pulse Width | 7, 8 | 20 |  |  | ns |
| tCRCS | CRC Initialize Set-Up Time | 7,8 | 20 | 12 |  | ns |
| tris | R/T Initialize Set-Up Time | 7,8 | 15 | 8 |  | ns |
| tGSS | Generate and Shift Set-Up Time | 7, 8, 10, 11 | 50 | 27 |  | ns |
| tGSH | Generate and Shift Hold Time | 7, 8, 10 | 0 |  |  | ns |
| tSIS | Serial Input Set-Up Time | 7, 8, 11 | 50 | 32 |  | ns |
| ${ }^{\text {tSIH}}$ | Serial Input Hold Time | 7,8 | 0 |  |  | ns |
| thS | Hold Set-Up Time | 6 | 45 | 24 |  | ns |
| the | Hold Time for Hold Input | 6 | 0 |  |  | ns |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | - | 0 | \% | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2 |  |  | V |
| VIC | Input clamp voltage | $V_{C C}=M I N$ | $11=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | 0.25 | mA |
| IIH | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 25 | $\mu \mathrm{A}$ |
| $1 /$ | Maximum input current | $V_{C C}=M A X$ | $V_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| VOL | Low level output voltage | $\begin{aligned} & V_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOL}=16 \mathrm{~mA}$ |  |  | 0.5 V | V |
| VOH | High level output voltage | $\begin{aligned} & V_{C C}=\mathrm{MIN} \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{OH}=-3.2 \mathrm{~mA}$ | 2.4 |  |  | V |
| Ios | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}$ | $\mathrm{V}_{0}=0 \mathrm{~V}$ | -30 |  | -130 | mA |
| Icc | Supply current | $\mathrm{V}_{C C}=\mathrm{MAX}$ |  |  | 280 | 360 | mA |

[^33]
## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MINCOMMERCIAL <br> TYP | MAX | UNIT |
| :--- | :--- | :---: | :---: | :---: | :---: |
| fMAX | Maximum Clock Frequency | 6 |  | 15 | MHz |
| tSIO | Serial Input to Output Delay | $7,8,11$ | 25 | 35 | ns |
| tGSO | Generate to Serial Output Delay | $7-11$ | 25 | 35 | ns |
| t (LKO | Clock to Output Delay | $7,9,10$ | 49 | 60 | ns |
| tERR | RGS to ERR Delay | $8,9,10$ | 20 | 30 | ns |
| tPAT | Clock to PATT Delay | 10,11 | 33 | 42 | ns |
| tEOC | Clock to EOC delay | 10,11 | 33 | 40 | ns |
| tFR | Initialize to Flags Reset Delay | 8 | 27 | 35 | ns |
| tCD | CLKIN to CLKOUT Delay | 6 | 12 | 18 | ns |

## Standard Test Load



Input Pulse = 3 V
Input Rise and Fall Time
( $10 \%-90 \%$ ) 2.5 ns
Measurement made at 1.5 V


NOTES: 1. After Initialization the chip is in a hold mode (idle) for as long as TGS is LOW.
2. When TGS is HIGH, the data to be encoded is shifted into SIT. The maximum data length is 1 K bytes.
3. When TGS is lowered in the transmit mode the checkbits are shifted out on SOR. There are 32 checkbits for the ECC polynomial and 16 for the CRC polynomial.

Figure 7. Transmit Mode


NOTES: 1. After Initialization the chip is in a hold mode (idle) for as long as RGS is LOW.
2. When RGS is HIGH, the data followed by the checkbits is shifted into SIR. The syndrome is generated from this data.
3. The error flage ERRFLG is pulled HIGH if the syndrome is non-zero or kept LOW if there is no error. SYN. = Syndrome Bit Valid

Figure 8. Receive Mode


$$
\begin{aligned}
& \text { PATT LOW } \\
& \text { EOC LOW }
\end{aligned}
$$

NOTES: 1. When RGS is pulled LOW in the receive mode and CGS and PATT are LOW, the 16 -bit syndrome for the CRC polynomial or the 32 -bit syndrome for the ECC polynomial is shifted out on SOT. This is called the search mode.
2. The error flag ERRFLG remains LOW when there is no error.

SYN. = Syndrome Bit Valid
Figure 9. Search Mode for Software Correction


NOTES: 1. When CGS is HIGH, the SIBER is clocked until PATT is flagged. This is the search mode in which the location of the error pattern is determined.
2. The error flag ERRFLG remains LOW if there is no error.
3. A multiple error is indicated when ERRFLG is HIGH and PATT remains LOW.
4. When CGS is LOWered after PATT goes HIGH, the error pattern is shifted out on SOT. This is called the correction mode.
5. 11 clock cycles after PATT is flagged, EOC goes HIGH.

Figure 10. Search and Correct Modes for Software/Hardware Correction


NOTES: 1. Data placed on SIC is transmitted to SOT. This feature allows the user to implement a ready-modify-write operation on buffered data without paying attention to the pattern flag PATT.
2. When CGS is HIGH the SIBER is clocked until PATT is flagged. This is the search mode in which the location of the error pattern is determined.
3. The error flag ERRFLG remains LOW if there is no error.
4. A multiple error is indicated when ERRFLG is HIGH and PATT remains LOW.
5. When PATT is HIGH, the data across SIC is inverted, if erroneous, and shifted out on SOT.
6. 11 clock cycles after PATT is flagged, EOC goes HIGH.
C.D. = Corrected Data Bit Valid

Figure 11. Search and Correct Modes for Hardware Correction

## Application



Figure 12. System Block Diagram

The SiBER and the Serializer/Deserializer (SERDES) block, shown in more detail in Figure 13, reside in the front end of a typical system. This block will append the checkbits to the data under transmission and it will generate the syndrome from the
received data. Correction can be performed in case of an error. Four operations take place under external control provided by the control logic block.


Figure 13. Detailed SiBER and Serializer/Deserializer (SERDES) Block



## Tin

Monolithic MM Memories

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## FIRST-IN FIRST-OUT BUFFER MEMORIES

## Product Selection and Application Reference Guide

Low-Power FIFOs

| CASCADABLE/ STANDALONE | MAXIMUM DATA RATE | ORG. | MAXIMUM ICC | FEATURES | PACKAGES | PINS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 67L401* | 5 MHz | $64 \times 4$ | 100 mA |  | N,J,NL (20) | 16 |
| 67L402* | 5 MHz | 64x5 | 130 mA |  | N,J,NL (20) | 18 |
| C67L401D* | 15 MHz | $64 \times 4$ | 100 mA | $\mathrm{IOL}=24 \mathrm{~mA}$ | N,J,NL (20) | 16 |
| C67L402D | 15 MHz | $64 \times 5$ | 100 mA | $1 \mathrm{OL}=24 \mathrm{~mA}$ | N,J,NL (20) | 18 |
| C67L4033D | 15 MHz | 64x5 | 115 mA | $\mathrm{IOL}=24 \mathrm{~mA}$, Three-State, Status Flags | N,J,NL (20) | 20 |
| C67L4013D | 15 MHz | 64×4 | 100 mA | $1 \mathrm{OL}=24 \mathrm{~mA}$, Three-State | N,J;NL (20) | 16 |

* Standalone only.


## High-Performance FIFOs

| STANDALONE | MAXIMUM <br> DATA RATE | ORGANIZATION | FEATURES | PACKAGES | PINS |
| :--- | :--- | :--- | :--- | :---: | :---: |
| 67411 A | 35 MHz | $64 \times 4$ | $\mathrm{IOL}=24 \mathrm{~mA}$ | J | 16 |
| 67412 A | 35 MHz | $64 \times 5$ | $\mathrm{IOL}=24 \mathrm{~mA}$ | J | 18 |
| 67413 A | 35 MHz | $64 \times 5$ | $\mathrm{IOL}=24 \mathrm{~mA}$, Three-State, Status Flags | J | 20 |
| 67411 | 25 MHz | $64 \times 4$ | $\mathrm{IOL}=24 \mathrm{~mA}$ | J | 16 |
| 67412 | 25 MHz | $64 \times 5$ | $\mathrm{IOL}=24 \mathrm{~mA}$ | J | 18 |
| 67413 | 25 MHz | $64 \times 5$ | $\mathrm{IOL}=24 \mathrm{~mA}$, Three-State, Status Flags | J | 20 |

Standard FIFOs

| CASCADABLE | STANDALONE | MAXIMUM DATA RATE | ORGANIZATION | PACKAGES | PINS |
| :--- | :--- | :---: | :---: | :---: | :---: |
| C 67401 | 67401 | 10 MHz | $64 \times 4$ | $\mathrm{~N}, \mathrm{~J}, \mathrm{NL}(20)$ | 16 |
| C 67402 | 67402 | 10 MHz | $64 \times 5$ | $\mathrm{~N}, \mathrm{~J}, \mathrm{NL}(20)$ | 18 |
| C 67401 A | 67401 A | 15 MHz | $64 \times 4$ | $\mathrm{~N}, \mathrm{~J}, \mathrm{NL}(20)$ | 16 |
| C 67402 A | 15 MHz | $64 \times 5$ | $\mathrm{~N}, \mathrm{~J}, \mathrm{NL}(20)$ | 18 |  |
| C 67401 B | 67402 A | 16.7 MHz | $64 \times 4$ | $\mathrm{~N}, \mathrm{~J}$ | 16 |
| C 67402 B | 67401 B | 16.7 MHz | $64 \times 5$ | $\mathrm{~N}, \mathrm{~J}$ | 18 |

## System FIFOs

| DEVICE | DESCRIPTION | ORGANIZATION | PACKAGES | PINS | MAXIMUM <br> FREQUENCY |
| :---: | :--- | :---: | :---: | :---: | :---: |
| 67417 | Serializing FIFO Memory <br> Serial data buffering with optional Serial-to- <br> Parallel or Parallel-to-Serial data conversion | $64 \times 8 / 9$ | J | 24 | 28 MHz Serial <br> 10 MHz Parallel <br> 674219FIFO RAM Controller <br> Provides control for SRAM to act as a <br> FIFO buffer |

## FIFO Applications

| APPLICATION | KEY REQUIREMENTS | FIFO PRODUCTS |
| :---: | :---: | :---: |
| Microprocessor/CPU Buffering | Data rate of processor System architecture (word width) | $\begin{aligned} & 74 \text { S225/A } \\ & \text { C/67401/2A/B } \\ & 67411 / 2 / 3 A \end{aligned}$ |
| Peripherals | High data rate or low power Status flag | C/67401/2A/B 67L401/2 C67L401/2/3D |
| Data/Telecom | High data rate or low power Status flags Word depth (high storage capacity) Data format (serial or parallel) | $\begin{aligned} & \text { C67L401/2/3D } \\ & \text { C67401/2/3D } \\ & 674219 \\ & 67417 \end{aligned}$ |
| Data Acquisition | High data rate | $\begin{aligned} & 67411 / 2 / 3 A \\ & 74 S 225 A \end{aligned}$ |

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# FIFOs: Rubber-Band Memories to Hold Your System Together 

## Chuck Hastings

## Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than other system components, but often operate with severly degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices - "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-bymicrosecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the $64 \times 4$ and $64 \times 5$ Monolithic Memories FIFOs in particular.

## What is a FIFO?

FIFO is one of those made-up words, or acronyms, formed from the initials of a phrase - in this case, "First-In, First-Out." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a queue discipline which may be applied to the processing of the elements of any queue or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel - "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices for coins which handle the coins in this same manner. (See Figure 1.)


Figure 1. Primitive Mechanical FIFO Device
Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an asynchronous FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/oûtput programming practice, a FIFO memory region is sometimes referred to as a circular buffer, and in programming for computer-controlled telephone systems it is called a hopper. A LIFO memory region is usually referred to as a stack.

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

## Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type $6740164 \times 4$ FIFO and type $6740264 \times 5$ FIFO which have been available for several years from Monolithic Memories. (" $64 \times 4$ " here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:


Figure 2. Architecture of the $\mathbf{6 7 4 0 1}$ FIFO
The list of signals/pins for the 67401 is:

| TYPE | HOW MANY | (CUM.) | I/O/V |
| :--- | :---: | :---: | :---: |
| Data In | 4 | 4 | 1 |
| Output | 4 | 8 | O |
| Control: | 1 | 9 |  |
| Shift In | 1 | 10 | 1 |
| Shift Out | 1 | 11 | 1 |
| Master Reset |  |  |  |
| Status: | 1 | 12 | 0 |
| Input Ready | 1 | 13 | 0 |
| Output Ready | 1 | 14 | - |
| Not Connected | 1 | 15 | V |
| Voltage: | 1 | 16 | V |
| VCC (+5V) |  |  |  |
| Ground |  |  |  |

The corresponding list for the 67402 differs only in that there are five Data in lines rather than four, and five Output lines rather than four. The reason that there is an unused pin is that the

67401 was originally designed as a faster bipolar upgrade of a MOS part, the Fairchild 3341, which needs a second powersupply voltage ( -12 V ) as well as $\mathrm{V}_{\mathrm{CC}}$. Much of the description to be given here of the 67401 also applies to the 3341, except for data rate - the 67401 can operate at $5-35 \mathrm{MHz}$ depending on the exact version, compared with approximately 1 MHz for the 3341 . Pinouts are indicated in the data sheet.

The reason for having a 5 -bit model as well as a 4-bit model of basically the same part is that if two 4-bit FIFOs are placed side-by-side they make only an 8-bit FIFO, and many people have FIFO applications which entail using a parity bit with each byte, and/or a frame-marker bit with the last byte of a frame or block, which means that they want 9-bit or 10-bit FIFOs. A67402 next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.
A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted. Likewise, a logic HIGH on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data in lines (the top of the FIFO, as it were), this word automatically sinks all the way to the bottom (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym hopper?) in keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn only in the order in which they were originally inserted.

There is no provision for random access in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401 ) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO from a magnetic-tape perspective. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.


[^34]We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00 , the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01 , the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest vacant word in the FIFO - the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO - word 63 - has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequences of this manner of operation in shift-register-technology FIFOs is that it takes quite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402 , rated at 5,7 , $10,15,16.7$ or 35 MHz over commercial ( $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ ) or military $\left(-55^{\circ} \mathrm{C}\right.$ to $\left.+125^{\circ} \mathrm{C}\right)$ temperature ranges. Thus, for instance, a $16.7-\mathrm{MHz}$ FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 60 nanoseconds. However, the "fall-through" time, ${ }^{\text {t PT }}$ for these same FIFOs is stated in the data sheet as 1.3 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00 , which should be identical to tPT, and probably is although as measured on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement By the way, the stated operating frequencies and the tpT value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice.

Besides Monolithic Memories, other manufacturers of highspeed FIFOs include Fairchild Semiconductor, Mostek, National Semiconductor, RCA, Texas Instruments, and TRW LSI Products. MOS (slow) FIFOs are available from Advanced Micro

Devices, Fairchild Semiconductor, Texas Instruments, Western Digital, Zilog, and probably other firms. FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well as parallel data ports, and additional status flags. For instance, Monolithic Memories now has the 67413 FIFO which has a "half-full" flag which tells when half of the FIFO's words contain data, and also a second flag which indicates that the FIFO is either "almost full" (within 8 words of full) or "almost empty" (within 8 words of empty), reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that some action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap around" from the highest RAM address back to zero. The outpointer chases the in-pointer, the region just traversed by the inpointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other - unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be quite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of fullblown binary counters. What this means in practice is that there are now two extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small $(16 \times 4)$ bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fallthrough time but needs proportionally more silicon area to store a given number of bits.

## Designing with FIFOs

Returning now to the Monolithic Memories 67401 and 67402, if what you really need is a "deeper". FIFO, say $128 \times 4$ instead of just $64 \times 4$, these parts are designed to cascade using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift in control input of FIFO B is connected to the Output Ready status output of FIFO A, and likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 3.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.

"...THE MONOLITHIC MEMORIES C674OI AND C67402...ARE DESIGNED TO CASCADE USING A SIMPLE 'HANDSHAKING' PROCEDURE..."


Figure 3. Cascading FIFOs to Form $128 \times 4$ FIFO
If what you really need is a "wider" FIFO, then you simply arrange $64 \times 4$ or $64 \times 5$ FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74 S 08 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 12 in the FIFO data sheet.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array - and if you chose wrongly, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungus number of 67401 s and 67402 s are in use world-wide giving hassle-free service, it should be kept in mind that these devices are asynchronous sequential circuits. (One definition of "asynchronous sequential circuit" is "a fortuitous collection of race conditions," but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setuptime and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a Master Reset. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be told to issue a Master Reset as part of your power-up sequence.) In the event that you still get what appear to be occasional errors, very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to
ground will often eliminate these. But by all means start with a good circuit board - these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1 -microfarad disk capacitors between $V_{\mathrm{CC}}$ and ground for each chip to bypass switching noise.

The sequence of events which occurs during the operation of shifting a new data word into the "top" of a FIFO is shown in Figure 3 in the FIFO data sheet, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 7 in the FIFO data sheet. In both of these figures, it has been assumed that the external logic - whether it be the rest of your system, or just another FIFO - refrains from raising the respective Shift line to HIGH until the respective Ready line has gone HIGH. If the Shift line is raised any earlier, it simply gets ignored.

When two FIFOs are cascaded as shown in Figure 3, the sequences of events shown in data-sheet Figures 3 and 7 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 3 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using. FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider data-sheet Figures 3 and 7 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 or FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go HIGH and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going HIGH. Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from data-sheet Figure 3 that the conditions for inputting a word into FIFO B have now been met, and from data-sheet Figure 7 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been met. The time delays shown in both data-sheet Figure 3 and data-sheet Figure 7 from the event at 2 to the event at 3 , and from the event at 4 to the event at 5A, are asynchronous internal-logic-determined times of the order of four or five gate delays, where the gates in question are high-speed-Schottky LSI internal gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.
Returning now to applying the timing analysis shown in datasheet Figures 3 and 7 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in
the opposite sense (falling or rising, that is) for the Ready signal from the other part. The two signals, ORA/SIB (meaning "Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain HIGH at the same time for more than a few nanoseconds, since if they are both HIGH a data word will pass between the two FIFOs as already described. So, at the point when both the sequence of events shown in data-sheet Figure 3 and the sequence of events shown in data-sheet Figure 7 have been completed, and consequently ORA/SIB and IRB/SOA have both gone HIGH again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks LOW, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks LOW, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

## Various Uses for FIFOs

The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter - it's all the same to an asynchronous FIFO such as the 67401 or 67402 , as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modus operandi is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic - or perhaps even a microprocessor - which is otherwise occupied most of the time.

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some
way for the system to sense that all is not well and halt itself. Such a record of jumps can be very valuable in tracing out what happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt - perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO per bit-stream is required - but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.
References (1), (2), and (3) are formal applications notes available from Monolithic Memories, which discuss FIFOs from different viewpoints than this paper has taken. Each of them presents a more detailed explanation of one or more applications than there has been room for here. Reference (1) is mainly an overall applications survey, reference (2) emphasizes digital communications, and reference (3) emphasizes digital spectrum analyzers and also includes an overview of digital signal processing in general.

"A LESS OBVIOUS BUT INTERESTING APPLICATION OF FIFOS IS AS AUTOMATIC 'BUS-WATCHERS'...."

## References

(1) "First In First Out Memories...Operations and Applications," applications note published March 1978 by Monolithic Memories Inc. and being reissued.
(2) "Understanding FIFO's," applications note published by Monolithic Memories Inc. The author, Alan Weissberger, has also gotten a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in Electronic Design, November 27, 1981, Despite the general title, the emphasis is on digital communications applications.
(3) "PROMs, PALs, FIFOs and Multipliers Team Up to Implement SingleBoard High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories Inc. The author, Richard Wm. Blasco, also got this note published in Electronic Design in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.

## Asynchronous First-In First-Out Memory (FIFO) 16x5 74S225/A

## Features/Benefits

- DC to $\mathbf{2 0 - M H z}$ shift-in/shift-out rates
- Fully expandable by word width and depth
- Three-state outputs
- TTL-compatible inputs and outputs
- Functionally compatible with T.I. SN74S225
- Designed for extended testability


## Description

The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) $16 \times 5$ First-In-First-Out memory (FIFO) which operates from DC to $10 / 20 \mathrm{MHz}$. The data is loaded and emptied on a

## Pin Names

| PIN\# | PIN NAME | DESCRIPTION |
| :---: | :--- | :--- |
| 1 | CLK A | Load clock A |
| 2 | IR | Input ready |
| 3 | UNCK OUT | Unload clock output |
| $4-8$ | DO-D4 | Data inputs |
| 9 | $\overline{\text { OE }}$ | Output enable |
| 10 | GND | Ground pin |
| $11-15$ | Q4-Q0 | Data outputs |
| 16 | UNCLK IN | Unload clock input |
| 17 | OR | Output ready |
| 18 | $\overline{\text { CLR }}$ | Clear |
| 19 | CLK B | Load clock B |
| 20 | VCC | Supply voltage |

## Block Diagram

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 74 S 225 | $\mathrm{~J}, \mathrm{~N}$ | 10 MHz Com |
| 74 S 225 A | $\mathrm{~J}, \mathrm{~N}$ | 20 MHz Com |

first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of $\mathrm{V}_{\mathrm{OL}}$.

## Pin Configuration



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | FIGURE | 745225 |  |  | 74S225A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 |  | 5.25 | 4.75 |  | 5.25 | V |
| $t_{A}$ | Operating free-air temperature |  | 0 |  | 75 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }_{\text {tLCKH }}$ | LOAD CLOCK pulse width, A or B, $\mathrm{t}_{\mathrm{w}}$ (HIGH) | 2 | 25 |  |  | 22 |  | 36 | ns |
| tIDS | Setup time, data to load clock | 2 | $-201^{*}$ |  |  | -201 * |  |  | ns |
| $\mathrm{t}_{\text {IDH }}$ | Hold time, data from load clock | 2 | 701 |  |  | $50 \dagger$ |  |  | ns |
| tUCKL | UNLOAD CLOCK INPUT pulse width, $\mathrm{t}_{\mathrm{w}}$ (LOW) | 4 | 7 |  |  | 7 |  | 36 | ns |
| ${ }^{\text {t CLW }}$ | CLEAR pulse width, ${ }_{\text {w }}$ (low) | 2 | 40 |  |  | 20 |  |  | ns |
| ${ }^{\text {t }}$ CLCK | Setup time, clear release to load clock, $\mathrm{t}_{\text {su }}$ | 2 | 251 |  |  | 10 |  |  | ns |

* Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).
$\dagger=$ Arrow indicates that it is referenced to the o-high transition.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | FIGURE | 745225 |  |  | 74S225A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }_{\text {fin }}$ | Load clock A or clock B | Cascade Mode** |  | 2 | 10 | 20 |  | 20 | 22 |  | MHz |
|  |  | Standalone Mode |  |  |  |  |  |  |  |  |  |
| t LCIRL | CLK A or CLK B to IR! ** |  | 2 |  | 55 | 75 |  | 43 | 55 | ns |  |
| $\mathrm{t}_{\mathrm{LCCOL}}$ | CLK A or CLK B to UNCK OUTI |  | 2 |  | 25 | 50 |  | 31 | 40 | ns |  |
| ${ }^{\text {f OUT }}$ | Unload clock input | Cascade Mode*** | 4 | 10 | 20 |  | 20 | 22 |  | MHz |  |
|  |  | Standalone Mode |  |  |  |  |  |  |  |  |  |
| tUCKORL | UNCK IN + to OR LOW |  | 4 |  | 30 | 45 |  | 26 | 35 | ns |  |
| tUCKORH | UNCK IN $\dagger$ to OR HIGH |  | 4 |  | 40 | 60 |  | 32 | 45 | ns |  |
| todh | Output data hold, UNCK IN to output data |  | 4 | 20 | 50 |  | 20 | 30 |  | ns |  |
| tods | Output data setup, UNCK IN to output data |  | 4 |  | 50 | 75 |  | 41 | 55 | ns |  |
| $\mathrm{t}_{\text {RIP }}$ | CLK A or CLK B to OR 1 |  | 7 |  | 190 | 300 |  | 167 | 220 | ns |  |
| ${ }^{\text {t CLOL }}$ | CLR to OR $\downarrow$ |  | 6 | $2 \times$ | 35 | 60 |  | 31 | 40 | ns |  |
| ${ }^{\text {t CLIH }}$ | CLR to IR 1 |  | 6 |  | 16 | 35 |  | 15 | 20 | ns |  |
| tuckow | Pulse width, UNCK OUT, $\mathrm{t}_{\text {w }}$ |  | 2 | 7 | 14 |  | 7 | 11 |  | ns |  |
| tord | OR 1 to output data |  | 4 |  | 10 | 20 |  | 9 | 15 | ns |  |
| $t_{\text {BUBI }}$ | UNCK IN to IR 1 (bubble-back time) |  | 8 |  | 255 | 400 |  | 214 | 290 | ns |  |
| $t_{\text {BUBC }}$ | UNCK IN to UNCK OUT । (bubble-back time) |  | 8 |  | 270 | 400 |  | 226 | 290 | ns |  |

[^35]
## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | 74S225 |  |  | 74S225A |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {P PHZ }}$ | Output disable delay, $\overline{O E}$ to $Q_{i}, C_{L}=5 \mathrm{pF}$ | 1 | 10 |  | 25 |  | 8 | 25 | ns |
| ${ }^{\text {t PLZ }}$ |  |  |  |  |  | 18 | 25 |  |
| ${ }^{\text {tPZL }}$ | Output enable delay, $\overline{O E}$ to $\mathrm{Q}_{\mathrm{i}}, \mathrm{C}_{\mathrm{L}}=5 \mathrm{pF}$ | 1 | 25 |  |  | 40 |  | 19 | 40 | ns |
| $\mathrm{t}_{\mathrm{PZH}}$ |  |  |  |  |  |  | 23 | 40 |  |  |

Test Load for Bi-State Output

$C L=30 \mathrm{pF}$ $R \mathrm{~L}=300 \Omega$

## Test Load for Three-State Output



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse Amplitude $=3.0 \mathrm{~V}$
Input Rise and Fall Time ( $15 \%-90 \%$ ) $=2.5$ ns
Measurements made at 1.5 V


Figure 1. Enable and Disable

[^36]
## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAM |  |  | EST CONDITIO |  | MIN TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  |  | 2.0 |  | V |
| VIC | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | $\checkmark$ |
| $\mathrm{I}_{\text {IL1 }}$ | Low-level input current | $\mathrm{D}_{0}-\mathrm{D}_{4}$ | $V_{C C}=\operatorname{MAX}$ | $V_{1}=0.5 \mathrm{~V}$ |  |  | -1 | mA |
| IIL2 |  | All others |  |  |  |  | -. 25 | mA |
| ${ }^{1} \mathrm{H}$ | High-level input current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ | Data inputs |  | 40 | A |
|  |  |  | Others |  |  | 25 | A |
| 1 | Maximum input current |  |  | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage* |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OL}}=16 \mathrm{~mA}$ (Data outputs) |  | 0.5 |  | V |
|  |  |  | $\mathrm{I}_{\mathrm{OL}}=8 \mathrm{~mA}$ (All others) |  |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OH}}=-6.5 \mathrm{~mA}$ (Data outputs) |  | 2.4 |  | V |
|  |  |  | $\mathrm{I}^{\mathrm{OH}}=-3.2 \mathrm{~mA}$ (All others) |  |  |  |  |  |
| Ios | Output short-circuit current** |  | $V_{C C}=M A X$ |  | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -30 | -100 | mA |
| $\mathrm{I}_{\mathrm{Hz}}$ | Off-state output current |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| L L |  |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ |  |  | -50 | $\mu \mathrm{A}$ |
| ${ }^{\prime} \mathrm{Cc}$ | Supply current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | Inputs low, All outputs open | 74S225 | 80 | 120 | mA |
|  |  |  | 74S225A |  | 80 | 125 |  |  |

* To measure $\mathrm{V}_{\mathrm{OL}}$ on Pin 3 , force 10 V on Pin 9 (Extended Testability).
** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


## Functional Description

## Data Input

After power up the CLEAR is pulsed low (Figure5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the $D_{x}$ inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tRIP defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

## Data Output

Data is read from the $Q_{x}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least $\mathrm{t}_{\mathrm{BUBI}}$ ) or completely empty (Output Ready stays LOW for at least tRIP).

## AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between $\mathrm{V}_{\mathrm{CC}}$ and GND with very short lead length. In addition, care must beexercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) - Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by ( $\overline{\mathrm{CLR}}$ ), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $\mathrm{tIDH}_{\mathrm{I}}$ ) and the next activity of Input Ready (tLCIRL) to beextended relative to Load Clock (A or B) going HIGH.

## 745225/A



NOTES: 1. Permissible negative setup time for input data
2. Measure t LCIRL for 16 th input word only

Figure 2 Input Timing


NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.
2. Input Data is loaded into the first word.
3. Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.
4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

Figure 3. The Mechanism of Clocking Data into the FIFO

## 74S225/A



Figure 4. Output Timing


> NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.
> 2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.
> 3. Output Ready goes LOW.
> 4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.
> 5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO


NOTE: Assume FIFO is full before $\overline{\text { CLEAR goes active. }}$
Figure 6. Clear Timing


INPUT
NOTES: 1. FIFO is initially empty.
2. Unload Clock Input and one Load Clock held HIGH throughout.

Figure 7. $\mathbf{t}_{\text {RIP }}$ Specifications


LOAD CLOCK
(A and B)

NOTES: 1. FIFO is initially full.
2. Load Clock (A and B) held HIGH throughout.

Figure 8. $t_{B U B l}$ t $_{B U B C}$ Specifications


Figure 9. $\mathbf{4 8 \times 1 0}$ FIFO with 74S225/A

## First-In First-Out (FIFO) 64x4 64x5 Cascadable Memory <br> C5/67401 C5/67401A C67401B C5/67402 C5/67402A C67402B

## Features/Benefits

- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word and bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster


## Description

The $C 5 / C 67401 B / 2 B / 1 A / 2 A / 1 / 2$ are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

## Block Diagrams



## Ordering Information

| PART NUMBER | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| C57401 | $J$ (20) (L) | Mil | $7 \mathrm{MHz} \quad 64 \times 4$ FIFO |
| C67401 | J,N,NL(20) | Com | $10 \mathrm{MHz} 64 \times 4$ FIFO |
| C57402 | $J(20)(L)$ | Mil | $7 \mathrm{MHz} 64 \times 5$ FIFO |
| C67402 | J,N,NL(20) | Com | $10 \mathrm{MHz} \quad 64 \times 5$ FIFO |
| C57401A | J,(20)(L) | Mil | $10 \mathrm{MHz} \quad 64 \times 4$ FIFO |
| C67401A | J,N,NL (20) | Com | $15 \mathrm{MHz} \quad 64 \times 4$ FIFO |
| C57402A | J, (20) (L) | Mil | $10 \mathrm{MHz} \quad 64 \times 5$ FIFO |
| C67402A | J,N,NL(20) | Com | $15 \mathrm{MHz} \quad 64 \times 5$ FIFO |
| C67401B | $J$ | Com | $16.7 \mathrm{MHz} \mathrm{64} \mathrm{\times 4} \mathrm{FIFO}$ |
| C67402B | $J$ | Com | 16.7 MHz $64 \times 5$ FIFO |



## Absolute Maximum Ratings



## Operating Conditions C67401B/2B

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }} \mathrm{SIH}^{+}$ | Shift in HIGH time | 1 | 18 |  |  | ns |
| ${ }^{\text {t SIL }}$ | Shift in LOW time | 1 | 18 |  |  | ns |
| ${ }_{\text {I IDS }}$ | Input data setup | 1 | 0 |  |  | ns |
| ${ }^{\text {tIDH }}$ | Input data hold time | 1 | 40 |  |  | ns |
| ${ }^{\text {t }} \mathrm{SOH}^{+}$ | Shift Out HIGH time | 5 | 18 |  |  | ns |
| ${ }^{\text {t }} \mathrm{SOL}$ | Shift Out LOW time | 5 | 18 |  |  | ns |
| ${ }_{\text {t MRW }}$ | Master Reset pulse | 10 | 35 |  |  | ns |
| ${ }^{\text {t MRS }}$ | Master Reset to SI | 10 | 35 |  |  | ns |

## Switching Characteristics C67401B/2B

Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP MAX |  |
| ${ }^{\text {f }} \mathrm{N}$ | Shift in rate | 1 | 16.7 |  | MHz |
| ${ }^{\text {t }}$ IRL | Shift In to Input Ready LOW | 1 |  | 35 | ns |
| ${ }_{\text {t }}^{\text {R }}{ }^{\text {+ }}$ | Shift In to Input Ready HIGH | 1 |  | 37 | ns |
| fout | Shift Out rate | 5 | 16.7 |  | MHz |
| ${ }^{\text {O ORL }}{ }^{\dagger}$ | Shift Out to Output Ready LOW | 5 |  | 38 | ns |
| ${ }^{\text {O ORH }}{ }^{\dagger}$ | Shift Out to Output Ready HIGH | 5 |  | 48 | ns |
| ${ }^{\text {todH }}$ | Output Data Hold (previous word) | 5 | 5 |  | ns |
| ${ }^{\text {t ODS }}$ | Output Data Shift (next word) | 5 |  | 44 | ns |
| ${ }_{\text {t }}^{\text {PT }}$ | Data throughput or "fall through" | 4, 8 |  | 1.45 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$ | Master Reset to OR LOW | 10 |  | 55 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  | 55 | ns |
| ${ }^{1} \mathrm{PPH}^{*}$ | Input Ready pulse HIGH | 4 | 20 |  | ns |
| ${ }^{\text {OPPH }}$ * | Output Ready pulse HIGH | 8 | 20 |  | ns |

$\dagger$ See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.


## Operating Conditions C5/C67401A/2A

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | $\checkmark$ |
| ${ }^{\text {T }}$ A | Operating free-air temperature |  | -55 |  | *125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }_{\text {SIH }}{ }^{\text {d }}$ | Shift in HIGH time | 1 | 35 |  |  | 23 |  |  | ns |
| ${ }^{\text {tSIL }}$ | Shift in LOW time | 1 | 35 |  |  | 25 |  |  | ns |
| IIDS | Input data setup | 1 | 0 |  |  | 0 |  |  | ns |
| ${ }_{1}{ }^{\text {d }}$ ( ${ }^{\text {d }}$ | Input data hold time | 1 | 45 |  |  | 40 |  |  | ns |
| ${ }^{\text {t }}{ }^{\text {SOH }}{ }^{+}$ | Shift Out HIGH time | 5 | 35 |  |  | 23 |  |  | ns |
| ${ }^{\text {t }}$ SOL | Shift Out LOW time | 5 | 35 |  |  | 25 |  |  | ns |
| tMRW | Master Reset pulse | 10 | 40 |  |  | 35 |  |  | ns |
| ${ }^{\text {tMRS }}$ | Master Reset to SI | 10 | 45 |  |  | 35 |  |  | ns |

## Switching Characteristics C5/C67401A/2A Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{f}_{\mathrm{IN}}$ | Shift in rate | 1 | 10 |  |  | 15 |  |  | MHz |
| $\mathrm{t}_{\text {IRL }}{ }^{+}$ | Shift In to Input Ready LOW | 1 |  |  | 50 |  |  | 40 | ns |
| ${ }^{\text {t/ }} \mathrm{RH}^{+}$ | Shift In to Input Ready HIGH | 1 |  |  | 50 |  |  | 40 | ns |
| fout | Shift Out rate | 5 | 10 |  |  | 15 |  |  | MHz |
| ${ }^{\text {O ORL }}{ }^{+}$ | Shift Out to Output Ready LOW | 5 |  |  | 65 |  |  | 45 | ns |
| ${ }^{\text {O }} \mathrm{ORH}^{+}$ | Shift Out to Output Ready HIGH | 5 |  |  | 65 |  |  | 50 | ns |
| ${ }^{\mathrm{t}} \mathrm{ODH}$ | Output Data Hold (previous word) | 5 | 10 |  |  | 10 |  |  | ns |
| tods | Output Data Shift (next word) | 5 |  |  | 60 |  |  | 45 | ns |
| ${ }_{\text {tPT }}$ | Data throughput or "fall through" | 4, 8 |  |  | 2.2 |  |  | 1.6 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$. | Master Reset to OR LOW | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }_{1 / \mathrm{PH}}{ }^{*}$ | Input Ready pulse HIGH | 4 | 30 |  |  | 23 |  |  | ns |
| ${ }^{\text {t }} \mathrm{OPH}^{*}$ | Output Ready pulse HIGH | 8 | 30 |  |  | 23 |  |  | ns |

[^37]* This parameter applies to FIFOs communicating with each other in a cascaded mode.


## Absolute Maximum Ratings

| Supply voltage |
| :---: |
| Input voltage |
| Off-state output voltage |
|  |

## Operating Conditions C5/C67401/2

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature |  | -55 |  | *125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }} \mathrm{SIH}^{+}$ | Shift in HIGH time | 1 | 45 |  |  | 23 |  |  | ns |
| ${ }^{\text {t SIL }}$ | Shift in LOW time | 1 | 45 |  |  | 35 |  |  | ns |
| tids | Input data setup | 1 | 0 |  |  | 0 |  |  | ns |
| tidh | Input data hold time | 1 | 55 |  |  | 45 |  |  | ns |
| ${ }^{\text {}} \mathrm{SOH}^{+}$ | Shift Out HIGH time | 5 | 45 |  |  | 23 |  |  | ns |
| ${ }^{\text {t SOL }}$ | Shift Out LOW time | 5 | 45 |  |  | 35 |  |  | ns |
| tMRW | Master Reset pulse | 10 | 30 |  |  | 35 |  |  | ns |
| ${ }^{\text {t MRS }}$ | Master Reset to SI | 10 | 45 |  |  | 35 |  |  | ns |

* Case temperature.


## Switching Characteristics C5/C67401/2 Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\mathrm{f}} \mathrm{N}$ | Shift in rate | 1 | 7 |  |  | 10 |  |  | MHz |
| $\mathrm{t}_{\text {IRL }}{ }^{+}$ | Shift In to Input Ready LOW | 1 |  |  | 60 |  |  | 45 | ns |
| ${ }_{\text {t }}^{\text {R }}{ }^{\text {d }}{ }^{+}$ | Shift In to Input Ready HIGH | 1 |  |  | 60 |  |  | 45 | ns |
| fout | Shift Out rate | 5 | + 7 |  |  | 10 |  |  | MHz |
| ${ }^{\text {O ORL }}{ }^{+}$ | Shift Out to Output Ready LOW | 5 |  |  | 65 |  |  | 55 | ns |
| ${ }^{\text {toRH }}{ }^{\dagger}$ | Shift Out to Output Ready HIGH | 5 |  |  | 70 |  |  | 60 | ns |
| $\mathrm{t}_{\mathrm{ODH}}$ | Output Data Hold (previous word) | 5 | 10 |  |  | 10 |  |  | ns |
| tods | Output Data Shift (next word) | 5 |  |  | 65 |  |  | 55 | ns |
| ${ }^{\text {tPT }}$ | Data throughput or "fall through" | 4, 8 |  |  | 4 |  |  | 3 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$ | Master Reset to OR LOW | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }_{1 / 8 H^{*}}$ | Input Ready pulse HIGH | 4 | 30 |  |  | 23 |  |  | ns |
| ${ }^{\text {toPH }}$ * | Output Ready pulse HIGH | 8 | 30 |  |  | 23 | 4 |  | ns |

$\dagger$ See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

## Test Load

Input Pulse 0 to 3 V
Input Rise and Fall Time ( $10 \%-90 \%$ )
5 ns minimum
Measurements made at 1.5 V

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  | , |  |  | $0.8 \dagger$ | V |
| $V_{1 H}$ | High-level input voltage |  |  |  | $2 \dagger$ |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| IIL1 | Low-level input current | $D_{0}-D_{n}, \overline{M R}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $V_{1}=0.45 \mathrm{~V}$ |  |  | -0.8 | mA |
| IIL.2 |  | SI, SO |  |  |  |  | -1.6 | mA |
| $\mathrm{I}_{1 \mathrm{H}}$ | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V C C=M A X$ | $V_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | ${ }^{1} \mathrm{OL}=8 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $V_{\text {CC }}=\mathrm{MIN}$ | ${ }^{\mathrm{OHH}}=-0.9 \mathrm{~mA}$ | 2.4 |  |  | $\checkmark$ |
| - | Output short-circuit current * |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX} \quad \mathrm{V}_{0}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current |  | $V_{C C}=M A X$ <br> Inputs low, outputs open | C5/67401 |  |  | 160 | mA |
|  |  |  | C5/67402 |  |  | 180 |  |
|  |  |  | C67401A |  |  | 170 |  |
|  |  |  | C6702A |  | 4 | 190 |  |
|  |  |  | C67401B, C57401A |  |  | 180 |  |
|  |  |  | C67402B, C57402A | 5an |  | 200 |  |

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ There are absolute voltage with respect to device GND (Pin 8 or 9 ) and includes all overshoots due to test equipment

## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Fig, 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{x}$ inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneousiy, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

## Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tPT defines the time required for the first data to travel from input to the output of a previously empty device.

## Data Output

Data is read from the Ox outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes

HIGH. If the FIFO is emptied, OR stays LOW, and $O_{x}$ remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least tPT).

## AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 $\mu \mathrm{F}$ directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t|DH) and the next activity of Input Ready (IIRL) to be extended relative to ShiftIn going High. This same type of problem is also related to tIRH, tORL and tORH as related to Shift-Out.

C5/C67401A/2A/1/2, C67401B/2B Cascadable


Figure 1. Input Timing


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate


INPUT DATA


Figure 3. The Mechanism of Shifting Data Into the FIFO
(1) Input Ready HIGH indicates space is available and a Shift in pulse may be applied.
(2) Input Data is loaded into the first word.
(3) Input Ready goes LOW indicating the first word is full
(4) The Data from the first word is released for "fall-through" to second word
(51) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

58 If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. NOTE: Shift In puises applied while Input Ready is LOW will be ignored (See Figure 4).


Figure 4. Data is Shifted in Whenever Shift in and Input Ready are Both HIGH
(1) FIFO is initially full
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift in is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.

(1) The diagram assumes, that at this time, words $63,62,61$ are loaded with A, B, C Data, respectively.
(2) Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate
(1) The diagram assumes, that at this time, words $63,62,61$ are loaded with $A, B, C$ Data, respectively. (2) Data in the crosshatched region may be $A$ or $B$ Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO.
(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
(2) Shift Out goes HIGH causing the next step.
(3) Output Ready goes LOW
(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs
(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs
NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

(1) FIFO initially empty.

Figure 8. $\mathrm{t}_{\mathrm{PT}}$ and $\mathrm{t}_{\mathrm{OPH}}$ Specification
SHIFT OUT (5)


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.
(1) Word 63 is empty.
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW
(2) New data (A) arrives at the outputs (word 63)
(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed tine on Output Ready.
(3) Output Ready goes HIGH indicating the arrival of the new data



Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.


Figure 12. 192×12 FIFO with C5/C67401/1A/1B

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

## Applications



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100 ns . If 100 ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate


NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application

## First-In First-Out (FIFO) 64x4 64x5 Standalone Memory

## 5/67401 5/67401A 67401B 5/67402

## Features/Benefits

- Choice of $16.7,15$ and 10 MHz shift-out/shift-in rates
- Choice of 4 -bit or 5 -bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times as fast


## Description

The $5 / 67401 \mathrm{~B} / 2 \mathrm{~B} / 1 \mathrm{~A} / 2 \mathrm{~A} / 1 / 2$ are "fall-through" high speed FirstIn First-Out (FIFO) memory organized 64 words by 4 -bits and 64 words by 5 -bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | DESCRIPTION |  |  |
| :---: | :---: | :---: | :---: | :---: | :--- |
| 57401 | $\mathrm{~J}(20)(\mathrm{L})$ | Mil | 7 MHz | $64 \times 4$ | FIFO |
| 67401 | $\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)$ | Com | 10 MHz | $64 \times 4$ | FIFO |
| 57402 | $\mathrm{~J}(20)(\mathrm{L})$ | Mil | 7 MHz | $64 \times 5$ | FIFO |
| 67402 | $\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)$ | Com | 10 MHz | $64 \times 5$ | FIFO |
| 57401 A | $\mathrm{~J},(20)(\mathrm{L})$ | Mil | 10 MHz | $64 \times 4$ | FIFO |
| 67401 A | $\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)$ | Com | 15 MHz | $64 \times 4$ | FIFO |
| 57402 A | $\mathrm{~J},(20)(\mathrm{L})$ | Mil | 10 MHz | $64 \times 5$ | FIFO |
| 67402 A | $\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)$ | Com | 15 MHz | $64 \times 5$ | FIFO |
| 67401 B | J | Com | $16.7 \mathrm{MHz} 64 \times 4$ FIFO |  |  |
| 67402 B | J | Com | $16.7 \mathrm{MHz} 64 \times 5$ FIFO |  |  |

## Block Diagrams



5/67402/A/B 64x5 57402/A 64x5


Pin Configurations


Plastic Chip Carrier


## Absolute Maximum Ratings

| Supply voltage $\mathrm{V}_{\mathrm{CC}}$ |
| :---: |
| Input voltage |
| Off-state output voltage |
| Storage temperature . ........................................................................................ $-65^{\circ}$ to $+150^{\circ}$ |

## Operating Conditions 67401B/2B

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| $V_{\text {CC }}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $T_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {S SIH }}{ }^{\dagger}$ | Shift in HIGH time | 1 | 18 |  |  | ns |
| ${ }^{\text {t SIL }}$ | Shift in LOW time | 1 | 18 |  |  | ns |
| tids | Input data setup | 1 | 5 |  |  | ns |
| ${ }^{\text {t }} \mathrm{IDH}$ | Input data hold time | 1 | 40 |  |  | ns |
| ${ }^{\text {t }} \mathrm{SOH}^{\dagger}$ | Shift Out HIGH time | 5 | 18 |  |  | ns |
| ${ }^{\text {t }} \mathrm{SOL}$ | Shift Out LOW time | 5 | 18 |  |  | ns |
| ${ }^{\text {t MRW }}$ | Master Reset pulse | 10 | 35 |  |  | ns |
| $t_{\text {MRS }}$ | Master Reset to SI | 10 | 35 |  |  | ns |

## Switching Characteristics 67401B/2B

## Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP MAX |  |
| $\mathrm{fiN}^{\text {N }}$ | Shift in rate | 1 | 16.7 |  | MHz |
| IIRL | Shift In to input ready LOW | 1 |  | 35 | ns |
| tIRH | Shift in to input ready HIGH | 1 |  | 37 | ns |
| fout | Shift Out rate | 5 | 16.7 |  | MHz |
| ${ }^{\text {t ORL }}{ }^{+}$ | Shift Out to Output Ready LOW | 5 |  | 38 | ns |
| ${ }^{\text {t }} \mathrm{ORH}^{+}$ | Shift Out to Output Ready HIGH | 5 |  | 48 | ns |
| ${ }^{\text {tod }}$ | Output Data Hold (previous word) | 5 | 5 |  | ns |
| tods | Output Data Shift (next word) | 5 |  | 44 | ns |
| ${ }^{\text {tPT }}$ | Data throughput or "fall through" | 4,8 |  | 1.45 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$ | Master Reset to OR LOW | 10 |  | 55 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  | 55 | ns |
| IIPH | Input Ready pulse HIGH | 4 | 15 |  | ns |
| ${ }^{\text {t OPH }}$ | Output Ready pulse HIGH | 8 | 15 |  | ns |

$\dagger$ See AIC Test and High Speed Application Note.

## Absolute Maximum Ratings



Operating Conditions 5/67401A/2A

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $V_{\text {CC }}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | *125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {S }} \mathrm{SIH}^{+}$ | Shift in HIGH time | 1 | 35 |  |  | 23 |  | $28 \dagger$ | ns |
| ${ }^{\text {t SIL }}$ | Shift in LOW time | 1 | 35 |  |  | 25 |  |  | ns |
| ${ }_{\text {I IDS }}$ | Input data setup | 1 | 5 |  |  | 5 |  |  | ns |
| ${ }^{\text {tidH }}$ | Input data hold time | 1 | 45 |  |  | 40 |  |  | ns |
| ${ }^{\text {t }} \mathrm{SOH}^{+}$ | Shift Out HIGH time | 5 | 35 |  |  | 23 |  |  | ns |
| ${ }^{\text {t SOL }}$ | Shift Out LOW time | 5 | 35 |  |  | 25 |  |  | ns |
| ${ }^{\text {t MRW }}$ | Master Reset pulse | 10 | 40 |  |  | 35 |  |  | ns |
| ${ }^{\text {t MRS }}$ | Master Reset to SI | 10 | 45 |  |  | 35 |  |  | ns |

* Case temperature.


## Switching Characteristics 5/67401A/2A

Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{f}_{\mathrm{IN}}$ | Shift in rate | 1 | 10 |  |  | 15 |  |  | MHz |
| $\mathrm{t}_{\text {IRL }}{ }^{+}$ | Shift In to Input Ready LOW | 1 |  |  | 50 |  |  | 40 | ns |
| ${ }_{\text {t }}^{1 \mathrm{RH}^{+}}$ | Shift In to Input Ready HIGH | 1 |  |  | 50 |  |  | 40 | ns |
| ${ }^{\text {fout }}$ | Shift Out rate | 5 | 10 |  |  | 15 |  |  | MHz |
| ${ }^{\text {torL }}{ }^{+}$ | Shift Out to Output Ready LOW | 5 |  |  | 65 |  |  | 45 | ns |
| ${ }^{\text {t }}{ }^{\text {ORH }}{ }^{\dagger}$ | Shift Out to Output Ready HIGH | 5 |  |  | 65 |  |  | 50 | ns |
| ${ }^{\text {todH }}$ | Output Data Hold (previous word) | 5 | 10 |  |  | 10 |  |  | ns |
| ${ }^{\text {tods }}$ | Output Data Shift (next word) | 5 |  |  | 60 |  |  | 45 | ns |
| ${ }^{t}{ }^{\text {PT }}$ | Data throughput or "fall through" | 4, 8 |  |  | 2.2 |  |  | 1.6 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$ | Master Reset to OR LOW | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }^{\text {I IPH }}$ | Input Ready pulse HIGH | 4 | 20 |  |  | 20 |  |  | ns |
| ${ }^{\text {t }} \mathrm{OPH}$ | Output Ready pulse HIGH | 8 | 20 |  |  | 20 |  |  | ns |

## Absolute Maximum Ratings



Storage temperature ............................................................................................. $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions 5/67401/2

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $V_{\text {CC }}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | $\checkmark$ |
| ${ }^{T}$ A | Operating free-air temperature |  | -55 |  | *125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {S }} \mathrm{SHH}^{+}$ | Shift in HIGH time | 1 | 45 |  |  | 35 |  |  | ns |
| ${ }^{\text {t SiL }}$ | Shift in LOW time | 1 | 45 |  |  | 35 |  |  | ns |
| ${ }_{\text {IIDS }}$ | Input data setup | 1 | 10 |  |  | 5 |  |  | ns |
| ${ }^{\text {I IDH }}$ | Input data hold time | 1 | 55 |  |  | 45 |  |  | ns |
| ${ }^{\text {'SOH }}{ }^{\text {¢ }}$ | Shift Out HIGH time | 5 | 45 |  |  | 35 |  |  | ns |
| ${ }^{\text {t SOL }}$ | Shift Out LOW time | 5 | 45 |  |  | 35 |  |  | ns |
| ${ }^{\text {t MRW }}$ | Master Reset pulset | 10 | 30 |  |  | 35 |  |  | ns |
| ${ }^{\text {t MRS }}$ | Master Reset to SI | 10 | 45 |  |  | 35 |  |  | ns |

## * Case temperature

## Switching Characteristics 5/67401/2

Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{f}_{\mathrm{IN}}$ | Shift in rate | 1 | 7 |  |  | 10 |  |  | MHz |
| ${ }^{\text {I }}{ }^{\text {L }}{ }^{+}$ | Shift In to input ready LOW | 1 |  |  | 60 |  |  | 45 | ns |
| ${ }_{\text {t } \mathrm{RRH}^{+}}$ | Shift In to input ready HIGH | 1 |  |  | 60 |  |  | 45 | ns |
| ${ }^{\text {fout }}$ | Shift Out rate | 5 | 7 |  |  | 10 |  |  | MHz |
| ${ }^{\text {t ORL }}{ }^{\text {t }}$ | Shift Out to Output Ready LOW | 5 |  |  | 65 |  |  | 55 | ns |
| ${ }^{\text {TORH }}$ | Shift Out to Output Ready HIGH | 5 |  |  | 70 |  |  | 60 | ns |
| ${ }^{\text {t }} \mathrm{ODH}$ | Output Data Hold (previous word) | 5 | 10 |  |  | 10 |  |  | ns |
| toDS | Output Data Shift (next word) | 5 |  |  | 65 |  |  | 55 | ns |
| ${ }^{\text {tPT }}$ | Data throughput or "fall through" | 4,8 |  |  | 4 |  |  | 3 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$ | Master Reset to OR LOW | 10 |  |  | 65 |  |  | 60 | ns |
| ${ }_{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  |  | 65 |  |  | 60 | ns |
| $\mathrm{t}_{\mathrm{IPH}}$ | Input Ready pulse HIGH | 4 | 20 |  |  | 20 |  |  | ns |
| ${ }^{\text {t OPH }}$ | Output Ready pulse HIGH | 8 | 20 |  |  | 20 |  |  | ns |

$\dagger$ See AC test and high speed application note.

## Test Load

* The "TEST POINT" is driven by the output under test,
and observed by instrumentation.


Input Pulse 0 to 3 V
Input Rise and Fall Time ( $10 \%-90 \%$ )
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage |  |  |  |  |  | $0.8 \dagger$ | $V$ |
| $V_{1 H}$ | High-level input voltage |  |  |  | $2 \dagger$ |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \quad 11=-18 \mathrm{~mA}$ |  |  |  | $-1.5$ | V |
| ILI | Low-level input current | $\mathrm{D}_{0}-\mathrm{D}_{\mathrm{n}}, \overline{\mathrm{MR}}$ | $V_{C C}=$ MAX $\quad V_{1}=0.45 \mathrm{~V}$ |  |  |  | -0.8 | mA |
| 1162 |  | SI, SO |  |  |  |  | -1.6 | mA |
| 1 IH | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $\mathrm{VCC}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $V_{C C}=\mathrm{MIN}$ | ${ }^{1} \mathrm{OL}=8 \mathrm{~mA}$ |  |  | 0.5 | $\checkmark$ |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | ${ }^{1} \mathrm{OH}=-0.9 \mathrm{~mA}$ | 2.4 |  |  | V |
| 'os | Output short-circuit current * |  | $V_{C C}=$ MAX $\quad V_{0}=0 \mathrm{~V}$ |  | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current |  | $V_{C C}=M A X$ <br> Inputs low, outputs open. | 5/67401 |  |  | 160 |  |
|  |  |  | 5/67402 |  |  | 180 |  |
|  |  |  | 67401A |  |  | 170 |  |
|  |  |  | 67402A |  |  | 190 |  |
|  |  |  | 67401B, 57401A |  |  | 180 |  |
|  |  |  | 67402B, 57402A |  |  | 200 |  |

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second
$\dagger$ There are absolute voltages with respect to degree GND (PIN 8 or 9 ) and includes all overshoots due to test equipment.


## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift $\operatorname{In}(\mathrm{SI})$ is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

## Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpT defines the time required for the first data to travel from input to the output of a previously empty device.

## Data Output

Data is read from the Ox outputs. When data is shifted to the output stage. Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes

HIGH. If the FIFO is emptied, OR stays LOW, and $O_{x}$ remains as before, (i.e. data does not change if FIFO is empty).
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tpT) or completely empty (Output Ready stays LOW for at least tpT).

## AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between $\mathrm{V}_{\mathrm{CC}}$ and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (tIDH) and the next activity of Input Ready (t|RL) to be extended relative to Shift-In going High. This same type of problem is also related to tIRH, tORL and tORH as related to Shift-Out.


Figure 1. Input Timing


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)


INPUT DATA


Figure 3. The Mechanism of Shifting Data Into the FIFO
(1)

Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
(2) Input Data is loaded into the first word
(3) Input Ready goes LOW indicating the first word is full.
(4) The Data from the first word is released for "fall-through" to second word.
(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
(58) If the second word is already full then the data remains at the first word Since the FIFO is now full input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.


Figure 5. Output Timing
(1) The diagram assumes. that at this time words $63,62.61$ are loaded with A B. C Data, respectively
(2) Data is shifted out when Shift Out makes a HIGH to LOW transition.


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)
(1) The diagram assumes, that at this time, words $63,62.61$ are loaded with $A, B, C$ Data, respectively
(2) Data in the crosshatched region may be $A$ or $B$ Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO.
(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
(2) Shift Out goes HIGH causing the next step.
(3) Output Ready goes LOW.
(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
(5A) Output Ready goes HIGH indicating that new data $(B)$ is now available at the FIFO outputs.
(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.


Figure 8. $t_{\text {PT }}$ and $t_{O P H}$ Specification
(1) FIFO initially empty.

SHIFT OUT


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.
(1) Word 63 is empty.
(2) New data (A) arrives at the outputs (word 63).
(3) Output Ready goes HIGH indicating the arrival of the new data
(4) Since Shift Out is held HIGH. Output Ready goes immediately LOW
(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.


Figure 10. Master Reset Timing
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(1) FIFO initially full

# First-In First-Out (FIFO) <br> $64 \times 4$ 64x5 Memory 15 MHz (Cascadable) 

C67L401D
C67L402D

## Features/Benefits

- High-speed $15-\mathrm{MHz}$ shift-in/shift-out rates
- Low power consumption
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in word width and depth
- Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation

Ordering Information

| PART | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| C6MBER |  |  |  |

C67L401D
(C67L402D)

## Description

The C67L401D/2D are "fall-through" high-speed First-In FirstOut (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. They feature high-drive ( $1 \mathrm{OL}=24 \mathrm{~mA}$ ) outputs.

## $\square$



## Pin Configurations



## Absolute Maximum Ratings


Input voltage .............................................................................................................. -1.5 V to 7 V
Off-state output voltage . .................................................................................................... . -0.5 V to 5.5 V
Storage temperature . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions Over Temperature Range

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL <br> TYP | MAX |
| :--- | :--- | :--- | :--- | :---: | :---: | UNIT

* If the FIFO is not full (IR High), $\overline{M R}$ low forces iR low, followed by IR returning high when $\overline{M R}$ goes high.
** See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITION |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8** | V |
| $\mathrm{V}_{1 \mathrm{H}}$ | High-level input voltage |  |  |  | $2^{* *}$ |  |  | V |
| VIC | Input clamp voltage |  | $V_{C C}=\mathrm{MIN}$ | $11=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| IIL | Low-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.45 \mathrm{~V}$ |  |  | -250 | $\mu \mathrm{A}$ |
| IIH | High-level input current |  | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=$ MAX | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{VOL}_{\text {OL }}$ | Low-leve! Output voltage | Output, O | $V_{C C}=$ MIN | $1 \mathrm{OL}=24 \mathrm{~mA}$ |  |  | 0.5 | V |
|  |  | IR, OR | $V_{C C}=$ MIN | $\mathrm{lOL}=8 \mathrm{~mA}$ |  |  |  |  |
| VOH | High-level Output voltage | Output, O | $V_{C C}=M 1 N$ | $1 \mathrm{OH}=-3.0 \mathrm{~mA}$ | 2.4 |  |  | V |
|  |  | IR, OR | $V_{C C}=$ MIN | $\mathrm{IOH}=-0.9 \mathrm{~mA}$ |  |  |  |  |
| Ios | Output short-circuit current* |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ICC | Supply current |  | $V_{C C}=M A X$ <br> All inputs low. <br> All outputs open. | L401D/2D |  |  | 100 | mA |

[^38]
## C67L401D C67L402D

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL MAX TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| tIRL $\dagger$ | Shift In 1 to Input Ready LOW | 1 |  | 40 | ns |
| ${ }_{\text {t }}$ RH ${ }^{\text {¢ }}$ | Shift In $\mid$ to Input Ready HIGH |  |  | 26 | ns |
| torlt $\dagger$ | Shift Out t to Output Ready LOW | 5 |  | 45 | ns |
| torn ${ }^{\dagger}$ | Shift Out / to Output Ready HIGH |  |  | 50 | ns |
| toDHt | Output Data Hold (previous word) |  | 12 |  | ns |
| tods | Output Data Shift (next word) |  |  | 40 | ns |
| tpT | Data throughput | 4,8 |  | 1600 | ns |
| TMRORL | Master Reset 1 to Output Ready LOW | 10 |  | 60 | ns |
| tMRIRH* | Master Reset 1 to Input Ready HIGH |  |  | 30 | ns |
| tMRIRL* | Master Reset / to Input Ready LOW |  |  | 50 | ns |
| tMRO | Master Reset \| to Outputs LOW |  |  | 60 | ns |
| tIPH | Input ready pulse HIGH | 4 | 17 |  | ns |
| tOPH | Output ready pulse HIGH | 8 | 24 |  | ns |
| tord | Output ready $\dagger$ to Data Valid | 5 |  | $-3$ | ns |

* If the FIFO is not full (IR High), $\overline{M R}$ low forces IR low, followed by IR returning high when $\overline{M R}$ goes high.
$\dagger$ See AC test and high-speed application note.


## Standard Test Load



Input Pulse Amplitude $=3 \mathrm{~V}$
Input Rise and Fall Time $(10 \%-90 \%)=2.5 \mathrm{~ns}$
Measurements made at 1.5 V

## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the $D_{X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tPT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

## Data Output

Data is read from the $O_{X}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage,

| IOL | R1 | R2 |
| :---: | :---: | :---: |
| 24 mA | $200 \Omega$ | $300 \Omega$ |
| 8 mA | $600 \Omega$ | $1200 \Omega$ |

OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least tPT).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input

Data Hold time (TIDH) and the next activity of Input Ready (TIRL) to be extended relative to shift-in going HIGH. This same type of situation occurs with TORL and TORH as related to

Shift-Out. For high-speed applications, proper grounding technique is essential.


Figure 1. Input Timing


Figure 2. Typical Waveforms for $15-\mathrm{MHz}$ Shift-In Rate


Figure 3. The Mechanism of Shifting Data into the FIFO
(1) Input Feady HIGH indicates space is available and a Shift-in pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift in is held HIGH
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.


Figure 5. Output Timing
(1) The diagram assumes that at this time, words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.


Figure 6. Typical Waveforms for $15-\mathrm{MHz}$ Shift-Out Data Rate
(1) The diagram assumes that at this time words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Data in the first crosshatched region may be A or B Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63 . Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.


Figure 8. $\mathbf{t}_{\mathbf{P T}}$ and $\mathrm{t}_{\mathrm{OPH}}$ Specification
(1) FIFO initially empty.
(2) Shift Out held HIGH


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.
(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 63).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

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Figure 10. Master Reset Timing

## Low Power <br> First-In First-Out (FIFO) 64x4 Memory 67L401

## Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low Power Consumption
- TTL inputs and outputs
- Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and much faster


## Description

The 67L401 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a $64 \times 4$-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67 L 401 is particularly useful where low-power consumption is critical.

## Pin Configurations



## Ordering Information

| PART <br> NUMBER | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| 67 L 401 | N, NL | COM | $5 \mathrm{MHz} 64 \times 4$ FIFO |
| 67 L 401 | J, NL | COM | $5 \mathrm{MHz} 64 \times 4$ FIFO |

## Block Diagram

## 67L401 64×4



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## Absolute Maximum Ratings



## Operating Conditions



## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| fiN | Shift in rate | 1 | 5 |  |  | MHz |
| ${ }_{\text {I IRL }}{ }^{\dagger}$ | Shift in to Input Ready LOW | 1 |  |  | 75 | ns |
| ${ }_{\text {IR }}{ }^{\text {H }}{ }^{\dagger}$ | Shift in to Input Ready HIGH | 1 |  |  | 75 | ns |
| ${ }^{\text {fout }}$ | Shift Out rate | 5 | 5 |  |  | MHz |
| tork $\dagger$ | Shift Out to Output Ready LOW | 5 |  |  | 75 | ns |
| ${ }^{\text {t ORH }}{ }^{\dagger}$ | Shift Out to Output Ready HIGH | 5 |  |  | 80 | ns |
| tod | Output Data Hold (previous word) | 5 | 8 |  |  | ns |
| tods | Output Data Shift (next word) | 5 |  |  | 70 | ns |
| ${ }^{\text {tPT }}$ | Data throughput or "fall through" | 4,8 |  |  | 4 | $\mu \mathrm{s}$ |
| ${ }^{\text {t MRORL }}$ | Master Reset to OR LOW | 10 |  |  | 85 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset to IR HIGH | 10 |  |  | 85 | ns |
| ${ }^{\text {t/ }}{ }^{\text {PH }}{ }^{*}$ | Input Ready pulse HIGH | 4 | 20 |  |  | ns |
| ${ }^{1} \mathrm{OPH}^{*}$ | Output Ready pulse HIGH | 8 | 20 |  |  | ns |

$\dagger$ See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.


## Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

| 5 V | Input Pulse 0 to 3 V <br> Input Rise and Fall Time (10\% -90\%) |
| :--- | :--- |
| $560 \Omega$ | 5 ns minimum |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | $2 \dagger$ |  |  | V |
| $V_{1 C}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $1=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\begin{aligned} & I_{I L 1} \\ & I_{I L 2} \end{aligned}$ | Low-level input current | $\begin{aligned} & D_{0}-D_{3} M R \\ & \text { SI, SO } \end{aligned}$ | $V_{C C}=M A X$ | $V_{1}=0.45 \mathrm{~V}$ |  |  | $\begin{array}{r} -0.8 \\ -1.6 \end{array}$ | $\mathrm{mA}$ |
| $\mathrm{I}_{\mathrm{IH}}$ | High-level input current |  | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | $\mathrm{I}^{\mathrm{OL}}=8 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $V_{C C}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OH}}=-0.9 \mathrm{~mA}$ | 2.4 |  |  | V |
| Ios | Output short-circuit current* |  | $V_{C C}=M A X$ | $\mathrm{V}_{0}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{Cc}$ | Supply Current |  | $V_{C C}=M A X$ | Low, Outputs Open |  | 95 | 110 | mA |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ This is an absolute voltage with respect to device GND (Pin 8 or 9 ) and includes all overshoots due to test equipment.


## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{x}$ inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

## Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpT defines the time required for the first data to travel from input to the output of a previously empty device.

## Data Output

Data is read from the $O_{x}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and $O_{x}$ remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least t ${ }^{\text {PT }}$ ).

## AC Test and Application Note

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing. Though the external data rate is 5 MHz internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO will respond to very small glitches caused by long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between $\mathrm{V}_{\mathrm{CC}}$ and GND with very short lead length. In addition, care must be exercised in timing set up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination, as well as the Shift Out-Output Ready Combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until InputReady is High.If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time ( $\mathrm{t} \mid \mathrm{DH}$ ) and the next activity of Input Ready (tIRL) to be extended relative to Shift-In going High.

## 67 L401



Figure 1. Input Timing


Figure 2. Typical Waveforms for $5-\mathrm{MHz}$ Shift In Data Rate


Figure 3. The Mechanism of Shifting Data Into the FIFO
(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied
(2) Input Data is loaded into the first word.
(3) Input Ready goes LOW indicating the first word is full.
(4) The Data from the first word is released for "fall-through" to second word
(5) The Data from the first word is transferred to second word The first word is now empty as indicated by Input Ready HIGH.
(58) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.

(1) The diagram assumes, that at this time, words 63.62 .61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate
(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with $A, B, C$ Data, respectively (2) Data in the crosshatched region may be A or B Data


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1)

Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
(2) Shift Out goes HIGH causing the next step.
(3) Output Ready goes LOW
(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
(5A) Output Ready goes HIGH indicating that new data $(B)$ is now available at the FIFO outputs.
(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs


Figure 9. Data is, Shifted Out Whenever Shift Out and Output Ready are Both HIGH
(1) Word 63 is empty.
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(2) New data (A) arrives at the outputs (word 63).
(3) Output Ready goes HIGH indicating the arrival of the new data.
(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

(1) FIFO initially full.

Figure 10. Master Reset Timing


Figure 12. 64x8 FIFO With Two 67L401's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

## Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.


The 67 L401 can also be used in a bidirectional operation as shown in Figure 14.


NOTE: Both depth and width expansion can be used in this mode.

Figure 13. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate

Figure 14. Bidirectional FIFO Application

# Low Power First-In First-Out (FIFO) 64x5 Memory 67 L 402 

## Features/Benefits

- Guaranteed 5 MHz shift-out/shift-in rates
- Low power consumption
- TTL inputs and outputs
- Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation


## Description

The 67L402 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a $64 \times 5$-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.
Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67 L 402 is particularly useful where low-power consumption is critical.

## Ordering Information

| PART <br> PACKAGE | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| 67 L 402 | N, NL | Com | $5 \mathrm{MHz} 64 \times 5$ FIFO |
| 67 L 402 | $\mathrm{~J}, \mathrm{NL}$ | Com | $5 \mathrm{MHz} 64 \times 5$ FIFO |

## Block Diagram

67L402 64x5


## Pin Configurations

 Q_5

## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Supply voltage |  | 4.75 | $5 \quad 5.25$ | V |
| $T_{\text {A }}$ | Operating free-air temperature |  | 0 | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {S }} \mathrm{SIH}^{\dagger}$ | Shift in HIGH time | 1 | 55 |  | ns |
| ${ }_{\text {tSIL }}$ | Shift in LOW time | 1 | 55 |  | ns |
| tids | Input data setup | 1 | 10 |  | ns |
| $\mathrm{t}_{\mathrm{IDH}}$ | Input data hold time | 1 | 80 |  | ns |
| ${ }^{\text {t }}{ }^{\text {SOH }}{ }^{\dagger}$ | Shift Out HIGH time | 5 | 55 |  | ns |
| ${ }^{\text {tSOL}}$ | Shift Out LOW time | 5 | 55 |  | ns |
| ${ }^{\text {t MRW }}$ | Master Reset pulse | 10 | 40 |  | ns |
| $t_{\text {MRS }}$ | Master Reset to SI | 10 | 35 |  | ns |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | $\begin{array}{c}\text { COMMERCIAL } \\ \text { TYP }\end{array}$ | MAX |
| :--- | :--- | :---: | :---: | :---: | :---: |$]$ UNIT

$\dagger$ See AC test and application note

## Test Load

* The "TEST POINT" is driven by the output under test and observed by instrumentation.


Input Puise 0 to 3 V
Input Rise and Fall Time ( $10 \%-90 \%$ )
5 ns minimum
Measurements made at 1.5 V

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MIN | TYP | Max | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}}$ | High-level input voltage |  |  |  | $2 \dagger$ | ? | \%. | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | I $=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\begin{aligned} & \mathrm{I}_{1 / 1} \\ & \text { IIL2 } \end{aligned}$ | Low-level input current | $\begin{aligned} & \mathrm{D}_{0}-\mathrm{D}_{3} \mathrm{MR} \\ & \mathrm{si}, \mathrm{so} \end{aligned}$ | $V_{C C}=M A X$ | $v_{1}=0.45 \mathrm{~V}$ |  |  | -0.8 -1.6 |  |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  | $\mathrm{V}_{C C}=$ MAX | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $v_{C C}=\mathrm{MIN}$ | $\mathrm{I}^{\mathrm{OL}}=8 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OH}}=-0.9 \mathrm{~mA}$ | 2.4 |  |  | V |
| los | Output short-circuit current* |  | $\mathrm{V}_{\text {CC }}=\mathrm{MAX}$ | $\mathrm{V}_{0}=0 \mathrm{~V}$ | -20 |  | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply Current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | Low, Outputs Open |  | 113 | 130 | mA |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ This is an absolute voltage with respect to device GND (Pin 8 or 9 ) and includes all overshoots due to test equipment.


## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the $D_{x}$ inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

## Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tPT defines the time required for the first data to travel from input to the output of a previously empty device.

## Data Output

Data is read from the $O_{x}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and $O_{x}$ remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least $t_{\mathrm{PT}}$ ).

## AC Test and Application Note

Since the FIFO is a high-speed device, care must be exercised in design of the hardware and the timing. Though the external data rate is 5 MHz , internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO is sensitive to very small glitches caused by long reflective lines, high capacitances, and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between VCC and GND with a very short lead length. In addition, care must be exercised in timing setup and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination as well as the Shift Out-Output Ready Combination, timing measurements may be misleading. i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time ( $t_{\mid D H}$ ) and the next activity of Input Ready ( $t_{\mid R L}$ ) to be extended relative to Shift-In going High.


Figure 1. Input Timing


Figure 2. Typical Waveforms for 5 MHz Shift in Data Rate

input data


Figure 3. The Mechanism of Shifting Data into the FIFO
(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied
(2) Input Data is loaded into the first word.
(3) Input Ready goes LOW indicating the first word is full.
(4) The Data from the first word is released for "fall-through" to second word
(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH
(58) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low

NOTE: Shift In pulses applied while Input Ready is L.OW will be ignored (See Figure 5).


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full:
(2) Shift Out pulse is applied An empty location start "bubbling" to the front
(3) Shift In is held HIGH
(4) As soon as input Ready becomes HIGH the input Data is loaded into the first word
(5) The Data from the first word is released for "fall through" to second word.

(1) The diagram assumes, that at this time words $63,62,61$ are loaded with $A, B, C$ Data, respectively

Figure 5. Output Timing


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate
(1) The diagram assumes, that at this time, words $63,62,61$ are loaded with $A, B, C$ Data, respectively.
(2) Data in the crosshatched region may be $A$ or $B$ Data


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
(2) Shift Out goes HIGH causing the next step.
(3) Output Ready goes LOW.
(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
(5A) Output Ready goes HIGH indicating that new data $(B)$ is now available at the FIFO outputs.
(58) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

SHIFT IN

(1) FIFO initially empty

Figure 8. $\mathrm{t}_{\mathrm{PT}}$ and $\mathrm{t}_{\mathrm{OPH}}$ Specification


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH
(1) Word 63 is empty.
(4) Since Shift Out is held HIGH. Output Ready goes immediately LOW.
(2) New data (A) arrives at the outputs (word 63).
(5) As soon as Shift Out goes LOW the Output Data is subject to change
Output Ready goes HIGH indicating the arrival of the new data as shown by the dashed line on Output Ready.

(1) FIFO initially full.

Figure 10. Master Reset Timing


Figure 11. 64x8 FIFO With 67L402's
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

## Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 12.


Figure 12. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate

The 67LS402 can also be used in a bidirectional operation as shown in Figure 13.


NOTE: Both depth and width expansion can be used in this mode.

Figure 13. Bidirectional FIFO Application

# First-In First-Out (FIFO) $64 \times 5$ Memory 35 MHz (Standalone) 

67413A
67413

## Features/Benefits

- High-speed 35 MHz shift-in/shift-out rates
- High-drive capability
- Three-state outputs
- Half-full and Almost-fuli/Empty status flags
- Structured pinouts. Output pins directly opposite corresponding input pins.
- Asynchronous operation
- TTL-compatible inputs and outputs


## Description

The 67413A is a high-speed, $64 \times 5$ First-In-First-Out (FIFO) memory which operates at $35-\mathrm{MHz}$ input/output rates ( 67413 operates at $25-\mathrm{MHz}$ in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive ( $\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}$ ) data outputs. These devices can be connected in paraliel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| 67413 A | J | Com | 35 MHz -in/out |
| 57413 | J | Com | 25 MHz -in/out |

## Pin Configuration



## Block Diagram



## Absolute Maximum Ratings



67413 A Operating Conditions Over Temperature Range

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {S }} \mathrm{SIH}^{+}$ | Shift in HIGH time | 1 | 9 |  |  | ns |
| ${ }^{\text {t SIL }}$ + | Shift in LOW time | 1 | 17 |  |  | ns |
| tids | Input data set up | 1 | 2 |  |  | ns |
| ${ }^{1} \mathrm{IDH}$ | Input data hold time | 1 | 15 |  |  | ns |
| ${ }^{\text {t }}{ }^{\text {SOH }}{ }^{\dagger}$ | Shift Out HIGH time | 5 | 9 |  |  | ns |
| ${ }^{\text {t SOL }}$ | Shift Out LOW time | 5 | 17 |  |  | ns |
| ${ }^{\text {t MRW }}$ | Master Reset pulse $\dagger$ | 10 | 30 |  |  | ns |
| $t_{\text {MRS }}$ | Master Reset to SI | 10 | 35 |  |  | ns |

## 67413A Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| ${ }^{\prime} / \mathrm{N}$ | Shift in rate | 1 | $\begin{aligned} & \mathrm{DC} \\ & \mathrm{DC} \end{aligned}$ |  | $\begin{array}{r} \dagger+30 \\ \dagger \dagger+35 \end{array}$ | MHz |
| $t_{\text {IRL }}{ }^{\dagger}$ | Shift In 1 to Input Ready LOW | 1 |  | 12 | 18 | ns |
| ${ }^{\text {I }} \mathrm{RH}^{\dagger}{ }^{\dagger}$ | Shift In $\mid$ to Input Ready HIGH | 1 |  | 14 | 20 | ns |
| fout | Shift Out rate | 5 | $\begin{aligned} & \mathrm{DC} \\ & \mathrm{DC} \end{aligned}$ |  | $\begin{array}{r} \dagger \dagger 30 \\ t \dagger 35 \end{array}$ | MHz |
| ${ }^{\text {t ORL }}{ }^{\dagger}$ | Shift Out 1 to Output Ready LOW | 5 |  | 12 | 18 | ns |
| ${ }^{\text {t ORH }}{ }^{\dagger}$ | Shift Out $\downarrow$ to Output Ready HIGH | 5 |  | 14 | 20 | ns |
| ${ }^{\text {O ORH }}{ }^{\text {¢ }}$ | Output Data Hold (previous word) | 5 | 12 |  |  | ns |
| ${ }^{\text {t O }}$ OS | Output Data Shift (next word) | 5 |  |  | 34 | ns |
| ${ }^{\text {t }}{ }_{\text {PT }}$ | Data throughput or "fall through" | 4,8 |  | 510 | 650 | ns |
| ${ }^{\text {t MRORL }}$ | Master Reset I to Output Ready LOW | 10 |  | 18 | 28 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset $\dagger$ to Input Ready HIGH | 10 |  | 21 | 28 | ns |
| ${ }^{\text {t MRIRL }}$ | Master Reset \ Input Ready LOW* | 10 |  | 18 | 28 | ns |
| ${ }_{\text {tMRO }}$ | Master Reset \\| to Outputs LOW | 10 |  | 32 | 45 | ns |

[^39]67413A Switching Characteristics Over Operating Conditions (continued)

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| $\mathrm{t}_{\mathrm{IPH}}$ | Input ready pulse HIGH | 4 | 5 | 12 |  | ns |
| ${ }^{\mathrm{t}} \mathrm{OPH}$ | Output ready pulse HIGH | 8 | 5 | 12 |  | ns |
| torn | Output ready 1 HIGH to Data Valid | 5 |  |  | 18 | ns |
| ${ }^{\text {t }}{ }^{\text {EEH }}{ }^{*}$ | Shift Out 1 to AF/E HIGH | 11 |  | 100 | 135 | ns |
| ${ }^{\text {t } A E L}{ }^{\text {* }}$ | Shift In 1 to AF/E LOW | 11 |  | 450 | 600 | ns |
| $\mathrm{t}_{\mathrm{AFL}}{ }^{\text {* }}$ | Shift Out $\dagger$ to AF/E LOW | 12 |  | 450 | 600 | ns |
| ${ }^{\text {taFH }}{ }^{*}$ | Shift In 1 to AF/E HIGH | 12 |  | 100 | 135 | ns |
| $t_{\text {HFH }}{ }^{\text {* }}$ | Shift In 1 to HF HIGH | 13 |  | 280 | 360 | ns |
| $t_{\text {HFL }}{ }^{*}$ | Shift Out 1 to HF LOW | 13 |  | 280 | 360 | $s$ |
| ${ }^{\text {t }}{ }^{\text {PHZ }}$ | Output Disable Delay | A |  | 14 | 25 | ns |
| ${ }^{\text {tpLZ }}$ |  | A |  | 14 | 25 | ns |
| $\mathrm{t}_{\mathrm{PZL}}$ | Output Enable Delay | A |  | 14 | 25 | ns |
| $\mathrm{t}_{\mathrm{PZH}}$ |  | A |  | 24 | 38 | ns |

Note: Input rise and fall time $(10 \%-90 \%)=2.5 \mathrm{~ns}$. * See timing diagram for explanation of parameters.

## Standard Test Load



Input Pulse Amplitude $=3 \mathrm{~V}$ Input Rise and Fall Time ( $10 \%-90 \%$ ) $=2.5 \mathrm{~ns}$ Measurements made at 1.5 V

## Design Test Load



| IOL | R1 | R2 |
| :---: | :---: | :---: |
| 24 mA | $200 \Omega$ | $300 \Omega$ |
| 8 mA | $600 \Omega$ | $1200 \Omega$ |



## Absolute Maximum Ratings



67413 Operating Conditions Over Temperature Range

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {S }}{ }^{\text {S }} \mathrm{SH}^{\dagger}$ | Shift in HIGH time | 1 | 16 |  |  | ns |
| ${ }^{\text {t SIL }}{ }^{+}$ | Shift in LOW time | 1 | 20 |  |  | ns |
| tids | Input data set up | 1 | 3 |  |  | ns |
| ${ }_{\text {I IDH }}$ | Input data hold time | 1 | 25 |  |  | ns |
| ${ }^{\text {tSOH }}{ }^{\text {t }}$ | Shift Out HIGH time | 5 | 16 |  |  | ns |
| ${ }^{\text {t SOL }}$ | Shift Out LOW time | 5 | 20 |  |  | ns |
| ${ }^{\text {t MRW }}$ | Master Reset pulse $\dagger$ | 10 | 35 |  |  | ns |
| ${ }^{\text {t MRS }}$ | Master Reset to SI | 10 | 35 |  |  | ns |

## 67413 Switching Characteristics over Temperature Range

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| $\mathrm{fin}^{\text {N }}$ | Shift in rate | 1 | DC |  | 25 | MHz |
| $t_{\text {IRL }}{ }^{\dagger}$ | Shift In 1 to Input Ready LOW | 1 |  | 12 | 28 | ns |
| ${ }^{\text {I }} \mathrm{RHH}^{\dagger}$ | Shift In 1 to Input Ready HIGH | 1 |  | 14 | 25 | ns |
| ${ }_{\text {f OUT }}$ | Shift Out rate | 5 | DC |  | 25 | MHz |
| torL ${ }^{\text {+ }}$ | Shift Out 1 to Output Ready LOW | 5 |  | 12 | 28 | ns |
| ${ }^{\text {torH }}{ }^{\dagger}$ | Shift Out \& to Output Ready HIGH | 5 |  | 14 | 25 | ns |
| ${ }^{\text {t }}{ }^{\text {ORH }}{ }^{\dagger}$ | Output Data Hold (previous word) | 5 | 10 |  |  | ns |
| ${ }^{\text {t O }}$ O | Output Data Shift (next word) | 5 |  |  | 40 | ns |
| ${ }^{\text {t }}$ T | Data throughput or "fall through" | 4,8 |  | 510 | 750 | ns |
| ${ }^{\text {t MRORL }}$ | Master Reset / to Output Ready LOW | 10 |  | 18 | 30 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset $\uparrow$ to Input Ready HIGH | 10 |  | 21 | 30 | ns |
| ${ }^{\text {t MRIRL }}$ | Master Reset + Input Ready LOW* | 10 |  | 18 | 30 | ns |
| ${ }^{\text {t MRO }}$ | Master Reset \| to Outputs LOW | 10 |  | 32 | 55 | ns |

Note: Typicals at $5 \vee \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$

* If the FIFO is not full (IR High), $\overline{M R}$ low forces IR low, followed by IR returning high when $\overline{M R}$ goes high.
$\dagger$ See AC test and high-speed application note.


## 67413 Switching Characteristics Over Operating Conditions (continued)



Note: Input rise and fall time ( $10 \%-90 \%$ ) $=2.5 \mathrm{~ns}$.

* See timing diagram for explanation of parameters.


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  |  | MIN | YP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | $0.8 \dagger$ | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  |  | $2 \dagger$ |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| 1 IL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.45 \mathrm{~V}$ |  |  |  | -250 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{H}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
|  |  |  | ${ }^{1} \mathrm{OL}$ (Data outputs) | $\begin{aligned} & 67413 A \\ & 67413 \end{aligned}$ | 24 mA |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=M I N$ | ${ }^{\text {I OL }}$ (IR, OR) | $\begin{aligned} & \text { 67413A } \\ & 67413 \end{aligned}$ | $8 \mathrm{~mA} \dagger \dagger$ |  | 0.5 | V |
|  |  |  | ${ }^{1} \mathrm{OL}$ (Flag outputs) | $\begin{aligned} & \text { 67413A } \\ & 67413 \end{aligned}$ | 8 mA |  |  |  |
|  |  |  | ${ }^{1} \mathrm{OH}$ (Data outputs) |  | $-3.0 \mathrm{~mA}$ |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOH}^{\text {(IR,OR) }}$ | $\begin{aligned} & \text { 67413A } \\ & 67413 \end{aligned}$ | -0.9 mA | 2.4 |  | v |
|  |  |  | ${ }^{1} \mathrm{OH}$ (Flag outputs) |  | -0.9 mA |  |  |  |
| IOS | Output short-circuit current* | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  |  | -20 | -90 | mA |
| ${ }^{\mathrm{H} Z}$ | 仡 | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | +20 | $\mu \mathrm{A}$ |
| LLZ | ate output | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  |  | -20 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{CC}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | All inputs low. All ou | pen. 1674 | A/67413) |  | **240 | mA |

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** See curve for ${ }^{1} \mathrm{CC}$ vs. temp.
$\dagger$ There are absolute voltages with respect to GND (PIN 8 or 9 ) and includes all overshoots due to test equipment.
† $\dagger$ Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz .


## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the $D_{X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift-ln $(\mathrm{SI})$ is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). tPT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

## Data Output

Data is read from the $\mathrm{O}_{x}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the
presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least tPT).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between VCC and GND with very short lead length. In addition,
care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity
will be ignored. This will affect the device from a funcitonal standpoint, and will also cause the "effective" timing of Input Data Hold time (TIDH) and the next activity of Input Ready ( $T_{I R L}$ ) to be extended relative to Shift-ingoing HIGH. This same type of problem is also related to TIRH, TORL and TORH as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.


Figure 1. Input Timing


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate (67413A)


Figure 3. The Mechanism of Shifting Data into the FIFO
(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
5. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.


Figure 5. Output Timing
(1) The diagram assumes that at this time, words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate (67413A)
(1) The diagram assumes that at this time words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Data in the first crosshatched region may be A or B Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.


Figure 8. tPT $^{\text {P }}$ and IOPH $^{\text {Specification }}$
(1) FIFO initially empty.


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH
(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 63).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.


Figure 10. Master Reset Timing
(1) FIFO is partially full.


Figure 11. $\mathbf{t}_{A E H}, \mathbf{t}_{A E L}$ Specifications
(1) FIFO contains 9 words (one more than almost empty).


Figure 12. $\mathbf{t}_{\mathrm{AFH}}, \mathrm{t}_{\mathrm{AFL}}$ Specifications
(1) FIFO contains 55 words (one short of almost full)


Figure 13. ${ }^{\text {HFL }}$, HFH Specifications
(1) FIFO contains 31 words (one short of half full).


Figure 14. $64 \times 15$ FIFO with $67413 \mathrm{~A} / 67413$

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.


Figure 15. Application for 67413A "Slow and Steady Rate to Fast 'Blocked Rate'"
8

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

## Three-State Test Load



## Design Test Load



## Enable and Disable

Notes: A. All diodes are 1 N916 or 1N3064
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
D. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

# First-In First-Out (FIFO) 64x4 64x5 Memory 

## Features/Benefits

- High-speed $35-\mathrm{MHz}$ shift-in/shift-out rates
- Choice of 4 -bit or 5 -bit data width
- TTL inputs and outputs
- Readily expandable in word width
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin-compatible with Fairchild's F3341 MOS FIFO and many times faster


## Description

The 67411/2A are "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width only. It is

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| 67411 A | J | Com | $35 \mathrm{MHz} 64 \times 4$ FIFO |
| 67412 A | J | Com | $35 \mathrm{MHz} 64 \times 5$ FIFO |

the fastest FIFO available on the market. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc.

## Block Diagrams



Pin Configurations


## Absolute Maximum Ratings

Supply voltage $\mathrm{V}_{\mathrm{C}}$. ............................................................................................. -0.5 V to 7 V
Input voltage ........................................................................................................... -1.5 V to 7 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ......... -5.5 V to 5.5 V
Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

Operating Conditions Over Temperature Range

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | 48 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }} \mathrm{SIH}^{\dagger}$ | Shift in HIGH time | 1 | 9 |  |  | ns |
| tids | Input data set up | 1 | 2 |  |  | ns |
| tIDH | Input data hold time | 1 | 14 |  |  | ns |
| ${ }^{\text {tSOH }}$ | Shift Out HIGH time | 5 | 11 |  |  | ns |
| $t_{\text {MRW }}$ | Master Reset pulse $\dagger$ | 10 | 30 |  |  | ns |
| ${ }^{\text {tMRS }}$ | Master Reset to $\mathrm{SI}^{*}$ | 10 | 35 |  |  | ns |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | MAX |  |
| $\mathrm{fin}^{\prime}$ | Shift In rate | 1 | DC | , | $\dagger \dagger 30$ | MHz |
|  |  |  | DC |  | $\dagger \dagger \dagger 35$ |  |
| $t_{\text {IRL }}{ }^{\dagger}$ | Shift In 1 to Input Ready LOW | 1 |  | 12 | 18 | ns |
| ${ }^{\text {I }}$ RH ${ }^{\dagger}$ | Shift In I to Input Ready HIGH | 1 |  | 14 | 20 | ns |
| fout | Shift Out rate | 5 | DC |  | $\dagger \dagger 30$ | MHz |
|  |  |  | DC |  | t†t35 |  |
| ${ }^{\text {O ORL }}{ }^{\dagger}$ | Shift Out $\dagger$ to Output Ready LOW | 5 |  | 12 | 18 | ns |
| ${ }^{\text {ORH }}{ }^{\dagger}$ | Shift Out \\| to Output Ready HIGH | 5 |  | 14 | 20 | ns |
| ${ }^{\text {t ODH }}{ }^{\text {¢ }}$ | Output Data Hold (previous word) | 5 | 9 |  | \% | ns |
| tods | Output Data Shift (next word) | 5 |  |  | 31 | ns |
| ${ }_{\text {tPT }}$ | Data throughput or "fall through" | 4,8 |  | 510 | 650 | ns |
| ${ }^{\text {t MRORL }}$ | Master Reset $\downarrow$ to Output Ready LOW | 10 |  | 18 | 28 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset $\dagger$ to Input Ready HIGH* | 10 |  | 21 | 35 | ns |
| ${ }^{\text {m MRIRL }}$ | Master Reset I Input Ready LOW* | 10 |  | 18 | 28 | ns |
| ${ }^{\text {t MRO }}$ | Master Reset I to Outputs LOW | 10 |  | 32 | 45 | ns |

Note: Typical at $5 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} T_{A A}$.

* If the FIFO is not full (IR High), $\overline{M R}$ low forces IR low returning high when $\overline{M R}$ goes high
$\dagger$ See AC test and high-speed application note.
$\dagger \dagger$ Tested
$\dagger \dagger \dagger$ Guaranteed by design (see test load).

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITION |  |  |  | MIN TYP MAX |  | $\frac{\text { UNIT }}{V}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | $0.8 \dagger$ |  |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  |  |  |  | $2 \dagger$ |  | V |
| $V_{\text {I }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.45 \mathrm{~V}$ |  |  |  | -50 | $\mu \mathrm{A}$ |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  |  | 50 | $\mu \mathrm{A}$ |
| 11 | Maximum input current | $V_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
|  |  |  | $\mathrm{I}^{\prime} \mathrm{L}$ (Data Outputs) | 67411/2A | 24 mA |  | 5 | V |
|  |  |  | $\mathrm{I}^{\prime} \mathrm{L}$ (IR, OR) | 67411/2A | $8 \mathrm{~mA} \mathrm{t} \dagger$ |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $V_{C C}=$ MIN | $\mathrm{I}_{\mathrm{OH}}$ (Data Out) | 67411/2A | -3.0 mA | 2.4 |  | V |
| OH | High-level output volage | $V_{C C}-\mathrm{MIN}$ | $\mathrm{IOH}^{(I R, O R)}$ |  | -0.9 mA | 2.4 |  |  |
| Ios | Output short-circuit current* | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  |  | -20 | -90 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $V_{C C}=M A X$ | Inputs low, outputs o | 67411/2A) |  |  | **240 | mA |

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** See curve for ICC vs. temp.
$\dagger$ These are absolute voltages with respect to GND (Pin 8 or 9 ) and includes all overshoots due to test equipment.
$\dagger \dagger$ Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz .


## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the $D_{x}$ inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

## Data Output

Data is read from the $O_{x}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage,

OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.
Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least tPT).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input

Switching Characteristics Over Operating Conditions (continued)

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL <br> MIN TYP | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| IIPH | Input ready pulse HIGH | 4 | 5 | 12 |
| tOPH | Output ready pulse HIGH | 8 | ns |  |
| tORD | Ouput ready 1 to Data Valid | 5 | 12 | ns |

## Standard Test Load



Input Pulse Amplitude $=3 \mathrm{~V}$
Input Rise and Fall Time ( $10 \%-90 \%$ ) $=2.5 \mathrm{~ns}$ Measurements made at 1.5 V

## Test Load

## Design Test Load

( 35 MHz )


| IOL | R1 | R2 |
| :---: | :---: | :---: |
| 24 mA | $200 \Omega$ | $300 \Omega$ |
| 8 mA | $600 \Omega$ | $1200 \Omega$ |

## Typical ICC vs Temperature $\left(\mathbf{V}_{\mathbf{C C}}+\mathrm{MAX}\right)$



Data Hold time (TIDH) and the next activity of Input Ready ( $T_{\text {IRL }}$ ) to be extended relative to shift-in going HIGH. This same type of situation occurs with TORL and TORH as related to

Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.


Figure 1. Input Timing


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate


Figure 3. The Mechanism of Shifting Data into the FIFO
(1) Input Feady HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows input Ready to sense the status of first word. The first word is now empty as indicated by input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.


Figure 5. Output Timing
(1) The diagram assumes that at this time, words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate
(1) The diagram assumes that at this time words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Data in the first crosshatched region may be A or B Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.


Figure 8. $t_{P T}$ and $t_{O P H}$ Specification
(1) FIFO initially empty.
(2) Shift Out held HIGH


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.
(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 63).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.


Figure 10. Master Reset Timing

## Features/Benefits

- High-speed $\mathbf{2 8 - M H z}$ serial shift-in/shift-out rate
- $10-\mathrm{MHz}$ parallel shift-in/shift-out rate
- Three-state outputs with Hi-current drive
- Cascadable at parallel port only
- Half-full flag (32 or more)
- Selectable $\mathbf{6 4 \times 8}$ or $\mathbf{6 4 \times 9}$ FIFO configuration thus providing "frame mark bit"


## Typical Applications

- LAN equipment
- Data communication
- Office automation
- Microcomputers
- Minicomputers
- Disk/tape controllers


## Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words $\times 8 / 9$ bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

## Pin Configuration



## Ordering Information

| PART <br> NUMBER | PACKAGE | TEMPERATURE | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| 67417 | J | Com | $64 \times 8 / 9$ |

In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a chip."
The FIFO basically has three modes of operation;

1. Serial in to parallel out
2. Parallel in to serial out
3. Serial in to serial out (requires non-standard logic level on PDIR).
In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz . Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

## Pin Names

| PO-P8 | Parallel Data |
| :--- | :--- |
| PS | Parallel Shift In/Out |
| PR | Parallel Input/Output Ready |
| $\overline{\text { POE }}$ | Parallel Output Enable |
| SID | Serial Input Data |
| SIS | Serial Input Shift |
| SIR | Serial Input Ready |
| SOD | Serial Output Data |
| SOS | Serial Output Shift |
| SOR | Serial Output Ready |
| PDIR | Parallel Port Direction |
| WL | Word Length |
| $\overline{\text { MR }}$ | Master Reset |
| HF | Half Full Flag |
| VCC | VCC |
| GND | Ground |

## Block Diagram



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | FIGURE | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
|  | SERIAL INPUT PARAMETERS |  |  |  |  |  |
| ${ }^{\text {f SIN }}$ | Max. Serial Shift-In Rate | 1 |  |  | 28 | MHz |
| tSISH | Serial Shift-In HIGH time | 1 | 23 |  |  | ns |
| ${ }^{\text {t SISL }}$ | Serial Shift-In LOW time | 1 | 12 |  |  | ns |
| ${ }^{\text {t SIDS }}$ | Serial Input Data Setup time | 1 | 14 |  |  | ns |
| ${ }^{\text {t SIDH }}$ | Serial Input Data Hold time | 1 | 0 |  |  | ns |
| ${ }^{\text {tSIRHS }}$ | Recovery Time Serial Input Ready 1 to Serial Input Shift $\dagger$ | 1 | 0 |  |  | ns |
|  | SERIAL OUTPUT PARAMETERS |  |  |  |  |  |
| fSOUT | Max. Serial Shift-Out Rate | 1 |  |  | 28 | MHz |
| tSOSH | Serial Shift-Out HIGH time | 3 | 15 |  |  | ns |
| tSOSL | Serial Shift-Out LOW time | 3 | 15 |  |  | ns |
| tORHS | Recovery time Serial Output Ready 1 to Serial Output Shift $\dagger$ | 3 | 5 |  |  | ns |
|  | WORD LENGTH PARAMETERS |  |  |  |  |  |
| tSWL | Setup SIS, SOS | 1,3 | 18 |  |  | ns |
| $t_{\text {HWL }}$ | Hold SIS, SOS | 1,3 | 3 |  |  | ns |
|  | PARALLEL PORT PARAMETERS |  |  |  |  |  |
| ${ }_{f}{ }_{P}$ | Parallel shift-in/shift-out rate | 8 |  |  | 10 | MHz |
| ${ }^{\text {tPSH }}$ | Parallel Shift-In/Out HIGH time | 5/8 | 30 |  |  | ns |
| ${ }^{\text {tPSL }}$ | Parallel Shift-In/Out LOW time | 5/8 | 30 |  |  | ns |
| tPIDS | Parallel Input Data Setup time | 5 | -5 |  |  | ns |
| ${ }^{\text {P PIDH }}$ | Parallel Input Data hold time | 5 | 35 |  |  | ns |
| tPDIRSL | Shift LOW to parallel direction transition | 14 | 50 |  |  | ns |
| tPDIRSH | Parallel direction transition to Shift HIGH | 14 | 50 |  |  | ns |
| tPRHS | Parallel Ready 1 to Parallel Shift Low | 10/11 | 30 |  |  | ns |
|  | MASTER RESET PARAMETER |  |  |  |  |  |
| ${ }^{\text {tMRW }}$ | Master Reset LOW time | 12/13 | 40 |  |  | ns |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| SERIAL INPUT PARAMETERS |  |  |  |  |  |  |
| ${ }^{\text {t }}$ ITRL | Serial Input Shift $\dagger$ to Serial Input Ready LOW | 2 |  |  | 23 | ns |
| ${ }^{\text {t SIHFH }}$ | Serial Input Shift $\dagger$ to Halt-Full Flag HIGH | 7 |  |  | 1.3 | $\mu \mathrm{s}$ |
| SERIAL OUTPUT PARAMETERS |  |  |  |  |  |  |
| ${ }^{\text {tSORL }}$ | Serial Output Shift $\dagger$ to Serial Output Ready LOW | 4 |  |  | 23 | ns |
| tSOD | Serial Output Shift 1 to Serial Output data | 3 |  |  | 23 | ns |
| ${ }^{\text {t O O }}$ ORH | Serial Output Data valid to Serial Output Ready HIGH | 3 | 0 | 25 |  | ns |
| ${ }^{\text {tSOHFL }}$ | Serial Output Shift $\dagger$ to Half-Full LOW | 7 |  |  | 1.3 | $\mu \mathrm{s}$ |
|  | PARALLEL INPUT/OUTPUT PARAMETERS |  |  |  |  |  |
| ${ }^{\text {tPSPRL }}$ | Parallel Shift 1 to Parallel Ready LOW | 5/8 |  |  | 65 | ns |
| tPSPRH | Parallel Shift $\downarrow$ to Parallel Ready HIGH | 5/8/10 |  |  | 80 | ns |
| $t_{\text {PSHFH }}$ | Parallel Shift-In $\downarrow$ to Half-Full HIGH | 6 |  |  | 1.3 | $\mu \mathrm{S}$ |
| $t_{\text {PSHFL }}$ | Parallel Shift-Out $\downarrow$ to Half-Full LOW | 9 |  |  | 1.3 | $\mu \mathrm{s}$ |
|  | PARALLEL OUTPUT PARAMETERS |  |  |  |  |  |
| ${ }^{\text {tPODH }}$ | Minimum Parallel Shift $\downarrow$ to Ouput data | 8 | 20 |  |  | ns |
| ${ }^{\text {tPOD }}$ | Maximum Parallel Shift $\downarrow$ to Output data | 8 |  |  | 60 | ns |
| ${ }^{\text {t PODV }}$ | Minimum Output data valid to parallel ready HIGH | 8 | 0 | 15 |  | ns |
|  | OTHER PARAMETERS |  |  |  |  |  |
| $t_{\text {PT }}$ | Fall-through time | 10/11/16/17 |  |  | 2.6 | $\mu \mathrm{s}$ |
| ${ }^{1} \mathrm{PH}$ | Parallel Input Ready pulse HIGH | 11 | 30 |  |  | ns |
| ${ }^{\text {toPH }}$ | Parallel Output Ready pulse HIGH | 10 | 30 |  |  | ns |
| $\mathrm{t}_{\mathrm{MRO}}$ | Master Reset ! to Data Out LOW | 12 |  |  | 65 | ns |
| ${ }^{\text {t MRSIRL }}$ | Master Reset $\downarrow$ to Serial Input Ready LOW | 12 |  |  | 40 | ns |
| ${ }^{\text {t MRSIRH }}$ | $\overline{\text { Master Reset } \dagger \text { to Serial Input Ready HIGH }}$ | 12 |  |  | 40 | ns |
| ${ }^{\text {t MRPRL }}$ | Master Reset $\downarrow$ to Parallel Ready LOW | 12/13 |  |  | 40 | ns |
| ${ }^{\text {t MRPRH }}$ |  | 13 |  |  | 30 | ns |
| ${ }^{\text {t MRSORL }}$ | Master Reset $\downarrow$ to Serial Output Ready LOW | 13 |  |  | 40 | ns |
| ${ }^{\text {t MRHFL }}$ | Master Reset 1 to Half-Full LOW | 12/13 |  |  | 60 | ns |
| tPDIROR | Parallel Direction change to new Output Ready | 14 |  |  | 60 | ns |
| ${ }^{\text {tPDIROD }}$ | Parallel Direction change to Output data valid | 14 |  |  | 60 | ns |
| ${ }^{\text {t PDIRPZ }}$ | Parallel Direction change to Parallel Output data Hi-Z | 14 |  |  | 35 | ns |
| tPDIRSZ | Parallel Direction changes to Serial Output-data Hi-Z | 14 |  |  | 80 | ns |
| ${ }_{\text {t } P Z X}$ | Output enable time $\overline{\mathrm{POE}}$ to $\mathrm{P} 0-8$ | 15 |  |  | 30 | ns |
| tPXZ | Output disable time $\overline{\mathrm{POE}}$ to $\mathrm{PO}-8$ | 15 |  |  | 35 | ns |

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  |  |  | COM <br> TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | $0.8 \dagger$ | V |
| $V_{1 H}$ | High-level input voltage |  |  |  |  | $2 \dagger$ |  | V |
| $V_{1 C}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| IL | Low-level input current |  | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  | -0.4 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  |  | 0.1 | mA |
| 1 | Maximum input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 0.4 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | Data OutputsPO-P8, SOD | 0-80 ${ }^{\circ} \mathrm{C}$ |  | 0.58 | V |
|  |  |  | $\mathrm{OL}^{2}=24 \mathrm{~mA}$ 25 $25^{\circ} \mathrm{C}$ |  |  | 0.55 |  |
|  |  |  | $\mathrm{I}^{\mathrm{OL}}=16 \mathrm{~mA} 0-80^{\circ} \mathrm{C}$ |  |  | 0.5 |  |
|  |  |  | All other outputs | $\mathrm{I}^{\mathrm{OL}}=8 \mathrm{~mA}$ |  | 0.5 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OH}}=-3 \mathrm{~mA}$ |  | 2.4 |  | $\checkmark$ |
| ${ }^{1} \mathrm{OS}$ | Output short-circuit current* |  |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -20 | -90 | mA |
| ILZ | Off-state output current* | $\begin{aligned} & \mathrm{SOD} \\ & \mathrm{PO} \text { to } \mathrm{P8} \end{aligned}$ |  | $\mathrm{V}_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{\mathrm{H}} \mathrm{HZ}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 100 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current |  | $V_{C C}=M A X$ |  |  |  | 350 | mA |
| OV | PDIR non-standard over voltage |  | Serial-In, Serial-Out |  |  | 10 | 16 | V |

[^40]
## Test Waveforms

| TEST | S = OPEN | S = CLOSED | OUTPUT WAVEFORM-MEAS-LEVEL |
| :---: | :---: | :---: | :---: |
| All $\mathrm{t}_{\text {PD }}$ |  | All tpo |  |
| ${ }^{\text {tPXZ }}$ | ${ }^{\text {PrHz }}$ | ${ }^{\text {tPLZ }}$ |  |
| ${ }^{\text {tPZ }}$ P | ${ }^{\text {tPZH }}$ | ${ }^{\text {PPZL }}$ |  |



## ICC VS Temperature



## Definition of Waveforms


(1) FIFO is full.
(2) Shift-out (serial or parallel) is asserted, SIR goes High.
(3) SIS can be asserted tSIRHS after serial input ready changes from low-to-high.

Figure 1. Serial Input Timing


Figure 2. FIFO Full Specification (tSIRL)

## Definition of Waveforms (cont'd)


(1) FIFO is empty, output ready remains Low and shift-out cannot be applied.
(2) After a word is shifted in, output ready goes High and shift-out can be applied.
(3) The first serial bit is PO.

Figure 3. Serial Output Timing

(1) After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications (tSORL),

## Definition of Waveforms (cont'd)



NOTE: $P_{\text {DIR }}=$ High for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.
(1) FIFO is not full and ready for input.
(2) PS (In) is asserted, shifting in parallel data P0-8.

PR (In) goes Low indicating parallel port is in use and no longer ready.
PR (In) will remain Low as long as PS (In) remains High.
(3) PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing

(1) for PDIR $=$ High, the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

Figure 6. Half-full Flag Specifications on Parallel (tPSHFH)

(1) When there are 31 words in the FIFO, the next shift-in on the 32 nd word sets the half-full flag (HF) High indicating that there are 32 or more words.
(2) As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation (tSIHFH, ${ }^{\text {SOHFL }}$ )

## Definition of Waveforms (cont'd)



NOTE: For above conditions $P_{\text {DIR }}$ = Low indicating that the direction is from serial-in to parallel-out. Thus parallel ready indicates the output status.
(1) FIFO is not empty and at least one word is valid and ready at P0-8 outputs.
(2) PS (Out) is asserted, shifting out parallel data. Data remains valid, but: PR (Out) goes Low to indicate parallel port is in use and no longer ready. PR (Out) will remain Low as long as PS (Out) remains High.
(3) PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and PR (Out) is asserted to indicate valid data ready.

Figure 8. Serial-in to Parallel-out Specifications (tPOD, tPODH, tODV)


NOTE: For PDIR = Low the direction is serial-in to parallel-out.
(1) When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

Figure 9. Half-full Flag Specification on Parallel Shift-out (tPSHFL)


NOTE: $P_{\text {DIR }}=$ Low indicating serial-in to parallel-out.
(1) FIFO initially empty.
(2) PS (Out) held High.

Figure 10. ${ }^{\text {tPSPRH, }}$, ${ }_{\text {PT }}$, tPOH Specifications (Serial Input Mode)

## Definition of Waveforms (cont'd)



NOTE: PDIR $=$ High (parallel-in to serial-out).
(1) FIFO is full.
(2) PS (I) held High.

Figure 11. Fall-through Specifications


NOTE: $P_{\text {DIR }}=$ Low.
(1) PR ( O ) and HF go Low.
(2) After $\overline{M R}$ goes High, SIR goes. High.

Figure 12. Master Reset Timing Serial-in to Parallel-out

## Definition of Waveforms (cont'd)



NOTE: PDIR $=$ High.
(1) SOR and HF go Low.
(2) Affter $\overline{M R}$ goes High, PR(I) goes High.

Figure 13. Master Reset Timing (Parallel-in to Serial-out)


NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.
Figure 14. P $_{\text {DIR }}$ Transition Parameters


Figure 15. Parallel Port Enable and Disable Timing

## Definition of Waveforms (cont'd)



Figure 16. $t_{\mathrm{PT}}$ Specification (Shift-in to Serial Output Ready)

(2) FIFO empty

Figure 17. tpT Specification (Shift-in to Serial Input Ready)

## Appendix Detailed Functional/Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment. The 67417 is a word-oriented device. It is meant to function with complete 8 - or 9 -bit words of data.

## Parallel Port

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz . The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array; and the OSR inputs are likewise driven by the final parallel data stage of the cell array


Basically the major internal subsystems of the 67417 are:
(i) The serial input port
(ii) The serial output port
(iii) The parallel port
(iv) The FIFO control logic and
(v) The cell array

## Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz . These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.
The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).
The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the $8 / 9$-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is
disabled (during Master Reset) and PDIR = Low. The parallel port is controlled by Parallel Shift (PS) input and Parallel Direction Input (PDIR). Parallel Ready (PR) is the handshake/status output. At the Parallel Port PS and PR do accomplish a handshake with the outside world as SI, IR, SO and OR on the 67401/2.

## Modes of Operation

There are three modes in which the 67417 can operate
(i) Parallel-in to serial-out
(ii) Serial-in to parallel-out and
(iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR $=$ HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR). The first bit shifted out of the serial port will be bit 0 of the parallel word input.
Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out(SO) and Parallel Ready (PR) as Output Ready (OR). The first bit shifted into the serial port will be bit 0 of the parallel word output.
If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HGH.
In the serial-in to serial-out mode, PDIR $=10 \mathrm{~V}$ minimum.
The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

## Cell Array

The 67417 cell array can function either as a $64 \times 8$ FIFO (with the 9 th bit padded to a zero) or as a $64 \times 9$ FIFO, according to the setting of the word length (WL) control input. Like the PDIR
control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is never to change during system operation, WL for that part can be strapped to ground or $V_{C C}$.
It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8 -bit operation, then switch WL to 9 -bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9 -bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.
It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8-or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

## Half-Full Flag

This status output indicates when the 67417 statically contains 32 words or more. This provides an indication to send in more data if the device is operated in a mostly-empty mode or send out more data if the 67417 is operated in a mostly-full mode.

## Cascading

The 67417 is designed to be cascaded at the parallel port only, due to very high data transfer rates at the serial ports. Cascading two 67417's is accomplished by connecting Parallel Input/Output Ready (PR) of each part to control the Parallel Shift In/Out (PS) of the other part, with one FIFO in serial-in to parallel-out mode, and the other FIFO in parallel-in to serial-out mode. The combined effect of this is a reversible $128 \times 8$ or $128 \times 9$ serial-in serial-out FIFO. The 67417 can not be cascaded at the serial ports because SIR and SOR are not acknowledged signals but rather status signals only.

## Applications



NOTE: It can shift in data serially in the multiples of 8-or 9-bit according to WL.
Figure 18. 512/576x1 Serial-in to Serial-out Mode


$$
\begin{aligned}
* \text { SIPO } & =\text { Serial-in to Parallel-out. } \\
* * \text { PISO } & =\text { Parallel-in to Serial-out. }
\end{aligned}
$$

Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out Operation as a 128x9 (1152x1) FIFO


Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO

An 18-bit data word is multiplexed into the two $67401 / 2$ FIFOs. $\quad 67401 / 2$ FIFOs were used along with the 67417 to obtain the Since the 67417 FIFO is cascadable at the parallel port only, two appropriate organization.


Figure 21. Another Example of an Expansion Scheme for a $64 \times 18$ Parallel-in to Serial-out FIFO Two 67417 FIFOs Are Used to Implement a $64 \times 18$ Parallel-in to Serial-out FIFO

## 67417



Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While
the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.

# First-In First-Out (FIFO) $64 \times 5$ Memory <br> 15 MHz (Cascadable) 

## Features/Benefits

- High-speed 15 MHz shift-in/shift-out rates
- High drive capability
- Low-power consumption
- Three-state outputs
- Fully expandable by word width and depth
- Hali-Full and Almost-Full/Empty status flags
- Structured pinouts. Output pins directly opposite corresponding input pins.
- Asynchronous operation
- TTL-compatible inputs and outputs


## Description

The C67L4033D is a high-speed, $64 \times 5$ First-In-First-Out (FIFO) memory which operates at 15 MHz input/output rates. The data is loaded and emptied on a first-in-first-out basis. It is a threestate device with high-drive ( $I_{\mathrm{OL}}=24 \mathrm{~mA}$ ) data outputs. These devices can be expanded to any word width and depth. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main application of C67L4033D is as a rate buffer; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | DESCRIPTION |
| :---: | :---: | :---: | :---: |
| C67L4033D | $\mathrm{N}, \mathrm{J}$ | Com | 15 MHz in/out |

Pin Configuration



## Absolute Maximum Ratings

Supply voltage $\mathrm{V}_{\mathrm{CC}}$
-0.5 V to 7 V
Input voltage
-1.5 V to 7 V
Off-state output voltage
-0.5 V to 5.5 V
Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions Over Temperature Range

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |
| $\mathrm{f}_{\mathrm{IN}}$ | Shift In rate | 1 |  |  | 15 | MHz |
| ${ }^{\text {t }}$ SIH ${ }^{*}$ | Shift in HIGH time | 1 | 24 |  |  | ns |
| $\mathrm{t}_{\text {SIL }}{ }^{\text {* }}$ | Shift in LOW time | 1 | 15 |  |  | ns |
| tIDS | Input data setup to SI (Shift In) | 1 | 0 |  |  | ns |
| ${ }_{\text {t }}$ DH | Input data hold time from SI (Shift In) | 1 | 26 |  |  | ns |
| $t_{\text {RIDS }}$ | Input data setup to IR (Input Ready) | 4 | 0 |  |  | ns |
| $t_{\text {RIDH }}$ | Input data hold time from IR (Input Ready) | 4 | 26 |  |  | ns |
| ${ }^{\text {fout }}$ | Shift Out rate | 5 |  |  | 15 | MHz |
| $\mathrm{t}^{\text {SOH }}{ }^{* *}$ | Shift Out HIGH time | 5 | 17 |  |  | ns |
| ${ }^{\text {t SOL }}$ | Shift Out LOW time | 5 | 15 |  |  | ns |
| $\mathrm{t}_{\text {MRW }}{ }^{\text {* }}$ | Master Reset pulse | 10 | 35 |  |  | ns |
| tMRS** | Master Reset to SI | 10 | 35 |  |  | ns |

* See AC test and high-speed application note.
** If the FIFO is not full (IR High), $\overline{M R}$ low forces IR low, followed by IR returning high when $\overline{M R}$ goes high.
Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITION |  | MIN | COMMERCIAL <br> MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{VIL}^{*}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}}{ }^{\text {* }}$ | High-level input voltage |  |  |  | 2 |  | V |
| VIC | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | I $=-18 \mathrm{~mA}$ |  | -1.5 | V |
| ILL | Low-level input current |  | $V_{C C}=$ MAX | $\mathrm{V}_{1}=0.45 \mathrm{~V}$ |  | -250 | $\mu \mathrm{A}$ |
| IIH | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  | 1 | mA |
| VOL | Low-level output voltage | Output, O | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{IOL}=24 \mathrm{~mA}$ |  | 0.5 |  |
|  |  | IR,OR, HF, AF/E |  | $1 \mathrm{OL}=8 \mathrm{~mA}$ |  | 0.5 | V |
| $\mathrm{VOH}^{\text {O }}$ | High-level output voltage | Output, O | $\mathrm{VCC}=\mathrm{MIN}$ | $\mathrm{IOH}=-3 \mathrm{~mA}$ | 2.4 |  |  |
|  |  | IR,OR,HF,AF/E |  | $1 \mathrm{OH}=-0.9 \mathrm{~mA}$ |  |  | $v$ |
| Ios** | Output short-circuit current |  | $V_{C C}=M A X$ | $\mathrm{V}_{0}=0 \mathrm{~V}$ | -20 | -90 | mA |
| lozl | Off-state output current |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -50 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  | 50 | $\mu \mathrm{A}$ |
| ICC | Supply current |  |  | $V_{C C}=M A X$ | All inputs low. <br> All outputs open. |  | 120 | mA |

* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.
** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | COMMERCIAL |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX |  |
| $\mathrm{t}_{\mathrm{IRL}}$ | Shift In 1 to Input Ready LOW | 1 |  | 40 | ns |
| $\mathrm{t}_{\text {IRH }}$ | Shift In $\downarrow$ to Input Ready HIGH | 1 |  | 26 | ns |
| torl | Shift Out $\dagger$ to Output Ready LOW | 5 |  | 45 | ns |
| ${ }^{\text {torh }}$ | Shift Out $\downarrow$ to Output Ready HIGH | 5 |  | 50 | ns |
| ${ }^{\text {todH }}$ | Output Data Hold (previous word) | 5 | 12 |  | ns |
| tods | Output Data Shift (next word) | 5 |  | 40 | ns |
| $\mathrm{t}_{\mathrm{PT}}$ | Data throughput | 4,8 |  | 1600 | ns |
| $\mathrm{t}_{\text {MRORL }}$ | Master Reset $\downarrow$ to Output Ready LOW | 10 |  | 60 | ns |
| $\mathrm{t}_{\text {MRIRH }}{ }^{\text {* }}$ | Master Reset $\dagger$ to Input Ready HIGH | 10 |  | 30 | ns |
| $\mathrm{t}_{\text {MRIRL }}{ }^{*}$ | Master Reset \\| to Input Ready LOW | 10 |  | 50 | ns |
| $\mathrm{t}_{\text {MRO }}$ | Master Reset $\downarrow$ to Outputs LOW | 10 |  | 60 | ns |
| ${ }^{\text {t }}$ PH | Input ready pulse HIGH | 4 | 17 |  | ns |
| ${ }^{\text {t }} \mathrm{OPH}$ | Output ready pulse HIGH | 8 | 24 |  | ns |
| ${ }^{\text {tord }}$ | Output ready $\uparrow$ to Data Valid | 5 |  | -3 | ns |
| ${ }^{\text {t }}{ }^{\text {EEH }}{ }^{*}$ | Shift Out 1 to AF/E HIGH | 11 |  | 320 | ns |
| $\mathrm{t}_{\mathrm{AEL}}{ }^{*}$ | Shift In $\dagger$ to AF/E LOW | 11 |  | 1400 | ns |
| $\mathrm{t}_{\mathrm{AFL}}{ }^{\text {* }}$ | Shift Out $\dagger$ to AF/E LOW | 12 |  | 1400 | ns |
| ${ }^{\text {t }} \mathrm{AFH}^{\text {* }}$ | Shift In $\dagger$ to AF/E HIGH | 12 |  | 320 | ns |
| ${ }^{\text {HFH }}{ }^{\text {* }}$ | Shift In 1 to HF HIGH | 13 |  | 800 | ns |
| $\mathrm{t}_{\mathrm{HFL}}{ }^{\text {* }}$ | Shift Out 1 to HF LOW | 13 |  | 800 | ns |
| ${ }^{\text {t }}{ }^{\text {PHZ }}{ }^{*}$ | Output Disable Delay | A |  | 30 | ns |
| ${ }^{1} P L Z{ }^{*}$ |  |  |  | 30 |  |
| ${ }^{\text {P PLL }}$ * | Output Enable Delay |  |  | 30 | ns |
| ${ }^{\text {tPZH }}{ }^{*}$ |  |  |  | 40 |  |

* See timing diagram for explanation of parameters.


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is
low except when disabled by the output control.
Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

## Standard Test Load



Input Pulse Amplitude $=3 \mathrm{~V}$ Input Rise and Fall Time ( $10 \%-90 \%$ ) $=2.5 \mathrm{~ns}$
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the $D_{x}$ inputs. Data then present at the the data inputs is entered into the first location when the Shift-ln (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). tPT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using Master Reset before starting the operation.

## Data Output

Data is read from the $\mathrm{O}_{\mathrm{X}}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

| IOL | R1 | R2 |
| :---: | :---: | :---: |
| 24 mA (Data) | $200 \Omega$ | $300 \Omega$ |
| 8 mA (IR, OR, Flags) | $600 \Omega$ | $1200 \Omega$ |

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least tPT).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between $V_{C C}$ and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time ( $\mathrm{T}_{\mathrm{IDH}}$ ) and the next activity of Input Ready ( $T_{I R L}$ ) to be extended relative to Shift-in going HIGH. This same type of problem is also related to TIRH, TORL and TORH as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

## Timing Waveforms



Figure 1. Input Timing


Figure 2. Typical Waveforms for 15 MHz Shift-In Data Rate


Figure 3. The Mechanism of Shifting Data into the FIFO
(1) Input Ready HIGH indicates space is available and a Shift-In puise may be applled.
(2) Input Data is loaded into the first word. The data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(1) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HluH.
(5) If the second word is already full then data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.


Figure 5. Output Timing
(1) The diagram assumes that at this time, words 64,63 and 62 are loaded with A, B and C Data, respectively.
(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.


Figure 6. Typical Waveforms for 15 MHz Shift-Out Data Rate
(1) The diagram assumes that at this time words 64,63 and 62 are loaded with $A, B$ and $C$ Data, respectively.
(2) Data in the first crosshatched region may be A or B Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 63 (B-Data) to be released for fall-through to word 64. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.


Figure 8. tPT and tOPH Specification
(1) FIFO initially empty.
(2) Shift-Out is held HIGH.

SHIFT OUT


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH
(1) Word 64 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 64).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.


Figure 10. Master Reset Timing
(1) FIFO is partially full.


Figure 11. $\mathbf{t}_{\text {AEH }}$, t $_{\text {AEL }}$ Specifications
(1) FIFO contains 9 words (one more than almost empty).


Figure 12. tAFH, taFL $^{\text {Specifications }}$
(1) FIFO contains 55 words (one short of almost full).


Figure 13. $\mathbf{t} \mathbf{H F L}$, thFH $^{\text {Specifications }}$
(1) FIFO contains 31 words (one short of half full).


[^41]Figure 14. 192×15 FIFO with C67L4033D


Figure 15. Application for C67L4033D "Slow and Steady Rate to Fast 'Blocked Rate'"

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

## Features/Benefits

- High-speed $15-\mathrm{MHz}$ shift-in/shift-out rates
- Low power consumption
- TTL inputs and outputs
- Readily expandable in word width and depth
- Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation
- Output Enable feature


## Description

The C67L4013D is a "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. The C67L4013D has three-state, highdrive ( $1 \mathrm{OL}=24 \mathrm{~mA}$ ) outputs.

Pin Configuration


## Ordering Information

| PART <br> NUMBER | PKG | TEMP | O/P | DESCRIPTION |
| :---: | :---: | :---: | :---: | :---: |
| C67L4013D | N, J | Com | 3-state | $15 \mathrm{MHz} 64 \times 4$ FIFO |

## Block Diagram

C67L4013D


## Absolute Maximum Ratings





Operating Conditions Over Temperature Range

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |
| fin | Shift in rate | 1 |  | $\cdots$ | 15 | MHz |
| ${ }_{\text {tSIH }}$ | Shift in High time | 1 | 24 |  |  | ns |
| ${ }^{\text {tSIL }}$ | Shift in Low time | 1 | 15 |  |  | ns |
| tids | Input data setup to SI (Shift In) | 1 | 0 |  |  | ns |
| tide | Input data hold time to SI (Shift In) | 1 | 26 |  |  | ns |
| trids | Input data setup to IR (Input Ready) | 4 | 0 |  |  | ns |
| triDh | Input data hold time to IR (Input Ready) | 4 | 26 |  |  | ns |
| fout | Shift out rate | 5 |  |  | 15 | MHz |
| ${ }^{\text {t }} \mathrm{SOH}$ | Shift out High time | 5 | 17 |  |  | ns |
| tSOL | Shift out Low time | 5 | 15 |  |  | ns |
| tMRW | Master Reset pulse ${ }^{* *}$ | 10 | 35 |  |  | ns |
| tMRS | Master Reset to $\mathrm{SI}^{*}$ | 10 | 35 |  |  | ns |

* If the FIFO is not full (IR High), $\overline{M R}$ low forces IR low, followed by IR returning high when $\overline{M R}$ goes high.
** See AC test and high-speed application note.


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITION |  | MIN | COMMERCIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  |  | $0.8 * *$ | V |
| $\mathrm{V}_{1 \mathrm{H}}$ | High-level input voltage |  |  |  | 2** |  | V |
| $V_{1 C}$ | Input clamp voltage |  | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  | -1.5 | V |
| IL | Low-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.45 \mathrm{~V}$ |  | -250 | $\mu \mathrm{A}$ |
| I H | High-level input current |  | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=M A X$ | $V_{1}=5.5 \mathrm{~V}$ |  | 1 | mA |
| VOL | Low-level Output voltage | Output, O | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $1 \mathrm{OL}=24 \mathrm{~mA}$ |  | 0.5 | V |
|  |  | IR, OR |  | $1 \mathrm{OL}=8 \mathrm{~mA}$ |  |  |  |
| VOH | High-level Output voltage | Output, O | $V_{C C}=$ MiN | $\mathrm{IOH}=-3.0 \mathrm{~mA}$ | 2.4 |  | V |
|  |  | IR, OR |  | $\mathrm{IOH}=-0.9 \mathrm{~mA}$ |  |  |  |
| Ios | Output short-cir | cuit current* | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 | -90 | mA |
| IOZL | Off-state output current |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -50 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  | +50 |  |
| ICC | Supply current |  |  | $V_{C C}=M A X$ <br> All inputs low. All outputs open. |  |  | 110 | mA |

[^42]
## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | COMMERCIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{\text {tIRL }}{ }^{\dagger}$ | Shift In 1 to Input Ready LOW | 1 |  | 40 | ns |
| $t_{\text {IRH }}{ }^{\dagger}$ | Shift In \ to Input Ready HIGH |  |  | 26 | ns |
| torl $\dagger$ | Shift Out $\uparrow$ to Output Ready LOW | 5 |  | 45 | ns |
| ${ }^{\text {torH }}{ }^{\dagger}$ | Shift Out $\downarrow$ to Output Ready HIGH |  |  | 50 | ns |
| ${ }^{\text {to }}{ }^{\text {d }}{ }^{+}$ | Output Data Hold (previous word) |  | 12 |  | ns |
| tods | Output Data Shift (next word) |  |  | 40 | ns |
| tpT | Data throughput | 4,8 |  | 1600 | ns |
| ${ }^{\text {tMRORL }}$ | Master Reset \| to Output Ready LOW | 10 |  | 60 | ns |
| ${ }^{\text {t MRIRH }}$ | Master Reset $\dagger$ to Input Ready HIGH* |  |  | 30 | ns |
| tMRIRL | Master Reset \| to Input Ready LOW* |  |  | 50 | ns |
| tMRO | Master Reset \| to Outputs LOW |  |  | 60 | ns |
| tiPH | Input ready pulse HIGH | 4 | 17 |  | ns |
| toph | Output ready pulse HIGH | 8 | 24 |  | ns |
| torD | Output ready 1 to Data Valid | 5 |  | -3 | ns |
| ${ }^{\text {t }} \mathrm{HPZ}$ | Output Disable Delay, C67L4013D | A |  | 30 | ns |
| tPLZ |  |  |  | 30 | ns |
| ${ }^{\text {tPZL }}$ | Output Enable Delay, C67L4013D |  |  | 30 | ns |
| tPZH |  |  |  | 40 |  |

## Note: Typicals at $5 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

* If the FIFO is not full (IR High), $\overline{\mathrm{MR}}$ low forces IR low, followed by IR returning high when $\overline{\mathrm{MR}}$ goes high.
$\dagger$ See $A C$ test and high-speed application note.


Figure A. Enable and Disable
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

## Standard Test Load



Input Pulse Amplitude $=3 \mathrm{~V}$
Input Rise and Fall Time ( $10 \%-90 \%$ ) $=2.5 \mathrm{~ns}$
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

## Functional Description

## Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the $D_{X}$ inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. tpT defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

## Data Output

Data is read from the $O_{x}$ outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

| IOL | R1 | R2 |
| :---: | :---: | :---: |
| 24 mA | $200 \Omega$ | $300 \Omega$ |
| 8 mA | $600 \Omega$ | $1200 \Omega$ |

## Three-State Test Load



Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least tPT) or completely empty (Output Ready stays LOW for at least tPT).

## AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of $0.1 \mu \mathrm{~F}$ directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-InputReady combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-in puise is not recognized until input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (TIDH) and the next activity of Input Ready ( $T_{I R L}$ ) to be extended relative to shift-in going HIGH. This same type of situation occurs with TORL and TORH as related to Shift-Out. For high-speed applications, proper grounding technique is essential.


Figure 1. Input Timing


Figure 2. Typical Waveforms for 15 MHz Shift-In Rate


Figure 3. The Mechanism of Shifting Data into the FIFO

[^43](3) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-in going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low. Note: Shift-In puises applied while Input Ready is LOW will be ignored (See Figure 5).


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH
(1) FIFO is initially full.
(2) Shift Out puised is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH.
(1) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.


Figure 5. Output Timing
(1) The diagram assumes that at this time, words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.


Figure 6. Waveforms for 15 MHz Shift-Out Data Rate
(1) The diagram assumes that at this time words 63,62 and 61 are loaded with $A, B$ and $C$ Data, respectively.
(2) Data in the first crosshatched region may be $A$ or $B$ Data.


Figure 7. The Mechanism of Shifting Data Out of the FIFO
(1) Output Ready HIGH indicates that data is available and a Shift-Out puise may be applied
(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.


Figure 8. tPT and tOPH Specification
(1) FIFO initially empty.
(2) Shift Out held HIGH.

SHIFT OUT


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.
(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 63).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.


Figure 10. Master Reset Timing
(1) FIFO initially partially full.


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# 8-Bit Dynamic-RAM Driver with Three-state Outputs SN54/74S730/-1 SN54/74S734/-1 

## Features/Benefits

- Provides MOS voltage levels for 16K and 64K DRAMs
- Undershoot of low-going output is less than -0.5 V
- Large capacitive drive capability
- Symmetric rise and fall times due to balanced output impedence
- Glitch-free outputs at power-up and power-down
- 20-pin SKINNYDIP®saves space
- 'S730/734 are exact replacement for the Am2965/66
- 'S730/734 are pin-compatible with 'S240/244, and can replace them in many applications
- 'S730-1/734-1 have a larger resistor in the output stage for better undershoot protection
- Commercial devices are specified at VCC $\pm 10 \%$


## Description

The 'S730 and 'S734 are buffers that can drive multiple address and control lines of MOS dynamic RAMs. The 'S730 is an inverting driver, and the 'S734 is a non-inverting driver. The 'S730 is pin-compatible with the 'S240 and an exact replacement for the Am2965. The 'S734 is pin-compatible with the 'S244 and an exact replacement for the Am2966.
These devices have been designed with an additional internal resistor in the lower output driver transistor circuit, unlike regular 8 -bit buffers. This resistor serves two purposes: it causes a slower fall time for a high-to-low transition, and it limits the undershoot without the use of an external series resistor.

## Logic Symbols



## Ordering Information

| PART <br> NUMBER | PKG | TEMP | ENABLE | POLARITY | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54S730/-1 | J,W,L | Mil | Low | Invert |  |
| SN74S730/-1 | N,J,NL | Com |  | S |  |
| SN54S734/-1 | J,W,L | Mil | Low |  |  |
| SN74S734/-1 | N,J,NL | Com | Lown |  |

The 'S730 and 'S734 have been designed to drive the highlycapacitive input lines of dynamic RAMs. The drivers provide a guaranteed $\mathrm{VOH}_{\mathrm{OH}}$ of $\mathrm{V}_{\mathrm{CC}}-1.15 \mathrm{~V}$, limit undershoot to 0.5 V , and exhibit a rise time symmetrical to their fall time by having balanced outputs. These features enhance dynamic RAM performance.
For a better-controlled undershoot for lightly capacitive-loaded circuits the 'S730-1 and 'S734-1 provide a larger resistor in the lower output stage. Also an improved undershoot voltage of -0.3 V is provided in the 'S730-1 and 'S734-1.
A typical fully-loaded-board dynamic-RAM array consists of four banks of dynamic-RAM memory. Each bank has its own $\overline{\text { RAS }}$ and $\overline{C A S}$, but has identical address lines. The $\overline{R A S}$ and $\overline{\mathrm{CAS}}$ inputs to the array can come from one driver, reducing the skew between the $\overline{R A S}$ and $\overline{C A S}$ signals. Also, only one driver is needed to drive eight address lines of a dynamic RAM. The propagation delays are specified for 50 pF and 500 pF load capacitances, and the commercial-range specifications are extended to $V_{C C} \pm 10 \%$.
All of the drivers are available in 20-pin/DIP and 20-pin PLCC packages.

## Function Tables

'S730/-1

| $\overline{E 1}$ | $\overline{E 2}$ | $1 A$ | $2 A$ | $1 Y$ | $2 Y$ |
| :--- | :--- | :--- | :--- | :--- | :--- |
| $L$ | $L$ | $L$ | $L$ | $H$ | $H$ |
| $L$ | $L$ | $L$ | $H$ | $H$ | $L$ |
| $L$ | $L$ | $H$ | $L$ | $L$ | $H$ |
| $L$ | $L$ | $H$ | $H$ | $L$ | $L$ |
| $L$ | $H$ | $L$ | $X$ | $H$ | $Z$ |
| $L$ | $H$ | $H$ | $X$ | $L$ | $Z$ |
| $H$ | $L$ | $X$ | $L$ | $Z$ | $H$ |
| $H$ | $L$ | $X$ | $H$ | $Z$ | $L$ |
| $H$ | $H$ | $X$ | $X$ | $Z$ | $Z$ |

'S734/-1

| $\overline{E 1}$ | E2 | 1A | 2A | 1Y | 2Y |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $L$ | $L$ | $L$ | $L$ | $L$ | $L$ |
| $L$ | $L$ | $L$ | $H$ | $L$ | $H$ |
| $L$ | $L$ | $H$ | $L$ | $H$ | $L$ |
| $L$ | $L$ | $H$ | $H$ | $H$ | $H$ |
| $L$ | $H$ | $L$ | $X$ | $L$ | $Z$ |
| $L$ | $H$ | $H$ | $X$ | $H$ | $Z$ |
| $H$ | $L$ | $X$ | $L$ | $Z$ | $L$ |
| $H$ | $L$ | $X$ | $H$ | $Z$ | $H$ |
| $H$ | $H$ | $X$ | $X$ | $Z$ | $Z$ |

## IEEE Symbol




## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL MIN TYP MAX |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| TA | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | $\operatorname{MIN}^{\text {MII }}$ | $\begin{aligned} & \text { ILITAF } \\ & \text { TYP } \end{aligned}$ | MAX | $\begin{aligned} & \text { COM } \\ & \text { MIN } \end{aligned}$ | $\begin{aligned} & \text { MMER } \\ & \text { TYP } \end{aligned}$ | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}{ }^{*}$ | Low-level input voltage |  | 3 |  |  |  | 0.8 |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}}{ }^{*}$ | High-level input voltage |  | $\cdots$ |  | 2 |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\boldsymbol{y}=-18 \mathrm{~mA}$ |  |  | -1.2 |  |  | -1.2 | V |
| ILL | Low-level input current | Any A | $V_{C C}=M A X$ | $V_{1}=0.4 \mathrm{~V}$ |  |  | -0.2 |  |  | -0.2 | mA |
|  |  | Any E |  |  |  |  | -0.4 |  |  | -0.4 |  |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 |  |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=M A X$ |  |  |  | 0.1 |  |  | 0.1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOL}=1 \mathrm{~mA}$ |  |  | 0.5 |  |  | 0.5 | V |
|  |  |  | $\mathrm{IOL}=12 \mathrm{~mA}$ |  |  | 0.8 |  |  | 0.8 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOH}=-1 \mathrm{~mA}$ | $\begin{array}{cc} V_{C C} & V_{C C} \\ -1.15 & -0.7 \end{array}$ |  |  | $\begin{array}{cc} V_{C C} & V_{C C} \\ -1.15 & -0.7 \end{array}$ |  |  | V |
| IOZL | Off-state output current |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MAX} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -200 |  |  | -200 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  |  | 100 |  |  | 100 | $\mu \mathrm{A}$ |  |
| Ios | Output short-circuit current $\dagger$ |  |  | $V_{C C}=M A X$ |  | -60 |  | -200 | -60 |  | -200 | mA |
| ${ }^{1} \mathrm{OL}$ | Output sink current |  | $\mathrm{VOL}=2.0 \mathrm{~V}$ | 'S7XX | 50 |  |  | 50 |  |  | mA |
|  |  |  | 'S7XX-1 | 40 |  |  | 40 |  |  |  |
| ${ }^{1} \mathrm{OH}$ | Output source current |  |  | $\mathrm{VOH}=2.0 \mathrm{~V}$ |  | -35 |  |  | -35 |  |  | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | Outputs | $V_{C C}=M A X$ <br> Outputs open | 'S730/-1 |  | 24 | 50 |  | 24 | 50 | mA |
|  |  | high |  | 'S734/-1 |  | 53 | 75 |  | 53 | 75 |  |
|  |  | Outputs |  | 'S730/-1 |  | 86 | 125 |  | 86 | 125 |  |
|  |  |  |  | 'S734/-1 |  | 92 | 130 |  | 92 | 130 |  |
|  |  | Outputs disabled |  | 'S730/-1 |  | 86 | 125 |  | 86 | 125 |  |
|  |  |  |  | 'S734/-1 |  | 116 | 150 |  | 116 | 150 |  |

[^44]Switching Characteristics $\mathbf{v}_{\mathbf{C C}}=\mathbf{5 V}, \mathrm{T}_{\mathbf{A}}=25^{\circ} \mathrm{C}$ For the 'S730 and ' S 734

| SYMBOL | PARAMETER | FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Data to output delay | 1 \& 3 | $C_{L}=50 \mathrm{pf}$ | 6 | 9 | 15 | ns |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=500 \mathrm{pf}$ | 18 | 22 | 30 |  |
| ${ }^{\text {tPHL }}$ |  |  | $C_{L}=50 \mathrm{pf}$ | 5 | 7 | 15 |  |
|  |  |  | $C_{L}=500 \mathrm{pf}$ | 18 | 22 | 30 |  |
| ${ }^{\text {t }}$ PZL | Output enable delay | 2 \& 4 | $\mathrm{S}=1$ |  | 12 | 20 | ns |
| ${ }^{\text {t PZH }}$ |  |  | $\mathrm{S}=2$ |  | 12 | 20 |  |
| ${ }^{\text {t PLZ }}$ | Output disable delay | 2 \& 4 | $\mathrm{S}=1$ |  | 11 | 20 | ns |
| ${ }^{\text {t PHZ }}$ |  |  | $\mathrm{S}=2$ |  | 6.5 | 12 |  |
| ${ }^{\text {t SKEW }}$ | Output-to-output skew | $1 \& 3$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ | * | $\pm 0.5$ | $\pm 3.0$ | ns |
| $V_{\text {ONP }}$ | Output voltage undershoot | 1 \& 3 | $C_{L}=50 \mathrm{pf}$ |  | 0 | -0.5 | $\checkmark$ |

*The SKEW timing specification is guaranteed by design, but not tested.
Switching Characteristics Over Operating Range** For the 'S730 and 'S734

| SYMBOL | PARAMETER | FIGURE | TEST CONDITIONS | $\begin{aligned} & \text { MII } \\ & \mathbf{V}_{\mathrm{CC}} \\ & \text { MIN } \end{aligned}$ | $\begin{aligned} & \text { LITARY } \dagger \dagger \\ & =5.0 \mathrm{~V} \pm 10 \% \\ & \text { TYP MAX } \end{aligned}$ |  | MMERCIAL $=5.0 \mathrm{~V} \pm 10 \%$ TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPLH }}$ | Data to output delay | 1 \& 3 | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ | 4 | 20 | 4 | 17 | ns |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=500 \mathrm{pf}$ | 18 | 40 | 18 | 35 |  |
|  |  |  | $C_{L}=50 \mathrm{pf}$ | 4 | 20 | 4 | 17 |  |
| L |  |  | $C_{L}=500 \mathrm{pf}$ | 18 | 40 | 18 | 35 |  |
| ${ }^{\text {tPZL }}$ | Output enable delay | 2 \& 4 | $S=1 \dagger$ |  | 28 |  | 28 | ns |
| ${ }^{\text {tPZH }}$ |  |  | $S=2 \dagger$ |  | 28 |  | 28 |  |
| ${ }^{\text {t PLZ }}$ | Output disable delay | $2 \& 4$ | $S=1 \dagger$ |  | 24 |  | 24 | ns |
| ${ }^{\text {P PHZ }}$ |  |  | $S=2 \dagger$ |  | 16 |  | 16 |  |
| $\mathrm{V}_{\text {ONP }}$ | Output voltage undershoot | 1 \& 3 | $C_{L}=50 \mathrm{pf}$ |  | -0.5 |  | -0.5 | V |

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.
$\dagger$ " $S=1$ " and " $S=2$ " refer to the switch setting in Figure 2.
$\dagger \dagger T_{C}=-55$ to $+125^{\circ} \mathrm{C}$ for flatpack versions.
Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=\mathbf{5 V} \mathrm{V}, \mathrm{T}_{\mathrm{A}}=\mathbf{2 5 ^ { \circ }} \mathrm{C}$ For the 'S730 and 'S734

| SYMBOL | PARAMETER | FIGURE | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Data to output delay | 1 \& 3 | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ | 6 | 9 | 15 | ns |
|  |  |  | $C_{L}=500 \mathrm{pf}$ | 18 | 22 | 30 |  |
| ${ }^{\text {tPHL }}$ |  |  | $C_{L}=50 \mathrm{pf}$ | 5 | 7 | 15 |  |
|  |  |  | $C_{L}=500 \mathrm{pf}$ | 18 | 22 | 40 |  |
| ${ }^{\text {tPZL }}$ | Output enable delay | $2 \& 4$ | $S=1$ |  | 12 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PZH}$ |  |  | $\mathrm{S}=2$ |  | 12 | 20 |  |
| ${ }^{\text {t PLZ }}$ | Output disable delay | $2 \& 4$ | $S=1$ |  | 11 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | $\mathrm{S}=2$ |  | 6.5 | 12 |  |
| ${ }^{\text {t SKEW }}$ | Output-to-output skew | $1 \& 3$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ |  | $\pm 0.5$ | $\pm 3.0$ | ns |
| $\mathrm{V}_{\text {ONP }}$ | Output voltage undershoot | $1 \& 3$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ |  | 0 | -0.3 | V |

${ }^{*}$ The SKEW timing specification is guaranteed by design, but not tested.

Switching Characteristics Over Operating Range** For the 'S730 and 'S734

| SYMBOL | PARAMETER | FIGURE | TEST CONDITIONS | $\begin{array}{\|r\|} \hline \text { MII } \\ \mathbf{V}_{\mathrm{CC}} \\ \text { MIN } \end{array}$ | ITARY $\dagger \dagger$ $=5.0 \mathrm{~V} \pm 10 \%$ TYP MAX |  | MERCIAL <br> $=5.0 \mathrm{~V} \pm 10 \%$ <br> TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | Data to output delay | 1 \& 3 | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ | 4 | 20 | 4 | 17 |  |
|  |  |  | $C_{L}=500 \mathrm{pf}$ | 18 | 40 | 18 | 35 |  |
| ${ }^{\text {tPHL }}$ |  |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ | 4 | 20 | 4 | 17 |  |
|  |  |  | $\mathrm{C}_{\mathrm{L}}=500 \mathrm{pf}$ | 18 | 50 | 18 | 45 |  |
| ${ }^{\text {tPZL }}$ | Output enable delay | 2 \& 4 | $S=1 \dagger$ |  | 28 |  | 28 | ns |
| ${ }^{\text {t }} \mathrm{PZH}$ |  |  | $S=2 \dagger$ |  | 28 |  | 28 |  |
| ${ }^{\text {tPLZ }}$ | Output disable delay | 2 \& 4 | $S=1 \dagger$ |  | 24 |  | 24 | ns |
| ${ }^{\text {t PHZ }}$ |  |  | $S=2 \dagger$ |  | 16 |  | 16 |  |
| $\mathrm{V}_{\text {ONP }}$ | Output voltage undershoot | $1 \& 3$ | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pf}$ |  | -0.3 |  | -0.3 | V |

**AC performance over the operating temperature is guaranteed by testing as defined in Group A, Subgroup 9, Mil Std 883B.
$\dagger " S=1$ " and " $S=2$ " refer to the switch setting in Figure 2.
$\dagger \dagger^{T} C=-55$ to $+125^{\circ} \mathrm{C}$ for flatpack versions.

## Test Loads



Figure 1. Capacitive Load Switching
Figure 2. Three-State Enable/Disable

## Typical Switching Characteristics

## VOLTAGE WAVEFORMS



Figure 3. Output Voltage Levels

## Typical Performance Characteristics:



## Applications

The 'S730 and 'S734 are 8-bit bipolar dynamic RAM drivers and are pin-compatible with the 'S240 and 'S244 respectively.

The actual circuit conditions that arise for driving dynamic RAM memories are as follows: Typically, in dynamic RAM arrays address lines and control lines, $\overline{\mathrm{RAS}}, \overline{\mathrm{CAS}}$, and $\overline{\mathrm{WE}}$ have a fair amount of "daisy chaining." The daisy chaining causes an inductive effect due to the traces in the printed circuit board; the dominant factor in the RAM loading is input capacitance, and these two conditions contribute to the actual driver conditions shown in Figure 7. The result is a transmission line with distributed inductance and capacitance connected to the driver outputs.


Figure 7. RAM Driver Output To Array
The transmission line effect can imply reflections, which in turn cause ringing, and it takes some time before the output settles from the low-to-high transition. On the high-to-low transition, along with ringing, a voltage undershoot can occur, and the circuit takes even longer to settle to an acceptable zero level. The main cause for the shorter high-to-low transition as compared to the low-to-high transition is the output impedance of typical Schottky drivers. Figure 8, shows a typical Schottky driver output stage and Figure 9 shows the output impedance for high and low output states.


Figure 8. Typical Schottky Driver Output


Figure 9. Driver Output Impedance

In Figure 9 when $S=1$, the output is high and the driver output impedance is approximately $30 \Omega 2$. When $\mathrm{S}=2$, the output is low and the driver output impedance is approximately $3 \Omega$. There is a $10: 1$ ratio for the output impedances for the low and high states. The high-to-low transition causes a problem as the output transistor turns on fast due to the low impedance and undershoot results at the RAM inputs.


Figure 10. '\$730 and 'S734 Output Stage


Figure 11. Driver Output Impedence For the 'S730 and 'S734

The 'S730 and 'S734 have a modification in their output stage, in that an internal resistor is added to the lower output stage as shown in Figure 10.
The 'S730-1 and 'S734-1 have a larger resistor, R2, comparted to the "non-dash" parts, which give better undershoot protection at a slightly slower switching performance.
The structure in Figure 10 provides a driver output impedence of approximately $18 \Omega$ to $25 \Omega$ in either high ( $S=1$ ) or low ( $S=2$ ) states as shown in Figure 11. In addition, this circuit limits undershoot to -0.5 V , essentially eliminating that problem; provides a symmetrical rise and fall time; and guarantees output levels of $\mathrm{V}_{\mathrm{CC}}-1.15 \mathrm{~V}$ needed for MOS High levels. Also, when using the 'S730 asnd 'S734, no external resistors are needed. 'S240-series parts used with external resistors to provide drive capability, but the rise times and fall times are unsymmetrical due to higher impedance for low-to-high transitions.
Figure 12 shows the undershoot problem using a 'S240 without external resistors and the elimination of the problem by using the 'S730. Thus from a dynamic-RAM system-design viewpoint, the 'S730 and 'S734 are very effective RAM drivers.


Figure 12. Comparison of Undershoots and tpHL
An application using these 8 -bit drivers to interface address and control lines (and data lines) to a dynamic RAM array using 64 K DRAMs is discussed. The signals needed for the controls are $\overline{R A S}, \overline{C A S}$, and $\overline{W E}$. The address lines are $A O-A 7$ and the data lines are shown as the high and low byte. The array is shown in Figure 13. It consists of four rows of DRAMs; each row has individual $\overline{R A S}, \overline{C A S}$, and $\overline{W E}$ lines. However, all four rows have common address lines AO-A7. The RAM capacitive loading for $\overline{\mathrm{RAS}}, \overline{\mathrm{CAS}}$, and $\overline{\mathrm{WE}}$ is about 10 pf per input. The loading of the address lines is about 5 to 7 pf per input. The loading of the $\overline{\operatorname{AS}}_{i}, \overline{\mathrm{CAS}}_{i}$ and $\overline{W E}_{i}$ inputs to each row of memories is 160 pf . Note that $\overline{\mathrm{RAS}}_{i}$ and $\overline{\mathrm{CAS}}$; come from the same driver, which reduces timings skews which might arise if they were output from separate drivers. The address lines are outputs from another driver, and the loading on each line is 320 pf ( 5 pf loading times 64 DRAMs). At this point it is worth noting that if a $320-\mathrm{pf}$ loading affects performance unduly, then the address lines can be split between two drivers with each having a load of 160 pf, reducing overall signal delay.

If an error-detection-and-correction scheme is used, then typically the row size expands to 22 bits from the 16 bits shown in the exampie. The 'S730 and 'S734 drivers lend themseives to such expansion, as their propagation delays are specified at 50 pF and also at 500 pF .


Figure 13. 256K X 16 Dynamic RAM Array with RAM Drivers

## Features/Benefits

- Supports 16K, 64K, and 256K DRAMs
- Capable of addressing up to $\mathbf{2}$ M 16-bit words or $\mathbf{2}$ M bytes
- On-chip capacitive-load drivers are capable of driving up to 88 DRAMs with 30 -nsec typical address propagation delay and 128 DRAMs with $35-$ nsec typical address propagation delay
- $\overline{\operatorname{RASIN}}$ to $\overline{\mathrm{RAS}}$ delay of 20 nsec max ( $\overline{\mathrm{RAS}}$ driving 22 DRAMs)
- Max and Min skews are specified to simplity system design
- Two $\overline{\text { CASIN }}$ inputs and two $\overline{C A S}$ outputs simplity byte addressing
- An Auto-Access mode with extended $\overline{C A S}$ capability takes advantage of full periormance of $\mathbf{1 2 0}$ and 150 nsec DRAMs
- An output series resistor reduces undershoot


## Modes of Operation

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 673102 | $48 D, 48 \mathrm{~N}, 68 \mathrm{NL}$, | Com |
| 673102 A | 68 NP |  |

## Pin Configurations



## Block Diagram



Figure 1. 673102 Functional Block Diagram

## Description

The 673102 is a 48 -pin LSI device which performs most of the functions needed to control and address Dynamic RAMs. Twenty address inputs, nine address outputs, four $\overline{\text { RAS }}$ outputs, and two CASIN-CAS input-output pairs allow the 673102 to directly address 2 M 16-bit words or bytes. The two CASINn inputs and the two $\overline{\mathrm{CAS}}$ n outputs simplify individual byte access in 16-bit wide memory arrays (see Figure 2).
The 673102 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Reíresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the $\overline{\mathrm{RAS}}$ m outputs, the CASn outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access, and static column mode access.
The Auto-Access mode provides on-chip delays that automatically control the timing delays between $\overline{\text { RASm }} \mathrm{m}$ signals, address multiplexing, and CASn signals. In the Auto-Access mode CASINO-1 inputs serve as enables for the respective CAS0-1 outputs, allowing the access of either or both bytes of the
memory array (for 16-bit wide memory arrays organized in two bytes). In this mode $\overline{\text { CAS }} 0-1$ outputs go HIGH only when the respective CASIN0-1 inputs go HIGH, and the address switches back to row address only when both CASINO and CASIN1 go HIGH. This feature allows extension of the $\overline{\mathrm{CAS}} 0$ or $\overline{\mathrm{CAS}} 1 \mathrm{LOW}$ time and column address time while $\overline{\text { RASIN }}$ and $\overline{\text { RASm can go }}$ HIGH to satisfy the precharge requirements of the dynamic RAMs.
When the Refresh mode is selected ( $\overline{\text { RFSH }}$ is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and $R / \bar{C}$ LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.
The 673102 can drive eight banks of DRAMs. $\overline{\text { RAS }} m$ control signals are used to select a pair of banks, while leaving the other three pairs of banks in standby. The two $\overline{\text { CASn }}$ outputs enable the selection of one bank out of the pair. The address lines and the WE signal can be connected to all eight banks. In a 16-bit wide, byte-oriented, memory array the $\overline{\mathrm{RAS}} \mathrm{m}$ signals select one out of four banks while the CASn signals select the bytes as shown in Figure 2.


Each $\overline{\text { RAS }}$ output drives 16 DRAMs Each $\overline{\text { CAS }}$ output drives 32 DRAMs Each Q0-8 output drives 64 DRAMs WE output drives 64 DRAMs

Figure 2. $\mathbf{6 7 3 1 0 2}$ Addressing Four Banks of 16-bit Memory Array Organized in Two Bytes

## Pin Definitions

VCC, GND: VCC-GND $=5 \mathrm{~V} \pm 10 \%$. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low-inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A $1 \mu \mathrm{~F}$ multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.
R0-R8: Row Address Inputs

## C0-C8: Column Address Inputs

B0-B1: Bank-Pair Select Inputs - Strobed by ADS. Decoded to enable one of the $\overline{\text { RAS }}$ outputs when $\overline{\text { RASIN }}$ goes LOW in the access modes.

Q0-Q8: Multiplexed Address Outputs - Selected from the row address input latch, the column address input latch, or the refresh counter.
$\overline{\text { RASIN }}$ : Row Address Strobe Input - Drives the selected $\overline{\text { RAS }}$ m output in the access modes and all $\overline{\text { RAS }}$ outputs in the Refresh mode.
ADS: Address (Latch) Strobe Input - Strobes input row address, column address and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.
$\overline{O E}$ : Output Enable - When $\overline{O E}$ is LOW the address and control outputs are enabled. When $\overline{O E}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.
R/C्C: Row/Column Select Input - In the Externally-ControlledAccess mode it is used to select either the row address input
latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{\text { AUTO }}$ is HIGH, it is used to select between the refresh address ( $\mathrm{R} / \overline{\mathrm{C}} \mathrm{HIGH}$ ) and the column address ( $\mathrm{R} / \overline{\mathrm{C}}$ LOW). When $\overline{A U T O}$ is LOW R/ $\overline{\mathrm{C}}$ is disabled.
CASIN0-1: Column Address Strobe Inputs - In the Externally-Controlled-Access mode the CASINn directly drives $\overline{\text { CASn out- }}$ put. In the Auto-Access mode each is used to enable the corresponding CASn output (See CAS0-1 description).

## WEIN: Write Enable Input.

## $\overline{W E}$ Write Enable Output.

CAS0-1: Column Address Strobe Outputs - In the Externally-Controlled-Access mode the CAS outputs follow the CASIN inputs. In the Auto-Access mode the CASIN inputs are used to enable the $\overline{C A S}$ outputs. The CAS outputs are asserted LOW, with proper delay from the $\overline{\text { RAS }}$ output, by the $\overline{\text { RASIN }}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{\text { CASn }}$ goes HIGH only when the corresponding $\overline{\text { CASIN }}$ noes HIGH. Extending the CASn LOW duration while RASIN and $\overline{\text { RASm }}$ go HIGH satisfies the precharge requirement of the dynamic RAMs.
RAS0-3: Row Address Strobe Outputs - When $\overline{\text { RFSH }}$ is HIGH the selected row address strobe output (decoded from signals
 outputs go LOW together following RASIN going LOW.
AUTO: Auto-Access Input - When $\overline{A U T O}$ is LOW and $\overline{\text { RFSH }}$ is HIGH the Auto-Access mode is selected (see AutoAccess mode description).
$\overline{\text { RFSH: Refresh Input - When RFSH }}$ is LOW the Refresh mode is selected (see Refresh mode description).

## Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{A U T O}$ and $\overline{\text { FSSH }}$ are held HIGH, the 673102 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{\text { RASm }}$ output selected by the $B 0$ and $B 1$ inputs follows the $\overline{\text { RASIN input, and }}$ each of the $\overline{\text { CAS }}$ outputs follows its corresponding $\overline{\text { CASIN }}$ input. When $\mathrm{R} / \overline{\mathrm{C}}$ is HIGH the row address is enabled onto the $\mathrm{Q} 0-8$ outputs. When R/C is LOW the column address latch is enabled onto Q0-8 outputs.
The $\overline{\text { RASIN }}$ - $\overline{\text { RAS }}, \overline{C A S I N}-\overline{C A S}$, and R/ $\bar{C}-Q 0-8$ control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{\mathrm{CAS}}$ before $\overline{\mathrm{RAS}}$, etc.
To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These
parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics $t_{d 7}$ and $t_{d 8}$ is very useful when designing the delay from $\overline{\text { RASIN }}$ going LOW to $/ \overline{\mathrm{C}}$ and the delay between R/C going LOW to $\overline{\text { CASIN }}$ going LOW (see Applications).

| BANK SELECT (STROBED BY ADS) |  | ENABLED $\overline{\text { RASn }}$ |
| :---: | :---: | :---: |
| B1 | B0 |  |
| 0 | 0 | $\overline{\text { RAS0 }}$ |
| 0 | 1 | $\overline{\text { RAS } 1}$ |
| 1 | 0 | $\overline{\text { RAS2 }}$ |
| 1 | 1 | $\overline{\text { RAS } 3}$ |

Table 1. Memory Bank Decode


Figure 3. Externally-Controlled-Access-- $\overline{\operatorname{RASIN}}$-to- $\overline{\mathrm{RAS}}$ Timing


Figure 4. Externally-Controlled-Access-CASIN to $\overline{C A S}$ Timing


Figure 5. Externally-Controlled-Access R/C Timing

Note: $t_{R C C}$ will be met only if the column address is available $t_{A P D}$ before it appears on Q0-8 outputs or if it is latched by ADS.

## Auto-Access Mode (AA)

In the Auto-Access mode the 673102 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when AUTO is held LOW and $\overline{\text { RFSH }}$ is held HIGH. The R/C input is disabled, and $\overline{\text { RASIN }}$ going LOW initiates the sequence of control signals to access the DRAMs. The CASINO-1 inputs are used as enables for the respective $\overline{\mathrm{CA}}$ S outputs. A LOW on a $\overline{\mathrm{CASIN}} \mathrm{n}$ input enables the
$\overline{\mathrm{CAS}}$ n output to be driven LOW with the internally generated delay from $\overline{R A S}$. Each $\overline{\text { CAS }}$ n output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when both CASINO and $\overline{\mathrm{CASIN}} 1 \mathrm{go} \mathrm{HIGH}$. This feature allows extension of the $\overline{\mathrm{CAS}} 0$ or CAS1 LOW time and the column address time, while RASIN and $\overline{\mathrm{RAS}} \mathrm{m}$ can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabied in this mode.


Figure 6. Auto-Access (AA) Timing

## Refresh Mode (RFSH)

When $\overline{\mathrm{RFSH}}$ is held LOW the refresh counter contents are enabled onto the Q0-8 address outputs, provided either R/ $\overline{\mathrm{C}}$ is held HIGH, or AUTO is held LOW, or both conditions exist. In this mode all four $\overline{\text { RAS }}$ outputs follow the $\overline{\text { RASIN }}$ input signal. The refresh counter increments the refresh address when either $\overline{\text { RASIN }}$ or $\overline{\mathrm{RFSH}}$ goes HIGH while the other is LOW. When $\overline{\text { AUTO }}$ is LOW the CASINO-1 inputs are isolated and CAS0-1 are held HIGH. Also, when $\overline{A U T O}$ is LOW the R/ $\bar{C}$ input is isolated from the output multiplexer, and the refresh address appears at the Q0-8 outputs.
When $\overline{\mathrm{AUTO}}$ is HIGH, pulling R/ $\overline{\mathrm{C}}$ LOW enables the column address onto the Q0-8 outputs. Also, each of the $\overline{\mathrm{CAS}}$ outputs follows its corresponding CASIN input. This feature may be
used when implementing error correction and detection "scrubbing" for two-bank memory array. "Scrubbing" is a term describing the cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed, and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673102 provides the facilities to force a column address onto the Q0-8 address outputs and to assert the $\overline{\mathrm{CAS}} 0-1$ outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter must be added externally to provide the column addresses for scrubbing.
The refresh counter is a 9-bit counter that resets to 0 on powerup and rolls over to 0 at 511 .


Figure 7. Refresh Timing

Note: In the REFRESH mode, $\overline{A U T O}$ must be LOW or R/C must be HIGH to guarantee the refresh address on the Q0-8 outputs.


Figure 8. Address Setup and Hold Time to ADS


Figure 9. Address Input/Output Propagation Delay Note: Row or Column address ( $\overline{\text { RFSH }}=\mathrm{HIGH}$ ).


Figure 10. High-Z Timing


| SYMBOL | PARAMETER | CONDITIONS | FIGURE/ NUMBER | MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VIC | Input clamp voltage | $\mathrm{I}^{\prime} \mathrm{N}=-18 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | $-0.8-1.2$ | V |
| $\mathrm{IIH}^{\text {H }}$ | Input high current | $\mathrm{V}_{\text {IN }}=2.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | 50 | $\mu \mathrm{A}$ |
| ICTL | Output load current for $\overline{\mathrm{RAS}}, \overline{\mathrm{CAS}}, \overline{\mathrm{WE}}$ | $\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ <br> Chip deselect |  | -1.5-2.5 | mA |
| IIL | Input low current except for $\overline{\text { RFSH }}$ | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=\mathrm{MAX}$ |  | -20-250 | $\mu \mathrm{A}$ |
| IILRF | Input low current for $\overline{\text { RFSH }}$ | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -80-500 | $\mu \mathrm{A}$ |
| $V_{\text {IL }}$ | Input low threshold (Note 1) |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | Input high threshold (Note 1) |  |  | 2.0 | V |
| VOL1 | Output low voltage | IOUT $=1 \mathrm{~mA}, \mathrm{~V}_{C C}=\mathrm{MIN}$ |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OL} 2}$ | Output low voltage | lout $=12 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 0.8 | V |
| VOH | Output high voltage | IOUT $=-1 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 2.43 .0 | V |
| IOH | Output source current (Note 2) | $\mathrm{V}_{\text {OUT }}=0.8 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | $\begin{array}{ll}-50 & -140\end{array}$ | mA |
| 1 OL | Output sink current (Note 2) | $\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | $40 \quad 100$ | mA |
| IOZ | Three-state output current (address output) | $0.4 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 2.7 \mathrm{~V}$ <br> $V_{C C}=$ MAX, Chip deselect |  | $\begin{array}{ll}-50 & 50\end{array}$ | $\mu \mathrm{A}$ |
| ICC | Supply current | $V_{C C}=M A X$ |  | $150 \quad 240$ | mA |
| CIN | Input capacitance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 10 | pF |

## Switching Characteristics (See Note 3)

| SYMBOL | EXTERNALLY CONTROLLED ACCESS PARAMETER | FIGURE/ NUMBER | $\begin{aligned} & \text { 673102A } \\ & \text { MIN TYP MAX } \end{aligned}$ | $\begin{gathered} 673102 \\ \text { MIN TYP MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| trHA |  | 5/3 | 0 | 0 | ns |
| trPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay | 3/11 | 20 | 20 | ns |
| trPDH | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay | 3/12 | 31 | 31 | ns |
| ${ }^{\text {t }}$ APD | Address input to output delay | 9/2 | 50 | 50 | ns |
| tWPDL | $\overline{\text { WEIN }}$ to WE LOW delay | 48 | 45 | 45 | ns |
| tWPDH | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ HIGH delay |  | 40 | 40 | ns |
| ${ }^{\text {t CPDL }}$ | $\overline{\text { CASIN }}$ to CAS LOW delay | 4/3 | 28 | 28 | ns |
| ${ }^{\text {t }} \mathrm{CPDOH}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay | 4/4 | 40 | 40 | ns |
| $\mathrm{t}_{\mathrm{R} C \mathrm{C}}$ | Column select to column address valid | 5/5 | 41 | 41 | ns |
| treR | Row select to row address valid | 5/6 | 45 | 45 | ns |
| $t_{\text {d } 1}$ | ( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | $-2 \quad 13$ | -2 13 | ns |
| $t_{d 2}$ | (Address input to output delay)-( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay) |  | 30 | 30 | ns |
| $\mathrm{t}_{\mathrm{d} 3}$ | (Address input to output delay)-( (-ASIN to $\overline{\mathrm{CAS}}$ LOW delay) |  | $-5 \quad 23$ | $\begin{array}{ll}-5 & 23\end{array}$ | ns |
| $t_{d 4}$ | Skew between address output lines |  | 10 | 10 | ns |
| $t_{\text {d } 5}$ | ( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | $\begin{array}{ll}-7 & 13\end{array}$ | -7 13 | ns |
| $t_{\text {d6 }}$ | ( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}} \mathrm{HIGH}$ delay)-( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay) |  | $-12 \quad 12$ | $-12 \quad 12$ | ns |
| tSPD | ADS HIGH to address output valid | 9/1 | 55 | 55 | ns |
| trche | Column addresses remaining valid from R/C HIGH | 5/4 | 0 | 0 | ns |
| $t_{\text {d7 }}$ | trPDL - trHA |  | 13 | 13 | ns |
| $\mathrm{t}_{\mathrm{d} 8}$ | $\mathrm{t}_{\text {RCC }}-\mathrm{t}_{\text {cPDL }}$ |  | 20 | 20 | ns |

## Switching Characteristics (Continued)

| SYMBOL | AUTO ACCESS PARAMETER | FIGURE/ NUMBER | $\begin{gathered} \text { 673102A } \\ \text { MIN TYP MAX } \end{gathered}$ | $\begin{gathered} 673102 \\ \text { MIN TYP MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {RICL }}$ | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ LOW delay | 6/20 | 75 | 85 | ns |
| trCDL | $\overline{\mathrm{RAS}}$ to $\overline{\mathrm{CAS}}$ LOW delay | 6/23 | $30 \quad 65$ | $30 \quad 75$ | ns |
| trPDL | $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay | 6/13 | 20 | 20 | ns |
| tRPDH | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay | 6/14 | 31 | 31 | ns |
| ${ }^{\text {t }}$ APD | Address input to output delay | 6/16 | 50 | 50 | ns |
| tWPDL | $\overline{\text { WEIN }}$ to $\overline{W E}$ LOW delay |  | 45 | 45 | ns |
| tWPDH | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ HIGH delay |  | 40 | 40 | ns |
| ${ }^{\text {t CPPD }}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay | 6/22 | 40 | 40 | ns |
| traH | Row address hold time from $\overline{\mathrm{RAS}}$ LOW | 6/17 | 15 | 15 | ns |
| $\mathrm{t}_{\mathrm{d} 2}$ | (Address input to output delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | 30 | 30 | ns |
| tSPD | ADS HIGH to address output valid | 6/19 | 55 | 55 | ns |
| ${ }^{\text {taSC }}$ | Column address setup to $\overline{\text { CAS }}$ LOW | 6/21 | 0 | 0 | ns |
| tcahc | Column address remaining valid from $\overline{\text { CASINO}} 10$ HIGH | 6/18 | 5 | 5 | ns |
| tASR | Row address valid before $\overline{\mathrm{RAS}}$ LOW | 6/24 | 0 | 0 | ns |
| td5 | ( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay)-( $\overline{\text { RASIN }}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -7 13 | -7 13 | ns |
|  | REFRESH PARAMETER |  |  |  |  |
| trFLCT | $\overline{\text { RFSH }}$ LOW to refresh address valid ( $\overline{A U T O}$ LOW or R/C̄ HIGH) | 7/5 | 40 | 40 | ns |
| trRPDL | $\overline{\text { RASIN }}$ LOW to $\overline{\mathrm{RAS}}$ LOW delay during refresh | 7/11 | 23 | 23 | ns |
| trFPDD | $\overline{\text { RASIN }}$ HIGH to $\overline{\mathrm{RAS}}$ HIGH delay during refresh | 7/12 | 38 | 38 | ns |
| trFAH | Refresh address held from $\overline{\text { RASIN }}$ HIGH ( $\overline{\text { RFSH }}$ LOW) | 7/7 | 0 | 0 | ns |
| trHNC | $\overline{\text { RASIN }}$ HIGH to new refresh address valid | 7/9 | 66 | 66 | ns |
| trafahr | Refresh address held from $\overline{\text { RFSH }}$ HIGH | 7/6 | 0 | 0 | ns |
| tris | Refresh address valid to $\overline{\mathrm{RAS}}$ LOW (provided tRFQS is satisfied) | 7/13 | 0 | 0 | ns |
| trFRDH | $\overline{\mathrm{RFSH}} \mathrm{HIGH}$ to $\overline{\mathrm{RAS}} \mathrm{HIGH}$ (for 3 banks, $\overline{\text { RASIN }}=$ LOW) | 7/15 | 40 | 40 | ns |
| $t_{d 9}$ | ( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}} \mathrm{HIGH}$ delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -9 16 | -9 16 | ns |
|  | THREE-STATE PARAMETER |  |  |  |  |
| ${ }^{\text {t }}$ AZL | $\overline{\mathrm{OE}}$ LOW to address output LOW | 10/1 | 45 | 45 | ns |
| ${ }^{\text {taZH }}$ | $\overline{\text { OE LOW to address output HIGH }}$ | 10/2 | 60 | 60 | ns |
| ${ }^{\text {t }}$ ALZ | $\overline{\mathrm{OE}}$ HIGH to address output HI-Z from LOW | 10/3 | 35 | 35 | ns |
| ${ }^{\text {tahz }}$ | $\overline{\text { OE HIGH to address output HI-Z from HIGH }}$ | 10/4 | 25 | 25 | ns |
| tCTZL | $\overline{\text { OE LOW }}$ to control output LOW | 10/5 | 40 | 40 | ns |
| ${ }^{\text {t }}$ CTZH | $\overline{\text { OE LOW }}$ to control output HIGH | 10/6 | 50 | 50 | ns |
| tCTLZ | $\overline{\text { OE HIGH to control output HI-Z from LOW }}$ | 10/7 | 30 | 30 | ns |
| tCTHZ | $\overline{\text { OE HIGH to control output HI-Z from HIGH }}$ | 10/8 | 25 | 25 | ns |

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.
Note 3: Output load capacitance is typical for four banks of 22 DRAMs with trace capacitance.
The values are: $Q 0-8 C_{L}=500 \mathrm{pF}, \overline{\mathrm{RAS}} 0-3 \mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}, \overline{\mathrm{WE}} \mathrm{C}_{\mathrm{L}}=500 \mathrm{pF}, \overline{\mathrm{CAS} 0}-1 \mathrm{C}_{\mathrm{L}}=300 \mathrm{pF}$.

| Absolute Maximum Ratings (See Note) |  |
| :---: | :---: |
| Supply voltage, VCC | -0.5 V to 7 V |
| Storage temperature range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| Input voltage | -1.5 V to 5.5 V |
| Output current | 150 mA |
| Lead temperature (soldering, 10 seconds) | $300^{\circ} \mathrm{C}$ |

Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

## Operating Conditions

| SYMBOL | PARAMETER | FIGURE/ NUMBER | $\begin{aligned} & 673102 A \\ & \text { MIN TYP MAX } \end{aligned}$ |  | $\begin{gathered} 673102 \\ \text { MIN TYP MAX } \end{gathered}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Supply voltage |  | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Ambient temperature |  | 0 | 75 | 0 | 75 | C |
| $t_{\text {ASA }}$ | Address setup time to ADS LOW | 8/1 | 18 |  | 18 |  | ns |
| ${ }^{\text {t }}$ ADS | Address strobe pulse width HIGH |  | 26 |  | 26 |  | ns |
| ${ }^{\text {taHA }}$ | Address hold time from ADS LOW | 8/2 | 10 |  | 10 |  | ns |
|  | EXTERNALLY CONTROLLED ACCESS PARAMETER |  |  |  |  |  |  |
| ${ }^{\text {taDHAR }}$ | ADS LOW hold from $\overline{\text { RASIN }}$ HIGH | $3 / 7$ | 0 |  | 0 |  | ns |
| tBSR | Bank select setup to $\overline{\text { RASIN }}$ LOW (ADS $=$ HIGH) | 3/8 | 10 |  | 10 |  | ns |
| tBSH | Bank select hold from RASIN HIGH (ADS = HIGH) | 3/9 | 10 |  | 10 |  | ns |
| tSSR | Address strobe HIGH setup to RASIN LOW (B0, B1 STABLE) | 3/10 | 20 |  | 20 |  | ns |
| tAUHE | AUTO hold from RASIN HIGH | 3/4 | 55 |  | 55 |  | ns |
| taUSRC | AUTO HIGH setup to R/C LOW | $5 / 1$ | 25 |  | 25 |  | ns |
| taUHRC | $\overline{\text { AUTO }}$ HIGH hold from R/ट̈ HIGH | 5/2 | 10 |  | 10 |  | ns |
| taUSCA | $\overline{\text { AUTO }}$ HIGH setup to CASIN LOW | $4 / 1$ | 45 |  | 45 |  | ns |
| taUHCA | AUTO HIGH hold from CASIN HIGH | 4/2 | 0 |  | 0 |  | ns |
| ${ }^{t}$ AUS | $\overline{\text { AUTO setup to RASIN LOW }}$ | 3/3 | 0 |  | 0 |  | ns |
| trFSR | $\overline{\text { RFSH }}$ HIGH setup to $\overline{\text { RASIN }}$ LOW (to guarantee tASR) | $3 / 1$ | 10 |  | 10 |  | ns |
| tRFHR | $\overline{\text { RFSH }}$ HIGH hold from $\overline{\text { RASIN }}$ HIGH | $3 / 2$ | 10 |  | 10 |  | ns |
|  | AUTOMATIC ACCESS PARAMETER |  |  |  |  |  |  |
| tadhar | ADS LOW hold from RASIN HIGH | 3/7 | 0 |  | 0 |  | ns |
| $t_{\text {BSR }}$ | Bank select setup to RASIN LOW (ADS = HIGH) | $6 / 12$ | 10 |  | 10 |  | ns |
| tBSH | Bank select hold from RASIN HIGH (ADS = HIGH) | 3/9 | 10 |  | 10 |  | ns |
| tASRL | Address setup to RASIN LOW (ADS = HIGH) <br> ( $\mathrm{t}_{\mathrm{ASRL}}=\mathrm{t}_{\mathrm{d} 2}$ max to guarantee $\mathrm{t}_{\mathrm{ASR}}$ ) | 6/4 | 30 |  | 30 |  | ns |
| ${ }_{\text {taUS }}$ | $\overline{\text { AUTO }}$ setup to $\overline{\text { RASIN }}$ LOW | 6/5 | 0 |  | 0 |  | ns |
| tRFSR | $\overline{\text { RFSH }}$ HIGH setup to $\overline{\text { RASIN }}$ LOW (to guarantee tASR) | 6/6 | 10 |  | 10 |  | ns |
| tSSR | Address strobe HIGH to $\overline{\text { RASIN }}$ LOW (B0, B1 STABLE) | 6/7 | 20 |  | 20 |  | ns |
| tCASA | $\overline{\text { CASINO-1 setup to } \overline{\text { RASIN }} \text { LOW }}$ | 6/8 | -30 |  | -30 |  | ns |
| taUH | $\overline{\text { AUTO }}$ hold from $\overline{\text { RASIN }}$ HIGH | 6/9 | 50 |  | 50 |  | ns |
| taUCH | $\overline{\text { AUTO }}$ LOW hold from CASIN HIGH | 6/10 | 0 |  | 0 |  | ns |
|  | REFRESH PARAMETER |  |  |  |  |  |  |
| tAUHRF | AUTO LOW hold from $\overline{\text { RFSH }}$ HIGH (R/C LOW) | $7 / 1$ | 10 |  | 10 |  | ns |
| tresRf | R/言 HIGH setup to $\overline{\text { RFSH }}$ LOW ( $\overline{\text { AUTO }}$ HIGH) | $7 / 2$ | 20 |  | 20 |  | ns |
| tAUSRF | $\overline{\text { AUTO }}$ LOW setup to $\overline{\text { RFSH }}$ LOW (R/C LOW) | 7/3 | 20 |  | 20 |  | ns |
| tRCHRE | R/ट्ट HIGH hold from निFSH HIGH ( (АUTO HIGH) | $7 / 4$ | 10 |  | 10 |  | ns |
| $t_{\text {RFH }}$ | $\overline{\text { RASIN HIGH during refresh }}$ | 7/10 | 30 |  | 30 |  | ns |
| tRFQS | $\overline{\text { RFSH }}$ LOW setup to RASIN LOW (to guarantee tRFS) | 7/14 | 30 |  | 30 |  | ns |

## 673102 Test Loads (See Note)



Note: Input pulse 0 V to $3.0 \mathrm{~V}, \mathrm{t}_{\mathrm{R}}=\mathrm{t}_{\mathrm{F}}=2.5 \mathrm{~ns}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{t}_{\mathrm{PW}}=200 \mathrm{~ns}$. Input reference point on $A C$ measurements is 1.5 V .
Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

## Control Outputs

| TEST | S1 | S2 | CL | MEASURED AT |
| :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t }}$ PD | Open | Closed | CL | $0.8 \mathrm{~V}, 2.4 \mathrm{~V}$ |
| ${ }^{\text {tPZH }}$ | Open | Closed | CL | 2.4 V |
| ${ }^{\text {tPHZ }}$ | Open | Closed | 15 pF | $\mathrm{VOH}^{-0.5 \mathrm{~V}}$ |
| ${ }^{\text {tPZL }}$ | Open | Open | CL | 0.8 V |
| ${ }^{\text {tPLZ }}$ | Open | Open | 15 pF | $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ |

Where $\mathrm{CL}=150 \mathrm{pF}$ for $\overline{\mathrm{RAS}}, 300 \mathrm{pF}$ for $\overline{\mathrm{CAS}}$, and 500 pF for $\overline{\mathrm{WE}}$.

## Control Driver <br> Output Stage



## Applications

## Microprocessor Interface

The 673102 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 16-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. Two PAL® devices may be used to perform these functions, as
shown in Figure 1. One PAL device is used to generate the refresh clock, while the other performs all arbitration and handshake functions. A hidden refresh (refresh which is transparent to the system) scheme is implemented in the interface PAL device which takes advantage of "free" system time to refresh the memory, and falls back to "forced" refresh when hidden refresh cannot be performed.


Figure 1. A CPU Interfaced to the 673102 Driving 2 M Bytes of Dynamic Memory

## Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is tRAC (Data access time from $\overline{R A S}$ going LOW) or tCAC (Data access time from CAS going LOW), which-
ever results in the later appearance of Data at the dynamic RAM output. Since the $\overline{\text { RAS }} \overline{\text { and }} \overline{\text { CAS }}$ coming out of the controller are initiated by the RASIN, the controller-memory performance is measured from the $\overline{\text { RASIN }}$ HIGH-to-LOW transition (See Figure 2).


Figure 2. Access Time from $\overline{\text { RASIN }}$

The time from $\overline{\operatorname{RASIN}}$ to data is calculated to be the longer of:
$t_{\text {RICL }}+\mathrm{t}_{\mathrm{CAC}}(\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{CAS}}+\overline{\mathrm{CAS}}$ to data)
$t_{\text {RPDL }}+t_{\text {RAC }}(\overline{\text { RASIN }}$ to $\overline{\text { RAS }}+\overline{\text { RAS }}$ to data)
Table 1 illustrates the access times from $\overline{\text { RASIN }}$ achieved for various dynamic RAM speeds.

| CONTROLLER/MEMORY | PARAMETER |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | trac | trPDL | tCAC | $t_{\text {RICL }}$ | ACCESS TIME FROM $\overline{\text { RASIN }}$ |
| 673102/HM256-12 | 120 | 20 | 60 | 85 | 145 |
| 673102A/HM256-12 | 120 | 20 | 60 | 75 | 140 |
| 673102/HM256-15 | 150 | 20 | 75 | 85 | 170 |
| 673102A/HM256-15 | 150 | 20 | 75 | 75 | 170 |
| 673102/MB8265A-10 | 100 | 20 | 50 | 85 | 135 |
| 673102A/MB8265A-10 | 100 | 20 | 50 | 75 | 125 |
| 673102/MB8265A-12 | 120 | 20 | 60 | 85 | 145 |
| 673102A/MB8265A-12 | 120 | 20 | 60 | 75 | 140 |
| 673102/IMS2620-10 | 100 | 20 | 60 | 85 | 145 |
| 673102A/IMS2620-10 | 100 | 20 | 60 | 75 | 135 |
| 673102/IMS2620-12 | 120 | 20 | 70 | 85 | 155 |
| 673102A/IMS2620-12 | 120 | 20 | 70 | 75 | 145 |

Table 1. Access Times from $\overline{\text { RASIN }}$ for Various Memory Speeds

## 673102 Parameters

tRPDL - $\overline{\text { RASIN }}$ LOW to $\overline{R A S}$ LOW delay
tricL - $\overline{\text { RASIN }}$ TO $\overline{\text { CAS }}$ LOW delay

## DRAM Parameters

trAC - Access time from $\overline{R A S}$ LOW
${ }^{t}$ CAC - Access time from $\overline{\text { CAS }}$ LOW

## Using the Externally Controlled Access

In the Externally Controlled Access mode RASIN controls the selected $\overline{\mathrm{RAS}}$ output, and the $\overline{\mathrm{CASIN}} 0,1$ inputs control $\overline{\mathrm{CAS}} 0,1$ outputs respectively. The R/C input controls the address multiplexer. The system designer may create, using the RASIN, CASIN and $R / \bar{C}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access
modes such as Nibble mode, Page mode, and static column mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.


Figure 3. The 673102 in the Externally-Controlled Access Mode

## Externally Controlled Access (ECA) (Continued)

## Example 1: Computing $\overline{\operatorname{RASIN}}$ to $\mathbf{R} / \overline{\mathbf{C}}$ Delay

The delay between $\overline{\text { RASIN }}$ going LOW to R/C going LOW (tRASINRC) which is required in order to satisfy the dynamic RAMs' row address hold time (tRAH) is computed as follows:
$t_{\text {RASINRC }}=$ trAH $(\mathrm{min})+\mathrm{t}_{\mathrm{d} 7}$
Where:
$t_{\text {RAH }}(\mathrm{min})$ - Row address hold time (dynamic RAM parameter)
$t_{d 7}(\max )=t_{\text {RPDL }}{ }^{-t_{R H A}}$
tRPDL - $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay
trHA - Row address held valid from R/C LOW

## Example 2: Computing R/C to $\overline{\text { CASIN Delay }}$

The delay between R/C going LOW and $\overline{C A S I N}$ going LOW ( $\mathrm{t}_{\text {RCCASIN }}$ ) which is required in order to satisfy the dynamic RAMs' column address setup ( $\mathrm{t}_{\mathrm{ASC}}$ ) is computed as follows:
$\mathrm{t}_{\text {RCCASIN }}=\mathrm{t}_{\text {ASC }}($ min $)+\mathrm{t}_{\mathrm{d} 8}+$ tpD F32(max)
Where:
${ }^{t}$ ASC $(\min )$ - Column address setup (dynamic RAM parameter)
$t_{d 8}(\max )=t_{R C C}-t_{C P D L}$
$t_{R C C}-R / \bar{C}$ low to column address valid
${ }^{\mathrm{t}} \mathrm{CPDL}$ - $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay
$t_{\text {PD F }}$ F32(max) - Propagation delay of the OR gate used to validate CASIN
Better system performance may be achieved using the $\mathrm{t}_{\mathrm{d} 7}, \mathrm{t}_{\mathrm{d} 8}$ switching parameters to calculate tRASINRC and tRCCASIN than when using the tRPDL, tRCDL, tRCC and thHA parameters (see $\mathrm{t}_{\mathrm{d} 7}, \mathrm{t}_{\mathrm{d} 8}$ in Externally Controlled Access switching parameters).


Figure 4. Externally Controlled Access Timing

## Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to $\mathbf{8} \mathbf{M} 16$-bit words or $\mathbf{8}$ M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with 35 -nsec typical address propagation delay
- $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ delay of 20 nsec $\max (\overline{\text { RAS }}$ driving 22 DRAMs)
- Max and Min skews are specified to simplity system design
- Two CASIN inputs and two CAS outputs simplity byte addressing
- An Auto-Access mode with extended CAS capability takes advantage of full performance of 120 and 150 nsec DRAMs
- An output series resistor reduces undershoot


## Modes of Operation

- Refresh
- Auto Access (AA)
- Externally Controlled Access (ECA)



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 673103 | Com |  |
| 673103 A |  | $68 \mathrm{NL}, 68 \mathrm{NP}$ |

Pin Configurations


Switching Characteristics (Continued)

| SYMBOL | AUTO ACCESS PARAMETER | FIGURE/ NUMBER | $\begin{aligned} & \text { 673103A } \\ & \text { MIN TYP MAX } \end{aligned}$ | $\begin{gathered} 673103 \\ \text { MIN TYP MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| tricl | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ LOW delay | 6/20 | 75 | 85 | ns |
| trCDL | $\overline{\mathrm{RAS}}$ to $\overline{\mathrm{CAS}}$ LOW delay | 6/23 | $30 \quad 65$ | $30 \quad 75$ | ns |
| trPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay | 6/13 | 20 | 20 | ns |
| tRPDH | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay | 6/14 | 31 | 31 | ns |
| ${ }^{\text {t }}$ APD | Address input to output delay | 6/16 | 50 | 50 | ns |
| tWPDL | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ LOW delay |  | 45 | 45 | ns |
| tWPDH | $\overline{\text { WEIN }}$ to $\overline{\text { WE HIGH delay }}$ |  | 40 | 40 | ns |
| ${ }^{\text {t }} \mathrm{CPDH}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay | 6/22 | 40 | 40 | ns |
| traH | Row address hold time from $\overline{\mathrm{RAS}}$ LOW | 6/17 | 15 | 15 | ns |
| $\mathrm{t}_{\mathrm{d} 2}$ | (Address input to output delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | 30 | 30 | ns |
| tSPD | ADS HIGH to address output valid | 6/19 | 55 | 55 | ns |
| ${ }^{\text {t }}$ ASC | Column address setup to $\overline{\mathrm{CAS}}$ LOW | 6/21 | 0 | 0 0 | ns |
| ${ }^{\text {t CAHC }}$ | Column address remaining valid from $\overline{\text { CASINO}}-1$ HIGH | 6/18 | 5 | 5 | ns |
| ${ }^{\text {t ASR }}$ | Row address valid before $\overline{\mathrm{RAS}} \mathrm{LOW}$ | 6/24 | 0 | 0 | ns |
| $t_{\text {d5 }}$ | ( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ HIGH delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -7 | -7 13 | ns |
|  | REFRESH PARAMETER |  |  |  |  |
| trfLCT | $\overline{\text { RFSH LOW to refresh address valid }}$ ( $\overline{\text { AUTO }}$ LOW or R/C CIGH ) | 7/5 | 40 | 40 | ns |
| trapPD | $\overline{\text { RASIN }}$ LOW to $\overline{\mathrm{RAS}}$ LOW delay during refresh | 7/11 | 23 | 23 | ns |
| trapdh | $\overline{\text { RASIN }}$ HIGH to $\overline{\mathrm{RAS}}$ HIGH delay during refresh | 7/12 | 38 | 38 | ns |
| trFAH | Refresh address held from $\overline{\text { RASIN }}$ HIGH ( $\overline{\text { RFSH }}$ LOW) | 7/7 | 0 | 0 | ns |
| trHNC | RASIN HIGH to new refresh address valid | 7/9 | 66 | 66 | ns |
| trfaHR | Refresh address held from $\overline{\text { RFSH }}$ HIGH | 7/6 | 0 | 0 | ns |
| tris | Refresh address valid to $\overline{\mathrm{RAS}}$ LOW (provided tRFQS is satisfied) | 7/13 | 0 | 0 | ns |
| trFRDH | $\overline{\text { RFSH }}$ HIGH to $\overline{\text { RAS }}$ HIGH (for 3 banks, $\overline{\text { RASIN }}=$ LOW) | 7/15 | 40 | 40 | ns |
| $\mathrm{t}_{\mathrm{d} 9}$ | ( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay)-( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay) |  | -9 16 | -9 16 | ns |
|  | THREE-STATE PARAMETER |  |  |  |  |
| ${ }^{\text {t }}$ AZL | $\overline{\text { OE }}$ LOW to address output LOW | 10/1 | 45 | 45 | ns |
| ${ }^{\text {taZ }}$ H | $\overline{\mathrm{OE}}$ LOW to address output HIGH | 10/2 | 60 | 60 | ns |
| ${ }^{\text {t }}$ LLZ | $\overline{\mathrm{OE}}$ HIGH to address output $\mathrm{HI}-\mathrm{Z}$ from LOW | 10/3 | 35 | 35 | ns |
| ${ }^{\text {taHz }}$ | $\overline{\mathrm{OE}} \mathrm{HIGH}$ to address output $\mathrm{HI}-\mathrm{Z}$ from HIGH | 10/4 | 25 | 25 | ns |
| ${ }^{\text {t CTEL }}$ | $\overline{\text { OE LOW to control output LOW }}$ | 10/5 | 40 | 40 | ns |
| ${ }^{\text {t }}$ CTZH | $\overline{\mathrm{OE}}$ LOW to control output HIGH | 10/6 | 50 | 50 | ns |
| tCTLZ | $\overline{\mathrm{OE}}$ HIGH to control output HI-Z from LOW | 10/7 | 30 | 30 | ns |
| tCTHZ | $\overline{\text { OE }}$ HIGH to control output HI-Z from HIGH | 10/8 | 25 | 25 | ns |

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.
Note 3: Output load capacitance is typical for four banks of 22 DRAMs with trace capacitance. The values are: $Q 0-8 C_{L}=500 \mathrm{pF}, \overline{\mathrm{RAS}} 0-3 \mathrm{C}_{\mathrm{L}}=150 \mathrm{pF}, \overline{\mathrm{WE}} \mathrm{C}_{\mathrm{L}}=500 \mathrm{pF}, \overline{\mathrm{CAS}} 0-1 \mathrm{C}_{\mathrm{L}}=300 \mathrm{pF}$.


## Block Diagram



## Description

The 673103 is an LSI device, provided in 52-pin and 68 -pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four RAS outputs, and two $\overline{\mathrm{CASIN}}-\overline{\mathrm{CAS}}$ input-output pairs allow the 673103 to directly address 8 M 16-bit words or bytes. The $\overline{\text { CASINn inputs and the CASn outputs }}$ simplify individual byte access in 16 -bit wide memory arrays (see Figure 2).
The 673103 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the $\overline{R A S}$ m outputs, the $\overline{\mathrm{CAS}}$ n outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access, and static column mode access.
The Auto-Access mode provides on-chip delays that automatically control the timing delays between $\overline{\mathrm{RAS}} \mathrm{m}$ signals, address multiplexing, and $\overline{\mathrm{CAS}} \mathrm{n}$ signals. In the Auto-Access mode $\overline{\mathrm{CASIN}} 0-1$ inputs serve as enables for the respective $\overline{\mathrm{CAS}} 0-1$
outputs, allowing the access of any byte of the memory array (for 16 -bit wide memory arrays organized in two bytes). In this mode CASO-1 outputs go HIGH only when the respective CASIN $0-1$ inputs go HIGH, and the address switches back to row address only when both $\overline{\text { CASIN }} 0-1$ go HIGH. This feature allows extension of the $\overline{C A S}$ LOW time, and column address time while $\overline{\text { RASIN }}$ and $\overline{\text { RASm }}$ can go HIGH to satisfy the precharge requirements of the dynamic RAMs.
When the Refresh mode is selected ( $\overline{\mathrm{RFSH}}$ is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and $\mathrm{R} / \overline{\mathrm{C}}$ LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.
The 673103 can drive eight banks of DRAMs. $\overline{\text { RASm }}$ control signals are used to select a pair of banks, while leaving the other banks in standby. The two $\overline{\text { CAS }} n$ outputs enable the selection of one bank out of two. The address lines and the $\overline{W E}$ signal can be connected to all eight banks. In a 16 -bit wide, byte-oriented, memory array the $\overline{\mathrm{RAS}} \mathrm{m}$ signals select the banks while the $\overline{\mathrm{CAS}} \mathrm{n}$ signals select the bytes, as shown in Figure 2.


ADDRESS


Each $\overline{\text { RAS }}$ output drives 16 DRAMs Each $\overline{\text { CAS }}$ output drives 32 DRAMs Each Q0-9 output drives 64 DRAMs $\overline{W E}$ output drives 64 DRAMs

Figure 2. 673103 Addressing Four Banks of 16-bit Memory Array Organized in Two Bytes

## Pin Definitions

VCC, GND: VCC-GND $=\mathbf{5} \mathrm{V} \pm \mathbf{1 0 \%}$. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low-inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A $1-\mu \mathrm{F}$ multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.
R0-R9: Row Address Inputs
C0-C9: Column Address Inputs
B0-B1: Bank-Pair Select Inputs - Strobed by ADS. Decoded to enable one of the $\overline{\text { RAS }}$ outputs when $\overline{\text { RASIN }}$ goes LOW in the access modes.
Q0-Q9: Multiplexed Address Outputs - Selected from the row address input latch, the column address input latch, or the refresh counter.
RASIN: Row Address Strobe Input - Drives the selected $\overline{\text { RAS }} m$ output in the access modes, and all $\overline{\operatorname{RAS}}$ outputs in the Refresh mode.
ADS: Address (Latch) Strobe Input - Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.
$\overline{\mathrm{OE}}$ : Output Enable - When $\overline{\mathrm{OE}}$ is LOW the address and control outputs are enabled. When $\overline{\mathrm{OE}}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.
R/C: Row/Column Select Input - In the Externally-ControlledAccess mode, it is used to select either the row address input
latch or the column address input latch onto the address outputs. In the Refresh mode, when $\overline{\mathrm{AUTO}}$ is HIGH , it is used to select between the refresh address ( $\mathrm{R} / \overline{\mathrm{C}} \mathrm{HIGH}$ ) and the column address ( $\mathrm{R} / \overline{\mathrm{C}}$ LOW). When $\overline{\mathrm{AUTO}}$ is LOW R/ $\overline{\mathrm{C}}$ is disabled.
CASIN0-1: Column Address Strobe Inputs - In the Externally-Controlled-Access mode, the $\overline{\text { CASIN }} n$ directly drives the $\overline{\text { CASn }}$ output. In the Auto-Access mode, it is used to enable the corresponding $\overline{\mathrm{CAS}}$ output (See $\overline{\mathrm{CAS}} 0-1$ description).

## WEIN: Write Enable Input.

## $\overline{\text { WE: Write Enable Output. }}$

CAS0-1: Column Address Strobe Outputs - In the Externally-Controlled-Access mode the CAS outputs follow the CASIN inputs. In the Auto-Access mode the CASIN inputs are used to enable the $\overline{\mathrm{CAS}}$ outputs. The $\overline{\mathrm{CAS}}$ outputs are asserted LOW, with proper delay from the $\overline{\mathrm{RAS}}$ output, by the $\overline{\mathrm{RASIN}}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{\mathrm{CAS}}$ goes HIGH only when the corresponding $\overline{\mathrm{CASINn}}$ goes HIGH. Extending the CASn LOW duration while $\overline{\text { RASIN }}$ and $\overline{\mathrm{RAS}} \mathrm{m}$ go HIGH to satisfy precharge requirements of the dynamic RAMis.
(RAS0-3: Row Address Strobe Outputs - When $\overline{\text { RFSH }}$ is HIGH the selected row address strobe output (decoded from signals
 outputs go LOW together following RASIN going LOW.

[^45]
## Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{A U T O}$ and $\overline{\text { FFSH }}$ are held HIGH, the 673103 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{\text { RASm output }}$ selected by the B0 and B1 inputs follows the RASIN input, and each of the CAS outputs follows its corresponding $\overline{C A S I N}$ input. When R/ $\overline{\mathrm{C}}$ is HIGH the row address is enabled onto the Q0-9 outputs. When R/C is LOW the column address iatch is enabled onto Q0-9 outputs.
The $\overline{\text { RASIN }}-\overline{\text { RAS }}, \overline{\text { CASIN }}-\overline{\mathrm{CAS}}$, and R/C - Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{\mathrm{CAS}}$ before $\overline{\mathrm{RAS}}$, etc.
To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These
parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics $t_{d 7}$ and $t_{d 8}$ is very useful when designing the delay from $\overline{\text { RASIN }}$ going LOW to $R / \overline{\mathrm{C}}$ and the delay between R/C going LOW to $\overline{\text { CASIN }}$ going LOW (see Applications).

| BANK SELECT (STROBED BY ADS) |  | ENABLED $\overline{\text { RASn }}$ |
| :---: | :---: | :---: |
| B1 | Bo |  |
| 0 | 0 | $\overline{\mathrm{RAS} 0}$ |
| 0 | 1 | $\overline{\mathrm{RAS} 1}$ |
| 1 | 0 | $\overline{\mathrm{RAS} 2}$ |
| 1 | 1 | $\overline{\mathrm{RAS} 3}$ |

Table 1. Memory Bank Decode


Figure 3. Externally Controlled Access-- $\overline{\operatorname{RASIN}}-\mathrm{to}-\overline{\mathrm{RAS}}$ Timing


Figure 4. Externally Controlled Access-प्CASIN to $\overline{\mathbf{C A S}}$ Timing


Figure 5. Externally Controlled Access R/C Timing

## Auto-Access Mode (AA)

In the Auto-Access mode the 673103 provides the system designer with built-in delays and sequencing to accommodate DRAMs with 150 nanoseconds and faster access time. The Auto-Access mode is selected when AUTO is held LOW and $\overline{\text { RFSH }}$ pin is held HIGH. The R/C input is disabled, and $\overline{\text { RASIN }}$ goes LOW initiating the sequence of control signals to access the DRAMs. The CASIN0-1 inputs are used as enables for the respective $\overline{\mathrm{CAS}}$ outputs. A LOW on a $\overline{\mathrm{CASIN}} n$ input enables the
$\overline{\mathrm{CAS}}$ n output to be driven LOW with the internally-generated delay from $\overline{\mathrm{RAS}}$. Each $\overline{\mathrm{CAS}}$ output goes HIGH only when the corresponding CASINn input goes HIGH, and the address switches back to row address only when all CASIN go HIGH. This feature allows extension of the $\overline{C A S}$ LOW time and the column address time, while $\overline{\text { RASIN }}$ and $\overline{\text { RASm }}$ can go HIGH to satisfy precharge requirements of the dynamic RAMs. The R/C input is disabled in this mode.


Figure 6. Auto-Access (AA) Timing

## Refresh Mode (RFSH)

When $\overline{\text { RFSH }}$ is held LOW the refresh counter contents are enabled onto the Q0-9 address outputs, provided either $\mathrm{R} / \mathrm{C}$ is held HIGH, or AUTO is held LOW, or both conditions exist. In this mode all four $\overline{\mathrm{RAS}}$ outputs follow the $\overline{\text { RASIN }}$ input signal. The refresh counter increments the refresh address when either $\overline{\text { RASIN }}$ or RFSH goes HIGH while the other is LOW. When AUTO is LOW the CASINO-1 inputs are isolated and CASO-1 are held HIGH. Also, when $\overline{\text { AUTO }}$ is LOW the R/C input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.
When $\overline{A U T O}$ is HIGH, pulling R/C LOW enables the column address onto the Q0-9 outputs. Also, each of the $\overline{\mathrm{CAS}}$ outputs follows its respective $\overline{\mathrm{CASIN}}$ input. This feature may be used
when implementing error correction and detection "scrubbing" for two-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed, and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673103 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the CASO-1 outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column address for scrubbing.

The refresh counter is a 10-bit counter that resets to 0 on powerup and rolls over to 0 at 1023.


Figure 7. Refresh Timing


Figure 8. Address Setup and Hold Time to ADS
Figure 9. Address Input/Output Propagation Delay


Figure 10. High-Z Timing

## Absolute Maximum Ratings (See Note)



## Operating Conditions

| SYMBOL | PARAMETER | FIGURE/ NUMBER | $\begin{aligned} & \text { 673103A } \\ & \text { MIN TYP MAX } \end{aligned}$ |  | $\begin{gathered} 673103 \\ \text { MIN TYP MAX } \end{gathered}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{C C}$ | Supply voltage |  | 4.5 | 5.5 | 4.5 | 5.5 | V |
| TA | Ambient temperature |  | 0 | 75 | 0 | 75 | C |
| ${ }_{\text {t }}$ ASA | Address setup time to ADS LOW | 8/1 | 18 |  | 18 |  | ns |
| tads | Address strobe pulse width HIGH |  | 26 |  | 26 |  | ns |
| ${ }^{\text {taHA }}$ | Address hold time from ADS LOW | 8/2 | 10 |  | 10 |  | ns |
|  | EXTERNALLY CONTROLLED ACCESS PARAMETER |  |  |  |  |  |  |
| ${ }^{\text {tadHAR }}$ | ADS LOW hold from $\overline{\text { RASIN }}$ HIGH | 3/7 | 0 |  | 0 |  | ns |
| $t_{\text {BSR }}$ | Bank select setup to $\overline{\text { RASIN }}$ LOW (ADS $=$ HIGH) | 3/8 | 10 |  | 10 |  | ns |
| tBSH | Bank select hold from RASIN HIGH (ADS = HIGH) | 3/9 | 10 |  | 10 |  | ns |
| tSSR | Address strobe HIGH setup to $\overline{\text { RASIN }}$ LOW (B0, B1 STABLE) | 3/10 | 20 |  | 20 |  | ns |
| $t^{\text {taUHE }}$ | $\overline{\text { AUTO }}$ hold from RASIN HIGH | 3/4 | 55 |  | 55 |  | ns |
| taUSRC | $\overline{\text { AUTO }}$ HIGH setup to R/C LOW | 5/1 | 25 |  | 25 |  | ns |
| taUHRC | $\overline{\text { AUTO }}$ HIGH hold from R/टे HIGH | 5/2 | 10 |  | 10 |  | ns |
| tausca | $\overline{\text { AUTO }}$ HIGH setup to CASIN LOW | 4/1 | 45 |  | 45 |  | ns |
| $t_{\text {AUHCA }}$ | $\overline{\text { AUTO }}$ HIGH hold from CASIN HIGH | 4/2 | 0 |  | 0 |  | ns |
| taUS | $\overline{\text { AUTO }}$ setup to RASIN LOW | 3/3 | 0 |  | 0 |  | ns |
| trFSR | $\overline{\text { RFSH }}$ HIGH setup to $\overline{\text { RASIN }}$ LOW (to guarantee tASR) | 3/1 | 10 |  | 10 |  | ns |
| trFHR | $\overline{\text { RFSH }}$ HIGH hold from $\overline{\text { RASIN }}$ HIGH | 3/2 | 10 |  | 10 |  | ns |
|  | AUTOMATIC ACCESS PARAMETER |  |  |  |  |  |  |
| tadHAR | ADS LOW hold from $\overline{\text { RASIN }}$ HIGH | 3/7 | 0 |  | 0 |  | ns |
| tBSR | Bank select setup to RASIN LOW (ADS = HIGH) | 6/12 | 10 |  | 10 |  | ns |
| $t_{\text {tBSH }}$ | Bank select hold from $\overline{\text { RASIN }}$ HIGH (ADS = HIGH) | 3/9 | 10 |  | 10 |  | ns |
| ${ }^{\text {t }}$ ASRL | Address setup to $\overline{\text { RASIN }}$ LOW (ADS $=$ HIGH) ( $\mathrm{t}_{\mathrm{ASRL}}=\mathrm{t}_{\mathrm{d} 2}$ max to guarantee $\mathrm{t}_{\mathrm{ASR}}$ ) | 6/4 | 30 |  | 30 |  | ns |
| ${ }_{\text {taUS }}$ | $\overline{\text { AUTO }}$ setup to $\overline{\text { RASIN }}$ LOW | 6/5 | 0 |  | 0 |  | ns |
| tRFSR | $\overline{\text { RFSH }}$ HIGH setup to RASIN LOW (to guarantee tASR) | 6/6 | 10 |  | 10 |  | ns |
| tSSR | Address strobe HIGH to $\overline{\text { RASIN }}$ LOW (B0, B1 STABLE) | 6/7 | 20 |  | 20 |  | ns |
| tCASR | $\overline{\text { CASIN } 0-1 ~ s e t u p ~ t o ~ \overline{R A S I N ~}}$ LOW | 6/8 | -30 |  | -30 |  | ns |
| ${ }^{\text {taUH }}$ | $\overline{\text { AUTO }}$ hold from RASIN HIGH | 6/9 | 50 |  | 50 |  | ns |
| taUCH | $\overline{\text { AUTO }}$ LOW hold from CASIN HIGH | 6/10 | 0 |  | 0 |  | ns |
|  | REFRESH PARAMETER |  |  |  |  |  |  |
| tAUHRF | $\overline{\text { AUTO }}$ LOW hold from $\overline{\text { RFSH }}$ HIGH (R/C COW$)$ | 7/1 | 10 |  | 10 |  | ns |
| trCSRF | R/言 HIGH setup to $\overline{\text { RFSH }}$ LOW ( $\overline{\text { AUTO }}$ HIGH) | 7/2 | 20 |  | 20 |  | ns |
| taUSRF | $\overline{\text { AUTO }}$ LOW setup to $\overline{\text { RFSH }}$ LOW (R/ट्C LOW) | 7/3 | 20 |  | 20 |  | ns |
| trCHRF | R// $\overline{\mathrm{C}}$ HIGH hold from $\overline{\text { RFSH }}$ HIGH ( (АUTO HIGH) | $7 / 4$ | 10 |  | 10 |  | ns |
| tRFH | $\overline{\text { RASIN }}$ HIGH during refresh | 7/10 | 30 |  | 30 |  | ns |
| tRFQS | $\overline{\text { RFSH }}$ LOW setup to $\overline{\text { RASIN }}$ LOW (to guarantee trFS) | 7/14 | 30 |  | 30 |  | ns |

Electrical Characteristics $\mathbf{V C C}_{\mathbf{C l}}=5 \mathrm{~V} \pm 10 \%, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 75^{\circ} \mathrm{C}$. Typicals are for $\mathrm{V}_{\mathbf{C C}}=\mathbf{5 V}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | CONDITIONS | FIGURE/ NUMBER | MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VIC | Input clamp voltage | $\mathbb{I}_{1 N}=-18 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | -0.8-1.2 | V |
| IIH | Input high current | $\mathrm{V}_{\text {IN }}=2.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | 50 | $\mu \mathrm{A}$ |
| ICTL | Output load current for $\overline{\mathrm{RAS}}, \overline{\mathrm{CAS}}, \overline{\text { WE }}$ | $\text { VOUT }=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ <br> Chip deselect |  | -1.5-2.5 | mA |
| IIL | Input low current except for $\overline{\text { RFSH }}$ | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=\mathrm{MAX}$ |  | -20-250 | $\mu \mathrm{A}$ |
| IILRF | Input low current for $\overline{\text { RFSH }}$ | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -80-500 | $\mu \mathrm{A}$ |
| $V_{\text {IL }}$ | Input low threshold (Note 1) |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | Input high threshold (Note 1) |  |  | 2.0 | V |
| $\mathrm{V}_{\text {OL1 }}$ | Output low voltage | $\mathrm{I}_{\text {OUT }}=1 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OL} 2}$ | Output low voltage | IOUT $=12 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 0.8 | V |
| VOH | Output high voltage | IOUT $=-1 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | $2.4 \quad 3.0$ | V |
| IOH | Output source current (Note 2) | $\mathrm{V}_{\text {OUT }}=0.8 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | -50 -140 | mA |
| 1 OL | Output sink current (Note 2) | $\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | $40 \quad 100$ | mA |
| loz | Three-state output current (address output) | $\begin{aligned} & 0.4 \mathrm{~V} \leq \mathrm{V}_{\text {OUT }} \leq 2.7 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=\text { MAX, Chip deselect } \end{aligned}$ |  | $\begin{array}{ll}-50 & 50\end{array}$ | $\mu \mathrm{A}$ |
| ICC | Supply current | $V_{C C}=M A X$ |  | $170 \quad 260$ | mA |
| CIN | Input capacitance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 10 | pF |

## Switching Characteristics (See Note 3)

| SYMBOL | EXTERNALLY CONTROLLED ACCESS PARAMETER | FIGURE/ NUMBER | $\begin{aligned} & \text { 673103A } \\ & \text { MIN TYP MAX } \end{aligned}$ | $\begin{gathered} 673103 \\ \text { MIN TYP MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| tRHA | Row addresses remaining valid from R//̄ LOW | 5/3 | 0 | 0 | ns |
| tRPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay | 3/11 | 20 | 20 | ns |
| tRPDH | $\overline{\text { RASIN }}$ to $\overline{R A S}$ HIGH delay | 3/12 | 31 | 31 | ns |
| ${ }^{\text {t APD }}$ | Address input to output delay | 9/2 | 50 | 50 | ns |
| TWPDL | $\overline{\text { WEIN }}$ to WE LOW delay |  | 45 | 45 | ns |
| TWPDH | $\overline{\text { WEIN }}$ to WE HIGH delay |  | 40 | 40 | ns |
| ${ }^{\text {t }}$ CPDL | $\overline{\text { CASIN }}$ to CAS LOW delay | 4/3 | 28 | 28 | ns |
| ${ }^{\text {t }} \mathrm{CPDOH}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay | 4/4 | 40 | 40 | ns |
| trec | Column select to column address valid | 5/5 | 41 | 41 | ns |
| tRCR | Row select to row address valid | 5/6 | 45 | 45 | ns |
| $\mathrm{t}_{\mathrm{d} 1}$ | ( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -2 13 | -2 13 | ns |
| $t_{d 2}$ | (Address input to output delay)-(-ᄌ) | - | 30 | 30 | ns |
| $t_{\text {d }}$ | (Address input to output delay)-( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay) |  | -5 23 | -5 23 | ns |
| $\mathrm{t}_{\mathrm{d} 4}$ | Skew between address output lines |  | 10 | 10 | ns |
| td5 | ( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay)-( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay) |  | -7 | -7 | ns |
| $\mathrm{t}_{\mathrm{d} 6}$ | ( $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay)-(CASIN to $\overline{\text { CAS }}$ LOW delay) |  | -12 12 | -12 12 | ns |
| tSPD | ADS HIGH to address output valid | 9/1 | 55 | 55 | ns |
| trCHC | Column addresses remaining valid from R/C HIGH | 5/4 | 0 | 0 | ns |
| $\mathrm{t}_{\mathrm{d} 7}$ | tRPDL - tria |  | 13 | 13 | ns |
| $\mathrm{t}_{\mathrm{d} 8}$ | tRCC - ${ }^{\text {chePDL }}$ |  | 20 | 20 | ns |

## 673103 Test Loads (See Note)



Note: input pulse 0 V to $3.0 \mathrm{~V}, \mathrm{t}_{R}=\mathrm{t}_{\mathrm{F}}=2.5 \mathrm{~ns}, \mathrm{f}=1 \mathrm{MHz}, \mathrm{tpW}=200 \mathrm{~ns}$ Input reference point on $A C$ measurements is 1.5 V .
Output reference points are 2.4 V for HIGH and 0.8 V for LOW.

## Control Outputs

| TEST | S1 | S2 | CL | MEASURED AT |
| :--- | :---: | :---: | :---: | :---: |
| $t_{\text {PD }}$ | Open | Closed | CL | $0.8 \mathrm{~V}, 2.4 \mathrm{~V}$ |
| $t_{P Z H}$ | Open | Closed | CL | 2.4 V |
| $t_{P H Z}$ | Open | Closed | 15 pF | $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ |
| $\mathrm{t}_{\mathrm{PZL}}$ | Open | Open | CL | 0.8 V |
| $t_{P L Z}$ | Open | Open | 15 pF | $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ |

Where $C_{L}=150 \mathrm{pF}$ for $\overline{\mathrm{RAS}}, 300 \mathrm{pF}$ for $\overline{\mathrm{CAS}}$, and 500 pF for $\overline{W E}$.

## Address Driver Output Stage

## Control Driver

Output Stage


## Applications

## Microprocessor Interface

The 673103 Dynamic RAM controller provides the address and control signals required to access and refresh dynamic RAMs. When interfaced to a 16-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions. Two PAL® devices may be used to perform these functions, as shown in Figure 1. One PAL device is used to generate the
refresh clock, while the other performs all arbitration and handshake functions. A hidden refresh (refresh which is transparent to the system) scheme is implemented in the interface PAL device which takes advantage of "free" system time to refresh the memory, and falls back to "forced" refresh when hidden refresh cannot be performed.


Figure 1. A CPU Interfaced to the $\mathbf{6 7 3 1 0 3}$ Driving 8 M Bytes of Dynamic Memory

## Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is tRAC (Data access time from RAS going LOW) or tCAC (Data access time from CAS going LOW), which-
ever results in the later appearance of data at the Dynamic RAM output. Since the $\overline{\text { RAS }}$ and $\overline{\mathrm{CAS}}$ coming out of the controller are initiated by the $\overline{R A S I N}$, the controller-memory performance is measured from the $\overline{\text { RASIN }}$ HIGH-to-LOW transition (see Figure 2).


Figure 2. Access Time from $\overline{\text { RASIN }}$

The time from $\overline{\text { RASIN }}$ to data is calculated to be the longer of:
$t_{\text {RICL }}+t_{C A C}(\overline{R A S I N}$ to $\overline{C A S}+\overline{\mathrm{CAS}}$ to data)
$t_{R P D L}+t_{\text {RAC }}(\overline{R A S I N}$ to $\overline{R A S}+\overline{R A S}$ to data)
Table 1 illustrates the access times from $\overline{\text { RASIN }}$ achieved for various dynamic RAM speeds.

| CONTROLLER/MEMORY | PARAMETER |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | trac | $t_{\text {RPDL }}$ | tcac | tricl | ACCESS TIME FROM $\overline{\text { RASIN }}$ |
| 673103/HM256-12 | 120 | 20 | 60 | 85 | 145 |
| 673103A/HM256-12 | 120 | 20 | 60 | 75 | 140 |
| 673103/HM256-15 | 150 | 20 | 75 | 85 | 170 |
| 673103A/HM256-15 | 150 | 20 | 75 | 75 | 170 |
| 673103/MB8265A-10 | 100 | 20 | 50 | 85 | 135 |
| 673103A/MB8265A-10 | 100 | 20 | 50 | 75 | 125 |
| 673103/MB8265A-12 | 120 | 20 | 60 | 85 | 145 |
| 673103A/MB8265A-12 | 120 | 20 | 60 | 75 | 140 |
| 673103/IMS2620-10 | 100 | 20 | 60 | 85 | 145 |
| 673103A/IMS2620-10 | 100 | 20 | 60 | 75 | 135 |
| 673103/IMS2620-12 | 120 | 20 | 70 | 85 | 155 |
| 673103A/IMS2620-12 | 120 | 20 | 70 | 75 | 145 |

Table 1. Access Times from RASIN for Various Memory Speeds

## 673103 Parameters

trRDL - $\overline{\text { RASIN }}$ LOW to $\overline{\text { RAS }}$ LOW delay
$t_{\text {RICL }}$ - $\overline{\text { RASIN }}$ TO $\overline{\text { CAS }}$ LOW delay

## DRAM Parameters

$t_{\text {RAC }}$ - Access time from $\overline{R A S}$ LOW
${ }^{t}$ CAC - Access time from $\overline{\text { CAS }}$ LOW

## Using the Externally Controlled Access

In the Externally Controlled Access mode RASIN controls the selected $\overline{\text { RAS }}$ output, $\overline{\mathrm{CASIN}} 0-1$ control $\overline{\mathrm{CAS}} 0-1$ outputs respectively and $R / \bar{C}$ controls the address multiplexer. The system designer may create, using the $\overline{\operatorname{RASIN}}, \overline{\mathrm{CASIN}}$ and $\mathrm{R} / \overline{\mathrm{C}}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as

Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.


Figure 3. The 673103 in the Externally-Controlled Access Mode

## Externally Controlled Access (ECA) <br> (Continued)

Example 1: Computing $\overline{\operatorname{RASIN}}$ to R/C Delay
The delay between $\overline{\operatorname{RASIN}}$ going LOW to R/ $\overline{\mathrm{C}}$ going LOW
(tRASINRC) which is required in order to satisfy the dynamic
RAMs' row address hold time (tRAH) is computed as follows:
$t_{\text {RASINRC }}=$ t $_{\text {RAH }}(\mathrm{min})+\mathrm{t}_{\mathrm{d} 7}$
Where:
$t_{\text {RAH }}(\mathrm{min})$ - Row address hold time (dynamic RAM parameter)
$t_{d 7}(\max )=t_{\text {RPDL }}{ }^{-t_{R H A}}$
$t_{\text {RPDL }}-\overline{\text { RASIN }}$ to $\overline{R A S}$ LOW delay
$t_{\text {RHA }}$ - Row address held valid from R/C LOW

## Example 2: Computing R/C to $\overline{\text { CASIN }}$ Delay

The delay between R/C going LOW to going $\overline{\mathrm{CASIN}}$ LOW (tRCCASIN) which is required in order to satisfy the dynamic RAMs' column address setup (tASC) is computed as follows:
$t_{\text {RCCASIN }}=t_{\text {ASC }}(\min )+t_{\mathrm{d} 8}+\mathrm{t}_{\text {PD }}$ F32(max)
Where:
${ }^{\text {t}}$ ASC $($ min $)$ - Column address setup (dynamic RAM parameter) $t_{\mathrm{d} 8}(\max )=\mathrm{t}_{\mathrm{RCC}}-\mathrm{t}_{\mathrm{CPD}}$
$t_{R C C}-R / C$ low to column address valid
${ }^{t}$ CPDL $-\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ LOW delay
${ }^{\text {t PD }}$ F32(max) - Propagation delay of the OR gate used to validate CASIN

Better system performance may be achieved using the $t_{\mathrm{d} 7}, \mathrm{t}_{\mathrm{d} 8}$ switching parameters to calculate tRASINRC and tRCCASIN than when using the tRPDL, tRCDE, tRCC and tRHA parameters (see $t_{d 7}, t_{d 8}$ in Externally Controlled Access switching parameters).


Figure 4. Externally Controlled Access Timing

## Features/Benefits

- Supports up to 1 M DRAMs
- Capable of addressing up to 16 M bytes
- On-chip capacitive-load drivers capable of driving up to 88 DRAMs with 30-nsec typical address propagation delay and 128 DRAMs with $35-n s e c$ typical address propagation delay
- $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ delay of 23 nsec max ( $\overline{\text { RAS }}$ driving 32 DRAMs)
- Max and Min skews are specified to simplify system design
- Four $\overline{\text { CASIN }}$ inputs and four $\overline{\text { CAS }}$ outputs simplify byte addressing
- An Auto-Access mode with extended CAS capability takes advantage of full performance of 120 - and $150-$ nsec DRAMs
- An output series resistor reduces undershoot


## Modes of Operation

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh



## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 673104 | $64 \mathrm{D}, 68 \mathrm{NL}, 68 \mathrm{NP}$ | Com |
| 673104 A |  |  |

## Pin Configurations




## Block Diagram



Figure 1. 673104 Functional Block Diagram

## Description

The 673104 is an LSI device, provided in 64-pin and 68-pin packages, which performs most of the functions needed to control and address Dynamic RAMs. Twenty-two address inputs, ten address outputs, four $\overline{\mathrm{RAS}}$ outputs, and four $\overline{\mathrm{CASIN}}-\overline{\mathrm{CAS}}$ input-output pairs allow the 673104 to directly address 16 M bytes. The four $\overline{C A S I N} n$ inputs and the four $\overline{C A S}$ n outputs simplify individual byte access in 32-bit wide memory arrays (see Figure 2).
The 673104 has three operating modes:

- Externally Controlled Access (ECA)
- Auto Access (AA)
- Refresh (RFSH).

The Externally-Controlled-Access mode gives the system direct control over the $\overline{\mathrm{RAS}}$ m outputs, the $\overline{\mathrm{CAS}}$ n outputs, and Row/Column multiplexing. It also supports PAGE mode access, NIBBLE mode access and static column mode access.
The Auto-Access mode provides on-chip delays that automatically control the timing delays between $\overline{\mathrm{RASm}} \mathrm{m}$ signals, address multiplexing, and CASn signals. In the Auto-Access mode $\overline{\mathrm{CASINO}}-3$ inputs serve as enables for the respective $\overline{\mathrm{CAS}} 0-3$ outputs, allowing the access of any byte of the memory array
(for 32-bit wide memory arrays organized in four bytes). In this mode CAS0-3 outputs go HIGH only when the respective $\overline{\mathrm{CASIN}} 0-3$ inputs go HIGH, and the address switches back to row address only when CASIN0-3 go HIGH. This feature allows extension of the CAS LOW time and column address time while $\overline{\text { RASIN }}$ and $\overline{\text { RASm can go HIGH to satisfy the precharge }}$ requirements of the dynamic RAMs.
When the Refresh mode is selected ( $\overline{\mathrm{RFSH}}$ is LOW) an on-chip refresh counter provides the refresh address; with AUTO HIGH and $R / \bar{C}$ LOW the column address is forced onto the address output multiplexer, facilitating an access of a particular memory location while refreshing a row. This feature may be useful when implementing error detection and correction scrubbing.
The 673104 can drive sixteen banks of DRAMs. $\overline{\text { RASm }}$ control signals are used to select four banks, while leaving the other twelve banks in standby. The four $\overline{\mathrm{CAS}} \mathrm{n}$ outputs enable the selection of one bank out of four. The address lines and the $\overline{W E}$ signal can be connected to all sixteen banks. In a 32-bit wide, byte-oriented, memory array the $\overline{\mathrm{RAS}} \mathrm{m}$ signals select one out of four banks while the $\overline{\mathrm{CAS}} \mathrm{n}$ signals select the bytes, as shown in Figure 2.


Each $\overline{\text { RAS }}$ output drives 32 DRAMs Each $\overline{\text { CAS }}$ output drives 32 DRAMs Each Q0-9 output drives 128 DRAMs $\overline{\text { WE }}$ output drives 128 DRAMs

Figure 2. 673104 Addressing Four Banks of 32-bit Memory Array Organized in Four Bytes

## Pin Definitions

VCC, GND: VCC-GND = $\mathbf{5} \mathbf{V} \pm \mathbf{1 0 \%}$. The supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. A low inductance connection between the ground pin and a solid ground plane will minimize fluctuations in the ground level of the device that may occur when the address outputs switch from HIGH to LOW simultaneously. A $1-\mu \mathrm{F}$ multilayer ceramic capacitor in parallel with a low voltage tantalum capacitor, both connected close to the VCC and GND pins, will properly decouple the device.

## R0-R9: Row Address Inputs

## C0-C9: Column Address Inputs

B0-B1: Bank-Pair Select Inputs - Strobed by ADS. Decoded to enable one of the $\overline{\text { RAS }}$ outputs when $\overline{\text { RASIN }}$ goes LOW in the access modes.
Q0-Q9: Multiplexed Address Outputs - Selected from the row address input latch, the column address input latch, or the refresh counter.
RASIN: Row Address Strobe Input - Drives the selected $\overline{\text { RASm }}$ output in the access modes and all $\overline{\mathrm{RAS}}$ outputs in the Refresh mode.

ADS: Address (Latch) Strobe Input - Strobes input row address, column address, and Bank Select inputs into the respective latches when HIGH; latches on HIGH-to-LOW transition.
$\overline{\mathrm{OE}}$ : Output Enable - When $\overline{\mathrm{OE}}$ is LOW the address and control outputs are enabled. When $\overline{\mathrm{OE}}$ is HIGH the address outputs are in high-impedance and the control outputs are pulled HIGH.
R/C: Row/Column Select Input - In the Externally-ControlledAccess, it is used to select either the row address input latch or
the column address input latch onto the address outputs. In the Refresh mode, when AUTO is HIGH, it is used to select between the refresh address (R/ $\overline{\mathrm{C}} \mathrm{HIGH}$ ) and the column address (R/C LOW). When $\overline{A U T O}$ is LOW R/C is disabled.
CASINO-3: Column Address Strobe Inputs - In the Externally-Controlled-Access mode the $\overline{\text { CASIN }} n$ directly drives $\overline{\text { CASn }}$ output. In the Auto-Access mode, it is used to enable the corresponding $\overline{\mathrm{CAS}}$ output (See $\overline{\mathrm{CASO}} 0-3$ description).

## $\overline{\text { WEIN: }}$ Write Enable Input.

## WE: Write Enable Output.

CAS0-3: Column Address Strobe Outputs - In the Externally-Controlled-Access mode the $\overline{\text { CAS }}$ outputs follow the $\overline{\text { CASIN }}$ inputs. In the Auto-Access mode the CASIN inputs are used to enable the $\overline{\mathrm{CAS}}$ outputs, but the $\overline{\mathrm{CAS}}$ outputs are asserted LOW, with proper delay from the $\overline{\mathrm{RAS}}$ output, by the $\overline{\mathrm{RASIN}}$ signal via the Auto-Access timing generator. In the Auto-Access mode, the $\overline{\mathrm{CAS}} \mathrm{n}$ goes HIGH only when the corresponding $\overline{\text { CASIN }}$ n goes HIGH. Extending the CASn LOW duration while RASIN and $\overline{\text { RASm }}$ go HIGH satisfies the precharge requirement of the dynamic RAMs.
(RAS0-3: Row Address Strobe Outputs - When $\overline{\text { RFSH }}$ is HIGH the selected row address strobe output (decoded from signals
 outputs go LOW together following $\overline{\text { RASIN }}$ going LOW.
$\overline{\text { AUTO: Auto-Access Input - When } \overline{A U T O} \text { is LOW the Auto- }}$ Access mode is selected (see Auto-Access mode description).
$\overline{\text { RFSH: Refresh Input - When } \overline{\text { RFSH }} \text { is LOW the Refresh mode }}$ is selected (see Refresh mode description).

## Externally-Controlled-Access Mode (ECA)

In this mode, selected when $\overline{\text { AUTO }}$ and $\overline{\text { RFSH }}$ are held HIGH, the 673104 serves as a straightforward multiplexer and driver for the address and control signals to the DRAMs. The $\overline{\text { RASm output }}$ selected by the $B 0$ and B1 inputs follows the RASIN input, and each of the $\overline{\text { CAS }}$ outputs follows its corresponding $\overline{\text { CASIN }}$ input. When $\mathrm{R} / \overline{\mathrm{C}}$ is HIGH the row address is enabled onto the $\mathrm{Q} 0-9$ outputs. When R/C is LOW the column address latch is enabled onto Q0-9 outputs.
The $\overline{\text { RASIN }}-\overline{\text { RAS }}, \overline{\text { CASIN }}-\overline{\text { CAS }}$, and R/ $\overline{\mathrm{C}}-$ Q0-9 control paths are independent to allow the system designer maximum flexibility and support of special DRAM access and refresh modes such as NIBBLE mode, PAGE mode, $\overline{\mathrm{CAS}}$ before $\overline{\mathrm{RAS}}$, etc.

To allow tighter timing of the sequence of control signals to the Dynamic RAM, several difference timing parameters have been specified for the Externally Controlled Access mode. These
parameters specify the maximum difference between the various "control channels" of the device. In particular, using switching characteristics $t_{d 7}$ and $t_{d 8}$ is very useful when designing the
 going LOW to $\overline{\text { CASIN }}$ going LOW (see Applications).

| BANK SELECT (STROBED BY ADS) |  | ENABLED $\overline{\text { RASn }}$ |
| :---: | :---: | :---: |
| B1 | B0 |  |
| 0 | 0 | $\overline{\text { RAS } 0}$ |
| 0 | 1 | $\overline{\text { RAS } 1}$ |
| 1 | 0 | $\overline{\text { RAS } 2}$ |
| 1 | 1 | $\overline{\text { RAS } 3}$ |

Table 1. Memory Bank Decode


Figure 3. Externally-Controlled-Access- $\overline{\mathbf{R A S I N}}-\mathrm{to}-\overline{\mathrm{RAS}}$ Timing


Figure 4. Externally-Controlled-Access- $\overline{\operatorname{CASIN}}$ to $\overline{\mathrm{CAS}}$ Timing


Figure 5. Externally-Controlled-Access R/C Timing

## Auto-Access Mode (AA)

In the Auto-Access mode the 673104 provides the system designer with built-in delays and sequencing to accommodate $\overline{\text { DRAMs }}$ with 150 nanoseconds and faster access time. The Auto-Access mode is selected when $\overline{\text { AUTO }}$ is held LOW and RFSH is held HIGH. The R/C input is disabled, and $\overline{\text { RASIN going }}$ LOW initiates the sequence of control signals to access the DRAMs. The CASINO-3 inputs are used as enables for the respective $\overline{\mathrm{CAS}}$ outputs. A LOW on a $\overline{\mathrm{CASIN}}$ n input enables the
$\overline{\mathrm{CAS}}$ n output to be driven LOW with the internally generated delay from $\overline{\text { RAS }}$. Each $\overline{\text { CASn output goes HIGH only when the }}$ corresponding $\overline{\text { CASINn }}$ input goes HIGH, and the address switches back to row address only when all $\overline{\text { CASIN }}$ go HIGH. This feature allows extension of the $\overline{C A S}$ LOW time and the column address time, while $\overline{\mathrm{RASIN}}$ and $\overline{\text { RAS }} \mathrm{m}$ can go HIGH to satisfy precharge requirements of the dynamic $\overline{\mathrm{RAMs}}$. The R/C input is disabled in this mode.


Figure 6. Auto-Access (AA) Timing

## Refresh Mode (RFSH)

When $\overline{\text { RFSH }}$ is held LOW the refresh counter contents are enabled onto the QO-9 address outputs, provided either $\mathrm{R} / \overline{\mathrm{C}}$ is held HIGH, or $\overline{\text { UUTO }}$ is held LOW, or both conditions exist. In this mode all four $\overline{\mathrm{RAS}}$ outputs follow the $\overline{\mathrm{RASIN}}$ input signal. The refresh counter increments the refresh address when either $\overline{\text { RASIN }}$ or $\overline{\text { RFSH }}$ goes HIGH while the other is LOW. When $\overline{\text { AUTO }}$ is LOW the CASINO-3 inputs are isolated and CAS0-3 are held HIGH. Also, when $\overline{A U T O}$ is LOW the R/C input is isolated from the output multiplexer, and the refresh address appears at the Q0-9 outputs.
When $\overline{A U T O}$ is HIGH , pulling R/ $\overline{\mathrm{C}}$ LOW enables the column address onto the QO-9 outputs. Also, each of the $\overline{\mathrm{CAS}}$ outputs follows its respective $\overline{\text { CASIN }}$ input. This feature may be used
when implementing error correction and detection "scrubbing" for four-bank memory arrays. "Scrubbing" is a term describing a cyclic error correction of soft errors in the memory array, done within the refresh cycles. On every refresh cycle one location of the memory array is accessed and the data in that location goes, if necessary, through a correction cycle (a read-modify-write memory cycle). The 673104 provides the facilities to force a column address onto the Q0-9 address outputs and to assert the $\overline{\mathrm{CAS}} 0-3$ outputs within a refresh cycle to allow scrubbing. A column counter and a bank counter need to be added externally to provide the column addresses for scrubbing.
The refresh counter is a 10-bit counter that resets to 0 on powerup and rolls-over to 0 at 1023.


Figure 7. Refresh Timing

[^46]
## 673104 <br> $673104 A$



Figure 8. Address Setup and Hold Time to ADS


Figure 9. Address Input/Ouiput Propagation Delay
Note: Row or Column address $(\overline{\text { RFSH }}=\mathrm{HIGH})$.


Figure 10. High-Z Timing

## Absolute Maximum Ratings (See Note)

Supply voltage, $\mathrm{V}_{\mathrm{CC}}$. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to 7 V
$\qquad$
Input voltage . ......................................................................................................... -1.5 V to 5.5 V
Output current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 150 mA
Lead temperature (soldering, 10 seconds) . ............................................................................................. $300^{\circ} \mathrm{C}$
Note: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

## Operating Conditions

| SYMBOL | PARAMETER | FIGURE/ NUMBER | $\begin{aligned} & \text { 673104A } \\ & \text { MIN TYP MAX } \end{aligned}$ |  | $\begin{gathered} 673104 \\ \text { MIN TYP MAX } \end{gathered}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{C C}$ | Supply voltage |  | 4.5 | 5.5 | 4.5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Ambient temperature |  | 0 | 75 | 0 | 75 | C |
| ${ }^{\text {t }}$ ASA | Address setup time to ADS LOW | 8/1 | 18 |  | 18 |  | ns |
| tADS | Address strobe pulse width HIGH |  | 26 |  | 26 |  | ns |
| tAHA | Address hold time from ADS LOW | 8/2 | 10 |  | 10 |  | ns |
|  | EXTERNALLY CONTROLLED ACCESS PARAMETER |  |  |  |  |  |  |
| tadHAR | ADS LOW hold from $\overline{\text { RASIN }}$ HIGH | 3/7 | 0 |  | 0 |  | ns |
| tBSR | Bank select setup to $\overline{\text { RASIN }}$ LOW (ADS = HIGH) | 3/8 | 10 |  | 10 |  | ns |
| tBSH | Bank select hold from $\overline{\text { RASIN }}$ HIGH (ADS = HIGH) | 3/9 | 10 |  | 10 |  | ns |
| tSSR | Address strobe HIGH setup to $\overline{\text { RASIN }}$ LOW (B0, B1 STABLE) | 3/10 | 20 |  | 20 |  | ns |
| taUHE | $\overline{\text { AUTO }}$ hold from RASIN HIGH | 3/4 | 55 |  | 55 |  | ns |
| taUSRC | $\overline{\text { AUTO }}$ HIGH setup to R/C C LOW | 5/1 | 25 |  | 25 |  | ns |
| taUHRC | $\overline{\text { AUTO }}$ HIGH hold from R/C̄ HIGH | 5/2 | 10 |  | 10 |  | ns |
| taUSCA | $\overline{\text { AUTO }}$ HIGH setup to CASIN LOW | 4/1 | 45 |  | 45 |  | ns |
| taUHCA | $\overline{\text { AUTO }}$ HIGH hold from CASIN HIGH | $4 / 2$ | 0 |  | 0 |  | ns |
| $t \mathrm{t}$ U | $\overline{\text { AUTO }}$ setup to $\overline{\text { RASIN }}$ LOW | $3 / 3$ | 0 |  | 0 |  | ns |
| tRFSR | $\overline{\text { RFSH }}$ HIGH setup to $\overline{\text { RASIN }}$ LOW (to guarantee tASR $^{\text {a }}$ () | 3/1 | 10 |  | 10 |  | ns |
| tRFHR | $\overline{\text { RFSH }}$ HIGH hold from $\overline{\text { RASIN }}$ HIGH | 3/2 | 10 |  | 10 |  | ns |
|  | AUTOMATIC ACCESS PARAMETER |  |  |  |  |  |  |
| tadHAR | ADS LOW hold from RASIN HIGH | 3/7 | 0 |  | 0 |  | ns |
| tBSR | Bank select setup to $\overline{\text { RASIN }}$ LOW (ADS = HIGH) | 6/12 | 10 |  | 10 |  | ns |
| tBSH | Bank select hold from $\overline{\text { RASIN }}$ HIGH (ADS $=$ HIGH) | 3/9 | 10 |  | 10 |  | ns |
| tASRL | Address setup to $\overline{\text { RASIN }}$ LOW (ADS $=$ HIGH) <br> ( $\mathrm{t}_{\mathrm{ASRL}}=\mathrm{t}_{\mathrm{d} 2}$ max to guarantee $\mathrm{t}_{\mathrm{ASR}}=0$ ) | 6/4 | 34 |  | 34 |  | ns |
| $t_{\text {t }}$ | $\overline{\text { AUTO }}$ setup to $\overline{\text { RASIN }}$ LOW | 6/5 | 0 |  | 0 |  | ns |
| tRFSR | $\overline{\text { RFSH }}$ HIGH setup to $\overline{\text { RASIN }}$ LOW (to guarantee tASR $=0$ ) | 6/6 | 10 |  | 10 |  | ns |
| tSSR | Address strobe HIGH to $\overline{\text { RASIN }}$ LOW (B0, B1 STABLE) | 6/7 | 20 |  | 20 |  | ns |
| ${ }^{\text {t CASR }}$ | $\overline{\text { CASIN0-1 setup to } \overline{\text { RASIN }} \text { LOW }}$ | 6/8 | -30 |  | -30 |  | ns |
| $t \mathrm{t}$ UH | $\overline{\text { AUTO }}$ hold from RASIN HIGH | 6/9 | 50 |  | 50 |  | ns |
| ${ }^{\text {t }} \mathrm{AUCH}$ | $\overline{\text { AUTO }}$ LOW hold from CASIN HIGH | 6/10 | 0 |  | 0 |  | ns |
|  | REFRESH PARAMETER |  |  |  |  |  |  |
| taUHRF | $\overline{\text { AUTO }}$ LOW hold from $\overline{\text { RFSH }}$ HIGH (R/C LOW$)$ | 7/1 | 10 |  | 10 |  | ns |
| tRCSRF | R/C̄ HIGH setup to $\overline{\text { RFSH }}$ LOW ( $\overline{\text { AUTO }}$ HIGH) | 7/2 | 20 |  | 20 |  | ns |
| taUSRF | $\overline{\overline{A U T O}}$ LOW setup to $\overline{\text { RFSH }}$ LOW (R/C̄ LOW) | 7/3 | 20 |  | 20 |  | ns |
| trCHRF | R/ट्ट HIGH hold from $\overline{\text { RFSH }}$ HIGH ( $\overline{\text { AUTO }}$ HIGH) | 7/4 | 10 |  | 10 |  | ns |
| traj | $\overline{\text { RASIN HIGH during refresh }}$ | 7/10 | 30 |  | 30 |  | ns |
| tRFQS | $\overline{\mathrm{RFSH}}$ LOW setup to $\overline{\text { RASIN }}$ LOW (to guarantee tris) | 7/14 | 34 |  | 34 |  | ns |

Electrical Characteristics $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V} \pm 10 \%, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 75^{\circ} \mathrm{C}$. Typicals are for $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5 ^ { \circ }} \mathbf{C}$

| SYMBOL | PARAMETER | CONDITIONS | FIGURE/ NUMBER | MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| VIC | Input clamp voltage | $\mathrm{I}_{\mathrm{N}}=-18 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | -0.8-1.2 | V |
| IIH | Input high current | $\mathrm{V}_{\text {IN }}=2.7 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | 50 | $\mu \mathrm{A}$ |
| ICTL | Output load current for $\overline{\mathrm{RAS}}, \overline{\mathrm{CAS}}, \overline{\mathrm{WE}}$ | $\mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ <br> Chip deselect |  | -1.5-2.5 | mA |
| IIL | Input low current except for $\overline{\text { RFSH }}$ | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -20-250 | $\mu \mathrm{A}$ |
| IILRF | Input low current for RFSH | $\mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -80-500 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\text {IL }}$ | Input low threshold (Note 1) |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | Input high threshold (Note 1) |  |  | 2.0 | V |
| $\mathrm{V}_{\mathrm{OL} 1}$ | Output low voltage | IOUT $=1 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 0.5 | V |
| VOL2 | Output low voltage | IOUT $=12 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 0.8 | V |
| VOH | Output high voltage | IOUT $=-1 \mathrm{~mA}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | 2.430 | V |
| IOH | Output source current (Note 2) | $\mathrm{V}_{\text {OUT }}=0.8 \mathrm{~V}, \mathrm{~V}_{\text {CC }}=\mathrm{MIN}$ |  | $\begin{array}{lll}-50 & -140\end{array}$ | mA |
| IOL | Output sink current (Note 2) | $\mathrm{V}_{\text {OUT }}=2.4 \mathrm{~V}, \mathrm{~V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | $40 \quad 100$ | mA |
| loz | Three-state output current (address output) | $\begin{aligned} & 0.4 \mathrm{~V} \leq \mathrm{V}_{O U T} \leq 2.7 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CC}}=\text { MAX, Chip deselect } \end{aligned}$ | ; | -50 50 | $\mu \mathrm{A}$ |
| ICC | Supply current | $V_{C C}=$ MAX |  | $190 \quad 280$ | mA |
| CIN | Input capacitance | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 10 | pF |

## Switching Characteristics (See Note 3)

| SYMBOL | EXTERNALLY CONTROLLED ACCESS PARAMETER | FIGURE/ NUMBER | $\begin{gathered} \text { 673104A } \\ \text { MIN TYP MAX } \end{gathered}$ | $\begin{gathered} 673104 \\ \text { MIN TYP MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| trHA | Row addresses remaining valid from R/C LOW | 5/3 | 0 | 0 | ns |
| tRPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay | 3/11 | 23 | 23 | ns |
| trPDH | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay | 3/12 | 33 | 33 | ns |
| tAPD | Address input to output delay | 9/2 | 60 | 60 | ns |
| tWPDL | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ LOW delay |  | 50 | 50 | ns |
| tWPDH | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ HIGH delay | r | 45 | 45 | ns |
| tCPDL | $\overline{\text { CASIN }}$ to CAS LOW delay | 4/3 | 28 | 28 | ns |
| ${ }^{\text {t CPPDH }}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay | 4/4 | 40 | 40 | ns |
| trce | Column select to column address valid | 5/5 | 50 | 50 | ns |
| treR | Row select to row address valid | 5/6 | 53 | 53 | ns |
| $\mathrm{t}_{\mathrm{d} 1}$ | ( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -5 | -5 10 | ns |
| $\mathrm{t}_{\mathrm{d} 2}$ | (Address input to output delay)-( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay) |  | 34 | 34 | ns |
| $t_{\text {d }} 3$ | (Address input to output delay)-( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay) |  | $0 \quad 28$ | 0 28 | ns |
| $\mathrm{t}_{\mathrm{d} 4}$ | Skew between address output lines |  | 12 | 12 | ns |
| $t_{\text {d } 5}$ | ( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}} \mathrm{HIGH}$ delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -10 10 | $\begin{array}{ll}-10 & 10\end{array}$ | ns |
| $t_{\text {d } 6}$ | ( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay)-( $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ HIGH delay) |  | -12 12 | -12 12 | ns |
| tSPD | ADS HIGH to address output valid | 9/1 | 64 | 64 | ns |
| trehe | Column addresses remaining valid from R/C CIGH | 5/4 | 0 | 0 | ns |
| $\mathrm{t}_{\mathrm{d} 7}$ | tRPDL - trHA |  | 16 | 16 | ns |
| td8 | trce - ${ }^{\text {ctePDL }}$ |  | 27 | 27 | ns |

## Switching Characteristics (Continued)

| SYMBOL | AUTO ACCESS PARAMETER | FIGURE/ NUMBER | $\begin{gathered} \text { 673104A } \\ \text { MIN TYP MAX } \end{gathered}$ | $\begin{gathered} 673104 \\ \text { MIN TYP MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| tricl | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ LOW delay | 6/20 | 83 | 90 | ns |
| trCDL | $\overline{\mathrm{RAS}}$ to $\overline{\mathrm{CAS}}$ LOW delay | 6/23 | $30 \quad 73$ | $30 \quad 80$ | ns |
| trPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ LOW delay | 6/13 | 23 | 23 | ns |
| trPDH | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay | 6/14 | 33 | 33 | ns |
| ${ }^{\text {taPD }}$ | Address input to output delay | 6/16 | 60 | 60 | ns |
| tWPDL | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ LOW delay |  | 50 | 50 | ns |
| tWPDH | $\overline{\text { WEIN }}$ to $\overline{\text { WE }}$ HIGH delay |  | 45 | 45 | ns |
| ${ }^{\text {t }}$ CPDH | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ HIGH delay | 6/22 | 40 | 40 | ns |
| traH | Row address hold time from $\overline{\text { RAS }}$ LOW | 6/17 | 15 | 15 | ns |
| $\mathrm{t}_{\mathrm{d} 2}$ | (Address input to output delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | 34 | 34 | ns |
| tSPD | ADS HIGH to address output valid | 6/19 | 64 | 64 | ns |
| ${ }^{\text {taSC }}$ | Column address setup to $\overline{\mathrm{CAS}}$ LOW | 6/21 | 0 | 0 | ns |
| t'CAHC | Column address remaining valid from $\overline{\text { CASINO}} 3$ - 3 HIGH | 6/18 | 5 | 5 | ns |
| ${ }^{\text {t ASR }}$ | Row address valid before $\overline{\mathrm{RAS}}$ LOW | 6/24 | 0 | 0 | ns |
| $t_{d 5}$ | ( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay)-( $\overline{\text { RASIN }}$ to $\overline{\mathrm{RAS}}$ LOW delay) | $\cdots$ | -10 10 | $\begin{array}{ll}-10 & 10\end{array}$ | ns |
|  | REFRESH PARAMETER |  |  |  |  |
| trFLCT | $\overline{\mathrm{RFSH}}$ LOW to refresh address valid ( $\overline{\text { UUTO LOW }}$ or R/C HIGH) | 7/5 | 50 | 50 | ns |
| tRFPDL | $\overline{\mathrm{RASIN}}$ LOW to $\overline{\mathrm{RAS}}$ LOW delay during refresh | 7/11 | 26 | 26 | ns |
| trFPDH | $\overline{\text { RASIN }}$ HIGH to $\overline{\mathrm{RAS}}$ HIGH delay during refresh | 7/12 | 38 | 38 | ns |
| trFAH | Refresh address held from $\overline{\text { RASIN }}$ HIGH ( $\overline{\text { RFSH }}$ LOW) | 7/7 | 0 | 0 | ns |
| trinc | $\overline{\text { RASIN }}$ HIGH to new refresh address valid | 7/9 | 72 | 72 | ns |
| trfaHR | Refresh address held from $\overline{\text { RFSH }}$ HIGH | 7/6 | 0 | 0 | ns |
| tris | Refresh address valid to $\overline{\text { RAS }}$ LOW (provided tRFQS is satisfied) | 7/13 | 0 | 0 | ns |
| trFRDH | $\overline{\text { RFSH }}$ HIGH to $\overline{\text { RAS }}$ HIGH (for three banks, $\overline{\text { RASIN }}=$ LOW) | 7/15 | 45 | 45 | ns |
| $t_{d} 9$ | ( $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ HIGH delay)-( $\overline{\mathrm{RASIN}}$ to $\overline{\mathrm{RAS}}$ LOW delay) |  | -9 16 | -9 16 | ns |
|  | THREE-STATE PARAMETER |  |  |  |  |
| ${ }^{\text {t }}$ AZL | $\overline{\text { OE LOW }}$ to address output LOW | 10/1 | 50 | 50 | ns |
| ${ }^{\text {t }}$ AZH | $\overline{\text { OE LOW }}$ to address output HIGH | 10/2 | 60 | 60 | ns |
| ${ }^{\text {t } A L Z ~}$ | $\overline{\mathrm{OE}}$ HIGH to address output HI-Z from LOW | 10/3 | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{AHZ}$ | $\overline{\text { OE }} \mathrm{HIGH}$ to address output HI-Z from HIGH | 10/4 | 25 | 25 | ns |
| ${ }^{\text {t CTIZL }}$ | $\overline{\text { OE LOW }}$ to control output LOW | 10/5 | 50 | 50 | ns |
| tCTZH | $\overline{\text { OE LOW }}$ to control output HIGH | 10/6 | 50 | 50 | ns |
| tcTLZ | $\overline{\text { OE HIGH to control output HI-Z from LOW }}$ | 10/7 | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{CTHZ}$ | $\overline{\mathrm{OE}}$ HIGH to control output HI-Z from HIGH | 10/8 | 30 | 30 | ns |

Note 1: These are absolute voltage levels with respect to the ground pins on the device and includes all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
Note 2: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. One output should be tested at a time and test duration should not exceed one second.
Note 3: Output load capacitance is typical for four banks of 32 DRAMs with trace capacitance.
The values are: $Q 0-8 C_{L}=800 \mathrm{pF}, \overline{\operatorname{RAS} 0}-3 \mathrm{C}_{\mathrm{L}}=250 \mathrm{pF}, \overline{\mathrm{WE}} \mathrm{C}_{\mathrm{L}}=800 \mathrm{pF}, \overline{\mathrm{CAS} 0-3 C_{L}}=300 \mathrm{pF}$.

## 673104 Test Loads (See Note)



Change in Propagation Delays vs. Change in Loading Capacitance Relative to the Specified Load

Address Outputs

| TEST | s1 | s2 | CL | MEASURED AT |
| :--- | :---: | :---: | :---: | :---: |
| ${ }^{\text {t}} \mathrm{PD}$ | Open | Closed | 800 pF | $0.8 \mathrm{~V}, 2.4 \mathrm{~V}$ |
| ${ }^{t_{\mathrm{PZH}}}$ | Closed | Closed | 800 pF | 2.4 V |
| $\mathrm{t}_{\mathrm{PHZ}}$ | Open | Closed | 15 pF | $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ |
| $\mathrm{t}_{\mathrm{PZL}}$ | Closed | Closed | 800 pF | 0.8 V |
| $\mathrm{t}_{\mathrm{PLZ}}$ | Closed | Open | 15 pF | $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ |

## Control Outputs

| TEST | S1 | S2 | CL | MEASURED AT |
| :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t }}$ PD | Open | Closed | CL | $0.8 \mathrm{~V}, 2.4 \mathrm{~V}$ |
| ${ }^{\text {P P }}$ PH | Open | Closed | CL | 2.4 V |
| ${ }^{\text {t }} \mathrm{PHZ}$ | Open | Closed | 15 pF | $\mathrm{V}_{\mathrm{OH}}-0.5 \mathrm{~V}$ |
| ${ }^{\text {t }}$ PZL | Open | Open | CL | 0.8 V |
| ${ }^{\text {PPLZ }}$ | Open | Open | 15 pF | $\mathrm{V}_{\mathrm{OL}}+0.5 \mathrm{~V}$ |

Where $\mathrm{C}_{\mathrm{L}}=250 \mathrm{pF}$ for $\overline{\mathrm{RAS}}, 300 \mathrm{pF}$ for $\overline{\mathrm{CAS}}$, and 800 pF for $\overline{\mathrm{WE}}$.


## Control Driver Output Stage



## Applications

## Microprocessor Interface

The 673104 Dynamic RAM Controller provides the address and control signals required to access and refresh dynamic RAMs When interfaced to a 32-bit microprocessor, some external logic is required to generate a refresh clock as well as to perform access/refresh arbitration and interface handshake functions For some microprocessors external logic is required also to
decode the address and control signal to arrive at four data strobes. A hidden refresh (refresh which is transparent to the system) scheme may be implemented in the interface circuitry taking advantage of "free" system time to refresh the memory, and falling back to "forced" refresh when hidden refresh cannot be performed.


Figure 1. A CPU Interfaced to the 673104 Driving 16 M Bytes of Dynamic Memory

## Determining System Performance (Auto-Access)

When determining system performance the dynamic RAM parameters must be considered as well as the controller's propagation delays. For both read and write cycles the access time for the dynamic RAM is tRAC ( $\overline{R A S}$ access time) from $\overline{R A S}$
going LOW or tCAC ( $\overline{\text { CAS }}$ access time) from $\overline{\text { CAS }}$ going LOW. Since the $\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ coming out of the controller are initiated by the $\overline{R A S I N}$, the controller-memory performance is measured from the RASIN HIGH-to-LOW transition (see Figure 2).


Figure 2. Access Time from $\overline{\text { RASIN }}$

The time from $\overline{\text { RASIN }}$ to data is calculated to be the longer of:
${ }^{t_{R I C L}}{ }^{+}{ }^{\text {t }}$ CAC $(\overline{\text { RASIN }}$ to $\overline{\text { CAS }}+\overline{\text { CAS }}$ to data)
${ }^{t_{R P D L}}+{ }^{\text {t }}$ RAC $(\overline{R A S I N}$ to $\overline{\text { RAS }}+\overline{\text { RAS }}$ to data)
Table 1 illustrates the access times from $\overline{\text { RASIN }}$ achieved for various dynamic RAM speeds.

| CONTROLLER/MEMORY | PARAMETER |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | traC | tRPDL | tcAC | ${ }^{\text {tRICL }}$ | ACCESS TIME FROM $\overline{\text { RASIN }}$ |
| 673104/HM256-12 | 120 | 23 | 60 | 90 | 150 |
| 673104A/HM256-12 | 120 | 23 | 60 | 83 | 143 |
| 673104/HM256-15 | 150 | 23 | 75 | 90 | 173 |
| 673104A/HM256-15 | 150 | 23 | 75 | 83 | 173 |
| 673104/MB8265A-10 | 100 | 23 | 50 | 90 | 140 |
| 673104A/MB8265A-10 | 100 | 23 | 50 | 83 | 133 |
| 673104/MB8265A-12 | 120 | 23 | 60 | 90 | 150 |
| 673104A/MB8265A-12 | 120 | 23 | 60 | 83 | 143 |
| 673104/IMS2620-10 | 100 | 23 | 60 | 90 | 150 |
| 673104A/IMS2620-10 | 100 | 23 | 60 | 83 | 143 |
| 673104/IMS2620-12 | 120 | 23 | 70 | 90 | 160 |
| 673104A/IMS2620-12 | 120 | 23 | 70 | 83 | 153 |

Table 1. Access Times from $\overline{\text { RASIN }}$ for Various Memory Speeds

## 673104 Parameters

$t_{\text {RICL }}$ - $\overline{\text { RASIN }}$ LOW to $\overline{\text { CAS }}$ LOW delay
$t_{\text {RPDL }}-\overline{\text { RASIN }}$ LOW to $\overline{R A S}$ LOW delay

## DRAM Parameters

$t_{\text {RAC }}$ - Access time from $\overline{R A S}$ LOW
${ }^{t}$ CAC - Access time from $\overline{\text { CAS }}$ LOW

## Using the Externally Controlled Access

In the Externally Controlled Access mode $\overline{\text { RASIN }}$ controls the selected $\overline{\mathrm{RAS}}$ output, $\overline{\mathrm{CASIN}} 0-3$ control $\overline{\mathrm{CAS}} 0-3$ outputs respectively and $R / \bar{C}$ controls the address multiplexer. The system designer may create, using the $\overline{\operatorname{RASIN}}, \overline{\mathrm{CASIN}}$ and $\mathrm{R} / \overline{\mathrm{C}}$ inputs, the required control signal sequence for the specific system being designed. Special dynamic RAM access modes such as

Nibble mode and Page mode access cycles may be performed simply by toggling the appropriate control inputs. Special skew timing specifications have been specified to allow tighter timing control as outlined in the following examples. Both following examples relate to the scheme depicted in Figure 3.


Figure 3. The 673104 in the Externally-Controlled Access Mode

## Externally Controlled Access (ECA) (Continued)

## Example 1: Computing $\overline{\text { RASIN }}$ to R/C Delay

The delay between $\overline{\text { RASIN }}$ going LOW to R/C going LOW (tRASINRC) which is required in order to satisfy the dynamic RAMs' row address hold time (tRAH) is computed as follows:
$t_{\text {RASINRC }}=t_{\text {RAH }}(\mathrm{min})+t_{d 7}$
Where:
$t_{\text {RAH }}(\mathrm{min})$ - Row address hold time (dynamic RAM parameter)
$t_{d 7}(\max )=t_{\text {RPDL }}{ }^{-t_{R H A}}$
$t_{\text {RPDL }}-\overline{R A S I N}$ to $\overline{R A S}$ LOW delay
trHA - Row address held valid from R/C LOW

## Example 2: Computing R/C to CASIN Delay

The delay between R/C going LOW and $\overline{C A S I N}$ going LOW ( $\mathrm{t}_{\mathrm{RCC}}$ CASIN) which is required in order to satisfy the dynamic RAMs' column address setup ( $\mathrm{t}_{\mathrm{ASC}}$ ) is computed as follows:
$\mathrm{t}_{\mathrm{RCC}} \mathrm{ASIN}=\mathrm{t}_{\mathrm{ASC}}(\mathrm{min})+\mathrm{t}_{\mathrm{d} 8}+\mathrm{t}_{\mathrm{PD}} \mathrm{F} 32$ (max)
Where:
$t_{\text {ASC }}$ (min) - Column address setup (dynamic RAM parameter)
$\mathrm{t}_{\mathrm{d} 8}(\max )=\mathrm{t}_{\mathrm{RCC}}{ }^{-\mathrm{t}} \mathrm{CPDL}$
$t_{R C C}-R / \bar{C}$ low to column address valid
${ }^{\mathrm{t}} \mathrm{CPDL}$ - $\overline{\mathrm{CASIN}}$ to $\overline{\mathrm{CAS}}$ LOW delay
$t_{\text {PD }}$ F32(max) - Propagation delay of the OR gate used to validate $\overline{\text { CASIN }}$
Better system performance may be achieved using the $t_{d} 7, t_{d 8}$ switching parameters to calculate tRASINRC and tRCCASIN than when using the tRPDL, tRCDL, tRCC and tRHA parameters (see Externally Controlled Access switching parameters).


Figure 4. Externally Controlled Access Timing

## 64K Dynamic RAM Controller/Driver

## Features/Benefits

- All DRAM drive functions on one chip have on-chip high-capacitance-load drivers (specified up to 88 DRAMs)
- Drives directly all 16K and 64K DRAMs: Capable of addressing up to 256K words
- Propagation delays of 25 nsec typical at 500-pF load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Six operating modes support externally-controlled access and refresh, automatic access, as well as special memory initialization access
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- Direct replacement for National DP8408, DP8408A

| MODE | MODE OF OPERATION |
| :---: | :--- |
| $0,1,2$ | Externally-controlled refresh |
| 3 | Externally-controlled All- $\overline{R A S}$ write |
| 4 | Externally-controlled access |
| 5 | Auto access, slow tRAH |
| 6 | Auto access, fast tRAH |
| 7 | Set end of count |


$74 S 408$ interface Between System and DRAM Banks

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN74S408 | 48 N, D | Com |
| SN74S408-2 | 48 N, D | Com, Speed Option |

## Pin Configuration



NC = NO CONNECTION

9-64

## Block Diagram



Figure 1. 74S408 Functional Block Diagram

## Description

The 74S408 is a Multi-Mode Dynamic RAM Controller/Driver capable of driving directly up to 88 DRAMs. 18 address lines allow the 74 S 408 to drive all 16 K and 64 K DRAMs and addresses up to 256 K words. Since the 74 S 408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.

The 74S408's 6 operating modes offer externally-controlled or on-chip automatic access and externally-controlled refresh. An on-chip refresh counter makes refreshing less complicated; and automatic memory initialization is both simple and fast.

The 74S408 is a 48 -pin DRAM Controller/Driver with 8 multiplexed address outputs and 6 control signals. It consists of two 8 -bit address latches, an 8 -bit refresh counter,
and control logic. All address output drivers are capable of driving 500pf loads with propagation delays of 25 nsec . The 74S408 timing parameters are specified driving the typical load capitance of 88 DRAMs, including trace capitance.

The 745408 can drive up to 4 banks of DRAMs, with each bank comprised of 16 Ks , or 64 Ks . Control signal outputs $\overline{\text { RAS }}, \overline{\mathrm{CAS}}$, and $\overline{\mathrm{WE}}$ are provided with the same driving capability. Each $\overline{\text { RAS }}$ output drives one bank of DRAMs so that the four $\overline{R A S}$ outputs are used to select the banks, while $\overline{\mathrm{CAS}}, \overline{\mathrm{WE}}$ and the multiplexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the data output in three-state. Only the bank with its associated $\overline{\text { RAS }}$ low will be written to or read from, except in mode 3 where all $\overline{R A S}$ signals go low to allow fast memory initialization.

## Pin Definitions

$\mathbf{V}_{\mathbf{c c}}$ GND, $G N D-\mathrm{V}_{\mathrm{Cc}}=5 \mathrm{~V} \pm 5 \%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from $V_{C c}$, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. Recommended solution would be a $1 \mu \mathrm{~F}$ multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

## R0-R7: Row Address Inputs.

## C0-C7: Column Address Inputs.

B0, B1: Bank Select Inputs-Strobed by ADS. Decoded to enable one of the $\overline{R A S}$ outputs when RASIN goes low, in modes 4-6. In mode 7 B0, B1 are used to define End-ofCount (see table 3).

Q0-Q8: Multiplexed Address Outputs-Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.
$\overline{\text { RASIN: }}$ : Row Address Strobe Input-Enables selected $\overline{\text { RAS }}_{n}$ output when M2 ( $\overline{\mathrm{RFSH}}$ ) is high (modes $4-6$ ), and all $\overline{\mathrm{RAS}}_{\mathrm{n}}$ outputs in modes $0,1,2$ and 3.

R/C: Row/Column Select Input-Selects either the row or column address input latch onto the output bus.
$\overline{\text { CASIN: }}$ Column Address Strobe Input-Inhibits $\overline{\text { CAS }}$ output when high in Modes 4 and 3 . In Mode 6 it can be used to prolong $\overline{\mathrm{CAS}}$ output.

ADS: Address (Latch) Strobe Input-Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.
$\overline{\mathbf{C S}}$ : Chip Select Input-Three-state's the Address Outputs and puts the control signal into a high-impedance logic " 1 " state when high (unless refreshing in mode 0, 1, 2). Enables all outputs when low.

M0, M1, M2 ( $\overline{\text { RFSH }})$ : Mode Control Inputs - These 3 control pins determine the 6 modes of operation of the 74 S 408 as depicted in Table 1.

RF I/O-The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active (low) when M2 $=0$ (modes 0 , 1,2 or 3 ) and the End-of-Count output is at 127 or 255 (see Table 3).
$\overline{\text { WIN: Write Enable Input. }}$
WE: Write Enable Output-Buffered output from $\overline{\text { WIN }}$.
$\overline{\text { CAS: }}$ Column Address Strobe Output—In Modes 5 and 6,
$\overline{\text { CAS }}$ transitions low following valid column address. In Modes 3 and 4, it goes low after R/C goes low, or follows $\overline{\mathrm{CASIN}}$ going low if R/C is already low. $\overline{\mathrm{CAS}}$ is high during refresh.
$\overline{\text { RAS }} 0$-3: Row Address Strobe Outputs-When M2( $\overline{\mathrm{RFSH}})$ is high (modes 4-7), the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When M2 ( $\overline{\mathrm{RFSH}}$ ) is low (modes $0-3$ ) all $\overline{\mathrm{RAS}}_{n}$ outputs go low together following RASIN going low.

| BANK SELECT <br> (STROBED BY ADS) | ENABLED $\overline{\mathrm{RAS}}_{\mathbf{n}}$ |
| :---: | :---: |
| B1 1 |  |
| 0 | 0 |
| 0 | 1 |

Table 1. Memory Bank Decode

## Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.
In normal memory access operation, $\overline{\text { RASIN }}$ and R/C are initially high. When the address inputs are enabled into the address latches (modes 4-6) the row addresses appear on the Q outputs. The Address Strobe also inputs the bank-select address, ( B 0 and B 1 ). If $\overline{\mathrm{CS}}$ is low, all outputs are enabled. When $\overline{\mathrm{CS}}$ is transitioned high, the address outputs go threestate and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S408s for multiaddressing. All outputs go active about 50 ns after the chip is selected again. If $\overline{C S}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

## Drive Capability

The 74S408 has timing parameters that are specified with up to 600 pF loads for $\overline{\mathrm{CAS}}, 500 \mathrm{pF}$ loads for $\mathrm{Q}_{0}-\mathrm{Q}_{7}$ and $\overline{W E}$, and 150 pF loads for $\overline{\mathrm{RAS}}_{\mathrm{n}}$ outputs. In a typical memory system this is equivaient to about 885 V -oniy DRAMis, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.
Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6). The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

## 745408 Driving Any $16 K$ or 64K DRAMs

The 74 S 408 can drive any 16 K or 64 K DRAMs. The on-chip 8 -bit counter with selectable End-of-Count can support refresh of 128 or 512 rows, while the 8 address and $4 \overline{\operatorname{RAS}}_{\mathrm{n}}$ outputs can address 4 banks of 16 K or 64 K DRAMs.

## Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{W E}$, determines what type of memory access cycle the memory will perform. If $\overline{W E}$ is kept high while $\overline{\mathrm{CAS}}$ goes low, a read cycle occurs. If $\overline{W E}$ goes low before $\overline{\text { CAS }}$ goes low, a write cycle occurs and DATA at DI (DRAM input data) is written into the DRAM as $\overline{C A S}$ goes low. If $\overline{W E}$ goes low later than tCWD after $\overline{C A S}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data $D_{1}$ is written into the same address in the DRAM when $\bar{W}$ goes low. In this read-modify-write case, DI and DO can-
not be linked together. The type of cycle is therefore controlled by $\overline{W E}$, which follows $\overline{W I N}$.

## Power-Up Initialize

When $V_{C C}$ is first applied to the 74 S 408 , an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As VCC increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below $V_{C C}$, and the output address to three-state. As VCC increases above 2.3 volts, control of these outputs is granted to the system.

## 74S408 Functional Mode Description

The 74S408 operates in 6 different functional modes. The operating mode is selected by signals $M_{0}, M_{1}, M_{2}$. Selecting $M_{2}, M_{1}, M_{0}=0,0,0$ or $0,0,1$ or $0,1,0$ will result at the same operating mode designated as mode $0,1,2$ (see Table 2).

| MODE | $\begin{gathered} (\overline{\mathrm{RFSH}}) \\ \mathrm{M} 2 \end{gathered}$ | M1 | MO | MODE OF OPERATION | CONDITIONS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0,1,2 | $\begin{aligned} & 0 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \end{aligned}$ | Externally-controlled refresh | RF I/O = EOC |
| 3 | 0 | 1 | 1 | Externally-controlled All-बRAS write | All- $\overline{\mathrm{RAS}}$ active |
| 4 | 1 | 0 | 0 | Externally-controlled access | Active $\overline{\mathrm{RAS}}$ defined by Table 2 |
| 5 | 1 | 0 | 1 | Auto access, slow traH | Active $\overline{R A S}$ defined by Table 2 |
| 6 | 1 | 1 | 0 | Auto access, fast traH | Active $\overline{R A S}$ defined by Table 2 |
| 7 | 1 | 1 | 1 | Set end of count | See Table 3 for Mode 7 |

Table 2. 74S408 Mode Select Options

## 745408 Functional Mode Descriptions

## Modes 0, 1, 2-Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled onto $\mathrm{R}_{0}-\mathrm{R}_{7}$ outputs, all $\overline{\mathrm{RAS}}$ outputs are enabled following $\overline{\mathrm{RASIN}}$, and CAS is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either RASIN or $\mathrm{M}_{2}(\overline{\mathrm{RFSH}})$ goes low-to-high while the other is low. RF I/O goes low when the count is 127 or 255 with $\overline{\text { RASIN }}$ and $\overline{\text { RFSH }}$ as set by End-of-Count (see Table 3), low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.
During refresh, $\overline{\text { RASIN }}$ and $M_{2}(\overline{\mathrm{RFSH}})$ can transition low simultaneously because the refresh counter becomes valid on the output but $t_{\text {RFLCT }}$. This means the counter address is valid on the $Q$ outputs before $\overline{R A S}$ occurs on all $\overline{R A S}$ out-
puts, strobing the counter address into that row of all the DRAMS (see Figure 2). To perform externally controlled burst refresh $M_{2}(\overline{\mathrm{RFSH}})$ initially can again have the same edge as RASIN, but then can maintain a low state, since RASIN going low-to-high increments the counter (performing the burst refresh).

## Mode 3-Externally Controlled All-RAS Write

This mode is useful at system initialization. The memory address is provided by the processor, which also perform the incrementing. All four $\overline{\mathrm{RAS}}$ outputs follow $\overline{\text { RASIN }}$ (supplied by the processor), strobing the row address into the DRAMs. R/C can now go low, while CASIN may be used to control $\overline{\mathrm{CAS}}$ (as in the Externally Controlled Access mode), so that $\overline{\mathrm{CAS}}$ strobes the column address contents into the DRAMs. At this time $\overline{W E}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74 S 408 for the next write cycle.

*INDICATES DYNAMIC RAM PARAMETERS

Figure 2. External Control Refresh Cycle (Modes 0, 1, 2)

## Mode 4-Externally Controlled Access

This mode facilitates externally controlling all accesstiming parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

## Output Address Selection

Refer to Figure 4a. With M2 ( $\overline{\mathrm{RFSH}}$ ) and R/C high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided $\overline{\mathrm{CS}}$ is set low. The column address latch contents are output after R/C goes low. RASIN can go low after the row addresses have been set up on Q0-Q7. This selects one of the $\overline{\mathrm{RAS}}$ outputs, strobing the row address on the $Q$ outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/C can go low so that about 40 ns later column addresses appear on the $Q$ outputs.

## Automatic CAS Generation

In a normal memory access cycle $\overline{\mathrm{CAS}}$ can be derived from
inputs $\overline{\text { CASIN }}$ or R/C. If $\overline{\text { CASIN }}$ is high, then R/C going low switches the address output drivers from rows to columns. $\overline{\text { CASIN }}$ then going low causes $\overline{\text { CAS }}$ to go low approximately 40 ns later, allowing $\overline{\text { CAS }}$ to occur at a predictable time (see Figure 4b). For maximum system speed, CASIN can be kept low, since $\overline{\text { CAS }}$ will automatically occur approximately 20 ns after the column addresses are valid, or about 60 ns after $R / \bar{C}$ goes low (see Figure 4a). Most DRAMs have a column address set-up time before $\overline{\text { CAS }}\left(\mathrm{t}_{\mathrm{ASC}}\right)$ of 0 ns or -10 ns . In other words, a $t_{\text {Asc }}$ greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

## Fast Memory Access

For faster access time, R/C̄ can go low a time delay ( $\mathrm{t}_{\mathrm{RPDL}}+$ $t_{\text {RAH }}-t_{\text {RHA }}$ ) after RASIN goes low, where $t_{\text {RAH }}$ is the RowAddress hold-time of the DRAM.


Figure 3. Typical Application of $\mathbf{7 4 S 4 0 8}$ Using Externally Controlled Access and Refresh in Modes 0 and 4

## SN74S408/DP8408A SN74S408-2/DP8408A-2


*INDICATES DYNAMIC RAM PARAMETERS
Figure 4a. Read Cycle Timing (Mode 4)

*INDICATES DYNAMIC RAM PARAMETERS
Figure 4b. Write Cycle Timing (Mode 4)

## Mode 5-Automatic Access

In the Auto Access mode all outputs except $\overline{\text { WE }}$ are initiated from RASIN. Inputs R/C and CASIN are unnecessary and the output control signals are derived internally from one input signal ( $\overline{\operatorname{RASIN}}$ ) minimizing timing-skew problems, thereby reducing memory-access time substantially and allowing the use of slower DRAMs.

## Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{R A S}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for $\mathrm{t}_{\text {RAH }}$, (the Row-Address hold-time of the DRAM), the column address is set up and then CAS occurs. This is all performed automatically by the 74S408 in this mode.

Provided the input address is valid as ADS goes low, $\overline{\text { RASIN }}$ can go low any time after ADS. This is because the selected $\overline{R A S}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S408. The Address Set-Up time ( $\mathrm{t} A \mathrm{AR}$ ), is 0 ns on most DRAMs. The 74S408 in this mode (with ADS and RASIN edges simultaneously applied) produces a minimum $t_{\text {ASR }}$ of 0 ns . This is true provided the input address was valid $t_{\text {ASA }}$ before ADS went low (see Figure 5a).

Next, the row address is disabled after $t_{\text {RAH }}$ ( 30 ns minimum); in most DRAMs, $\mathrm{t}_{\text {RAH }}$ minimum is less than 30 ns . The column address is then set up and $\mathrm{t}_{\text {Asc }}$ later, $\overline{\mathrm{CAS}}$ occurs. The only other control input required is $\overline{\mathrm{WIN}}$. When a
 before CAS Is output low.


Figure 5a. Modes 5, 6 Timing (CASIN High in Mode 6)

This gives a total typical delay from: input address valid to $\overline{\text { RASIN }}$ ( 15 ns ); to $\overline{\text { RAS }}(27 \mathrm{~ns}$ ); to rows held ( 50 ns ); to columns valid ( 25 ns ); to $\overline{\mathrm{CAS}}(23 \mathrm{~ns})=140 \mathrm{~ns}$ (that is, 125 ns from $\overline{\text { RASIN }}$ ). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{\text { RASIN. }}$

## Mode 6-Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster $t_{\text {RAH }}$ of 20 ns , minimum. It therefore can only be used with fast 16 k or 64 k DRAMs (which have a $\mathrm{t}_{\text {RAH }}$ of 10 ns to 15 ns )
in applications requiring fast access times; $\overline{\operatorname{RASIN}}$ to $\overline{\mathrm{CAS}}$ is typically 105 ns .

In this mode, the R/ $\overline{\mathrm{C}}$ pin is not used, but $\overline{\mathrm{CASIN}}$ is used to allow an extended $\overline{\mathrm{CAS}}$ after $\overline{\mathrm{RAS}}$ has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where $\overline{\text { RAS }}$ has to be terminated as soon as possible before the next $\overline{R A S}$ begins (to meet the precharge time, or $t_{R P}$, requirements of the DRAM). CAS may then be held low by $\overline{\text { CASIN }}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{\text { CASIN }}$ subsequently going high ends $\overline{\mathrm{CAS}}$. If this extended $\overline{\mathrm{CAS}}$ is not required, CASIN should be set high in Mode 6.


Figure 5b. Mode 6 Timing, Extended CAS

## Mode 7-Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127 ; with B1=0
and $\mathrm{BO}=1, \mathrm{EOC}$ is 255 ; and with $\mathrm{B} 1=1$ and $\mathrm{BO}=0$, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

| BANK SELECT <br> (STROBED BY ADS) |  | END OF COUNT <br> SELECTED |
| :---: | :---: | :---: |
| B1 | B0 |  |
| 0 | 0 | 127 |
| 0 | 1 | 255 |
| 1 | 0 | 127 |
| 1 | 1 | 127 |



Figure 6. Change in Propagation Delay vs Loading Capacitance Relative to a 500pF Load

## SN74S408/-2 Specifications:

## Absolute Maximum Ratings (Note 1)

```
Supply voltage \mp@subsup{V}{CC}{} ........................................................................................ -0.5 V to 7.0 V
Storage temperature range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . - }6. 6\mp@subsup{5}{}{\circ}\mathrm{ to +150年 C
```





```
NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.
```


## Operating Conditions

| SYMBOL | PARAMETER | FIGURE | 'S408 |  |  | 'S408-2 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $V_{C C}$ | Supply voltage |  | 4.75 |  | 5.25 | 4.25 |  | 5.25 | V |
| TA | Operating free-air temperature |  | 0 |  | + 75 | 0 |  | + 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{\text {ASA }}$ | Address setup time to ADS | Figures 4a,4b,5a,5b | 15 |  |  | 15 |  |  | ns |
| taHA | Address hold time from ADS | Figures 4a,4b,5a,5b | 15 |  |  | 15 |  |  | ns |
| ${ }^{\text {t }}$ ADS | Address strobe pulse width | Figures 4a,4b,5a,5b | 30 |  |  | 30 |  |  | ns |
| trHA | Row address held from column select | Figure 4a | 10 |  |  | 10 |  |  | ns |
| trasinl, H | Pulse width of $\overline{\text { RASIN }}$ during refresh | Figure 2 | 50 |  |  | 50 |  |  | ns |
| trst | counter reset pulse width | Figure 2 | 70 |  |  | 70 |  |  | ns |

Electrical Characteristics: $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 5.0 \%, 0^{\circ} \mathrm{C} \leqslant \mathrm{T}_{\mathrm{A}} \leqslant 75^{\circ} \mathrm{C}$ Typicals are for $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{C}}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{I}_{\mathrm{C}}=-12 \mathrm{~mA}$ |  | $-0.8$ | -1.2 | V |
| IIH1 | Input high current for ADS. R/C only. | $V_{1 N}=2.5 \mathrm{~V}$ |  | 2.0 | 100 | $\mu \mathrm{A}$ |
| 1/H2 | Input high current for other inputs, except RF I/O | $\mathrm{V}_{\text {IN }}=2.5 \mathrm{~V}$ |  | 1.0 | 50 | $\mu \mathrm{A}$ |
| IIRSI | Output load current for RF I/O | $\mathrm{V}_{\text {IN }}=0.5 \mathrm{~V}$, output high |  | -1.5 | -2.5 | mA |
| IJCTL | Output load current for $\overline{\text { RAS }}$, $\overline{\mathrm{CAS}}, \overline{\text { WE }}$ | $\mathrm{V}_{\text {IN }}=0.5 \mathrm{~V}$, chip deselect |  | -1.5 | -2.5 | mA |
| ILI | Input low current for ADS. R/C̄ only | $\mathrm{V}_{1 \mathrm{~N}}=0.5 \mathrm{~V}$ |  | -0.1 | -1.0 | mA |
| IIL2 | Input low current for other inputs, except RF I/O | $V_{I N}=0.5 \mathrm{~V}$ |  | -0.05 | -0.5 | mA |
| $\mathrm{V}_{\text {IL }}{ }^{* *}$ | Input low threshold |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}{ }^{* *}$ | Input high threshold |  | 2.0 | V |  |  |
| $\mathrm{V}_{\mathrm{OL} 1}$ | Output low voltage, except RF I/O | $1 \mathrm{OL}=20 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\text {OL2 }}$ | Output low voltage for RF I/O | $\mathrm{lOL}=10 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| $\mathrm{VOH1}$ | Output high voltage, except RF I/O | $\mathrm{VOH}=-1 \mathrm{~mA}$ | 2.4 | 3.5 |  | V |
| $\mathrm{V}_{\mathrm{OH} 2}$ | Output high voltage for RF I/O | $\mathrm{IOH}=-100 \mu \mathrm{~A}$ |  | 3.5 |  | V |
| 110 | Output high drive current except RF I/O | $\mathrm{V}_{\text {OUT }}=0.8 \mathrm{~V}$ (Note 3) |  | -200 |  | mA |
| 10 D | Output low drive current, except RF I/O | $\mathrm{V}_{\text {OUT }}=2.7 \mathrm{~V}$ (Note 3) |  | 200 |  | mA |
| Ioz | Three-state output current (address outputs) | $\begin{aligned} & 0.4 \mathrm{~V} \leqslant \mathrm{~V}_{\text {OUT }} \leqslant 2.7 \mathrm{~V}, \\ & \mathrm{CS}=2.0 \mathrm{~V}, \text { Mode } 4 \end{aligned}$ | $-50$ | 1.0 | 50 | $\mu \mathrm{A}$ |
| ICC | Supply current | $\mathrm{V}_{\text {CC }}=$ MAX |  | 210 | 285 | mA |
| $\mathrm{CIN}_{\text {IN }}$ | Input capacitance ADS, R/C̄ | $T_{A}=25^{\circ} \mathrm{C}$ |  | 8 |  | pF |
| $\mathrm{CIN}_{1}$ | Input capacitance all other inputs | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 5 |  | pF |

Switching Characteristics: VCC $=5.0 \mathrm{~V} \pm 5.0 \%, 0^{\circ} \mathrm{C} \quad \mathrm{T}_{\mathrm{A}} \quad 75^{\circ} \mathrm{C}$ See Figure 7 for test load (switches S1 and S2 are closed unless otherwise specified) typicals are for VCC $=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

| SYMBOL | ACCESS PARAMETER | TEST CONDITIONS | 'S408 |  |  | 'S408-2 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\text {RICL }}$ | $\overline{\text { RASIN }}$ to $\overline{\mathrm{CAS}}$ output delay (Mode 5) | Figure 5a | 95 | 125 | 160 | 75 | 100 | 130 | ns |
| $\mathrm{t}_{\text {RICL }}$ | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 6) | Figures 5a,5b | 80 | 105 | 140 | 65 | 90 | 115 | ns |
| $\mathrm{t}_{\mathrm{RICH}}$ | $\widehat{\text { RASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 5) | Figure 5a | 50 | 63 | 80 | 50 | 63 | 80 | ns |
| ${ }^{\text {t } \mathrm{RICH}}$ | RASIN to $\overline{\text { CAS }}$ output delay (Mode 6) | Figures 5a,5b | 40 | 48 | 60 | 40 | 48 | 60 | ns |
| $\mathrm{t}_{\text {RCDL }}$ | $\overline{\mathrm{RAS}}$ to $\overline{\mathrm{CAS}}$ output delay (Mode 5) | Figure 5a |  | 98 | 125 |  | 75 | 100 | ns |
| ${ }^{\text {t RCDL }}$ | $\widehat{\text { RAS }}$ to $\overline{\mathrm{CAS}}$ output delay (Mode 6) | Figures 5a,5b |  | 78 | 105 |  | 65 | 85 | ns |
| $\mathrm{t}_{\mathrm{RCDH}}$ | $\overline{\mathrm{RAS}}$ to $\overline{\mathrm{CAS}}$ output delay (Mode 5) | Figure 5a |  | 27 | 40 |  | 27 | 40 | ns |
| ${ }^{\text {tRCDH }}$ |  | Figure 5a |  | 40 | 65 |  | 40 | 65 | ns |
| ${ }^{\text {t }} \mathrm{CCDH}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 6) | Figure 5b | 40 | 54 | 70 | 40 | 54 | 70 | ns |
| trcV | $\overline{\text { RASIN }}$ to column address valid (Mode 5) | Figure 5a |  | 90 | 120 |  | 30 | 105 | ns |
| trev | $\overline{\text { RASIN }}$ to column address valid (Mode 6) | Figure 5a |  | 75 | 105 |  | 70 | 90 | ns |
| trPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ delay | Figures 4a,4b,5a,5b | 20 | 27 | 35 | 20 | 27 | 35 | ns |
| tRPDH | $\overline{\text { RASIN }}$ to $\overline{\mathrm{RAS}}$ delay | Figures 4a,4b,5a,5b | 15 | 23 | 32 | 15 | 23 | 32 | ns |
| ${ }^{\text {t }}$ APDL | Address input to output low delay | Figures 4a,4b,5a,5b |  | 25 | 40 |  | 25 | 40 | ns |
| tAPDH | Address input to output high delay | Figures 4a,4b,5a,5b |  | 25 | 40 |  | 25 | 40 | ns |
| tSPDL | Address strobe to address output low | Figure 4b,4a |  | 40 | 60 |  | 40 | 60 | ns |
| tSPDH | Address strobe to address output high | Fibure 4b,4a |  | 40 | 60 |  | 40 | 60 | ns |
| tWPDL | $\overline{\text { WIN }}$ to $\overline{\text { WE output delay }}$ | Figure 4b | 15 | 25 | 30 | 15 | 25 | 30 | ns |
| tWPDH | $\overline{\text { WIN }}$ to $\overline{\text { WE }}$ output delay | Figure 4b | 15 | 30 | 60 | 15 | 30 | 60 | ns |
| ${ }^{\text {t CPPDL }}$ | $\overline{\text { CASIN }}$ to $\overline{\text { CAS }}$ delay (RiC) low in Mode 4) | Figure 4b | 32 | 41 | 58 | 32 | 41 | 58 | ns |
| tCPDH | $\overline{\text { CASIN }}$ to $\overline{\mathrm{CAS}}$ delay | Figure 4b | 25 | 39 | 50 | 25 | 39 | 50 | ns |
| $\mathrm{t}_{\mathrm{RCC}}$ | Column select to column address valid | Figure 4a |  | 40 | 58 |  | 40 | 58 | ns |
| $t_{\text {t }}$ | Row select to row address valid | Figure 4a,4b |  | 40 | 58 |  | 40 | 58 | ns |
| tcTL | RF I/O low to counter outputs all low | Figure 2 |  |  | 100 |  |  | 100 | ns |
| trFPDL | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ delay during refresh | Figure 2 | 35 | 50 | 70 | 35 | 50 | 70 | ns |
| trFPDH | $\widehat{\text { RASIN }}$ to $\widehat{\mathrm{RAS}}$ delay during refresh | Figure 2 | 30 | 40 | 55 | 30 | 40 | 55 | ns |
| trFLCT | $\overline{\text { RFSH }}$ low to counter address valid | $C S=X$, Figure 2 |  | 47 | 60 |  | 47 | 60 | ns |
| trfing | $\overline{\text { RFSH }}$ high to row address valid | Figure 2 |  | 45 | 60 |  | 45 | 60 | ns |
| trohnc | $\overline{\text { RAS }}$ high to new count valid | Figure 2 |  | 30 | 55 |  | 30 | 55 | ns |
| $t_{\text {RLEOC }}$ | $\overline{\text { RASIN }}$ low to end-of-count low | $C_{L}=50 \mathrm{pF}$, Figure 2 |  |  | 80 |  |  | 80 | ns |
| $t_{\text {RHEOC }}$ | $\overline{\text { RASIN }}$ high to end-of-count high | $C_{L}=50 \mathrm{pF}$, Figure 2 |  |  | 80 |  |  | 80 | ns |
| $t_{\text {RAHI }}$ | Row address hold time (Mode 5) | Figure 5a | 30 |  |  | 20 |  |  | ns |
| traH | Row address hold time (Mode 6) | Figures 5a,5b | 20 |  |  | 12 |  |  | ns |
| tASC | Column address setup time (Mode 5) | Figure 5a | 8 |  |  | 3 |  |  | ns |
| tasc | Column address setup time (Mode 6) | Figures 5a,5b | 6 |  |  | 3 |  |  | ns |
| trHA | Row address held from column select | Figure 4a | 10 |  |  | 10 |  |  | ns |
| tCRS | $\overline{\text { Casin }}$ setup time to $\overline{\text { Rasin }}$ high (Mode 6) | Figure 5b | 35 |  |  | 35 |  |  | ns |

## Switching Characteristics: (Cont.)

| SYMBOL | ACCESS PARAMETER | TEST CONDITIONS | 'S408 |  |  | 'S408-2 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| THREE-STATE PARAMETER |  |  |  |  |  |  |  |  |  |
| tzH | $\overline{\mathrm{CS}}$ low to address output high from HI-Z | Figure 7 $\begin{aligned} & R 1=3.5 \mathrm{k} \\ & \mathrm{R} 2=1.5 \mathrm{~K} \end{aligned}$ |  | 35 | 60 |  | 35 | 60 | ns |
| $\mathrm{t}_{\mathrm{Hz}}$ | $\overline{\mathrm{CS}}$ high to address output $\mathrm{Hi}-\mathrm{Z}$ from high | $\begin{aligned} & C_{L}=15 p, \text { Figure } 7 \\ & R 2=1 \mathrm{k}, S 1 \text { open } \end{aligned}$ |  | 20 | 40 |  | 20 | 40 | ns |
| TZL | $\overline{\mathrm{CS}}$ low to address output low from $\mathrm{Hi}-\mathrm{Z}$ | Figure 7 $\begin{aligned} & \mathrm{R} 1=3.5 \mathrm{k} \\ & \mathrm{R} 2=1.5 \mathrm{k} \end{aligned}$ |  | 35 | 60 |  | 35 | 60 | ns |
| tLz | $\overline{\mathrm{CS}}$ high to address output $\mathrm{Hi}-\mathrm{Z}$ from low | $\begin{aligned} & C_{L}=15 \mathrm{pF}, \text { Figure } 7 \\ & R 1=1 \mathrm{k}, \mathrm{~S} 2 \text { open } \end{aligned}$ |  | 25 | 50 |  | 25 | 50 | ns |
| THZH | $\overline{\mathrm{CS}}$ low to control output high from Hi-Z high | Figure 7 $R 2=750 \Omega$ <br> S1 open |  | 50 | 80 |  | 50 | 80 | ns |
| thHZ | $\overline{\mathrm{CS}}$ high to control output Hi -Z high from high | $\begin{aligned} & C_{L}=15 \mathrm{pF} \\ & \text { Figure } 7 \\ & \text { R2 }=750 \Omega, \text { S1 open } \end{aligned}$ |  | 40 | 75 |  | 45 | 75 | ns |
| thzL | $\overline{\mathrm{CS}}$ low to control output low from Hi-Z high* | Figure 7, S1, S2 open |  | 45 | 75 |  | 45 | 75 | ns |
| tLHz | $\overline{\mathrm{CS}}$ high to control output Hi Z high from low* | $C_{L}=15 \mathrm{pF}$ <br> Figure 7 $R 2=750 \Omega$ <br> S1 open |  | 50 | 80 |  | 50 | 80 | ms |

*Internally the device contains a 3 K resistor in series with a Schottky Diode to VCC.
Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: $Q 0-Q 8, \overline{W E} C_{L}=500 \mathrm{pF}$; $\overline{\operatorname{RAS}} \mathrm{C}_{\mathrm{L}}=150 \mathrm{pF} ;$ CAS $C_{L}=600 \mathrm{pF}$ unless otherwise noted.
Note 2: All typical values are for $T_{A}=25^{\circ}$ and $V_{C}=5.0 \mathrm{~V}$.
Note 3: This test is provided as a monitor of driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters a $15 \Omega$ resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.
Note 4: Input pulse 0 V to $3.0 \mathrm{~V}, \mathrm{t}_{\mathrm{R}}=\mathrm{t}_{\mathrm{F}}=2.5 \mathrm{~ns}, \mathrm{f}=2.5 \mathrm{MHz}, \mathrm{t}_{\mathrm{PW}}=200 \mathrm{~ns}$. Input reference point on AC measurements is 1.5 V . Output reference points are 2.7 V for High and 0.8 V for Low.

Note 5: The load capacitance on RF //O should not exceed 50 pF .

$R_{1}, R_{2}=4.7 \mathrm{~K}$ Except as specified


Figure 7. Waveform

[^47]
## Features/Benefits

- All DRAM drive functions on one chip have on-chip highcapacitance load drivers (specified up to 88 DRAMs)
- Drives directly all 16K, 64K and 256K DRAMs; capable of addressing up to 1 M words
- Propagation delays of $\mathbf{2 5}$ nsec typical at $\mathbf{5 0 0} \mathbf{~ p F}$ load
- Supports READ, WRITE and READ-MODIFY-WRITE cycles
- Eight modes of operation support externally-controlled and automatic access and refresh, as well as special memory initialization access
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255 or 511)
- Direct replacement for National DP8409, DP8409A


## Operating Modes

| 0 | Externally-controlled fresh |
| :---: | :--- |
| 1 | Auto refresh - forced |
| 2 | Automatic burst refresh |
| 3 a | All- $\overline{\mathrm{RAS}}$ auto write |
| 3 b | Externally-controlled All- $\overline{\mathrm{RAS}}$ write |
| 4 | Externally-controlled access |
| 5 | Auto access, slow tRAH, hidden refresh |
| 6 | Auto access, fast tRAH |
| 7 | Set end of count |



Interface Between System and DRAM Banks

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN74S409 | 48 N, D | Com |
| SN74S409-2 | 48 N, D | Com, Speed Option |

## Pin Configuration



## Block Diagram



Figure 1. 74S409 Functional Block Diagram

## Description

The 74S409 is a Multi-Mode Dynamic RAM Controller/Driver capable of directly driving up to 88 DRAMs. 20 address lines to the 74 S 409 allow it to address up to 1 M words and it can drive $16 \mathrm{~K}, 64 \mathrm{~K}$ and 256 K DRAMs. Since the 74 S 409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, and saves board space.
The 74S409's 8 operating modes offer externally-controlled or on-chip automatic access and refresh. An on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.
The 74S409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control
logic. The 74S409 timing parameters are specified when driving the typical load capitance of 88 DRAMs, including trace capacitance.
The 745409 can drive up to 4 banks of DRAMs, with each bank comprised of $16 \mathrm{Ks}, 64 \mathrm{Ks}$ or 256 Ks . Control signal outputs $\overline{C A S}$ and $\overline{W E}$ are provided with the same driving capability. Each $\overline{R A} \bar{S}$ output drives one bank of DRAMs so that the four $\overline{R A S}$ outputs are used to select the banks, while $\overline{C A S}, \overline{W E}$ and the muitipiexed addresses can be connected to all the banks of DRAMs. This leaves the nonselected banks in the standby mode (less than one tenth of the operating power) with the respective data outputs in three-state. Only the bank with its associated $\overline{\text { RAS }}$ low will be written to or read from, except in mode 3 where all RAS signals go low to allow fast memory initialization.

## Pin Definitions

$V_{c c}$ GND, $G N D-V_{c C}=5 V \pm 5 \%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from $V_{\mathrm{CC}}$, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution is a $1-\mu \mathrm{F}$ multilayer ceramic capacitor in parallet with a lowvoltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

## RO-R8: Row Address Inputs.

## Co-C8: Column Address Inputs.

B0, B1: Bank Select Inputs - Strobed by ADS. Decoded to enable one of the RAS outputs when RASIN goes low, in modes 4-6. In mode 7 BO, B1 are used to define End-ofCount (see table 3), and select mode 3a or 3b.
QO-Q8: Multiplexed Address Outputs - Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.
RASIN: Row Address Strobe Input-Enables selected $\overline{\text { RAS }_{n}}$ output when M2 (RFSH) is high (modes 4-6), and all $\overline{R A S}_{n}$ outputs in modes 0 and 3 . RASIN input is disabled in modes 1 and 2.
R/C (RFCK) - In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input, selecting either the row or column address input latch onto the output bus.
CASIN (RGCK)-In modes 1,2 and 3a, this pin is the RAS Generator Clock input. In all other modes it is $\overline{\text { CASIN (Column }}$ Address Strobe Input), which inhibits CAS output when high in Modes 3b and 4. In Mode 6 it can be used to prolong CAS output.
ADS: Address (Latch) Strobe Input-Strobes Input Row Address, Column Address, and Bank Select Inputs into respective latches when high; latches on High-to-Low transition.
$\overline{\mathbf{C S}}$ : Chip Select Input-three-state's the Address Outputs and puts the control signal into a high-impedance logic " 1 " state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.
M0, M1, M2 ( $\overline{\mathrm{RFSH}}$ ): Mode Control Inputs - These 3 control pins determine the 8 major modes of operation of the 74S409 as depicted in Table 2.
RF I/O $\overline{\mathbf{R F R Q}}$ - This I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0,2 and

| BANK SELECT <br> (STROBED BY ADS) |  | ENABLED RAS ${ }_{\boldsymbol{n}}$ |
| :---: | :---: | :---: |
| B1 | B0 |  |
| 0 | 0 | RAS $_{0}$ |
| 0 | 1 | RAS $_{1}$ |
| 1 | 0 | RAS $_{2}$ |
| 1 | 1 | RAS $_{3}$ |

Table 1. Memory Bank Decode

3a when the End-of-Count output is at 127, 255, or 511 (see Table 3). In Auto-Refresh Mode (mode 5) it is the Refresh $\overline{\text { Request ( } \overline{R F R Q} \text { ) output. }}$
WIN: Write Enable Input.
$\overline{\text { WE: Write Enable Output - Buffered output from WIN. }}$
CAS: Column Address Strobe Output - In Modes 3a, 5, and 6, CAS transitions low following valid column address. In Modes 3b and 4, it goes low after R/C goes low, or follows $\overline{\mathrm{CASIN}}$ going low if $\mathrm{R} / \overline{\mathrm{C}}$ is already low. $\overline{\mathrm{CAS}}$ is high during refresh.
$\overline{\text { RAS }} 0-3$ : Row Address Strobe Outputs - When M2( $\overline{\mathrm{RFSH}})$ is high (modes 4-6), the selected row address strobe output (decoded from signals B0, B1) follows the RASIN input. When M2 ( $\overline{\mathrm{RFSH}}$ ) is low (modes $0-3$ ) all $\overline{\mathrm{RAS}}_{\mathrm{n}}$ outputs go low together following RASIN going low in modes 0 and 3 and automatically in modes 1 and 2 .

## Input Addressing

The address block consists of a row-address latch, a columnaddress latch, and a resettable refresh counter.
The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid address until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the address is still valid.
In normal memory-access operation, $\overline{\operatorname{RASIN}}$ and $\mathrm{R} / \overline{\mathrm{C}}$ are initially high. When the address inputs are enabled into the address latches (modes 3-6) the row addresses appear on the $Q$ outputs. The Address Strobe also inputs the bankselect address, (BO and B1). If CS is low, all outputs are enabled. When CS goes high, the address outputs go threestate and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other 74S409s for multiaddressing. All outputs go active about 50 ns after the chip is selected again. If CS is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

## Drive Capability

The 74S409 has timing parameters that are specified with up to 600 pF loads for $\overline{\mathrm{CAS}}$ and $\overline{\mathrm{WE}}, 500 \mathrm{pF}$ loads for $\mathrm{Q}_{0}-\mathrm{Q}_{8}$, and 150pF loads for $\overline{R A S}_{n}$ outputs. In a typical memory system this is equivalent to about 885 V -only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 14. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

## 74S409 Driving Any 16K, 64K or 256K DRAMs

The 74 S 409 can drive any $16 \mathrm{~K}, 64 \mathrm{~K}$, or 256 K DRAMs. The on-chip 9-bit counter with selectable End-of-Count can support refresh of 128,256 and 512 rows, while the 9 address and $4 \overline{\mathrm{RAS}}_{\mathrm{n}}$ outputs can address 4 banks of $16 \mathrm{~K}, 64 \mathrm{~K}$ or 256K DRAMs.

## Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{W E}$, determines what type of memory access cycle the memory will perform. If WE is kept high while $\overline{C A S}$ goes low, a read cycle occurs. If $\overline{W E}$ goes low
before $\overline{C A S}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as CAS goes low. If $\overline{W E}$ goes low later than tCWD after $\overline{C A S}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data $D I$ is written into the same address in the DRAM when WE goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{W E}$, which follows $\overline{W I N}$.

## Power-Up Initialize

When $\mathrm{V}_{\mathrm{CC}}$ is first applied to the 74 S 409 , an internal pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As VCC increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below $\mathrm{V}_{\mathrm{CC}}$, and the output address to three-state. As VCC increases above 2.3 volts, control of these outputs is granted to the system.

## 745409 Functional Modes Description

The 74S409 operates in 8 different functional modes selected by signals $M_{0}, M_{1}, M_{2}$. Mode 3 splits further to modes $3 a$ and $3 b$ determined by signals $B_{0}, B_{1}$ in mode 7 .
Mode 0 and mode 1 are generally used as Refresh modes for mode 4 and mode 5 respectively, and therefore will be described as mode-pairs 0,4 and 1,5.
Mode 6 is a fast access made for very fast DRAMs and mode 7 is used only to determine choice of mode 3 a or 3 b and for setting End-of-Count for the refresh modes.

| MODE | $\begin{aligned} & \text { (RFSH) } \\ & \text { M2 } \end{aligned}$ | M1 | MO | MODE OF OPERATION | CONDITIONS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | Externally-controlled refresh | RF I/O = EOC |
| 1 | 0 | 0 | 1 | Auto refresh-forced | RF I/O = Refresh request (RFRQ) |
| 2 | 0 | 1 | 0 | Automatic burst refresh | $\mathrm{RF} \mathrm{I} / \mathrm{O}=\mathrm{EOC}$ |
| $3 a^{*}$ | 0 | 1 | 1 | All-RAS auto write | RF I/O = EOC; all RAS active |
| 3b* | 0 | 1 | 1 | Externally-controlled All- $\overline{\mathrm{RAS}}$ write | All- $\overline{\mathrm{RAS}}$ active |
| 4 | 1 | 0 | 0 | Externally-controlled access | Active RAS defined by Table 2 |
| 5 | 1 | 0 | 1 | Auto access, slow trAH, hidden refresh | Active $\overline{\text { RAS }}$ defined by Table 2 |
| 6 | 1 | 1 | 0 | Auto access, fast trAH | Active RAS defined by Table 2 |
| 7 | 1 | 1 | 1 | Set end of count; determines mode 3a or 3b | See Table 3 for Mode 7 |

*Mode $3 b$ is selected by setting $\mathrm{B}_{1}, \mathrm{~B}_{0}$ to 11 in mode 7 .

Table 2. 74S409 Mode Select Options

## Mode 0-Externally-Controlled Refresh Mode 4 - Externally-Controlled Access

Modes 0 and 4 facilitate external control of all timing parameters associated with the DRAMs. These modes are independent modes of operation though generally used together in the same application as shown in Figure 2.

## Mode 0-Externally-Controlled Refresh

In this mode the input address latches are disabled from the address outputs and the refresh counter is enabled. All RAS outputs go low following RASIN and refresh the enabled row in all four banks. $\overline{C A S I N}$ and $R / \bar{C}$ inputs are not used and $\overline{\mathrm{CAS}}$ is inhibited. The refresh counter increments when either RASIN or M2 (RFSH) switch high while the other is still low.

RF I/O goes low when the count equals End-of-Count (as set in mode 7), and RASIN is low. The 9-bit counter will always roll-over to zero at 512, regardless of End-of-Count. However, the counter can be reset at any time by driving RF I/O low through an external open-collector.

During refresh, $\overline{\text { RASIN }}$ and M2 ( $\overline{\mathrm{RFSH}}$ ) can transition low simultaneously because the refresh counter becomes valid on the output bus tRFLCT after RFSH goes low, which is a shorter time than tRFPDL. This means the counter address is valid on the $Q$ outputs before $\overline{R A S}$ occurs on all $\overline{R A S}$ outputs, strobing the counter address into that row of all the DRAMs (see Figure 2.). To perform externally-controlled burst refresh, $\overline{\text { RFSH }}$ initially can again have the same edge as $\overline{\text { RASIN }}$, but then maintains a low state, since $\overline{\text { RASIN }}$ going low-to-high increments the counter (performing the burst refresh).


Figure 2. Typical Application of 74S409 Using Externally-Controlled Access and Refresh in Modes 0 and 4

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Figure 3. External Control Refresh Cycle (Mode 0)

## Mode 4 - Externally-Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. Figures 4 and 5 show the timing for read and write cycles.

## Output Address Selection

In this mode $\overline{\mathrm{CS}}$ has to be low at least 50 nsec before the outputs will be valid. With R/C high, the row address latch
contents are transfered to the multiplexed address bus output Q0-Q8. $\overline{R A S I N}$ can go low after the row addresses have been set up on Q0-Q8, and enables one RAS output selected by signals B0, B1 to strobe the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/C can go low so that about 40 nsec later, the column address appears on the $Q$ output.

S409 INPUTS

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Figure 4. Read Cycle Timing (Mode 4)

## S409 INPUTS


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Figure 5. Write Cycle Timing (Mode 4)

## Automatic CAS Generation

In a normal memory access cycle $\overline{\mathrm{CAS}}$ can be derived from inputs $\overline{C A S I N}$ or $R / \bar{C}$. If CASIN is high, then $R / \bar{C}$ going low switches the address output drivers from rows to columns. CASIN then going low causes CAS to go low approximately 40 ns later, allowing $\overline{\text { CAS }}$ to occur at a predictable time (see Figure 5). For maximum system speed, CASIN can be kept low, since $\overline{\text { CAS }}$ will automatically occur approximately 60 ns after R/C goes low (see Figure 4). Most DRAMs have a column address set-up time before $\overline{C A S}$ ( $t$ ASC) of 0 ns or -10 ns . In other words, a tASC greater than 0 ns is safe. This
feature reduces timing-skew problems, thereby improving access time of the system.

## Fast Memory Access

For faster access time, R/C can go low a time delay (tRPDL $+t_{\text {RAH }}$ - tRHA) after RASIN goes low, where tRAH is the Row-Address hold-time of the DRAM, and CASIN can go low $t_{R C C}-\mathrm{t}_{\mathrm{C}} \mathrm{COL}+\mathrm{t}_{\mathrm{ASC}}$ (min.) after R/C goes low (see tDiF1, $t_{\text {DiF2 }}$ switching characteristics).

## Mode 1-Automatic Forced Refresh <br> Mode 5 -Automatic Access with Hidden Refresh

Mode 1 and Mode 5 are generally used together incorporating the advantages of the "hidden refresh" performed in mode 5 with the possibiity to force a refresh by changing to mode 1. An advantage of the Automatic Access over the Externally-Controlled Access is the reduced memory access time, due to the fact that the output control signals are derived internally from one input signal ( $\overline{\operatorname{RASIN}}$ ).

## Hidden and Forced Refresh

Hidden Refresh is a term describing memory refresh performed when the system does not access the portion of memory controlled by the $74 \mathrm{~S} 409(\overline{\mathrm{CS}}=1)$. A hidden refresh will occur once per Refresh Clock (RFCK) cycle provided $\overline{\mathrm{CS}}$ went high and RASIN went low. If no hidden refresh occurred while RFCK was high, the RF I/O ( $\overline{R F R Q}$ ) goes low immediately after RFCK goes low, indicating to the system when a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low by driving M2 ( $\overline{\mathrm{RFSH}}$ ) low, thereby changing mode of operation to Mode 1.
The Refresh Request on RF I/O ( $\overline{\mathrm{RFRQ}})$ is terminated as soon as RAS goes low, indicating to the system that the foced refresh has been done. The system should then drive M2 ( $\overline{\mathrm{RFSH}})$ high, changing the mode of operation back to Mode 5 (see Figure 6).

## Mode 1-Automatic Forced Refresh

In Mode 1, the R/C (RFCK) pin functions as RFCK (refresh cycle clock) instead of R/ $\bar{C}$, and $\overline{C A S}$ remains high. If RFCK is kept permanently high then whenever M2 ( $\overline{\mathrm{RFSH}}$ ) goes
low, an externally-controlled refresh will occur and all $\overline{R A S}$ outputs will follow $\overline{R A S I N}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but can be set low externally through an open-collector driver, to reset the refresh counter.
If RFCK is an input clock, one and only one refresh cycle must take place every RFCK cycle. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O (Refresh Request) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is required. The system must allow a forced refresh to take place while RFCK is low The Refresh Request signal on RF I/O may be connected to a Hold or Bus Request input to the system. The system acknowledges the Hold or Bus Request when ready, and outputs Hold Acknowledge or Bus Request Acknowledge. If this is connected to the M2 ( $\overline{\mathrm{RFSH}}$ ) pin, a forced-refresh cycle will be initiated by the S409, and RAS will be internally generated on all four RAS outputs, strobing the refresh counter contents on the address ouputs into all the DRAMs. An external $\overline{R A S}$ Generator Clock (RGCK) is requred for this function. It is fed to the $\overline{\text { CASIN }}$ (RGCK) pin, and may be up to 10 MHz . Whenever M 2 goes low (inducing a forced refresh), $\overline{\text { RAS }}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{\text { RAS }}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{R A S}$ going low, M2 should go low tRFSRG before the next falling edge of RGCK. The Refresh Request on RF I/O is terminated as RAS begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{R A S}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{\text { RAS }}$ end in less than 2 periods of RGCK from the time $\overline{R A S}$ went low, then M2 may go high earlier than tFRQH after RF I/O goes high and RAS will go high tRFRH after M2.

## Mode 5-Automatic Access with Hidden Refresh

In this mode all address outputs, $\overline{\mathrm{RAS}}$ and $\overline{\mathrm{CAS}}$ are initiated from $\overline{\text { RASIN }}$ making the DRAM access appear similar to static RAM access. The hidden refresh feature enables DRAM refresh accomplished with no time-loss to the system.
Provided the input address is valid as ADS goes low, $\overline{\text { RASIN }}$ can go low any time after ADS. This is because the selected RAS occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address Set-Up time (tASR), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and RASIN edges simultaneously applied) produces a minimum tASR of 0 ns . This is true provided the input address was valid tASR before ADS went low (see Figure 7).

Next, the row address is disabled tRAH after $\overline{R A S}$ goes low ( 30 ns minimum); in most DRAMs, trAH minimum is less than 30 ns . The column address is then set up and (tASC later,) CAS occurs. The only other control input required is WIN. When a write cycle is required, $\overline{\text { WIN }}$ must go low at least 30 ns before $\overline{\mathrm{CAS}}$ is output low.

This gives a total typical delay from: input address valid to
 umns valid ( 25 ns ); to $\overline{\mathrm{CAS}}(23 \mathrm{~ns})=140 \mathrm{~ns}$ (that is, 125 ns from RASIN). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

## Refreshing

In this mode R/C (RFCK) functions as Refresh Clock and $\overline{\text { CASIN (RGCK) functions as } \overline{\text { RAS }} \text { Generator Clock. }}$
One refresh cycle must occur during each refresh clock period, and then the refresh address must be incremented before the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every $16 \mu \mathrm{~s}$ ), all 16K and 64K DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than $16 \mu \mathrm{~s}$. RFCK going high sets an internal refresh-request flipflop. First the 74S409 will attempt to perform a hidden refresh so that the system thruput will not be affected. If, during the time RFCK
is high, $\overline{\mathrm{CS}}$ on the 745409 goes high and $\overline{\text { RASIN }}$ occurs, a hidden refresh will occur. In this case, $\overline{\text { RASIN }}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the 74S409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{\mathrm{CS}}$ goes high with RFCK high, and all $\overline{R A S}$ outputs follow $\overline{R A S I N}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flipflop is reset so on further refresh can occur until the next RFCK period starts with the posi-tive-going edge of RFCK (see Figure 6). $\overline{\text { RASIN }}$ should go low at least 20 ns before RFCK goes low, to ensure occurrence of the hidden refresh.

To determine the probability of a hidden refresh occurring, goes low, (and the internal-request flipflop has not been for $8 \mu \mathrm{~s}$, then the system has 20 chances to not select the 74 S 409 . If during this time a hidden refresh did not occur, then the 74 S 409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ( $\overline{\mathrm{RFSH}}$ ) low does the 74S409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 6. The internal refresh request flipflop is then reset.

Figure 6 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and CS again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic " 1 ") and the address outputs go three-state until CS again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50 percent; in fact, the low-time should be designed to be a minimum This is determined by the worst-case time (required by the system) to respond to the 74S409's forced-refresh request.


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Figure 7. Mode 5 Timing

## Mode 2-Automatic Burst Refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 8). When the 74 S 409 enters this mode, $\overline{\mathrm{CASIN}}$ (RGCK) becomes the $\overline{\text { RAS }}$ Generator Clock (RGCK), and RASIN is disabled. $\overline{\text { CAS }}$ remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last RAS has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four $\overline{\text { RAS }}$ outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, $\overline{R A S}$ is high and low for 200 ns each cycle. The refresh counter increments at the end of each $\overline{\mathrm{RAS}}$, starting from the count it contained when the mode was entered. If this was zero then for a RGCK with a 100 ns period with End-of Count set to 127 , RF I/O will go low after $128 \times 0.4 \mu \mathrm{~S}$, or $51.2 \mu \mathrm{~s}$. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the 74S409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-bust occurs (after $26 \mu \mathrm{~s}$ ), power can then be removed from the 74 S 409 for 2 ms , consuming an average power of $1.3 \%$ of normal operating power. No control signal glitches occur when switching power to the 74S409.

## Mode 3a-All-RAS Automatic Write

Mode 3 a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All $\overline{\mathrm{RAS}}$ outputs are activated, as in refresh, and so are $\overline{C A S}$ and $\overline{W E}$. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations. The refresh counter is used to address the rows, and $\overline{\mathrm{RAS}}$ is low for two RGCK cycles and high for two cycles.


Figure 8. Auto-Burst Mode, Mode 2

To select this mode, B1 and B0 must have previously been set to 00,01 , or 10 in Mode 7, depending on the DRAM size. For example, for 16K DRAMs, B1 and B0 are 00. For 64K DRAMs, B1 and B0 are 01.

In this mode, $R / \bar{C}$ is disabled, $\overline{W E}$ is permanently enabled low, and CASIN (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127,255 , or 511 (as set by End-of-Count in Mode 7), and the RAS outputs are active.




Figure 9. 74S409 All-RAS Auto Write Mode, Mode 3a, Timing Waveform

## Mode 3b - Externally-Controlled All-RAS Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four RAS outputs follow $\overline{R A S I N}$ (supplied by the processor), strobing the row address into the DRAMs. R/C can now go low, while $\overline{C A S I N}$ may be used to control $\overline{\text { CAS }}$ (as in the Externally-Controlled Access mode), so that $\overline{\mathrm{CAS}}$ strobes the column address contents into the DRAMs. At this time WE should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the 74S409 for the next write cycle. This method is slower than Mode 3a, since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

## Mode 4 - Externally-Controlled Access

Mode 4 is described in with mode 0 in section "Mode 0 and Mode 4.'

## Mode 5-Automatic Access with Hidden Refresh

See description of mode 0 and mode 5 .

## Mode 6-Fast Automatic Access

The Fast Automatic Access mode can only be used with fast DRAMs which have trAH of 10 nsec-15nsec. The typical $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ delay is 105 nsec . In this mode $\overline{\text { CAS }}$ can be extended after $\overline{R A S}$ goes high to extend the data output valid time. This feature is useful in applications with short cycles where $\overline{\mathrm{RAS}}$ has to be terminated as soon as possible to meet the precharge (t $\mathrm{t}_{\mathrm{RP}}$ ) requirements of the DRAM.
Mode 6 timing is illustrated in Figures 10 and 11. Provided that the input address is valid as ADS goes low, RASIN can go low any time after ADS. This is because the selected $\overline{\text { RAS }}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the 74S409. The Address

Set-Up time ( $t_{\text {ASR }}$ ), is 0 ns on most DRAMs. The 74S409 in this mode (with ADS and RASIN edges simultaneously applied) produces a minimum taSR of 0 ns . This is true provided the input address was valid tASA before ADS went low (see Figure 10).

Next, the row address is disabled tRAH after RAS goes low ( 20 ns minimum); the column address is then set up and tASC later, CAS occurs. The only other control input required is $\overline{\text { WIN. When a write cycle is required, WIN must go low at }}$ least 30 ns before CAS is output low.
This gives a total typical delay from: input address valid to $\overline{\text { RASIN }}$ ( 15 ns ); to $\overline{\text { RAS }}$ ( 27 ns ): to rows valid ( 50 ns ); to columns valid ( 25 ns ); to $\overline{\mathrm{CAS}}(23 \mathrm{~ns})=140 \mathrm{~ns}$ (that is, 125 ns from RASIN). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.
This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is RASIN.
In this mode, the R/C (RFCK) pin is not used, but CASIN (RGCK) is used as CASIN to allow an extended CAS after $\overline{\text { RAS }}$ has already terminated. Refer to Figure 11.

## Mode 7 - Set End-of-Count (3a, 3b select)

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and BO (see Table 3). With B1 and B0 the same EOC is 127; with B1 $=0$ and $B 0=1, E O C$ is 255 ; and with $B 1=1$ and $B O=0$, $\overline{E O C}$ is 511 . This selected value of $\overline{E O C}$ will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 ( $B 1$ and $B 0$ set to 11).

When $B_{1}, B_{2}$ are set to 11 in mode 7 , mode $3 b$ will be selected if mode 3 is selected $\left(M_{2}, M_{1}, M_{0}=0,1,1\right)$. If $B_{1}, B_{2}$ is set to 00,01 or 10 then mode 3 a will be selected.

| BANK SELECT <br> (STROBED BY ADS) |  | END OF COUNT <br> SELECTED |
| :---: | :---: | :---: |
| B1 | B0 |  |
| 0 | 0 | 127 |
| 0 | 1 | 255 |
| 1 | 0 | 511 |
| 1 | 1 | 127 |

Table 3. Mode 7


Figure 10. Mode 6 Timing (CASIN High)

*INDICATES DYNAMIC RAM PARAMETERS

Figure 11. Mode 6 Timing, Extended CAS

## SN74S409/-2 Specifications:

## Absolute Maximum Ratings (Note 1)


Storage temperature range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $65^{\circ}$ to $+150^{\circ} \mathrm{C}$
Input voltage
-1.5 V to 5.5 V
Output current . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 150 mA
Lead temperature (soldering, 10 seconds) . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . $300^{\circ} \mathrm{C}$
NOTE 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of operating conditions provides conditions for actual device operation.

## Operating Conditions

| SYMBOL | PARAMETER | FIGURE | MIN | $\begin{aligned} & \text { 'S409 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \text { S409-2 } \\ & \text { TYP MAX } \end{aligned}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 |  | 5.25 | 4.75 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 75 | 0 | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{\text {ASA }}$ | Address setup time to ADS | Figures 4, 5, 7, 10, 11 | 15 |  |  | 15 |  | ns |
| taHA | Address hold time from ADS | Figures 4, 5, 7, 10, 11 | 15 |  |  | 15 |  | ns |
| taDS | Address strobe pulse width | Figures 4, 5, 7, 10, 11 | 30 |  |  | 30 |  | ns |
| $t_{\text {RASINL, }}$ | Pulse width of RASIN during refresh | Figure 3 | 50 |  |  | 50 |  | ns |
| $t_{\text {RST }}$ | Counter reset pulse width | Figure 3 | 70 |  |  | 70 |  | ns |
| trFCKL, H | Minimum pulse width of RFCK | Figure 6 | 100 |  |  | 100 |  | ns |
| T | Period of $\overline{\mathrm{RAS}}$ generator clock | Figure 6 | 100 |  |  | 100 |  | ns |
| trGCKL | Minimum pulse width low of RGCK | Figure 6 | 35 |  |  | 35 |  | ns |
| $t_{\text {RGCKH }}$ | Minimum pulse width high of RGCK | Figure 6 | 35 |  |  | 35 |  | ns |
| tCSRL | $\overline{\mathrm{CS}}$ low to access $\overline{\mathrm{RASIN}}$ low | See Mode 5 description | 10 |  |  | 10 |  | ns |
| trFSRG | $\overline{\text { RFSH }}$ low set-up to RGCK low (Mode 1) | See Mode 1 description | 35 |  |  | 35 |  | ns |
| tRQHRF | $\overline{\mathrm{RFSH}}$ hold time from $\overline{\mathrm{RFRQ}}$ (RF 1/O) | Figure 6 | 2 T |  |  | 2T |  | ns |

Electrical Characteristics: $V_{C C}=5.0 \mathrm{~V} \pm 5.0 \%, 0^{\circ} \mathrm{C} \leq T_{A} \leq 75^{\circ} \mathrm{C}$ Typicals are for $\mathrm{V}_{\mathrm{C}} \mathrm{C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{C}}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{IC}=-12 \mathrm{~mA}$ |  | -0.8 | -1.2 | V |
| l/H1 | Input high current for ADS, R/C only | V IN $=2.5 \mathrm{~V}$ |  | 2.0 | 100 | $\mu \mathrm{A}$ |
| I/H2 | Input high current for other inputs, except RF I/O | V IN $=2.5 \mathrm{~V}$ |  | 1.0 | 50 | $\mu \mathrm{A}$ |
| I\|RSI | Output load current for RF I/O | $\mathrm{V}_{\text {IN }}=0.5 \mathrm{~V}$, output high |  | -1.5 | -2.5 | mAV |
| I/CTL | Output load current for RAS, CAS, WE | $\mathrm{VIN}=0.5 \mathrm{~V}$, chip deselct |  | -1.5 | -2.5 | mA |
| IIL1 | Input low current for ADS, R/C only | $\mathrm{VIN}=0.5 \mathrm{~V}$ |  | -0.1 | -1.0 | mA |
| IIL2 | Input low current for other inputs, except RF I/O | V IN $=0.5 \mathrm{~V}$ |  | -0.05 | -0.5 | mA |
| VIL** | Input low threshold |  |  |  | 0.8 | V |
| $\mathrm{VIH}^{* *}$ | Input high threshold |  | 2.0 |  |  | V |
| VOL1 | Output low voltage, except RF I/O | $\mathrm{IOL}=20 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| VOL2 | Output low voltage for RF I/O | $\mathrm{IOL}=10 \mathrm{~mA}$ |  | 0.3 | 0.5 | V |
| VOH 1 | Output high voltage, except RF I/O | ${ }^{1} \mathrm{OH}=-1 \mathrm{~mA}$ | 2.4 | 3.5 |  | V |
| $\mathrm{VOH}_{2}$ | Output high voltage for RF I/O | $\mathrm{IOH}=-100 \mu \mathrm{~A}$ | 2.4 | 3.5 |  | V |
| 11 D | Output high drive current, except RF I/O | VOUT $=0.8 \mathrm{~V}$ ( Note 3) |  | -200 |  | mA |
| IOD | Output low drive current, except RF I/O | $\mathrm{V}_{\text {OUT }}=2.7 \mathrm{~V}$ ( Note 3) |  | 200 |  | mA |
| IOZ | Three-state output current (address outputs) | $\begin{aligned} & 0.4 \mathrm{~V} \leq \mathrm{VOUT} \leq 2.7 \mathrm{~V}, \\ & \mathrm{CS}=2.0 \mathrm{~V}, \text { Mode } 4 \end{aligned}$ | -50 | 1.0 | 50 | $\mu \mathrm{A}$ |
| ICC | Supply current | $\mathrm{V}_{C C}=\mathrm{MAX}$ |  | 250 | 325 | mA |
| CIN | Input capacitance ADS, R/C | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 8 |  | pF |
| CIN | Input capacitance all other inputs | $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ |  | 5 |  | pF |

[^48]Switching Characteristics: $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 5.0 \%, 0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq 75^{\circ} \mathrm{C}$ See Figure 12 for test load (switches S1 and $\mathbf{S 2}$ are closed unless otherwise specified) typicals are for $\mathrm{VCC}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

| SYMBOL | ACCESS PARAMETER | FIGURE | MIN | $\begin{aligned} & \text { S409 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \text { S409- } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| trHA | Row address held from column select | Figure 4 | 10 |  |  | 10 |  |  | ns |
| tricl | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 5) | Figures 7, 10 | 95 | 125 | 160 | 75 | 100 | 130 | ns |
| tricl | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 6) | Figures 7, 10, 11 | 80 | 105 | 140 | 65 | 90 | 115 | ns |
| $\mathrm{t}_{\text {RICH }}$ | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 5) | Figures 7, 10 | 50 | 63 | 80 | 50 | 63 | 80 | ns |
| $t_{\text {RICH }}$ | $\overline{\text { RASIN }}$ to $\overline{\text { CAS }}$ output delay (Mode 6) | Figures 7, 10, 11 | 40 | 48 | 60 | 40 | 48 | 60 | ns |
| $\mathrm{t}_{\mathrm{RCDL}}$ | $\overline{\text { RAS }}$ to CAS output delay (Mode 5) | Figures 7, 10 |  | 98 | 125 |  | 75 | 100 | ns |
| $\mathrm{t}_{\mathrm{RCDL}}$ | $\overline{\text { RAS }}$ to $\overline{\text { CAS }}$ output delay (Mode 6) | Figures 7, 10, 11 |  | 78 | 105 |  | 65 | 85 | ns |
| $\mathrm{t}_{\mathrm{RCDH}}$ | $\overline{\text { RAS }}$ to $\overline{\text { CAS }}$ output delay (Mode 5) | Figures 7, 10 |  | 27 | 40 |  | 27 | 40 | ns |
| $\mathrm{t}_{\mathrm{RCDH}}$ | $\overline{\text { RAS }}$ to CAS output delay (Mode 6) | Figures 7, 10 |  | 40 | 65 |  | 40 | 65 | ns |
| ${ }^{\text {t }} \mathrm{CCDH}$ | $\overline{\text { CASIN }}$ to $\overline{\mathrm{CAS}}$ output delay Mode 6) | Figure 11 | 40 | 54 | 70 | 40 | 54 | 70 | ns |
| trev | RASIN to column address valid (Mode 5) | Figures 7, 10 |  | 90 | 120 |  | 80 | 105 | ns |
| trev | $\overline{\text { RASIN }}$ to column address valid (Mode 6) | Figures 7, 10, 11 |  | 75 | 105 |  | 70 | 90 | ns |
| $t_{\text {RPDL }}$ | $\overline{\text { RASIN }}$ to RAS delay | Figures 4,5, 7, 10, 11 | 20 | 27 | 35 | 20 | 27 | 35 | ns |
| trPDH | $\overline{\text { RASIN }}$ to RAS delay | Figures 4, 5, 7, 10, 11 | 15 | 23 | 32 | 15 | 23 | 32 | ns |
| $\mathrm{t}_{\mathrm{APDL}}$ | Address input to output low delay | Figures 4, 5, 7, 10, 11 |  | 25 | 40 |  | 25 | 40 | ns |
| ${ }^{\text {taPDH }}$ | Address input to output high delay | Figures 4,5, 7, 10, 11 |  | 25 | 40 |  | 25 | 40 | ns |
| tSPDL | Address strobe to address output low | Figures 4,5 |  | 40 | 60 |  | 40 | 60 | ns |
| tSPDH | Address strobe to address output high | Figures 4,5 |  | 40 | 60 |  | 40 | 60 | ns |
| tWPDL | $\overline{\text { WIN }}$ to WE output delay | Figure 5 | 15 | 25 | 30 | 15 | 25 | 30 | ns |
| tWPDH | $\overline{\text { WIN }}$ to WE output delay | Figure 5 | 15 | 30 | 60 | 15 | 30 | 60 | ns |
| tCRS | $\overline{\text { CASIN }}$ setup time to $\overline{\text { RASIN }}$ high (Mode 6) | Figure 11 | 35 |  |  | 35 |  |  | ns |
| ${ }^{\text {t CPPL }}$ | $\overline{\text { CASIN }}$ to CAS delay (R/C low in Mode 4) | Figure 5 | 32 | 41 | 58 | 32 | 41 | 58 | ns |
| tCPDH | $\overline{\text { CASIN }}$ to CAS delay | Figure 5 | 25 | 39 | 50 | 25 | 39 | 50 | ns |
| trce | Column select to column address valid | Figure 4 |  | 40 | 58 |  | 40 | 58 | ns |
| trcR | Row select to row address valid | Figures 4,5 |  | 40 | 58 |  | 40 | 58 | ns |
| traH | Row address hold time (Mode 5) | Figures 7, 10 | 30 |  |  | 20 |  |  | ns |
| traH | Row address hold time (Mode 6) | Figures 7, 10, 11 | 20 |  |  | 12 |  | M | ns |
| tasc | Column address setup time (Mode 5) | Figures 7, 10 | 8 |  |  | 3 |  |  | ns |
| tASC | Column address setup time (Mode 6) | Figures 7, 10, 11 | 6 | 8 |  | 3 |  |  | ns |
| t DiF1 | Maximum (tRPDL - trHA) (Mode 4) |  |  |  | 15 |  |  | 15 | ns |
| t ${ }_{\text {DiF2 }}$ | Maximum (tRCC - tcPDL) (Mode 4) |  |  |  | 15 |  |  | 15 | ns |


| SYMBOL | REFRESH PARAMETER | TEST CONDITIONS | MIN | $\begin{aligned} & \text { S409 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \text { S409-2 } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{t}_{\mathrm{FRRQ}}$ | RFCK low to forced $\overline{\text { RFRQ low }}$ | $C_{L}=50 \mathrm{pF}$, Figure 6 |  | 20 | 30 |  | 20 | 30 | ns |
| $\mathrm{t}_{\mathrm{FRRQH}}$ | RGCK low to force $\overline{R F R Q}$ high | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$, Figure 6 |  | 50 | 75 |  | 50 | 75 | ns |
| trgRL | RGCK low to RAS low | Figure 6 | 50 | 65 | 95 | 50 | 65 | 95 | ns |
| trGRH | RGCK low to RAS high | Figure 6 | 40 | 60 | 85 | 40 | 60 | 85 | ns |
| $t_{\text {RFRH }}$ | $\overline{\text { RFSH }}$ high to $\overline{\mathrm{RAS}}$ high (encoding forced RFSH) | See Mode 1 description | 55 | 80 | 110 | 55 | 80 | 110 | ns |
| ${ }^{\text {t }}$ CSCT | $\overline{\text { CS }}$ high to $\overline{\mathrm{RFSH}}$ counter valid | Figure 6 |  | 55 | 70 |  | 55 | 70 | ns |
| tcti | RF I/O low to counter outputs all low | Figure 3 |  |  | 100 |  |  | 100 | ns |
| $\mathrm{t}_{\text {RFPDL }}$ | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ delay during refresh | Figures 3, 6 | 35 | 50 | 70 | 35 | 50 | 70 | ns |
| trapdr | $\overline{\text { RASIN }}$ to $\overline{\text { RAS }}$ delay during refresh | Figures 3, 6 | 30 | 40 | 55 | 30 | 40 | 55 | ns |
| trflct | RFSH low to counter address valid | $\overline{\mathrm{CS}}=\mathrm{X}$, Figures $3,6,8$ |  | 47 | 60 |  | 47 | 60 | ns |
| trFHRV | RFSH high to row address valid | Figures 3, 6 |  | 45 | 60 |  | 45 | 60 | ns |
| trohnc | $\overline{\text { RAS }}$ high to new count valid | Figures 3, 8 |  | 30 | 55 |  | 30 | 55 | ns |
| trLEOC | RASIN low to end-of-count low | $C_{L}=50 \mathrm{pF}$, Figure 3 |  |  | 80 |  |  | 80 | ns |
| trHEOC | RASIN high to end-of-count high | $C_{L}=50 \mathrm{pF}$, Figure 3 |  |  | 80 |  |  | 80 | ns |
| trGEOB | RGCK low to end-of-burst low | $C_{L}=50 \mathrm{pF}$, Figure 8 |  |  | 95 |  |  | 95 | ns |
| ${ }^{\text {tMCEOB }}$ | Mode change to end-of-burst high | $C_{L}=50 \mathrm{pF}$, Figure 8 |  |  | 75 |  |  | 75 | ns |

Switching Characteristics: (Contd)

| SYMBOL | ACCESS PARAMETER | TEST CONDITIONS | MIN | $\begin{aligned} & \text { 'S409 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{gathered} \text { S409-2 } \\ \text { TYP } \end{gathered}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | THREE-STATE PARAMETER |  |  |  |  |  |  |  |  |
| ${ }^{\text {t }} \mathrm{H}$ | $\overline{\mathrm{CS}}$ low to address output high from Hi | Figures 6, 12 $\mathrm{R} 1=3.5 \mathrm{k}, \mathrm{R} 2=1.5 \mathrm{k}$ |  | 35 | 60 |  | 35 | 60 | ns |
| ${ }_{\text {thz }}$ | $\overline{\mathrm{CS}}$ high to address output $\mathrm{Hi}-\mathrm{Z}$ from high | $\begin{aligned} & C_{L}=15 \mathrm{pF}, \text { Figures } 6,12 \\ & R 2=1 \mathrm{k}, \mathrm{~S} 1 \text { Open } \\ & \hline \end{aligned}$ |  | 20 | 40 |  | 20 | 40 | ns |
| t ZL | $\overline{\mathrm{CS}}$ low to address output low from $\mathrm{Hi}-\mathrm{Z}$ | Figures 6, 12 $\mathrm{R} 1=3.5 \mathrm{k}, \mathrm{R} 2=1.5 \mathrm{k}$ |  | 35 | 60 |  | 35 | 60 | ns |
| tLZ | $\overline{\mathrm{CS}}$ high to address output $\mathrm{Hi}-\mathrm{Z}$ from low | $\begin{aligned} & C_{L}=15 \mathrm{pF}, \text { Figures } 6,13 \\ & R_{1}=1 \mathrm{k}, \mathrm{~S} 2 \text { Open } \\ & \hline \end{aligned}$ |  | 25 | 50 |  | 25 | 50 | ns |
| thzH | $\overline{\mathrm{CS}}$ low to control output ( $\overline{\mathrm{WE}}, \overline{\mathrm{CAS}}$, (RASO-3) high from Hi-Z high | Figures 6,12 R2 $=750$, S1 open |  | 50 | 80 |  | 50 | 80 | ns |
| thHz | $\overline{\mathrm{CS}}$ high to control output ( $\overline{\mathrm{WE}}, \overline{\mathrm{CAS}}$, (RASO-3) Hi-Z high from high | $\begin{aligned} & C_{L}=15 \mathrm{pF} \\ & R 2=750 \Omega, \text { S1 open } \end{aligned}$ |  | 40 | 75 |  | 40 | 75 | ns |
| thzL | $\overline{\mathrm{CS}}$ low to control output ( $\overline{\mathrm{WE}}, \overline{\mathrm{CAS}}$, (RASO-3) low from Hi-Z high | Figure 12 S1, S2 Open |  | 45 | 75 |  | 45 | 75 | ns |
| tLHZ | $\overline{\mathrm{CS}}$ high to control output ( $\overline{\mathrm{WE}}, \overline{\mathrm{CAS}}$, (RASO-3) Hi-Z high from low | $\begin{aligned} & C_{L}=15 \mathrm{pF}, \text { Figure } 12 \\ & \mathrm{R} 2=750 \Omega, \mathrm{~S} 1 \text { open } \end{aligned}$ |  | 50 | 80 |  | 50 | 80 | ns |

*Internally the device contains a 3 K resistor in series with a Schottky Diode to $V_{\mathrm{CC}}$.
Note 1: Output load capacitance is typical for 4 banks of 22 DRAMs or 88 DRAMs including trace capacitance. These values are: Q0-Q8. $\mathrm{C}_{\mathrm{L}}=500 \mathrm{pF}$; RAS0-RAS3, $C_{L}=150 p F ; C A S C_{L}=600 \mathrm{pF}$ unless otherwise noted.
Note 2: All typical values are for $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ and $\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}$.
Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter In testing these parameters, a $15 \Omega$ resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.
Note 4: Input pulse OV to $3.0 \mathrm{~V}, \mathrm{t}_{\mathrm{R}}=\mathrm{t}_{\mathrm{F}}=2.5 \mathrm{~ns}, \mathrm{f}=2.5 \mathrm{MHz} . \mathrm{t}_{\mathrm{PW}}=200 \mathrm{~ns}$. Input reference point on AC measurements is 1.5 V . Output reference points are 2.7 V for High and $0: 8 \mathrm{~V}$ for Low.
Test Load

ns


Figure 13. Change in Propagation Delay vs Loading Capacitance Relative to a $\mathbf{5 0 0}$ pF Load


Figure 12. Waveform

## Applications

The 74S409 Dynamic RAM Controller provides all the address and control signals necessary to access and refresh dynamic RAMs. Since the 74S409 is not compatible with a specific bus or microprocessor, an interface is often necessary between the 74S409 and the system. A general application using PAL to implement the interface and two additional
chips to provide refresh clock and chip select is shown in Figure 14.

The 74S409 operating modes may vary from application to application. For efficient refresh it is recommended to use mode 1 and mode 5 to take advantage of the hidden (transparent) refresh with forced refresh backup.


Figure 14. 74S409 in General Application


| Introduction | 1 |
| :---: | :---: |
| Military Products Division | 2 |
| PROM | 3 |
| PLE ${ }^{\text {m }}$ Devices | 4 |
| PAL ${ }^{\text {® }}$ Devices | 5 |

## System Building Blocks/HMST ${ }^{\text {w }}$



Representatives/Distributors 19

## ARITHMETIC ELEMENTS AND LOGIC

SN74S381 Arithmetic Logic Unit/Function Generator ... 10-3

## Features/Benefits

- A fully parallel 4-bit ALU
- Ideally suited for high-speed processors
- Generate and propagate outputs for full carry lookahead
- Three arithmetic functions
- Three logic functions
- Preset and clear functions


## Description

The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4 -bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full lookahead carry circuit is provided for fast, simultaneous carry generation by means of two cascaded outputs (Pand G) for the four bits in the package.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN74S381 | $\mathrm{N}, \mathrm{J}$ | Commercial |

## Pin Configuration



## Function Table

| SELECTION |  |  | ARITHMETIC/LOGIC OPERATION |
| :---: | :---: | :---: | :---: |
| 52 | S1 | So |  |
| L | L | L | Clear $\dagger$ |
| L | $L$ | H | B minus A |
| L | H | L | A minus $B$ |
| L | H | H | A plus B |
| H | L | L | $A \oplus B$ |
| H | L | H | $A+B$ |
| H | H | L | $A B$ |
| H | H | H | Preset $\dagger \dagger$ |

$\dagger$ Force all F outputs to be Lows.
$\dagger \dagger$ Force all F outputs to be Highs.

Logic Diagram


Function Table

|  | INPUTS |  |  |  |  |  |  |  |  |  |  |  | OUTPUTS |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FUNCTION | S2 | S1 | so | Cn | A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | F3 | F2 | F1 | F0 | $\overline{\mathbf{G}}$ | $\bar{p}$ |
| Clear | 0 | 0 | 0 | X | X | X | X | X | X | X | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| B minus A (Inverse Subtraction) | 0 | 0 | 1 | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ |
| A minus B (Subtract) | 0 | 1 | 0 | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \end{aligned}$ |
| A plus B (Add) | 0 | 1 | 1 | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | 0 1 0 1 0 1 0 1 | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & \hline 0 \\ & 1 \\ & 1 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 0 \\ & 1 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ & 0 \\ & 0 \\ & 0 \end{aligned}$ |

## Function Table

|  | INPUTS |  |  |  |  |  |  |  |  |  |  |  | OUTPUTS |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FUNCTION | S2 | S1 | So | Cn | A3 | A2 | A1 | A0 | B3 | B2 | B1 | B0 | F3 | F2 | F1 | FO |
| $\begin{aligned} & A \biguplus B \\ & (\mathrm{OR}) \end{aligned}$ | 1 | 0 | 0 | $\begin{aligned} & \mathrm{x} \\ & \mathrm{x} \\ & \mathrm{X} \\ & \mathrm{X} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 0 \end{aligned}$ |
| $\begin{aligned} & A \oplus B \\ & \text { (XOR) } \end{aligned}$ | 1 | 0 | 1 | $\begin{aligned} & \mathrm{X} \\ & \mathrm{x} \\ & \mathrm{X} \\ & \mathrm{X} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |
| $\begin{aligned} & A \bullet B \\ & (A N D) \end{aligned}$ | 1 | 1 | 0 | $\begin{aligned} & \mathrm{X} \\ & \mathrm{X} \\ & \mathrm{X} \\ & \mathrm{X} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 0 \\ & 1 \end{aligned}$ |
| Preset | 1 | 1 | 1 | $\begin{aligned} & \mathrm{x} \\ & \mathrm{x} \\ & \mathrm{x} \\ & \mathrm{x} \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 0 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 0 \\ & 1 \\ & 0 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ | $\begin{aligned} & 1 \\ & 1 \\ & 1 \\ & 1 \end{aligned}$ |

[^49]
## Absolute Maximum Ratings



## Operating Conditions



## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~m}$ |  |  |  | -1.2 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $V_{1}=0.5 \mathrm{~V}$ | Any S input |  |  | -2 | mA |
|  |  |  |  | Cn |  |  | -8 |  |
|  |  |  |  | All others |  |  | -6 |  |
| ${ }^{\prime} \mathrm{IH}$ | High-level input current | $V_{C C C}=M A X$ | $V_{1}=2.7 \mathrm{~V}$ | Any S input |  |  | 50 | $\mu \mathrm{A}$ |
|  |  |  |  | Cn |  |  | 250 |  |
|  |  |  |  | All others |  |  | 200 |  |
| I | Maximum input current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-Level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =\mathrm{MIN} \\ \mathrm{~V}_{\mathrm{IL}} & =0.8 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{OL}}=20 \mathrm{~mA} \end{aligned}$ |  |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} \mathrm{V}_{\mathrm{CC}} & =\mathrm{MIN} \\ \mathrm{~V}_{\mathrm{IL}} & =0.8 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & \mathrm{v}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \mathrm{I}_{\mathrm{OH}}=-1 \mathrm{~mA} \end{aligned}$ |  | 2.7 | 3.4 |  | V |
| 'os | Output shortcircuit current* | $V_{C C}=M A X$ |  |  | -40 |  | -100 | mA |
| ${ }^{\text {I CC }}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | 10 |  | 160 | mA |

[^50]
## Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Interface Test Load/Waveforms) | FROM (INPUT) | $\begin{gathered} \text { TO } \\ \text { (OUTPUT) } \end{gathered}$ | $\begin{aligned} & \text { 74! } \\ & \text { TYP } \end{aligned}$ | 381 <br> MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $t_{p}$ | Propagation delay time | $C_{L}=15 \mathrm{pF}$ | C | Any F | 10 | 17 | ns |
| $t_{p}$ | Propagation delay time |  | Any A or B | $\overline{\mathrm{G}}$ | 12 | 20 | ns |
| $t_{p}$ | Propagation delay time |  | Any A ar B | $\bar{P}$ | 11 | 18 | ns |
| ${ }^{\text {P PLH }}$ | Propagation delay, low-to-high |  | Any A or B | Any F | 18 | 27 | ns |
| ${ }^{\text {tPHL }}$ | Propagation delay, high-to-low |  |  |  | 16 | 25 | ns |
| ${ }^{\text {t }}$ P | Propagation delay time |  | Any S | Any $\mathrm{F}, \overline{\mathrm{G}}, \overline{\mathrm{P}}$ | 18 | 30 | ns |

## Test Load



16-BIT ALU (USING 74S381)


MAXIMUM DELAY OF ADDITION/SUBTRACTION.

|  | $745381+74 S 182$ |
| :---: | :---: |
| $1-4$ bits | 27 ns |
| $5-16$ bits | 44 ns |
| $17-64$ bits | 64 ns |



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## Cray Multipliers

| DESCRIPTION | PART NUMBER | MAX DELAY | PINS |
| :--- | :---: | :---: | :---: |
| $8 \times 8$ Multiplier (latched) | SN74S557 | $60 \mathrm{~ns}\left(X_{i}, Y_{i}\right.$, to $\left.S_{15}\right)$ | 40 |
| $8 \times 8$ Multiplier | SN74S558 | 60 ns | 40 |
| $8 \times 8$ Multiplier | SN54S558 | 60 ns | 40 |
| $16 \times 16$ Multiplier | SN74S556 | $76 \mathrm{~ns}\left(X_{i}, Y_{i}\right.$ to $\left.S_{15-0}\right)$ | 84 |
|  |  | $90 \mathrm{~ns}\left(X_{i}, Y_{i}\right.$ to $\left.S_{31-16}\right)$ | 84 |

# Five New Ways to Go Forth and Multiply 

## Chuck Hastings

## Our Multiplier Population Explosion

Recently it has seemed as if every time you turned around Monolithic Memories was announcing another new multiplier. Want to catch your breath, and find out where each of these fits into the overall scheme of things? Read on.
Actually, there have been five new multipliers in all within the last three years, plus two which had previously been available for several years. In time order of introduction, these are:
$\left.\begin{array}{ll}\text { Parts No. } & \text { Description }{ }^{\text {A }} \\ 57 / 67558 & 150-\text { nsec } 8 \times 8 \text { Flow-Through Cray Multiplier }{ }^{\text {B }}\end{array}\right\}$

NOTES: A. Times are worst-case times for commercial-temperature-range parts.
B. Obsolete. 54/74S558 replaces these in both new and existing designs.

You will notice that the above parts fall into two categories: flow-through Cray multipliers, and bus-oriented sequential multiplier/dividers. Although all of these parts get referred to rather casually as "multipliers," there are major differences between the two general types; see Table 1 below.

## The Cray Multipliers

The essential idea of a Cray multiplier, as originally put together by Seymour Cray in the late 1950s with discrete logic at Control Data Corporation, is to wire up an array of full adders in the form of a binary-arithmetic-multiplication pencil-and-paper example. ${ }^{3}$ That is, everywhere that there is a " 1 " or a " 0 " in a longhand binary-multiplication example, the Cray type of multiplication uses a full adder. One may visualize a Cray multiplier functionally as a "diamond," as follows:


DOUBLE-LENGTH PRODUCT
Figure 1. Pencil-and-Paper Analogy to Cray-Multiplier Operation

|  | Flow-Through Cray Multiplier | Bus-Oriented Sequential Multiplier/Divider |
| :--- | :--- | :--- |
| Role in <br> System | Building-block role - as many as 34 parts used in one super- <br> minicomputer (NORD-500 from Norsk Data'). | Co-processor role - one, or occasionally two, parts used in <br> one microcomputer2. |
| Internal <br> Operation | Static arithmetic-logic network; multiplies without being <br> clocked', using eight bits of the multiplier at a time. | State machine; requires clocking to operate; contains edge- <br> triggered registers; sequenced by a state counter; multiplies <br> using two bits of the multiplier at a time |
| External | Controlled by several mode-control input signals. | Controlled by sequences of micro-opcodes which come from <br> a microprocessor, a registered PAL, or some other sequential- <br> control device. |
| Pantrol |  |  |

## Table 1. A comparison of the two types of Monolithic Memories Multipliers

Our 57/67558, introduced in the mid-1970s, was the original single-chip Cray multiplier. To achieve what was for that time very high performance for a Schottky-TTL-technology part, the internal design of the 57/67558 also exploited other speed-freak multiplication techniques such as Booth multiplication ${ }^{4}$ and Wallace-Tree addition ${ }^{5}$. All of these techniques achieve increased speed through extensive parallelism, and can be used at the system level as well as within LSI components. Subsequently, process improvements made it possible to offer a faster final-test option, the 57/67550-1, which attained a sales-volume level essentially equal to that of the original part.
About five years ago, AMD paid us the sincere compliment of second-sourcing these parts with the 75-nsec 25S558. Three years ago, we returned the compliment with the 60 -nsec 54/74S558. All of these '558 parts, and the 70-nsec 54/74F558 announced by Fairchild, are fully compatible drop-in equivalents except for the variations in logic delay.


When AMD introduced the 25S558, they introduced along with it the $80-$ nsec 25 S557, a "metal option" of the same basic design with "transparent" output latches to hold the double-length product. "Transparent" means that the latches go away when you don't want them there; a latch-control line like that of the $54 / 74 \mathrm{~S} 373$ controls whether these output latches store information, or simply behave as output buffers. Anyway, when we introduced our 54/74S558, we followed it within a few weeks with the 60-nsec $54 / 74$ S557, which is a much faster drop-in replacement for AMD's part. And subsequently, Fairchild has announced a 70-nsec 54/74F557.

Because AMD's 'S557 has the output latches implemented in TTL technology after the ECL-to-TTL converters, whereas our ' S 557 has them implemented in ECL technology before the conversion, the latches operate much faster in ours. Our ' S 557 is typically only about a nanosecond slower than our 'S558, whereas the logic-delay difference between AMD's two parts is considerably greater. Consequently, our margin of superiority over AMD for the 'S557 is even greater than for the 'S558.
More recentily, we introduced the $90-$ nsec ' S 556 , which is a $16 \times 16$ direct size-upgrade of the 'S557/8 architecture, with the addition of input latches. In a "pipelined" mode, an 'S556 can produce a new 32 -bit product every 75 nsec.
'S557/8 Cray multipliers come in a 40-pin dual-inline package, either ceramic or plastic. Worst-case power-supply current is 280 mA . The ' S 556 comes in your choice of an 84-pin LCC (Leadless Chip Carrier) or an 88-pin PGA (Pin-Grid Array) package. Worst-case power-supply current is $800 \mathrm{~mA}(900 \mathrm{~mA}$ over military temperature range). The data-bus outputs can sink up to $8 \mathrm{~mA} \mathrm{l}_{\mathrm{OL}}$, for all of these multipliers.

References 5 and 6 discuss technical approaches to using Cray multipliers in high-performance minicomputers. The 'S558, together with PROMs organized in a "Wallace-tree" configuration, can sail right along at the rate of four $56 \times 56$ multiplications every microsecond, on the basis of fixed-point arithmetic with no renormalization. (See table 7 on page 16 of reference 5; the multiplication time is 238 nsec for a "division step,"' which is a fixed-point multiplication, and 319 nsec for a floating-point multiplication where extra time is required for renormalization and correction of the exponent of the product.) 34 'S558s or 'S557s are required to perform this multiplication if the computer system architecture does not call for the computation of the least-significant half of the double-length product; 49 are required if it does.


The "local" architecture of the multiplier section of a digital system can take two rather different forms. A minicomputer ${ }^{5}$, which executes an unpredictable mixture of arithmetic and logical instructions one after the other, typically needs to be able to get the complete multiplication over and done with before going on to the next program step - which is probably not another multiplication. An array processor or digital correlator, however, tends to do very regular iterative computations; and the performance of such a system can often be greatly increased by a technique called "pipelining," in which the arithmetic unit consists of stages with registers or latches in between each stage, and partial computational results move from one stage to the next on each clock.

The "flow-through" architecture of the "S558 works equally well in synchronous or asynchronous pipelined systems, but registers or latches must be provided externally. The 'S557, however, is actually a superset of the 'S558, and the added internal-output-latch feature adapts it particularly well to pipelined systems. The 'S556 provides latches atboth ends.


Even a smaller-scale system can make effective use of these parts. To return to the case of $56 \times 56$ multiplication, which corresponds to the word-length needed for multiplying mantissas in several popular floating-point-number formats, an iterative clocked scheme using just seven $8 \times 8$ multipliers, some adders, and an accumulator register can form the entire 112-bit doublelength product in just seven multiply/add cycles. A number of mid-range minicomputers today multiply in this manner. The multipliers are configured as suggested by the following block diagram:


Figure 2. $8 \times 56$ Cray Multiplier In Diamond Representation
There is even an occasional 8 -bit or 16 -bit microprocessorbased system with a need for very fast multiplication, where 'S557/8s or 'S556s may get used as microprocessor peripher$\mathrm{als}^{7,8}$. Digital-video systems, in particular electronic games, with "vector graphic" capabilities are one example.

The world of 'S556/7/8 applications has turned out to include all sizes of minicomputers, digital video systems, and signal processors - FFT (Fast Fourier Transform) processors, voice recognition equipment, radar systems, digital correlators and filters, electronic seismographs, brain and body scanners, and so forth. And there are many unexpected off-beat applications, such as real-time data-rescaling circuits in instruments, altogether too numerous to list here. After all, an'S556 can multiply two 16-bit numbers together and output their entire 32-bit product in 90 nsec worst case... less time than it would take a speeding bullet to move the distance equal to the thickness of this piece of paper. How's that for Supermultiplier?

## The Multiplier/Dividers

The Monolithic Memories 'S516 and 'S508 are state-of-theart TTL-compatible intelligent peripherals for microprocessors, somewhere between arithmetic sequential circuits and specialized bipolar microprocessors. The 'S516 and 'S508 each can perform any of 28 different multiply and multiply-and-accumulate instructions, plus any of 13 different divide instructions, at bipolar speeds under the control of an internal state counter. (See Figure 2 of the 'S516 data sheet.) The state counter's sequence is in turn guided by 3-bit instruction codes which are external inputs to the 'S516/508. The ' S 516 computes with 16 -bit binary numbers, and the 'S508 computes with 8 -bit binary numbers, as the part numbers none-too-subtly imply.

A 16-bit bi-directional data bus connects the S 516 with the outside world for bringing in multipliers, multiplicands, dividends, and divisors; and returning products, quotients and remainders. It also has clock (CK) and run/wait (GO) inputs, and an overflow indication (OVR) output.

The 'S508 has all of the above inputs and outputs also, except that it has only an 8-bit bidirectional data bus. Since it comes in the same 24-pin package as the 'S516, it obviously has eight more pins available for other purposes. Four of these are used to bring out the internal-state-counter value; one each is used for a completion ( $\overline{\mathrm{DONE}}$ ) status output, an output-enable control (OE) input, and a masterreset $(\overline{\mathrm{MR}})$ control input; and one is not used at all.

A simple, general interfacing scheme can be used to team a 'S516 with any of the currently popular 16-bit microprocessors,or an ' S 508 with any 8-bit microprocessor. (See Figure 7 of the'S516 data sheet.) With a couple extra interface circuits, an'S516 can also be interfaced to an 8-bit microprocessor. Particularly if the system software is written in a highly-structured language such as PASCAL or FORTH, an'S516/508 can be retrofitted into an existing system with a large gain in performance and very little impact on either hardware or software - calls to the previous software-implemented one-step-at-a-time multiply and divide subroutines are simply rerouted to substitute a command from the microprocessor to the ' $\$ 516 / 508$ to accept an operand and start its operation sequence.

The 'S516 and 'S508 are in fact two different "metal options" of one basic design; the 'S516 has twice as many data bits in each internal register. The 'S516 and 'S508 both have a worst-case clock rate of 6 MHz (commercial) or 5 MHz (military); the typical rate is 8 MHz . The simplest complete twos-complement $16 \times 16$ multiplication instruction can be performed in nine clock cycles by an 'S516, or in five by an 'S508, since 2-bits-at-a-time Booth multiplication is used; ${ }^{4}$ thus, the worst-case time required by the ' S 516 to multiply in this mode is $1.5 \mu \mathrm{sec}$ for a commercial part, and for an ' S 508 it is 833 nsec . On the same basis, $32 / 16$ division can be done in 21 clock cycles, or $3.5 \mu \mathrm{sec}$ worst-case, by an 'S516; and 16/8 division can be done in 13 clock cycles, or $2.2 \mu \mathrm{sec}$ worst-case, by an 'S508.

An 'S516/508 can perform either positive or negative multiplication or multiply-accumulation, and many of the instructions provide for "chaining" of successive computations to eliminate extra operand transfers on the bus; these features further enhance the computational speed of the 'S516/508 in particular applications. Arithmetic can be either integer or fractional with respect to positioning of the results.

An 'S516 can powerfully enhance the capabilities of any present-day 16 -bit or 8 -bit microprocessor in a computebound application. In fact, it can be used in any digital system where there is a need to multiply and divide on a bus. An 'S508 can likewise enhance the capabilities of any 8-bit microprocessor.


The 'S516 comes in an industry-standard 600-mil 24-pin dual-inline package, modified to include an integral aluminum heatsink which does not add appreciably to the package height: It requires only +5 V and ground power connections, and draws a worst-case power-supply current of 450 mA (commercial) or 500 mA (military). Power consumption is greatest at cold temperatures, and decreases substantially as operating temperature increases. The 16 databus inputs require at most 0.25 mA input current; the other inputs require at most 1 mA . The 16 databus outputs can sink up to 8 mA lol. The 'S508 also fits the above description, except that its worst-case power-supply current is 380 mA (commercial) or 400 mA (military), and it has only 8 databus inputs and outputs.

In describing applications of these parts, it is difficult to know where to start - they can be used in almost any design where a microprocessor can be used, and you know how many places that is today. So, perhaps a good starting point is to see what uses customers have thought up all by themselves. One customer even used two " S 516 s in "pingpong" mode on a single 16 -bit bus! So, rather than merely speculating as to what these parts might be good for, here's a list of what Monolithic Memories's customers have already proven they are good for:

- Real-time control of heavy machinery ${ }^{9}$
- Low-cost, high-performance digital modems
- CRT graphics, including video games
- Military avionics
- Cartographic analysis

As it happens, the above are 'S516 applications, except that digital modem designs have been done with both the 'S516 and the 'S508. Several of the 'S516 designs are already in production. In each of these applications, the microprocessor could have coped all right with the computational complexity, albeit at its own less-than-tremendous speed, but a 'S516 used together with the microprocessor can provide extra muscle for handling formidable problems.


Competition? Well, since there are no second sources for the 'S516, and no competitor at present has a similar fast part capable of performing division as well as multiplication, right now the 'S516 has no direct competition. Indirectly, there are some competing parts which perform only multiplication, and would have to perform division by Newton-Raphson iteration to be usable for any application where division is required. However, the ' S 516 is (as far as we know) by far the lowest-
priced bipolar 16-bit multiplier, and the other microprocessor peripheral chips which can perform division as well as multiplication are relatively-slow MOS devices. In one case, an 8 -bit cascadable CMOS part requires a 50\% reduction in clock rate to do 16 -bit arithmetic. And considerable numer-ical-analysis and programming sophistication are required to implement Newton-Raphson division with fixed-point operands. (It's easier with floating-point operands.) In contrast, the ' $\mathrm{S} 516 / 508$ can be easily interfaced to almost any microprocessor using one or two PALs, ${ }^{\circledR}$ and can perform either multiplication or division on command?

The 'S516 is so much faster than the competing MOS chips that it can even take them on for floating-point computations (which some of them are designed to do) and win. A conference paper ${ }^{10}$ describes the design of an 'S516-based S-100-bus card capable of beating an Intel 8087 2:1 on floating-point arithmetic.

Some competing parts, in particular the AMI 2811 and Nippon Electric $\mu$ PD7720, include an on-board ROM which must be mask-programmed at the factory, which makes life difficult for small companies (or even larger ones) which are trying to get a microprocessor-based product to market quickly. Also, some competing parts require sequencing by external TTL jellybeans.

And, as for using AMD/TRW 64-pin 16x16 Cray multiplier chips as microprocessor peripherals, these cost much more than the 'S516, occupy about three times the circuit-board space, multiply faster, don't divide at all except by NewtonRaphson iteration, and also require one or two "overhead" microprocessor instructions to interface for a given arithmetic operation. From a system viewpoint, when this overhead time is reckoned with, these chips provide little actual gain in multiply performance over the 'S516 at lots of extra cost, and an actual loss in divide performance: the 'S516 is much more cost-effective overall.
'S516s potentially fit into many, many places in commercial, industrial, and military electronics, particularly into small-scale real-time systems. The part is fast enough to enhance the performance of a 16-bit Motorola 68000, Zilog Z8000, or Intel 8086, as well as that of any 8-bit microprocessor. It is also fast enough to considerably improve the multiplication and division performance of 16-bit 2901-based "bit-slice" bipolar microcomputers, which are often used as processors in desktop graphics CRT terminals.

It is worth bringing the 'S516 to the attention of any designer who is developing:

- A personal computer or small business computer.
- A word processor, or a more grandiose "office automation system:'
- A cruise missile, or any other "smart weapon."
- A digital modem.
- A small-scale speech-processing system. (These are very multiplication-intensive. We have one magazine article on the 'S516 in such an application.1')
- A smart instrument, which does data conversion.
- An industrial control system, particularly one which must do many coordinate transformations.
- An all-digital studio-quality high-fidelity system.
- A cost-reduced computerized medical scanning system.
- A multiprocessor system for scientific computations. ${ }^{12}$ )

If an ' $\mathrm{S} 516 / 508$ is introduced into a system configured around an older microprocessor as a "co-processor" or
helpmate for the microprocessor, and the application is arithmetic-intensive, the end effect can be a major upgrading of performance at the system level. ${ }^{2.7}$ Consequently, a major reason for designing these parts in is microprocessor life-cycle enhancement. In particular, many MOS microprocessors have single-length and double-length add and subtract instructions: but either they have no multiply or divide instructions at all, or else they perform their multiply and divide instructions so slowly as to jeopardize the ability of the entire system to handle its computing load in real time.

So picture, if you will, the entrepreneur or chief engineer of a firm making a successful microprocessor-based widget which has been on the market for a few months, which uses an older 8-bit microprocessor such as a 6800 or 8085 or Z80. Just when his/her sales are really taking off, here comes a new start-up competitor with a similar system, using a Motorola 68000, with added features and faster performance made possible by the 68000's 16 -bit word length and multiply/divide capabilities. The 'S516 can, in this instance, serve as a "great equalizer" - it can be retrofitted into the older system as previously described, and provides even higher-speed multiplication and division than the 68000. (Enough so, actually, that there are designers using the 'S516 with the 68000.) Thus, the 'S516 can dramatically extend the life cycle of existing microcomputer systems based on microprocessors which either don't have multiplication and division instructions, or perform these operations relatively slowly.

"... THE'S516 CAN DRAMATICALLY EXTEND THE LIFE CYCLE OF EXISTING MICROCOMPUTER SYSTEMS BASED ON MICROPROCESSORS WHICH EITHER DON'T HAVE MULTIPLICATION AND DIVISION INSTRUCTIONS, OR PERFORM THESE OPERATIONS RELATIVELY SLOWLY..."
'S508s are somewhat easier to control from a logic-design viewpoint than 'S516s, purely because they have more control inputs and outputs. However, the shorter 'S508 word length makes the part naturally fit into smaller-scale systems than those which might use an 'S516. Essentially, the 'S508 is optimized for small-scale systems.

Now that you know what these parts are, can't you think of at least half a dozen prime uses for them right in your own back yard?

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## $16 \times 16$ Multiplier/Divider SN74S516

## Features/Benefits

- Co-processor for enhancing the arithmetic speed of all present 16 -bit and 8 -bit microprocessors
- Bus-oriented organization
- 24-pin package
- 16/16 or $32 / 16$ division in less than $3.5 \mu \mathrm{sec}$
- $16 \times 16$ multiplication in less than $1.5 \mu \mathrm{sec}$
- 28 different multiplication instructions such as "fractional multiply and accumulate"
- 13 different divide instructions
- Seli-contained and microprogrammable


## Description

The SN74S516 ('S516) is a bus-organized $16 \times 16$ Multiplier/ Divider. The device provides both multiplication and division of 2 s -complement 16 -bit numbers at high speed. There are 28 different multiply options, including: positive and negative multiply, positive and negative accumulation, multiplication by a constant, and both single-length and double-length addition in conjunction with multiplication. 13 different divide options allow single-length or double-length division, division of a previouslygenerated result, division by a constant, and continued division of a remainder or quotient.

The 'S516 is a time-sequenced device requiring a single clock. It loads operands from, and presents results to, a bidirectional 16 -bit bus. Loading of the operands, reading of the results, and sequential control of the device is performed by a 3-bit instruction field.

The 'S516 has the additional feature that operands and results can be either integers or fractions; when it deals with fractions, automatic scaling occurs. Results can be rounded if required, and an Overflow output indicates whenever a result is outside the normally-accepted number range.

For a simple multiplication of two operands the device takes nine clock periods - one for initialization, and eight for the actual multiplication. A realistic clock period is 167 ns , which gives a multiplication time of 1333 ns typical for $16 \times 16$ multiplication, plus 167 ns additionally for initialization, or 1500 ns in all. More complex multiplications will take additional clock periods for loading the additional operands. A simple division operation requires $16+4=20$ clock periods for a typical time of 3.333 ns ( 32 bits/16 bits), also plus 167 ns for initialization, or 3500 ns in all.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN74S516 | $24 T$ | Commercial |

## Logic Symbol



## Pin Configuration



| INSTRUCTION SEQUENCE | OPERATION | CLOCK CYCLES |
| :---: | :---: | :---: |
| ARITHMETIC OPERATIONS |  |  |
| 0 | $X 1 \cdot Y$ | 9 |
| 1 | -X1 - Y | 9 |
| 2 | $X_{1} \cdot Y+K_{Z}, K_{W}$ | 9 |
| 3 | $-X_{1} \cdot Y+K_{z}, K_{w}$ | 9 |
|  | $\mathrm{K}_{\mathrm{z}}, \mathrm{K}_{\mathrm{w}} / \mathrm{X} 1$ | 21 |
| 5/6 | $X \cdot Y$ | 10 |
| 5/6 | -X $\cdot \mathrm{Y}$ | 10 |
| 5/6 | $X \cdot Y+K_{Z}, K_{W}$ | 10 |
| 5/6 | $-X \cdot Y+K_{Z}, K_{W}$ | 10 |
| 5/6 | $\mathrm{K}_{\mathrm{w}} / \mathrm{X}$ | 22 |
| 5/6 | $\mathrm{K}_{\mathrm{z}} / \mathrm{X}$ | 22 |
| 5/6 6 | $X \cdot Y+Z$ | 11 |
| $5 / 66$ | $-X \cdot Y+Z$ | 11 |
| $5 / 6 \quad 6$ | $X \cdot Y+K_{Z} \cdot 2^{-16}$ | 11 |
| $5 / 6 \quad 6$ | $-X \cdot Y+K_{Z} \cdot 2^{-16}$ | 11 |
| $5 / 6 \quad 6$ | $\mathrm{z}, \mathrm{W} / \mathrm{X}$ | 23 |
| $5 / 66$ | $Z / X$ | 23 |
| 5/6 666 | $X \cdot Y+Z, W$ | 12 |
| $5 / 6 \quad 6 \quad 6$ | $-X \cdot Y+Z, W$ | 12 |
| $5 / 6 \quad 6 \quad 6$ | $X \cdot Y+W_{\text {sign }}$ | 12 |
| $5 / 6 \quad 6 \quad 6$ | $-X \cdot Y+W_{\text {sign }}$ | 12 |
| $\begin{array}{llll}5 / 6 & 6\end{array}$ | W/X | 24 |
| $5 / 6 \quad 6 \quad 6$ | $\mathrm{W}_{\text {sign }} / \mathrm{X}$ | 24 |
| $5 / 666$ | (See Note 9 below.) | - |
| $5 / 6 \quad 6 \quad 6$ | Load X, Load Z, Load W, Clear Z | 4 |
| $5 / 6 \quad 6$ | Load X, Load Z, Read Z | 3 |
| READING OPERATIONS |  |  |
|  | Read Z | 1 |
| 7 | Read Z, W | 2 |
| 77 | Read Z, W, Z | 3 |
| $\begin{array}{lll}7 & 7\end{array}$ | Read Z, W, Z, W | 4 |
| 5 | Round, then Read $Z$ | 2 |
| 577 | Round, then Read Z, W | 3 |

## NOTES:

1. $X, Y$ are input multiplier and multiplicand.
2. $X 1$ is the previous contents of the first rank of the $X$ register (either the old $X$ or a new $X$ ).
3. Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with " $5 / 6$ " in effect represent two instructions. 5 does fractional arithmetic and 6 does integer arithmetic.
4. $Z, W$ is a double-precision number. $Z$ is the most significant half. $Z, W$ represents addend upon input, and product (or accumulated sum) after multiplication.
5. $\mathrm{K}_{\mathbf{Z}}, \mathrm{K}_{\mathbf{W}}$ represents previous accumulator contents. $\mathrm{K}_{\mathbf{Z}}$ is the most-significant half.
6. $W_{\text {sign }}$ is a single-length signed number, with sign extension.
7. Maximum clock cycle $=167 \mathrm{~ns}$ for an $6-\mathrm{MHz}$ clock.
8. If $n$ instruction codes are shown at the left under "instruction sequences," the number of clock cycles at the right is $n+8$ for multiplication and $n+20$ for division.
9. The code " $5 / 6666$ " represents an incomplete operation since it leaves the ' S 516 in state 1 rather than in state 0,8 , or 10.

Figure 1. 'S516 Instruction Set (Partial List)

| SUMMARY OF SIGNALS/PINS |  |
| :--- | :--- |
| $\mathrm{B}_{15}-\mathrm{B}_{0}$ | Bidirectional data bus inputs/outputs |
| $\mathrm{I}_{2} \mathrm{I}_{0}$ | Instruction (sequential control) input |
| CK | Clock pulse input |
| $\overline{\mathrm{GO}}$ | Chip activation input |
| OVR | Arithmetic overflow output |

## Description (continued)

The 'S516 device uses standard low-power Schottky technology, requires a single +5 V power supply, and is fully TTL compatible. Bus inputs require at most $250 \mu \mathrm{~A}$ input current, and control and clock inputs require at most 1 mA input current. Bus outputs are three-state, and are capable of sinking 8 mA at the low logic level. The ' S 516 is available in both commercial-temperature and military-temperature ranges, in a 600-mil 24-pin dual-in-line ceramic package.

## Device Operation

The 'S516 contains four 16 -bit working registers. $Y$ is the multiplier register; X is the multiplicand and divisor register; W is the least-significant half of a double-length accumulator, and holds the least-significant half of the product after a multiplication operation, or the remainder after a division operation; and $Z$ is the most-significant half of this same accumulator. In addition to these registers, there is a high-speed arithmetic unit which performs addition, subtraction, and shifting steps in order to accomplish the various arithmetic operations; a loading sequencer; and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period, under the control of this sequencer. The chip-activation signal $\overline{\mathrm{GO}}$ must be LOW in order to begin the loading process and continue to the next step in the loading operation. If $\overline{\mathrm{GO}}$ is continually held HIGH, the ' S 516 remains in a wait state with its outputs held in their high-impedance states, so that the other devices attached to the bus may drive it. In this condition, the ' $\$ 516$ does not respond to any codes on its instruction inputs; in effect, it does not "wake up" until $\overline{\mathrm{GO}}$ goes LOW. Also, $\overline{\mathrm{GO}}$ may change only when the clock input CK is HIGH. After all of the operands are loaded, the ' S 516 jumps to the multiply routine, or to the divide routine, and performs the required operations as indicated in Figure 1. After 9 clock periods for a simple multiply or 21 clock periods for a simple divide, for example, the result is placed on the bus in time sequence.


KEY:
The numbers inside the circles indicate the state of the 'S516 multiplier/divider. These states are represented by a four-bit state counter, where $A$ is the least-significant bit of this state counter and $D$ is the most-significant bit. (These four bits are not available externally on the ' S 516 .)
The next state of the 'S516 is a function of the present state and the instruction lines. For example if the ' S 516 is at state 0 and the instruction is $0,1,2$, or 3 , then the next state is state 4 (multiply instruction); if the instruction is 4 , the next state is state 5 (divide instruction); and so forth. The instructions which take the 'S516
from one state to another are indicated by the numbers written next to the state-transition path lines. "0123," for instance, implies that any of instructions $0,1,2$, or 3 will take the ' S 516 along the path marked "0123."
" $X$ " next to a path implies that the path will be followed regardless of the value of the instruction inputs at that time. In other words, for the purpose of state transitions, X means "don't care." There are cases, however, where the particular instruction used may affect when the contents of the registers are available on the bus - see Figures 9 and 10 for contrasting examples of how this effect operates.

Figure 2. Transition Diagram for the 'S516 Multiplier/Divider

Three instruction inputs $!_{2}, I_{1}, I_{0}$, which may change only when the clock input CK is HIGH , select the required function and drive the sequencer from state to state. Thus, the action of the multiplier/divider at any clock period is a function of the machine state and the state of the control inputs. Figure 2 shows the multiply/divide state table, and all possible operations. After a Read or Round operation, the machine is driven back to state 0 , and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulation of products, state 0 is bypassed, and loading of an operand or jumping to the next arithmetic operation occurs at the end of the
previous arithmetic operation - at state 8 for a multiplication instruction, or at state 10 for a division instruction.

Register $X$ is a dual-rank register, which allows the loading of an operand $X$ during the multiplication or division process. If the machine enters the loading sequence and a new $X$ operand has not been loaded, then the machine proceeds with the previouslyloaded X , denoted in this text as " X 1 ." This loading-whileprocessing capability allows a cycle to be saved during "chained" calculations, and also allows multiplication and division by a constant. (See Figure 13).

Figures 3 and 4 show the codes and durations for the 41 different possible arithmetic operations. These operations can be concatenated in strings to perform complicated 2 s -com-
plement arithmetic operations at high-speed. Rounding and reading of results can be performed after any operation. Figure 5 is a block diagram of the ' $\$ 51616 \times 16$ Multiplier/Divider.
(continued page after next)

TIME-SLOT


NOTES: 1) $X 1$ is the previous contents of the first rank of the $X$ register (either old $X$ or a new $X$ ).
2) $K_{Z} \cdot 2^{-16}$ is a single-length signed number comprising the most-significant half of the previous double-length product and here gets added in at the least-significant end of the new result.
3) $W_{\text {sign }}$ is a single-length signed number, with sign-extension as needed.
4) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with " $5 / 6$ " in effect represent two instructions. 5 does fractional arithmetic and 6 does integer arithmetic.

Figure 3. Multiplication Codes and Times for 16x16 Multiplication in the 'S516

TIME-SLOT


NOTES: 1) $X 1$ is the previous contents of the first rank of the $X$ register (either old $X$ or a new $X$ ).
2) Fractional division divides a 32 -bit $2 s$-complement number in 1 clock period less than integer division.
3) $W_{\text {sign }}$ is a single-length signed number, with sign-extension as needed.
4) Division operation $W_{\text {sign }} / X$ requires that the $Z$ register be initialized with all-zero contents at the time $Z$ is loaded.
5) Fractional or integer arithmetic is specified by having the next-to-the-last operand loaded using a 5 or 6 instruction respectively. All rows beginning with " $5 / 6$ " in effect represent two instructions, one of which does fractional arithmetic and one of which does integer arithmetic.

Figure 4. Division Codes and Times for 32/16 Division in 'S516


Figure 5. Internal Architecture of the 'S516

## Initialization

The 'S516 has no direct master reset input. However, initialization of the 'S516 can easily be performed by continually presenting instruction code 7 , which after a maximum of 21 clock periods forces the machine back to state 0 .

## Multiplication

The ' $\$ 516$ provides 2 s -complement 16 -bit multiplication, and can also accumulate previously-generated double-length products. No time penalty is incurred for accumulation, since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation, the device can add into a product either a single-length or a double-length number. It can also use a previously-loaded operand as a constant, so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive multiplications and negative multiplications, again without any speed penalty. This feature allows complex-arithmetic multiplications to be programmed with very little overhead. Another important feature is the ability to work with either fractions or integers.

## Division

The 'S516 also provides a range of division operations. A double-length number in $\mathrm{Z}, \mathrm{W}$ is divided by X ; the result Q is stored in $Z$, and the remainder R in W. Again all numbers are in the 2 s -complement number representation, with the most significant bit of an operand (whether single-length or doublelength) having a negative weight. In order to facilitate repeated division, with the multiple-length quotient always keeping the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible, and division and multiplication operations can be concatenated. For example, the operations $(A \times B) / C,(A+B) / C$ can easily be performed. The dividend can be any previously-generated result - product, quotient, or remainder; or it may be a double-length or singlelength signed operand.

## Reading Results

The result of an arithmetic operation, or of a string of operations, can be read onto the 16 -bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the $\overline{G O}$ signal be held LOW so that the information is read out onto the bidirectional bus, when code 7 is specified. (See Figure 6.) Since there is a double-length accumulator $\mathrm{Z}, \mathrm{W}$, reading can take two cycles. First, register $Z$ is read. After another clock has been received, if code 7 is still present, the least-significant half of the product from the $W$ register is placed on the bus, or likewise the remainder if a division operation had been performed.

If the 'S516 is instructed to perform a read operation during the loading sequence, then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Control read operations at state 0 just swap the contents of register $Z$ and $\mathbf{W}$.

## Integer and Fractional Arithmetic

The 'S516 can work with either fractional or integer number representations. When working with integers, all numbers are scaled from the least-significant end, and the least-significant bit
is assumed to have a weight of $2^{0}$. For integer multiplication, accumulation, and division, all numbers are scaled from this least-significant weight, and results are correct if interpreted in this manner. The double-length register $Z, W$ can therefore hold numbers in the range $-2^{31}$ to $+2^{31}-1$; the operands $X$ and $Y$, and single-length results, are in the range $-2^{15}$ to $+2^{15}-1$.

When working with fractions, the machine automatically performs scaling so that input operands and results have a consistent format. All numbers in the fractional representation are scaled from the most significant end, which has a weight of $-2^{0}$ (negative). The binary point is one place to the right of this mostsignificant bit, so that the next bit has a weight of $2^{-1}$. The double-length register $Z, W$ therefore holds numbers in the range -1 to $+1-2^{-31}$ and the operands $X$ and $Y$ and single-length results are in the range -1 to $+1-2^{15}$. Since automatic scaling occurs, the product of two numbers always has the leastsignificant bit as a 0 , unless an accumulation is performed with the least-significant bit being a 1 .

During a chain operation with the partial results not being read onto the bus, the ' $\$ 516$ will stay in either the fractional or integer mode. At the start of a sequence of operations, fractional or integer operation is designated by loading operands using instruction code 5 or instruction code 6 respectively.
Mixed fractional and integer arithmetic is also possible, by redefining the weight of the least-significant or most-significant bits. However, care must be exercised, due to the automatic scaling feature, when fractional arithmetic is programmed.

## Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation, but nothing in the ' $\mathbf{S} 516$ precludes forming a rounded result during integer arithmetic.

Rounding for multiplication provides the best single-length most-significant half of the product. Rounding occurs at the end of a multiplication, and is performed instead of a Load or Read operation when a code 5 is specified, instead of a code 7, to get from state 8 or state 10 back to state 0 . (See Figure 2; also, note that this mode of operation precludes "stealing" a cycle according to the method illustrated in Figure 9.) The ' S 516 looks at the most-significant bit of the least-significant half of the product $W_{15}$, and adds 1 to the most-significant half of the product at the least-significant end if $W_{15}$ is a 1 . After the operation, the ' S 516 is in state 0 , so that the rounded product can be read, and the W register is cleared.

Rounding for division is performed by forcing the leastsignificant bit of the quotient in $Z$ to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again, after rounding the ' S 516 goes to state 0 , so that a read operation can be performed, and the $W$ register is cleared.

## Overflow

The 'S516 has an overflow output OVR which is cleared prior to each operation, and is set during an operation if the product or quotient goes outside the normally-accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used: $(-1) \times(-1)=+1$, which cannot be held in the 'S516's internal registers. Overflow can more easily occur during either positive or negative accumulation of products. For fractional arithmetic, if the product or accumulation goes outside the range of -1 to $+1-2^{-31}$, then the overflow flipflop will be set.

The overflow flip-flop is enabled in state 8 for the multiply operation or in state 10 for a divide operation. It only gets reset when a transition to state 0 from states $0,3,8,10$ and 11 , when instruction 7 is being presented to the ' $\$ 516$.

Overflow may also occur during division if the quotient goes outside the generally-accepted number range of -1 to $+1-2^{-15}$ during fractional operation. This would occur if the divisor is less than the dividend, or equal to the dividend if a positive quotient is being generated. For integer arithmetic the numbers must be scaled by $2^{15}$.


Figure 6. 'S516 Internal Circuitry of "GO" Line and Three-State-Enable

During the states $0,1,3,8,10$ and 11 if the "GO" line ( $\overline{\mathrm{GO}}$ ) is held at logic HIGH then the machine will be in a wait state until $\overline{\mathrm{GO}}$ goes to logic LOW.


Figure 7. Interfacing the 'S516 to a Microprocessor

Figure 7 shows the block diagram of a microprocessor system with its arithmetic capabilities enhanced by the use of a 'S516 $16 \times 16$ multiplier/divider. The relatively small number of instruction lines (only 3) of the ' $\$ 516$ provides a unique way to control the multiplier/divider. As may be seen from Figure 7, these three instruction lines are assigned to the three leastsignificant bits (LSBs) of the address bus, while the remaining
address bits are decoded by a Programmable Array Logic (PAL®) circuit to determine when the multiplier/divider is selected. For example, suppose the ' $\$ 516$ is assigned address 100 ; then any address in the range of $100-107$ will enable the ' S 516 (i.e., the $\overline{\mathrm{GO}}$ line is LOW). Thus, if the address is 100 the ' S 516 instruction is 0 ; if the address is 106 the ' S 516 instruction is 6 ; and so forth.

## Data Formats

## Fractional Multiply

$X_{i}, \mathbf{Y}_{1}$ - Input, Multiplicand, Multipler

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

## $Z_{i}$ - MS Half Output Product

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

$\mathbf{W}_{\mathbf{i}}$ - LS Half Output Product*

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $2^{-16}$ | $2^{-17}$ | $2^{-18}$ | $2^{-19}$ | $2^{-20}$ | $2^{-21}$ | $2^{-22}$ | $2^{-23}$ | $2^{-24}$ | $2^{-25}$ | $2^{-26}$ | $2^{-27}$ | $2^{-28}$ | $2^{-29}$ | $2^{-30}$ | "0" |

*The least significant bit of $\mathrm{W}_{\mathrm{i}}$ is always a binary 0 due to normalization. Note that $-1 \mathrm{x}-1$ yields an overflow in fractional multiply.

## Integer Multiply

$X_{i}, Y_{1}$ - Input, Multiplicand, Multiplier

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

## $Z_{i}$ - MS Half Output Product

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{30}$ | $2^{29}$ | $2^{28}$ | $2^{27}$ | $2^{26}$ | $2^{25}$ | $2^{24}$ | $2^{23}$ | $2^{22}$ | $2^{21}$ | $2^{20}$ | $2^{19}$ | $2^{18}$ | $2^{17}$ | $2^{16}$ |

$\mathbf{W}_{\mathbf{i}}$ - LS Half Output Product**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

* The least significant bit of $W_{i}$ is a valid data bit. Note that $2^{-15} \times 2^{-15}$ yields $+2^{30}$ which can be represented in the output bits without overflowing.


## Fractional Divide

$Z_{i}$ - Input Dividend

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

## X - Input Divisor

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

## Z- Output Quotient

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

## W- Output Partial Remainder $\dagger$

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{-1}$ | $2^{-2}$ | $2^{-3}$ | $2^{-4}$ | $2^{-5}$ | $2^{-6}$ | $2^{-7}$ | $2^{-8}$ | $2^{-9}$ | $2^{-10}$ | $2^{-11}$ | $2^{-12}$ | $2^{-13}$ | $2^{-14}$ | $2^{-15}$ |

$\dagger$ Note that the partial remainder $\mathrm{R}=2^{-15}(\mathrm{~W})$

## Integer Divide Example (Z, W)/X

$Z_{i}$ - MSB Input Dividend

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{30}$ | $2^{29}$ | $2^{28}$ | $2^{27}$ | $2^{26}$ | $2^{25}$ | $2^{24}$ | $2^{23}$ | $2^{22}$ | $2^{21}$ | $2^{20}$ | $2^{19}$ | $2^{18}$ | $2^{17}$ | $2^{16}$ |

$W_{i}$ - LSB Input Dividend

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $2^{15}$ | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

## X - Input Divisor

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

## $Z_{i}$ - Output Quotient

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

## $\mathbf{W}_{\mathbf{i}}$ - Output Partial Remainder

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Sign | $2^{14}$ | $2^{13}$ | $2^{12}$ | $2^{11}$ | $2^{10}$ | $2^{9}$ | $2^{8}$ | $2^{7}$ | $2^{6}$ | $2^{5}$ | $2^{4}$ | $2^{3}$ | $2^{2}$ | $2^{1}$ | $2^{0}$ |

Absolute Maximum Ratings

Input voltage ..... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETERS | FIGURE | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | 0 |  | 45** | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {f MAX }}$ | Clock frequency | 8 | 6 |  |  | MHz |
| ${ }^{\text {t }}$ CWP | Positive clock pulse width | 8 | 70 |  |  | ns |
| ${ }^{t}$ CWN | Negative clock pulse width | 8 | 50 |  |  | ns |
| ${ }^{\text {t }}$ BS | Bus setup time for inputting data* | 8 | 50 |  |  | ns |
| ${ }^{\text {t }}$ B ${ }^{\text {d }}$ | Bus hold time for inputting data* | 8 | 35 |  |  | ns |
| t INSS | Instruction, GO setup time | 8 | 10 |  |  | ns |
| ${ }_{\text {I }}$ NSH | Instruction, GO hold time | 8 | 30 |  |  | ns |

** During operations when the bus is being used to input data.
** This device has a limited operating temperature range.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\text {CC }}=\mathrm{MIN} \quad \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=\operatorname{MAX} \quad V_{1}=0.5 \mathrm{~V}$ | $\mathrm{B}_{15} \mathrm{~B}_{0}$ |  |  | -250 | $\mu \mathrm{A}$ |
|  |  |  | All other inputs |  |  | -1 | mA |
| ${ }_{1} \mathrm{H}$ | High-level input current | $V_{C C}=$ MAX $V_{1}=2.4 \mathrm{~V}$ |  |  |  | 250 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=\mathrm{MAX} \quad \mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ IOL $=8 \mathrm{~mA}$ |  |  | 0.3 | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}$ |  | 2.4 |  |  | V |
| IOS | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX} \mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ |  | -10 |  | -90 | mA |
| ${ }^{\text {ICC }}$ | Supply current | $\mathrm{V}_{\text {CC }}=$ MAX |  |  | 370 | 450 $\dagger$ | mA |

* Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
$\dagger$ At cold temperatures see the "I CC vs Temperature" curves on the next page for more complete information. The typical values shown here are at 5.0 V .


## Switching Characterictics Over Operating Conditions

| SYMBOL | PARAMETER |  | FIGURE | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t }}$ BO | Bus output delay from CK for outputting data;*$C_{L}=30 \mathrm{pF}$ |  | 8 |  | 70 | 95 | ns |
| ${ }^{\text {tPXZ }}$ | Output disable delay | FROM ${ }_{2}{ }^{-1} 0$ to bus |  |  | 30 | 65 | ns |
|  |  | From GO to bus |  |  | 20 | 40 |  |
| tPZX | Output enable delay;$C_{L}=30 \mathrm{pF}$ | FROM $\mathrm{I}^{-1} 0$ to bus |  |  | 55 | 80 | ns |
|  |  | From GO to bus |  |  | 25 | 45 |  |
| tovR | Overflow output delay from CK; $\mathrm{C}_{\mathrm{L}}=30 \mathrm{pF}$ |  | 8 |  | 60 | 95 | ns |

[^51]
## Test Waveforms

| TEST | $\mathbf{v}_{\mathbf{x}}{ }^{\text {a }}$ |  | OUTPUT WAVEFORM - MEAS. Level |
| :---: | :---: | :---: | :---: |
| All tpd | 5.0 V |  |  |
| tpxz | tPHz | tpLz |  |
| tpZX | tPZH | tpzL |  |

"At diode; see "Test Circuit" figure below.

## AC Test Conditions

Inputs 0 V LOW, $3 \mathrm{~V}_{\text {HIGH }}$. Rise and fall time $1-3 \mathrm{~ns}$ from 1 V to 2 V . Measurements are made from $1.5 \mathrm{~V}_{\mathrm{IN}}$ to $1.5 \mathrm{~V}_{\text {OUT }}$, except that tPXZ is measured by a delta in the outputs of 0.5 V from $\mathrm{V}_{\mathrm{OL}}$ or $\mathrm{V}_{\mathrm{OH}}$ respectively.

## Timing

Timing waveforms are shown in Figure 8. Specific instruction timing examples are shown in Figures 9 through 13.

## Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.


NOTE: $\overline{\mathrm{GO}}$ and $\mathrm{I}_{2}-\mathrm{I}_{0}$ can change only when CK is high.
Figure 8. Timing Diagram of the 'S516


NOTES: Register $Z$ is read at the same time that the overflow signal (if present) is set. If the instruction remains at code 7 after time-slot 11 , the contents of registers $Z$ and $W$ are swapped each cycle.
$\dagger$ "Any code" means any of code 0 through code 7 . However, code 6 will load a new value of X , and code 7 will cause the ' S 516 to attempt to drive the data bus. *Not available externally on the 'S516.

Figure 9. Instruction Timing Example No. 1: Load X, Load Y, Multiply, Read Z, Read W. By Presenting Code 7 on the Instruction Lines During the Last Multiply Cycle (State 8), the Results May Be Read During Time-Slots 10 and 11


NOTES: The instruction lines may be changed only when CK is high.
†"Any code" means any of code 0 through code 7 . Code 6 may be used here since a new X explicitly gets loaded for the next multiply operation. However, code 7 will cause the ' $S 516$ to attempt to drive the data bus.
*Not available externally on the 'S516.

Figure 10. Instruction Timing Example No. 2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W"


NOTES: Code 7 is given in time-slot 9, but has no effect until time-slot 10 since $\overline{\mathrm{GO}}$ is HIGH . After $\overline{\mathrm{GO}}$ goes LOW in time-slot 10 , Z may be read. $\dagger$ "Any code" means any of code 0 through code 7.
*Not available externally on the 'S516.
Figure 11. Instruction Timing Example No. 3: Load X, Load Y, Multiply, Read Z, Read W. This Timing Diagram Corresponds to Table 1. Only After Eight Clock Pulses of the Operation Cycle, the Result Is Read - Z During Time-Slot 10 and W During Time-Slot 11


NOTES: '†"Any code" means any of code 0 through code 7 . Code 6 or code 7 may be used here, since $\overline{G O}$ is HIGH, no new $X$ can be loaded, and the 'S516 cannot attempt to drive the data bus.
*Not available externally on the 'S516.

Figure 12. Instruction Timing Example No. 4: Load X, Load Y, Multiply, Wait, Read Z, Read W


NOTES: This sequence of operations is suitable for use when reading is to be done only at the very end of the operation sequence. The new X value is loaded during the time that the previous multiplication is being performed. See Programming Example \#3 for N

$$
\sum_{i=1} x_{i} \cdot Y_{i}
$$

$\dagger$ "Any code" means any of code 0 through code 7 . However, code 7 will cause the 'S516 to attempt to drive the data bus.
*Not available externally on the 'S516.
$\dagger \dagger$ Code 6 allows loading of a new X in State 12 and it takes the 'S516 State Counter to State 8. In State 8, Y is loaded via instruction 2 and the next multiply-accumulate cycle is initiated.

Figure 13. Instruction Timing Example No. 5: Sum of Products

## Programming Examples

In the following examples assume that each line with a separate instruction corresponds to one clock pulse. Instruction codes are $0,1,2,3,4,5,6,7$ and $x$ according to the usage explained in the key to Figure 2.

| Programming Example 1 |  |
| :---: | :---: |
| Calculating $\mathrm{X} \cdot \mathrm{Y}(\mathrm{A} \cdot \mathrm{B})$ |  |
| INST 6 | $X-A$ |
| INST 0 | $Y-B$ |
| INST X | MULT |
| INST X | MULT |
| INST X | MULT |
| INST X | MULT |
| INST X | MULT |
| INST X | MULT |
| INST X | MULT |
| INST 7 | MULT AND READ $Z=16 \mathrm{MSB}$ OF ( $\mathrm{A} \cdot \mathrm{B}$ ) |
| INST 7 | READ W = 16 LSB OF (A•B) |

## Programming Example 2

Calculating $\mathrm{X} 1 \cdot \mathrm{Y}(\mathrm{A} \cdot \mathrm{C})$
X 1 is a previous multiplier value. It was previously loaded (in example 1) with A.

| INST 0 | $Y-C$ |
| :--- | :--- |
| INST $X$ | MULT |
| INST $X$ | MULT |
| INST $X$ | MULT |
| INST $X$ | MULT |
| INST $X$ | MULT |
| INST $X$ | MULT |
| INST $X$ | MULT |
| INST 7 | MULT and READ Z = 16 MSB OF $(A \cdot C)$ |
| INST 7 | READ $W=16$ LSB OF $(A \cdot C)$ |

## Programming Example 3

Calculating $\sum_{i=1}^{N} X_{i} \cdot Y_{i}(A \cdot B+C \cdot D+E \cdot F+\ldots)$
In this case we read only after $N$ multiplications. $A$ new $X_{i}+1$ is loaded during the multiplication process for $X_{i} Y_{i}$.
Assume $\mathrm{N}=3$.
The sequence of instructions and operations for calculating

$$
\sum_{i=1}^{3} X_{i} \cdot Y_{i} \text { is: }(A \cdot B+C \cdot D+E \cdot F)
$$


INST 2 Y-D
INST $X$ MULT
INST X MULT
INST X MULT
INST $X \quad$ MULT $\}$ Perform C•D $+\left(K_{Z}, K_{w}\right)$
INST $X$ MULT
INST X MULT
INST X MULT
$\left(\begin{array}{rl}\text { INST } 6 & \text { MULT and LOAD } X-E \\ & Z-16 \text { MSB of }(C \cdot D+A \cdot B\end{array}\right.$
$W-16 L S B$ of $(C \cdot D+A \cdot B)$
INST 2 Y-F
INST X MULT
INST X MULT
$N=3$

READ $Z$
INST X MULT
INST 7 MULT and
READ $Z=16$ MSB of $(E \cdot F+C \cdot D+A \cdot B)$
READ W
INST 7

READ $W=16 L S B$ of $(E \cdot F+C \cdot D+A \cdot B)$

## Programming Example 4

Multiplication plus a constant (A•B + Constant)
Assume that the constant is a 32-bit 2s-complement number.

INST $6 \quad \mathrm{X}$ - A
INST 6 Z - C LOAD 16 MSB of constant
INST $6 \quad \mathrm{~W}-\mathrm{D}$ LOAD 16 LSB of constant
INST $0 \quad Y-B$
INST X MULT
INST $X$ MULT
INST X MULT
INST $X \quad$ MULT $\quad$ Perform A•B $+(Z, W)$
INST $X \quad$ MULT
INST X MULT
NST X MULT
INST 7 MULT and READ $Z=16$ MSB of ( $A \cdot B+(C, D)$ ) INST 7 READ $W=16$ LSB of ( $A \cdot B+(C, D)$ )

## Programming Example 5

Dividing a 32 -bit number by a 16 -bit number ( $(B, C) / A)$
INST $6 \quad \mathrm{X}-\mathrm{A}$
INST $6 \quad Z-B$
INST $4 \quad W-C$
INST X
INST $X$
INST X
INST X
INST X
INST $X$
INST X
INST X
INST X
INST $X$
INST X
INST $X$
INST X
INST X
INST X
INST $X$
INST X
INST X

INST 7 READ the remainder $W$ of $\frac{(B, C)}{A}$

## 16x 16 Flow-Thru ${ }^{\text {TM }}$ Multiplier Slice 745556

## Features/Benefits

- Twos-complement, unsigned, or mixed operands
- Full 32-bit product immediately available on each cycle
- High-speed 16x16 parallel multiplier
- Latched or transparent inputs/outputs
- Three-state output controls, independent for each half of the product
- Single +5 V supply (via multiple pins)
- Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages


## Description

The ' S 556 is a high-speed $16 \times 16$ combinatorial multiplier which can multiply two 16 -bit unsigned or signed twos-complement numbers on every cycle. Each operand $X$ and $Y$ has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16 -bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16 -bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding. The entire 32-bit double-length product is available at the outputs at one time.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 74 S 556 | P88, L84* | Commercial |

P88 is an 88-Pin-Grid-Array Package.
L84 is an 84-terminal Leadless-Chip Carrier Package.

* The 84-terminal leadless chip carrier, L84, and its socket, L84-2, are in development; contact the factory for further details.

The most-significant product bit, S31, is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM ( $\overline{\mathrm{OEM}})$ control input, while the LSP outputs are controlled by the TRIL ( $\overline{\mathrm{OEL}}$ ) control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.
All inputs and outputs have transparent latches. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84-terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

## 'S556 Logic Diagram



| SUMMARY OF SIGNALS/PINS |  |
| :---: | :--- |
| $\mathrm{X}_{15-0}$ | Multiplicand 16-bit data inputs |
| $\mathrm{Y}_{15-0}$ | Multiplier 16-bit data inputs |
| $\mathrm{XM}, \mathrm{YM}$ | Mode-control inputs for each data word; <br> LOW for unsigned data and HIGH for twos- <br> complement data |
| $\mathrm{S}_{31-0}$ | Product 32-bit output |
| $\bar{S}_{31}$ | Inverted MS product bit (for expansion) |
| RS, RU | Rounding inputs for signed and unsigned <br> data, respectively |
| GX | Gate control for $\mathrm{X}_{\mathrm{i}}$, RS, RU |
| GY | Gate control for $\mathrm{Y}_{\mathrm{i}}$ |

## Rounding Inputs

| INPUTS |  | ADDS |  | USUALLY USED WITH |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| RU | RS | $\mathbf{2}^{\mathbf{1 5}}$ | $\mathbf{2}^{\mathbf{1 4}}$ | $\mathbf{X M}$ | YM. |
| L | L | NO | NO | X | X |
| L | H | NO | YES | $H^{\dagger}$ | $H^{\dagger}$ |
| H | L | YES | NO | L | L |
| $H$ | $H$ | YES | YES | $\star$ | $\star$ |

$\dagger$ In mixed mode, one of these could be low but not both.

* Usually a nonsense operation.


## Mode-Control Inputs

| OPERATING <br> MODE | INPUT DATA |  | MODE- <br> CONTROL <br> INPUTS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{X}_{15-0}$ | $\mathrm{Y}_{15-0}$ | XM | YM |
|  | Unsigned | Unsigned | L | L |
| Mixed | Unsigned | Twos-Comp. | L | H |
|  | Twos-Comp. | Unsigned | H | L |
| Signed | Twos-Comp. | Twos-Comp. | H | H |

## 84-Terminal Leadless Chip Carrier Pinout



All $V_{C C}$ and GND pins must be connected to the respective $V_{C C}$ and GND connections on the board and should not be used for daisychaining through the IC.

Operating Conditions

| SYMBOL | PARAMETER |  | FIGURE | MIN | MER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Supply voltage |  |  | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ 1 | Setup time ( $\mathrm{X}_{\mathrm{i}}, \mathrm{R}_{\mathrm{j}}$ )/Y $\mathrm{Y}_{\text {j }}$ to GX/GY |  | 2a, 2b | 10 |  |  | ns |
| ${ }^{\text {t }}$ S 2 | Setup time $X_{i}, Y_{i}, R_{i}$ to $G M, G L$ | ts2L | 3a, 3b | 60 |  |  | ns |
|  |  | ${ }^{\text {t }}$ 2M |  | 74 |  |  |  |
| ${ }^{\text {t }} 33$ | Setup time GX, GY to GL, GM | ts3L | 4a, 4b, 4c, $4 \mathrm{~d}, 4 \mathrm{e}, 4 \mathrm{f}$ | 60 |  |  | ns |
|  |  | ${ }^{\text {t }} 33 \mathrm{M}$ |  | 75 |  |  |  |
| $\mathrm{t}_{\mathrm{H} 1}$ | Hold time ( $\left.\mathrm{X}_{\mathrm{i}}, \mathrm{R}_{\mathrm{i}}\right) / \mathrm{Y}_{\mathrm{i}}$ to GX/GY |  | 2a, 2b | 8 |  |  | ns |
| $\mathrm{t}_{\mathrm{H} 2}$ | Hold time $X_{i}, Y_{i}, R_{i}$ to $G M, G L$ | $\mathrm{t}_{\mathrm{H} 2 \mathrm{~L}}, \mathrm{t}_{\mathrm{H} 2 \mathrm{M}}$ | 3a, 3b | 3 |  |  | ns |
| $\mathrm{t}_{\mathrm{H} 3}$ | Hold time GX, GY to GM, GL | ${ }^{\text {tH3L }}$, ${ }^{\text {H3M }}$ | $\begin{gathered} 4 \mathrm{a}, 4 \mathrm{~b}, 4 \mathrm{c}, \\ 4 \mathrm{~d}, 4 \mathrm{e}, 4 \mathrm{f} \end{gathered}$ | 0 |  |  | ns |
| $\mathrm{t}_{\mathrm{w}}$ | Latch enable pulse width |  | 6 | 12 |  |  | ns |

* Indicates case temperature.

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{IL}}$ | Low-level input voltage** |  |  |  | 0.8 | V |
| $\mathrm{V}_{1} \mathrm{H}$ | High-level input voltage** |  |  | 2 |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -1.5 | V |
| ILL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.4 | mA |
| ${ }_{1} \mathrm{H}$ | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.4 \mathrm{~V}$ |  | 75 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{\text {CC }}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OL}}=8 \mathrm{~mA}$ |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{\mathrm{OH}}=-2 \mathrm{~mA}$ | 2.4 |  | V |
| IOZL | tate output current | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ |  | -100 | $\mu \mathrm{A}$ |
| $\mathrm{IOZH}^{\text {I }}$ | ate output current | $V_{C C}=$ MAX | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  | 100 | $\mu \mathrm{A}$ |
| los | Output short-circuit current* | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 | -90 | mA |
| ${ }^{\text {ICC }}$ | Supply current | $V_{C C}=M A X$ |  | 600 | 800 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current at hot temperature limit | $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}$ | $\mathrm{T}_{\mathrm{A}}=75^{\circ} \mathrm{C}$ |  | 700 | mA |

[^52]
## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | 74 S 556 COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| ${ }^{\text {t DTL }}$ | Transparent Multiply GX, GY, GM, GL = H | $X_{i}, Y_{i}, R_{i} \text { to } S_{15-0}$ <br> Figs. 1, 2c, 3b, 4c, 4f |  | $\begin{aligned} & \mathrm{CL}=30 \mathrm{pF} \\ & \mathrm{RL}=560 \Omega \\ & \text { See figure } 7 \end{aligned}$ |  | 50 | 76 | ns |
| ${ }^{\text {t }}$ DTM |  | $X_{i}, Y_{i}, R_{j} \text { to } S_{31}, \bar{S}_{31-16}$ <br> Figs. 1, 2c, 3b, 4c, 4f |  |  | 60 | 90 | ns |
| ${ }^{\text {t }}$ 11L | Transparent Output Multiply GM, GL = H | GX, GY to $\mathrm{S}_{15-0}$ <br> Figs. 2a, 2b, 4d, 4e |  |  |  | 80 | ns |
| ${ }^{t} \mathrm{D} 1 \mathrm{M}$ |  | GX,GY, to $S_{31}, \bar{S}_{31-16}$ Figs. 2a, 2b, 4d, 4e |  |  |  | 92 | ns |
| ${ }^{t}$ D2 | Transparent Input Multiply $\text { GX, GY }=\mathrm{H}$ | GM, GL to $\mathrm{S}_{\mathrm{i}}$ <br> Figs. 3a, 4a, 4b |  |  |  | 35 | ns |
| ${ }^{\text {tPXZ }}$ | Three-State Disable Timing | TRIL ( $\overline{\text { OEL }}$ ), TRIM ( $\overline{\text { OEM }}$ ) to $\mathrm{S}_{\mathrm{i}}$ Fig. 5 |  |  |  | 30 | ns |
| $t^{\prime}$ PZX | Three-State Enable Timing | TRIL ( $\overline{O E L})$, TRIM ( $\overline{O E M})$ to $S_{i}$ Fig. 5 |  |  |  | 30 | ns |

Transparent Multiply - Flowthrough Operation


Figure 1

The transparent multiply is a flowthrough operation of the 'S556. Both the input and output latches are made transparent by keeping GX, GY, GM, and GL at a HIGH level. The operands are
presented to the $X, Y$, and $R$ inputs; the results are available ${ }^{t} D T L$ and tDTM later, for the least and most significant halves of the product respectively.


* With this particular timing, set-up time $\mathrm{t}_{\mathrm{S} 1}$ will automatically be met.

Figure 2a.


Figure 2b

By tying the GL and GM lines HIGH, the 'S556 can perform transparent output (or pipelined input) multiplies. Data present is latched at the inputs using the GX and GY control signals. The time at which the result $S$ is present at the outputs depends on when the rising edges of GX and GY occur. If the rising edges of GX and GY occur after the operand inputs change, then Figure 2a applies; the result will be available at the outputs tD1L and ${ }^{t} D 1 M^{*}$ after the rising edges of GX and GY. If the rising edges of GX and GY occur less than ( ${ }^{t}$ W min ${ }^{-t_{S 1}}$ min) before the oper-


Figure 2c
and inputs change, then Figure 2 b applies; in this case the result will also be available at the outputs ${ }^{\mathrm{t}} \mathrm{D} 1 \mathrm{~L}$ and ${ }^{\mathrm{t}} \mathrm{D}_{1} \mathrm{M}^{*}$ after the rising edges of GX and GY. However, if the rising edges of GX and GY occur more than ( ${ }^{2}$ W min ${ }^{-1}$ S1 min) before the operand inputs change, then Figure 2c applies; the result will appear at the outputs IDTL $^{\text {DT }}$ IDTM ${ }^{*}$ after the operand inputs change.

* For the least and most significant halves of the product, respectively.


## Transparent Input Multiply - Pipelined Output



Figure 3a
By tying the GX and GY lines HIGH, the 'S556 can perform transparent input (or pipelined output) multiplies. Data is presented at the inputs, and $\mathrm{t}_{\mathrm{S}}$ after $X, Y$ and $R$ change, the results can be latched. The time at which the result $S$ is present at the outputs depends upon when the rising edges of GL and GM



Figure 3b
changing, then Figure 3 a applies; the result appears at the outputs $\mathrm{I}_{\mathrm{D} 2}$ after the rising edges of GL and GM. If the rising edges of GL and GM occur before ( ${ }_{\mathrm{S}} \mathrm{SL} \mathrm{min}^{-}{ }^{-} \mathrm{W}$ min ) from the inputs changing, then Figure 3b applies; the result appears at the outputs TDTL and IDTM ${ }^{*}$ after the operand inputs change.

* For the least and most significant halves of the product, respectively.


## Gated Multiply - Pipelined Input and Output



Figure 4a


Figure 4c



Figure 4b


GX, GY


GL, GM


Figure 4d


* With this particular timing setup time $\mathrm{t}_{\mathrm{S} 1}$ will be automatically met.

Figure 4 e
The gated multiply represents the pipelined input and output operation. The latch enable lines GX, GY, GL, GM are used to store incoming operands and outgoing results. The particular set-up times that must be met and the time the result takes to reach the outputs depends on two timing relationships. The first is when the rising edges of GX and GY occur with respect to the operand inputs changing, and the second is when the rising edges of GL and GM occur with respect to the rising edges of GX and GY. On the above timing diagrams, denote the absolute time

Figure $4 f$
that the operand inputs change as $T_{X Y R}$, the absolute time that the rising edges of GX and GY occur as TGXY, and the absolute time that the rising edges of GL and GM occur as TGLM. Thus, the two delays of concern can be explicitly stated as ( $T_{G X Y}{ }^{-}$ $T_{X Y R}$ ) and ( $T_{G L M}-T_{G X Y}$ ). Notice that either of these quantities can be positive or negative depending on which event occurs first. Timing for gated multiplies can then be summarized in the following table:

| $\mathbf{T}_{\text {GXY }}{ }^{-\mathbf{T}_{\text {XYR }}}$ | TGLM - ${ }_{\text {GXX }}$ | FIGURE | WHICH SET-UP TIMES MUST BE MET | WHEN RESULT IS PRESENT AT OUTPUTS |
| :---: | :---: | :---: | :---: | :---: |
| $T_{G X Y}-T_{X Y R} \geq 0$ | $T_{G L M}{ }^{-T_{G X Y}} \geq{ }^{\text {S }}{ }^{\text {min }}{ }^{-{ }^{-} W_{\text {min }}}$ | 4a | ${ }_{\text {t }} 3$ | $\mathrm{T}_{\mathrm{GLM}}{ }^{+t_{\text {D2 }}}$ |
|  |  | 4 b | $\mathrm{t}_{\mathrm{S} 1}, \mathrm{t}_{\mathrm{S} 2}, \mathrm{t}_{\mathrm{S} 3}$ | $\mathrm{T}_{\mathrm{GLM}}{ }^{+t_{\text {D2 }}}$ |
|  |  | 4 c | $\mathrm{t}_{\mathrm{s} 1} \mathrm{t}_{\mathrm{s} 2}$ | $T_{X Y R}+\left({ }_{\text {DTL }}, t_{\text {DTM }}\right)^{*}$ |
| $T_{G X Y}-T_{X Y R} \geq 0$ |  | 4d | ${ }_{\text {t }}$ 3 | $T_{G X Y}+\left({ }_{\text {D1L }}, t_{\text {D1M }}\right)^{*}$ |
|  |  | 4 e | $t_{\text {S } 1, ~} \mathrm{t}_{\mathbf{S} 2}, \mathrm{t}_{\text {S }}$ | $T_{G X Y}+\left(t_{D 1 L}, t_{D 1 M}\right)^{*}$ |
|  |  | 4 f | ${ }^{\text {t }}$ 1, $\mathrm{t}_{\text {S2 }}$ | $\mathrm{T}_{\text {XYR }}+\left(\mathrm{I}_{\text {DTL }}, \mathrm{T}_{\text {DTM }}{ }^{*}\right.$ |

* For the least and most significant halves of the product respectively.

NOTE: TXYR represents the absolute time when the operand inputs change.
$T_{G X Y}$ and $T_{G L M}$ represent the absolute times when the rising edges of the latch controls occur.

## Three-State Timing



Figure 5

## Test Waveforms

| TEST | $\mathbf{V}_{\mathbf{X}}$ |  | OUTPUT WAVEFORM - MEAS. LEVEL |
| :---: | :---: | :---: | :---: |
| All tpd | 5.0V |  |  |
| tPXZ | tPHZ <br> $t_{\text {PLZ }}$ | 0 |  |
| tPZX | tPZH <br> tPZL | 0 |  |

Latch Enable Pulse Width (GL, GM, GX, GY)


Figure 6

## Load Test Circuit



Figure 7

## Recommended Bypass Capacitors

The switching currents when the outputs change can be fairly high, and bypass capacitors are recommended to adequately decouple the VCC and GND connections.
For example, on the 84-terminal LCC package, pins 21 and 22 are VCC2 supplies and should be decoupled with pin 33, a GND input, using a $0.1 \mu \mathrm{f}$ monolithic ceramic disk capacitor. The
capacitor must have good high-frequency characteristics. Also pins 64 and 65, VCC1 and VCC2, should be decoupled with pin 74, a GND input, with a similar capacitor arrangement.
For the 88-pin-grid-array package pins 21 and 22 are VCC2 supplies and should be decoupled with pin 35 , the GND pin. Pins 66 and 67, VCC1 and VCC2, should be decoupled with pin 77, the GND pin.

## Decoupling Capacitors Shown with the 84-Terminal LCC Package



Typical Supply Current Over Temperature Range


## 88 Pin-Grid-Array

Pin Locations
Bottom View
(11) (14) (16) (17) (19) (21) (23) (25) (26) (28) (30) (31) (33)
(9) (12) (13) (15) (18) (20) (22) (24) (27) (29) (32) (34) (36)
(8) (10) (35) (38)
(6) (7)
(37) (39)

IDENTIFIER
(4) (5)

| (3) 22 |
| :--- |
| (1) 88 |

(87) ${ }^{(36)}$
(85) (84)
(83) (81)

(40) (41)
(42) (43)
(44) (45)
(46) (47)
(49) (48)
(51) (50)
(82) (79)
(54) (52)
(80) (78) (76) (73) (11) (68) (66) (64) (62) (59) (57) (56)
(77) (75) (14) (12) (70) (69) (6) (65) (63) (11) (6) (58) (55)

## Pin-Guide For Pin Grid Array

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | X9 | 23 | N/C* | 45 | S25 | 67 | VCC2 $\dagger$ |
| 2 | X10 | 24 | Y8 | 46 | S24 | 68 | N/C* |
| 3 | X11 | 25 | Y9 | 47 | S23 | 69 | S7 |
| 4 | X12 | 26 | Y10 | 48 | S22 | 70 | S6 |
| 5 | X13 | 27 | Y11 | 49 | S21 | 71 | S5 |
| 6 | X14 | 28 | Y12 | 50 | S20 | 72 | S4 |
| 7 | X15 | 29 | Y13 | 51 | S19 | 73 | S3 |
| 8 | XM | 30 | Y14 | 52 | S18 | 74 | S2 |
| 9 | GX | 31 | Y15 | 53 | S17 | 75 | S1 |
| 10 | RS | 32 | YM | 54 | S16 | 76 | S0 |
| 11 | RU | 33 | GY | 55 | GND | 77 | GND |
| 12 | GND | 34 | N/C* | 56 | TRIL ( $\overline{\mathrm{OEL}})$ | 78 | N/C* |
| 13 | YO | 35 | GND | 57 | GL | 79 | GND |
| 14 | Y1 | 36 | TRIM ( $\overline{\text { OEM }}$ ) | 58 | S15 | 80 | X0 |
| 15 | Y2 | 37 | GM | 59 | S14 | 81 | X1 |
| 16 | Y3 | 38 | $\overline{531}$ | 60 | S13 | 82 | X2 |
| 17 | Y4 | 39 | S31 | 61 | S12 | 83 | X3 |
| 18 | Y5 | 40 | S30 | 62 | S11 | 84 | X4 |
| 19 | Y6 | 41 | S29 | 63 | S10 | 85 | X5 |
| 20 | Y7 | 42 | S28 | 64 | S9 | 86 | X6 |
| 21 | VCC2 $\dagger$ | 43 | S27 | 65 | S8 | 87 | X7 |
| 22 | VCC2 $\dagger$ | 44 | S26 | 66 | VCC1† $\dagger$ | 88 | X8 |

* Not connected. $\dagger \mathrm{VCC} 2=$ Logic VCC. $\dagger \dagger \mathrm{VCC} 1=$ Output buffer VCC .


## Rounding

Multiplication of two n-bit operands results in a $2 n$-bit product $\dagger$. Therefore, in a pure n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

$$
\begin{aligned}
& 39.2 \rightarrow 39 \\
& 39.6 \rightarrow 39 \\
& 39.2+0.5=39.7 \rightarrow 39 \\
& 39.6+0.5=40.1 \rightarrow 40
\end{aligned} \quad \text { Rounding }
$$

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding
0.05 to the number and truncating the LSB:

$$
39.28+0.05=39.33 \rightarrow 39.3
$$

The situation in binary arithmetic is quite similar, but two cases need to be considered; signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are -1 ; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 8 illustrates these two cases for the $16 \times 16$ multiplier. In the signed case, adding one-half of the $S_{15}$ weight is accomplished by adding 1 in bit position 14, and in the unsigned case by adding 1 in bit position 15. Therefore, the 'S556 multiplier has two rounding inputs. RS and RU. Thus, to get a rounded single-length result, the appropriate $R$ input is tied to $\mathrm{V}_{\mathrm{CC}}$ (logic High) and the other $R$ input is grounded. If a double-length result is desired, both $R$ inputs are grounded.
†In general multiplication of an M -bit operand by an N -bit operand results in an $(\mathrm{M}+\mathrm{N})$-bit product.
(a) SIGNED MULTIPLY (OMIT $S_{31}$ as $S_{30}=S_{31}=$ sign of result)

(b) UNSIGNED MULTIPLY

BINARY POINT


BEST 16-BIT PRODUCT
ADD $1 / 2$ THE MSB
WEIGHT OF THE
DISCARDED PART

## NOTES:

(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best 16 -bit product is from $\mathrm{S}_{30}$ through $\mathrm{S}_{15}$, and rounding is performed by adding " 1 " to bit position $\mathrm{S}_{14}$.
(b) In unsigned notation the best 16 -bit product is the most significant half of the product and is corrected by adding " 1 " to bit position $\mathrm{S}_{15}$.

Figure 8. Rounding the Result of Binary Fractional Multiplication

## 745556

## Using the 'S556 in a Pipelined Positive-Edge Triggered Clock System

The 'S556 has internal latches which can be used affectively in systems where things happen on positive-going clock edges. This application is an extension of the gated multiply mode shown in Figure 1, in which a 32-bit product can be latched every ${ }^{t}$ S3 $n s e c$ in the 'S556.
If the signals GX, GY, GM and GL can be derived from the system clock then the latches can almost have the same effect as having a register. The basic philosophy behind the recommended timing is that the input latches are closed when the output latches are open; the outputs are then closed (and have
latched results) and new data is presented to the input latches, which are opened. This is shown by the relation between GX, GY and GL, GM in Figure 9. The set-up time $\mathrm{t}_{\mathrm{S} 3}$ is shown as one value but strictly speaking, it is split as ${ }_{t_{S}} \mathrm{~S}_{\mathrm{L}}$ and $\mathrm{t}_{\mathrm{S}} \mathrm{M}$ for the least significant and most significant half of the product respectively. The value of ${ }^{\text {S }} 3 \mathrm{~L}$ is less than $\mathrm{t}_{\mathrm{S} 3 \mathrm{M}}$, for applications requiring the least significant bits of the result as fast as possible.
One note of caution is that a design must always meet the set-up and hold times for $X_{i}, R_{i}$ with respect to $G X$ and for $Y_{i}$ with respect to GY.
The result $\mathrm{S}_{\mathrm{i}}$ is available ${ }_{\mathrm{D} 2}$ after the rising edge of GM and GL .


Figure 9

## Totally Parallel 32x32 Multiplier



Figure 10. Partial Products for a $32 \times 32$ Multiplication

A twos-complement $32 \times 32$ multiplication can be performed within 220 nsec using 4 'S556s, 20 'S381s, and 7 'S182s. This $32 \times 32$ multiply operation involves adding up four partial products as shown in Figure 10. These four partial products are generated in four multipliers; the outputs are $X A^{*} Y A, X A^{*} Y B$, $X B^{*} Y A, X B * Y B$, where $X 31-16=X B, X 15-0=X A, Y 31-16=Y B$, Y15-0 = YA.
The implementation of this twos-complement $32 \times 32$ multiplier is shown in Figure 11. The outputs of the $16 \times 16$ multipliers are connected to two levels of adders to give a 64-bit product. The first level of adders is needed to add the two central partial products of Figure 10, XA* $Y$ B and $X B^{*} Y A$. Notice the technique which is used to generate the "sign extension", or the mostsignificant sum bit of the first level of adders. The 'S556 provides, as a direct output, the complement of the most-significant product bit; having this signal immediately speeds up the signextension computation, and reduces the external parts count.


Figure 11. Implementation of the $32 \times 32$ Multiplier

For example, the inputs to the adder in the most significant position are the $\overline{\mathrm{S} 31}$ outputs from the two central multipliers. The sign extension of the addition of $X A^{*} Y B$ and $X B^{*} Y A$ is defined as
SIGN EXT $=\overline{\bar{A} . \bar{B} .+\bar{A} . C . ~+\bar{B} . C .}$, where
$A$ is the most-significant bit of the term $X A^{*} Y B$;
$B$ is the most-significant bit of the term $X B^{*} Y A$; and
$C$ is the carry-in to the most-significant bits of $X A^{*} Y B$ and $X B^{*} Y A$, in the adder.
The sign extension can be computed as the negation of the carry-out term of three terms, $\bar{A}, \bar{B}$, and $C$. This term corresponds to the negative of the carry-out of the bit position just one place to the right of the most-significant bit position of the first level of adders. The negative of the carry-out can be generated by presenting a carry-out and a binary "one" to the most significant bit of the adder. The generated sum bit then corresponds to the negation of the carry-out of the previous stage, which is the sign
extension required to be added to the 16 most -significant bits of the XB*YB partial product term.
The second level of adders, which performs a 48-bit add function, is fairly straightforward. These adders can be implemented using 'S381 four-bit ALUs and 'S182 carry-bypasses ("carrylookahead generators") which are available from Monolithic Memories Inc. and from other vendors.
Other configurations such as $48 \times 48$ and $64 \times 64$ multipliers can be designed using the same methodology, $r 1$.

## References

1. "Fast $64 \times 64$ Multiplication using $16 \times 16$ Flow-through Multiplier and Wallace Trees," Marvin Fox, Chuck Hastings and Suneel Rajpal, Monolithic Memories System Design Handbook, pages 8-53 to 8-61.

# 8x8 High Speed Schottky Multipliers 

## Features/Benefits

- Industry-standard $8 \times 8$ multiplier
- Multiplies two $\mathbf{8}$-bit numbers; gives $\mathbf{1 6 - b i t}$ result
- Cascadable; 56x56 fully-parallel multiplication uses only $\mathbf{3 4}$ multipliers for the most-significant half of the product
- Full $\mathbf{8 x 8}$ multiply in $\mathbf{6 0 n s}$ worst case
- Three-state outputs for bus operation
- Transparent 16-bit latch in 'S557
- Plug-in compatible with original Monolithic Memories' 67558


## Description

The ' $\mathrm{S} 557 /$ ' S 558 is a high-speed $8 \times 8$ combinatorial multiplier which can multiply two eight-bit unsigned or signed twoscomplement numbers and generate the sixteen-bit unsigned or signed product. Each input operand $X$ and $Y$ has an associated Mode control line, $X_{M}$ and $Y_{M}$ respectivelv: When a Mode control line is at a Low logic level, the operand is treated as an unsigned eight-bit number; whereas, if the Mode control is at a High logic level, the operand is treated as an eight-bit signed twos-complement number. Additional inputs, $R_{S}$ and $R_{U}$, ( $R$, in the 'S557) allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers.
The 'S557 internally develops proper rounding for either signed or unsigned numbers by combining the rounding input $R$ with $X_{M}, Y_{M}, \overline{X_{M}}$, and $\overline{Y_{M}}$ as follows:
$R_{U}=\overline{X_{M}} \cdot \overline{Y_{M}} \cdot R=$ Unsigned rounding input to $2^{7}$ adder.
$R_{S}=\left(X_{M}+Y_{M}\right) R=$ Signed rounding input to $2^{6}$ adder.

Since the 'S558 has no latches, it does not require the use of pin 11 for the latch enable input $G$, so $R_{S}$ and $R_{U}$ are brought out separately.

The most-significant product bit is available in both true and complemented form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an assertive-low Output Enable which allows several multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5 V power supply and is packaged in a standard 40-pin DIP.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| 54 S 558 | $\mathrm{~J},(44),(\mathrm{L})$ | Military |
| $74 \mathrm{~S} 557,74 \mathrm{~S} 558$ | $\mathrm{~N}, \mathrm{~J}$, | Commercial |

## Logic Symbol



## Pin Configuration


$\dagger$ For 74 S 557 Pin 9 is R and Pin 11 is G .

## Logic Diagram


$\dagger$ For 74 S 557 Pin 9 is R and $\operatorname{Pin} 11$ is G .

## Absolute Maximum Ratings


Input voltage .......................................................................................................................... 7.0 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V
Storage temperature ................................................................................................ $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | DEVICE | MILITARY |  |  | COMMERCIAL |  |  | UNITS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | all | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | all | -55 |  | 125* | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ su | $X_{i}, Y_{i}$ to $G$ set | 'S557 |  |  |  | 40 |  |  | ns |
| $t_{h}$ | $X_{i}, Y_{i}$ to $G$ hold time | 'S557 |  |  |  | 0 |  |  | ns |
| $t_{\text {w }}$ | Latch enable pulse width | 'S557 |  |  |  | 15 |  |  | ns |

* Case temperature


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS | MIN TYP $\dagger$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 | V |
| $\mathrm{V}_{1 \mathrm{H}}$ | High-level input voltage |  |  | 2 |  | V |
| $V_{\text {IC }}$ | Input clamp voltage | $V_{C C}=$ MIN | $1 /=-18 \mathrm{~mA}$ |  | -1.5 | V |
| ILL | Low-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=0.5 \mathrm{~V}$ |  | -1 | mA |
| ${ }_{1} \mathrm{H}$ | High-level input current | $V_{C C}=M A X$ | $V_{1}=2.4 \mathrm{~V}$ |  | 100 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $V_{C C}=$ MIN | $\mathrm{I}^{\mathrm{OL}}=8 \mathrm{~mA}$ |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}^{\mathrm{OH}}=-2 \mathrm{~mA}$ | 2.4 |  | V |
| 'OZL | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ |  | -100 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  | 100 | $\mu \mathrm{A}$ |
| Ios | Output short-circuit current* | $V_{C C}=M A X$ | $\mathrm{v}_{\mathrm{O}}=0 \mathrm{~V}$ | -20 | -90 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current | $V_{C C}=M A X$ |  | 200 | 280 | mA |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ Typicals at $5.0 \mathrm{~V} V_{C C}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | DEVICE | TEST CONDITIONS | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  |  | MIN | TYP $\dagger$ | MAX | MIN | TYP $\dagger$ | MAX |  |
| ${ }^{\text {t PD1 }}$ | $X_{i}, Y_{i}$ to $S_{7-0}$ | All | $\begin{aligned} & C_{L}=30 \mathrm{pF} \\ & R_{L}=560 \Omega \end{aligned}$ <br> see test figures |  | 40 | 60 |  | 40 | 50 | ns |
| ${ }^{\text {t PD2 }}$ | $X_{i}, Y_{i}$ to $S_{15-8}$ | All |  |  | 45 | 70 |  | 45 | 60 | ns |
| ${ }^{\text {t PD3 }}$ | $X_{i}, Y_{i}$ to $\bar{S}_{15}$ | All |  |  | 50 | 75 |  | 50 | 65 | ns |
| ${ }^{\text {t PD4 }}$ | G to $\mathrm{S}_{\mathrm{i}}$ | 'S557 |  |  | 20 | 40 |  | 20 | 35 | ns |
| ${ }^{\text {t PXZ }}$ | $\overline{\mathrm{OE}}$ to $\mathrm{S}_{\mathrm{i}}$ | All |  |  | 20 | 40 |  | 20 | 30 | ns |
| ${ }^{\text {t P Z X }}$ | $\overline{\mathrm{OE}}$ to $\mathrm{S}_{\mathrm{i}}$ | All |  |  | 15 | 40 |  | 15 | 30 | ns |

## Timing Waveforms

## Setup and Hold Times ('S557)



NOTE: If the rising edge of $G$ occurs before ( ${ }^{(S U}$ MIN $^{-t} W_{M I N}$ ) from the inputs changing, then the applicable propagation delays are tPD, tPD2 and tPD3, (and not tPD4). In this case the time at which the results arrive at the outputs depends on when the inputs change instead of when the rising edge of G occurs.

## Propagation Delay



## Latch-Enable Pulse Width ('S557)



## Test Waveforms

| TEST | $\mathbf{v}_{\mathbf{X}}$ |  | OUTPUT WAVEFORM - MEAS. LEVEL |
| :---: | :---: | :---: | :---: |
| All tpd | 5.0 V |  |  |
| tPXZ | for ${ }^{\text {t }} \mathrm{PHZ}$ | for <br> $\mathbf{t}_{\text {PLZ }}$$\|$5.0V |  |
| tpzX | for <br> $\mathbf{t}_{\text {PZH }}$ <br> 0.0 V | for <br> tPZL <br> 5.0 V |  |

## Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.


## Definition of Timing Diagram

## WAVEFORM

INPUTS
OUTPUTS


NOT APPLICABLE

| SUMMARY OF SIGNALS/PINS |  |
| :---: | :--- |
| $\mathrm{X}_{7}-\mathrm{X}_{0}$ | Multiplicand 8-bit data inputs |
| $\mathrm{Y}_{7}-\mathrm{Y}_{0}$ | Multiplier 8-bit data inputs |
| $\mathrm{X}_{\mathrm{M}}, \mathrm{Y}_{\mathrm{M}}$ | Mode control inputs for each data word; LOW for <br> unsigned data and HIGH for twos-complement <br> data |
| $\mathrm{S}_{15}-\mathrm{S}_{0}$ | Product 16-bit output |
| $\bar{S}_{15}$ | Inverted MSB for expansion |
| $\mathrm{R}_{\mathrm{S}}, \mathrm{R}_{\mathrm{U}}$ | Rounding inputs for signed and unsigned data, <br> respectively ('S558 only) |
| G | Transparent latch enable ('S557 only) |
| $\overline{\mathrm{OE}}$ | Three-state enable for $\mathrm{S}_{15}-\mathrm{S}_{\mathrm{O}}$ and $\overline{\mathrm{S}_{15}}$ outputs |
| R | Rounding input for signed or unsigned data; <br> combined internally with $\mathrm{X}_{\mathrm{M}}, \mathrm{Y}_{\mathrm{M}}$ ('S557 only) |

## ROUNDING INPUTS

'S557

| INPUTS |  |  | ADDS |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{X}_{\mathbf{M}}$ | $\mathbf{Y}_{\mathbf{M}}$ | $\mathbf{R}$ | $\mathbf{2}^{\mathbf{7}}$ | $\mathbf{2}^{\mathbf{6}}$ |  |
| L | L | $H$ | YES | NO |  |
| L | $H$ | $H$ | NO | YES |  |
| $H$ | L | $H$ | NO | YES |  |
| $H$ | $H$ | $H$ | NO | YES |  |
| $X$ | $X$ | L | NO | NO |  |

'S558

| INPUTS |  | ADDS |  | USUALLY USED WITH |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{R}_{\mathbf{U}}$ | $\mathbf{R}_{\mathbf{S}}$ | $\mathbf{2}^{\mathbf{7}}$ | $\mathbf{2}^{\mathbf{6}}$ | $\mathbf{X}_{\mathbf{M}}$ | $\mathbf{Y}_{\mathbf{M}}$ |
| L | L | NO | NO | X | X |
| L | H | NO | YES | $\mathrm{H} \dagger$ | $H \dagger$ |
| $H$ | L | YES | NO | L | L |
| $H$ | $H$ | YES | YES | $\boldsymbol{*}$ | $\boldsymbol{*}$ |

fin mixed mode, one of these could be Low but not both.
*Usually a nonsense operation. See applications section of data sheet.
745557 FUNCTION TABLE

| INPUTS |  | PRODUCT RESULT FROM ARRAY | LATCH CONTENTS (INTERNAL TO PART) | OUTPUTS | FUNCTION |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\overline{\mathrm{OE}}$ | G | $\mathrm{T}_{\mathbf{i}}$ | $\mathbf{Q}_{\mathbf{i}}$ | $\mathbf{S}_{\mathbf{i}}$ |  |
| L | L | $\begin{aligned} & x \\ & x \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | Latched |
| $\begin{aligned} & L \\ & L \end{aligned}$ | $\begin{aligned} & \mathrm{H} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & (\mathrm{L})^{*} \\ & (\mathrm{H})^{*} \end{aligned}$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \end{aligned}$ | Transparent |
| H | L | $\begin{aligned} & \mathrm{X} \\ & \mathrm{X} \end{aligned}$ | $\begin{aligned} & (L) \\ & (H) \end{aligned}$ | $\begin{aligned} & Z \\ & Z \end{aligned}$ | Hi-Z; Latched Data not Changed |
| H | H | X | (X)* | Z | Hi-Z |

[^53]MODE CONTROL INPUTS

| OPERATING MODE | INPUT DATA |  | MODE CONTROL INPUTS |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $\mathrm{X}_{7}-\mathrm{X}_{0}$ | $Y_{7}-Y_{0}$ | $\mathrm{X}_{\mathbf{M}}$ | $\mathbf{Y}_{\mathbf{M}}$ |
| Unsigned | Unsigned | Unsigned | L | L |
| Mixed | Unsigned | Twos-Comp. | L | H |
|  | Twos-Comp. | Unsigned | H | L |
| Signed | Twos-Comp. | Twos-Comp. | H | H |

## Functional Description

The 'S557 and 'S558 multipliers are $8 \times 8$ full-adder Cray arrays capable of multiplying numbers in unsigned, signed, twoscomplement, or mixed notation. Each 8-bit input operand $X$ and $Y$ has associated with it a mode control which determines whether the array treats this number as signed or unsigned. If the mode control is at High logic level, then the operand is treated as a twos-complement number with the most-significant bit having a negative weight; whereas, if the mode control is at a Low logic level, then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most-significant product bit is available in both true and complemented form. This allows an adder to be used as a subtractor in many applications and eliminates the need for certain SSI circuits.

Two additional inputs to the array, $\mathrm{R}_{\mathrm{S}}$ and $\mathrm{R}_{\mathrm{U}}$, allow the addition of a bit at the appropriate bit position so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers. In the 'S557, these two inputs are generated internally from the mode controls and a single $R$ input.

The product outputs of the multiplier are controlled by an assertive-low Output Enable control. When this control is at a Low logic level the multiplier outputs are active, while if the control is at a High logic level then the outputs are placed in a high-impedance state. This three-state capability allows several multipliers to drive a common bus, and also allows pipelining of multiplication for higher-speed systems.

## Rounding

Multiplication of two $n$-bit operands results in a $2 n$-bit product $\dagger$. Therefore, in an n-bit system it is necessary to convert the double-length product into a single-length product. This can be accomplished by truncating or rounding. The following examples illustrate the difference between the two conversion techniques in decimal arithmetic:

$$
\begin{aligned}
& \left.\begin{array}{l}
39.2 \rightarrow 39 \\
39.6 \rightarrow 39
\end{array}\right\} \text { Truncating } \\
& \left.\begin{array}{l}
39.2+0.5=39.7 \rightarrow 39 \\
39.6+0.5=40.1 \rightarrow 40
\end{array}\right\} \text { Rounding }
\end{aligned}
$$

Obviously, rounding maintains more precision than truncating, but it may take one more step to implement. The additional step involves adding one-half of the weight of the single-length LSB to the MSB of the discarded part; e.g., in decimal arithmetic rounding 39.28 to one decimal point is accomplished by adding 0.05 to the number and truncating the LSB:

$$
39.28+0.05=39.33 \rightarrow 39.3
$$

The situation in binary arithmetic is quite similar, but two cases need to be considered: signed and unsigned data representation. In signed multiplication, the two MSBs of the result are identical, except when both operands are -1 ; therefore, the best single-length product is shifted one position to the right with respect to the unsigned multiplications. Figure 1 illustrates these two cases for the $8 \times 8$ multiplier. In the signed case, adding one-half of the $S_{7}$ weight is accomplished by adding 1 in bit position 6, and in the unsigned case 1 is added to bit position 7. Therefore, the 'S558 multiplier has two rounding inputs, $R_{s}$ and $R_{u}$. Thus, to get a rounded single-length result, the appropriate R input is tied to $\mathrm{V}_{\mathrm{CC}}$ (logic High) and the other $R$ input is grounded. If a double-length result is desired, both $R$ inputs are grounded for the ' S 558 , and the single R input is grounded for the 'S557.
$\dagger$ In general: multiplication of an $M$-bit operand by an N -bit operand results in an ( $\mathrm{M}+\mathrm{N}$ )-bit product.


NOTES:
(a) In signed (twos-complement) notation, the MSB of each operand is the sign bit, and the binary point is to the right of the MSB. The resulting product has a redundant sign bit and the binary point is to the right of the second MSB of the product. The best eight-bit product is from $\mathrm{S}_{14}$ through $\mathrm{S}_{7}$, and rounding is performed by adding " 1 " to bit position $\mathrm{S}_{6}$.
(b) In unsigned notation the best 8 -bit product is the most significant half of the product and is corrected by adding " 1 " to bit position $\mathrm{S}_{7}$.

Figure 1. Rounding the Result of Binary Fractional Multiplication

## Signed Expansion

The most-significant product bit has both true and complement outputs available. When building larger signed multipliers, the partial products (except at the lower stages) are signed numbers. These unsigned and signed partial products must be added together to give the correct signed product. Having both the true and complemented form of the mostsignificant product bit available assists in this addition. For example, say that two signed partial products must be added and MSI adders are used; we then have the situation of adding together the carry from the previous adder stage plus the addition of the two negative most-significant partial-product bits. The result of adding these variables must be a positive sum and a negative carry (borrow). The equations for this are:

$$
\begin{aligned}
& S=A \oplus B \oplus C \\
& C_{O U T}=A B+B C+C A
\end{aligned}
$$

where $C$ is the carry-in and $A$ and $B$ are the sign bits of the two partial products.
Now an adder produces the equations:

$$
\begin{aligned}
& S=A \oplus B \oplus C \\
& C_{O U T}=A B+B C+C A
\end{aligned}
$$

Examining these equations, it can be seen that, if the inversions of $A$ and $B$ are used, then the most significant sum bit of the
adder is the sign extension bit.
Sign ext $=A B+B \bar{C}+\bar{C} A=\overline{\bar{A} \bar{B}+\bar{B} C+C \bar{A}}$,
and the sum remains the same.

## 16x16 Twos-Complement Multiplication

The 16 -bit $X$ operand is broken into two 8 -bit operands ( $X_{7}-X_{0}$ and $\left.X_{15}-X_{8}\right)$, as is the $Y$ operand. Since the situation is that of a cross-product, four partial products are generated as follows:

$$
\begin{aligned}
& A=X_{L} * Y_{L} \\
& B=X_{L} * Y_{H} \\
& C=X_{H} * Y_{L} \\
& D=X_{H} * Y_{H}
\end{aligned}
$$

where the subscript $L$ stands for bits $7-0$, ("low or least-significant half), and the subscript H stands for bits 15-8.
Expanded twos-complement multiplication requires a sign extension of the B and C partial products. Thus, $\mathrm{B}_{15}$ and $\mathrm{C}_{15}$ need to be extended eight positions to the left (to align with $\mathrm{D}_{15}$ ). In this approach two more adders are required. But the complement of the MSB ( $\bar{S}_{15}$ ) on the 'S557/8 can be used to save these two adders. Figure 2 shows the implementation of $16 \times 16$ signed twos-complement multiplication in this manner.


Figure 2. $16 \times 16$ Twos-Complement Signed Multiplication

|  |  |  |  |  |  |  |  |  | $\begin{aligned} & X_{15} \\ & \mathbf{Y}_{15} \\ & \hline \end{aligned}$ | $\begin{aligned} & X_{14} \\ & Y_{14} \\ & \hline \end{aligned}$ | $\begin{aligned} & X_{13} \\ & r_{13} \\ & \hline \end{aligned}$ | $X_{12}$ $Y_{12}$ | $X_{11}$ $Y_{11}$ | $\begin{aligned} & X_{10} \\ & Y_{10} \end{aligned}$ | $X_{9}$ $Y_{9}$ | $X_{8}$ $Y_{8}$ | $X_{7}$ $Y_{7}$ | $X_{6}$ $Y_{6}$ | $\begin{aligned} & X_{5} \\ & Y_{5} \end{aligned}$ | $\begin{aligned} & X_{4} \\ & Y_{4} \end{aligned}$ | $\begin{aligned} & x_{3} \\ & y_{3} \end{aligned}$ | $\begin{aligned} & X_{2} \\ & Y_{2} \end{aligned}$ | $\begin{array}{ll} x_{1} & x_{0} \\ y_{1} & y_{0} \\ \hline \end{array}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | B15 | B14 | B13 |  | B11 | B10 | B9 | B8 | B7 | B6 | B5 | $\mathrm{B}_{4}$ | B3 | $\mathrm{B}_{2}$ | $\mathrm{B}_{1}$ | $\mathrm{B}_{0}$ |  |  |  |  |  |  |  |
|  | D7 | $\mathrm{D}_{6}$ | D5 | $\mathrm{D}_{4}$ | D3 | $\mathrm{D}_{2}$ | $\mathrm{D}_{1}$ | D0 | A15 | A14 | $A_{13}$ | A12 | A11 | A10 | A9 | $\mathrm{A}_{8}$ | A7 | A6 | A5 | A4 | $\mathrm{A}_{3}$ | A2 | $A_{1} \quad A_{0}$ |
|  | $\mathrm{C}_{15}$ | $\mathrm{C}_{14}$ | $\mathrm{C}_{13}$ | $\mathrm{C}_{12}$ | $\mathrm{C}_{11}$ | $\mathrm{C}_{10}$ | C9 | $\mathrm{C}_{8}$ | $C_{7}$ | C6 | C5 | $\mathrm{C}_{4}$ | C3 | C2 | $\mathrm{C}_{1}$ | $\mathrm{C}_{0}$ |  |  |  |  |  |  |  |
|  | $\mathrm{S}_{23}$ | S22 | $\mathrm{S}_{21}$ | $\mathrm{S}_{20}$ | S19 | $\mathrm{S}_{18}$ | S17 | S16 | $\mathrm{S}_{15}$ | S14 | $\mathrm{S}_{13}$ | $\mathrm{S}_{12}$ | $\mathrm{S}_{11}$ | S 10 | S9 | $\mathrm{S}_{8}$ | S7 | S6 | S5 | S4 | S3 | S2 | $\mathrm{S}_{1} \mathrm{~S} 0$ |

Figure 3. Unsigned Expansions of the $\mathbf{8 \times 8}$ Multiplier to $16 \times 16$ Multiplication

Memories

## Applications:

## How to Design Superspeed Cray Multipliers with '558s by Chuck Hastings

Multiplication, as most of us think of it, is performed by repeated addition and shifting. When we multiply using pencil and paper, according to the familiar elementary-school method, we first write down the multiplicand, and then write down the multiplier immediately under it and underline the multiplier. Then we take the least-significant digit of the multiplier, multiply that digit by the entire multiplicand, and record the answer in the top row of our workspace, underneath the line. Then we repeat, using now the second-least-significant multiplier digit, and record that answer below the first one, pushed one digit position (that is, "shifted") to the left. This process continues until we run out of multiplier digits (or out of patience), at which point we add up the constants of the whole diamond-shaped workspace and record at the bottom an answer which consists of either $m+n-1$ digits or $m+n$ digits, where there are $m$ digits in the multiplier and $n$ digits in the multiplicand. An example, voila':

$$
\begin{aligned}
125 & \text { (multiplicand) } \\
\times 107 & \text { (multiplier) } \\
\hline 875 & (7 \times 125) \\
000 & (0 \times 125, \text { shifted left one digit position) } \\
125 & (1 \times 125, \text { shifted left two digit positions) } \\
\hline 13375 & \text { (sum of the above) }
\end{aligned}
$$

## Figure 4. Decimal Multiplication

The decimal number system has no monopoly on truth our ancestors simply happened to have ten fingers at the time when someone came up with the idea of counting. Binary numbers, as you know, are more copacetic than are decimal numbers with digital-logic elements, which like to settle comfortably into one voltage state ("High) or another ("Low"), rather than into one of ten different states. So we can repeat the above example using binary numbers, right? First, we convert our multiplicand and multiplier to binary:

$$
\begin{aligned}
& 125_{10}=01111101_{2} \\
& 107_{10}=01101011_{2}
\end{aligned}
$$

The subscripts 10 and 2 refer to the "base" or "radix" of the number system, 10 for decimal and 2 for binary. (Remember your New Math?) For sneaky reasons to be revealed soon, I've used 8 -bit binary numbers, which is one bit more than necessary for my example, and added a leading zero. So, we multiply:

$$
\begin{aligned}
& 01111101_{2}=125_{10} \\
& \times 01101011_{2}=107_{10} \\
& 01111101 \\
& 01111101 \\
& 00000000 \\
& 01111101 \\
& 00000000 \\
& 01111101 \\
& 01111101 \\
& \frac{00000000}{0011010000111111}=13375_{10}
\end{aligned}
$$

Figure 5. Binary Multiplication
l've left off the remarks this time, but they're just like the remarks in the decimal example, at least in principle. Just in case you doubt this answer, l'll convert it back:

| 1 | 1 |  |
| :--- | ---: | :--- |
| 1 | 2 |  |
| 1 | 4 |  |
| 1 | 8 |  |
| 1 | 16 |  |
| 1 | 32 |  |
| 0 | 0 | $\left(\begin{array}{r}64) \\ 0\end{array}\right.$ |
| 0 | 0 | $(128)$ |
| 0 | 0 | $(256)$ |
| 1 | 1024 | $(512)$ |
| 0 | 0 | $(2048)$ |
| 1 | 4096 |  |
| 1 | 8192 |  |
| 0 | 0 | $(16384)$ |
| 0 | 0 | $(32768)$ |

Figure 6. Binary-to-Decimal Conversion

Now look carefully at the diamond-shaped array of numbers in the workspace in Figure 5. Each row is either the multiplicand 01111101 , or else all zeroes. The 01111101 rows correspond to " 1 " digits in the multiplier, and the all-zero rows to " 0 " digits in the multiplier. Life does get simpler in some ways when we switch to binary numbers: "multiplying a multiplier digit by the multiplicand" now means just gating a copy of the multiplicand into that position if the digit is "1," and not doing so if the digit is "0."

Seymour Cray, the master computer designer from Chippewa Falls, Wisconsin, whose career has spanned three companies (Univac, Control Data, and now Cray Research) and many inventions, first observed some time in the late 1950s that computers also could actually multiply this way, if one merely provided enough components. This last qualifying remark; in those days when even transistors, let alone integrated circuits, in computers were still a novelty was by no means a trivial one! To prove his point (and satisfy a government contract), Cray designed, and Control Data built, a $48 \times 48$ multiplier which operated in one microsecond, about 1960. This multiplier was part of a special-purpose array processor for a classified application, and was so big that a CDC 1604 (then considered a large-scale processor) served as its input/output controller. In principle, such a multiplier at that time would have had to consist of 4848 -bit full adders or "mills," each of which received one input 48 -bit number from the outputs of the mill immediately above it in the array, and the other 48-bit number from a gate which either allowed the multiplicand to pass through, or else supplied an ali-zero 48 -bit number. Actually, these mills have to be somewhat longer than 48 bits. Anyway, that is at least 2304 full adders, and in 1960 a full-adder circuit normally occupied one small plug-in circuit card.

A later version of this multiplier, in the CDC 7600 supercomputer, could produce one $48 \times 48$ product out every 275 nanoseconds on a pipelined basis. The pipelining was asynchronous, and the entire humungous array of adders and gating logic could have up to three different products rippling down it at a given instant!

Back to the 1980s. Monolithic Memories has for several years produced an $8 \times 8$ Cray multiplier, the 67588 , as a single 600-mil 40-pin DIP. After we invented this part, AMD second-sourced it, and by now it has become an industry standard. We now also have faster pin-compatible parts, the 54/74S558 and 74S557. Like other West Coast companies 2,000 miles from Wisconsin and Minnesota where Seymour Cray does his inventing, Monolithic Memories previously used the term "combinatorial multiplier" instead of "Cray multiplier" for this type of part. However, "combinatorial multiplier" has nine extra letters and five extra syllables, and also inadvertently implies that the technique involves combinatorial logic rather than arithmetic circuits. Some West Coast designs, including our 67588, use a modified internal array with only half as many full-adder circuits and slightly different interconnections, based on the two-bit "Boothmultiplication" algorithm (see reference 1), plus the two-bit "Wallace-tree" or "carry-save adder" technique (see references 2 and 3). Conceptually, however, the entire chip or system continues to operate as a Cray multiplier.

The '558, in particular can be thought of as a static logic network which fits exactly the binary multiplication example of Figure 5. (See now why 1 insisted on using 8 -bit binary numbers?) There are no flipflops or latches whatever in the '558 - it is a "flowthrough" device. Its 40 pins are used up as follows:

| Use of Pins | Input, Output, <br> or Voltage | Number <br> of Pins |
| :--- | :---: | :---: |
| Multiplier | 1 | 8 |
| Multiplicand | 1 | 8 |
| Double-Length Product | 0 | 16 |
| Complement of Most- | 0 | 1 |
| Significant Bit of Double- <br> Length Product |  |  |
| 3-State Output Enable | 1 | 1 |
| Number-Interpretation- <br> Mode Control | 1 | 2 |
| Rounding Control for Product | 1 | 2 |
| Power and Ground | V | 2 |
|  |  | 40 |

Table 1. Use of Pins in the '558

The two number-interpretation-mode control pins, one for the multiplier and one for the multiplicand, allow the format for each of these two 8 -bit input numbers to be chosen independently, as follows:

| Control Input | Interpretation of 8-bit Input Number |
| :---: | :---: |
| L | 8-bit unsigned |
| H | 7-bit plus a sign bit |

Table 2. Mode Control Input Encoding

The two rounding control pins allow either integer (rightjustified) or fractional (left-justified) interpretation of the 14-bits-plus-sign double-length product of two 7 -bits-plus-sign numbers for internal rounding of the double-length result to the most accurate 8 -bit number. The control encoding is:

| $\mathbf{R}_{\mathbf{S}}$ Input | $\mathbf{R}_{\mathbf{U}}$ Input |
| :---: | :---: |
| $L$ | $L$ |
| $L$ | $H$ |
| $H$ | $L$ |
| $H$ | $H$ |

Effect<br>Disable Rounding<br>Round Unsigned<br>Round Signed<br>Nonsense (see below)

## Table 3. Rounding Control Input Encoding

Rounding is normally disabled if the entire 16 -bit double-length product output is to be used. If only an 8 -bit subset of this product is to be used, this subset can be either bits $15-8$ for unsigned rounding as shown in Figure 7, or bits 14-7 for signed rounding as shown in Figure 8. In either case, a " 1 " is forced into the '558's internal adder network at the bit position indicated by the arrow; adding a " 1 " into the bit position below the least-significant bit of the final answer has the effect of rounding, as you can see after a little thought. Obviously, forcing a " 1 " into both of these adder positions at the same time is a nonsense operation for most applications - it adds a " 3 " into the middle of the double-length result.


Figure 7. Unsigned Rounding


Figure 8. Signed Rounding

By now you probably have a fairly good idea of what a '558 is, and would like a few hints as to how to use it, right? First of all, there is an occasional application in things like video games for very fast multiplication, either $8 \times 8$ or $16 \times 16$, controlled by an 8 bit microprocessor, where there would be one ' 558 per system (see reference 4). More typically, however, the ' 558 is a building block, and several of them are used within one system; in fact, maybe more than several - "many." In the usual Silicon-Valley jargon, we can cascade a number of '558 (8×8) Cray-multiplier chips to create larger Cray multipliers at the systems level.

For the sake of concreteness, I'll discuss the case of $56 \times 56$ multipliers, which are appropriate in floating-point units which deal with "IBM-long-format" numbers which have a 56 -bit mantissa. Any computer which emulates, or uses the same floating-point format as, any of the following computers can use such a multiplier:

## IBM 360/370

## Amdahl 470

Data General Eclipse
Gould/System Engineering SEL 32
Norsk Data 500 (different format)
There are two basic approaches: serial-parallel, and fully parallel. The serial-parallel approach uses seven '558s, and requires seven full multiply-and-add cycles. On the first cycle, the least-significant eight bits of the multiplier are multiplied by the entire multiplicand, and this partial product is saved. On the second cycle, the next-least significant eight bits of the multiplier are multiplied by the multiplicand, and that product (shifted eight bit positions to the left) is added into the first partial product to form the new partial product. And so forth, for five more cycles. It's almost like our decimal-multiplication example of Figure 1, except that instead of base-10 decimal digits we now have base-256 superdigits.

The fully-parallel approach totally applies Cray's usual design philosophy (sometimes characterized as "big, fast, and simple") at the systems level. It uses 49 '558s, in seven ranks; the 'i'th rank performs an operation corresponding to that done during the 'i'th cycle in the serial-parallel implementation. In principle, a complete mill is used to add the outputs of one rank of '558s to those of the rank above it. Or, alternatively, these mills can be laid out in a "tree" arrangement, such as:


Figure 9. "Tree" Summing Arrangement of Mills for a $56 \times 56$ Cray Multiplier

Each letter stands for one rank of '558s, and each " + " stands for a mill of the indicated length. More involved "Wallace-tree" techniques are usually preferable. (See reference 3). If the least-significant half of the double-length product is never needed, only 34 'S558s are required. There is one subtlety which needs to be mentioned. If, conceptually, a '558 looks like a diamond -


Figure 10. A Single '558 in "Diamond" Notation
then, the $8 \times 56$ multiplier for the serial-parallel configuration (which is also one rank of the fully-parallel configuration, which has seven such ranks) looks like this:


Figure 11. $8 \times 56$ Cray Multiplier in "Diamond" Notation
As you may discover after a moment's thought, each slanted double line in Figure 8 calls for addition of the outputs of two '558s - the eight most significant bits of one, and the eight least-significant bits of the next one to the left. There must also be an extra adder (or at least a "half adder") to propagate the carries from this addition all the way over to the left end of the result. The upshot is that an extra 56-bit mill is needed, in addition to the '558s. The eight least-significant bits of the leastsignificant ' 558 do not have to go through this mill, since they do not get added to anything else.

One final note: building up a large Cray-multiplier configuration out of '558s requires a lot of full adders, or else a lot of something else equivalent to them. Monolithic Memories also makes 74S381 (a 4-bit "ALU" or "Arithmetic Logic Unit") and the 74S182 (a carry-bypass circuit which works well with the '381); and two faster ALUs, the 54/74F381 and the 54/74F382 are in design. These ALUs and bypasses are excellent building blocks from which to assemble the mills used for summation within a rank of ' 558 s , and also the mills used for tree-summation of the outputs of all ranks. For how to put together one of these mills using '381s, '382s, and '182s, see reference 1. For how to use PROMs as Wallace trees, see reference 3.

Now you can go ahead, design your Cray multiplier out of '558s, and start multiplying full-length numbers together in a fraction of a microsecond. Sound like fun?

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NOTE: All of these references are available as application notes from Monolithic Memories Inc.

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## 8-Bit Interface

| MILITARY PART NUMBER | FUNCTION | POWER | POLARITY | FEATURE |
| :---: | :---: | :---: | :---: | :---: |
| SN54LS240 | Buffer | LS | Invert | - |
| SN54LS241 | Buffer | LS | Noninvert | - |
| SN54LS244 | Buffer | LS | Noninvert | - |
| SN54S240 | Buffer | S | Invert | - |
| SN54S241 | Buffer | S | Noninvert | - |
| SN54S244 | Buffer | S | Noninvert | - |
| SN54LS245 | Buffer Transceiver | LS | Noninvert | - |
| SN54LS273 | Register | LS | Noninvert | Master Reset |
| SN54LS373 | Latch | LS | Noninvert | - |
| SN54S373 | Latch | S | Noninvert | - |
| SN54LS374 | Register | LS | Noninvert | - |
| SN54S374 | Register | S | Noninvert |  |

# Pick the Right 8-Bit - or 16-Bit - Interface Part for the Job 

Chuck Hastings and Bernard Brafman

## Introduction

A few years ago, 20-pin 8-bit buffers, registers, latches, and transceivers came into existence as a rather haphazard upwards evolution from the MSI devices available in the mid-1970s. As time went on, usage of these parts increased until they became one of the fundamental computer-system building-block "primitives"-the "glue" which holds the entire system together. System designers demanded, and semiconductor manufacturers provided, many refinements such as inverting outputs to reduce parts count in assertive-low-bus systems, high-drive outputs to rescue designs with overloaded buses, Schmitt-trigger inputs to likewise rescue designs troubled with severe bus noise, high-voltage outputs specifically suited for driving MOS inputs, seriesresistor outputs for driving highly-capacitive loads such as dynamic-MOS address buses, and so forth.
Today the demands are to reduce component costs and system board area. Reducing parts count achieves both of these objectives at one stroke. With the development of the 300-mil 24-pin SKINNYDIP ${ }^{\text {m }}$ package, it is now possible to effectively incorporate the equivalent of two 20 -pin 8 -bit interface parts into one 24 -pin " 16 -bit interface" part. The approach is to look for common configurations of pairs of 8 -bit parts, and implement the pair as a single chip. Common configurations include back-to-back "registered (or latched) transceivers," with the same options already available in the 20-pin 8-bit parts read back registers or latches, and pipelined registers or latches.

## Interface Basics

Where Do Interface Circuits Fit In?
Interface circuits appear as unglamorous bread-and-butter commodity items, as compared to many of the other more complex integrated circuits of today: their sales volume is very high, their average selling price is comparatively low, and essentially interchangeable parts are offered by several suppliers. They have the humble role of being the "glue" which holds digital systems together; they are means rather than ends in themselves.
When preliminary system block diagrams turn into detailed schematics, the blocks turn into complex circuits microprocessors, multipliers/dividers, automatic dynamicMOSRAM refresh controllers, high-speed FIFOs, program-mable-logic circuits, arithmetic-logic units, and so forth. But then, however, the lines between those blocks turn into interface circuits, which must be there in the final design but never explicitly get noticed during the conceptual-design stage!
The term "interface" is actually a bit of a misnomer, since it implies that these parts always occur at a boundary between two somewhat different types of logic. That may have been true once, and it is still true that many of the circuits commonly called "interface" have inputs and/or outputs which are different electrically from those of, say, triple three-input NAND gates produced using the identical solid-state-circuit technologies. But a general working definition of "interface circuits" also has to cover some other parts which get used

in similar system roles, but have normal inputs and normal totem-pole or three-state outputs. One such definition, current today at Monolithic Memories, is
". . . ultra-high performance integrated circuits which do not lend themselves to higher levels of integration, due either to their parallel data structure or to the electrical properties of their inputs and/or outputs."
Interface circuits get used wherever data must be held, transmitted on demand, power-amplified, level-shifted, read from a noisy bus, inverted, or otherwise operated upon in some simple electrical way. If more complex transformations of the data are called for, of a predominantly mathematical rather than electrical nature, the designer will typically try to perform the required operations with readymade LSI or MSI circuits. Even here, of course, interface circuits often have the inconspicuous but crucial role of performing format conversion so that several LSI circuits can communicate with each other. Still, they are viewed as "overhead," which system designers try to minimize and semiconductor producers often rank well below their top level of corporate priorities.
But interface circuits are here to stay, at least for several more years. And the realization is growing among both users and producers of semiconductors that, since interface parts are not about to vanish soon, they need to be treated as something more than afterthoughts to the design process. Users who select interface circuits shrewdly are achieving real gains in system performance and reliability, and significant reductions in system size, weight, and power consumption. Producers who do a conscientious and professional job of developing and marketing these humble parts are finding increased demand for their wares, even during recessions.

Two major trends currently evident in the world of interface circuits are:

- The emergence of an orderly, matrix-like approach to interface products, so that taken all together they form an array rather than simply a splendid jumble of assorted types.
- A strong emphasis on increasing the number of data bits which can be handled or accomodated by a single interfacecircuit package.

This paper will discuss each of these trends in some detail, and will then go on to present some realistic interface applications based on several actual designs.

## What Kinds of Interface Circuits Are There?

Commonly, the label "interface circuit" is applied to any of a diverse collection of miscellaneous devices which don't seem to fit into any other classification. As the term is used here, however, it means either one of three basic 8 -bit types-buffers, latches, and registers - which are simple interface circuits, or else one of several 16-bit compound interface circuit types such as transceivers and pipelines.
Buffers merely "pass" or transmit information at increased power levels.Most contemporary buffer circuits, including 20-pin 8-bit buffers, also have an electronically-selectable electrical-isolation capability. Such a three-state buffer has a type of output which can be switched into a "hi-Z" (highimpedance) state in which it does not drive, nor appreciably load, the circuit node to which it is attached.
True or noninverting buffers pass the input information along with the same polarity (i.e., conventions in the representation of ones and zeroes by high and low voltages) that it had when it was received. Inverting buffers reverse the polarity of the input information from what was received, complementing all ones to zeroes and all zeroes to ones.

Most buffers feature standard PNP inputs. However, the 'S/'LS340/341/344/310 buffers feature Schmitt-trigger inputs, with a guaranteed 300/400-millivolt deadband (typically twice that) centered about the switching threshold voltage. (This notation is shorthand for " $54 / 74 \mathrm{~S} 340,54 / 74 \mathrm{~S} 341,54 / 74 \mathrm{~S} 344$, 54/74S310, 54/74LS340, 54/74LS341, 54/74LS344 and 54/74LS310;" and will be used frequently hereafter.) These Schmitt-trigger buffers won't respond to input noise pulses which would make buffers with normal inputs start to switch, as long as the noise pulses do not completely cross the deadband; thus noise immunity is improved.


Latches and registers have the same basic capability as buffers, but also have the additional capability that they retain stored information as long as power is supplied to them. Each of these circuit types requires an additional controi signai in order to periorm its system function.
More specifically, latches use an enable signal. When this signal is on, they store information, and their outputs do not change even if the information presented to their inputs changes. When their enable signal is off, latches act just like buffers. Turning on the enable signal in effect "freezes" in place whatever information was passing through the latch, so that the latch stores it.
Registers use a clock signal instead of an enable signal. When the clock signal goes through a transition from off to on, this "rising edge" causes the information present at the
inputs to be stored in the register, and then to remain present at the register outputs until another rising edge occurs. When the clock is in a steady-state condition (a "level"), either on or off, or even when the clock goes through a transition from on to off (a "falling edge"), the outputs of the register do not change. Thus, unlike latches, registers lack a mode in which they act exactly like buffers and pass information directly from their inputs to their outputs. This lack is a consequence of the control signal being "edge-sensitive" rather than "level-sensitive."
Transceivers are bidirectional interface circuits capable of interconnecting two buses so that information can pass in either direction. Most of the transceiver parts in production today are buffer transceivers - they are like two crosscoupled buffer circuits within a single 20-pin package. A 16-bit buffer transceiver has eight A-bus data pins and eight B-bus data pins. Either the A-to-B buffers may be enabled, or the B-to-A buffers, or neither; if both sets of buffers were to be enabled, obviously there would be a race condition on each of the data lines, and so the control structure of some buffer transceivers specifically disallows that mode of operation. (Some other types do allow it.) Buffers which are not enabled are, of course, in the hi-Z state. Thus each buffer transceiver interface circuit consists of eight logical elements, and each of these logical elements consists of two simple-buffer elements cross-coupled back-to-back so that the input line for one is the output line for the other and conversely.
Latch transceivers and register transceivers are now positioned to become major factors in the marketplace; several semiconductor houses now offer such devices. In particular, Monolithic Memories now supplies several different families of these devices in the 24 -pin 300-mil SKINNYDIP® package; some of these families are also supplied by Texas Instruments. A variety of speeds and architectures are available; see section 12 of this Databook for details.
Pipelines are unidirectional interface circuits having more than one full-width internal latch/register or"stage," but typically having just one set of parallel data inputs and one set of parallel data outputs. Two-stage latch pipelines, and both two-stage and four-stage register pipelines, are available. The four-stage devices can store twice as much information per package, but the two-stage devices can be reconfigured more flexibly and have a greater degree of separate control for each stage.

## Understanding and Using Interface

How Designers Choose Interface Circuits
In the real world, a digital-logic designer doesn't set out deliberately to use some particular interface circuit whose properties he has carefully learned, in the same way that he might for instance set out to use a bit-slice registered ALU or a multiplier/divider. Rather, as we have said, it is much more likely that it all starts with some innocent-looking little line between two blocks on his preliminary system block diagram which, it turns out, can't really be just a simple little line after all.
Maybe the data which travels on that little line goes away at the source unless the little line is actually also capable of seizing it at the proper time and remembering it. Or maybe the end of the little line is an assertive-low system bus, with enough loads hanging off it to call for almost 30 milliamps of drive capability in whatever contemplates driving the bus, which doesn't quite jibe with the 2 -milliamp drive capabilities and assertive-high outputs of the MOS LSI device from which the data is coming.

At this point the designer needs an interface circuit, andwittingly or unwittingly - he must go through a several-stage decision process to determine what interface circuit he needs to actually implement that little line, before his block diagram can turn into a system. He must also fervently hope that, by the time he gets to the final twig on his decision tree, the interface part he needs will turn out to actually exist. Figure 1 is an example.
A top-down design approach, as illustrated in Figure 1, isn't always wise with integrated circuits, simply because the chances are fairly good that the desperately needed circuit actually won't exist ${ }^{11}$. And there was a time, not all that long ago, when only a quasi-random subset of all of the obviously possible variations of the basic interface parts had reached full production status, so that they could be bought and plugged in. The hapless designer just had to memorize what that subset was, and do his design bottom-up from there.
Today, chaos is giving way to order, and enough of the possible interface parts which a designer might want do by now exist (or will exist shortly) that the kind of top-down thought process portrayed in Figure 1 really will work out all right when designing with interface. For instance, the line of interface parts now in production at Monolithic Memories is sufficiently orderly to be ordanizable into the matrix of the Interface Selection Guide on page 11-3 of this databook. Although this Guide is still somewhat irregular, it is at least recognizable as first-cousin to a logic-design Karnaugh map, and you can actually get your hands on any of the interface parts in the matrix.


Figure 1. Interface-Circuit-Selection Decision Tree
The dimensions of variation for interface parts in any such Karnaugh map are, of course, two-valued "Boolean" variables. It is realistic from both logical and historical viewpoints to consider that all of the interface parts of the Inter-
face Selection Guide have been derived from a very few basic types, by implementing those combinations which make sense of several two-valued properties of interface parts. These are:

- Commercial versus military temperature-range operation.
- High-speed Schottky (S-TTL) or low-power Schottky (LS-TTL) speed/power range.
- Noninverting or inverting outputs.
- No memory capabilities in the logical elements, so that they operate as buffers; or memory capabilities therein, further subdivided according to whether the logical elements operate as latches or registers.
- Compound 16 -bit interface circuits or simple 8 -bit interface circuits.
- Hi-drive or standard levels of current-sinking capability ( $\mathrm{I}_{\mathrm{OL}}$ ) at the outputs.
- Schmitt-trigger or standard inputs.
- For non-three-state parts, master-reset or clock-enable control inputs.
- Series-resistor or standard outputs.

Obviously, not all imaginable combinations of the above properties actually exist as parts, or would even be useful if they did; and semiconductor houses cannot afford for long to offer $2^{n}$ interface-circuit part types for rapidly increasing n . Moreover, certain of the properties which in the past have had just two possible major choices (e.g., S-TTL and LS-TTL) today have more than two; for instance, Section 12 of this Databook includes some CMOS parts.
Nevertheless, by now the matrix approach has been fullyenough implemented to offer a very helpful perspective to the working designer.
Part numbers today allow some of the properties of interface circuits to be directly inferred, at least if the part number follows the conventions of the industry-standard " $54 / 74$ " numbering series. 54/74 part numbers have a well-defined format VVE4TxxxP, with the following interpretation:

- VV - a prefix which varies somewhat from vendor to vendor.
- E4 - a temperature-range environmental specification.
" $54^{\prime \prime}$ implies the military temperature range $\left(-55^{\circ} \mathrm{C}\right.$
to $\left.+125^{\circ} \mathrm{C}\right)$, and " $74^{\prime}$ the commercial temperature
" $54^{\prime \prime}$ implies the military temperature range $\left(-55^{\circ} \mathrm{C}\right.$
to $\left.+125^{\circ} \mathrm{C}\right)$, and " $74^{\prime}$ the commercial temperature range $\left(0^{\circ} \mathrm{C}\right.$ to $+70^{\circ} \mathrm{C}$ for several vendors, and $0^{\circ} \mathrm{C}$ to $+75^{\circ} \mathrm{C}$ for Monolithic Memories). In any case, interface circuits must run properly over a very wide temperature range.
- T - a solid-state-circuit technology. Upwards of a dozen
of these have been promoted, with widely varying success, during the last decade. The earliest one, plain old gold-doped TTL, omitted using any special letter in part numbers. Today, the two dominant technologies are " $S$ " (high-speed Schottky) and "LS" (Low-power Schottky). Others becoming quite important include " $F$ " (for "FAST," a lower-power form of high-speed Schottky); "ALS" (advanced low-power Schottky); and "SC," "HCT" and "ACT" (isoplanar CMOS processed to be fully TTL-voltage-level compatible).
- xxx - a two-digit, three-digit, and today sometimes even four-digit number which uniquely specifies the pinout of the part and its "functional behavior" (see the explanation which follows), independent of speed/ power range. L es


Figure 2. Pinouts for the Three Basic 20-Pin Interface Parts

- P - a package type: plastic, cerdip, flatpack, leadless chip carrier, sidebrazed ceramic, small-outline surface-mount, or whatever.

The functional behavior of a circuit can be defined somewhat circularly as "what a designer needs to know about the circuit in order to construct designs which operate properly using parts from any supplier interchangeably." This definition is akin to one classic definition of computer architecture as "...the structure of the computer a programmer needs to know in order to be able to write any program that will correctly run on the computer."'2

"... INTERFACE CIRCUITS MUST
RUN PROPERLY OVER A VERY WIDE TEMPERATURE RANGE ...
Two parts produced using different solid-state-circuit technologies may exhibit essentially the same functional behavior. If that is the case, and if either part will also satisfy system timing constraints (which is an issue quite separate from that of "functional behavior") and input/output voltage compatibility constraints, the designer does not need to care what kind of internal gates are used within the part-Schottky TTL, ECL, CMOS, NMOS, or water wheels. On the other hand, two parts produced using the same technology may have subtle, or even drastic, differences in their functional behavior; for example, one may have inverting outputs, or hi-drive outputs, or Schmitt-trigger inputs whereas the other does not.

## The Matrix of Interface Part Types

The interface parts of the Interface Selection Guide mostly have one of just three different pinouts, shown in Figure 2, in their usual 20-pin plastic or cerdip SKINNYDIP form.

All of the buffers have the same pinout as the 'S240. They differ in speed/power range, in the polarity of the outputs, in the noise-rejection capabilities of the inputs (Schmitttrigger or standard), and in enable structure (complementary or assertive-low) as shown in Figure 3, which really is unequivocally a Karnaugh map.


Figure 3. 8-Bit Three-State Buffers

Most of the latches and registers have the same pinout as the 'S374. They differ in whether the memory control line is level-sensitive (latch) or edge-sensitive (register), in speed/power range, in the polarity of the outputs, and in the IOL (current-sinking drive) capability of the outputs as shown in the Karnaugh map of Figure 4.


Figure 4. 8-Bit Three-State Latches and Registers

The three transceivers of the Interface Selection Guide are more specifically buffer transceivers-compound 16-bit interface circuits like two 8 -bit buffer circuits cross-coupled "back-to-back" within a single device. They differ in inputcurrent and output-leakage-current specifications, which here are indistinguishable for test purposes since every data pin is both an input and an output; the 'LS245 specification is tighter. (The 'LS245-1 is also specified as faster, but that is not a difference in "functional behavior.") There is also a difference in $\mathrm{I}_{\mathrm{OL}}$ capability; the 'LS645-1 is specified as higher. Actually, all three devices undergo identical fabrication, and are separated only at final testing; for instance, those 'LS645s capable of meeting the $48-\mathrm{mA} \mathrm{I}_{\mathrm{OL}}$ specification in both directions drop into a separate bin.
Upcoming developments in interface parts will tend in many cases to follow the matrix approach, at least partially. Even where the new parts do not fit perfectly into the matrix of existing parts, some attention is likely to be paid to issues of balance and symmetry over the entire interface-circuit


In some cases, new interface parts directly "fill in the holes" in the matrix. For instance, some recent additions to Monolithic Memories' line of interface parts are:

| Function | Speed/ <br> Power | Polarity | Feature | Part Number |
| :--- | :---: | :---: | :---: | :---: |
| Register | S | Noninv. | Master <br> Reset | SN54/74S273 |

Table 1. Recent Additions to the Monolithic Memories Inter-face-Part-Type Matrix

"... THE 'S273 AND 'S377, LIKE THEIR LS-TTL COUNTERPARTS, ARE DESIGNED WITH STANDARD TTL 'TOTEM-POLE' OUTPUTS..."

The 'S273 and 'S377 bring to higher-performance TTL systems the same functional behavior which has long been available for medium-performance TTL systems, with the popular 'LS273 and 'LS377 parts. The 'S273 and 'S377, like their LS-TTL counterparts, are designed with standard TTL "totem-pole" outputs. Somehow, in the somewhat more chaotic early days of 8 -bit interface, the need for high-speed Schottky versions of these parts got overlooked by most interface producers.
Since the 'S273 and 'S377 are totem-pole-output parts, the control pin which gets used on the 'S374 (whose pinout they otherwise follow) for "Output Enable" for the three-state outputs is available for something else. The 'S273 uses it as a "Master Reset" (MR) input, capable of forcing all of the eight $D$-type flipflops on the chip into the off (low) state simultaneously, regardless of their previous state-or of the state of the clock line and/or the data-input lines. The 'S377, on the other hand, uses that same pin as a "Clock Enable" (CK EN) input, which in effect either allows the clock signal to reach the eight D-type flipflops on the chip, or else cuts it off from reaching the flipflops so that they are not clocked and just sit there holding whatever information they contained previously. The 'S383 is a slight modification of the 'S377 to provide open-collector rather than totem-pole outputs.
The major applications for these parts are in situations where 'S374s would be difficult to control appropriately. Because of the 'S273's MR input, its forte is control applicationsinstruction registers, microinstruction registers, timingpulse registers, and sequential circuits in general, and sometimes as eight individual separate D-type control flipflops in one package. In all of these applications, there has to be a way to force the system into some proper initial state, so that it "starts off on the right foot" and does not get into some unplanned-for, untestable, unpredictable machinepsycho condition on power-up. The S377, on the other hand, because of its CKEN input, is the optimum choice for the highest-performance TTL pipeline paths for data, instructions, microinstructions, and address parameters in "overlapped-architecture" machines such as array processors and high-performance minicomputers. Its opencollector counterpart, the 'S383, can be used to drive opencollector buses or to provide wired-OR or wired-AND logic functions.
The 'S700, 'S730, 'S731, and 'S734 feature a new type of output stage incorporating a series resistor, designed to efficiently drive highly-capacitative loads such as arrays of dynamic-MOSRAM inputs. Rise and fall times are more

## Pick the Right 8-Bit or 16-Bit Interface for the Job

symmetric than with 'S240-type buffers, and the latter need an external series limiting resistor for their own protection when driving highly capacitative loads.
Consequently, although 'S240-type buffers may exhibit greater speed when tested under light loading conditions, 'S730-type buffers are likely to perform better under realistic system conditions when driving large distributed capacitative loads is a major factor in the application.
Of these four new buffers, two - the 'S730 and 'S734-are second-source versions of the Am2965 and Am2966 respectively, originally introduced by AMD. The other two - the 'S700 and 'S731 - are complementary-enable versions of the 'S730 and 'S734 respectively, just as the 'S210 and 'S241 are complementary-enable versions of the 'S240 and 'S244 respectively. Complementary-enable buffers excel in driving buses with two multiplexed sources for the information, such as instruction addresses and data addresses in a bit-slice bipolar microcomputer system.

The four 'S730-type parts may be grouped with Monolithic Memories' line of conventional and Schmitt-trigger-input buffers in a $2 \times 2$ matrix chart or Karnaugh map, with the dimensions of this map chosen to be the polarity of the second-buffer-group enable input $E_{2}$ (here across the top) and the polarity of the data-buffer logical elements themselves (here down the side), thus:


* Since $\bar{E}_{1}$ is assertive-low for all of these parts, the parts with an assertive-low $\overline{E_{2}}$ are "assertive-low-enable" parts, whereas the parts with an assertivehigh $\mathrm{E}_{2}$ are "complementary-enable" parts.

Table 2. 8-Bit Buffers Grouped by Polarity and Enable Structure

By this time, many presently-unused SN54/74xxx part numbers have already been reserved for other potential new parts, even though not all of these parts are yet in production. Nevertheless, it was at least possible to part-number these four series-output-resistor buffers in such a way that the relationship among the four types remains the same as for 'S240-type buffers. To state this another way, one can add 490 to the last three digits of the usual buffer part number to get the part number for the corresponding series-outputresistor part, e.g., 'S241 + 490 = 'S731, etc.

## Directions In The Evolution of Interface Parts

## More Bits per Package

Historically, the first interface parts were 16-pin TTL devices offered during the early 1970s, usually with four or six "logi-
cal elements" per package. One "logical element" handles one data bit; in simple interface parts, a logical element may be a buffer, a latch, or a register (with "register" here implying an edge-triggered flipflop).

As the digital-electronics industry shifted from MSI to LSI integrated circuits, and from the quaint and irregular oldtime computer word lengths to word lengths which are multiples of eight bits (most often 8,16 , or 32 ), 8 -bit interface devices became the only way to go for simple electrical data transformations - chip counts got intolerably high with 4-bit devices, and 6-bit devices were awkward misfits in most of the newer designs! 3 And, to have eight input data lines, eight output data lines, power and ground, and two control signals, an integrated-circuit package has to have 20 pins.
To conserve board space, the width of this 20-pin package was chosen to be 300 mils (.300") like that of the overwhelming majority of the then-existing bipolar MSI and SSI devices. Hence, during the 1970s, the present 20-pin 300-mil SKINNYDIP package became the standard for interface circuits. One 20-pin SKINNYDIP takes up only about half as much board space as one of the older 600-mil 24-pin packages, which were then being used for a few early 8-bit interface parts such as the Intel 8212.

"...ONE 2O-PIN SKINNYDIP™ TAKES UP ONLY ABOUT half as much board space as one of the older 600-MIL 24-PIN PACKAGES . . ."
24-pin interface parts were obviously the next major development to come. In the early 1980s, mechanical packaging problems which previously had inhibited the introduction of a 24-pin $300-\mathrm{mil}$ SKINNYDIP were solved, and this package is now also in widespread use for PROMs, PAL programmable-logic circuits, and so forth. So what might one do with four additonal pins in an interface part?
One answer is to spend all four of them for additional control signals in order to achieve more flexible parts, such as the Monolithic Memories SN54/74LS380 "multifunction" 8-bit register. (See page 6-16 of this databook.) This part is actually implemented with "hard-array logic" technology, and has an internal structure like one form of PAL.
Another answer is to spend all four of them for additional data signals, equally for inputs and outputs. The result is 10-bit interface parts with functionality similar to that of existing 20-pin 8 -bit parts.
A middle-of-the-road answer is to divide them equally between control signals and data signals. This approach leads to 9-bit interface parts with improved functionality

16-bit "double-density" interface-circuits - dual 8-bit circuits in a single 24 -pin SKINNYDIP - are a more farreaching answer than the preceding ones. These circuits use the four extra pins to provide separate control inputs for both 8 -bit internal groups, and also to provide improved functionality. The number of data pins is held at 16 by multiplexing the use of two 8 -bit groups of input and/or output pins.

The motivation for 16-bit interface parts is, first of all, to cut component counts by replacing two parts with one in as many situations as possible, in order to save board space and assembly costs. Particularly in high-performance computers and array processors, the packaging itself is expensive when it must be designed to provide a proper signaltransmission environment for ultra-fast logic. An almost-50\% cut in the board area required for the interface parts-here, as always, the "glue" which holds the whole system together-may result in major indirect savings.
But there are other incentives besides sheer cost reduction which favor cramming as much logic as possible into a given board area. There usually is only one board size in a chassis (or even in a system), and any logic subsystem which cannot fit onto one such board immediately incurs a speed penalty attributable to board-to-board communications-extra buffers for noise-free signal transmission, extra signal-path length on each board over to the edge where the connectors are, more extra length in the backplane wiring, and lots of additional inductance and capacitance permeating all of the above.
So, saving board area is very likely to improve both system cost and system performance, by increasing the probability that a given logic subsystem will fit onto just one board.

Interface-part internal element density has for many years been increasing at a rate which is, to say the least, unspectacular. Going from four to six to eight to sixteen logical elements in an interface-circuit package doesn't seem like a whole lot, compared for instance to going from 1 K to 4 K to 16 K to 64 K to 256 K bits in a single dynamic-MOSRAM package in roughly the same number of years.
But, consider what a true LSI interface circuit would have to look like-one with the same magnitude of "equivalent gate count" being bandied about for today's microprocessors, dynamic MOSRAMs, and so forth. First of all, it would need to have several hundred data inputs and several hundred data outputs, so that the most immediately-plausible mechanical design for a package would resemble a sea urchin! And, if it were implemented using any present-day TTL technology, the part would dissipate enough watts to need cooling fins like a Porsche cylinder head!

And so it has turned out that progress over time in increasing the logical-element density for interface parts has been more or less linear, while progress in increasing the level of integration for microprocessors and dynamic MOSRAMs has been more or less exponential. It is no accident that a basic phrase of the definition for "interface circuits" quoted earlier in this paper is ". . . which do not lend themsives to higher levels of integration . . ." If these same density trends continue, digital electronic systems of the future may actually have a higher proportion of packages allocated to interface circuits than is typical today, which if it happens is likely to surprise quite a few people.

## Structure of 16-Bit Interface Circuits

Common configurations of two 8-bit interface parts used together furnish a natural starting point for the definition of useful 16 -bit interface parts. When the same configuration tends to occur over and over again, it is natural to "draw a boundary around it and put it all on one chip," unless of course the resulting compound chip turns out to need too many pins.

Figure 5 illustrates three such two-part configurations which are observably very common, and intuitively very plausible:

- "Back-to-back" or "cross-coupled." (Figure 5A).

■ "Nose-to-tail" or "pipelined." (Figure 5B.)
■ "Side-by-side" or "parallel." (Figure 5C.)


Figure 5A. Back-to-Back Configuration


Figure 5B. Nose-to-Tail Configuration


Figure 5C. Side-by-Side Configuration
Figure 5. Common Configurations of Two 8-Bit Interface Parts

The back-to-back configuration, when applied to simple 8-bit buffers, leads to buffer transceivers such as the 'LS245. The 'LS245 is, of course, still a 20 -pin part; the choice was made to change its enable structure from that which would be strictly implied by placing two 'LS244s back-to-back, in order to hold the package size to 20 pins and to disallow having both directions simultaneously enabled. These same statements continue to hold for the 'LS645 and 'LS645-1. The 'LS640 and 'LS640-1 are inverting buffer transceivers, and the LS643 and LS643-1 incorporate an 8-bit inverting buffer back-to-back with an 8-bit noninverting buffer; there are also open-collector equivalents to these parts and the 'LS645 and 'LS645-1. The entire series features the same
enable structure, with a master enable line E controlling both sets of buffers and a direction line DIR to allow just one direction to be enabled at a time.


Figure 6. Two-Stage Pipeline Register Configuration
Applied to 'LS373 latches and 'LS374 registers, the back-to-back configuration leads to the 24-pin 'LS547 latch transceiver and the 'LS546 register transceiver respectively. These parts are just what one would expect them to be, with individual output-enable and clock control inputs for each 8 -bit group, except that there are enough pins to also give each group clock-enable control inputs like the 'S377. The 'LS567 and 'LS566 are the corresponding inverting parts.

The nose-to-tail and side-by-side configurations do not lead to anything very interesting with buffers, at least as long as there are only enough pins for one 8 -bit input data path and one 8-bit output data path. Latches and registers, however, are entirely another matter. It turns out to be attractive to combine these two configurations, even though at first glance they look quite dissimilar, into a single "two-stage pipeline" configuration as shown in Figure 6. Such a twostage pipeline can operate in either a nose-to-tail mode or a side-by-side mode, according to the setting of the two internal multiplexers shown in Figure 6. Applied to 'LS373 latches and 'LS374 registers, this more powerful configuration leads to the 24 -pin 'LS549 latch pipeline and the 'LS548 register pipeline. For these parts, the control inputs are a final-stage output enable, selects for each mux, a common clock (or latch-enable for the 'LS549) input for both stages, and individual clock-enable inputs for each stage.

To clarify the timing control of these parts, the 16-bit register parts ('LS546, 'LS566, and 'LS548) have individual clockenable signals for each 8 -bit group, and either individual clock signals ('LS546 and 'LS566) or a common clock signal ('LS548). The 16-bit latch parts ('LS547, 'LS567, and 'LS549), since the "clock" signal turns into a level-sensitive latchenable signal, have two independent ways of enabling storage in each of the two stages. Thus, the 'LS547 and 'LS567 parts feature two separate and equivalent latch-enable control inputs for each 8-bit group, either one of which can cause the group to "latch up" and store information. The 'LS549 part has the same operating mode, except that each 8 -bit group has one separate latch-enable control input and there is one more latch-enable input common to both groups. Read-back latches and registers ('LS793 and 'LS794) also have a back-to-back structure; but their "return" element is a buffer (resembling, say, a '244), rather than another latch or register.

As with other TTL 8-bit latches and registers, the part-numbering scheme for all of the parts just mentioned assigns odd numbers to latches and even numbers to registers.
Front-loading latches are one other type of 16-bit interface part. The 'LS646 (noninverting) is to a first approximation an LS645 superimposed upon an 'LS546. (The numbering scheme wasn't planned to be that cute-it just happened.) The 'LS648 is a similar inverting part. To clarify what is
meant, each of the eight logical elements of an 'LS646 consists of two back-to-back buffers and two back-to-back flipflops, with a parallelled buffer and flipflop pointing in the A-to-B direction and a similar buffer-flipflop pair pointing in the B-to-A direction. The 'LS646 and 'LS648 are three-state parts: the 'LS647 and 'LS649 are respectively the equivalent open-collector parts. The 'LS651 (inverting) and the 'LS652 (noninverting) are equivalent to the 'LS648 and 'LS646 respectively, but have a different control structure which allows independent enabling of either direction; the 'LS653 and 'LS654 are versions of the 'LS651 and 'LS652 respectively in which the A-direction output buffers are open-collector, and the Bdirection buffers are still three-state.
32-bit interface parts are also visible on the horizon. Two four-stage pipelines, the Am29520 and Am29521, are offered by AMD as members of a series of signal-processing parts, and Monolithic Memories is introducing them also as the 'S720 and 'S721. As compared to the 'LS548 and 'LS549, they offer twice as many stored bits per square inch of board, but considerably less flexibility in accessing and controlling register contents.
The matrix approach to classifying various interface parts can be extended to encompass transceivers and pipelines, as is done in Table 3. The correspondence between the various 8 -bit simple-interface parts and the 16 -bit compound interface parts which are in a sense derived from them, is summarized in Table 4.

| Configuration | Buffers | Latches | Registers | Front Loading Latches |
| :---: | :---: | :---: | :---: | :---: |
| Simple | '210'310 | '373 '531 | '374 '532 | --- |
|  | '240'340 | '533 '535 | '534 '536 |  |
|  | '241 '341 |  |  |  |
|  | '244 '344 |  |  |  |
| Back-toBack | '245 | $\begin{aligned} & \text { '547 } \\ & \hline \end{aligned}$ | $\begin{array}{r} \mathbf{5} 56 \\ \mathbf{\prime} 566 \end{array}$ | '646 '647 |
|  | '640 '640-1 |  |  | '648 '649 |
|  | '643 '643-1 |  |  | '651 '652 |
|  | '645 '645-1 |  |  | '653 '654 |
| Two-Stage | --- | '549 | 548 | ---- |
| Pipeline |  |  |  |  |

Table 3. Matrix Classification Scheme for 8-Bit and 16-Bit Interface Parts

| Simple Interface Type | Compound Interface Type | Number <br> Of <br> Pins | Buffer | Latch | Regis ter |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Transceivers: |  |  |  |  |
| '244 | $\begin{aligned} & 245 \text { '645 } \\ & 645-1 \end{aligned}$ | 20 | X |  |  |
| '240 | $\begin{aligned} & 640 \\ & 640-1 \end{aligned}$ | 20 | X |  |  |
| '240/'244 | $\begin{aligned} & 643 \\ & ' 643-1 \end{aligned}$ | 20 | X |  |  |
| '373 | '547 | 24 |  | X |  |
| '374 | '546 | 24 |  |  | X |
| '533 | '567 | 24 |  | X |  |
| '534 | '566 | 24 |  |  | X |
|  | Pipelines: |  |  |  |  |
| '373 | '549 | 24 |  | X |  |
| '374 | '548 | 24 |  |  | X |

[^54]
## Various Applications of Interface Parts

## Some Logic-Design Examples

Several illustrative designs using various interface parts may suggest some design insights and some creative ways to use interface. The designs presented have generally been excerpted from actual digital systems.
Reading a switch setting to establish an externally-defined system parameter, such as a device address, is a mundane but essential task in many microprocessor-based systems. Figure 7 illustrates how a group of eight switches may conveniently be read using a byte-wide buffer such as the 'LS244. Since the switches must be electrically isolated from the bus, the 'LS244's three-state outputs are disabled by control signals originated by the microprocessor until the time comes to read in the switch settings. Because the 'LS244 can supply up to 24 milliamps of loL to drive the bus, this simple scheme can be utilized even on heavily-loaded system data buses.
If still more drive capability is needed, an 'S244 in the same configuration can sink up to 64 milliamps. And, if the system is to be operated in an industrial environment and the switch signals entering the buffer inputs are subject to severe noise, the Schmitt-trigger 'LS344 type of buffer can also be substituted for the 'LS224 with no other change to the circuit.


Figure 7. Switch-Setting Readin Circuit
Interfacing two separate buses is a very standard application for transceivers. Figure 8 shows an 'LS245, which has a control structure such that one control signal selects the direction of data transfer and the other one independently allows data transfer to be enabled or disabled. Thus, the two buses can be operated totally isolated from each other, or else either one may be made to follow the other. Depending on the drive-capability and polarity requirements of the application, any of the other buffer transceivers might be used here instead. Or, if memory as well as cross-coupling is required, a latch transceiver or register transceiver might also be used in a similar manner.
Driving a dynamic-MOSRAM address bus with a multiplexed row/column address can conveniently be done with an 'S700 as shown in Figure 9. This part is an inverting complementaryenable buffer with a series-resistor output structure, which is an ideal combination of characteristics here.
First of all, a TTL inverting buffer normally has one less transistor - and hence one less delay - in its internal data path than does an equivalent noninverting buffer, and hence is faster. And dynamic MOSRAMs really don't care if their addresses come in "true" or "complemented" form as long as that form never changes.

Second, a complementary-enable buffer can easily multiplex two different address sources to the same set of outputs without introducing extra switching delay, or allowing a momentary "bus fight" condition, if the same control signal (here $\overline{\mathrm{CAS}}$ or "Column Address Strobe") is tied directly to both $\bar{E}_{1}$ and $E_{2}$ and the two 4-bit groups of outputs are tied together.
Finally, because of the internal series resistor in the'S700's output structure, this part (like the 'S730/1/4) can drive highly capacitative loads, of say up to 70 dynamic-MOSRAM inputs, without the need for external limiting resistors to control undershoot, resulting in a net system speed gain since signal rising and falling transition times remain symmetric. Otherwise, the effective logic delay of the buffer (which is simply the


Figure 8. Interfacing Two Separate Buses


Figure 9. Multiplexed Row/Column Address Drivers
worse of the two transition times would get degraded, since the use of an external series resistor would have greatly lengthened the low-to-high transition time.

Demultiplexing and holding address and data words for single-bus microprocessors is an application which takes advantage of the strong points of the S531 as shown in Figure 10. Since the 'S531 is a "transparent latch" and can operate as a buffer when necessary, the memory system designer can take advantage of the full time slots when the address and data signals are present on the microprocessor outputs. Because the address and data signals are then present for a longer period of time at the 'S531 outputs, it may be possible to use slower (and therefore less expensive!) memory devices than if edge-triggered registers had been used here instead. The three-state outputs of the 'S531 allow the designer to implement bidirectional data buses and DMA address schemes. Variations on this approach can use 'S373s if less drive capability is needed, or 'LS373s if less speed is needed as well; or 'S535s, 'S533s, or LS533s under the same respective circumstances if the address and data buses to be driven are assertive-low

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Figure 10. Address/Data Demultiplexer for Single-Bus Microprocessors
according to the system definition. If the data-bus interface needs to have latching capability also for data returning to the microprocessor, then 'LS547s are an excellent choice.
Synchronizing the state changes of a PROM-based control sequencer is easily performed using a register with a clock-enable feature, like the 'LS377 shown in Figure 11. In this simple sequencer, a 4-bit counter steps through the PROM addresses. The counter may be reset to address 0000 , or loaded with any 4 -bit address. The $32 \times 8$ PROM, with five address lines, allows for one external input as well as the four bits from the counter. The PROM outputs are pipelined using the 'LS377, which eliminates PROM output glitches, synchronizes the state changes of the sequencer with the system clock, and speeds up the effective cycle time. The availability of enable control inputs on both the counter and the 'LS377 allows forcing "wait" states, where both the counter and the register hold their current state for extended periods of time. If a higher-speed implementation of this design is needed, a 74 S 161 or 93 S 16 counter can replace the 74LS161, one of Monolithic Memories' new 63S081A ultra-speed $32 \times 8$ PROMs ( 15 nsec worst-case and 9 nsec typical for tAA, instead of 50 and 37 nsec respectively) can replace the 6331-1, and an 'S377 can replace the 'LS377.

## Saving Designs at the Last Minute, or Planning Ahead

Designs hanging out over the edge of unworkability can sometimes be salvaged without any redesign effort, by replacing standard interface parts with hi-drive, Schmitt-trigger-input, or even just inverting pin-compatible parts. Hi-drive parts such as the 'S532 or 'LS645-1 get dropped into 'S374 or 'LS645 sockets respectively late in the design cycle, when the designer suddenly discovers that he has hung several too many inputs on his main system bus. Schmitt-trigger-input parts such as the 'LS341 likewise get
dropped into 'LS241 sockets shortly after the designer has recovered from his first observation of his actual bus waveforms on a good laboratory oscilloscope-it's that or back to the old drawing board. And, when he suddenly remembers after laying out a tightly packed board that "Oh, xxxx, that particular bus is assertive-low," it's nice to be able to simply substitute an 'S534 for an 'S374 in a few places rather than having to find room for several inverter packages. So a designer who has learned to think of interface parts in terms of the matrix approach will now and then find a particularly quick route to saving his skin.


## Figure 11. Synchronous PROM-Based Control Sequencer

However, an astute designer may use hi-drive, Schmitt-trigger-input, and inverting parts quite deliberately in order to gain speed, economy, drive capability, or noise immunity. A number of the industry-standard buses in the microcomputer world are assertive-low; and inverting buffers, latches, and registers are much more appropriate for connecting these to a microprocessor, or to a bit-slice arithmetic unit, than non-inverting parts with extra inverters in series just to make the polarity come out right. Similarly, Schmitt-trigger hex inverters whose only function in the data path is to provide noise immunity can be eliminated by using 'LS340-type buffers, which also provide significant drive capability and three-state outputs. The need to parallel three-state drivers and registers and split drive lines, just for extra drive capability, can be reduced or eliminated by using hi-drive parts. And, in an obvious but not trivial switch, substituting a high-speed Schottky part for a low-power Schottky equivalent part can beef up drive capability considerably.


Figure 12. Flat-Cable Transmission Scheme Using Hi-Drive and Schmitt-Trigger-Input Interface Parts

Board-to-board signal transmission via flat cable is a particularly nice application for both hi-drive and Schmitt-triggerinput interface parts. The 32 -milliamp outputs of, say, an 'S532 are better matched to the characteristic impedance of flat cable (usually 100 to 120 ohms) than 20 -milliamp outputs would be. An adequate scheme, in many cases, for the

## Pick the Right 8-Bit or 16-Bit Interface for the Job

transmission of data from board to board uses 3M or similar flat cable. Every second cable wire is grounded at both ends for shielding, so that signal wires alternate with ground wires ("signal-ground-signal-ground"), and there is at least one ground wire at each edge of the cable. Signal wires are driven by $32-\mathrm{mA}$ hi-drive latches or registers, and the receivers are Schmitt-trigger-input buffers, and that's all there is to it - no resistors, capacitors, or black magic. For a strobe, clock, or control signal, a linear receiver such as a National Semiconductor 8837 is used together with a 180 -ohm series resistor and a 3300 -ohm shunt resistor to $\mathrm{V}_{\mathrm{cc}}$, as shown in Figure 12. This overall scheme is compatible with some Digital Equipment Corporation buses, and is good for transmission distances of up to 25 feet.


## Conclusion

Interface parts seem primitive alongside of LSI microprocessors and dynamic MOSRAMs, but they are inescapable and smart designers today have learned how to use them astutely. A powerful aid in doing so is to think of the set of interface parts as an array, which fits into a matrix whose dimensions are various circuit properties. Even though the rate of progress seems slow, the bit-density and functionality of interface parts is steadily increasing, and the time is approaching for designers to learn to take the next logical step and use 16-bit interface parts extensively in their systems, in order both to save cost and to improve overall system performance.

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## Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '241 combines multiplexer and driver functions


## Description

These 8-bit buffers provide high speed and high current interface capability for bus organized digital systems. The threestate drivers will source a termination to ground (up to $133 \Omega$ ) or sink a pull-up to $\mathrm{V}_{\mathrm{CC}}$ as in the popular $220 \Omega / 330 \Omega$ computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA ILL on the low-power Schottky buffers and 0.4 mA IIL on the Schottky buffers.
The '240 and '244 provide inverting and noninverting outputs respectively, with assertive low enables. The ' 241 also provides inverting and noninverting outputs, but with complementary (both assertive-low and assertive-high) enables, to allow transceive or multiplexer operation.

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | ENABLE | POLARITY | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS240 | J,L,W | Mil | Low | Invert |  |
| SN54LS241 | J,L,W | Mil | High- <br> Low | Non- <br> Invert | LS |
| SN54LS244 | J,L,W | Mil | Low |  |  |
| SN54S240 | J,L,W | Mil | Low | Invert |  |
| SN54S241 | J,L,W | Mil | High- <br> Low | Non- <br> Invert | S |
| SN54L244 | J,L,W | Mil | Low |  |  |

## Logic Symbols



## Function Tables

| E1 | E2 | 1A | 2A | 1Y | 2 Y | E1 | E2 | 1A | 2A | 19 | $2 Y$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| L | L | L | L | H | H | L | L | L | X | L | z |
| L | L | L | H | H | L | L | L | H | X | H | Z |
| L | L | H | L | L | H | L | H | L | L | L | L |
| L | L | H | H | L | L | L | H | L | H | L | H |
| L | H | L | $x$ | H | Z | L | H | H | L | H | L |
| L | H | H | X | L | Z | L | H | H | H | H | H |
| H | L | $x$ | L | Z | H | H | H | $X$ | L | Z | L |
| H | L | $x$ | H | Z | L | H | H | $x$ | H | z | H |
| H | H | X | X | Z | Z | H | L | X | X | Z | Z |

'244

| $\overline{\mathbf{E 1}}$ | $\overline{\text { E2 }}$ | $\mathbf{1 A}$ | 2A | 1Y | 2Y |
| :--- | :---: | :---: | :---: | :---: | :---: |
| $L$ | $L$ | $L$ | $L$ | $L$ | $L$ |
| $L$ | $L$ | $L$ | $H$ | $L$ | $H$ |
| $L$ | $L$ | $H$ | $L$ | $H$ | $L$ |
| $L$ | $L$ | $H$ | $H$ | $H$ | $H$ |
| $L$ | $H$ | $L$ | $X$ | $L$ | $Z$ |
| $L$ | $H$ | $H$ | $X$ | $H$ | $Z$ |
| $H$ | $L$ | $X$ | $L$ | $Z$ | $L$ |
| $H$ | $L$ | $X$ | $H$ | $Z$ | $H$ |
| $H$ | $H$ | $X$ | $X$ | $Z$ | $Z$ |

## IEEE Symbols



## Absolute Maximum Ratings


Input voltage .................................................................................................................... -1.5 V to 7 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to 5.5 V
Storage temperature $\quad$. ......................................................................................... $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$
Operating Conditions


## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST C | ONDITIONS | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.7 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2.0 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $V_{C C}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\Delta \mathrm{V}_{\mathrm{T}}$ | Hysteresis ( $\mathrm{V}_{\mathrm{T}_{+}-\mathrm{V}_{\mathrm{T}_{-}} \text {) }}$ |  | $V_{C C}=\mathrm{MIN}$ |  | 0.2 | 0.4 |  | V |
| IL | Low-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.2 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  | 0.1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}$ |  |  | 0.4 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\mathrm{I}_{\mathrm{OH}}=-3 \mathrm{~mA}$ | 2.4 | 3.4 |  | V |
|  |  |  | $\mathrm{I}^{\mathrm{OH}}=-12 \mathrm{~mA}$ | 2.0 |  |  |  |
| ${ }^{1} \mathrm{OZL}$ | Off-state output current |  |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 V \\ & \hline \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -20 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OS}$ | Output short-circuit current* |  | $V_{C C}=M A X$ |  | -40 |  | -225 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply Current | Outputs | $V_{C C}=M A X$ Outputs open | 'LS240 |  | 17 | 27 | mA |
|  |  | High |  | 'LS241, 'LS244 |  | 17 | 27 |  |
|  |  | Outputs |  | 'LS240 |  | 26 | 44 |  |
|  |  | Low |  | 'LS241, 'LS244 |  | 27 | 46 |  |
|  |  | Outputs <br> Disabled |  | 'LS240 |  | 29 | 50 |  |
|  |  |  |  | 'LS241, 'LS244 |  | 32 | 54 |  |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $\mathrm{vCC}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { 'LS240 } \\ & \text { TYP } \end{aligned}$ | MAX | 'LS241, 'L MIN TYP | $5244$ MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPLH | Data to output delay | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ |  | 9 | 14 | 12 | 18 | ns |
| tPHL |  |  |  | 12 | 18 | 12 | 18 | ns |
| tPZL | Output enable delay |  |  | 20 | 30 | 20 | 30 | ns |
| tPZH |  |  |  | 15 | 23 | 15 | 23 | ns |
| tPZL | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ |  | 15 | 25 | 15 | 25 | ns |
| tPHZ |  |  |  | 10 | 18 | 10 | 18 | ns |

## Absolute Maximum Ratings


Input voltage ............................................................................................................... -1.5 V to 7 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.5 V to 5.5 V
Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MIN | MILITARY <br> TYP | MAX |
| :---: | :---: | :---: | :---: | :---: | UNIT 

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST C | NDITIONS | MIN | $\begin{gathered} \text { MILITARY } \\ \text { TYP } \\ \hline \end{gathered}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  |  |  | 2.0 |  |  | V |
| VIC | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.2 | V |
| $\Delta \mathrm{V}_{\mathrm{T}}$ | Hysteresis ( $\mathrm{V}_{\mathrm{T}_{+}-\mathrm{V}_{\mathrm{T}_{-}} \text {) }}$ |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | 0.2 | 0.4 |  | V |
| ILL | Low-level input current | Any A | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $V_{1}=0.5 \mathrm{~V}$ |  |  | -0.4 |  |
|  |  | Any E |  |  |  |  | -2 | mA |
| 1 IH | High-level input current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 1 | Maximum input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOL}=48 \mathrm{~mA}$ |  |  | 0.55 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{IOH}^{\prime}=-3 \mathrm{~mA}$ | 2.4 | 3.4 |  | V |
|  |  |  | $\mathrm{IOH}^{\prime}=-12 \mathrm{~mA}$ | 2.0 |  |  |  |
| ${ }^{\prime} \mathrm{OZL}$ | Off-state output current |  |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ |  |  | -50 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  |  | 50 | $\mu \mathrm{A}$ |
| los | Output short-circuit current $\dagger$ |  | $V_{C C}=M A X$ |  | -50 |  | -225 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply Current | Outputs | $V_{C C}=M A X$ <br> Outputs open | 'S240 |  | 80 | 123 | mA |
|  |  | High |  | 'S241, 'S244 |  | 95 | 147 |  |
|  |  | Outputs |  | 'S240 |  | 100 | 145 |  |
|  |  | Low |  | 'S241, 'S244 |  | 120 | 170 |  |
|  |  | Outputs Disabled |  | 'S240 |  | 100 | 145 |  |
|  |  |  |  | 'S241, 'S244 |  | 120 | 170 |  |

$\dagger$ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { 'S240 } \\ & \text { TYP } \end{aligned}$ | MAX | 'S241, 'S <br> MIN TYP | 44 MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPLH | Data to output delay | $C_{L}=50 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=90 \Omega$ |  | 4.5 | 7 | 6 | 9 | ns |
| tPHL |  |  |  | 4.5 | 7 | 6 | 9 | ns |
| tPZL | Output enable delay |  |  | 10 | 15 | 10 | 15 | ns |
| tpZH |  |  |  | 6.5 | 10* | 8 | 12 | ns |
| tPZL | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=90 \Omega$ |  | 10 | 15 | 10 | 15 | ns |
| tpHz |  |  |  | 6 | 9 | 6 | 9 | ns |

* For the S 210 add 2 ns for the $\mathrm{E}_{2}$ (Pin 19) enable.


## Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.


## Test Waveforms



Propagation Delay


Enable and Disable

Notes: A. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1 N 916 or 1 N 3064 .
C. For Series $54 \mathrm{~S}, \mathrm{R}_{\mathrm{O}}=1 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.5 \mathrm{~V}$.

For Series 54LS, $\mathrm{R}_{\mathrm{O}}=5 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}$. ZOUT $=50 \Omega$ and: For series $54 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$. For Series 54LS and PAL devices, $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

# 8-Bit Buffers with Schmitt Trigger Inputs 

# SN54/74LS310 SN54/74S310 SN54/74LS340 SN54/74S340 SN54/74LS341 SN54/74S341 SN54/74LS344 SN54/74S344 

## Features

- Schmitt-trigger inputs guarantee high noise margin
- Three-state outputs drive bus lines
- Typical input and output capacitance $\leq 10 \mathrm{pf}$
- Low-current PNP inputs reduce loading
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Complementary-enable '310 and '341 types combine multiplexer and driver functions
- Pin-compatible with SN54/74S210/240/1/4 and SN54/74LS210/240/1/4; can be direct replacement in systems with noise problems


## Description

In addition to the standard Schottky and low-power Senotiky 8 -bit buffers, Monolithic Memories provides full hysteresis with a "true" Schmitt-trigger circuit. The improve perfokmande characteristics are designed (1) for the low pever Schottky buffers, to be consistent with the SNF4/74LS 14 Nex Schmitttrigger inverter, and to guarantee a fulluomvioiselmmunity; (2) for the Schottky buffers to have low propagation delays and to guarantee a full 500 m , loise minunity the Schmitt-trigger operation makes these 1 S/S buffers ideal for buseceiversin a noisy environtrant.
These 8-bit buffersproyde high-speedand high currect nterface capability fot bus-brganizod digtat systems. The threestate drivers will source a termination to draund fut to $133 \Omega$ ) or sink a pull-up to $\mathrm{V}_{\mathrm{CC}}$ as in the popular-220n/330 $\Omega$ computer

## Ordering Information

| PART NUMBER | PKG* | TEMP | ENABLE | POLARITY | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS310 | J,F | mil | HighLow | Invert |  |
| SN74LS310 | N, J | com |  |  |  |
| SN54LS340 | J,F | mil | Low |  |  |
| SN74LS340 | N, J | com |  |  |  |  |
| SN54LS341 | J,F | mil |  |  |  |
| SN74LS341 | N, J | com. |  |  |  |
| SN54LS344 | J, F- | mil |  |  |  |
| SN74LS344 | N, ${ }^{5}$ | com |  |  |  |
| SN54S310 | d, 5 | mil |  |  | S |
| SN74S310 | N, | com |  |  |  |  |
| SN54S340 | N, E | mil |  |  |  |  |
| SN745340 | N, J | com |  |  |  |  |
| SN54S341 | J, $\mathrm{F}_{\text {A }}$ | mil | Aigh | NonInvert |  |
| SNT 46341 | N, ${ }^{\text {, }}$, | com | Low |  |  |
| SN54S344/ | U.E | mil | Low |  |  |
| SN74S344 | N,d | com |  |  |  | peripheraltermination. The PNP inputs provide improved fan-in With $0.2 \mathrm{~mA} /$, tor the low-power Schottky buffers and 0.25 mA IIL IO the Schottky buffers.

The '340 and '344 provide inverting and non-inverting outputs respectively, with assertive-low enables. The ' 310 and ' 341 also provide inverting and non-inverting outputs respectively, but with complementary (both assertive-low and assertive-high) enables, to allow transceiver or multiplexer operation.
All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

## Logic Symbols



[^55]
## IEEE Symbols



## Absolute Maximum Ratings

$\qquad$
Input voltage ...................................................................................................................................... 7 V Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V


## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | TYP | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | .25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 |  |  | 75 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions



[^56]
## Switching Characteristics $\mathbf{V}_{\mathbf{C C}}=5 \mathrm{~V}, \mathrm{~T}_{\mathbf{A}}=25^{\circ} \mathrm{C}$



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 525 | $\checkmark$ |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics Over Operating Conditions


[^57]
## Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{v}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | 'S310, 'S <br> MIN TYP | $\begin{aligned} & 340 \\ & \text { MAX } \end{aligned}$ | 'S341, 'S344 <br> MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {P PLH }}$ | Data to Output delay | $C_{L}=50 \mathrm{pF}$ | 11 | 15 | $16 \quad 22$ | ns |
| ${ }^{\text {t PHL }}$ |  |  | 16 | 22 | $10 \quad 15$ | ns |
| ${ }_{\text {t }}^{\text {PZL }}$ | Output Enable delay |  | 8 | 15 | 10 < 15 | ns |
| ${ }^{\text {t }}$ PZH |  |  | 6 | 12 | $\cdots 12$ | ns |
| ${ }^{\text {t PLZ }}$ | Output Disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=90 \Omega$ | 10 |  | 10 / 15 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | 7 | 12 | ) 12 | ns |



Function Tables

| $\overline{E_{1}}$ | $E_{2}$ | 1Y OUTPUTS | 2Y OUTPUTS |
| :---: | :---: | :---: | :---: |
| $H$ | $H$ | $Z$ | Enabled <br> (Inverting) |
| $H$ | L | Z | Z |
| L | H | Enabled <br> (Inverting) <br> Enabled <br> (Inverting) | Enabled <br> (Inverting) |
| L | L | Z |  |

'340

| $\overline{E_{1}}$ | $\overline{E_{2}}$ | 1Y OUTPUTS | 2Y OUTPUTS |
| :---: | :---: | :---: | :---: |
| $H$ | $H$ | $Z$ | $Z$ |
| $H$ | $L$ | $Z$ | Enabled <br> (Inverting) |
| L | H | Enabled <br> (Inverting) | Z |
| L | Enabled <br> (Inverting) | Enabled <br> (Inverting) |  |

'341

| $\overline{E_{1}}$ | $E_{2}$ | 1Y OUTPUTS | 2Y OUTPUTS |
| :---: | :---: | :---: | :---: |
| $H$ | $H$ | $Z$ | Enabled |
| $H$ | $L$ | $Z$ | $Z$ |
| $L$ | $H$ | Enabled | Enabled |
| $L$ | $L$ | Enabled | $Z$ |


output

VOL

| $\overline{E_{1}}$ | $\overline{E_{2}}$ | 1Y OUTPUTS | 2YOUTPUTS |
| :---: | :---: | :---: | :---: |
| $H$ | $H$ | $Z$ | $Z$ |
| $H$ | $L$ | $Z$ | $Z$ |
| $L$ | $H$ | Enabled |  |
| $L$ | $L$ | Enabled | Enabled |

$Z \equiv$ High impedance (output off).


* Dead Band: The hysteresis is guaranteed at any operating temperature and voltage.



## Test Load

Test Waveforms


# 8-Bit Buffer Transceiver SN54/74LS245 

## Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric -- equal driving capability in each direction
- 20-pin SKINNYDIP© saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54/74LS645 -- Improved speed, IL and IOZL specifications

Ordering Information

| PART <br> NUMBER | TYPE | TEMP | PQLAATY | POWER |
| :---: | :---: | :---: | :---: | :---: |
| SN54LS245 | J,L,W | MiV | Non- |  |
| SN74LS245 | N,J | Com | invert |  |

## Description

These 8-bit bus transceivers are designed for asynchronous two-way communication hetureen eate buses. The contnofunc tion implementation minimites extennat timing requirements.

The device allow data trensmissiph from the $A$ busto the B bus, or from the Beus to the A pusdependingupan the logk level at the directipricontral $(\mathbb{1}$ R) input. The enable input (E) can be


Function Table

| ENABLE | DIRECTION <br> CONTROL <br> DIR | OPERATION |
| :---: | :---: | :---: |
| L | L | B data to $A$ bus <br> L |
| H | H | A data to $B$ bus |
| Isolated |  |  |

## IEEE Symbol



# 8-Bit Buffer Transceiver SN54/74LS645 SN74LS645-1 

## FOR <br> MORE DETAIL SEE SECTION 13

## Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric - equal driving capability in each direction
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- SN74LS645-1 rated at IOL $=48 \mathrm{~mA}$


## Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The contry function implementation minimizes extefhat timing requirements.

The device allows data trapstrission 5 fom $A$ bus to the $B$ Bus or from the $B$ bus to the $A$ ope derenting upon the logic level at the direction contro (DR) input tbe enable input (E) San be used to disable the delice so that the buses are effectively


## Ordering Information



Function Table

| ENABLE | DIRECTION <br> CONTROL <br> DIR | OPERATION |
| :---: | :---: | :---: |
| L | L | B data to $A$ bus <br> L |
| H | X | A data to $B$ bus <br> Isolated |

## IEEE Symbol



# 8-Bit Registers with Master Reset or Clock Enable 

## Features/Benefits

- 8-bit data path matches byte boundaries
- Ideal for microprogram instruction registers
- Ideal for microprogram interface
- Suitable for pipeline data registers
- Useful in timing, sequencing, and control circuits
- Three '273s may replace four '174s


## Description

These 8-bit registers contain eight D-type flip-flops, they feature very low ICC ( 17 mA typical) on the low-power Schottky devices and very-high-speed operation on the Schottky devices. The ' 273 register is loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the master reset line, $\overline{\mathrm{MR}}$, is low.

## Function Table

|  | INPUTS |  | OUTPUT |
| :---: | :---: | :---: | :---: |
| $\overline{\text { MR }}$ | CLOCK | DATA | Q |
| $L$ | $X$ | $X$ | $L$ |
| $H$ | 1 | $H$ | $H$ |
| $H$ | $\dagger$ | $L$ | $L$ |
| $H$ | Lor Hor | $X$ | $Q_{0}$ |

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | POLAR- <br> ITY | CONTROL <br> OPTION | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS273 | J,L,W | Mil | Non- <br> Invert | Master <br> Reset | LS |

## Logic Symbols

Absolute Maximum Ratings
Supply voltage $\mathrm{V}_{\mathrm{CC}}$ ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 5.5 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature range ..... $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## IEEE Symbols



## Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See Interface, Test Load/Waveforms) | FIGURE | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{t} w$ | Width of clock | High-t WH | 1 | 20 |  |  | ns |
|  |  | Low-t WL |  |  |  |  |  |
| ${ }^{\text {t WMR }}$ | Width of Master Reset | Low-tWMRL | 2 | 20 |  |  | ns |
| $\mathrm{t}_{\text {rec }}$ |  | $\overline{\mathrm{MR}}$ to CK | 2 | 251 |  |  | ns |
| ${ }^{\text {tsu }}$ | Setup time | Data input to CK | 3 | 201 |  |  | ns |
|  |  |  | 4 | 251 |  |  |  |
|  |  |  |  | 101 |  |  |  |
| $t_{h}$ | Hold time | Data input | 3 | 51 |  |  | ns |
|  |  |  | 4 | 51 |  |  |  |
|  |  |  |  | 51 |  |  |  |

if The arrow indicates the transition of the clock/enable input used for reference. $\uparrow$ for the low-to-high transition. I for the high-to-low transition.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | $\begin{array}{c}\text { MILITARY } \\ \text { TYP }\end{array}$ | MAX |
| :--- | :--- | :--- | :--- | :--- | :---: |$]$ UNIT

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
$\dagger$ ICC is measured after first a momentary ground, and then 4.5 V is applied to clock, while the following other input conditions are held: For the 'LS273-4.5 V on all data and master-reset inputs.


## Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIN | 'LS273 <br> TYP | MAX |
| :---: | :---: | :---: | :---: | :---: | :---: | UNIT | M |
| :--- |



Figure 1


Figure 2


Figure 3

## Test Waveforms



## Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

> LOAD CIRCUIT FOR
> BI-STATE TOTEM-POLE OUTPUTS

Notes: A. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series $54 \mathrm{LS}, \mathrm{V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$.

## 8- Bit Latches, 8-Bit Registers SN54LS373 SN54S373 SN54LS374 SN54S374

## Features/Benefits

- Three-state outputs drive bus lines
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface

Ordering Information

| PART NUMBER | PKG | TEMP | POLARITY | TYPE | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS373 | J,L,W | Mil | Noninvert | Latch | LS |
| SN54LS374 |  |  |  | Register |  |
| SN54S373 |  |  |  | Latch | S |
| SN54S374 |  |  |  | Register |  |

## Description

The latch passes eight bits of data from the inputs (D) to the outputs $(Q)$ when the gate $(G)$ is high. The data is "latched" when the gate $(G)$ goes low. The register loads eight bits of input data and passes it to output on the "rising edge" of the clock.

The three-state outputs are active when $\overline{O E}$ is low, and highimpedance when $\overline{\mathrm{OE}}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

## Function Tables

'373 8-Bit Latch

| $\overline{\mathbf{O E}}$ | $\mathbf{G}$ | $\mathbf{D}$ | $\mathbf{Q}$ |
| :--- | :--- | :--- | :--- |
| $\mathbf{L}$ | $H$ | $H$ | $H$ |
| $L$ | $H$ | $L$ | $L$ |
| $L$ | L | $X$ | $Q_{0}$ |
| $H$ | $X$ | $X$ | $Z$ |

'374 8-Bit Register

| $\overline{\mathbf{O E}}$ | CK | $\mathbf{D}$ | $\mathbf{Q}$ |
| :---: | :---: | :---: | :---: |
| $L$ | $\dagger$ | $H$ | $H$ |
| $L$ | $\dagger$ | $L$ | $L$ |
| $L$ | Lor Hor t | $X$ | $Q_{0}$ |
| $H$ | $X$ | $X$ | $Z$ |

## Logic Symbols



## Absolute Maximum Ratings


Input voltage ..................................................................................................... -1.5 V to 7 V

Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VCC | Supply voltage |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{t}$ w | Width of Clock/Gate | High | 15 |  |  | ns |
|  |  | Low | 15 |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time | 'LS373 | 51 |  |  | ns |
|  |  | 'LS374 | 201 |  |  |  |
| $t_{h}$ | Hold time | 'LS373 | 201 |  |  | ns |
|  |  | 'LS374 | 01 |  |  |  |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.7 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  |  | 2.0 |  |  | V |
| VIC | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| IIL | Low-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.4 | mA |
| IIH | High-level input current | $V_{C C}=$ MAX | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  | 0.1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}$ |  | 0.25 | 0.4 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \\ & \hline \end{aligned}$ | $\mathrm{I}^{\mathrm{OH}}=-1 \mathrm{~mA}$ | 2.4 | 3.4 |  | V |
| 'OZL | Off-state output current | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -20 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| IOS | Output short-circuit current* | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -30 |  | -130 | mA |
| ${ }^{\prime} \mathrm{CC}$ | Supply current | $V_{C C}=M A X$ <br> Outputs open | 'LS373 |  | 24 | 40 | mA |
|  |  |  | 'LS374 |  | 27 | 40 |  |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.


## Switching Characteristics $\mathrm{vCC}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { 'LS373 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \text { 'LS374 } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| fMAX | Maximum clock frequency | $C_{L}=45 \mathrm{pF}$ |  |  |  | 35 | 50 |  | MHz |
| tPLH | Data to output delay |  |  | 12 | 18 |  |  |  | ns |
| tPHL |  |  |  | 12 | 18 |  |  |  | ns |
| tPLH | Clock/Gate to output delay |  |  | 20 | 30 |  | 15 | 28 | ns |
| tPHL |  |  |  | 18 | 30 |  | 19 | 28 | ns |
| tPZL | Output enable delay |  |  | 25 | 36 |  | 21 | 28 | ns |
| tPZH |  |  |  | 15 | 28 |  | 20 | 28 | ns |
| tPLZ | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ |  | 15 | 25 |  | 14 | 25 | ns |
| tPHZ |  |  |  | 12 | 20 |  | 12 | 20 | ns |

## IEEE Symbols



## '373 Timing Diagrams



## '374 Timing Diagrams



## Test Waveforms



Propagation Delay


Enable and Disable

Notes: $\mathrm{A} . \mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
B. All diodes are 1 N 916 or 1 N 3064 .
C. For Series $54 \mathrm{~S}, \mathrm{R}_{\mathrm{O}}=1 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.5 \mathrm{~V}$.

For Series 54LS, $\mathrm{R}_{\mathrm{O}}=5 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
$E$. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}$. $\mathrm{Z}_{\text {OUT }}=50 \Omega$ and:
For series $54 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$.
For Series 54LS and PAL devices, $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

## Standard Test Load



[^58]
## Absolute Maximum Ratings

Supply voltage $\mathrm{V}_{\mathrm{CC}}$
-0.5 V to 7 V
Input voltage
-1.5 V to 7 V

Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {CC }}$ | Supply voltage |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |
| $t_{\text {w }}$ | Width of Clock/Gate | High | 6 |  |  | ns |
|  |  | Low | 7.3 |  |  |  |
| $t_{\text {su }}$ | Setup time | 'S373 | 01 |  |  | ns |
|  |  | 'S374 | 51 |  |  |  |
| $t_{h}$ | Hold time | 'S373 | 101 |  |  | ns |
|  |  | 'S374 | $2 \dagger$ |  |  |  |

$\uparrow$ The arrow indicates the transition of the clock input used for reference. $\uparrow$ for the low-to-high transition, $\downarrow$ for the high-to-low transition.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| VIL | Low-level input voltage |  |  |  |  | 0.8 | V |
| VIH | High-level input voltage |  |  | 2.0 |  |  | V |
| Vic | Input clamp voltage | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.2 | V |
| IIL | Low-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.5 \mathrm{~V}$ |  |  | -0.25 | mA |
| 1 IH | High-level input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| 11 | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\mathrm{I}_{\mathrm{OL}}=20 \mathrm{~mA}$ |  |  | 0.5 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=0.8 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\mathrm{IOH}=-2 \mathrm{~mA}$ | 2.4 | 3.4 |  | V |
| IOZL | Off-state output current | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=0.8 \mathrm{~V} \\ & V_{\mathrm{IH}}=2 \mathrm{~V} \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.5 \mathrm{~V}$ |  |  | -50 | $\mu \mathrm{A}$ |
| IOZH |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ |  |  | 50 | $\mu \mathrm{A}$ |
| IOS | Output short-circuit current* | $\mathrm{V}_{C C}=\mathrm{MAX}$ |  | -40 |  | -100 | mA |
| ${ }^{\prime} \mathrm{CC}$ | Supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ <br> Outputs open | 'S373 |  | 105 | 160 | mA |
|  |  |  | 'S374 |  | 90 | 140 |  |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $\mathbf{v c C}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { 'S373 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \text { 'S374 } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| fMAX | Maximum clock frequency | $C_{L}=15 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  |  |  | 75 | 100 |  | MHz |
| tPLH | Data to output delay |  |  | 7 | 12 |  |  |  | ns |
| tPHL |  |  |  | 7 | 12 |  |  |  | ns |
| tPLH | Clock/Gate to output delay |  |  | 7 | 14 |  | 8 | 15 | ns |
| tPHL |  |  |  | 12 | 18 |  | 11 | 17 | ns |
| tPZL | Output enable delay |  |  | 11 | 18 |  | 11 | 18 | ns |
| tPZH |  |  |  | 8 | 15 |  | 8 | 15 | ns |
| tPLZ | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 8 | 12 |  | 7 | 12 | ns |
| tphz |  |  |  | 6 | 9 |  | 5 | 9 | ns |

## 8-Bit Register With Clock Enable and Open-Collector Outputs SN54/74S383

## Features

- 20-Pin SKINNYDIP® Saves Space
- 8-bit data path matches byte boundaries
- Only available TTL open-collector-output register
- Ideal for certain microprocessor system buses
- Suitable for pipeline data registers
- Excellent for multiple, physically-separated connections to buses in microprocessor-based systems
- Wired-OR or wired-AND logic with outputs


## Description

This 8-bit register contains 8 D-type flip-flops and features very fast switching. The 'S383 register is loaded on the rising edge of the clock provided that the clock enable line, $\overline{\mathrm{CK} E N}$, is low. Like other 8-bit interface devices, the 'S383 is packaged in the popular 20-pin SKINNYDIP.

## Logic Symbol

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | POLAR- <br> ITY | CONTROL <br> OPTIONS | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54S383 | J,L,W | Mil | Non- <br> OPlock | Clock <br> Enable |  |
| SN74S383 | $\mathrm{N}, \mathrm{J}$ | Com |  |  |  |

## Function Table 'S383



IEEESymbol


## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS (See Interface, Test Load/Waveforms) | FIGURE | MILITARY MIN TYP MAX | COMMERCIAL MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  | $\begin{array}{lll}4.5 & 5 & 5.5\end{array}$ | $4.75 \quad 5 \quad 5.25$ | $\square$ |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  | $-55 \quad 125$ | $0 / 15$ | V |
| ${ }^{t} w$ | Width of clock | High-t WH | 1 | 7 | 7, 1) | ns |
|  |  | Low-t WL |  |  |  |  |
| ${ }^{\text {tsu }}$ | Setup time | Data input to CK | 2 | 51 | $5 \dagger$ |  |
|  |  | Low CK EN to CK |  | 91 | 91 < |  |
|  |  | High CK EN to CK |  | 1 | $91 \ldots$ |  |
| $t^{\prime}$ | Hold time | Data input | 2 |  | 31 | ns |
|  |  | Low $\overline{\mathrm{CK} E N}$ to CK |  | 1 | 31 |  |
|  |  | High $\overline{C K}$ EN to CK , |  | $012$ |  |  |

1t The arrow indicates the transition of the clock/enable input used for reference: for the low-to-bigh transition, f for the high-to-low transition.

## Electrical Characteristics Over Qperating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\text {IL }}$ | Low-level hput voltage |  | 2 |  |  | 0.8 |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | High-levelingut volitage | , |  | 2 |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp yoltage | VCC MIN | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.2 |  |  | -1.2 | V |
| ${ }^{\text {IL }}$ | Low-level input current | VCC MAX | $\mathrm{V}_{1}=0.5 \mathrm{~V}$ |  |  | -250 |  |  | -250 | $\mu \mathrm{A}$ |
| ${ }_{1} \mathrm{H}$ | High-level input current | $V^{C C}=$ MAX | $V_{1}=2.7 \mathrm{~V}$ |  |  | 50 |  |  | 50 | $\mu \mathrm{A}$ |
| $1 /$ | Maximum input current | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 1 |  |  | 1 | mA |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | ${ }^{\prime} \mathrm{OL}=24 \mathrm{~mA}$ |  |  | 0.5 |  |  | 0.5 | V |
| ${ }^{1} \mathrm{OH}$ | High-level output current | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{OH}}=5.5 \mathrm{~V}$ |  |  | 250 |  |  | 250 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{CC}$ | Supply current | $V_{C C}=M A X$ | Outputs HIGH |  |  | 160 |  |  | 160 | mA |
| ${ }^{\text {c }}$ C |  | Outputs open | Outputs LOW |  |  | 160 |  |  | 160 |  |

## Switching Characteristics vcc $=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { 'S383 } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{\text {f MAX }}$ | Maximum Clock frequency | $C_{L}=15 \mathrm{pF} \quad R_{L}=280 \Omega$ | 75 | 110 |  | MHz |
| ${ }^{\text {tPLH }}$ | Clock to output delay |  |  | 10 | 17 | ns |
| ${ }_{\text {tPHL }}$ |  |  |  | $\cdots 14$ | 22 | ns |

## Test Waveforms



DATA AND CLOCK ENABLE
SETUP AND HOLD TIMES


Figure 1

## Test Load

TEST POINT*

* The "TEST POINT" is driven by the output undeentest, and observed by instrumentation.


Includes probe and jig capacitance.
In the examples above, the phase relationships between inputs and outputs haye been chosen arbitrarily.

Allipitt pulses are auppleed by generators having the following
characteristics $P$ PRR ,
$\leq N M H Z Z_{\text {ut }}=509$ and:

For Senes $54 / 74 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$.

## Open Collector Bus Application Information For Determination of $\mathbf{R}_{\mathbf{L}}$ For Wired-And Applications

1. CALCULATE $R_{L}$ (Min):
$R_{L}($ Min $)=\frac{V_{C C}-V_{O L}(M a x)}{I_{O L}-\left(T O T A L ~ I_{I L}\right)}$
where $\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}$ at

$$
\mathrm{V}_{\mathrm{OL}}(\mathrm{Max})=0.5 \mathrm{~V}
$$


where $\mathrm{I}_{\mathrm{OH}}=250 \mu \mathrm{~A}$ at

—"


## 2. CALCULATE $\mathbf{R}_{\mathrm{L}}(\operatorname{Max})$ :

$$
R_{\mathrm{L}}(\mathrm{Max})=\frac{\mathrm{V}_{\mathrm{CC}}-\mathrm{V}_{\mathrm{OH}}(\operatorname{Min})}{\left(\text { TOTAL } I_{O H}+T O T A L I_{I H}\right)}
$$


3. SELECT a value for $R_{L}$ in the range of $R_{L}$ (Min) to $R_{L}$ (Max), based on power consumption and speed requirements:


RL vs. Tr FOR SN 54/74S383

# 8-Bit Latches, 8-Bit Registers with Inverting Outputs SN54/74LS533 SN54/74S533 SN54/74LS534 SN54/74S534 

## Features/Benefits

## - Inverting outputs

- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN54/74L.S373/4 or SN54/74S373/4 can be direct replacement when bus polarity must be changed


## Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides inverting outputs instead of noninverting outputs. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-bit slice to an assertive-low bus.
The latch passes eight bits of data from the inputs (D) to the outputs $(Q)$ when the gate $(G)$ is high. Theodata is vatched

## Function Tables



## Logic Symbols



## Ordering Information

| PART NUMBER | PKG | TEMP | POLARITY | TYPE | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & \text { 54LS533 } \\ & \text { 74LS533 } \end{aligned}$ | $\begin{gathered} \mathrm{J}, \mathrm{~W}, \mathrm{~L} \\ \mathrm{~N}, \mathrm{~J} \end{gathered}$ | Mil <br> Com | Invert | Latch |  |
| $\begin{aligned} & \text { 54LS534 } \\ & \text { 74LS534 } \end{aligned}$ | $\begin{gathered} \hline \text { J,W,L } \\ \mathrm{N}, \mathrm{~J} \end{gathered}$ | $\begin{gathered} \mathrm{Mil} \\ \mathrm{Com} \end{gathered}$ |  | Register |  |
| $\begin{aligned} & 54 \mathrm{~S} 533 \\ & 74 \mathrm{~S} 533 \end{aligned}$ | $\begin{gathered} \mathrm{J}, \mathrm{~W}, \mathrm{~L} \\ \mathrm{~N}, \mathrm{~J} \end{gathered}$ | $\begin{gathered} \mathrm{Mil} \\ \text { Com } \\ \hline \end{gathered}$ |  | Latch | $\mathrm{S}_{\mathrm{s}}$ |
| $\begin{aligned} & 54 S 534 \\ & 74 S 534 \end{aligned}$ | $\begin{gathered} \mathrm{J}, \mathrm{~W}, \mathrm{~L} \\ \mathrm{~N}, \mathrm{~J} \end{gathered}$ | Mil Com |  | Register |  |

when the gate (G) goeslow. The register oads eight bits of input data and passes tt to the output on the "rising edge" of the clock.
The three-state outputs are acive when OE is low, and highimpedance when $\overline{O E}$ is high. Schmifttrigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.
All of the 8-bit devices are packaged in the popular 20-pin SKINAYPDP
'534 8-Bit Register (Inverting)

| $\overline{O E}$ | $C K$ | $D$ | $\bar{Q}$ |
| :---: | :---: | :---: | :---: |
| $L$ | $\dagger$ | $H$ | $H$ |
| $L$ | $\dagger$ | $L$ | $L$ |
| $L$ | Lor Hor $\downarrow$ | $X$ | $Q_{0}$ |
| $H$ | $X$ | $X$ | $Z$ |



## IEEE Symbols



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  |  | LITAR |  |  | MER |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{t}$ w | Width of Clock/Gate | High | 15 |  |  | 15 |  |  | ns |
|  |  | Low | 15 |  |  |  |  |  |  |
| ${ }^{\text {tsu }}$ | Setup time | LS533 | 31 |  |  | 31 |  |  | ns |
|  |  | LS534 | 201 |  |  |  | + |  |  |
| $t_{h}$ | Hold time | LS533 | 10. |  |  | 10 |  |  | ns |
|  |  | LS534 |  |  |  | $01$ |  |  |  |

$1 \downarrow$ The arrow indicates the transition of the clock/enable input used for reference. 1 for the low-to-high transifion, $\downarrow$ for the high-to-low tranfition
Electrical Characteristics Over Operating Conditions


* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.


## Switching Characteristics vcc $=5 \mathrm{~V}, \mathrm{TA}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | LS533 TYP | MAX | MIN | LS534 | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| f MAX | Maximum Clock frequency | $C_{L}=45 p F \quad R_{L}=667 \Omega$ |  |  |  | 35 | 50 |  | MHz |
| ${ }_{\text {t PLH }}$ | Data to Output delay |  |  | 17 | 25 |  |  |  | ns |
| ${ }_{\text {t }}$ |  |  |  | 12 | 25 |  |  |  | ns |
| ${ }_{\text {t PLH }}$ | Clock/Gate to output delay |  |  | 20 | 35 |  | 19 | 30 | ns |
| ${ }^{\text {t PHL }}$ |  |  |  | 18 | 35 |  | 15 | 30 | ns |
| ${ }^{\text {tPZL }}$ | Output Enable delay |  |  | 25 | 36 |  | 21 | 30 | ns |
| ${ }^{\text {tPZH }}$ |  |  |  | 17 | 30 |  | 20 | 30 | ns |
| ${ }^{\text {tPLZ }}$ | Output Disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ |  | 18 | 29 |  | 18 | 29 | ns |
| ${ }^{\text {tPHZ }}$ |  |  |  | 16 | 24 |  | 16 | 24 | ns |

## Absolute Maximum Ratings



Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of Clock/Gate | High | 6 |  |  | 6 |  |  | ns |
|  |  | Low | 7.3 |  |  | 7.3 |  |  |  |
| ${ }^{\text {t }}$ su | Setup time | S533 | 01 |  |  | 01 | + |  | ${ }^{\square} \mathrm{ns}$ |
|  |  | S534 | $5 \dagger$ |  |  |  |  |  |  |
| $t_{h}$ | Hold time | S533 | 10. |  |  | 19 |  |  | ns |
|  |  | \$534 | 51 |  |  | 51 |  |  |  |

$\dagger \downarrow$ The arrow indicates the transition of the clock/enable input used for reference. $\uparrow$ for the low-to-high frahsition/ for the hign-to-low transition.
Electrical Characteristics Over Operating Conditions


* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics vcc $=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \hline \text { S533 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{gathered} \hline \mathbf{S 5 3 4} \\ \text { TYP } \end{gathered}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| f MAX | Maximum Clock frequency | $C_{L}=15 p F \quad R_{L}=280 \Omega$ |  |  |  | 75 | 100 |  | M Hz |
| ${ }^{\text {P PLH }}$ | Data to Output delay |  |  | 9 | 18 |  |  |  | ns |
| ${ }^{\text {t }}$ PHL |  |  |  | 5 | 16 |  |  |  | ns |
| ${ }^{\text {t PLH }}$ | Clock/Gate to output delay |  |  | 12 | 22 |  | 11 | 20 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 7 | 20 |  | 8 | 18 | ns |
| ${ }^{\text {P P PL }}$ | Output Enable delay |  |  | 11 | 20 |  | 11 | 20 | ns |
| ${ }^{\text {P PZH }}$ |  |  |  | 8 | 17 |  | 8 | 17 | ns |
| tplZ | Output Disable delay | $C_{L}=5 p F \quad R_{L}=280 \Omega$ |  | 8 | 16 |  | 7 | 16 | ns |
| ${ }^{\text {tPHZ }}$ |  |  |  | 6 | 13 |  | 5 | 13 | ns |

## Test Waveforms



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

NOTES: A. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
B. All diodes are 1 N 916 or 1 N 3064 .
C. For Series $54 / 74 \mathrm{~S}, \mathrm{R}_{\mathrm{O}}=1 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.5 \mathrm{~V}$.

For Series 54/74LS, $\mathrm{R}_{\mathrm{O}}=5 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
$E$. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and: For Series $54 / 74 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$. For Series $54 / 74$ LS and PALs, $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns} . \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of 3 -state outputs, switches S1 and S2 are closed.

# 8-Bit Latch, 8-Bit Register with 32 mA Outputs SN74S531 SN74S532 

## Features/Benefits

- High drive capability ( $\mathrm{IOL}_{\mathrm{OL}}=\mathbf{3 2} \mathrm{mA}$ )
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S373/4 - can be a direct replacement when high drive capability is required


## Description

In addition to the standard S and LS latches and registers, Monolithic Memories provides increased output sink current (IOL) from the standard Schottky $\mathrm{IOL}^{\circ}$ of 20 mA to an improved 32 mA.
The higher IOL is intended for upgrading systems which presently satisfy $32-\mathrm{mA}$ requirements with the SN $54 / 74365 \mathrm{~A} / 366 \mathrm{~A}$ 367A/368A hex buffers.

## Function Tables

## Logic Symbols


'S532 8-Bit Register

| $\overline{\mathbf{O E}}$ | $\mathbf{C K}$ | $\mathbf{D}$ | $\mathbf{Q}$ |
| :---: | :---: | :---: | :---: |
| $L$ | $\dagger$ | $H$ | $H$ |
| $L$ | $\dagger$ | $L$ | $L$ |
| $L$ | Lor $H$ or $\downarrow$ | $X$ | $Q_{0}$ |
| $H$ | $X$ | $X$ | $Z$ |

'S532 8-Bit Register


## Ordering Information

| PART <br> NUMBER | PKG | TEMP | POLARITY | ITPE | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN74S531 | $\mathrm{N}, \mathrm{J}$ | com | Non | Latch |  |
| SN74S532 | $\mathrm{N}, \mathrm{J}$ | com |  |  |  |

The latch passes eight bits of data from the inputs (D) to the outputs $(Q)$ when the gate $(G)$ is bigh. The date is "latched" when the gate (G) goes low. The register loads eight bits of input date and passesit to the output orthe rising edge of the clock.
The three-state outputs are active when $\overline{O E}$ is low, and highimpedance when OE is high Schmitt-trigger buffers at the gate/clock inpets improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP®.

## IEEE Symbols



## Absolute Maximum Ratings

Supply voltage $\mathrm{V}_{\mathrm{CC}}$ ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 VStorage temperature$65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MMERC <br> TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5. | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | 0 |  |  | ${ }^{\circ} \mathrm{C}$ |
| $t_{\text {w }}$ | Width of Clock/Enable | High | 6 |  |  |  |
|  |  | Low | 7.3 | 3 |  |  |
| $t_{\text {su }}$ | Setup time | S531 | 01 | 04 |  |  |
|  |  | S532 | 51 |  |  |  |
| $t_{h}$ | Hold time | S531 |  |  |  |  |
|  |  | S532 | 24 |  |  | ns |

it The arrow indicates the transition of the clock/enable input used for reference. 1 forthe low-to-high trensition, $\downarrow$ forthe finghato-low trathsition.
Electrical Characteristics Over Operating Condiffons


* Not maresthan one output should be shorted at a time and duration of the short-circuit should not exceed one second.
- ${ }^{2}$ witching Characteristics vcc $=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { S531 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \hline \text { S532 } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| f MAX | Maximum Clock frequency | $C_{L}=15 \mathrm{pF} \quad R_{L}=280 \Omega$ |  |  |  | 75 | 100 |  | MHz |
| ${ }^{\text {t PLH }}$ | Data to Output delay |  |  | 7 | 12 |  |  |  | ns |
| ${ }^{\text {t PHL }}$ |  |  |  | 7 | 12 |  |  |  | ns |
| ${ }^{\text {t PLH }}$ | Clock/Gate to output delay |  |  | 7 | 14 |  | 8 | 15 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 12 | 18 |  | 11 | 17 | ns |
| ${ }^{\text {P P Z }}$ | Output Enable delay |  |  | 11 | 18 |  | 11 | 48 | ns |
| ${ }^{\text {t PZH }}$ |  |  |  | 8 | 15 |  | 8 | 15 | ns |
| ${ }^{\text {tPLZ }}$ | Output Disable delay | $C_{L}=5 p F \quad R_{L}=280 \Omega$ |  | 8 | 12 |  | 7 | 12 | ns |
| ${ }^{\text {P PHZ }}$ |  |  |  | 6 | 9 |  | 5 | 9 | ns |

## 'S531 Timing Diagrams



## 'S532 Timing Diagrams



## Test Load

NOTES: $A . C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series $54 / 74 \mathrm{~S}, \mathrm{R}_{\mathrm{O}}=1 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.5 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and: For Series $54 / 74 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{F} \leq 2.5 \mathrm{~ns}$.
For Series 54/74LS and PALs, $\mathrm{t}_{\mathrm{R}} \leq 15$ ns. $\mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of 3 -state outputs, switches S1 and S2 are closed.

# 8-Bit Latch, 8-Bit Register with Inverting, 32 mA Outputs SN74S535 SN74S536 

## Features/Benefits

- Inverting outputs
- High-drive capability ( $\mathrm{I}_{\mathrm{OL}}=32 \mathrm{~mA}$ )
- Three-state outputs drive bus lines
- 20-pin SKINNYDIP® saves space
- 8-blt data path matches byte boundaries
- Hysteresis improves noise margin
- Low current PNP inputs reduce loading
- Ideal for microprocessor interface
- Pin-compatible with SN74S533/4 - can be a direct replacement when high-drive capability is required


## Description

In addition to the standard S and LS latches and tegisters, Monolithic Memories provides increased output sink current (IOL) from the standard Schottky 10 ol of 20 mA to ap inproved 32 mA ; also, inverting outputs instead of the startare noninvert ing outputs.
The higher IOL is intenfed for upgrading systemswhich pres-

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | POLARITY TYPE | POWER |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN74S535 | $\mathrm{N}, \mathrm{J}$ | Com |  | Hert | Latch |
| SN74S536 | $\mathrm{N}, \mathrm{J}$ | Com |  | Register | S |

ently satisfy 32 mA requirements with the SN54/74365/366/ 367/368 hex buffers. The inveiting outputsare intended for bus applicafions that require inversion as in interfacing the Am2901A 4 -bit slice to an assertive low.
The atch passes eight bits of data from the inputs (D) to the outputs $(Q)$ when the gate ( $Q$ ) is high. The data is "latched" when the gate (G)goes low. The register loads eight bits of input data and passes it to the output on the rising edge of the clock.
The threestate quiputs are active when $\overline{\mathrm{OE}}$ is low, and highirnpedance whed $\overline{O E}$ is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

All of the 8 -bit devices are packaged in the popular 20-pin SKINNYDIP®.

Function_tables
S53 8 -Bit Latch (Inverting)

| $\overline{O L}$ | $G$ | $D$ | $\vec{Q}$ |
| :---: | :---: | :---: | :---: |
| $L$ | $H$ | $H$ | $L$ |
| $L$ | $H$ |  | $H$ |
| $L$ | $L$ | $X$ | $Q_{0}$ |
| $H$ | $X$ | $X$ | $Z$ |

'S536 8-Bit Register (Inverting)

| $\overline{\mathbf{O E}}$ | $\mathbf{C K}$ | $\mathbf{D}$ | $\overline{\mathbf{Q}}$ |
| :---: | :---: | :---: | :---: |
| $\mathbf{L}$ | $\hat{y}$ | $\mathbf{H}$ | $\mathbf{L}$ |
| $\mathbf{L}$ | $\uparrow$ | $\mathbf{L}$ | $\mathbf{H}$ |
| $\mathbf{L}$ | Lor $H$ or $\downarrow$ | $X$ | $Q_{0}$ |
| $H$ | $X$ | $X$ | $Z$ |

## Logic Symbols

'S535 8-Bit Latch (Inverting)

'S536 8-Bit Register (Inverting)


## IEEE Symbols



## Absolute Maximum Ratings


Input voltage ...................................................................................................................... 5.5 V
Off-state output voltage . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 5.5 V


## Operating Conditions

| SYMBOL | PARAMETER |  | -MIN | MERC <br> TYP | $u x$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.75 | 5 | 5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | 0 |  | $\times 75$ | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of Clock/Enable | High | 6 |  |  |  |
|  |  | Low | 7.3 | 73 |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time | S535 | 01. | 01 |  |  |
|  |  | S536 | 11 |  |  |  |
| $t_{h}$ | Hold time | S535 | j01 | 101 |  |  |
|  |  | S536 | $51$ |  |  | ns |



* Notwhe thameme output should be shorted at a time and duration of the short-circuit should not exceed one second.
switehing Charcteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN | $\begin{aligned} & \text { S535 } \\ & \text { TYP } \end{aligned}$ | MAX | MIN | $\begin{aligned} & \text { S536 } \\ & \text { TYP } \end{aligned}$ | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $f_{\text {MAX }}$ | Maximum Clock frequency | $C_{L}=15 p F \quad R_{L}=280 \Omega$ |  |  |  | 75 | 100 |  | MHz |
| ${ }^{\text {P PLH }}$ | Data to Output delay |  |  | 9 | 18 |  |  |  | ns |
| ${ }^{\text {t PHL }}$ |  |  |  | 5 | 16 |  |  |  | ns |
| tpLH | Clock/Enable to output delay |  |  | 12 | 22 |  | 11 | 20 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 7 | 20 |  | 8 | 18 | ns |
| ${ }^{\text {tPZL }}$ | Output Enable delay |  |  | 11 | 20 |  | 11 | 20 | ns |
| ${ }^{\text {tPZH }}$ |  |  |  | 8 | 17 |  | 8 | 17 | ns |
| ${ }^{\text {P PLZ }}$ | Output Disable delay | $C_{L}=5 p F \quad R_{L}=280 \Omega$ |  | 8 | 16 |  | 7 | 16 | ns |
| ${ }^{\text {t PHZ }}$ |  |  |  | 6 | 13 |  | 5 | 13 | ns |

## 'S535 Timing Diagrams

'S536 Timing Diagrams


## Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.


## Test Waveforms



NOTES: A. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series $54 / 74 \mathrm{~S}, \mathrm{R}_{\mathrm{O}}=1 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.5 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and: For Series $54 / 74 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$. For Series 54/74LS and PALs, $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns} . \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of 3 -state outputs, switches S1 and S2 are closed.

## FOR <br> MORE DETAIL SEE SECTION

## Features/Benefits

- High-drive capability: IOL = 32 mA (Com), 24 mA (Mil)
- Assists on-line and off-line system diagnostic testing
- Swaps the content of shadow register and output register
- Shadow register for diagnostic testing
- Edge-triggered "D" registers
- Cascadable for wide control words for use in microprogramming
- Features RAM write-back for writable control store initialization
- PNP inputs for low-input current
- 24-pin SKINNYDIP ${ }^{\circledR}$ saves space

Applications

- Register for microprogram control store
- Status register
- Data register
- Instruction register
- Address register
- Interrupt mask register
- Pipeline register
- General purpose register
- Parallel-serial/Serial-parallel converter


## Description

The SN54/74S818 is an 8-bit register with diagnostic features. There is a shadow register in each diagnostic register. Diagnostic data is shifted in serially into the shadow register (S7-S0), while the output register is loaded with either the content of the shadow register or the input data (D7-D0). Moreover, D7-D0 can also be used as the outputs from the shadow register to the data bus, while the outputs ( $B 7-B 0$ ) can also be converted to inputs when disabled.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN54S818 | JS,F,L | Mil |
| SN74S818 | NS,JS | Com |

NOTE: L package here is L28. The other packages are 24-pin.

## Block Diagram



Function Table

| INPUTS |  |  |  | OUTPUTS |  |  | OPERATION | SEE FIG. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MODE | SDI | CLK | DCLK | B7-B0 | S7-S0 | SDO |  |  |
| L | X | $\dagger$ | * | $\mathrm{Bn} \leftarrow \mathrm{Dn}$ | HOLD | S7 | Load output register from input bus | 1 |
| L | X | * | $\dagger$ | HOLD | $\begin{aligned} & S n \leftarrow S n-1 \\ & S O \leftarrow S D I \end{aligned}$ | S7 | Shift shadow register data | 2 |
| L | X | $\dagger$ | $\dagger$ | $B n \leftarrow D n$ | $\begin{aligned} & S n \leftarrow S n-1 \\ & S 0 \leftarrow S D I \end{aligned}$ | S7 | Load output register from input bus while shifting shadow register data | 1 \& 2 |
| H | X | 1 | * | $\mathrm{Bn} \leftarrow \mathrm{Sn}$ | HOLD | SDI | Load output register from shadow register | 2,3,4 |
| H | L | * | $\dagger$ | HOLD | Sn - Bn | SDI | Load shadow register from output bus | 3 |
| H | L | $\dagger$ | $\dagger$ | $\mathrm{Bn} \leftarrow \mathrm{Sn}$ | $S n \leftarrow B n$ | SDI | Swap shadow register and output register |  |
| H | H | * | $\dagger$ | HOLD | HOLD | SDI | Enable D7-D0 as outputs for RAM write-back | 4 |

[^59]
## Test Load



LOAD CIRCUIT FOR THREE-STATE OUTPUTS


* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

LOAD CIRCUIT FOR BI-STATE
TOTEM-POLE OUTPUTS

## Test Waveforms



SETUP AND HOLD


PROPAGATION DELAY


PULSE WIDTH


ENABLE AND DISABLE

Notes: $A$. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series $54, \mathrm{R}_{\mathrm{O}}=1 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.5 \mathrm{~V}$. For Series 54LS, $\mathrm{R}_{\mathrm{O}}=5 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \mathrm{MHz}$. $\mathrm{Z}_{\text {OUT }}=50 \Omega$ and:
For Series $54, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$.
For Series 54 S and PALs, $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.


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## Table of Contents <br> DOUBLE-DENSITY PLUS ${ }^{\text {TM }}$ INTERFACE

## Double-Density PLUS Selection Guide

| PART NUMBER | PART DESCRIPTION |  |  | POWER | POLARITY | OUTPUT | ${ }^{\prime} \mathrm{OL}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| COMMERCIAL | ARCHITECTURE | FUNCTION | FEATURE |  |  |  |  |
| 74LS546 | Transceiver | Register | Independent enable controls | LS | Noninvert | Three-state | 32 mA |
| 74LS566 | Transceiver | Register |  | LS | Invert | Three-state | 32 mA |
| 74LS547 | Transceiver | Latch |  | LS | Noninvert | Three-state | 32 mA |
| 74LS567 | Transceiver | Latch |  | LS | Invert | Three-state | 32 mA |
| 74LS646 | Transceiver | Front load latch | Direction control | LS | Noninvert | Three-state | 24 mA |
| 74LS647 | Transceiver | Front load latch |  | LS | Noninvert | Open-collector | 24 mA |
| 74LS648 | Transceiver | Front load latch |  | LS | Invert | Three-state | 24 mA |
| 74LS649 | Transceiver | Front load Latch |  | LS | Invert | Open-collector | 24 mA |
| 74LS651 | Transceiver | Front load latch | Independent enable controls | LS | Invert | Three-state | 24 mA |
| 74LS652 | Transceiver | Front load latch |  | LS | Noninvert | Three-state | 24 mA |
| 74LS653 | Transceiver | Front load latch |  | LS | Invert | A: Open-collector | 24 mA |
| 74LS654 | Transceiver | Fr/load latch |  | LS | Noninvert |  | 24 mA |
| 74ACT547 | Transceiver | Latch | Independent enable controls | CMOS | Noninvert | Three-state | 12 mA |
| 74ACT567 | Transceiver | Latch |  | CMOS | Invert | Three-state | 12 mA |
| 74ACT646 | Transceiver | Front load latch | Direction control | CMOS | Noninvert | Three-state | 12 mA |
| 74ACT648 | Transceiver | Front load latch |  | CMOS | Invert | Three-state | 12 mA |
| 74ACT651 | Transceiver | Front load latch | Independent enable controls | CMOS | Invert | Three-state | 12 mA |
| 74ACT652 | Transceiver | Front load latch |  | CMOS | Noninvert | Three-state | 12 mA |
| 74ACT793 | Readback | Latch | Readback enable control | CMOS | Noninvert | Three-state | 12 mA |
| 74ACT794 | Readback | Register |  | CMOS | Noninvert | Three-state | 12 mA |
| 74LS793 | Readback | Latch | Readback enable control | LS | Noninvert | Three-state | 24 mA |
| 74LS794 | Readback | Register |  | LS | Noninvert | Three-state | 24 mA |
| 74LS548 | Two-stage pipeline | Register | Input, Output individual select controls | LS | Noninvert | Three-state | 32 mA |
| 74LS549 | Two-stage pipeline | Latch |  | LS | Noninvert | Three-state | 32 mA |
| 745818 | Pipeline | Register | Mode controls | S | Noninvert | Three-state | 32 mA |

# Small But Mighty; New Components Give You More Logic in Less Chips* 

Chuck Hastings and Suneel Rajpal

Interface circuits are generally thought of as unglamorous bread-and-butter items. They have the humble role of being the "glue" which holds digital systems together. Contemporary custom-LSI wizards often claim to be on the point of getting rid of all these bothersome little low-complexity circuits, and yet more interface circuits are sold with each passing year. According to recent estimates, during 1983 the personal computer industry alone consumed one-fourth as many interface circuits as all users consumed during 1982. Figure 1 graphically portrays a realistic scenario for interface for the next few years - everything else will shrink, so interface will grab an increasing share of board area in the future!


What this means to you is that, if interface does its part and does some shrinking too, you'll get some major shrinkage in your overall system. Interface is low-complexity stuff to start with, and over the years it has stubbornly resisted being shrunk. Nonetheless, today Monolithic Memories offers a broad line of interface parts which arose from commonly-encountered circumstances, and which - where they fit your design - shrink parts count by a factor of 2:1. Unsurprisingly, they are called "Double-Density PLUS Interface." Actually, under optimal conditions certain of these parts can shrink your parts count by as much as 4:1.

Double-Density PLUS ${ }^{m}$ Interface can do wonders to compress the physical size of your logic. Consider, for example, a simple sychronous cross-connection between two 8-bit microprocessor buses, capable of transferring information in either direction one byte at time. This crossconnection can be implemented using two 'LS374 8-bit
noninverting registers, connected "back-to-back" - that is, each 'LS374 has all of its eight outputs tied respectively to the eight inputs of the other one. Together, these two parts total 40 pins and $2\left(0.6^{* 1.1}\right)=2(0.66)=1.32$ square inches, allowing for 100 mils end clearance and 300 mils side clearance as is common practice in board layout.

"... DOUBLE-DENSITY PLUS ${ }^{\text {MM }}$ INTERFACE CAN DO WONDERS TO COMPRESS THE PHYSICAL SIZE OF YOUR LOGIC..."

You may notice that, when these two parts are considered as a functional block, far fewer than 40 pins go to the outside world; there are only the 16 data pins corresponding to the two 8 -bit buses, two clock pins, two output-enable pins, and power and ground. Now, since Monolithic Memories also noticed back-to-back 'LS374s as an attractive low-pin-count combination a couple of years ago, today you have the option of replacing both of these 'LS374's with a single 24-pin, 300-mil "SKINNYDIP ${ }^{\text {® }}$ " 'LS546, which takes up only $\left(0.6^{*} 1.3\right)=0.78$ square inches of your board - slightly more than half as much board area as the two 'LS374s. To summarize:

| DESIGN | BOARD AREA |  | WIRE ENDS |  |
| :---: | :---: | :---: | :---: | :---: |
| SOLUTION | Sq. In. | Normalized | Pin Count | Normalized |
| Two 'LS374s | 1.32 | 1.00 | 40 | 1.00 |
| One 'LS546 | 0.78 | 0.59 | 24 | 0.60 |

Table 1. Board Area and Wire Savings Using 'LS546

[^60]

Figure 1. Logic Distribution on a Typical Board

You also pick up some other benefits along the way making this swap. The two registers within the 'LS546 are appreciably faster than the 'LS374s, and also have a higher output drive - 32 mA sinking current instead of 24 mA . The 'LS546 and 'LS566 have clock enables which operate independently for each register. The 'LS546 also has a cleaned-up "structured" pinout with the 8 pins for each data bus together, each bus having its own side of the 24-pin dual-inline package.

The 'LS546 is comprised of two non-inverting edge-triggered registers. If you are dealing with assertive-low buses and need inverting registers, use an 'LS566. If you prefer latches to registers, use either an 'LS547 (non-inverting) or an 'LS567 (inverting). All of these parts have a common "back-to-back" internal architecture, as shown in Figure 2.


Figure 2. The 546/547/566/567 Block Diagram
Two more famiiies of back-to-back parts also come in the same pinout: the 'LS646/7/8/9 family, and the 'LS651/2/3/4 family. These differ from each other in enable structure; the 'LS646 et. al. have a "direction-control line" so that you can't perform certain operations on both sides of the part simultaneously, whereas the 'LS651 et. al. have generally independent operations on both sides. In each of these families there are two non-inverting parts and two inverting parts; in each case, there is a three-state part and an open-collector part. All of the parts from both families are comprised of "front-loading-latch" individual elements (see


BACK-TO-BACK CONFIGURATION
Figure 3); a front-loading latch is an edge-triggered flipflop in parallel with a buffer, so that the data can be piped through the buffer to reach the output rapidly and then can be subsequently recorded in the flipflop. It is also possible, in a front-loadinglatch structure, to pipe data temporarily around the flipflop to the output without ever recording it in the flipflop. The 'LS646/7/8/9 feature hysteresis on their data inputs as well as on their control inputs, which makes them function well in high-noise environments. The 'LS653/4 are open-collector in one direction, but three-state in the other direction.


Figure 3. The '646-Series/'651-Series Block Diagram

Then there are two "readback" parts, which consists of a latch or register back-to-back with a buffer: the 'LS793 readback latch, and the 'LS794 readback register. Both of these are just 20-pin, and hence offer a full $2: 1$ saving in board area as well as in parts count. They have structured pinouts compatible with those of the 'LS573 and 'LS574, but a very different internal architecture; each of the 8 elements (latch or flipflop) has 2 outputs, one of which is totem-pole and goes to the presumed "output pin" of that element, and the other of which is three-state and goes back to the "input pin" for the element (see Figure 4). Thus, it is possible to read the contents of an 'LS793 or 'LS794 from its input lines by enabling its three-state outputs.


Figure 4. The '793/'794 Block Diagram

The 'LS793 and 'LS794 are intended for use in decentralized systems, for instance industrial-control systems in which a large number of slowly-changing setpoints and displays are under the control of a central microprocessor. The readback feature permits reading one of these, updating it, and replacing it. Without the readback feature, the system would have to keep a redundant copy of the setpoint or display value in main memory, which could cause additional system overhead due to the time-slicing of the microprocessor's activities, or even due to virtual-memory page-faulting in larger systems. Moreover, there is the reliability issue of whether the alleged redundant copy always agrees exactly with the real thing out there in the register controlling the actuator or the display, and what happens whenever it doesn't.

| CONFIGURATION | LATCHES | REGISTERS |
| :--- | :---: | :---: |
| Back-to-Back | '547('373) | $' 546(' 374)$ |
| L/R | '567('533) | $' 566(' 534)$ |
| Back-to-Back |  | $' 646 / 7(' 374)$ |
| Front-Loading |  | $\prime 648 / 9(' 534)$ |
| Latches |  | $' 652 / 4(' 374)$ |
|  |  | $' 651 / 3(' 534)$ |
| Readback L/R | '793('373) | $' 794(' 374)$ |

Table 2. Double-Density PLUS Interface Product

Note that the bracketed part numbers represent the element inside the Double-Density PLUS Interface. For example, a '245 can replace two '244s and a ' 546 can replace two '374s. The same holds true for the ' 646 and ' 651 series. However the '793/'794 are the equivalent of a '373/'374 and a readback buffer such as a '244.

Table 2 is a summary of the Double-Density PLUS Interface product presently available from Monolithic Memories.

Two other common and intuitively-plausible combinations of a couple of 8-bit latches or registers are "nose-to-tail" (one after the other), and "side-by-side" (alternate). If two registers are used in a nose-to-tail combination, for instance, data from the inputs enters the first register when it is clocked, and the outputs of the first register are the inputs of the second register, and thus the same data finally reach the outputs of the combination when the second register is subsequently clocked. And, if two registers are used in a side-by-side combination, their inputs come from the same input bus, and their outputs go to the same output bus, but they can be controlled separately and the output bus can be driven from either one.

Although the nose-to-tail configuration and the side-by-side configuration seem quite different, with the provision of some internal multiplexing the same Double-Density PLUS ${ }^{m}$ Interface part can satisfy both requirements. Such a part is called a pipeline - register or latch, as the case may be. The internal architecture of a two-level pipeline is shown in Figure 5.


Figure 5. The '548/9 Block Diagram

The 'LS548, with the edge-triggered registers, and the 'LS549, with latches, follow the Figure 5 block diagram exactly. Their pinouts resemble those of 'LS546, 'LS646, and 'LS651 families. Their speeds are similar, and they also feature $32-\mathrm{mA}-\mathrm{I} \mathrm{OL}$ outputs.
Typical applications for Double-Density PLUS Interface include computer peripherals, minicomputers, and microcomputers. Applications for the open-collector parts are in the telecommunication and games areas. The drive of these parts enables them to drive heavily-loaded buses, and flat cables.

## 8-Bit Buffer Transceiver <br> SN54LS245

## Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric - equal driving capability in each direction
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface
- Pin-compatible with SN54LS645 - improved speed, IL and IOZL specifications


## Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.
The device allows data transmission from the $A$ bus to the $B$ bus or from the $B$ bus to the $A$ bus depending upon the logic level at the direction-control (DIR) input. The enable input ( $\overline{\mathrm{E}}$ ) can be used to disable the device so that the buses are effectively isolated.

## Logic Symbol



## Ordering Information

| PART <br> NUMBER | TYPE | TEMP | POLARITY | POWER |
| :---: | :---: | :---: | :---: | :---: |
| SN54LS245 | J,L,W | Mil | Noninvert | LS |

## Function Table

| ENABLE <br> $\overline{\mathbf{E}}$ | DIRECTION <br> CONTROL <br> DIR | OPERATION |
| :---: | :---: | :---: |
| L | L | B data to $A$ bus <br> L <br> $H$ |
| H | A data to $B$ bus |  |
| Isolated |  |  |

## IEEE Symbol



## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.7 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\Delta \mathrm{V}_{\mathrm{T}}$ | Hysteresis ( $\mathrm{V}_{\mathrm{T}_{+}-\mathrm{V}_{\mathrm{T}_{-}} \text {) } \mathrm{A} \text { or } \mathrm{B}}$ |  | $V_{C C}=\mathrm{MIN}$ |  | 0.2 | 0.4 |  | V |
| IIL | Low-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.2 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  | $\mathrm{V}_{C C}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | A or B | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 0.1 | mA |
|  |  | DIR or $\bar{E}$ |  | $\mathrm{V}_{1}=7.0 \mathrm{~V}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{IOL}=12 \mathrm{~mA}$ |  | 0.25 | 0.4 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{~V}_{\mathrm{IL}}=\mathrm{MAX} \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \hline \end{aligned}$ | $\mathrm{I}^{\mathrm{OH}}=-3 \mathrm{~mA}$ | 2.4 | 3.4 |  | V |
|  |  |  | $\mathrm{I}^{\mathrm{OH}}=-12 \mathrm{~mA}$ | 2 |  |  |  |  |
| ${ }^{\text {I OZL }}$ | Off-state output current |  |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -200 | $\mu \mathrm{A}$ |
| $\mathrm{I}^{\mathrm{OZH}}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IOS | Output short-circuit current* |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -40 |  | -225 | mA |
| ${ }^{\prime} \mathrm{CC}$ | Supply Current | Outputs High | $V_{C C}=$ MAX. Outputs open |  |  | 48 | 70 | mA |
|  |  | Outputs Low |  |  |  | 62 | 90 |  |
|  |  | Outputs Disabled |  |  |  | 64 | 95 |  |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $\mathrm{vcC}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | A to B DIRE MIN TYP | CTION MAX | B to A DIRE MIN TYP | CTION MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| tPLH | Data to output delay | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ | 8 | 12 | 8 | 12 | ns |
| tPHL |  |  | 8 | 12 | 8 | 12 | ns |
| tPZL | Output enable delay |  | 27 | 40 | 27 | 40 | ns |
| tpZH |  |  | 25 | 40 | 25 | 40 | ns |
| tPZL | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ | 15 | 25 | 15 | 25 | ns |
| tPHZ |  |  | 15 | 25 | 15 | 25 | ns |

## Test Load



## Test Waveforms

> and observed by instrumentation.


Notes: $A$. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series $54 \mathrm{LS}, \mathrm{R}_{\mathrm{O}}=5 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $P R R \leq 1 \mathrm{MHz}$. $\mathrm{Z}_{\text {OUT }}=50 \Omega$ and:
For series 54S, $\mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$.
For Series 54LS, $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

## 8-Bit Buffer Transceivers SN54LS645

## Features/Benefits

- Three-state outputs drive bus lines
- Low current PNP inputs reduce loading
- Symmetric - equal driving capability in each direction
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface


## Description

These 8-bit bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.
The device allows data transmission from the $A$ bus to the $B$ bus or from the $B$ bus to the $A$ bus depending upon the logic level at the direction-control (DIR) input. The enable input ( $\bar{E}$ ) can be used to disable the device so that the buses are effectively isolated.
All of the 8 -bit devices are packaged in the popular 20-pin SKINNYDIP.

## Logic Symbol



## Ordering Information

| PART <br> NUMBER | TYPE | TEMP | POLARITY | POWER |
| :---: | :---: | :---: | :---: | :---: |
| SN54LS645 | J,L,W | Mil | Noninvert | LS |

## Function Table

| ENABLE <br> $\bar{E}$ | DIRECTION <br> CONTROL <br> DIR | OPERATION |
| :---: | :---: | :---: |
| $L$ | $L$ | B data to $A$ bus <br> $L$ |
| $H$ | $X$ | A data to $B$ bus |
| Isolated |  |  |

## IEEE Symbol



## Absolute Maximum Ratings

Supply voltage $\mathrm{V}_{\mathrm{C}}$. .................................................................................................. -0.5 V to 7 V
Input voltage ................................................................................................................... -1.5 V to 7 V
Off-state output voltage
-0.5 V to 5.5 V
Storage temperature
$-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER | MILITARY |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature | -55 |  | 125 | ${ }^{\circ} \mathrm{C}$ |

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MIN | MILITARY TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.7 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 |  |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $I_{1}=-18 \mathrm{~mA}$ |  |  | -1.5 | V |
| $\Delta \mathrm{V}_{\mathrm{T}}$ |  |  | $V_{C C}=$ MIN |  | 0.2 | 0.4 |  | V |
| $\mathrm{I}_{\text {IL }}$ | Low-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  |  | -0.2 | mA |
| ${ }^{1} \mathrm{H}$ | High-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | A or B | $V_{C C}=$ MAX | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ |  |  | 0.1 | mA |
|  |  | DIR or $\bar{E}$ |  | $\mathrm{V}_{1}=7.0 \mathrm{~V}$ |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{lOL}=12 \mathrm{~mA}$ |  | 0.25 | 0.4 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{I}^{\mathrm{OH}}=-3 \mathrm{~mA}$ | 2.4 | 3.4 |  | V |
|  |  |  | $\mathrm{l}^{\mathrm{OH}}=-12 \mathrm{~mA}$ | 2 |  |  |  |  |
| 'OZL | Off-state output current |  |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  |  | -200 | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  |  |  | 20 | $\mu \mathrm{A}$ |
| IOS | Output short-circuit current* |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -40 |  | -225 | mA |
| ${ }^{1} \mathrm{Cc}$ | Supply Current | Outputs High | $V_{C C}=$ MAX. Outputs open |  |  | 48 | 70 | mA |
|  |  | Outputs Low |  |  |  | 62 | 90 |  |
|  |  | Outputs Disabled |  |  |  | 64 | 95 |  |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.


## Switching Characteristics $\mathrm{VCC}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | A to B DIRECTION MIN TYP MAX | B to A DIRECTION MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| tPLH | Data to output delay | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ | $8 \quad 15$ | $8 \quad 15$ | ns |
| tPHL |  |  | $11 \quad 15$ | $11 \quad 15$ | ns |
| tPZL | Output enable delay |  | 31.40 | 31.40 | ns |
| tPZH |  |  | $26 \quad 40$ | $26 \quad 40$ | ns |
| tplZ | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=667 \Omega$ | $15 \quad 25$ | $15 \quad 25$ | ns |
| tPHZ |  |  | 15 - 25 | $15 \quad 25$ | ns |

## Test Load

## Test Waveforms

* The "TEST POINT" is driven by the output under test,
and observed by instrumentation.


Propagation Delay
$\mathbf{V}_{\mathbf{T}}=\mathbf{1 . 3} \mathbf{V}$
Enable and Disable

Notes: $A$. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. For Series $54 \mathrm{LS}, \mathrm{R}_{\mathrm{O}}=5 \mathrm{~K}, \mathrm{~V}_{\mathrm{T}}=1.3 \mathrm{~V}$.
D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz} . \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and: For series $54 \mathrm{~S}, \mathrm{t}_{\mathrm{R}} \leq 2.5 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$. For Series $54 \mathrm{LS}, \mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns}, \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
G. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

# 8-Bit Bus Register Transceivers and Latch Transceivers SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567 

## Features/Benefits

- Bidirectional transceivers utilizing registers or latches
- Faster than other LS-TTL registers/latches
- Independent registers/latches for $A$ bus and B bus
- Data can be swapped between internal registers/latches
- 8-bit data paths match byte boundaries
- 'LS546/547/566/567 can replace two 'LS374/373/534/533 devices
- Independent clock/gate enables for rank $A$ and rank $B$
- High drive capability: IOL = 32 mA (COM), 24 mA (MIL)
- 24-pin SKINNYDIP® saves space
- Three-state outputs drive bus lines
- The clock, clock-enable, and latch-enable inputs typically have $\mathbf{3 0 0} \mathbf{~ m V}$ hysteresis

There are independent clock and clock enable controls for the two directions namely CKA, CKB, CKEĀ, CKEB for 'LS546/ 'LS566, and independent gate enable control GA1, GA2, GB1 and $\overline{G B 2}$ for 'LS547/'LS567. The CKA/B and CKEA/B can control the internal registers $A / B$ to load data or hold data. Similarly, the GA1, $\overline{\mathrm{GA} 2}, \mathrm{~GB} 1$ and $\overline{\mathrm{GB2}}$ can govern the internal latches, $A / B$ to pass or hold data.

## Description

These devices are comprised of a pair of 8-bit registers ('LS546, 'LS566), or a pair of 8-bit latches ('LS547, 'LS567).
The direction of operation is controlled by $\overline{\mathrm{OEAB}}$ and $\overline{\mathrm{OEBA}}$. When $\overline{O E A B}$ is Low and $\overline{O E B A}$ is High, the operation of the registers/latches is A-to-B direction; when $\overline{O E A B}$ is High and $\overline{\text { OEBA }}$ is low, the operation of the registers/latches is B-to-A direction; when $\overline{O E A B}$ and $\overline{O E B A}$ both are High, the $A, B$ buses both are inputs, data will be stored into registers/latches; when $\overline{O E A B}$ and $\overline{O E B A}$ both are Low, the $A, B$ buses both are outputs, data will transfer from internal registers/latches to $A, B$ buses.
There are independent clock and clock enable controls for the two directions: namely CKA, CKB, $\overline{\mathrm{CKEA}}$ and $\overline{\mathrm{CKEB}}$ for 'LS546/'LS566, and independent gate enable control GA1, $\overline{\mathrm{GA} 2}$, GB1 and GB2 for 'LS547/'LS567. The CKA/B and CKEA/B can control the internal registers $A / B$ to load data or hold data. Similarly, the GA1, GA2, GB1 and $\overline{\mathrm{GB} 2}$ govern the internal latches, A/B to pass or hold data.
The 'LS546/'547 provide non-inverting polarity; the 'LS566/'LS567 provide inverting polarity. The 'LS546/'LS547/'LS566/'LS567 all have 3 -state outputs, and have $32-\mathrm{mA}$ output drive $\mathrm{I}^{\mathrm{OL}}$ (COM) over the commercial temperature range and $24-\mathrm{mA}$ output drive $\mathrm{I}_{\mathrm{OL}}$ (MIL), over the military temperature range.
All of the devices are packaged in the popular 24-pin SKINNYDIP package.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE | POLARITY | TYPE | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS546 | JS, W, L (28) | Mil | Non-invert |  | LS |
| SN74LS546 | NS, JS, NL (28) | Com |  | Register |  |
| SN54LS547 | JS, W, L (28) | Mil |  | Latch |  |
| SN74LS547 | NS, JS, NL (28) | Com |  | Laton |  |
| SN54LS566 | JS, W, L (28) | Mil | Invert | Register |  |
| SN74LS566 | NS, JS, NL (28) | Com |  |  |  |
| SN54LS567 | JS, W, L (28) | Mil |  | Latch |  |
| SN74LS567 | NS, JS, NL (28) | Com |  | Latch |  |

## Pin Configurations



SN74LS566

|  | 4 | 3 | 2 | 1 | 28 | 27 | 26 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| OEAB CKA NC VCC CKB CKEB |  |  |  |  |  |  |  |  |
| 5 | AO | $\overline{C K E A}$ |  |  |  |  | $\overline{\text { OEBA }}$ | 25 |
| 6 | A1 |  |  |  |  |  | B0 | 24 |
| 7 | A2 |  |  |  |  |  | B1 | 23 |
| 8 | NC |  |  |  |  |  | NC | 22 |
| 9 | A3 |  |  |  |  |  | B2 | 21 |
| 10 | A4 |  |  |  |  |  | B3 | 20 |
| 11 | A5 |  |  |  |  |  | B4 | 19 |
|  |  | A7 | GND | NC | B7 | B6 | B5 |  |
|  | 12 | 13 | 14 | 15 | 16 | 17 | 18 |  |
|  |  | Plas | stic | Chip | Ca | rier |  |  |

SN74LS567


## Logic Diagram

SN54/74LS546
REGISTER TRANSCEIVER NON-INVERTING OUTPUTS


## Logic Diagram



## Logic Diagram

## SN54/74LS566

REGISTER TRANSCEIVER INVERTING OUTPUTS


## Logic Diagram



## Block Diagrams


'LS547 (Non-inverting)


## 'LS566 (Inverting)


'LS567 (Inverting)


## IEEE Symbols

'LS546

'LS566

'LS547

'LS567


## Function Table Nomenclature Description

A0-A7:
Eight input/output pins on the A side.
B0-B7
Eight input/output pins on the $B$ side.
X:
Hor Lstate irrelevant ("Don't Care" conditions).

GA1/GA2:
Gate enables for rank $A$ of 'LS547/'LS567.
GB1/GB2: Gate enables for rank B of 'LS547/'LS567.

QoA/QoB: Previous data of the internal rank $A / B$.

| GA1 | GA2 | RANK A | GB1 | GB2 | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: |
| X | L | Enabled <br> (Flush) | X | L | Enabled <br> (Flush) |
| X | L | Enabled <br> (Flush) | L | H | Disabled <br> (Freeze) |
| X | L | Enabled <br> (Flush) | H | X | Enabled <br> (Flush) |
| L | H | Disabled <br> (Freeze) | H | X | Enabled <br> (Flush) |
| L | H | Disabled <br> (Freeze) | X | L | Enabled <br> (Flush) |
| L | H | Disabled <br> (Freeze) | L | H | Disabled <br> (Freeze) |
| H | X | Enabled <br> (Flush) | X | L | Enabled <br> (Flush) |
| H | X | Enabled <br> (Flush) | L | H | Disabled <br> (Freeze) |
| H | X | Enabled <br> (Flush) | H | X | Enabled <br> (Flush) |

$\overline{\text { CKEA }} / \overline{\text { CKEB: }}$ : Clock enable for rank $A / B$ of 'LS546/'LS566.
CKA/CKB: Clock for rank A/B of 'LS546/'LS566.
UC: $\quad H$ or L or ! case (nonclocked operation)
$t: \quad$ Positive edge of CK causes clocking, if clock enable is asserted.

| CKA | $\overline{C K E A}$ | RANK A | CKB | CKEB | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: |
| UC | X | Disabled | UC | X | Disabled |
| $\dagger$ | L | Enabled | 1 | L | Enabled |
| $\dagger$ | L | Enabled | 1 | H | Disabled |
| 1 | H | Disabled | 1 | L | Enabled |
| $\dagger$ | H | Disabled | 1 | H | Disabled |

$\overline{\text { OEAB: }} \quad$ To enable the A-to-B operation.
$\overline{\text { OEBA: }} \quad$ To enable the $B$-to-A operation.

| $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | OPERATION DIRECTION |
| :---: | :---: | :--- |
| L | L | A, B buses both are outputs <br> (Transfer stored data to bus stored) |
| L | $H$ | A-to-B |
| $H$ | L | B-to-A |
| $H$ | H | A, B buses both are inputs (storage) |

## Pin Configuration



## Bus Operation For 'LS546

| OPERATION | DIRECTION CONTROL |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{array}{\|c\|} \hline \text { CLOCK } \\ \text { ENABLE }(\mathrm{A}) \\ \hline \end{array}$ |  | RANK A | CLOCK <br> ENABLE (B) |  | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | A0-A7 | B0-B7 |  | CKA | $\overline{\text { CKEA }}$ |  | CKB | $\overline{\text { CKEB }}$ |  |
| Storage | H | H | Input | Input |  | UC | X | QoA | UC | X | Qob |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | L | $B$ bus |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | H | Qob |
|  |  |  |  |  |  | $\dagger$ | L | A bus | UC | X | Qob |
|  |  |  |  |  |  | $\dagger$ | L | A bus | 1 | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | L | A bus | 1 | H | Qob |
|  |  |  |  |  |  | 1 | H | QoA | UC | X | Qob |
|  |  |  |  |  |  | $\dagger$ | H | QoA | 1 | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | H | QoA | 1 | H | Qob |
| B-to-A <br> Operation | H | L | Output of <br> Rank B | Input |  | UC | X | QoA | UC | X | Qob |
|  |  |  |  |  |  | UC | X | QoA | 1 | L | $B$ bus |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | H | QoB |
|  |  |  |  |  |  | $\dagger$ | L | Rank B | UC | X | QoB |
|  |  |  |  |  |  | $\dagger$ | L | Rank B | 1 | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | L | Rank B | $\dagger$ | H | Qob |
|  |  |  |  |  |  | $\dagger$ | H | QoA | UC | X | QoB |
|  |  |  |  |  |  | $\dagger$ | H | QoA | 1 | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | H | QoA | $\dagger$ | H | QoB |
| A-to-B <br> Operation | L | H | Input |  |  | UC | X | QoA | UC | X | QoB |
|  |  |  |  |  |  | UC | X | QoA | 1 | L | Rank A |
|  |  |  |  |  |  | UC | X | QoA | 1 | H | Qob |
|  |  |  |  |  |  | 1 | L | A bus | UC | X | QoB |
|  |  |  |  |  |  | $\dagger$ | L | A bus | 1 | L | Rank A |
|  |  |  |  |  |  | $\dagger$ | L | A bus | 1 | H | QoB |
|  |  |  |  |  |  | $\dagger$ | H | QoA | UC | X | QoB |
|  |  |  |  |  |  | 1 | H | QoA | 1 | L | Rank A |
|  |  |  |  |  |  | 1 | H | QoA | $\dagger$ | H | Qob |
| Transfer Stored Data | L | L | Output of Rank B |  |  | UC | X | QoA | UC | X | QoB |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | L | Rank A |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | H | Qob |
|  |  |  |  |  |  | 1 | L | Rank B | UC | X | Qob |
|  |  |  |  |  |  | $\dagger$ | L | Rank B | 1 | L | Rank A |
|  |  |  |  |  |  | 1 | L | Rank B | 1 | H | Qob |
|  |  |  |  |  |  | $\dagger$ | H | QoA | UC | X | Qob |
|  |  |  |  |  |  | $\dagger$ | H | QoA | 1 | L | Rank A |
|  |  |  |  |  |  | 1 | H | QoA | 1 | H | Qob |

## Bus Operation For 'LS547

| OPERATION | DIRECTION CONTROL |  | DATA I/O |  | BLOCK DIAGRAM | GATE ENABLE (A) |  | RANK A | GATE <br> ENABLE (B) |  | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | A0-A7 | B0-B7 |  | GA1 | $\overline{\text { GA2 }}$ |  | GB1 | $\overline{\text { GB2 }}$ |  |
| Storage | H | H | Input | Input |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | L | H | QoB |
|  |  |  |  |  |  | H | X | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | L | H | QoB |
|  |  |  |  |  |  | X | L | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | X | L | $B$ bus |
| B-to-A <br> Operation | H | L | Output of Rank B | Input |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | B bus |
|  |  |  |  |  |  | H | X | Rank B | L | H | QoB |
|  |  |  |  |  |  | H | X | Rank B | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | Rank B | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | Rank B | L | H | QoB |
|  |  |  |  |  |  | X | L | Rank B | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | Rank B | X | L | $B$ bus |
| A-to-B Operation | L | H | Input | Output of <br> Rank A |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | Rank A |
|  |  |  |  |  |  | L | H | QoA | X | L | Rank A |
|  |  |  |  |  |  | H | X | A bus | L | H | QoB |
|  |  |  |  |  |  | H | X | A bus | H | X | Rank A |
|  |  |  |  |  |  | H | X | A bus | X | L | Rank A |
|  |  |  |  |  |  | X | L | A bus | L | H | Qob |
|  |  |  |  |  |  | X | L | A bus | H | X | Rank A |
|  |  |  |  |  |  | X | L | A bus | X | L | Rank A |
| Transfer Stored Data | L | L | Output of <br> Rank B | Output of <br> Rank A |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | Rank A |
|  |  |  |  |  |  | L | H | QoA | X | L | Rank A |
|  |  |  |  |  |  | H | X | Rank B | L | H | Qob |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | $x$ | Rank B | H | X | Rank A |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | X | Rank B | X | L | Rank A |
|  |  |  |  |  |  | X | L | Rank B | L | H | Qob |
|  |  |  |  |  |  | $\mathrm{X}^{\star}$ | L | Rank B | H | X | Rank A |
|  |  |  |  |  |  | ${ }^{*}$ | L | Rank B | X | L | Rank A |

[^61]Bus Operation For 'LS566

| OPERATION | DIRECTION CONTROL |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{gathered} \text { CLOCK } \\ \text { ENABLE (A) } \end{gathered}$ |  | RANK A | $\begin{array}{\|c\|} \hline \text { CLOCK } \\ \text { ENABLE (B) } \\ \hline \end{array}$ |  | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | A0-A7 | B0-B7 |  | CKA | $\overline{\text { CKEA }}$ |  | CKB | $\overline{\text { CKEB }}$ |  |
| Storage | H | H | Input | Input |  | UC | X | QoA | UC | X | Qob |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | L | $B$ bus |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | H | QoB |
|  |  |  |  |  |  | $\dagger$ | L | A bus | UC | X | Qob |
|  |  |  |  |  |  | 1 | L | A bus | 1 | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | L | A bus | $\dagger$ | H | QoB |
|  |  |  |  |  |  | $\dagger$ | H | QoA | UC | X | Qob |
|  |  |  |  |  |  | $\dagger$ | H | QoA | 1 | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | H | QoA | $\dagger$ | H | Qob |
| B-to-A Operation | H | L | $\begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { Rank B } \end{aligned}$ | Input |  | UC | X | QoA | UC | X | QoB |
|  |  |  |  |  |  | UC | X | QoA | 1 | L | $B$ bus |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | H | Qob |
|  |  |  |  |  |  | $\dagger$ | L | $\overline{\text { Rank B }}$ | UC | X | QoB |
|  |  |  |  |  |  | $\dagger$ | L | $\overline{\text { Rank B }}$ | $\dagger$ | L | $B$ bus |
|  |  |  |  |  |  | $\dagger$ | L | $\overline{\text { Rank B }}$ | $\dagger$ | H | Qob |
|  |  |  |  |  |  | 1 | H | QoA | UC | X | Qob |
|  |  |  |  |  |  | 1 | H | QoA | $\dagger$ | L | B bus |
|  |  |  |  |  |  | 1 | H | QoA | 1 | H | Qob |
| A-to-B <br> Operation | L | H | Input | $\begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { Rank A } \end{aligned}$ |  | UC | X | QoA | UC | X | Qob |
|  |  |  |  |  |  | UC | X | QoA | 1 | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | UC | X | QoA | 1 | H | Qob |
|  |  |  |  |  |  | $\dagger$ | L | A bus | UC | X | Qob |
|  |  |  |  |  |  | 1 | L | A bus | $\dagger$ | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | 1 | L | A bus | $\dagger$ | H | Qob |
|  |  |  |  |  |  | 1 | H | QoA | UC | X | QoB |
|  |  |  |  |  |  | 1 | H | QoA | 1 | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | 1 | H | QoA | $\dagger$ | H | QoB |
| Transfer Stored Data | L | L | $\begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { Rank B } \end{aligned}$ |  |  | UC | X | QoA | UC | X | QoB |
|  |  |  |  |  |  | UC | X | QoA | 1 | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | UC | X | QoA | $\dagger$ | H | Qob |
|  |  |  |  |  |  | 1 | L | $\overline{\text { Rank B }}$ | UC | X | QoB |
|  |  |  |  |  |  | 1 | L | $\overline{\text { Rank B }}$ | $\dagger$ | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | 1 | L | $\overline{\text { Rank B }}$ | $\dagger$ | H | QoB |
|  |  |  |  |  |  | 1 | H | QoA | UC | X | QoB |
|  |  |  |  |  |  | 1 | H | QoA | 1 | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | 1 | H | QoA | $\dagger$ | H | QoB |

## Bus Operation For 'LS567

| OPERATION | DIRECTION CONTROL |  | DATA I/O |  | BLOCK DIAGRAM | GATE ENABLE (A) |  | RANK A | GATE ENABLE (B) |  | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | A0-A7 | B0-B7 |  | GA1 | $\overline{\text { GA2 }}$ |  | GB1 | $\overline{\text { GB2 }}$ |  |
| Storage | H | H | Input | Input |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | L | H | QoB |
|  |  |  |  |  |  | H | X | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | L | H | QoB |
|  |  |  |  |  |  | X | L | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | X | L | $B$ bus |
| B-to-A <br> Operation | H | L | $\begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { ank B } \end{aligned}$ | Input |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | $\overline{\text { Rank B }}$ | L | H | QoB |
|  |  |  |  |  |  | H | X | $\overline{\text { Rank B }}$ | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | $\overline{\text { Rank B }}$ | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | $\overline{\text { Rank B }}$ | L | H | Qob |
|  |  |  |  |  |  | X | L | $\overline{\text { Rank B }}$ | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | $\overline{\text { Rank B }}$ | X | L | B bus |
| A-to-B <br> Operation | L | H | Input | $\begin{array}{\|l} \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ \hline \text { Rank A } \end{array}$ |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | L | H | QoA | X | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | H | X | A bus | L | H | Qob |
|  |  |  |  |  |  | H | X | A bus | H | X | Rank A |
|  |  |  |  |  |  | H | X | A bus | X | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | X | L | A bus | L | H | Qob |
|  |  |  |  |  |  | X | L | A bus | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | X | L | A bus | X | L | $\overline{\text { Rank A }}$ |
| Transfer Stored Data | L | L | $\begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { Rank B } \end{aligned}$ | $\begin{aligned} & \left.\begin{array}{l} \text { Output } \\ \text { of } \\ \hline \text { Rank A } \end{array} \right\rvert\, \end{aligned}$ |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | L | H | QoA | X | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | H | X | Rank B | L | H | Qob |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | X | $\overline{\text { Rank B }}$ | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | X | Rank B | X | L | Rank A |
|  |  |  |  |  |  | X | L | $\overline{\text { Rank B }}$ | L | H | QoB |
|  |  |  |  |  |  | $\mathrm{X}^{*}$ | L | $\overline{\text { Rank B }}$ | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | $\mathrm{X}^{*}$ | L | $\overline{\text { Rank B }}$ | X | L | $\overline{\text { Rank A }}$ |

[^62]
## Absolute Maximum Ratings



## Operating Conditions

|  | PARAMETER |  |  |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{T} W$ | Width of clock/gate | 'LS546, 'LS566 | High | CK | 11 |  |  | 8 |  |  | ns |
|  |  |  | Low |  | 19 |  |  | 15 |  |  |  |
|  |  | 'LS547, 'LS567 | High | GA1,GB1 | 10 |  |  | 8 |  |  |  |
|  |  |  | Low | $\overline{\mathrm{GA2}}, \overline{\mathrm{GB2}}$ | 18 |  |  | 16 |  |  |  |
| $\mathrm{T}_{\text {su }}$ | Setup time | 'LS546 | CKA, | CKB | 141 |  |  | 111 |  |  | ns |
|  |  | 'LS547 | GA1, | GB1 | 51 |  |  | 51 |  |  |  |
|  |  |  | $\overline{\mathrm{GA} 2}$, | GB2 | $15 \dagger$ |  |  | 151 |  |  |  |
|  |  | 'LS566 | CKA, | CKB | 141 |  |  | 111 |  |  |  |
|  |  | 'LS567 | GA1, | B1 | 13. |  |  | 13. |  |  |  |
|  |  |  | GA2, | B2 | 221 |  |  | 221 |  |  |  |
| $T_{h}$ | Hold time | 'LS546 | CKA, | CKB | 01 |  |  | 01 |  |  | ns |
|  |  | 'LS547 | GA1, | B1 | 13. |  |  | 131 |  |  |  |
|  |  |  | $\overline{\text { GA2, }}$ | B2 | 51 |  |  | 51 |  |  |  |
|  |  | 'LS566 | CKA, | KB | 01 |  |  | 01 |  |  |  |
|  |  | 'LS567 | GA1, | B1 | 11. |  |  | 111 |  |  |  |
|  |  |  | $\overline{\mathrm{GA2}}$, | B2 | 51 |  |  | $5 \uparrow$ |  |  |  |
| $\mathrm{T}_{\text {suce }}$ | Setup time for $\overline{\text { CKEA }}$, $\overline{\mathrm{CKEB}}$, ('LS546, 'LS566 only) |  |  |  | 151 |  |  | 111 |  |  | ns |
| Thce | Hold time for $\overline{\text { CKEA, }}$, $\overline{\text { CKEB }}$ ('LS546, 'LS566 only) |  |  |  | 51 |  |  | 41 |  |  | ns |

$\dagger \downarrow$ the arrow indicates the transition of the clock/gate input used for reference:
$t$ for the low-to-high transitions.
। for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | MILITARY MIN TYP MAX | COM MIN | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  | 2 | 2 |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \quad \mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -1.5 |  | -1.5 | V |
| IIL | Low-level input current |  | $\begin{aligned} & V_{C C}=\mathrm{MAX} \\ & V_{1}=0.4 \mathrm{~V} \end{aligned}$ | A or B | -250 |  | -250 | $\mu \mathrm{A}$ |
|  |  |  | All others | -400 |  | -400 |  |
| 1 IH | High-level input current |  |  | $V_{C C}=$ MAX |  | 20 |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | A or B | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ | 0.1 | 0.1 |  | mA |
|  |  | All others |  | $\mathrm{V}_{1}=7.0 \mathrm{~V}$ |  |  |  |  |
| $\mathrm{V}_{\text {OL }}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{I}_{\mathrm{OL}}=24 \mathrm{~mA}$ | 0.5 |  |  | V |
|  |  |  | $\mathrm{I}_{\mathrm{OL}}=32 \mathrm{~mA}$ |  |  | 0.5 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | ${ }^{1} \mathrm{OH}=-1 \mathrm{~mA}$ | 2.43 .4 |  |  | V |
|  |  |  | $\mathrm{IOH}^{\prime}=-2.6 \mathrm{~mA}$ |  |  | 2.4 |  |  |  |
| ${ }^{1} \mathrm{OZL}$ | Ofi-state output current |  | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ | -250 |  | -250 | $\mu \mathrm{A}$ |  |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.4 \mathrm{~V}$ | 20 |  | 20 |  |  |
| ${ }^{\prime} \mathrm{OS}$ | Output short-circuit current* |  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  | -30 -130 | $-30$ | -130 | mA |
| ${ }^{\prime} \mathrm{Cc}$ | Supply current |  | $V_{C C}=M A X$ <br> Outputs open | 'LS546 | 180 |  | 180 | mA |  |
|  |  |  | 'LS547 | 180 |  | 180 |  |  |
|  |  |  | 'LS566 | 180 |  | 180 |  |  |
|  |  |  | 'LS567 | 180 |  | 180 |  |  |

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.


## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY |  |  |  | COMMERCIAL |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 'LS546 |  | 'LS547 |  | 'LS546 |  | 'LS547 |  |  |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency |  |  | 33 |  |  |  | 43 |  |  | MHz |
| ${ }^{\text {P PLH }} /{ }^{\text {t PHL }}$ | CK to output delay ('LS546 only) | $=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 26 |  |  |  | 21 |  |  | ns |
| ${ }^{\text {tPLH }} /{ }^{\text {t PHL }}$ | GA1, $\overline{\mathrm{GA}}$, GB1 or GB2 to output delay ('LS547 only) | $\overline{\mathrm{OE}}=\mathrm{L}$ |  |  |  | 27 |  |  |  | 24 | ns |
| ${ }^{\text {t }}$ PLH/t ${ }^{\text {PHL }}$ | Data D to output delay ('LS547 only) |  |  |  |  | 23. |  |  |  | 18 | ns |
| ${ }^{\text {t }}$ PZL $/{ }^{\text {P }}$ PZH | Output enable delay | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 25 |  | 25 |  | 21 |  | 21 | ns |
| ${ }^{\text {t }} \mathrm{PLZ} /{ }^{\text {/ }} \mathrm{PHZ}$ | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 22 |  | 22 |  | 19 |  | 19 | ns |

## Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=\mathbf{5} \mathbf{V}, \mathrm{T}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS | $\begin{aligned} & \text { 'LS546 } \\ & \text { MIN MAX } \end{aligned}$ | $\begin{gathered} \text { 'LS547 } \\ \text { MIN MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency | $\begin{gathered} \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \quad R_{\mathrm{L}}=280 \Omega \\ \overline{\mathrm{OE}}=\mathrm{L} \end{gathered}$ | 50 |  | MHz |
| ${ }^{\text {P PLH }} /{ }^{\text {t }} \mathrm{PHL}$ | CK to output delay ('LS546 only) |  | 19 |  | ns |
| ${ }^{\text {P PLH }} /{ }^{\text {P PHL }}$ | GA1, $\overline{\mathrm{GA2}}, \mathrm{~GB} 1$ or $\overline{\mathrm{GB} 2}$ to output delay ('LS547 only) |  |  | 23 | ns |
|  | Data D to output delay ('LS547 only) |  |  | 17 | ns |
|  | Output enable delay | $\mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 19 | 19 | ns |
| ${ }_{\text {t }}$ | Output disable delay | $\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 17 | 17 | ns |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS | MILITARY |  |  |  | COMMERCIAL |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 'LS566 |  | 'LS567 |  | 'LS566 |  | 'LS567 |  |  |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency |  |  | 33 |  |  |  | 43 |  |  | MHz |
| ${ }^{\text {tPLH }} /{ }^{\text {P }}$ PHL | CK to output delay ('LS566 only) | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 26 |  |  |  | 21 |  |  | ns |
| ${ }^{\text {tPLH }} /{ }^{\text {/ }} \mathrm{PHL}$ | GA1, $\overline{\mathrm{GA} 2}, \mathrm{~GB} 1$ or GB2 to output delay ('LS567 only) |  |  |  |  | 26 |  |  |  | 24 | ns |
| ${ }^{\text {tPLH }} /{ }^{\text {tPHL }}$ | Data D to output delay ('LS567 only) |  |  |  |  | 29 |  |  |  | 23 | ns |
| ${ }^{\text {t }}$ LZL $/{ }^{\text {t }}$ PZH | Output enable delay | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 25 |  | 25 |  | 21 |  | 21 | ns |
| ${ }^{\text {t PLZ }}$ / ${ }^{\text {P }}$ PHZ | Output disable delay | $C_{L}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 22 |  | 22 |  | 19 |  | 19 | ns |

Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS | $\begin{gathered} \text { 'LS566 } \\ \text { MIN } \quad \text { MAX } \end{gathered}$ | $\begin{gathered} \text { 'LS567 } \\ \text { MIN } \quad \text { MAX } \end{gathered}$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{\text {f MAX }}$ | Maximum clock frequency | $\begin{gathered} \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF} \quad R_{\mathrm{L}}=280 \Omega \\ \overline{\mathrm{OE}}=\mathrm{L} \end{gathered}$ | 50 |  | MHz |
| ${ }^{\text {t }}$ [LH $/{ }^{\text {t }}$ PHL | CK to output delay ('LS566 only) |  | 19 |  | ns |
| ${ }^{\text {t }}{ }^{\text {LH }} /{ }^{\text {t }} \mathrm{PHL}$ | GA1, $\overline{\mathrm{GA} 2}, \mathrm{~GB} 1$ or $\overline{\mathrm{GB} 2}$ to output delay ('LS567 only) |  |  | 21 | ns |
| ${ }^{\text {t }}{ }_{\text {LH }} /{ }^{\text {t }}$ PHL | Data D to output delay ('LS567 only) |  |  | 19 | ns |
| ${ }^{\text {t }}{ }^{\text {PLL }} /{ }^{\text {P }} \mathrm{PZH}$ | Output enable delay | $C_{L}=45 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 19 | 19 | ns |
| ${ }^{\text {t PLZ }} /{ }^{\text {P }} \mathrm{PHZ}$ | Output disable delay | $\mathrm{C}_{\mathrm{L}}=5 \mathrm{pF} \quad \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 17 | 17 | ns |

## Definition of Waveforms



## Definition of Waveforms



GA1, $\overline{\mathbf{G A 2}}, \mathrm{GB} 1$ or $\overline{\mathrm{GB2}}$ to Output Delay

$V_{T}=1.3 V$

## Test Load



ENABLE AND DISABLE

NOTES: A. $\mathrm{C}_{\mathrm{L}}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{Z}_{\mathrm{Out}}=50 \Omega$ and $\mathrm{t}_{\mathrm{R}} \leq 15 \mathrm{~ns} \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

## 8-Bit Bus Front-Loading-Latch Transceivers

## Features/Benefits

- Bidirectional bus transceivers and registers
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® ${ }^{\circledR}$ saves space
- 8-bit data path matches byte boundaries
- Three-state or open-collector outputs drive bus lines


## Description

The 8-bit bus transceivers with 3-state ('LS646, 'LS648) or opencollector ('LS647, 'LS649) outputs have 16 D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS646/647 and 'LS648/649 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "frontloading latch."
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register $A$, which receives data from the $B$ bus directly at

## Pin Configurations

'LS646/647/648/649
8-Bit Bus Front-Loading-Latch Transceivers


## Ordering Information

| PART NUMBER | PKG | TEMP | POLARITY | O/P | PWR |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS646 | JS,W,L (28) | Mil | Noninvert | Three-state | LS |
| SN54LS646 | $\begin{aligned} & \text { NS,JS } \\ & \text { NL (28) } \end{aligned}$ | Com | Noninvert | Three-state | LS |
| SN54LS647 | JS,W,L (28) | Mil | Noninvert | Opencollector | LS <br> LS |
| SN74LS647 | NS,JS <br> NL (28) | Com | Noninvert |  |  |
| SN54LS648 | JS,W,L (28) | Mil | Invert | Three-state | LS |
| SN54LS648 | NS,JS <br> NL (28) | Com | Invert | Three-state | LS |
| SN54LS649 | JS,W,L (28) | Mil | Invert | Open- <br> collector | LS |
| SN74LS649 | NS,JS <br> NL (28) | Com | Invert |  | LS |

its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\bar{E}$, and direction line DIR.
When $\bar{E}$ is High data from the buses can be stored into register $A$ and $B$. When $\bar{E}$ is Low and DIR is High, the direction of operation is from $A$ to $B$; when $\bar{E}$ and DIR are LOW, the direction of operation is from $B$ to $A$.
SRA is used to select between register $A$ and the $B$ bus, and then to route the data to a controlled buffer connected to the $A$ bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the $B$ bus through a controlied buffer.


## Logic Diagrams



* For the 'LS646 devices, the A and B bus outputs are 3-state.

For the 'LS647 devices, the A and B bus outputs are open-collector.


[^63]
## IEEE Symbols

'LS646

'LS648

'LS647

'LS649


## Block Diagrams



## Function Table Nomenclature Description

E: $\quad$ To enable the A-to-B or B-to-A operation
DIR: To select the direction of operation.

| $\bar{E}$ | DIR | OPERATION DIRECTION |
| :---: | :---: | :---: |
| $L$ | $L$ | B-to-A |
| $L$ | $H$ | A-to-B |
| $H$ | $X$ | A and B buses both are inputs (storage) |

SRA/SRB: To select the output data coming from the $A / B$ register if SRA/SRB is a High level; otherwise, directly from the input data bus.
A0-A7: Eight input/output pins on the $A$ side.
B0-B7: Eight input/output pins on the $B$ side.
CKA/CKB: Clock for Register A/B.
X: $\quad H$ or $L$ state irrelevant ("Don't Care" conditions).
t: Positive edge of CK causes clocking, if clock enable is asserted.

UC: $\quad H$ or L or I case (nonclocked operation).
RGTR: Register.

## Bus Operation for 'LS646/647

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | LS646/647 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\bar{E}$ | DIR | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | H | X | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time $A$ bus data $\rightarrow$ RGTR B Real time $B$ bus data $\rightarrow$ RGTR A |
| Real time <br> B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $B$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $B$ bus data $\rightarrow A$ bus <br> Real time $B$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $B$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | $\begin{aligned} & \text { Real time } B \text { bus data } \rightarrow A \text { bus } \\ & \text { Real time } B \text { bus data } \rightarrow \text { RGTR } A \\ & \text { Real time } B \text { bus data } \rightarrow \text { RGTR } B \end{aligned}$ |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | UC | 1 | RGTR A data $\rightarrow$ A bus RGTR A data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time $B$ bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow A$ bus RGTR A data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | L | H | X | L | Input | Output |  | UC | UC | Real time $A$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time $A$ bus data $\rightarrow B$ bus Real time $A$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | $\begin{aligned} & \text { Real time } A \text { bus data } \rightarrow B \text { bus } \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR A } \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR B } \end{aligned}$ |
| Stored data <br> A-to-B <br> Operation | L | H | X | H | Input | Output |  | UC | UC | RGTR B data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time A bus data $\rightarrow$ RGTR B RGTR $B$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR B data $\rightarrow B$ bus RGTR B data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | Real time $A$ bus data $\rightarrow$ RGTR $B$ RGTR B data $\rightarrow B$ bus RGTR B data $\rightarrow$ RGTR A |

## Bus Operation for 'LS648/649

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | 'LS648/649 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\bar{E}$ | DIR | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | H | X | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time $A$ bus data $\rightarrow$ RGTR $B$ Real time B bus data $\rightarrow$ RGTR A |
| Real time B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time $\bar{B}$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR A Real time $\bar{B}$ bus data $\rightarrow$ RGTR $B$ |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR $\bar{A}$ data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | UC | 1 | $\begin{aligned} & \text { RGTR } \bar{A} \text { data } \rightarrow \mathrm{A} \text { bus } \\ & \text { RGTR } \bar{A} \text { data } \rightarrow \text { RGTR } B \end{aligned}$ |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time B bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $\rightarrow A$ bus RGTR $\bar{A}$ data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | L | H | X | L | Input | Output |  | UC | UC | Real time $\bar{A}$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $\bar{A}$ bus data $\rightarrow B$ bus Real time $A$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $\bar{A}$ bus data $\rightarrow B$ bus Real time $\bar{A}$ bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | $\begin{array}{\|l} \hline \text { Real time } \overline{\bar{A}} \text { bus data } \rightarrow B \text { bus } \\ \text { Real time } \bar{A} \text { bus data } \rightarrow \text { RGTR A } \\ \text { Real time } A \text { bus data } \rightarrow \text { RGTR B } \\ \hline \end{array}$ |
| Stored data <br> A-to-B <br> Operation | L | H | X | H | Input | Output |  | UC | UC | RGTR $\bar{B}$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR $\bar{B}$ data $\rightarrow B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR A |

## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of clock | High | 20 |  |  | 20 |  |  | ns |
|  |  | Low | 20 |  |  | 20 |  |  |  |
| ${ }^{\text {tsu }}$ | Setup time | 'LS646 | 201 |  |  | 201 |  |  | ns |
|  |  | 'LS648 | 20 † |  |  | 201 |  |  |  |
| $t^{\prime}$ | Hold time | 'LS646 | 01 |  |  | 01 |  |  | ns |
|  |  | 'LS648 | 01 |  |  | 01 |  |  |  |
| ${ }^{\mathrm{I}} \mathrm{OH}$ | High-level output current |  |  |  | -12 |  |  | -15 | mA |
| $\mathrm{I}_{\mathrm{OL}}$ | Low-level output current |  |  |  | 12 |  |  | 24 | mA |

$\dagger \downarrow$ The arrow indicates the transition of the clock input used for reference. $\dagger$ for the low-to-high transitions. $\downarrow$ for the high-to-low transitions.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  |  | $\begin{gathered} \text { MI } \\ \text { MIN } \end{gathered}$ | ITARY <br> TYP MAX | CON MIN | MERCIAL TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.7 |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  |  | 2 |  | 2 |  | V |
| $V_{I C}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | $I_{1}=-18 \mathrm{~mA}$ |  | -1.5 |  | -1.5 | V |
| $\Delta V_{T}$ | Hysteresis ( $\mathrm{V}_{\mathrm{T}_{+}-\mathrm{V}_{\mathrm{T}_{-}} \text {) }}$ |  | $V_{C C}=$ MIN |  |  | 0.1 | 0.4 | 0.2 | 0.4 | V |
| $\mathrm{IIL}^{\text {L }}$ | Low-level input current |  | $V_{C C}=$ MAX |  | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.4 |  | -0.4 | mA |
| $\mathrm{IIH}^{\text {I }}$ | High-level input current |  | $V_{C C}=M A X$ |  | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | A or B | $V_{C C}=M A X$ |  | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ | 0.1 |  | 0.1 |  | mA |
|  |  | All others |  |  | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ |  | $\mathrm{I}^{\mathrm{OL}}=12 \mathrm{~mA}$ |  | $0.25 \quad 0.4$ |  | $0.25 \quad 0.4$ | V |
|  |  |  | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  |  | $\begin{array}{ll}0.35 & 0.5\end{array}$ |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{\text {IL }}=M A X \\ & V_{I H}=2 V \end{aligned}$ |  | ${ }^{\prime} \mathrm{OH}=-3 \mathrm{~mA}$ | 2.4 | 3.4 | 2.4 | 3.4 | V |
|  |  |  | $\mathrm{IOH}^{\prime}=\mathrm{MAX}$ | 2 |  |  |  | 2 |  |  |  |
| ${ }^{\text {I OZL }}$ | Off-state output current |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -400 |  | -400 | $\mu \mathrm{A}$ |  |
| ${ }^{\text {IOZH }}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |  |  |
| IOS | Output short-circuit current* |  |  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | -40 | -225 | -40 | -225 | mA |
| ${ }^{1} \mathrm{Cc}$ | Supply current |  | $\begin{aligned} & V_{C C}= \\ & M A X \end{aligned}$ | $\begin{aligned} & \text { 'LSS- } \\ & 646 \end{aligned}$ | Outputs High |  | 145 |  | 145 | mA |  |
|  |  |  | Outputs Low |  |  | 165 |  | 165 |  |  |
|  |  |  | Outputs Disabled |  |  | 165 |  | 165 |  |  |
|  |  |  | $\begin{aligned} & \text { 'LS- } \\ & 648 \end{aligned}$ | Outputs High |  | 145 |  | 145 |  |  |
|  |  |  | Outputs Low |  | 165 |  | 165 |  |  |  |  |
|  |  |  | Outputs Disabled |  | 165 |  | 165 |  |  |  |  |

[^64]Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | $\operatorname{MIN} \begin{gathered} \text { 'LS646 } \\ \text { MAX } \end{gathered}$ | $\text { MIN }{ }^{\text {LS648 }} \text { MAX }$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t PLH }}$ | Data to output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 18 | 18 | ns |
| ${ }^{\text {t PHL }}$ |  |  | 20 | 25 | ns |
| ${ }^{\text {tPLH}}$ | Clock to output delay |  | 25 | 25 | ns |
| ${ }^{\text {t PHL }}$ |  |  | 35 | 40 | ns |
| ${ }^{\text {tPLH }}$ | Select to output delay (data input High) |  | 40 | 55 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 35 | 40 | ns |
| ${ }^{\text {t }}$ L ${ }^{\text {LH }}$ | Select to output delay (data input Low) |  | 50 | 40 | ns |
| ${ }^{\text {tPHL }}$ |  |  | 25 | 40 | ns |
| ${ }_{\text {t }}^{\text {PZL }}$ | Output enable delay |  | 65 | 55 | ns |
| ${ }^{\text {tPZH}}$ |  |  | 55 | 50 | ns |
| tplz | Output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | 35 | 45 | ns |
| ${ }^{\text {tPZL }}$ | Direction enable delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 60 | 45 | ns |
| $t_{\text {PZH }}$ |  |  | 45 | 40 | ns |
| ${ }^{\text {t PLZ }}$ | Direction disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 30 | 30 | ns |
| ${ }^{\text {tPHZ }}$ |  |  | 30 | 35 | ns |

## Switching Characteristics Over Operating Range

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIL |  | COM |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{array}{\|c\|} \hline \text { 'LS646 } \\ \text { MIN } \\ \hline \end{array}$ | $\begin{array}{\|c\|c\|c\|c\|c\|} \hline \text { LLS } & \text { MAX } \\ \hline \end{array}$ | $\begin{gathered} \text { 'LS646 } \\ \text { MIN MAX } \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { 'LS648 } \\ \text { MIN MAX } \end{array}$ |  |
| ${ }^{\text {tPLH }}$ | Data to output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 25 | 18 | 25 | 18 | ns |
| ${ }_{\text {tPHL }}$ |  |  | 25 | 25 | 25 | 25 | ns |
| ${ }^{\text {tPLH }}$ | Clock to output delay |  | 28 | 25 | 28 | 25 | ns |
| ${ }_{\text {tPHL }}$ |  |  | 35 | 40 | 35 | 40 | ns |
| ${ }^{\text {tPLH }}$ | Select to output delay $\dagger$ (data input High) |  | 40 | 55 | 40 | 55 | ns |
| ${ }_{\text {tPHL }}$ |  |  | 35 | 40 | 35 | 40 | ns |
| ${ }_{\text {tPLH }}$ | Select to output delay $\dagger$ (data input Low) |  | 50 | 40 | 50 | 40 | ns |
| ${ }^{\text {tPHL }}$ |  |  | 30 | 40 | 30 | 40 | ns |
| ${ }^{\text {tPZL }}$ | Output enable delay |  | 65 | 55 | 65 | 55 | ns |
| ${ }_{\text {tPZH }}$ |  |  | 55 | 50 | 55 | 50 | ns |
| ${ }^{\text {tpLZ }}$ | Output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 45 | 35 | 45 | 35 | ns |
| ${ }^{\text {t PHZ }}$ |  |  | 45 | 50 | 45 | 50 | ns |
| ${ }^{\text {tPZL }}$ | Direction enable delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 60 | 45 | 60 | 45 | ns |
| ${ }^{\text {tPZH }}$ |  |  | 45 | 40 | 45 | 40 | ns |
| $\mathrm{t}_{\mathrm{PL}}$ | Direction disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 40 | 30 | 40 | 30 | ns |
| ${ }_{\text {t }}^{\text {PHZ }}$ |  |  | 45 | 45 | 45 | 45 | ns |

[^65]Absolute Maximum Ratings
Supply voltage, $\mathrm{V}_{\mathrm{CC}}$ ..... 7.0 V
Input voltage, ..... 7.0 V
Off-state output voltage ..... 5.5 V
Storage temperature $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {tw }}$ | Width of clock | High | 20 |  |  | 20 |  |  | ns |
|  |  | Low | 20 |  |  | 20 |  |  |  |
| $\mathrm{t}_{\mathrm{su}}$ | Setup time | 'LS647 | 201 |  |  | 201 |  |  | ns |
|  |  | 'LS649 | 201 |  |  | 201 |  |  |  |
| $t_{h}$ | Hold time | 'LS647 | 01 |  |  | 01 |  |  | ns |
|  |  | 'LS649 | 01 |  |  | 01 |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  |  | 5.5 |  |  | 5.5 | V |
| ${ }^{1} \mathrm{OL}$ | Low-level output current |  |  |  | 12 |  |  | 24 | mA |

$\dagger \downarrow$ The arrow indicates the transition of the clock input used for reference. $\dagger$ for the low-to-high transitions. $\downarrow$ for the high-to-low transitions.

## Electrical Characteristics Over Operating Conditions



* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


## Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveforms) | MIN ${ }^{\text {LS } 647}$ |  | MIN ${ }^{\text {'LS649 }}$ MAX |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX |  |  |  |
| ${ }^{\text {tPLH }}$ | Data to output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ |  | 26 |  | 25 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 27 |  | 30 | ns |
| ${ }^{\text {P PLH }}$ | Clock to output delay |  |  | 35 |  | 30 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  |  | 45 |  | 45 | ns |
| ${ }_{\text {tPLH }}$ | Select to output delay $\dagger$ (data input High) |  |  | 50 |  | 55 | ns |
| ${ }^{\text {t }}$ PHL |  |  |  | 45 |  | 45 | ns |
| ${ }^{\text {tPLH }}$ | Select to output delay $\dagger$ (data input Low) |  |  | 60 |  | 45 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  |  | 30 |  | 40 | ns |
| ${ }^{\text {tPLH }}$ | Output enable delay |  |  | 40 |  | 40 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  |  | 50 |  | 50 | ns |
| $\mathrm{t}_{\mathrm{PLH}}$ | Direction enable delay |  |  | 35 |  | 30 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  |  | 40 |  | 45 | ns |

## Switching Characteristics Over Operating Range

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIL |  | COM |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{array}{\|c\|} \hline \text { 'LS647 } \\ \text { MIN MAX } \end{array}$ | $\begin{gathered} \text { LS } 649 \\ \text { MIN } \end{gathered}$ | $\begin{gathered} \text { 'LS647 } \\ \text { MIN MAX } \end{gathered}$ | $\begin{gathered} \text { 'LS649 } \\ \text { MIN MAX } \end{gathered}$ |  |
| ${ }^{\text {t }}$ PLH | Data to output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 32 | 35 | 32 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 27 | 30 | 27 | 30 | ns |
| ${ }^{\text {tPLH }}$ | Clock to output delay |  | 35 | 40 | 35 | 40 | ns |
| ${ }_{\text {t }}$ PHL |  |  | 45 | 45 | 45 | 45 | ns |
| ${ }_{\text {PLH }}$ | Select to output delay $\dagger$ (data input High) |  | 50 | 55 | 50 | 55 | ns |
| ${ }_{\text {t }}$ |  |  | 45 | 45 | 45 | 45 | ns |
| ${ }_{\text {P PLH }}$ | Select to output delay $\dagger$ (data input Low) |  | 60 | 50 | 60 | 50 | ns |
| ${ }^{\text {tPHL }}$ |  |  | 30 | 40 | 30 | 40 | ns |
| ${ }_{\text {tPLH }}$ | Output enable delay |  | 40 | 45 | 40 | 45 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 50 | 50 | 50 | 50 | ns |
| ${ }^{\text {PLLH }}$ | Direction enable delay |  | 40 | 45 | 40 | 45 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 40 | 45 | 40 | 45 | ns |

[^66]
## Test Waveforms



CK To Bus Output Propagation Delay Time


Figure 3


Figure 4
NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

## Enable/Disable/Direction-Change Delay



$$
v_{T}=1.3 \mathrm{~V}
$$

Figure 5

## Test Loads



Load Circuit For Open-Collector Outputs


Load Circuit For Three-State Outputs

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: $A$. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz} . \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and $\mathrm{t}_{\mathrm{R}}=15 \mathrm{~ns} \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
$F$. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

## 8-Bit Bus Front-Loading-Latch Transceivers SN54/74LS651 SN54/74LS653

## Features/Benefits

- Bidirectional bus transceivers and registers
- Independent registers for $\mathbf{A}$ and $\mathbf{B}$ buses
- Real-time data transfer or stored data transfer
- Simultaneous outputs on both buses
- 24-pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Three-state or open-collector outputs drive bus lines
- 'LS653/4 are open-collector in A direction, three-state in B direction


## Description

These 8-bit bus transceivers with 3-state ('LS651, 'LS652) or open-collector ('LS653, 'LS654) outputs have 16D-type flip-flops and multiplexers. The bus-oriented pinout of the parts is shown in the Pin Configuration. The internal gate-level hardware configurations for the 'LS651/653 and 'LS652/654 are given in their respective Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path or "feed-through" into a two-way mux, is sometimes called a "front-loading latch."
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA clocks register A, which receives data from the B bus directly at its inputs.

## Pin Configurations



## Ordering Information

| PART NUMBER | PKG | TEMP | POLARITY | OUTPUTS | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS651 | JS,W,L* | Mil | Invert | Three-state | LS |
| SN74LS651 | $\begin{array}{\|l\|} \hline \text { NS, JS, } \\ \text { NL (28) } \end{array}$ | Com | Invert | Three-state | LS |
| SN54LS652 | JS,W,L* | Mil | Noninvert | Three-state | LS |
| SN74LS652 | $\begin{array}{\|l\|} \hline \text { NS, JS, } \\ \text { NL (28) } \end{array}$ | Com | Noninvert | Three-state | LS |
| SN54LS653 | JS,W,L* | Mil | Invert | A bus opencollector; B bus three-state | LS |
| SN74LS653 | $\begin{array}{\|l\|} \hline \text { NS, JS, } \\ \text { NL (28) } \end{array}$ | Com | Invert |  | LS |
| SN54LS654 | JS,W,L* | Mil | Noninvert |  | LS |
| SN74LS654 | $\begin{array}{\|l} \text { NS,JS, } \\ \text { NL (28) } \end{array}$ | Com | Noninvert |  | LS |

* L package here is L28. The other packages are 24-pin.

Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{\mathrm{GBA}}$.
When GAB is Low and $\overline{\mathrm{GBA}}$ is High, data from the buses can be loaded into registers $A$ and $B$. When $\overline{G B A}$ is Low, the $A$ bus is configured for output. When GAB is High, the $B$ bus is configured for output. The $A$ and $B$ buses can be enabled at the same time, to operate as outputs simultaneously.
SRA is used to select between register $A$ and the $B$ bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the $B$ bus through a controlled buffer.


## Logic Diagrams



* For the 'LS652 devices, the A bus outputs are 3-state. For the 'LS654 devices, the A bus outputs are open-collector. The $B$ bus outputs are 3 -state for both devices.

* For the 'LS651 devices, the A bus outputs are 3-state. For the 'LS653 devices, the A bus outputs are open-collector.
The B bus outputs are 3 -state for both devices.


## IEEE Symbols

'LS651

'LS652

'LS653

'LS654


## Block Diagrams



* For the 'LS651/652 devices, the A bus outputs are 3-state.

For the 'LS653/654 devices, the A bus outputs are open-collector.
The B bus outputs are 3-state for both devices.

## Function Table <br> Nomenclature Description

GAB: To enable the A-to-B operation.
GBA: To enable the B-to-A operation.

| GAB | $\overline{\text { GBA }}$ | OPERATION DIRECTION |
| :---: | :---: | :--- |
| L | L | B to A |
| L | H | A and B buses both are inputs (storage) |
| H | L | A and B buses both are outputs <br> (Transfer stored data to bus) |
| H | H | A to B |

SRA/SRB: To select the output data coming from the A/B register if SRA/SRB is High level; otherwise, directly from the input data bus.

A0-A7: Eight input/output pins on the $A$ side.
B0-B7: Eight input/output pins on the $B$ side.
CKA/CKB: Clock for Register A/B.
X: $\quad \mathrm{H}$ or L state irrelevant ("Don't Care" conditions).
$t$ : Positive edge of CK causes clocking, if clocking enable is asserted.

UC: $\quad H$ or L or $\downarrow$ case (nonclocked operation).
RGTR: Register.

## Bus Operation for 'LS651/653

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | 'LS651/653 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | GAB | $\overline{\text { GBA }}$ | SRA | SRB | A0-A7 | B0-87 |  | CKA | CKB |  |
| Storage | L | H | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time $A$ bus data $\rightarrow$ RGTR B Real time $B$ bus data $\rightarrow$ RGTR A |
| Real time <br> B-to-A <br> Operation | L | L | L | x | Output | Input |  | UC | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | $\begin{aligned} & \text { Real time } \bar{B} \text { bus data } \rightarrow A \text { bus } \\ & \text { Real time } \bar{B} \text { bus data } \rightarrow \text { RGTR } \end{aligned}$ |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $\bar{B}$ bus data $\rightarrow \mathrm{A}$ bus Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | $\begin{aligned} & \text { Real time } \bar{B} \text { bus data } \rightarrow A \text { bus } \\ & \text { Real time } B \text { bus data } \rightarrow \text { RGTR A } \\ & \text { Real time } \bar{B} \text { bus data } \rightarrow \text { RGTR } B \end{aligned}$ |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR $\bar{A}$ data $\rightarrow \mathrm{A}$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | $\begin{aligned} & \text { RGTR } \overline{\mathrm{A}} \text { data } \rightarrow \mathrm{A} \text { bus } \\ & \text { RGTR } \overline{\mathrm{A}} \text { data } \rightarrow \text { RGTR } B \end{aligned}$ |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | $\begin{aligned} & \text { Real time } B \text { bus data } \rightarrow \text { RGTR } A \\ & \text { RGTR } \bar{A} \text { data } \rightarrow A \text { bus } \\ & \text { RGTR } \bar{A} \text { data } \rightarrow \text { RGTR } B \end{aligned}$ |
| Real time A-to-B Operation | H | H | x | L | Input | Output |  | UC | UC | Real time $\bar{A}$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1. | $\begin{aligned} & \text { Real time } \bar{A} \text { bus data } \rightarrow B \text { bus } \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR } B \end{aligned}$ |
|  |  |  |  |  |  |  |  | 1 | UC | $\begin{aligned} & \text { Real time } \overline{\bar{A}} \text { bus data } \rightarrow B \text { bus } \\ & \text { Real time } \bar{A} \text { bus data } \rightarrow \text { RGTR } A \end{aligned}$ |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | Real time $\overline{\bar{A}}$ bus data $\rightarrow$ B bus Real time bus data $\rightarrow$ RGTR A Real time A bus data $\rightarrow$ RGTR B |
| Stored data <br> A-to-B <br> Operation | H | H | x | H | Input | Output |  | UC | UC | RGTR $\bar{B}$ data $-B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR $\bar{B}$ data $\rightarrow B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR $A$ |
|  |  |  |  |  |  |  |  | 1 | 1 | $\begin{aligned} & \text { Real time A bus data } \rightarrow \text { RGTR B } \\ & \text { RGTR } \bar{B} \text { data } \rightarrow B \text { bus } \\ & \text { RGTR } \bar{B} \text { data } \rightarrow \text { RGTR A } \end{aligned}$ |
| Transfer <br> Stored <br> Data | H | L | H | H | Output | Output |  | UC | UC | RGTR $\bar{A} / \bar{B}$ data $-A / B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | RGTR $\bar{A} / \bar{B}$ data $-A / B$ bus RGTR $\bar{A}$ data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR $\bar{A} / \bar{B}$ data $\rightarrow A / B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | RGTR $\bar{A} / \bar{B}$ data $\rightarrow A / B$ bus RGTR $\bar{A}$ data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow$ RGTR A |

## Bus Operation for 'LS652/654

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | 'LS652/654 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | GAB | $\overline{\text { GBA }}$ | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | L | H | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time A bus data $\rightarrow$ RGTR B Real time B bus data $\rightarrow$ RGTR A |
| Real time <br> B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $B$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $B$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time $B$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR A Real time $B$ bus data $\rightarrow$ RGTR B |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | RGTR A data $\rightarrow$ A bus RGTR A data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time $B$ bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow$ A bus RGTR A data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | H | H | $x$ | L | Input | Output |  | UC | UC | Real time $A$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1. | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR A Real time A bus data $\rightarrow$ RGTR B |
| Stored data <br> A-to-B <br> Operation | H | H | X | H | Input | Output |  | UC | UC | RGTR B data $\rightarrow$ B bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time A bus data $\rightarrow$ RGTR B RGTR B data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR B data $\rightarrow$ B bus RGTR B data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR B data $\rightarrow B$ bus RGTR B data $\rightarrow$ RGTR A |
| Transfer <br> Stored <br> Data | H | L | H | H | Output | Output |  | UC | UC | RGTR A/B data $\rightarrow A / B$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | RGTR A/B data $\rightarrow A / B$ bus RGTR A data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | RGTR A/B data $\rightarrow A / B$ bus RGTR B data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | RGTR A/B data $\rightarrow A / B$ bus RGTR A data $\rightarrow$ RGTR B RGTR B data $\rightarrow$ RGTR A |

```
Absolute Maximum Ratings
Supply voltage V }\mp@subsup{\textrm{VC}}{\textrm{C}}{
    -0.5 V to 7 V
Input voltage .............................................................................................................. - . . . . . . V to 7 VOff-state output voltage0.5 V to 5.5 VStorage temperature\(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
```


## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {w }}$ w | Width of clock | High | 20 |  |  | 20 |  |  | ns |
|  |  | Low | 20 |  |  | 20 |  |  |  |
| ${ }^{\text {tsu}}$ | Setup time | 'LS651 | 201 |  |  | 20 † |  |  | ns |
|  |  | 'LS652 | 201 |  |  | $20 \dagger$ |  |  |  |
| $t_{h}$ | Hold time | 'LS651 | 01 |  |  | 01 |  |  | ns |
|  |  | 'LS652 | 01 |  |  | 01 |  |  |  |
| ${ }^{\mathrm{I}} \mathrm{OH}$ | High-level output current |  |  |  | -12 |  |  | -15 | mA |
| ${ }^{\text {OLI }}$ | Low-level output current |  |  |  | 12 |  |  | 24 | mA |

$\uparrow \downarrow$ The arrow indicates the transition of the clock input used for reference. $\uparrow$ for the low-to-high transitions. $\downarrow$ for the high-to-low transitions.
Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  |  | $\begin{gathered} M \\ \text { MIN } \end{gathered}$ | ITARY TYP MAX | $\begin{aligned} & \text { COM } \\ & \text { MIN } \end{aligned}$ | MERCIAL TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.7 |  | 0.8 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  |  | 2 |  | 2 |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ |  | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -1.5 |  | -1.5 | V |
| ILL | Low-level input current |  | $V_{C C}=$ MAX |  | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.4 |  | -0.4 | mA |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  | $V_{C C}=$ MAX |  | $V_{1}=2.7 \mathrm{~V}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | A or B | $V_{C C}=M A X$ |  | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ | 0.1 |  | 0.1 |  | mA |
|  |  | All others |  |  | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ |  | $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}$ |  | $0.25 \quad 0.4$ |  | $\begin{array}{ll}0.25 & 0.4\end{array}$ | V |
|  |  |  | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  |  | $0.35 \quad 0.5$ |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ |  | ${ }^{\prime} \mathrm{OH}=-3 \mathrm{~mA}$ | 2.4 | 3.4 |  | 3.4 | V |
|  |  |  | $\mathrm{IOH}=$ MAX | 2 |  |  |  | 2 |  |  |  |
| 'OZL | Off-state output current |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 \mathrm{~V} \end{aligned}$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -400 |  | -400 | $\mu \mathrm{A}$ |  |
| $\mathrm{I}^{\mathrm{OZH}}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |  |  |
| Ios | Output short-circuit current* |  |  |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |  | -40 | -225 | -40 | -225 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply current |  | $\begin{aligned} & V_{C C}= \\ & M A X \end{aligned}$ | 'LS- | Outputs High |  | 145 |  | 145 | mA |  |
|  |  |  | Outputs Low |  |  | 165 |  | 165 |  |  |
|  |  |  | Outputs disabled |  |  | 165 |  | 165 |  |  |
|  |  |  | $\begin{aligned} & \text { 'LS- } \\ & 652 \end{aligned}$ | Outputs High |  | 145 |  | 145 |  |  |
|  |  |  | Outputs Low |  | 165 |  | 165 |  |  |  |  |
|  |  |  | Outputs disabled |  | 165 |  | 165 |  |  |  |  |

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics $\mathbf{v}_{\mathbf{C C}}=\mathbf{5 V}, \mathrm{T}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | $\text { MIN }{ }^{\text {'LS651 }} \text { MAX }$ | $\text { MIN }{ }^{\text {'LS652 }} \text { MAX }$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {P PLH }}$ | Data to output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 15 | 15 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 15 | 20 | ns |
| ${ }^{\text {t PLH }}$ | Clock to output delay |  | 20 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 30 | 30 | ns |
| ${ }^{\text {t PLH }}$ | Select to output delay $\dagger$ (data input High) |  | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 20 | 25 | ns |
| ${ }^{\text {P PLH }}$ | Select to output delay $\dagger$ (data input Low) |  | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 30 | 20 | ns |
| ${ }^{\text {t PRL }}$ | $\overline{\mathrm{GBA}}$ to <br> A bus output enable delay |  | 25 | 25 | ns |
| ${ }^{\text {t }} \mathrm{PZ}$ |  |  | 20 | 20 | ns |
| ${ }^{\text {t PLZ }}$ | $\overline{\text { GBA }}$ to <br> A bus output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 25 | 25 | ns |
| ${ }^{\text {t PHZ }}$ |  |  | 35 | 35 | ns |
| ${ }^{\text {t PRL }}$ | GAB to <br> $B$ bus output enable delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 30 | 30 | ns |
| ${ }^{\text {tPZH }}$ |  |  | 25 | 25 | ns |
| $t_{\text {PLZ }}$ | GAB to <br> B bus output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 25 | 25 | ns |
| $\mathrm{t}_{\mathrm{PHZ}}$ |  |  | 35 | 35 | ns |

$\dagger$ See Figure 4.

## Switching Characteristics Over Operating Range

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIL |  | COM |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $$ | $$ | $$ | $$ |  |
| ${ }^{\text {P PLH }}$ | Data to output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 20 | 20 | 15 | 20 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 20 | 25 | 17 | 22 | ns |
| ${ }^{\text {t PLH }}$ | Clock to output delay |  | 25 | 25 | 22 | 22 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 35 | 35 | 30 | 30 | ns |
| ${ }^{\text {P PLH }}$ | Select to output delay $\dagger$ (data input High) |  | 40 | 40 | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 25 | 30 | 25 | 28 | ns |
| ${ }^{\text {t PLH }}$ | Select to output delay $\dagger$ (data input Low) |  | 40 | 40 | 35 | 35 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 35 | 25 | 30 | 22 | ns |
| ${ }^{\text {t PRL }}$ | $\overline{G B A}$ to <br> A bus output enable delay |  | 30 | 30 | 25 | 25 | ns |
| ${ }^{\text {tPZH }}$ |  |  | 25 | 25 | 20 | 20 | ns |
| $t_{\text {PLZ }}$ | $\overline{\mathrm{GBA}} \text { to }$ <br> A bus output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 35 | 30 | 30 | 28 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | 40 | 45 | 40 | 40 | ns |
| ${ }_{\text {t }}^{\text {PZL }}$ | GAB to <br> B bus output enable delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 35 | 35 | 30 | 32 | ns |
| $t_{\text {PZH }}$ |  |  | 30 | 30 | 25 | 25 | ns |
| $t_{\text {PLZ }}$ | GAB to <br> B bus output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 35 | 35 | 30 | 30 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | 40 | 45 | 35 | 40 | ns |

[^67]
## Absolute Maximum Ratings


Input voltage .............................................................................................................. . . 1.5 V to 7 V



## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  | MIN | TYP | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of clock | High | 20 |  |  | 20 |  |  | ns |
|  |  | Low | 20 |  |  | 20 |  |  |  |
|  | Setup time | 'LS653 | $20 \uparrow$ |  |  | $20 \uparrow$ |  |  | ns |
| ${ }_{\text {su }}$ |  | 'LS654 | $20 \uparrow$ |  |  | $20 \uparrow$ |  |  |  |
| $t^{\prime}$ | Hold time | 'LS653 | 01 |  |  | $0 \dagger$ |  |  | ns |
|  |  | 'LS654 | 01 |  |  | 01 |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage (A bus only) |  |  |  | 5.5 |  |  | 5.5 | V |
| ${ }^{\mathrm{I}} \mathrm{OH}$ | High-level output current (B bus only) |  |  |  | -12 |  |  | -15 | mA |
| $\mathrm{I}_{\mathrm{OL}}$ | Low-level output current |  |  |  | 12 |  |  | 24 | mA |

$\dagger \downarrow$ The arrow indicates the transition of the clock input used for reference. $\dagger$ tor the low-to-high transitions, $\downarrow$ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  |  | MIN | LITARY <br> TYP MAX |  | MERCIAL <br> TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  |  | 0.7 |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  |  |  | 2 |  | 2 |  | V |
| $\mathrm{V}_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{C C}=\mathrm{MIN}$ |  | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -1.5 |  | -1.5 | V |
| IIL | Low-level input current |  | $V_{C C}=$ MAX |  | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -0.4 |  | -0.4 | mA |
| IIH | High-level input current |  | $V_{C C}=$ MAX |  | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | A or B | $v_{C C}=$ MAX |  | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ | 0.1 |  | 0.1 |  | mA |
|  |  | All others |  |  | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & v_{C C C}=\text { MIN } \\ & v_{1 L}=M A X \\ & v_{1 H}=2 \mathrm{~V} \\ & \hline \end{aligned}$ |  | $\mathrm{I}^{\mathrm{O}} \mathrm{OL}=12 \mathrm{~mA}$ |  | $0.25 \quad 0.4$ |  | 0.250 .4 | v |
|  |  |  | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  |  | $\begin{array}{lll}0.35 & 0.5\end{array}$ |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage (B bus only) |  |  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{MIN} \\ & \mathrm{v}_{\mathrm{IL}}=M A X \\ & \mathrm{~V}_{\mathrm{IH}}=2 \mathrm{~V} \\ & \hline \end{aligned}$ |  | $\mathrm{IOH}^{\prime}=-3 \mathrm{~mA}$ | 2.4 | 3.4 | 2.4 | 3.4 | v |
|  |  |  | $\mathrm{IOH}=\mathrm{MAX}$ | 2 |  |  |  | 2 |  |  |  |
| ${ }^{1} \mathrm{OH}$ | High-level output current (A bus only) |  | $\begin{aligned} & v_{C C}=M I N \\ & v_{I L}=M A X \\ & v_{I H}=2 V \end{aligned}$ |  | $\mathrm{V}_{\mathrm{OH}}=5.5 \mathrm{~V}$ |  | 100 |  | 100 | $\mu \mathrm{A}$ |  |
| 'OzL | Off-state output current (B bus only) |  | $\begin{aligned} & v_{C C}=M A X \\ & v_{I L}=M A X \\ & v_{I H}=2 v \end{aligned}$ |  | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -400 |  | -400 | $\mu \mathrm{A}$ |  |
| IOZH |  |  | $\begin{gathered} \hline V_{\mathrm{O}}=2.7 \mathrm{~V} \\ \text { (B bus only) } \end{gathered}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |  |  |
| Ios | Output short-circuit current* (B bus only) |  |  |  | $V_{C C}=M A X$ |  |  | -40 | -225 | -40 | -225 | mA |
| ${ }^{\text {I Co }}$ | Supply current |  | $\begin{aligned} & \mathrm{v}_{\mathrm{CC}}= \\ & \text { AAX } \end{aligned}$ | 'LS- | Outputs High |  | 145 |  | 145 | mA |  |
|  |  |  | Outputs Low |  |  | 165 |  | 165 |  |  |
|  |  |  | Outputs disabled |  |  | 165 |  | 165 |  |  |
|  |  |  | $\begin{aligned} & \text { 'LS- } \\ & 654 \end{aligned}$ | Outputs High |  | 145 |  | 145 |  |  |
|  |  |  | Outputs Low |  | 165 |  | 165 |  |  |  |  |
|  |  |  | Outputs disabled |  | 165 |  | 165 |  |  |  |  |

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.


## Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=\mathbf{2 5 ^ { \circ }} \mathbf{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS* <br> (See Test Load/Waveforms) | $\text { MIN }{ }^{\text {'LS653 }} \text { MAX }$ | $\text { MIN }{ }^{\text {'LS654 }} \text { MAX }$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {t PLH }}$ | Data to A bus output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 25 | 25 | ns |
| ${ }^{\text {tPHL }}$ |  |  | 20 | 25 | ns |
| ${ }^{\text {tPLH }}$ | Data to B bus output delay |  | 15 | 15 | ns |
| ${ }^{\text {P PHL }}$ |  |  | 15 | 20 | ns |
| ${ }^{\text {tPLH }}$ | Clock to A bus output delay |  | 30 | 30 | ns |
| ${ }_{\text {tPHL }}$ |  |  | 30 | 30 | ns |
| ${ }^{\text {tPLH }}$ | Clock to B bus output delay |  | 20 | 20 | ns |
| ${ }^{\text {t PHL }}$ |  |  | 30 | 30 | ns |
| ${ }^{\text {tPLH }}$ | Select to A bus $\dagger$ output delay (data input High) |  | 45 | 45 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 25 | 30 | ns |
| ${ }^{\text {tPLH }}$ | Select to A bus $\dagger$ output delay (data input Low) |  | 40 | 45 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 30 | 25 | ns |
| ${ }^{\text {PPLH }}$ | Select to B bus $\dagger$ output delay (data input High) |  | 35 | 35 | ns |
| ${ }^{\text {t PHL }}$ |  |  | 25 | 25 | ns |
| ${ }^{\text {PPLH }}$ | Select to B bus $\dagger$ output delay (data input Low) |  | 35 | 35 | ns |
| ${ }_{\text {t }}^{\text {PHL }}$ |  |  | 30 | 20 | ns |
| $t_{\text {PLH }}$ | $\overline{\mathrm{GBA}}$ to <br> A bus output enable delay |  | 35 | 35 | ns |
| ${ }^{\text {tPHL }}$ |  |  | 25 | 30 | ns |
| ${ }^{\text {tPZL }}$ | GAB to <br> $B$ bus output enable delay |  | 30 | 30 | ns |
| ${ }^{\text {t }} \mathrm{PZH}$ |  |  | 25 | 25 | ns |
| $t_{\text {PLZ }}$ | GAB to <br> B bus output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 25 | 25 | ns |
| ${ }^{\text {t PHZ }}$ |  |  | 35 | 35 | ns |

[^68]
## Switching Characteristics over Operating Range

| SYMBOL | PARAMETER | TEST CONDITIONS* <br> (See Test Load/Waveforms) | MIL |  | COM |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | $\begin{array}{\|c\|} \hline \text { 'LS653 } \\ \text { MIN MAX } \end{array}$ | $$ | $\begin{array}{\|c\|} \hline \text { 'LS } 653 \\ \text { MIN MAX } \end{array}$ | $$ |  |
| ${ }^{\text {t PLH }}$ | Data to A bus output delay | $C_{L}=45 p F \quad R_{L}=667 \Omega$ | 30 | 30 | 28 | 30 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 25 | 30 | 23 | 28 | ns |
| ${ }^{\text {t PLH }}$ | Data to B bus output delay |  | 20 | 20 | 18 | 18 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 20 | 25 | 18 | 20 | ns |
| ${ }^{\text {tPLH }}$ | Clock to A bus output delay |  | 40 | 40 | 35 | 35 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 40 | 40 | 35 | 35 | ns |
| ${ }^{\text {t PLH }}$ | Clock to B bus output delay |  | 25 | 25 | 23 | 23 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 35 | 35 | 30 | 30 | ns |
| ${ }_{\text {t }}$ | Select to A bus output $\dagger$ delay (data input High) |  | 50 | 50 | 45 | 48 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 30 | 40 | 25 | 35 | ns |
| ${ }^{\text {t }}$ PLH | Select to A bus output $\dagger$ delay (data input Low) |  | 45 | 55 | 43 | 50 | ns |
| ${ }^{\text {t PHL }}$ |  |  | 35 | 30 | 30 | 28 | ns |
| ${ }^{\text {P PLH }}$ | Select to B bus output $\dagger$ delay (data input High) |  | 40 | 35 | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 25 | 35 | 25 | 30 | ns |
| ${ }^{\text {t PLH }}$ | Select to B bus output $\dagger$ delay (data input Low) |  | 40 | 45 | 35 | 40 | ns |
| ${ }^{\text {t }}$ PHL |  |  | 35 | 25 | 30 | 23 | ns |
| ${ }^{\text {t PLH }}$ | $\overline{\mathrm{GBA}}$ to <br> A bus output enable delay |  | 40 | 35 | 35 | 35 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 30 | 40 | 28 | 35 | ns |
| ${ }^{\text {t P Z }}$ | GAB to <br> B bus output enable delay |  | 35 | 35 | 30 | 33 | ns |
| ${ }^{\text {tPZH }}$ |  |  | 30 | 30 | 25 | 28 | ns |
| ${ }^{\text {t PLZ }}$ | GAB to <br> B bus output disable delay | $C_{L}=5 p F \quad R_{L}=667 \Omega$ | 35 | 35 | 30 | 30 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | 40 | 45 | 38 | 40 | ns |

* For A bus, the test load will refer to the open-collector test load. See Figure 6.

For $B$ bus, the test load will refer to the three-state test load. See Figure 7.
$\dagger$ See Figure 4.

Test Waveforms


CK To Bus Output Propagation Delay Time


Figure 4
NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

## Enable/Disable Delay



Figure 5

## Test Loads



Load Circuit For Open-Collector Outputs


## Load Circuit For

 Three-State Outputs* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: $A . C_{L}$ includes probe and jig capacitance.
B. All diodes are 1 N916 or 1 N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz} . \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and $\mathrm{t}_{\mathrm{R}}=15 \mathrm{~ns} \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

# 8-Bit Two-Stage Pipelined Register/Latch SN54/74LS548 SN54/74LS549 

## Feature/Benefits

- Two 8-bit high-speed registers/latches
- Faster than other LS-TTL registers/latches
- Three-state outputs drive bus lines
- 24-pin SKINNYDIP® ${ }^{\circledR}$ saves space
- 8-bit data path matches byte boundaries
- Multiplexer selects either rank at input/output
- Output can drive bus directly: IOL 32 mA (com), 24 mA (mil)
- Registers/latches configurable for nose-to-tail or side-byside operation
- Individual clock/gate enables for each rank


## Applications

- Registers for pipelined arithmetic units or digital signal processors
- Bus monitor for popular 8-bit microprocessors to restart instructions upon virtual memory page fault
- Video display character/attribute pipelined registers
- Sequence/state generator for systems: dual-rank registers/ latches allow storing a backup previous state for redundancy, or diagnostics
- Two-stage buffer for pipelined interfacing input/output


## Description

The 54/74LS548 and 54/74LS549 contain a pair of high-speed 8 -bit registers ('LS548) or latches ('LS549) which perform various pipeline storage functions. Two control pins govern a pair of internal multiplexers, as shown in the block diagrams; using these, several useful data paths can be configured. The input selection multiplexer determines the source of data to the second register/latch, as controlled by the INSEL line. In this way, data from either the D7-D0 inputs, or the outputs of the first register/ latch, are stored in the second register/latch. The output selection multiplexer determines the source of data that will be sent to
the outputs $\mathrm{Y} 7-\mathrm{YO}$. This multiplexer is controlled by the OUTSEL line, and allows either the first or second register/latch data to be output. The outputs are fully buffered, provide high-drive current, and allow three-state control through the $\overline{\mathrm{OE}}$ line.

## Ordering Information

| PART <br> NUMBER | PKG | TEMP | TYPE | POWER |
| :---: | :---: | :---: | :---: | :---: |
| SN54LS548 | JS,W,L(28) | Mil | Register | LS |
| SN74LS548 | NS,JS,NL(28) | Com | Register | LS |
| SN54LS549 | JS,W,L(28) | Mil | Latch | LS |
| SN74LS549 | NS,JS,NL(28) | Com | Latch | LS |

The arrangement of registers/latches within the 'LS548/'LS549 can be thought of a two 8-bit storage ranks, rank 1 and rank 2. The 'LS548 has a common clock line CK, and separate clock enables $\overline{\mathrm{CKE}}$ and $\overline{\mathrm{CKE} 2}$ for rank 1 and rank 2 respectively. In contrast, the 'LS549 operates as a flow-through latch, and has separate latch enables $\overline{\mathrm{G} 1}$ and $\overline{\mathrm{G} 2}$ for each rank, as well as a common latch-enable input $G$.
In the 'LS548, data present at the D7-D0 inputs are stored in rank 1 on the positive edge of CK, if CKE1 has been previously asserted. Data for rank 2 are stored similarly, if $\overline{\mathrm{CKE} 2}$ is asserted prior to the clock. In the 'LS549, data pass through the latches when the latch controls ( $\overline{\mathrm{G} 1}$ or $\overline{\mathrm{G} 2}$ ) for either rank are enabled simultaneously with the common latch enable $G$. Data remain in a rank when the latch controls are disabled, or 'unasserted'.
The clock/gate control lines are used with the INSEL and OUTSEL controls for flexible data storage and movement operations. Two representative examples are shown in Figure 1 (a) and 1 (b). The first example is a classical 2 -stage pipelined register, or 'nose-to-tail' configuration. Data at D7-D0 are first stored in rank 1, then stored in rank 2 on the next clock/gate. If the clock/gate enable for either rank becomes unasserted, then the previouslystored data are simply retained. In the second example, data at D7-D0 are stored in either or both ranks if the respective clock/gate enable signals are asserted. In this 'side-by-side' configuration, data sent to the Y7-Y0 outputs are selected from either rank 1 or rank 2, under control of the OUTSEL line.

## Pin Configurations



## Block Diagrams




Figure 1


## Function Table Nomenclature Description

Rank 1-Q or Rank 2-Q = Data available at the internal flipflop/latch outputs for the 8 rank 1 or rank 2 registers/latches respectively.
$D=$ Data at the DO-D7 input pins.
$Y=$ Data at the $\mathrm{Y} 0-\mathrm{Y} 7$ output pins.
$X=H$ or L state irrelevant ("don't care" conditions)
$Q_{0}=$ Previous states of the internal register/latch data are retained.
$Z=$ Indicates that the $Y 0-Y 7$ outputs are in high-impedance state.
INSEL = Input select mux control pin; determines the source of input data for rank 2.

| INSEL | RANK 2 INPUT |
| :---: | :---: |
| L | Rank 1 |
| $H$ | D |

OUTSEL = Output select mux control pin; selects either rank 1 or rank 2 for output.

| OUTSEL | OUTPUT |
| :---: | :---: |
| L | Rank 2 |
| $H$ | Rank 1 |

$\overline{\mathbf{O E}}=$ Output enable pin.

| $\overline{O E}$ | OUTPUT |
| :---: | :---: |
| $L$ | Rank 1 or Rank 2 |
| $H$ | $\mathrm{Hi}-\mathrm{Z}$ |

$\dagger$ = Positive edge of CK causes clocking, if clocking is enabled.
$\mathbf{C K}=$ The common clock line for the 54/74LS548.
$\overline{\mathrm{CKE} 1} / \overline{\mathrm{CKE} 2}=$ Clock enable line for the rank 1/ rank 2 register in the 54/74LS548.

| CK | $\overline{\text { CKE1 }}$ | $\overline{\text { CKE2 }}$ | RANK 1 | RANK 2 |
| :---: | :---: | :---: | :--- | :--- |
| L or H or $\downarrow$ | X | X | Disabled | Disabled |
| 1 | L | L | Enabled | Enabled |
| 1 | L | H | Enabled | Disabled |
| $\uparrow$ | H | L | Disabled | Enabled |
| X | H | H | Disabled | Disabled |

$\mathbf{G}=$ The common latch control line for the 54/74LS549.
$\overline{\mathbf{G 1}} / \overline{\mathbf{G 2}}=$ Latch enable line for the rank 1/ rank 2 latch in the 54/74LS549.

| G | $\overline{\text { G1 }}$ | $\overline{\text { G2 }}$ | RANK 1 | RANK 2 |
| :---: | :---: | :---: | :---: | :---: |
| L | L | L | Enabled <br> (Flush) | Enabled <br> (Flush) |
| L | L | H | Enabled <br> (Flush) | Disabled <br> (Freeze) |
| L | H | L | Disabled <br> (Freeze) | Enabled <br> (Flush) |
| L | H | H | Disabled <br> (Freeze) | Disabled <br> (Freeze) |
| H | X | X | Enabled <br> (Flush) | Enabled <br> (Flush) |

## 'LS548 Function Table

| CK | CKE1 | RANK 1 | $\overline{\text { CKE2 }}$ | INSEL | RANK 2 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L or H <br> or | X | Q0 | X | X | Q0 |
| i | H | Q0 | H | X | Q0 |
| i | L | D | H | X | Q0 |
| i | L | D | L | L | Rank 1-Q |
| I | L | D | L | H | D |
| † | H | Q0 | L | L | Rank 1-Q |
| i | H | Q0 | L | H | D |

'LS549 Function Table

| G | $\overline{\text { G1 }}$ | RANK 1 | $\overline{\text { G2 }}$ | INSEL | RANK 2 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| L | L | D | L | L | Rank 1-Q |
| L | L | D | L | H | D |
| L | L | D | H | X | Q0 |
| L | $H$ | Q0 | L | L | Rank 1-Q |
| L | $H$ | Q0 | L | $H$ | D |
| L | $H$ | Q0 | H | X | Q0 |
| $H$ | X | D | X | L | Rank 1-Q |
| $H$ | X | D | X | H | D |

'LS548/549 Output Function Table

| OUTSEL | $\overline{\mathbf{O E}}$ | $\mathbf{Y}$ |
| :---: | :---: | :---: |
| L | L | Rank 2-Q |
| H | L | Rank 1-Q |
| X | H | Hi-Z |

## Logic Diagram



Logic Diagram


## Pin Configurations



## IEEE Symbols



## Absolute Maximum Ratings


Input voltage ........................................................................................................... -1.5 V to 7 V



Operating Conditions

| SYMBOL | PARAMETER |  |  |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  | MIN | TYP | MAX | MIN |  | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  |  |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {tw }}$ | Width of CK, G, $\overline{\mathrm{G} 1}, \overline{\mathrm{G} 2}$ | High | 'LS548 | CK | 15 |  |  | 11 |  |  | ns |
|  |  |  | 'LS549 | G |  |  |  |  |  |  |  |
|  |  | Low | 'LS548 | CK | 15 |  |  | 11 |  |  | ns |
|  |  |  | 'LS548 | $\overline{\mathrm{G} 1}, \overline{\mathrm{G} 2}$ | 18 |  |  | 16 |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time for Data |  | 'LS548 | CK | 201 |  |  | 151 |  |  | ns |
|  |  |  | 'LS549 | G | 10. |  |  | 61 |  |  |  |
|  |  |  | $\overline{\mathrm{G} 1}, \overline{\mathrm{G} 2}$ | 171 |  |  | 41 |  |  |  |
| $t_{h}$ | Hold time for Data |  |  | 'LS548 | CK | 01 |  |  | 01 |  |  | ns |
|  |  |  | 'LS549 | G | 121 |  |  | 101 |  |  |  |  |
|  |  |  | $\overline{\mathrm{G} 1}, \overline{\mathrm{G} 2}$ | 51 |  |  | 5 |  |  |  |  |
| tsu-CKEX | Setup time for clock enables $\overline{\text { CKE1 }}$, $\overline{\mathrm{CKE2}}$ ('LS548 only) |  |  |  | 151 |  |  | $10 \%$ |  |  | ns |  |
| $t_{\text {h-CKEX }}$ | Hold time for clock enable $\overline{\mathrm{CKE1}}$, $\overline{\mathrm{CKE} 2}$, ('LS548 only) |  |  |  | 81 |  |  | 51 |  |  | ns |  |
| $\mathrm{t}_{\text {su-INSEL }}$ | Setup time for INSEL ${ }^{1}$ |  |  |  | 30 |  |  | 25 |  |  | ns |  |
| $t^{\text {h-INSEL }}$ | Hold time for INSEL ${ }^{2}$ |  |  |  | 0 |  |  | 0 |  |  | ns |  |

NOTES: 1. This is the minimum setup time needed for INSEL prior to the rising edge of the clock/ $\overline{\mathrm{GX}}$, and to the falling edge of the G , to ensure data transfer to rank 2.
2. This is the minimum hold time needed for INSEL after the rising edge of the clock/ $\overline{G X}$, and to the falling edge of the $G$, to ensure data transfer to rank 2 .
if the arrow indicates the transition of the clock/gate input used for reference:
$t$ for the low-to-high transitions,
$\downarrow$ for the high-to-low transitions.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | $\underset{\operatorname{MIN}}{\text { MI }}$ | Y MAX |  | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 |  | 0.8 | V |
| $V_{\text {IH }}$ | High-level input voltage |  |  |  | 2.0 |  | 2.0 |  | V |
| $\mathrm{V}_{1 \mathrm{C}}$ | Input clamp voltage |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -1.5 |  | -1.5 | V |
| IIL | Low-level input current |  | $\begin{aligned} V_{C C} & =M A X \\ V_{1} & =0.4 \mathrm{~V} \end{aligned}$ | D or Y |  | -250 |  | -250 | $\mu \mathrm{A}$ |
|  |  |  | All others |  | -400 |  | -400 |  |
| $\mathrm{IIH}^{\text {H }}$ | High-level input current |  |  | $V_{C C}=$ MAX | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  | 20 |  | 20 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | D or Y | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ | 0.1 |  | 0.1 |  | mA |
|  |  | All others |  | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{IOL}=32 \mathrm{~mA}$ |  |  |  | 0.5 | V |
|  |  |  | $\mathrm{I}^{\mathrm{OL}}=24 \mathrm{~mA}$ |  | 0.5 |  |  |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \\ & \hline \end{aligned}$ | ${ }^{1} \mathrm{OH}=-1 \mathrm{~mA}$ |  |  |  |  | V |
|  |  |  | $\mathrm{I}^{\mathrm{OH}}=-2.6 \mathrm{~mA}$ |  |  |  | 2.4 |  |  |  |
| 'OZL | Off-State output current |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -20 |  | -20 | $\mu \mathrm{A}$ |  |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  | 20 |  | 20 |  |  |
| 'os | Output short-circuit current* |  |  | $V_{C C}=M A X$ |  | -30 | -130 | -30 | -130 | mA |
| ${ }^{1} \mathrm{CC}$ | Supply Current |  | $V_{C C}=M A X$ <br> Outputs open | 'LS548 |  | 150 |  | 150 | mA |  |
|  |  |  | 'LS549 |  | 160 |  | 160 |  |  |

[^69]
## Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=\mathbf{5 V} \mathrm{V}_{\mathrm{A}}=\mathbf{2 5}{ }^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | $\operatorname{MIN} \quad \text { MAX }$ | $\text { MIN }{ }^{\text {'LS549 }} \text { MAX }$ | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency | $\begin{gathered} \mathrm{C}_{\mathrm{L}}=45 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega \\ \overline{\mathrm{OE}=\mathrm{L}} \end{gathered}$ | 50 |  | MHz |
| ${ }^{\text {t }}{ }^{\text {PLH }} /{ }^{\text {/ }}$ PHL | CK, $\overline{\mathrm{G1}}$, or $\overline{\mathrm{G} 2}$ to output delay |  | 18 | 22 | ns |
| ${ }^{\text {P PLH }} /{ }^{\text {/ }} \mathrm{PHL}$ | G to output delay ('LS549) |  |  | 23 | ns |
| ${ }^{\text {P }}{ }_{\text {LH }} /{ }^{\text {/ }} \mathrm{PHL}$ | Data D to output delay ('LS549) |  |  | 16 | ns |
|  | Output multiplexer control OUTSEL to output delay |  | 20 | 20 | ns |
| ${ }^{\mathrm{P}_{\mathrm{PLL}} /{ }^{\text {P }} \mathrm{PZH}}$ | Output enable delay | $C_{L}=45 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 18 | 18 | ns |
| ${ }^{{ }^{\text {PLZ }} /{ }^{\prime}{ }^{\text {PHHZ }} \text { }}$ | Output disable delay | $C_{L}=5 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 15 | 15 | ns |

## Switching Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIL |  |  |  | COM |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | 'LS548 |  | 'LS549 |  | 'LS548 |  | 'LS549 |  |  |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $\mathrm{f}_{\text {MAX }}$ | Maximum clock frequency |  | 33 |  |  |  | 45 |  |  |  | MHz |
| ${ }^{\text {t }}$ PLH $/{ }^{\text {P }}$ PHL | CK, $\overline{\mathrm{G} 1}$ or $\overline{\mathrm{G} 2}$ to output delay | $\begin{gathered} C_{L}=45 \mathrm{pF} \\ R_{\mathrm{L}}=280 \Omega \\ \overline{\mathrm{OE}}=\mathrm{L} \end{gathered}$ | 25 |  | 26 |  | 20 |  | 24 |  | ns |
| ${ }^{\mathrm{PLLH}^{\prime}} \mathrm{t}_{\mathrm{PHL}}$ | G to output delay ('LS549) |  |  |  |  | 28 |  |  |  | 25 | ns |
| ${ }^{\text {t }}{ }^{\text {LH }} /{ }^{\text {t }} \mathrm{PHL}$ | Data D to output delay ('LS549) |  |  |  |  | 24 |  |  |  | 18 | ns |
| ${ }^{\text {t }}{ }^{\text {LH }} /{ }^{\text {t }} \mathrm{PHL}$ | Output multiplexer control OUTSEL to output delay |  |  | 27 |  | 27 |  | 22 |  | 22 | ns |
| ${ }^{\text {t }}$ PZL $/{ }^{\text {P }} \mathrm{PZH}$ | Output enable delay | $\begin{aligned} & C_{\mathrm{L}}=45 \mathrm{pF} \\ & \mathrm{R}_{\mathrm{L}}=280 \Omega \\ & \hline \end{aligned}$ |  | 23 |  | 23 |  | 20 |  | 20 | ns |
| ${ }^{\text {t }}$ PLZ $/{ }^{\text {/ }} \mathrm{PHZ}$ | Output disable delay | $\begin{aligned} & C_{L}=5 \mathrm{pF} \\ & R_{L}=280 \Omega \end{aligned}$ |  | 20 |  | 20 |  | 17 |  | 17 | ns |



## Standard Test Load



Load Circuit for Three-state Outputs

$V_{\mathbf{T}}=1.3 \mathrm{~V}$

## 'LS548/549 Enable and Disable

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Notes: $A . C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $P R R \leq 1 \mathrm{MHz} . \mathrm{Z}_{\mathrm{OUT}}=50 \Omega$ and $\mathrm{t}_{\mathrm{R}}=15 \mathrm{~ns} \mathrm{t}_{\mathrm{F}} \leq 6 \mathrm{~ns}$.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

## 8-Bit Latch/Register with Readback SN54/74LS793 SN54/74LS794

## Features/Benefits

- I/O port configuration enables output data back onto input bus
- 8-bit data path matches byte boundaries
- Ideal for microprocessor interface


## Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an 'LS793/4, for verification and/or updating.


The data is loaded in the registers on the low-to-high transition of the clock (CK), for the 'LS794. The data is passed through the 'LS793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{\mathrm{OE}}$ is used to enable data on D7-DO. When $\overline{\mathrm{OE}}$ is low the output of the latches/registers is enabled on D0-D7, enabling D as an output bus so that the host can perform a read operation. When $\overline{\mathrm{OE}}$ is High, D7-D0 are inputs to the latches/registers configuring $D$ as an input bus.
The output drive of these commercial parts for any output pin is $I_{\mathrm{OL}}=24 \mathrm{~mA}$.

## 'LS793 Function Table

| $\mathbf{G}$ | $\overline{\mathbf{O E}}$ | $\mathbf{Q}$ | $\mathbf{D}$ |
| :---: | :---: | :---: | :--- |
| $\mathbf{L}$ | L | $\mathrm{Q}_{0}{ }^{* *}$ | Output, $\mathbf{Q}$ |
| L | H | $\mathrm{Q}_{0^{* *}}$ | Input |
| $\mathrm{H}^{\dagger}$ | L | $\mathbf{D}^{*}$ | Output, $\mathrm{Q}^{*}$ |
| $H$ | $H$ | $D$ | Input |

[^70]
## Ordering Information

| PART NUMBER | PKG | TEMP | POLARITY | TYPE | POWER |
| :---: | :---: | :---: | :---: | :---: | :---: |
| SN54LS793 <br> SN74LS793 | $J, W, L,$ <br> N,J,NL | Mil Com | Noninvert | Latch | LS |
| SN54LS794 SN74LS794 | $\begin{aligned} & \mathrm{J}, \mathrm{~W}, \mathrm{~L}, \\ & \mathrm{~N}, \mathrm{~J}, \mathrm{NL} \end{aligned}$ | $\begin{gathered} \text { Mil } \\ \text { Com } \end{gathered}$ |  | Register |  |

## Logic Symbols



## 'LS794 Function Table

| CK | $\overline{O E}$ | Q | D |
| :---: | :---: | :---: | :---: |
| Lor Hor! Lor Hor $\downarrow$ $\dagger$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \\ & \mathrm{~L} \\ & \mathrm{H} \end{aligned}$ | $\begin{gathered} Q_{0} \\ Q_{0} \\ Q_{0} \\ D \end{gathered}$ | Output, Q Input Output, Q* Input |

[^71]
## Pin Configurations



## IEEE Symbols



## Absolute Maximum Ratings



## Operating Conditions

|  | PARAMETER |  |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SYMBOL |  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  |  | 4.5 | 5 | 5.5 | 4.75 | 5. | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of Clock/Gate | High |  | 15 |  |  | 15 |  |  | ns |
|  |  | Low ('LS794 only) |  | 15 |  |  | 15 |  |  |  |
| ${ }^{\text {s }}$ su | Setup time |  | 'LS793 | $15 \downarrow$ |  |  | 101 |  |  | ns |
|  |  |  | 'LS794 | 151 |  |  | $15 \dagger$ |  |  |  |
| $t_{h}$ | Hold time |  | 'LS793 | 10. |  |  | 101 |  |  |  |
|  |  |  | 'LS794 | 01 |  |  | $0 \uparrow$ |  |  |  |

$\dagger \downarrow$ The arrow indicates the transition of the clock/gate input used for reference. $\uparrow$ for the low-to-high transitions, $\downarrow$ for the high-to-low transitions.

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER |  | TEST CONDITIONS |  | $\underset{\text { MIN }}{\mathbf{M I}}$ | LITARY <br> TYP MAX |  | MERCIAL TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.7 |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  |  |  | 2 |  | 2 |  | V |
| $V_{\text {IC }}$ | Input clamp voltage |  | $\mathrm{V}_{\text {CC }}=\mathrm{MIN}$ | $\mathrm{I}_{1}=-18 \mathrm{~mA}$ |  | -1.5 |  | -1.5 | V |
| IIL | Low-level input current |  | $V_{C C}=M A X$ | $\mathrm{V}_{1}=0.4 \mathrm{~V}$ |  | -250 |  | -250 | $\mu \mathrm{A}$ |
| ${ }_{1} \mathrm{H}$ | High-level input current |  | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=2.7 \mathrm{~V}$ |  | 40 |  | 40 | $\mu \mathrm{A}$ |
| 1 | Maximum input current | D or Q | $V_{C C}=M A X$ | $\mathrm{V}_{1}=5.5 \mathrm{~V}$ | 0.1 |  | 0.1 |  | mA |
|  |  | All others |  | $\mathrm{V}_{1}=7 \mathrm{~V}$ |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}$ |  | $0.25 \quad 0.4$ |  | $0.25 \quad 0.4$ | V |
|  |  |  | $\mathrm{I}^{\mathrm{OL}}=24 \mathrm{~mA}$ |  |  |  | $0.35 \quad 0.5$ |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage |  |  | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=2 V \end{aligned}$ | $\mathrm{I}^{\mathrm{OH}}=-1 \mathrm{~mA}$ | 2.4 | 3.4 |  |  | V |
|  |  |  | $\mathrm{I}^{\mathrm{OH}}=-2.6 \mathrm{~mA}$ |  |  |  | 2.4 | 3.1 |  |  |
| IOZL | Off-state output current |  | $\begin{aligned} & V_{C C}=M A X \\ & V_{I L}=M A X \\ & V_{\mathrm{IH}}==2 V \end{aligned}$ | $\mathrm{V}_{\mathrm{O}}=0.4 \mathrm{~V}$ |  | -250 |  | -250 | $\mu \mathrm{A}$ |  |
| ${ }^{1} \mathrm{OZH}$ |  |  | $\mathrm{V}_{\mathrm{O}}=2.7 \mathrm{~V}$ |  | 40 |  | 40 |  |  |
| IOS | Output short-circuit current ${ }^{*}$ |  |  | $V_{C C}=M A X$ |  | -30 | -130 | -30 | -130 | mA |
| ${ }^{1} \mathrm{Cc}$ | Supply current |  | $V_{C C}=M A X$ Outputs open | 'LS793 |  | 120 |  | 120 | mA |  |
|  |  |  | 'LS794 |  | 120 |  | 120 |  |  |

- Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $\mathrm{V}_{\mathrm{CC}}=\mathbf{5 V}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Interface Test Load/Waveforms) | 'LS793 |  |  | 'LS794 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| ${ }^{\text {f MAX }}$ | Maximum clock frequency | $C_{L}=45 p F \quad R_{L}=280 \Omega$ |  |  |  | 35 | 50 |  | MHz |
| ${ }^{\text {P PLH }}$ | Data to output delay |  |  | 12 | 18 |  |  |  | ns |
| ${ }^{\text {t PHL }}$ |  |  |  | 12 | 18 |  |  |  | ns |
| ${ }^{\text {P PLH }}$ | Clock/gate to output delay |  |  | 17. | 25 |  | 9 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  |  | 12 | 25 |  | 14 | 20 | ns |
| ${ }^{\text {tPZL }}$ | Output enable delay ${ }^{\dagger}$ |  |  | 15 | 20 |  | 15 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PZH}$ |  |  |  | 11 | 20 |  | 11 | 20 | ns |
| ${ }^{\text {t PLZ }}$ | Output disable delay ${ }^{\dagger}$ | $C_{L}=5 p F R_{L}=280 \Omega$ |  | 8 | 20 |  | 8 | 20 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  |  | 9 | 20 |  | 9 | 20 | ns |

+ For the 'LS793, G should remain LOW during these tests.


## 'LS793 Timing Diagrams



## 'LS794 Timing Diagrams



The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. $\left(\mathrm{V}_{\mathrm{T}}=1.3 \mathrm{~V}\right)$.

Test Loads
FOR D OUTPUTS-ENABLE AND DISABLE TEST POINT FOR Di*


FOR Q OUTPUTS
TEST POINT FOR Qi*


[^72] and observed by instrumentation.

PULSE WIDTH


ENABLE AND DISABLE WAVEFORMS


For the 'LS793, the latch control "G" should be low while testing the enable and disable times, so that the output ( $Q$ ) does not change. $\left(V_{\mathbf{T}}=1.3 \mathrm{~V}\right)$.
NOTES: A. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

## Features/Benefits

- High drive capability. IOL = 32 mA (Com)
- Alternate source to Am29818
- Serial-parallel/Parallel-serial pipeline register
- Independent pathing and clocking controls
- Expandable in multiples of 8 bits
- Three-state outputs
- PNP inputs for low-inputcurrent
- 24-pin SKINNYDIP® saves space


## Applications

- Universal interface element for systems using both serial and parallel data formats
- Serial communication and peripheral interface
- Microprogram control store output register
- Serial-parallel/Parallel-serial pipeline conversion
- State machine feedback path isolation/diagnostics
- Serial readback register


## Description

The SN54/74S818 is an 8-bit serializing/deserializing pipeline register. It can also be used as a serial readback register as well as a diagnostic register. All of these configurations are expandable in multiples of eight bits.
The 54/74S818 internally consists of a universal shift register and an 8-bit register. Its wide application results from a combination of powerful interconnection modes and independent clocking and pathing controls. It is ideally suited as a universal interface element involving both serial and parallel data formats.

## Function Table

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| SN74S818 | NS, JS, NL (28) | Com |
| SN54S818 | JS, W, L (28) | Mil |



## Logic Diagram



## Pin Configuration

SN74S818


## Typical Configurations



Serializing Pipeline Register


Serial Readback Register


Deserializing Pipeline Register


Diagnostic Register

## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | MILITARY |  |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX | MIN | TYP | MAX |  |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free air temperature |  | -55 |  | 125 | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of CLK | High | 15 |  |  | 12 |  |  | ns |
|  |  | Low | 15 |  |  | 13 |  |  | ns |
| ${ }^{\text {twd }}$ | Width of DCLK | High | 25 |  |  | 20 |  |  | ns |
|  |  | Low | 25 |  |  | 20 |  |  | ns |
| $\mathrm{t}_{\text {suc }}$ | Setup time from MODE to CLK |  | 201 |  |  | 171 |  |  | ns |
| the | Hold time from CLK to MODE |  | 01 |  |  | 01 |  |  | ns |
| $\mathrm{t}_{\text {sud }}$ | Setup time from data to CLK |  | 211 |  |  | 141 |  |  | ns |
| thd | Hold time from CLK to data |  | 01 |  |  | 01 |  |  | ns |
| $\mathrm{t}_{\text {sudc }}$ | Setup time from SDI, MODE to DCLK |  | 311 |  |  | 201 |  |  | ns |
| thde | Hold time from DCLK to SDI, MODE |  | 01 |  |  | 01 |  |  | ns |
| $\mathrm{t}_{\text {sudq }}$ | Setup time from output to DCLK |  | 251 |  |  | 181 |  |  | ns |
| $\mathrm{t}_{\mathrm{hdq}}$ | Hold time from DLCK to output |  | 01 |  |  | 01 |  |  | ns |

$\dagger \downarrow$ The arrow indicates the transition of the clock/gate input used for reference: $\dagger$ for the low-to-high transitions. $\downarrow$ for the high-to-low transitions.

Electrical Characteristics Over Operating Conditions


* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics $\mathrm{v}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$

| SYMBOL | PARAMETER |  | TEST CONDITIONS <br> (See Test Load/Waveforms) | MIN | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }_{\text {f MAX }}$ | Maximum output clock frequency |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega \overline{\mathrm{OE}}=\mathrm{L}$ | 40 |  | MHz |
| ${ }^{\text {f MAXD }}$ | Maximum diagnostic clock frequency | Cascaded | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ | 20 |  | MHz |
|  |  | Uncascaded |  | 25 |  |  |
| ${ }^{\text {t CLK }}$ | CLK to output delay |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega \overline{\mathrm{OE}}=\mathrm{L}$ |  | 14 | ns |
| ${ }^{\text {t }}$ S | SDI to SDO delay (MODE = HIGH) |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ |  | 12 | ns |
| ${ }^{\text {m }}$ MS | MODE to SDO delay |  |  |  | 17 | ns |
| ${ }^{t} \mathrm{DS}$ | DCLK to SDO delay (MODE = LOW) |  |  |  | 28 | ns |
| ${ }^{\text {t }}$ DEZL | DCLK to D7-D0 enable delay |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ |  | 25 | ns |
| tDEZH |  |  |  | 20 | ns |  |
| ${ }^{\text {t DDLZ }}$ | DCLK to D7-D0 disable delay |  |  | $C_{L}=5 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ |  | 36 | ns |
| $\mathrm{t}_{\mathrm{DDHZ}}$ |  |  |  |  | 60 | ns |
| ${ }^{t} \mathrm{DC}$ | DCLK to CLK separation |  | $C_{L}=50 \mathrm{pF} R_{L}=280 \Omega \overline{O E}=L$ | 22 |  | ns |
| ${ }^{t} \mathrm{CD}$ | CLK to DCLK separation |  |  | 35 |  | ns |
| ${ }^{\text {tPZL }}$ | Output enable delay |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 19 | ns |
| ${ }_{\text {tPZH }}$ |  |  |  | 13 | ns |  |
| $t_{\text {PLZ }}$ | Output disable delay |  |  | $C_{L}=5 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega$ |  | 12 | ns |
| ${ }_{\text {t }}$ PHZ |  |  |  |  | 22 | ns |

## Switching Characteristics Over Operating Range

| SYMBOL | PARAMETER |  | TEST CONDITIONS <br> (See Interface Test Load/Waveforms) | MILITARY MIN MAX | COMMERCIAL MIN MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {f MAX }}$ | Maximum output clock frequency |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{OE}=\mathrm{L}$ | 33 | 40 | MHz |
| $\mathrm{f}_{\text {MAXD }}$ | Maximum diagnostic clock frequency | Cascaded | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ | 16 | 20 | MHz |
|  |  | Uncascaded |  | 20 | 25 |  |
| tCLK | CLK to output delay |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega \mathrm{OE}=\mathrm{L}$ | 18 | 14 | ns |
| ${ }^{\text {t }}$ SS | SDI to SDO delay (MODE $=$ HIGH) |  | $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ | 18 | 15 | ns |
| ${ }^{\text {t }} \mathrm{MS}$ | MODE to SDO delay |  |  | 27 | 18 | ns |
| ${ }^{t} \mathrm{DS}$ | DCLK to SDO delay (MODE = LOW) |  |  | 38 | 30 | ns |
| ${ }^{\text {t DEZL }}$ | DCLK to D7-D0 enable delay |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ | 35 | 25 | ns |
| tDEZH |  |  | 30 | 25 | ns |  |
| ${ }^{\text {t DDL }}$ | DCLK to D7-D0 disable delay |  |  | $C_{L}=5 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=2 \mathrm{~K} \Omega$ | 45 | 45 | ns |
| ${ }^{\text {t DDHZ }}$ |  |  | 90 |  | 80 | ns |
| ${ }^{\text {D }}$ DC | DCLK to CLK separation |  | $C_{L}=50 \mathrm{pF} R_{L}=280 \Omega O E=L$ | 30 | 30 | ns |
| ${ }^{t} \mathrm{CD}$ | CLK to DCLK separation |  |  | 45 | 40 | ns |
| ${ }^{\text {tPZL }}$ | Output enable delay |  | $C_{L}=50 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 25 | 20 | ns |
| ${ }_{\text {tPZH }}$ |  |  | 20 | 15 | ns |  |
| ${ }^{\text {t PLZ }}$ | Output disable delay |  |  | $C_{L}=5 \mathrm{pF} \mathrm{R}_{\mathrm{L}}=280 \Omega$ | 20 | 15 | ns |
| $\mathrm{t}_{\mathrm{PH}}$ |  |  | 30 |  | 25 | ns |

## Timing Waveforms



Figure 1. Switching waveforms for typical register applications ( $\overline{\mathrm{OE}}=\mathrm{L}$ )


Figure 2. Switching waveforms for shift-in followed by diagnostic load

## Timing Waveforms



Figure 3. Switching waveforms for data bus (D7-D0) disabling

## Enable/Disable Delay



## Test Load



* The "TEST POINT" is drived by the output under test, and observed by instrumentation.

NOTES: $A$. $C_{L}$ includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: $P R R \leq 1 \mathrm{MHz} \mathrm{Z}_{\text {out }}=50 \Omega$ and for series $54 / 74 \mathrm{~S} \mathrm{t}_{\mathrm{R}}=2.5 \mathrm{~ns} \mathrm{t}_{\mathrm{F}} \leq 2.5 \mathrm{~ns}$.
F. When measuring propagation delay times of 3 -state outputs, switches S1 and S2 are closed.

|  | B7-B0 | D7-D0, SDO |
| :---: | :---: | :---: |
| $R_{\mathrm{O}}$ | $1 \mathrm{~K} \Omega$ | $5 \mathrm{~K} \Omega$ |

## Basics of Diagnostics

The basic theory of diagnostics is to insert test data to the inputs of a typical system and sample the test results from certain nodes of the circuits. For a combinatorial circuit, testing is very easy since the circuit has no memory of the previous states. But for a sequential circuit, the data to be sampled at a node depends not only on the inputs, but also on the current state it is in. If the previous state contains some error, it will possibly perform an illegal jump. In that case, depending on which state the system is currently in, the next state may be different. After several illegal jumps, it will be quite impossible to keep track of the jumps which it performs.
A way to solve the problem is by converting a sequential circuit to a combinatorial one. A sequential circuit can often be viewed as a network with a clock and a number of inputs and outputs, with some outputs being routed back to the inputs (see Figure $5 a)$. If the loop is broken and inputs which are fed back from the outputs are instead fed in from some external sources (see Figure 5b), the system can be viewed as combinatorial and system testing will be easier. The "shadow register" concept involves shifting in serial data to the hidden register (the shadow register) and then loading test data to the output register. Together with other system inputs, the test results will appear on the output end of the network and can be sampled and analyzed. and analysed.


Figure 5a. A typical digital system


Figure 5b. The feedback of figure 5 a is broken to convert the system to a non-sequential one

## Diagnostic On-Chip ${ }^{\text {TM }}$ (DOC'™ Using Shadow Register

The diagnostic register is an 8-bit register with two levels of registers-a shadow register and an output register. A shadow register is basically a buried register with shift capability. There is also an output register whose outputs appear to the rest of the system. There is an output flipflop to each shadow flipflop. An output flipflop drives a three-state output buffer before going to the output pin. If the output is disabled, the output pin may be converted to an input pin. This feature is very important if the output is driving a bus and sampling of data on the bus is desired.

The input to a bit of the shadow register is a multiplexer which can select from one of the following nodes:
a) Output of the preceding bit of the shadow register (or SDI for the least significant bit).
b) Output of the same bit of the shadow register.
c) Data on the output pin of the same bit. This data may be the output of the corresponding bit of the output register if there is no output enable pin and the output is enabled, or the input to that pin if there is an output enable pin and output is disabled. Refer to Figure 6 for some general information on a typical diagnostic functional part with output enable ( $\overline{\mathrm{OE}}$ ).


Figure 6. A typical functional block diagram for a diagnostic part

The input to any bit of the output register is also selected from one of the following nodes:
a) Corresponding input bit.
b) Corresponding output bit of the shadow register.

The reasons why a shadow register is preferred, as compared to shifting in diagnostic data directly to the output register, are:
a) The output register contains control signals for the system. Certain bits of this register may control different ports which are driving the same bus. As diagnostic data is shifted in, these bits become random and the ports they are controlling may drive a bus simultaneously. Invalid data may appear and worst of all, with a low-impedance path between the power supply, severe damage may be done to these ports.
b) As a diagnostic word is shifted in, the system is performing different tasks from what it is supposed to do. For example, when an ALU is performing an addition, diagnostic data is shifted in. The ALU then performs some other functions. The status of the system keeps changing. In some cases, illegal states may appear which produces unpredictable test results; for example, a flag may appear unpredictably.
c) The shadow register enables diagnostic data to be shifted in as background data without holding up the processor operation.

The diagnostic register is one part in a series of diagnostic products which follows a new standard for diagnostics. The basic standard is described in Figure 6 and the table on page one. This standard implies that all diagnostic parts in this series are cascadable.

## Diagnostic Pins

There are several pins in the diagnostic register in addition to the regular 8-bit inputs and outputs:

1) Diagnostic Clock (DCLK)-The diagnostic clock is used to clock the shadow register.
2) MODE-This pin is used in selecting the data to the registers. For the output register, MODE = LOW indicates that the output register is being used as a normal register; MODE = HIGH means that the next state of the output register will be obtained from the shadow register. For the shadow register, MODE = LOW indicates serial data from SDI (see below) is shifted in every diagnostic clock; MODE $=$ HIGH switches SDI from a data input to a control input. See below for details.
3) Serial Data In (SDI)-When MODE = LOW, this pin is for shifting serial data in. When MODE $=$ HIGH, SDI serves as a control pin. If MODE $=$ HIGH and SDI = LOW, data from the output pins will be loaded to the shadow register on the next DCLK. MODE $=$ HIGH and SDI $=$ HIGH indicate a reserved operation. The data from the diagnostic clock is held the same. This reserved operation will be very significant when more operations than what is described are needed. The diagnostic register gives an example of how it can be used.
4) Serial Data Out (SDO) -When MODE = LOW, this pin carries the shift-out bit of the shadow register. When MODE $=$ HIGH, the SDI becomes a control pin and the control signal should be passed along if several diagnostic parts are connected together serially. So SDO should carry SDI along in this case.

## Write-Back to RAMs

Due to the applications of a diagnostic register in a writable microprogram control store, this part also includes an additional feature to initialize the control RAMs; when necessary, the input data pins to the register can be operated as output pins. In short, a diagnostic register is an 'asymmetric register transceiver' with shift capability. The term 'asymmetric register transceiver' means that there are two bidirectional registered ports on a chip, and these ports are enabled with different methodologies and have different timings. One port is still primarily for inputs (D7-D0), while the other is primarily for outputs (B7-B0).
When MODE and SDI are both HIGHs, the D7-D0 will be converted to an output port on the rising edge of the next DCLK by enabling the three-state buffers driving the D7-D0. The input for the three-state buffers is from the outputs of the shadow register (S7-S0).

## Applications

This part can be used as a: microprogram control store register, data register, status register, address register, instruction register, interrupt mask register, interrupt vector, program counter, stack pointer, and for other general purposes.
If the diagnostic registers are used in a system using microprogram control words, status registers, and instruction registers, etc., one way to connect them together is shown in Figure 7. There is only one data input and one data output to the diagnostic parts. When serial data is shifted in or shifted out, data has to be passed from one diagnostic chip to another. Since SDI must be passed from chip-to-chip if it is used for control, it is necessary for logic designers to make sure the fall-through time of SDI to the last chip and the setup time from SDI to DCLK are satisfied.


Figure 7. One way diagnostic registers can be linked together

The diagnostic registers are basically used for diagnostic purposes, although they may also function as parallel-to-serial and serial-to-parallel converters.

Two examples of how the diagnostic parts can be built into a system are shown in Figures 8, 9. The diagnostic registers are used to substitute the instruction register, memory data registers, status register, memory address registers, and the registers for a non-writable (Figure 8) or a writable (Figure 9) microprogram control store. The only additional block to a typical system without diagnostic features is the diagnostics controller. The diagnostics controller should be able to supply the system with signals like MODE, SDI, DCLK, and the register clock (CLK). In order words, the diagnostics controller in itself is a supercontroller of the processing unit. It should also be noted that all sequential paths, except for the register files, should be converted to combinatorial paths if all the diagnostic parts are to break the sequential loops.


Figure 8. An application example of using diagnostic registers in a CPU using non-writable control store


Figure 9. An application example of using diagnostic registers in a CPU using writable control store

In normal operation, the diagnostic controller will make the diagnostic feature inactive by setting MODE $=$ LOW and disabling DCLK and have the CLK free running.
When diagnostics are needed, the following sequence is performed:

1) Shift in diagnostic test data bit-by-bit. In order to perform this operation, CLK is disabled; MODE remains LOW; SDI contains the bit to be shifted in, and the diagnostic clock is enabled. This will continue until a full test vector is shifted into the shadow register.
2) MODE switches to HIGH. Then DCLK is disabled and CLK is enabled. The contents of the shadow register, which is the test vector, will be loaded into the output register.
3) The test result is set up at the inputs of the diagnostic registers. MODE switches to LOW again. DCLK is still disabled and CLK is still enabled. The test result will be clocked into the output register.
4) With MODE HIGH and DCLK enabled and CLK disabled, the test result will be clocked to the shadow register.
5) With MODE held LOW and DCLK still enabled and CLK still disabled, the test result can be shifted out and analyzed while another test vector is shifted in.

A block diagram of such a diagnostics controller is shown in Figure 10. The central control unit of this controller may be a disk-based unit or even a diagnostic PROM. Note that, in normal operation, MODE remains LOW and only CLK is active.
Figure 9 is an example with writable programmable control store where initialization of the control RAMs is necessary. This can be done by loading in a sequence of data and address
through the diagnostics controller. What this controller must be able to do, in addition to what is described above (see Figure 10), is to disable the outputs from the microprogram sequencer and feed in the address through another diagnostic register. There is a switch, S1, which switches the SDI to the registers of the writable control store from some other register (in Figure 9, it is the memory address register) to the diagnostic 'control store address' register. The initialization data is shifted into the shadow register by resetting MODE to LOW and enabling DCLK. After all data is shifted into the shadow register, MODE and SDI are set HIGH and then followed by a CLK, a DCLK, and a write to control store. The CLK loads the present control store address in the output registers of the 'control store address' register, and the MODE = HIGH and SDI = HIGH will enable the inputs to the diagnostic register as outputs, so that the data in the shadow register can be written back to the control store.


Figure 10. A diagnostic controller unit

# 8-Bit Bus Latch TransceiversAdvanced CMOS-TTL Compatible 74ACT547 74ACT567 

## Features/Benefits

- Bidirectional transceivers utilizing latches
- Independent latches for $\mathbf{A}$ bus and $B$ bus
- Data can be swapped between internal latches
- 8-blt data paths match byte boundaries
- '547/'567 devices can replace two '373 devices
- Independent gate enables for rank A and rank B
- Low quiescent supply current of $<10 \mu \mathrm{~A}$ (typical)
- Active supply current at about $\mathbf{2 0 \%}$ LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to $5.5 \mathrm{~V} ;-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
- 24-pin SKINNYDIP® saves space.


## Description

These transceivers have a pair of 8-bit latches connected back-to-back, i.e. the bus pins are used for input or output. The latches are followed by either non-inverting ('ACT547) or inverting ('ACT567) three-state buffers.
Both devices have independent gate enable inputs for ranks $A$ and B (GA1, GA2, GB1, GB2), and independent output enables for ranks $A$ and $B$ ( $\overline{O E A B}, \overline{O E B A})$.
The direction of operation is controlled by $\overline{O E A B}$ and $\overline{O E B A}$. When OEAB is Low and OEBA is High, the devices operate in the A-to-B direction. When $\overline{O E A B}$ is High and $\overline{O E B A}$ is Low, the devices operate in the $B$-to-A direction. When $\overline{O E A B}$ and $\overline{O E B A}$ are both High, the $A$ and $B$ buses are configured as inputs. When $\overline{O E A B}$ and $\overline{O E B A}$ are both Low, the $A$ and $B$ buses are configured as outputs. See the Bus Operation Tables for the detailed operation.
Data is passed through the latch whenever either of the gate enables for the respective rank (GA1 or $\overline{\mathrm{GA} 2}, \mathrm{~GB} 1$ or $\overline{\mathrm{GB} 2}$ ) are asserted.
All of the 8-bit devices are packaged in the popular 24-pin SKINNYDIP® package.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE | POLARITY | TYPE | TECH |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 74ACT547 | NS, JS | Commercial | Noninvert | Latch | CMOS |
| 74ACT567 | NS, JS | Commercial | Invert |  |  |

## Logic Symbol



## Logic Symbol

74ACT567
LATCH TRANCEIVER
INVERTING OUTPUTS


## Block Diagrams


'ACT567 (Inverting)


## IEEE Symbols


'ACT567 (Inverting)


## Function Table <br> Nomenclature Description

A0-A7: Eight input/output pins on the $A$ side.
B0-B7: Eight input/output pins on the $B$ side.

X: ... Hor L state irrelevant ("Don't Care" conditions).

GA1/GA2: Gate enables for rank A of 'ACT547/'ACT567.
GB1/GB2: Gate enables for rank B of 'ACT547/'ACT567.
QoA/QoB: Previous data of the internal rank $A / B$.

| GA1 | $\overline{\text { GA2 }}$ | RANK A | GB1 | $\overline{\text { GB2 }}$ | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathbf{X}$ | L | Enabled <br> (Flush) | X | L | Enabled <br> (Flush) |
| X | L | Enabled <br> (Flush) | L | H | Disabled <br> (Freeze) |
| L | H | Disabled <br> (Freeze) | X | L | Enabled <br> (Flush) |
| L | H | Disabled <br> (Freeze) | L | H | Disabled <br> (Freeze) |
| H | X | Enabled <br> (Flush) | X | L | Enabled <br> (Flush) |
| H | X | Enabled <br> (Flush) | L | H | Disabled <br> (Freeze) |
| $\mathbf{X}$ | Enabled <br> (Flush) | H | X | Enabled <br> (Flush) |  |


| $\overline{\text { OEAB: }}$ | To enable the A-to-B operation. |
| :--- | :--- |
| $\overline{\text { OEBA: }}$ | To enable the B-to-A operation. |


| $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | OPERATION DIRECTION |
| :---: | :---: | :--- |
| L | L | A, B buses both are outputs <br> (Transfer stored data to bus stored) |
| L | H | A-to-B |
| H | L | B-to-A |
| H | H | A, B buses both are inputs (storage) |

## Bus Operation for 'ACT547

| OPERATION | DIRECTION CONTROL |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { GATE } \\ & \text { ENABLE }(\mathbf{A}) \end{aligned}$ |  | RANK A | GATE <br> ENABLE (B) |  | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | A0-A7 | B0-B7 |  | GA1 | $\overline{\text { GA2 }}$ |  | GB1 | $\overline{\text { GB2 }}$ |  |
| Storage | H | H | Input | Input |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | L | H | Qob |
|  |  |  |  |  |  | H | X | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | X | L | $B$ bus |
|  |  |  |  |  |  | $x$ | L | A bus | L | H | QoB |
|  |  |  |  |  |  | X | L | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | X | L | $B$ bus |
| B-to-A Operation | H | L | Output of Rank B | Input |  | L | H | QoA | L' | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | B bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | Rank B | L | H | QoB |
|  |  |  |  |  |  | H | X | Rank B | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | Rank B | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | Rank B | L | H | Qob |
|  |  |  |  |  |  | X | L | Rank B | H | X | B bus |
|  |  |  |  |  |  | X | L | Rank B | X | L | $B$ bus |
| A-to-B Operation | L | H | Input | Output of <br> Rank A |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | Rank A |
|  |  |  |  |  |  | L | H | QoA | X | L | Rank A |
|  |  |  |  |  |  | H | X | A bus | L | H | Qob |
|  |  |  |  |  |  | H | X | A bus | H | X | Rank A |
|  |  |  |  |  |  | H | X | A bus | X | L | Rank A |
|  |  |  |  |  |  | X | L | A bus | L | H | Qob |
|  |  |  |  |  |  | X | L | A bus | H | X | Rank A |
|  |  |  |  |  |  | X | L | A bus | X | L | Rank A |
| Transfer Stored Data | L | L | Output of Rank B | Output of Rank A |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | Rank A |
|  |  |  |  |  |  | L | H | QoA | X | L | Rank A |
|  |  |  |  |  |  | H | X | Rank B | L | H | Qob |
|  |  |  |  |  |  | $\mathrm{H}^{\star}$ | X | Rank B | H | X | Rank A |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | X | Rank B | X | L | Rank A |
|  |  |  |  |  |  | X | L | Rank B | L | H | Qob |
|  |  |  |  |  |  | $\mathrm{X}^{*}$ | L | Rank B | H | X | Rank A |
|  |  |  |  |  |  | $\mathrm{X}^{*}$ | L | Rank B | X | L | Rank A |

* Note: These controls for $\overline{\mathrm{OEAB}}, \overline{\mathrm{OEBA}}, \mathrm{GA} 1, \overline{\mathrm{GA} 2}, \mathrm{GB1}$ and $\overline{\mathrm{GB} 2}$ can cause race conditions.


## Bus Operation for 'ACT567

| OPERATION | DIRECTION CONTROL |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{gathered} \text { GATE } \\ \text { ENABLE }(A) \end{gathered}$ |  | RANK A | GATE ENABLE (B) |  | RANK B |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\text { OEAB }}$ | $\overline{\text { OEBA }}$ | A0-A7 | B0-B7 |  | GA1 | $\overline{\text { GA2 }}$ |  | GB1 | $\overline{\text { GB2 }}$ |  |
| Storage | H | H | Input | Input |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | L | H | Qob |
|  |  |  |  |  |  | H | X | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | A bus | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | L | H | Qob |
|  |  |  |  |  |  | X | L | A bus | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | A bus | X | L | $B$ bus |
| B-to-A Operation | H | L | $\left\lvert\, \begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { Rank B } \end{aligned}\right.$ | Input |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $B$ bus |
|  |  |  |  |  |  | L | H | QoA | X | L | $B$ bus |
|  |  |  |  |  |  | H | X | Rank B | L | H | Qob |
|  |  |  |  |  |  | H | X | Rank B | H | X | $B$ bus |
|  |  |  |  |  |  | H | X | Rank B | X | L | $B$ bus |
|  |  |  |  |  |  | X | L | $\overline{\text { Rank B }}$ | L | H | Qob |
|  |  |  |  |  |  | X | L | Rank B | H | X | $B$ bus |
|  |  |  |  |  |  | X | L | Rank B | X | L | $B$ bus |
| A-to-B Operation | L | H | Input |  |  | L | H | QoA | L | H | QoB |
|  |  |  |  |  |  | L | H | QoA | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | L | H | QoA | X | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | H | X | A bus | L | H | QoB |
|  |  |  |  |  |  | H | $x$ | A bus | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | H | X | A bus | X | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | X | L | A bus | L | H | Qob |
|  |  |  |  |  |  | X | L | A bus | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | X | L | A bus | X | L | $\overline{\text { Rank A }}$ |
| Transfer Stored Data | L | L | $\begin{aligned} & \begin{array}{l} \text { Output } \\ \text { of } \end{array} \\ & \hline \text { Rank } \end{aligned}$ | $\left\|\begin{array}{l} \text { Output } \\ \text { of } \end{array}\right\|$ |  | L | H | QoA | L | H | Qob |
|  |  |  |  |  |  | L | H | QoA | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | L | H | QoA | X | L | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | H | X | $\overline{\text { Rank B }}$ | L | H | QoB |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | $x$ | $\overline{\text { Rank B }}$ | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | $\mathrm{H}^{*}$ | X | $\overline{\text { Rank B }}$ | X | L | Rank A |
|  |  |  |  |  |  | X | L | $\overline{\text { Rank B }}$ | L | H | Qob |
|  |  |  |  |  |  | $\mathrm{X}^{*}$ | L | Rank B | H | X | $\overline{\text { Rank A }}$ |
|  |  |  |  |  |  | $\mathrm{X}^{*}$ | L | $\overline{\text { Rank B }}$ | X | L | $\overline{\text { Rank A }}$ |

[^73]
## Absolute Maximum Ratings





 Input diode current, $\mathrm{I}_{\mathrm{I}}$ :

Output diode current, IOK:


## Operating Conditions

| SYMBOL | PARAMETER |  |  | MIN | MER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{C C}$ | Supply voltage |  |  | 4.5 | 5 | 5.5 | V |
| TA | Operating free air temperature |  |  | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of gate | High |  | 12 |  |  | ns |
|  |  | Low |  | 12 |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Setup time | 'ACT547 | GA1, GB1 | 81. |  |  | ns |
|  |  |  | $\overline{\mathrm{GA} 2}, \overline{\mathrm{~GB} 2}$ | 81 |  |  |  |
|  |  | 'ACT567 | GA1, GB1 | 81 |  |  |  |
|  |  |  | $\overline{\mathrm{GA} 2}, \overline{\mathrm{~GB} 2}$ | 81 |  |  |  |
| th | Hold time | 'ACT547 | GA1, GB1 | 81 |  |  | ns |
|  |  |  | $\overline{\mathrm{GA} 2}, \overline{\mathrm{~GB} 2}$ | 81 |  |  |  |
|  |  | 'ACT567 | GA1, GB1 | 81 |  |  |  |
|  |  |  | $\overline{\mathrm{GA} 2}, \overline{\mathrm{~GB} 2}$ | 1 |  |  |  |
| $t_{r}$ | Input rise time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  |  | 0 |  | 500 | ns |
| $\mathrm{tf}_{f}$ | Input fall time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  |  | 0 |  | 500 | ns |

! ! The arrows indicate the transition of the gate control input used as reference: 1 for the LOW-to-HIGH transitions, $\downarrow$ for the HIGH-to-LOW transitions.

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{O}}<0 \\
& \text {-20 mA }
\end{aligned}
$$

$$
\begin{aligned}
& V_{1}<0 \\
& \text {-20 mA }
\end{aligned}
$$

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  |  | 0.8 | V |
| $\mathrm{V}_{\text {IH }}$ | High-level input voltage |  |  | 2 |  |  | V |
| IN | Input current | $V_{C C}=$ MAX | $\begin{gathered} V_{1}=V_{C C} \\ \text { or GND } \end{gathered}$ |  |  | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{\mathrm{CC}}=\text { MAX } \\ & V_{\mathrm{IL}}=\mathrm{MAX} \\ & V_{I H}=\text { MIN } \end{aligned}$ | $\mathrm{I}_{\mathrm{OL}}=20 \mu \mathrm{~A}$ |  |  | 0.1 | V |
|  |  |  | $\mathrm{I}^{\mathrm{OL}}=6 \mathrm{~mA}$ |  |  | 0.37 |  |
|  |  |  | $\mathrm{l}^{\mathrm{OL}}=12 \mathrm{~mA}$ |  |  | 0.4 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $\mathrm{IOH}^{\prime}=-20 \mu \mathrm{~A}$ | 3.4 |  |  | V |
|  |  |  | ${ }^{1} \mathrm{OH}=-6 \mathrm{~mA}$ | 2.4 |  |  |  |
| Ioz | Off-state output current | $V_{C C}=$ MAX | $\begin{gathered} V_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}} \\ \text { or GND } \end{gathered}$ |  |  | $\pm 30$ | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{CC}$ | Quiescent supply current | $V_{C C}=M A X$ | $\begin{gathered} V_{1}=V_{C C C} \\ \text { or GND } \end{gathered}$ |  |  | 80 | $\mu \mathrm{A}$ |

## Switching Characteristics

| SYMBOL | PARAMETER | TEST CONDITIONS <br> (See Interface Test Load/Waveform) | MIN | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPLH }}$ | GA1, $\overline{\mathrm{GA} 2}, \mathrm{GB1}$ or $\overline{\mathrm{GB} 2}$ | $C_{L}=50 \mathrm{pF}$ |  | 32 |  |
| tPHL | to output delay |  |  | 32 | ns |
| ${ }^{\text {tPLH }}$ | Data to output delay |  |  | 32 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 32 |  |
| ${ }_{\text {tPZL }}$ | Output enable delay | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=1 \mathrm{~K} \Omega \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | 34 | ns |
| ${ }^{\text {tPZH }}$ |  |  |  | 34 |  |
| $t_{\text {PLZ }}$ | Output disable delay |  |  | 34 | ns |
| ${ }^{\text {tPHZ }}$ |  |  |  | 34 |  |

## Typical ICC vs Frequency

74ACT547/567


## 74ACT547 74ACT567

## Definition of Waveforms



GA1, $\overline{\mathrm{GA2}}, \mathrm{~GB} 1$ or $\overline{\mathrm{GB2}}$ to Output Delay

$V_{\mathbf{T}}=1.3 \mathrm{~V}$

## Enable/Disable Waveforms



## Test Load



Notes: 1. $C_{L}$ includes probe and jig capacitance.
2. When measuring $t_{P Z L}, S_{1} 1$ is tied to $V_{C C}$. When measuring $t_{P H Z}$ and $t_{P Z H}$, $S_{1}$ is tied to ground.
When measuring propagation delay times of three-state outputs, $S_{1}$ is open, i.e. not connected to $\mathrm{V}_{\mathrm{CC}}$ or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
Waveform 1 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \mathrm{MHz}, \mathrm{t}_{\mathrm{r}} \leq 6 \mathrm{~ns}$, $\mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}, \mathrm{Z}_{\text {out }}=50 \Omega$.

## 8-Bit Bus Front-Loading Latch Transceivers Advanced CMOS-TTL Compatible 74 ACT646

## Features/Benefits

- Bidirectional bus transceiver and register
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- 24-pin SKINNYDIP® ${ }^{\circledR}$ saves space
- Three-state outputs drive bus lines
- Low quiescent supply current of $<\mathbf{1 0} \mu \mathrm{A}$ (typical)
- Active supply current at about $20 \%$ LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to $5.5 \mathrm{~V} ;-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$


## Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gatelevel hardware configurations for the 'ACT646/648 are given in the Logic Diagram. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B upon the rising edge of the appropriate clock signals. CKA

## Ordering Information

clocks register A , which receives data from the B bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by enable line $\bar{E}$, and direction line DIR.
When $\bar{E}$ is High, data from the buses can be stored into register $A$ and $B$. When $\bar{E}$ is Low and DIR is High, the direction of operation is from $A$ to $B$, when $\bar{E}$ and DIR are Low, the direction of operation is from $B$ to $A$.
SRA is used to select between register $A$ and the $B$ bus, and then to route the data to a controlled buffer connected to the A bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the $B$ bus through a controlled buffer.

| PART <br> NUMBER | PKG | TEMP | POLARITY | OUTPUT | TECH |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 74ACT646 | NS,JS | Com | Noninvert | Three- | CMOS |
| state |  |  |  |  |  |

## Pin Configurations



## Logic Diagrams

'ACT646 (Non-Inverting)

'ACT648 (Inverting)


## IEEE Symbols



## Block Diagrams

'ACT646 (Non-inverting)

'ACT648


ACT648 (Inverting)


## Function Table Nomenclature Description

E:
To enable A-to-B or B-to-A operation.
DIR: To select the direction of operation.

| $\overline{\mathbf{E}}$ | DIR | OPERATION DIRECTION |
| :---: | :---: | :---: |
| L | L | B-to-A |
| L | H | A-to-B |
| H | X | A and B buses both are inputs <br> (Storage) |

SRA/SRB: To select the output data coming from the $A / B$ register if SRA/SRB is a High level; otherwise, directly from the input data bus.
A0-A7: $\quad$ Eight input/output pins on the $A$ side.
B0-B7: Eight input/output pins on the $B$ side.
CKA/CKB: Clock for Register A/B.
X: $\quad H$ or L state irrelevant ("Don't Care" condition).
t: Positive edge of clock causes clocking, if clock enable is asserted.

UC: $\quad H$ or L or 1 case (nonclocked operation).
RGTR: Register.

## Bus Operation for 'ACT646

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | 'ACT646 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\bar{E}$ | DIR | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | H | X | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | Real time $A$ bus data $\rightarrow$ RGTR $B$ Real time B bus data $\rightarrow$ RGTR A |
| Real time <br> B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $B$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $B$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time $B$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR A Real time $B$ bus data $\rightarrow$ RGTR B |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | RGTR A data $\rightarrow$ A bus RGTR A data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time B bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time B bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow A$ bus <br> RGTR A data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | L | H | X | L. | Input | Output |  | UC | UC | Real time $A$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $A$ bus data $\rightarrow B$ bus <br> Real time A bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | $\begin{aligned} & \text { Real time } A \text { bus data } \rightarrow B \text { bus } \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR A } \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR B } \end{aligned}$ |
| Stored data <br> A-to-B <br> Operation | L | H | X | H | Input | Output |  | UC | UC | RGTR $B$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR B data $\rightarrow$ B bus |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | RGTR B data $\rightarrow B$ bus RGTR B data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time A bus data $\rightarrow$ RGTR B RGTR B data $\rightarrow$ B bus RGTR B data $\rightarrow$ RGTR A |

## Bus Operation for 'ACT648

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | 'ACT648 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\overline{\mathrm{E}}$ | DIR | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | H | X | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | Real time A bus data $\rightarrow$ RGTR B <br> Real time B bus data $\rightarrow$ RGTR A |
| Real time <br> B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $\bar{B}$ bus data $\rightarrow A$ bus <br> Real time $\bar{B}$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1. | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR A Real time $\bar{B}$ bus data $\rightarrow$ RGTR $B$ |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR $\bar{A}$ data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | UC | 1 | $\begin{aligned} & \text { RGTR } \overline{\bar{A}} \text { data } \rightarrow \mathrm{A} \text { bus } \\ & \text { RGTR } \overline{\mathrm{A}} \text { data } \rightarrow \text { RGTR B } \end{aligned}$ |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | Real time $B$ bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $\rightarrow A$ bus RGTR A data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | L | H | X | L | Input | Output |  | UC | UC | Real time $\bar{A}$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time $\bar{A}$ bus data $\rightarrow B$ bus Real time $A$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $\overline{\bar{A}}$ bus data $\rightarrow B$ bus Real time $\bar{A}$ bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | $\begin{aligned} & \text { Real time } \overline{\bar{A}} \text { bus data } \rightarrow B \text { bus } \\ & \text { Real time } \bar{A} \text { bus data } \rightarrow \text { RGTR A } \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR B } \end{aligned}$ |
| Stored data <br> A-to-B <br> Operation | L | H | X | H | Input | Output |  | UC | UC | RGTR $\bar{B}$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time A bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | RGTR $\bar{B}$ data $\rightarrow B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR $A$ |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time $A$ bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR A |

## Absolute Maximum Ratings

Supply voltage, $\mathrm{V}_{\mathrm{CC}}$ ..... -0.5 V to 7.0 V
DC input voltage, $\mathrm{V}_{1}$ ..... -0.5 V to $\mathrm{V}_{\mathrm{CC}}+0.5 \mathrm{~V}$
DC output voltage, $\mathrm{V}_{\mathrm{O}}$ -0.5 V to $\mathrm{VCC}^{+0.5} \mathrm{~V}$
DC output source/sink current per output pin, 10 ..... $\pm 35 \mathrm{~mA}$
DC $V_{C C}$ or ground current, I CC or IGND ..... $\pm 100 \mathrm{~mA}$
Input diode current, IIK:
$V_{1}<0$ ..... $-20 \mathrm{~mA}$
$V_{1}>V_{C c}$ ..... $+20 \mathrm{~mA}$
Output diode current, IOK:
$V_{0}<0$ ..... $-20 \mathrm{~mA}$
$\mathrm{V}_{\mathrm{O}}>\mathrm{V}_{\mathrm{CC}}$ ..... $+20 \mathrm{~mA}$
Storage temperature -65 to $+150^{\circ} \mathrm{C}$

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | AMER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of clock | High | 20 |  |  | ns |
|  |  | Low | 20 |  |  |  |
| ${ }^{\text {tsu }}$ | Set up time |  | 251 |  |  | ns |
| $t_{h}$ | Hold time |  | $0 \dagger$ |  |  | ns |
| $t_{r}$ | Input rise time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  | 0 |  | 500 | ns |
| $t_{f}$ | Input fall time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  | 0 |  | 500 | ns |
| ${ }^{1} \mathrm{OH}$ | High-level output current |  |  |  | -6 | mA |
| ${ }^{1} \mathrm{OL}$ | Low-level output current |  |  |  | 12 | mA |

[^74]
## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | $\begin{aligned} & 25^{\circ} \mathrm{C} \\ & \text { TYP MAX } \end{aligned}$ | COMMERCIAL MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2 |  | 2 | V |
| IN | Input current | $V_{C C}=$ MAX | $V_{1}=V_{C C}$ or GND |  | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| VOL | Low-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $\mathrm{IOL}=20 \mu \mathrm{~A}$ |  | 0.1 | 0.1 | V |
|  |  |  | $10=6 \mathrm{~mA}$ |  | 0.32 | 0.37 |  |
|  |  |  | $\mathrm{IOL}=12 \mathrm{~mA}$ |  | 0.4 | 0.4 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $\mathrm{IOH}^{\prime}=-20 \mu \mathrm{~A}$ | 3.4 |  | 3.4 | V |
|  |  |  | $\mathrm{IOH}^{\prime}=-6 \mathrm{~mA}$ | 2.4 |  | 2.4 |  |
| ${ }^{1} \mathrm{OZ}$ | Off-state output current | $V_{C C}=$ MAX | $V_{O}=V_{C C}$ or GND |  | $\pm 10$ | $\pm 30$ | $\mu \mathrm{A}$ |
| 'CC* | Quiescent supply current | $V_{C C}=$ MAX | $V_{1}=V_{C C}$ or GND |  | 10 | 40 | $\mu \mathrm{A}$ |

* See ICC vs. Frequency chart.


## Switching Characteristics

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveform) | $\begin{gathered} \text { COMMERCIAL } \\ \text { MIN } \mathrm{T}_{A}=25^{\circ} \mathrm{C} \end{gathered}$ | MIN | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPLH }}$ | Data to output delay | $C_{L}=50 \mathrm{pF}$ | 38 |  | 45 | ns |
| ${ }_{\text {tPHL }}$ |  |  | 38 |  | 45 |  |
| ${ }^{\text {tPLH }}$ | Clock to output delay |  | 32 |  | 38 | ns |
| ${ }^{\text {t }} \mathrm{PHL}$ |  |  | 32 |  | 38 |  |
| ${ }^{\text {tPLH }}$ | Select to output delay* (data input high) |  | 32 |  | 35 | ns |
| ${ }_{\text {t }}^{\text {PHL }}$ |  |  | 32 |  | 35 |  |
| ${ }^{\text {tPLH }}$ | Select to output delay* (data input low) |  | 32 |  | 35 | ns |
| ${ }^{\text {tPHL }}$ |  |  | 32 |  | 35 |  |
| ${ }^{\text {tPZL }}$ | Output enable delay | $\begin{aligned} R_{\mathrm{L}} & =1 \mathrm{~K} \Omega \\ \mathrm{C}_{\mathrm{L}} & =50 \mathrm{pF} \end{aligned}$ | 40 |  | 45 | ns |
| ${ }^{\text {t }} \mathrm{PZH}$ |  |  | 40 |  | 45 | ns |
| ${ }^{\text {t PLZ }}$ | Output disable delay |  | 35 |  | 40 | ns |
| ${ }^{\text {t }} \mathrm{PHZ}$ |  |  | 35 |  | 40 |  |
| ${ }^{\text {tPZL }}$ | Direction enable delay |  | 40 |  | 45 | ns |
| ${ }^{\text {tPZH }}$ |  |  | 35 |  | 40 |  |
| ${ }^{\text {t PLZ }}$ | Direction disable delay |  | 30 |  | 35 | ns |
| ${ }^{\text {tPHZ }}$ |  |  | 30 |  | 35 |  |

${ }^{*}$ See Figure 4.

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## Test Waveforms

## Setup Time/Hold Time


$\mathbf{V}_{\mathbf{T}}=1.3 \mathrm{~V}$
Figure 1.

Bus Data To Bus Output Delay


Figure 2.

CK To Bus Output Propagation Delay Time

$\mathrm{V}_{\mathbf{T}}=1.3 \mathrm{~V}$
Figure 3.


NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4.

## Enable/Disable/Direction-Change Delay



Figure 5.

## Test Load



Figure 6.

NOTES 1. $C_{L}$ includes probe and jig capacitance.
2. When measuring $t_{P L Z}$ and $t_{P Z L}, S_{1}$ is tied to $V_{C C}$. When measuring $t_{P H Z}$ and $t_{P Z H}$, $\mathrm{S}_{1}$ is tied to ground.
When measuring propagation delay times of three-state outputs, $S_{1}$ is open, i.e., not connected to $\mathrm{V}_{\mathrm{CC}}$ or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: $\operatorname{PRR} \leq 1 \mathrm{MHz}, \mathrm{t}_{\mathrm{r}} \leq 6 \mathrm{~ns}$, $\mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}, \mathrm{Z}_{\text {out }}=50 \Omega$.

## Typical ICC vs. Frequency



# 8-Bit Bus Front-Loading Latch Transceivers - <br> Advanced CMOS-TTL Compatible 74ACT651 74ACT652 

## Features/Benefits

- Bidirectional bus transceiver and register
- Independent registers for A and B buses
- Real-time data transfer or stored data transfer
- Simultaneous outputs on both buses
- 24-pin SKINNYDIP ${ }^{\circledR}$ saves space
- Three-state outputs drive bus lines
- Low quiescent supply current of $<10 \mu \mathrm{~A}$ (typical)
- Active supply current at about $\mathbf{2 0 \%}$ LS equivalent
- Wide commercial operating supply and temperature ranges 4.5 V to $5.5 \mathrm{~V} ;-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$


## Description

This 8-bit bus transceiver with three-state outputs has sixteen D-type flip-flops and multiplexers. The bus-oriented pinout of the part is shown in the Pin Configuration. The internal gatelevel hardware configurations for the 'ACT651/652 are given in the Logic Diagrams. The basic repeated element, consisting of an edge-triggered flip-flop paralleled with a bypassing path, or "feed-through", into a two-way multiplexer is sometimes called a "front-loading latch."
A pair of multiplexers are used to distribute two bytes of data through the part. The data-routing combinations offered by the multiplexers provide flexibility in directing data to or from either bus, and/or either register. Data is loaded into registers A or B

## Pin Configurations

'ACT651/652
8-Bit Bus Front-Loading Latch Transceiver


## Ordering Information

| PART <br> NUMBER | PKG | TEMP | POLARITY | OUTPUT | TECH |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 74ACT651 | NS,JS | Com | Noninvert | Three- <br> state | CMOS |
| 74ACT652 | NS,JS | Com | Invert |  |  |

upon the rising edge of the appropriate clock signals. CKA clocks register $A$, which receives data from the $B$ bus directly at its inputs. Similarly, CKB clocks register B, which has the A bus available directly at its inputs. Control of the multiplexers is provided by two select lines (one per register), SRA and SRB. Command of the outputs is performed by two enable lines, GAB and $\overline{\text { GBA }}$.

When GAB is low and $\overline{G B A}$ is high, data from the buses can be loaded into registers $A$ and $B$. When $\overline{G B A}$ is low, the $A$ bus is configured for output. When GAB is high, the $B$ bus is configured for output. The $A$ and $B$ buses can be enabled at the same time, to operate as outputs simultaneously.

SRA is used to select between register $A$ and the $B$ bus, and then to route the data to a controlled buffer connected to the $A$ bus. Likewise, SRB selects between register B and the A bus, and then routes the data to the $B$ bus through a controlled buffer.

## Logic Diagrams

'ACT651 (Inverting)

'ACT652 (Non-Inverting)


## IEEE Symbols

'ACT651


## Block Diagrams


'ACT652

'ACT652 (Non-inverting)


## 74ACT651 74ACT652

## Function Table Nomenclature Description

GAB: To enable A-to-B operation.
GBA: $\quad$ To enable B-to-A operation.

| GAB | $\overline{\text { GBA }}$ | OPERATION DIRECTION |
| :---: | :---: | :---: |
| L | L | B-to-A |
| L | H | A and B buses both are inputs <br> (Storage) |
| $H$ | L | A and B buses both are outputs <br> (Transfer stored data to bus) |
| H | H | A-to-B |

SRA/SRB: To select the output data coming from the $A / B$ register if SRA/SRB is a High level; otherwise, directly from the input data bus.
AO-A7: Eight input/output pins on the $A$ side.
B0-B7: Eight input/output pins on the $B$ side.
CKA/CKB: Clock for register A/B.
X: $\quad H$ or L state irrelevant ("Don't Care" condition).
$t: \quad$ Positive edge of CK causes clocking, if clock enable is asserted.

UC: $\quad H$ or L or 1 case (nonclocked operation).
RGTR: Register.

## Bus Operation for 'ACT651

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | CLOCKENABLE |  | 'ACT651 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | GAB | $\overline{\text { GBA }}$ | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | L | H | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time A bus data $\rightarrow$ RGTR B <br> Real time B bus data $\rightarrow$ RGTR A |
| Real time B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time $\bar{B}$ bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | $\dagger$ | Real time $\bar{B}$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR A Real time $\bar{B}$ bus data $\rightarrow$ RGTR B |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR $\bar{A}$ data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | $\begin{aligned} & \text { RGTR } \bar{A} \text { data } \rightarrow A \text { bus } \\ & \text { RGTR } \bar{A} \text { data } \rightarrow \text { RGTR B } \end{aligned}$ |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $-A$ bus |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | Real time $B$ bus data $\rightarrow$ RGTR A RGTR $\bar{A}$ data $\rightarrow \mathrm{A}$ bus RGTR $\bar{A}$ data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | H | H | X | L | Input | Output |  | UC | UC | Real time $\bar{A}$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $\bar{A}$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $\bar{A}$ bus data $\rightarrow B$ bus Real time $\bar{A}$ bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | $\begin{aligned} & \text { Real time } \bar{A} \text { bus data } \rightarrow B \text { bus } \\ & \text { Real time } \bar{A} \text { bus data } \rightarrow \text { RGTR } A \\ & \text { Real time } A \text { bus data } \rightarrow \text { RGTR } B \\ & \hline \end{aligned}$ |
| Stored data <br> A-to-B <br> Operation | H | H | X | H | Input | Output |  | UC | UC | RGTR $\bar{B}$ data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data - B bus |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR $\bar{B}$ data $-B$ bus RGTR $\bar{B}$ data - RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR $\bar{B}$ data $\rightarrow$ B bus RGTR $\bar{B}$ data $\rightarrow$ RGTR $A$ |
| Transfer <br> Stored <br> Data | H | L | H | H | Output | Output |  | UC | UC | RGTR $\bar{A} / \bar{B}$ data $\rightarrow$ A/B bus |
|  |  |  |  |  |  |  |  | UC | $\dagger$ | $R G T R \bar{A} / \bar{B}$ data $\rightarrow A / B$ bus RGTR $\bar{A}$ data - RGTR $B$ |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | RGTR $\bar{A} / \bar{B}$ data $\rightarrow A / B$ bus RGTR $\bar{B}$ data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | RGTR $\bar{A} / \bar{B}$ data $\rightarrow A / B$ bus RGTR $\bar{A}$ data - RGTR B RGTR $\bar{B}$ data - RGTR A |

## Bus Operation for 'ACT652

| OPERATION | CONTROL |  |  |  | DATA I/O |  | BLOCK DIAGRAM | $\begin{aligned} & \text { CLOCK } \\ & \text { ENABLE } \end{aligned}$ |  | 'ACT652 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | GAB | $\overline{\mathbf{G B A}}$ | SRA | SRB | A0-A7 | B0-B7 |  | CKA | CKB |  |
| Storage | L | H | X | X | Input | Input |  | UC | UC | No operation |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data - RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time A bus data $\rightarrow$ RGTR B Real time $B$ bus data $\rightarrow$ RGTR A |
| Real time <br> B-to-A <br> Operation | L | L | L | X | Output | Input |  | UC | UC | Real time $B$ bus data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $B$ bus data $\rightarrow A$ bus Real time B bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow A$ bus <br> Real time B bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | $\dagger$ | Real time $B$ bus data $\rightarrow A$ bus Real time $B$ bus data $\rightarrow$ RGTR A Real time $B$ bus data $\rightarrow$ RGTR B |
| Stored data <br> B-to-A <br> Operation | L | L | H | X | Output | Input |  | UC | UC | RGTR $A$ data $\rightarrow A$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | $\begin{aligned} & \text { RGTR A data } \rightarrow \text { A bus } \\ & \text { RGTR A data } \rightarrow \text { RGTR B } \end{aligned}$ |
|  |  |  |  |  |  |  |  | 1 | UC | Real time $B$ bus data $\rightarrow$ RGTR A RGTR A data $\rightarrow$ A bus |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time $B$ bus data $\rightarrow$ RGTR $A$ RGTR A data $\rightarrow$ A bus RGTR A data $\rightarrow$ RGTR B |
| Real time <br> A-to-B <br> Operation | H | H | X | L | Input | Output |  | UC | UC | Real time $A$ bus data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time $A$ bus data $\rightarrow B$ bus <br> Real time A bus data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | $\dagger$ | UC | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | $\dagger$ | 1 | Real time $A$ bus data $\rightarrow B$ bus Real time A bus data $\rightarrow$ RGTR A Real time A bus data $\rightarrow$ RGTR B |
| Stored data <br> A-to-B <br> Operation | H | H | X | H | Input | Output |  | UC | UC | RGTR B data $\rightarrow$ B bus |
|  |  |  |  |  |  |  |  | UC | 1 | Real time A bus data $\rightarrow$ RGTR B RGTR B data $\rightarrow B$ bus |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR B data $\rightarrow$ B bus RGTR B data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | Real time $A$ bus data $\rightarrow$ RGTR B RGTR B data $\rightarrow B$ bus RGTR B data $\rightarrow$ RGTR A |
| Transfer <br> Stored <br> Data | H | L | H | H | Output | Output |  | UC | UC | $R G T R A / B$ data $\rightarrow A / B$ bus |
|  |  |  |  |  |  |  |  | UC | 1 | RGTR A/B data $\rightarrow A / B$ bus RGTR A data $\rightarrow$ RGTR B |
|  |  |  |  |  |  |  |  | 1 | UC | RGTR A/B data $\rightarrow A / B$ bus RGTR B data $\rightarrow$ RGTR A |
|  |  |  |  |  |  |  |  | 1 | 1 | RGTR A/B data $\rightarrow$ A/B bus RGTR A data $\rightarrow$ RGTR B RGTR B data $\rightarrow$ RGTR A |

## Absolute Maximum Ratings






Input diode current, $\mathrm{I}_{\mathrm{K}}$ :


Output diode current, IOK:




## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | MER TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\mathrm{A}}$ | Operating free-air temperature |  | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {t }}$ w | Width of clock | High | 20 |  |  | ns |
|  |  | Low | 20 |  |  |  |
| $\mathrm{t}_{\text {su }}$ | Set up time |  | 251 |  |  | ns |
| $t_{h}$ | Hold time |  | 01 |  |  | ns |
| $\mathrm{t}_{\mathrm{r}}$ | Input rise time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  | 0 |  | 500 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | Input fall time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  | 0 |  | 500 | ns |
| ${ }^{1} \mathrm{OH}$ | High-level output current |  |  |  | -6 | mA |
| ${ }^{\text {OL }}$ | Low-level output current |  |  |  | 12 | mA |

$\dagger$ The arrow indicates the Low-to-High transition of the clock input used as reference.

## 74ACT651 74ACT652

## Electrical Characteristics Over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | $\begin{aligned} & 25^{\circ} \mathrm{C} \\ & \text { TYP MAX } \end{aligned}$ | COMMERCIAL MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2 |  | 2 | V |
| IN | Input current | $V_{C C}=\mathrm{MAX}$ | $V_{1}=V_{C C}$ or GND |  | $\pm 1.0$ | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=\text { MIN } \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $\mathrm{IOL}=20 \mu \mathrm{~A}$ |  | 0.1 | 0.1 | V |
|  |  |  | $10=6 \mathrm{~mA}$ |  | 0.32 | 0.37 |  |
|  |  |  | $\mathrm{IOL}=12 \mathrm{~mA}$ |  | 0.4 | 0.4 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $1 \mathrm{OH}=-20 \mu \mathrm{~A}$ | 3.4 |  | 3.4 | V |
|  |  |  | $\mathrm{IOH}=-6 \mathrm{~mA}$ | 2.4 |  | 2.4 |  |
| 'oz | Off-state output current | $V_{C C}=$ MAX | $V_{O}=V_{C C}$ or GND |  | $\pm 10$ | $\pm 30$ | $\mu \mathrm{A}$ |
| ${ }^{1} \mathrm{CC*}$ | Quiescent supply current | $V_{C C}=M A X$ | $V_{1}=V_{C C}$ or GND |  | 10 | 40 | $\mu \mathrm{A}$ |

* See ICC vs. Frequency chart.


## Switching Characteristics



[^75]
## Test Waveforms

Setup Time/Hold Time


Figure 1

## CK To Bus Output Propagation Delay Time



Figure 3


NOTES: 1. When SRA/SRB is low, the input data will transfer to output bus.
2. When SRA/SRB is high, the data of register will transfer to output bus.
3. For the inverting devices, the timing is similar, but the output is opposite to that for the non-inverting devices.

Figure 4

# 74ACT651 74ACT652 

## Typical ICC vs. Frequency

74ACT651/652


## Enable/Disable/Direction-Change Delay



Figure 5

## Standard Test Load



Figure 6

NOTES 1. $C_{L}$ includes probe and jig capacitance.
2. When measuring $t_{P L Z}$ and $t_{P Z L}, S_{1}$ is tied to $V_{C C}$. When measuring $t_{P H Z}$ and $t_{P Z H}$, $\mathrm{S}_{1}$ is tied to ground.
When measuring propagation delay times of three-state outputs, $S_{1}$ is open, i.e., not connected to $V_{C C}$ or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: $\mathrm{PRR} \leq 1 \mathrm{MHz}, \mathrm{t}_{\mathrm{r}} \leq 6 \mathrm{~ns}$, $\mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}, Z_{\text {out }}=50 \Omega$.

# 8-Bit Latches/Registers with ReadbackAdvanced CMOS-TTL Compatible 74ACT793 74ACT794 

## Features/Benefits

- I/O port configuration enables output data back onto input bus
- Low quiescent supply current of $<\mathbf{1 0} \mu \mathrm{A}$ (typical)
- Eighth bits matches byte boundaries
- Ideal for microprocessor interface
- Wide commercial operating supply and temperature ranges 4.5 V to $5.5 \mathrm{~V} ;-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$


## Description

These 8-bit latches/registers are useful for I/O operations on a microprocessor bus. An image of the output data can be read back by the CPU. This operation is important in control algorithms which make decisions based on the previous status of output controls. Rather than storing a redundant copy of the output data in memory, simply reading the register as an I/O port allows the data to be retrieved from where it has been stored in an ACT793/4, for verification and/or updating.


The data is loaded in the registers on the low-to-high transition of the clock (CK), for the ACT794. The data is passed through the ACT793 when the gate, (G), is High, and it is "latched" when G changes to Low. The output enable, $\overline{\mathrm{OE}}$ is used to enable data on D7-D0. When $\overline{\mathrm{OE}}$ is low the output of the latches/registers is enabled on D0-D7, enabling $D$ as an outut bus so that the host can perform a read operation. When $\overline{\mathrm{OE}}$ is High, D7-D0 are inputs to the latches/registers configuring $D$ as an input bus.
The output drive of these commercial parts for any output pin is $\mathrm{I}_{\mathrm{OL}}=12 \mathrm{~mA}$.

## 'ACT793 Function Table

| G | $\overline{O E}$ | Q | D |
| :---: | :---: | :---: | :---: |
| L | L | $Q_{0}{ }^{* *}$ | Output, 0 |
| L | H | $Q_{0}{ }^{* *}$ | Input |
| $\mathrm{H}^{\dagger}$ | L | $\mathrm{D}^{*}$ | Output, Q* |
| H | H | D | Input |

[^76]
## Ordering Information

| PART <br> NUMBER | PKG | TEMP | POLARITY | TYPE | TECH |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 74ACT793 | N,J | Com | Non- | Latch | NMOS |
| 74ACT794 | N,J | Com | invert | Register |  |

## Logic Symbols


'ACT794

'ACT794 Function Table

| CK | $\overline{O E}$ | Q | D |
| :---: | :---: | :---: | :---: |
| L or H or Lor Hor $\dagger$ | $\begin{aligned} & \mathrm{L} \\ & \mathrm{H} \\ & \mathrm{~L} \\ & \mathrm{H} \end{aligned}$ | $\begin{aligned} & Q_{0} \\ & Q_{0} \\ & Q_{0} \\ & D \end{aligned}$ | Output, Q Input Output, Q* Input |

[^77]
## Absolute Maximum Ratings

| Supply voltage, VCC | -0.5 V to 7.0 V |
| :---: | :---: |
| DC input voltage, $\mathrm{V}_{1}$ | -0.5 V to $\mathrm{V} \mathrm{CC}+0.5 \mathrm{~V}$ |
| DC output voltage, $\mathrm{V}_{\mathrm{O}}$ | -0.5 V to VCC +0.5 V |
| DC output source/sink current per output pin, IO | $\pm 35 \mathrm{~mA}$ |
| DC VCC or ground current, ICC or IGND | $\pm 100 \mathrm{~mA}$ |
| Input diode current, lik: |  |
| $\mathrm{V}_{1}<0$ | -20 mA |
| $\mathrm{V}_{1}>\mathrm{V}_{C C}$ | +20 mA |
| Output diode current, IOK: |  |
| $\mathrm{V}_{\mathrm{O}}<0$ | -20 mA |
| $\mathrm{V}_{\mathrm{O}}>\mathrm{V}_{\mathrm{CC}}$ | . +20 mA |
| Storage temperature | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

## Operating Conditions

| SYMBOL | PARAMETER |  | MIN | COMMERCIAL TYP | MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{CC}}$ | Supply voltage |  | 4.5 | 5 | 5.5 | V |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -40 |  | 85 | ${ }^{\circ} \mathrm{C}$ |
| $t_{w}$ | Width of Clock/Gate | High | 15 |  |  | ns |
|  |  | Low | 15 |  |  |  |
| $t_{\text {su }}$ | Setup time | 'ACT793 | 81 |  |  | ns |
|  |  | 'ACT794 | 251 |  |  |  |
| $t^{\prime}$ | Hold time | 'ACT793 | 81 |  |  |  |
|  |  | 'ACT794 | 01 |  |  |  |
| $\mathrm{t}_{\mathrm{r}}$ | Input rise time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  | 0 |  | 500 | ns |
| $\mathrm{t}_{\mathrm{f}}$ | Input fall time at $\mathrm{V}_{1}=4.5 \mathrm{~V}$ |  | 0 |  | 500 | ns |
| ${ }^{\mathrm{OH}}$ | High-level output current |  |  |  | -6 | mA |
| ${ }^{1} \mathrm{OL}$ | Low-level output current |  |  |  | 12 | mA |

$1 \downarrow$ The arrows indicates the transition of the clock/gate input used for reference. $\uparrow$ for the low-to-high transitions, $\downarrow$ for the high-to-low transitions.

Electrical Characteristics over Operating Conditions

| SYMBOL | PARAMETER | TEST CONDITIONS |  | MIN | COMMERCIAL TYP <br> MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  |  | 2 |  | V |
| IN | Input current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $\mathrm{V}_{1}=\mathrm{V}_{\mathrm{CC}}$ or GND |  | $\pm 1.0$ | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | Low-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $\mathrm{I}^{\mathrm{OL}}=20 \mu \mathrm{~A}$ |  | 0.1 | V |
|  |  |  | $\mathrm{l}^{\mathrm{OL}}=6 \mathrm{~mA}$ |  | 0.37 |  |
|  |  |  | $\mathrm{I}^{\mathrm{OL}}=12 \mathrm{~mA}$ |  | 0.4 |  |
| $\mathrm{V}_{\mathrm{OH}}$ | High-level output voltage | $\begin{aligned} & V_{C C}=M I N \\ & V_{I L}=M A X \\ & V_{I H}=M I N \end{aligned}$ | $1 \mathrm{OH}=-20 \mu \mathrm{~A}$ | 3.4 |  | V |
|  |  |  | $\mathrm{IOH}=-6 \mathrm{~mA}$ | 2.4 |  |  |
| l OZ | Off-state output current | $V_{C C}=M A X$ | $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{CC}}$ or GND |  | $\pm 30$ | $\mu \mathrm{A}$ |
| ${ }^{\text {I C }}$ | Quiescent supply current | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ | $V_{1}=v_{\text {CC }}$ or GND |  | 80 | $\mu \mathrm{A}$ |

## Switching Characteristics for 'ACT793

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveform) | MIN | COMMERCIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPLH }}$ | Data to output delay | $C_{L}=50 \mathrm{pF}$ |  | 40 | ns |
| ${ }_{\text {tPHL }}$ |  |  |  | 40 | , |
| ${ }_{\text {tPLH }}$ | Gate to output delay |  |  | - 40 | ns |
| $\mathrm{t}_{\mathrm{PHL}}$ |  |  |  | 40 |  |
| ${ }^{\text {P P ZL }}$ | Output enable delay $\dagger$ | $\begin{aligned} & \mathrm{R}_{\mathrm{L}}=1 \mathrm{~K} \Omega \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | 30 | ns |
| ${ }_{\text {tPZH }}$ |  |  |  | 30 |  |
| ${ }^{\text {tPLZ }}$ | Output disable delay $\dagger$ |  |  | 33 | ns |
| ${ }_{\text {t }}$ |  |  |  | 33 |  |

$\dagger$ For the 'ACT793, G should remain LOW during these tests.

## Switching Characteristics for 'ACT7 94

| SYMBOL | PARAMETER | TEST CONDITIONS (See Test Load/Waveform) | MIN | COMMERCIAL <br> MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ${ }^{\text {tPLH }}$ | Clock to output delay | $C_{L}=50 \mathrm{pF}$ |  | 40 | ns |
| ${ }^{\text {tPHL }}$ |  |  |  | 40 |  |
| ${ }_{\text {t }}^{\text {PZL }}$ | Output enable delay | $\begin{aligned} & R_{\mathrm{L}}=1 \mathrm{~K} \Omega \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \end{aligned}$ |  | 30 | ns |
| ${ }^{\text {tPZH }}$ |  |  |  | 30 |  |
| tpLZ | Output disable delay |  |  | 30 | ns |
| tPHZ |  |  |  | 30 |  |

## 'ACT793 Timing Diagrams



[^78]
## Enable/Disable Waveforms



## Standard Test Load



Notes 1. $\mathrm{C}_{\mathrm{L}}$ includes probbe and jig capacitance.
2. When measuring $t_{P L Z}$ and $t_{P Z L}, S_{1}$ is tied to $V_{C C}$. When measuring $t_{P H Z}$ and $t_{P Z H}$, $S_{1}$ is tied to ground.
When measuring propagation delay times of three-state outputs, $S_{1}$ is open, i.e., not connected to $\mathrm{V}_{\mathrm{CC}}$ or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.
4. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
5. All input pulses are supplied by generators having the following characteristics: PRR $\leq 1 \mathrm{MHz}, \mathrm{t}_{\mathrm{r}} \leq 5 \mathrm{~ns}$, $\mathrm{t}_{\mathrm{f}} \leq 6 \mathrm{~ns}, \mathrm{Z}_{\text {out }}=50 \mathrm{\Omega}$.

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## ECL10KH Selection Guide

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|  | NOR Gate |  |  |
| MC10H102 | Quad 2-Input |  |  |
| MC10H211 | Dual 3-Input, 3-Output |  |  |
|  | OR Gate |  |  |
| MC10H103 | Quad 2-Input |  |  |
| MC10H210 | Dual 3-Input, 3-Output |  |  |
|  | AND Gates |  |  |
| MC10H104 | Quad AND |  |  |
|  | Complex Gates |  |  |
| MC10H101 | Quad OR/NOR |  |  |
| MC10H105 | Triple 2-3-2 Input OR/NOR |  |  |
| MC10H107 | Triple Exclusive OR/NOR |  |  |
| MC10H109 | Dual 4-5 Input OR/NOR |  |  |
| MC10H117 | Dual 2-Wide OR-AND/OR-AND Invert |  |  |
| MC10H118 | Dual 2-Wide 3-Input OR/AND |  |  |
| MC10H121 | 4-Wide OR-AND/OR-AND Invert |  |  |
|  | Translators |  |  |
| MC10H124 | Quad TTL/ECL |  |  |
| MC10H125 | Quad ECL/TTL |  |  |
|  | Receivers |  |  |
| MC10H115 | Quad Line Receiver |  |  |
| MC10H116 | Triple Line Receiver |  |  |
|  | Flip-FLop Latches | J, N | 16 |
| MC10H130 | Dual latch |  |  |
| MC10H131 | Dual D Master Slave Flip-FLop |  |  |
| MC10H175 | Quint Latch |  |  |
| MC10H176 | Hex D-Flip-Flop |  |  |
|  | Parity Checker |  |  |
| MC10H160 | 12-Bit Parity Generator-Checker |  |  |
|  | Encoders/Decodes |  |  |
| MC10H161 | Binary to 1-8 (Low) |  |  |
| MC10H162 | Binary to 1-8 (High) |  |  |
|  | Data Selector Multiplexer |  |  |
| MC10H158 | Quad 2-Input Multiplexers (Non-inverting) |  |  |
| MC10H159 | Quad 2-Input Multiplexers (Inverting) |  |  |
| MC10H164 | 8-Line Multiplexer |  |  |
| MC10H173 | Quad 2-Input Multiplexer Latch |  |  |
| MC10H174 | Dual 4-1 multiplexer |  |  |
|  | Counters |  |  |
| MC10H016 | Binary Counter |  |  |
| MC10H136 | Universal Hexadecimal |  |  |
|  | Arithmetic Functions |  |  |
| MC10H179 | Lookahead Carry Block |  |  |
|  | Special Functions |  |  |
| MC10H141 | Universal Shift Register |  |  |
| MC10H166 | 5-Bit Magnitude Comparator |  |  |

# ECL 10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H016 <br> 4-Bit Binary Counter 

## Features/Benefits

- Counting frequency, 200 MHz min.
- Power dissipation 570 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H016 is a high-speed synchronous, presettable, cascadable 4-bit Binary Counter. This device is a member of Monolithic Memories' new ECL 10KH family. It is useful for a large number of conversion, counting, and digital integration applications.

## Pin Configuration

MC10H016 4-bit Binary Counter


MC10H016


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC 10 H 016 | $\mathrm{~J}, \mathrm{~N}, \mathrm{NL}$ | Com |

Function Select Table

| $\overline{\mathbf{C E}}$ | $\overline{\text { PE }}$ | MR | $\mathbf{C P}$ | FUNCTION |
| :---: | :---: | :---: | :---: | :--- |
| $L$ | $L$ | $L$ | $Z$ | Load parallel $\left(P_{n}\right.$ to $\left.Q_{n}\right)$ |
| $H$ | $L$ | $L$ | $Z$ | Load parallel $\left(P_{n}\right.$ to $\left.Q_{n}\right)$ |
| $L$ | $H$ | $L$ | $Z$ | Count |
| $H$ | $H$ | $L$ | $Z$ | Hold |
| $X$ | $X$ | $L$ | $Z Z$ | Masters respond; <br> slaves hold |
| $X$ | $X$ | $H$ | $X$ | Reset $\left(Q_{n}=\right.$ LOW, <br> $\left.T_{C}=H I G H\right)$ |

Z = Clock Pulse (Low to High)
ZZ = Clock Pulse (High to Low).
Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

## Logic Diagram

 achieved internally without incurring a full gate delay.

## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{E E}$ | Supply voltage |  | -5.46 | -5.2 | -4.94 | V |
| ${ }^{\text {T }}$ A | Operating temperature range |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| ${ }^{\text {T }}$ STG | Storage Temperature Range | Plastic | -55 |  | 150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 |  | 165 |  |

## Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} E$ | Power supply current |  | - | 126 | - | 115 | - | 126 | mA |
| $\mathrm{I}_{\mathrm{inH}}$ | Input current HIGH | All except MR | - | 450 | - | 265 | - | 265 | $\mu \mathrm{A}$ |
|  |  | Pin 12 MR | - | 1190 | - | 700 | - | 700 |  |
| $\mathrm{I}_{\mathrm{inL}}$ | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $\mathrm{V}_{\text {IL }}$ | Low input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathrm{V}_{\mathrm{EE}}=5.2 \mathrm{~V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{t} \mathrm{pd}$ | Propagation delay | Clock to Q | 1.0 | 2.4 | 1.0 | 2.5 | 1.0 | 2.7 | ns |
|  |  | Clock to TC | 0.7 | 2.4 | 0.7 | 2.5 | 0.7 | 2.6 |  |
|  |  | MR to Q | 0.7 | 2.4 | 0.7 | 2.5 | 0.7 | 2.6 |  |
| $t_{\text {set }}$ | Setup time | Pn to Clock | 2.0 | - | 2.0 | - | 2.0 | - | ns |
|  |  | CE or PE to Clock | 2.5 | - | 2.5 | - | 2.5 | - |  |
| $t^{\text {thold }}$ | Hold time | Clock to Pn | 1.0 | - | 1.0 | - | 1.0 | - | ns |
|  |  | Clock to CE or PE | 0.5 | - | 0.5 | - | 0.5 | - |  |
| ${ }^{\text {c }}$ count | Counting frequency |  | 200 | - | 200 | - | 200 | - | MHz |
| $\mathrm{tr}_{\mathrm{r}}, \mathrm{t}+$ | Rise time |  | 0.5 | 2.0 | 0.5 | 2.1 | 0.5 | 2.2 | ns |
| $\mathrm{t}_{\mathrm{f},} \mathrm{t}$ - | Fall time |  | 0.5 | 2.0 | 0.5 | 2.1 | 0.5 | 2.2 | ns |

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

## ECL 10KH High Speed <br> Emitter Coupled Logic Family MC10H100 <br> Quad 2-Input NOR Gate with Strobe

## Features/Benefits

- Propagation delay, 1 ns typical
- 25 mW typical/gate (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The M10H100 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Quad 2-Input NOR Gate with Strobe. This device is a functional/pinout duplication of the standard ECL 10K family part, with $100 \%$ improvement in propagation delay and no increase in power supply current.

## Pin Configuration

## MC10H100

Quad 2-Input NOR Gate with Strobe

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H100 | J, N, NL | Com |

## Logic Diagram

MC10H100


MC10H100


## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERC MIN TYP | IAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{E E}$ | Supply voltage |  | $-5.46-5.20$ | -4.94 | V |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range |  | 0 | 75 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 | 150 | C |
|  |  | Ceramic | -55 | 165 |  |

Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| IE | Power supply current |  | - | 29 | - | 26 | - | 29 | mA |
| linH | Input current HIGH | Pin 9 | - | 900 | - | 560 | - | 560 | $\mu \mathrm{A}$ |
|  |  | All other pins | - | 500 | - | 310 | - | 310 |  |
| 1 inL | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{1 \mathrm{H}}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $\mathrm{V}_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

Switching Characteristics $\mathbf{V}_{\text {EE }}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\text {tpd }}$ | Propagation delay | Pin 9 | 0.65 | 1.6 | 0.7 | 1.7 | 0.7 | 1.8 | ns |
|  |  | All other pins | 0.4 | 1.3 | 0.45 | 1.35 | 0.5 | 1.5 |  |
| $\mathrm{tr}_{\mathrm{r}}$ | Rise time ( $20 \%-80 \%$ ) |  | 0.5 | 2.0 | 0.5 | 2.1 | 0.5 | 2.2 | ns |
| $\mathrm{tf}^{\text {f }}$ | Fall time (80\%-20\%) |  | 0.5 | 2.0 | 0.5 | 2.1 | 0.5 | 2.2 | ns |

Note: Each ECL. 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50-\Omega$ resistor to -2.0 V .

# ECL10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H101 <br> Quad OR/NOR Gate 

## Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible.


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H101 | J,N,NL(20) | Com |

## Description

The MC10H101 is a member of Monolithic Memories' ECL family. This ECL 10 KH part is a functional/pinout duplication of the standard ECL 10 K family part, with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Pin Configurations

MC10H101
Quad OR/NOR Gate


MC10H101


MC10H101 Quad OR/NOR Gate

Absolute Maximum Ratings
Supply voltage $\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)$ ..... -8.0 to $0 \mathrm{~V}_{\mathrm{dc}}$
Input voltage $\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=0\right.$ ) ..... $0 V_{d c}$ to $V_{E E}$
Output Current:
Continuous ..... 50 mA
Surge. ..... 100 mA

## Operating Conditions



## Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathrm{V} \pm \mathbf{5 \%}$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | 25 ${ }^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $I_{E}$ | Power supply current |  | - | 29 | - | 26 | - | 29 | mA |
| linH | Input current high | MC10H101 | - | 425 | - | 265 | - | 265 | $\mu \mathrm{A}$ |
|  |  | MC10H101 (Pin 12 only) | - | 850 | - | 535 | - | 535 |  |
| $\mathrm{l}_{\text {inL }}$ | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $\mathrm{V}_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathbf{V E E}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{t} \mathrm{pd}$ | Propagation delay | All others | 0.5 | 1.45 | 0.5 | 1.5 | 0.5 | 1.6 | ns |
|  |  | 12 Pin | 0.5 | 1.6 | 0.5 | 1.6 | 0.5 | 1.7 |  |
| $t_{r},{ }^{+}$ | Rise time |  | 0.5 | 2.1 | 0.5 | 2.2 | 0.5 | 2.3 | ns |
| $t_{f}, t-$ | Fall time |  | 0.5 | 2.1 | 0.5 | 2.2 | 0.5 | 2.3 | ns |

Note: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

# ECL 10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H103 <br> Quad 2-Input OR Gate 

## Features/Benefits

- Propagation delay, 1.0 ns typical
- Power dissipation 25 mW/gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K compatible


## Description

The MC10H103 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H103 | J,N,NL(20) | Com |

## Logic Diagram

MC10H103
Quad 2-Input OR Gate

Absolute Maximum Ratings
Input voltage $V_{1}\left(V_{C C}=0\right)$ ..... $O \mathrm{~V}_{\mathrm{dc}}$ to $\mathrm{V}_{\mathrm{EE}}$Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

## Operating Conditions

| SYMBOL |  | PARAMETER | COMMERCIAL MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| $V_{\text {EE }}$ | Supply voltage |  | $\begin{array}{llll}-5.46 & -5.2 & -4.94\end{array}$ | $V$ |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range |  | $0 \quad 75$ | ${ }^{\circ} \mathrm{C}$ |
|  | S | Plastic | -55 150 |  |
| T | Storage temperature range | Ceramic | -55 165 | C |

## Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} \mathrm{E}$ | Power supply current | - | 29 | - | 26 | - | 29 | mA |
| 1 inH | Input current HIGH | - | 425 | - | 265 | - | 265 | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\mathrm{inL}}$ | Input current LOW | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $\mathrm{V}_{\text {IL }}$ | LOW input voltage | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathbf{V E E}^{\mathbf{E}}=-\mathbf{5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\text {p }}$ d | Propagation delay | 0.4 | 1.3 | 0.4 | 1.3 | 0.4 | 1.45 | ns |
| $t_{r},{ }^{\text {t }}$ | Rise time ( $20 \%-80 \%$ ) | 0.5 | 1.7 | 0.5 | 1.8 | 0.5 | 1.9 | ns |
| $t_{f},{ }_{\text {t }}$ | Fall time ( $80 \%-20 \%$ ) | 0.5 | 1.7 | 0.5 | 1.8 | 0.5 | 1.9 | ns |

Note: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

## ECL 10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H102/Quad 2-Input NOR Gate <br> MC10H105/Triple 2-3-2 Input OR/NOR Gate

## Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation $25 \mathrm{~mW} /$ gate
- Noise margin 150 mV
- Voltage compensated
- ECL 10K compatible.


## Description

The MC10H102 and MC10H105 are members of Monolithic Memories new ECL family. These ECL 10KH parts are functional/ pinout duplications of the standard ECL 10K family parts, with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Pin Configurations

MC10H102
Quad 2-Input NOR Gate


MC10H105
Triple 2-3-2 Input OR/NOR Gate

| $\mathrm{vccl}_{1}$ | 16] $\mathrm{v}_{\text {cc2 }}$ |
| :---: | :---: |
| $A_{\text {out }} 2$ | $15 \mathrm{c}_{\text {out }}$ |
| $\overline{A_{\text {out }}} 3$ | $14 \overline{C o u t}^{\text {col }}$ |
| $A_{i n 1} 4$ | $13 \mathrm{c} \mathrm{c}_{\mathrm{in} 2}$ |
| $A_{\text {in2 }} 5$ | ${ }^{12} c_{i n 1}$ |
| $B_{\text {out }} 6$ | 11] $\mathrm{B}_{\mathrm{in} 3}$ |
| $B_{\text {out }} 7$ | ${ }^{10} \mathrm{~B}_{\mathrm{in} 2}$ |
| $\mathrm{v}_{\mathrm{EE}} \mathrm{B}^{1}$ | 9] $\mathrm{B}_{\mathrm{in} 1}$ |

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H102 | J,N,NL(20) | Com |
| $M C 10 \mathrm{H} 105$ |  |  |

## Logic Diagrams

## MC10H102



Quad 2-Input NOR Gate

MC10H105


Triple 2-3-2 input OR/NOR Gate

MC10H102


MC10H105


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## Absolute Maximum Ratings



Output Current:
Continuous
.50 mA
Surge
100 mA

## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL <br> MIN |  |
| :--- | :--- | :--- | :--- | :--- |
|  |  |  | UNIT |  |

Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} E$ | Power supply current | MC10H102 | - | 29 | - | 26 | - | 29 | mA |
|  |  | MC10H105 | - | 23 | - | 21 | - | 23 |  |
| $\mathrm{l}_{\mathrm{inH}}$ | Input current HIGH |  | - | 425 | - | 265 | - | 265 | $\mu \mathrm{A}$ |
| $\mathrm{l}_{\mathrm{inL}}$ | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $\mathrm{V}_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathbf{V E E}^{\mathbf{E}}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\text {tpd }}$ | Propagation delay | MC10H102 | 0.4 | 1.25 | 0.4 | 1.25 | 0.4 | 1.4 | ns |
|  |  | MC10H105 | 0.4 | 1.2 | 0.4 | 1.2 | 0.4 | 1.3 |  |
| $t_{r},{ }^{+}$ | Rise time | MC10H102 | 0.5 | 1.5 | 0.5 | 1.6 | 0.55 | 1.7 | ns |
|  |  | MC10H105 | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 |  |
| $t_{f}, t-$ | Fall time | MC10H102 | 0.5 | 1.5 | 0.5 | 1.6 | 0.55 | 1.7 | ns |
|  |  | MC10H105 | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 |  |

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

# ECL 10KH High Speed <br> Emitter Coupled Logic Family <br> MC10H106 <br> Triple 4-3-3 Input NOR Gate 

## Features/Benefits

- Propagation delay, 1 ns typical
- 36 mW typical/gate (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The M10H106 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Triple 4-3-3 Input NOR Gate. This device is a functional/pinout duplication of the standard ECL 10 K family part, with $100 \%$ improvement in propagation delay and no increase in power supply current.

## Pin Configuration

## MC10H106

Triple 4-3-3 Input NOR Gate


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H106 | $\mathrm{J}, \mathrm{N}, \mathrm{NL}$ | Com |

## Logic Diagram

MC10H106


$$
\begin{aligned}
\text { VCC1 } & =\text { PIN } 1 \\
\text { VCC2 } & =\text { PIN } 16 \\
\text { VEE } & =\text { PIN } 8
\end{aligned}
$$

MC10H106


## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL MIN TYP MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: |
| $V_{E E}$ | Supply voltage |  | $-5.46-5.20-4.94$ | V |
| TA | Operating temperature range |  | $0 \quad 75$ | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 165 |  |

## Electrical Characteristics $\mathbf{V E E}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| IE | Power supply current | - | 23 | - | 21 | - | 23 | mA |
| linH | Input current HIGH | - | 500 | - | 310 | - | 310 | $\mu \mathrm{A}$ |
| l inL | Input current LOW | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| V OH | HIGH output voltage | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage | -1.17 | -0.84 | $-1.13$ | -0.81 | -1.07 | -0.735 | Vdc |
| $V_{\text {IL }}$ | LOW input voltage | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathrm{V}_{\text {EE }}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

|  | PARAMETER | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $\mathrm{t}_{\mathrm{pd}}$ | Propagation delay | 0.5 | 1.3 | 0.5 | 1.5 | 0.55 | 1.55 | ns |
| $t_{r}$ | Rise time (20\%-80\%) | 0.5 | 1.7 | 0.5 | 1.8 | 0.55 | 1.9 | ns |
| $\mathrm{tf}_{f}$ | Fall time (80\%-20\%) | 0.5 | 1.7 | 0.5 | 1.8 | 0.55 | 1.9 | ns |

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50-\Omega$ resistor to -2.0 V .

# ECL 10KH High-Speed <br> Emitter-Coupled Logic Family MC10H104/MC10H107 <br> ,Quad 2-Input AND Gate/Triple 2-Input Exclusive OR/NOR Gate 

## Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation $35 \mathrm{~mW} /$ gate typical
- Noise margin $\mathbf{1 5 0} \mathbf{~ m V}$
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H104 and MC10H107 are members of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Pin Configurations

MC10H104
Quad 2-Input AND Gate


MC10H107
Triple 2-Input Exclusive OR/NOR Gate


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H104 <br> $M C 10 H 107$ | J,N,NL(20) | Com |

## Logic Diagrams

## MC10H104



VCC1 $=$ PIN 1 VCC2 $=$ PIN 16 VEE $=$ PIN 8

MC10H107


VCC1 $=$ PIN 1
VCC2 $=$ PIN 16 VEE $=$ PIN 8 PIN $6=$ NC


MC10H107


## MC10H104 MC1OH107

## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| $V_{E E}$ | Supply Voltage |  | -5.46 | -5.2 | -4.94 | V |
| $T_{\text {A }}$ | Operating temperature range |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 |  | 150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 |  | 165 |  |

## Electrical Characteristics $\mathrm{VEE}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} \mathrm{E}$ | Power supply current | MC10H104 MC10H107 | - | $\begin{aligned} & 39 \\ & 31 \end{aligned}$ | - | $\begin{aligned} & 35 \\ & 28 \end{aligned}$ | - | $\begin{aligned} & 39 \\ & 31 \end{aligned}$ | mA |
| $\mathrm{l}_{\mathrm{inH}}$ | Input current HIGH |  | - | 425 | - | 265 | - | 265 | $\mu \mathrm{A}$ |
| 1 inL | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | 0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | $-1.60$ | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | $-0.735$ | Vdc |
| $V_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

Switching Characteristics $\mathbf{V E E}_{\mathbf{E E}}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\text {p }}$ d | Propagation delay | MC10H104 | 0.4 | 1.6 | 0.45 | 1.75 | 0.45 | 1.9 | ns |
|  |  | MC10H107 | 0.4 | 1.5 | 0.4 | 1.6 | 0.4 | 1.7 |  |
| $t_{\mathbf{r}},{ }^{\text {t }}$ | Rise time | MC10H104 | 0.5 | 1.6 | 0.5 | 1.7 | 0.5 | 1.8 | ns |
|  |  | MC10H107 | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 |  |
| $t_{f}, t^{-}$ | Fall time | MC10H104 | 0.5 | 1.6 | 0.5 | 1.7 | 0.5 | 1.8 | ns |
|  |  | MC10H107 | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 |  |

[^80]
# ECL 10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H109 <br> Dual 4-5 Input OR/NOR Gate 

## Features/Benefits

- Propagation delay, 1 ns typical
- Power dissipation $35 \mathrm{~mW} /$ gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H109 is a member of Monolithic Memories' new ECL family. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10K family parts with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC 10 H 109 | $\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)$ | Com |

## Logic Diagram

## Pin Configuration

MC10H109
Dual 4-5 Input OR/NOR Gate


MC10H109


Absolute Maximum Ratings
Power supply $\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)$ ..... 8.0 V to 0 Vdc
Input voltage $\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=0\right)$ 0 Vdc to $\mathrm{V}_{\mathrm{EE}}$
Output current
Continuous ..... 50 mA
Surge ..... 100 mA

## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | TYP | MAX |  |
| $V_{\text {EE }}$ | Supply Voltage |  | -5.46 | -5.2 | -4.94 | V |
| ${ }^{T}$ A | Operating temperature range |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 |  | 150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 |  | 165 |  |

## Electrical Characteristics $\mathbf{V E E}_{\text {EE }}=-\mathbf{5 . 2} \mathbf{V} \pm \mathbf{5 \%}$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} \mathrm{E}$ | Power supply current | MC10H109 | - | 15 | - | 14 | - | 15 | mA |
| 1 inH | Input current HIGH |  | - | 425 | - | 265 | - | 265 | $\mu \mathrm{A}$ |
| 1 inL | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | 0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage |  | -1.17 | -0.84 | $-1.13$ | -0.81 | -1.07 | -0.735 | Vdc |
| $\mathrm{V}_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathbf{V E E}_{\text {EE }}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

|  | PARAMETER | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| tpd | Propagation delay | 0.4 | 1.3 | 0.4 | 1.3 | 0.45 | 1.45 | ns |
| $t_{r},{ }^{\text {t }}$ | Rise time | 0.5 | 2.0 | 0.5 | 2.1 | 0.5 | 2.2 | ns |
| $t_{f}, t-$ | Fall time | 0.5 | 2.0 | 0.5 | 2.1 | 0.5 | 2.2 | ns |

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

## Quad Line Receiver

## Features/Benefits

- Propagation delay 1.0 ns typical
- Power dissipation, 175 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H115 is a Quad Differential Amplifier designed for use in sensing double-ended signals over long lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part, with $100 \%$ improvement in counting frequency and no increase in power-supply current.

## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H115 | J,N,NL(20) | Com |

## Application Information

The base bias supply ( $\mathrm{V}_{\mathrm{BB}}$ ) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necesary. Active current sources provide the MC10H115 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to VBB (pin 9) to prevent upsetting the current source bias network.

## Logic Diagram

MC10H115

$V_{C C 1}=$ PIN 1
$V_{C C 2}=$ PIN 16
$V_{E E}=$ PIN 8

[^81]Absolute Maximum Ratings

Input voltage $\mathrm{V}_{\mathrm{I}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)$ 0 Vdc to $\mathrm{V}_{\mathrm{EE}}$Output Current:
Continuous 50 mA
Surge ..... 100 mA

## Operating Conditions



Electrical Characteristics $\mathbf{V E E}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} \mathrm{E}$ | Power supply current | - | 29 | - | 26 | - | 29 | mA |
| $\mathrm{I}_{\mathrm{inH}}$ | Input current HIGH | - | 150 | - | 95 | - | 95 | $\mu \mathrm{A}$ |
| ${ }^{\text {I CBO }}$ | Input leakage current | - | 1.5 | - | 1.0 | - | 1.0 | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $V_{\text {IL }}$ | LOW input voltage | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |
| $\mathrm{V}_{\mathrm{BB}}$ | Reference voltage | -1.42 | -1.28 | -1.35 | -1.23 | -1.295 | -1.15 | Vdc |

## Switching Characteristics $\mathbf{V E E}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }_{\text {t }}^{\text {pd }}$ | Propagation delay | 0.4 | 1.3 | 0.4 | 1.3 | 0.45 | 1.45 | ns |
| $t_{r},{ }^{+}$ | Rise time | 0.5 | 1.4 | 0.5 | 1.5 | 0.5 | 1.6 | ns |
| $t_{f}, t^{\prime}$ | Fall time | 0.5 | 1.4 | 0.5 | 1.5 | 0.5 | 1.6 | ns |

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V.

## ECL 10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H116 <br> Triple Line Receiver

## Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 85 mW typ/pkg
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H116 is a Triple Line Receiver. This device is a member of Monolithic Memories' new ECL family. It is a functional/pinout duplication of the standard ECL 10K family part with $100 \%$ improvement in propagation delay and no increase in power-supply current.

## Pin Configuration

MC10H116
Triple Line Receiver


MC10H116


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H116 | J,N,NL(20) | Com |

## Application Information

The MC10H116 is designed to be used in sensing differential signals over long lines. The bias supply ( $\mathrm{V}_{\mathrm{BB}}$ ) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.
Active current sources provide these receivers with excellent common-mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to $V_{B B}$ to prevent unbalancing the current-source bias network.
The MC10H116 does not have internal-input pull-down resistors. This provides high impedance to the amplifier input and facilitates differential connections.
Typical applications:

- Low level receiver
- Schmitt trigger
- Voltage level interface


## Logic Diagram

MC10H116

$\mathbf{v}_{\text {CC1 }}=$ PIN 1
$\mathbf{V}_{\mathbf{C C} 2}=$ PIN 16
$\mathbf{V}_{\text {EE }}=$ PIN 8

Portions of this data sheet reproduced with the courtesy of Motorola Inc.


## Operating Conditions

| SYMBOL |  | PARAMETER | COMMERCIAL <br> MIN | UNIT |
| :--- | :--- | :--- | :--- | :---: |
| $V_{\text {EE }}$ | Supply voltage |  | -5.46 | -5.2 |

## Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V}+5 \%$ (See Note)

| SYMBOL | PARAMETER | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} \mathrm{E}$ | Power supply current | - | 23 | - | 21 | - | 23 | mA |
| $\mathrm{l}_{\mathrm{inH}}$ | Input current HIGH | - | 150 | - | 95 | - | 95 | $\mu \mathrm{A}$ |
| ${ }^{\text {I CBO }}$ | Input leakage current | - | 1.5 | - | 1.0 | - | 1.0 | $\mu \mathrm{A}$ |
| $V_{B B}$ | Reference voltage | -1.37 | -1.25 | -1.35 | -1.23 | -1.31 | -1.19 | Vdc |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage | -1.95 | $-1.63$ | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{1 \mathrm{H}}$ | HIGH input voltage (1) | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $V_{\text {IL }}$ | LOW input voltage (1) | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |
| $\mathrm{V}_{\text {CMR }}$ | Common mode range (3) | - | - | -2.85 | -0.8 | - | - | Vdc |
| $V_{\text {PP }}$ | Input sensitivity (4) | - | - | 150 typ |  | - | - | mVPP |

## Switching Characteristics $\mathbf{V E E}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $\mathrm{t}_{\mathrm{pd}}$ | Propagation delay | 0.4 | 1.3 | 0.4 | 1.3 | 0.45 | 1.45 | ns |
| $t_{r},{ }^{\text {t }}$ | Rise time | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 | ns |
| $t_{f}, t-$ | Fall time | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 | ns |

Notes: 1. When $V_{B B}$ is used as the reference voltage.
2. Each ECL 10KH series circuit has been designed to meet the specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50-\Omega$ resistor to $\mathbf{- 2 . 0} \mathrm{V}$.
3. Differential input not to exceed 1.0 Vdc .
4. Differential input required to obtain full logic swing on output.

# ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H117 <br> Dual 2-Wide 2-3 Input <br> OR-AND/OR-AND-INVERT Gate 

## Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, $100 \mathrm{~mW} / \mathrm{gate}$ typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H117 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2 wide 2-3 input OR-AND/OR-AND-INVERT gate designed for use in data distribution and as a data controller for digital multiplexers.
This general purpose logic element is a functional pinout duplication of the standard ECL 10 K part, with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Pin Configurations

MC10H117
Dual 2-Wide 2-3 Input
OR-AND/OR-AND-Invert Gate


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H117 | J,N,NL(20) | Com |

## Logic Diagram

MC10H117


## Absolute Maximum Ratings



## Operating Conditions



Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} E$ | Power supply current |  | - | 29 | - | 26 | - | 29 | mA |
| l inH | Input current HIGH | Pins 3,4,5, 12,13,14 | - | 465 | - | 275 | - | 275 | $\mu \mathrm{A}$ |
|  |  | Pin 6,7,10,11 | - | 545 | - | 320 | - | 320 |  |
|  |  | Pin 9 | - | 710 | - | 415 | - | 415 |  |
| $\mathrm{l}_{\mathrm{inL}}$ | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | $V_{\text {dc }}$ |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | $\mathrm{V}_{\mathrm{dc}}$ |
| $\mathrm{V}_{\text {IH }}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | $\mathrm{V}_{\mathrm{dc}}$ |
| $\mathrm{V}_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | $\mathrm{V}_{\mathrm{dc}}$ |

Switching Characteristics $\mathrm{V}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| tpd | Propagation delay | 0.45 | 1.35 | 0.45 | 1.35 | 0.5 | 1.5 | ns |
| $t_{r},{ }^{\text {t }}$ | Rise time | 0.5 | 1.50 | 0.5 | 1.6 | 0.5 | 1.7 | ns |
| $t_{f}, t-$ | Fall time | 0.5 | 1.50 | 0.5 | 1.6 | 0.5 | 1.7 | ns |

Note: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V.

## Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, $100 \mathrm{~mW} /$ Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H118 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a Dual 2-Wide 3-Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10 K part with $100 \%$ improvement in propagation delay and no increase in power supply current.

## Pin Configurations

MC10H118
Dual 2-Wide 3-Input OR-AND Gate


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H118 | $J, N, N L(20)$ | Com |

## Logic Diagram

MC10H118
Dual 2-Wide
3-Input OR-AND Gate

Absolute Maximum Ratings
Supply voltage $\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)$ ..... -8.0 V to 0 Vdc
Input voltage $\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=0\right)$ 0 Vdc to $\mathrm{V}_{\mathrm{EE}}$Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

## Operating Conditions

| SYMBOL | PARAMETER |  | $\begin{aligned} & \text { COM } \\ & \text { MIN } \end{aligned}$ | MER <br> TYP | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {EE }}$ | Supply voltage |  | -5.46 | -5.2 | -4.94 | V |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 |  | 150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 | . | 165 |  |

Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} \mathrm{E}$ | Power supply current |  | - | 29 | - | 26 | - | 29 | mA |
| $\operatorname{linH}$ | Input current HIGH | Pins 3,4,5,12,13,14 | - | 465 | - | 275 | - | 275 | $\mu \mathrm{A}$ |
|  |  | Pins 6,7,10,11 | - | 545 | - | 320 | - | 320 |  |
|  |  | Pin 9 | - | 710 | - | 415 | - | 415 |  |
| l inL | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| VOH | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\text {IH }}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $V_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

Switching Characteristics $\mathrm{VEE}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| $t_{\text {pd }}$ | Propagation delay | 0.5 | 1.6 | 0.5 | 1.7 | 0.55 | 1.85 | ns |
| $t_{\text {r }},{ }^{\text {t }}$ | Rise time | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 | ns |
| $\mathrm{t}_{\mathrm{f}}, \mathrm{t}-$ | Fall time | 0.5 | 1.5 | 0.5 | 1.6 | 0.5 | 1.7 | ns |

Note: Each ECL. 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50-\Omega$ resistor to -2.0 V .

# ECL 10KH High-Speed <br> Emitter Coupled Logic Family <br> MC10H119 <br> 4-Wide 4-3-3-3 Input OR-AND Gate 

## Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, $100 \mathrm{~mW} /$ Gate typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H119 is a member of Monolithic Memories' ECL 10KH family. This ECL device is a 4-Wide 4-3-3-3 Input OR-AND Gate. It is a functional pinout duplication of the standard ECL 10K part with 100\% improvement in propagation delay and no increase in power supply current.

## Pin Configurations

MC10H119
4-Wide 4-3-3-3 Input OR-AND Gate


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H119 | $\mathrm{J}, \mathrm{N}, \mathrm{NL}(20)$ | Com |

## Logic Diagram

MC10H119
4-Wide 4-3-3-3 Input OR-AND Gate


## Absolute Maximum Ratings



## Operating Conditions

| SYMBOL | PARAMETER |  | COMMERCIAL |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{V}_{\mathrm{EE}}$ | Supply voltage |  | -5.46 | -5.2 | -4.94 | V |
| ${ }^{T}$ A | Operating temperature range |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 |  | 150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 |  | 165 |  |

Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} E$ | Power supply current |  | - | 29 | - | 26 | - | 29 | mA |
| linH | Input current HIGH | $\begin{gathered} \text { Pins } 3,4,5,6,7,9,11 \\ 12,13,14,15 \end{gathered}$ | - | 500 | - | 295 | - | 295 | $\mu \mathrm{A}$ |
|  |  | Pin 10 | - | 610 | - | 360 | - | 360 |  |
| l inL | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| VOH | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| VOL | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\text {IH }}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $V_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

## Switching Characteristics $\mathrm{V}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathrm{V}, \pm \mathbf{5 \%}$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\text {t }}$ pd | Propagation delay | All others | 0.7 | 2.0 | 0.75 | 2.0 | 0.8 | 2.15 | ns |
|  |  | Pin 10 | 0.75 | 2.2 | 0.75 | 2.25 | 0.8 | 2.35 |  |
| $t_{r}, t+$ | Rise time |  | 0.7 | 2.4 | 0.7 | 2.3 | 0.7 | 2.4 | ns |
| $t_{f}, t-$ | Fall time |  | 0.7 | 2.4 | 0.7 | 2.3 | 0.7 | 2.4 | ns |

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

## ECL 10KH High-Speed Emitter-Coupled Logic Family <br> MC10H121 <br> 4-Wide OR-AND/OR-AND-INVERT Gate

## Features/Benefits

- Propagation delay 1 ns typical
- Power dissipation, 145 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC1OH121 is a 4-Wide OR-AND/OR-AND-INVERT Gate. This device is a member of Monolithic Memories' new ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K family part with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Pin Configuration

MC10H121
4-Wide OR-AND/OR-AND-INVERT Gate


MC10H121


## Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H121 | $\mathrm{J}, \mathrm{N}, \mathrm{NL}$ | Com |

## Logic Diagram

MC10H121


## Absolute Maximum Ratings



Operating Conditions

| SYMBOL | PARAMETER |  | COM | MER TYP | CIAL MAX | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {EE }}$ | Supply voltage |  | -5.46 | -5.2 | -4.94 | V |
| $\mathrm{T}_{\text {A }}$ | Operating temperature range |  | 0 |  | 75 | ${ }^{\circ} \mathrm{C}$ |
| TSTG | Storage temperature range | Plastic | -55 |  | +150 | ${ }^{\circ} \mathrm{C}$ |
|  |  | Ceramic | -55 |  | +165 |  |

## Electrical Characteristics $\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{\prime} E$ | Power supply current |  | - | 29 | - | 26 | - | 29 | mA |
| $\mathrm{I}_{\mathrm{inH}}$ | Input current HIGH | Pins 4-7, 9, 11-15 | - | 500 | - | 295 | - | 295 | $\mu \mathrm{A}$ |
|  |  | Pin 10 | - | 610 | - | 360 | - | 360 |  |
| $\mathrm{l}_{\mathrm{inL}}$ | Input current LOW |  | 0.5 | - | 0.5 | - | 0.3 | - | $\mu \mathrm{A}$ |
| $\mathrm{V}_{\mathrm{OH}}$ | HIGH output voltage |  | -1.02 | -0.84 | -0.98 | -0.81 | -0.92 | -0.735 | Vdc |
| $\mathrm{V}_{\mathrm{OL}}$ | LOW output voltage |  | -1.95 | -1.63 | -1.95 | -1.63 | -1.95 | -1.60 | Vdc |
| $\mathrm{V}_{\mathrm{IH}}$ | HIGH input voltage |  | -1.17 | -0.84 | -1.13 | -0.81 | -1.07 | -0.735 | Vdc |
| $V_{\text {IL }}$ | LOW input voltage |  | -1.95 | -1.48 | -1.95 | -1.48 | -1.95 | -1.45 | Vdc |

Switching Characteristics $\mathrm{V}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%$ (See Note)

| SYMBOL | PARAMETER |  | $0{ }^{\circ}$ |  | $25^{\circ}$ |  | $75^{\circ}$ |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | MAX | MIN | MAX | MIN | MAX |  |
| ${ }^{t} \mathrm{pd}$ | Propagation delay | All others | 0.55 | 1.95 | 0.6 | 2.0 | 0.7 | 2.40 | ns |
|  |  | Pin 10 | 0.45 | 1.8 | 0.45 | 1.8 | 0.55 | 2.2 |  |
| $t_{r},{ }^{+}$ | Rise time |  | 0.5 | 1.7 | 0.5 | 1.8 | 0.5 | 1.9 | ns |
| $\mathrm{t}_{\mathrm{f}}, \mathrm{t}$ - | Fall time |  | 0.5 | 1.7 | 0.5 | 1.8 | 0.5 | 1.9 | ns |

Note: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

# ECL 10KH High-Speed <br> Emitter-Coupled Logic Family <br> MC10H124 <br> Quad TTL-to-ECL Translator 

## Features/Benefits

- Propagation delay 1.5 ns typical
- Power dissipation 520 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible


## Description

The MC10H124 is a Quad TTL-to-ECL translator. This device is a member of Monolithic Memories' new ECL family. This quad translator is used for interfacing data and control signals between a saturated logic section and the ECL section of digital systems. The 10 KH part is a functional/pinout duplication of the standard ECL 10K family part, with $100 \%$ improvement in propagation delay, and no increase in power-supply current.

## Pin Configuration

MC10H124
Quad TTL-to-ECL Translator


MC10H124


Ordering Information

| PART NUMBER | PACKAGE | TEMPERATURE |
| :---: | :---: | :---: |
| MC10H124 | J, N, NL | Com |

## Application Information

The MC10H124 has TTL-compatible inputs and ECL complementary open-emitter outputs that allow use as an inverting/ non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to an ECL low logic state and all inverting outputs to an ECL high logic state.
An advantage of this device is that TTL-level information can be transmitted differentially, via balanced twisted-pair lines, to ECL equipment, where the signal can be received by the MC 10 H 115 or MC 10 H 116 differential line receivers. The power supply requirements are ground, +5.0 volts, and -5.2 volts.

## Logic Diagram



[^82]14-33

## Absolute Maximum Ratings

```Supply voltage \(\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right)\)-8.0 V to 0 Vac
Supply voltage, VCC (VEE = -5.2 V) ........................................................................... 0 0 to +7.0 Vdc
```



```
Output Current:
    Continuous
Surge ..... 100 mA

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & \multicolumn{3}{|l|}{COMMERCIAL} & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[t]{2}{*}{Storage temperature range} & Plastic & -55 & & +150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & - & +165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathbf{V}_{E E}=-5.2 \mathrm{~V} \pm 5 \% \mathbf{V}_{\mathbf{C C}}=5.0 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Negative power supply drain current} & - & 72 & - & 66 & - & 72 & mA \\
\hline \({ }^{1} \mathrm{CCH}\) & \multicolumn{2}{|l|}{\multirow[t]{2}{*}{Positive power supply drain current*}} & - & 16 & - & 16 & - & 18 & mA \\
\hline \({ }^{1} \mathrm{CCL}\) & & & - & 25 & - & 25 & - & 25 & mA \\
\hline \multirow[b]{2}{*}{\({ }^{1} \mathrm{H}\)} & \multirow[t]{2}{*}{Input current HIGH
\[
\left(\mathrm{V}_{1}=2.4 \mathrm{~V}\right)
\]} & Pin 6 & - & 200 & - & 200 & - & 200 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 5, 7, 10, 11 & - & 50 & - & 50 & - & 50 & \\
\hline \multirow{2}{*}{IIL} & \multirow[t]{2}{*}{Input current LOW
\[
\left(V_{1}=0.4 \mathrm{~V}\right)
\]} & Pin 6 & - & -12.8 & - & -12.8 & - & -12.8 & \multirow{2}{*}{mA} \\
\hline & & Pins 5, 7, 10, 11 & - & -3.2 & - & -3.2 & - & -3.2 & \\
\hline \(I_{L}\) & \multicolumn{2}{|l|}{Input breakdown current ( \(\mathrm{V}_{\text {in }}=5.5 \mathrm{~V}\) )} & - & 1.0 & - & 1.0 & - & 1.0 & mA \\
\hline \(V_{\text {IC }}\) & \multicolumn{2}{|l|}{\[
\begin{array}{r}
\text { Input clamp voltage }(-10 \mathrm{~mA}, \text { pins } 5,7,10,11) \\
\\
\hline(-20 \mathrm{~mA}, \operatorname{pin} 6) \\
\hline
\end{array}
\]} & - & -1.5 & - & -1.5 & - & -1.5 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & 2.0 & - & 2.0 & - & 2.0 & - & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & - & 0.8 & - & \(0: 8\) & - & 0.8 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathbf{V}, \pm \mathbf{5 \%}\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline tpd & Propagation delay & 0.55 & 2.25 & 0.55 & 2.4 & 0.85 & 2.95 & ns \\
\hline \(t_{r},{ }^{\text {t }}\) & Rise time & 0.5 & 1.5 & 0.5 & 1.6 & 0.5 & 1.70 & ns \\
\hline \(t_{f}, t-\) & Fall time & 0.5 & 1.5 & 0.5 & 1.6 & 0.5 & 1.70 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
* ICCH - Current drain from VCC power supply with all inputs at Logic HIGH level

ICCL - Current drain from VCC power supply with all inputs at Logic LOW level.

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H125 Quad ECL-to-TTL Translator
}

\section*{PRELIMINARY INFORMATION}

This document contains specifications and information which are subject to change.

\section*{Features/Benefits}
- Propagation delay, 2.5 ns typical
- Power Dissipation 520 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H125 is a member of Monolithic Memories' ECL family. The MC 10 H 125 is a quad translator for interfacing data and control signals between the ECL section and TTL compatible section of digital systems. The 10KH part is a functional/ pinout duplication of the standard ECL 10K family part, with \(100 \%\) improvement in propagation delay, and no increase in powersupply current.

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H125 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Application Information}

The MC10H125 incorporates differential inputs and Schottky TTL "totem pole" outputs. The differential inputs don't have input pull-down and allow for use as an inverting/non-inverting translator or as a differential line receiver. The \(\mathrm{V}_{\mathrm{BB}}\) reference voltage is available from Pin 1 for use in single-ended input biasing. The outputs of the MC10H125 go to a low logic level whenever the inputs are left floating.
An advantage of this device is that ECL-level information can be received via balanced twisted pair lines in the TTL equipment. This isolates the ECL-logic from the noisy TTL environment. Power supply requirements are ground, +5.0 volts and -5.2 volts.

\section*{Logic Diagram}

MC10H125
Quad ECL-to-TTL
Translator


\section*{Absolute Maximum Ratings}
\begin{tabular}{|c|}
\hline Power supply \(\mathrm{VEE}^{\left(\mathrm{V}_{\mathrm{CC}}+5.0\right.}\) \\
\hline Power Supply \(\mathrm{V}_{\mathrm{CC}}\left(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V}\right)\) \\
\hline Input voltage \(\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right)\) \\
\hline
\end{tabular}

Operating Conditions
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline & \multicolumn{2}{|c|}{\multirow[b]{2}{*}{PARAMETER}} & & MMER & & \\
\hline SYMBOL & & & MIN & TYP & MAX & UNIT \\
\hline \(\mathrm{V}_{\text {EE }}\) & Supply Voltage & & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow{2}{*}{TSTG} & \multirow{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathbf{V} \pm \mathbf{5} \%, \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|l|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} E\) & \multicolumn{2}{|l|}{Negative power supply drain current} & - & 44 & - & 40 & - & 44 & mAdc \\
\hline \({ }^{1} \mathrm{CCH}\) & \multirow[b]{2}{*}{Positive power supply drain current} & Outputs \(=\mathrm{H}\) & - & 63 & - & 63 & - & 63 & \\
\hline \({ }^{1} \mathrm{CCL}\) & & Outputs \(=\mathrm{L}\) & - & 40 & - & 40 & - & 40 & \\
\hline 1 inH & \multicolumn{2}{|l|}{Input current} & - & 225 & - & 145 & - & 145 & \(\mu\) Adc \\
\hline \({ }^{\text {I CBO }}\) & \multicolumn{2}{|l|}{Input leakage current} & - & 1.5 & - & 1.0 & - & 1.0 & \(\mu \mathrm{Adc}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH output voltage & \(\mathrm{l}_{\mathrm{OH}}=-1 \mathrm{~mA}\) & 2.5 & - & 2.5 & - & 2.5 & - & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & \(\mathrm{I}^{\mathrm{OL}}=+20 \mathrm{~mA}\) & - & 0.5 & - & 0.5 & - & 0.5 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(V_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline IOS & \multicolumn{2}{|l|}{Short circuit current} & 60 & 150 & 60 & 150 & 60 & 150 & mAdc \\
\hline \(\mathrm{V}_{\mathrm{BB}}\) & \multicolumn{2}{|l|}{Reference voltage} & -1.37 & -1.25 & -1.35 & -1.23 & -1.31 & -1.19 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathrm{V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow[b]{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow[b]{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline tpd & Propagation delay* & 0.8 & 3.3 & 0.85 & 3.35 & 0.9 & 3.4 & ns \\
\hline \(t_{r},{ }^{\text {t }}+\) & Rise time & 0.3 & 1.2 & 0.3 & 1.2 & 0.3 & 1.2 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}}, \mathrm{t}\) - & Fall time & 0.3 & 1.2 & 0.3 & 1.2 & 0.3 & 1.2 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
* Drives a \(25-\mathrm{pF}\) load.

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family Dual Latch MC10H130
}

\section*{Features/Benefits}
- Propagation delay, 1 ns typical
- Power dissipation, 155 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H130 is a dual latch which has two different mechanisms to retain data through latch control signals. Each latch can be operated separately by holding the common latch control signal ( \(\overline{\mathrm{C}})\) LOW, then switching an individual latch control signal ( \(\overline{\mathrm{CE}} 1 / \overline{\mathrm{CE}}\) ) from LOW to HIGH to cause retention of data in the relevant latch. If simultaneous operation of both latches is required, \(\overline{\mathrm{CE}}\) and \(\overline{\mathrm{CE}}\) are held LOW and the common latch control \(C\) is switched from LOW to HIGH.
For either latch, data present at the inputs (D1/D2) will be seen at the outputs (Q1/Q1 and Q2/Q2) when both latch control signals are LOW. This condition allows data to be setup within the latch, after which time causing a positive transition to the HIGH state on either or both latch control signals causes data retention. After either or both of these signals are HIGH, subsequent changes in data at an input are ignored by the latch, provided the hold time requirement is met.

An alternative means to load data in the latches is to use the direct set and reset (S1/S2 and R1/R2, respectively) lines. These inputs do not override the latch controls, or the D inputs. Instead, set or reset are only effective when either \(\overline{\mathrm{C}}, \overline{\mathrm{CE}} / \overline{\mathrm{CE} 2}\) or both, are HIGH. Note that this relationship is different than the case for a similar part, the MC10H131, which is a Dual Master-Slave D-type Flip-Flop.

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|}
\hline \(\mathbf{D}\) & \(\overline{\text { C }}\) & \(\overline{\text { CE1/CE2 }}\) & R & \(\boldsymbol{S}\) & \(\mathbf{Q}_{n=1}\) \\
\hline\(L\) & \(L\) & \(L\) & \(X\) & \(X\) & \(L\) \\
\hline\(H\) & \(L\) & \(L\) & \(X\) & \(X\) & \(H\) \\
\hline\(X\) & \(H\) & \(X\) & \(L\) & \(L\) & \(Q_{n}\) \\
\hline\(X\) & \(H\) & \(X\) & \(L\) & \(H\) & \(H\) \\
\hline\(X\) & \(H\) & \(X\) & \(H\) & \(L\) & \(L\) \\
\hline\(X\) & \(H\) & \(X\) & \(H\) & \(H\) & \(N . D\). \\
\hline\(X\) & \(X\) & \(H\) & \(L\) & \(L\) & \(Q_{n}\) \\
\hline\(X\) & \(X\) & \(H\) & \(L\) & \(H\) & \(H\) \\
\hline\(X\) & \(X\) & \(H\) & \(H\) & \(L\) & \(L\) \\
\hline\(X\) & \(X\) & \(H\) & \(H\) & \(H\) & N.D. \\
\hline
\end{tabular}

\footnotetext{
\(X=\) Don't Care
N.D. Not Defined
}

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline MC10H130 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}


\section*{Pin Configurations}


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\section*{Absolute Maximum Ratings}
\begin{tabular}{|c|c|}
\hline Supply voltage \(\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)\) & -8.0 V to \(0 \mathrm{~V}_{\mathrm{dc}}\) \\
\hline Input voltage \(\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=0\right)\). & \(O V_{d c}\) to \(V_{E E}\) \\
\hline Output Current: & \\
\hline Continuous & . 50 mA \\
\hline Surge. & . 100 mA \\
\hline
\end{tabular}

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|c|}{PARAMETER} & \[
\begin{aligned}
& \text { COM! } \\
& \text { MIN }
\end{aligned}
\] & \[
\begin{aligned}
& \text { MMER } \\
& \text { TYP }
\end{aligned}
\] & CIAL MAX & UNIT \\
\hline VEE & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline TA & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{\(\mathrm{T}_{\text {stg }}\)} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 38 & - & 35 & - & 38 & mA \\
\hline \multirow{3}{*}{\(\mathrm{I}_{\mathrm{inH}}\)} & \multirow{3}{*}{Input current HIGH} & Pins 6, 11 & - & 468 & - & 275 & - & 275 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 7, 9, 10 & - & 545 & - & 320 & - & 320 & \\
\hline & & Pins 4, 5, 12, 13 & - & 434 & - & 255 & - & 255 & \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & \(-0.84\) & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & \(-1.63\) & -1.95 & -1.60 & Vdc \\
\hline \(V_{\text {IH }}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{V E E}^{\mathbf{E}} \mathbf{- 5 . 2} \mathbf{V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{3}{*}{\({ }^{t} \mathrm{pd}\)} & \multirow{3}{*}{Propagation delay} & Data & 0.40 & 1.60 & 0.40 & 1.70 & 0.40 & 1.80 & \multirow{3}{*}{ns} \\
\hline & & Set, Reset & 0.60 & 1.70 & 0.70 & 1.80 & 1.80 & 1.90 & \\
\hline & & Clock, CE & 0.50 & 1.60 & 0.50 & 1.70 & 1.70 & 1.80 & \\
\hline \(\mathrm{t}_{\mathrm{r}}, \mathrm{t}^{+}\) & \multicolumn{2}{|l|}{Rise time ( \(20 \%-80 \%\) )} & 0.5 & 1.6 & 0.5 & 1.7 & 0.5 & 1.8 & ns \\
\hline \(\mathrm{t}_{\mathrm{f},}, \mathrm{t}\) & \multicolumn{2}{|l|}{Fall time ( \(80 \%-20 \%\) )} & 0.5 & 1.6 & 0.5 & 1.7 & 0.5 & 1.8 & ns \\
\hline \(\mathrm{t}_{\text {set }}\) & \multicolumn{2}{|l|}{Setup time} & 0.5 & 1.6 & 0.5 & 1.7 & 0.5 & 1.8 & ns \\
\hline \(t_{\text {hold }}\) & \multicolumn{2}{|l|}{Hold time} & 0.5 & 1.6 & 0.7 & - & 0.7 & - & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.
The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated
through a \(50 \Omega\) resistor to -2.0 V .

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H131 \\ Dual Master-Slave Type D Flip-Flop
}

\section*{Features/Benefits}
- Propagation delay, 1 ns typical
- Power dissipation, 235 mW typical
- Noise margin of \(\mathbf{1 5 0} \mathbf{~ m V}\)
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H131 is a member of Monolithic Memories' ECL family. The MC10H131 is a dual master-slave D-type flip-flop. Asynchronous Set ( S ) and Reset ( R ) override Clock ( \(\mathrm{C}_{\mathrm{C}}\) ) and Clock Enable ( \(\overline{\mathrm{CE}}\) ) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking fuction. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.
The output states of the flip-flop change on the positive transition of the controlling input(s). A change in the information present at the data (D) input will not affect the data output at any other time due to master slave construction.

This ECL 10 KH part is a functional/pinout duplication of the standard ECL 10 K family part, with \(100 \%\) improvement in clock speed and propagation delay and no increase in power supply current.

\section*{Function Tables}

R-S TRUTH TABLE
\begin{tabular}{|c|c|c|}
\hline\(R\) & \(s\) & \(Q_{n}+\mathbf{1}\) \\
\hline\(L\) & \(L\) & \(Q_{n}\) \\
\hline\(L\) & \(H\) & \(H\) \\
\hline\(H\) & \(H\) & \(L\) \\
\hline\(H\) & \(N\) & \(N . D\). \\
\hline
\end{tabular}
N.D. \(=\) Not Defined.

CLOCKED TRUTH TABLE
\begin{tabular}{|c|c|c|}
\hline\(C\) & \(D\) & \(Q_{n}+1\) \\
\hline\(L\) & \(X\) & \(Q_{n}\) \\
\hline\(H \dagger\) & \(L\) & \(L\) \\
\hline\(H \dagger\) & \(H\) & \(H\) \\
\hline
\end{tabular}
\(\mathrm{X}=\) Don't Care.
\(\mathrm{C}=\overline{\mathrm{CE}}+\mathrm{C}_{\mathrm{C}}\).

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline MC10H131 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}


\section*{Pin Configurations}

MC10H131
Dual Master-Slave Type D Flip-Flop
MC10H131


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\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & & PARAMETER & CON & MERC
TYP & CIAL MAX & UNIT \\
\hline \(\mathrm{V}_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{\({ }^{\text {T STG }}\)} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(V_{E E}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|l|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} E\) & \multicolumn{2}{|l|}{Power supply current} & - & 62 & - & 56 & - & 62 & mA \\
\hline \multirow{4}{*}{\(\mathrm{linH}^{\text {in }}\)} & \multirow[t]{4}{*}{Input current HIGH} & Pins 6, 11 & - & 530 & - & 310 & - & 310 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pin 9 & - & 660 & - & 390 & - & 390 & \\
\hline & & Pins 7, 10 & - & 485 & - & 285 & - & 285 & \\
\hline & & Pins 4, 5, 12, 13 & - & 790 & - & 465 & - & 465 & \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IL}}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\({ }^{\text {tpd }}\)} & \multirow[b]{2}{*}{Propagation delay} & Clock, \(\overline{\mathrm{CE}}\) & 0.80 & 1.6 & 0.8 & 1.7 & 0.8 & 1.8 & \multirow[b]{2}{*}{ns} \\
\hline & & Set, Reset & 0.6 & 1.6 & 0.7 & 1.7 & 0.7 & 1.8 & \\
\hline \(t_{r}, t+\) & \multicolumn{2}{|l|}{Rise time (20\%-80\%)} & 0.6 & 2.0 & 0.6 & 2.0 & 0.6 & 2.2 & ns \\
\hline \(t_{f}, t-\) & \multicolumn{2}{|l|}{Fall time ( \(80 \%-20 \%\) )} & 0.6 & 2.0 & 0.6 & 2.0 & 0.6 & 2.2 & ns \\
\hline \(\mathrm{t}_{\text {set }}\) & \multicolumn{2}{|l|}{Setup time} & 0.7 & - & 0.7 & - & 0.7 & - & ns \\
\hline thold & \multicolumn{2}{|l|}{Hold time} & 0.8 & - & 0.8 & - & 0.8 & - & ns \\
\hline \(\mathrm{t}_{\text {tog }}\) & \multicolumn{2}{|l|}{Toggle frequency} & 250 & - & 250 & - & 250 & - & MHz \\
\hline
\end{tabular}

\footnotetext{
Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.
The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
}

\section*{Switching Time Comparison ECL 10 KH versus ECL 10K}


CLOCK то \(\bar{Q}\)



NOTE: \(\quad t_{r}\) and \(t_{f}\) measured from the \(20 \%\) to the \(80 \%\) level of the output signal swing. \(\mathrm{t}_{\mathrm{pd}}\) is measured from the \(50 \%\) level of the input to the \(50 \%\) level of the output.

\section*{ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H136 \\ Universal Hexadecimal Counter}

\section*{Features/Benefits}
- Counting frequency, 250 MHz min.
- Power dissipation, 715 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H136 is a high-speed synchronous hexadecimal counter. This device is a member of Monolithic Memories' new ECL 10KH family. This 10 KH part is a functional/pinout duplication of the standard ECL 10K family part, with \(100 \%\) improvement in propagation delay, and no increase in power-supply current.

\section*{Pin Configuration}

MC10H136
Universal Hexadecimal Counter


MC10H136


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC 10 H 136 & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}\) & Com \\
\hline
\end{tabular}

\section*{Application Information}

The MC10H136 is a high-speed synchronous counter that operates at 250 MHz . Counter operating modes include count up, count down, preset and hold count. This device allows the designer to use one basic counter for many applications.
The \(\mathrm{S}_{1}, \mathrm{~S}_{2}\) control lines determine the operating modes of the counter. In the preset mode, a clock pulse is necessary to load the counter with the information present on the data inputs ( \(D_{0}\), \(D_{1}, D_{2}\) and \(D_{3}\) ). Carry out goes low on the terminal counter or when the counter is being preset.

Function Select Table
\begin{tabular}{|c|c|l|}
\hline \(\mathbf{S}_{\mathbf{1}}\) & \(\mathbf{S}_{\mathbf{2}}\) & \multicolumn{1}{|c|}{ OPERATING MODE } \\
\hline L & L & Preset (Program) \\
\hline L & H & Increment (Count up) \\
\hline\(H\) & L & Decrement (Count down) \\
\hline\(H\) & \(H\) & Hold (Stop count) \\
\hline
\end{tabular}

\footnotetext{
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}

\section*{Logic Diagram}


Sequential Truth Table*
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{8}{|c|}{INPUTS} & \multicolumn{6}{|c|}{OUTPUTS} \\
\hline \(S_{1}\) & \(\mathrm{S}_{2}\) & \(\mathrm{D}_{0}\) & \(\mathrm{D}_{1}\) & \(\mathrm{D}_{2}\) & \(\mathrm{D}_{3}\) & CARRY IN & \[
\begin{aligned}
& \text { CLOCK } \\
& v_{\mathrm{IL}} \sqrt{v_{\mathrm{IH}}}
\end{aligned}
\] & \(Q_{0}\) & \(Q_{1}\) & \(Q_{2}\) & \(\mathrm{Q}_{3}\) & CARRY OUT & SELECT MODE \\
\hline L & L & L & L & H & H & X & \(\checkmark\) & L & L & H & H & L & Preset \\
\hline L & H & X & X & X & X & L & \(\Gamma\) & H & L & H & H & H & Increment \\
\hline L & H & X & X & X & X & L & \(\int\) & L & H & H & H & H & Increment \\
\hline L & H & X & X & X & X & L & - & H & H & H & H & L & Increment \\
\hline L & H & X & X & X & X & H & 2 & H & H & H & H & H & Increment \\
\hline L & H & X & X & X & X & H & 5 & H & H & H & H & H & Increment \\
\hline H & H & X & X & X & X & X & \(\bigcirc\) & H & H & H & H & H & Hold \\
\hline L & L & H & H & L & L & X & 5 & H & H & L & L & L & Preset \\
\hline H & L & X & X & X & X & L & 5 & L & H & L & L & H & Decrement \\
\hline H & L & X & X & X & X & L & \(\checkmark\) & H & L & L & L & H & Decrement \\
\hline H & L & X & X & X & X & L & \(\checkmark\) & L & L & L & L & L & Decrement \\
\hline H & L & X & X & X & X & L & \(\int\) & H & H & H & H & H & Decrement \\
\hline
\end{tabular}

\footnotetext{
\(x=\) Don't care.
}
* Truth table shows logic states assuming that the inputs vary in sequence from top to bottom, as shown.

The states of the Q0-Q3 outputs are shown assuming the occurance of a L-to-H edge transition (e.g. after clocking).

\section*{Absolute Maximum Ratings}
\begin{tabular}{|c|c|}
\hline Supply voltage \(\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}\right)\) & -8.0 V to 0 Vdc \\
\hline Input voltage \(\mathrm{V}_{\mathrm{I}}\left(\mathrm{V}_{\mathrm{CC}}=0 \mathrm{~V}\right)\) & 0 Vdc to VEE \\
\hline Output Current: & \\
\hline Continuous & 50 mA \\
\hline Surge & 100 mA \\
\hline
\end{tabular}

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & \[
\begin{aligned}
& \text { COM } \\
& \text { MIN }
\end{aligned}
\] & \begin{tabular}{l}
MER \\
TYP
\end{tabular} & CIAL MAX & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & +150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & +165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathrm{V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 165 & - & 150 & - & 165 & mA \\
\hline \multirow{4}{*}{\(\mathrm{l}_{\mathrm{inH}}\)} & \multirow{4}{*}{Input current HIGH} & Pins 5, 6, 11, 12, 13 & - & 430 & - & 275 & - & 275 & \multirow{4}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pin 9 & - & 670 & - & 420 & - & 420 & \\
\hline & & Pin 7 & - & 535 & - & 335 & - & 335 & \\
\hline & & Pin 10 & - & 380 & - & 240 & - & 240 & \\
\hline \(\mathrm{l}_{\text {inL }}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The Circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{Switching Characteristics \(\mathbf{V E E}_{\text {EE }}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{3}{*}{\({ }^{\text {t }}\) d} & \multirow{3}{*}{Propagation delay} & Clock to Q & 0.7 & 2.3 & 0.7 & 2.4 & 0.7 & 2.5 & \multirow{3}{*}{ns} \\
\hline & & Clock to carry out & 1.0 & 4.8 & 1.0 & 4.9 & 1.0 & 5.0 & \\
\hline & & Carry in to carry out & 0.7 & 2.5 & 0.7 & 2.6 & 0.7 & 2.7 & \\
\hline \multirow{4}{*}{\(\mathrm{t}_{\text {set }}\)} & \multirow{4}{*}{Setup time} & Data (D0 to C) & 2.0 & - & 2.0 & - & 2.0 & - & \multirow{4}{*}{ns} \\
\hline & & Select (S to C) & 3.5 & - & 3.5 & - & 3.5 & - & \\
\hline & & Carry in (Cin to C) & 2.0 & - & 2.0 & - & 2.0 & - & \\
\hline & & Carry in (C to Cin) & 0 & - & 0 & - & 0 & - & \\
\hline \multirow{4}{*}{\(t_{\text {hold }}\)} & \multirow{4}{*}{Hold time} & Data (C to D0) & 0 & - & 0 & - & 0 & - & \multirow{4}{*}{ns} \\
\hline & & Select (C to S) & -0.5 & - & -0.5 & - & -0.5 & - & \\
\hline & & Carry in (C to Cin) & 0 & - & 0 & - & 0 & - & \\
\hline & & Carry in (Cin to C) & 2.2 & - & 2.2 & - & 2.2 & - & \\
\hline \(\mathrm{f}_{\text {count }}\) & \multicolumn{2}{|l|}{Counting frequency} & 250 & - & 250 & - & 250 & - & MHz \\
\hline \(\mathrm{tr}_{\mathrm{r}}, \mathrm{t}^{+}\) & \multicolumn{2}{|l|}{Rise time} & 0.5 & 2.3 & 0.5 & 2.4 & 0.5 & 2.5 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}, \mathrm{t}}\), & \multicolumn{2}{|l|}{Fall time} & 0.5 & 2.3 & 0.5 & 2.4 & 0.5 & 2.5 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H141 \\ Four-Bit Universal Shift Register}

\section*{PRELIMINARY INFORMATION}

This document contains specifications and information which are subject to change.

\section*{Features/Benefits}
- Shift frequency, 250 MHz min
- Power dissipation, 425 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H141 is a four-bit universal shift register which performs shift-left, or shift-right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control
(See following page)

\section*{Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{SELECT} & \multicolumn{4}{|c|}{OUTPUTS} & \multirow[t]{2}{*}{OPERATING MODE} \\
\hline S1 & S2 & Q0n-1 & Q1 \({ }_{\text {n-1 }}\) & Q2n-1 & Q3 \({ }_{\text {n-1 }}\) & \\
\hline L & L & D0 & D1 & D2 & D3 & Parallel entry \\
\hline L & H & Q1n & Q2 \({ }^{\text {n }}\) & Q3 \({ }^{\text {n }}\) & DR & Shift right* \\
\hline H & L & DL & Q0 \({ }_{\text {n }}\) & Q1n & Q2n & Shift left* \\
\hline H & L & Q0 \({ }_{\text {n }}\) & Q1n & Q2n & Q3 \({ }_{n}\) & Stop shift \\
\hline
\end{tabular}
* Outputs as exist after pulse appears at " \(C\) " input with input conditions as shown (Pulse Positive transition of clock input).

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H141 & J,N,NL(20) & Com \\
\hline
\end{tabular}

MC10H141
Four-Bit Universal Shift Register
MC10H141


\section*{Logic Diagram}


\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{PARAMETER}} & \multicolumn{3}{|c|}{MILITARY} & \multirow[t]{2}{*}{UNIT} \\
\hline SYMBOL & & & MIN & TYP & MAX & \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating free-air temperature} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{C} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 112 & - & 102 & - & 112 & mA \\
\hline \multirow{3}{*}{1 inH} & \multirow{3}{*}{Input current HIGH} & Pins 5, 6, 9, 11, 12, 13 & - & 405 & - & 255 & - & 255 & \multirow{3}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 7, 10 & - & 416 & - & 260 & - & 260 & \\
\hline & & Pins 4, & - & 510 & - & 320 & - & 320 & \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{1 \mathrm{H}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(V_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -0.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{V E E}^{\mathbf{E E}} \mathbf{= - 5 . 2} \mathbf{V}, \pm \mathbf{5 \%}\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \(\mathrm{t}_{\mathrm{pd}}\) & \multicolumn{2}{|l|}{Propagation delay} & 1.1 & 2.0 & 1.0 & 2.0 & 1.1 & 2.1 & ns \\
\hline \(t_{\text {hold }}\) & \multicolumn{2}{|l|}{Hold time} & 1.0 & - & 1.0 & - & 1.0 & - & ns \\
\hline \multirow[b]{2}{*}{\({ }^{\text {set }}\)} & \multirow[b]{2}{*}{Setup time} & Data & 1.5 & - & 1.5 & - & 1.5 & - & \multirow[b]{2}{*}{ns} \\
\hline & & Select & 3.0 & - & 3.0 & - & 3.0 & - & \\
\hline \(t_{r},{ }^{\text {t }}\) & \multicolumn{2}{|l|}{Rise time} & 0.5 & 2.4 & 0.5 & 2.4 & 0.5 & 2.4 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}, \mathrm{t}}\) - & \multicolumn{2}{|l|}{Fall time} & 0.5 & 2.4 & 0.5 & 2.4 & 0.5 & 2.4 & ns \\
\hline \(\mathrm{f}_{\text {shift }}\) & \multicolumn{2}{|l|}{Shift frequency} & 250 & - & 250 & - & 250 & - & MHz \\
\hline
\end{tabular}

NOTE: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{Description (Continued)}
the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift-left, shiftright, and parallel entry of data. The other six inputs are all data
type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR). This device is a functional/pinout duplication of the standard ECL 10 K part, with \(100 \%\) improvement in propagation delay and operation frequency and no increase in power supply current.

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H158 QUAD 2-Input Multiplexer
}

\section*{PRELIMINARY}

INFORMATION
This document contains specifications and information which are subject to change.

\section*{Features/Benefits}
- Propagation delay, 1.5 ns typical
- Power dissipation, 197 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-Compatible

\section*{Description}

The MC10H158 is a member of Monolithic Memories' ECL Family. The MC10H158 is a quad 2 -input multiplexer. When the select line (SELECT) is LOW D_1 data appear at the outputs (Q3-Q0). Conversely, when the select input is HIGH, D_0 data appear at the outputs. This ECL part is a functional/pinout duplication of the standard ECL 10K family part, with \(100 \%\) improvement in propagation delay and no increase in powersupply current.

\section*{MC10H158 Function Table}
\begin{tabular}{|c|c|c|c|}
\hline SELECT & D_0 \(^{*}\) & D_1 \(^{*}\) & \(\mathbf{Q}\) \\
\hline \hline\(L\) & \(X\) & \(L\) & \(L\) \\
\hline\(L\) & \(X\) & \(H\) & \(H\) \\
\hline\(H\) & \(L\) & \(X\) & \(L\) \\
\hline\(H\) & \(H\) & \(X\) & \(H\) \\
\hline
\end{tabular}
* D_0/D_1 indicate each of four bit positions for the "zero" or "one" inputs, as controlled by the select line.
X = Don't care.

\section*{Pin Configurations}

\section*{MC10H158}

Quad 2-Input Multiplexer


Ordering Information
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H158 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H158
Quad 2-Input Multiplexer



\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & CON & \[
\begin{aligned}
& \text { AMERC } \\
& \text { TYP }
\end{aligned}
\] & CIAL MAX & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply Voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[t]{2}{*}{TSTG} & \multirow[t]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathbf{V E E}_{\text {EE }}=\mathbf{- 5 . 2} \mathbf{V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \(I_{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 53 & - & 48 & - & 53 & mA \\
\hline \multirow[t]{2}{*}{linH} & \multirow[t]{2}{*}{Input current HIGH} & Pin 9 & - & 475 & - & 295 & - & 295 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 3-6 and 10-13 & - & 515 & - & 320 & - & 320 & \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{v}_{\mathrm{EE}}=-5.2 \mathrm{~V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\({ }^{\text {tpd }}\)} & \multirow[b]{2}{*}{Propagation delay} & Data & 0.5 & 1.9 & 0.5 & 1.9 & 0.5 & 2.0 & \multirow[b]{2}{*}{ns} \\
\hline & & Select & 1.0 & 2.9 & 1.0 & 2.9 & 1.0 & 2.9 & \\
\hline \(t_{r},{ }^{+}\) & Rise time & & 0.7 & 2.2 & 0.7 & 2.0 & 0.7 & 2.2 & ns \\
\hline \(t_{f}, \mathrm{t}\) - & Fall time & & 0.7 & 2.2 & 0.7 & 2.0 & 0.7 & 2.2 & ns \\
\hline
\end{tabular}

\footnotetext{
NOTES: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow. greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
}

\section*{ECL 10KH High-Speed \\ Emitter-Coupled Logic Family MC10H159 \\ Quad 2-Input Inverting Multiplexer with Enable}

\section*{Features/Benefits}
- Propagation delay, 1.5 ns typical
- Power dissipation, \(\mathbf{2 1 8 \text { mW typical }}\)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H159 is a member of Monolithic Memories' ECL family. The MC10H159 is a quad 2 -input inverting multiplexer with enable. A HIGH level on the enable input (ENABLE) overrides the select input (SELECT) and forces all of the outputs (Q3-Q0) to the LOW level. A LOW level on the enable input allows multiplexer action, which is controlled by the select input. When the select input is LOW, D_1 data appear at the outputs. Conversely, when the select input is HIGH, D_0 data appear at the outputs.

\section*{MC10H159 Function Table}
\begin{tabular}{|c|c|c|c|c|}
\hline ENABLE & SELECT & D_0* & D_1 \(^{*}\) & Q \\
\hline \hline L & L & X & L & H \\
\hline L & L & X & H & L \\
\hline L & H & L & X & H \\
\hline L & H & H & X & L \\
\hline H & X & X & X & L \\
\hline
\end{tabular}
* D_0/D_1 indicate each of 4 bit positions for the "zero" or "one" inputs, as controlled by the select line.
X = Don't care.

\section*{Pin Configurations}

\section*{MC10H159}

Quad 2-Input Inverting Multiplexer with Enable


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H159 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

\section*{MC10H159}

Quad 2-Input Inverting Multiplexer with Enable


MC10H159


\footnotetext{
Portions of this Data Sheet reproduced with the courtesy of Motorola, Inc.
}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{Absolute Maximum Ratings} \\
\hline Supply voltage \(\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)\) & -8.0 to \(0 V_{\text {dc }}\) \\
\hline Input voltage \(\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=0\right)\) & \(0 \mathrm{~V}_{\mathrm{dc}}\) to \(\mathrm{V}_{\mathrm{EE}}\) \\
\hline \multicolumn{2}{|l|}{Output Current:} \\
\hline Continuous & 50 mA \\
\hline Surge & 100 mA \\
\hline
\end{tabular}

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{3}{|l|}{\multirow[t]{2}{*}{COMMERCIAL}} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & & & MAX & \\
\hline \(\mathrm{V}_{\mathrm{EE}}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{C} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{VEE}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathrm{V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} E\) & \multicolumn{2}{|l|}{Power supply current} & - & 58 & - & 53 & - & 58 & mA \\
\hline \multirow{2}{*}{inH} & \multirow{2}{*}{Input current HIGH} & Pin 9 & - & 475 & - & 295 & - & 295 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 3-7 and 10-13 & & 515 & - & 320 & - & 320 & \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.75 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{v E E}=-\mathbf{5 . 2} \mathbf{V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{3}{*}{\({ }^{t} \mathrm{pd}\)} & \multirow{3}{*}{Propagation delay} & Data & 0.5 & 2.2 & 0.5 & 2.2 & 0.5 & 2.2 & \multirow{3}{*}{ns} \\
\hline & & Select & 1.0 & 3.2 & 1.0 & 3.2 & 1.0 & 3.2 & \\
\hline & & Enable & 1.0 & 3.2 & 1.0 & 3.2 & 1.0 & 3.2 & \\
\hline \(\mathrm{tr}_{\mathrm{r}}, \mathrm{t}^{+}\) & \multicolumn{2}{|l|}{Rise time} & 0.5 & 2.2 & 0.5 & 2.2 & 0.5 & 2.2 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}, \mathrm{t}}\) - & \multicolumn{2}{|l|}{Fall time} & 0.5 & 2.2 & 0.5 & 2.2 & 0.5 & 2.2 & ns \\
\hline
\end{tabular}

\footnotetext{
Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established.
} The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H160 12-Bit Parity Generator-Checker}

\section*{Features/Benefits}
- Propagation delay, 2.5 ns typical
- Power dissipation, \(\mathbf{3 2 0} \mathbf{~ m W}\) typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H160 is a member of Monolithic Memories' new ECL family. The MC10H160 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits. The MC10H160 is a functional/pin out duplication of the standard ECL 10K family part with \(100 \%\) improvement in propagation delay and no increase in power-supply current.

\section*{Pin Configuration}

MC10H160
12-Bit Parity Generator-Checker


MC10H160


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H160 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H160 12-Bit Parity Generator-Checker


Function Table
\begin{tabular}{|c|c|}
\hline \begin{tabular}{c} 
INPUT \\
SUM OF HIGH LEVEL INPUTS
\end{tabular} & \begin{tabular}{c} 
OUTPUT \\
PIN 2
\end{tabular} \\
\hline Even & LOW \\
\hline Odd & HIGH \\
\hline
\end{tabular}

\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & & CIAL MAX & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.4 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & +75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & +150 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & +165 & \\
\hline
\end{tabular}

Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 88 & - & 78 & - & 86 & mA \\
\hline \multirow[b]{2}{*}{linH} & \multirow[b]{2}{*}{Input current HIGH} & Pins 3,5,7,10, 12,14 & - & 391 & - & 246 & - & 246 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 4,6,9,11,13,15 & - & 457 & - & 285 & - & 285 & \\
\hline l inL & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & \(-0.735\) & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \(\mathrm{t}_{\mathrm{pd}}\) & Propagation delay & 1.1 & 3.1 & 1.1 & 3.3 & 1.2 & 3.5 & ns \\
\hline \(\mathrm{t}_{\mathrm{r}},{ }^{\text {t }}\) & Rise time & 0.55 & 1.5 & 0.55 & 1.6 & 0.75 & 1.7 & ns \\
\hline \(t_{f}, t-\) & Fall time & 0.55 & 1.5 & 0.55 & 1.6 & 0.75 & 1.7 & ns \\
\hline
\end{tabular}

\footnotetext{
Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
}

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family \\ MC10H161 \\ Binary to 1 -of-8 Decoder
}

\section*{Features/Benefits}
- Propagation delay, 1 ns typical
- Power dissipation, 315mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H161 is a high-speed Binary to 1-of-8 Decoder. This device is a member of Monolithic Memories' expanding ECL 10KH family. This ECL device is designed to decode a three-bit word to a one-of-eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.
The MC10H161 is a true parallel decoder. No series gating is used internally, eliminating unequal delay time found in other decoders. The MC10H161 is useful in high-speed multiplexer/ demultiplexer applications.

This ECL 10KH part is a functional/pinout duplication of the standard ECL 10 K part with \(100 \%\) improvement in propagation delay, and no increase in power-supply current.

\section*{Pin Configuration}

\section*{MC10H161}

Binary to 1-of-8 Decoder


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H161 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{2}{|l|}{ENABLE INPUTS} & \multicolumn{3}{|r|}{INPUTS} & \multicolumn{8}{|c|}{OUTPUTS} \\
\hline \(\overline{E_{1}}\) & E \({ }_{0}\) & C & B & A & \(\mathbf{Q}_{0}\) & \(Q_{1}\) & \(\mathbf{Q}_{2}\) & \(\mathbf{Q}_{3}\) & \(\mathbf{Q}_{4}\) & \(\mathrm{Q}_{5}\) & \(Q_{6}\) & \(Q_{7}\) \\
\hline L & L & L & L & L & L & H & H & H & H & H & H & H \\
\hline L & L & L & L & H & H & L & H & H & H & H & H & H \\
\hline L & L & L & H & L & H & H & L & H & H & H & H & H \\
\hline L & L & L & H & H & H & H & H & L & H & H & H & H \\
\hline L & L & H & L & L & H & H & H & H & L & H & H & H \\
\hline L & L & H & L & H & H & H & H & H & H & L & H & H \\
\hline L & L & H & H & L & H & H & H & H & H & H & L & H \\
\hline L & L & H & H & H & H & H & H & H & H & H & H & L \\
\hline H & X & X & X & X & H & H & H & H & H & H & H & H \\
\hline X & H & X & X & X & H & H & H & H & H & H & H & H \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H161

\(\mathbf{V C C 1}=\) PIN 1
\(V_{\text {CC2 }}=\) PIN 16
\(V_{E E}=\) PIN 8

\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & \[
\begin{aligned}
& \text { CON } \\
& \text { MIN }
\end{aligned}
\] & \[
\begin{aligned}
& \text { UMER } \\
& \text { TYP }
\end{aligned}
\] & CIAL MAX & UNIT \\
\hline \(\mathrm{V}_{\mathrm{EE}}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\text {C }}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{VEE}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & Power supply current & - & 84 & - & 76 & - & 84 & mA \\
\hline \(\mathrm{l}_{\text {inH }}\) & Input current HIGH & - & 465 & - & 275 & - & 275 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{I}_{\mathrm{inL}}\) & Input current LOW & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH output voltage & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & HIGH input voltage & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\text {IL }}\) & LOW input voltage & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{v e E}=\mathbf{- 5 . 2 V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{3}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\({ }^{t} \mathrm{pd}\)} & \multirow[b]{2}{*}{Propagation delay} & Data Pi & ns 7, 9, 14 & 0.6 & 2.0 & 0.65 & 2.1 & 0.7 & 2.2 & \multirow{2}{*}{ns} \\
\hline & & Enable & Pins 2, 15 & 0.8 & 2.3 & 0.8 & 2.4 & 0.9 & 2.5 & \\
\hline \(t_{r},{ }^{+}\) & \multicolumn{3}{|l|}{Rise time} & 0.55 & 1.7 & 0.65 & 1.8 & 0.7 & 1.9 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}, \mathrm{t}}\) - & \multicolumn{3}{|l|}{Fall time} & 0.55 & 1.7 & 0.65 & 1.8 & 0.7 & 1.9 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\title{
ECL 10KH High-Speed Emitter Coupled Logic Family MC10H162 \\ Binary to 1-of-8 Decoder
}

\section*{Features/Benefits}
- Propagation delay 1 ns typical
- Power dissipation, 315 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H162 is a high-speed Binary to 1-of-8 Decoder. This device is a member of Monolithic Memories' ECL 10KH family. This ECL device is designed to convert a three-bit word to one-of-eight output lines. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10H162 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. This device is ideally suited for high-speed multiplexer/ demultiplexer applications.

This ECL 10 KH part is a functional/pinout duplication of the standard ECL 10K part with 100\% improvement in propagation delay and no increase in power-supply current.

\section*{Pin Configurations}

MC10H162
Binary to 1-of-8 Decoder (Inverting)


Ordering Information
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H162 & J,N,NL & Com \\
\hline
\end{tabular}

Truth Table
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{5}{|c|}{INPUTS} & \multicolumn{8}{|c|}{OUTPUTS} \\
\hline E0 & E1 & C & B & A & Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7 \\
\hline L & L & L & L & L & H & L & L & L & L & L & L & L \\
\hline L & L & L & L & H & L & H & L & L & L & L & L & L \\
\hline L & L & L & H & L & L & L & H & L & L & L & L & L \\
\hline L & L & L & H & H & L & L & L & H & L & L & L & L \\
\hline L & L & H & L & L & L & L & L & L & H & L & L & L \\
\hline L & L & H & L & H & L & L & L & L & L & H & L & L \\
\hline L & L & H & H & L & L & L & L & L & L & L & H & L \\
\hline L & L & H & H & H & L & L & L & L & L & L & L & H \\
\hline H & X & X & X & X & L & L & L & L & L & L & L & L \\
\hline X & H & X & X & X & L & L & L & L & L & L & L & L \\
\hline
\end{tabular}

X = Don't Care.

\section*{Logic Diagram}

MC10H162
Binary to 1-of-8 Decoder


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\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & \multicolumn{3}{|l|}{COMMERCIAL} & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\mathrm{A}}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & Power supply current & - & 84 & - & 76 & - & 84 & mA \\
\hline linH & Input current HIGH & - & 465 & - & 275 & - & 275 & \(\mu \mathrm{A}\) \\
\hline linL & Input current LOW & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH output voltage & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline V IH & HIGH input voltage & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(V_{\text {IL }}\) & LOW input voltage & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\({ }^{\text {t }}\) d} & \multirow[b]{2}{*}{Propagation delay} & Data & 0.7 & 2.0 & 0.7 & 2.1 & 0.8 & 2.5 & \multirow[b]{2}{*}{ns} \\
\hline & & Enable & 0.8 & 2.3 & 0.8 & 2.4 & 0.9 & 2.6 & \\
\hline \(t_{r},{ }^{+}\) & \multicolumn{2}{|l|}{Rise time} & 0.6 & 1.8 & 0.6 & 1.9 & 0.6 & 2.0 & ns \\
\hline \(t_{f}, t-\) & \multicolumn{2}{|l|}{Fall time} & 0.6 & 1.8 & 0.6 & 1.9 & 0.6 & 2.0 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{Typical Applications}


Figure 1. High Speed 16-Bit Multiplexer/Demultiplexer

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family \\ MC10H164 \\ 8-Line Multiplexer
}

\section*{Features/Benefits}
- Propagation delay, 1 ns typical
- Power dissipation, 310 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H164 is a member of Monolithic Memories' ECL family. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100\% improvement in propagation delay, and no increase in power supply current.

\section*{Pin Configuration}

MC10H164
8-Line Multiplexer


\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow{2}{*}{ ENABLE } & \multicolumn{4}{|c|}{ ADDRESS INPUTS } \\
\cline { 2 - 4 } & C & B & A & Z \\
\hline \hline L & L & L & L & X0 \\
\hline L & L & L & H & X1 \\
\hline L & L & H & L & X2 \\
\hline L & L & H & H & X3 \\
\hline L & H & L & L & X4 \\
\hline L & H & L & H & X5 \\
\hline L & H & H & L & X6 \\
\hline L & H & H & H & X7 \\
\hline H & X & X & X & L \\
\hline
\end{tabular}

\footnotetext{
X = Don't Care
}

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC 10 H 164 & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)\) & Com \\
\hline
\end{tabular}

The MC10H164 is designed to be used in data multiplexing and parallel-to-serial conversion applications. Full parallel gating provides equal delays through any data path. The MC10H164 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the MC10H164 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than eight lines using additional MC10H164s.

\section*{Logic Diagram}

MC10H164
8-Line Multiplexer


\footnotetext{
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}

\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|l|}{PARAMETER} & & MMERC TYP & CIAL MAX & UNIT \\
\hline \(\mathrm{V}_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline TA & \multicolumn{2}{|l|}{Operating free-air temperature} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{\({ }^{\text {TSTG }}\)} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }_{\text {I }}\) & Power supply current & - & 83 & - & 75 & - & 83 & mA \\
\hline \(\mathrm{linH}^{\text {in }}\) & Input current HIGH & - & 512 & - & 320 & - & 320 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & Input current LOW & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH output voltage & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & -1.95 & -1.63 & -1.95 & -1.63 & -0.735 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & HIGH input voltage & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & LOW input voltage & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{VEE}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathbf{V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{5}{*}{\(t_{\text {pd }}\)} & \multirow{5}{*}{Propagation delay} & \(\mathrm{X}_{0}-\mathrm{X}_{7}\) & 1.0 & 2.8 & 0.7 & 2.7 & 0.7 & 2.9 & \multirow{5}{*}{ns} \\
\hline & & A,B,C, & 1.0 & 3.8 & 0.7 & 3.6 & 0.7 & 3.9 & \\
\hline & & Data & 0.7 & 2.4 & 0.8 & 2.5 & 0.9 & 2.6 & \\
\hline & & Address & 1.0 & 2.8 & 1.1 & 2.9 & 1.2 & 3.2 & \\
\hline & & Enable & 0.4 & 1.45 & 0.4 & 1.5 & 0.5 & 1.7 & \\
\hline \(t_{r},{ }^{\text {t }}\) & \multicolumn{2}{|l|}{Rise time} & 0.6 & 1.8 & 0.6 & 1.9 & 0.6 & 2.0 & ns \\
\hline \(t_{\text {f }}, t-\) & \multicolumn{2}{|l|}{Fall time} & 0.6 & 1.8 & 0.6 & 1.9 & 0.6 & 2.0 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\title{
ECL 10KH High-Speed \\ Emitter Coupled Logic Family \\ MC10H166 \\ 5-Bit Magnitude Comparator
}

\section*{Features/Benefits}
- Propagation delay, Data-to-Output, 2.0 ns typical
- Power dissipation, 440 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H166 is a member of Monolithic Memories' ECL 10KH family. This device is a 5-Bit Magnitude Comparator and is a functional/pinout duplication of the standard ECL 10K part with \(100 \%\) improvement in propagation and no increase in powersupply current.

The MC10H166 is a high-speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: \(A<B\) and \(A>B\). The \(A=B\) function can be obtained by wire-ORing these outputs (a low level indicates \(A=B\) ) or by wire-NORing the outputs (a high level indicates \(A=B\) ). \(A\) high level on the enable function forces both outputs low.

\section*{Pin Configurations}

MC10H166
5-Bit Magnitude Comparator


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline MC10H166 & J,N,NL & Com \\
\hline
\end{tabular}

\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ INPUTS } & \multicolumn{2}{c|}{ OUTPUTS } \\
\hline \(\bar{E}\) & \(A\) & \(B\) & \(A<B\) & \(A>B\) \\
\hline\(H\) & \(X\) & \(X\) & \(L\) & \(L\) \\
\hline\(L\) & Word A \(=\) Word B & \(L\) & \(L\) \\
\hline\(L\) & Word A > Word B & \(L\) & \(H\) \\
\hline\(L\) & \multicolumn{2}{|c|}{ Word A < Word B } & \(H\) & \(L\) \\
\hline
\end{tabular}

\section*{Logic Diagram}


\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & \[
\begin{aligned}
& \text { CON } \\
& \text { MIN }
\end{aligned}
\] & \[
\begin{aligned}
& \text { АMER } \\
& \text { TYP }
\end{aligned}
\] & IAL. MAX & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & Power supply current & - & 117 & - & 106 & - & 117 & mA \\
\hline linH & Input current HIGH & - & 350 & - & 220 & - & 220 & \(\mu \mathrm{A}\) \\
\hline linL & Input current LOW & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline VOH & HIGH output voltage & -1.02 & -0.84 & -0.98 & \(-0.81\) & -0.92 & \(-0.735\) & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & HIGH input voltage & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\text {IL }}\) & LOW input voltage & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\({ }^{\text {tpd }}\)} & \multirow[b]{2}{*}{Propagation delay} & Data-to-Output & 1.1 & 3.5 & 1.1 & 3.7 & 1.2 & 4.1 & \multirow{2}{*}{ns} \\
\hline & & Enable-to-Output & 0.6 & 1.7 & 0.7 & 1.7 & 0.7 & 1.8 & \\
\hline \(t_{r}, t+\) & \multicolumn{2}{|l|}{Rise time} & 0.6 & 1.5 & 0.6 & 1.6 & 0.6 & 1.7 & ns \\
\hline \(t_{f, t}\) t & \multicolumn{2}{|l|}{Fall time} & 0.6 & 1.5 & 0.6 & 1.6 & 0.6 & 1.7 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50-\Omega\) resistor to -2.0 V .


Figure 1. 9-Bit Magnitude Comparator
For longer word lengths, the MC10H166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9 -bit word length. The \(A>B\) and \(A<B\) outputs are fed to the \(A_{0}\) and \(B_{0}\) inputs respectively of the next device. The connection for an \(A=B\) output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data-to-output delay.


\(B_{4}\)
\(A_{4}\)
\(B_{3}\)
\(A_{3}\)
\(B_{2}\)
\(A_{2}\)
\(B_{1}\)
\(A_{1}\)
\(B_{0}\)
\(A_{0}\)\(\quad \begin{aligned} & B_{4} \\ & A_{4} \\ & B_{3} \\ & A_{3} \\ & B_{2} \\ & A_{2} \\ & B_{1} \\ & A_{1} \\ & B_{0} \\ & A_{0}\end{aligned}\)
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{3}{*}{\[
A<B
\]}} \\
\hline & \\
\hline & \\
\hline
\end{tabular}

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25-bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

Figure 2. 25-Bit Magnitude Comparator

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H173 QUAD 2-Input Multiplexer With Latch
}

PRELIMINARY
INFORMATION
This document contains specifications and information which are subject to change

\section*{Features/Benefits}
- Propagation delay, 1.5 ns typical
- Power dissipation, 275 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H173 is a quad 2-input multiplexer with latch. This device is a functional/pinout duplication of the standard ECL 10K part, with \(100 \%\) improvement in propagation delay and no increase in power-supply current.

It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high \((H)\) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the data outputs.

\section*{MC10H173 Function Table}
\begin{tabular}{|c|c|c|}
\hline SELECT & CLOCK & \(\mathbf{Q}_{\mathbf{n}}=\mathbf{1}\) \\
\hline \hline H & L & D 00 \\
\hline L & L & D 01 \\
\hline X & H & \(\mathrm{QO}_{\mathrm{n}}\) \\
\hline
\end{tabular}
\(X=\) Don't care.

\section*{Pin Configurations}

MC10H173
Quad 2-Input Multiplexer with Latch


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H173 & \(\mathrm{J}, \mathrm{N}, \mathrm{NL}(20)\) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H173
Quad 2-Input Multiplexer with Latch


MC10H173


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\section*{Operating Conditions}


\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathrm{V} \pm \mathbf{5 \%}\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 73 & - & 66 & - & 73 & mA \\
\hline \multirow[b]{2}{*}{linH} & \multirow[b]{2}{*}{Input current HIGH} & Pins 3-7 and 10-13 & - & 510 & - & 320 & - & 320 & \multirow[t]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pin 9 & - & 475 & - & 300 & - & 300 & \\
\hline 1 inL & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & \(-0.735\) & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{V E E}^{\mathbf{E}}=\mathbf{- 5 . 2} \mathbf{V}, \pm \mathbf{5 \%}\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{3}{*}{\({ }^{\text {p }}\) d} & \multirow{3}{*}{Propagation delay} & Data & 0.7 & 2.3 & 0.7 & 2.3 & 0.7 & 2.3 & \multirow{3}{*}{ns} \\
\hline & & Clock & 1.0 & 3.7 & 1.0 & 3.7 & 1.0 & 3.7 & \\
\hline & & Select & 1.0 & 3.6 & 1.0 & 3.6 & 1.0 & 3.6 & \\
\hline \multirow[t]{2}{*}{\(\mathrm{t}_{\text {set }}\)} & \multirow[t]{2}{*}{Setup time} & Data & 0.7 & - & 0.7 & - & 0.7 & - & \multirow[t]{2}{*}{ns} \\
\hline & & Select & 1.0 & - & 1.0 & - & 1.0 & - & \\
\hline \multirow[t]{2}{*}{\(t_{\text {hold }}\)} & \multirow[t]{2}{*}{Hold time} & Data & 0.7 & - & 0.7 & - & 0.7 & - & \multirow[t]{2}{*}{ns} \\
\hline & & Select & 1.0 & - & 1.0 & - & 1.0 & - & \\
\hline \(t_{r}, t+\) & \multicolumn{2}{|l|}{Rise time} & 0.7 & 2.4 & 0.7 & 2.4 & 0.7 & 2.4 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}, \mathrm{t}}\) - & \multicolumn{2}{|l|}{Fall time} & 0.7 & 2.4 & 0.7 & 2.4 & 0.7 & 2.4 & ns \\
\hline
\end{tabular}

NOTE: Each ECL 10 KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H174 \\ Dual 4-to-1 Multiplexer}

\section*{Features/Benefits}
- Propagation delay 1.5 ns typical
- Power dissipation, 305 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H174 is a Dual 4-to-1 Multiplexer. This device is a member of Monolithic Memories' new ECL family. This device is a functional/pinout duplication of the standard ECL 10K part with \(100 \%\) improvement in propagation delay, and no increase in power-supply current.

\section*{Pin Configuration}

MC10H174
Dual 4-to-1 Multiplexer


MC10H174


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC 10 H 174 & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)\) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H174


Function Table
\begin{tabular}{|c|c|c|c|c|}
\hline ENABLE & ADDRESS & INPUTS & \multicolumn{2}{|c|}{ OUTPUTS } \\
\hline \(\bar{E}\) & B & A & Z & W \\
\hline H & X & X & L & L \\
\hline L & L & L & \(\mathrm{X}_{0}\) & \(\mathrm{Y}_{0}\) \\
\hline L & L & H & \(\mathrm{X}_{1}\) & \(\mathrm{Y}_{1}\) \\
\hline L & H & L & \(\mathrm{X}_{2}\) & \(\mathrm{Y}_{2}\) \\
\hline L & H & H & \(\mathrm{X}_{3}\) & \(\mathrm{Y}_{3}\) \\
\hline
\end{tabular}
\(X=\) Don't care

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\section*{Absolute Maximum Ratings}
\begin{tabular}{|c|c|}
\hline \multicolumn{2}{|l|}{\multirow[t]{2}{*}{}} \\
\hline & 0 Vdc to VEE \\
\hline \multicolumn{2}{|l|}{Output Current:} \\
\hline Continuous & 50 mA \\
\hline Surge & 100 mA \\
\hline
\end{tabular}

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & \multicolumn{3}{|l|}{COMMERCIAL} & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & , & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} E\) & \multicolumn{2}{|l|}{Power supply current} & - & 80 & - & 73 & - & 80 & mA \\
\hline \multirow[b]{2}{*}{\(\mathrm{I}_{\mathrm{inH}}\)} & \multirow[b]{2}{*}{Input current HIGH} & Pins 3-7 and 9-13 & - & 475 & - & 300 & - & 300 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pin 14 & - & 670 & - & 420 & - & 420 & \\
\hline \(\mathrm{I}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{v e E}^{\text {E }}=\mathbf{- 5 . 2} \mathbf{V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{3}{*}{\({ }^{t} \mathrm{pd}\)} & \multirow{3}{*}{Propagation delay} & Data (All others) & 0.7 & 2.4 & 0.8 & 2.3 & 0.9 & 2.6 & \multirow{3}{*}{ns} \\
\hline & & Select (A,B) Pin 7, 9 & 1.0 & 2.8 & 1.1 & 2.9 & 1.2 & 3.2 & \\
\hline & & Enable Pin 14 & 0.4 & 1.45 & 0.4 & 1.50 & 0.5 & 1.70 & \\
\hline \(t_{r}, t+\) & \multicolumn{2}{|l|}{Rise time} & 0.5 & 1.5 & 0.5 & 1.6 & 0.5 & 1.70 & ns \\
\hline \(t_{f}, t-\) & \multicolumn{2}{|l|}{Fall time} & 0.5 & 1.5 & 0.5 & 1.6 & 0.5 & 1.70 & ns \\
\hline
\end{tabular}

\footnotetext{
Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
}

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family MC10H175 \\ Quint Latch
}

\section*{Features/Benefits}
- Propagation delay, 1.2 ns typical
- Power dissipation, \(\mathbf{4 0 0} \mathbf{~ m W}\) typical
- Noise margin \(\mathbf{1 5 0} \mathbf{~ m V}\)
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H175 is a member of Monolithic Memories' ECL family. The MC10H175 is a quint D-type latch with common reset and clock lines. This ECL 10KH part is a functional/pinout duplication of the standard ECL 10K part, with 100\% improvement in propagation delay, and no increase in power-supply current.

\section*{Pin Configuration}


\section*{Truth Table}
\begin{tabular}{|c|c|c|c|c|}
\hline\(D\) & \(C_{0}\) & \(C_{1}\) & RESET & \(Q_{n+1}\) \\
\hline \hline\(L\) & \(L\) & \(L\) & \(X\) & \(L\) \\
\hline\(H\) & \(L\) & \(L\) & \(X\) & \(H\) \\
\hline\(X\) & \(H\) & \(X\) & \(L\) & \(Q_{n}\) \\
\hline\(X\) & \(X\) & \(H\) & \(L\) & \(Q_{n}\) \\
\hline\(X\) & \(H\) & \(X\) & \(H\) & \(L\) \\
\hline\(X\) & \(X\) & \(H\) & \(H\) & \(L\) \\
\hline
\end{tabular}

X \(=\) Don't Care
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Ordering Information
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC 10 H 175 & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(20)\) & Com \\
\hline
\end{tabular}

\section*{Application Information}

The MC10H175 is a high-speed, low-power quint latch. It features five D-type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are ORed together.
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

\section*{Logic Diagram}


\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|c|}{\multirow[t]{2}{*}{PARAMETER}} & & MER & & UNIT \\
\hline & & & MIN & TYP & MAX & \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathbf{V E E}_{\text {EE }}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow[b]{2}{*}{CHARACTERISTIC}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow[b]{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} E\) & \multicolumn{2}{|l|}{Power supply current} & - & 107 & - & 97 & - & 107 & mA \\
\hline \multirow[b]{2}{*}{\(\mathrm{l}_{\mathrm{inH}}\)} & \multirow[b]{2}{*}{Input current HIGH} & Pins 5,6,7,9,10,12,13 & - & 565 & - & 335 & - & 335 & \multirow{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pin 11 & - & 1120 & - & 660 & - & 660 & \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=\mathbf{- 5 . 2} \mathrm{V}, \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|r|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow{3}{*}{\({ }^{\text {t p }}\)} & \multirow{3}{*}{Propagation delay} & Data & 0.6 & 1.6 & 0.6 & 1.6 & 0.6 & 1.7 & \multirow{3}{*}{ns} \\
\hline & & Clock & 0.7 & 1.9 & 0.7 & 2.0 & 0.8 & 2.1 & \\
\hline & & Reset & 1.0 & 2.2 & 1.0 & 2.3 & 1.0 & 2.4 & \\
\hline \(t_{\text {set }}\) & \multicolumn{2}{|l|}{Setup time} & 1.5 & - & 1.5 & - & 1.5 & - & ns \\
\hline thold & \multicolumn{2}{|l|}{Hold time} & 0.8 & - & 0.8 & - & 0.8 & - & ns \\
\hline \(t_{r}, t+\) & \multicolumn{2}{|l|}{Rise time} & 0.5 & 1.8 & 0.5 & 1.9 & 0.5 & 2.0 & ns \\
\hline \(t_{f}, t-\) & \multicolumn{2}{|l|}{Fall time} & 0.5 & 1.8 & 0.5 & 1.9 & 0.5 & 2.0 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\section*{ECL 10KH High-Speed \\ Emitter Coupled Logic Family MC10H176 \\ Hex D Master-Slave Flip-Flop}

\section*{Features/Benefits}
- Propagation delay 1.7 ns typical
- Power dissipation, 460 mW typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H176 is a member of Monolithic Memories' ECL 10KH family. This ECL device includes six high speed master-slave D-type flip-flops with one common input clock for all six. Data enters into the master during the LOW state of the clock and is transferred to the slave during the positive-going clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

This ECL 10 KH part is a functional/pinout duplication of the standard ECL 10K part, with \(100 \%\) improvement in clock frequency and propagation delay and no increase in powersupply current.

\section*{Pin Configurations}

MC10H176
Hex D Master-Slave Flip-Flop


Ordering Information
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H176 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Truth Table}
\begin{tabular}{|c|c|c|}
\hline \(\mathbf{C}\) & \(\mathbf{D}\) & \(\mathbf{Q}_{\boldsymbol{n}+\mathbf{1}}\) \\
\hline L & X & \(\mathbf{Q}_{\boldsymbol{n}}\) \\
\hline \(\mathrm{H}^{\star}\) & L & L \\
\hline \(\mathrm{H}^{\star}\) & \(H\) & \(H\) \\
\hline
\end{tabular}

X = Don't Care
* A clock H is a clock transition from a low to a high state

\section*{Logic Diagram}

MC2OH176 Hex D Master-Slave Flip-Flop

Absolute Maximum Ratings
Supply voltage \(\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)\) ..... -8.0 V to 0 Vdc
Input voltage \(\mathrm{V}_{1}\left(\mathrm{~V}_{\mathrm{CC}}=0\right)\) 0 Vdc to VEEOutput Current:
Continuous ..... 50 mA
Surge ..... 100 mA

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & COM & \[
\begin{aligned}
& \text { AMERC } \\
& \text { TYP }
\end{aligned}
\] & IAL MAX & UNIT \\
\hline \(\mathrm{V}_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline TA & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|l|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 123 & - & 112 & - & 123 & mA \\
\hline \multirow[b]{2}{*}{1 inH} & \multirow[b]{2}{*}{Input current HIGH} & Pins 5,6,7,10,11,12 & - & 425 & - & 265 & - & 265 & \multirow[b]{2}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pin 9 & - & 670 & - & 420 & - & 420 & \\
\hline linL & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\text {IH }}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & \(V_{\text {dc }}\) \\
\hline \(V_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline
\end{tabular}

Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \(\mathrm{t}_{\mathrm{pd}}\) & Propagation delay & 0.9 & 2.1 & 0.9 & 2.2 & 1.0 & 2.4 & ns \\
\hline \(\mathrm{t}_{\text {set }}\) & Setup time & 1.5 & - & 1.5 & - & 1.5 & - & ns \\
\hline thold & Hold time & 0.9 & - & 0.9 & - & 0.9 & - & ns \\
\hline \(t_{r},{ }^{+}\) & Rise time & 0.5 & 1.8 & 0.5 & 1.9 & 0.5 & 2.0 & ns \\
\hline \(t_{f}, t-\) & Fall time & 0.5 & 1.8 & 0.5 & 1.9 & 0.5 & 2.0 & ns \\
\hline \(f_{\text {tog }}\) & Toggle frequency & 250 & - & 250 & - & 250 & - & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\title{
ECL 10KH High-Speed Emitter-Coupled Logic Family \\ MC1OH179 \\ Look-Ahead Carry Block
}

\section*{Features/Benefits}
- Propagation delay, 1 ns typical
- Power dissipation, \(\mathbf{3 0 0} \mathbf{~ m W}\) typical
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H179 is a Look-Ahead Carry Block. This device is a member of Monolithic Memories' ECL 10KH family.

This ECL 10 KH part is a functional/pinout duplication of the standard ECL 10K part with 100\% improvement in propagation delay, and no increase in power-supply current.

\section*{Pin Configuration}

MC10H179
Look-Ahead Carry Block


MC10H179


\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H179 & J,N,NL(20) & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H179 Look-Ahead Carry Block

\(P_{G}=\mathbf{P O}_{0}+\mathbf{P} 1+\mathbf{P}_{2}+\mathbf{P}_{3}\)
\(\mathbf{G}_{\mathbf{G}}=(\mathbf{G} 0+\mathbf{P} 1+\mathbf{P} 2+\mathrm{P} 3)(\mathbf{G} 1+\mathbf{P} 2+\mathrm{P} 3)(\mathbf{G} 2+\mathrm{P} 3) \mathbf{G} 3\)
\(\begin{array}{ll}C_{n+2} & =\left(C_{n}+P 0+P 1\right)(G 0+P 1) G 1 \\ C_{n+4} & =(C, P 0+P 1+P 2+P 3)(G 0\end{array}\)
\(C_{n+4}=\left(C_{n}+P 0+P 1+P 2+P 3\right)(G 0+P 1+P 2+P 3)(G 1+P 2+P 3)\) (G2 +P 3 ) G 3

\section*{Application}

The MC10H179 is a high-speed, low-power, standard ECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10H181 4-bit ALU directly, or with the MC10H180 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high-speed arithmetic operation on long words.

When used with the MC10H181, the MC10H179 performs a second order or higher look-ahead. Figure 2 shows a 16 -bit look-ahead carry arithmetic unit Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10H179 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

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Figure 1. 32-Bit ALU with Carry Look-Ahead


Figure 2. 16-Bit Full Look-Ahead Carry Arithmetic Logic Unit

\section*{Absolute Maximum Ratings}


\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|r|}{PARAMETER} & CON & \[
\begin{aligned}
& \text { AMERC } \\
& \text { TYP }
\end{aligned}
\] & \[
\overline{\text { CIAL }}
\]
MAX & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{\({ }^{\text {T STG }}\)} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|l|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & \multicolumn{2}{|l|}{Power supply current} & - & 79 & - & 72 & - & 79 & mA \\
\hline \multirow{5}{*}{\(\mathrm{I}_{\mathrm{inH}}\)} & \multirow{5}{*}{Input current HIGH} & Pins 5 and 9 & - & 465 & - & 275 & - & 275 & \multirow{5}{*}{\(\mu \mathrm{A}\)} \\
\hline & & Pins 4, 7 and 11 & - & 545 & - & 320 & - & 320 & \\
\hline & & Pin 14 & - & 705 & - & 415 & - & 415 & \\
\hline & & Pin 12 & - & 790 & - & 465 & - & 465 & \\
\hline & & Pins 10 and 13 & - & 870 & - & 510 & - & 510 & \\
\hline \(\mathrm{I}_{\text {inL }}\) & \multicolumn{2}{|l|}{Input current LOW} & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & \multicolumn{2}{|l|}{HIGH output voltage} & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & \multicolumn{2}{|l|}{LOW output voltage} & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & \multicolumn{2}{|l|}{HIGH input voltage} & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline \(\mathrm{V}_{\text {IL }}\) & \multicolumn{2}{|l|}{LOW input voltage} & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & \(\mathrm{V}_{\mathrm{dc}}\) \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\(t_{\text {pd }}\)} & \multirow[b]{2}{*}{Propagation delay} & \(P\) to PG & 0.40 & 1.40 & 0.40 & 1.50 & 0.50 & 1.70 & \multirow[b]{2}{*}{ns} \\
\hline & & G, P, Cn to Cn or GG & 0.60 & 2.30 & 0.70 & 2.40 & 0.80 & 2.60 & \\
\hline \(t_{r},{ }^{\text {t }}\) & \multicolumn{2}{|l|}{Rise time} & 0.5 & 1.7 & 0.5 & 1.8 & 0.5 & 1.9 & ns \\
\hline \(t_{f},{ }^{\text {t }}\) & \multicolumn{2}{|l|}{Fall time} & 0.5 & 1.7 & 0.5 & 1.8 & 0.5 & 1.9 & ns \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .

\title{
ECL 10KH High Speed \\ Emitter Coupled Logic Family \\ MC10H209 \\ Dual 4-5 Input OR/NOR Gate
}

\section*{Features/Benefits}
- Propagation delay, 0.75 ns typical
- 125 mW typical (no load)
- Noise margin 150 mV
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H209 is a member of the Monolithic Memories' ECL 10KH Family. This ECL device is a dual 4-5 input OR/NOR gate. This device is a functional/pinout duplication of the standard ECL 10 K family part, with \(100 \%\) improvement in propagation delay and no increase in power supply current.

\section*{Pin Configuration}

MC10H209
Dual 4-5 Input OR/NOR Gate

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline MC10H209 & J,N,NL & Com \\
\hline
\end{tabular}

\section*{Logic Diagram}

MC10H209
Dual 4-5 Input OR/NOR Gate

\(V_{C C 1}=\operatorname{Pin} 1\)
\(V_{\text {CC1 }}=\operatorname{Pin} 16\)
\(V_{E E}=\operatorname{Pin} 8\)
-

MC10H209

Absolute Maximum Ratings

Input voltage \(\mathrm{V}_{\mathrm{I}}(\mathrm{V} C \mathrm{C}=0)\) \(0 V_{d c}\) to \(V_{E E}\)Output current:
Continuous ..... 50 mA
Surge ..... 100 mA

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|c|}{PARAMETER} & \[
\begin{aligned}
& \text { CON } \\
& \text { MIN }
\end{aligned}
\] & \[
\begin{aligned}
& \text { MMER } \\
& \text { TYP }
\end{aligned}
\] & CIAL MAX & UNIT \\
\hline \(V_{\text {EE }}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & \(-5.20\) & -4.94 & V \\
\hline \(\mathrm{T}_{\text {A }}\) & \multicolumn{2}{|l|}{Operating temperature range} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{\(T_{\text {STG }}\)} & \multirow{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[t]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathbf{V E E}_{\text {EE }}=-5.2 \mathrm{~V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \(\mathrm{I}_{\mathrm{E}}\) & Power supply current & - & - & - & 30 & - & - & mA \\
\hline \(\mathrm{I}_{\text {in }}\) & Input current HIGH & - & 640 & - & 400 & - & 400 & \(\mu \mathrm{A}\) \\
\hline I inL & Input current LOW & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH output voltage & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(\mathrm{V}_{\mathrm{IH}}\) & HIGH input voltage & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(\mathrm{V}_{\text {IL }}\) & LOW input voltage & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathbf{v E E}^{\mathbf{E E}} \mathbf{- 5 . 2} \mathbf{V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \(\mathrm{t}_{\mathrm{pd}}\) & Propagation delay & 0.4 & 1.15 & 0.4 & 1.15 & 0.7 & 1.15 & ns \\
\hline \(t_{r}\) & Rise time & 0.4 & 1.5 & 0.4 & 1.5 & 0.4 & 1.6 & ns \\
\hline \(\mathrm{t}_{\mathrm{f}}\) & Fall time & 0.4 & 1.5 & 0.4 & 1.5 & 0.4 & 1.6 & ns \\
\hline
\end{tabular}

Note:Each ECL. 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50-\Omega\) resistor to -2.0 V .

\section*{ECL 10 KH High-Speed Emitter-Coupled Logic Family MC10H210/MC10H211 3-Input, 3-Output OR/NOR Gates}

\section*{Features/Benefits}
- Propagation delay, 1.0 ns typical
- Power dissipation, 160 mW typical
- Noise margin 150 mV (over operating voltage and temperature range)
- Voltage compensated
- ECL 10K-compatible

\section*{Description}

The MC10H210 and MC10H211 are members of Monolithic Memories' ECL family. These devices are dual 3-input, 3-output "OR" and "NOR" gates respectively. These ECL 10KH parts are functional/pinout duplications of the standard ECL 10KH family parts, with 100\% improvement in propagation delay and no increase in power supply current.

\section*{Pin Configurations}

MC10H210
3-INPUT 3-OUTPUT OR GATE


MC10H211
3-INPUT 3-OUTPUT NOR GATE

* Pins 1 and 15 internally connected

Ordering Information
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline \hline \begin{tabular}{c} 
MC10H210 \\
MC 10 H 211
\end{tabular} & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL},(20)\) & Com \\
\hline
\end{tabular}


MC1OH211


MC10H210


MC10H211


\footnotetext{
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}
Absolute Maximum Ratings
Supply voltage, \(\mathrm{V}_{\mathrm{EE}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)\) ..... -8.0 V to \(0 \mathrm{~V}_{\mathrm{dc}}\)Input voltage, \(\mathrm{V}_{\mathrm{I}}\left(\mathrm{V}_{\mathrm{CC}}=0\right)\)\(.0 \mathrm{~V}_{\mathrm{dc}}\) to \(\mathrm{V}_{\mathrm{EE}}\)Output Current:
Continuous ..... 50 mA
Surge ..... 100 mA

\section*{Operating Conditions}
\begin{tabular}{|c|c|c|c|c|c|c|}
\hline SYMBOL & \multicolumn{2}{|c|}{PARAMETER} & COM
MIN & AMERC
TYP & CIAL MAX & UNIT \\
\hline \(V_{E E}\) & \multicolumn{2}{|l|}{Supply voltage} & -5.46 & -5.2 & -4.94 & V \\
\hline TA & \multicolumn{2}{|l|}{Operating free-air temperature} & 0 & & 75 & \({ }^{\circ} \mathrm{C}\) \\
\hline \multirow[b]{2}{*}{TSTG} & \multirow[b]{2}{*}{Storage temperature range} & Plastic & -55 & & 150 & \multirow[b]{2}{*}{\({ }^{\circ} \mathrm{C}\)} \\
\hline & & Ceramic & -55 & & 165 & \\
\hline
\end{tabular}

\section*{Electrical Characteristics \(\mathrm{V}_{\mathrm{EE}}=-\mathbf{5 . 2} \mathrm{V} \pm \mathbf{5 \%}\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multirow{2}{*}{SYMBOL} & \multirow{2}{*}{PARAMETER} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \({ }^{\prime} \mathrm{E}\) & Power supply current & - & 42 & - & 38 & - & 42 & mA \\
\hline \(\mathrm{linH}_{\mathrm{in}}\) & Input current HIGH & - & 720 & - & 450 & - & 450 & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{l}_{\mathrm{inL}}\) & Input current LOW & 0.5 & - & 0.5 & - & 0.3 & - & \(\mu \mathrm{A}\) \\
\hline \(\mathrm{V}_{\mathrm{OH}}\) & HIGH output voltage & -1.02 & -0.84 & -0.98 & -0.81 & -0.92 & \(-0.735\) & Vdc \\
\hline \(\mathrm{V}_{\mathrm{OL}}\) & LOW output voltage & -1.95 & -1.63 & -1.95 & -1.63 & -1.95 & -1.60 & Vdc \\
\hline \(V_{1 H}\) & HIGH input voltage & -1.17 & -0.84 & -1.13 & -0.81 & -1.07 & -0.735 & Vdc \\
\hline \(V_{\text {IL }}\) & LOW input voltage & -1.95 & -1.48 & -1.95 & -1.48 & -1.95 & -1.45 & Vdc \\
\hline
\end{tabular}

\section*{Switching Characteristics \(\mathrm{V}_{\mathrm{EE}}=-\mathbf{5 . 2 V} \pm 5 \%\) (See Note)}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{SYMBOL} & \multicolumn{2}{|c|}{\multirow[b]{2}{*}{PARAMETER}} & \multicolumn{2}{|c|}{\(0{ }^{\circ}\)} & \multicolumn{2}{|c|}{\(25^{\circ}\)} & \multicolumn{2}{|c|}{\(75^{\circ}\)} & \multirow{2}{*}{UNIT} \\
\hline & & & MIN & MAX & MIN & MAX & MIN & MAX & \\
\hline \multirow[b]{2}{*}{\({ }^{t} \mathrm{pd}\)} & \multirow[b]{2}{*}{Propagation delay} & MC10H210 & 0.5 & 1.55 & 0.55 & 1.55 & 0.6 & 1.7 & \multirow{2}{*}{ns} \\
\hline & & MC10H211 & 0.7 & 1.6 & 0.7 & 1.6 & 0.7 & 1.7 & \\
\hline \multirow[b]{2}{*}{\(t_{r},{ }^{+}\)} & \multirow[b]{2}{*}{Rise time} & MC10H210 & 0.75 & 1.8 & 0.75 & 1.9 & 0.8 & 2.0 & \multirow[b]{2}{*}{ns} \\
\hline & & MC10H211 & 0.9 & 2.0 & 0.9 & 2.2 & 0.9 & 2.4 & \\
\hline \multirow[b]{2}{*}{\(t_{f}, t-\)} & \multirow[b]{2}{*}{Fall time} & MC10H210 & 0.75 & 1.8 & 0.75 & 1.9 & 0.8 & 2.0 & \multirow[t]{2}{*}{ns} \\
\hline & & MC10H211 & 0.9 & 2.0 & 0.9 & 2.2 & 0.9 & 2.4 & \\
\hline
\end{tabular}

Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a \(50 \Omega\) resistor to -2.0 V .
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LOGIC CELL ARRAY
Logic Cell Array

\section*{Logic Cell Array \({ }^{\text {™ }}\)}

\section*{Introduction}

The Logic Cell Array (LCA) \({ }^{\text {Tm }}\) is a CMOS integrated circuit with a flexible, uncommitted architecture and VLSI-level density. The LCA is manufactured on Monolithic Memories' 1.6 micron CMOS process. The device architecture as is shown in Figure 1, similar to that of a gate array, with an interior matrix of programmable logic blocks, a surrounding ring of I/O interface blocks and programmable interconnect used to define the overall device structure.
Unlike gate arrays, Logic Cell Array functionality is defined by the user simply by loading the internal writable storage cells with the configuration data. An additional benefit, reprogrammability in system, allows in-circuit-emulation to be used for design verification.
The M2064 family of Logic Cell Arrays has been developed to allow Monolithic Memories to offer a device and technology that offer both the density benefits of gate arrays and the programmability benefits of user-configurable devices. These parts have been designed for maximum flexibility in system applications and are easy to use.
Using the XACT'M software development system, the designer can define and interconnect logic blocks to build larger-scale, multi-level logic functions. These are then connected to external circuitry. Interconnections throughout the Array are defined automatically by the development system, unless otherwise specified by the designer. Because the Logic Cell Array's logic functions and interconnections are established with memory cells, the array is never physically altered; instead it is simply reprogrammed.

\section*{XACT Evaluation Kit (LCA-MEK01)}

Monolithic Memories offers evaluation software and documentation that will allow a designer to determine if his or her logic design fits and assess its performance as a Logic Cell Array. All that is needed is an IBM PC-XT, AT, or compatible, a three-button Mouse System or compatible mouse.

\section*{XACT Development System (LCA-MDS21)}

The XACT Development System is the "power behind the machine." It will allow a designer to sit down with a concept and walk away with a completely tested, completely finished part.
The reason is that XACT functions as both a CAE and CAM system. The CAE part of the system allows the designer to simply draw out the design using a sophisticated graphicsbased design editor. The CAM part then converts the drawing to code, similar to a PALASM-generated JEDEC file, that allowsprogramming with conventional programming hardware of an EPSOM containing the configuration data for system phototyping.
The XACT Development System currently has 113 macros and, in addition, allows the user to define his or her own macro. To insure that internal timing constraints are satisfied, a Timing Analyzer is included to calculate propagation delays along any path within the Array.
As the design is being entered, the Automatic Design Checker insures that no design rules are violated, and when the design is completed, a final design rule check is performed.

\section*{The XACT Development System}

Contents:
- Editor
- Macro Library
- Design Checker
- Timing Analyzer
- Simulator
- Configuration File Generator
- Configuration File Formatter

\section*{In-Circuit-Emulator (LCA-MDS24)}

The In-Circuit-Emulator is a software/hardware package that enables a designer to connect his or her target system to the workstation where a design has just been completed. The emulator package allows:
- User control and monitoring of device function
- Interactive or file-driven setup and configuration
- Daisy-chain configuration capabilities for up to seven LCAs in a chain
- Simultaneous in-circuit emulation of up to four devices
- Single step capability for device clocks
- Readback display of device internal register states
- Dynamic reconfiguration capability.

The In-Circuit-Emulator comes with a single "pod". Up to three additional pods (LCA-MDS25) may be ordered for each emulator.

\section*{P-SILOS Simulation Package (LCA-MDS22)}

After a design is completed, the next step is to simulate. Monolithic Memories offers an integrated simulation package manufactured by Simucad, called P-SILOS.
\begin{tabular}{|c|c|}
\hline PART NUMBER & DESCRIPTION \\
\hline LCA-MEK01 & LCA Evaluation Kit \\
\hline LCA-MDS21 & LCA Development system \\
\hline LCA-MDS22 & LCA Simulator - P-SILOS \\
\hline LCA-MDS24 & LCA In-Circuit-Emulator \\
\hline LCA-MDS25 & LCA In-Circuit-Emulator Pod \\
\hline LCA-MTB01 & LCA Demonstration Board \\
\hline
\end{tabular}

Table 1

The introduction of the Logic Cell Array will allow customers to reduce inventories of discrete components, reduce the time to market and development cost for new products, save money in manufacturing and spare parts inventory management, reduce test costs and improve system reliability.

\section*{Configurable Logic Block}

The core of the Logic Cell Array is an \(8 \times 8\) matrix of Configurable Logic Blocks. Each CLB provides four logic inputs, a clock input, a combinatorial logic section, two logic outputs, and a programmable storage element.
The inputs drive a combinatorial logic section that can perform any logic function from a simple gate to a three-out-of-four majority decoder.
The combinatorial portion accepts and generates both positiveand negative-true logic, eliminating the need for inverters or the routing of complementary signals.
The storage element can serve as a flip-flop (D-type) and can be programmed to have clock enable, synchronous set and reset, and various gated inputs. In addition, since all these options can be specified independently for each logic block, designers can mix asynchronous and synchronous logic in any combination.


\section*{Configurable I/O Block}

External signals enter and leave the chip through generalpurpose, user-definable I/O blocks positioned around the periphery of the array. Each block can be programmed independently to be an input, output or bidirectional pin with a tristate control on the output. When configured as an input, the designer can select TTL or CMOS thresholds. In addition, each I/O bloc contains an input register option whose clock line is common to all the other I/O blocks along the same edge of the die.
I/O blocks can also handle more than input and output functions. For example, the Input registers of unused I/O blocks can be used for read/write storage registers or as stages of a shift register.

Figure 1

\title{
Logic Cell Array \({ }^{\text {TM }}\) \\ M2064
}

\section*{Features/Benefits}
- CMOS programmable Logic Cell Array (LCA \({ }^{\text {w }}\) ) for replacement of standard logic
- Completely reconfigurable by the user in the final system
- High performance
-20 MHz flip-flop toggle rate (-20 speed grade)
-33 MHz flip-flop toggle rate (-33 speed grade)
- 50 MHz flip-flop toggle rate ( \(\mathbf{- 5 0}\) speed grade)
- User-configurable logic functions, interconnect and I/O for maximum flexibility
- 64 user-Configurable Logic Blocks (CLBs) providing usable gate equivalency of up to \(\mathbf{1 5 0 0}\) gates
- 58 individually-configurable I/O pins allowing any mix of inputs, outputs or bidirectional signals (68-pin package)
- User-selectable TTL or HCMOS input threshold levels
- Multiple configuration modes for greatest flexibility and ease of use
- Verification feature allows user to check configuration data
- User-selectable security feature prevents read-back of configuration data
- Read-back of internal register states for system debug
- On-chip clock oscillator and clock buffer circuits provide flexible internal and external clocking functions
- Master reset of all internal register elements in addition to user-configurable Reset and/or Set control of individual CLB storage elements

\section*{General Description}

The M2064 is the first member of a family of configurable Logic Cell Arrays (LCAs) available from Monolithic Memories. These general purpose CMOS integrated circuit devices allow the user to rapidly implement complex digital logic functions directly without the requirement for masking or other vendor performed programming steps. Unique configuration circuitry allows complete reconfiguration within a user's final system to allow system changes "on-the-fly."
User configuration is controlled by internal storage elements. These are loaded with data bits which control definition of logic functions, configuration of I/O blocks, routing of internal signals, and other options. Configuration data can be loaded in one of several methods to minimize impact on overall system design.
CMOS technology optimized for system level performance provides LS-TTL compatible speeds with power consumption less than \(10 \%\) of equivalent TTL systems. The use of innovative I/O buffers providing either TTL or CMOS input switching levels insures lowest possible power consumption in totally CMOS systems without any compromise in performance.

\section*{Ordering Information}

\begin{tabular}{|l|l|}
\hline \multicolumn{1}{|c|}{ PART NUMBER } & \multicolumn{1}{c|}{ DESCRIPTION } \\
\hline \hline LCA-MDS21 & XACT Development System \\
\hline LCA-MDS22 & P-SILOS Simulation Package \\
\hline LCA-MDS24 & LCA In-Circuit Emulator \\
\hline LCA-MDS25 & In-Circuit Emulator Pod \\
\hline LCA-MEK01 & XACT Evaluation Kit \\
\hline
\end{tabular}


\section*{Pin Description}

\section*{I/O}

User-configurable Input/Output pins.

\section*{~PWRDN}

Input forces device into low power mode; operation is suspended.

\section*{M0-~RT}

Dual function input. During initial power up, the state of MO and M1 determines the configuration mode. After configuration, a rising edge on \(\sim\) RT initiates a configuration read operation.

\section*{M1-~RD}

Dual function input/output. During initial power up, the state of M1 and M0 determines the configuration mode. After configuration is complete, \(\sim\) RD outputs configuration data during a configuration read back operation synchronously with the toggling of the CCLK input.

\section*{~RESET}

Input. A low level on this input after configuration causes all register elements internal to the LCA to be forced to 0 . If asserted prior to the start of configuration, causes the LCA to remain in the initialization state (configuration is not started). If asserted during configuration the LCA returns to the initialization state.

\section*{DONE-~PG}

Dual function output/input. During configuration the LCA pulls DONE low and releases it when configuration is complete (output is open drain). After configuration is complete, a falling edge on \(\sim\) PG initiates an LCA programming cycle (if enabled in the current configuration). This pin has an internal user-enabled pull-up resistor.

\section*{XTAL1-I/O}

Dual function input and \(\mathrm{I} / \mathrm{O}\). This pin may be configured by the user to be a normal I/O pin equivalent to any of the general purpose I/O pins. Alternatively, this pin and XTAL2 may be used to connect a crystal for use with the internal crystal oscillator configuration.

\section*{XTAL2-I/O}

Dual function output and \(\mathrm{I} / \mathrm{O}\). This pin may be configured by the user to be a normal I/O pin equivalent to any of the general purpose I/O pins. Alternatively, this pin and XTAL1 may be used to connect a crystal for use with the internal crystal oscillator configuration.

\section*{CCLK}

Configuration mode dependent input/output. CCLK is the master configuration clock used to configure the LCA. In slave mode it is an input; in all other modes it is an output designed to provide the input clocking of additional slave mode daisy chain connected LCA devices. During a configuration read back operation, CCLK serves as the clock input used to read the internal configuration data.

\section*{DOUT-I/O}

Dual function output and I/O. General purpose user-configurable I/O pin during normal operation. During configuration, the serial data stream supplied from the first LCA to LCAs down the serial daisy chain is output on DOUT.

\section*{~RCLK-I/O}

Dual function output and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, a low level output on \(\sim\) RCLK indicates that the external memory device is being accessed.

\section*{DO-DIN-I/O}

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 0 of the 8 -bit parallel input data bus (DO). During slave mode or peripheral mode configuration, this pin is the serial input data pin (DIN).
D1-~WS-I/O
Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 1 of the 8 -bit parallel input data bus (D1). During peripheral mode configuration, a low level on \(\sim W S\) indicates that a write operation is being performed by the controlling processor. See note.

\section*{D2-CS-I/O}

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 2 of the 8 -bit parallel input data bus (D2). During peripheral mode configuration, a high level on CS indicates that a write operation is being performed by the controlling processor. See note.

\section*{D3-~CEO-I/O}

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 3 of the 8 -bit parallel input data bus (D3). During peripheral mode configuration, a low level on~CEO indicates that a write operation is being performed by the controlling processor. See note.

\section*{D4-~CE1-I/O}

Multi-function input and I/O. General purpose user-configurable I/O pin during normal operation. During master mode configuration, this pin is bit 4 of the 8 -bit parallel input data bus (D4). During peripheral mode configuration, a low level on~CE1 indicates that a write operation is being performed by the controlling processor. See note.

\section*{D5-I/O to D7-I/O}

Input and I/O. General purpose user-configurable I/O pins during normal operation. During master mode configuration, these pins are bits 5 through 7 of the 8 -bit parallel input data bus (D5-D7).

\section*{A0-I/O to A15-I/O}

Output and I/O. General purpose user-configurable I/O pins during normal operation. During master mode configuration these pins are address output pins (AO-A15) used to address the external storage element used for configuration data.

Note: to perform a peripheral mode write, the following logical combination is necessary: \(\sim\) WS . CS \(\cdot \sim\) CEO \(\cdot \sim\) CE1.

\section*{Functional Description}

The M2064 is a high-performance CMOS Logic Cell Array providing superior system performance with greatest user flexibility. Complete user-configurability provides an optimized solution to logic implementation problems.
The M2064 utilizes a unique Configurable Logic Block (CLB) structure as the basic functional building block of the device. Each CLB is a combination of a programmable logic function and a storage element. The CLB has the capability of performing any function of its inputs with the option of the output of the storage element included in the input field. User-defined logic is implemented in a matrix of sixty-four CLBs which are interconnected with user-configurable interconnect resources.
Fifty-eight independently configurable I/O Blocks; each of which can be a direct or latched input, a direct or open drain output, or a bidirectional I/O buffer; provide the interface to external circuits. Input voltage levels are user definable and may be either standard TTL or CMOS for all I/O Blocks, depending on the user's configuration choice.
User-definable path selector or multiplexers are utilized to select configuration options for the CLBs and I/O Blocks. These selectors are set in the desired state by the configuration data loaded into the device upon power up.

\section*{Logic}

User logic is implemented in one or more CLBs which are general purpose 4-input, 2-output elements. Figure 1 shows a block diagram of a single CLB. Each element is composed of a 4-input combinational logic module with two outputs, a general purpose storage element, and routing selection logic. The module can generate any combinational logic function of the four inputs, or it can generate any two independent functions of any three of the four inputs. If a function of four inputs is selected, that same function will be available on both of the outputs of the combinational module. The inputs to the combinational module are three of the four inputs to the CLB (A, B and C) and either the D input to the CLB, or the Q output of the storage element.
The general purpose storage element has a data input, a clock input, a set direct input, a reset direct input and an output, Q. The storage characteristic may be defined as either a transparent latch or as an edge-triggered flip-flop. The data input is connected to one of the outputs of the combinational logic module. The set direct and reset direct inputs may be individually enabled or disabled.
The reset direct input, if enabled, may come from either the \(D\) input to the CLB, or from the G output of the combinational logic module. Set direct control, if enabled, can come from either the A input to the CLB or from the F output of the combinational logic module.

Clock for the storage element may be individually enabled or disabled and can be driven by the clock input, \(K\), to the CLB, the C input to the CLB, or the G output of the combinational logic module. Final outputs, \(X\) and \(Y\), from the CLB can be selected to be either of the two outputs, F and G, of the combinational logic module, or the Q output from the storage element.


Figure 1. Block Diagram of a Single CLB

\section*{I/O Elements}

The M2064 contains fifty-eight user-configurable I/O blocks for connection to external circuits. Each block is a general purpose device containing a three-state output buffer, an input buffer, and an input flip-flop as shown in Figure 2. The input buffer always reflects the status of the I/O pin or the contents of the input flip-flop. If the flip-flop is selected, data present on the I/O pin will be clocked to the input buffer by the I/O block clock signal. All I/O blocks on a particular edge of the device share a common I/O clock signal. The output buffer may be enabled, disabled, or under the control of the three-state connection.


Figure 2. Block Diagram of an I/O Element

\section*{Interconnect}

There are nine rows and nine columns of metal interconnect resources with one row or column located between each row or column of CLBs or I/O blocks. Each row or column of interconnect resources contains local use lines, long lines and programmable interconnect points between I/O blocks, CLBs and interconnect resources. Local lines run either vertically from one row of resources to the adjacent row or horizontally from one column to the adjacent column. Long lines run the full height or width of the device. At the intersection of every row and column of interconnect resources are user configurable interconnect elements which allow multiple combinations of connections between local lines in adjacent rows and columns. In addition, selected intersections of local and long lines can be connected by user programmable interconnect points.
Inputs and outputs from each CLB or I/O block have programmable connections to the interconnect resources in the adjacent rows and columns. These connections allow CLBs or I/O block connections to be made for proper signal routing to or from the I/O blocks or CLBs. In addition to the programmable connections to adjacent interconnect resources, there are direct connection paths which do not utilize the general interconnect resources. These paths allow selected connection between some I/O blocks and CLBs and between adjacent CLBs. For example, the outputs of a CLB in the interior of the matrix of CLBs may be connected to adjacent CLBs without using any interconnect resources.


Figure 3. Overview Functional Layout of the M2064

\section*{Clock Generation and Buffering}

The M2064 contains two special purpose clock buffers for generating and driving clock signals to multiple CLBs or I/O blocks
with negligible skew. The Global Clock Buffer, is dedicated to driving a matrix of long lines which have configurable connections to the K input of each CLB register. This clock buffer may be driven from an internally generated register source, or configured with a connection directly to an I/O block for driving it with an external clock signal. The output from the Global Clock Buffer may be configured to directly drive an I/O block for driving clock signals off the device.

The alternate clock buffer can be configured either as a simple buffer or as a buffer for the crystal oscillator. In the crystal oscillator mode, an externally connected crystal and optional passive components form a clock generator for use on the chip or for driving other external circuits (see Figure 4). When configured in the buffer mode, the alternate clock buffer can have either one or both of its input and output configured to directly drive, or be driven by, an I/O block. The output of the alternate clock buffer can drive long lines in any column of CLBs as well as local interconnect.


Suggested component values:
\begin{tabular}{ll} 
R1 & \begin{tabular}{l}
\(1-4 \mathrm{M} \Omega\) \\
R2
\end{tabular} \\
& \begin{tabular}{l}
\(0-1 \mathrm{~K} \Omega\) \\
(may be required for \\
shift and/or compe
\end{tabular} \\
C1, C2 & \(5-20 \mathrm{pF}\) \\
Y1 & \begin{tabular}{l}
\(1-10 \mathrm{MHz}\) AT cut
\end{tabular}
\end{tabular}

Figure 4. Crystal Oscillator
Each CLB has a special clock input (K) which can be selected as the clock input of the storage element. Clock inputs to user selected CLBs can be configured to be driven from either the Global Clock Buffer, the oscillator/buffer or from other local interconnect. Clocks to the I/O blocks can be configured from either of the clock buffers or the local interconnect.

\section*{Programming}

Configuration of the device may be performed in any one of three modes. The desired configuration mode is set by the state of the mode pins M0 and M1 at power up (see Table 1). All configuration data relating to CLB function definition, interconnect resource utilization, and I/O block programming must be loaded into the device prior to use. In the peripheral and slave modes the data is supplied in a serial stream in conjunction with the configuration clock signal, CCLK. In master mode, the device automatically loads data from an external memory device by supplying addresses and reading bytes of data. In all modes the data patterns required to create a specific configuration are the same.
\begin{tabular}{|l|c|c|}
\hline \multicolumn{1}{|c|}{ MODE SELECT PINS } & M0 & M1 \\
\hline \hline Master LOW mode & 0 & 0 \\
\hline Master HIGH mode & 0 & 1 \\
\hline Peripheral mode & 1 & 0 \\
\hline Slave mode & 1 & 1 \\
\hline
\end{tabular}

Note: During configuration, Pin 27 on the 68 -pin package or Pin 7 on the 48-pin package must be held HIGH.

\section*{Table 1. Modes}

Data patterns for a specific user-configuration are created with the Monolithic Memories XACT LCA Development System and can be output to a standard EPROM programmer or saved on disk for inclusion with other software. Users who are using the Monolithic Memories XACT debugging system can directly access the configuration data and load the device directly during a debug session. Because of the complexity of the data patterns and difficulty in generating them without a thorough knowledge of the device, users are discouraged from attempting to generate data patterns on their own. Data pattern files for M2064 devices contain 1536 bytes.

\section*{Special Features}

The M2064 contains several special features which enhance its capacity for use in a wide variety of applications. Among these are the following:

\section*{Data Security}

The M2064 configuration data contains special control bits which enable or disable configuration data security control. If enabled, the security control will prevent the read-back of configuration data after the initial configuration. There are two possible modes of operation under security control. One mode allows a single read-back after configuration to allow verification of the data. In the second mode, all access to the configuration data is prevented.

\section*{Reprogrammability}

Configuration data changes are controlled by reprogramming control bits in the configuration data supplied to the device. If reprogramming is enabled, the user may supply new configuration data at any time by asserting the correct control sequence on the DONE-~PG and M0 and M1 mode control pins. Alternatively, the user may elect to prevent reconfiguration of the device. When operating in this mode, the only method to remove the configuration is to remove all power from the device.

\section*{Inactive Power-down}

In a system which is to remain in its current configuration through power loss, the M2064 may be forced into a low power inactive state by using the \(\sim\) PWRDN pin. When held low, the LCA will retain all configuration data but will not operate. All clocks will be stopped and all outputs put into a high-impedance state. Power is reduced to a very low level, allowing a simple external battery arrangement to supply the required configuration data saving power (see electrical characteristics).

\section*{Configuration Data Read-back}

A mechanism is provided in the M2064 to provide verification of stored configuration data. The configuration read-back is initiated by toggling the \(\sim\) RT pin and clocking the CCLK pin. Each clock applied to CCLK will read out a configuration data bit on the \(\sim\) RD pin. When all configuration data has been read out, the \(\sim\) RD pin will return to its inactive state. The configuration data may be read at any time with no effect on the operation of the device. Once a configuration read-back has been initiated, all data must be read out of the device to insure that subsequent read-back operations will begin at the start of the configuration data.

\section*{Master Reset}

After device configuration, the \(\sim\) RESET pin becomes a master reset for all CLB and IOB storage elements in the device. Asserting this control signal will asynchronously reset all of the internal storage registers regardless of the operating condition of the circuit.

\section*{Development System}

The Monolithic Memories Design System is an integrated package of design tools for developing configuration data for LCAs. All aspects of configuration are specified through interactive graphics software. Facilities to verify functionality and timing of the designed configuration insure that designs operate as desired.
XACT is a graphic design system used to specify LCA designs. It contains several standard and several optional software and hardware packages. The basic package runs on an IBM PC/XT or AT compatible computer with 640K memory, a color monitor and a mouse. The tools accessible from the executive, including the optional packages, are:
- LCA Editor and Macros
- Timing Analyzer
- Simulator (P-Silos, optional)
- Configuration-File Generator
- Configuration-File Formatter
- XACTOR 2 In-circuit-emulator (optional).

XACTOR 2 consists of a software program plus a hardware attachment that allows control of up to four LCAs. The program contains commands for:
- Loading configuration data
- Activating the Master Reset input
- Reconfiguring
- Single stepping the device clock
- Reading back configuraiton data and state of all 122 internal registers on any clock cycle.
- Real time system debug.

An evaluation kit is available which includes:
- Complete documentation of the Development System
- A sample LCA design
- XACT software package.

Contact your local Monolithic Memories Representative or Distributor for more information.

\section*{Absolute Maximum Ratings*}

Power down \(V_{\text {CC }}\).................................................................................................................. 2 V to 7 V
Input voltage .................................................................................................... -0.5 V to \(\mathrm{V}_{\mathrm{CC}} 0.5 \mathrm{~V}\)

Storage temperature range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . \(-65^{\circ} \mathrm{C}\) to \(+150^{\circ} \mathrm{C}\)
Lead temperature (soldering, 10 seconds) .................................................................................. \(260^{\circ} \mathrm{C}\)
"Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those listed under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" conditions for extended periods of time may affect device reliability.

\section*{Operating Conditions}
\begin{tabular}{|l|l|l|c|}
\hline SYMBOL & PARAMETER & MIN TYP & MAX \\
\hline \hline\(V_{\text {CC }}\) & UNIT \\
\hline\(V_{\text {IHT }}\) & High level input voltage-TTL configuration & 4.75 & 5.25 \\
\hline\(V_{\text {IHC }}\) & High level input voltage-CMOS configuration & 2.0 & \\
\hline\(V_{\text {ILT }}\) & Low level input voltage-TTL configuration & 0.7 & V \\
\hline\(V_{\text {ILC }}\) & Low level input voltage-CMOS configuration & 0 & V \\
\hline\(l_{\text {IT }}\) & Input leakage current-TTL configuration & 0 & 0.8 \\
\hline\(I_{\text {IC }}\) & Input leakage current-CMOS configuration & \(\pm 1\) & 0.2 \\
\hline\(l_{\mathrm{OZ}}\) & Three-state output off current \(\left(\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}\right)\) & \(\pm\) \\
\hline \(\mathrm{t}_{\mathrm{OP}}\) & Operating free-air temperature & \(\pm 10\) & \(\mu \mathrm{~A}\) \\
\hline
\end{tabular}

\section*{Electrical Characteristics Over Operating Conditions}
\begin{tabular}{|l|l|l|l|c|c|}
\hline SYMBOL & \multicolumn{1}{|c|}{ PARAMETER } & \multicolumn{1}{|c|}{ TEST CONDITION } & MIN TYP & MAX & UNIT \\
\hline \hline \(\mathrm{V}_{\mathrm{OH}}\) & High level output voltage & \(\mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}\) & \(\mathrm{I}_{\mathrm{OH}}=-4.0 \mathrm{~mA}\) & 3.86 & \\
\hline \(\mathrm{~V}_{\mathrm{OL}}\) & Low level output voltage & \(\mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}\) & \(\mathrm{IOL}=4.0 \mathrm{~mA}\) & & 0.32 \\
\hline \multirow{2}{*}{I CCO} & \begin{tabular}{l} 
Quiescent operating \\
power supply current
\end{tabular} & CMOS inputs & \(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\) & V \\
\cline { 2 - 6 } & TTL inputs & \(\mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\) & 5 & mA \\
\hline \(\mathrm{I}_{\mathrm{CCPD}}\) & Power down supply current & \(\mathrm{V}_{\mathrm{CC}}=2.0 \mathrm{~V}\) & Consult factory & V \\
\hline
\end{tabular}

Note: All switching characteristics are at worst case conditions.

\section*{Power on Timing}

The M2064 contains on-chip reset timing logic for power-up operation. To insure proper master mode system operation, VCC must rise from 2.0 V to minimum specification level in 10 ms or
less. For other modes, initiation of configuration must be delayed for 60 ms after VCC reaches the minimum specified level.

Switching Characteristics-CLB
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{ITEM} & \multirow[t]{2}{*}{DESCRIPTION} & \multicolumn{2}{|r|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|r|}{M2064-20} & \multirow[t]{2}{*}{UNIT} \\
\hline & & MIN & TYP MAX & MIN & TYP & MAX & MIN & & MAX & \\
\hline tilo & Input through logic to \(X\) or \(Y\) & & 15 & & & 20 & & & 35 & ns \\
\hline \(\mathrm{t}_{17 \mathrm{O}}\) & Input through logic and latch to X or Y & & 20 & & & 25 & & & 45 & ns \\
\hline \({ }^{\text {t CKO }}\) & Storage element clock from K to output & & 15 & & & 20 & & & 35 & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CCO}\) & Storage element clock from C to output & & 19 & & & 25 & & & 45 & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{ClO}\) & Logic to storage element clock to output & & 27 & & & 37 & & & 65 & ns \\
\hline \({ }^{\text {t QLO }}\) & Storage element \(Q\) to logic to output & & 8 & & & 13 & & & 30 & ns \\
\hline \(\mathrm{t}_{\mathrm{ICK}}\) & Input setup to K clock to storage element & 8 & & 12 & & & 22 & & & ns \\
\hline \({ }^{\text {t }} \mathrm{CKI}\) & Input hold to K clock to storage element & 0 & & 0 & & & 0 & & & ns \\
\hline ticc & Input setup to C clock to storage element & 9 & & 12 & & & 18 & & & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CCl}\) & Input hold to C clock to storage element & 0 & & 6 & & & 10 & & & ns \\
\hline \({ }^{t} \mathrm{Cl}\) & Input setup to input clock to storage element & 4 & & 6 & & & 10 & & & ns \\
\hline \({ }^{\text {t }} \mathrm{Cl}\) & Input hold to input clock to storage element & 5 & & 9 & & & 15 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{RIO}}\) & Input to storage element Reset/Set to output & & 22 & & & 25 & & & 45 & ns \\
\hline \(t_{\text {t }}\) & Logic to storage element Reset/Set to output & & 28 & & & 37 & & & 65 & ns \\
\hline \({ }^{\text {t RPW }}\) & Reset/Set pulse width & 9 & & 12 & & & 20 & & & ns \\
\hline \(t_{\text {RS }}\) & Storage element control separation & 9 & & 17 & & & 30 & & & ns \\
\hline \({ }^{t} \mathrm{CH}\) & Storage element clock high time & 9 & & 12 & & & 20 & & & ns \\
\hline \({ }^{\text {t }} \mathrm{CL}\) & Storage element clock low time & 9 & & 12 & & & 20 & & & ns \\
\hline \({ }^{\mathrm{f}} \mathrm{CLK}\) & Storage element clock frequency & & 50 & & & 33 & & & 20 & MHz \\
\hline \({ }^{\text {t MRQ }}\) & Master reset to storage element Q to output & & 25 & & & 35 & & & 60 & ns \\
\hline
\end{tabular}

\section*{Cross Reference Guide}

Cross Reference Guide
\begin{tabular}{|l|c|c|c|c|}
\hline \multirow{2}{*}{ XILINX } & \multirow{2}{*}{\begin{tabular}{c} 
MONOLITHIC \\
\\
\\
\\
MEMORIES
\end{tabular}} & \multicolumn{2}{|c|}{ VCC } & \multirow{2}{*}{ FMAX } \\
\cline { 3 - 4 } & & MIN & MAX & \\
\hline \hline XC-2064-1 & & 4.5 V & 5.5 V & 20 MHz \\
\hline & M2064-20 & 4.75 V & 5.25 V & 20 MHz \\
\hline XC-2064-2 & & 4.5 V & 5.5 V & 33 MHz \\
\hline XC-2064-33 & M2064-33 & 4.75 V & 5.25 V & 33 MHz \\
\hline XC-2064-50 & M2064-50 & 4.75 V & 5.25 V & 50 MHz \\
\hline
\end{tabular}
*For commercial product only.

\section*{Switching Characteristics - CLB}


Note: 1. Input refers to CLB inputs A, B, C or D
2. Output refers to CLB output \(X\) or \(Y\)
3. Clock refers to the CLB storage element clock
4. FF (Flip-Flop) or L (Latch) refers to the CLB storage element
5. Set and Reset refer to CLB storage element controls

\section*{Switching Characteristics-IOB}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{ITEM} & \multirow[t]{2}{*}{DESCRIPTION} & \multicolumn{3}{|c|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|c|}{M2064-20} & \multirow[t]{2}{*}{UNIT} \\
\hline & & MIN & & MAX & MIN & TYP & MAX & MIN & & MAX & \\
\hline \({ }^{\text {t PID }}\) & Pad to input direct & & & 8 & & & 12 & & & 20 & ns \\
\hline \({ }^{\text {tPL }}\) & Pad input setup to I/O clock & 8 & & & 12 & & & 20 & & & ns \\
\hline \({ }_{\text {t }}\) LP & Pad input hold to I/O clock & 0 & & & 0 & & & 0 & & & ns \\
\hline \(f_{L}\) & Frequency, I/O clock & & & 50 & & & 33 & & & 20 & MHz \\
\hline t LW & Pulse width input latch clock & 9 & & & 12 & & & 20 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{LI}}\) & Input latch clock to input & & & 15 & & & 20 & & & 30 & ns \\
\hline \({ }^{\text {t }} \mathrm{OP}\) & Output to pad output (three-state enabled) & & & 12 & & & 15 & & & 25 & ns \\
\hline \({ }^{\text {T }}\) HZ & Three-state inactive to high impedance & & & 20 & & & 25 & & & 35 & ns \\
\hline \({ }^{\text {TOM }}\) & Three-state active to output on & & & 20 & & & 25 & & & 40 & ns \\
\hline \(t_{\text {RI }}\) & Master Reset to latched input reset & & & 25 & & & 30 & & & 50 & ns \\
\hline
\end{tabular}


Note: 1. Output (O) refers to the output connection on the \(1 O B\)
2. Input (I) refers to the input connection on the IOB
3. Three-state ( \(T\) ) refers to the three-state control on the IOB
4. Pad or Pin (P) refers to the device pin connected to the IOB
5. Latch (L) refers to the input Flip-Flop clock connection

\section*{Switching Characteristics-Programming - Slave Mode}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[b]{2}{*}{ITEM} & \multirow[b]{2}{*}{DESCRIPTION} & \multicolumn{3}{|c|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|c|}{M2064-20} & \multirow[b]{2}{*}{UNIT} \\
\hline & & MIN & TYP & MAX & MIN & TYP & MAX & MIN & & MAX & \\
\hline \({ }^{\text {t }} \mathrm{CCH}\) & CCLK high time & 300 & & & 300 & & & 500 & & & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CCL}\) & CCLK low time & 200 & & & 200 & & & 300 & & & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CCL}\) & CCLK low time & & & 5000 & & & 5000 & & & 10000 & ns \\
\hline \({ }^{t} \mathrm{DCC}\) & DIN data setup to CCLK rising edge & 25 & & & 25 & & & 50 & & & ns \\
\hline \({ }^{t} \mathrm{CCD}\) & DIN data hold from CCLK rising edge & 40 & & & 40 & & & 75 & & & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CCO}\) & DOUT data delay from CCLK falling edge & & & 65 & & & 65 & & & 100 & ns \\
\hline \({ }^{\mathrm{f}} \mathrm{CC}\) & CCLK maximum frequency & & & 2 & & & 2 & & & 1 & MHz \\
\hline
\end{tabular}

\section*{Switching Characteristics-Programming - Peripheral Mode}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline & \multirow[b]{2}{*}{DESCRIPTION} & \multicolumn{3}{|c|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|c|}{M2064-20} & \multirow[b]{2}{*}{UNIT} \\
\hline ITEM & & MIN & TYP & MAX & MIN & TYP & MAX & MIN & TYP & MAX & \\
\hline \({ }^{\text {t }} \mathrm{CA}\) & Control input active period & 200 & & & 200 & & & 300 & & & ns \\
\hline \({ }^{\text {t }} \mathrm{CA}\) & Control input active period & & & 5000 & & & 5000 & & & 10000 & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{Cl}\) & Control input inactive period & 150 & & & 150 & & & 250 & & & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CCC}\) & CCLK delay from control input edge & & & 75 & & & 75 & & & 100 & ns \\
\hline \({ }^{\text {t }}\) DC & DIN setup to control transition & 35 & & & 35 & & & 50 & & & ns \\
\hline \({ }^{\text {t }} \mathrm{CD}\) & DIN hold from control transition & 5 & & & 5 & & & 10 & & & ns \\
\hline
\end{tabular}

Notes: 1. Peripheral mode timing determined from last control signal ( \(\sim\) CEO,\(\sim\) CE1, \(\sim\) WS, CS) to transition to active or inactive state.
2. CCLK timing minima and maxima same as for slave mode.
3. CCLK and DOUT timing same as for slave mode.


\section*{Switching Characteristics-Programming - Master Mode}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline \multirow[t]{2}{*}{ITEM} & \multirow[t]{2}{*}{DESCRIPTION} & \multicolumn{3}{|c|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|c|}{M2064-20} & \multirow[t]{2}{*}{UNIT} \\
\hline & & & & MAX & MIN & TYP & MAX & & & MAX & \\
\hline \({ }^{\text {t }}\) ARC & Address invalid prior to \(\sim\) RCLK edge & & & 0 & & & 0 & & & 0 & ns \\
\hline \(t_{\text {t }}\) & Address valid from ~RCLK edge & & & 200 & & & 200 & & & 300 & ns \\
\hline \({ }^{\text {t DRC }}\) & Data bus setup to \(\sim\) RCLK edge & 60 & & & 60 & & & 100 & & & ns \\
\hline \(t_{\text {RCD }}\) & Data bus hold from ~RCLK edge & 0 & & & 0 & & & 0 & & & ns \\
\hline \({ }^{\text {tr }} \mathrm{CH}\) & \(\sim\) RCLK high & 600 & & & 600 & & & 600 & & & ns \\
\hline \({ }^{\text {tr }}\) CL & ~RCLK low & 4000 & & & 4000 & & & 4000 & & & ns \\
\hline
\end{tabular}

Note: Timing for DOUT and CCLK out is same as for slave mode.


\section*{Switching Characteristics-Program Readback}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline EM & \multirow[t]{2}{*}{DESCRIPTION} & \multicolumn{3}{|c|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|c|}{M2064-20} & \multirow[t]{2}{*}{UNIT} \\
\hline & & MIN & TYP & MAX & MIN & TYP & MAX & MIN & & MAX & \\
\hline \({ }^{\text {tr }}\) RTH & Read trigger (RT) high time & 150 & & & 150 & & & 250 & & & ns \\
\hline \(t_{\text {RTCC }}\) & Delay from RT assertion to first CCLK & 60 & & & 60 & & & 100 & & & ns \\
\hline \({ }^{\text {t CCRD }}\) & Delay from CCLK edge to RD data valid & & & 60 & & & 60 & & & 100 & ns \\
\hline \({ }^{\text {t DRT }}\) & Wait period from DONE to RT assertion & 75 & & & 175 & & & 300 & & & ns \\
\hline
\end{tabular}

Notes: 1. Timing for CCLK is same as for slave programming mode.
2. DONE/~PG output/input must be high (device programmed) prior to assertion of \(\sim\) PG.


\section*{Switching Characteristics-General}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|c|c|c|}
\hline ITEM & \multirow[t]{2}{*}{DESCRIPTION} & \multicolumn{3}{|c|}{M2064-50} & \multicolumn{3}{|c|}{M2064-33} & \multicolumn{3}{|c|}{M2064-20} & \multirow[t]{2}{*}{UNIT} \\
\hline & & MIN & & MAX & MIN & & MAX & MIN & & MAX & \\
\hline \(t_{\text {VMR }}\) & Master Reset delay from valid \(\mathrm{V}_{\mathrm{CC}}\) & 150 & & & 150 & & & 250 & & & ns \\
\hline \({ }^{\text {tMRW }}\) & Master Reset pulse width & 150 & & & 150 & & & 250 & & & ns \\
\hline \({ }^{\text {tMR }}\) & Mode control setup to Master Reset & 60 & & & 60 & & & 100 & & & ns \\
\hline \(\mathrm{t}_{\mathrm{RM}}\) & Mode control hold from Master Reset & 7 & & & 7 & & & 10 & & & ns \\
\hline \({ }^{\text {tPGW }}\) & Program control pulse width & 6000 & & & 6000 & & & 6000 & & & ns \\
\hline \({ }^{\text {tPGI }}\) & Program control to I/O initialized & & & 7000 & & & 7000 & & & 7000 & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CLH}\) & Clock buffer input high time & 9 & & & 12 & & & 20 & & & ns \\
\hline \({ }^{\mathrm{t}} \mathrm{CLL}\) & Clock buffer input low time & 9 & & & 12 & & & 20 & & & ns \\
\hline \({ }^{\mathrm{f}} \mathrm{CL}\) & Clock buffer input frequency & & & 50 & & & 33 & & & 20 & MHz \\
\hline
\end{tabular}


\section*{Test Conditions:}

Outputs loaded with rated DC current and 50-pF capacitance to GND.

\section*{Design Aids}

XACT \({ }^{\text {M }}\) provides complete design automation for users to specify and implement designs utilizing Monolithic Memories' LCA products. Configuration of CLBs, internal routing, I/O block definitions and global routing are all handled in an integrated, easy-to-use system.
Placement and routing of logic and I/O blocks is accomplished using interactive graphics. Final programming bit patterns are automatically produced for debugging, transfer to other systems, or downloading to standard EPROM programmers. Debugging with the XACTOR \(2^{\text {Tm }}\) emulation system allows full device emulation and operation analysis in the target system.
The user inputs data via a graphics-oriented physical editing environment. User functions are translated into CLB logic specifications and interconnections automatically. Standard
logic libraries and other macro capabilities can be utilized for rapid design entry.

Physical placement and hard connections are performed with the graphics placement and connection capabilities. Final device layout and routing are visible and can be modified without disturbing the logical arrangement. Logical connectivity and physical layout rules checking are performed automatically.

Full timing analysis and functional simulation of user configurations allows device performance and functional checking without external test hardware. In addition, point-to-point path timing calculation capability is provided to simpiify generai timing analysis and critical path determination.
The debugging system provides full emulation in the user's target system. User configurations may be transferred directly from the design phase into the target system and tested through the emulation system.
Additional capabilities include a tool for automatic hard copy generation of the user's logic design and physical implementation and a tool for transferring programming bit patterns to EPROM programming systems.

\section*{Recommended Sockets}

The following 68-pin PLCC sockets have been evaluated by Monolithic Memories and have been found to exhibit acceptable connectivity, device retention and device extraction characteristics:
\begin{tabular}{|l|l|l|}
\hline VENDOR & \multicolumn{1}{|c|}{ DESCRIPTION } & \multicolumn{1}{|c|}{ PART NUMBER } \\
\hline \hline AMP & PCB solder tail, tin plate & \(821574-1\) \\
\hline AMP & Surface mount, tin plate & \(821542-1\) \\
\hline Burndy & PCB solder tail, tin plate & QILE68P-410T \\
\hline \begin{tabular}{l} 
Midland- \\
Ross
\end{tabular} & PCB solder tail, tin plate & \(709-2000-068-4-1-1\) \\
\hline
\end{tabular}


The following 68-pin PLCC sockets are also available:
\begin{tabular}{|c|c|c|}
\hline VENDOR & DESCRIPTION & \multicolumn{1}{|c|}{ PART NUMBER } \\
\hline \hline Methode & PCB solder tail, tin plate & \(213-068-001\) \\
\hline Methode & Surface mount, tin plate & \(213-068-002\) \\
\hline
\end{tabular}

Notes: 1. The standard device extraction tools supplied with the XACT development system will work with all of the above sockets.
2. All of the above PCB solder tail sockets have the same hold pattern and pinout.



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\begin{tabular}{|c|c|}
\hline Introduction & 1 \\
\hline \multicolumn{2}{|l|}{Military Products Division} \\
\hline PROM & 3 \\
\hline \multicolumn{2}{|l|}{PLE \({ }^{\text {TM }}\) Devices} \\
\hline \multicolumn{2}{|l|}{PAL® Devices 5} \\
\hline \multicolumn{2}{|l|}{HAL \(^{\circledR} /\) ZHAL \(^{\text {M }}\) Devices} \\
\hline \multicolumn{2}{|l|}{System Building Blocks/HMSI \({ }^{\text {rm }}\)} \\
\hline \multicolumn{2}{|l|}{FIFO 8} \\
\hline \multicolumn{2}{|l|}{Memory Support 9} \\
\hline \multicolumn{2}{|l|}{Arithmetic Elements and Logic 10} \\
\hline \multicolumn{2}{|l|}{Multipliers 11} \\
\hline \multicolumn{2}{|l|}{8-Bit Interface 12} \\
\hline
\end{tabular}

\section*{Double-Density PLUS \({ }^{\text {TM }}\) Interface 15}

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\section*{Clock Frequency}

\section*{Maximum clock frequency, \(\boldsymbol{f}_{\text {max }}\)}

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

\section*{Current}

High-level input current, \(I_{\mathbf{I}}\)
The current into* an input when a high-level voltage is applied to that input.
High-level output current, \(\mathbf{I}_{\mathbf{O H}}\)
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

\section*{High-level output current, ICEX}

The high-level leakage current of an open collector output.

\section*{Low-level input current, IIL}

The current into* an input when a low-level voltage is applied to that input.
Low-level output current, \(\mathrm{I}_{\mathrm{OL}}\)
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.
Off-state (high-impedance-state) output current (of a threestate output), IOZ
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

\section*{Short-circuit output current, IOS}

The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

\section*{Supply current, ICC}

The current into* the \(\mathrm{V}_{\mathrm{CC}}\) supply terminal of an integrated circuit.
*Current out of a terminal is given as a negative value.

\section*{Hold Time}

\section*{Hold time \(t_{h}\)}

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

\section*{Output Enable and Disable Time}

Output enable time (of a three-state output) to high level, tPZH (or low level, tpZL)
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.
Output enable time (of a three-state output) to high or low level, \({ }^{\text {tPZX }}\)
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).
Output disable time (of a three-state output) from high level, \({ }^{\text {tpHZ }}\) (or low level, tpLZ)
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.
Output disable time (of a three-state output) from high or low level, \(t_{\text {PXZ }}\)
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.
\({ }^{t} E A\) is the output enable access time of memory devices.
\({ }^{\text {t }}\) ER is the output disable (enable recovery) time of memory devices.

\section*{Propagation Time}

\section*{Propagation delay time, t \(_{\text {PD }}\)}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.
Propagation delay time, low-to-high-level output, tPLH
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
Propagation delay time, high-to-low-level output, tPHL
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
\({ }^{t_{A A}}\) is the address (to output) access time of memory devices.

\section*{Pulse Width}

Pulse width, \(\mathrm{t}_{\mathrm{w}}\)
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

\section*{Setup Time}

\section*{Setup time, \(\mathrm{t}_{\text {su }}\)}

The time interval between the application of a signal that is maintained at one specified input terminal and a consecutive active transition at another specified input terminal

NOTES: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the device is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the device is guaranteed.

\section*{Voltage}

\section*{High-level input voltage, \(\mathbf{V}_{\mathbf{I H}}\)}

An input voltage within the more positive (less negative) of the two ranges of values assumable by a binary variable.
NOTE: A minimum is specified that is the least positive value of high-level voltage for which operation of the logic element within specification limits is guaranteed.

\section*{High-level output voltage, \(\mathrm{V}_{\mathrm{OH}}\)}

The voltage at an output terminal with input conditions applied that will establish a high level at the output. The actual input conditions needed are determined by the individual product specification.

\section*{Input clamp voltage, \(\mathbf{V}_{\text {IC }}\)}

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.
Low-level input voltage, \(\mathbf{V}_{\mathbf{I L}}\)
An input voltage level within the less positive (more negative) of the two ranges of values assumable by a binary variable.
NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

\section*{Low-level output voltage, \(\mathbf{V}_{\mathbf{O L}}\)}

The voltage at an output terminal with input conditions applied that will establish a low level at the output. The actual input conditions needed are determined by the individual product specification.

\section*{Negative-going threshold voltage \(\mathbf{V}_{\mathbf{T}}\) -}

The voltage level at an input that causes a transition as the input voltage falls from a level above the positive-going threshold voltage, \(\mathrm{V}_{\mathrm{T}+}\).

\section*{Positive-going threshold voltage, \(\mathbf{V}_{\mathbf{T}+}\)}

The voltage level at an input that causes a transition as the input voltage rises from a level below the negative-going threshold voltage, \(\mathrm{V}_{\mathrm{T}-}\).

\section*{Truth Table Explanations}
\(\mathrm{H}=\) high level (steady-state)
L = low level (steady-state)
1 = transition from low-to-high level
\(1 .=\) transition from high-to-low level
\(X \quad=\) don't care (any input, including transitions)
\(Z \quad=\) off (high-impedance) state of a three-state output
a..h = the level of steady-state inputs at inputs \(A\) through \(H\) respectively
\(Q_{0}=\) level of \(Q\) before the indicated steady-state input conditions were established
\(\bar{Q}_{0}=\) complement of \(Q_{0}\) or level of \(\bar{Q}\) before the indicated steady-state input conditions were established
\(Q_{n}=\) level of \(Q\) before the most recent active transition indicated by 1 or 1

If, in the input columns, a row contains only the symbols \(\mathrm{H}, \mathrm{L}\), and/or \(X\), this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists as long as the input configuration is maintained.
If, in the input columns, a row contains \(\mathrm{H}, \mathrm{L}\), and/or X together with \(t\) and/or \(\downarrow\), this means the output is valid whenever the input configuration is achieved and the indicated transition has occured (the transition(s) must occur following the achievement of the steady-state levels). If the output is shown as a level ( \(\mathrm{H}, \mathrm{L}\), \(Q_{0}\), or \(\bar{Q}_{0}\) ), it persists as long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output.


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\section*{PAL® Devices 20D Series}

\section*{/ / / / / /////////////////////|///////|/|/|/|/|||||ADVANCE INFORMATION}

\section*{Features/Benefits}
- 10 ns maximum propagation delay
- \(8 \mathbf{n s}\) maximum delay from clock input to data output
- f MAX \(=55.5 \mathrm{MHz}\)
- Advanced oxide-isolated technology
- Programmable replacement for TTL logic
- Reduces chip count by greater than 4:1
- Instant prototyping and easier board layout
- Programmable on standard programmers
- Programmable three-state outputs
- Security fuse prevents duplication
- 20-pin DIP and PLCC packages

\section*{Description}

The PAL20D Series provides the highest speed available for TTL PAL devices. The 10 ns maximum propagation delay is a \(33 \%\) speed improvement over the 20B Series from Monolithic Memories, at no increase in power consumption. The 20D Series is functionally compatible with the earlier 20, 20A and 20B Series.
The PAL20D Series utilizes Monolithic Memories' advanced oxide-isolated process and proven TiW fuse link technology.

\section*{Areas of Application}
- Control logic for mainframe and super-minicomputers
- Computer-aided graphics
- High-performance communication equipment
- High-speed test instruments

\section*{Features}

The PAL20D Series includes the four standard 20-pin PAL device architectures. All four devices have sixteen array inputs and eight outputs, with varying numbers of registers: zero (16L8), four (16R4), six (16R6), and eight (16R8). The combinatorial outputs on the registered devices, and six of the outputs on the 16L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.
These features allow a great deal of flexibility for the design engineer when using the devices. The four different devices offer an optimized number of registers, while the number of inputs and combinatorial outputs can be balanced for the particular application. All of these features are automatically handled by the CAD software used to describe the design. Monolithic Memories' PALASM \({ }^{\circledR} 2\) software and third-party CAD tools all offer full support for these products.

\section*{Pin Configurations}


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\section*{Ordering Information}


\section*{fMAX Parameters}

The parameter fMAX is the maximum speed at which the PAL device is guaranteed to operate. Because flexibility inherent to PAL devices allows a choice of clocked flip-flop designs, for the convenience of the user, fMAX is specified to address two major classes of synchronous designs.
The simplest type of synchronous design can be described as a data path application. In this case, data is presented to the data terminal of the flip-flop and clocked through; no feedback is employed (Figure 1). Under these conditions, the frequency of

\section*{Programming}

The PAL20D Series is programmable on the same standard programmers as the rest of the 20-pin PAL device products. No upgrades are necessary. The configuration required is the same as that for the standard \(20,20 \mathrm{~A}\), and 20 B Series.

\section*{Logic Development Software}

The following logic development software packages can be used for configuring the PAL20D Series:
PALASM \({ }^{\oplus}\), from Monolithic Memories
ABEL \({ }^{\text {™ }}\), from Data I/O Corporation
CUPL™ , from Assisted Technology, Inc.
operation is limited by the greater of the data setup time ( \(t_{\mathrm{su}}\) ) or the minimum clock period ( \(\mathrm{t} w\) high \(+\mathrm{t} w\) low). This parameter is designated fMAX (no feedback).
For synchronous sequential designs, i.e., state machines, where logical feedback is required, inputs to flip-flop data terminals originate from the device input pins or flip-flop outputs via the internal feedback paths (Figure2). Under these conditions, fMAX is defined as the reciprocal of ( \(\mathrm{t}_{\text {su }}+\mathrm{t}_{\text {CLK }}\) ) and is designated \({ }^{\mathrm{f}}\) MAX (feedback). For the PAL20D Series, this value calculates as \(1 /(10+8)=55.5 \mathrm{MHz}\).


Figure 1. Data Path Register Configuration Without Feedback


Figure 2. State Machine Configuration With Feedback
\(A B E L^{\text {™ }}\) is a trademark of Data I/O Corporation.
CUPL \({ }^{\text {T }}\) is a trademark of Assisted Technology, Inc.

\author{
ZHAL'M24A Series \\ Zero-Power Hard Array Logic
}

\section*{/ / / / / /|/|||||||||||||||||||||||||||||||||||||ADVANCE INFORMATION}

\section*{Features/Benefits}
- CMOS technology provides zero standby power
- 25 ns maximum propagation delay (20L8, 20R4, 20R6 and 20R8)
- Low power mask-programmed alternative for most 24-pin PAL® devices
- Space-saving 24-pin SKINNYDIP® or 28-pin PLCC and LCC packages
- Available in Commercial, Industrial and Military operating ranges

\section*{Description}

The ZHAL24A Series is a mask-programmed, zero-power option to most of the 24-pin PAL devices. The ZHAL24A Series offers not only higher density than the ZHAL20 Series, but also improved speed, matching the bipolar speeds of the Small 24 and Medium 24A, 24XA and 24RS PAL device series.

\section*{Design Procedures}

ZHAL device prototyping can be done using standard PAL devices before converting to the ZHAL device for production. ZHAL devices are fabricated by Monolithic Memories with a custom mask defined by a user-supplied HAL® device Design Specification. The ZHAL24A Series utilizes a unique architecture that can implement \(90 \%\) of the 24 -pin PAL device patterns. To determine whether a given pattern will fit, run the ZHAL24 option in the PALASM®2 software package. Patterns that could not fit in the ZHAL20 Series will fit in the 20-pin option of the ZHAL24A Series.

\section*{ZHAL24A Device Options (continued on back)} 20L8


\section*{Areas of Application}
- Portable computers
- Battery-operated instrumentation
- Low-power industrial or military equipment
- Standard CMOS/TTL logic replacement
- CMOS gate array alternative Preliminary Data
(Commercial operating conditions, 20L8, 20R4, 20R6 and 20R8) (other families may differ)
\begin{tabular}{ll}
\(\mathrm{t}_{\mathrm{PD}}=25 \mathrm{~ns}\) & \(\mathrm{t}_{\mathrm{CLK}}=15 \mathrm{~ns}\) \\
\(\mathrm{t}_{\mathrm{Su}}=25 \mathrm{~ns}\) & fMAX \(=28.5 \mathrm{MHz}\)
\end{tabular}
\(\mathrm{V}_{\mathrm{OH}}=3.76 \mathrm{~V}\) at \(\mathrm{I}_{\mathrm{OH}}=-6 \mathrm{~mA}\) (HCT compatible)
\(\mathrm{VOL}_{\mathrm{OL}}=0.4 \mathrm{~V}\) at \(\mathrm{IOL}=8 \mathrm{~mA}\)
\(\operatorname{ICC}(\) standby \()=100 \mu \mathrm{~A}\)
ICC (operating) \(=5 \mathrm{~mA}\) at \(1 \mathrm{MHz}(+3 \mathrm{~mA}\) per additional 1 MHz )
Ordering Information

\(20 R 8\)


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ZHAL \(^{\text {™ }}\) is a trademark of Monolithic Memories.
TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
}


\section*{PAL10H20P8}

\section*{/ / / / / / / /////////////////////////////////|/||/|ADVANCE INFORMATION}

\section*{Features/Benefits}
- 20 logic inputs; 12 external, 8 feedback
- 8 outputs
- Programmable output polarity
- ECL technology for ultra-high speed
- 32 product terms with term sharing
- 10KH ECL compatible
- \(50 \Omega\) termination drive
- Input pull-down resistors
- Voltage compensated
- 24-pin SKINNYDIP® package
- Programmable using standard TTL programmers

\section*{Description}

The PAL10H20P8 is a 10KH compatible ECL PAL® device having twelve dedicated inputs and eight outputs with feedback. A programmable AND array and a fixed OR array make possible a wide variety of logic functions.
Device functionality can be specified using standard sum-ofproducts expressions. Logic development software is then used to transform the Boolean equations into a fuse map for use in programming the device.

\section*{Features}

Each output has a polarity fuse. Programmable polarity allows the user to optimize his design equations without using DeMorgan's theorem to give the correct output polarity. This can simplify the design and save product terms.

The programmable AND array contains a total of thirty-two product terms. Product terms are arranged in groups of eight. The terms in each group can be shared mutually exclusively between two output cells.

\section*{Device Programmer Support}

The PAL10H20P8 can be programmed using the following systems:

Data I/O LogicPak \({ }^{\text {tw }}\) V04, P/T Adapter 303A-ECL
Family Pinout Code 22-42
Kontron EPP-80, Family Pinout Code 22-42

\section*{Logic Development Software Support}

The following logic development software packages can be used for configuring the PAL10H20P8:

PALASM® 2, Ver. 2.19, from Monolithic Memories, Inc. ABEL'T, Ver. 2.0, from Data I/O Corp.

\section*{Preliminary Data}
6.0 ns propagation delay

210 mA maximum IEE current

\section*{Areas of Application}

High-performance communication equipment
Glue logic joining ECL gate arrays
High-speed test instruments
Control logic for mainframe and super-mini computers
Computer-aided graphics

\section*{Pin Configuration}


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\section*{Logic Diagram}


\section*{CMOS ZPAL™ 24 Series}

\section*{Features/Benefits}
- CMOS technology provides zero standby power
- Lowest power 24-pin PAL® device family; consumes only \(3 \mathrm{~mA} / \mathrm{MHz}\)
- 35 ns maximum propagation delay
- Programmable replacement for CMOS/TTL logic
- Reduces chip count by greater than six to one
- Instant prototyping and easier board layout
- HC/HCT compatible for use in CMOS or TTL systems
- Offered over both the Commercial and Industrial temperature ranges
- Low-cost, one-time programmable SKINNYDIP® and PLCC packages save board space

\section*{Description}

The CMOS ZPAL24 Series offers the first family of PAL devices with true CMOS power consumption. Under standby conditions (inputs and clock not changing), the devices consume a maximum current of \(100 \mu \mathrm{~A}\), less than \(1 \%\) that of the quarter-power PAL devices. This low power consumption allows the devices to be powered by a battery almost indefinitely.

While operating, the devices consume additional power only when the inputs or clock change. Power consumption is directly proportional to the frequency of changes to the inputs. ICC is therefore specified as 3 mA per 1 MHz of operating frequency, starting from 5 mA at 1 MHz . Thus, the maximum current at 8 MHz would be \(5 \mathrm{~mA}+7 \times 3 \mathrm{~mA}\), or 26 mA .

The devices have HC and HCT compatible inputs and outputs for use in CMOS and TTL systems. This feature allows the ZPAL

\section*{Pin Configurations}

circuits to be used for direct replacement of discrete CMOS as well as TTL logic.

\author{
Areas of Application \\ - Portable computers \\ - Battery-operated instrumentation \\ - Low-power industrial equipment \\ - Standard CMOS/TTL logic replacement
}

\section*{Features}

The CMOS ZPAL24 Series includes the four standard 24-pin PAL device architectures. All four devices have twenty array inputs and eight outputs, with varying numbers of registers: zero (20L8), four (20R4), six (20R6), and eight (20R8). The combinatorial outputs on the registered devices, and six of the outputs on the 20L8, are I/O pins that can be individually programmed as inputs or outputs. Each output register, a D-type flip-flop, also feeds back into the array, for implementation of synchronous state machine designs. Registered outputs are enabled by an external input, while the combinatorial outputs use a product term to control the enable function.

The basic PAL device architecture is a programmable AND array feeding a fixed OR array. The programmable AND array consists of a set of cells similar to those used in EPROMs. Erasable by UV light, the cells can be programmed and erased in the factory to ensure \(100 \%\) programming and functional yields.
Windowed packages will be made available in the future, allowing erasure in the field. Windowed packages allow easy prototype testing and reconfiguration.

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ZPAL \(^{\text {™ }}\) is a trademark of Monolithic Memories. ABEL \({ }^{\text {™ }}\) is a trademark of Data I/O Corporation. CUPLT is a trademark of Assisted Technology.
}

\section*{Ordering Information}


\section*{Programming}

The ZPAL24 Series is programmable using the same standard programmers used for other PAL devices. The CMOS programming algorithm is different from that for the bipolar PAL devices, and requires a different family code.

\section*{PLCC Logic Symbols}

ZPAL20L8CNL


ZPAL20R6CNL


ZPAL20R8CNL


ZPAL20R4CNL


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\section*{Features/Benefits}
- User-programmable synchronous state machine
- 25 MHz maximum frequency for compatibility with 12.5 MHz processors
- 14 inputs ( 8 external), 8 outputs, 128 states
- PAL® array optimizes product terms and states
- Internal feedback adds versatility and control
- Optimized for four-way branching
- User-selectable asynchronous initialize or asynchronous enable function
- Power-up reset for start-up in known state
- Diagnostics-On-Chip \({ }^{\text {TM }}\) shadow register eases chip and board-level testing
- PROSE device software makes it easy to "write your sequencer in PROSE"
- Programmed on standard logic programmers
- Security fuse prevents pattern duplication
- Space-saving 24-pin 300-mil SKINNYDIP \({ }^{\circledR}\) and 28 -pin PLCC and LCC packages

\section*{Block Diagram}


\section*{Definition of Signals}
\begin{tabular}{ll}
\(10-17\) & Primary inputs to the PAL array \\
Q0-Q7 & Outputs from the register \\
\(\mathrm{I} / \mathrm{E}\) & Programmable asynchronous initialize (I) \\
& or asynchronous enable (E)
\end{tabular}
\begin{tabular}{ll} 
CLK & Clock for output register \\
DCLK & Clock for diagnostic register \\
MODE & Selects diagnostic functions \\
SDI & Serial data input to shadow register \\
SDO & Serial data output from shadow register
\end{tabular}

ABEL \({ }^{\text {tw }}\) is a trademark of Data I/O Corporation.
PROSE Part Numbering System


\section*{Diagnostics-On-Chip Feature}

The PMS14R21 is the newest member of the Diagnostics-OnChip family. These devices incorporate a serial shadow register on-chip which facilitates board-level testing. The shadow register has a Serial Data Input (SDI), Serial Data Output (SDO) and its own clock (DCLK). The MODE control configures the shadow register either in parallel with the output register or in serial shift mode (see function table). Other devices with this feature are listed below.

\section*{Diagnostics Family Members}
\begin{tabular}{|l|l|}
\hline \multicolumn{1}{|c|}{ PART NUMBER } & \multicolumn{1}{|c|}{ DESCRIPTION } \\
\hline \hline \(53 / 63 D A 441\) & 1K \(\times 4\) PROM (async. enables) \\
\hline \(53 / 63 D A 442\) & 1K \(\times 4\) PROM (async./sync. enables) \\
\hline \(53 / 63 D A 841\) & 2K \(\times 4\) PROM \\
\hline \(53 / 63 D 1641\) & 4K \(\times 4\) PROM (async. enable) \\
\hline \(53 / 63 D A 1643\) & 4K \(\times 4\) PROM (async. initialization) \\
\hline \(54 / 74 \mathrm{~S} 818\) & 8-bit register \\
\hline
\end{tabular}

\section*{Software Support}

PROSE device software from Monolithic Memories provides full support for the PMS14R21. Based on PALASM \({ }^{\circledR} 2\) syntax, the software automatically converts a state machine description directly into the PAL and PROM array fuse maps, for downloading to a programmer. The syntax supports both Mealy and Moore state machine models, and makes optimal use of the features of the PROSE device. Simulation support is also provided, both for design checking and for generation of test vectors for device testing. Additional support is available from thirdparty software vendors, including the ABEL \({ }^{\text {TM }}\) package from Data I/O.

\section*{Programming}

Both the PAL and PROM arrays are programmed on standard logic programmers using the JEDEC programming format. The TiW fuses program from the low to the high state. Programming also sets the architectural fuse which selects between asynchronous initialize or asynchronous output enable; the unprogrammed state is initialize. If asynchronous initialize is selected, asserting the pin low will set all outputs and feedback bits high.

\section*{Power-up Reset}

Power-up reset is provided for system start-up in a known state. It has the same effect as initialization; all output register bits go high.

\section*{Diagnostic Function Table}
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline \multicolumn{4}{|c|}{INPUTS} & \multicolumn{3}{|c|}{OUTPUTS} & \multirow{2}{*}{OPERATION} \\
\hline MODE & SDI & CLK & DCLK & \(\mathrm{Q}_{20} \mathrm{Q}_{0}\) & \(\mathrm{S}_{20} \mathrm{~S}_{0}\) & SDO & \\
\hline L & X & 1 & * & Qn \(\leftarrow\) PROM & HOLD & \(\mathrm{S}_{20}\) & Load output register from PROM array \\
\hline L & X & * & \(\dagger\) & HOLD & \[
\begin{aligned}
& s_{n}-s_{n-1} \\
& s_{0}-s_{D I}
\end{aligned}
\] & \(\mathrm{S}_{20}\) & Shift shadow register data \\
\hline L & X & \(\dagger\) & \(\uparrow\) & Qn \(\leftarrow\) PROM & \[
\begin{aligned}
& s_{n} \leftarrow s_{n-1} \\
& s_{0} \leftarrow s_{D I}
\end{aligned}
\] & \(S_{20}\) & Load output register from PROM array while shifting shadow register data \\
\hline H & X & \(\dagger\) & * & \(\mathrm{Q}_{\mathrm{n}} \leftarrow \mathrm{S}_{\mathrm{n}}\) & HOLD & SDI & Load output register from shadow register \\
\hline H & L & * & \(\dagger\) & HOLD & \(S_{n} \leftarrow Q_{n}\) & SDI & Load shadow register from output bus and feedback \\
\hline H & H & * & 1 & HOLD & HOLD & SDI & \(\dagger\) No operation \\
\hline
\end{tabular}

\footnotetext{
* Clock must be steady or falling.
\(\dagger\) Reserved operation for 54/74S818 8-Bit Diagnostic Register.
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}

High Speed Programmable Array Logic PAL32VX10 PAL32VX10A
U.S. Patent 4124899

\section*{Features/Benefits}
- 10 input/output macrocells
- Programmable registered or combinatorial outputs
- Dual independent feedback paths allow I/O with combinatorial or feedback register outputs
- Programmable flip-flops allow J-K, S-R, T or D types
- Programmable output polarity
- Register set and register reset can be asynchronous or synchronous
- Automatic register preset on power up
- Varied product term distribution
- Up to 16 product terms per output
- Pin compatible functional superset of 22V10
- Maximum propagation delay
- 25 ns "A"
- 35 ns "STD"
- 24-pin 300-mil-wide SKINNYDIP® package or 28-pin chip carriers save space

\section*{General Description}

The PAL32VX10 is a high-density Programmable Array Logic device which implements the familiar sum of products transfer function via a user-programmable AND array and a fixed OR array. Featured are ten highly flexible input/output macrocells which are user configurable for combinatorial or registered operation. Each flip-flop is also programmable to be either J-K, S-R, T, or D-types for optimal design of state machines and other synchronous logic. In addition, a unique dual feedback architecture allows I/O capability for each macrocell in both combinatorial or registered configurations, even when register feedback is present, and allows implementation of buried registers while preserving the macro input function. Supplied in space-saving 300 -mil-wide dual in-line packages or 28-pin chip carriers, the PAL32VX10 offers a powerful, space-saving alternative to SSI/MSI logic devices, while providing the advantage of instant prototyping over other semicustom approaches.
The PAL32VX10 is fabricated in Monolithic Memories' advanced, oxide isolated bipolar process for high speed and low power. TiW fuse links provide high reliability and programming yields. Special on-chip test circuits allow full AC, DC, and functional testing before programming. Preloadable output registers facilitate functional testing.
The PAL32VX10 can be programmed on standard PAL® device programmers, fitted with appropriate programming modules and configuration software. Design development is supported by Monolithic Memories' PALASM® \({ }^{\circledR}\) software as well as by other programmable logic CAD tools available from third-party vendors.

\section*{Logic Symbol}


\section*{PAL32VX10 PAL32VX10A}

The PAL32VX10 is a pin-compatible functional superset of the 22 V 10 architecture, with an improved macrocell. Details of the PAL32VX10 macrocell are shown in the diagram below. Significant features of the macrocell are:
Dual Feedback Paths. Each macrocell has two completely independent feedback paths associated with each macrocell. One feeds back into the array from the macrocell output pin. The second feeds back into the array from the flip-flop output. This architecture provides I/O capability for both combinatorial and registered outputs, even when register feedback is needed. In addition, it allows registers to be loaded directly from outputs, and provides the capability for buried registers, while permitting use of the macrocell pin as an input.
Programmable Flip-Flops. Each macro has an XOR gate which provides the capability of emulating the operation of \(J-K, S-R, T\), or D flip-flops. When J-K or S-R flip-flops are implemented, the
available product term resources for each macrocell are shared between \(J(S)\) and \(K(R)\) functions, according to the expression:
\[
Q:=Q:+:\left(J_{1} \ldots J_{m}\right) * / Q+\left(K_{1} \ldots K_{n}\right) * Q
\]
where \((m+n)\) is the total number of product terms found in each macrocell.
Varied Product Term Distribution. The PAL32VX10 has a different number of product terms for each pair of macrocells. There are two macros each with \(8,10,12,14\), or 16 product terms, to allow optimal use of the available product term resources.
Other Features:
- Macrocells programmable as registered or combinatorial
- Programmable output polarity
- Preset and reset can be synchronous or asynchronous

\section*{PAL32VX10 MACROCELL}


\section*{PAL32VX10 MACROCELL CONFIGURATION OPTIONS}

The PAL32VX10 can implement any of the architecture options shown

\section*{COMBINATORIAL I/O}


\section*{BURIED REGISTER WITH DEDICATED INPUT}


\section*{D REGISTER WITH I/O}


J-K REGISTER WITH I/O


T REGISTER WITH I/O


\section*{Logic Diagram}


\section*{Monolithic M.M \\ Memories}

> PLE5P16 REVISED PLE6P16 Programmable Logic Element Family

\section*{}

\section*{Features/Benefits}
- Programmable replacement for conventional TTL logic
- Reduces IC inventories and simplifies their control
- Expedites and simplifies prototyping and board layout
- Saves space with 24 -pin 0.3 inch SKINNYDIP® packages and 28-pin Plastic Leaded Chip Carriers (PLCC)
- Programmed on standard PROM programmers
- Reliable TIW fuses guarantee \(>99 \%\) programming yields
- Test and simulation made simple with PLEASM \({ }^{\text {ru }}\) software
- Proposed JEDEC standard pinout
- Revised pinout with center VCC and GND for higher noise immunity

\section*{Description}

The PLE5P16 and PLE6P16 are the two newest members of the Programmable Logic Element (PLE \({ }^{\text {TM }}\) ) Family. A PLE device has a programmable OR-array, preceded by a fixed AND-array. This provides unlimited product terms and programmable polarity for each output, while maintaining the high speeds necessary for logic applications. The PLE Family complements the PAL® (Programmable Array Logic) Family, which has programmability in the opposite array.
The PLE5P16 has five inputs, sixteen outputs, and thirty-two product terms per output. The PLE6P16 has six inputs, sixteen

\section*{Typical Applications}
- Address decoding
- Random logic replacement
- Code converters
- Look-up tables (both trigonometric and arithmetic)
- Data scaling

\section*{Preliminary Data}
\begin{tabular}{|l|c|c|}
\hline PARAMETER & PLE5P16 & PLE6P16 \\
STANDARD & STANDARD \\
\hline\(t_{\mathrm{PD}}(\mathrm{ns})\) & 15 & 15 \\
\hline \(\mathrm{I}_{\mathrm{CC}}(\mathrm{mA})\) & 180 & 190 \\
\hline
\end{tabular}
outputs, and sixty-four product terms per output.
The devices feature low-current PNP inputs and full Schottky clamping; the PLE5P16 has three-state outputs with an output enable. The fuses store a logical low and are programmed to the high state. Special on-chip circuitry and extra fuses provide pre-programming testing which assures high programming yields and high reliability.

\section*{Loyic Symbols}


\section*{Ordering Information}

PLE Family


\section*{Block Diagrams (DIP Pinout)}

PLE5P16


Pin Configurations

PLE5P16


PLE6P16


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\section*{Monolithic Memories}

16-Bit
Barrel Shifter Slice
677530

\section*{/ / / //////////////////////|/|/|/|/|/|/|/||||||||ADVANCE INFORMATION}

\section*{Features/Benefits}
- Left/Right shift and rotate to any position within 1 cycle
- Expandable to any multiples of \(\mathbf{1 6}\)-bit paths
- Works on sign magnitude and two's complement shift count inputs
- High speed operation:

Data to output: \(\quad 25\) ns (max)
Shift count to output: \(\mathbf{3 0}\) ns (max)
- Sticky bit available for floating point rounding operation
- Bit insert and bypass operations

\section*{Applications}
- Mantissa adjustment for floating point addition/ subtraction and fixed point scaling in minicomputers, mainframes, array processors and digital signal processors
- Positioning non-numeric patterns in image processing, word processing and symbol processing systems
- Implement a funnel shifter for the Bit Block Transfer operation in graphics
- Implement a compression-expansion engine using the modified Huffman coding method
- Bit insertion for EDAC applications


16-Bit Barrel Shifter Slice

\section*{Packaging Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline 677530 & D48 & Commercial \\
\hline
\end{tabular}

\section*{Pin Configuration}

677530



Figure 1. Internal Organization of the ' 7530 Barrel Shifter Slice

\section*{Description}

The '7530 16-Bit Barrel Shifter Slice is designed to be used as a general-purpose one-cycle shifter in numerical processing and symbol processing systems. The basic slice can handle data in 16 -bit packets, shift and rotate to any desired number of positions within one cycle. They can also be cascaded together to form a barrel shifter function module with longer word length. Cascading shifter slices to form a functional module will not put additional delays into the datapath.
The ' 7530 can perform nine different operations. A 3-bit opcode (12-10) and the \(\overline{\text { PI }}\) (Polarity Insertion) input determines which function is to be performed. The shift count for the device is determined by the 4 -bit input ( \(\mathrm{S} 3-\mathrm{SO}\) ). The entire shifter is combinatorial with no internal states.

All data outputs (Y15-Y0) can be tristated. This output design is crucial to the cascading architecture because outputs from different barrel shifter slices will be tied together in an expanded array. The \(\overline{O E R}, \overline{O E L}\) (Output Enable Right/Left) and the LID (Location IDentifier) input signals together determine the enable states of each individual output.
The \(F\) (Fill) input bit provides the signal to be inserted into the outputs.
The \(\overline{Y_{s}}\) output (Sticky Bit) is provided as an open collector output. It is the negation of the logical OR of all the bits shifted out during the shift left or shift right operation.
The \(\overline{\text { PI (Polarity/Insertion) input is used to complement the }}\) outputs for all the opcodes except when \(\mathrm{I}=010\) when it is used to distinguish between Bit InserT and BYPass operation.

\section*{Architecture}

As shown in Figure 1, the architecture of the '7530 Barrel Shifter Slice is centered around the internal barrel shifter array and the shift count decoder. The outputs of the array are fed into a mask generator which determines the enable states of each individual data outputs. These enable states are primarily determined by the LID (Location IDentifier) input signal that represents the location of each shifter slice when they are cascaded. The Location IDentifier will transform the actual operation of every shifter to make cascading possible. Please refer to the section Cascading Architecture for the Barrel Shifter Slice for a detailed description.
The output control circuitry consists of the polarity control, Fill bit insertion and Sticky Bit generation.
Two enable inputs, OEL and OER, provide the tristate control to the two portions of the output data separated by the left margin (D15) of the original input data.

\section*{Signal Description}

D15-D0: Inputs. Input data to the Barrel Shifter Slice.
Y15-Y0: Outputs. Output data from the Barrel Shifter Slice.
12-10: Inputs. A 3-bit opcode to select one of nine possible operations for the device. Please see Table 1 for further detail.
S3-S0: Inputs. Shift count input. For opcodes 00X or 11X (i.e., I2I1IO = 0, 1, 6 or 7), S3-S0 represent the magnitude of bit positions shifted or rotated. For opcodes \(10 \times\) (i.e., \(121110=4\) or 5 ), the number of bits to be shifted or rotated is given by the two's complement of the five-digit number: I2S3S2S1S0. Since \(12=1\) in both cases, only sixteen different bit positions (ranging from +1 to +16 ) are allowed within one cycle. For the opcodes X01 (i.e., 121110=1 or 5), the shift count inputs can be considered in two ways: either as a rotate right two's complement I2S3S2S1S0 operation or as a rotate left S3S2S1S0 operation when \(12=0\).
\(\overline{\text { PI: Input. Polarity/Insertion signal input. This signal serves }}\) two purposes. When the opcode is 010 (i.e., \(121110=2\) ), it is used to resolve between Bit InserT operation ( \(\overline{\mathrm{PI}}=0\) ) and BYPass operation ( \(\overline{P I}=1\) ). When the opcode is in some other states, \(\overline{P I}\) determines the output data polarity ( \(\overline{\mathrm{P}}=0\) for complemented data, \(\overline{\mathrm{PI}}=1\) for uncomplemented (true) data).

F: Input. Fill bit input. The value of this input is used to insert into positions left empty from shift operations, or insert into the designated bit positions for the Bit InserT and FILL operations.
\(\overline{\mathrm{Ys}}\) : Output. The inverse of the sticky bit. This is an open collector output signal. Functionally this signal is the negation of the logical OR of the bits shifted out in the shift left/right operations. In the Bit Insertion operation, \(\overline{\mathrm{Ys}_{s}}\) is the negation of the input bit that is replaced by the Fill bit.
LID: Input. Location IDentifier. The input to this pin can either be VCC, ground, or left open. In the case when the input is open, there is an internal resistor network to divide this signal to 2.5 V (VCC/2). The LID signal is used in the expansion scheme of the barrel shifter slices. Different barrel shifter slices can be cascaded in a two-dimensional array to form a barrel shifter module of wider path width. The LID input signal is required to be one of the above three states according to its position inside the array.
OEL, \(\overline{\text { OER: In }}\) Inputs. Output enable left and output enable right. These two signals will separately enable the left and the right halves of the output data separated by the left margin (D15) of the input word.
GNDE, GNDT: Power supply grounds. GNDE is the internal ECL circuit ground and GNDT is the internal TTL cricuit ground. These two ground signals should be routed separately in the system. The ECL ground is more sensitive to noise problems and should be bypassed with capacitive components to VCC.
VCC: Power supply. A \(+5 \vee\) power supply to the internal circuit of the Barrel Shifter Slice.

\section*{Function Tables}
\begin{tabular}{|c|c|c|c|c|c|c|c|c|}
\hline \multicolumn{3}{|c|}{OPCODE} & \multirow[t]{3}{*}{POLARITY/ INSERT \(\overline{\mathbf{P}}\)} & \multicolumn{2}{|r|}{\multirow[t]{2}{*}{OPERATION PERFORMED IF LID PIN IS "OPEN"}} & \multirow[t]{3}{*}{OUTPUT POLARITY} & \multicolumn{2}{|l|}{ALTERNATE OPERATION} \\
\hline \multirow[b]{2}{*}{12} & & & & & & & LID \(=\) & LID = \\
\hline & 11 & 10 & & MN. & NAME & & VCC & GND \\
\hline 0 & 0 & 0 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & LSH & Left SHift & Complemented True & LRT & FIL \\
\hline 0 & 0 & 1 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & LRT & Left RoTate & Complemented True & LRT & LRT \\
\hline 0 & 1 & 0 & 0 & BIT & Bit InserT & True & High Z & High Z \\
\hline & & & 1 & BYP & BYPass & True & High Z & High Z \\
\hline 0 & 1 & 1 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & FIL & FILL & Complemented True & \begin{tabular}{l}
High Z \\
High Z
\end{tabular} & High Z High Z \\
\hline 1 & 0 & 0 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & RSC & Right Shift with two'sComplement shift count & Complemented True & FIL & RRC \\
\hline 1 & 0 & 1 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & RRC & Right Rotate with two'sComplement rotate count & Complemented True & RRC & RRC \\
\hline 1 & 1 & 0 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & RSH & Right SHift & Complemented True & FIL & RRT \\
\hline 1 & 1 & 1 & \[
\begin{aligned}
& 0 \\
& 1
\end{aligned}
\] & RRT & Right RoTate & Complemented True & RRT & RRT \\
\hline
\end{tabular}

Figure 1. Shifter Instruction Set

\footnotetext{
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}

\section*{Features/Benefits}
- 16x16 parallel multiplier
- High speed multiply
- 35 ns Max '7016-35/'7017-35
- 45 ns Max '7016-45/'7017-45
- 55 ns Max '7016-55/'7017-55
- Low power CMOS technology
- Zero standby power
- 7 mA per MHz active ICC (Typical)
- Mixed mode 2's complement, unsigned or mixed operand
- '7017 is optimized for microprocessor systems, single clock with register enables
- Plug-in compatible with TRW MPY016H/K, AMD29516/A, 29517/A
- Single 5 V supply
- Available in DIP or PLCC

\section*{Functional Block Diagrams}


\section*{Packaging Information}
\begin{tabular}{|c|c|c|c|}
\hline \begin{tabular}{c} 
PART \\
NUMBER
\end{tabular} & \begin{tabular}{c} 
SPEED \\
(TMC)
\end{tabular} & PACKAGE & TEMP \\
\hline \hline \(67 \mathrm{C} 7016-35\) & 35 ns & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(68)\) & Com \\
\hline \(67 \mathrm{C} 7017-35\) & 35 ns & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(68)\) & Com \\
\hline \(67 \mathrm{C} 7016-45\) & 45 ns & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(68)\) & Com \\
\hline \(67 \mathrm{C} 7017-45\) & 45 ns & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(68)\) & Com \\
\hline \(67 \mathrm{C} 7016-55\) & 55 ns & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(68)\) & Com \\
\hline \(67 \mathrm{C} 7017-55\) & 55 ns & \(\mathrm{~J}, \mathrm{~N}, \mathrm{NL}(68)\) & Com \\
\hline
\end{tabular}

This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

\section*{Pin Configurations}


\section*{Pin Configurations}


\section*{Descriptions}

The '7016/7017 are CMOS \(16 \times 16\) high speed parallel multipliers. Designed with state-of-the-art CMOS technology and a multiplication scheme based on modified Booth's algorithm, these devices can achieve bipolar TTL speed at a significantly reduced power level. In addition, the product is designed to be pin-for-pin replacement for the TRW MPY016H/K and the AMD 29516/A, 29517/A.

The architecture of the '7016/7017 family generates a 32-bit product of two 16 -bit input operands. Two 16 -bit registers are provided for the \(X\) and \(Y\) operands. These operands can be specified as either 2's complement or unsigned numbers through the XM and the YM control inputs. These two signals are registered simultaneously at their respective operand clocks.
At the output of the multiplier array a format adjust control (FA) allows the user to select either a full 32-bit product or a left shifted 31 -bit product. Two 16 -bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by FA. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high. A round control (RND) allows the rounding of the MSP. This control is registered, and is entered at the rising edge of the logical OR of both CLKX and CLKY for the '7016 and is enabled by a LOW signal in either ENX or ENY in the '7017. the two halves of the product may be routed to a 16 -bit three-state output port ( \(P\) ) via a multiplexer. In addition the LSP is connected to the \(Y\)-input port through a separate three-state buffer so that a 32-bit product can be available simultaneously.
In the '7016, the X, Y, MSP and LSP registers have independent clocks (CLKX, CCLKY, CLKM, CLKL). The output multiplexer control (MSPSEL) uses a pin which is a supply ground in the TRW MPY16H. When this control is LOW the function is that of the MPY16H, thus allowing full compatibility.
The ' 7017 differs in that it has a single clock input (CLK) and three register enables ( \(\overline{\mathrm{ENX}}, \overline{\mathrm{ENY}}, \overline{\mathrm{ENP}}\) ) for the two input registers and the entire product. This facilitates the use of the part in microprocessor systems. In both parts data is entered into the registers on the positive edge of the clock.
The '7016/7017 family has a wide variety of applications in high performance computers and digital signal processing. In computer applications this multiplier can be used to construct numerical processing functional units (e.g., array processors, matrix processors, floating point multiplier/dividers etc.). In digital signal processing the multiplier can be used to construct special algorithm engines for applications like digital filtering, FFT, speech recognition and synthesis, adaptive controls and image processing.

\section*{Signal Description}

\section*{Input/Output data}

X15-X0: 16 bit data inputs.
Y15-Y0: 16 bit data inputs. These inputs are multiplexed with the least significant product (LSP) outputs.
P15-P0: The least significant product (LSP) outputs. These signals are multiplexed with the Y data inputs. The product term is available when OEL is low. Alternatively, these outputs can be accessed from the MSP output port when MSPSEL is high.

P31-P16: The most significant product (MSP) outputs.

\section*{Input Clocks (67C7016 only)}

CLKX: The rising edge of this clock loads the input data (X15-X0) and the associated mode control signal XM into the input register.
CLKY: The rising edge of this clock loads the input data (Y15-Y0) and the associated mode control signal YM into the input register.
CLKM: The rising edge of this clock loads the most significant product (MSP) output register.
CLKL: The rising edge of this clock loads the least significant product (LSP) output register.
Input Clocks (67C7017 only)
CLK: The rising edge of this clock loads all input/output registers.
ENX: Clock enable for the X15-X0 input register, XM input register and the round register.
ENY: \(\quad\) Clock enable for the Y15-Y0 input register, YM input register and the round register.
ENP: Clock enable for the most significant product (MSP) and least significant product (LSP) register.

\section*{Control Signals}

XM, YM: Mode control signals for the input data word. A low input indicates unsigned data format and a high input represents 2's complement data format.
FA: Format Adjust. When this input is high, a full 32-bit product is produced in MSP and LSP registers. When this input is low, the sign bit will appear in the most significant bit of both the MSP and the LSP. In such cases only a 31-bit product is provided. The FA input is required to be a high when either integer unsigned magnitude or mixed mode formats are used. (See the DATA FORMATS section for further detail.)
FT: Flow-through. When this input is high, both the MSP register and the LSP register are transparent.
\(\overline{\text { OEL: }} \quad\) Three-state enable signal for routing LSP to the Y/LSP I/O ports.
©EP: Three-state enable signal for the product output port.
RND: Round control signal for the most significant product (MSP). When this input is high, a one will be added to the most significant bit of the least significant product (LSP). This rounding operation is done before the output is sent to the format adjust clock. As a result, the location of this round bit in the final product depends on the FA input. When \(F A=0\), the round bit is added to location \(P 14\); when \(F A=1\), the round bit is added to location P15. The RND input is registered at the rising edge of the logical \(O R\) of both the CLKX and CLKY. In the single clock architecture, the RND register is enabled when either the \(X\) register or the \(Y\) register is enabled.
MSPSEL: When the MSPSEL input is low, the MSP is available for the output port. When this input is high, the LSP is available at the output port.

\section*{Features/Benefits}
- Twos-complement, unsigned, or mixed operands
- Full 32-bit product immediately available on each cycle
- High-speed \(16 \times 16\) parallel multiplier
- Latched or registered inputs/outputs
- Three-state output controls, independent for each half of the product
- Single +5 V supply (via multiple pins)
- Zero standby power CMOS technology
- Available in 84-terminal Leadless-Chip Carrier and 88-Pin-Grid-Array packages

\section*{Description}

The 'C7555 and 'C7556 are high-speed \(16 \times 16\) combinatorial multipliers which can multiply two 16 -bit unsigned or signed twos-complement numbers on every cycle. Each operand \(X\) and \(Y\) has an associated mode-control line, XM and YM respectively. When a mode-control line is at a LOW logic level, the operand is treated as an unsigned 16-bit number; when the mode-control line is at a HIGH logic level, the operand is treated as a 16-bit signed twos-complement number. Additional inputs RS and RU allow the addition of a bit into the multiplier array at the appropriate bit positions for rounding.

\section*{Ordering Information}
\begin{tabular}{|c|c|c|}
\hline PART NUMBER & PACKAGE & TEMPERATURE \\
\hline 67 C 7555 & P88, L84 & Com \\
\hline 67 C 7556 & P88, L84 & Com \\
\hline
\end{tabular}

The entire 32-bit double-length product is available at the outputs at one time.

The most-significant product bit, S 31 , is available in both true and complemented form to simplify longer-wordlength multiplications. The product outputs are three-state, controlled by assertive-low enables. The MSP outputs are controlled by the TRIM ( \(\overline{\mathrm{OEM}}\) ) control input, while the LSP outputs are controlled by the TRIL ( \(\overline{O E L}\) ) control input. This allows one or more multipliers to be connected to a parallel bus or to be used in a pipelined system.
All inputs and outputs have transparent latches in the 'C7556. The latches become transparent when the input to the corresponding gate control line GX, GY, GM, GL is HIGH. If latches are not required, these control inputs may be tied HIGH, leaving the multiplier fully transparent for combinatorial cascading. The device uses a single +5 V power supply, and is available both in an 84 -terminal leadless chip carrier (LCC) package and in an 88-pin-grid-array package.

\section*{Block Diagram} 'C7555 (Register) 'C7556 (Latch)
\begin{tabular}{|c|l|}
\hline \multicolumn{2}{|c|}{ SUMMARY OF SIGNALS/PINS } \\
\hline \(\mathrm{X}_{15-0}\) & Multiplicand 16-bit data inputs \\
\hline \(\mathrm{Y}_{15-0}\) & Multiplier 16-bit data inputs \\
\hline XM, YM & \begin{tabular}{l} 
Mode-control inputs for each data word; \\
LOW for unsigned data and HIGH for twos- \\
complement data
\end{tabular} \\
\hline \(\mathrm{S}_{31-0}\) & Product 32-bit output \\
\hline \(\bar{S}_{31}\) & Inverted MS product bit (for expansion) \\
\hline RS, RU & \begin{tabular}{l} 
Rounding inputs for signed and unsigned \\
data, respectively
\end{tabular} \\
\hline GX/CX & Gate contro/clock for \(\mathrm{X}_{\mathrm{i}}\), RS, RU \\
\hline GY/CY & Gate control/clock for \(\mathrm{Y}_{\mathrm{i}}\)
\end{tabular}

Rounding Inputs
\begin{tabular}{|c|c|c|c|c|c|}
\hline \multicolumn{2}{|c|}{ INPUTS } & \multicolumn{2}{c|}{ ADDS } & \multicolumn{2}{c|}{ USUALLY USED WITH } \\
\hline RU & RS & \(\mathbf{2 1 5}\) & \(\mathbf{2 1 4}\) & XM & YM \\
\hline \hline L & L & No & No & X & X \\
\hline L & H & No & Yes & H \(\dagger\) & H \(\dagger\) \\
\hline H & L & Yes & No & L & L \\
\hline H & H & Yes & Yes & \(\star\) & \(*\) \\
\hline
\end{tabular}
\(\dagger\) In mixed mode, one of these could be low but not both.
* Usually a nonsense operaion.

\section*{Mode-Control Inputs}
\begin{tabular}{|c|c|c|c|c|}
\hline \multirow{3}{*}{\begin{tabular}{c} 
OPERATING \\
MODE
\end{tabular}} & \multicolumn{2}{|c|}{ INPUT DATA } & \multicolumn{2}{c|}{\begin{tabular}{c} 
MODE- \\
CONTROL \\
INPUTS
\end{tabular}} \\
\cline { 2 - 5 } & X15-0 & Y15-0 & XM & YM \\
\hline \hline Unsigned & Unsigned & Unsigned & L & L \\
\hline \multirow{3}{*}{ Mixed } & Unsigned & Twos-Comp. & L & H \\
\cline { 2 - 5 } & Twos-Comp. & Unsigned & H & L \\
\hline Signed & Twos-Comp. & Twos-Comp. & H & H \\
\hline
\end{tabular}

\section*{84-Terminal Leadless Chip Carrier Pinout}


All \(V_{C C}\) and GND pins must be connected to the respective \(V_{C C}\) and GND connections on the board and should not be used for daisychaining through the IC.

\section*{88 Pin-Grid-Array Pin Location \\ Bottom View}
(11) (11) (16) (1) (18) (21) (3) (25) (27) (27) (3) (31) (3)
(9) (12) (13) (13) (1) (27) (27) (21) (27) (29) (32) (3) (3)
(B) (1)
(3) (3)
\begin{tabular}{|c|c|c|c|}
\hline \multirow[t]{9}{*}{} & \multirow[t]{3}{*}{\begin{tabular}{l}
(6) (7) \\
(1) (5)
\end{tabular}} & & (31) (3) \\
\hline & & \begin{tabular}{|l|l|}
\hline \(11^{12}\) & \({ }^{39}{ }^{34}\) \\
\hline
\end{tabular} & (1) (1) \\
\hline & & & (12) (3) \\
\hline & (1) (8) & \(\begin{array}{ll}1 \\ 1 & 67 C 7555 \\ 88 & 67 C 756\end{array}\) & (14) (15) \\
\hline & (3) (3) & \(88 \quad 67 C 7556\) & (75) (1) \\
\hline & (35) (3) & & (14) (8) \\
\hline & (3) (11) & & (11) (3) \\
\hline & (3) (3) \({ }^{\text {(3) (2) }}\) & & (3) (3) \\
\hline & (8) (17) (3) & (6) (6) (4) (1) & (3) (3) \\
\hline & (717) (3) (1) & (6) (6) (6) 6 & (35) 3 \\
\hline
\end{tabular}

Pin-Guide for Pin Grid Array
\begin{tabular}{|c|c|c|c|c|c|c|c|}
\hline PIN NUMBER & PIN NAME & PIN NUMBER & PIN NAME & PIN NUMBER & PIN NAME & PIN NUMBER & PIN NAME \\
\hline 1 & X9 & 23 & N/C* & 45 & S25 & 67 & \(\mathrm{V}_{\mathrm{CC} 2}{ }^{\dagger}\) \\
\hline 2 & X10 & 24 & Y8 & 46 & S24 & 68 & N/C* \\
\hline 3 & X11 & 25 & Y9 & 47 & S23 & 69 & S7 \\
\hline 4 & X12 & 26 & Y10 & 48 & S22 & 70 & S6 \\
\hline 5 & X13 & 27 & Y11 & 49 & S21 & 71 & S5 \\
\hline 6 & X14 & 28 & Y12 & 50 & S20 & 72 & S4 \\
\hline 7 & X15 & 29 & Y13 & 51 & S19 & 73 & S3 \\
\hline 8 & XM & 30 & Y14 & 52 & S18 & 74 & S2 \\
\hline 9 & GX/CX & 31 & Y15 & 53 & S17 & 75 & S1 \\
\hline 10 & RS & 32 & YM & 54 & S16 & 76 & SO \\
\hline 11 & RU & 33 & GY/CY & 55 & GND & 77 & GND \\
\hline 12 & GND & 34 & N/C* & 56 & TRIL ( \(\overline{\mathrm{OEL}}\) ) & 78 & N/C* \\
\hline 13 & Yo & 35 & GND & 57 & GL/CL & 79 & GND \\
\hline 14 & Y 1 & 36 & TRIM ( \(\overline{\mathrm{OEM}})\) & 58 & S15 & 80 & X0 \\
\hline 15 & Y2 & 37 & GM/CM & 59 & S14 & 81 & X1 \\
\hline 16 & Y3 & 38 & \(\overline{\text { S31 }}\) & 60 & S13 & 82 & X2 \\
\hline 17 & Y4 & 39 & S31 & 61 & S12 & 83 & X3 \\
\hline 18 & Y5 & 40 & S30 & 62 & S11 & 84 & X4 \\
\hline 19 & Y6 & 41 & S29 & 63 & S10 & 85 & X5 \\
\hline 20 & Y7 & 42 & S28 & 64 & 59 & 86 & X6 \\
\hline 21 & \(\mathrm{V}_{\mathrm{CC} 2 \dagger} \dagger\) & 43 & S27 & 65 & S8 & 87 & X7 \\
\hline 22 & VCC2 \(\dagger\) & 44 & S26 & 66 & \(\mathrm{V}_{\mathrm{CCl}}+\dagger\) & 88 & X8 \\
\hline
\end{tabular}
* Not connected. \(\dagger V_{C C 2}=\) Logic \(V_{C C} . ~ \dagger \dagger V_{C C 1}=\) Output buffer \(V_{C C}\).

This document contains information on a product under development at Monolithic Memories Inc. The information is intended to help you to evaluate this product. Monolithic Memories reserves the right to change or discontinue work on this proposed product without notice.

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\section*{Package Drawing}

\section*{Side Brazed Package}


\section*{PACKAGE BODY}

Alumina
(Standard Dark)

BONDING WIRE
1.25 Mil Aluminum

LID
Gold Plated Kovar With
Nickel Underplating

CAVITY/SEAL RING
Gold Over Nickel Over Tungsten

LEAD MATERIAL
Alloy 42

\section*{LEAD FINISHES}

Gold Plate (Standard) Solder Dip Over Gold Plate

\section*{Package Drawings}

\section*{Package Drawings}

48D Side Brazed Ceramic DIP (1/2"x2 7/16")


\section*{UNLESS OTHERWISE SPECIFIED:}

ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}

\section*{Flat Pack}


\section*{PACKAGE BODY}

Alumina

BONDING WIRE
1.25 Mil Aluminum

\section*{LID}

Gold Plated Kovar With Nickel Underplating CAVITY/SEAL RING

Gold Over Nickel Over Tungsten

\section*{LEAD MATERIAL}

Alloy 42

\section*{LEAD FINISHES}

Gold Plate (Standard)
Solder Dip Over Gold Plate

\section*{Package Drawings}

\section*{Package Drawing}

20F Flat Pack
Mil-M-38510,
Appendix C, F-9


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}


\section*{LEAD FRAME}

Alloy 42

GLASS
Vitreous Solder Glass

BONDING WIRE
1.25 Mil Aluminum

\section*{CAVITY}

Gold Over Alumina For Eutectic Die Attach

\section*{CAP AND BASE}

Pressed Alumina

\section*{LEAD FINISHES}

Solder DIP Over Matte Tin Plate

\section*{Package Drawings}

14J Ceramic DIP (5/16"x3/4") Mil-M-38510,


\section*{16J Ceramic DIP (5/16"x3/4")} Mil-M-38510,
Appendix C, D-2
\(\rightarrow \|<\frac{.018 \pm .004}{.457 \pm .102}\)


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS ALL TOLERANCES ARE \(\pm .007\) INCHES


Notes:
1. Specified body dimensions allow for differences between SSI, MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

\section*{Package Drawings}

18J Ceramic DIP (5/16"x3/4") Mil-M-38510, Appendix C, D-6


\section*{20J Ceramic DIP} (5/16"x1") Mil-M-38510,
Appendix C, D-8


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES


Notes:
1. Specified body dimensions allow for differences between SSI, MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

\section*{Package Drawings}

24JS Ceramic SKINNYDIP \(\left(5 / 16^{\prime \prime} \times 1-1 / 4^{\prime \prime}\right)\)
Mil-M-38510,
Appendix C, D-9


24J Ceramic DIP
Mil-M-38510,
Appendix C, D-3


UNLESS OTHERWISE SPECIFIED: ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAXX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES


Notes:
1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds

2-10 mils thickness to all lead tip dimensions.

\section*{Package Drawing}

\section*{28J Ceramic DIP}
(1/2"x1 1/2")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawing}

\section*{40J Ceramic DIP}
(9/16"x2-1/16")
Mil-M-38510,
Appendix C, D-5


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

Notes:
1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

\section*{Leadless Chip Carrier}


\section*{Package Drawings}

\section*{Package Drawings}

1. Solder fillets on lid edges not shown.

\section*{Package Drawing}

44L Leadless Chip Carrier Mil-M-38510,
Appendix C, C-5


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawing}

52L Leadless Chip Carrier (.750"x.750")


TOP VIEW
BOTTOM VIEW


UNLESS OTHERWISE SPECIFIED: ALL DIMENSIONS MIN.-MAX. IN INCHES ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS ALL TOLERANCES ARE \(\pm .007\) INCHES
Notes:
1. Solder fillets on lid edges not shown.

\section*{Package Drawings}

68L Leadless Chip Carrier (.950"x.950")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES
Notes:
1. Solder fillets on lid edges not shown.

\section*{Package Drawing}

84L-2 Leadless Chip Carrier (Cavity Down)
(1.380" \(\times 1.380^{\prime \prime}\) )


\section*{UNLESS OTHERWISE SPECIFIED:}

ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAXX IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES
Notes:
1. Solder fillets on lid edges not shown.

\section*{Package Drawings}

84L-2 Socket


\section*{Socket Specifications (all values from Yamaichi/Nepenthe data sheet):}
\begin{tabular}{|c|c|}
\hline 1. Insulation Resistance & C \\
\hline 2. Dielectric Withstanding Voltage & 700 V AC RMS for one (1) minute \\
\hline 3. Contact Resistance & \(20 \mathrm{M} \Omega\) maximum at \(10 \mathrm{~mA}, 20 \mathrm{mV}\) \\
\hline 4. Rated Current Per Contact & 1 A maximum \\
\hline 5. Operating Temperature & -55 to \(+100^{\circ} \mathrm{C}\) \\
\hline 6. Contact Force & 85 grams min for each contact \\
\hline
\end{tabular}

\section*{Cerpack}


\section*{Package Drawings}

\section*{Package Drawings}

16W Cerpack Mil-M-38510,


18W Cerpack


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}


24W Cerpack Mil-M-38510, Appendix C, F-6


\section*{Package Drawing}

\section*{Pin Grid Array}


PACKAGE BODY
Alumina (Standard Dark) BONDING WIRE
1.25 Mil Aluminum

LID
Gold Plated Kovar With Nickel Underplating
CAVITY/SEAL RING
Gold Over Tungsten

PIN MATERIAL
Gold Plated Kovar

\section*{Package Drawings}

\section*{68P Ceramic Pin Grid Array (Cavity Up)}
(1.100x1.100)


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}

\section*{88P-1 Pin Grid Array (Cavity Up)}
(1.300"x1.300")


TOP VIEW


> UNLESS OTHERWISE SPECIFIED:
> ALL DIMENSIONS MIN.-MAX. IN INCHES
> ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
> ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}

88P-2 Pin Grid Array (Cavity Down)
\[
\left(1.300 " \times 1.300^{\prime \prime}\right)
\]


TOP VIEW


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Molded DIP}


\section*{LEAD FRAME}

Copper Alloy 194.
Copper Alloy Tamac 5.

\section*{LEAD FINISH}

Solder Dip.

BONDING WIRE
1.0 Mil Gold Wire. 1.25 Mil Gold Wire. 1.30 Mil Gold Wire.

\section*{DIE PAD}

Spot Silver Plating
(150 Micro-Inches)

PACKAGE BODY
Thermoset Plastic.

\section*{DIE BOND}

Silver Filled Epoxy.

\section*{Package Drawings}

\section*{16N Molded DIP}
(1/4"x3/4")



18N Molded DIP
(1/4"x7/8")


NOTES:
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both Version 1 and Version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on Version 1 are optional.


24NS Molded SKINNYDIP
(1/4"x1 3/16")

1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

\section*{Package Drawings}

\section*{Package Drawings}

24N Molded DIP


VERSION 2


28N Molded DIP




NOTES:
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

UNLESS OTHERWISE SPECIFIED:
2. Both Version 1 and Version 2 configurations are manufactured interchangeably.

ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL. DIMENSIONS MIN.-MAX. IN MILLIMETERS ALL TOLERANCES ARE +.007 INCHES

\section*{Package Drawings}

\section*{Package Drawings}

40N Molded DIP
(9/16" \(\left.\times 2-1 / 16^{\prime \prime}\right)\)


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAXX IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES


\section*{Package Drawings}

48N Molded DIP
(9/16"x2 13/32")



VERSION 2


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Notes:}
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

\section*{Molded Chip Carrier}


\section*{LEAD FRAME}

Copper Alloy 195.
Copper Alloy Tamac 5.

\section*{LEAD FINISH}

Tin Plating.
Solder Dip.

BONDING WIRE
1.25 Mil Gold Wire

\section*{DIE PAD}

Spot Silver Plating (150 Microinches).

PACKAGE BODY
Thermoset Plastic.

\section*{DIE BOND}

Silver Filled Epoxy.

\section*{Package Drawing}

\section*{20NL Molded Chip Carrier} (.351"x.351")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}

\section*{28NL Molded Chip}
(.451"x.451")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawing}

44NL Molded Chip Carrier (.650"x.650")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. TN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{Package Drawing}

68NL Molded Chip Carrier
(.950"x.950")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Package Drawings}

\section*{84 NL Molded Chip Carrier}
(1.154"x1.154")


\section*{Package Drawings}

\section*{Package Drawing}

\section*{Top Brazed}


PACKAGE BODY
Alumina

BONDING WIRE
1.25 Mil Aluminum

LID
Gold Plated Kovar With Nickel Underplating
CAVITY/SEAL RING
Gold Over Tungsten

\section*{LEAD MATERIAL}

Alloy 42

LEAD FINISHES
Gold Plate (Standard) Solder Dip Over Gold Plate

\section*{Package Drawing}

\section*{24T Top Brazed Ceramic Dip}
(With Heat Sink)
(1/2"x1 1/4")


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE \(\pm .007\) INCHES

\section*{Power Dissipation Determination}

\section*{Introduction}

Thermal resistance for a packaged integrated circuit determines the operating temperature, and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal impedance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data aquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal impedance in the form of \(\theta_{\mathrm{JC}}, \theta_{\mathrm{CA}}\), and a provision for obtaining \(\theta_{\mathrm{JA}}\) (resistance from junction to ambient) as a function of air movement over the package or package/board combination.

\section*{Use of Monolithic Memories data}

In this publication data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of \(\theta_{\mathrm{CA}}\) vs. airflow are provided for packages in common use. These include socket-mounted dual-in-line packages such as p-dip, cerdip, and side-brazed packages, board mounted cerpacks and flatpacks, and free-standing leadless-chip carriers. Since \(\theta_{C A}\) is a package geometry related function, the user need only look up the package type for the air-flow used. With this number, and knowledge of the die attach type, the total thermal resistance may be determined from the semiconductor junction
to the ambient. Since the \(\theta_{\mathrm{JC}}\) is largely dependent on the package type and die attach type, a table has been constructed for easy use. (Although \(\theta_{\mathrm{JC}}\) is a die-size dependent variable for eutectic die attach, the effect of \(\theta_{\mathrm{JC}}\) on \(\theta_{\mathrm{JA}}\) is small enough that a constant may be used in most cases. For other die-attach methods, the thermal resistance was only slightly dependent on die size). After obtaining \(\theta_{J C}\) and \(\theta_{C A}\) as described above, the total thermal resistance, \(\theta_{\mathrm{JA}}\), may be found by the addition of \(\theta_{J C}\) to \(\theta_{\mathrm{CA}}\) as:
\[
\theta_{\mathrm{JA}}=\theta_{\mathrm{JC}}+\theta_{\mathrm{CA}}
\]

\section*{Notes on the tabulated data}
1. All side-brazed, cerdip-sealed, and molded dual-in-line packages were mounted in zero insertion force sockets and placed transverse to the airstream. Thermocouples were mounted directly to the bottom of the package.
2. All cerpacks and flatpacks were board mounted in direct contact with a double-sided fiberglass-epoxy composite printed circuit board. The thermocouple was placed directly between the package and the board and fastened to the package.
3. All \(\mathrm{L}_{\mathrm{CC}}\) packages except the 84 PIN \(\mathrm{L}_{\mathrm{CC}}\) were freestanding, suspended by 28 GA. tinned copper wire soldered to pads corresponding to \(\mathrm{V}_{\mathrm{CC}}\) and GND. The 84 PIN LCC was mounted in a single insertion socket. Thermocouples were attached directly to the bottom of the parts.

\title{
Thermal Impedance Measurement Procedure
}

\section*{Definition}

Thermal impedance of a device is defined as the rise in the junction temperature against some reference point per unit of power dissipation or it may be described by the formula:
\[
\begin{array}{ll}
\frac{\Delta \mathrm{Tj}\left({ }^{\circ} \mathrm{C}\right)}{\mathrm{Pd}(\text { Watts })} & \begin{array}{l}
\mathrm{Tj}=\text { temperature of junction } \\
\mathrm{Pd}=\text { power dissipation }
\end{array}
\end{array}
\]

\section*{Theory}

The principle of measuring the Thermal Impedance of a device is based on measuring the temperature of the hottest junction on the die under power dissipation. This is done by using the substrate diode to monitor the chip temperature. By reverse biasing• and forcing a small forward current ( \(500 \mu \mathrm{~A}\) ) through the device under test (between \(+\mathrm{V}_{\mathrm{CC}}\) and ground), a large number of substrate diodes become forward-biased. By doing this, the hottest substrate diode junction is automatically detected, since it has the lowest voltage drop during this forward-biased condition. The forward voltage drop across the substrate diode is quite linear over a range of \(25^{\circ} \mathrm{C}\) to \(100^{\circ} \mathrm{C}\). The hottest substrate diode is used as a "thermometer" to monitor the chip under power.

\section*{Procedure}

A block diagram of the Thermal Impedance setup is shown in Figure 1. The substrate diode is forward biased by the Constant Current Source \((-500 \mu \mathrm{~A})\). The \(\mathrm{V}_{\mathrm{CC}}\) is supplied by the Power Supply, which is gated at 48.8 cycles/second, with a duty cycle of \(\simeq 99.5 \%\). The \(V_{F}\) of the substrate diode is 'sampled' by the

Sample/Hold circuit, which is gated synchronously with the \(\mathrm{V}_{\mathrm{CC}}\) supply, sampling is done for \(40 \mu \mathrm{~S}\), during each \(100 \mu \mathrm{~S}\) window when the \(V_{C C}\) power supply is OFF. In addition to the \(V_{F}\) readings, the case temperature (closest to die attach point) and the Ambient temperature are monitored. The power dissipated (Pd) by the device is measured by DVM and calculated:
\[
P d=I_{C C} \times V_{C C} .
\]

The device is mounted in a socket within a Wind Tunnel. The air speed within the wind tunnel is monitored with an Air Velocity meter. The air speed is adjustable from 0 to 1000 feet \(/ \mathrm{min}\). The use of a wind tunnel allows us to graph the temperature of the die, in relation to the cooling air speed. The worst case \(\theta_{J A}\) is at 0 air speed (STATIC).

\section*{Summary}

The Thermal Impedance measurement can be summarized as follows:
1). Calibration of the \(\Delta \mathrm{V}_{\mathrm{F}} /{ }^{\circ} \mathrm{C}\) of the D.U.T. This is done by measuring the \(V_{F}\) at two different temperatures with the \(V_{C C}\) power supply OFF, and dividing the \(\Delta V_{F}\) by the \(\Delta^{\circ} \mathrm{C}\).
2). Measurement of \(\Delta \mathrm{V}_{\mathrm{F}}\) under operating conditions, under different air flow rates ( \(0,100,500,1000 \mathrm{ft} / \mathrm{min}\).), while measuring \({ }^{\circ} \mathrm{C}\) case, \({ }^{\circ} \mathrm{C}\) ambient, \(\mathrm{I}_{\mathrm{CC}}\) and \(\mathrm{V}_{\mathrm{CC}}\). The readings are recorded when the change in the case ( \({ }^{\circ} \mathrm{C}\) case) temperature is less than \(2 \%\) (of \(\Delta{ }^{\circ} \mathrm{C}\) case \(-{ }^{\circ} \mathrm{C} \mathrm{amb}\) ) over a time of 30 seconds.
3). Calculation of Thermal Impedance

Symbol of Definitions
\(V_{F 1}=V_{F}\) @ low temp. cal. point ( \(V_{C C}\) OFF)
\(V_{F 2}=V_{F} @\) high temp. cal. point ( \(V_{C C}\) OFF)
\({ }^{\circ} \mathrm{C}_{1}=\) Case \({ }^{\circ} \mathrm{C}\) @ low temp. cal. point (V \(\mathrm{V}_{\mathrm{CC}}\) OFF)
\({ }^{\circ} \mathrm{C}_{2}=\) Case \({ }^{\circ} \mathrm{C}\) @ high temp. cal. point ( \(\mathrm{V}_{\mathrm{CC}} \mathrm{OFF}\) )
\(V_{F 3}=V_{F}\) under power, stablized
\({ }^{\circ} \mathrm{C}_{3}=\) Case \({ }^{\circ} \mathrm{C}\) under power, stabilized
\({ }^{\circ} \mathrm{C}_{\mathrm{A}}=\) Ambient \({ }^{\circ} \mathrm{C}\)
\[
P d=I_{C C} \times V_{C C}
\]
a) \(\theta_{J C}\) (Junction to case)
\[
\theta_{\mathrm{JC}}=\frac{\left[\begin{array}{l}
\left(\frac{\left.V_{F 1}-V_{F 3}\right)}{\left(\frac{V_{F 1}-V_{F 2}}{{ }^{\circ} \mathrm{C}_{2}-{ }^{\circ} \mathrm{C}_{1}}\right)}+\left({ }^{\circ} \mathrm{C}_{1}-{ }^{\circ} \mathrm{C}_{3}\right)\right] \\
\mathrm{Pd}
\end{array}{ }^{\circ} \mathrm{C}_{\mathrm{W}}\right.}{}
\]
b) \(\theta_{\mathrm{CA}}=\frac{\left({ }^{\circ} \mathrm{C}_{3}-{ }^{\circ} \mathrm{C}_{\mathrm{A}}\right)}{\mathrm{Pd}}\)
c) \(\theta_{J A}\) (Junction to ambient)
\[
\theta_{\mathrm{JA}}=\theta_{\mathrm{CA}}+\theta_{\mathrm{JC}}=\quad{ }^{\circ} \mathrm{C}_{\mathrm{W}}
\]

\section*{Block Diagram}

1). Digital Thermometer measures \({ }^{\circ} \mathrm{C}\) case and \({ }^{\circ} \mathrm{C}\) ambient
2). \(D V M:^{1}\) measures \(V_{C C}\) and \(I_{C C}\)
3). \(D V M^{2}\) measures \(V_{F}\) of the substrate diode
4). BINARY counter creates \(A_{0}\) thru \(A_{11}\);
\(A_{\theta}=100 \mathrm{kHz}, A_{1}=50 \mathrm{kHz}\),
\(A_{2}=25 \mathrm{kHz}\) etc. synchronious.
5). Timing gate switches the power supply, address buffers, and sample/hold circuits.
6). Constant current source provides \(-500 \mu \mathrm{~A}\) to the \(\mathrm{V}_{\mathrm{CC}}\) pin for the \(V_{F}\) measurement.
7). The airflow meter measures the air velocity for airflow measurements.


\title{
Thermal Characterization of Packages
}

\section*{Introduction}

Thermal resistance for a packaged integrated circuit determines the operating temperature and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal resistance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data acquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal resistance in the form of \(R_{\theta J C}\) (resistance from junction to case) and \(\mathrm{R}_{\theta \mathrm{JA}}\) (resistance from junction to ambient) as a function of air movement over the package/board combination.

\section*{Use of Monolithic Memories Data}

In this publication, data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of \(\mathrm{R}_{\boldsymbol{\theta} \mathrm{JA}}\) vs. airflow are provided for packages in
common use. These include socket-mounted pin grid arrays, dual-in-line p-dip, cerdip and side-brazed packages, board mounted cerpacks, flatpacks, leadless-chip carriers and plastic leaded chip carriers.
Resistance from junction to ambient \(\left(R_{\theta J A}\right)\) is a package geometry and die size related function. The user need only look up the package type and die size for the air-flow used. Since the \(\mathrm{R}_{\theta \mathrm{JC}}\) is largely dependent on the package type and die size, a table has been constructed for easy use.

\section*{Notes on the Tabulated Data}
1. All side-brazed, cerdip-sealed, molded dual-in-line and pin grid array packages were mounted in zero insertion force sockets and transverse to the airstream.
2. All cerpacks, flatpacks, LCC and PLCC packages were board mounted in direct contact with a double-sided fiberglassepoxy composite printed circuit board.
3. For measurement of \(\mathrm{R}_{\theta \mathrm{JC}}\), all packages were immersed in a constant temperature fluorinert bath. The thermocouple was mounted directly to the bottom of the package.

\section*{Thermal Resistance Measurement Procedure}

\section*{Definition}

Thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure (package) to provide for heat removal from the semiconductor element. It is defined as the rise in the junction temperature against some reference point per unit power of dissipation or it may be described by the formula:
\[
\begin{aligned}
\mathrm{R}_{\theta \mathrm{JR}}= & \text { Thermal resistance, junc- } \\
& \text { tion to reference point, in } \\
& { }^{\circ} \mathrm{C} / \text { watt }
\end{aligned}
\]

\section*{Thermal Measurement Technique}

Thermal resistance is measured using the temperature sensitive parameter (TSP) method. This method takes advantage of the linear relation between temperature and voltage drop across a \(p-n\) junction to measure the average die temperature. Thermal resistance measurement can be done either using an actual device or with thermal test chips. For the purpose of this study, thermal test chips are used.
Each test chip consists of sensing elements and a heating element. Sensing elements are two sets of diode pairs. One diode pair is located at the center of each die and one pair is near a corner. The heating element is a polysilicon resistor which covers 95 percent of the die surface area. The resistor extends underneath the bond pads but not the sensing elements.
Initially, diodes are forward biased to a low level current source ( \(50 \mu \mathrm{~A}\) ) and the voltage drop is calibrated with respect to temperature. Then, the resistor is powered and the diode voltage drop is monitored until thermal equilibrium is reached. Steady
state junction temperature is calculated from the calibration data.

For the \(R_{\theta J A}\) measurement the device is put in a wind tunnel. The air speed is adjustable from 0 to 1000 feet \(/ \mathrm{min}\). The use of a wind tunnel allows us to graph the \(R_{\theta J A}\) vs. air flow velocity. Average junction to case thermal resistance ( \(R_{\theta J C}\) ) is measured by immersing the package in a constant temperature fluorinert bath and sensing steady state junction temperature with case temperature being measured at the bottom of the package.

\section*{Summary}

The thermal resistance measurement can be summarized as follows:
1. Calibration of the voltage drop across the sensing element with respect to temperature. This is done by measuring the voltage drop at several different temperatures with the heating power off.
2. Measurement of voltage drop across the sensing element under operating conditions, under various air flow rates (from 0 to 1000 linear \(\mathrm{ft} / \mathrm{min}\).), while measuring \({ }^{\circ} \mathrm{C}\) ambient and power input for calculation of \(\mathrm{R}_{\theta \mathrm{JA}}\)
3. Measurement of voltage drop across the sensing element under operating conditions, package immersed in constant temperature fluorinert bath, while measuring the case temperature at the bottom of the package and power input for calculation of \(R_{\theta J C}\). The readings are recorded when the package has reached thermal equilibrium.
4. Calculation of thermal resistance

\section*{Package Drawings}

\section*{Cerdip (J) Packages}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE \((\mathrm{mils})^{\mathbf{2}}\) & R \(_{\theta \mathrm{JJC}}^{*}\left({ }^{\circ} \mathbf{C} /\right.\) WATT \()\) \\
\hline 18 J & 22,500 & 6 \\
\hline 20 J & 5,625 & 14 \\
\hline \(24 \mathrm{~J}-\mathrm{S}(1)\) & 5,625 & 16 \\
\hline \(24 \mathrm{~J}-\mathrm{S}(2)\) & 11,250 & 9 \\
\hline 24 J & 50,625 & 3 \\
\hline \(40 \mathrm{~J}(3)\) & 22,500 & 4 \\
\hline \(40 \mathrm{~J}(2)\) & 50,625 & 2 \\
\hline
\end{tabular}
* These are typical values for the given die size.

Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

\section*{Package Drawings}

\section*{Leadless Chip Carriers (L) Packages}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE (mils) \({ }^{\mathbf{2}}\) & \(\mathbf{R}_{\boldsymbol{\theta} \mathbf{J C}}\left({ }^{\circ} \mathbf{C} /\right.\) WATT \()\) \\
\hline \hline 20 L & 5,625 & 16 \\
\hline \(28 \mathrm{~L}(1)\) & 5,625 & 20 \\
\hline \(28 \mathrm{~L}(2)\) & 22,500 & 9 \\
\hline 44 L & 22,500 & 4 \\
\hline \(84 \mathrm{~L} \dagger\) & 50,625 & 4 \\
\hline
\end{tabular}
* These are typical values for the given die size. Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.
\(\dagger\) Cavity up.

\section*{Molded Dip (N) Packages}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE (mils) \({ }^{\mathbf{2}}\) & R \(_{\boldsymbol{\theta} \mathrm{JC}}\left({ }^{\circ}{ }^{\circ} \mathrm{C} /\right.\) WATT \()\) \\
\hline 16 N & 5,625 & 29 \\
\hline 18 N & 5,625 & 30 \\
\hline 20 N & 5,625 & 23 \\
\hline 24 N & 50,625 & 10 \\
\hline \(24 \mathrm{~N}-\mathrm{S}\) & 5,625 & 22 \\
\hline \(40 \mathrm{~N}-1\) & 22,500 & 16 \\
\hline \(40 \mathrm{~N}-3\) & 5,625 & 23 \\
\hline
\end{tabular}

\footnotetext{
* These are typical values for the given die size. Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.
}

\section*{Plastic Leaded Chip Carrier (NL) Packages}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE (mils) \({ }^{\mathbf{2}}\) & \(\mathbf{R}_{\boldsymbol{\theta} \mathrm{JC}}^{*}\left({ }^{\circ} \mathbf{C} /\right.\) WATT \()\) \\
\hline \hline 20 NL & 5,625 & 35 \\
\hline 28 NL & 22,500 & 16 \\
\hline 44 NL & 22,500 & 13 \\
\hline 68 NL & 50,625 & 8 \\
\hline
\end{tabular}
* These are typical values for the given die size. Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

\section*{Pin Grid Array (P) Packages}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE (mils) \({ }^{2}\) & R \(_{\text {өJC }}^{\star}\) ( \({ }^{\circ}\) C/WATT) \\
\hline \hline \(88 \mathrm{P} \dagger\) & 50,625 & 4 \\
\hline 68 P & 22,500 & 5 \\
\hline
\end{tabular}
* These are typical values for the given die size. Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.
\(\dagger\) Cavity up.

\section*{Package Drawings}

\section*{Top Brazed (T) Ceramic Package}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE (mils) \({ }^{2}\) & R \(_{\boldsymbol{\theta}}^{\star}{ }_{\text {JC }}\left({ }^{\circ}\right.\) C/WATT) \\
\hline \hline 64 T & 50,625 & 3 \\
\hline
\end{tabular}
* These are typical values for the given die size.

Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

\section*{Package Drawings}

\section*{Cerpack (W) Packages}

\begin{tabular}{|c|c|c|}
\hline PACKAGE & DIE SIZE (mils) \({ }^{\mathbf{2}}\) & R \(_{\boldsymbol{\theta}}^{\star}{ }_{\mathrm{JC}}{ }^{( }{ }^{\circ} \mathbf{C} /\) WATT \()\) \\
\hline \hline 16 W & 5,625 & 21 \\
\hline 18 W & 5,625 & 17 \\
\hline 20 W & 5,625 & 15 \\
\hline 24 W & 22,500 & 4 \\
\hline
\end{tabular}
* These are typical values for the given die size.

Other die size values to be supplied in the future.
Most Monolithic Memories products will be slightly lower.

\begin{tabular}{|c|c|}
\hline Introduction & 1 \\
\hline \multicolumn{2}{|l|}{Military Products Division 2} \\
\hline PROM & 3 \\
\hline \multicolumn{2}{|l|}{PLE \({ }^{\text {TM }}\) Devices} \\
\hline \multicolumn{2}{|l|}{PAL® Devices} \\
\hline \multicolumn{2}{|l|}{HAL \({ }^{\circledR} /\) ZHAL \(^{\text {TM }}\) Devices 6} \\
\hline \multicolumn{2}{|l|}{System Building Blocks/HMSI \({ }^{\text {M }}\)} \\
\hline \multicolumn{2}{|l|}{FIFO 3} \\
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\hline
\end{tabular}
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Arrow Electronics

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(305) 982-0661
(305) 841-1878
(305) 725-1480
(813) 576-1966
(404) 923-5750
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\end{tabular}

Kansas


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\footnotetext{






 processing for such applications
}```


[^0]:    **Converting from "A" to "B" PAL in third quarter 1986.

    1. Inactive for new designes using R Case Outline only. Use applicable QPL 38510 device.
[^1]:    *tCLK for Registered and Diagnostic PROM
    **Preliminary Information

[^2]:    * Three-state only.
    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^3]:    * Three-state only.
    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \vee V_{C C}$ and $25^{\circ} \mathrm{C} T_{A}$

[^4]:    * Three-state only.
    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V} V_{C C}$ and $25^{\circ} \mathrm{C} T_{A}$.

[^5]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    $\dagger$ Typicals at $5.0 \mathrm{~V} \vee_{\mathrm{CC}}$, and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.
    $\dagger \dagger \mathrm{V}_{I L}$ and $\mathrm{V}_{I H}$ limits are absolute values with respect to the device ground pin(s) and include all overshoots due to test equipment noise.

[^6]:    Three-state only.
    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^7]:    * Three-state only. $\quad * *$ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$

[^8]:    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typical at $5.0 \vee \mathrm{~V}_{\mathrm{CC}}$, and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^9]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    + Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^10]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typical at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$, and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^11]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \vee V_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^12]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \vee \vee_{C C}$ and $25^{\circ} \mathrm{C} T_{A}$

[^13]:    1

[^14]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^15]:    $\star$ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second
    $\dagger$ Typicals at 5.0 V VCC and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^16]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^17]:    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^18]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^19]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{VV}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C}_{\mathrm{A}}$.

[^20]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $5.0 \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$

[^21]:    $\dagger$ Contact manufacturer for availability and programming information.

[^22]:    * The PLE11P4M is available in a 20 - or 28-pin Leadless Chip Carrier

[^23]:    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$

[^24]:    $\dagger$ Typicals at $5.0 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

[^25]:    $\tau^{-1}$ selects $1: 16$ programmable initialization words.

[^26]:    $\dagger$ Contact manufacturer for availability and programming information

[^27]:    * Patent pending

[^28]:    PAL* (Programmable Array Logic). PALASM ${ }^{*}$, HAL* and SKINNYDIP ${ }^{*}$ are registered trademarks of Monolithic Memories.
    $\mathrm{HMSI}^{\text {tw }}$ is a trademark of Monolithic Memories.

[^29]:    * Minimum commercial $\mathrm{t}_{\text {su }}$ for devices with all registered outputs.
    ** Polarity fuse programmed (active High).

[^30]:    PAL, HAL, and PALASM are registered trademarks of Monolithic Memories, Inc.
    ProPAL, ZHAL, MegaPAL, MegaHAL and TGEN are trademarks of Monolithic
    Memories, Inc.
    ABEL is a trademark of Data I/O Corp.
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[^31]:    * The "Test Point" is driven by the outputs under test and observed by instrumentation

[^32]:    * $\mathrm{V}_{\mathrm{IL}}$ and $\mathrm{V}_{\mathrm{IH}}$ are input conditions of output tests and are not, themselves, directly tested. As conditions of tests, $\mathrm{V}_{\mathrm{IL}} \leq 0.8 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{IH}} \geq 2.0 \mathrm{~V}$.
    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
    $\dagger$ Typicals at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.

[^33]:    * Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

[^34]:    "'FIRST-IN, FIRST-OUT' .. DESCRIBES A QUEUE DISCIPLINE WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE ..."

[^35]:    $\downarrow$ Arrow indicates that it is referenced to the high-to-low transition.
    ** 16 th word only
    *** Devices connected to provide FIFO of greater than 16 word depth.

[^36]:    Waveform 1 is for an output with internal conditions such that the output is low except when disabled.
    Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

[^37]:    $\dagger$ See AC test and High Speed application note.

[^38]:    $\star$ Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second
    ** These are absolute voltages with respect to GND (Pin 8 or 9 ) and include all overshoots due to test equipment

[^39]:    Note Typicals at $5 \mathrm{~V} \mathrm{~V}_{\mathrm{CC}}$ and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

    * If the FIFO is not full (IR High), $\overline{M R}$ low forces IR low, followed by IR returning high when $\overline{M R}$ goes high.
    $\dagger$ See AC test and high-speed application note.
    $\dagger \dagger$ Tested
    $\dagger \dagger \dagger$ Guaranteed by design (see test load).

[^40]:    * Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
    $\dagger$ This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

[^41]:    Almost Full (AF) is eight words or less to FIFO full. Almost Empty (AE) is eight words or less to FIFO empty

[^42]:    ${ }^{\star}$ N Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
    ** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise.

[^43]:    (1) Input Ready HIGH indicates space is avialable and a Shift-In pulse may be applied.

[^44]:    $\dagger$ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

    * These are absolute voltages with respect to pin 10 on the device and includes all overshoots due to system and/or test noise. Do not attempt to test these values without suitable equipment.

[^45]:    AUTO: Auto-Access Input - When AUTO is LOW and $\overline{\text { RFSH }}$ is HIGH the Auto-Access mode is selected (see AutoAccess mode description).
    $\overline{\text { RFSH: }}$ Refresh Input - When $\overline{\text { RFSH }}$ is LOW the Refresh mode is selected (see Refresh mode description).

[^46]:    Note: In the REFRESH mode, $\overline{A U T O}$ must be LOW or R/ $\overline{\mathrm{C}}$ must be HIGH to guarantee the refresh address on the Q0-9 outputs.

[^47]:    * The "TEST POINT" is driven by the output under test, and observed by instrumentation.

[^48]:    ** These are absolute voltages with respect to pins 13 or 38 on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.

[^49]:    $1=$ HIGH voltage level
    $0=$ LOW voltage level
    X = Don't care

[^50]:    * Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

[^51]:    * During operations when the bus is being used to output data.

[^52]:    $\dagger$ Typicals at 5.0 V and $25^{\circ} \mathrm{C} \mathrm{T}_{\mathrm{A}}$.

    * Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
    $\star *$ These are absolute voltages with respect to the ground pins and inciude ail oversioots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

[^53]:    *Identical with product result passing through latch.

[^54]:    Table 4. Equivalences Between Simple and Compound Interface Types

[^55]:    *For other package types, please contact your local sales representative.

[^56]:    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

    * " $A$ " indicates data input, " $E$ " indicates enable input.

[^57]:    ** Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

    * " A " indicates data input, " E " indicates enable input.

[^58]:    * The "TEST POINT" is driven by the output under test, and observed by instrumentation.

[^59]:    * Clock must be steady or falling

[^60]:    *Note: This article is a portion of Monolithic Memories Conference Paper CP-112, which may be found in its entirety in the second edition of the Systems Design Handbook.

[^61]:    * NOTE: These controls for $\overline{\mathrm{OEAB}}, \overline{\mathrm{OEBA}}, \mathrm{GA} 1, \overline{\mathrm{GA} 2}, \mathrm{~GB} 1$ and $\overline{\mathrm{GB} 2}$ can cause race conditions.

[^62]:    * NOTE: These controls for $\overline{\mathrm{OEAB}}, \overline{\mathrm{OEBA}}, \mathrm{GA} 1, \overline{\mathrm{GA} 2}, \mathrm{~GB} 1$ and $\overline{\mathrm{GB} 2}$ can cause race conditions.

[^63]:    * For the 'LS648 devices, the A and B bus outputs are 3-state.

    For the 'LS649 devices, the A and B bus outputs are open-collector.

[^64]:    * Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

[^65]:    $\dagger$ See Figure 4.

[^66]:    $\dagger$ See Figure 4.

[^67]:    $\dagger$ See Figure 4.

[^68]:    * For A bus, the test load will refer to the open-collector test load. See Figure 6. For B bus, the test load will refer to the three-state test load. See Figure 7.
    $\dagger$ See Figure 4.

[^69]:    * Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

[^70]:    * In this case the output of the latch feeds the input, and a "race" condition results.
    ** $\mathrm{Q}_{0}$ represents the previous "latched" state.
    + This transition is not a normal mode of operation and may produce hazards.

[^71]:    * In this case the output of the register is clocked to the inputs and the overall $Q$ output is unchanged at $Q_{0}$.

[^72]:    * The "TEST POINT" is drived by the output under test,

[^73]:    * Note: These controls for $\overline{\mathrm{OEAB}}, \overline{\mathrm{OEBA}}, \mathrm{GA} 1, \overline{\mathrm{GA} 2}, \mathrm{~GB} 1$, and $\overline{\mathrm{GB2}}$ can cause race conditions.

[^74]:    $\dagger$ The arrow indicates the Low-to-High transition of the clock input used as reference

[^75]:    * See Figure 4.

[^76]:    * In this case the output of the latch feeds the input, and a "race" condition results.
    ** $\mathrm{Q}_{0}$ represents the previous "latched" state.
    $\dagger$ This transition is not a normal mode of operation and may produce hazards.

[^77]:    * In this case the output of the register is clocked to the inputs and the overall $Q$ output is unchanged at $Q_{0}$

[^78]:    The case when gate is HIGH and data flows through the part is specified as Data to Output delay in the Switching Characteristics table. $\left(V_{T}=1.3 \mathrm{~V}\right)$.

[^79]:    Portions of this Data Sheet reproduced with the courtesy of Motorola Inc

[^80]:    Note: Each ECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow grater than 500 linear fpm is maintained.
    Outputs are terminated through a $50 \Omega$ resistor to -2.0 V .

[^81]:    Portions of this data sheet reproduced with the courtesy of Motorola Inc.

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