MITSUBISHI SEMICONDUCTORS 1987

SINGLE-CHIP 8-BIT MICROCOMPUTERS Vol.2

DATA BOOK

MITSUBISHI ELECTRIC

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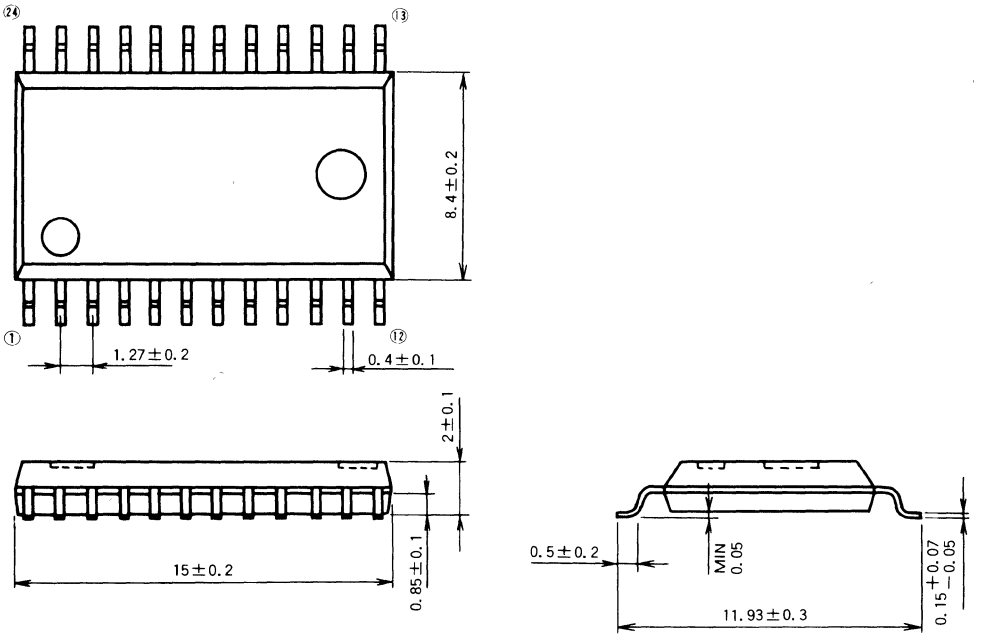
Development Support Systems

Type \ Development Support systems			Host machine	Debugging machine		Evaluation boards with EPROM
				Main unit	Option board	
8-bit CMOS	Series MELPS 8-48	M5M80C49A-XXXP M5M80C49H-XXXP	—	PC4000	PCA8400	PCA8403
		M5M80C39AP				—
		M5M80C39HP				—
		M5MC49A-XXXFP				—
		M5MC49H-XXXFP				—
		M5L8048-XXXP				PCA8403
8-bit NMOS		M5L8035LP				—
		M5L8049-XXXP M5L8049-XXXP-6				PCA8403
		M5L8039P-11				—
		M5L8039P-6				—
		M5M8050H-XXXP				PCA8403
		M5M8040HP				—
		M5L8049H1-XXXP				—
		M5L8039HLP-14				—
	Series MELPS 8-41	M5L8041A-XXXP		—	—	—
		M5L8041AH-XXXP		—	—	—
		M5L8042-XXXP		—	—	—

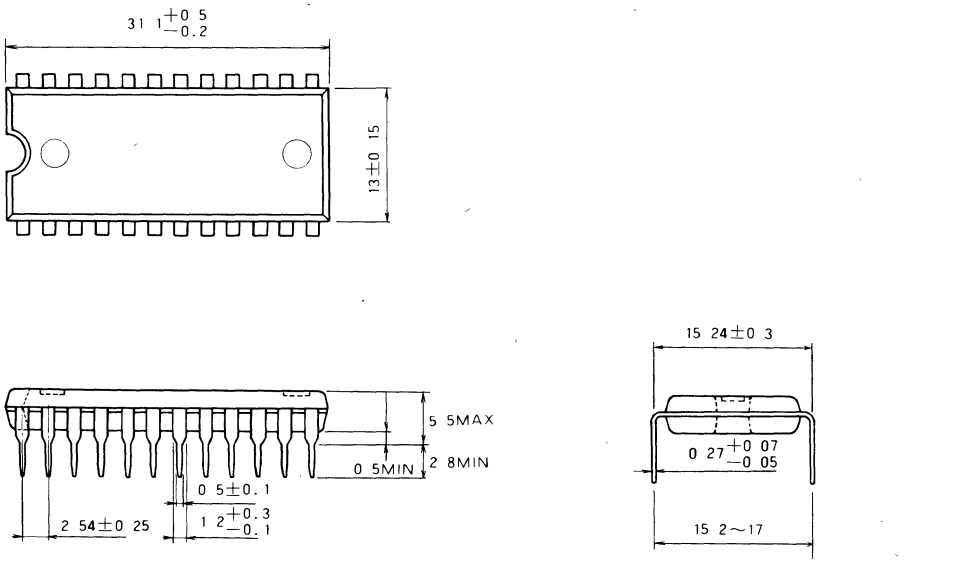
TYPE 24P2W 24-PIN MOLDED PLASTIC FLAT

Dimension in mm



TYPE 24P4 24-PIN MOLDED PLASTIC DIP

Dimension in mm



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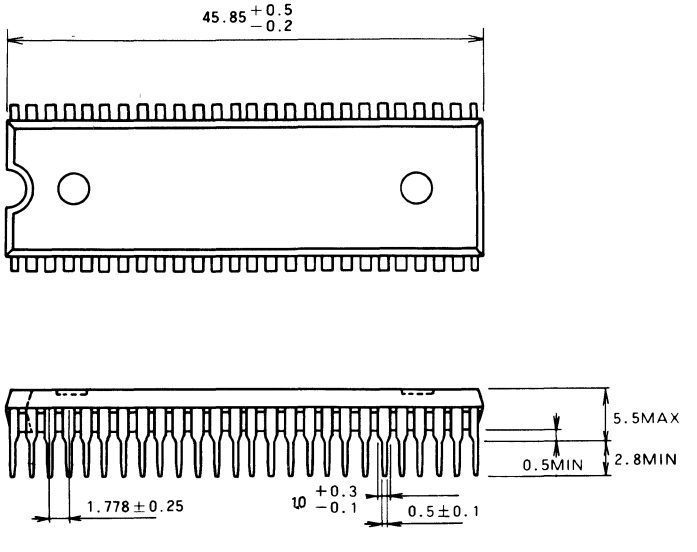
TYPE 52P4B 52-PIN MOLDED PLASTIC DIP (LEAD PITCH 1.778mm)

Dimension in mm



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b) those that are characteristics of the memory.
The letter symbols so far proposed for memory circuits are listed in sub-clauses 3.1 and 3.2 below.
All subscripts A should be in lower-case.

3.1. Timing Requirements

The letter symbols for the timing requirements of semiconductor memories are as follows :

Term	Subscript
Cycle time	c
Time interval between two signal events	d
Fall time	f
Hold time	h
Precharging time	pc
Rise time	r
Recovery time	rec
Refresh time interval	rf
Setup time	su
Transition time	t
Pulse duration (width)	w

3.2. Characteristics

The letter symbols for the dynamic characteristics of semiconductor memories are as follows :

Characteristic	Subscript
Access time	a
Disable time	dis
Enable time	en
Propagation time	P
Recovery time	rec
Transition time	T
Valid time	v

Note Recovery time for use as a characteristic is limited to sense recovery time

4. SUBSCRIPTS B AND D (For Signal Name or Terminal Name)

The letter symbols for the signal name or the name of the terminal are as given below.
All subscripts B and D should be in upper-case.

Signal or terminal	Subscript
Address	A
Clock	C
Column address	CA
Column address strobe	CAS
Data input	D
Data input/output	DQ
Chip enable	E
Erasure	ER
Output enable	G
Program	PR
Data output	Q
Read	R
Row address	RA
Row address strobe	RAS
Refresh	RF
Read/Write	RW
Chip select	S
Write (write enable)	W

Note 1 In the letter symbols for time intervals, bars over the subscripts, for example CAS, should not be used
2 It should be noted, when further letter symbols are chosen, that the subscript should not end with H, K, V, X, or Z (See clause 5)
3 If the same terminal, or signal, can be used for two functions (for example Data input/output, Read/Write) the waveform should be labelled with the dual function, if appropriate, but the symbols for the dynamic parameters should include only that part of the subscript relevant to the parameter

5. SUBSCRIPTS C AND E (For Transition of Signal)

The following symbols are used to represent the level or state of a signal :

Transition of signal	Subscript
High logic level	H
Low logic level	L
Valid steady-state level (either low or high)	V
Unknown, changing, or 'don't care' level	X
High-impedance state of three-state output	Z

The direction of transition is expressed by two letters, the direction being from the state represented by the first letter to that represented by the second letter, with the letters being as given above.
When no misunderstanding can occur, the first letter may be omitted to give an abbreviated symbol for subscripts C and E as indicated below.
All subscripts C and E should be in upper-case.

Examples	Subscript Full	Abbreviated
Transition from high level to low level	HL	L
Transition from low level to high level	LH	H
Transition from unknown or changing state to valid state	XV	V
Transition from valid state to unknown or changing state	VX	X
Transition from high-impedance state to valid state	ZV	V

Note Since subscripts C and E may be abbreviated, and since subscripts B and D may contain an indeterminate number of letters, it is necessary to put the restriction on the subscripts B and D that they should not end with H, L, V, X, or Z, so as to avoid possible confusion

FOR DIGITAL INTEGRATED CIRCUITS

New symbol	Former symbol	Parameter—definition
C_I		Input capacitance
C_O		Output capacitance
$C_{I/O}$		Input/output terminal capacitance
$C_{I(\phi)}$		Input capacitance of clock input
f		Frequency
$f_{(\phi)}$		Clock frequency
I		Current—the current into an integrated circuit terminal is defined as a positive value and the current out of a terminal is defined as a negative value
I_{BB}		Supply current from V_{BB}
$I_{BB(AV)}$		Average supply current from V_{BB}
I_{CC}		Supply current from Vcc
$I_{CC(AV)}$		Avarage supply current from Vcc
$I_{CC(PD)}$		Power-down supply current from Vcc
I_{DD}		Supply current from V_{DD}
$I_{DD(AV)}$		Average supply current from V_{DD}
I_{GG}		Supply current from V_{GG}
$I_{GG(AV)}$		Average supply current from V_{GG}
I_I		Input current
I_{IH}		High-level input current—the value of the input current when V_{OH} is applied to the input considered
I_{IL}		Low-level input current—the value of the input current when V_{OL} is applied to the input considered
I_{OH}		High-level output current—the value of the output current when V_{OH} is applied to the output considered
I_{OL}		Low-level output current—the value of the output current when V_{OL} is applied to the output considered
I_{OZ}		Off-state (high-impedance state) output current—the current into an output having a three-state capability with input condition so applied that it will establish according to the product specification, the off (high-impedance) state at the output
I_{OZH}		Off-state (high-impedance state) output current, with high-level voltage applied to the output
I_{OZL}		Off-state (high-impedance state) output current, with low-level voltage applied to the output
I_{OS}		Short-circuit output current
I_{SS}		Supply current from V_{SS}
Pd		Power dissipation
N_{EW}		Number of erase/write cycles
N_{RA}		Number of read access unrefreshed
R_I		Input resistance
R_L		External load resistance
R_{OFF}		Off-state output resistance
R_{ON}		On-state output resistance
t_a		Access time—the time interval between the application of a specified input pulse during a read cycle and the availability of valid data signal at an output
$t_{a(A)}$	$t_{a(AD)}$	Address access time—the time interval between the application of an address input pulse and the availability of valid data signals at an output
$t_{a(CAS)}$		Column address strobe access time
$t_{a(E)}$	$t_{a(CE)}$	Chip enable access time
$t_{a(G)}$	$t_{a(OE)}$	Output enable access time
$t_{a(PR)}$		Data access time after program
$t_{a(RAS)}$		Row address strobe access time
$t_{a(S)}$	$t_{a(CS)}$	Chip select access time
t_C		Cycle time
t_{CR}	$t_{C(RD)}$	Read cycle time—the time interval between the start of a read cylce and the start of the next cycle
t_{CRF}	$t_{C(REF)}$	Refresh cycle time—the time interval between successive signals that are intended to restore the level in a dynamic memory cell to its original level
t_{CPG}	$t_{C(PG)}$	Page-mode cycle time
t_{CRMW}	$t_{C(RMR)}$	Read-modify-write cycle time—the time interval between the start of a cycle in which the memory is read and new data is entered, and the start of the next cycle
t_{CW}	$t_{C(WR)}$	Write cycle time—the time interval between the start of a write cycle and the start of the next cycle

MITSUBISHI ELECTRIC

New symbol	Former symbol	Parameter—definition
$t_{su(D)}$	$t_{su(DA)}$	Data-in setup time
$t_{su(D-E)}$	$t_{su(DA-CE)}$	Chip enable setup time before data-in
$t_{su(D-W)}$	$t_{su(DA-WR)}$	Write setup time before data-in
$t_{su(E)}$	$t_{su(CE)}$	Chip enable setup time
$t_{su(E-P)}$	$t_{su(CE-P)}$	Precharge setup time before chip enable
$t_{su(G-E)}$	$t_{su(OE-CE)}$	Chip enable setup time before output enable
$t_{su(P-E)}$	$t_{su(P-CE)}$	Chip enable setup time before precharge
$t_{su(PD)}$		Power-down setup time
$t_{su(R)}$	$t_{su(RD)}$	Read setup time
$t_{su(R-CAS)}$	$t_{su(RA-CAS)}$	Column address strobe setup time before read
$t_{su(RA-CAS)}$		Column address strobe setup time before row address
$t_{su(S)}$	$t_{su(CS)}$	Chip select setup time
$t_{su(S-W)}$	$t_{su(CS-WR)}$	Write setup time before chip select
$t_{su(W)}$	$t_{su(WR)}$	Write setup time
t_{THL}		High-level to low-level transition time } the time interval between specified reference points on the edge of the output pulse when the output is going to the low (high) level and when a specified input signal is applied through a specified network and the output is loaded by another specified network
t_{TLH}		Low-level- to high-level transition time }
$t_{v(A)}$	$t_{dv(AD)}$	Data valid time after address
$t_{v(E)}$	$t_{dv(CE)}$	Data valid time after chip enable
$t_{v(E)PR}$	$t_{v(CE)PR}$	Data valid time after chip enable in program mode
$t_{v(G)}$	$t_{v(OE)}$	Data valid time after output enable
$t_{v(PR)}$		Data valid time after program
$t_{v(S)}$	$t_{v(CS)}$	Data valid time after chip select
t_W		Pulse width (pulse duration) the time interval between specified reference points on the leading and training edges of the waveforms
$t_{w(E)}$	$t_{w(CE)}$	Chip enable pulse width
$t_{w(EH)}$	$t_{w(CEH)}$	Chip enable high pulse width
$t_{w(EL)}$	$t_{w(CEL)}$	Chip enable low pulse width
$t_{w(PR)}$		Program pulse width
$t_{w(R)}$	$t_{w(RD)}$	Read pulse width
$t_{w(S)}$	$t_{w(CS)}$	Chip select pulse width
$t_{w(W)}$	$t_{w(WR)}$	Wrtie pulse width
$t_{w(\phi)}$		Clock pulse width
Ta		Ambient temperature
Topr		Operating temperature
Tstg		Storage temperature
V_{BB}		V_{BB} supply voltage
V_{CC}		V_{CC} supply voltage
V_{DD}		V_{DD} supply voltage
V_{GG}		V_{GG} supply voltage
V_I		Input voltage
V_{IH}		High-level input voltage—the value of the permitted high-state voltage at the input
V_{IL}		Low-level input voltage—the value of the permitted low-state voltage at the input
V_O		Output voltage
V_{OH}		High-level output voltage—the value of the guaranteed high-state voltage range at the output
V_{OL}		Low-level output voltage—the value of the guaranteed low-state voltage range at the output
V_{SS}		V_{SS} supply voltage

QUALITY ASSURANCE AND RELIABILITY TESTING

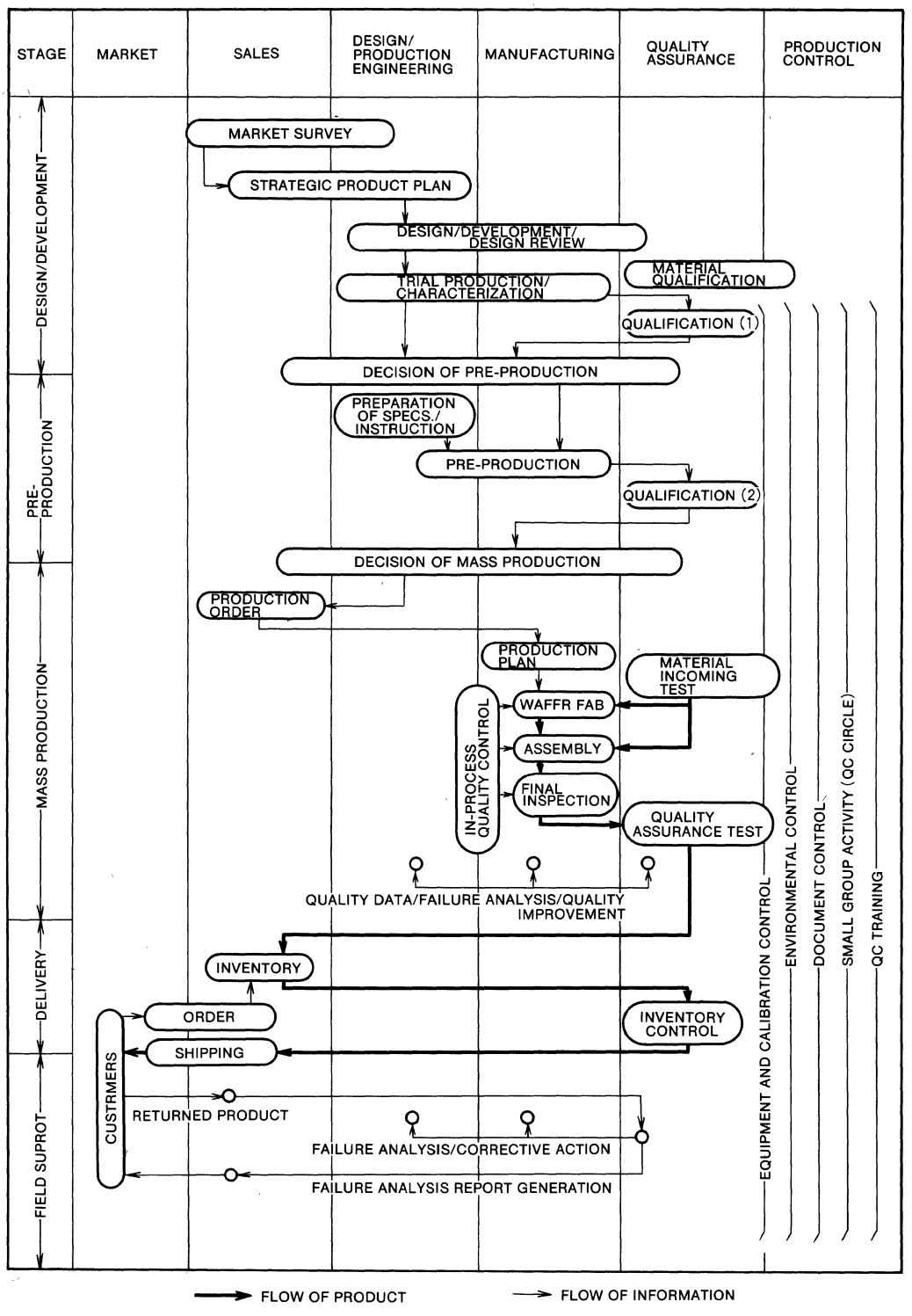


Fig.1 FLOW CHART OF QUALITY ASSURANCE SYSTEM

3 RELIABILITY TEST RESULTS

The reliability test results for Mitsubishi Single-chip 8-bit Microcomputers are shown in Table 2, Table 3 and Table 4.
Table 2 shows the result of endurance tests of steady-state operation life and high temperature storage life test for representative types of Single-chip 8-bit Microcomputers, MELPS 740, MELPS 8-48, MELPS 8-41, and Peripheral LSIs. From Table 2, the combined failure rate of Mitsubishi Single-chip 8-bit Microcomputers is calculated 0.16% /1000hours at 125℃ ambient temperature operation.
Table 3 shows the result of environment test of temperature cycling, high temperature/high humidity and pressure cooker test for the same type of products as of endurance tests.
Table 4 shows the results of mechanical tests for representative products of various package types.

Table 2 ENDURANCE TEST RESULTS

Test	Series	Type Number	Test Condition		Number of	Device Hours	Number of
			T_a(℃)	V_{CC}(volt)	Samples	(Hours)	Failures
High Temperature Operation Life	MELPS 740	M50740-XXXSP	125	7	1084	1,816,000	4
		M50743-XXXSP		6	36	36,000	0
		M50744-XXXSP		7	132	180,000	0
		M50745-XXXFP		6	48	96,000	0
		M50747-XXXSP		7	480	732,000	2
		M50753-XXXFP		6	48	48,000	0
		M50754-XXXSP		6	120	186,000	0
		M50757-XXXSP		6	48	48,000	0
		M50931-XXXFP		6	48	72,000	0
		M50943-XXXFP		6	36	36,000	0
		M50950-XXXSP		6	36	72,000	0
		M50734SP		6	84	132,000	0
		M50747ES	125	7	38	38,000	0
		M50747E-XXXSP		7	140	280,000	1
	MELPS 8-48	M5L8049-XXXP	125	5.5	66	66,000	0
		M5L8050H-XXXP		5.5	72	72,000	0
		M5M80C49-XXXP		5.5	170	170,000	0
	MELPS 8-41	M5L8041A-XXXP	125	5.5	44	44,000	0
		M5L8042-XXXP		5.5	88	88,000	0
	Peripheral	M5L8243P	125	5.5	44	44,000	0
		M5M82C43P		5.5	66	66,000	0
High Temperature Storage Life	MELPS 740	M50740-XXXSP	150	—	448	448,000	0
		M50744-XXXSP			120	120,000	0
		M50747-XXXSP			360	720,000	0
		M50753-XXXFP			32	32,000	0
		M50754-XXXSP			60	60,000	0
		M50931-XXXFP			32	32,000	0
		M50943-XXXFP			22	22,000	0
		M50734SP			48	48,000	0
		M50747ES	250	—	44	44,000	0
		M50747E-XXXSP	175		66	66,000	0
	MELPS 8-48	M5L8049-XXXP	150	—	66	66,000	0
		M5L8050H-XXXP			66	66,000	0
		M5M80C49-XXXP			88	88,000	0
	MELPS 8-41	M5L8041A-XXXP	150	—	44	44,000	0
		M5L8042-XXXP			88	88,000	0
	Peripheral	M5L8243P	150	—	44	44,000	0
		M5M82C43P			66	66,000	0
Low Temperature Storage Life	MELPS 740	M50740-XXXSP	−55	5.5	48	44,000	0
		M50744-XXXSP		5.5	36	36,000	0
		M50747-XXXSP		5.5	36	36,000	0
				—	22	22,000	0
		M50753-XXXSP		5.5	36	36,000	0
		M50757-XXXSP		5.5	48	48,000	0
		M50950-XXXSP		5.5	24	24,000	0
		M50734SP		—	22	44,000	0
		M50747E-XXXSP	−55	5.5	44	44,000	0
	MELPS 8-48	M5L8049-XXXP	−55	—	22	22,000	0
		M5M80C49-XXXP			22	22,000	0
	MELPS 8-41	M5L8042-XXXP	−55	—	22	22,000	0

QUALITY ASSURANCE AND RELIABILITY TESTING

Test	Series	Type Number	Test Condition	Number of Samples	Number of Failures		
					10Cycles	100Cycles	500Cycles
Temperature Cycling	MELPS 740	M50740-XXXSP	−65℃, 30min	220	0	0	1
		M50743-XXXSP	150℃, 30min	38	0	0	0
		M50744-XXXSP		120	0	0	0
		M50745-XXXFP		38	0	0	0
		M50747-XXXSP		400	0	0	0
		M50747-XXXFP		38	0	0	0
		M50753-XXXFP		38	0	0	0
		M50754-XXXSP		88	0	0	0
		M50754-XXXFP		96	0	0	0
		M50931-XXXFP		38	0	0	0
		M50734SP		72	0	0	0
		M50747ES	−65℃, 30min	38	0	0	0
		M50747E-XXXSP	150℃, 30min	38	0	0	0
	MELPS 8-48	M5L8049-XXXP	−65℃, 30min	88	0	0	0
		M5L8050H-XXXP	150℃, 30min	76	0	0	0
		M5M80C49-XXXP		220	0	0	0
		M5MC49-XXXFP		50	0	0	0
	MELPS 8-41	M5L8041A-XXXP	−65℃, 30min	82	0	0	0
		M5L8042-XXXP	150℃, 30min	50	0	0	0
	Peripheral	M5L8243P	−65℃, 30min	38	0	0	0
		M5M82C43P	150℃, 30min	38	0	0	0

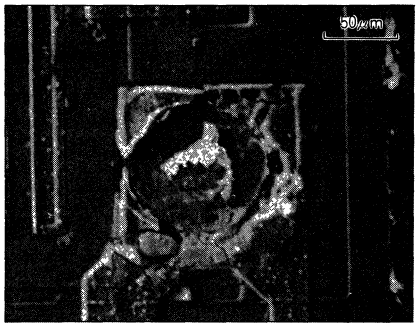


Fig.7 Enlarged micrograph of corroded Aluminum bonding pad

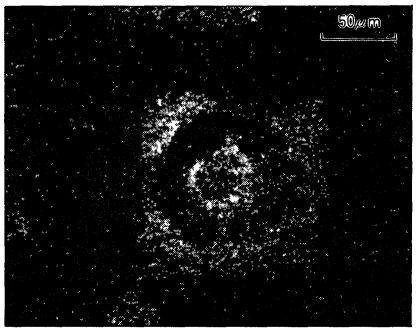


Fig.8 Cl distribution on corroded Aluminum bonding pad

(3) Destructive Failure by Electrical Overstress

Surge voltage marginal tests have been performed to reproduce the electrical overstress failure in field uses. Figure 9 and Figure 10 are an example of failure observed by surge voltage test. The trace of destruction is verified as the aluminum bridge by X ray micro analysis.

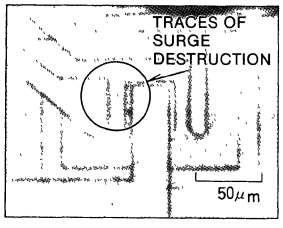


Fig.9 Micrograph of surge voltage destruction

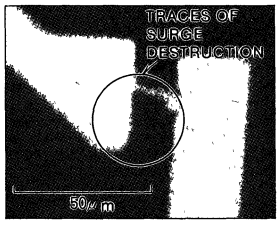


Fig.10 Aluminum trace of destructive spot

(4) Aluminum Electromigration

Figure 11 shows an open circuit of aluminum metallization in high current density region caused by accelerated operation life test. This failure is due to aluminum electromigration. Voids and hillock have been formed in aluminum metallization by high current density operation.

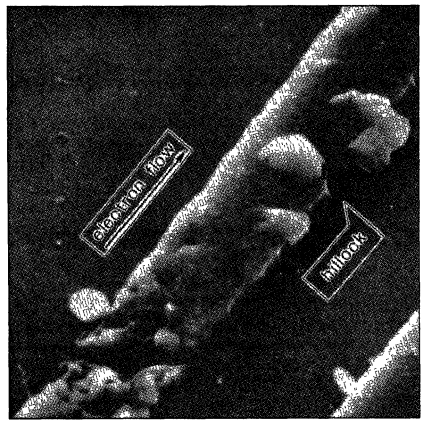


Fig.11 Voids and hillocks formation by Aluminum electromigration

5 SUMMARY

The Mitsubishi quality assurance system and examples of reliability control have been discussed. Customer's interest and requirement for high reliable IC & LSI are increasing significantly. To satisfy customer's expectancy. Mitsubishi as an IC vendor, would like to make perpetual efforts in the following areas.

(1) Emphasis on built-in reliability at design stage and reliability evaluation to investigate latent failure modes and acceleration factors.

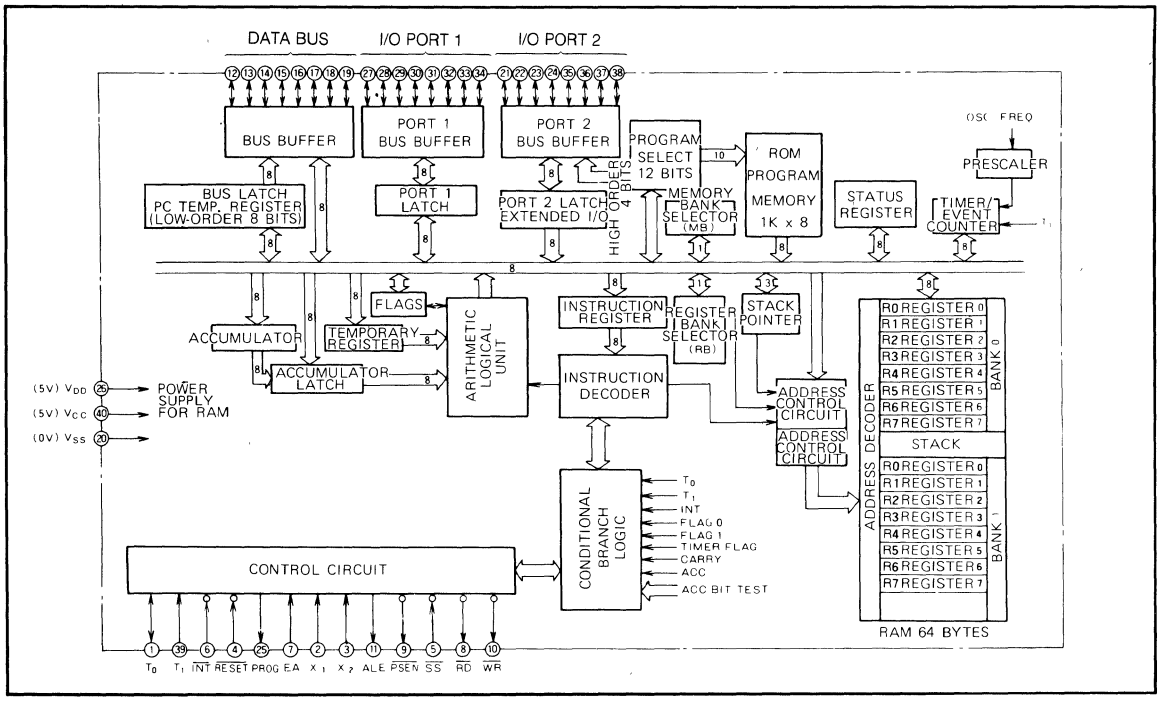
(2) Execution of periodical endurance, environment and mechanical test to verify reliability target and realize higher reliability.

(3) Focus on development of advanced failure analysis techniques. Detail failure analysis, intensive corrective action, and quick response to customer's analysis request.

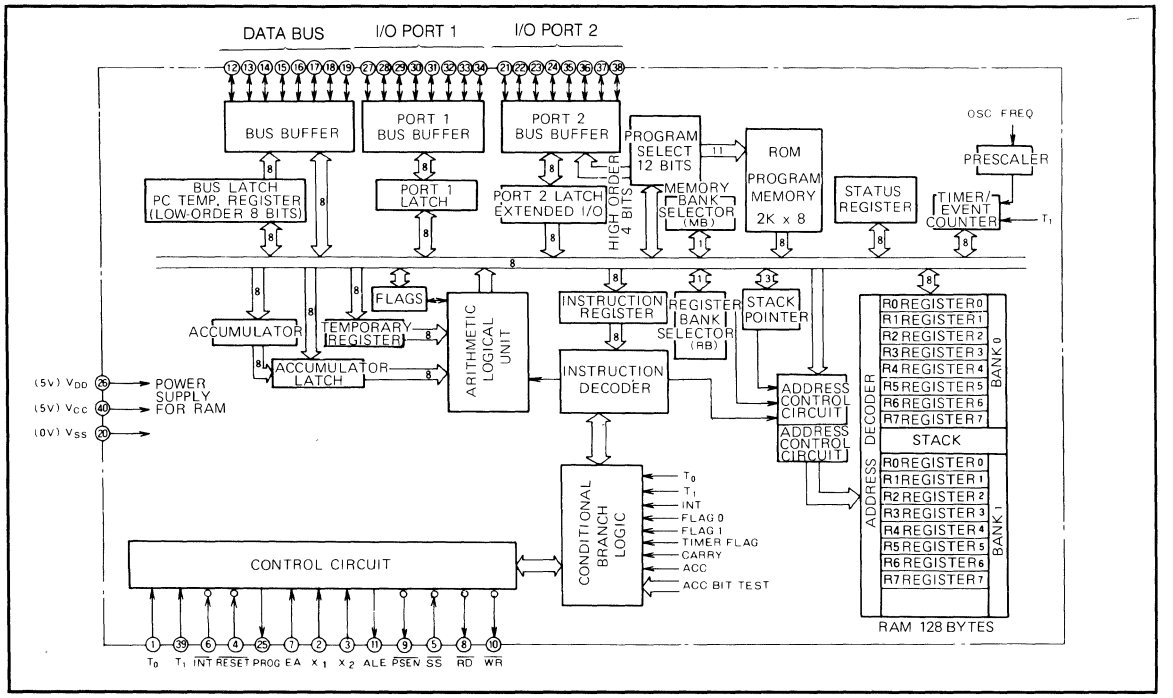
(4) Collection of customer's quality data in qualification, incoming inspection, production and field use to improve PPM, fraction defective and FIT, failure rate.

Mitsubishi would highly appreciate if the customer would provide quality and reliability data of incoming inspection or field failure rate essential to verify and improve the quality/reliability of IC & LSI.

M5L8048-XXXP Block Diagram



M5L8049-XXXP Block Diagram



BASIC FUNCTION BLOCKS

Program Memory (ROM)

The M5L8048-XXXP contain 1024 bytes of ROM. The M5L8049-XXXP contains 2048 bytes of ROM. The program for the users application is stored in this ROM. Addresses 0, 3, 7 of the ROM are reserved for special functions. Table 1 shows the meaning and function of these three special addresses.

Table 1 Reserved, defined addresses and their meanings and functions

Address	Meaning and function
0	The first instruction executed after a system reset
3	The first instruction executed after an external interrupt is accepted.
7	The first instruction executed after a timer interrupt is accepted.

The ROM can be used to store constants and other 8-bit fixed data in addition to the program. Instructions such as MOVP A, @A and MOVP3 A, @A can be used to access the constants and data. The data could be in the form of tables, and can be easily looked up.

Data Memory (RAM)

The M5L8048-XXXP and M5L8748S contain 64 bytes of RAM. The M5L8049-XXXP contains 128 bytes of RAM. The RAM is used for data storage and manipulation and is divided into sections for more efficient processing. Addresses 0~7 and 24~31 form two banks of general purpose registers that can be directly addressed. Addresses 0~7 compose bank 0 and are numbered R0~R7. Addresses 24~31 compose bank 1 and are also numbered R0~R7. Only one bank is active at a time. The instructions SEL RB0 and SEL RB1 are used to select the working bank. Fig. 1 shows the division of the RAM and its mapping.

Addresses 8~23 compose an 8-level program counter stack. The details for using the stack will be found in the "Program Counter and Stack" section. Please refer to that section for details.

The remaining section, addresses 32 and above, must be accessed indirectly using the general-purpose registers R0 or R1. Of course all addresses can be indirectly addressed using the general-purpose registers R0 and R1.

A good practice to simplify programming is to reserve general-purpose register bank 0 for use of the main program and register bank 1 for interrupt programs. For example if register bank 0 (addressed 0~7) is reserved for processing data by the main program, when an interrupt is accepted the first instruction would be to switch the working registers from bank 0 to bank 1. This would save the data of the main program (addresses 0~7). The interrupt program can then freely use register bank1 (addresses 24~31) without destroying or altering data of the main program. When the interrupt processing is complete and control is returned to the main program by the RETR instruction, register bank 0 (in this example) is automatically restored as the working register bank at the same time the main program counter is restored.

Addresses 0~31 have special functions, but when not all of the registers are required, the ones not needed can be used for general storage. This includes both banks of general-purpose registers and the stack.

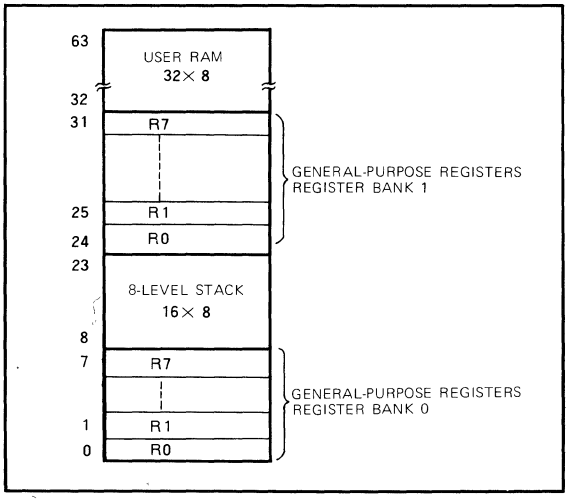


Fig. 4 Data memory (RAM)

PROGRAM COUNTER (PC) AND STACK (SK)

The Series MELPS8-48 program counter is composed of a 12-bit binary counter as shown in Fig. 5. The low-order 10 bits can address 1024 bytes of memory. When the high-order 2 bits are zero, the internal, on chip memory is accessed. The high-order 2 bits can have the values 1~3, which allows the user to add up to three banks of 1024 bytes. The program counter can address up to 4096 bytes of memory.

I/O PORTS

The Series MELPS8-48 has three 8-bit ports, which are called data bus, port 1 and port 2.

Port 1 and Port 2

Ports 1 and 2 and both 8-bit ports with identical properties. The output data of these ports are retained and do not change until another output is loaded into them. When used as inputs the input data is not retained so the input signals must be maintained until an input instruction is executed and completed.

Ports 1 and 2 so-called quasi-bidirectional ports have a special circuit configuration to accomplish this. The special circuit is shown in Fig. 8. All terminals of ports 1 and 2 can be used for input or output.

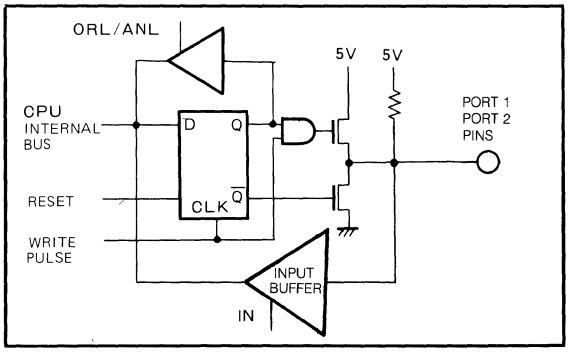


Fig. 8 I/O ports 1 and 2 circuit

Internal on chip pull-up resistors are provided for all the ports. Through the use of pull-up resistors, TTL standard high-level or low-level signals can be supplied. Therefore each terminal can be used for both input and output. To shorten switching time from low-level to high-level, when 1s are output, a device of about 5kΩ or lower is inserted for a short time (about 500ns when using a 6MHz crystal oscillator).

A port used for input must output all 1s before it reads the data from the input terminal. After resetting, a port is set to an input port and remains in this state, therefore it is not necessary to output all 1s if it is to be used for input. In short a port being used for output must output 1s before it can be used for input.

The individual terminals of quasi-bidirectional ports can be used for input or output. Therefore some terminals can be in the input mode while the remaining terminals of a port are in the output mode. This capability of ports 1 and 2 is convenient for inputting or outputting 1-bit or data with few bits. The logical instructions ANL and ORL can easily be used to manipulate the input or output of these ports.

Data Bus (Port 0)

The data bus is an 8-bit bidirectional port, which is used with I/O strobed signals. When the data bus is used for output the output data is latched, but if it is used for input the data is not latched. Unlike ports 1 and 2, which can have individual terminals in the input or output mode, all terminals of the data bus are in the input or output mode.

When the data bus is used as a static port the OUTL instruction can be used to output data and the INS instruction to input data. Strobe pulse $\overline{RD}$ is generated while the INS instruction is being executed or $\overline{WR}$ while OUTL is being executed.

The data bus read/write using MOVX instructions, but then the data bus is a bidirectional port. To write into the data bus a $\overline{WR}$ signal is generated and the data is valid when $\overline{WR}$ goes high. When reading from the data bus, an $\overline{RD}$ signal is generated. The input levels must be maintained until $\overline{RD}$ goes high. When the data bus is not reading/writing, it is in the high-impedance state.

CONDITIONAL JUMPS USING TERMINALS T_0, T_1 and $\overline{INT}$

Conditional jump instructions are used to alter program depending on internal and external conditions (states). Details of the jump instructions for the Series MELPS8-48 can be found in the section on machine instructions.

The input signal status of T_0, T_1 and $\overline{INT}$ can be checked by the conditional jump instructions. These input terminals, through conditional jump instructions such as JTO and JNTO, can be used to control a program. Programs and processing time can be reduced by being able to test data in input terminal rather than reading the data into a register and then testing it in the register.

Terminal T_0, T_1 and $\overline{INT}$ have other functions and uses that are not related to conditional jump instructions. The details of these other functions and uses can be found in the section on terminal functions.

The STRT T instruction is used to change the counter to a timer. The internal clock signal becomes the input to the timer. The internal clock is 1/32 of 400kHz (when using 6MHz crystal) or 12.5kHz. The timer is therefore counted up every 80μs. Fig. 9 shows the timer/event counter.

The counter can be initialized by executing an MOV T, A instruction. The timer can be used to measure 80μs~ 20ms in multiples of 80μs. When it is necessary to measure over 20ms (maximum count 256x80μs) of delay time the number of overflows,one every 20ms, can be counted by the program. To measure times of less than 80μs; external clock pulses can be input through T_1 while the counter is in the event counter mode. Every third (or more) ALE signal can be used instead of an external clock.

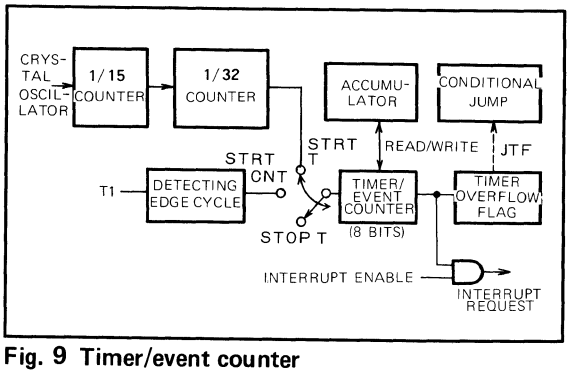


Fig. 9 Timer/event counter

SERIES MELPS8-48 CYCLE TIMING

The output of the state counter is 1/3 the input frequency from the oscillator. When a 6MHz crystal is used for input, the output would be 2MHz (500ns). A CLK signal is generated every 500ns (one state cycle) which is used for the demarcation of each machine state. The instruction ENT0 CLK will output the CLK signal through terminal T_0. The input of the cycle counter is CLK (state cycle) and the output is an ALE signal which is generated every 5 state cycles.

Fig. 11 Shows the relationship between clock and generated cycles.

One machine cycle contains 5 states with a CLK signal for demarcation of each state. The Series MELPS8-48 instructions are executed in one machine cycle or two machine cycles. An instruction cycle can be one or two machine cycles as shown in Fig. 12.

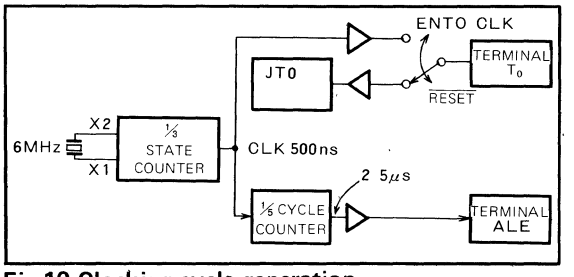


Fig.10 Clocking cycle generation

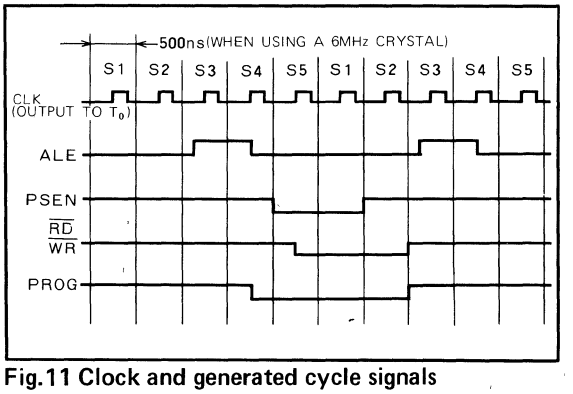


Fig.11 Clock and generated cycle signals

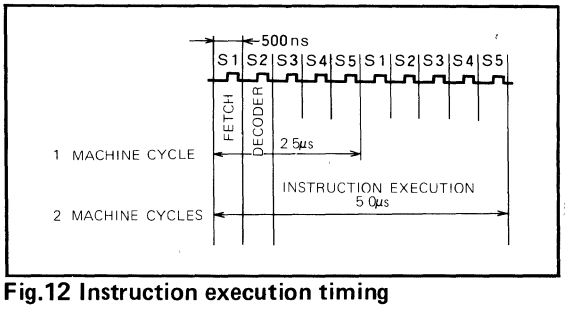


Fig.12 Instruction execution timing

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A type D flip-flop with preset and reset terminals, as shown in Fig. 11, is used to generate the signal for $\overline{SS}$. When the preset terminal goes to low-level, $\overline{SS}$ goes to high-level, which puts the CPU in RUN mode. When the preset terminal is grounded it goes to high-level. Then $\overline{SS}$ goes to low-level. When $\overline{SS}$ goes to low-level, the CPU stops. Then when the push-button switch is pushed, a pulse is sent to the clock terminal of the type D flip-flop which turns $\overline{SS}$ to high-level. When $\overline{SS}$ goes to high-level the CPU fetches the next instruction and begins to execute it, but then an ALE signal is sent to the reset terminal of the type D flip-flop which turns $\overline{SS}$ to low-level. The CPU again stops as soon as execution of the current instruction is completed. When the push-button switch is again pushed, the cycle is repeated and the CPU is in single-step operation as shown in Fig. 12. While the CPU is stopped in single-step operation, the data bus and the low-order 4 bits of port 2 are used to output the memory address of the next instruction to be fetched. This interferes with input and output, but essential input/output can be latched by using the rising edge of ALE as clock.

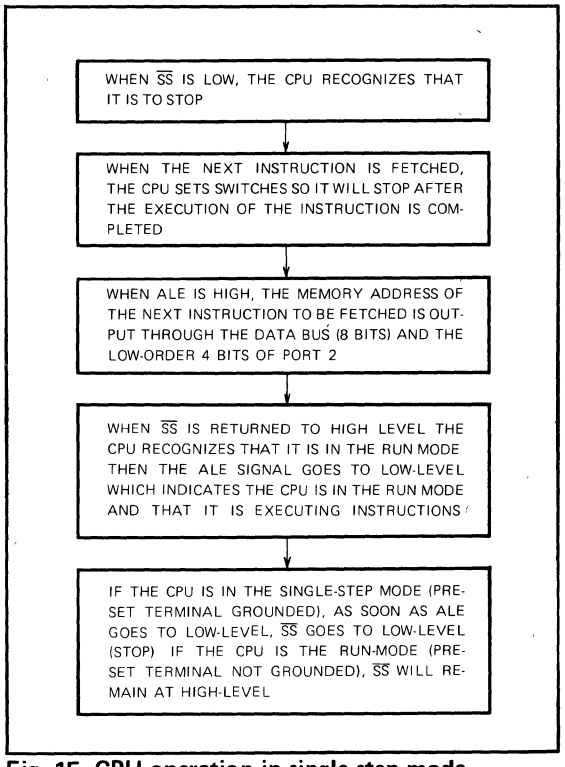


Fig. 15 CPU operation in single-step mode

Central Processing Unit (CPU)

Central Processing Unit (CPU) is composed of an 8-bit parallel arithmetic unit, accumulator, flag flip-flop and instruction decoder. The 8-bit parallel arithmetic unit has circuitry to perform the four basic arithmetic operations (plus, minus, multiply and divide) as well as logical operations such as AND and OR. The flag flip-flop is used to indicate status such as carry and zero. The accumulator contains one of the operations and the result is usually retained in the accumulator.

FUNCTION OF SERIES MELPS 8-48 MICROCOMPUTERS

Type	Mnemonic	Instruction code $D_7 D_6 D_5 D_4$ $D_3 D_2 D_1 D_0$	Hexa-decimal	Bytes	Cycles	Function	Effected carry C	AC	Note	Description
Arithmetic	**ANL A, #n**	0 1 0 1 0 0 1 1 $n_7 n_6 n_5 n_4$ $n_3 n_2 n_1 n_0$	5 3 n	2	2	(A) ← (A) ∧ n				The logical product of the contents of register A and data n, is stored in register A
	ANL A, Rr	0 1 0 1 1 $r_2 r_1 r_0$	5 8 + r	1	1	(A) ← (A) ∧ (Rr) r = 0 ~ 7				The logical product of the contents of register A and the contents of register R_r, is stored in register A
	ANL A, @Rr	0 1 0 1 0 0 0 r_0	5 0 + r	1	1	(A) ← (A) ∧ (M(Rr)) r = 0 ~ 1				The logical product of the contents of register A and the contents of memory location, of the current page, whose address is in register R_r, is stored in register A
	ORL A, #n	0 1 0 0 0 0 1 1 $n_7 n_6 n_5 n_4$ $n_3 n_2 n_1 n_0$	4 3 n	2	2	(A) ← (A) ∨ n				The logical sum of the contents of register A and data n, is stored in register A
	ORL A, Rr	0 1 0 0 1 $r_2 r_1 r_0$	4 8 + r	1	1	(A) ← (A) ∨ (Rr) r = 0 ~ 7				The logical sum of the contents of register A and the contents of register R_r is stored in register A
	ORL A, @Rr	0 1 0 0 0 0 0 r_0	4 0 + r	1	1	(A) ← (A) ∨ (M(Rr)) r = 0 ~ 1				The logical sum of the contents of register A and the contents of memory location, of the current page, whose address is in register R_r, is stored in register A
	XRL A, #n	1 1 0 1 0 0 1 1 $n_7 n_6 n_5 n_4$ $n_3 n_2 n_1 n_0$	D 3 n	2	2	(A) ← (A) ∀ n				The exclusive OR of the contents of register A and data n, is stored in register A
	XRL A, Rr	1 1 0 1 1 $r_2 r_1 r_0$	D 8 + r	1	1	(A) ← (A) ∀ (Rr) r = 1 ~ 7				The exclusive OR of the contents of register A and the contents of register R_r is stored in register A
	XRL A, @Rr	1 1 0 1 0 0 0 r_0	D 0 + r	1	1	(A) ← (A) ∀ (M(Rr)) r = 0 ~ 1				The exclusive OR of the contents of register A and the contents of memory location, of the current page, whose address is in register R_r, is stored in register A
	INC A	0 0 0 1 0 1 1 1	1 7	1	1	(A) ← (A) + 1				Increments the contents of register A by 1 The result is stored in register A, and the carries are unchanged
	DEC A	0 0 0 0 0 1 1 1	0 7	1	1	(A) ← (A) − 1				Decrements the contents of register A by 1 The result is stored in register A, and the carries are unchanged
	CLR A	0 0 1 0 0 1 1 1	2 7	1	1	(A) ← 0				Clears the contents of register A, resets to 0
	CPL A	0 0 1 1 0 1 1 1	3 7	1	1	(A) ← $(\overline{A})$				Forms 1's complement of register A, and stores it in register A
	DA A	0 1 0 1 0 1 1 1	5 7	1	1	(A) ← (A) 10 Hexadecimal	○	○	1	The contents of register A is converted to binary coded decimal notion, and it is stored in register A If the contents of register A are more than 99 the carry flags are set to 1 otherwise they are reset to 0
	SWAP A	0 1 0 0 0 1 1 1	4 7	1	1	$(A_4 \sim A_7) \longleftrightarrow (A_0 \sim A_3)$				Exchanges the contents of bits 0~3 of register A with the contents of bits 4~7 of register A
	RL A	1 1 1 0 0 1 1 1	E 7	1	1	$(A_{n+1}) \leftarrow (A_n)$ $(A_0) \leftarrow (A_7)$ n = 0 ~ 6				Shifts the contents of register A left one bit A_7 the MSB is rotated to A_0 the LSB
	RLC A	1 1 1 1 0 1 1 1	F 7	1	1	$(A_{n+1}) \leftarrow (A_n)$ $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$ n = 0 ~ 6	○			Shifts the contents of register A left one bit A_7 the MSB is shifted to the carry flag and the carry flag is shifted to A_0 the LSB
	RR A	0 1 1 1 0 1 1 1	7 7	1	1	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$ n = 0 ~ 6				Shifts the contents of register A right one bit A_0 the LSB is rotated to A_7 the MSB
	RRC A	0 1 1 0 0 1 1 1	6 7	1	1	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$ n = 0 ~ 6	○			Shifts the contents of register A right one bit A_0 the LSB is shifted to the carry flag and the carry flag is shifted to A_7 the MSB
Register arithmetic	**INC Rr**	0 0 0 1 1 $r_2 r_1 r_0$	1 8 + r	1	1	(Rr) ← (Rr) + 1 r = 0 ~ 7				Increments the contents of register R_r by 1 The result is stored in register R_r and the carries are unchanged
	INC @Rr	0 0 0 1 0 0 0 r_0	1 0 + r	1	1	(M(Rr)) ← (M(Rr)) + 1 r = 0 ~ 1				Increments the contents of the memory location, of the current page, whose address is in register R_r by 1 Register R_r uses bit 0~5
	DEC Rr	1 1 0 0 1 $r_2 r_1 r_0$	C 8 + r	1	1	(Rr) ← (Rr) − 1 r = 0 ~ 7				Decrements the contents of register R_r by 1 The result is stored in register R_r and the carries are unchanged

FUNCTION OF SERIES MELPS 8-48 MICROCOMPUTERS

Item / Type	Mnemonic	Instruction code $D_7 D_6 D_5 D_4$	$D_3 D_2 D_1 D_0$	Hexa-decimal	Bytes	Cycles	Function	Effected carry C	AC	Note	Description
Subroutine call	**CALL m**	$m_{10} m_9 m_8$ 1	0 1 0 0 $m_7 m_6 m_5 m_4$	14 + $(m_8 - m_{10}) \times 2$ m	2	2	((SP)) ← (PC) (PSW4 ~ PSW7) (SP) ← (SP) + 1 ($PC_{0 \sim 10}$) ← m (PC_{11}) ← MBF				Calls subroutine from address m The program counter and the 4 high-order bits of the PSW are stored in the address indicated by the stack pointer (SP) The SP is incremented by 1 and m is transferred to PC_0 ~ PC_{10} and the MBF is transferred to PC_{11}
	RET	1 0 0 0	0 0 1 1	83	1	2	(SP) ← (SP) − 1 (PC) ← ((SP))				The SP is decremented by 1 The program counter is restored to the saved setting in the stack indicated by the stack pointer The PSW is not changed and interrupt disabled is maintained
	RETR	1 0 0 1	0 0 1 1	93	1	2	(SP) ← (SP) − 1 (PC) (PSW4 ~ PSW7) ← ((SP))				The SP is decremented by 1 The program counter and the 4 high-order bits of the PSW are restored with the saved data in the stack indicated by the stack pointer The interrupt becomes enabled after the execution is completed
Input/Output control	**IN A, Pp**	0 0 0 0	1 0 $p_1 p_0$	08 + p	1	2	(A) ← (Pp) p = 1 ~ 2				Loads the contents of P_p to register A
	OUTL Pp, A	0 0 1 1	1 0 $p_1 p_0$	38 + p	1	2	(Pp) ← (A) p = 1 ~ 2				Output latches the contents of register A to P_p
	ANL Pp, #n	1 0 0 1 $n_7 n_6 n_5 n_4$	1 0 $p_1 p_0$ $n_3 n_2 n_1 n_0$	98 + p n	2	2	(Pp) ← (Pp) ∧ n p = 1 ~ 2				Logical ANDs the contents of P_p and data n Outputs the result to P_p
	ORL Pp, #n	1 0 0 0 $n_7 n_6 n_5 n_4$	1 0 $p_1 p_0$ $n_3 n_2 n_1 n_0$	88 + p n	2	2	(Pp) ← (Pp) ∨ n p = 1 ~ 2				Logical ORs the contents of P_p and data n Outputs the result to P_p
	INS A, BUS	0 0 0 0	1 0 0 0	08	1	2	(A) ← (BUS)				Enters the contents of data bus (port 0) to register A
	OUTL BUS, A	0 0 0 0	0 0 1 0	02	1	2	(BUS) ← (A)				Output latches the contents of register A data to data bus (port 0)
	ANL BUS, #n	1 0 0 1 $n_7 n_6 n_5 n_4$	1 0 0 0 $n_3 n_2 n_1 n_0$	98 n	2	2	(BUS) ← (BUS) ∧ n				Logical ANDs the contents of data bus (port 0) and data n Outputs the result to data bus (port 0)
	ORL BUS, #n	1 0 0 0 $n_7 n_6 n_5 n_4$	1 0 0 0 $n_3 n_2 n_1 n_0$	88 n	2	2	(BUS) ← (BUS) ∨ n				Logical ORs the contents of data bus (port 0) and data n Outputs the result to data bus (port 0)
	MOVD A, Pp	0 0 0 0	1 1 $p_1 p_0$	0C + $p_1 p_0$	1	2	(A_0 ~ A_3) ← (Pp_0 ~ Pp_3) (A_4 ~ A_7) ← 0 p = 4 ~ 7				Inputs the contents of P_p to the low-order 4 bits of register A and inputs 0 to the high-order 4 bits of register A
	MOVD Pp, A	0 0 1 1	1 1 $p_1 p_0$	3C + $p_1 p_0$	1	2	(Pp_0 ~ Pp_3) ← (A_0 ~ A_3) p = 4 ~ 7				Outputs the low-order 4 bits of register A to P_p
	ANLD Pp, A	1 0 0 1	1 1 $p_1 p_0$	9C + $p_1 p_0$	1	2	(Pp_0 ~ Pp_3) ← (Pp_0 ~ Pp_3) ∧ (A_0 ~ A_3) p = 4 ~ 7				Logical ANDs the 4 low-order bits of register A and the contents of P_p P_p contains the result
	ORLD Pp, A	1 0 0 0	1 1 $p_1 p_0$	8C + $p_1 p_0$	1	2	(Pp_0 ~ Pp_3) ← (Pp_0 ~ Pp_3) ∨ (A_0 ~ A_3) p = 4 ~ 7				Logical ORs the 4 low-order bits of register A and the contents of P_p P_p contains the result

P_p's used for multiplying 8243 ports are P_4 ~ P_7
Correspondence to p_2, p_1 is shown below
P4 $p_1 p_2 = 00$
P5 $p_1 p_2 = 01$
P6 $p_1 p_2 = 10$
P7 $p_1 p_2 = 11$

FUNCTION OF SERIES MELPS 8-48 MICROCOMPUTERS

Item	Details of execution
RESET input low level	TF(Timer Flag) ← 0 TIRF(Timer INT Request FF) ← 0 TCNTF(Timer INT Enable FF) ← 0 INTE(External INT Enable FF) ← 0 IFF(INT Enable FF) ← 1
JTF execution	TF(Timer Flag) ← 0
Timer/event counter overflow	TF(Timer Flag) ← 1 When TIRF(Timer INT Request FF) ← 1 TCNTF(Timer INT Enable FF) = 1
EN TCNTI execution	TCNTF(Timer INT Enable FF) ← 1
DIS TCNTI execution	TCNTF(Timer INT Enable FF) ← 0
EN I execution	INTF(External INT Enable FF) ← 1
DIS I execution	INTF(External INT Enable FF) ← 0
RETR execution	IEF(INT Enable FF) ← 1

Symbol	Meaning	Symbol	Meaning
A	8-bit register (accumlator)	PC	Program counter
A_0~A_3	The low-order 4 bits of the register A	PC_0~PC_7	The low-order 8 bits of the program counter
A_4~A_7	The high-order 4 bits of the register A	PC_8~PC_{10}	The high-order 3 bits of the program counter
A_0~A_n, A_{n+1}	The bits of the register A	PSW	Program status word
b	The value of the bits 5~7 of the first byte machine code		
$b_7b_6b_5$	The bits 5~7 of the first byte machine code	Rr	Register designator
BS	Register bank select	r	Register number
BUS	Corresponds to the port 0 (bus I/O port)	r_0	The value of bit 0 of the machine code
		$r_2r_1r_0$	The value of bits 0~2 of the machine code
AC	Auxiliary carry flag	$s_2s_1s_0$	The value of bits 0~2 of the stack pointer
C	Carry flag	SP	Stack pointer
DBB	Data bus buffer	ST_4~ST_7	Bits 4~7 of the status register
		STS	System status
F_0	Flag 0	T	Timer/event counter
F_1	Flag 1	T_0	Test pin 0
INTF	Interrupt flag	T_1	Test pin 1
IBF	Input buffer full flag	TCNTF	Timer/event counter overflow interrupt flag
m	The value of the 11-bit address	TF	Timer flag
$m_7m_6m_5m_4m_3m_2m_1m_0$	The second byte (low-order 8 bits) machine code of the 11-bit address		
$m_{10}m_9$ m_8	The bits 5~7 of the first byte (high-order 3 bits) machine code ofothe 11-bit address	#	Symbol to indicate the immediate data
(M (A))	The content of the memory location addressed by the register A	@	Symbol to indicate the cuntent of the memory location
(M (Rr))	The content of rhe memory location addressed by the register Rr		address by the register
(Mx(Rr))	The content of the external memory location addressed by the register Rr	←	Shows direction of data flow
MBF	Memory bank flag	↔	Exchanges the contents of data
n	The value of the immediate data	( )	Contents of register, memory location or flag
$n_7n_6n_5n_4n_3n_2n_1n_0$	The immediate data of the second byte machine code	∧	Logical AND
OBF	Output buffer full flag	∨	Inclusive OR
		∀	Exclusive OR
p	Port number	—	Negation
Pp	Port designator	○	Content of flag is set or reset after execution
p_1p_0	The bits of the machine code corresponding to the port number		

M5L8048-XXXP/M5L8035LP

SINGLE-CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The M5L8048-XXXP and M5L8035LP are 8-bit parallel microcomputer fabricated on a single chip using high-speed N-channel silicon-gate ED-MOS technology.

M5L8048-XXXP	Built-in ROM (1K bytes)
M5L8035LP	External ROM

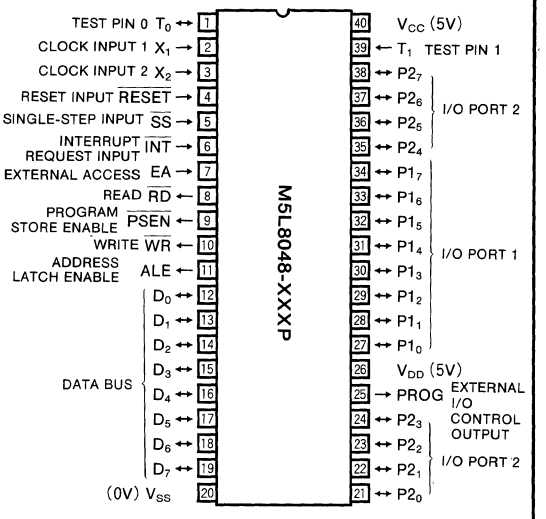
FEATURES

- Single 5V power supply
- Instruction cycle ..... 2.5μs (min)
- Basic machine instructions: 96
  - 1-byte instructions: 68
  - 2-byte instructions: 28
- Direct addressing ..... up to 4096 bytes
- Internal ROM ..... 1024 bytes (for M5L8048-XXXP only)
- Internal RAM ..... 64 bytes
- Built-in timer/event counter ..... 8 bits
- I/O Ports ..... 27 lines
- Easily expandable Memory and I/O
- Subroutine nesting ..... 8 levels
- External and timer/event counter interrupt . 1 level each
- Low power standby mode
- External RAM ..... 256 bytes
- Interchangeable with i8048 and i8035L in pin configuration and electrical characteristics

APPLICATION

- Control processor or CPU for a wide variety of applications

PIN CONFIGURATION (TOP VIEW)

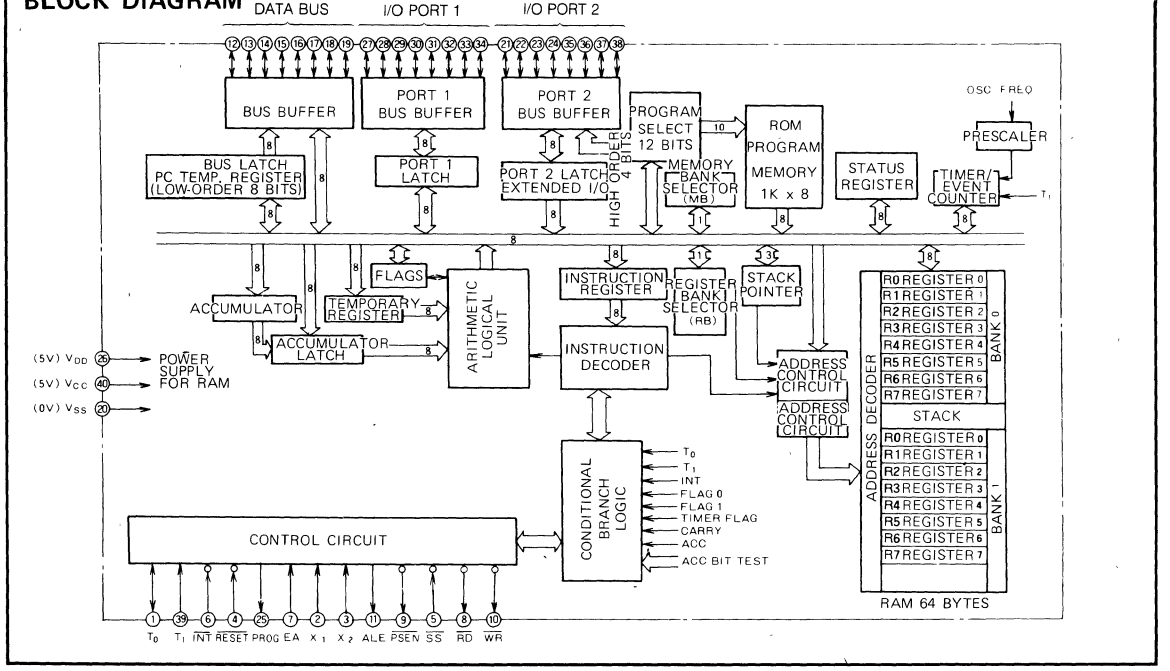


Outline 40P4

FUNCTION

The M5L8048-XXXP and M5L8035LP are integrated 8-bit CPU, with memory (ROM, RAM) and timer/event counter interrupt all contained on a single chip.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_{DD}	Supply voltage		−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Power dissipation	Ta＝25℃	1.5	W
Topr	Operating free-air temperature range		−20～75	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH1}	High-level input voltage, except X1, X2 and $\overline{RESET}$	2		V_{CC}	V
V_{IH2}	High-level input voltage, except X1, X2 and $\overline{RESET}$	3.8		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (Ta＝−20～75℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL1}	Low-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	$I_{OL}=2mA$			0.45	V
V_{OL2}	Low-level output voltage, except the above and PROG	$I_{OL}=1.6mA$			0.45	V
V_{OL3}	Low-level output voltage, PROG	$I_{OL}=1mA$			0.45	V
V_{OH1}	High-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	$I_{OH}=-100\mu A$	2.4			V
V_{OH2}	High-level output voltage, except the above	$I_{OH}=-50\mu A$	2.4			V
I_I	Input leak current, T1, $\overline{INT}$	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{OZ}	Output leak current, BUS, T0 high-impedance state	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{LI1}	Input current during low-level input, port	$V_{IL}=0.8V$		−0.2		mA
I_{LI2}	Input current during low-level input, $\overline{RESET}$, $\overline{SS}$	$V_{IL}=0.8V$		−0.05		mA
I_{DD}	Supply current from V_{DD}			10	20	mA
$I_{DD}+I_{CC}$	Supply current from V_{DD} and V_{CC}			65	135	mA

TIMING REQUIREMENTS (Ta＝−20～75℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Limits			Unit
			Min	Typ	Max	
t_C	Cycle time	t_{CY}	2.5		15.0	μs
$t_{h\ (PSEN-D)}$	Data hold time after $\overline{PSEN}$	t_{DR}	0		200	ns
$t_{h\ (R-D)}$	Data hold time after $\overline{RD}$	t_{DR}	0		200	ns
$t_{su\ (PSEN-D)}$	Data setup time after $\overline{PSEN}$	t_{RD}			500	ns
$t_{su\ (R-D)}$	Data setup time after $\overline{RD}$	t_{RD}			500	ns
$t_{su\ (A-D)}$	Data setup time after address	t_{AD}			950	ns
$t_{su\ (PROG-D)}$	Data setup time after PROG	t_{PR}			810	ns
$t_{h\ (PROG-D)}$	Data hold time before PROG	t_{PF}	0		150	ns

Note 1 The input voltage level of the input voltage is V_{IL}=0.45V and V_{IH}=2.4V

M5L8049-XXXP, P-6
M5L8039P-11, P-6

SINGLE-CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The M5L8049-XXXP, P-6 and M5L8039P-11, P-6 are 8-bit parallel microcomputers fabricated on a single chip using high-speed N-channel silicon gate ED-MOS technology.

Speed \ ROM Type	Internal ROM Type	External ROM Type
11 MHz Type	M5L8049-XXXP	M5L8039P-11
6 MHz Type	M5L8049-XXXP-6	M5L8039P-6

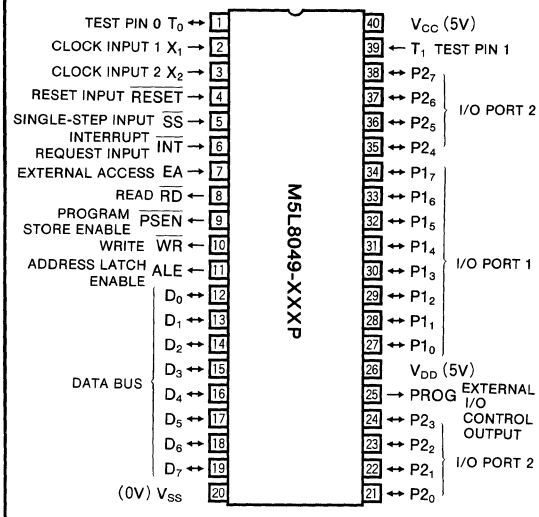
FEATURES

- Single 5V power supply
- Instruction cycle

11MHz	8MHz	6MHz
1.36μs(min)	1.875μs(min)	2.5μs(min)

- Basic machine instructions 96
  - 1-byte instructions: 68
  - 2-byte instructions: 28
- Direct addressing . . . . . up to 4096 bytes
- Internal RAM . . . . . 128 bytes
- Built-in timer/event counter . . . . . 8 bits
- I/O Ports . . . . . 27 lines
- Easily expandable Memory and I/O:
- Subroutine nesting . . . . . 8 levels
- External and timer/event counter interrupt . 1 level each
- External RAM . . . . . 256 bytes
- M5L8049-XXXP/M5L8039P-11, P-6 are interchangeable with i8049/i8039, i8039-6 in pin configuration and electrical characteristics.

PIN CONFIGURATION (TOP VIEW)

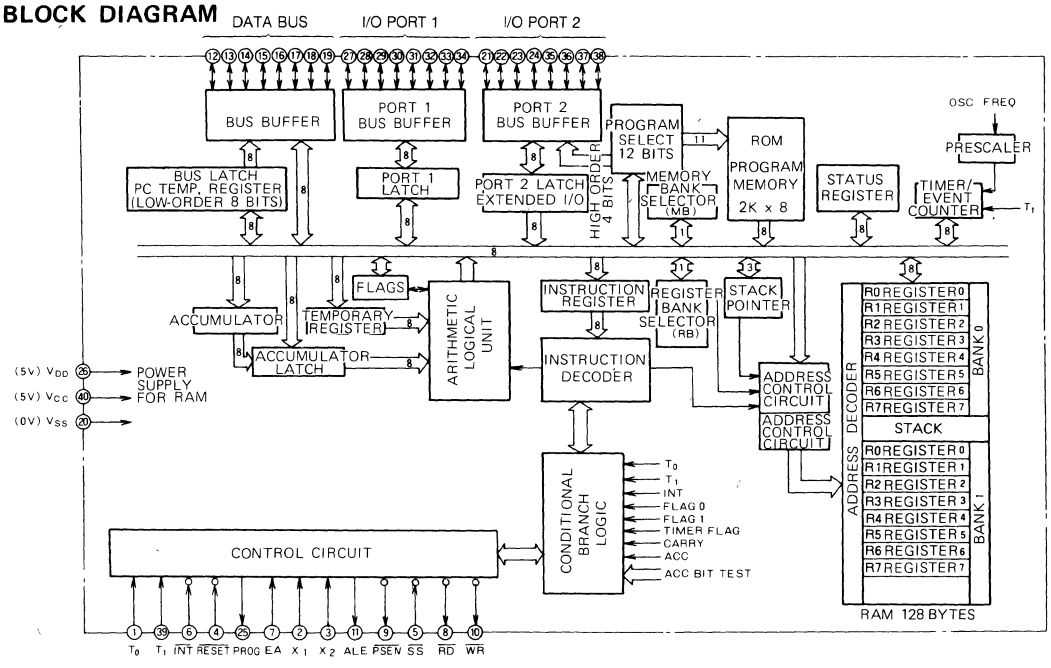


Outline 40P4

APPLICATION

- Control processor or CPU for a wide variety of applications

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_{DD}	Supply voltage		−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Power dissipation	Ta＝25℃	1.5	W
Topr	Operating free-air temperature range	M5L8049-XXXP-6 M5L8039P-6	−20～75	℃
		M5L8049-XXXP M5L8039-11	0～70	
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH1}	High-level input voltage, except for X_1, X_2, $\overline{RESET}$	2		V_{CC}	V
V_{IH2}	High-level input voltage, X_1, X_2, $\overline{RESET}$	3.8		V_{CC}	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (Ta＝−20～75℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL1}	Low-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	$I_{OL}=2mA$			0.45	V
V_{OL2}	Low-level output voltage, except for the above and PROG	$I_{OL}=1.6mA$			0.45	V
V_{OL3}	Low-level output voltage PROG	$I_{OL}=1mA$			0.45	V
V_{OH1}	High-level output voltage, BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE	$I_{OH}=-100\mu A$	2.4			V
V_{OH2}	High-level output voltage, except for the above	$I_{OH}=-50\mu A$	2.4			V
I_I	Input leak current, T1, $\overline{INT}$	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{OZ}	Output leak current, BUS, TO, high-impedance state	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{LI1}	Input current during low-level input, port	$V_{IL}=0.8V$		−0.2		mA
I_{LI2}	Input current during low-level input, $\overline{RESET}$, $\overline{SS}$	$V_{IL}=0.8V$		−0.05		mA
I_{DD}	Supply current from V_{DD}	Ta＝25℃		25	50	mA
$I_{DD}+I_{CC}$	Supply current from V_{DD} and V_{CC}	Ta＝25℃		100	170	mA

TIMING REQUIREMENTS (Ta＝−20～75℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Limits									Unit
			M5L8049-XXXP M5L8039P-11 (Note 2)			M5L8049-XXXP-8 M5L8039P-8			M5L8049-XXXP-6 M5L8039P-6			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
tc	Cycle time	t_{CY}	1.36		15.0	1.875		15.0	2.5		15.0	μs
th (PSEN-D)	Data hold time after $\overline{PSEN}$	t_{DR}	0		100	0		150	0		200	ns
th (R-D)	Data hold time after $\overline{RD}$	t_{DR}	0		100	0		150	0		200	ns
tsu (PSEN-D)	Data setup time after $\overline{PSEN}$	t_{RD}			200			350			500	ns
tsu (R-D	Data setup time after $\overline{RD}$	t_{RD}			200			350			500	ns
tsu (A-D)	Data setup time after address	t_{AD}			400			650			950	ns
tsu (PROG-D)	Data setup time after PROG	t_{PR}			650			700			810	ns
th (PROG-D)	Data hold time before PROG	t_{PF}	0		150	0		150	0		150	ns

Note 1 : The input voltage are $V_{IL}=0.45V$ and $V_{IH}=2.4V$.
2 : Ta＝0～70℃

M5M8050H-XXXP/M5M8040HP

SINGLE-CHIP 8-BIT MICROCOMPUTER

DESCRIPTION

The M5M8050H-XXXP/M5M8040HP is an 8-bit parallel microcomputer fabricated on a single chip using N-channel silicon gate ED-MOS technology.

M5M8050H-XXXP	Internal ROM Type (4K Bytes)
M5M8040HP	External ROM Type

FEATURES

- Single 5V power supply
- Instruction cycle ..... 1.36μs (min)
- Basic machine instructions .. 96 (1-byte instructions: 68)
- 4K-bytes memory addressing possible
  (direct addressing possible in 2K bytes memory)
- Memory capacity: ROM ..... 4K bytes
  RAM ..... 256 bytes
- Built-in timer/event counter ..... 8 bits
- I/O ports ..... 27 lines
- Easily expandable Memory and I/O
- Subroutine nesting ..... 8 levels
- External and timer/event counter interrupt, 1 level each
- Low power standby mode

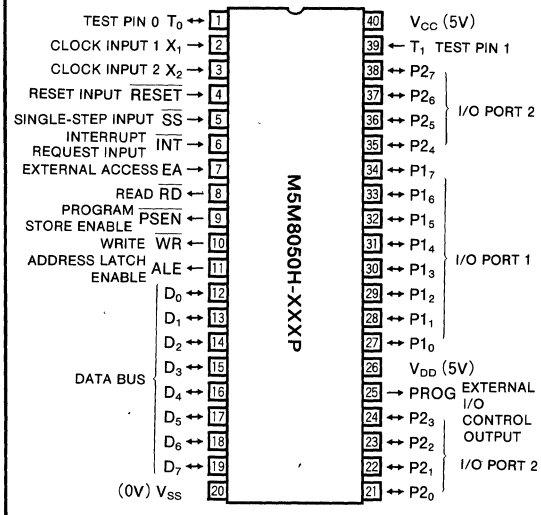
APPLICATION

Control processor or CPU for a wide variety of applications

FUNCTION

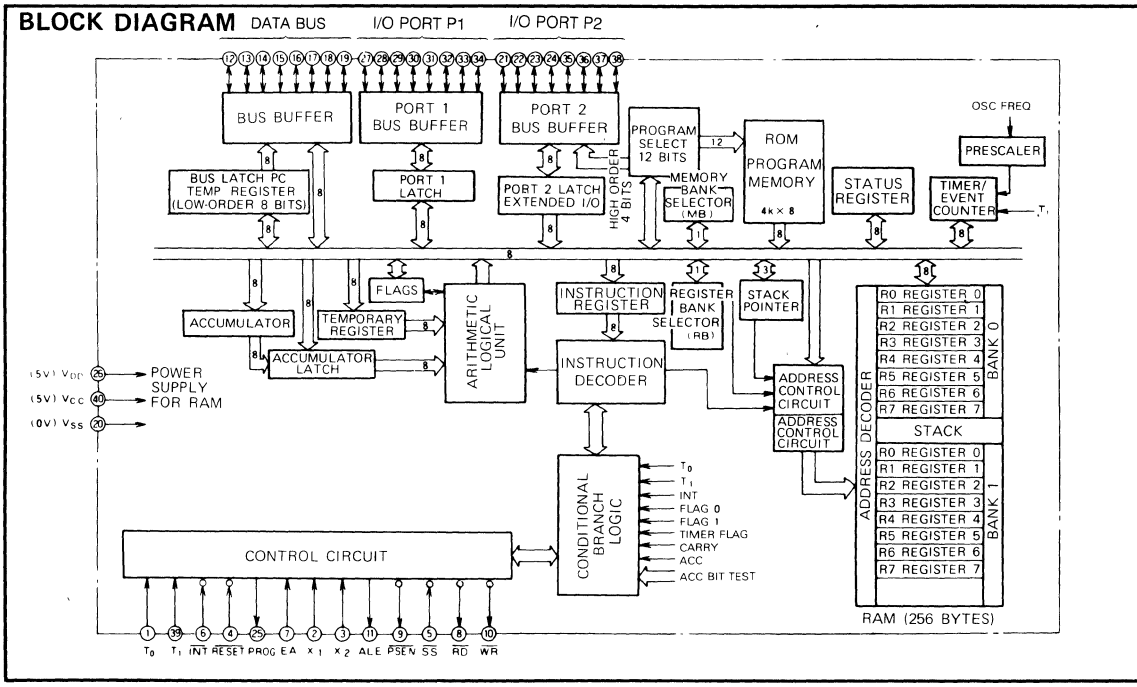
The M5M8050H-XXXP/M5M8040HP is an 8-bit CPU, with memory (ROM, RAM) and timer/event counter interrupt all contained a single chip.

PIN CONFIGURATION (TOP VIEW)



Outline 40P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_{DD}	Supply voltage		−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Power dissipation	Ta＝25℃	1.5	W
Topr	Operating free-air temperature range		0～70	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃, unless otherwise noted)

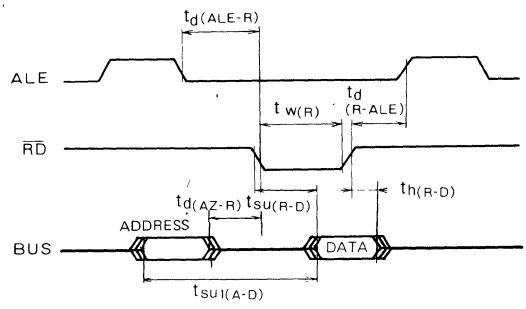
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH1}	High-level input voltage, except X_1, X_2 and $\overline{RESET}$	2		V_{CC}	V
V_{IH2}	High-level input voltage, X_1, X_2 and $\overline{RESET}$	3.8		V_{CC}	V
V_{IL1}	Low-level input voltage, except X_1, X_2 and $\overline{RESET}$	−0.5		0.8	V
V_{IL2}	Low-level input voltage, X_1, X_2 and $\overline{RESET}$	−0.5		0.6	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, $V_{CC}=V_{DD}=5V\pm10\%$, $V_{SS}=0V$, unless otherwise noted)

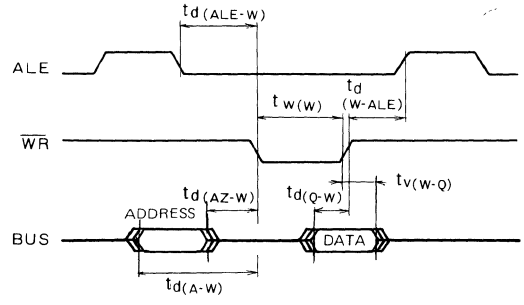
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL}	Low-level output voltage (BUS)	$I_{OL}=2mA$			0.45	V
V_{OL1}	Low-level output voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	$I_{OL}=1.8mA$			0.45	V
V_{OL2}	Low-level output voltage (PROG)	$I_{OL}=1mA$			0.45	V
V_{OL3}	Low-level output voltage (for other outputs)	$I_{OL}=1.6mA$			0.45	V
V_{OH}	High-level output voltage (BUS)	$I_{OH}=-400\mu A$	2.4			V
V_{OH1}	High-level output voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	$I_{OH}=-100\mu A$	2.4			V
V_{OH2}	High-level output voltage (for other outputs)	$I_{OH}=-40\mu A$	2.4			V
I_I	Input leak current (T_1, $\overline{INT}$)	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{OZ}	Output leak current (BUS, T_0) high-impedance state	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$	−10		10	μA
I_{I1}	Input leak current (PORT)	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$		−0.2	−0.5	mA
I_{I2}	Input leak current ($\overline{RESET}$, $\overline{SS}$)	$V_{SS}+0.45\leqq V_{IN}\leqq V_{CC}$		−0.05		mA
I_{DD}	Supply current from V_{DD}			10	20	mA
$I_{DD}+I_{CC}$	Supply current from V_{DD} and V_{CC}			70	140	mA

TIMING DIAGRAM

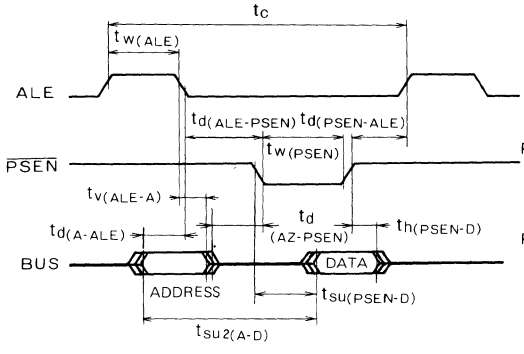
Read from External Data Memory



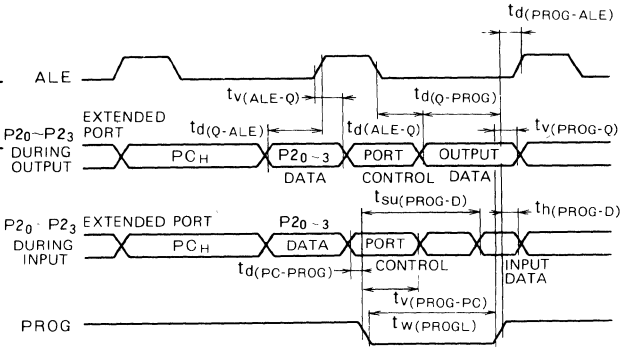
Write to External Data Memory



Instruction Fetch from External Program Memory



Port 2

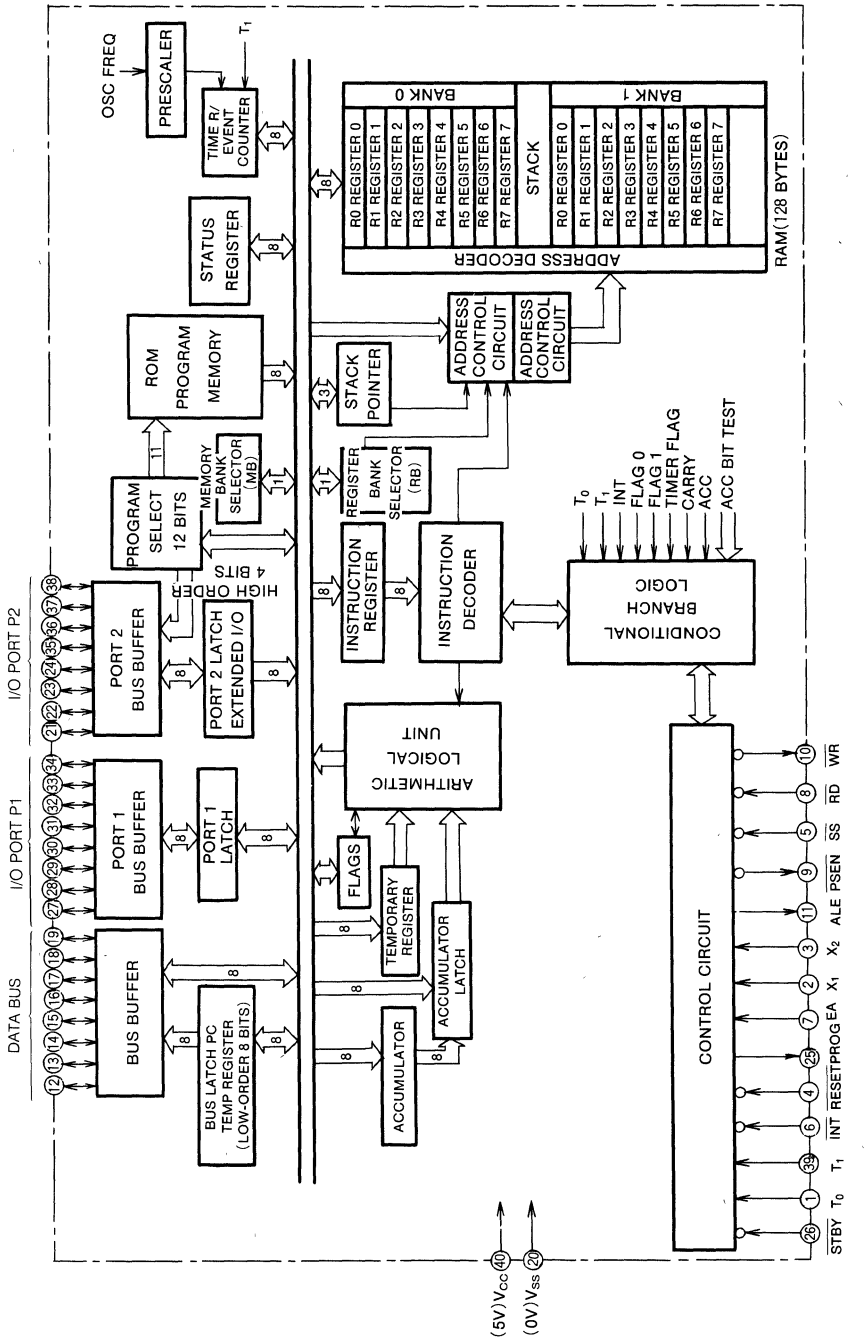


MITSUBISHI ELECTRIC

M5M80C49A-XXXP/M5M80C39AP
M5M80C49H-XXXP/M5M80C39HP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$V_{SS}-0.3\sim 7$	V
V_I	Input voltage		$V_{SS}-0.3\sim V_{CC}+0.3$	V
V_O	Output voltage		$V_{SS}-0.3\sim V_{CC}+0.3$	V
Pd	Power dissipation	T_a=25℃	1.5	W
Topr	Operating free-air temperature range		−20∼75	℃
Tstg	Storage temperature range		65∼150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Limits						Unit
		M5M80C49A-XXXP M5M80C39AP			M5M80C49H-XXXP M5M80C39HP			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0		V
V_{IH1}	High-level input voltage, except EA, $\overline{RESET}$, X_1, X_2	$0.7V_{CC}$		V_{CC}	2		V_{CC}	V
V_{IH2}	High-level input voltage, EA, $\overline{RESET}$, X_1, X_2	$0.8V_{CC}$		V_{CC}	3.8		V_{CC}	V
V_{IL1}	Low-level input voltage, except EA, $\overline{RESET}$, X_1, X_2	V_{SS}		$0.3V_{CC}$	V_{SS}		0.8	V
V_{IL2}	Low-level input voltage, EA, $\overline{RESET}$, X_1, X_2	V_{SS}		$0.2V_{CC}$	V_{SS}		0.6	V

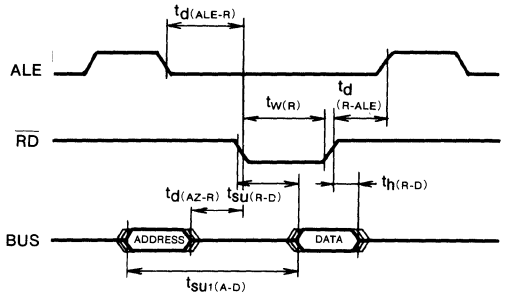
ELECTRICAL CHARACTERISTICS (T_a=−20∼75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5M80C49A-XXXP M5M80C39AP			M5M80C49H-XXXP M5M80C39HP			
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45			0.45	V
V_{OH1}	High-level output voltage, except $P1_0$∼$P1_7$, $P2_0$∼$P2_7$	I_{OH}=−400μA	$0.75V_{CC}$			2.4			V
V_{OH2}	High-level output voltage, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$	(Note 1)	$0.75V_{CC}$			2.4			V
I_I	Input current, T_1, $\overline{INT}$, $\overline{SS}$, EA, $\overline{STBY}$	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−1		1	−1		1	μA
I_{OZ}	Output current, BUS, T_0, high impedance state	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−1		1	−1		1	μA
I_{I1}	Input current during low level, Port	$V_{IL}=V_{SS}$		−40	−100		−200	−500	μA
I_{I2}	Input current during low level, $\overline{RESET}$, $\overline{SS}$	$V_{IL}=V_{SS}$		−40	−100		−40	−100	μA
I_{CC1}	Supply current	at 11MHz		5	10		5	10	mA
I_{CC2}	Supply current during HALT	at 11MHz(Note 2)		2.5	5		2.5	5	mA
I_{CC3}	Supply current during STAND BY	(Note 3)		1	10		1	10	μA
$V_{CC(STB)}$	Stand by power supply voltage		2			2			V

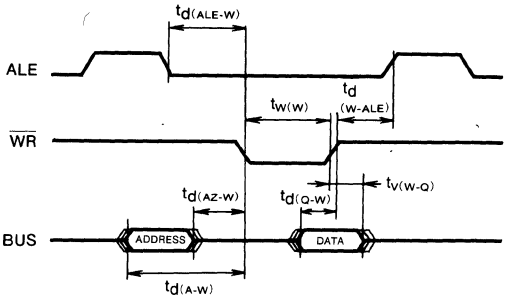
Note 1 : I_{OH}=−5μA (M5M80C49A-XXXP, M5M80C39AP)
I_{OH}=−40μA (M5M80C49H-XXXP, M5M80C49HP)
2 : BUS, T_0, T_1, EA, $\overline{INT}$=V_{CC} or V_{SS}
$\overline{SS}$, $\overline{RESET}$, $\overline{STBY}$=V_{CC}
3 : BUS, T_0, T_1, EA, $\overline{INT}$=V_{CC} or V_{SS}
$\overline{RESET}$, $\overline{STBY}$=V_{SS}
$\overline{SS}$=V_{CC}

TIMING DIAGRAM

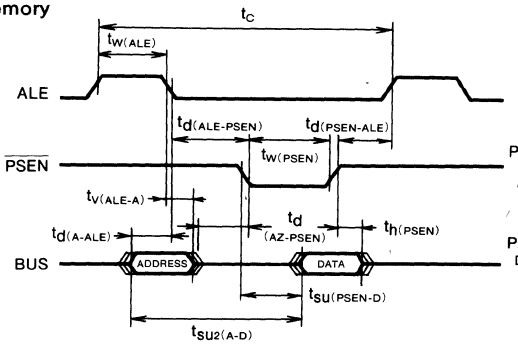
Read from Exteral Data Memory



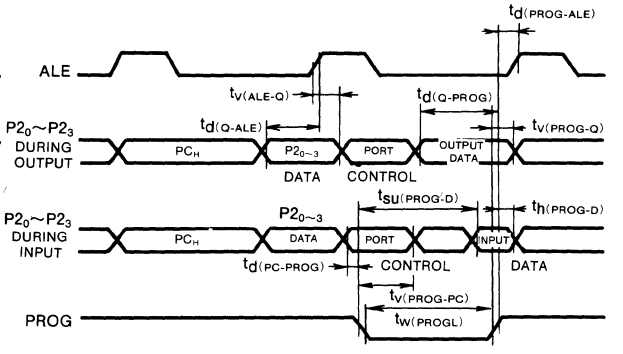
Write to External Data Memory



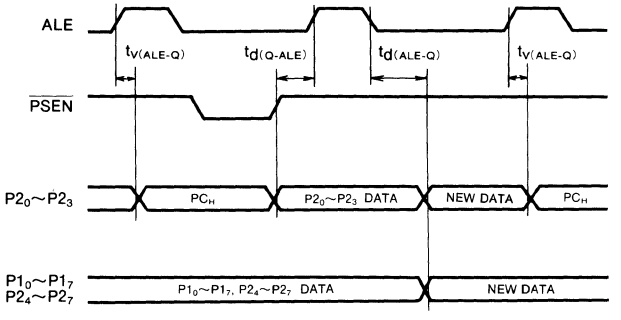
Instruction Fetch from External Program Memory



Port 2 (Expanded port)



Port 1, Port 2



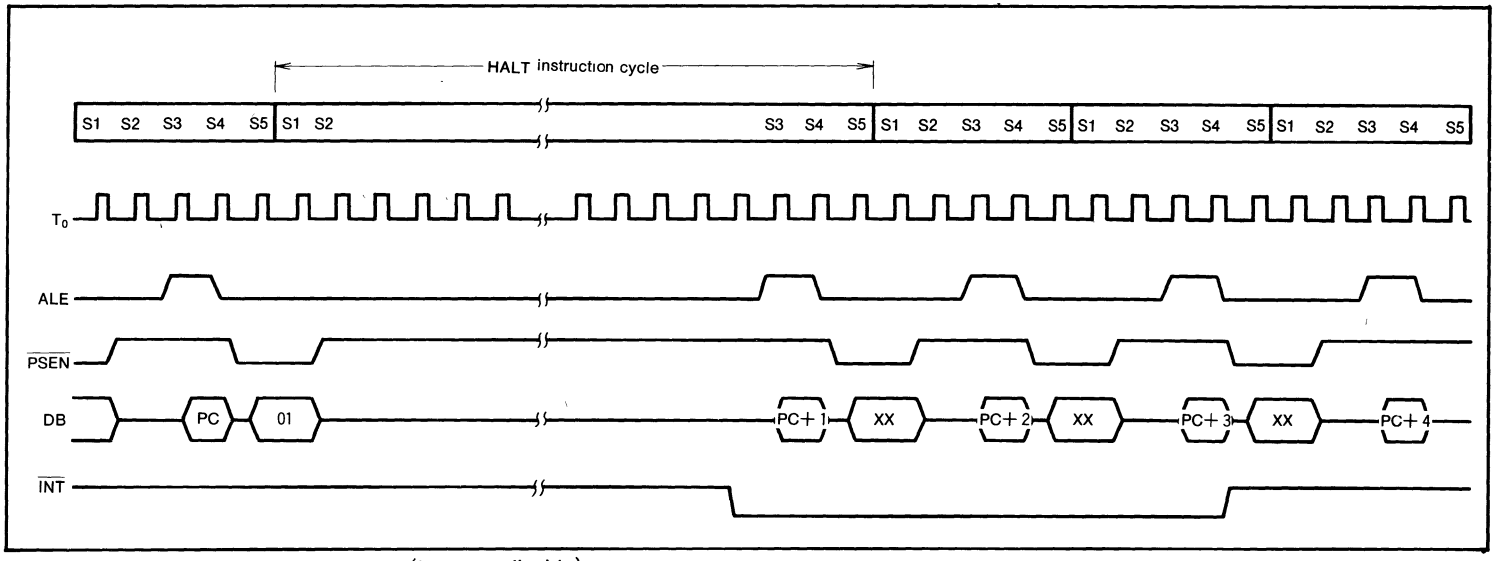


Fig.2 HALT instruction timming chart (Interrupt disable)

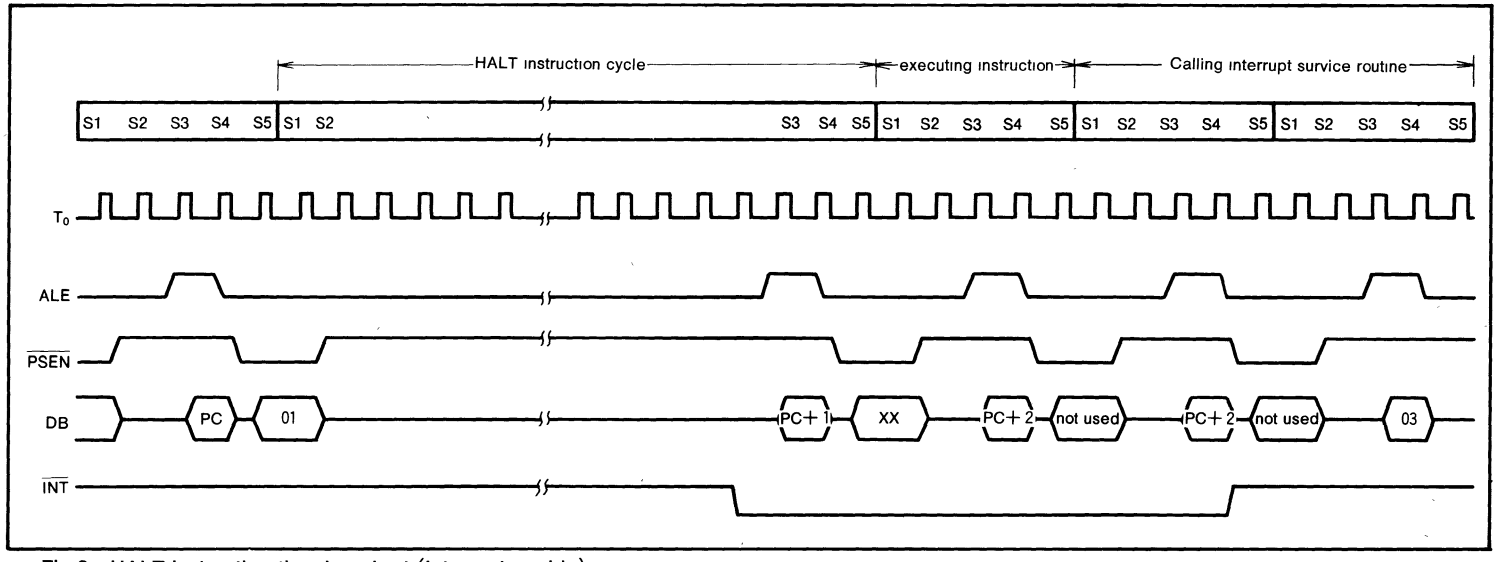


Fig.3 HALT instruction timming chert (Interrupt enable)

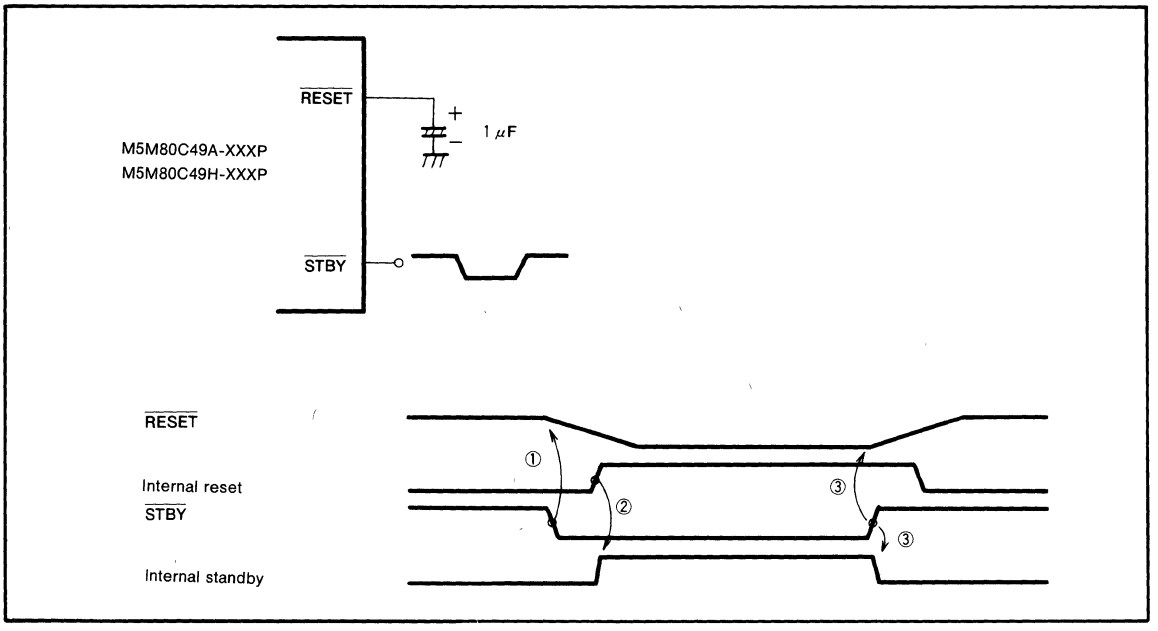


Fig.6 Control circuit example for standby mode

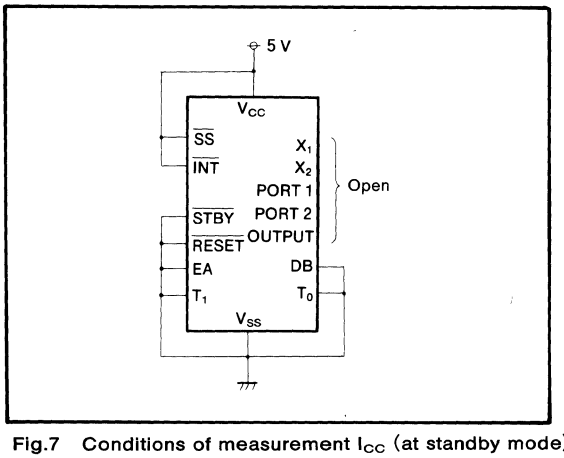
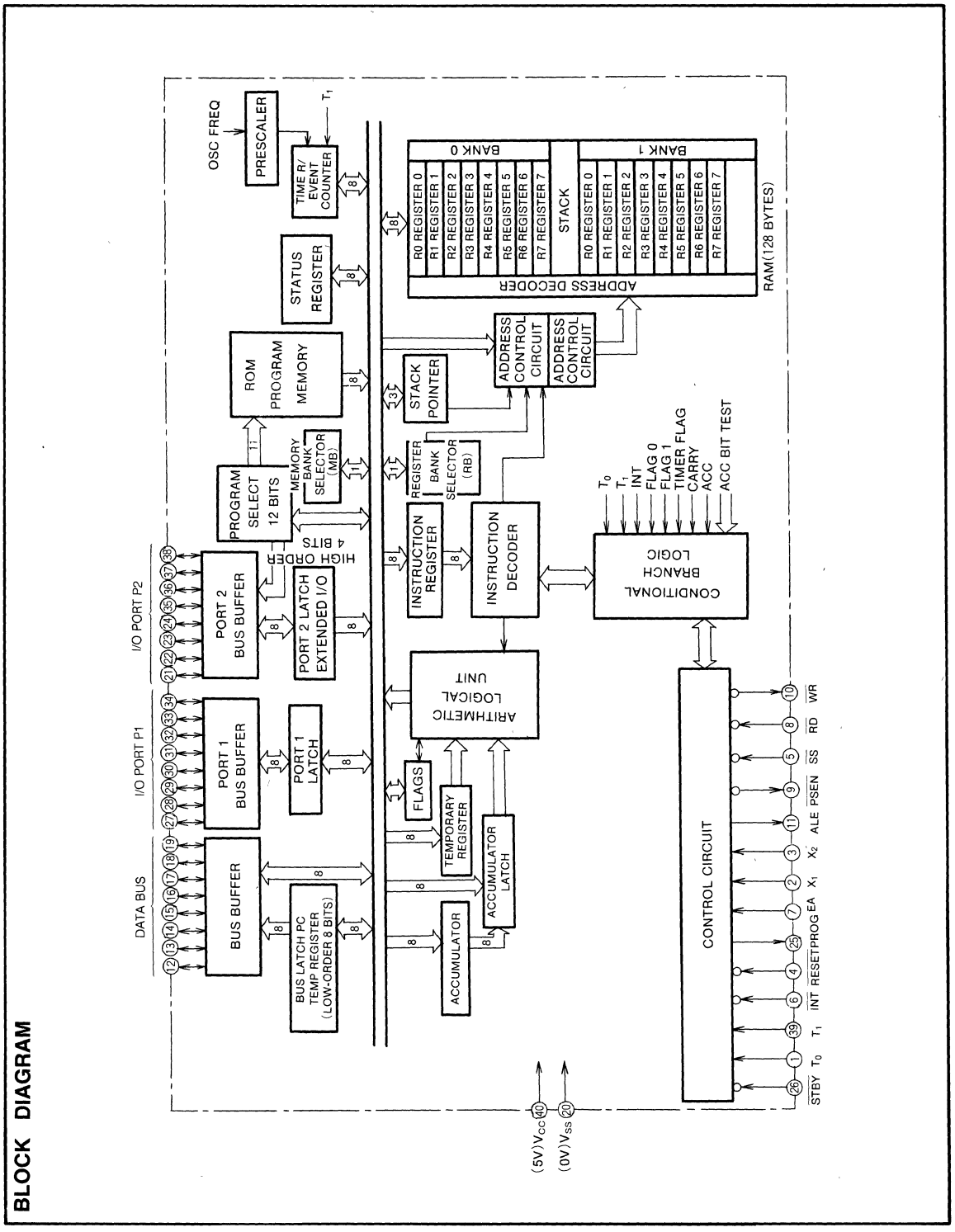


Fig.7 Conditions of measurement I_{CC} (at standby mode)

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$V_{SS}-0.3\sim 7$	V
V_I	Input voltage		$V_{SS}-0.3\sim V_{CC}+0.3$	V
V_O	Output voltage		$V_{SS}-0.3\sim V_{CC}+0.3$	V
P_d	Power dissipation	T_a=25℃	0.3	W
Topr	Operating free-air temperature range		−20∼75	℃
Tstg	Storage temperature range		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Limits						Unit
		M5MC49A-XXXFP			M5MC49H-XXXFP			
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage		0			0		V
V_{IH1}	High-level input voltage, except EA, $\overline{RESET}$, X_1, X_2	$0.7V_{CC}$		V_{CC}	2		V_{CC}	V
V_{IH2}	High-level input voltage, EA, $\overline{RESET}$, X_1, X_2	$0.8V_{CC}$		V_{CC}	3.8		V_{CC}	V
V_{IL1}	Low-level input voltage, except EA, $\overline{RESET}$, X_1, X_2	V_{SS}		$0.3V_{CC}$	V_{SS}		0.8	V
V_{IL2}	Low-level input voltage, EA, $\overline{RESET}$, X_1, X_2	V_{SS}		$0.2V_{CC}$	V_{SS}		0.6	V

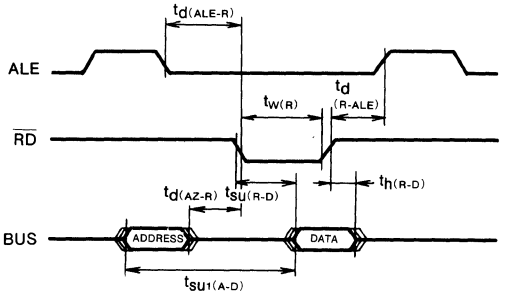
ELECTRICAL CHARACTERISTICS (T_a=−20∼75℃, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit
			M5MC49A-XXXFP			M5MC49H-XXXFP			
			Min	Typ	Max	Min	Typ	Max	
V_{OL}	Low-level output voltage	I_{OL}=2mA			0.45			0.45	V
V_{OH1}	High-level output voltage, except $P1_0\sim P1_7$, $P2_0\sim P2_7$	I_{OH}=−400μA	$0.75V_{CC}$			2.4			V
V_{OH2}	High-level output voltage, $P1_0\sim P1_7$, $P2_0\sim P2_7$	(Note 1)	$0.75V_{CC}$			2.4			V
I_I	Input current, T_1, $\overline{INT}$, $\overline{SS}$, EA, $\overline{STBY}$	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−1		1	−1		1	μA
I_{OZ}	Output current, BUS, T_0, high impedance state	$V_{SS}\leqq V_{IN}\leqq V_{CC}$	−1		1	−1		1	μA
I_{I1}	Input current during low level, Port	$V_{IL}=V_{SS}$		−40	−100		−200	−500	μA
I_{I2}	Input current during low level, $\overline{RESET}$, $\overline{SS}$	$V_{IL}=V_{SS}$		−40	−100		−40	−100	μA
I_{CC1}	Supply current	at 11MHz		5	10		5	10	mA
I_{CC2}	Supply current during HALT	at 11MHz(Note 2)		2.5	5		2.5	5	mA
I_{CC3}	Supply current during STAND BY	(Note 3)		1	10		1	10	μA
$V_{CC(STB)}$	Stand by power supply voltage		2			2			V

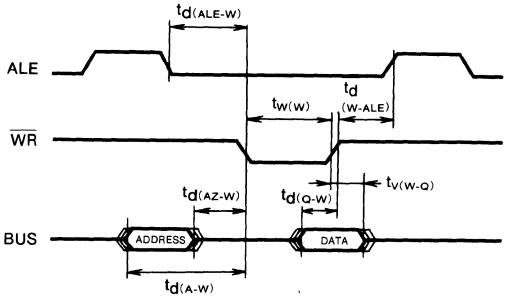
Note 1 : I_{OH}=−5μA (M5MC49A-XXXFP)
I_{OH}=−40μA (M5MC49H-XXXFP)
2 : BUS, T_0, T_1, EA, $\overline{INT}$=V_{CC} or V_{SS}
$\overline{SS}$, $\overline{RESET}$, $\overline{STBY}$=V_{CC}
3 : BUS, T_0, T_1, EA, $\overline{INT}$=V_{CC} or V_{SS}
$\overline{RESET}$, $\overline{STBY}$=V_{SS}
$\overline{SS}$=V_{CC}

TIMING DIAGRAM

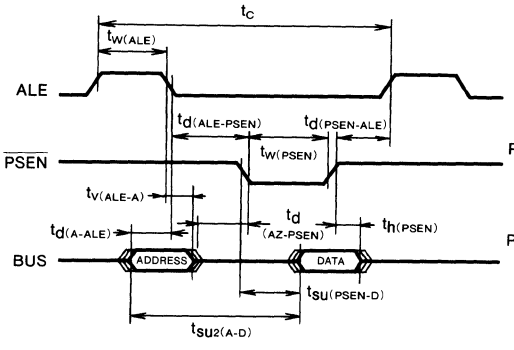
Read from Exteral Data Memory



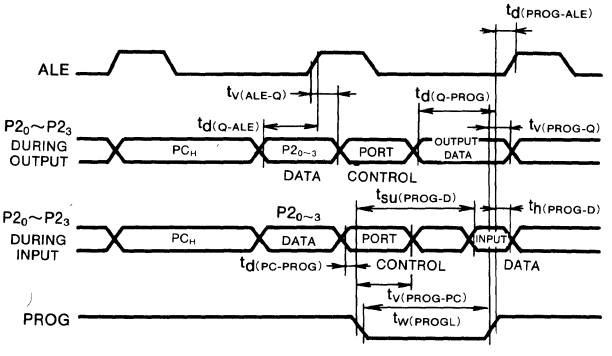
Write to External Data Memory



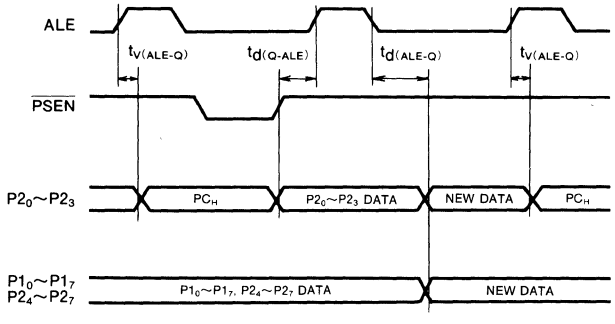
Instruction Fetch from External Program Memory



Port 2 (Expanded port)



Port 1, Port 2



MITSUBISHI ELECTRIC

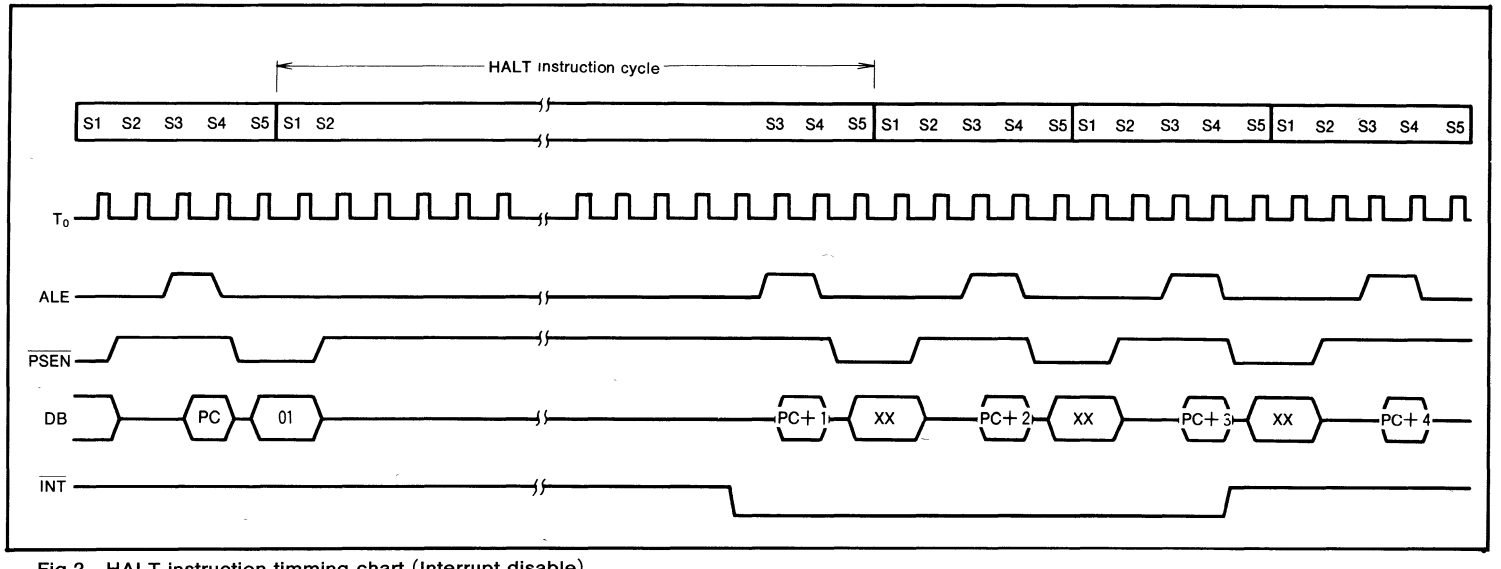


Fig.2 HALT instruction timming chart (Interrupt disable)

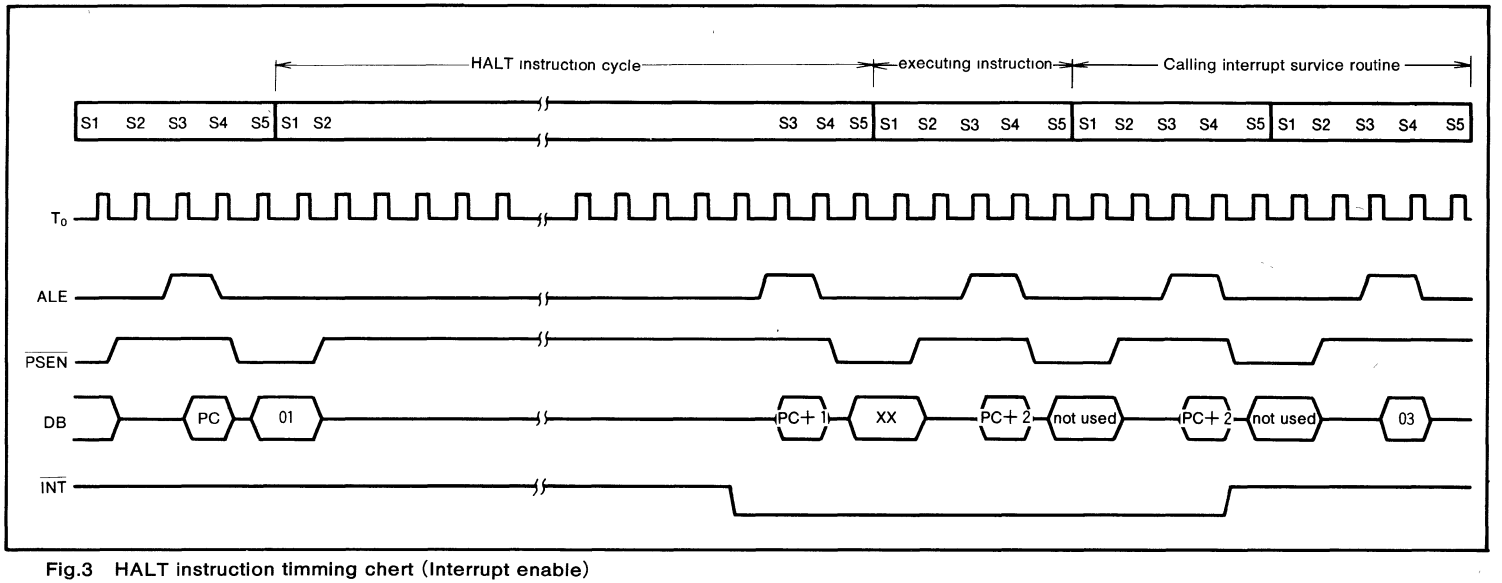


Fig.3 HALT instruction timming chert (Interrupt enable)

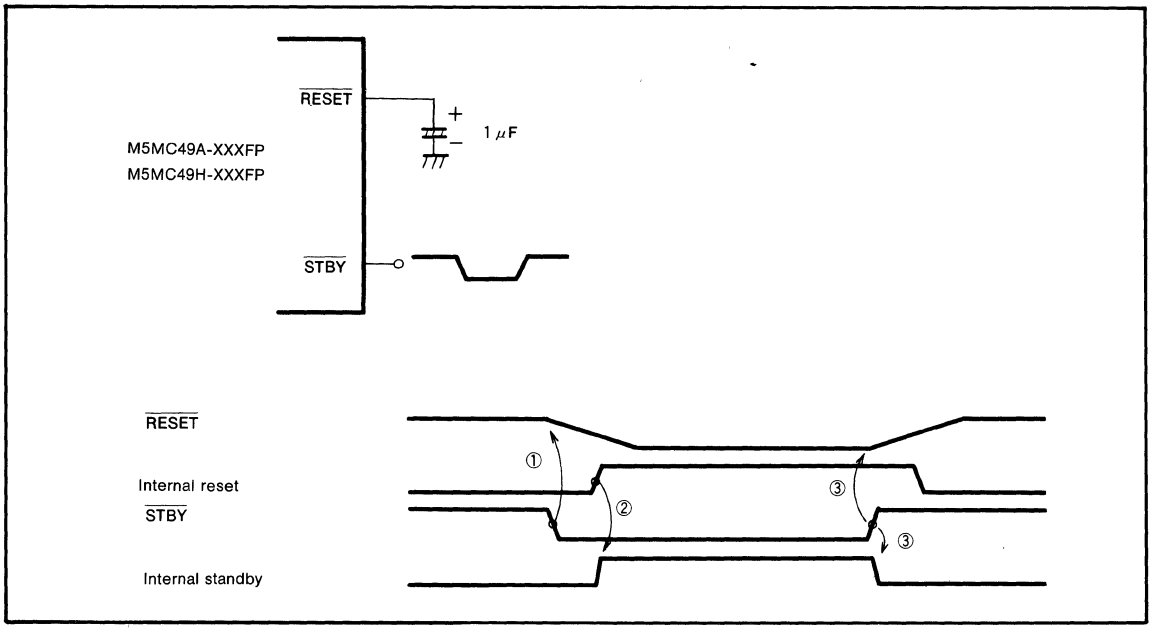


Fig.6 Control circuit example for standby mode

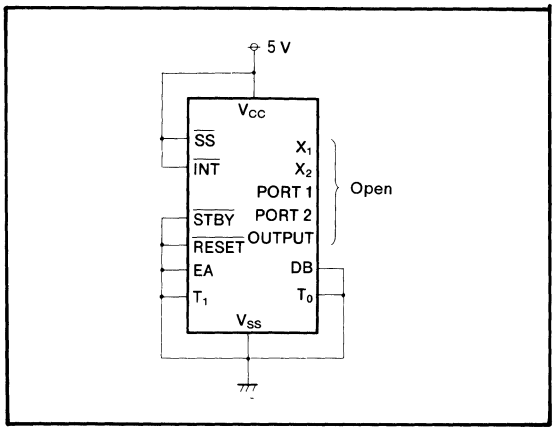


Fig.7 Conditions of measurement I_{CC} (at standby mode)

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground		Normally connected to ground (0V)
V_{CC}	Main power supply		Connected to 5V power supply
V_{DD}	Power supply		①Connected to 5V power supply ②Used for memory hold when V_{CC} is cut.
T_0	Test pin 0	Input	①Control signal from an external source for conditional jumping in a program Jumping is dependent on external conditions (JT0/JNT0)
		Output	②Used for outputting the internal clock signal (ENT0 CLK)
X_1, X_2	Crystal inputs	Input	External crystal oscillator or RC circuit input for generating internal clock signals An external clock signal can be input through X_1 or X_2
$\overline{RESET}$	Reset	Input	Control used to initialize the CPU
$\overline{SS}$	Single step	Input	Control signal used in conjunction with ALE to stop the CPU through each instruction, in the single-step mode
$\overline{INT}$	Interrupt	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JNI) ②Used for external interrupt to CPU
EA	External access	Input	①Normally maintained at 0V ②When the level is raised to 5V, external memory will be accessed even when the address is less than 400_{16} (2048) The M5L8039HLP-14 is raised to 5V
$\overline{RD}$	Read control	Output	Read control signal used when the CPU requests data from external data memory or external device to be transferred to the data bus (MOVX A, @R_r, and INS A, BUS)
$\overline{PSEN}$	Program store enable	Output	Strobe signal to fetch external program memory
$\overline{WR}$	Write control	Output	Write control signal used when the CPU sends data through the data bus to external data memory or external device. (MOVX @R_r, A and OUTL BUS, A)
ALE	Address latch enable	Output	A signal used for latching the address on the data bus. An ALE signal occurs once during each cycle
D_0~D_7	Data bus	Input/output	①Provides true bidirectional bus transfer of instructions and data between the CPU and external memory Synchronizing is done with signals $\overline{RD}$/$\overline{WR}$ The output data is latched.
			②When using external program memory, the output of the low-order 8 bits of the program counter are synchronized with ALE After that, the transfer of the instruction code or data from the external program memory is synchronized with $\overline{PSEN}$
			③The output of addresses for data using the external data memory is synchronized with ALE After that, the transfer of data with the external data memory is synchronized with $\overline{RD}$/$\overline{WR}$ (MOVX A, @R_r, and MOVX @R_r, A)
$P2_0$~$P2_7$	Port 2	Input/output	①Quasi-bidirectional port When used as an input port, FF_{16} must first be output to this port After reset, when not used as an output port, nothing needs to be output
		Output	②$P2_0$~$P2_3$ output high-order 4 bits of the program counter when using external program memory
		Input/output	③$P2_0$~$P2_3$ serve as a 4-bit I/O expander bus for the M5L8243P
PROG	Program	Output	Strobe signal for M5L8243P I/O expander
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port When used as an input port, FF_{16} must first be output to this port After reset, when not used as an output port, nothing needs to be output
T_1	Test pin 1	Input	①Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions (JT1/JNT1) ②When enabled, event signals are transferred to the timer/event counter (STRT CNT)

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = V_{DD} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Relationship to cycle time (t_C)	Alternative symbol	Limits			Unit
				Min	Typ	Max	
t	Clock cycle	$1/f_{XTAL}$	t	71.4		1000	ns
t_C	Cycle time	15t	t_{CY}	1.07		15	μs
$t_{h(PSEN-D)}$	Data hold time after $\overline{PSEN}$	1.5t − 30	t_{DR}	0		80	ns
$t_{h(R-D)}$	Data hold time after $\overline{RD}$	1.5t − 30	t_{DR}	0		80	ns
$t_{su(PSEN-D)}$	Data setup time after $\overline{PSEN}$	4.5t − 170	t_{RD2}			160	ns
$t_{su(R-D)}$	Data setup time after $\overline{RD}$	6t − 170	t_{RD1}			260	ns
$t_{su1(A-D)}$	Data setup time after address (external data memory read cycle)	10.5t − 220	t_{AD1}			530	ns
$t_{su2(A-D)}$	Data setup time after address (external program memory read cycle)	7.5t − 220	t_{AD2}			340	ns
$t_{su(PROG-D)}$	Data setup time after PROG	8.5t − 120	t_{PR}			530	ns
$t_{h(PROG-D)}$	Data hold time after PROG	1.5t	t_{PF}	0		110	ns

Note 1 : The input voltage level is V_{IL} = 0.45V and V_{IH} = 2.4V
2 : f_{XTAL} is the oscillator frequency entered at the crystal input terminals (X_1, X_2)

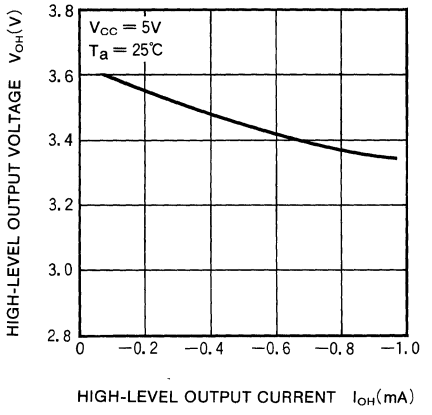
SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = V_{DD} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Relationship to cycle time (t_C)	Alternative symbol	Limits			Unit
				Min	Typ	Max	
$t_{W(ALE)}$	ALE pulse width	3.5t − 170	t_{LL}	80			ns
$t_{d(A-ALE)}$	Address to ALE signal delay time	2t − 110	t_{AL}	30			ns
$t_{v(ALE-A)}$	Address valid time after ALE	t − 40	t_{LA}	30			ns
$t_{W(PSEN)}$	$\overline{PSEN}$ pulse width	6t − 200	t_{CC2}	225			ns
$t_{W(R)}$	$\overline{RD}$ pulse width	7.5t − 200	t_{CC1}	330			ns
$t_{W(W)}$	$\overline{WR}$ pulse width	7.5t − 200	t_{CC1}	330			ns
$t_{d(Q-W)}$	Data to $\overline{WR}$ signal delay time	6.5t − 200	t_{DW}	260			ns
$t_{v(W-Q)}$	Data valid time after $\overline{WR}$	t − 50	t_{WD}	20			ns
$t_{d(A-W)}$	Address to $\overline{WR}$ signal delay time	5t − 150	t_{AW}	200			ns
$t_{d(AZ-R)}$	Address disable to $\overline{RD}$ signal delay time	2t − 40	t_{AFC1}	100			ns
$t_{d(AZ-W)}$	Address disable to $\overline{WR}$ signal delay time	2t − 40	t_{AFC1}	100			ns
$t_{d(AZ-PSEN)}$	Address disable to $\overline{PSEN}$ signal delay time	0.5t − 40	t_{AFC2}	5			ns
$t_{d(ALE-R)}$	ALE to $\overline{RD}$ signal delay time	3t − 75	t_{LAFC1}	140			ns
$t_{d(ALE-W)}$	ALE to $\overline{WR}$ signal delay time	3t − 75	t_{LAFC1}	140			ns
$t_{d(ALE-PSEN)}$	ALE to $\overline{PSEN}$ signal delay time	1.5t − 75	t_{LAFC2}	40			ns
$t_{d(R-ALE)}$	$\overline{RD}$ to ALE signal delay time	t − 65	t_{CA1}	10			ns
$t_{d(W-ALE)}$	$\overline{WR}$ to ALE signal delay time	t − 65	t_{CA1}	10			ns
$t_{d(PROG-ALE)}$	PROG to ALE signal delay time	t − 65	t_{CA1}	10			ns
$t_{d(PSEN-ALE)}$	$\overline{PSEN}$ to ALE signal delay time	4t − 70	t_{CA2}	210			ns
$t_{d(PC-PROG)}$	Port control to PROG signal delay time	1.5t − 80	t_{CP}	25			ns
$t_{v(PROG-PC)}$	Port control valid time after PROG	4t − 260	t_{PC}	25			ns
$t_{d(Q-PROG)}$	Data to PROG signal delay time	6t − 290	t_{DP}	130			ns
$t_{v(PROG-Q)}$	Data valid time after PROG	1.5t − 90	t_{PD}	15			ns
$t_{W(PROGL)}$	PROG low-level pulse width	10.5t − 250	t_{PP}	500			ns
$t_{d(Q-ALE)}$	Data to ALE signal delay time	4t − 200	t_{PL}	80			ns
$t_{v(ALE-Q)}$	Data valid time after ALE	0.5t − 30	t_{LP}	5			ns
$t_{d(ALE-Q)}$	Delay time after ALE	4.5t + 100	t_{PV}			420	ns
$t_{W(T0)}$	T_0 pulse spacing	3t	t_{OPRR}	210			ns

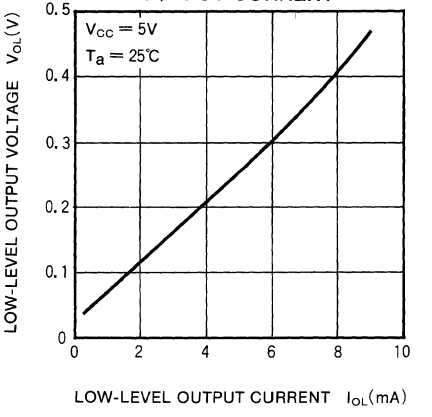
Note 3 : Conditions of measurement control output C_L = 80pF data bus output, port output C_L = 150pF
4 : Reference levels for input/output voltages are low-level = 0.8V high-level = 2V

TYPICAL CHARACTERISTICS

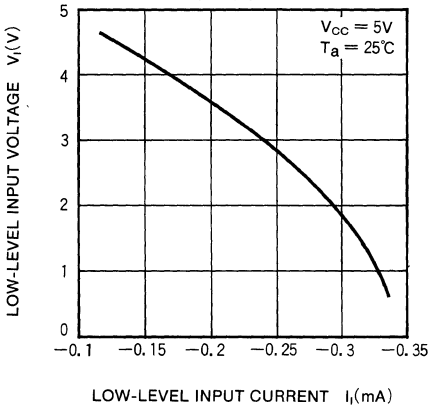
DATA BUS HIGH-LEVEL OUTPUT VOLTAGE VS. HIGH-LEVEL OUTPUT CURRENT



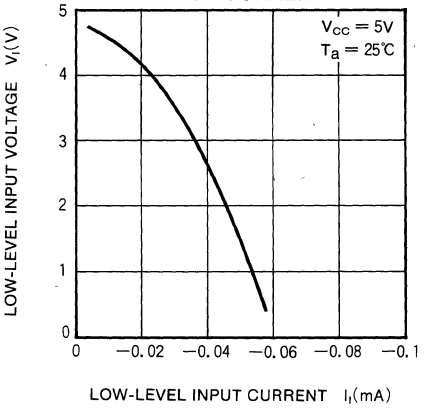
DATA BUS LOW-LEVEL OUTPUT VOLTAGE VS. LOW-LEVEL OUTPUT CURRENT



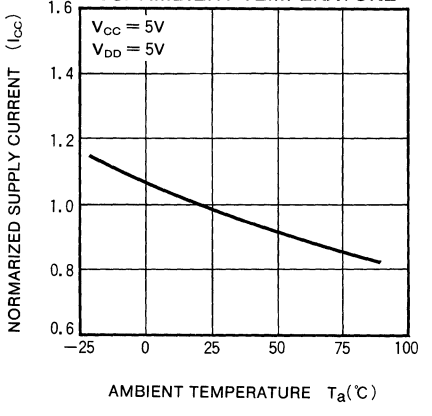
P_1, P_2 LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



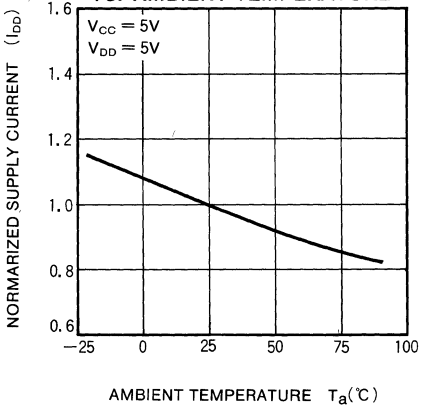
RESET LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



NORMARIZED SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE



NORMARIZED SUPPLY CURRENT (I_{DD}) VS. AMBIENT TEMPERATURE



BASIC FUNCTION BLOCKS

Program Memory (ROM)

The M5L8041A-XXXP contains a 1024-byte ROM while the M5L8042-XXXP has a built-in 2048-byte ROM. The program for the user application is stored in this ROM. Addresses 0, 3 and 7 of the ROM are reserved for special functions. Table 1 shows the meaning and functions of these special addresses.

Table 1 Reserved, defined addresses and their meanings and functions

Address	Meaning and function
0	The first instruction executed after a system reset
3	The first instruction executed after an external interrupt is accepted
7	The first instruction executed after a timer interrupt, based on the timer/event counter, is accepted.

Data Memory (RAM)

The M5L8041A-XXXP has a built-in 64-byte (128 bytes for M5L8042-XXXP) RAM. The RAM is used for data storage and manipulation and it is divided into sections for more efficient processing. Addresses 0～7 and 24～31 form two banks of general-purpose registers that can be directly addressed. Addresses 0～7 compose bank 0 and are numbered R_0～R_7. Addresses 24～31 compose bank 1 and are also numbered R_0～R_7. Only one bank is active at a time. The instructions SEL RB0 and SEL RB1 are used to select the working bank. Fig. 1 shows the division of the RAM and its mapping. The remaining sections, addresses 32 and above, must be accessed indirectly using the general-purpose registers R_0 or R_1. Of course, all addresses can be indirectly accessed using the general-purpose registers R_0 and R_1.

A good practice to simplify programming is to reserve general-purpose register bank 0 for use of the main program and register bank 1 for interrupt programs. For example, if register bank 0 (addresses 0～7) is reserved for processing data by the main program, when an interrupt is accepted, the first instruction would be to switch the working registers from bank 0 to bank 1. This saves the data of the main program (addresses 0～7). The interrupt program can then freely use register bank 1 (addresses 24～31) without destroying or altering data of the main program. When the interrupt processing is complete and control is returned to the main program by the RETR instruction, register bank 0 (in this example) is automatically restored as the working register bank at the same time the main program counter is restored.

Addresses 8～23 comprise an 8-level program counter stack. More information on using the stack is found in the section on the program counter and stack and so reference should be made here for further details.

The general-purpose registers and program counter stack sections may be used in exactly the same way as the other RAM sections.

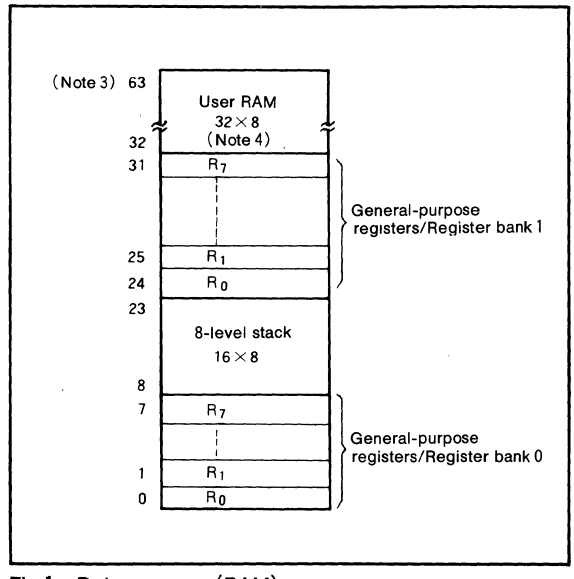


Fig.1 Data memory (RAM)

Note 3 : The corresponding address is 127 for the **M5L8042-XXXP**
4 : The corresponding capacity is 96 × 8 for the **M5L8042-XXXP**

Program Status Word (PSW)

The PSW (program status word) is stored in 8 bits in the register storage. The configuration is shown in Fig. 4. The high-order 4 bits of the PSW are stored in the stack, along with the PC, when an interrupt is accepted or a subroutine call executed. When control is returned to the main program by RETR, both the PC and the high-order 4 bits of PSW are restored. When control is returned by RET, only the PC is restored, so care must be taken to ensure that the contents of the PSW are not unintentionally changed.

The order and meaning of the 8 PSW bits are given below.

Bit 0~Bit 2 : Stack pointer (S_0, S_1, S_2)

Bit 3 : Not used

Bit 4 : Working register bank indicator
0 = Bank 0
1 = Bank 1

Bit 5 : Flag 0 (value is set by user and can be tested with JFO conditional jump instruction.)

Bit 6 : Auxiliary carry bit (AC). It is set/reset by the ADD and ADDC instructions and used by the DAA decimal compensation instruction.

Bit 7 : Carry bit (CY). This indicates an overflow after an arithmetic or logic operation.

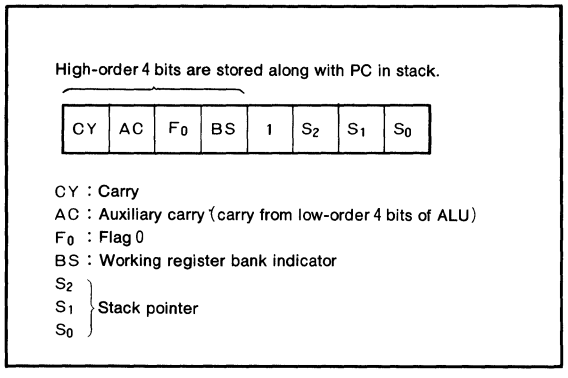


Fig.4 Program status word

I/O Ports

The Series MELPS 8-41 has two 8-bit ports, called port 1 and port 2.

(1) Port 1 and port 2

Ports 1 and 2 are both 8-bit ports with identical properties. The output data of these ports are retained and do not change until another output is loaded into them. When used as inputs, the input data is not retained so the input signals must be maintained until an input instruction is executed and completed.

Ports 1 and 2 are so-called quasi-bidirectional ports which have a special circuit configuration to accomplish this purpose. All the pins of the ports can be used for input or for output.

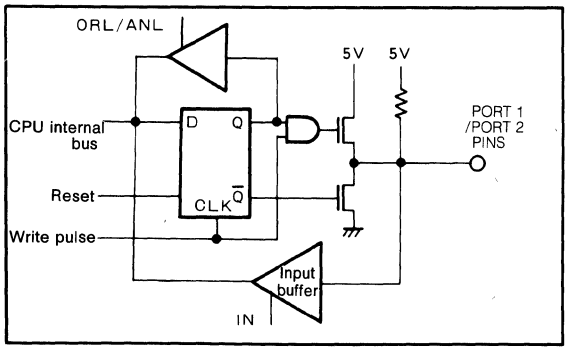


Fig.5 I/O port 1 and 2 circuit

The special circuit is shown in Fig. 5. Internal on-chip pull-up resistors are provided for all the ports for pull-up to 5V. The current required for setting the TTL signal high can be supplied through these pull-up resistors. In addition, the level can be pulled low by the standard TTL output. This means that any pin can be used for both input and output.

To shorten the switching time from a low level to high level, when 1's are output, a device with a relatively low impedance is turned on for a short time (approx. 500ns when a 6MHz crystal oscillator is used).

To use a particular port pin as an input, a logic "1" must first be written to that pin. After resetting, a port is set to an input port and remains in this state.

Therefore, it is not necessary to output all 1's if it is to be used for input. In short, a port being used for output must output 1's before it can be used for input.

F_1 (flag 1)

When the data or command is input into the input data/command bus buffer by the master CPU, the F_1 flag is set to the condition of the A_0 input.

The F_1 flag is also set by the flag setting instructions (CPL F_1, CLR F_1).

- Output Data Bus Buffer Register

The accumulator (A) contents are transferred to the DBB (0) output data bus buffer register by the OUT DBB, A instruction. Since the OBF flag is set at this time, the master CPU can judge whether the data has been transferred to the register by confirming the state of the OBF flag.

- Input Data/Command Bus Buffer (DBB(1)) Register

When the write request ($\overline{W}$ =0) is generated from the master CPU, the data on the data bus is transferred to the DBB (1) input data/command bus buffer register. Since the IBF flag is set at this time, it is possible to judge whether the data or command has been transferred inside the Series MELPS 8-41 by confirming the state of this flag.

Conditional Jumps Using Pins T_0, T_1 and Flags IBF, OBF

The conditional jump instructions are used to alter programs, depending on the internal and external conditions (states) of the CPU. Details of the jump instructions can be found in the section on machine instructions.

The input signal status of pins T_0 and T_1, and the states of the IBF and OBF flags can be checked by the conditional jump instructions. These input pins, through conditional jump instructions such as JTO and JNTO, can be used to control a program. This means that programs and processing time can be reduced by being able to test data in the input pin rather than reading the data into a accumulator and then testing it.

Pin T_1 has other functions and uses which are not related to conditional jump instructions. Details of these other functions and uses can be found on the section dealing with pin functions.

Interrupt

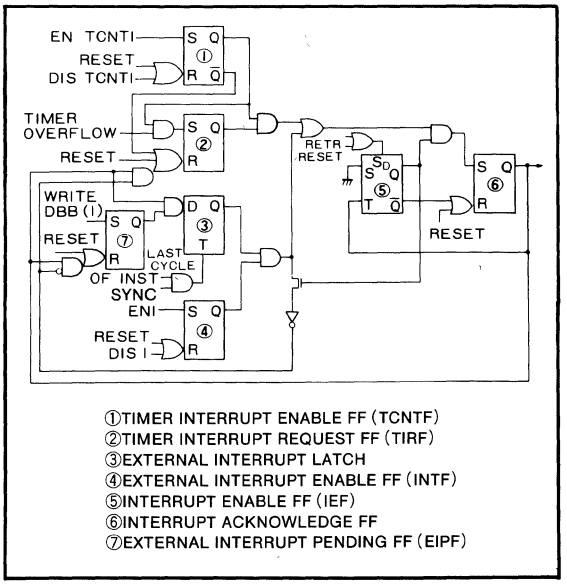
The CPU recognizes an external interrupt by a low-level signal at the $\overline{S}$ and $\overline{W}$ pins. When such an interrupt is accepted, the external interrupt pending flip-flop and IBF flag are set.

Interrupt requests are sampled between the SYNC signal outputs of every machine cycle. When a request is recognized, then as soon as the instruction being executed is terminated, a subroutine call is made to address 3 of the program memory. As with ordinary subroutine calls, the program counter and program status word (PSW) are saved in the program counter stack.

The unconditional jump instructions for enabling a jump to be made to the address where the ordinary interrupt processing program is stored are contained in address 3 of the program memory.

The interrupt level is one so that the next interrupt cannot be accepted until the current interrupt processing has been completed. The RETR instruction terminates the interrupt processing. That is to say, the next interrupt cannot be accepted until the RETR instruction is executed. The next interrupt can be accepted at the start of the second cycle of the RETR instruction (2-cycle instruction). Timer/event counter overflow which causes an interrupt request will also not be accepted.

Priority is given to the external interrupt when both an external interrupt and timer interrupt have been generated at the same time.



①TIMER INTERRUPT ENABLE FF (TCNTF)
②TIMER INTERRUPT REQUEST FF (TIRF)
③EXTERNAL INTERRUPT LATCH
④EXTERNAL INTERRUPT ENABLE FF (INTF)
⑤INTERRUPT ENABLE FF (IEF)
⑥INTERRUPT ACKNOWLEDGE FF
⑦EXTERNAL INTERRUPT PENDING FF (EIPF)

Fig.8 Interrupt control section configuration

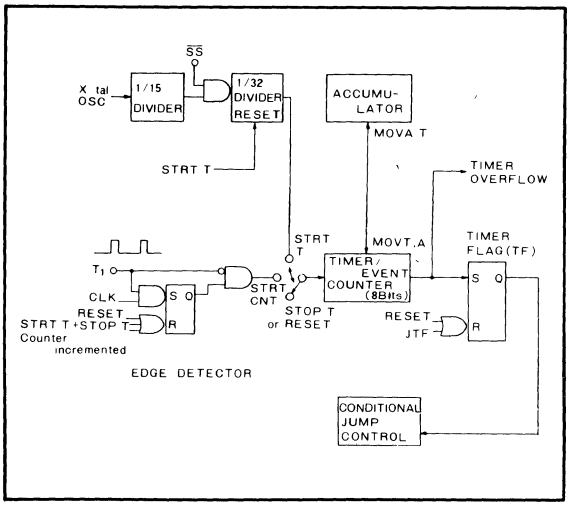


Fig.9 Timer/event counter configuration

Cycle Timing

The output of the state counter is $\frac{1}{3}$ the input frequency from the oscillator, and a CLK signal is produced which determines the times of each machine state (see Fig. 10). During the cycle count the CLK signal is prescaled by $\frac{1}{5}$ and a machine cycle containing 5 states is produced. The Series MELPS 8-41 instructions are executed in one or two machine cycles. Fig. 12 shows the internal operation with an instruction formed from one machine cycle.

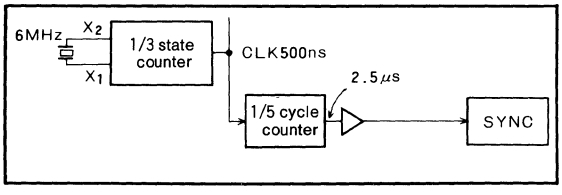


Fig.10 Clock generator circuit

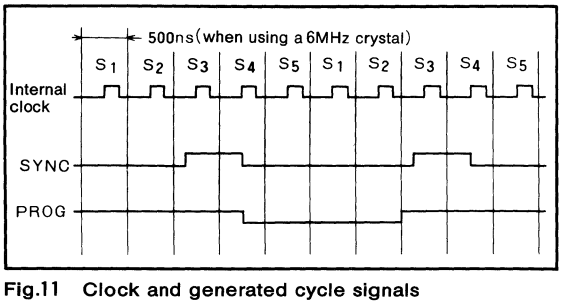


Fig.11 Clock and generated cycle signals

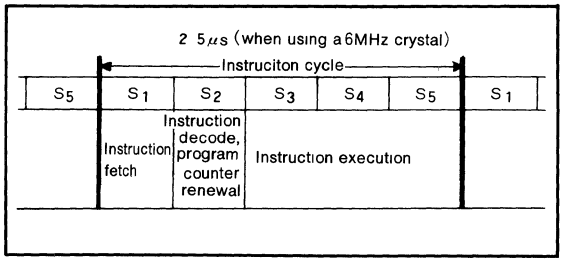


Fig.12 Instruction execution timing

Reset

The $\overline{\text{RESET}}$ pin is for resetting the CPU. A Schmitt trigger circuit along with a pull-up resistor are connected to it on the chip. A sufficiently long pulse can be obtained for resetting by attaching 1μF capacitor as shown in Fig. 13. An external reset pulse applied at $\overline{\text{RESET}}$ must remain at the low level for at least 10ms after the power has been turned on and after it has reached its normal level.

The reset function causes the following initialization within the CPU.

(1) The program counter is reset to 0.
(2) The stack pointer is reset to 0.
(3) The register bank 0 is selected.
(4) Ports 1 and 2 are reset to the input mode.
(5) External and timer interrupts are reset to disable state.
(6) Timer is stopped.
(7) Timer flag is cleared.
(8) Flags F_0 and F_1 are cleared.

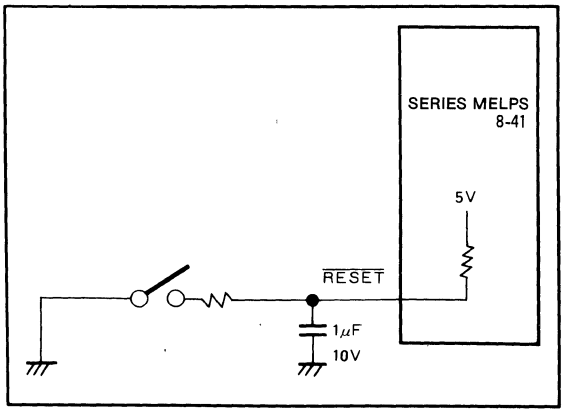


Fig.13 Example of reset circuit

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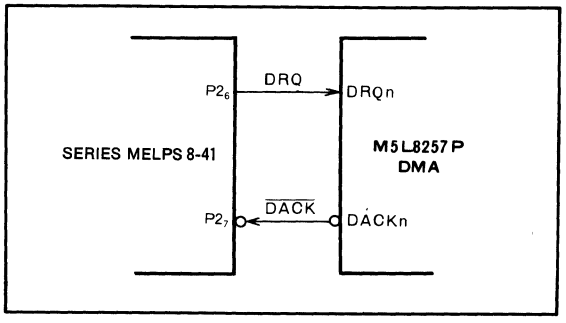

Fig.16 DMA control

When the EN DMA instruction is executed, $P2_6$ becomes the DRQ (DMA request) output. Subsequently, when $P2_6$ is set to "1", DRQ becomes "1" and DMA-based data transfer is requested.
DRQ is cleared when the $\overline{DACK} \cdot \overline{R}$, $\overline{DACK} \cdot \overline{W}$ or EN DMA instruction is executed.

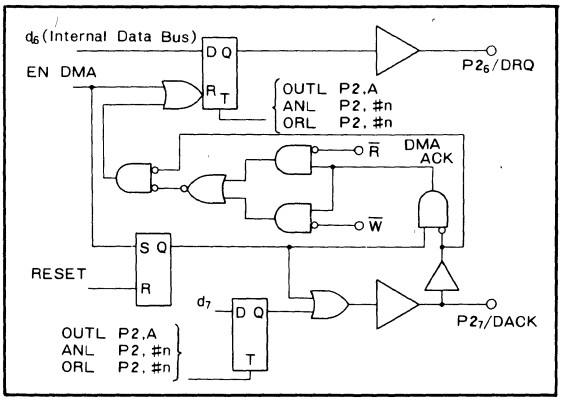

Fig.17 Internal configuration of DMA control

When the EN DMA instruction is executed, $P2_7$ becomes the $\overline{DACK}$ (DMA acknowledge) input. The $\overline{DACK}$ input is used as the chip select input for DMA transfer. There is, therefore, no connection with the state of $\overline{S}$ (chip select) during DMA transfer.

Interrupt Request to Master CPU

Ports $P2_4$ and $P2_5$ of Series MELPS 8-41 can be used not only as ordinary input/output ports but also as the outputs of the $\overline{IBF}$ (input buffer full) flag and OBF (output buffer full) flag. Immediately after resetting, both ports function as input ports.

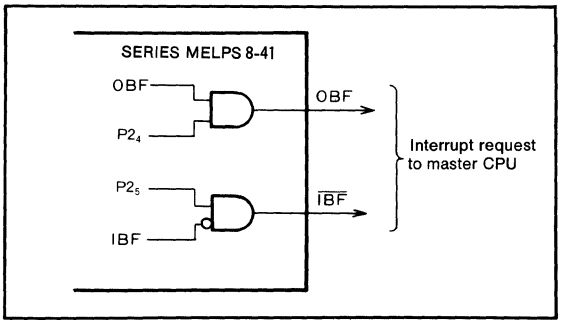

Fig.18 Interrupt request to master CPU

When the EN FLAGS instruction is executed, $P2_4$ functions as the OBF pin and $P2_5$ as the $\overline{IBF}$ pin. "1" must be output to both pins so that the OBF and $\overline{IBF}$ flag states are output to each pin, respectively. These states are not output while "0" is output to the pins. The OBF flag output indicates that data has been output to the output data bus buffer register; the $\overline{IBF}$ flag output indicates that the input data/command bus buffer register is in the data accept enable mode.

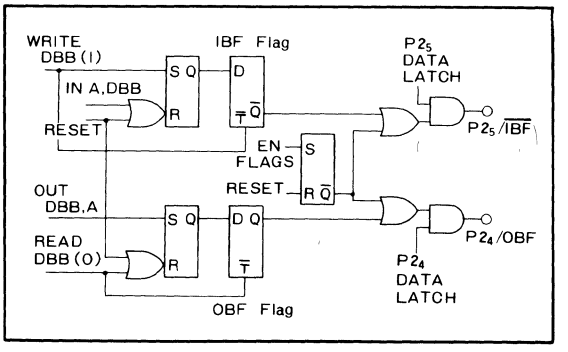

Fig.19 Internal configuration of IBF/OBF

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FUNCTIONS OF SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

MACHINE INSTRUCTIONS

Item / Type	Mnemonic	Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Instruction code Hexadecimal	Bytes	Cycles	Function
Transfer	MOV A, #n	0 0 1 0 $n_7n_6n_5n_4$	0 0 1 1 $n_3n_2n_1n_0$	2 3 n	2	2	(A) ← n
	MOV A, PSW	1 1 0 0	0 1 1 1	C 7	1	1	(A) ← (PSW)
	MOV A, Rr	1 1 1 1	1 $r_2r_1r_0$	F 8 + r	1	1	(A) ← (Rr) r = 0 ~ 7
	MOV A, @Rr	1 1 1 1	0 0 0 r_0	F 0 + r	1	1	(A) ← (M (Rr)) r = 0 ~ 1
	MOV PSW, A	1 1 0 1	0 1 1 1	D 7	1	1	(PSW) ← (A) (C) ← (A_7), (AC) ← (A_6)
	MOV STS, A	1 0 0 1	0 0 0 0	9 0	1	1	(STS) ← (A) (ST_4 ~ ST_7) ← (A_4 ~ A_7)
	MOV Rr, A	1 0 1 0	1 $r_2r_1r_0$	A 8 + r	1	1	(Rr) ← (A) r = 0 ~ 7
	MOV Rr, #n	1 0 1 1 $n_7n_6n_5n_4$	1 $r_2r_1r_0$ $n_3n_2n_1n_0$	B 8 + r n	2	2	(Rr) ← n r = 0 ~ 7
	MOV @Rr, A	1 0 1 0	0 0 0 r_0	A 0 + r	1	1	(M (Rr)) ← (A) r = 0 ~ 1
	MOV @Rr, #n	1 0 1 1 $n_7n_6n_5n_4$	0 0 0 r_0 $n_3n_2n_1n_0$	B 0 + r n	2	2	(M (Rr)) ← n r = 0 ~ 1
	MOVP A, @A	1 0 1 0	0 0 1 1	A 3	1	2	(A) ← (M (A))
	MOVP3 A, @A	1 1 1 0	0 0 1 1	E 3	1	2	(A) ← (M (page 3, A))
	XCH A, Rr	0 0 1 0	1 $r_2r_1r_0$	2 8 + r	1	1	(A) ⟷ (Rr) r = 0 ~ 7
	XCH A, @Rr	0 0 1 0	0 0 0 r_0	2 0 + r	1	1	(A) ⟷ (M (Rr)) r = 0 ~ 1
	XCHD A, @Rr	0 0 1 1	0 0 0 r_0	3 0 + r	1	1	(A_0 ~ A_3) ⟷ (M (Rr_0 ~ Rr_3)) r = 0 ~ 1
Arithmetic	ADD A, #n	0 0 0 0 $n_7n_6n_5n_4$	0 0 1 1 $n_3n_2n_1n_0$	0 3 n	2	2	(A) ← (A) + n
	ADD A, Rr	0 1 1 0	1 $r_2r_1r_0$	6 8 + r	1	1	(A) ← (A) + (Rr) r = 0 ~ 7
	ADD A, @Rr	0 1 1 0	0 0 0 r_0	6 0 + r	1	1	(A) ← (A) + (M (Rr)) r = 0 ~ 1
	ADDC A, #n	0 0 0 1 $n_7n_6n_5n_4$	0 0 1 1 $n_3n_2n_1n_0$	1 3 n	2	2	(A) ← (A) + n + (C)

FUNCTIONS OF SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

Item / Type	Mnemonic	Instruction code $D_7D_6D_5D_4$	Instruction code $D_3D_2D_1D_0$	Instruction code Hexadecimal	Bytes	Cycles	Function
Arithmetic	ADDC A, Rr	0 1 1 1	1 r_2 r_1 r_0	7 8+r	1	1	(A) ← (A) + (Rr) + (C) r = 0 ~ 7
	ADDC A, @Rr	0 1 1 1	0 0 0 r_0	7 0+r	1	1	(A) ← (A) + (M (Rr)) + (C) r = 0 ~ 1
	ANL A, #n	0 1 0 1 n_7 n_6 n_5 n_4	0 0 1 1 n_3 n_2 n_1 n_0	5 3 n	2	2	(A) ← (A) ∧ n
	ANL A, Rr	0 1 0 1	1 r_2 r_1 r_0	5 8+r	1	1	(A) ← (A) ∧ (Rr) r = 0 ~ 7
	ANL A, @Rr	0 1 0 1	0 0 0 r_0	5 0+r	1	1	(A) ← (A) ∧ (M (Rr)) r = 0 ~ 1
	ORL A, # n	0 1 0 0 n_7 n_6 n_5 n_4	0 0 1 1 n_3 n_2 n_1 n_0	4 3 n	2	2	(A) ← (A) ∨ n
	ORL A, Rr	0 1 0 0	1 r_2 r_1 r_0	4 8+r	1	1	(A) ← (A) ∨ (Rr) r = 0 ~ 7
	ORL A, @Rr	0 1 0 0	0 0 0 r_0	4 0+r	1	1	(A) ← (A) ∨ (M (Rr)) r = 0 ~ 1
	XRL A, # n	1 1 0 1 n_7 n_6 n_5 n_4	0 0 1 1 n_3 n_2 n_1 n_0	D 3 n	2	2	(A) ← (A) ∀ n
	XRL A, Rr	1 1 0 1	1 r_2 r_1 r_0	D 8+r	1	1	(A) ← (A) ∀ (Rr) r = 1 ~ 7
	XRL A, @Rr	1 1 0 1	0 0 0 r_0	D 0+r	1	1	(A) ← (A) ∀ (M (Rr)) r = 0 ~ 1
	INC A	0 0 0 1	0 1 1 1	1 7	1	1	(A) ← (A) + 1
	DEC A	0 0 0 0	0 1 1 1	0 7	1	1	(A) ← (A) − 1
	CLR A	0 0 1 0	0 1 1 1	2 7	1	1	(A) ← 0
	CPL A	0 0 1 1	0 1 1 1	3 7	1	1	(A) ← $\overline{(A)}$
	DA A	0 1 0 1	0 1 1 1	5 7	1	1	(A) ← (A) Decimal Conversion
	SWAP A	0 1 0 0	0 1 1 1	4 7	1	1	(A_4 ~ A_7) ⟷ (A_0 ~ A_3)
	RL A	1 1 1 0	0 1 1 1	E 7	1	1	(A_{n+1}) ← (A_n) (A_0) ← (A_7) n = 0 ~ 6
	RLC A	1 1 1 1	0 1 1 1	F 7	1	1	(A_{n+1}) ← (A_n) (A_0) ← (C) (C) ← (A_7) n = 0 ~ 6

SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

FUNCTIONS OF SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

Item / Type	Mnemonic	Instruction code			Bytes	Cycles	Function
		$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexadecimal			
Arithmetic	RR A	0 1 1 1	0 1 1 1	7 7	1	1	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (A_0)$ n= 0 ~ 6
	RRC A	0 1 1 0	0 1 1 1	6 7	1	1	$(A_n) \leftarrow (A_{n+1})$ $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$ n= 0 ~ 6
Register arithmetic	INC Rr	0 0 0 1	1 r_2 r_1 r_0	1 8 + r	1	1	(Rr) ← (Rr)+ 1 r= 0 ~ 7
	INC @Rr	0 0 0 1	0 0 0 r_0	1 0 + r	1	1	(M(Rr)) ← (M(Rr))+ 1 r= 0 ~ 1
	DEC Rr	1 1 0 0	1 r_2 r_1 r_0	C 8 + r	1	1	(Rr) ← (Rr)− 1 r= 0 ~ 7
Jump	JBb m	b_7 b_6 b_5 1 m_7 m_6 m_5 m_4	0 0 1 0 m_3 m_2 m_1 m_0	1 2 + b m	2	2	When (A_b)= 1 , $(PC_0 \sim PC_7) \leftarrow$ m When (A_b)= 0 , (PC) ← (PC)+ 2 $b_7b_6b_5$= 0 ~ 7
	JNIBF m	1 1 0 1 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	D 6	2	2	When (IBF)= 0 , $(PC_0 - PC_7) \leftarrow$ m
	JOBF m	1 0 0 0 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	8 6 m	2	2	When (OBF)= 1 , $(PC_0 - PC_7) \leftarrow$ m
	JTF m	0 0 0 1 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	1 6 m	2	2	When (TF)= 1 , $(PC_0 \sim PC_7) \leftarrow$ m When (TF)= 0 , (PC) ← (PC)+ 2
	JMP m	m_{10} m_9 m_8 0 m_7 m_6 m_5 m_4	0 1 0 0 m_3 m_2 m_1 m_0	0 4 + $m_{8\sim10}$ m	2	2	$(PC_8 \sim PC_{10}) \leftarrow m_8 \sim m_{10}$ $(PC_0 \sim PC_7) \leftarrow m_0 \sim m_7$
	JMPP @A	1 0 1 1	0 0 1 1	B 3	1	2	$(PC_0 - PC_7) \leftarrow (M(A))$
	DJNZ Rr, m	1 1 1 0 m_7 m_6 m_5 m_4	1 r_2 r_1 r_0 m_3 m_2 m_1 m_0	E 8 + r m	2	2	(Rr) ← (Rr)− 1 r= 0 ~ 7 When (Rr)≠ 0 , $(PC_0 \sim PC_7) \leftarrow$ m When (Rr)= 0 , (PC) ← (PC)+ 2
	JC m	1 1 1 1 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	F 6 m	2	2	When (C)= 1 , $(PC_0 \sim PC_7) \leftarrow$ m When (C)= 0 , (PC) ← (PC)+ 2
	JNC m	1 1 1 0 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	E 6 m	2	2	When (C)= 0 , $(PC_0 \sim PC_7) \leftarrow$ m When (C)= 1 , (PC) ← (PC)+ 2
	JZ m	1 1 0 0 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	C 6 m	2	2	When (A)= 0 , $(PC_0 \sim PC_7) \leftarrow$ m When (A)≠ 0 , (PC) ← (PC)+ 2
	JNZ m	1 0 0 1 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	9 6 m	2	2	When (A)≠ 0 , $(PC_0 \sim PC_7) \leftarrow$ m When (A)= 0 , (PC) ← (PC)+ 2
	JT0 m	0 0 1 1 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	3 6 m	2	2	When (T_0)= 1 , $(PC_0 \sim PC_7) \leftarrow$ m When (T_0)= 0 , (PC) ← (PC)+ 2
	JNT0 m	0 0 1 0 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	2 6 m	2	2	When (T_0)= 0 , $(PC_0 \sim PC_7) \leftarrow$ m When (T_0)= 1 , (PC) ← (PC)+ 2
	JT1 m	0 1 0 1 m_7 m_6 m_5 m_4	0 1 1 0 m_3 m_2 m_1 m_0	5 6 m	2	2	When (T_1)= 1 , $(PC_0 \sim PC_7) \leftarrow$ m When (T_1)= 0 , (PC) ← (PC)+ 2

FUNCTIONS OF SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

Item / Type	Mnemonic	Instruction code			Bytes	Cycles	Function
		$D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexadecimal			
Jump	JNT1 m	0 1 0 0 $m_7m_6m_5m_4$	0 1 1 0 $m_3m_2m_1m_0$	4 6 m	2	2	When $(T_1)=0$, $(PC_0 \sim PC_7) \leftarrow m$ When $(T_1)=1$, $(PC) \leftarrow (PC)+2$
	JF0 m	1 0 1 1 $m_7m_6m_5m_4$	0 1 1 0 $m_3m_2m_1m_0$	B 6 m	2	2	When $(F_0)=1$, $(PC_0 \sim PC_7) \leftarrow m$ When $(F_0)=0$, $(PC) \leftarrow (PC)+2$
	JF1 m	0 1 1 1 $m_7m_6m_5m_4$	0 1 1 0 $m_3m_2m_1m_0$	7 6 m	2	2	When $(F_1)=1$, $(PC_0 \sim PC_7) \leftarrow m$ When $(F_1)=0$, $(PC) \leftarrow (PC)+2$
Status Control	CLR C	1 0 0 1	0 1 1 1	9 7	1	1	$(C) \leftarrow 0$
	CPL C	1 0 1 0	0 1 1 1	A 7	1	1	$(C) \leftarrow (\overline{C})$
	CLR F_0	1 0 0 0	0 1 0 1	8 5	1	1	$(F_0) \leftarrow 0$
	CPL F_0	1 0 0 1	0 1 0 1	9 5	1	1	$(F_0) \leftarrow (\overline{F_0})$
	CLR F_1	1 0 1 0	0 1 0 1	A 5	1	1	$(F_1) \leftarrow 0$
	CPL F_1	1 0 1 1	0 1 0 1	B 5	1	1	$(F_1) \leftarrow (\overline{F_1})$
Subroutine	CALL m	$m_{10}m_9m_8$ 1 $m_7m_6m_5m_4$	0 1 0 0 $m_3m_2m_1m_0$	1 4 $m_8 \sim m_{10}$ m	2	2	$((SP)) \leftarrow (PC)(PSW_4 \sim PSW_7)$ $(SP) \leftarrow (SP)+1$ $(PC_0 \sim PC_{10}) \leftarrow m$
	RET	1 0 0 0	0 0 1 1	8 3	1	2	$(SP) \leftarrow (SP)-1$ $(PC) \leftarrow ((SP))$
	RETR	1 0 0 1	0 0 1 1	9 3	1	2	$(SP) \leftarrow (SP)-1$ $(PC)(PSW_4 \sim PSW_7) \leftarrow ((SP))$
Input/Output	IN A, P_p	0 0 0 0	1 0 P_1 P_0	0 8+p	1	2	$(A) \leftarrow (P_p)$ $p=1 \sim 2$
	OUTL P_p, A	0 0 1 1	1 0 P_1 P_0	3 8+p	1	2	$(P_p) \leftarrow (A)$ $P=1 \sim 2$
	ANL P_p, #n	1 0 0 1 $n_7n_6n_5n_4$	1 0 P_1 P_0 $n_3n_2n_1n_0$	9 8+p n	2	2	$(P_p) \leftarrow (P_p) \wedge n$ $p=1 \sim 2$
	ORL P_p, #n	1 0 0 0 $n_7n_6n_5n_4$	1 0 P_1 P_0 $n_3n_2n_1n_0$	8 8+p n	2	2	$(P_p) \leftarrow (P_p) \vee n$ $p=1 \sim 2$
	IN A, DBB	0 0 1 0	0 0 1 0	2 2	1	1	$(A) \leftarrow (DBB)$
	OUT DBB, A	0 0 0 0	0 0 1 0	0 2	1	1	$(DBB) \leftarrow (A)$

FUNCTIONS OF SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

Type \ Item	Mnemonic	Instruction code $D_7D_6D_5D_4$	$D_3D_2D_1D_0$	Hexadecimal	Bytes	Cycles	Function
I/O Expander Control	MOVD A, Pp	0 0 0 0	1 1 P_1 P_0	0 C + p_1p_0	1	2	$(A_0 \sim A_3) \leftarrow (P_{p0} \sim P_{p3})$ $(A_4 \sim A_7) \leftarrow 0$ p=4~7
	MOVD Pp, A	0 0 1 1	1 1 P_1 P_0	3 C + p_1p_0	1	2	$(P_{p0} \sim P_{p3}) \leftarrow (A_0 \sim A_3)$ P=4~7
	ANLD Pp, A	1 0 0 1	1 1 P_1 P_0	9 C + p_1p_0	1	2	$(P_{p0} \sim P_{p3}) \leftarrow (P_{p0} \sim P_{p3}) \wedge (A_0 \sim A_3)$ p=4~7
	ORLD Pp, A	1 0 0 0	1 1 P_1 P_0	8 C + p_1p_0	1	2	$(P_{p0} \sim P_{p3}) \leftarrow (P_{p0} \sim P_{p3}) \vee (A_0 \sim A_3)$ p=4~7
Control	EN I	0 0 0 0	0 1 0 1	0 5	1	1	(INTF) ← 1
	DIS I	0 0 0 1	0 1 0 1	1 5	1	1	(INTF) ← 0
	SEL RB0	1 1 0 0	0 1 0 1	C 5	1	1	(BS) ← 0
	SEL RB1	1 1 0 1	0 1 0 1	D 5	1	1	(BS) ← 1
	EN DMA	1 1 1 0	0 1 0 1	E 5	1	1	
	EN FLAGS	1 1 1 1	0 1 0 1	F 5	1	1	$(P2_4) \leftarrow$ (OBF) $(P2_5) \leftarrow$ (IBF)
Timer/Counter Control	MOV A, T	0 1 0 0	0 0 1 0	4 2	1	1	(A) ← (T)
	MOV T, A	0 1 1 0	0 0 1 0	6 2	1	1	(T) ← (A)
	STRT T	0 1 0 1	0 1 0 1	5 5	1	1	
	STRT CNT	0 1 0 0	0 1 0 1	4 5	1	1	
	STOP TCNT	0 1 1 0	0 1 0 1	6 5	1	1	
	EN TCNTI	0 0 1 0	0 1 0 1	2 5	1	1	(TCNTF) ← 1
	DIS TCNTI	0 0 1 1	0 1 0 1	3 5	1	1	(TCNTF) ← 0
Misc	NOP	0 0 0 0	0 0 0 0	0 0	1	1	

Note 1 : Executing an instruction may produce a carry (overflow or underflow) The carry may be lost or it may be transferred to C or AC The (○) mark indicates a carry which affects C or AC The detail affection of carries for instructions ADD, ADDC and DA is as follows

(C) ← 1 At overflow of accumulator
(C) ← 0 At no overflow of accumulator
(AC) ← 1 At overflow of bit 3 of accumulator
(AC) ← 0 At no overflow

2 : The contents of ST_4-ST_7 are read when host computer reads status of MELPS 8-41.

FUNCTIONS OF SERIES MELPS 8-41 SLAVE MICROCOMPUTERS

Item	Details of execution
RESET input low level	TF (Timer Flag) ← 0 TIRF (Timer INT Request FF) ← 0 TCNTF (Timer INT Enable FF) ← 0 INTF (External INT Enable FF) ← 0 IEF (INT Enable FF) ← 1 IBF ← 0 EIPF (External Interrupt Pending FF) ← 0
JTF execution	TF (Timer Flag) ← 0
Timer/event Counter overflow	TF (Timer Flag) ← 1 TCNTE (Timer INT Enable FF) = 1 When TIRF (Timer INT Request FF) ← 1
EN TNCTI execution	TCNTF (Timer INT Enable FF) ← 1
DIS TNCTI execution	TCNTF (Timer INT Enable FF) ← 0
EN I execution	INTF (External INT Enable FF) ← 1
DIS I execution	INTF (External INT Enable FF) ← 0
RETR execution	IEF (INT Enable FF) ← 1

Symbol	Contents	Symbol	Contents
A	8-bit register (accumulator)	PC	Program counter
A_0~A_3	Low-order 4 bits of register A	PC_0~PC_7	Low-order 8 bits of program counter
A_4~A_7	High-order 4 bits of register A	PC_8~PC_{10}	High-order 3 bits of program counter
A_0~A_n, A_{n+1}	Bits of register A	PSW	Program status word
b	Value of bits 5-7 of first byte machine code	Rr	Register designator
$b_7b_6b_5$	Bits 5-7 of first byte machine code	r	Register number
BS	Register bank select	r_0	Value of bit 0 of machine code
AC	Auxiliary carry flag	$r_2r_1r_0$	Value of bits 0-2 of machine code
C	Carry flag	$s_2s_1s_0$	Value of bits 0-2 of stack pointer
DBB	Data bus buffer	SP	Stack pointer
F_0	Flag 0	ST_4ST_7	Bits 4-7 of status register
F_1	Flag 1	STS	System status
INTF	External interrupt enable flip-flop	T	Timer/event counter
IBF	Input buffer full flag	T_0	Test pin 0
m	Destination address	T_1	Test pin 1
$m_7m_6m_5m_4m_3m_2m_1m_0$	Second byte (low-order 8 bits) machine code	TCNTF	Timer/event counter interrupt flip-flop
	corresponding to destination address	TF	Timer flag
$m_{10}m_9m_8$	Bits 5-7 of first byte (high-order 3 bits) machine code	#	Symbol to indicate immediate data
(M(A))	Content of memory location addressed by register A	@	Symbol to indicate content of memory location
(M(Rr))	Content of memory location addressed by register Rr		addressed by register
(Mx(Rr))	Content of external memory location addressed by	←	Shows direction of data flow
	register Rr	↔	Exchanges contents of data
n	Value of immediate data	( )	Contents of register, memory location or flag
$n_7n_6n_5n_4n_3n_2n_1n_0$	Immediate data of second byte machine code	∧	Logical AND
OBF	Output buffer full flag	∨	Logical OR
p	Port number	∀	Exclusive OR
P_P	Port designator	—	Negation
p_1p_0	Bits of machine code corresponding to port number	○	Content of flag is set or reset after execution

FUNCTION

The M5L8041A-XXXP is designed as an ordinary 8-bit CPU peripheral LSI chip and it contains a small stand-alone microcomputer. Although this microcomputer functions independently, when it is used as a peripheral controller, it is called the slave microcomputer in contrast to the master computer. These two devices can transfer the data alternatively through the buffer register between them. The M5L8041A-XXXP contains the buffer register to use this LSI as a slave microcomputer and it can be accessed in the same way as other standard peripheral devices. Since the M5L8041A-XXXP is a complete microcomputer, it is easy to develop a user-oriented mask-programmed peripheral LSI only by changing the control software.

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground	—	Connected to a 0V supply (ground)
V_{CC}	Main power supply	—	Connected to a 5V supply
V_{DD}	Power supply	—	Connected to a 5V supply
			Used as a memory hold when V_{CC} is cut off
T_0	Test pin 0	Input	Provides external control of conditional program jumps (JTO/JNTO instructions).
X_1, X_2	Crystal inputs	Input	An internal clock circuit is provided so that by connecting an RC circuit or crystal to these input pins the clock frequency can be determined. Pins X_1 and X_2 can also be used to input an external clock signal
$\overline{RESET}$	Reset	Input	CPU initialization input.
$\overline{SS}$	Single step	Input	Used to halt the execution of a command by the CPU When used in combination with the SYNC signal, the command execution of the CPU can be halted every instruction to enable single step operation
$\overline{CS}$	Chip select input	Input	Chip select input data bus control
EA	External access	Input	Normally maintained at 0V
$\overline{R}$	Read enable signal	Input	Serves as the read signal when the master CPU is accepting data on the data bus from the M5L8041A-XXXP.
A_0	Address input	Input	An address input used to indicate whether the signal on the data bus is data or a command
$\overline{W}$	Write enable signal	Input	Serves as the write signal when the master CPU is outputting data from the bus to the M5L8041A-XXXP
SYNC	Sync signal output	Output	Output 1 time for each machine cycle.
DQ_0~DQ_7	Data bus	Input/output	Three-state, bidirectional data bus. Data bus is used to interface the M5L8041A-XXXP to a master system data bus.
$P2_0$~$P2_7$	Port 2	Input/output	Quasi-bidirectional port When used as an input port, FF_{16} must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary.
			$P2_0$~$P2_3$ are used when the M5L8243P I/O port expander is used
PROG	Program	Output	Serves as the strobe signal when the M5L8243P I/O expander is used
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port When used as an input port, FF_{16} must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary
T_1	Test pin 1	Input	Provides external control of conditional program jumps (JT1/JNT1 instructions).
			Can serve as the input pin for the event counter (STRT CNT instructions)

TIMING REQUIREMENTS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

DBB Read

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Cycle time	t_{CY}		2.5		15	μs
$t_{W(R)}$	Read pulse with	t_{RR}	$t_{C(\phi)}$ = 2.5 μs	250			ns
$t_{su(CS-R)}$	Chip-select setup time befor read	t_{AR}		0			ns
$t_{h(R-CS)}$	Chip-select hold time after read	t_{RA}		0			ns

DBB Write

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(W)}$	Write pulse width	t_{WW}		250			ns
$t_{su(CS-W)}$ $t_{su(A0-W)}$	$\overline{CS}$, A_0, setup time before write	t_{AW}		0			ns
$t_{h(W-CS)}$ $t_{h(W-A0)}$	$\overline{CS}$, A_0, hold time after wirte	t_{WA}		0			ns
$t_{su(DQ-W)}$	Data setup time before write	t_{DW}		150			ns
$t_{h(W-DQ)}$	Data hold time after write	t_{WD}		0			ns

Port 2

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(PR)}$	PROG pulse width	t_{PP}		1200			ns
$t_{su(PC-PR)}$	Port control setup time before PROG	t_{CP}	C_L = 80pF	110			ns
$t_{h(PR-PC)}$	Port control hold time after PROG	t_{PC}	C_L = 20pF	100			ns
$t_{su(Q-PR)}$	Output data setup time before PROG	t_{DP}	C_L = 80pF	250			ns
$t_{su(D-PR)}$	Input data hold timer before PROG	t_{PR}	C_L = 80pF			810	ns
$t_{h(PR-D)}$	Input data hold time after PROG	t_{PF}	C_L = 20pF	0		150	ns

DMA

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{su(DACK-R)}$	Data acknowledge time before read	t_{ACC}		0			ns
$t_{h(R-DACK)}$	Data hold time after read	t_{CAC}		0			ns
$t_{su(DACK-W)}$	Data setup time before write	t_{ACC}		0			ns
$t_{h(W-DACK)}$	Data hold time after write	t_{CAC}		0			ns

SWITCHING CHARACTERISTICS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

DBB Read

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(CS-DQ)}$	Data enable time after $\overline{CS}$	t_{AD}	C_L = 150 pF			225	ns
$t_{PZX(A0-DQ)}$	Data enable time after address	t_{AD}	C_L = 150 pF			225	ns
$t_{PZX(R-DQ)}$	Data enable time after read	t_{RD}	C_L = 150 pF			225	ns
$t_{PXZ(R-DQ)}$	Data disable time after read	t_{DF}				100	ns

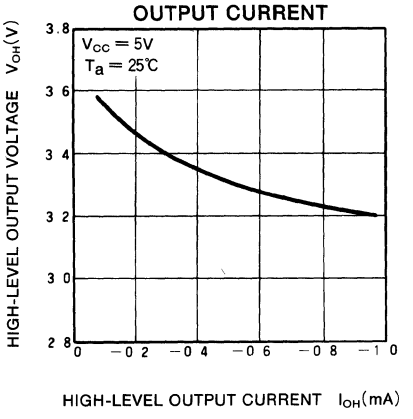
DMA

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(DACK-DQ)}$	Data enable time after DACK	t_{ACD}	150 pF Load			225	ns
$t_{PHL(R-DRQ)}$	DRQ disable time after read	t_{CRQ}	150 pF Load			200	ns
$t_{PHL(W-DRQ)}$	DRQ disable time after write	t_{CRQ}	150 pF Load			200	ns

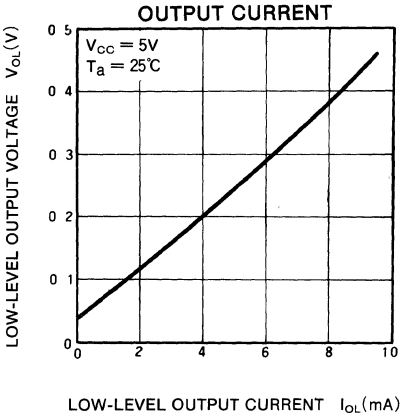
Note 2 : Output voltage discriminating levels, low and high, are 0.8V and 2.0V respectively

TYPICAL CHARACTERISTICS

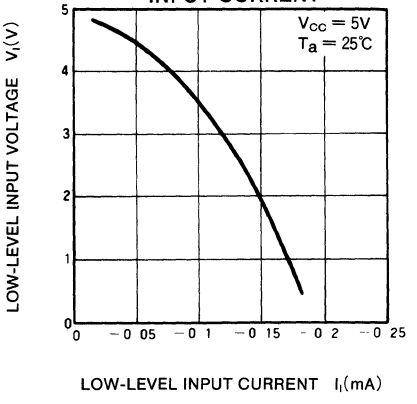
DATA BUS HIGH-LEVEL OUTPUT VOLTAGE VS. HIGH-LEVEL OUTPUT CURRENT



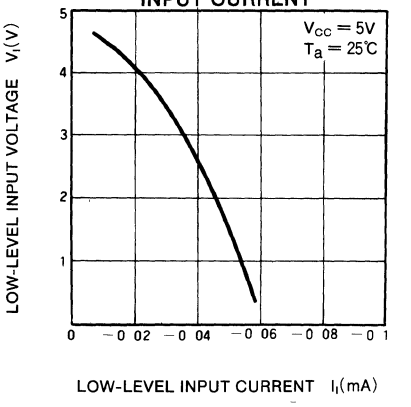
DATA BUS LOW-LEVEL OUTPUT VOLTAGE VS. LOW-LEVEL OUTPUT CURRENT



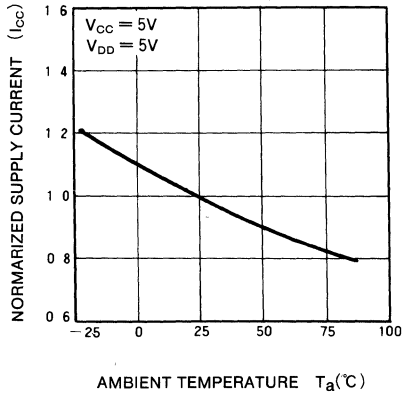
P_1, P_2 LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



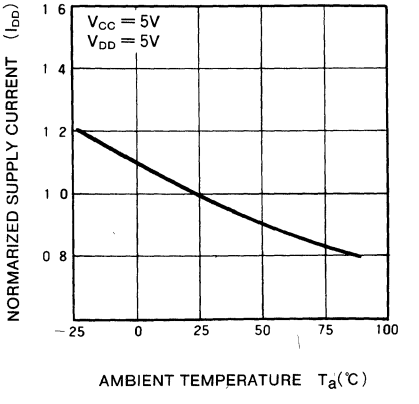
RESET LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



NORMARIZED SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE



NORMARIZED SUPPLY CURRENT (I_{DD}) VS. AMBIENT TEMPERATURE



M5L8041AH-XXXP

SLAVE MICROCOMPUTER

DESCRIPTION

The M5L8041AH-XXXP is a general-purpose, programmable interface device deisgned for use with a variety of 8-bit microcomputer systems. This device is fabricated using N-channel sillicon-gate ED-MOS technology.

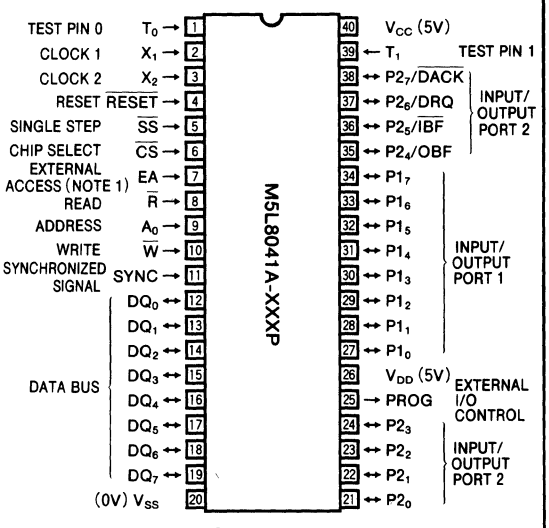
FEATURES

- Mask ROM ..... 1024-word by 8-bit
- Static RAM ..... 64-word by 8-bit
- Instruction cycle 1.25μs
  (Oscillator frequency 12MHz)
- 18 programmable I/O pins
- Asynchronous data register for interface to master processor
- 8-bit CPU, ROM, RAM, I/O, timer, clock and low power, stand-by mode
- Single 5V supply
- Alternative to custom LSI

APPLICATION

Alternative to custom LSI for peripheral interface

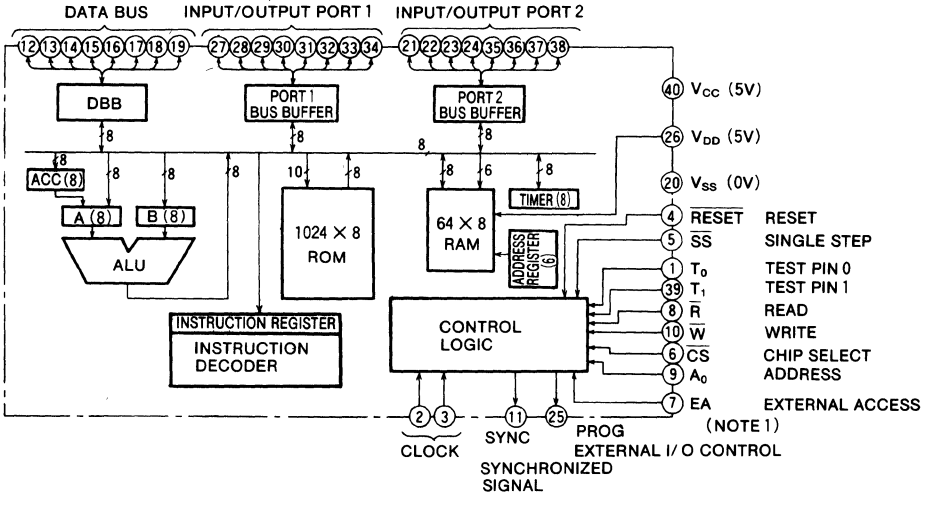
PIN CONFIGURATION (TOP VIEW)



Outline 40P4

Note 1 : Connect to V_{SS} in the operating condition.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.5～7	V
V_{DD}	Supply voltage		−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
P_d	Power dissipation	T_a = 25℃	1500	mW
T_{opr}	Operating temperature range		0～70	℃
T_{stg}	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS

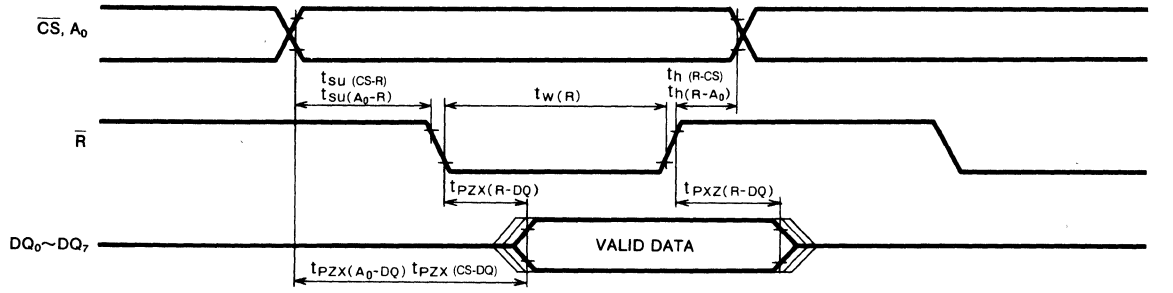
Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
$f_{(\phi)}$	Operating frequency	1		12	MHz

ELECTRICAL CHARACTERISTICS (T_a = 0～70℃, V_{CC} = 5 V±10%, unless otherwise noted)

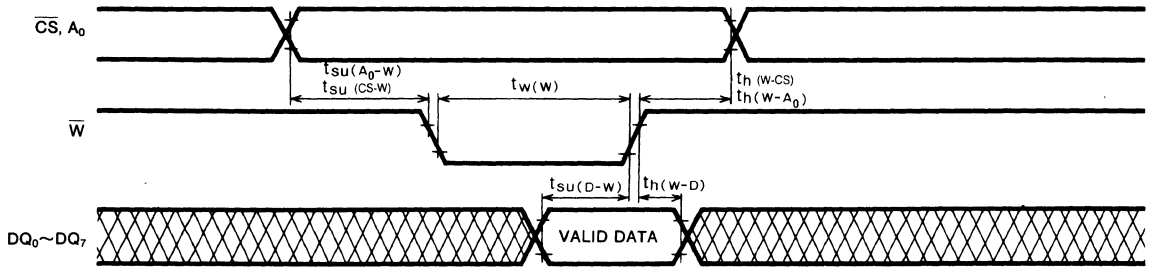
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{IH1}	High-level input voltage (all except X_1, X_2, $\overline{RESET}$)		2.0		V_{CC}	V
V_{IH2}	High-level input voltage (X_1, X_2, $\overline{RESET}$)		3.8		V_{CC}	V
V_{OL1}	Low-level output voltage (DQ_0～DQ_7)	I_{OL} = 2mA			0.45	V
V_{OL2}	Low-level output voltage ($P1_0$～$P1_7$, $P2_0$～$P2_7$, SYNC)	I_{OL} = 1.6 mA			0.45	V
V_{OL3}	Low-level output voltage (PROG)	I_{OL} = 1mA			0.45	V
V_{OH1}	High-level output voltage (DQ_0～DQ_7)	I_{OH} = −400μA	2.4			V
V_{OH2}	High-level output voltage (all other outputs)	I_{OH} = −50μA	2.4			V
I_I	Input leakage current (T_0, T_1, $\overline{R}$, $\overline{W}$, $\overline{CS}$, A_0, EA)	$V_{SS} \leqq V_1 \leqq V_{CC}$	−10		10	μA
I_{OZL}	High-impedance state output leakage current (DQ_0～DQ_7)	$V_{SS} + 0.45 \leqq V_0 \leqq V_{CC}$	−10		10	μA
I_{IL1}	Low-level input load current ($P1_0$～$P1_7$, $P2_0$～$P2_7$)	V_{IL} = 0.8V	−0.5			mA
I_{IL2}	Low-level input load current ($\overline{RESET}$, $\overline{SS}$)	V_{IL} = 0.8V	−0.2			mA
I_{DD}	Supply current from V_{DD}				10	mA
$I_{CC} + I_{DD}$	Total supply current				145	mA

TIMING DIAGRAMS

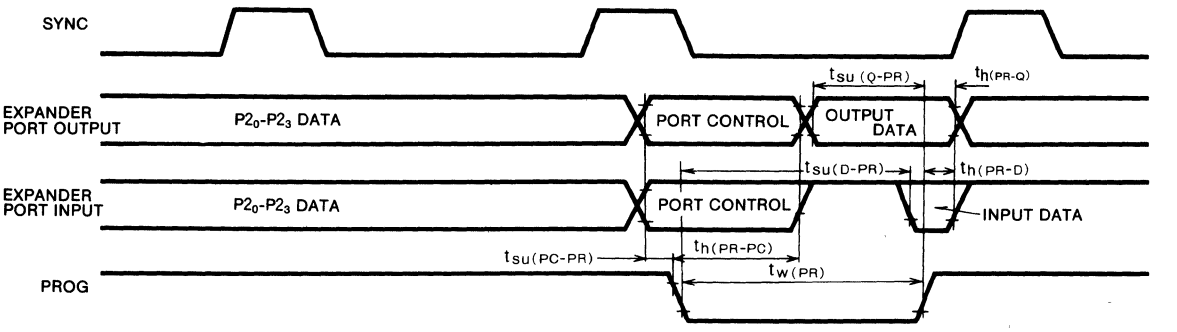
Read



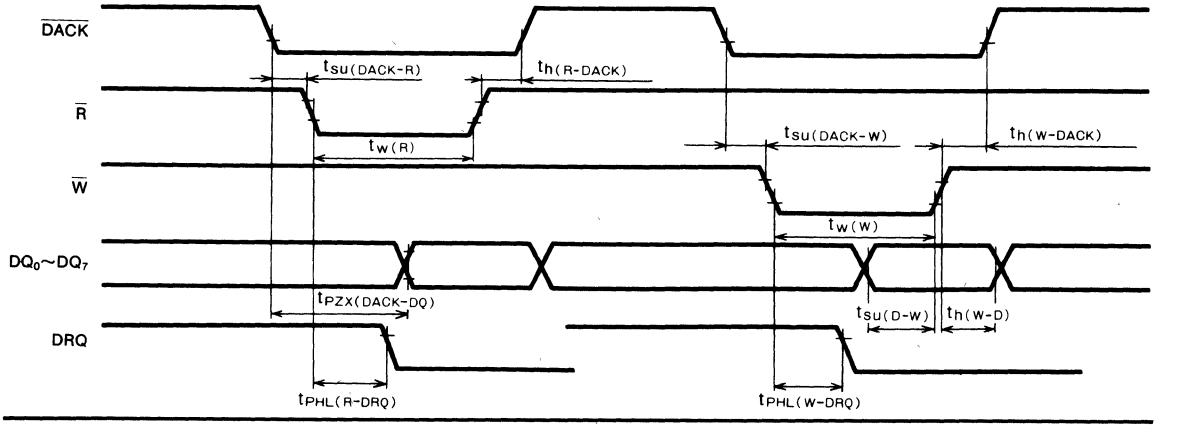
Write



Port 2

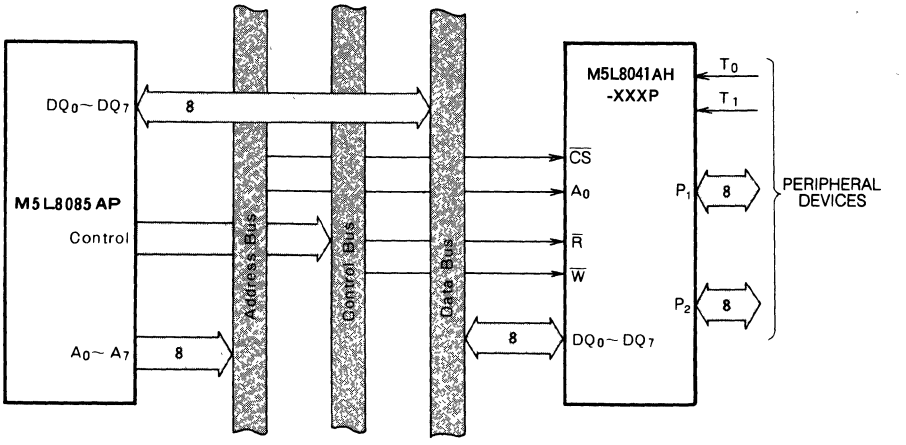


DMA

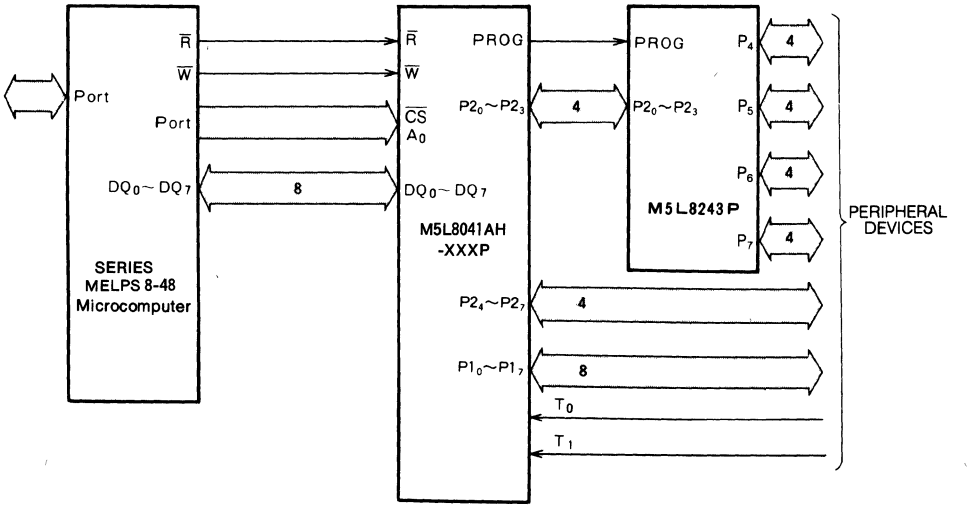


APPLICATION EXAMPLES

(1) Interface with M5L8085AP



(2) Interface with Series MELPS 8-48 Microcomputer and M5L8243P



FUNCTION

The M5L8042-XXXP is designed as an ordinary 8-bit CPU peripheral LSI chip and it contains a small stand-alone microcomputer. Although this microcomputer functions independently, when it is used as a peripheral controller, it is called the slave microcomputer in contrast to the master computer. These two devices can transfer the data alternatively through the buffer register between them. The M5L8042-XXXP contains the buffer register to use this LSI as a slave microcomputer and it can be accessed in the same way as other standard peripheral devices. Since the M5L8042-XXXP is a complete microcomputer, it is easy to develop a user-oriented mask-programmed peripheral LSI only by changing the control software.

PIN DESCRIPTION

Pin	Name	Input or output	Function
V_{SS}	Ground	—	Connected to a 0V supply (ground)
V_{CC}	Main power supply	—	Connected to a 5V supply
V_{DD}	Power supply	—	Connected to a 5V supply
			Used as a memory hold when V_{CC} is cut off
T_0	Test pin 0	Input	Provides external control of conditional program jumps (JTO/JNTO instructions)
X_1, X_2	Crystal inputs	Input	An internal clock circuit is provided so that by connecting an RC circuit or crystal to these input pins, the clock frequency can be determined. X_1 and X_2 can also be used to input an external clock signal
$\overline{RESET}$	Reset	Input	CPU initialization input.
$\overline{SS}$	Single step	Input	Used to halt the execution of a command by the CPU When used in combination with the SYNC signal, the command execution of the CPU can be halted every instruction to enable single step operation
$\overline{CS}$	Chip select input	Input	Chip select input for data bus control.
EA	External access	Input	Normally maintained at 0V
$\overline{R}$	Read enable signal	Input	Serves as the read signal when the master CPU is accepting data on the data bus from the M5L8042-XXXP
A_0	Address input	Input	An address input used to indicate whether the signal on the data bus is data or a command
$\overline{W}$	Write enable signal	Input	Serves as the write signal when the master CPU is outputting data from the bus to the M5L8042-XXXP.
SYNC	Sync signal output	Output	Output 1 time for each machine cycle.
DQ_0~DQ_7	Data bus	Input/output	Three-state, bidirectional data bus. Data bus is used to interface the M5L8042-XXXP to a master system data bus
$P2_0$~$P2_7$	Port 2	Input/output	Quasi-bidirectional port When used as an input port, FF_{16} must first be output to this port. After resetting, however, when not used afterwards as an output port, this is not necessary.
			$P2_0$~$P2_3$ are used when the M5L8243P I/O expander is used
PROG	Program	Output	Serves as the strobe signal when the M5L8243P I/O expander is used
$P1_0$~$P1_7$	Port 1	Input/output	Quasi-bidirectional port. When used as an input port, FF_{16} must first be output to this port After resetting, however, when not used afterwards as an output port, this is not necessary
T_1	Test pin 1	Input	Provides external control of conditional program jumps (JT1/JNT1 instructions)
			Can serve as the input pin for the event counter (STRT CNT instruction)

TIMING REQUIREMENTS (T_a = 0~70℃, V_{CC} = 5V±10%, unless otherwise noted)

DBB Read

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{C(\phi)}$	Cycle time	t_{CY}		1.25		15	μs
$t_{W(R)}$	Read pulse width	t_{RR}	$t_{C(\phi)}$ = 1.25 μs	160			ns
$t_{su(CS-R)}$	Chip select setup time before read	t_{AR}		0			ns
$t_{h(R-CS)}$	Chip select hold time after read	t_{RA}		0			ns

DBB Write

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(W)}$	Write pulse width	t_{WW}		160			ns
$t_{su(CS-W)}$ $t_{su(A0-W)}$	$\overline{CS}$, A_0, setup time before write	t_{AW}		0			ns
$t_{h(W-CS)}$ $t_{h(W-A0)}$	$\overline{CS}$, A_0, hold time after write	t_{WA}		0			ns
$t_{su(DQ-W)}$	Data setup time before write	t_{DW}		130			ns
$t_{h(W-DQ)}$	Data hold time after write	t_{WD}		0			ns

Port 2

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{W(PR)}$	PROG pulse width	t_{PP}		700			ns
$t_{su(PC-PR)}$	Port control setup time before PROG	t_{CP}	C_L = 80pF	80			ns
$t_{h(PR-PC)}$	Port control hold time after PROG	t_{PC}	C_L = 20pF	60			ns
$t_{su(Q-PR)}$	Output data setup time before PROG	t_{DP}	C_L = 80pF	200			ns
$t_{su(D-PR)}$	Input data hold time before PROG	t_{PR}	C_L = 80pF			650	ns
$t_{h(PR-D)}$	Input data hold time after PROG	t_{PF}	C_L = 20pF	0		150	ns

DMA

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{su(DACK-R)}$	$\overline{DACK}$ setup time before read	t_{ACC}		0			ns
$t_{h(R-DACK)}$	$\overline{DACK}$ hold time after read	t_{CAC}		0			ns
$t_{su(DACK-W)}$	$\overline{DACK}$ setup time before write	t_{ACC}		0			ns
$t_{h(W-DACK)}$	$\overline{DACK}$ hold time after write	t_{CAC}		0			ns

Note 1 : Input voltage level V_{IL} = 0.45V, V_{IH} = 2.4V

SWITCHING CHARACTERISTICS (T_a = 0~70℃, V_{CC} = 5V±10%, unless otherwise noted)

DBB Read

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(CS-DQ)}$	Data enable time after $\overline{CS}$	t_{AD}	C_L = 100 pF			130	ns
$t_{PZX(A0-DQ)}$	Data enable time after address	t_{AD}	C_L = 100 pF			130	ns
$t_{PZX(R-DQ)}$	Data enable time after read	t_{RD}	C_L = 100 pF			130	ns
$t_{PXZ(R-DQ)}$	Data disable time after read	t_{DF}				85	ns

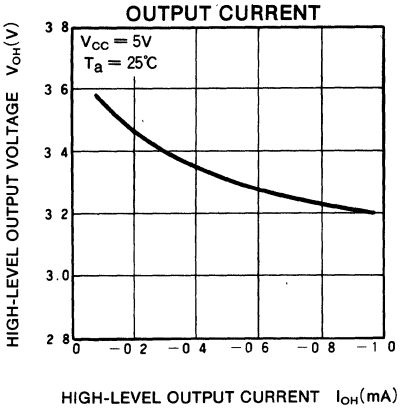
DMA

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PZX(DACK-DQ)}$	Data enable time after $\overline{DACK}$	t_{ACD}	C_L = 150 pF			130	ns
$t_{PHL(R-DRQ)}$	DRQ disable time after read	t_{CRQ}				90	ns
$t_{PHL(W-DRQ)}$	DRQ disable time after write	t_{CRQ}				90	ns

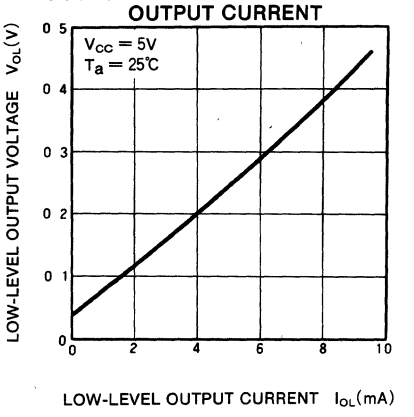
Note 2 : Output voltage discriminating levels, low and high, are 0.8V and 2.0V respectively

TYPICAL CHARACTERISTICS

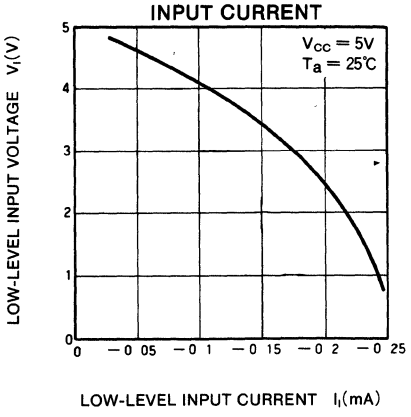
DATA BUS HIGH-LEVEL OUTPUT VOLTAGE VS. HIGH-LEVEL OUTPUT CURRENT



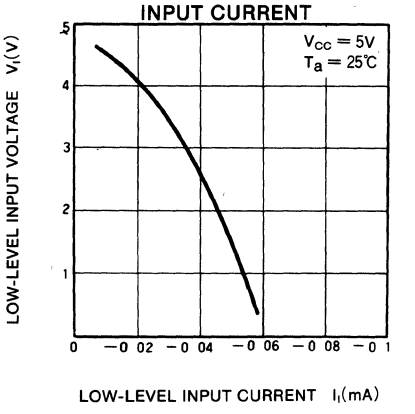
DATA BUS LOW-LEVEL OUTPUT VOLTAGE VS. LOW-LEVEL OUTPUT CURRENT



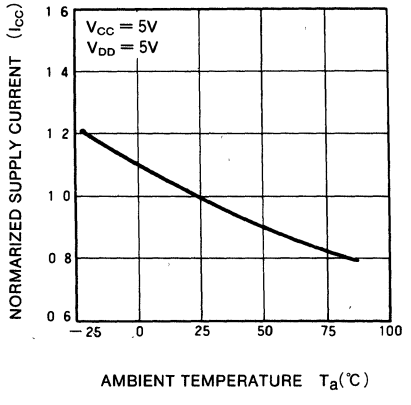
P_1, P_2 LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



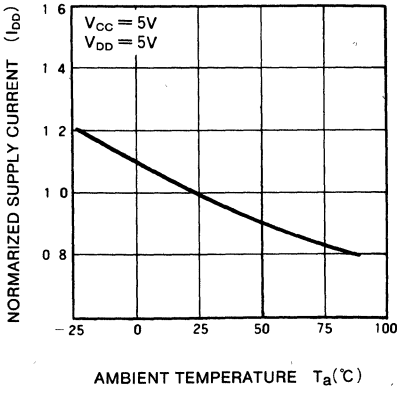
RESET LOW-LEVEL INPUT VOLTAGE VS. LOW-LEVEL INPUT CURRENT



NORMARIZED SUPPLY CURRENT (I_{CC}) VS. AMBIENT TEMPERATURE



NORMARIZED SUPPLY CURRENT (I_{DD}) VS. AMBIENT TEMPERATURE



PIN DESCRIPTION

Symbol	Name	Input or output	Function
$\overline{CS}$	Chip select	In	Chip select input. A high on $\overline{CS}$ causes PROG input to be regarded high inside the M5L8243P, then this inhibits any change of output or internal status.
PROG	Program	In	A high-to-low transition on PROG signifies that address (PORT 4-7) and control are available on PORT 2, and a low-to-high transition signifies that the designated data is available on the disignated port through PORT 2. The designation is shown in Table 1.
$P2_0 \sim P2_3$	Input/output port 2	In/out	The 4-bit bidirectional port contains the address and control bits shown in Table 1 on a high-to-low transition of PROG. During a low-to-high transition it contains the input (output) data on this port.
$P4_0 \sim P4_3$ $P5_0 \sim P5_3$ $P6_0 \sim P6_3$ $P7_0 \sim P7_3$	Input/output port 4 Input/output port 5 Input/output port 6 Input/output port 7	In/out	The 4-bit bidirectional I/O port. May be programmed to be input, low-impedance latched output or a three-state. This port is automatically set output mode when it is written. ANLed or ORLed then continues its mode until next read operation. After reset on a read operation, this port is in high-impedance and input mode.

OPERATION

The M5L8243P is an input/output expander designed specifically for the Series MELPS 8-41 and Series MELPS 8-48. The Series MELPS 8-41 and Series MELPS 8-48 already have instructions and PROG pin to communicate with the M5L8243P.

An example of the M5L8243P and the Series MELPS 8-41 or Series MELPS 8-48 is shown in Fig. 1. The following description of the M5L8243P basic operation is made according to Fig. 1.

Upon initial application of power supply to the device, and then about 500μs after, resident bias circuits become stable and each device is ready to operate. And each port of the M5L8243P is set input mode (high-impedance) by means of a resident power-on initialization circuit.

When the microcomputer begins to execute a transfer instruction

MOVD A , Pi i = 4, 5, 6, 7

which means the value on the port Pi is transferred to the accumulator, then the signals are sent out on the pins PROG and $P2_0 \sim P2_3$ as shown in Timing Diagram.

On the high-to-low transition of the pin PROG, the M5L8243P latches the instructions (ex. 0000) into itself from pins $P2_0 \sim P2_3$ and transfers them to the instruction register (① in Timing Diagram). During the low-level of PROG, the M5L8243P continuously outputs the contents of the specified input (output) port (in this case port P_4) to pins $P2_0 \sim P2_3$ (② in Timing Diagram). The microcomputer, at an appropriate time, latches the level of pins $P2_0 \sim P2_3$ and resumes high-level of PROG.

The next example is the case in which the microcomputer executes

MOVD Pi , A i = 4, 5, 6, 7

the transfer (output) instruction.

In this case, as in the previous case, on the high-to-low transition of the pin PROG, the M5L8243P latches the instructions (ex. 0110) into itself from pins $P2_0 \sim P2_3$ and transfers them to the instruction register (① in Timing Diagram). After this, the microcomputer sends out high to the pin PROG, transferring the data to pin $P2_0 \sim P2_3$ which is an output data to input/output port. Then the M5L8243P transfers the data of pins $P2_0 \sim P2_3$ to the port latch of the designated input/output port (in this case P_6). In a few seconds after a low-to-high transition on the PROG, the designated port (P_6) becomes in an output mode and the data of the port latch are transferred to the port pins (③ in Timing Diagram).

When instructions

ANLD Pi , A
ORLD Pi , A i = 4, 5, 6, 7

are executed, the microcomputer generally operates as same function as MOVD Pi, A.

It only differs in that the data of port latch after ④ in the Timing Diagram is ANDed or ORed with the data of port latch before ④ and the data of pins $P2_0 \sim P2_3$.

When instructions

MOVD Pi , A
ANLD Pi , A
ORLD Pi , A i = 4, 5, 6, 7

are executed toward the port in an output mode, the outputs are generated on the port as soon as low-to-high transition on the PROG occurs.

When the mode of the output port is going to be changed during the execution and the instruction

MOVD A , Pi i = 4, 5, 6, 7

is executed, it is preferable to execute one dummy instruction. Because it takes a little time to turn the designated port into a high-impedance state after high-to-low transition on the PROG, the result may be that the first instruction is not read correctly.

TIMING REQUIREMENTS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{su(INST-PR)}$	Instruction code setup time before PROG	t_A	80pF Load	100			ns
$t_{h(PR-INST)}$	Instruction code hold time after PROG	t_B	20pF Load	60			ns
$t_{su(DQ-PR)}$	Data setup time before PROG	t_C	80pF Load	200			ns
$t_{h(PR-DQ)}$	Data hold time after PROG	t_D	20pF Load	20			ns
$t_{w(PR)}$	PROG pulse width	t_K		700			ns
$t_{su(CS-PR)}$	Chip-select setup time before PROG	t_{CS}		50			ns
$t_{h(PR-CS)}$	Chip-select hold time after PROG	t_{CS}		50			ns
$t_{su(PORT-PR)}$	Port setup time before PROG	t_{IP}		100			ns
$t_{h(PR-PORT)}$	Port hold time after PROG	t_{IP}		100			ns

SWITCHING CHARACTERISTICS (T_a = −20~75℃, V_{CC} = 5V±10%, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(PR)}$	Data access time after PROG	t_{ACC}	80pF Load	0		650	ns
$t_{dv(PR)}$	Data valid time after PROG	t_H	20pF Load	0		150	ns
$t_{PHL(PR)}$ $t_{PLH(PR)}$	Output valid time after PROG	t_{PO}	100pF Load			700	ns
$t_{PZX(PR)}$ $t_{PXZ(PR)}$	Input/output switching time	—				800	ns

Example

To use 20mA sinking capability at port 7, find the effects on the sinking capabilities of the other I/O lines.

Assume the M5L8243P is driving loads as shown below.

3 lines: $-20mA$ ($V_{OL} = 1.0V$ max, port 7 only)

4 lines: $-4mA$ ($V_{OL} = 0.45V$ max)

9 lines: $-1.6mA$ ($V_{OL} = 0.45V$ max)

Is this within the allowable limit ?

$\Sigma I_{OL} = (20mA \times 3) + (4mA \times 4) + (1.6mA \times 9) = 90.4mA$

From the curve we see that with respect to $I_{OL} = 4mA$, I_{OL} is 93mA (Point B) and that the above load of 90.4mA is within the limit of 93mA.

Note: The sinking current of ports $4 \sim 7$ must not exceed 30mA regardless of the value of V_{OL}.

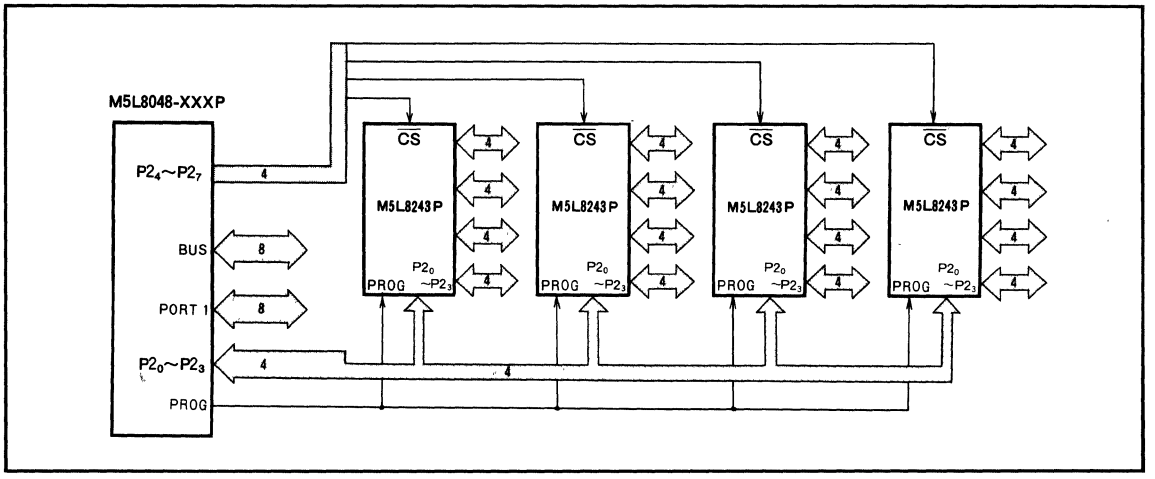


Fig.2 Expansion interface example

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Symbol	Name	Input or output	Function
$\overline{CS}$	Chip select	In	Chip select input. A high on $\overline{CS}$ causes PROG input to be regarded high inside the M5M82C43P. This then inhibits any change of output or internal status
PROG	Program	In	A high-to-low transition on PROG signifies that address (ports 4~7) and control are available on port 2, and a low-to-high transition signifies that the designated data is available on the designated port through port 2 The designation is shown in Table 1.
$P2_0 \sim P2_3$	Input/output port 2	In/out	This 4-bidirectional port contains the address and control bits shown in Table 1 on a high-to-low transition of PROG. During a low-to-high transition, it contains the input (output) data on this port
$P4_0 \sim P4_3$ $P5_0 \sim P5_3$ $P6_0 \sim P6_3$ $P7_0 \sim P7_3$	Input/output port 4 Input/output port 5 Input/output port 6 Input/output port 7	In/out	4-bit bidirectional I/O ports. May be programmed to be input, low-impedance latched or 3-state These ports are automatically set to the output mode when written, ANLed or ORLed and this mode continues until the next read operation After reset on a read operation, this port is placed in the high impedance and input mode

OPERATION

The M5M82C43P is an input/output expander designed specifically for the Series MELPS8-41 and Series MELPS8-48. The Series MELPS8-41 and Series MELPS8-48 already have instructions and PROG pin to communicate with the M5M82C43P.

An example of the M5M82C43P and the M5M80C49-XXXP is shown in Fig. 1. The following description of the M5M82C43P basic operation is made according to Fig. 1.

Upon initial application of the power supply to the device, each port of the M5M82C43P is set to the input mode (high-impedance) by means of the resident power-on initialization circuit.

When the microcomputer begins to execute a transfer instruction

MOVD A, Pi i = 4, 5, 6, 7

which means the value on the port Pi is transferred to the accumulator, then the signals are sent out on the pins PROG and $P2_0 \sim P2_3$, as shown in the timing diagram.

On the high-to-low transition of pin PROG, the M5M82C43P latches the instructions (e.g. 0000) into itself from pins $P2_0 \sim P2_3$ and transfers them to the instruction register (① in the timing diagram). During the low-level of PROG, the M5M82C43P continuously outputs the contents of the specified input (output) port (in this case, port P4) to pins $P2_0 \sim P2_3$ (② in the timing diagram). The microcomputer, at the appropriate time, latches the level of pins $P2_0 \sim P2_3$ and resumes the high level of PROG.

The next example is the case in which the microcomputer executes

MOVD Pi, A i = 4, 5, 6, 7

the transfer (output) instruction.

In this case, as in the previous case, on the high-to-low transition of pin PROG, the M5M82C43P latches the instructions (e.g.0110) into itself from pins $P2_0 \sim P2_3$ and transfers them to the instruction register (① in the timing diagram).

After this the microcomputer sends out high to pin PROG, transferring the data to pins $P2_0 \sim P2_3$ which is an output data to the input/output port. Then the M5M82C43P transfers the data of pins $P2_0 \sim P2_3$ to the port latch of the designated input/output port (in this case P6). In a few seconds after a low-to-high transition on the PROG, the designated port (P6) is set to the output mode and the data of the port latch is transferred to the port pins (③ in the timing diagram).

When instructions

ANLD Pi, A
ORLD Pi, A i = 4, 5, 6, 7

are executed, the microcomputer generally operates as the same function as MOVD Pi, A.

It only differs in that the data of the port latch after ④ in the timing diagram is ANDed or ORed with the data of the port latch before ④ and the data of pins $P2_0 \sim P2_3$

When instructions

MOVD Pi, A
ANLD Pi, A
ORLD Pi, A i = 4, 5, 6, 7

are executed toward the port in an output mode, the outputs are generated on the port as soon as low-to-high transition on the PROG occurs.

When the mode of the output port is going to be changed during the execution and the instruction

MOVD A, Pi i = 4, 5, 6, 7

is executed, it is preferable to execute one dummy instruction. Because it takes a little time to turn the designated port into a high-impedance state after the high-to-low transition on the PROG, the result may be that the first instruction is not read correctly

TIMING REQUIREMENTS (T_a = −20~75℃, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{su(INST-PR)}$	Instruction code setup time befor PROG	t_A	C_L = 80pF	100			ns
$t_{h(PR-INST)}$	Instruction code hold time after PROG	t_B	C_L = 20pF	60			ns
$t_{su(DQ-PR)}$	Data setup time before PROG	t_C	C_L = 80pF	200			ns
$t_{h(PR-DQ)}$	Data hold time after PROG	t_D	C_L = 20pF	20			ns
$t_{W(PR)}$	PROG pulse with	t_K		700			ns
$t_{su(CS-PR)}$	Chip select setup time before PROG	t_{CS}		50			ns
$t_{h(PR-CS)}$	Chip select hold time after PROG	t_{CS}		50			ns
$t_{su(PORT-PR)}$	Port setup time before PROG	t_{IP}		100			ns
$t_{h(PR-PORT)}$	Port hold time after PROG	t_{IP}		100			ns

SWITCHING CHARACTERISTICS (T_a = −40~85℃, V_{CC} = 5V±10%, V_{SS} = 0V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(PR)}$	Data access time after PROG	t_{ACC}	C_L = 80pF	0		650	ns
$t_{dv(PR)}$	Data valid time after PROG	t_H	C_L = 20pF	0		150	ns
$t_{PHL(PR)}$ $t_{PLH(PR)}$	Output valid time after PROG	t_{PO}	C_L = 100pF			700	ns
$t_{PZX(PR)}$ $t_{PXZ(PR)}$	Input/output switching time	—				800	ns

Example:
To use the 20mA sinking capability at port 7, find the effects on the sinking capabilities of the other I/O lines. Assume the M5M82C43P is driving loads as shown below:
3 lines: 20mA (V_{OL} = 1.0V max, port 7 only)
4 lines: 4mA (V_{OL} = 0.45V max)
9 lines: 1.6mA (V_{OL} = 0.45V max)
Is this within the allowable limit ?
ΣI_{OL} = (20mA × 3) + (4mA × 4) + (1.6mA × 9) = 90.4mA

From the curve it is seen that with respect to I_{OL} = 4mA, I_{OL} is 93mA (point B) and that the above load of 90.4mA is within the limit of 93mA.
Note: The sinking current of port 4 ~ 7 must not exceed 30mA regardless of the value of V_{OL}.

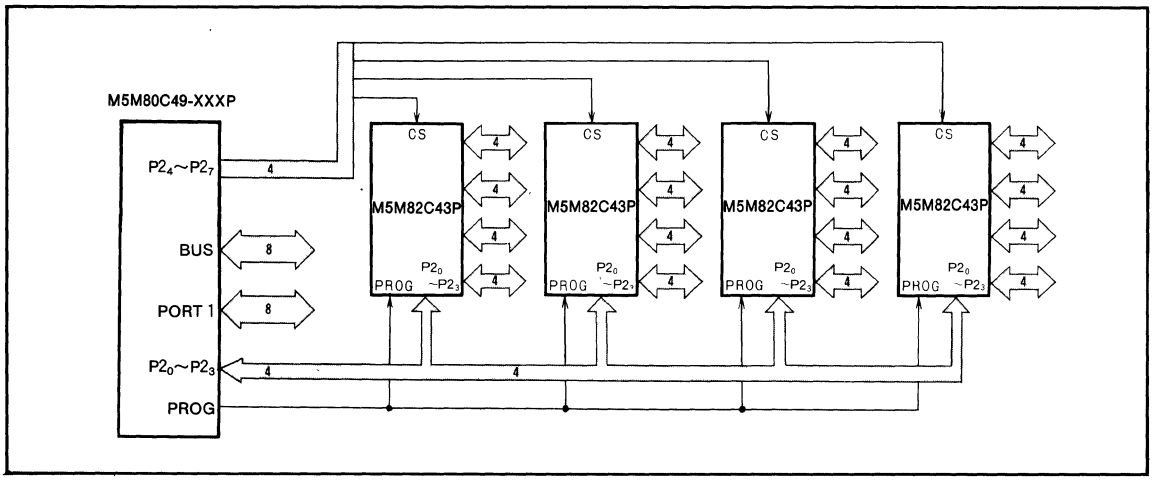


Fig.2 Expansion interface example

SERIES MELPS 8-48 MASK ROM ORDERING METHOD

SERIES MELPS 8-48 MASK-PROGRAMMABLE ROM CONFIRMATION MATERIAL

SINGLE-CHIP 8-BIT MICROCOMPUTERS M5L8048-XXXP, M5L8049-XXXP, P-6, M5L8049H1-XXXP and M5M8050H-XXXP

MITSUBISHI ELECTRIC

	Signature
Customer Company name _____ Company address _____ Tel _____	Prepared
Company contact _____ Date _____	Approved

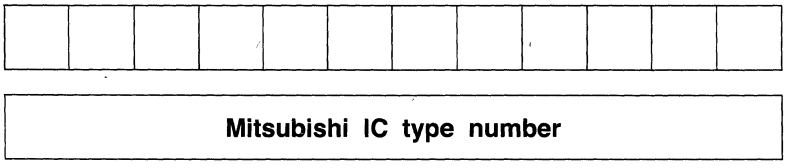
The single-chip microcomputer type number to order and the type of EPROMs to be supplied should be specified by checking ⁄ in the boxes. Three sets of EPROMs should be supplied.

EPROM type number / microcomputer type number	□2732	□2764	
□M5L8048-XXXP	□A (000_{16} ~ $3FF_{16}$)	□A (000_{16} ~ $3FF_{16}$)	□8748 □8748H
□M5L8049-XXXP □M5L8049-XXXP-6	□A (000_{16} ~ $7FF_{16}$)	□A (000_{16} ~ $7FF_{16}$)	□8749 □8749H
□M5L8049H1-XXXP	□A (000_{16} ~ $7FF_{16}$)	□A (000_{16} ~ $7FF_{16}$)	□8749 □8749H
□M5M8050H-XXXP	□A (000_{16} ~ FFF_{16})	□A (000_{16} ~ FFF_{16})	—

Note 1 : The high-level data of both data outputs and address inputs of the supplied EPROM will be programmed as '1', and low-level as '0'.
2 : Cleary indicate the type number of EPROMs and address designation letter symbols A and B on the supplied EPROMs
3 : The data of the addresses in parentheses on the EPROM are programmed onto the ROM
4 : The data from each PROM in the set is compared and if 2 of the 3 are equal, the equal value will be programmed into the ROM. When the 3 values are different programming is halted and the customer is notified of the error. The error report will show the address and data

CUSTOMER'S IDENTIFICATION MARK

If you require a special identification mark, please specify in the following format.



Note 5 : A mark field should start with the box at the extreme right
6 : The identification mard should be no more than 12 characters consisting of alphanumeric characters (except J,I and O) or dashes

COMMENTS

SERIES MELPS 8-41 MASK ROM ORDERING METHOD

MASK ROM ORDERING METHOD

Described below is the ordering method applicable when programs submitted by the customer are written into the mask ROMs.

An automatic mask ROM design program is prepared for writing programs into mask ROMs, and (1) the drafting data for mask ROM generation, (2) the reference list for mask ROM preparation error checks and (3) an automatic test protram for the large-scale tester designed to test the mask ROMs are all automatically generated.

When the object program is stored in the Series MELPS 8-41 single-chip microcomputer mask ROM, the order for the object program medium is received as an EPROM form. Consequently, the EPROM or EPROMs which have stored the object program equivalent to one single-chip microcomputer chip should be submitted accompanied by the prescribed confirmation sheets for 3 sets of EPROMs respectively.

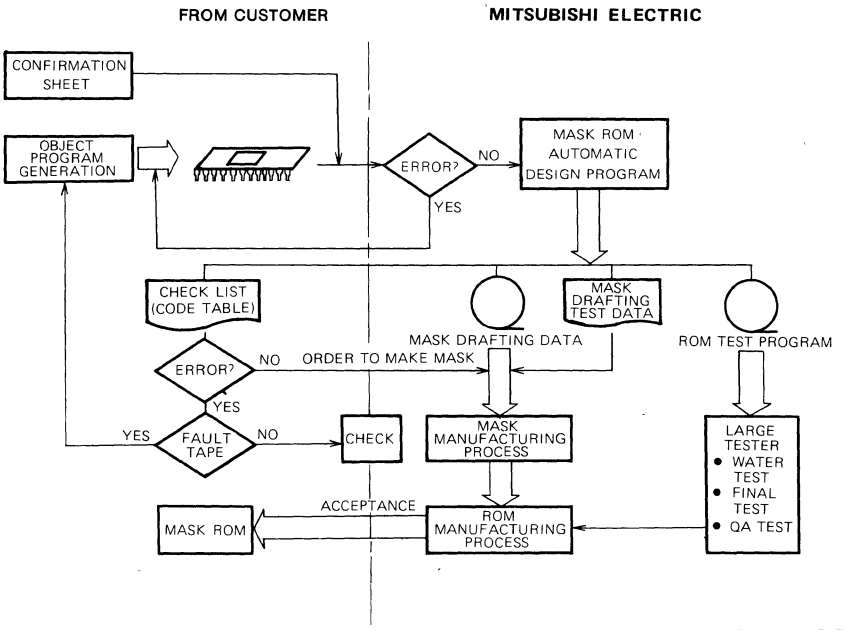
EPROM SPECIRICATIONS

1. Usable EPROMs include Mitsubishi's M5L2732K and M5L2764K or Intel's 2732, 8741, 8741A, 8742 or their equivalent. The M5L2732K and the M5L2764K are the standard EPROMs.
2. "High" is treated as 1 for the EPROM data and address.
3. All the data from the head address to the final address are treated as the EPROM's effective data.

CHECKPOINTS

1. Cleary indicate the type number of EPROM.

SERIES MELPS 8-41 MASK ROM DEVELOPMENT CAD SYSTEM



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