LOGIC

DEVICES INCORPORATED

Fast CMOS

Data Book

July 1990

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LOGIC

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Introduction

Logic Devices Incorporated continues its commitment to provide our customers with the highest performance products available without abandoning our dedication to improving price/performance and quality. To do this, we bring to bear submicron CMOS technology on a par with the most advanced production processes in the world. By coupling this technology with our crack engineering design teams, we offer the fastest devices available. Logic Devices' product diversification remains at the forefront of our ability to supply total solutions with high performance logic products, peripheral and memory products.

We proudly present this new edition of the Logic Devices Product Catalog containing our full line of some 84 products, nearly double last year's offering. Logic Devices' products bring new levels of performance to a wide range of application environments, including general-purpose computing, DSP and image processing, computer peripherals, and embedded control. We've worked hard to revise and reformat the data sheets in this year's catalog to ease your design effort and assist in your navigation of the device/package/temperature/speed maze.

Section 2, Memory Products, features the latest speed upgrades of our high-speed 16K and 64K-bit SRAM families. Also we're pleased to introduce our new 256K-bit SRAM family boasting the fastest access speeds available anywhere.

Section 3, FIFO Memory Products, details the latest augmentation of our product line. This family of FIFOs offers a wide range of widths, depths and status information. Plus, they're designed for expandability.

Section 4, Memory Modules, gathers together Logic Devices' offerings to solve high-speed/high-density memory problems.

Section 5, Logic Products, gives a roll call of our standard high-speed families of multipliers, multiplier/accumulators, ALUs, and pipeline registers including the latest speed enhancements and more than few new devices to help fill your design needs.

Background and reference information on the topics of Quality & Reliability, Latchup, ESD Protection, and Power Dissipation are supplied in Sections 7 & 8. Packaging information, including a detailed discussion of thermal considerations, can be found in Section 9. Application Notes and Technical Article reprints reside in Sections 10 & 11, respectively, and feature solutions to typical design problems.

Lastly, if further information is required, please contact your local Logic Devices sales office. Logic Devices locations worldwide are listed in Section 12, conveniently located at the end of this catalog.

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Part Numbering System

To construct a valid part number:

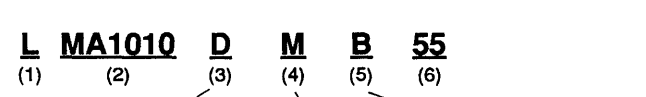
In order to construct a valid Logic Devices part number, begin with the generic number obtained from the datasheet header or the product selection guide. To this number, append three characters from the tables below indicating the desired package code, temperature range, and screening. Finally, append zero, one, or two digits indicating the performance grade desired. Most devices are offered in several speed grades with the part number suffix indicating a critical path delay in nanoseconds.

For more information on available part numbers:

All products are not offered with all combinations of package style, temperature range, and screening. The Ordering Information table on the last page of each product datasheet indicates explicitly all valid combinations of package, temperature, screening, and performance codes for a given product.

For more information on package options:

Also given in the Ordering Information tables in each product datasheet are the Logic Devices package codes. These are two character codes consisting of a letter designating a package type, and a number distinguishing the individual package drawing. Drawings giving detailed dimensions and tolerances for each package code can be found in the Mechanical Data section of this catalog. For example, the LMA1010DMB55 given below refers to a "D" or sidebraze, hermetic DIP package. The LMA1010/2010 datasheet indicates that the actual package used is D6. In the Mechanical Data section package type D6 is seen to be a 64-pin, cavity-down, sidebraze, hermetic DIP.



Key:
(1) Prefix, Logic Devices, Inc.
(2) Device number
(3) Package code
(4) Temperature range
(5) Screening
(6) Performance/speed

Package Code

Suffix	Description
C, I*	CerDIP
D, H*	Sidebraze, Hermetic DIP
F	Ceramic Flat Pack
G	Ceramic Pin Grid Array
J	Plastic J-Lead Chip Carrier
K, T*	Ceramic Leadless Chip Carrier
L	Ceramic Leaded Chip Carrier
P, N*	Plastic DIP
U, V*	Plastic SOIC (Gull-Wing)
W	Plastic SOJ (J-Lead)
X	Dice

Temperature Range

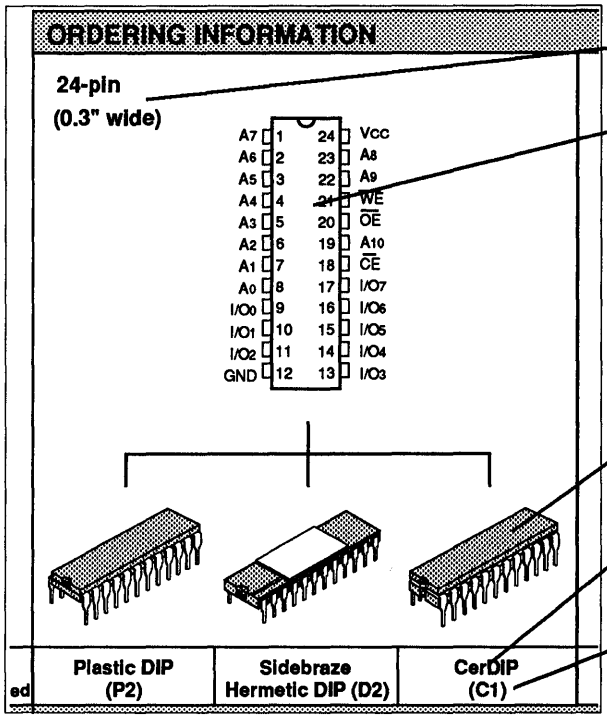
Suffix	Description
C	Commercial 0°C to +70°C
M	Military –55°C to +125°C

Screening

Suffix	Description
No Designator	Commercial Flow
R	48 Hour Burn-in at 125°C
E	Extended Screening
B	MIL-STD-883 Class B Compliant

*Some devices are available in packages of two widths. For devices available in a single width, C, D, K, P, and V are used.

ORDERING INFORMATION PAGE EXPLANATION



Pinout number and package width.

Package pinout drawing.

Package illustration.

Package type.

Mechanical drawing code (see Section 9 for specific package specifications)

Speeds available.

Part number base. A complete part number for example would be L6116PC25.

When parts are available in two package widths, for example, CerDIP 0.3" wide use L6116CC25 or 0.6" wide use L6116IC25.

Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic DIP (P1)	Sidebraze Hermetic DIP (D1)	CerDIP (C4)
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L6116PC 35 25 20 15 12 10 or L6116LPC	L6116DC 35 25 20 15 12 10 or L6116LDC	L6116CC 35 25 20 25 12 10 or L6116LCC	L6116NC 35 25 20 15 12 10 or L6116LNC	L6116HC 35 25 20 15 12 10 or L6116LHC	L6116IC 35 25 20 25 12 10 or L6116LIC
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns		L6116DM 35 35	L6116CM 35 25		L6116HM 35 35	L6116IM 35 25

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Radiation-Hard Static RAM Products

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Static RAM Package Availability Guide

Part No.[1]	No. Pins	Package Availability Code[2]						
		Plastic DIP	Sidebraze Hermetic DIP	CerDIP	SOIC (Gull-Wing)	SOJ (J-Lead)	Plastic LCC	Ceramic LCC
16K Static RAMs								
L7C167	20	P6	D7	C2	U3	W3		K6
L7C168	20	P6	D7	C2	U3	W3		
L7C170	22/24	P8	D8	C3		W1		
L7C171	24/28	P2	D2	C1		W1		K1
L7C172	24/28	P2	D2	C1		W1		K1
L6116	24/28/32	P1, P2	D1, D2	C1, C4	U1	W1		K1, K7
64K Static RAMs								
L7C187	22/24	P8	D8	C3	U1	W1		K4
L7C164	22/24	P8	D8	C3	U1	W1		K4
L7C165	24	P2	D2	C1	U1	W1		
L7C166	24/28	P2	D2	C1	U1	W1		K5
L7C161	28	P10	D10	C5	U2	W2		K5
L7C162	28	P10	D10	C5	U2	W2		K5
L7C185	28/32	P9, P10	D9, D10	C5, C6	U2, V2	W2		K5, K7
256K Static RAMs								
L7C197	24	P2		C1	V1	W1		
L7C194	24	P2		C1	V1	W1		
L7C195	28	P10		C5	V2	W2		
L7C196	28	P10		C5	V2	W2		
L7C191	28	P10		C5	V2	W2		
L7C192	28	P10		C5	V2	W2		
L7C199	28/32	P9, P10		C5, C6	V2	W2		K5, K7
Special Architecture RAMs								
L7C180	22/24	P8	D8	C3		W1		
L7C181	22/24	P8	D8	C3		W1		
L7C174	28/32	P9, P10	D9, D10	C5		W2		K7
L7C186	28/32	P9, P10	D9, D10	C5		W2		K7
L7C183	48/52	P5	D5				J5	K9
L7C184	48/52	P5	D5				J5	K9

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 9 – Packaging for package dimensions.

16K Static RAM — Product Selection

Part No.[1]	Description	Maximum Speed (ns) Com.	Mil.	Typical Power (mW) Oper.	Inactive	Pins	Packages Available[2]
L7C167	16K x 1 Separate I/O	8	10	135	75	20	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C168	4K x 4 Common I/O	8	10	190	75	20	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C170	4K x 4 Common I/O + OE	8	10	190	75	22/24	DIP SOJ (J-Lead)
L7C171	4K x 4 Separate I/O Transparent Write	8	10	190	75	24/28	DIP, LCC SOJ (J-Lead)
L7C172	4K x 4 Separate I/O High Impedance Write	8	10	190	75	24/28	DIP, LCC SOJ (J-Lead)
L6116/ L6116L	2K x 8 Common I/O + OE	10	12	250	75/60	24/28/32	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)

16K Static RAM — Product Cross Reference

Competitor	LOGIC DEVICES PART NUMBER L7C167 (16K x 1)	L7C168 (4K x 4)	L7C170 (4K x 4)	L7C171 (4K x 4)	L7C172 (4K x 4)	L6116 (2K x 8)
Cypress	CY7C167	CY7C168	CY7C170	CY7C171	CY7C172	CY7C128/6116
IDT	IDT6167	IDT6168	NA	IDT71681	IDT71682	IDT6116
Performance	NA	P4C168	P4C170	P4C1681	P4C1682	P4C116
Saratoga	SSM6167	SSM6168	SSM6170	SSM6171	SSM6172	SSM6116
Hitachi	HM6167/6267	HM6168/6268	NA	NA	NA	HM6116/6716
Fujitsu	MB81C67	MB81C68/69	NA	NA	NA	MB8416
Toshiba	NA	TMM2068	TMM2078	NA	NA	TMM2015/2018
Micron	MT5C1601	MT5C1604	MT5C1605	MT5C1606	MT5C1607	MT5C1608
Motorola	MCM2167	MCM6168/1423	NA	NA	NA	MCM2016/18
Inmos	IMS1400/03	IMS1420/21/23	NA	NA	NA	IMS1433
Sony	NA	CXK5416	NA	NA	NA	CXK5814/16
NEC	µPD4311	µPD4314	NA	NA	NA	µPD446

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 9 – Packaging for package dimensions.

64K Static RAM — Product Selection

Part No.[1]	Description	Maximum Speed (ns) Com.	Mil.	Typical Power (mW) Oper.	Inactive	Pins	Packages Available[2]
L7C187	64K x 1 Separate I/O	8	10	135	75	22/24	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C164	16K x 4 Common I/O 1 Chip Enable	8	10	210	75	22/24	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C165	16K x 4 Common I/O 2 Chip Enables + OE	8	10	210	75	24/28	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C166	16K x 4 Common I/O 1 Chip Enable + OE	8	10	210	75	24/28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C161	16K x 4 Separate I/O Transparent Write	8	10	210	75	28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C162	16K x 4 Separate I/O High Impedance Write	8	10	210	75	28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)
L7C185/ L7CL185	8K x 8 Common I/O + OE	10	12	320	75/60	28	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)

64K Static RAM — Product Cross Reference

Competitor	LOGIC DEVICES PART NUMBER L7C187 (64K x 1)	L7C164 (16K x 4)	L7C165 (16K x 4)	L7C166 (16K x 4)	L7C161 (16K x 4)	L7C162 (16K x 4)	L7C185 (8K x 8)
Cypress	CY7C187	CY7C164	NA	CY7C166	CY7C161	CY7C162	CY7C185/186
IDT	IDT7187	IDT7188	IDT7198	IDT6198	IDT71981	IDT71982	IDT7164
Performance	P4C187	P4C188	P4C198A	P4C198	P4C1981	P4C1982	P4C164
Saratoga	SSM7187	SSM7188	SSM7198	SSM7166	SSM7161	SSM7162	SSM7164
Hitachi	HM6287/6787	HM6288/6788	NA	HM6789	NA	NA	HM6264
Fujitsu	MB81C71	MB81C74	MB81C75	NA	NA	NA	MB81C78/8464
Toshiba	TC5561/5562	TC55416	NA	TC55417	NA	NA	TC5588
Micron	MT5C6401	MT5C6404	NA	MT5C6405	MT5C6406	MT5C6407	MT5C6408
Motorola	MCM6287	MCM6288/89	NA	MCM6290	NA	NA	MCM61/6264
Inmos	IMS1600/01	IMS1620	NA	IMS1624	NA	NA	IMS1630
Sony	CXK5164	CXK5464	NA	CXK5465	NA	NA	CXK5864/65
NEC	µPD4361	µPD4362	NA	µPD4363	NA	NA	µPD4364/4464

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 9 – Packaging for package dimensions.

256K Static RAM — Product Selection

Part No.[1]	Description	Maximum Speed (ns) Com.	Mil.	Typical Power (mW) Oper.	Inactive	Pins	Packages Available[2]
L7C197	256K x 1 Separate I/O	12	15	210	100	24	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C194	64K x 4 Common I/O 1 Chip Enable	15	20	265	100	24	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C195	64K x 4 Common I/O 1 Chip Enable + OE	15	20	265	100	28	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C196	64K x 4 Common I/O 2 Chip Enables + OE	15	20	265	100	28	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C191	64K x 4 Separate I/O Transparent Write	15	20	265	100	28	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C192	64K x 4 Separate I/O High Impedance Write	15	20	265	100	28	DIP SOIC (Gull-Wing) SOJ (J-Lead)
L7C199/ L7CL199	32K x 8 Common I/O + OE	15	20	380	100/60	28/32	DIP, LCC SOIC (Gull-Wing) SOJ (J-Lead)

256K Static RAM — Product Cross Reference

Competitor	LOGIC DEVICES PART NUMBER L7C197 (256K x 1)	L7C194 (64K x 4)	L7C195 (64K x 4)	L7C196 (64K x 4)	L7C191 (64K x 4)	L7C192 (64K x 4)	L7C199 (32K x 8)
Cypress	CY7C197	CY7C194	NA	CY7C196	CY7C191	CY7C162	CY7C199/198
IDT	IDT71257	IDT71258	IDT61298	NA	IDT71281	IDT71282	IDT71256
Performance	P4C1257	P4C1258	NA	NA	NA	NA	P4C1256
Saratoga	NA	NA	NA	NA	NA	NA	NA
Hitachi	HM6207/6707	HM6208/6708	NA	HM6789	NA	NA	HM6264
Fujitsu	MB81C81	MB81C84	NA	NA	NA	MB81C86	MB84256
Toshiba	NA	TC55464	TC55465	NA	NA	NA	TC55328
Micron	MT5C2561	MT5C2564	MT5C2565	NA	NA	NA	MT5C2568
Inmos	IMS1800	IMS1820	NA	NA	NA	NA	IMS1830
Mitsubishi	M5M5257	M5M5258	NA	NA	NA	NA	M5M5256
NEC	NA	µPD43254	NA	NA	NA	NA	µPD43256
Samsung	KM61257	KM64257	NA	NA	NA	NA	KM68257

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 9 – Packaging for package dimensions.

Special Architecture Static RAM — Product Selection

Part No.[1]	Description	Maximum Speed (ns) Com.	Mil.	Typical Power (mW) Oper.	Inactive	Pins	Packages Available[2]
L7C180	4K x 4 Cache-Tag Totem Pole MATCH Output	10	12	225	75	22/24	DIP SOJ (J-Lead)
L7C181	4K x 4 Cache-Tag Open Drain MATCH Output	10	12	225	75	22/24	DIP SOJ (J-Lead)
L7C174	8K x 8 Cache-Tag	12	15	320	75	28/32	DIP, LCC SOJ (J-Lead)
L7C186/ L7CL186	8K x 8 Flash Clear Reset	12	15	320	75/60	28/32	DIP, LCC SOJ (J-Lead)
L7C183	2 x 4K x 16 Cache-Data Fast A_{12} Access Two-Way Set Associative or Direct Map	25	35	350	75	48/52	DIP, LCC PLCC
L7C184	2 x 4K x 16 Cache-Data Two-Way Set Associative or Direct Map	25	35	350	75	48/52	DIP, LCC PLCC

Special Architecture Static RAM — Product Cross Reference

	LOGIC DEVICES PART NUMBER						
Competitor	L7C180 (4K x 4)	L7C181 (4K x 4)	L7C174 (8K x 8)	L7C186 (8K x 8)	L7C183 (2 x 4K x 16)	L7C184 (2 x 4K x 16)	
IDT	IDT6178	IDT7178	IDT7174	IDT7165	NA	NA	
Saratoga	SSL4180	SSL4181	NA	NA	NA	NA	
Motorola	MCM4180	NA	NA	NA	NA	NA	
SGS-Thomson	MK41H80	NA	NA	NA	NA	NA	
Cypress	NA	NA	NA	NA	CY7C183	CY7C184	

Radiation-Hard Static RAM — Product Selection

Part No.[1]	Description	Total Dose	Dose Rate Upset	Dose Rate Survivability	Neutron Hardness	Pins	Package[2] Availability
L7CX187	64K x 1 Radiation-Hard	$\geq 10^6$ Rads (SiO_2)	$\geq 10^9$ Rads (Si)/s	$>10^{12}$ Rads (Si)/s	$>10^{14}$ N/cm^2	24	DIP
L7CX197	256K x 1 Radiation-Hard	$\geq 10^6$ Rads (SiO_2)	$\geq 10^9$ Rads (Si)/s	$>10^{12}$ Rads (Si)/s	$>10^{14}$ N/cm^2	24	DIP

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 9 – Packaging for package dimensions.

The following Figures 1 through 8 represent typical DC and AC characteristic curves for the 16K and 64K static RAM products listed below:

16K Static RAMs
L7C167 — 16K × 1
L7C168 — 4K × 4
L7C170 — 4K × 4
L7C171 — 4K × 4
L7C172 — 4K × 4
L6116 — 2K × 8
L6116L — 2K × 8

64K Static RAMs
L7C187 — 64K × 1
L7C164 — 16K × 4
L7C165 — 16K × 4
L7C166 — 16K × 4
L7C161 — 16K × 4
L7C162 — 16K × 4
L7C185 — 8K × 8
L7CL185 — 8K × 8

Cache-Tag Static RAMs
L7C180 — 4K × 4
L7C181 — 4K × 4
L7C174 — 8K × 8
L7C186 — 8K × 8
L7CL186 — 8K × 8

FIGURE 1. NORMALIZED SUPPLY CURRENT VS AMBIENT TEMPERATURE — I_{CC1}

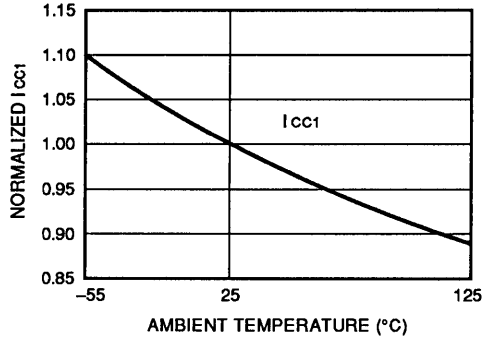


FIGURE 2. NORMALIZED SUPPLY CURRENT VS AMBIENT TEMPERATURE — I_{CC2}

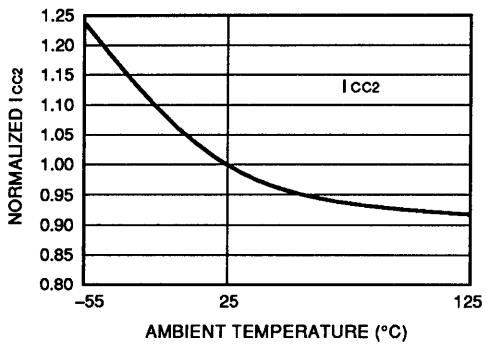


FIGURE 3. NORMALIZED SUPPLY CURRENT VS AMBIENT TEMPERATURE — I_{CC3}

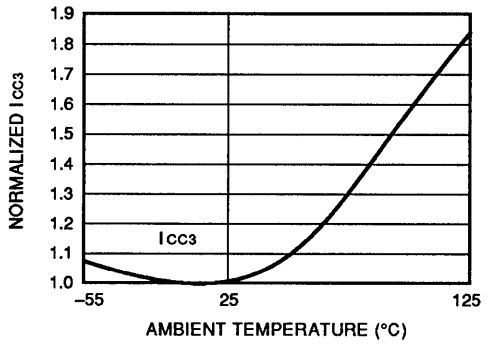


FIGURE 4. NORMALIZED SUPPLY CURRENT VS AMBIENT TEMPERATURE — I_{CC4}

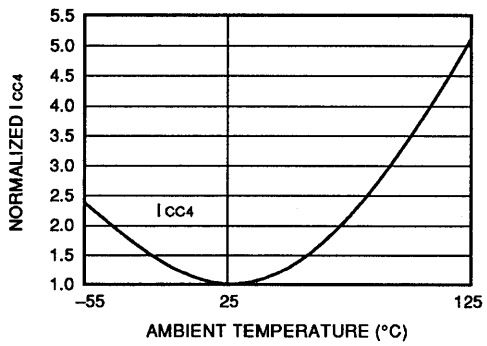


Figure 5. Output Sink Current vs Output Voltage

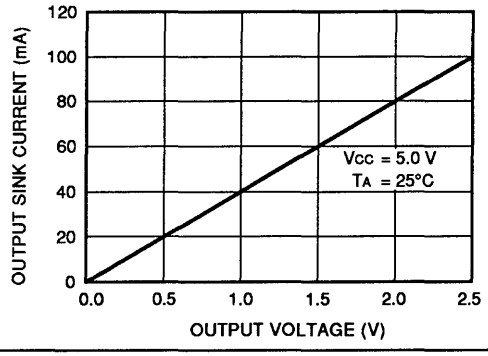


Figure 6. Output Source Current vs Output Voltage

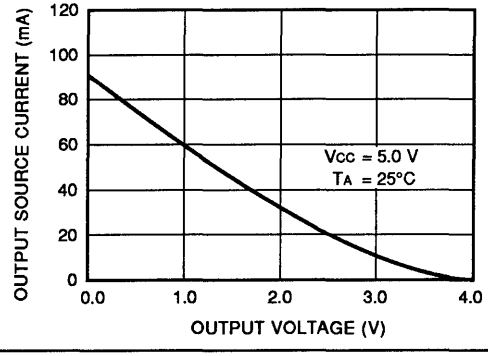


Figure 7. Normalized Access Time vs Supply Voltage

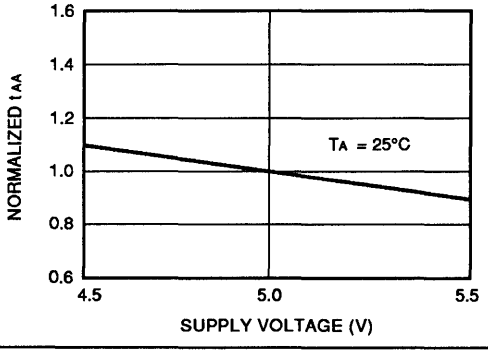
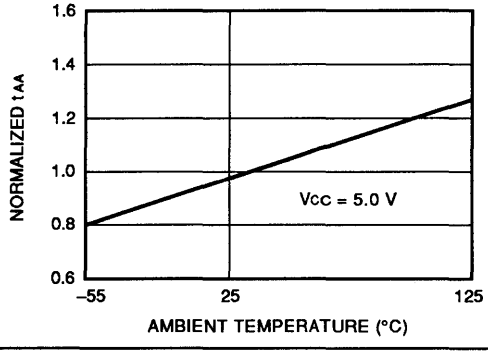


Figure 8. Normalized Access Time vs Ambient Temperature



The following Figures 1 through 8 represent typical DC and AC characteristic curves for the 256K static RAM products listed below:

256K Static RAMs

L7C197 — 256K × 1
L7C194 — 64K × 4
L7C195 — 64K × 4
L7C196 — 64K × 4
L7C191 — 64K × 4
L7C192 — 64K × 4
L7C199 — 32K × 8
L7CL199 — 32K × 8

Figure 1. Normalized Supply Current vs Ambient Temperature — I_{CC1}

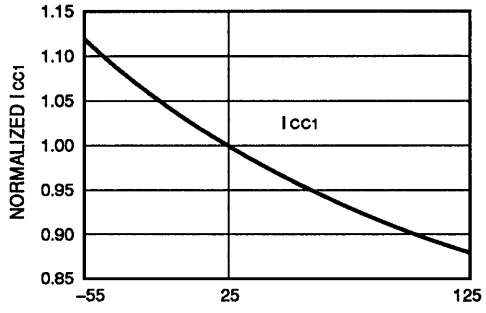


Figure 2. Normalized Supply Current vs Ambient Temperature — I_{CC2}

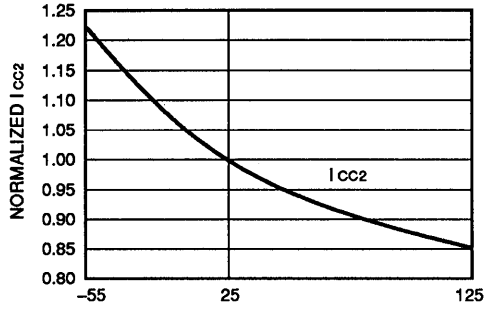


Figure 3. Normalized Supply Current vs Ambient Temperature — I_{CC3}

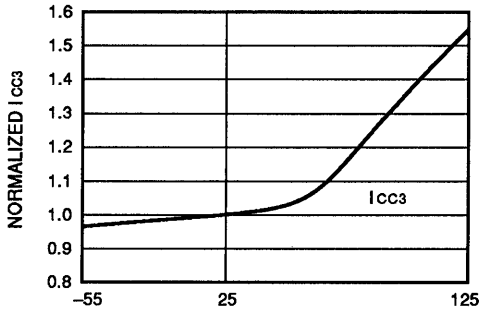


Figure 4. Normalized Supply Current vs Ambient Temperature — I_{CC4}

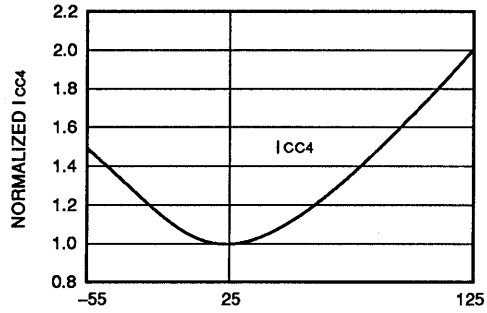


Figure 5. Output Sink Current vs Output Voltage

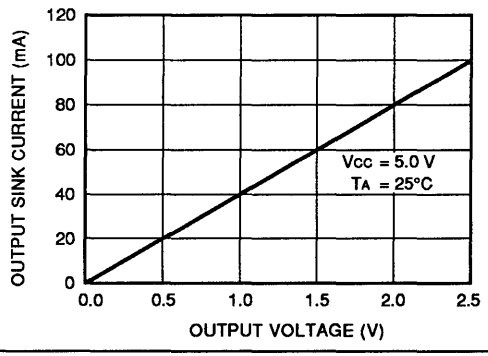


Figure 6. Output Source Current vs Output Voltage

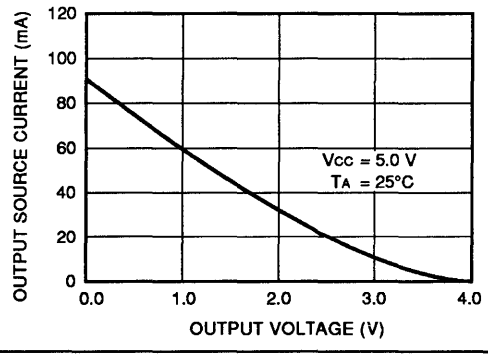


Figure 7. Normalized Access Time vs Supply Voltage

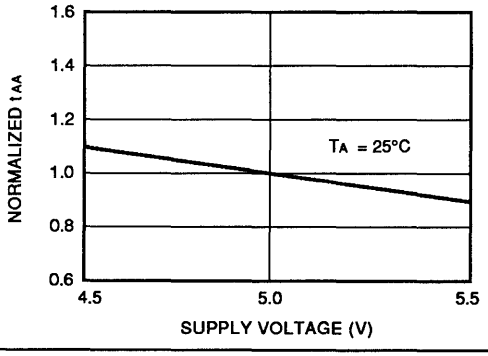


Figure 8. Normalized Access Time vs Ambient Temperature

To Be Determined

16K x 1 Static RAM — L7C167

FEATURES

- 16K × 1 Static RAM with Separate I/O, Chip Select Powerdown
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 8 ns maximum
- Low Power Operation
  Active: 135 mW typical at 35 ns
  Standby: 100 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 6167, Cypress CY7C167
- Package Styles Available:
  - 20-pin Plastic DIP
  - 20-pin Sidebraze, Hermetic DIP
  - 20-pin CerDIP
  - 20-pin Plastic SOIC
  - 20-pin Plastic SOJ
  - 20-pin Ceramic LCC

DESCRIPTION

The **L7C167** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 16,384 words by 1 bit per word. This device is available in seven speeds with maximum access times from 8 ns to 35 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 135 mW (typical) when being operated at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C167 consumes only 15 µW (typical) at 3 V, allowing effective battery backup operation.

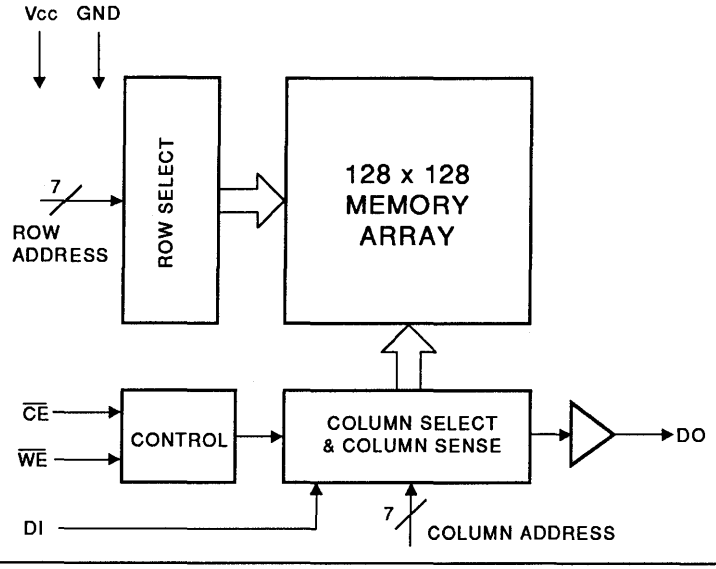
The L7C167 provides asynchronous (unclocked) operation with matching access and cycle times. Active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{13}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C167 can withstand an injection current of up to 200 mA on any pin without damage.

L7C167 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -4.0$ mA, $V_{CC} = 4.5$ V	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0$ mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		20	100	µA
I_{CC4}	V_{CC} Current, Data Retention	$V_{CC} = 3.0$ V (Note 9)		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, $V_{CC} = 5.0$ V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

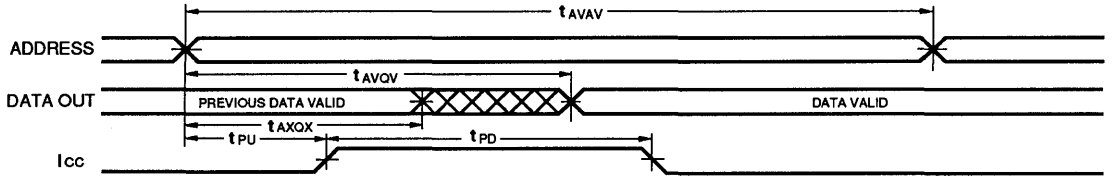
			L7C167-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10	8	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	50	65	85	110	135	150	165	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

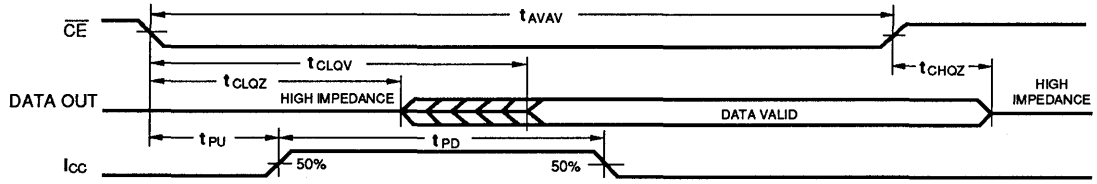
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C167- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Read Cycle Time	35		25		20		15		12		10		8	
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
tAXQX	Address Change to Output Change	3		3		3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

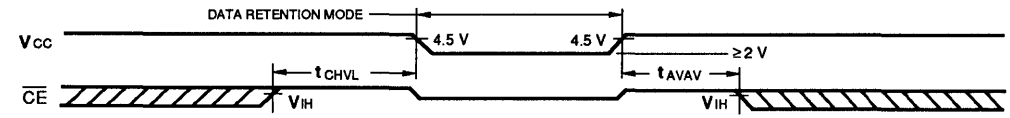
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — $\overline{CE}$ CONTROLLED *(Notes 13, 15)*



DATA RETENTION

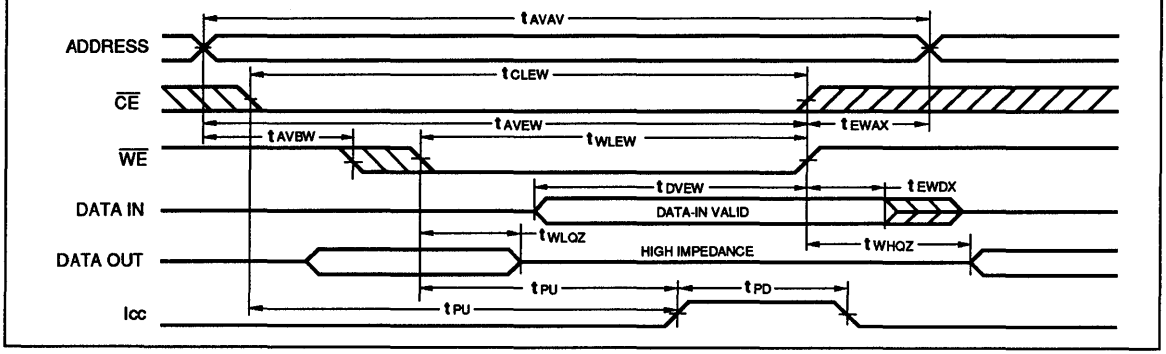


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

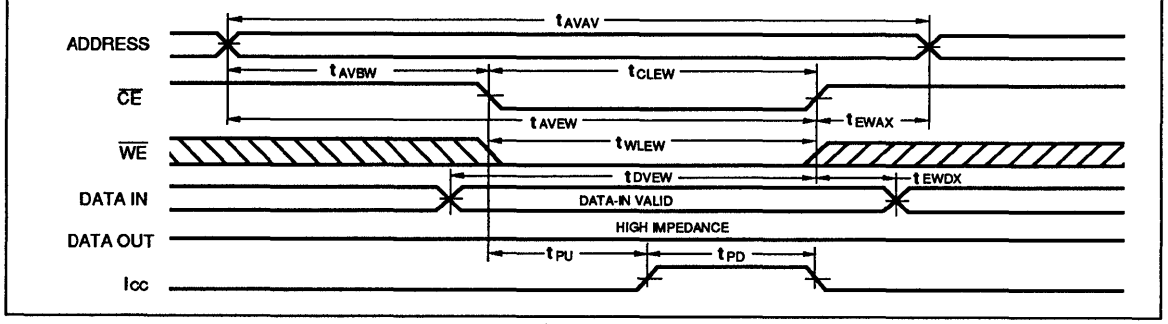
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C167- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8	
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1		1		1	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

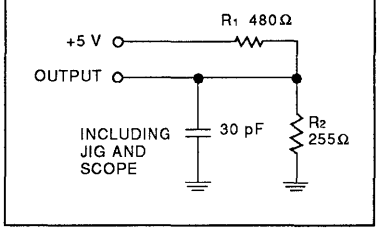


FIGURE 1b.

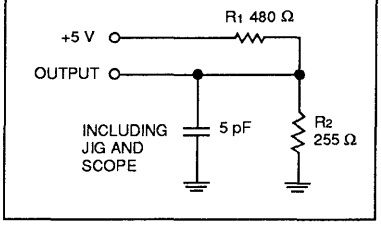
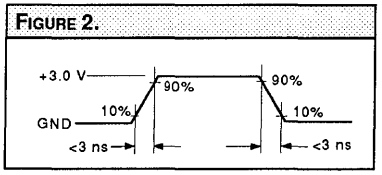
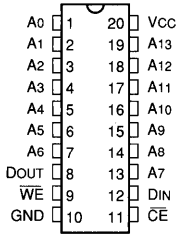


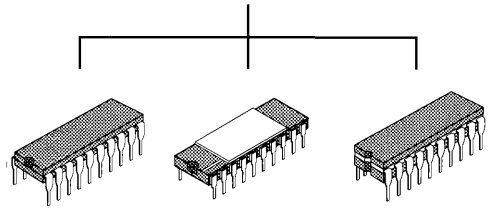
FIGURE 2.



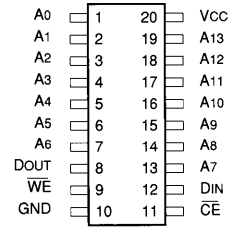
ORDERING INFORMATION

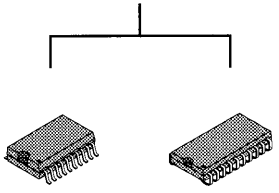
20-pin
(0.3" wide)



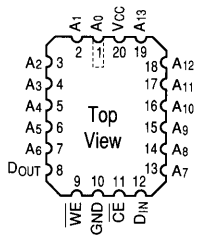


20-pin





20-pin
(290 x 425)



Speed	Plastic DIP (P6)	Sidebraze Hermetic DIP (D7)	CerDIP (C2)	Plastic SOIC (.300"—U3)	Plastic SOJ (.300"—W3)	Ceramic Leadless Chip Carrier (K6)
	0°C to +70°C — Commercial Screening					
35 ns	L7C167PC35	L7C167DC35	L7C167CC35	L7C167UC35	L7C167WC35	L7C167KC35
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	" " 25
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	" " 20
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	" " 15
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12	" " 12
10 ns	" " 10	" " 10	" " 10	" " 10	" " 10	" " 10
8 ns	" " 8	" " 8	" " 8	" " 8	" " 8	" " 8
	–55°C to +125°C — Commercial Screening					
35 ns		L7C167DM35	L7C167CM35			L7C167KM35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — Extended Screening					
35 ns		L7C167DME35	L7C167CME35			L7C167KME35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns		L7C167DMB35	L7C167CMB35			L7C167KMB35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						

FEATURES

- 4K x 4 Static RAM with Common I/O, Output Enable (L7C170 only)
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 8 ns maximum
- Low Power Operation
  Active: 190 mW typical at 35 ns
  Standby: 100 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 6168 and Cypress CY7C168/170
- Package Styles Available:
  - 20/22-pin Plastic DIP
  - 20/22-pin Sidebraze, Hermetic DIP
  - 20/22-pin CerDIP
  - 20-pin Plastic SOIC
  - 20/24-pin Plastic SOJ
  - 20-pin Ceramic LCC

DESCRIPTION

The **L7C168** and **L7C170** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 4096 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C170 version adds an active-low Output Enable control. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 190 mW (typical) when being operated at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C168 and L7C170 consume only 15 µW (typical) at 3 V, allowing effective battery backup operation.

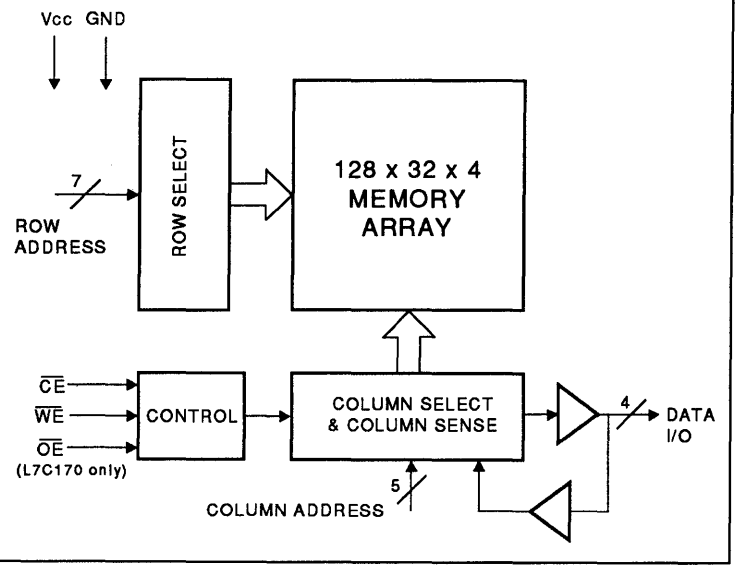
The L7C168 and L7C170 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{11}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data I/O pins within one access time. The I/O pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C168 and L7C170 can withstand an injection current of up to 200 mA on any pin without damage.

L7C168/170 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -4.0$ mA, $V_{CC} = 4.5$ V	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0$ mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		20	100	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

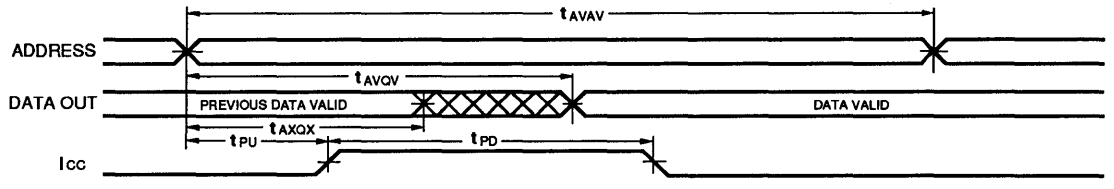
			L7C168/170-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10	8	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	50	65	85	110	135	150	165	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

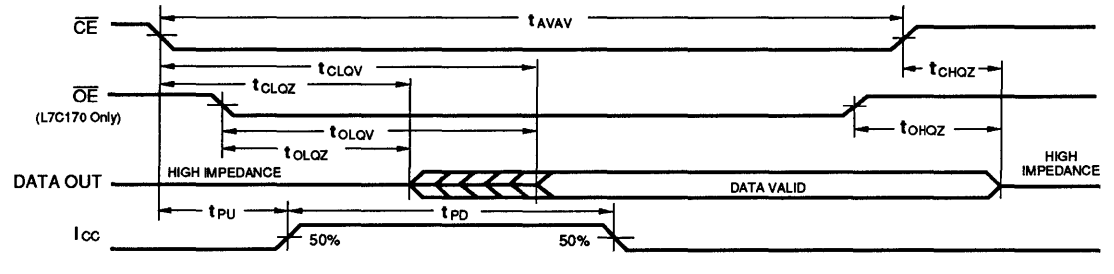
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C168/170- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
t_{AVAV}	Read Cycle Time	35		25		20		15		12		10		8	
t_{AVQV}	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
t_{AXQX}	Address Change to Output Change	3		3		3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
t_{CLQZ}	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8		6		4		4
t_{OLQZ}	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		4
t_{PU}	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
t_{PD}	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
t_{CHVL}	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

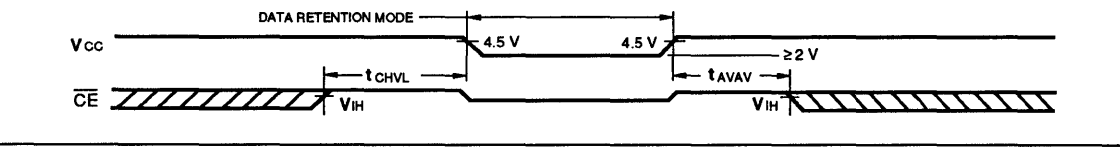
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — CE/OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

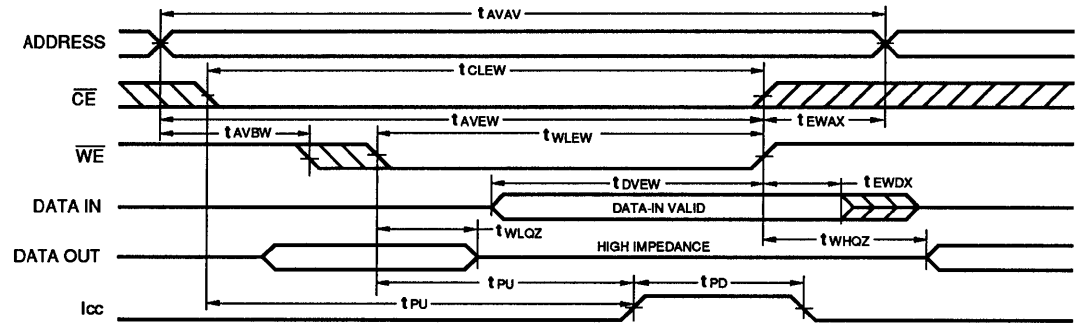


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

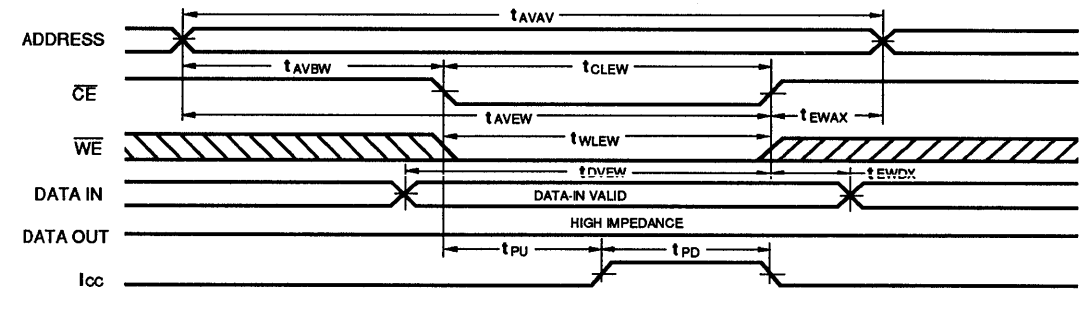
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C168/170- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
t_{AVAV}	Write Cycle Time	25		20		20		15		12		10		8	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
t_{EWDX}	End of Write Cycle to Data Change	1		1		1		1		1		1		1	
t_{WHQZ}	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

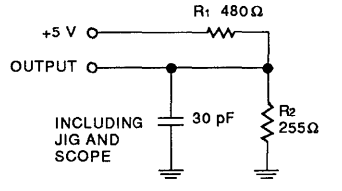


FIGURE 1b.

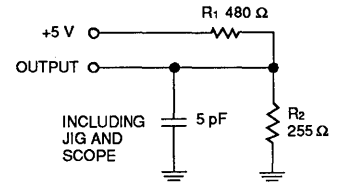
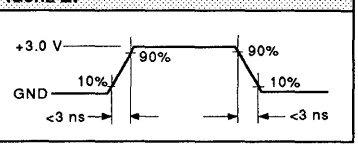
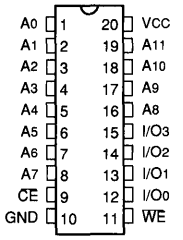


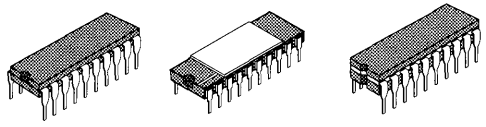
FIGURE 2.



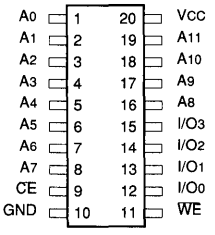
L7C168 — ORDERING INFORMATION

20-pin
(0.3" wide)

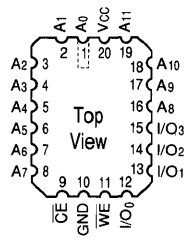




20-pin



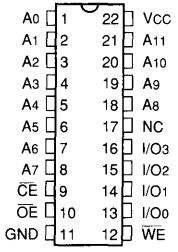
20-pin
(290 x 425)

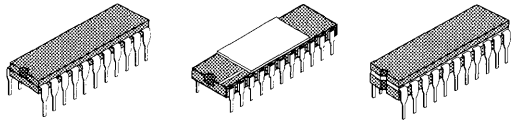


Speed	Plastic DIP (P6)	Sidebraze Hermetic DIP (D7)	CerDIP (C2)	Plastic SOIC (.300"— U3)	Plastic SOJ (.300"— W3)	Ceramic Leadless Chip Carrier (K6)
	0°C to +70°C — Commercial Screening					
35 ns	L7C168PC35	L7C168DC35	L7C168CC35	L7C168UC35	L7C168WC35	L7C168KC35
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	" " 25
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	" " 20
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	" " 15
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12	" " 12
10 ns	" " 10	" " 10	" " 10	" " 10	" " 10	" " 10
8 ns	" " 8	" " 8	" " 8	" " 8	" " 8	" " 8
	–55°C to +125°C — Commercial Screening					
35 ns		L7C168DM35	L7C168CM35			L7C168KM35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — Extended Screening					
35 ns		L7C168DME35	L7C168CME35			L7C168KME35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns		L7C168DMB35	L7C168CMB35			L7C168KMB35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						

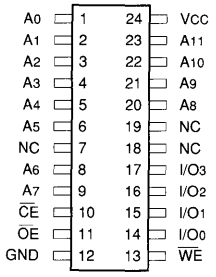
L7C170 — ORDERING INFORMATION

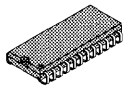
22-pin
(0.3" wide)





24-pin





Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOJ (.300" — W1)		
	0°C to +70°C — Commercial Screening					
35 ns	L7C170PC35	L7C170DC35	L7C170CC35	L7C170WC35		
25 ns	" " 25	" " 25	" " 25	" " 25		
20 ns	" " 20	" " 20	" " 20	" " 20		
15 ns	" " 15	" " 15	" " 15	" " 15		
12 ns	" " 12	" " 12	" " 12	" " 12		
10 ns	" " 10	" " 10	" " 10	" " 10		
8 ns	" " 8	" " 8	" " 8	" " 8		
	–55°C to +125°C — Commercial Screening					
35 ns		L7C170DM35	L7C170CM35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns		" " 15	" " 15			
12 ns		" " 12	" " 12			
10 ns		" " 10	" " 10			
8 ns						
	–55°C to +125°C — Extended Screening					
35 ns		L7C170DME35	L7C170CME35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns		" " 15	" " 15			
12 ns		" " 12	" " 12			
10 ns		" " 10	" " 10			
8 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns		L7C170DMB35	L7C170CMB35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns		" " 15	" " 15			
12 ns		" " 12	" " 12			
10 ns		" " 10	" " 10			
8 ns						

FEATURES

- 4K x 4 Static RAM with Separate I/O, Transparent Write (L7C171), or High Impedance Write (L7C172)
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 8 ns maximum
- Low Power Operation
  Active: 190 mW typical at 35 ns
  Standby: 100 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 71681/71682, Cypress CY7C171/172
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin CerDIP
  - 24-pin SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C171** and **L7C172** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 4096 words by 4 bits per word. Data In and Data Out are separate. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 190 mW (typical) when operating at 35 ns. Dissipation drops to75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C171 and L7C172 consume only 15 µW (typical) at 3 V, allowing effective battery backup operation.

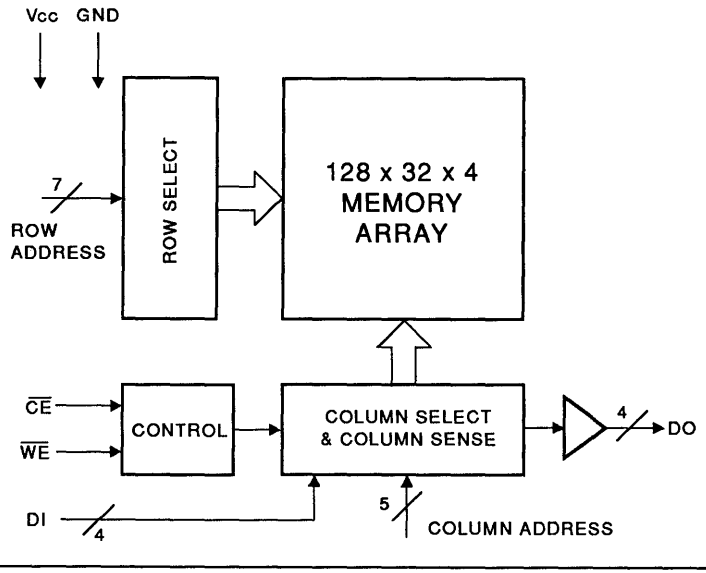
The L7C171 and L7C172 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output bus simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{11}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is low (L7C172 only) or $\overline{CE}$ is high.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C171 and L7C172 can withstand an injection current of up to 200 mA on any pin without damage.

L7C171/172 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		20	100	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

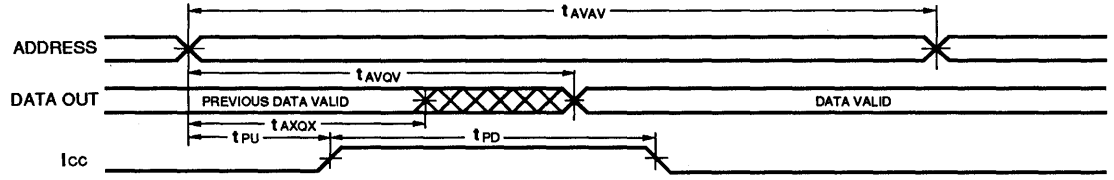
			L7C171/172-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10	8	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	50	65	85	110	135	150	165	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

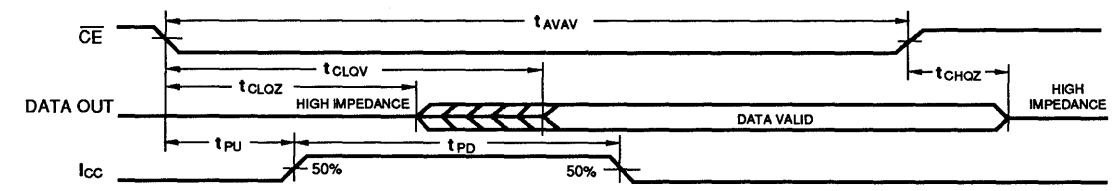
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C171/172- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
t_{AVAV}	Read Cycle Time	35		25		20		15		12		10		8	
t_{AVQV}	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
t_{AXQX}	Address Change to Output Change	3		3		3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
t_{CLQZ}	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
t_{PU}	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
t_{PD}	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
t_{CHVL}	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

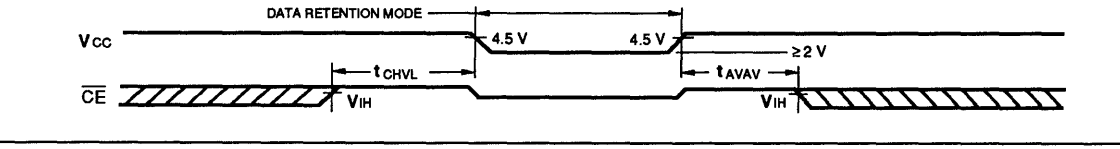
Read Cycle — Address Controlled (Notes 13, 14)



Read Cycle — $\overline{CE}$ Controlled (Notes 13, 15)



Data Retention

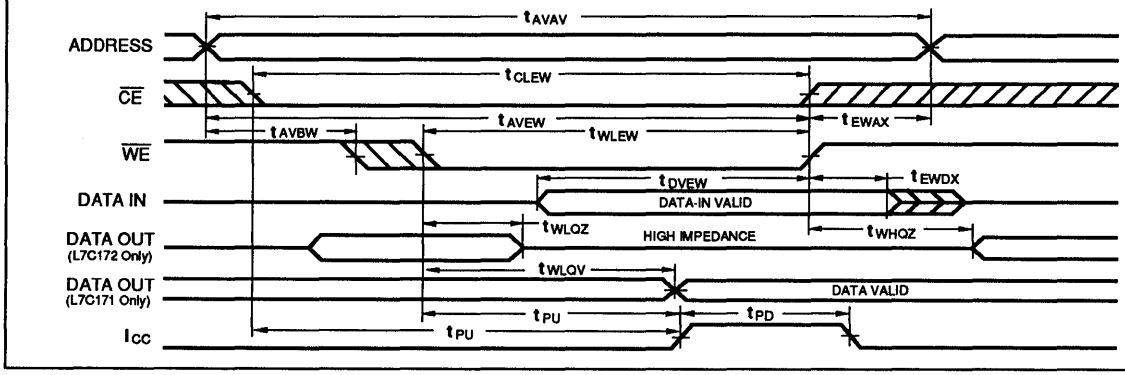


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

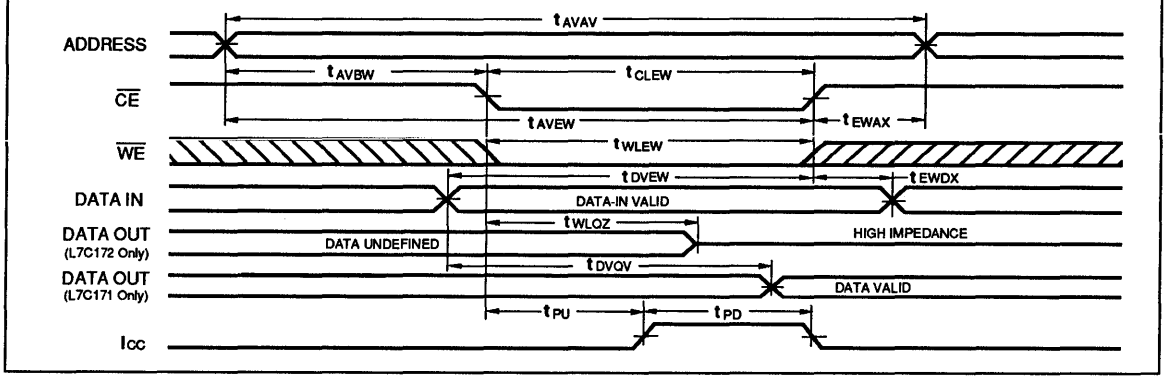
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C171/172- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8	
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1		1		1	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3
tWLQV	Write Enable Low to Output Valid		30		20		15		15		12		10		8
tDVQV	Data Valid to Output Valid		30		20		15		15		12		10		8

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

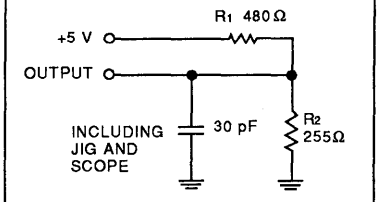


FIGURE 1b.

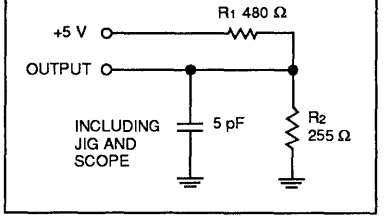
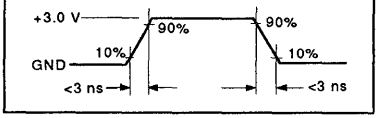
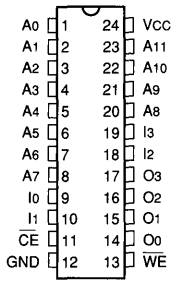


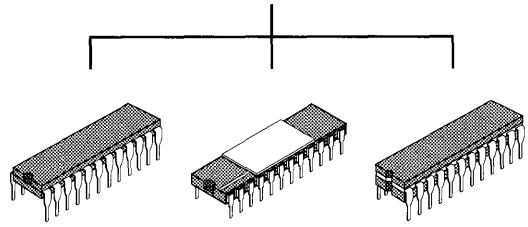
FIGURE 2.



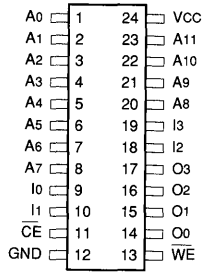
ORDERING INFORMATION

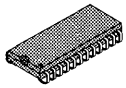
24-pin
(0.3" wide)



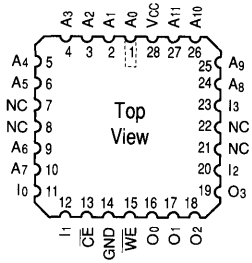


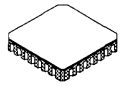
24-pin





28-pin
(450 x 450)





Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic SOJ (.300" — W1)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C171PC or L7C172PC 35 25 20 15 12 10 8	L7C171DC or L7C172DC 35 25 20 15 12 10 8	L7C171CC or L7C172CC 35 25 20 15 12 10 8	L7C171WC or L7C172WC 35 25 20 15 12 10 8	L7C171KC or L7C172KC 35 25 20 15 12 10 8
	–55°C to +125°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C171DM or L7C172DM 35 25 20 15 12 10	L7C171DM or L7C172DM 35 25 20 15 12 10	35 25 20 15 12 10	L7C171KM or L7C172KM 35 25 20 15 12 10
	–55°C to +125°C — Extended Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C171DME or L7C172DME 35 25 20 15 12 10	L7C171DME or L7C172DME 35 25 20 15 12 10	35 25 20 15 12 10	L7C171KME or L7C172KME 35 25 20 15 12 10
	–55°C to +125°C — MIL-STD-883 Compliant				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C171DMB or L7C172DMB 35 25 20 15 12 10	L7C171DMB or L7C172DMB 35 25 20 15 12 10	35 25 20 15 12 10	L7C171KMB or L7C172KMB 35 25 20 15 12 10

2K x 8 Static RAM (Low Power) L6116/L6116L

FEATURES

- 2K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 10 ns maximum
- Low Power Operation
  Active:
  250 mW (L6116) typical at 35 ns
  Standby (typical):
  100 µW (L6116)
  50 µW (L6116L)
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT6116, Cypress CY7C128/CY6116
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin CerDIP
  - 24-pin Plastic SOIC
  - 24-pin Plastic SOJ
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L6116** and **L6116L** are high-performance, low-power CMOS static RAM. The storage circuitry is organized as 2048 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in six speeds with maximum access times from 10 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L6116 is 250 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) for the L6116 and 60 mW (typical) for the L6116L when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L6116 and L6116L consume only 15 µW and 6 µW (typical) respectively at 3 V, allowing effective battery backup operation.

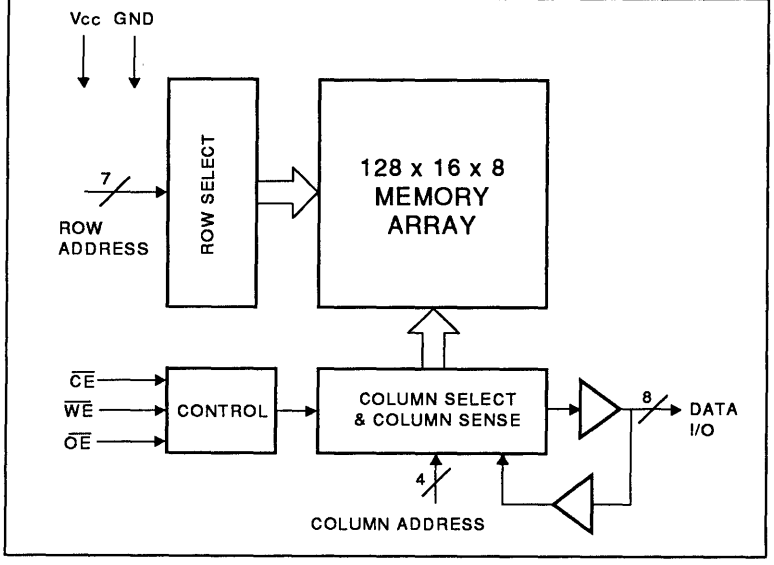
The L6116 and L6116L provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{10}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high, or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L6116 and L6116L can withstand an injection current of up to 200 mA on any pin without damage.

L6116/L6116L Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

			L6116			L6116L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10		+10	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–350			–350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30		12	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		20	100		10	30	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		5	50		2	10	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

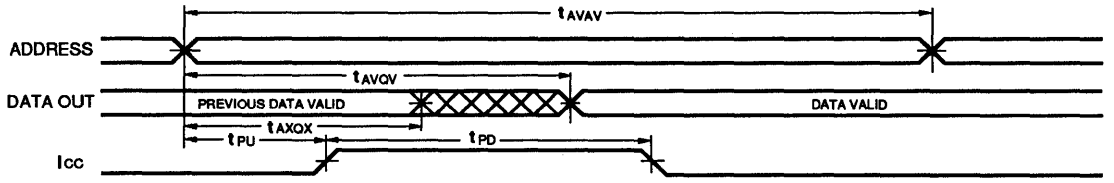
			L6116-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10		Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	75	100	125	160	200	220		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

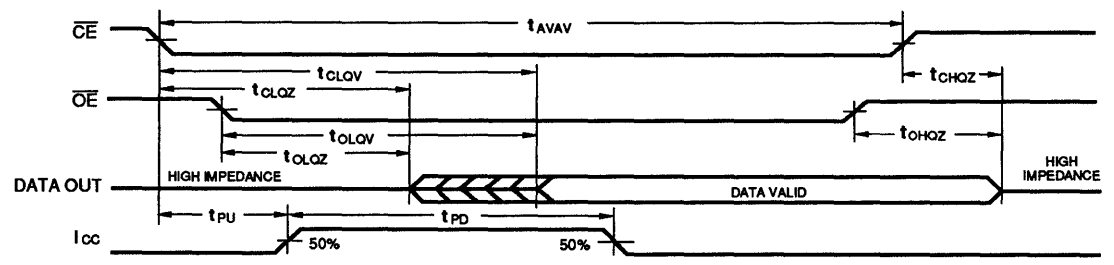
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L6116/L6116L- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max		
tAVAV	Read Cycle Time	35		25		20		15		12		10			
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		
tAXQX	Address Change to Output Change	3		3		3		3		3		3			
tCLQV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3			
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		5		
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0			

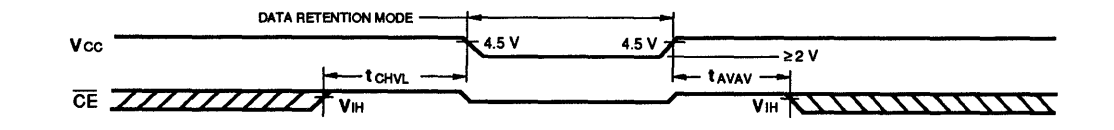
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — CE/OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

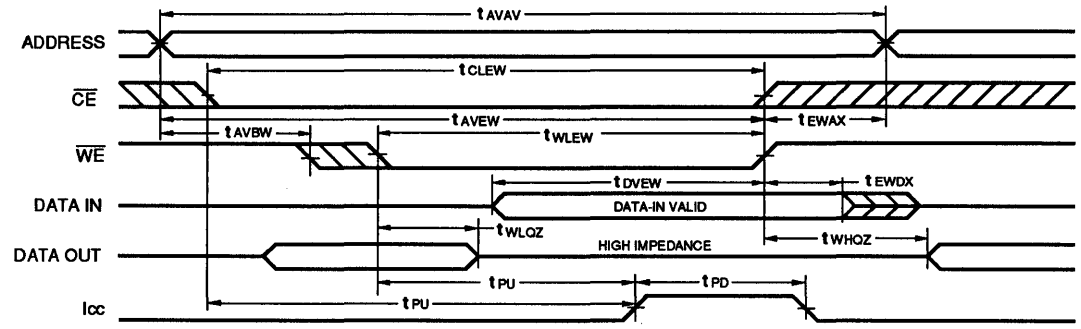


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

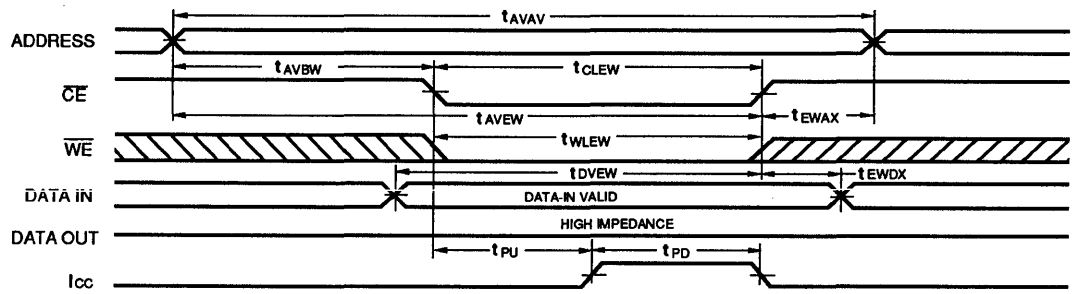
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L6116/L6116L- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12		10			
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0			
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8			
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5			
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1		1			
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0			
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \leq VIL$, $\overline{WE} \leq VIL$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \geq VIH$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = VCC$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be $\geq VCC - 0.2$ V. For all other inputs $VIN \geq VCC - 0.2$ V or $VIN \leq 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

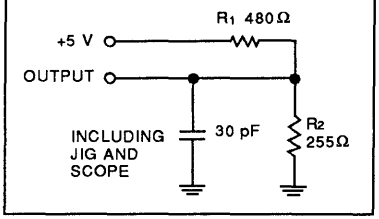


FIGURE 1b.

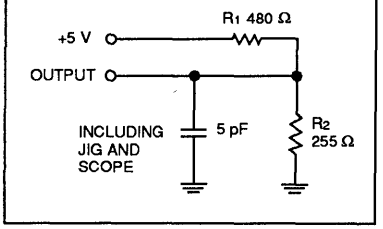
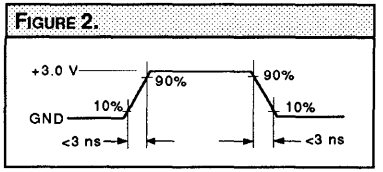
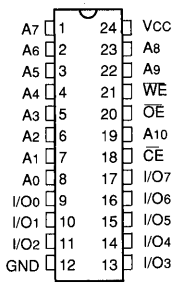


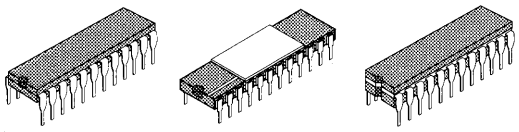
FIGURE 2.



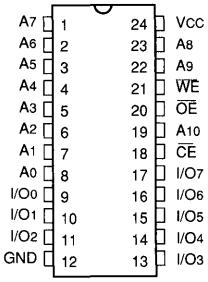
ORDERING INFORMATION

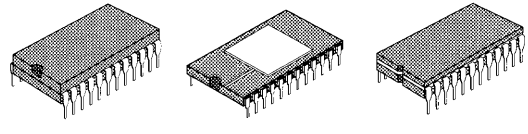
24-pin
(0.3" wide)





24-pin
(0.6" wide)

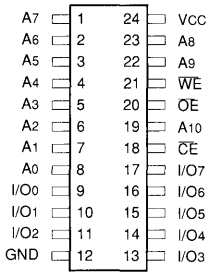




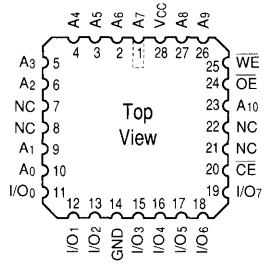
Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic DIP (P1)	Sidebraze Hermetic DIP (D1)	CerDIP (C4)
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L6116PC / L6116LPC: 35, 25, 20, 15, 12, 10	L6116DC / L6116LDC: 35, 25, 20, 15, 12, 10	L6116CC / L6116LCC: 35, 25, 20, 25, 12, 10	L6116NC / L6116LNC: 35, 25, 20, 15, 12, 10	L6116HC / L6116LHC: 35, 25, 20, 15, 12, 10	L6116IC / L6116LIC: 35, 25, 20, 25, 12, 10
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L6116DM / L6116LDM: 35, 35, 20, 15, 12	L6116CM / L6116LCM: 35, 25, 20, 15, 12		L6116HM / L6116LHM: 35, 35, 20, 15, 12	L6116IM / L6116LIM: 35, 25, 20, 15, 12
	–55°C to +125°C — Extended Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L6116DME / L6116LDME: 35, 35, 20, 15, 12	L6116CME / L6116LCME: 35, 25, 20, 15, 12		L6116HME / L6116LHME: 35, 35, 20, 15, 12	L6116IME / L6116LIME: 35, 25, 20, 15, 12
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L6116DMB / L6116LDMB: 35, 35, 20, 15, 12	L6116CMB / L6116LCMB: 35, 25, 20, 15, 12		L6116HMB / L6116LHMB: 35, 35, 20, 15, 12	L6116IMB / L6116LIMB: 35, 25, 20, 15, 12

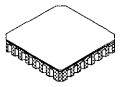
ORDERING INFORMATION

24-pin

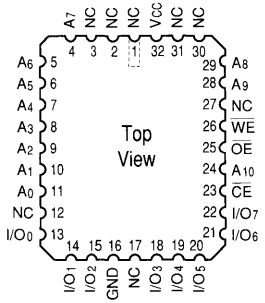


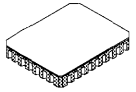
28-pin
(450 x 450)





32-pin
(450 x 550)





Speed	Plastic SOIC (.300"— U1)	Plastic SOJ (.300"— W1)	Ceramic Leadless Chip Carrier (K1)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L6116UC / L6116LUC — 35, 25, 20, 15, 12, 10	L6116WC / L6116LWC — 35, 25, 20, 15, 12, 10	L6116KC / L6116LKC — 35, 25, 20, 15, 12, 10	L6116TC / L6116LTC — 35, 25, 20, 15, 12, 10
	–55°C to +125°C — Commercial Screening			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L6116KM / L6116LKM — 35, 25, 20, 15, 12	L6116TM / L6116LTM — 35, 25, 20, 15, 12
	–55°C to +125°C — Extended Screening			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L6116KME / L6116LKME — 35, 25, 20, 15, 12	L6116TME / L6116LTME — 35, 25, 20, 15, 12
	–55°C to +125°C — MIL-STD-883 Compliant			
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L6116KMB / L6116LKMB — 35, 25, 20, 15, 12	L6116TMB / L6116LTMB — 35, 25, 20, 15, 12

64K x 1 Static RAM — L7C187

FEATURES

- 64K × 1 Static RAM with Separate I/O, Chip Select Powerdown
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 8 ns maximum
- Low Power Operation
  Active: 135 mW typical at 35 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 7187, Cypress CY7C187
- Package Styles Available:
  - 22-pin Plastic DIP
  - 22-pin Sidebraze, Hermetic DIP
  - 22-pin CerDIP
  - 24-pin Plastic SOIC
  - 24-pin Plastic SOJ
  - 22-pin Ceramic LCC

DESCRIPTION

The **L7C187** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 65,536 words by 1 bit per word. This device is available in seven speeds with maximum access times from 8 ns to 35 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 135 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C187 consumes only 30 µW (typical) at 3 V, allowing effective battery backup operation.

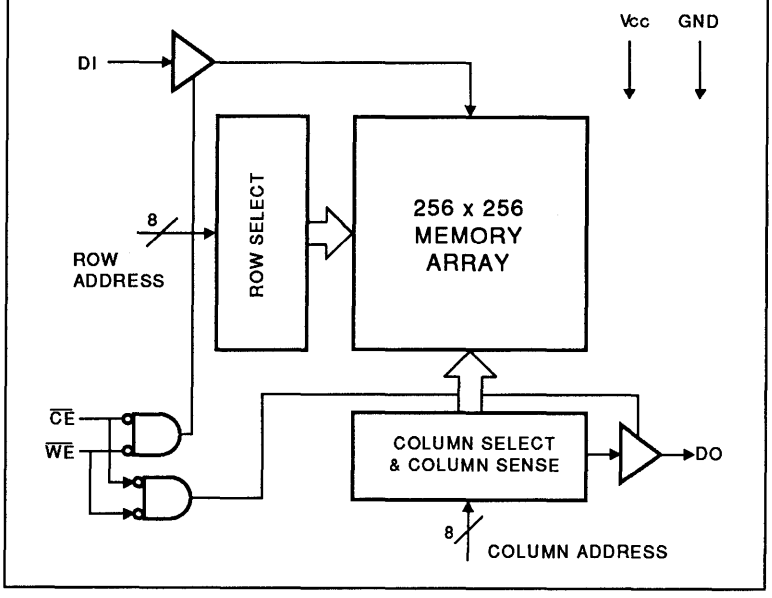
The L7C187 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C187 can withstand an injection current of up to 200 mA on any pin without damage.

L7C187 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	250	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

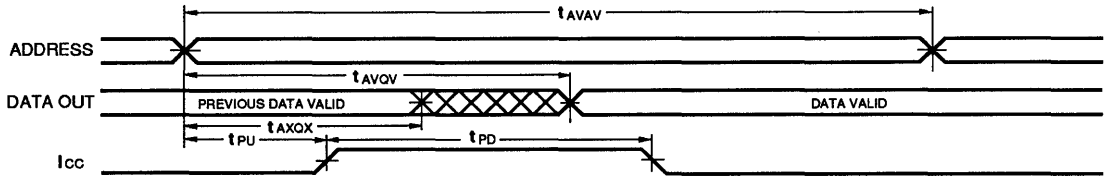
			L7C187-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10	8	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	75	100	125	160	190	205	225	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

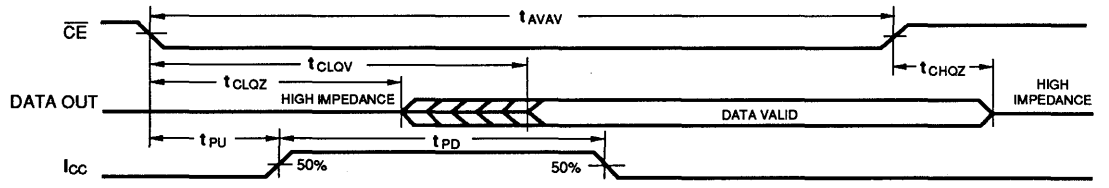
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C187- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Read Cycle Time	35		25		20		15		12		10		8	
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
tAXQX	Address Change to Output Change	3		3		3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

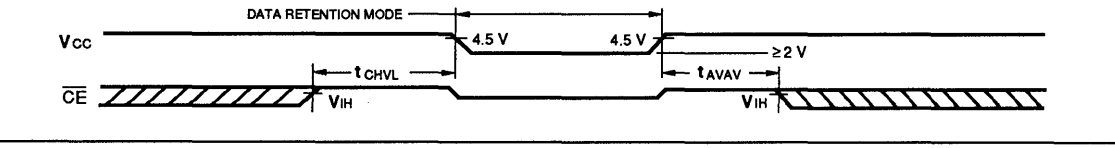
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — $\overline{CE}$ CONTROLLED *(Notes 13, 15)*



DATA RETENTION

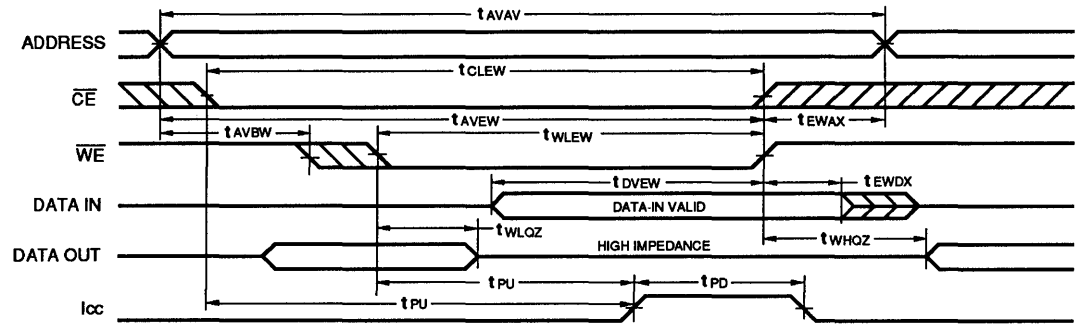


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

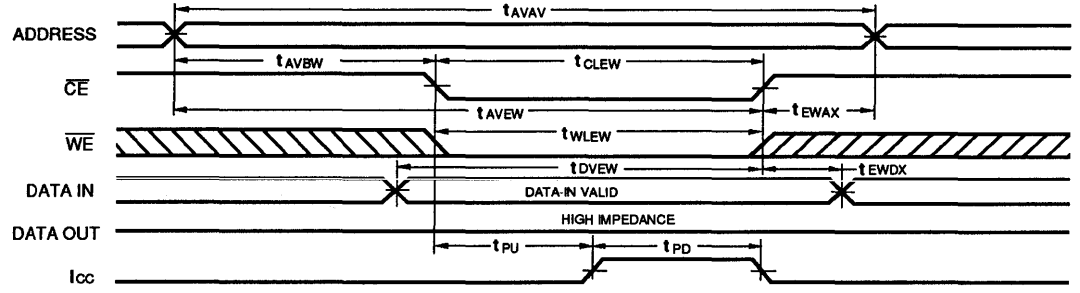
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C187- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
t_{AVAV}	Write Cycle Time	25		20		20		15		12		10		8	
t_{CLEW}	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.2 V. For all other inputs VIN ≥ VCC – 0.2 V or VIN ≤ 0.2 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

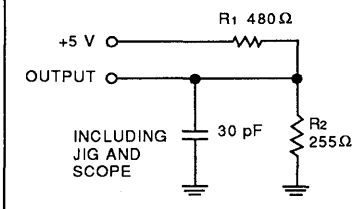


FIGURE 1b.

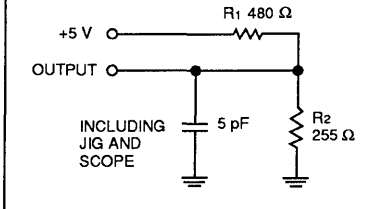
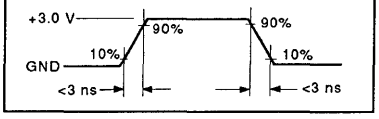
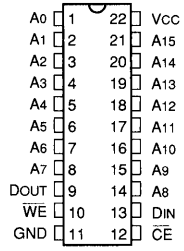


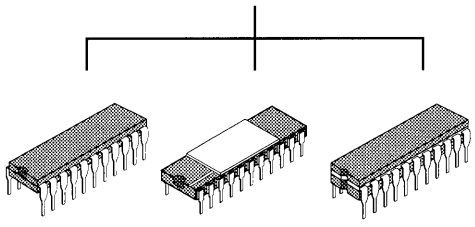
FIGURE 2.



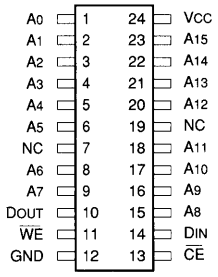
ORDERING INFORMATION

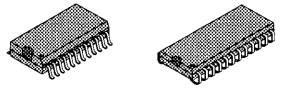
22-pin
(0.3" wide)



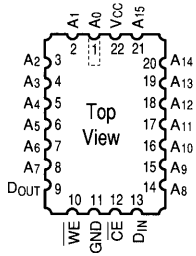


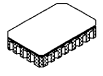
24-pin





22-pin
(290 x 490)





Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOIC (.300"— U1)	Plastic SOJ (.300"— W1)	Ceramic Leadless Chip Carrier (K4)
	0°C to +70°C — COMMERCIAL SCREENING					
35 ns	L7C187PC35	L7C187DC35	L7C187CC35	L7C187UC35	L7C187WC35	L7C187KC35
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	" " 25
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	" " 20
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	" " 15
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12	" " 12
10 ns	" " 10	" " 10	" " 10	" " 10	" " 10	" " 10
8 ns	" " 8	" " 8	" " 8	" " 8	" " 8	" " 8
	–55°C to +125°C — COMMERCIAL SCREENING					
35 ns		L7C187DM35	L7C187CM35			L7C187KM35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — EXTENDED SCREENING					
35 ns		L7C187DME35	L7C187CME35			L7C187KME35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — MIL-STD-883 COMPLIANT					
35 ns		L7C187DMB35	L7C187CMB35			L7C187KMB35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						

FEATURES

- 16K x 4 Static RAM with Common I/O
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 8 ns maximum
- Low Power Operation
  Active: 210 mW typical at 35 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 7188/7198, Cypress CY7C164/166
- Package Styles Available:
  - 22/24-pin Plastic DIP
  - 22/24-pin Sidebraze, Hermetic DIP
  - 22/24-pin CerDIP
  - 24-pin Plastic SOIC
  - 24-pin Plastic SOJ
  - 22-pin Ceramic LCC
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C164, L7C165,** and **L7C166** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C164 has a single active-low Chip Enable. The L7C165 has two Chip Enables and a separate Output Enable. The L7C166 has a single Chip Enable and an Output Enable. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 210 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C164, L7C165, and L7C166 consume only 30 µW (typical) at 3 V, allowing effective battery backup operation.

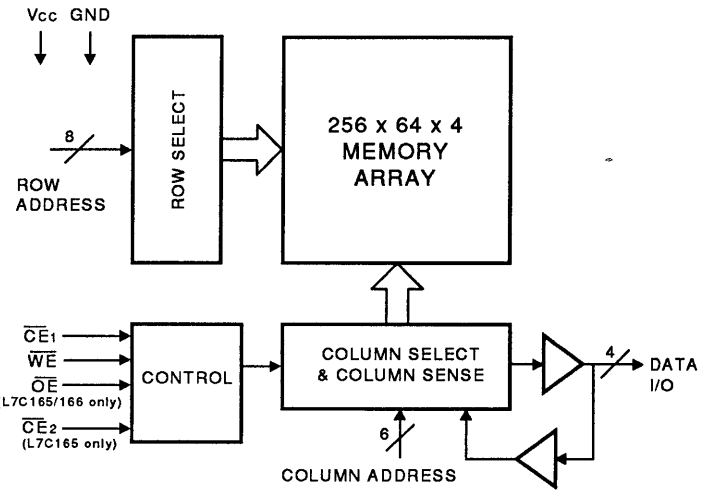
The L7C164, L7C165, and L7C166 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{13}. For the L7C164 and L7C166, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}_1$ low while $\overline{WE}$ remains high. For the L7C165, both $\overline{CE}_1$ and $\overline{CE}_2$ must be low. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C164, L7C165, and L7C166 can withstand an injection current of up to 200 mA on any pin without damage.

L7C164/165/166 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -4.0$ mA, $V_{CC} = 4.5$ V	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0$ mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	−10		+10	µA
I_{OS}	Output Short Current	$V_{OUT} = GND$, $V_{CC} = Max$ (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500	µA
I_{CC4}	V_{CC} Current,Data Retention	$V_{CC} = 3.0$ V (Note 9)		10	250	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, $V_{CC} = 5.0$ V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

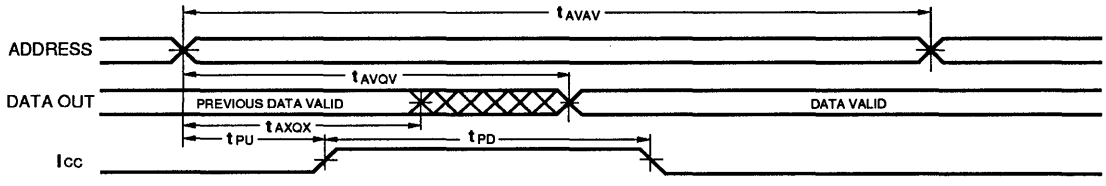
			L7C164/165/166-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10	8	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	75	100	125	160	190	205	225	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

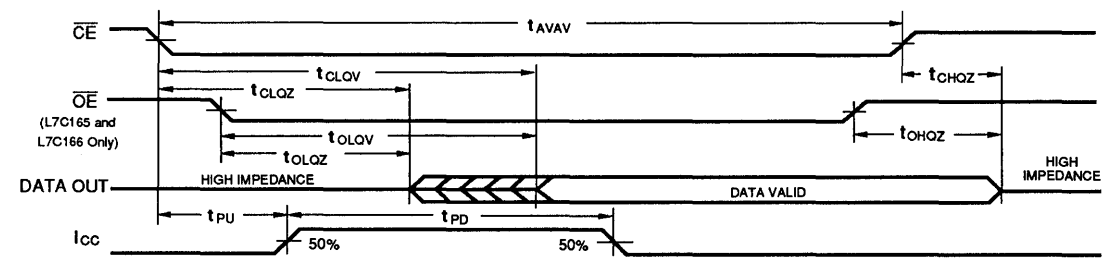
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C164/165/166- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
t_{AVAV}	Read Cycle Time	35		25		20		15		12		10		8	
t_{AVQV}	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
t_{AXQX}	Address Change to Output Change	3		3		3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
t_{CLQZ}	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
t_{OLQV}	Output Enable Low to Output Valid		15		12		10		8		6		4		4
t_{OLQZ}	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		4
t_{PU}	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
t_{PD}	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
t_{CHVL}	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

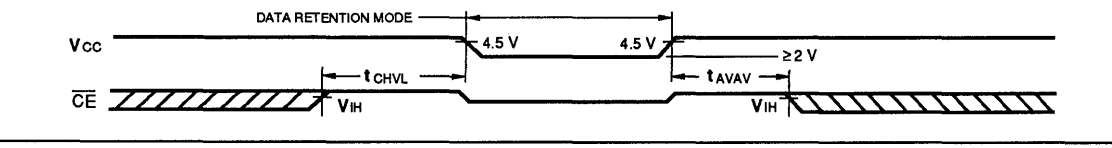
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *(Notes 13, 15)*



DATA RETENTION

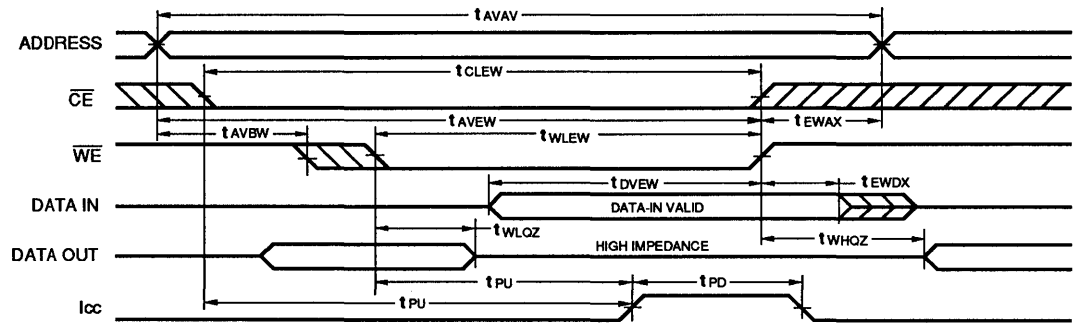


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

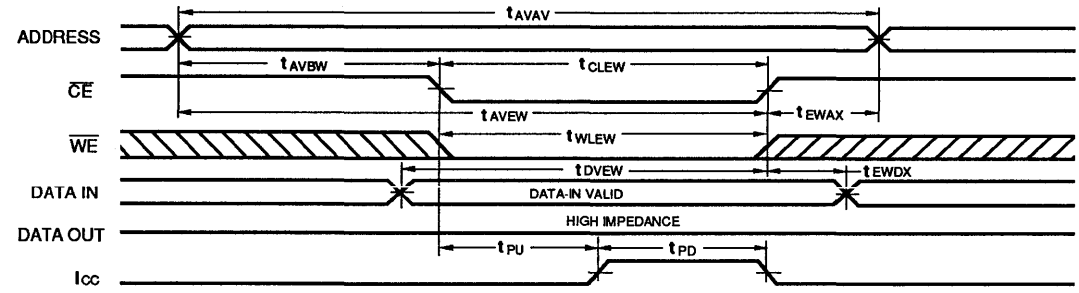
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C164/165/166- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8	
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}^* \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}^* \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}^* = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}^*$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}^*$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}^*$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}^*$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}^*$ going low, the output remains in a high impedance state.

18. If $\overline{CE}^*$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}^*$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}^*$ active).

c. Transition on any address line ($\overline{CE}^*$ active).

d. Transition on any data line ($\overline{CE}^*$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}^*$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

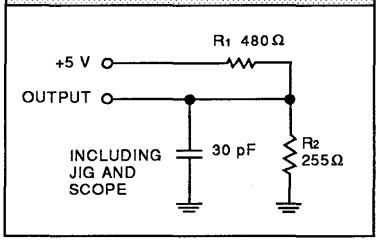


FIGURE 1b.

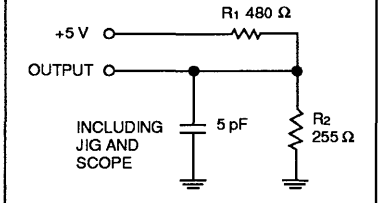
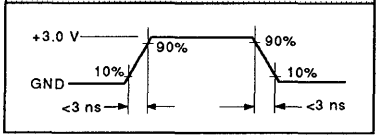


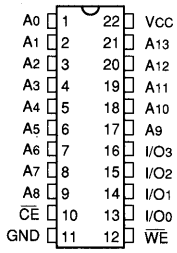
FIGURE 2.

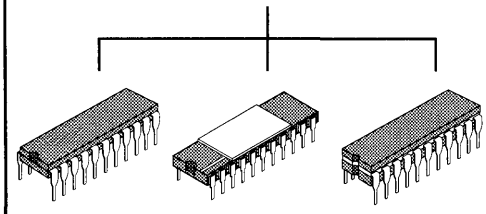


* For the L7C165, $\overline{CE}$ refers to the logical AND of $\overline{CE}_1$ and $\overline{CE}_2$.

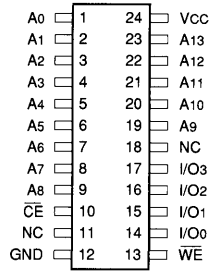
L7C164 — ORDERING INFORMATION

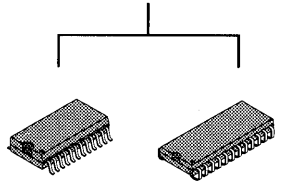
22-pin
(0.3" wide)



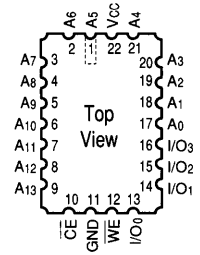


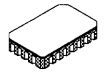
24-pin





22-pin
(290 x 490)

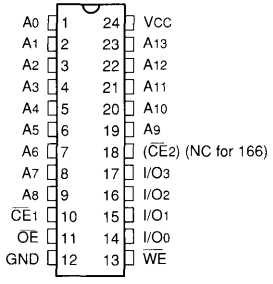


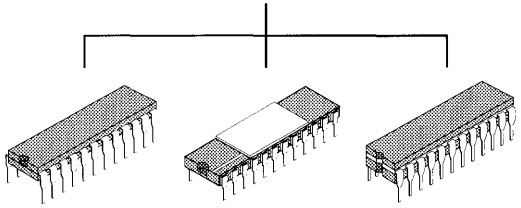


Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOIC (.300"— U1)	Plastic SOJ (.300"— W1)	Ceramic Leadless Chip Carrier (K4)
	0°C to +70°C — Commercial Screening					
35 ns	L7C164PC35	L7C164DC35	L7C164CC35	L7C164UC35	L7C164WC35	L7C164KC35
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	" " 25
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	" " 20
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	" " 15
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12	" " 12
10 ns	" " 10	" " 10	" " 10	" " 10	" " 10	" " 10
8 ns	" " 8	" " 8	" " 8	" " 8	" " 8	" " 8
	–55°C to +125°C — Commercial Screening					
35 ns		L7C164DM35	L7C164CM35			L7C164KM35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — Extended Screening					
35 ns		L7C164DME35	L7C164CME35			L7C164KME35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns		L7C164DMB35	L7C164CMB35			L7C164KMB35
25 ns		" " 25	" " 25			" " 25
20 ns		" " 20	" " 20			" " 20
15 ns		" " 15	" " 15			" " 15
12 ns		" " 12	" " 12			" " 12
10 ns		" " 10	" " 10			" " 10
8 ns						

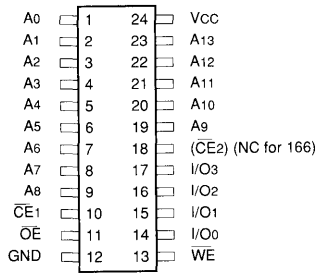
L7C165/166 — ORDERING INFORMATION

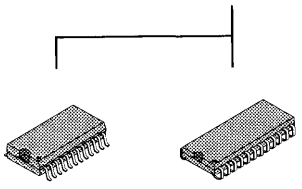
24-pin
(0.3" wide)





24-pin

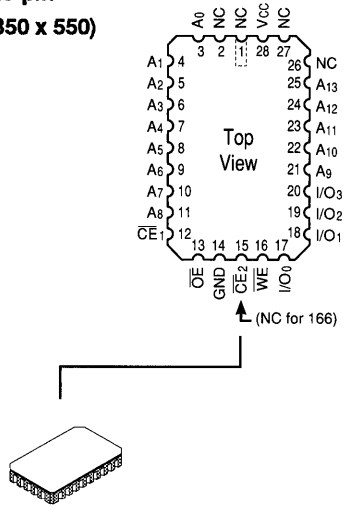




Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic SOIC (.300"— U1)	Plastic SOJ (.300"— W1)	
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C165PC or L7C166PC — 35, 25, 20, 15, 12, 10, 8	L7C165DC or L7C166DC — 35, 25, 20, 15, 12, 10, 8	L7C165CC or L7C166CC — 35, 25, 20, 15, 12, 10, 8	L7C165UC or L7C166UC — 35, 25, 20, 15, 12, 10, 8	L7C165WC or L7C166WC — 35, 25, 20, 15, 12, 10, 8	
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C165DM or L7C166DM — 35, 25, 20, 15, 12, 10	L7C165CM or L7C166CM — 35, 25, 20, 15, 12, 10			
	–55°C to +125°C — Extended Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C165DME or L7C166DME — 35, 25, 20, 15, 12, 10	L7C165CME or L7C166CME — 35, 25, 20, 15, 12, 10			
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C165DMB or L7C166DMB — 35, 25, 20, 15, 12, 10	L7C165CMB or L7C166CMB — 35, 25, 20, 15, 12, 10			

L7C165/166 — ORDERING INFORMATION

28-pin
(350 x 550)



Speed	Ceramic Leadless Chip Carrier (K5)					
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C165KC or L7C166KC — 35, 25, 20, 15, 12, 10, 8					
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C165KM or L7C166KM — 35, 25, 20, 15, 12, 10					
	–55°C to +125°C — Extended Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C165KME or L7C166KME — 35, 25, 20, 15, 12, 10					
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C165KMB or L7C166KMB — 35, 25, 20, 15, 12, 10					

FEATURES

- 16K × 4 Static RAM with Separate I/O, Transparent Write (L7C161), or High Impedance Write (L7C162)
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 8 ns maximum
- Low Power Operation
  Active: 210 mW typical at 35 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 71981/71982, Cypress CY7C161/162
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin CerDIP
  - 28-pin Plastic SOIC
  - 28-pin Plastic SOJ
  - 28-pin Ceramic LCC

DESCRIPTION

The **L7C161** and **L7C162** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 16,384 words by 4 bits per word. Data In and Data Out are separate. These devices are available in seven speeds with maximum access times from 8 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 210 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C161 and L7C162 consume only 30 µW (typical) at 3 V, allowing effective battery backup operation.

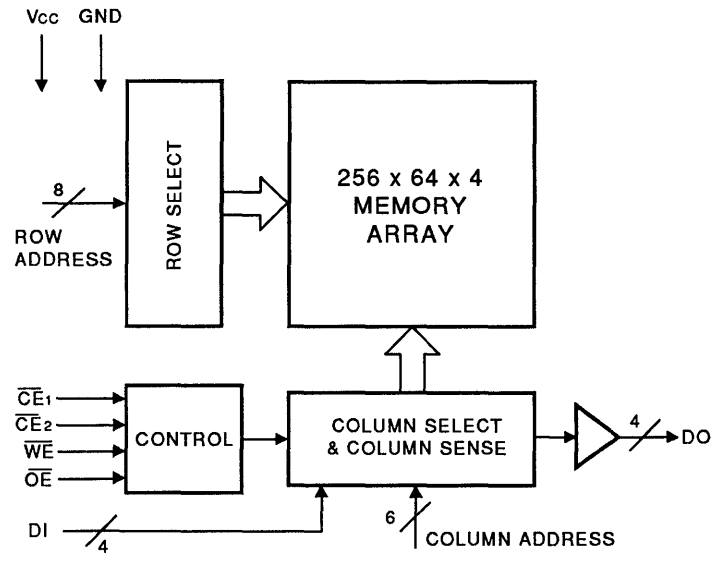
The L7C161 and L7C162 provide asynchronous (unclocked) operation with matching access and cycle times. Two active-low Chip Enables and a three-state bus output with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{13}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}_1$ and $\overline{CE}_2$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is low (L7C162 only) or $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{OE}$ is high.

Writing to an addressed location is accomplished when the active-low $\overline{CE}_1$ and $\overline{CE}_2$ and $\overline{WE}$ inputs are all low. Any of these signals may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C161 and L7C162 can withstand an injection current of up to 200 mA on any pin without damage.

L7C161/162 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	−10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	250	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

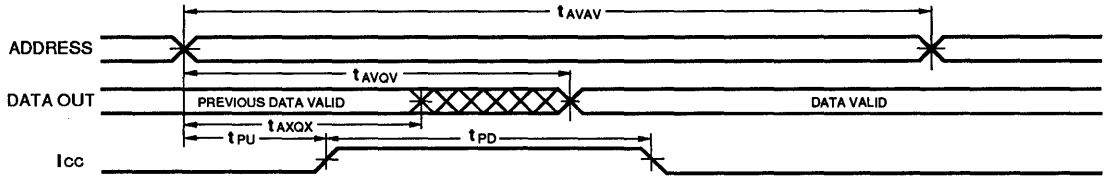
			L7C161/162-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10	8	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	75	100	125	160	190	205	225	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

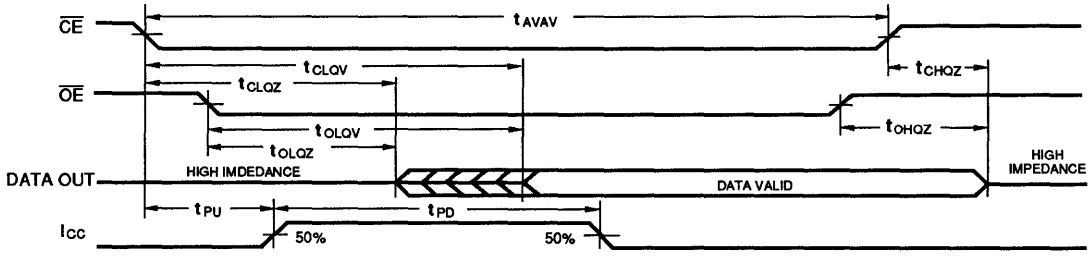
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C161/162- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Read Cycle Time	35		25		20		15		12		10		8	
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		8
tAXQX	Address Change to Output Change	3		3		3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12		10		8
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5		4		4
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		5		4
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		4
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		15
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0		0		0	

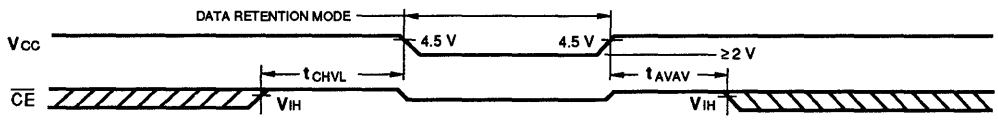
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *(Notes 13, 15)*



DATA RETENTION

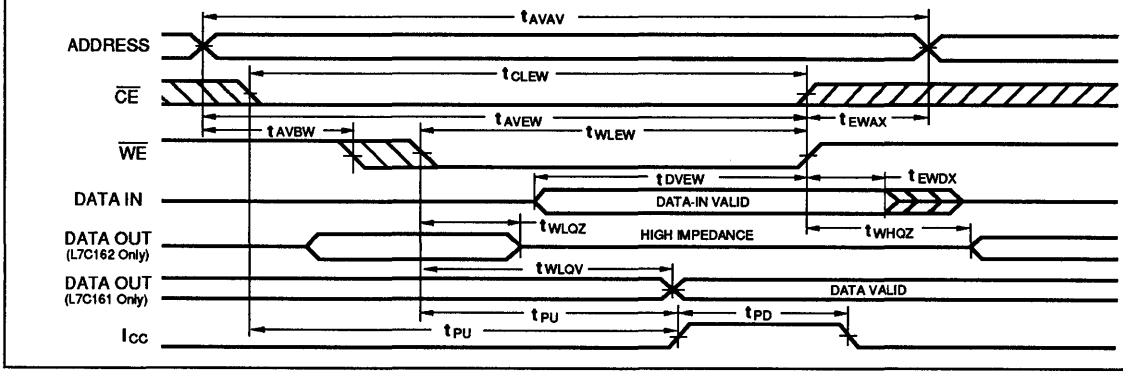


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

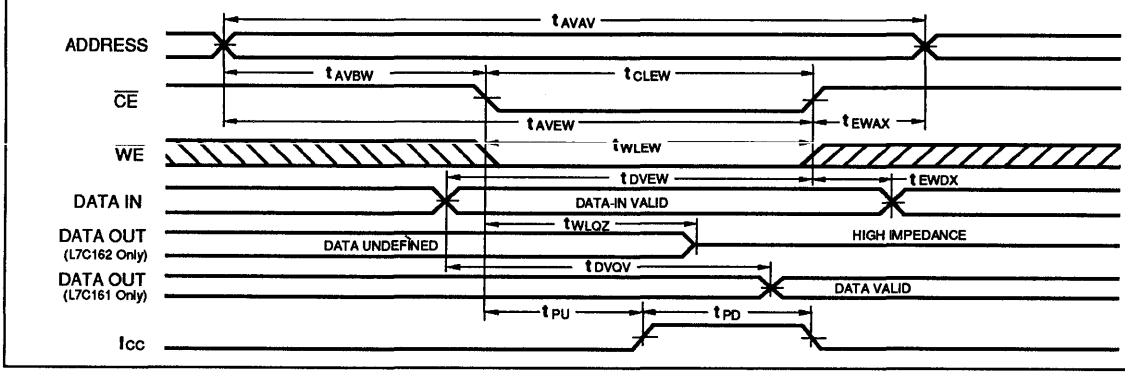
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C161/162- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	8 Min	8 Max
tAVAV	Write Cycle Time	25		20		20		15		12		10		8	
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10		8		8	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10		8		8	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10		8		6.5	
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6		5		4	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		3
tWLQV	Write Enable Low to Output Valid		30		20		15		15		12		10		8
tDVQV	Data Valid to Output Valid		30		20		15		15		12		10		8

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CEx} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE_1}$ or $\overline{CE_2} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE_1}$ or $\overline{CE_2} = V_{CC}$. Input levels are within 0.2 V of VCC or GND.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE_1}$ or $\overline{CE_2}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. WE is high for the read cycle.

14. The chip is continuously selected ($\overline{CE_1}$ and $\overline{CE_2}$ low).

15. All address lines are valid prior-to or coincident-with the later of $\overline{CE_1}$ and $\overline{CE_2}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE_1}$, $\overline{CE_2}$ low and $\overline{WE}$ low. All three signals must be low to initiate a write. Any signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with the later of $\overline{CE_1}$ and $\overline{CE_2}$ going low, the output remains in a high impedance state.

18. If $\overline{CE_1}$ or $\overline{CE_2}$ goes high before or concurrent with WE going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$x (other $\overline{CE}$ active).

b. Falling edge of $\overline{WE}$ ($\overline{CE_1}$, $\overline{CE_2}$ active).

c. Transition on any address line ($\overline{CE_1}$, $\overline{CE_2}$ active).

d. Transition on any data line ($\overline{CE_1}$, $\overline{CE_2}$, and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE_1}$, $\overline{CE_2}$, or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

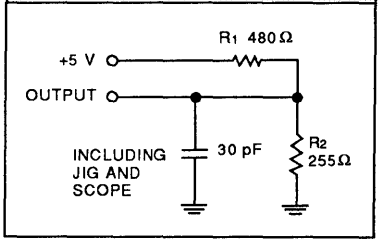


FIGURE 1b.

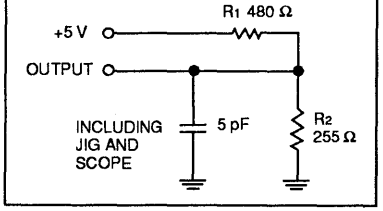
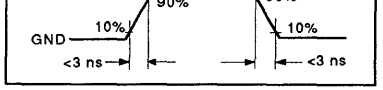
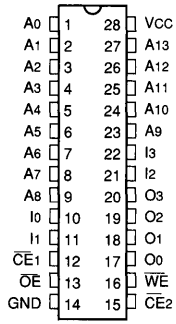


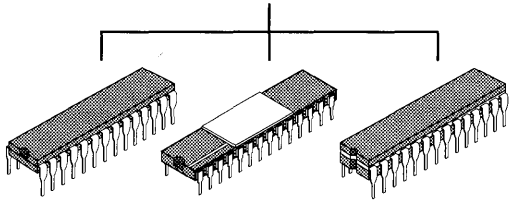
FIGURE 2.



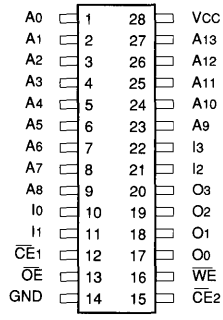
ORDERING INFORMATION

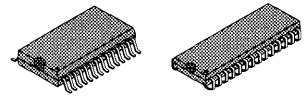
28-pin
(0.3" wide)



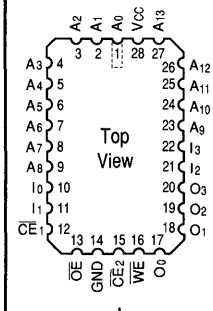


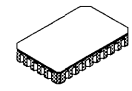
28-pin





28-pin
(350 x 550)





Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic SOIC (.300"— U2)	Plastic SOJ (.300"— W2)	Ceramic Leadless Chip Carrier (K5)
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C161PC or L7C162PC 35 25 20 15 12 10 8	L7C161DC or L7C162DC 35 25 20 15 12 10 8	L7C161CC or L7C162CC 35 25 20 15 12 10 8	L7C161UC or L7C162UC 35 25 20 15 12 10 8	L7C161WC or L7C162WC 35 25 20 15 12 10 8	L7C161KC or L7C162KC 35 25 20 15 12 10 8
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C161DM or L7C162DM 35 25 20 15 12 10	L7C161CM or L7C162CM 35 25 20 15 12 10			L7C161KM or L7C162KM 35 25 20 15 12 10
	–55°C to +125°C — Extended Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C161DME or L7C162DME 35 25 20 15 12 10	L7C161CME or L7C162CME 35 25 20 15 12 10			L7C161KME or L7C162KME 35 25 20 15 12 10
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C161DMB or L7C162DMB 35 25 20 15 12 10	L7C161CMB or L7C162CMB 35 25 20 15 12 10			L7C161KMB or L7C162KMB 35 25 20 15 12 10

8K x 8 Static RAM (Low Power) L7C185/L7CL185

FEATURES

- 8K × 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 10 ns maximum
- Low Power Operation
  Active:
  320 mW (L7C185) typical at 35 ns
  Standby (typical):
  500 µW (L7C185)
  250 µW (L7CL185)
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT7164, Cypress CY7C185/186
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin CerDIP
  - 28-pin Plastic SOIC
  - 28-pin Plastic SOJ
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C185** and **L7CL185** are high-performance, low-power CMOS static RAMs. The storage circuitry is organized as 8,192 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in six speeds with maximum access times from 10 ns to 35 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L7C185 is 320 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) for the L7C185 and 60 mW (typical) for the L7CL185 when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C185 and L7CL185 consume only 30 µW and 15 µW (typical) respectively at 3 V, allowing effective battery backup operation.

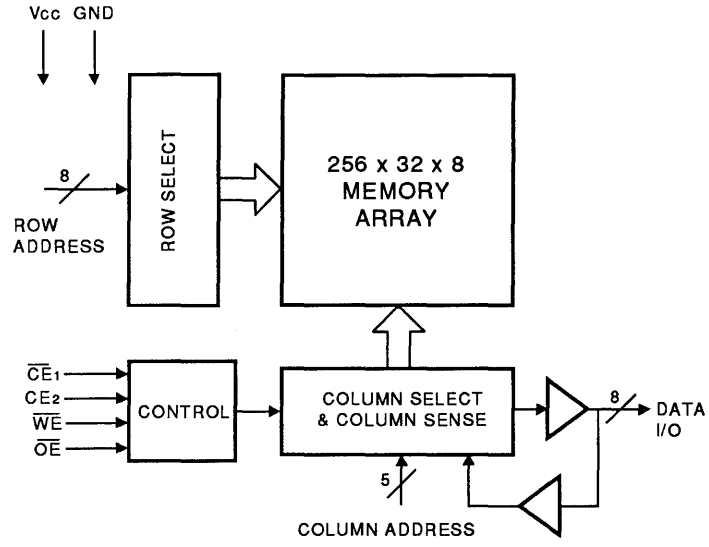
The L7C185 and L7CL185 provide asynchronous (unclocked) operation with matching access and cycle times. Two Chip Enables (one active-low) and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{12}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}_1$ low and CE_2 high while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data I/O pins within one access time. The I/O pins stay in a high-impedance state when $\overline{CE}_1$ is high or CE_2 or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}_1$ and $\overline{WE}$ inputs are both low, and CE_2 is high. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C185 and L7CL185 can withstand an injection current of up to 200 mA on any pin without damage.

L7C185/L7CL185 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C185			L7CL185			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10		+10	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–350			–350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		15	30		12	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500		50	150	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	250		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

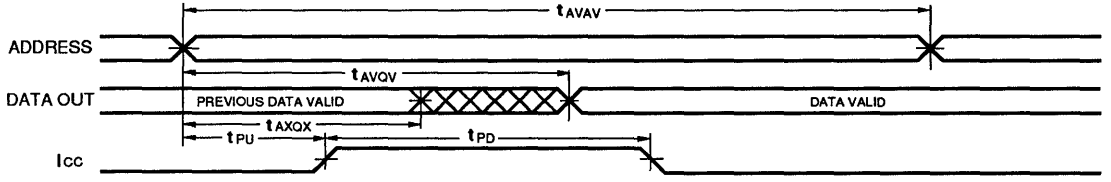
			L7C185-							
Symbol	Parameter	Test Condition	35	25	20	15	12	10		Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	110	150	185	240	275	300		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

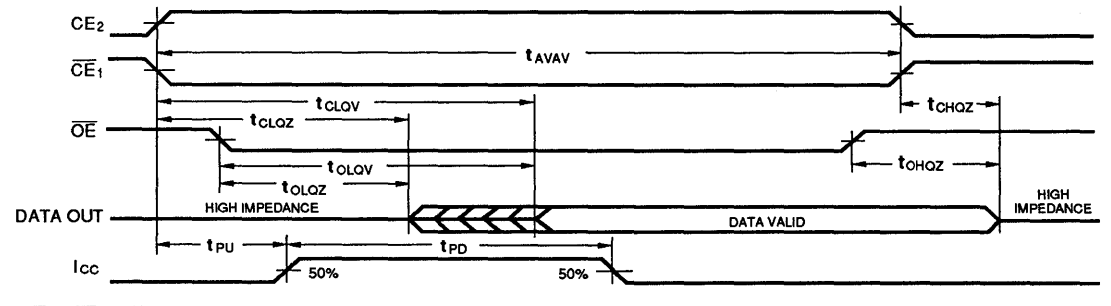
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C185/L7CL185- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12		10			
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		10		
tAXQX	Address Change to Output Change	3		3		3		3		3		3			
tCLQV	Chip Enable Active to Output Valid (13, 15)		35		25		20		15		12		10		
tCLQZ	Chip Enable Active to Output Low Z (20, 21)	3		3		3		3		3		3			
tCHQZ	Chip Enable Inactive to Output High Z (20, 21)		15		10		8		8		5		4		
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		5		
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		4		
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		18		
tCHVL	Chip Enable Inactive to Data Retention (10)	0		0		0		0		0		0			

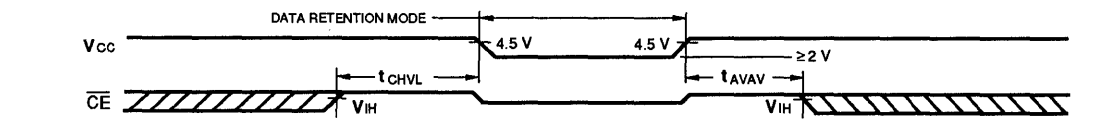
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — CE/OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

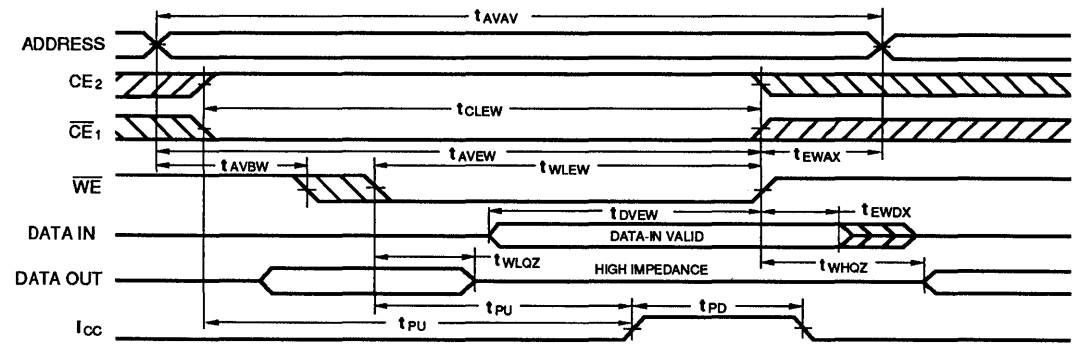


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

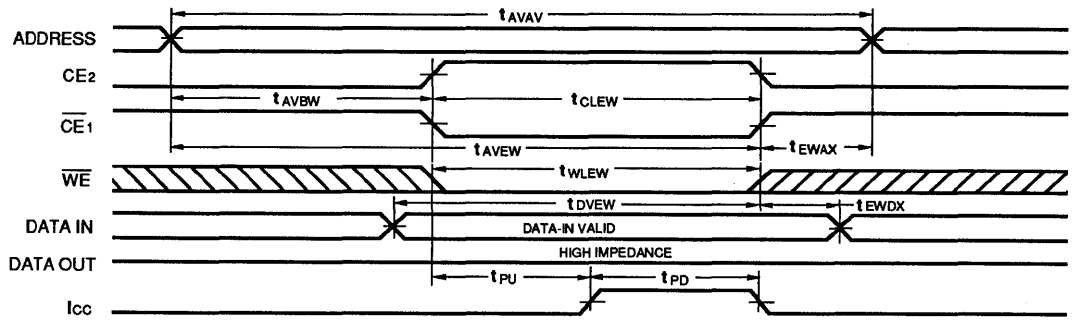
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C185/L7CL185- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
t_{AVAV}	Write Cycle Time	25		20		20		15		12		10			
t_{CLEW}	Chip Enable Active to End of Write Cycle	25		15		15		12		10		8			
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0			
t_{AVEW}	Address Valid to End of Write Cycle	25		15		15		12		10		8			
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0		0		0			
t_{WLEW}	Write Enable Low to End of Write Cycle	20		15		15		12		10		8			
t_{DVEW}	Data Valid to End of Write Cycle	15		10		10		7		6		5			
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0		0		0			
t_{WHQZ}	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0			
t_{WLQZ}	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4		4		

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}1$, $CE2 \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}1 \ge V_{IH}$, $CE2 \le V_{IL}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}1 = V_{CC}$, CE2 = GND. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}1$ must be $\ge V_{CC} - 0.2$ V. For the L7C185, all other inputs meet $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V to ensure full powerdown. For the L7CL185, this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}1$ low, CE2 high).

15. All address lines are valid prior-to or coincident-with the later of $\overline{CE}1$ and CE2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}1$ and CE2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with later of $\overline{CE}1$ and CE2 going active, the output remains in a high impedance state.

18. If $\overline{CE}1$ and CE2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Rising edge of CE2.

b. Falling edge of $\overline{WE}$ ($\overline{CE}1$, CE2 active).

c. Transition on any address line ($\overline{CE}1$, CE2 active).

d. Transition on any data line ($\overline{CE}1$, CE2, and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}1$, CE2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

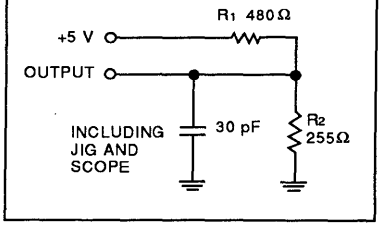


FIGURE 1b.

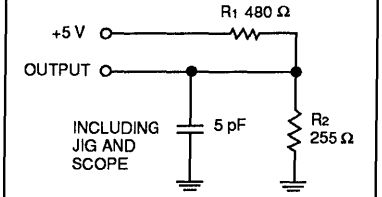
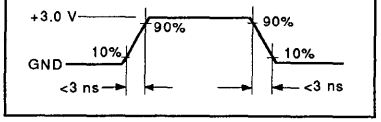
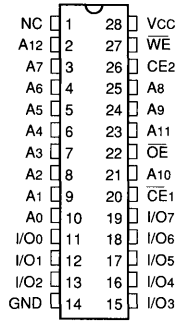


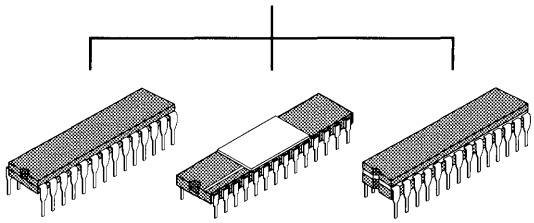
FIGURE 2.



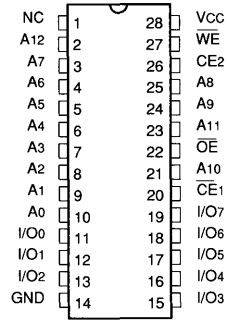
ORDERING INFORMATION

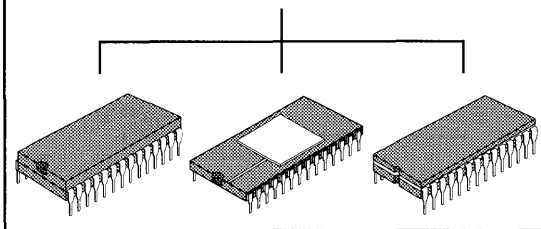
28-pin (0.3" wide)





28-pin (0.6" wide)

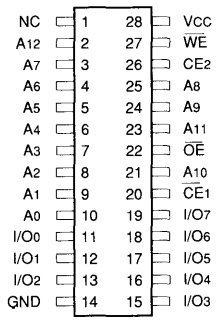


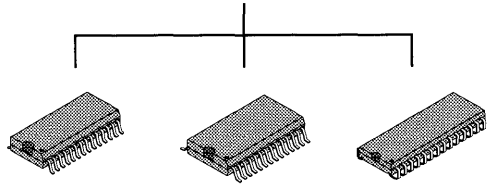


Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic DIP (P9)	Sidebraze Hermetic DIP (D9)	CerDIP (C6)
	0°C to +70°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C185PC or L7CL185PC — 35, 25, 20, 15, 12, 10	L7C185DC or L7CL185DC — 35, 25, 20, 15, 12, 10	L7C185CC or L7CL185CC — 35, 25, 20, 15, 12, 10	L7C185NC or L7CL185NC — 35, 25, 20, 15, 12, 10	L7C185HC or L7CL185HC — 35, 25, 20, 15, 12, 10	L7C185IC or L7CL185IC — 35, 25, 20, 15, 12, 10
	–55°C to +125°C — Commercial Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C185DM or L7CL185DM — 35, 25, 20, 15, 12	L7C185CM or L7CL185CM — 35, 25, 20, 15, 12		L7C185HM or L7CL185HM — 35, 25, 20, 15, 12	L7C185IM or L7CL185IM — 35, 25, 20, 15, 12
	–55°C to +125°C — Extended Screening					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C185DME or L7CL185DME — 35, 25, 20, 15, 12	L7C185CME or L7CL185CME — 35, 25, 20, 15, 12		L7C185HME or L7CL185HME — 35, 25, 20, 15, 12	L7C185IME or L7CL185IME — 35, 25, 20, 15, 12
	–55°C to +125°C — MIL-STD-883 Compliant					
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C185DMB or L7CL185DMB — 35, 25, 20, 15, 12	L7C185CMB or L7CL185CMB — 35, 25, 20, 15, 12		L7C185HMB or L7CL185HMB — 35, 25, 20, 15, 12	L7C185IMB or L7CL185IMB — 35, 25, 20, 15, 12

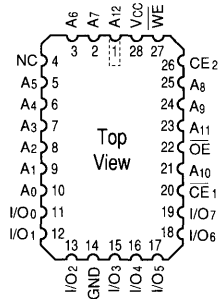
ORDERING INFORMATION

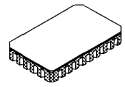
28-pin



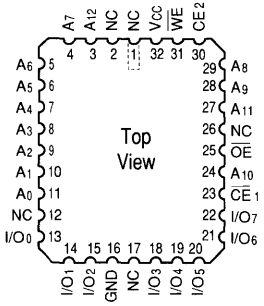


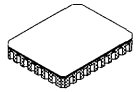
28-pin
(350 x 550)





32-pin
(450 x 550)





Speed	Plastic SOIC (.300"— U2)	Plastic SOIC (.340"— V2)	Plastic SOJ (.300"— W2)	Ceramic Leadless Chip Carrier (K5)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C185UC or L7CL185UC — 35, 25, 20, 15, 12, 10	L7C185VC or L7CL185VC — 35, 25, 20, 15, 12, 10	L7C185WC or L7CL185WC — 35, 25, 20, 15, 12, 10	L7C185KC or L7CL185KC — 35, 25, 20, 15, 12, 10	L7C185TC or L7CL185TC — 35, 25, 20, 15, 12, 10
	–55°C to +125°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns				L7C185KM or L7CL185KM — 35, 25, 20, 15, 12	L7C185TM or L7CL185TM — 35, 25, 20, 15, 12
	–55°C to +125°C — Extended Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns				L7C185KME or L7CL185KME — 35, 25, 20, 15, 12	L7C185TME or L7CL185TME — 35, 25, 20, 15, 12
	–55°C to +125°C — MIL-STD-883 Compliant				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns				L7C185KMB or L7CL185KMB — 35, 25, 20, 15, 12	L7C185TMB or L7CL185TMB — 35, 25, 20, 15, 12

FEATURES

- 256K x 1 Static RAM with Separate I/O, Chip Select Powerdown
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 12 ns maximum
- Low Power Operation
  Active: 210 mW typical at 45 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 71257, Cypress CY7C197
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin CerDIP
  - 24-pin Plastic SOIC
  - 24-pin Plastic SOJ

DESCRIPTION

The **L7C197** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 262,144 words by 1 bit per word. This device is available in six speeds with maximum access times from 12 ns to 45 ns.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 210 mW (typical) at 45 ns. Dissipation drops to 35 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C197 consumes only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

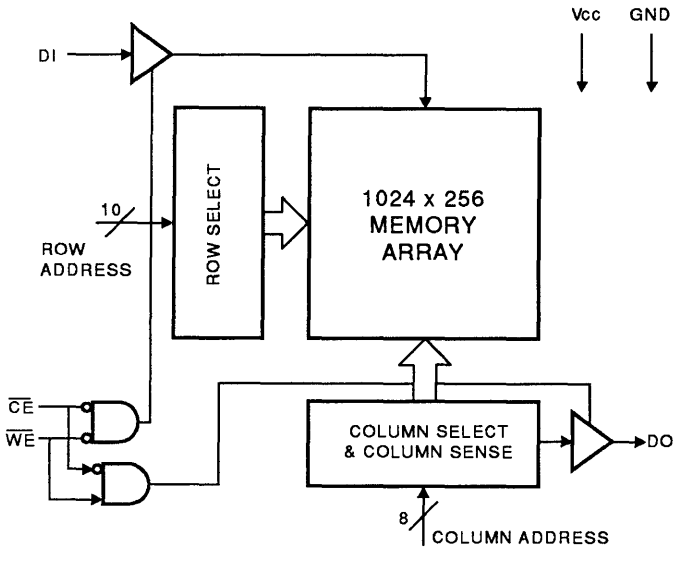
The L7C197 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{17}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C197 can withstand an injection current of up to 200 mA on any pin without damage.

L7C197 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Active Operation, Military	−55°C to +125°C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention, Commercial	0°C to +70°C	$2.0\ V \le V_{CC} \le 5.5\ V$
Data Retention, Military	−55°C to +125°C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	$I_{OH} = -4.0$ mA, $V_{CC} = 4.5$ V	2.4			V
V_{OL}	Output Low Voltage	$I_{OL} = 8.0$ mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Current	$GND \le V_{IN} \le V_{CC}$	−10		+10	µA
I_{OZ}	Output Leakage Current	$GND \le V_{OUT} \le V_{CC}$, $\overline{CE} = V_{CC}$	−10		+10	µA
I_{OS}	Output Short Current	$V_{OUT} = GND$, V_{CC} = Max (Note 4)			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		20	40	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		2	10	mA
I_{CC4}	V_{CC} Current, Data Retention	$V_{CC} = 3.0$ V (Note 9)		500	5000	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, $V_{CC} = 5.0$ V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

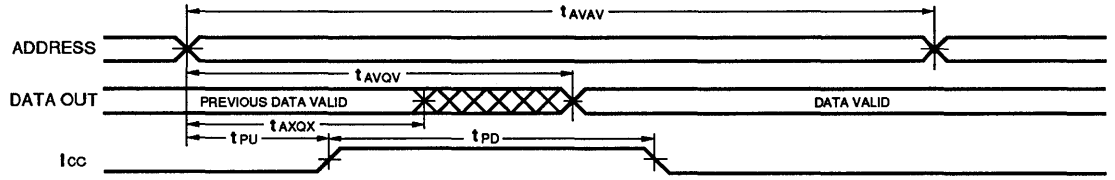
			L7C197-						
Symbol	Parameter	Test Condition	45	35	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	55	75	100	125	160	190	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

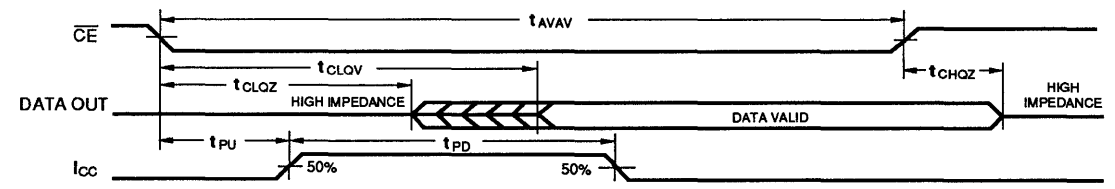
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C197- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max
t_{AVAV}	Read Cycle Time	45		35		25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (13, 14)		45		35		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (13, 15)		45		35		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (20, 21)		15		15		10		8		8		5
t_{PU}	Input Transition to Power Up (10, 19)	0		0		0		0		0		0	
t_{PD}	Power Up to Power Down (10, 19)		45		35		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (10)	0		0		0		0		0		0	

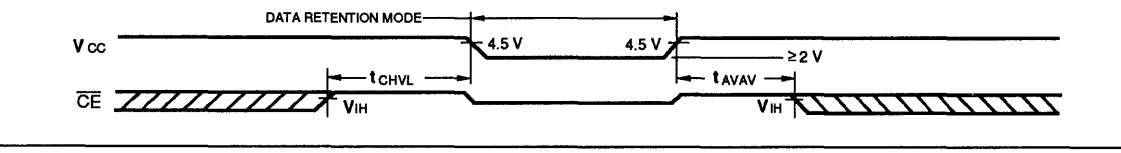
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — $\overline{CE}$ CONTROLLED *(Notes 13, 15)*



DATA RETENTION

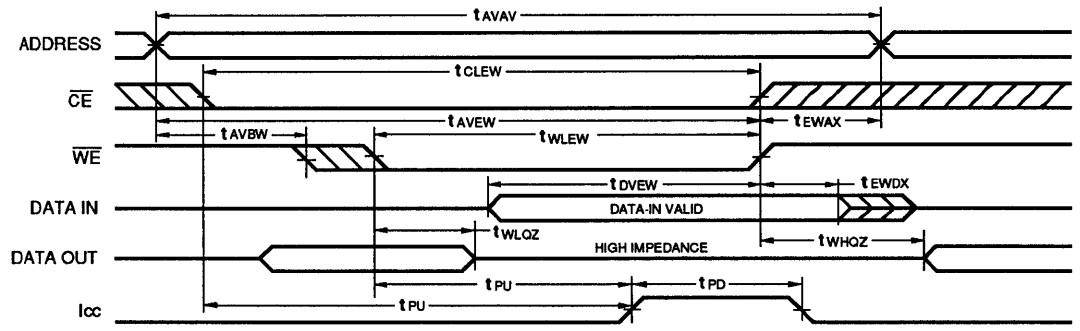


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

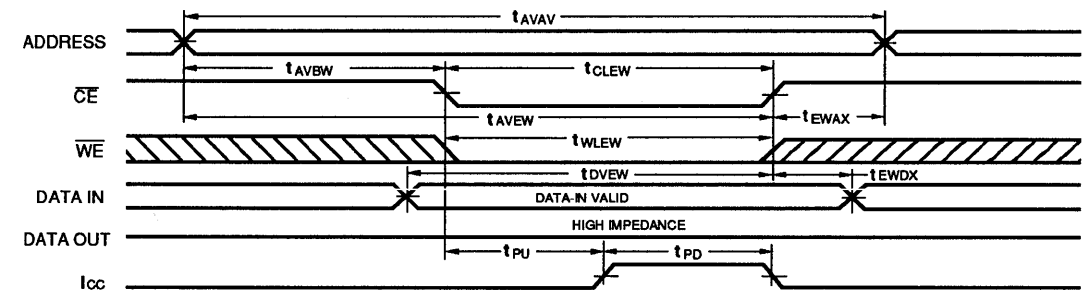
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C197- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max
tAVAV	Write Cycle Time	40		25		20		20		15		12	
tCLEW	Chip Enable Low to End of Write Cycle	30		25		15		15		12		10	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		25		15		15		12		10	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		20		15		15		12		10	
tDVEW	Data Valid to End of Write Cycle	15		15		10		10		7		6	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		15		10		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

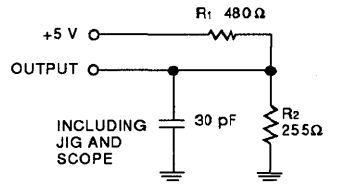


FIGURE 1b.

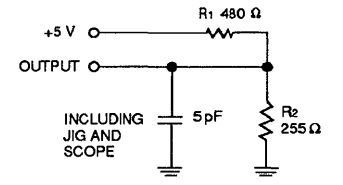
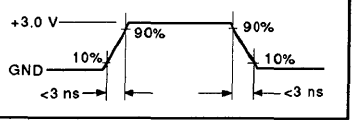
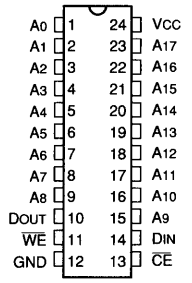


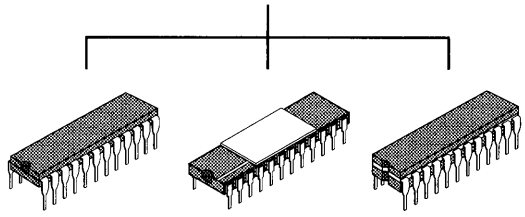
FIGURE 2.



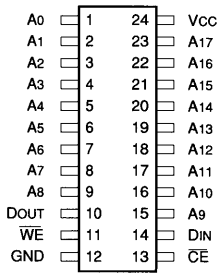
ORDERING INFORMATION

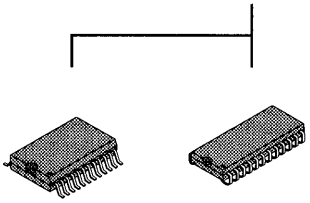
24-pin
(0.3" wide)





24-pin





Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic SOIC (.340"— V1)	Plastic SOJ (.300"— W1)	
	0°C to +70°C — Commercial Screening					
45 ns	L7C197PC45	L7C197DC45	L7C197CC45	L7C197VC45	L7C197WC45	
35 ns	" " 35	" " 35	" " 35	" " 35	" " 35	
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12	
	–55°C to +125°C — Commercial Screening					
45 ns		L7C197DM45	L7C197CM45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns		" " 15	" " 15			
12 ns						
	–55°C to +125°C — Extended Screening					
45 ns		L7C197DME45	L7C197CME45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns		" " 15	" " 15			
12 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns		L7C197DMB45	L7C197CMB45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns		" " 15	" " 15			
12 ns						

FEATURES

- 64K × 4 Static RAM with Common I/O
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active: 265 mW typical at 45 ns
  Standby: 10 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 71258/61298, Cypress CY7C194/196
- Package Styles Available:
  - 24/28-pin Plastic DIP
  - 24/28-pin Sidebraze, Hermetic DIP
  - 24/28-pin CerDIP
  - 24/28-pin Plastic SOIC
  - 24/28-pin Plastic SOJ

DESCRIPTION

The **L7C194, L7C195,** and **L7C196** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 65,536 words by 4 bits per word. Data In and Data Out signals share I/O pins. The L7C194 has a single active-low Chip Enable. The L7C195 has a single Chip Enable and an Output Enable. The L7C196 has two Chip Enables and a separate Output Enable. These devices are available in five speeds with maximum access times from 15 ns to 45 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 265 mW (typical) at 45 ns. Dissipation drops to 100 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C194, L7C195, and L7C196 consume only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

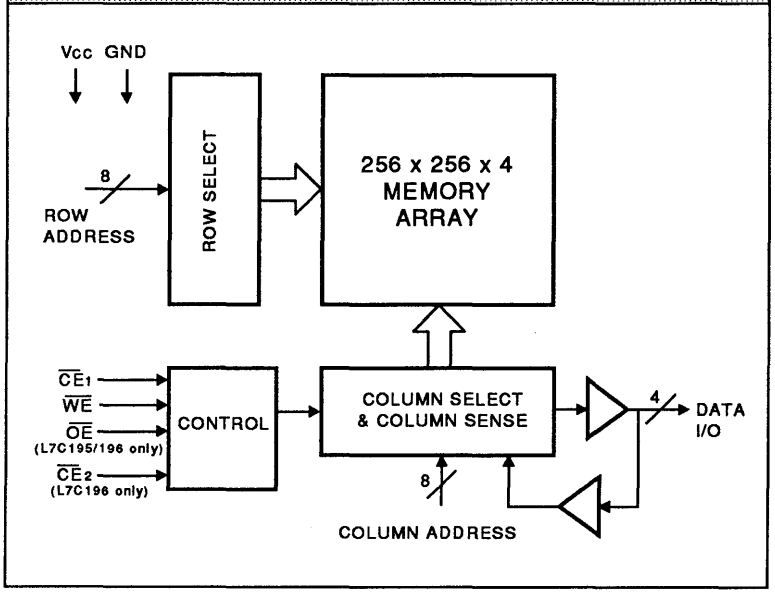
The L7C194, L7C195, and L7C196 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. For the L7C194 and L7C195, reading from a designated location is accomplished by presenting an address and driving $\overline{CE}_1$ low while $\overline{WE}$ remains high. For the L7C196, both $\overline{CE}_1$ and $\overline{CE}_2$ must be low. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{OE}$ is high, or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C194, L7C195, and L7C196 can withstand an injection current of up to 200 mA on any pin without damage.

L7C194/195/196 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		20	40	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		2	10	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		500	5000	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

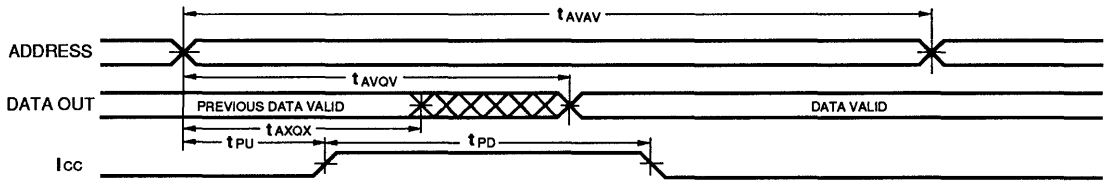
			L7C194/195/196-					
Symbol	Parameter	Test Condition	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	55	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

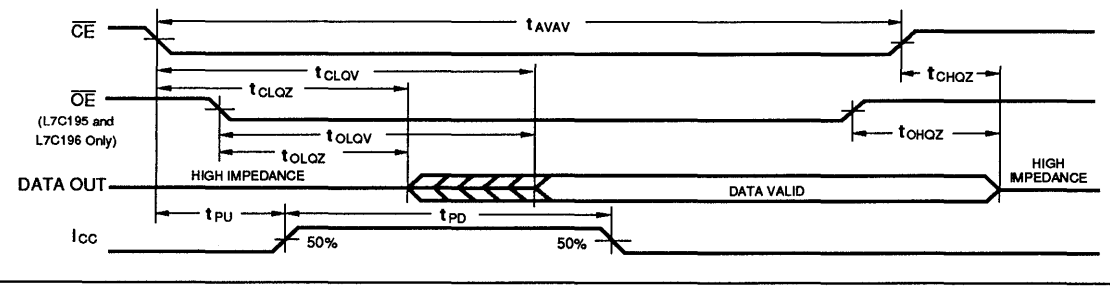
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C194/195/196- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Read Cycle Time	45		35		25		20		15	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		20		15
tAXQX	Address Change to Output Change	3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		15		10		8		8
tOLQV	Output Enable Low to Output Valid		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0	
tOHQZ	Output Enable High to Output High Z (20, 21)		15		12		10		8		5
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20		20
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0	

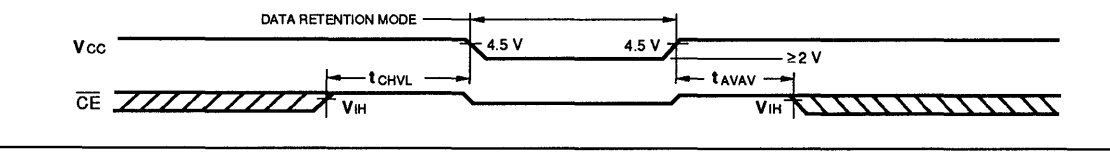
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — $\overline{CE}$/$\overline{OE}$ CONTROLLED *(Notes 13, 15)*



DATA RETENTION

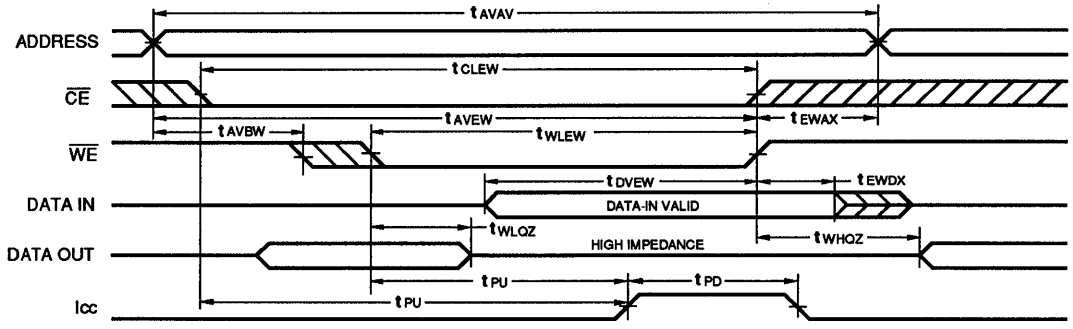


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

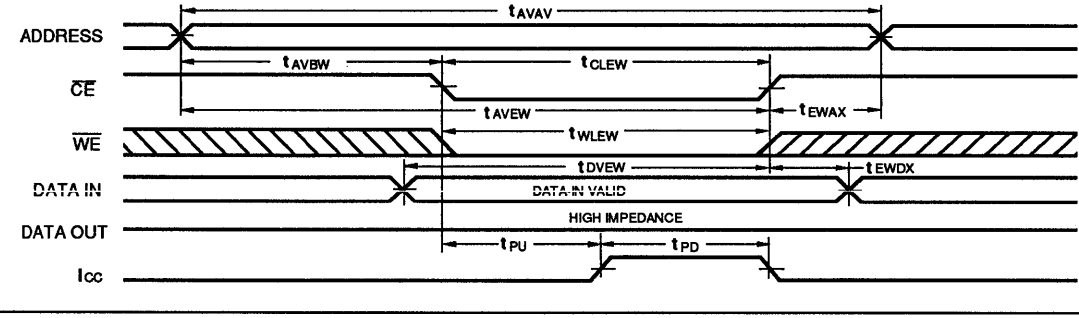
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C194/195/196- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Write Cycle Time	40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	30		25		15		15		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		25		15		15		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		20		15		15		12	
tDVEW	Data Valid to End of Write Cycle	15		15		10		10		7	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		15		10		7		7		5

Write Cycle — $\overline{WE}$ Controlled (Notes 16, 17, 18, 19)



Write Cycle — $\overline{CE}$ Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}^* \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE}^* \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}^* = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}^*$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}^*$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}^*$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}^*$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}^*$ going low, the output remains in a high impedance state.

18. If $\overline{CE}^*$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}^*$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}^*$ active).

c. Transition on any address line ($\overline{CE}^*$ active).

d. Transition on any data line ($\overline{CE}^*$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}^*$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

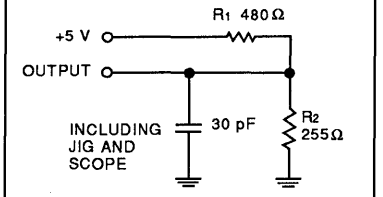


FIGURE 1b.

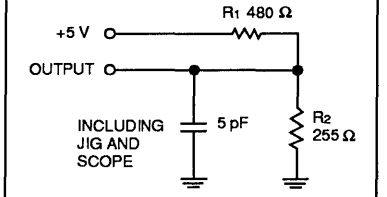
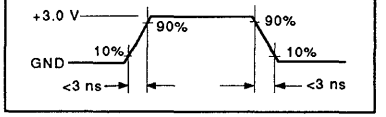


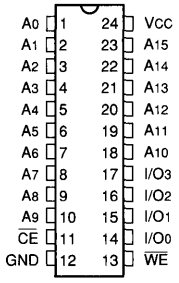
FIGURE 2.

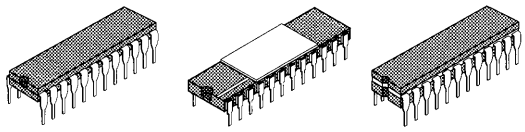


* For the L7C196, $\overline{CE}$ refers to the logical AND of $\overline{CE}_1$ and $\overline{CE}_2$.

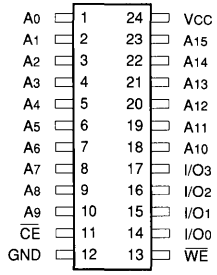
L7C194 — ORDERING INFORMATION

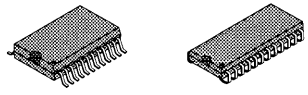
24-pin
(0.3" wide)





24-pin

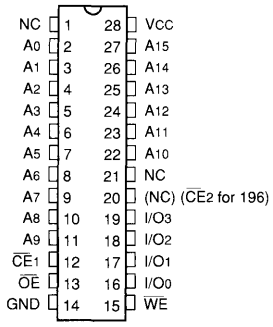


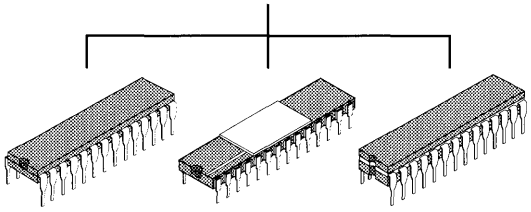


Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic SOIC (.340"— V1)	Plastic SOJ (.300"— W1)	
	0°C to +70°C — Commercial Screening					
45 ns	L7C194PC45	L7C194DC45	L7C194CC45	L7C194VC45	L7C194WC45	
35 ns	" " 35	" " 35	" " 35	" " 35	" " 35	
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25	
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20	
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15	
12 ns						
	–55°C to +125°C — Commercial Screening					
45 ns		L7C194DM45	L7C194CM45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns						
12 ns						
	–55°C to +125°C — Extended Screening					
45 ns		L7C194DME45	L7C194CME45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns						
12 ns						
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns		L7C194DMB45	L7C194CMB45			
35 ns		" " 35	" " 35			
25 ns		" " 25	" " 25			
20 ns		" " 20	" " 20			
15 ns						
12 ns						

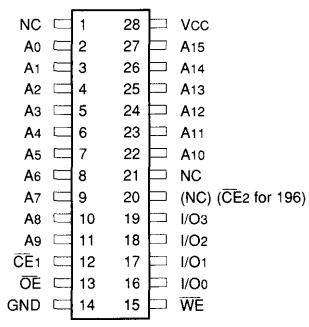
L7C195/196 — ORDERING INFORMATION

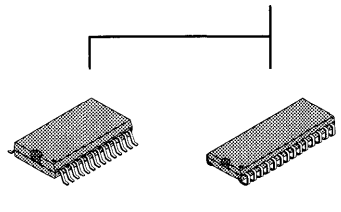
28-pin
(0.3" wide)





28-pin





Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic SOIC (.340"— V2)	Plastic SOJ (.300"— W2)	
	0°C to +70°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns	L7C195PC / L7C196PC — 45, 35, 25, 20, 15	L7C195DC / L7C196DC — 45, 35, 25, 20, 15	L7C195CC / L7C196CC — 45, 35, 25, 20, 15	L7C195VC / L7C196VC — 45, 35, 25, 20, 15	L7C195WC / L7C196WC — 45, 35, 25, 20, 15	
	–55°C to +125°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C195DM / L7C196DM — 45, 35, 25, 20	L7C195CM / L7C196CM — 45, 35, 25, 20			
	–55°C to +125°C — Extended Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C195DME / L7C196DME — 45, 35, 25, 20	L7C195CME / L7C196CME — 45, 35, 25, 20			
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C195DMB / L7C196DMB — 45, 35, 25, 20	L7C195CMB / L7C196CMB — 45, 35, 25, 20			

FEATURES

- 64K x 4 Static RAM with Separate I/O, Transparent Write (L7C191), or High Impedance Write (L7C192)
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active: 265 mW typical at 45 ns
  Standby: 10 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 71281/71282, Cypress CY7C191/192
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin CerDIP
  - 28-pin Plastic SOIC
  - 28-pin Plastic SOJ

DESCRIPTION

The **L7C191** and **L7C192** are high-performance, low-power CMOS static RAMs. The storage cells are organized as 65,536 words by 4 bits per word. Data In and Data Out are separate. These devices are available in five speeds with maximum access times from 15 ns to 45 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption is 265 mW (typical) at 45 ns. Dissipation drops to 100 mW (typical) when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C191 and L7C192 consume only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

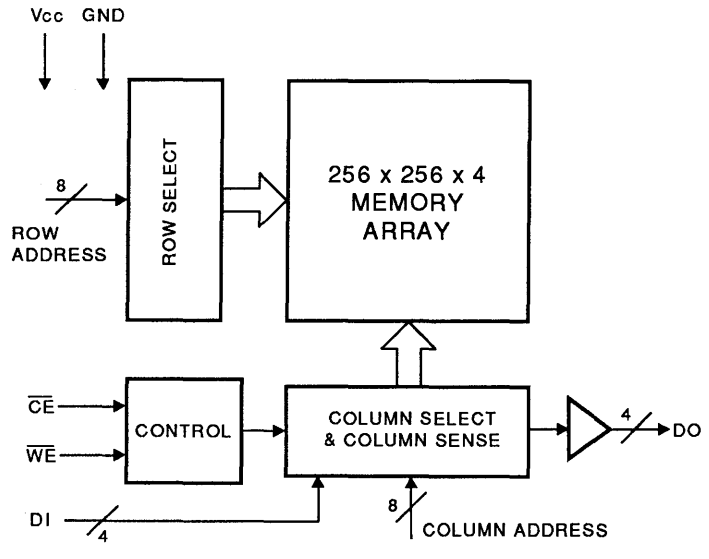
The L7C191 and L7C192 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state bus output simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{15}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{WE}$ is low (L7C192 only) or $\overline{CE}$ is high.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. The Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C191 and L7C192 can withstand an injection current of up to 200 mA on any pin without damage.

L7C191/192 BLOCK DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		20	40	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		2	10	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		500	5000	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

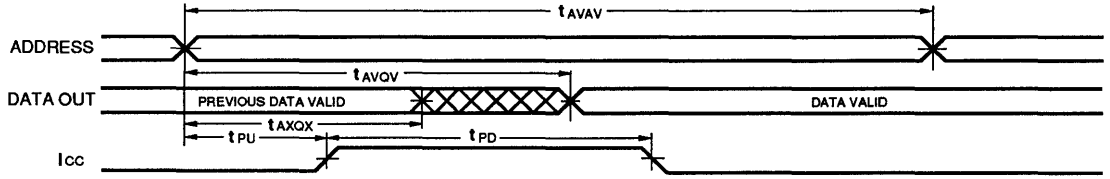
			L7C191/192-					
Symbol	Parameter	Test Condition	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	55	75	100	125	160	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

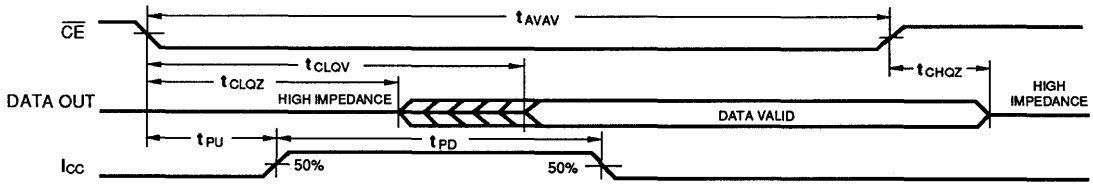
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C191/192- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Read Cycle Time	45		35		25		20		15	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		20		15
tAXQX	Address Change to Output Change	3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		15		10		8		5
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20		20
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0	

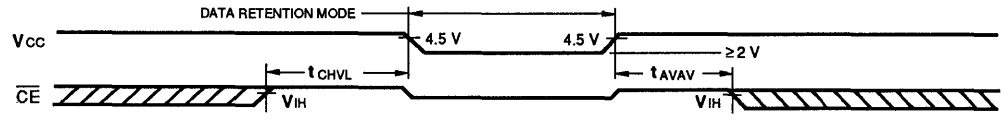
Read Cycle — Address Controlled (Notes 13, 14)



Read Cycle — $\overline{CE}$ Controlled (Notes 13, 15)



Data Retention

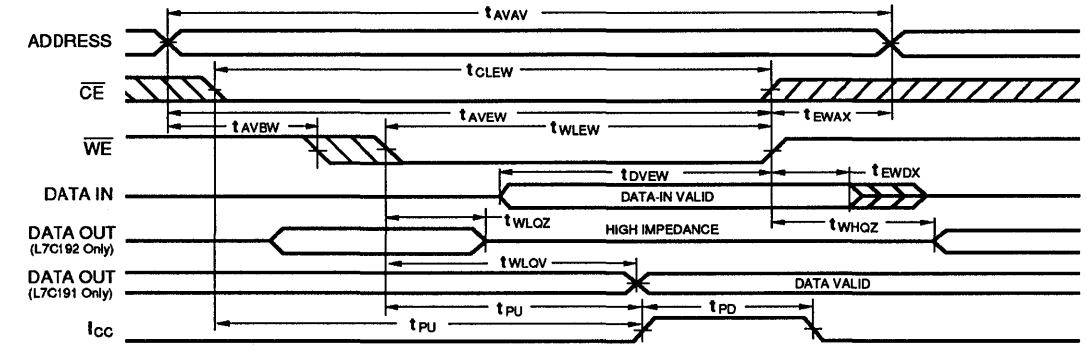


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

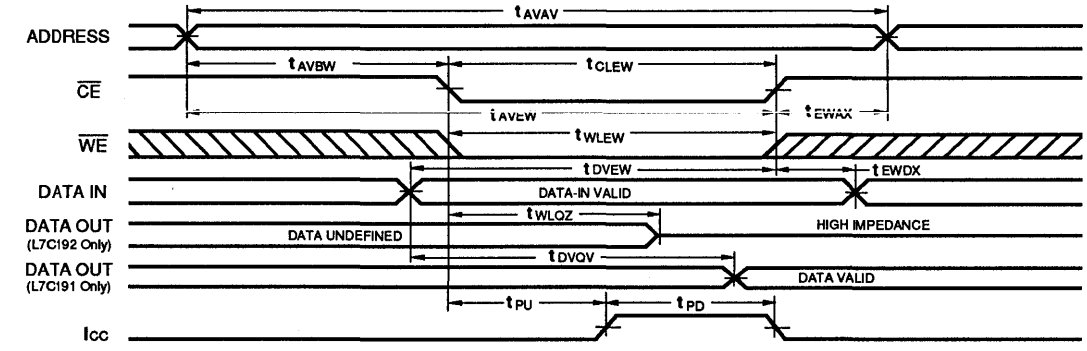
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C191/192- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Write Cycle Time	40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	30		25		15		15		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		25		15		15		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		20		15		15		12	
tDVEW	Data Valid to End of Write Cycle	15		15		10		10		7	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		15		10		7		7		5
tWLQV	Write Enable Low to Output Valid		35		30		20		15		15
tDVQV	Data Valid to Output Valid		35		30		20		15		15

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.2 V. For all other inputs VIN ≥ VCC – 0.2 V or VIN ≤ 0.2 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with WE going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

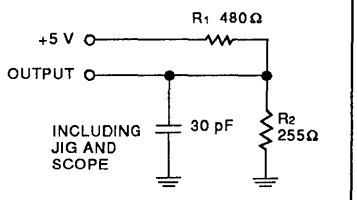


FIGURE 1b.

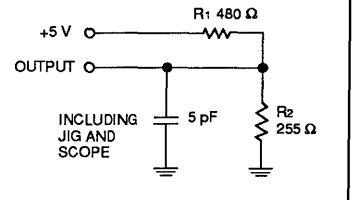
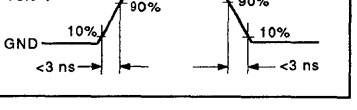
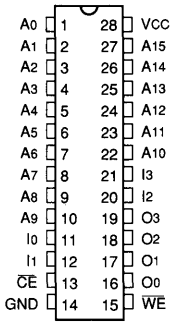


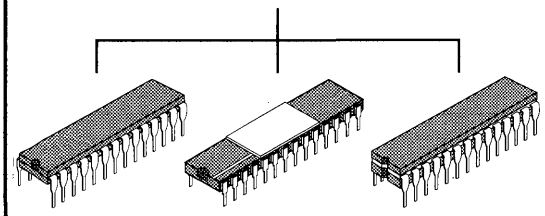
FIGURE 2.



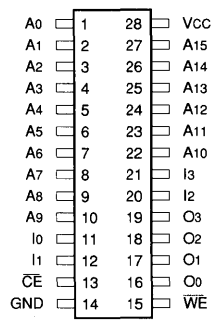
ORDERING INFORMATION

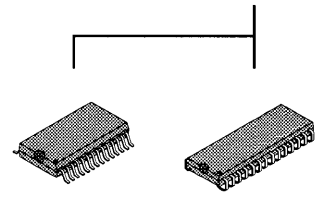
28-pin
(0.3" wide)





28-pin





Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic SOIC (.340"— V2)	Plastic SOJ (.300"— W2)	
	0°C to +70°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns	L7C191PC / L7C192PC — 45, 35, 25, 20, 15	L7C191DC / L7C192DC — 45, 35, 25, 20, 15	L7C191CC / L7C192CC — 45, 35, 25, 20, 15	L7C191VC / L7C192VC — 45, 35, 25, 20, 15	L7C191WC / L7C192WC — 45, 35, 25, 20, 15	
	–55°C to +125°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C191DM / L7C192DM — 45, 35, 25, 20	L7C191CM / L7C192CM — 45, 35, 25, 20			
	–55°C to +125°C — Extended Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C191DME / L7C192DME — 45, 35, 25, 20	L7C191CME / L7C192CME — 45, 35, 25, 20			
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C191DMB / L7C192DMB — 45, 35, 25, 20	L7C191CMB / L7C192CMB — 45, 35, 25, 20			

32K x 8 Static RAM (Low Power) L7C199/L7CL199

FEATURES

- 32K × 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 15 ns maximum
- Low Power Operation
  Active:
  380 mW (typical) at 45 ns
  Standby (typical):
  10 mW (L7C199)
  1.25 mW (L7CL199)
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT71256, Cypress CY7C198/199
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin CerDIP
  - 28-pin Plastic SOIC
  - 28-pin Plastic SOJ
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C199** and **L7CL199** are high-performance, low-power CMOS static RAMs. The storage circuitry is organized as 32,768 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in five speeds with maximum access times from 15 ns to 45 ns.

Inputs and output are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L7C199 is 380 mW (typical) at 45 ns. Dissipation drops to 100 mW (typical) for the L7C199 and 60 mW (typical) for the L7CL199 when the memory is deselected (Enable is high).

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C199 and L7CL199 consume only 1.5 mW (typical) at 3 V, allowing effective battery backup operation.

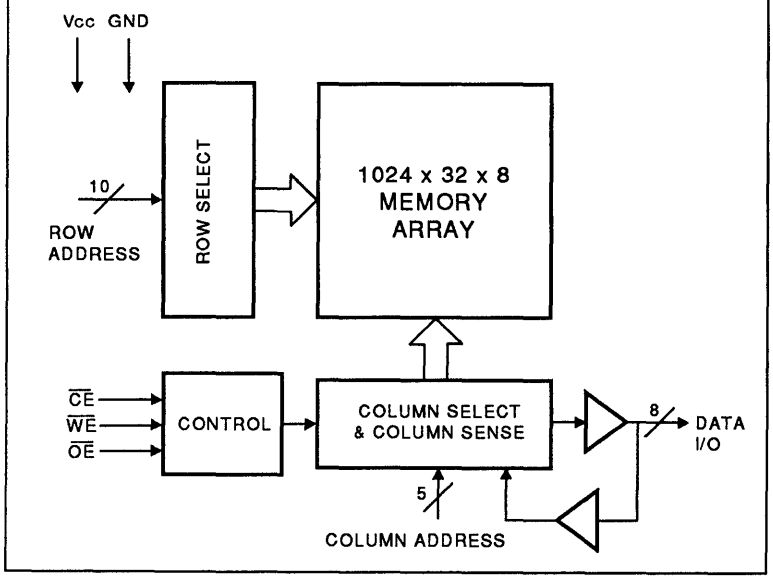
The L7C199 and L7CL199 provide asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{14}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ or $\overline{OE}$ is high, or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C199 and L7CL199 can withstand an injection current of up to 200 mA on any pin without damage.

L7C199/L7CL199 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C199			L7CL199			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	−3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	−10		+10	−10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	−10		+10	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			−350			−350	mA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		20	40		12	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		2	10		0.25	0.75	mA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		500	5000		20	200	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

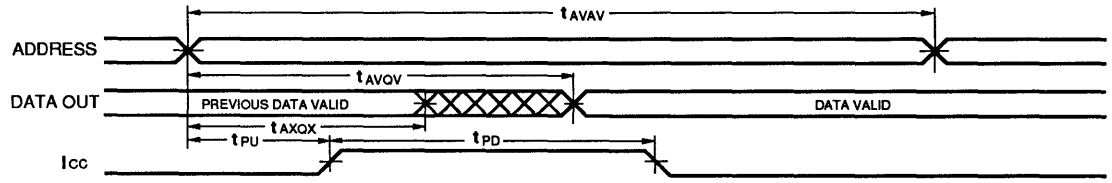
			L7C199/L7CL199-						
Symbol	Parameter	Test Condition	45	35	25	20	15		Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	85	110	150	185	240		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

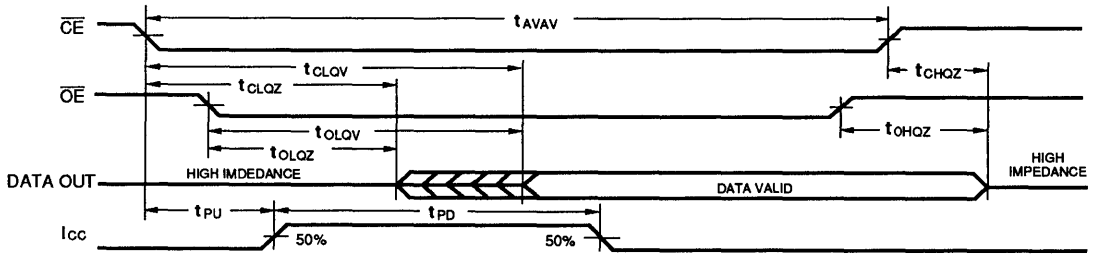
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C199/L7CL199- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tAVAV	Read Cycle Time	45		35		25		20		15	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		20		15
tAXQX	Address Change to Output Change	3		3		3		3		3	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		20		15
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3	
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		15		10		8		8
tOLQV	Output Enable Low to Output Valid		20		15		12		10		8
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0	
tOHQZ	Output Enable High to Output High Z (20, 21)		15		10		10		8		5
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20		20
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0	

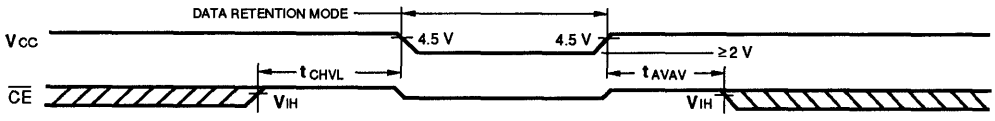
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — CE/OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

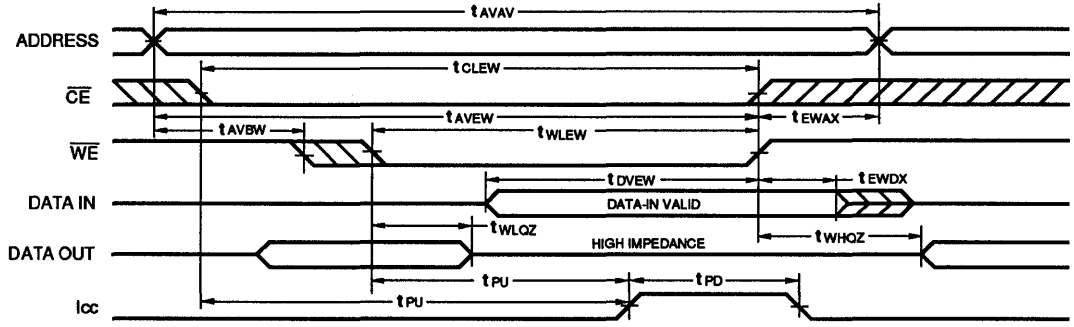


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

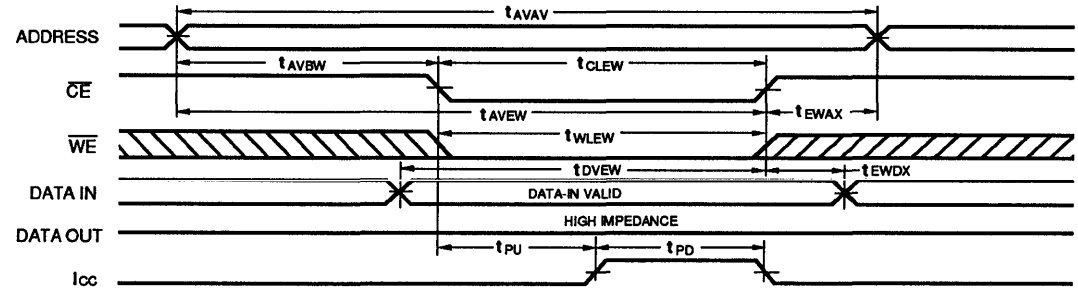
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

		L7C199/L7CL199-									
		45		35		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	40		25		20		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	30		25		15		15		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		25		15		15		12	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		20		15		15		12	
tDVEW	Data Valid to End of Write Cycle	15		15		10		10		7	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		15		10		7		7		5

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 16, 17, 18, 19)*



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3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$1 must be ≥ VCC – 0.2 V. For the L7C199, all other inputs meet VIN ≤ 0.2 V or VIN ≥ VCC – 0.2 V to ensure full powerdown. For the L7CL199, this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

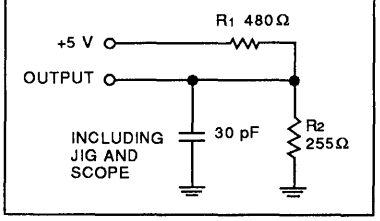


FIGURE 1b.

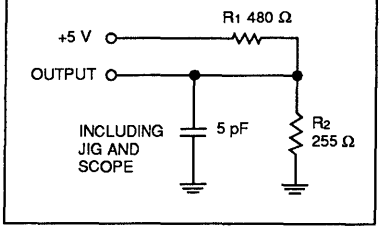
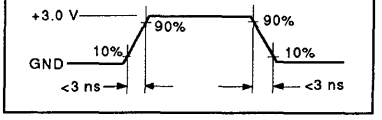
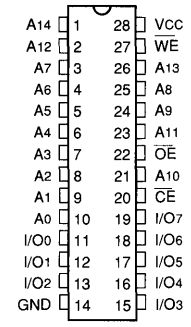


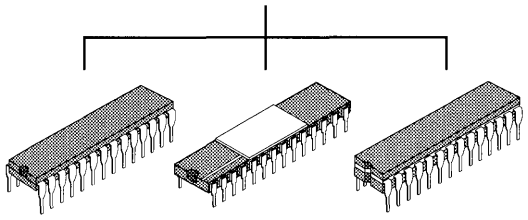
FIGURE 2.



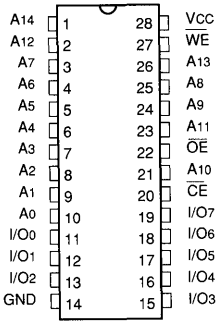
ORDERING INFORMATION

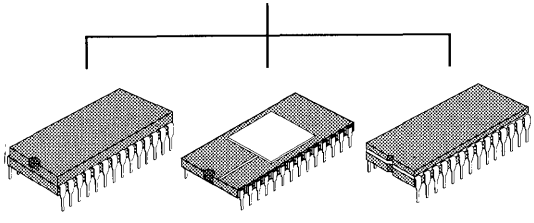
28-pin (0.3" wide)





28-pin (0.6" wide)

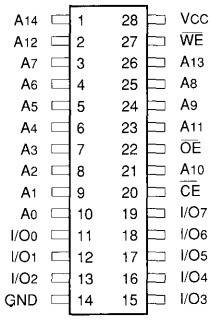


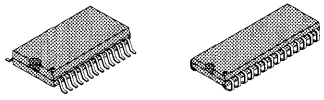


Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic DIP (P9)	Sidebraze Hermetic DIP (D9)	CerDIP (C6)
	0°C to +70°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns	L7C199PC / or / L7CL199PC — 45, 35, 25, 20, 15	L7C199DC / or / L7CL199DC — 45, 35, 25, 20, 15	L7C199CC / or / L7CL199CC — 45, 35, 25, 20, 15	L7C199NC / or / L7CL199NC — 45, 35, 25, 20, 15	L7C199HC / or / L7CL199HC — 45, 35, 25, 20, 15	L7C199IC / or / L7CL199IC — 45, 35, 25, 20, 15
	–55°C to +125°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C199DM / or / L7CL199DM — 45, 35, 25, 20	L7C199CM / or / L7CL199CM — 45, 35, 25, 20		L7C199HM / or / L7CL199HM — 45, 35, 25, 20	L7C199IM / or / L7CL199IM — 45, 35, 25, 20
	–55°C to +125°C — Extended Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C199DME / or / L7CL199DME — 45, 35, 25, 20	L7C199CME / or / L7CL199CME — 45, 35, 25, 20		L7C199HME / or / L7CL199HME — 45, 35, 25, 20	L7C199IME / or / L7CL199IME — 45, 35, 25, 20
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns		L7C199DMB / or / L7CL199DMB — 45, 35, 25, 20	L7C199CMB / or / L7CL199CMB — 45, 35, 25, 20		L7C199HMB / or / L7CL199HMB — 45, 35, 25, 20	L7C199IMB / or / L7CL199IMB — 45, 35, 25, 20

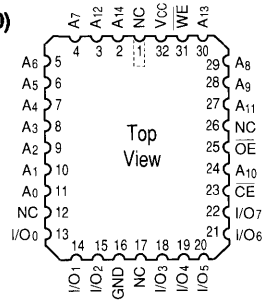
ORDERING INFORMATION

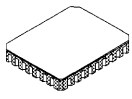
28-pin





32-pin (450 x 550)





Speed	Plastic SOIC (.340"— V2)	Plastic SOJ (.300"— W2)		Ceramic Leadless Chip Carrier (K7)		
	0°C to +70°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns	L7C199VC or L7CL199VC — 45, 35, 25, 20, 15	L7C199WC or L7CL199WC — 45, 35, 25, 20, 15		L7C199TC or L7CL199TC — 45, 35, 25, 20, 15		
	–55°C to +125°C — Commercial Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns				L7C199TM or L7CL199TM — 45, 35, 25, 20		
	–55°C to +125°C — Extended Screening					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns				L7C199TME or L7CL199TME — 45, 35, 25, 20		
	–55°C to +125°C — MIL-STD-883 Compliant					
45 ns 35 ns 25 ns 20 ns 15 ns 12 ns				L7C199TMB or L7CL199TMB — 45, 35, 25, 20		

4K x 4 CMOS Cache-Tag Static RAM — L7C180/181

FEATURES

- 4K × 4 CMOS Static RAM with 4-bit Tag Comparison Logic
- High Speed Address-to-MATCH — 10 ns maximum
- Totem Pole (L7C180) or Open Drain (L7C181) MATCH Output
- High Speed Flash Clear
- Auto-Powerdown™ Design
- Low Power Operation
  Active: 225 mW typical at 25 ns
  Standby: 100 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 6178, SSL4180, SSL4181, MK41H80, MCM4180
- Package Styles Available:
  22-pin Plastic DIP
  22-pin Sidebraze Hermetic DIP
  22-pin CerDIP
  24-pin SOJ

DESCRIPTION

The **L7C180** and **L7C181** are high performance, low power CMOS static RAMs optimized for use as the address tag comparator in high speed cache memory systems. The storage circuitry is organized as 4096 words by 4-bits per word and includes a 4-bit data comparator with MATCH output. The 4-bit data is input/output on shared I/O pins and comparison performed between 4-bit incoming data and accessed memory locations. Wide tag addresses are easily accommodated by paralleling devices and ANDing or Wire-ORing the MATCH outputs when working with L7C180's or L7C181's respectively. For either device, a low on the MATCH output indicates a data mismatch.

Also provided is a high speed $\overline{\text{CLEAR}}$ control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or flushing the cache.

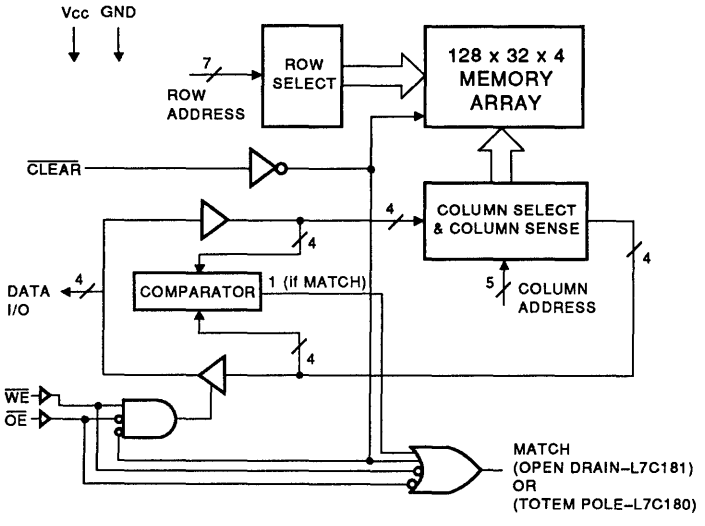
These devices are available in five speed grades with maximum address-to-MATCH times of 10 ns to 25 ns. Operation is from a single +5 V power supply with power consumption only 255 mW (typical) at 25 ns. Dissipation drops to 75 mW (typical) when the memory powers down.

Two power saving standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically whenever the inputs are stable for longer than the minimum access time. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C180 and L7C181 consume only 15 µW (typical) at 3 V allowing effective battery backup operation.

The L7C180 and L7C181 provide fully asynchronous (unclocked) operation with matching access and cycle times. Memory locations are specified on address pins A0 through A11 with functions defined in the Truth Table on the next page. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C180 and L7C181 can withstand an injection current of up to 200 mA on any pin without damage.

L7C180/181 Block Diagram



Truth Table

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	I/O	FUNCTION
X	X	L	H	High Z	Clear all bits to low
H	H	H	L	DIN	No MATCH
H	H	H	H	DIN	MATCH
H	L	H	H	DOUT	Memory Read
L	X	H	H	DIN	Memory Write

X = Don't Care; L = VIL; H = VIH

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground .... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions (Note 5)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = –4.0 mA, VCC = 4.5 V (all except MATCH pin)	2.4			V
	(Note 11)	IOH = –12.0 mA, VCC = 4.5 V (MATCH pin–L7C180)	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA (all except MATCH pin)			0.4	V
	(Note 11)	IOL = 10.0 mA (all except MATCH pin)			0.5	V
		IOL = 24.0 mA (MATCH pin)			0.4	V
		IOL = 30.0 mA (MATCH pin)			0.5	V
VIH	Input High Voltage		2.0		VCC + 0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	V
IIX	Input Current	GND ≤ VIN ≤ VCC	–10		+10	µA
IOZ	Output Leakage Current	GND ≤ VOUT ≤ VCC, $\overline{OE}$ = VCC (except MATCH pin)	–10		+10	µA
IOS	Output Short Current	VOUT = GND, VCC = Max (Note 4)			–350	mA
ICC2	VCC Current, TTL Inactive	(Note 7)		15	30	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		5	12	mA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		1.5	5	mA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

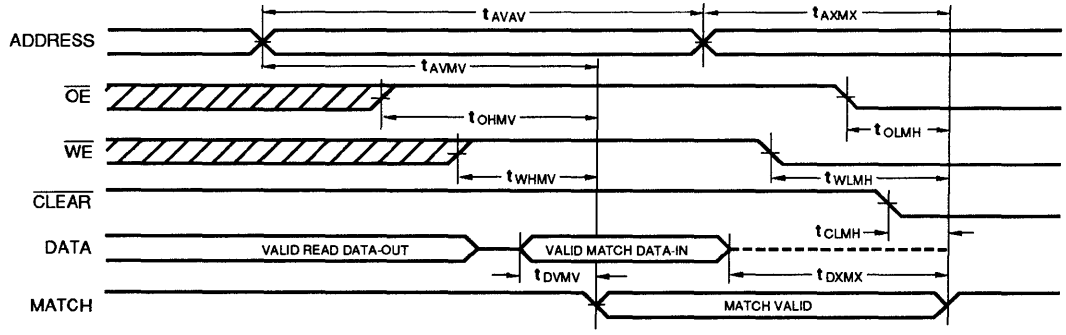
Symbol	Parameter	Test Condition	L7C180/181- 25	20	15	12	10		Unit
ICC1	VCC Current, Active	(Note 6)	65	85	110	135	150		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

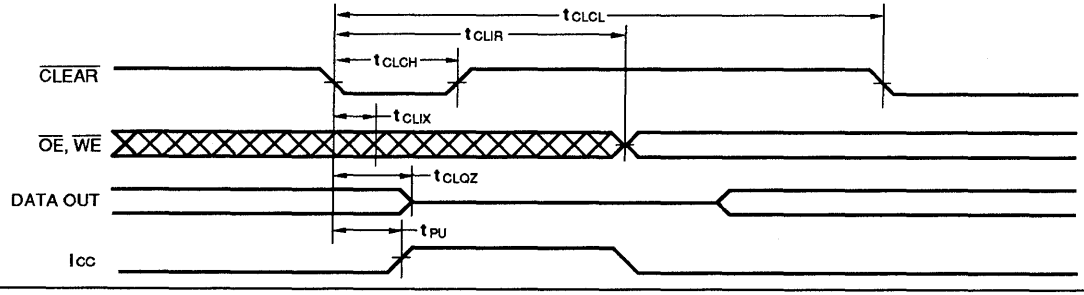
MATCH AND CLEAR CYCLE TIMING (Notes 5, 11, 12, 20, 21, 22)

Symbol	Parameter	L7C180/181- 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max		
tAVAV	MATCH Cycle Time	25		20		15		12		10			
tAVMV	Address Valid to MATCH Valid		22		20		15		12		10		
tAXMX	Address Change to MATCH Change	3		3		3		3		3			
tOHMV	Output Enable High to MATCH Valid		15		15		13		10		8		
tOLMH	Output Enable Low to MATCH High	3		3		3		3		3			
tWHMV	Write Enable High to MATCH Valid		15		15		13		10		8		
tWLMH	Write Enable Low to MATCH High	3		3		3		3		3			
tCLMH	$\overline{\text{CLEAR}}$ Low to MATCH High	0	20	0	15	0	12	0	10	0	8		
tDVMV	Data Valid to MATCH Valid		15		15		13		10		8		
tDXMX	Data Change to MATCH Change	0		0		0		0		0			
tCLCL	$\overline{\text{CLEAR}}$ Cycle Time (23)	55		45		35		30		25			
tCLCH	$\overline{\text{CLEAR}}$ Pulse Width (23)	15		15		12		12		10			
tCLIX	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care (23)	0		0		0		0		0			
tCLQZ	$\overline{\text{CLEAR}}$ Low to Output High Z (18, 19)		15		15		10		10		8		
tCLIR	$\overline{\text{CLEAR}}$ Low to Inputs Recognized (23)		55		45		35		30		25		

MATCH TIMING (Note 17)



CLEAR TIMING (Note 23)

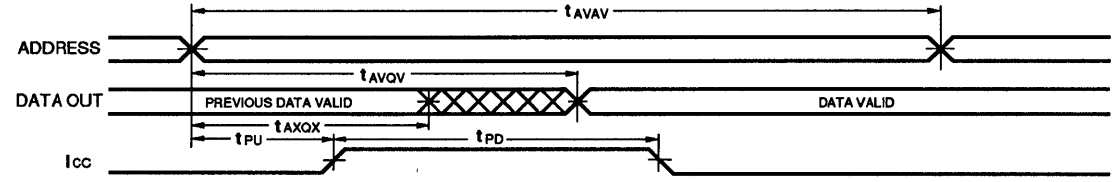


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

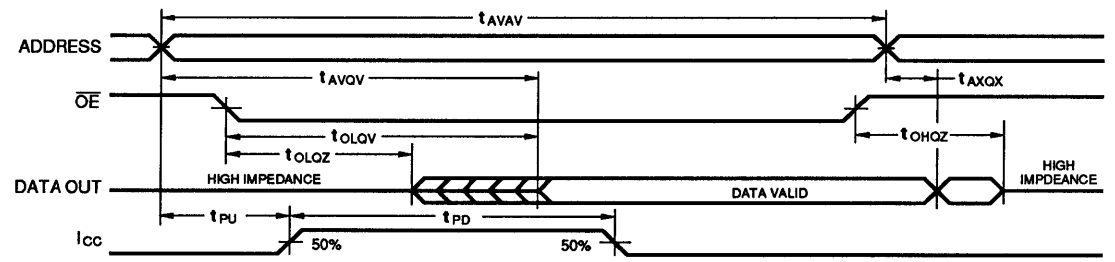
Read Cycle (Notes 5, 11, 12, 20, 21, 22)

Symbol	Parameter	L7C180/181- 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Read Cycle Time	25		20		15		12		10			
tAVQV	Address Valid to Output Valid (13, 14)		25		20		15		12		10		
tAXQX	Address Change to Output Change	3		3		3		3		3			
tOLQV	Output Enable Low to Output Valid		12		10		8		6		4		
tOLQZ	Output Enable Low to Output Low Z (18, 19)	0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (18, 19)		10		8		8		5		4		
tPU	Input Change to Power Up (10, 17)	0		0		0		0		0			
tPD	Power Up to Power Down (10, 17)		25		20		20		20		18		
tCHVL	Control Input High to Data Retention (10)	0		0		0		0		0			

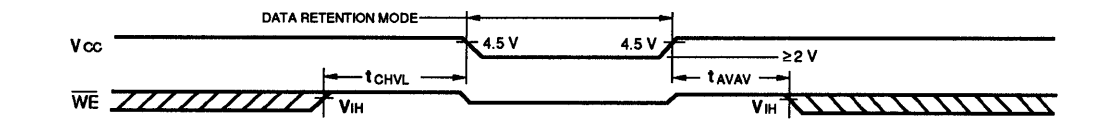
Read Cycle — Address Controlled (Notes 13, 14)



Read Cycle — OE Controlled (Notes 13, 15)



Data Retention

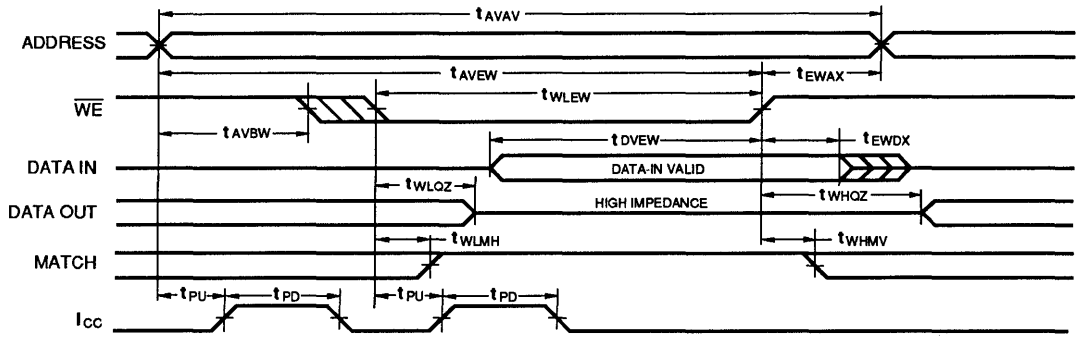


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

Write Cycle (Notes 5, 11, 12, 20, 21, 22)

Symbol	Parameter	L7C180/181- 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Write Cycle Time	20		20		15		12		10			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	15		15		12		10		8			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0			
tWLEW	Write Enable Low to End of Write Cycle	15		15		12		10		8			
tDVEW	Data Valid to End of Write Cycle	10		10		7		6		5			
tEWDX	End of Write Cycle to Data Change	1		1		1		1		1			
tWHQZ	Write Enable High to Output Low Z (18, 19)	0		0		0		0		0			
tWLQZ	Write Enable Low to Output High Z (18, 19)		7		7		5		4		4		

Write Cycle — WE Controlled (Notes 16, 17)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{OE}$, $\overline{WE}$ & $\overline{CLEAR} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs $\ge V_{IH}$. The device is continuously disabled, i.e., $\overline{WE}$, $\overline{OE}$, & $\overline{CLEAR} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{WE}$, $\overline{OE}$, and $\overline{CLEAR} = V_{CC}$. Input levels are within 0.2 V of VCC or GND.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{WE}$, $\overline{OE}$, and $\overline{CLEAR}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Figs. 1a, 1c, and 1d), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{WE}$ high and $\overline{OE}$ low).

15. All address lines are valid t_{AVQV} to t_{OLQV} prior to the $\overline{OE}$ transition to low.

16. The internal write cycle of the memory is defined by $\overline{WE}$ low. The address and data setup and hold times should be referenced to $\overline{WE}$ falling and rising edges.

17. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{WE}$.
b. Transition on any address line.
c. Transition on any data line ($\overline{WE}$ active).
d. Falling edge of $\overline{CLEAR}$.

The device automatically powers down from ICC1 to ICC2 after t_{PD} has elapsed from any of the power up triggers. The exception is $\overline{CLEAR}$ where the device remains powered up for the duration of the Clear cycle. This means that power dissipation is dependent on only cycle rate, and not on Write Enable pulse width.

18. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

19. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This para-meter is sampled and not 100% tested.

20. All address timings are referenced from the last valid address line to the first transitioning address line.

21. WE must be high during address transitions.

22. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

23. The Clear cycle is edge-triggered on the falling edge of $\overline{CLEAR}$. While the internal Clear cycle is in progress, all inputs, including multiple $\overline{CLEAR}$ pulses, are ignored. Inputs are recognized after t_{CLR} has elapsed from the falling edge of $\overline{CLEAR}$. For proper operation, Vcc must be within its specified normal operating voltage prior to assertion of $\overline{CLEAR}$.

FIGURE 1a.

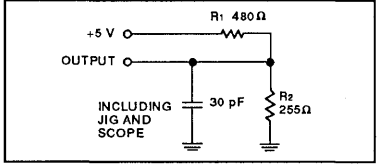


FIGURE 1b.

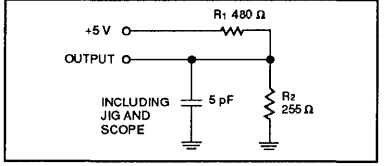


FIGURE 1c. MATCH OUTPUT TOTEM POLE

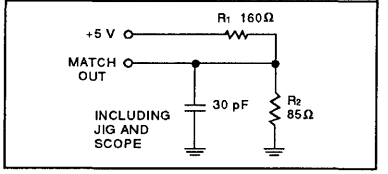


FIGURE 1d. MATCH OUTPUT OPEN DRAIN

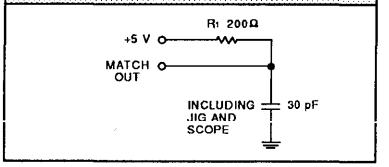
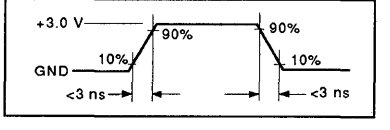
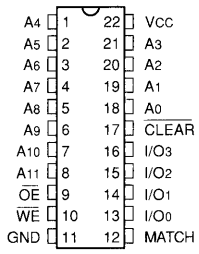


FIGURE 2.

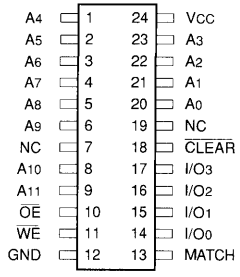


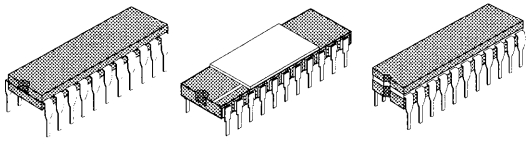
ORDERING INFORMATION

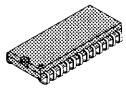
22-pin
(0.3" wide)



24-pin







Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOJ (.300"— W2)		
	0°C to +70°C — Commercial Screening					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C180PC or L7C181PC — 25, 20, 15, 12, 10	L7C180DC or L7C181DC — 25, 20, 15, 12, 10	L7C180CC or L7C181CC — 25, 20, 15, 12, 10	L7C180WC or L7C181WC — 25, 20, 15, 12, 10, 8		
	–55°C to +125°C — Commercial Screening					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C180DM or L7C181DM — 25, 20, 15, 12	L7C180CM or L7C181CM — 25, 20, 15, 12			
	–55°C to +125°C — Extended Screening					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C180DME or L7C181DME — 25, 20, 15, 12	L7C180CME or L7C180CME — 25, 20, 15, 12			
	–55°C to +125°C — MIL-STD-883 Compliant					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C180DMB or L7C181DMB — 25, 20, 15, 12	L7C180CMB or L7C181CMB — 25, 20, 15, 12			

8K x 8 CMOS Cache-Tag Static RAM — L7C174

FEATURES

- 8K × 8 CMOS Static RAM with 8-bit Tag Comparison Logic
- High Speed Address-to-MATCH — 12 ns maximum
- High Speed Flash Clear
- High Speed Read Access Time — to 12 ns maximum
- Auto-Powerdown™ Design
- Low Power Operation
  Active: 320 mW typical at 35 ns
  Standby: 500 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 7174, MK48H74
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze Hermetic DIP
  - 28-pin CerDIP
  - 28-pin SOJ
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C174** is a high performance, low power CMOS static RAM optimized for use as the address tag comparator in high speed cache memory systems. One L7C174 can be used to map 8K cache lines into a 1 megabyte address space by comparing 20 address bits organized as 13-line address bits and 7-page address bits.

The storage circuitry is organized as 8192 words by 8 bits per word and includes an 8-bit data comparator with MATCH output. The 8-bit data is input/output on shared I/O pins and comparison performed between 8 bit incoming data and accessed memory locations. Also provided is a high speed $\overline{\text{CLEAR}}$ control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or when flushing the cache.

This device is available in five speed grades with maximum address-to-MATCH times of 12 ns to 35 ns. Operation is from a single +5 V power supply with power consumption only 320 mW (typical) at 35 ns. Dissipation drops to 75 mW (typical) when the memory is deselected (Enable is high).

Two power saving standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically whenever the inputs are stable for longer than the minimum access time, or when the memory is deselected. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C174 consumes only 30 µW (typical) at 3 V allowing effective battery backup operation.

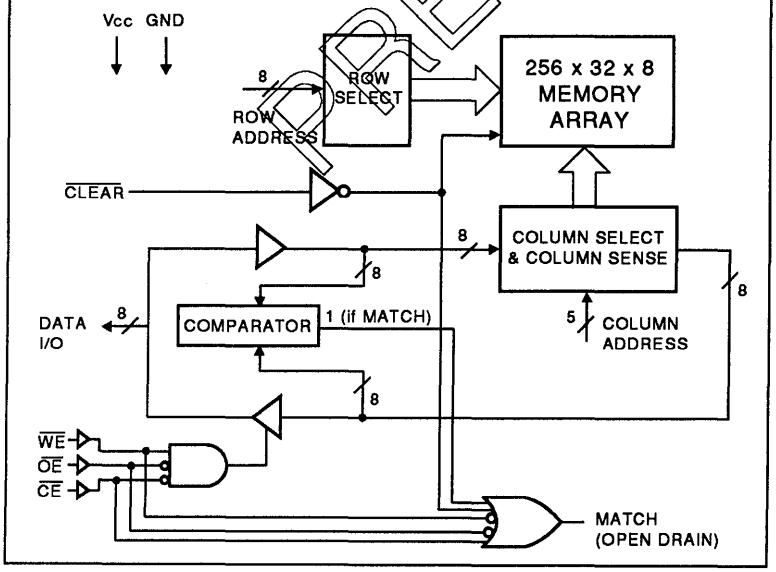
The L7C174 provides fully asynchronous (unclocked) operation with matching access and cycle times. An active low Chip Enable and Output Enable along with a three state I/O bus simplify the connection of several chips for increased storage capacity. Wide tag addresses are easily accommodated by paralleling devices and wire-ORing the MATCH outputs.

Memory locations are specified on address pins A_0 through A_{12} with functions defined in the Truth Table on the next page.

During $\overline{\text{CLEAR}}$ the state of the I/O pins remain completely defined by the $\overline{\text{WE}}$, $\overline{\text{CE}}$, and $\overline{\text{OE}}$ control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C174 can withstand an injection current of up to 200 mA an any pin without damage.

L7C174 Block Diagram



Truth Table

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{CLEAR}$	MATCH	I/O	Function
X	X	X	L	H	—	Reset all bits to low
X	H	X	H	H	High Z	Deselect chip
H	L	H	H	L	DIN	No MATCH
H	L	H	H	H	DIN	MATCH
H	L	L	H	H	DOUT	Read
L	L	X	H	H	DIN	Write

X = Don't Care; L = VIL; H = VIH

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
VCC supply voltage with
respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground.... –3.0 V to +7.0 V
Signal applied to high
impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = –4.0 mA, VCC = 4.5 V (except MATCH pin)	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA (all except MATCH pin)			0.4	V
		IOL = 10.0 mA (all except MATCH pin)			0.5	V
		IOL = 18.0 mA (MATCH pin)			0.4	V
		IOL = 22.0 mA (MATCH pin)			0.5	V
VIH	Input High Voltage		2.0		VCC + 0.3	V
VIL	Input Low Voltage	(Note 3)	–3.0		0.8	V
IIX	Input Current	GND ≤ VIN ≤ VCC	–10		+10	µA
IOZ	Output Leakage Current	GND ≤ VOUT ≤ VCC, $\overline{CE}$ = VCC	–10		+10	µA
IOS	Output Short Current	VOUT = GND, VCC = Max (Note 4)			–350	mA
ICC2	VCC Current, TTL Inactive	(Note 7)		15	30	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		100	500	µA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		10	250	µA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

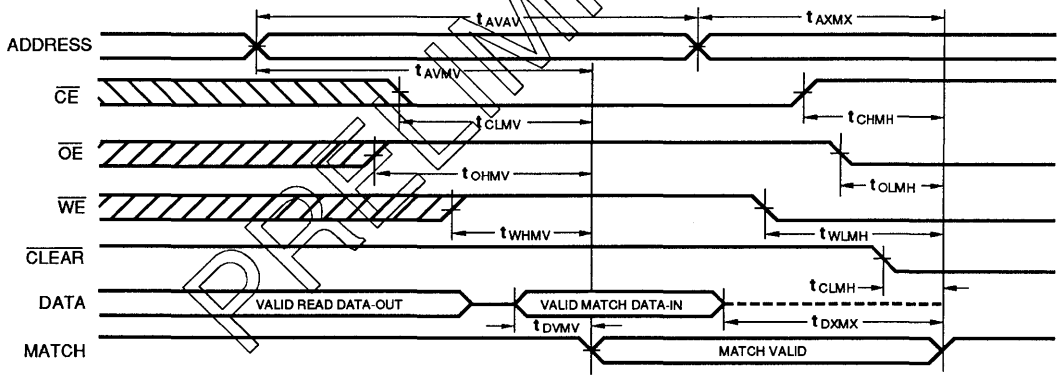
			L7C174-						
Symbol	Parameter	Test Condition	35	25	20	15	12		Unit
ICC1	VCC Current, Active	(Note 6)	110	150	185	240	275		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

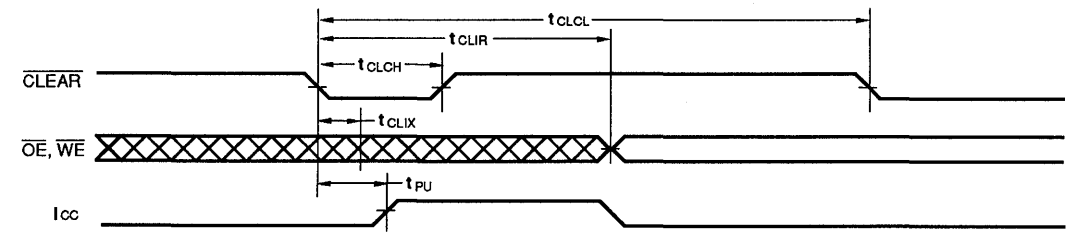
MATCH AND CLEAR CYCLE TIMING (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C174- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max				
t_{AVAV}	MATCH Cycle Time	35		25		20		15		12					
t_{AVMV}	Address Valid to MATCH Valid		30		22		20		15		12				
t_{AXMX}	Address Change to MATCH Change	3		3		3		3		3					
t_{CLMV}	Chip Enable Low to MATCH Valid		20		15		10		10		8				
t_{CHMH}	Chip Enable High to MATCH High		20		15		10		10		8				
t_{OHMV}	Output Enable High to MATCH Valid		20		15		15		13		10				
t_{OLMH}	Output Enable Low to MATCH High		25		20		15		12		10				
t_{WHMV}	Write Enable High to MATCH Valid		20		15		15		13		10				
t_{WLMH}	Write Enable Low to MATCH High		25		20		15		12		10				
t_{CLMH}	$\overline{CLEAR}$ Low to MATCH High	0	25	0	20	0	15	0	12	0	10				
t_{DVMV}	Data Valid to MATCH Valid		20		15		15		13		10				
t_{DXMX}	Data Change to MATCH Change	0		0		0		0		0					
t_{CLCL}	$\overline{CLEAR}$ Cycle Time	65		55		45		35		30					
t_{CLCH}	$\overline{CLEAR}$ Pulse Width	20		15		15		12		12					
t_{CLIX}	$\overline{CLEAR}$ Low to Inputs Don't Care	0		0		0		0		0					
t_{CLIR}	$\overline{CLEAR}$ Low to Inputs Recognized		65		55		45		35		30				

MATCH TIMING (Note 19)



CLEAR TIMING (Note 25)

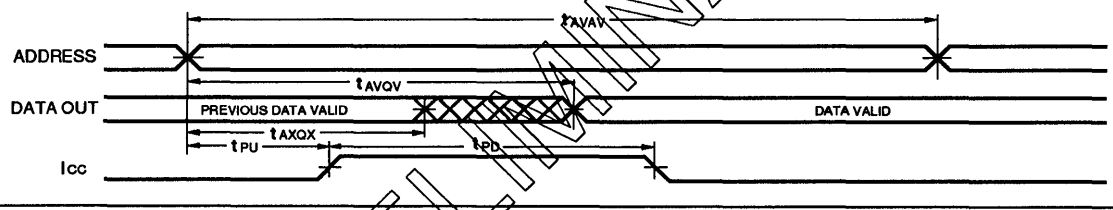


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

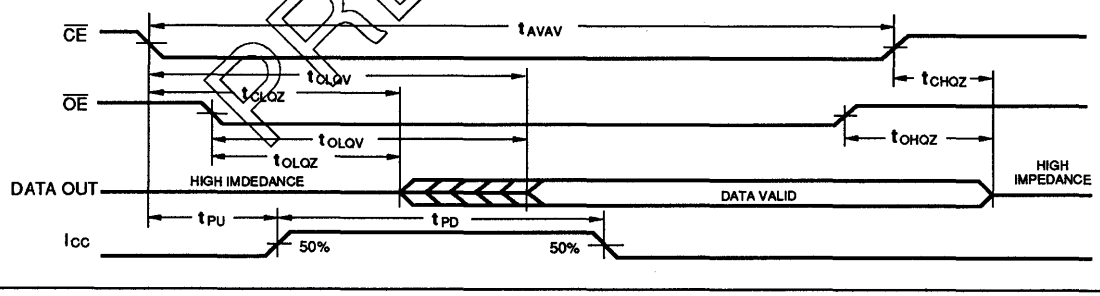
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C174- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max				
tAVAV	Read Cycle Time	35		25		20		15		12					
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12				
tAXQX	Address Change to Output Change	3		3		3		3		3					
tCLQV	Chip Enable Low to Output Valid (13, 15)		35		25		20		15		12				
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3		3					
tCHQZ	Chip Enable High to Output High Z (20, 21)		15		10		8		8		5				
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6				
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0					
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5				
tPU	$\overline{CE}$ or $\overline{WE}$ Low to Power Up (10, 19)	0		0		0		0		0					
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20				
tCHVL	Chip Enable High to Data Retention (10)	0		0		0		0		0					

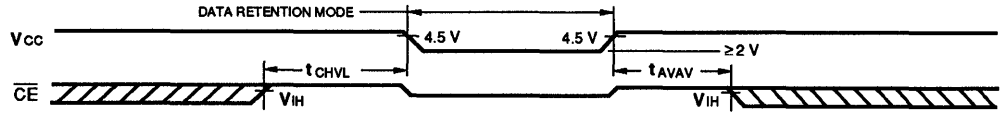
Read Cycle — Address Controlled (Notes 13, 14)



Read Cycle — $\overline{CE}$/$\overline{OE}$ Controlled (Notes 13, 15)



Data Retention

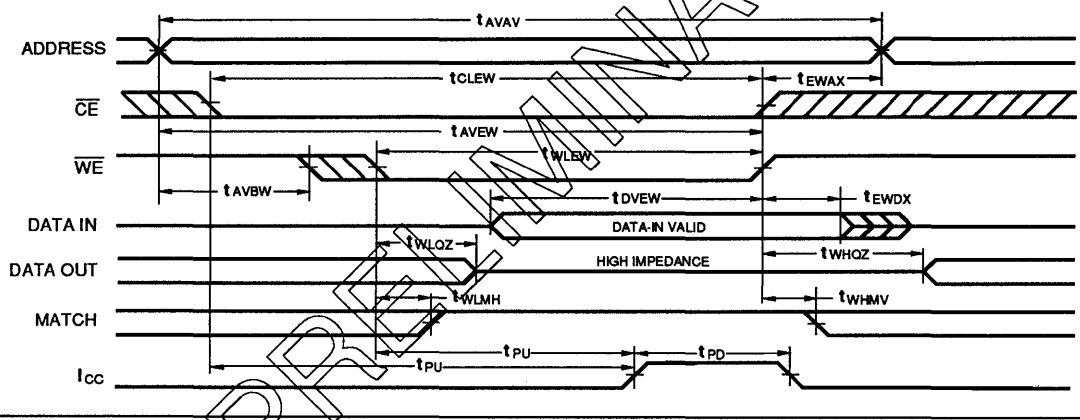


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

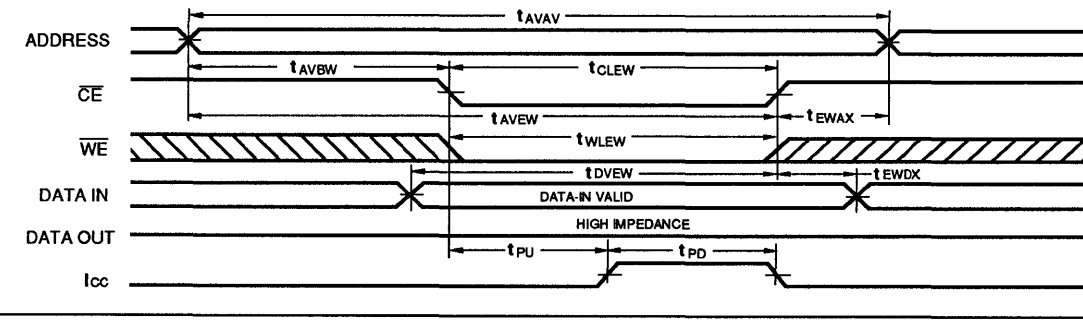
Write Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C174- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12					
tCLEW	Chip Enable Low to End of Write Cycle	25		15		15		12		10					
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0					
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10					
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0					
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10					
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6					
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0					
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0					
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4				

Write Cycle — $\overline{WE}$ Controlled (Notes 16, 17, 18, 19)



Write Cycle — $\overline{CE}$ Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at 0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$, $\overline{WE}$, and $\overline{OE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.2 V of VCC or GND.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.2 V. For all other inputs VIN ≥ VCC – 0.2 V or VIN ≤ 0.2 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Figs. 1a, 1c), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ active and $\overline{WE}$ low. Both signals must be active to initiate a write. Either signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going active, the output remains in a high impedance state.

18. If $\overline{CE}$ goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:
a. Falling edge of $\overline{CE}$.
b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).
c. Transition on any address line ($\overline{CE}$ active).
d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).
e. Falling edge of $\overline{CLEAR}$.
The device automatically powers down from ICC1 to ICC2 after t_{PD} has elapsed from any of the power up triggers. The exception is $\overline{CLEAR}$ where the device remains powered up for the duration of the Clear cycle. This means that power dissipation is dependent on only cycle rate, and not on Write Enable pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

25. The Clear cycle is edge-triggered on the falling edge of $\overline{CLEAR}$. While the internal Clear cycle is in progress, all inputs, including multiple $\overline{CLEAR}$ pluses, are ignored. Inputs are recognized after t_{CLR} has elapsed from the falling edge of $\overline{CLEAR}$. For proper operation, Vcc must be within its specified normal operating voltage prior to assertion of $\overline{CLEAR}$.

FIGURE 1a.

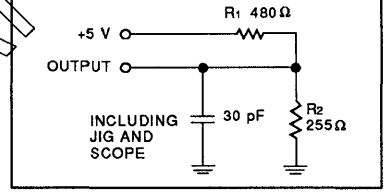


FIGURE 1b.

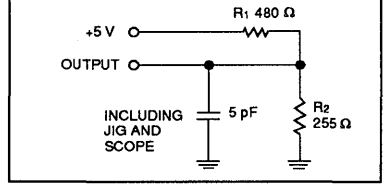


FIGURE 1c.

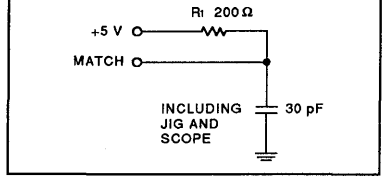
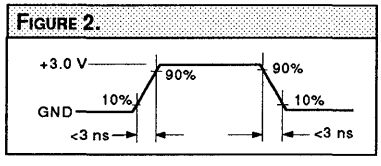
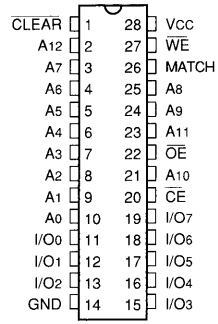


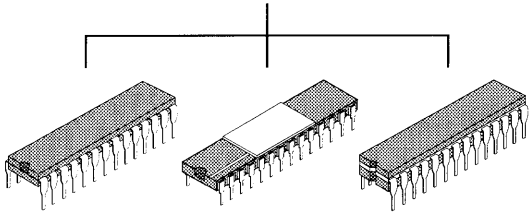
FIGURE 2.



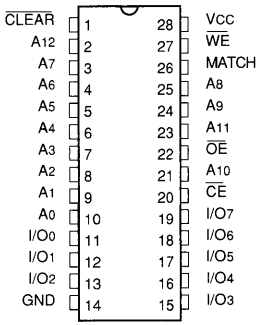
ORDERING INFORMATION

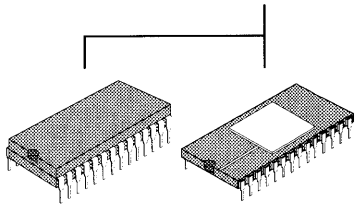
28-pin (0.3" wide)





28-pin (0.6" wide)

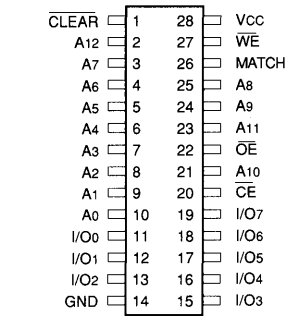




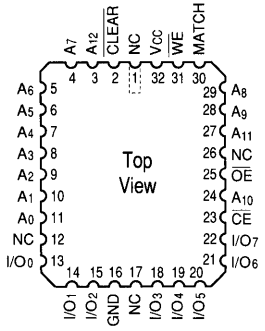
Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic DIP (P9)	Sidebraze Hermetic DIP (D9)
	0°C to +70°C — Commercial Screening				
35 ns	L7C174PC35	L7C174DC35	L7C174CC35	L7C174NC35	L7C174HC35
25 ns	" " 25	" " 25	" " 25	" " 25	" " 25
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20
15 ns	" " 15	" " 15	" " 15	" " 15	" " 15
12 ns	" " 12	" " 12	" " 12	" " 12	" " 12
10 ns					
8 ns					
	–55°C to +125°C — Commercial Screening				
35 ns		L7C174DM35	L7C174CM35		L7C174HM35
25 ns		" " 25	" " 25		" " 25
20 ns		" " 20	" " 20		" " 20
15 ns		" " 15	" " 15		" " 15
12 ns					
10 ns					
8 ns					
	–55°C to +125°C — Extended Screening				
35 ns		L7C174DME35	L7C174CME35		L7C174HME35
25 ns		" " 25	" " 25		" " 25
20 ns		" " 20	" " 20		" " 20
15 ns		" " 15	" " 15		" " 15
12 ns					
10 ns					
8 ns					
	–55°C to +125°C — MIL-STD-883 Compliant				
35 ns		L7C174DMB35	L7C174CMB35		L7C174HMB35
25 ns		" " 25	" " 25		" " 25
20 ns		" " 20	" " 20		" " 20
15 ns		" " 15	" " 15		" " 15
12 ns					
10 ns					
8 ns					

ORDERING INFORMATION

28-pin



32-pin
(450 x 550)



Speed	Plastic SOJ (.300"— W2)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
35 ns	L7C174WC35	L7C174TC35
25 ns	" " 25	" " 25
20 ns	" " 20	" " 20
15 ns	" " 15	" " 15
12 ns	" " 12	" " 12
10 ns		
8 ns		
	–55°C to +125°C — Commercial Screening	
35 ns		L7C174TM35
25 ns		" " 25
20 ns		" " 20
15 ns		" " 15
12 ns		
10 ns		
8 ns		
	–55°C to +125°C — Extended Screening	
35 ns		L7C174TME35
25 ns		" " 25
20 ns		" " 20
15 ns		" " 15
12 ns		
10 ns		
8 ns		
	–55°C to +125°C — MIL-STD-883 Compliant	
35 ns		L7C174TMB35
25 ns		" " 25
20 ns		" " 20
15 ns		" " 15
12 ns		
10 ns		
8 ns		

8K x 8 Static RAM with Flash Clear (Low Power)

L7C186/L7CL186

FEATURES

- 8K × 8 CMOS Static RAM with High Speed Flash Clear
- Auto-Powerdown™ Design
- High Speed Read Access Time — 12 ns maximum
- Industry Standard Pinout
- Low Power Operation
  Active:
  320 mW (typical) at 35 ns
  Standby (typical):
  500 µW (L7C186)
  250 µW (L7CL186)
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT7165
- Package Styles Available:
  28-pin Plastic DIP
  28-pin Sidebraze Hermetic DIP
  28-pin CerDIP
  28-pin SOJ
  32-pin Ceramic LCC

DESCRIPTION

The **L7C186** and **L7CL186** are high performance, low power CMOS static RAM with a high speed Flash Clear feature. The storage circuitry is organized as 8192 words by 8 bits per word with the 8-bit data input/output on shared I/O pins. The device is offered in the industry standard 8K × 8 SRAM pinout with the Flash Clear function implemented on Pin 1 which is normally a no-connect.

These devices are available in five speed grades with maximum access times of 12 ns to 35 ns. Operation is from a single +5 V power supply. Power consumption for the L7C186 is 320 mW (typical). Dissipation drops to 75 mW (typical) for the L7C186 and 60 mW for the L7CL186 when the memory is in Auto-Powerdown™ mode. To speed switching and reduce ground bounce noise proprietary 3-V™ output circuitry is incorporated to limit V_{OH} swings, while still maintaining full TTL compatibility.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses that are longer than the minimum access time, or when the memory is is put into powerdown mode by deselecting $\overline{CE}_2$. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C186 and L7CL186 consume only 30 µW and 15 µW (typical) respectively at 3 V, allowing effective battery backup operation.

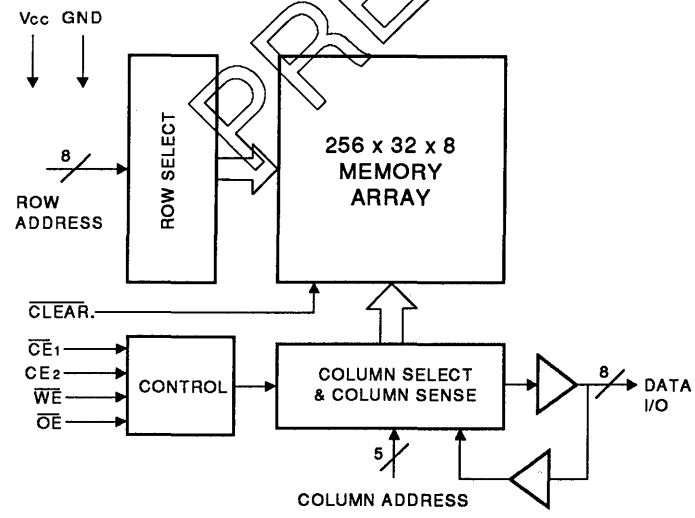
The L7C186 and L7CL186 provide fully asynchronous (unclocked) operation with matching access and cycle times. Two Chip Enables and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{12} with functions defined in the Truth Table on the next page.

During $\overline{CLEAR}$, the state of the I/O pins remain completely defined by the $\overline{WE}$, $\overline{CE}_1$, CE_2, and $\overline{OE}$ control inputs. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C186 and L7CL186 can withstand an injection current of up to 200 mA an any pin without damage.

L7C186/L7CL186 Block Diagram



Truth Table

$\overline{WE}$	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{CLEAR}$	I/O	Function
X	X	X	X	L	—	Reset Memory to 0
H	L	H	L	H	DOUT	Memory Read
L	L	H	X	H	DIN	Memory Write
H	L	H	H	H	High Z	Output Disable
X	H	X	X	H	High Z	Chip Deselect
X	X	L	X	H	High Z	Chip Deselect & Powerdown

X = Don't Care; L = V_{IL}; H = V_{IH}

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground .... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 200 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics

Over Operating Conditions (Note 5)

			L7C186			L7CL186			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10		+10	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–350			–350	mA
I_{CC2}	V_{CC} Current,TTL Inactive	(Note 7)		15	30		12	20	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		100	500		50	150	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	250		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

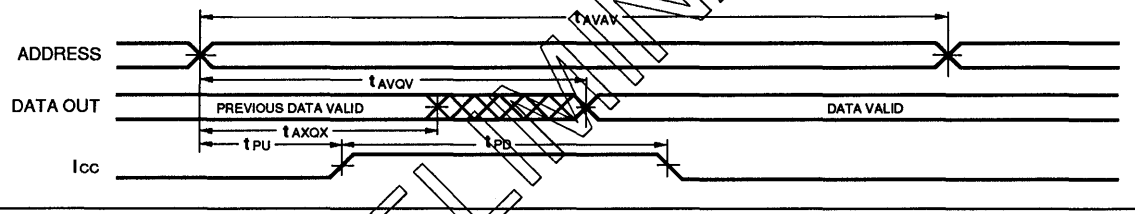
			L7C186-							
Symbol	Parameter	Test Condition	35	25	20	15	12			Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	110	150	185	240	275			mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

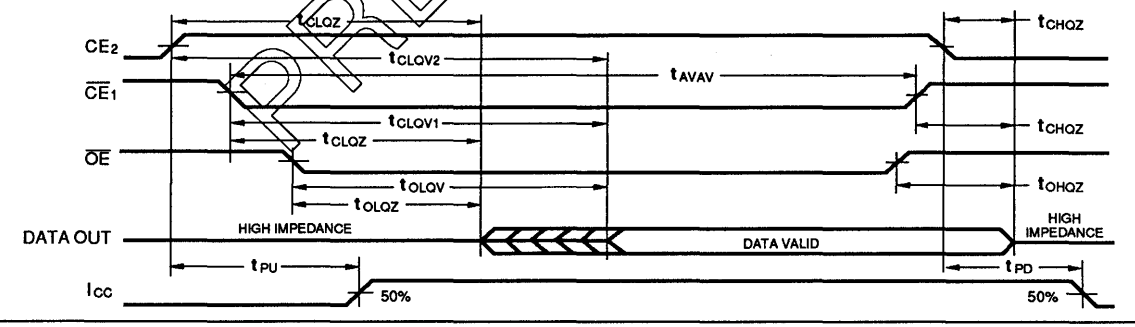
READ CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C186/L7CL186- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	Min	Max
tAVAV	Read Cycle Time	35		25		20		15		12			
tAVQV	Address Valid to Output Valid (13, 14)		35		25		20		15		12		
tAXQX	Address Change to Output Change	3		3		3		3		3			
tCLQV1	$\overline{CE}_1$ Low to Output Valid (13, 15)		15		12		10		8		6		
tCLQV2	CE_2 High to Output Valid (13, 15)		35		25		20		15		12		
tCLQZ	Chip Enable Active to Output Low Z (20, 21)	3		3		3		3		3			
tCHQZ	Chip Enable Inactive to Output High Z (20, 21)		15		10		8		8		5		
tOLQV	Output Enable Low to Output Valid		15		12		10		8		6		
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0		0			
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		5		5		
tPU	Input Transition to Power Up (10, 19)	0		0		0		0		0			
tPD	Power Up to Power Down (10, 19)		35		25		20		20		20		
tCHVL	Chip Enable Inactive to Data Retention (10)	0		0		0		0		0			

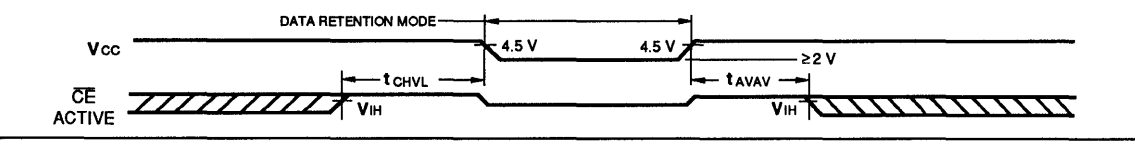
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — CE/OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

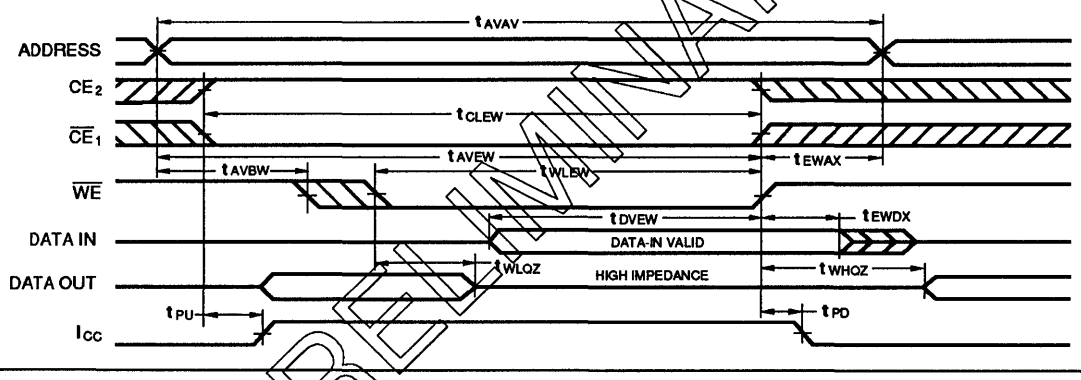


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

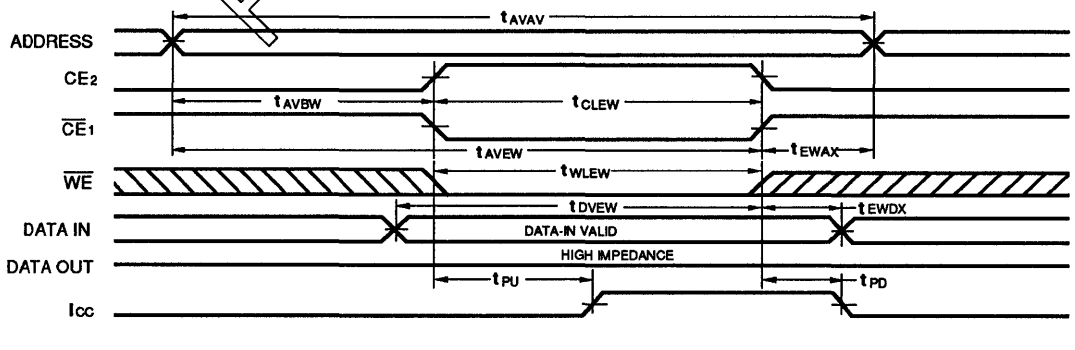
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

		L7C186/L7CL186-									
		35		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tAVAV	Write Cycle Time	25		20		20		15		12	
tCLEW	Chip Enable Active to End of Write Cycle	25		15		15		12		10	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	25		15		15		12		10	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	20		15		15		12		10	
tDVEW	Data Valid to End of Write Cycle	15		10		10		7		6	
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		10		7		7		5		4

WRITE CYCLE — WE CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — CE CONTROLLED *(Notes 16, 17, 18, 19)*

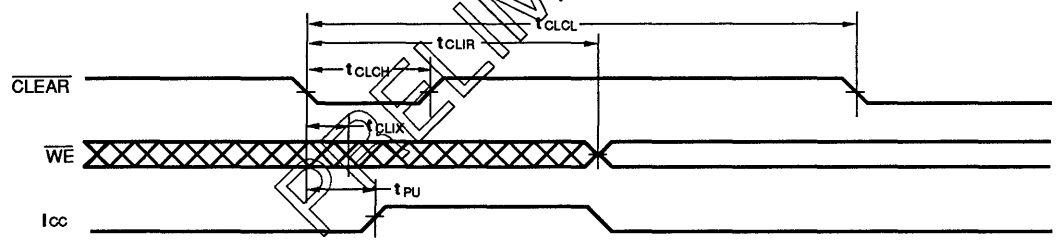


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

CLEAR Cycle Timing (Notes 5, 11, 12, 22, 23, 24, 25)

Symbol	Parameter	L7C186/L7CL186- 35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	Min	Max
t_{CLCL}	$\overline{CLEAR}$ Cycle Time	65		55		45		35		30			
t_{CLCH}	$\overline{CLEAR}$ Pulse Width	20		15		15		12		12			
t_{CLIX}	$\overline{CLEAR}$ Low to Inputs Don't Care	0		0		0		0		0			
t_{CLIR}	$\overline{CLEAR}$ Low to Inputs Recognized		65		55		45		35		30		

CLEAR Cycle Timing (Note 25)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE1} \le VIL$, CE2 and $\overline{WE} \le VIL$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE1} \ge VIH$, $CE2 \le VIL$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE1}$ = VCC, CE2 = GND. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE1}$ must be ≥ VCC – 0.2 V. For the L7C185, all other inputs meet VIN ≤ 0.2 V or VIN ≥ VCC –0.2 V to ensure full powerdown. For the L7CL185, this requirement applies only to $\overline{CE}$ and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE1}$ low, CE2 high).

15. All address lines are valid prior to or coincident with the later of $\overline{CE1}$ and CE2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with later of $\overline{CE1}$ and CE2 going active, the output remains in a high impedance state.

18. If $\overline{CE1}$ and CE2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Rising edge of CE2.

b. Falling edge of $\overline{WE}$ ($\overline{CE1}$, $\overline{CE2}$ active).

c. Transition on any address line ($\overline{CE1}$, CE2 active).

d. Transition on any data line ($\overline{CE1}$, CE2, and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE1}$, CE2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

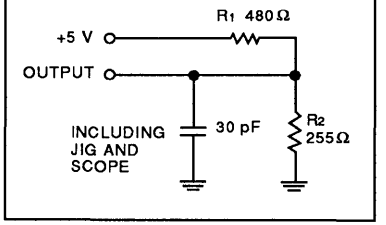


FIGURE 1b.

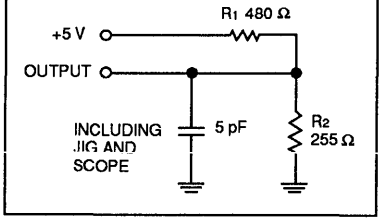
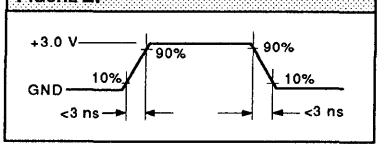
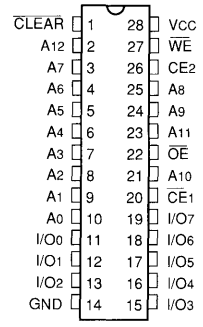


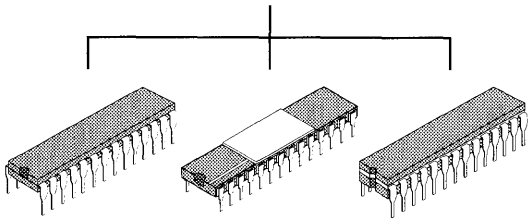
FIGURE 2.



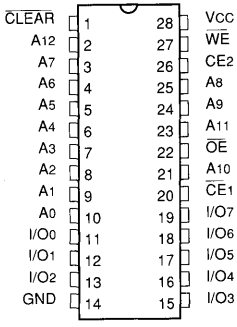
ORDERING INFORMATION

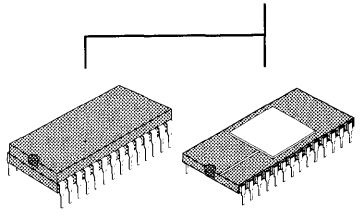
28-pin (0.3" wide)





28-pin (0.6" wide)

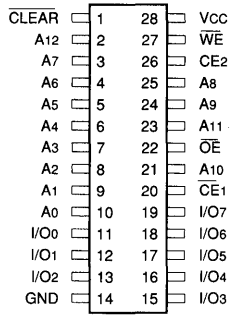


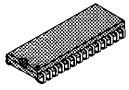


Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	CerDIP (C5)	Plastic DIP (P9)	Sidebraze Hermetic DIP (D9)
	0°C to +70°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C186PC / L7CL186PC — 35 / 25 / 20 / 15 / 12	L7C186DC / L7CL186DC — 35 / 25 / 20 / 15 / 12	L7C186CC / L7CL186CC — 35 / 25 / 20 / 15 / 12	L7C186NC / L7CL186NC — 35 / 25 / 20 / 15 / 12	L7C186HC / L7CL186HC — 35 / 25 / 20 / 15 / 12
	–55°C to +125°C — Commercial Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C186DM / L7CL186DM — 35 / 25 / 20 / 15	L7C186CM / L7CL186CM — 35 / 25 / 20 / 15		L7C186HM / L7CL186HM — 35 / 25 / 20 / 15
	–55°C to +125°C — Extended Screening				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C186DME / L7CL186DME — 35 / 25 / 20 / 15	L7C186CME / L7CL186CME — 35 / 25 / 20 / 15		L7C186HME / L7CL186HME — 35 / 25 / 20 / 15
	–55°C to +125°C — MIL-STD-883 Compliant				
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C186DMB / L7CL186DMB — 35 / 25 / 20 / 15	L7C186CMB / L7CL186CMB — 35 / 25 / 20 / 15		L7C186HMB / L7CL186HMB — 35 / 25 / 20 / 15

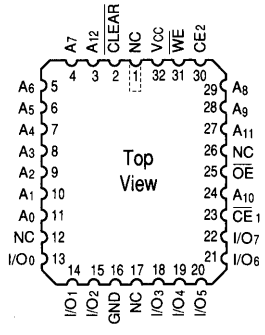
ORDERING INFORMATION

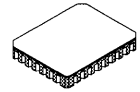
28-pin





32-pin
(450 x 550)





Speed	Plastic SOJ (.300"— W2)		Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C186VC or L7CL186VC — 35 / 25 / 20 / 15 / 12	L7C186WC or L7CL186WC — 35 / 25 / 20 / 15 / 12	L7C186TC or L7CL186TC — 35 / 25 / 20 / 15 / 12
	–55°C to +125°C — Commercial Screening		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L7C186TM or L7CL186TM — 35 / 25 / 20 / 15
	–55°C to +125°C — Extended Screening		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L7C186TME or L7CL186TME — 35 / 25 / 20 / 15
	–55°C to +125°C — MIL-STD-883 Compliant		
35 ns 25 ns 20 ns 15 ns 12 ns 10 ns 8 ns			L7C186TMB or L7CL186TMB — 35 / 25 / 20 / 15

2 x 4K x 16 Cache-Data Static RAM — L7C183/184

FEATURES

- 2 × 4K × 16 or 8K × 16 Cache-Data Static RAM with Direct Map or Two-Way Set Associative
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 20 ns worst-case
- Low Power Operation
  Active: 700 mW typical at 45 ns
  Standby: 75 mW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with Cypress CY7C183/184
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 48-pin Ceramic LCC
  - 52-pin Plastic LCC

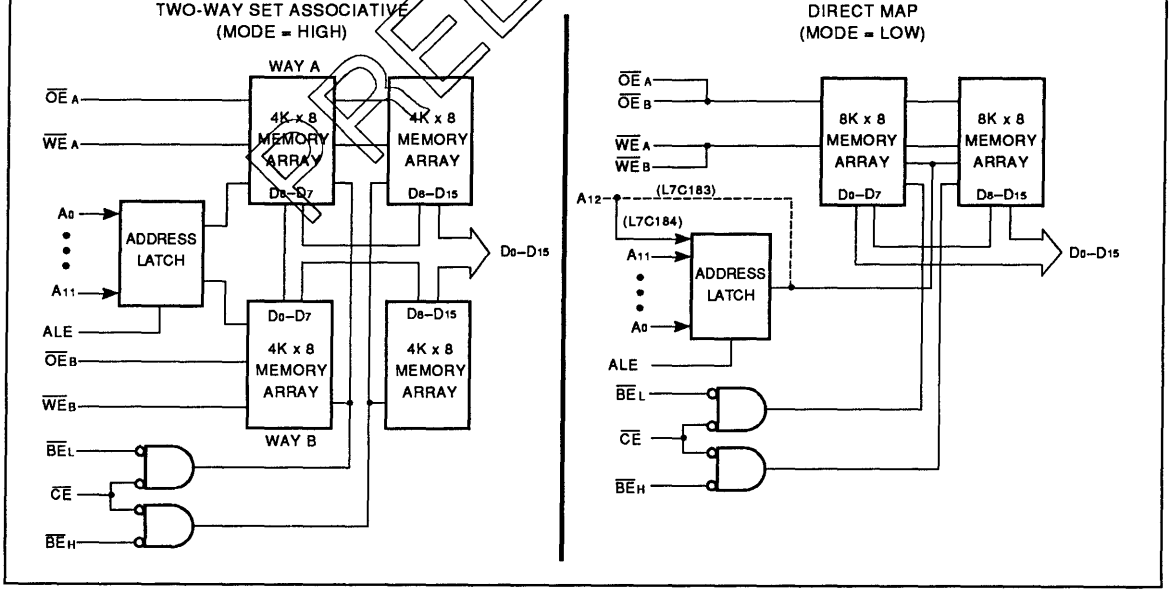
DESCRIPTION

The **L7C183** and **L7C184** are high-performance, low-power CMOS static RAMs which contain 128K bits organized into either two, two-way set associative blocks of 4K × 16 RAM, or one directly mapped 8K × 16-bit RAM.

The L7C183 and L7C184 are designed specifically for use with the Intel 82385 Cache Controller. Addresses are latched on the falling edge of the Address Latch Enable (ALE) signal. When ALE is HIGH, the latch is transparent. The L7C183 has all address bits latched by the ALE signal except A12, which is unlatched. A12, which bypasses the latch, has a faster access time. All address bits are latched by the ALE signal in the L7C184. The mode pin controls whether the L7C183 and L7C184 are configured as direct mapped 8K × 16 or two-way set associative 2 × 4K × 16 RAMs. When mode is HIGH, the circuits are placed in the two-way mode. In the two-way mode, the upper address bit, A12 is a "don't care", and should be externally wired to ground. When mode is LOW, the circuits are placed in the direct mapped mode.

Writing is accomplished in the two-way mode by taking $\overline{CE}$ LOW and by inserting the respective $\overline{BE}$x and $\overline{WE}$x signals LOW. $\overline{BE}_L$ enables bits D0–D7 while $\overline{BE}_H$ enables bits D8–D15. $\overline{WE}_A$ enables cache bank A, and $\overline{WE}_B$ enables cache bank B to receive whatever data resides on the data bus. $\overline{OE}_A$ and $\overline{OE}_B$ similarly enable cache banks A and B, respectively, to drive the data bus. Writing is accomplished in the direct mode by tying $\overline{WE}_A$ and $\overline{WE}_B$ together externally, and using A12 to determine which 4K × 16 memory bank is selected.

L7C183/184 Block Diagram



Reading is accomplished in the two-way mode by taking $\overline{CE}$ LOW, inserting the respective $\overline{OE}$x and $\overline{BE}$x signals LOW, and the respective $\overline{WE}$x signal HIGH. The contents of the memory location specified on the address pins which appear on the 16 outputs. Activation of $\overline{OE}_A$ and $\overline{OE}_B$ simultaneously will cause both banks to be deselected. Reading is accomplished in the direct mode by tying $\overline{OE}_A$ and $\overline{OE}_B$ together externally. A_{12} will determine which 4K × 16 memory bank is enabled.

Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 700 mW (typical) at 45 ns.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read accesses which are longer than the minimum access time, or when the memory is deselected and addresses do not change (stable). In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The memory typically consumes only 9 mW at 3 V, allowing effective battery backup operation.

Latchup and static discharge protection are provided on-chip. The L7C183 and L7C184 can withstand an injection current of up to 200 mA on any pin without damage.

Truth Table — Two-Way Mode (MODE = HIGH)

$\overline{CE}$	$\overline{BE}_L$	$\overline{BE}_H$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation	
H	X	X	X	X	X	X	Outputs Hi-Z, Write Disabled	
L	H	H	X	X	X	X	Outputs Hi-Z, Write Disabled	
X	X	X	H	H	X	X	Outputs Hi-Z	
X	X	X	L	L	X	X	Outputs Hi-Z	
L	L	H	L	H	H	H	Read I/O_0–I/O_7	Way A
L	L	H	H	L	H	H	Read I/O_0–I/O_7	Way B
L	H	L	L	H	H	H	Read I/O_8–I/O_{15}	Way A
L	H	L	H	L	H	H	Read I/O_8–I/O_{15}	Way B
L	L	L	L	H	H	H	Read I/O_0–I/O_{15}	Way A
L	L	L	H	L	H	H	Read I/O_0–I/O_{15}	Way B
L	L	H	X	X	L	H	Write I/O_0–I/O_7	Way A
L	L	H	X	X	H	L	Write I/O_0–I/O_7	Way B
L	H	L	X	X	L	H	Write I/O_8–I/O_{15}	Way A
L	H	L	X	X	H	L	Write I/O_8–I/O_{15}	Way B
L	L	L	X	X	L	H	Write I/O_0–I/O_{15}	Way A
L	L	L	X	X	H	L	Write I/O_0–I/O_{15}	Way B
L	L	H	X	X	L	L	Write I/O_0–I/O_7	Way A & B
L	H	L	X	X	L	L	Write I/O_8–I/O_{15}	Way A & B
L	L	L	X	X	L	L	Write I/O_0–I/O_{15}	Way A & B

Truth Table — Direct Mode (MODE = LOW)

$\overline{CE}$	$\overline{BE}_L$	$\overline{BE}_H$	$\overline{OE}_A$	$\overline{OE}_B$	$\overline{WE}_A$	$\overline{WE}_B$	Operation
H	X	X	X	X	X	X	Outputs Hi-Z, Write Disabled
L	H	H	X	X	X	X	Outputs Hi-Z, Write Disabled
X	X	X	H	H	X	X	Outputs Hi-Z
L	L	H	L	L	H	H	Read I/O_0–I/O_7
L	H	L	L	L	H	H	Read I/O_8–I/O_{15}
L	L	L	L	L	H	H	Read I/O_0–I/O_{15}
L	L	H	X	X	L	L	Write I/O_0–I/O_7
L	H	L	X	X	L	L	Write I/O_8–I/O_{15}
L	L	L	X	X	L	L	Write I/O_0–I/O_{15}

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–0.5 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –1.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, V_{CC} = Min.			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–350	mA
I_{CC2}	V_{CC} Current, Standby	(Note 8)		50	250	µA
I_{CC3}	V_{CC} Current, DR Mode	V_{CC} = 3.0 V (Note 9)		3.0	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

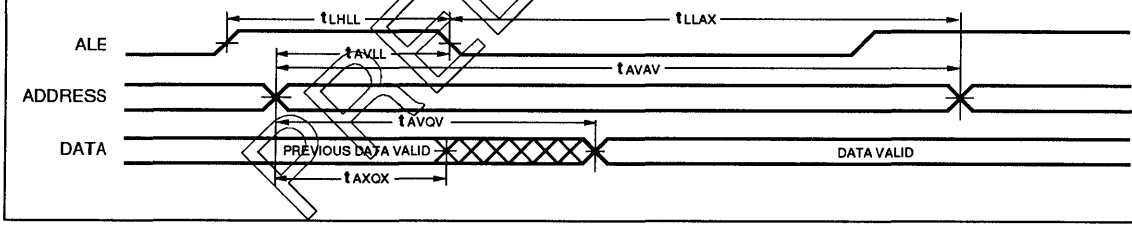
			L7C183/184-				
Symbol	Parameter	Test Condition	45	35	25	20	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	170	220	300	370	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

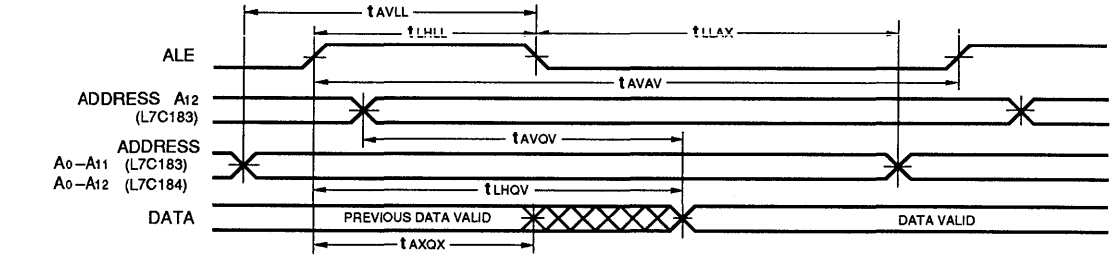
Read Cycle (Notes 5, 11, 12, 22, 23, 24)

Symbol	Parameter	L7C183/184- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max
tAVAV	Read Cycle Time	45		35		25		20	
tAVQV	Address Valid to Output Valid, A_0–A_{11} (13, 14)		45		35		25		20
tAVQV	Address Valid to Output Valid, A_{12} (13, 14)		35		25		17		12
tAXQX	Address Change to Output Change	3		3		3		3	
tLHQV	ALE High to Output Valid		45		35		25		20
tCLQV	Chip Enable Low to Output Valid (13, 15)		20		15		12		10
tBLQV	Byte Enable Low to Output Valid (13, 15)		20		15		12		10
tOLQV	Output Enable Low to Output Valid (13, 15, 20)		16		14		10		10
tCLQZ	Chip Enable Low to Output Low Z (20, 21)	3		3		3		3	
tBLQZ	Byte Enable Low to Output Low Z (20, 21)	3		3		3		3	
tOLQZ	Output Enable Low to Output Low Z (20, 21)	0		0		0		0	
tCHQZ	Chip Enable High to Output High Z (20, 21)		12		10		8		8
tBHQZ	Byte Enable High to Output High Z (20, 21)		12		10		8		8
tOHQZ	Output Enable High to Output High Z (20, 21)		12		10		8		8
tLHLL	ALE Pulse Width		12		10		8		8
tAVLL	Address Valid to ALE Low	6		6		4		4	
tLLAX	ALE Low to Address Change	4		4		4		4	
tOLOH	$\overline{OEA}$, $\overline{OEB}$ Overlap Time (20)	0		0		0		0	
tPU	$\overline{CE}$, $\overline{BEx}$ Low to Power Up (10, 19)	0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20
tCHVL	Chip Enable High to Output Retention (10)	0		0		0		0	

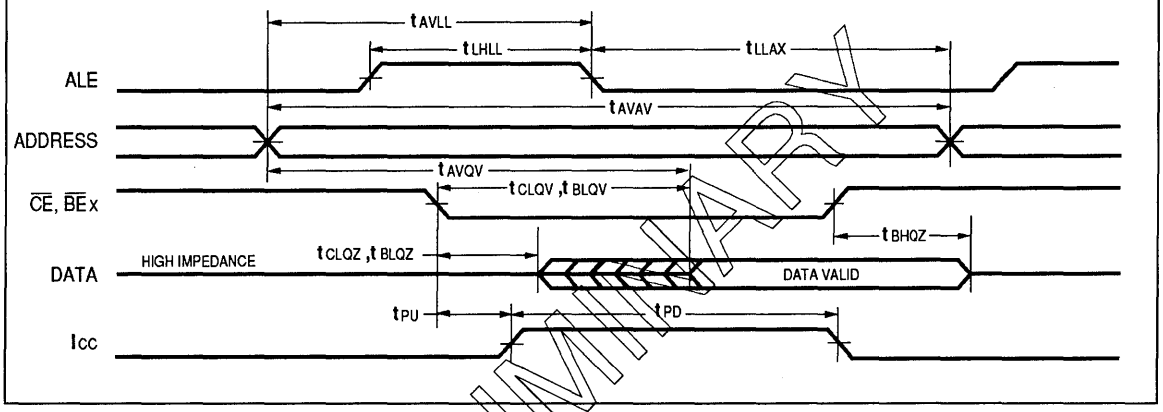
Read Cycle — Address Controlled (Notes 13, 14)



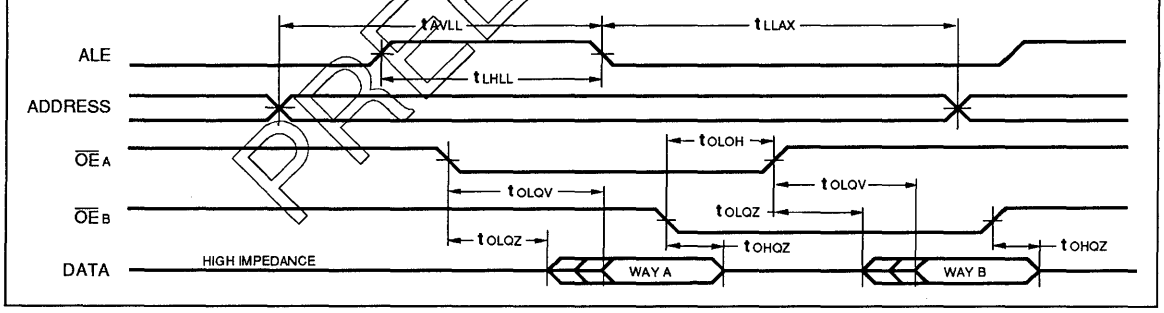
Read Cycle — ALE Controlled (Notes 13, 14)



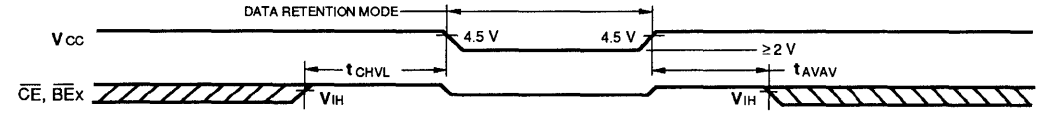
READ CYCLE — $\overline{CE}$, $\overline{BE}$x CONTROLLED (Notes 13, 15)



READ CYCLE — $\overline{OE}$ CONTROLLED (Notes 13, 15)



DATA RETENTION

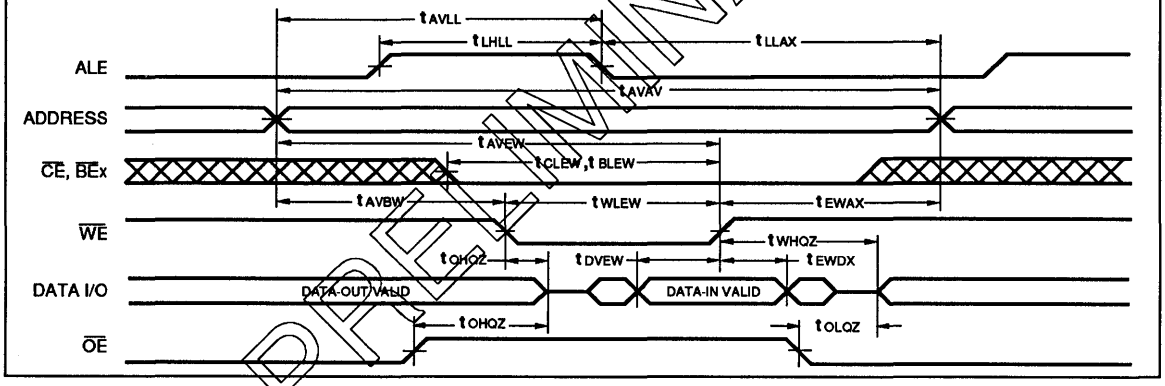


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

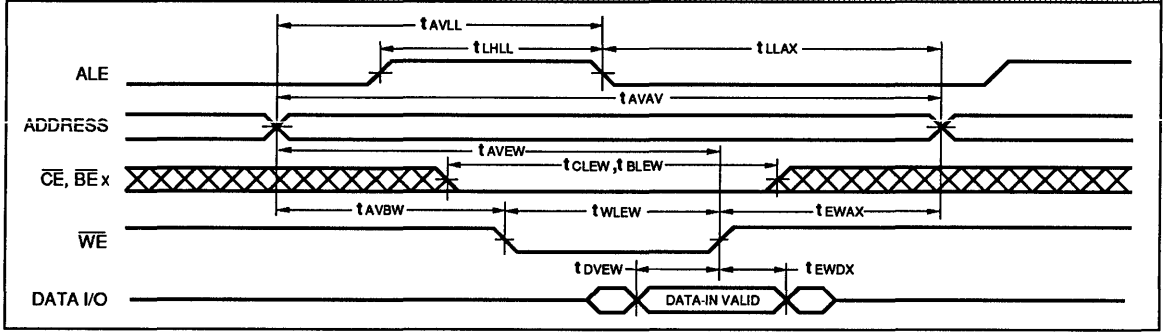
WRITE CYCLE *(Notes 5, 11, 12, 22, 23, 24)*

Symbol	Parameter	L7C183/184- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max
tAVAV	Write Cycle Time	45		35		25		20	
tCLEW	Chip Enable Low to End of Write Cycle	30		20		15		12	
tBLEW	Byte Enable Low to End of Write Cycle	30		20		15		12	
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0	
tAVEW	Address Valid to End of Write Cycle	30		20		15		12	
tEWAX	End of Write Cycle to Address Change	2		2		2		2	
tWLEW	Write Enable Low to End of Write Cycle	30		20		15		12	
tDVEW	Data Valid to End of Write Cycle	15		10		10		8	
tEWDX	End of Write Cycle to Data Change	0		0		0		0	
tWHQZ	Write Enable High to Output Low Z (20, 21)	0		0		0		0	
tWLQZ	Write Enable Low to Output High Z (20, 21)		12		10		8		8
tLHLL	ALE Pulse Width	12		10		8		8	
tAVLL	Address Valid to ALE Low	6		6		4		4	
tLLAX	ALE Low Address Change	4		4		4		4	

WRITE CYCLE — WE CONTROLLED *(Notes 16, 17, 18, 19)*



WRITE CYCLE — CE CONTROLLED *(Notes 16, 17, 18, 19)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. A series of normalized curves on pages 2-8 through 2-11 of this data book supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE},\overline{CS} \le V_{IL}$, $\overline{WE} \le V_{IL}$. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE},\overline{CS} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE},\overline{CS} = V_{CC}$. Input levels are within 0.2 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE},\overline{CS}$ must be $\ge V_{CC} - 0.2$ V. For all other inputs $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 100 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE},\overline{CS}$ low).

15. All address lines are valid prior-to the $\overline{CE},\overline{CS}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE},\overline{CS}$ low and $\overline{WE}$ low. Both signals must be LOW to initiate a write. Either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE},\overline{CS}$ going low, the output remains in a high impedance state.

18. If $\overline{CE},\overline{CS}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE},\overline{CS}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE},\overline{CS}$ active).

c. Transition on any address line ($\overline{CE},\overline{CS}$ active).

d. Transition on any data line ($\overline{CE},\overline{CS}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE},\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

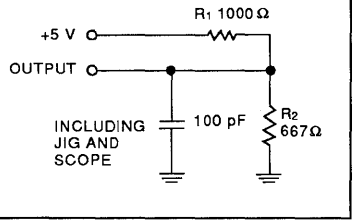


FIGURE 1b.

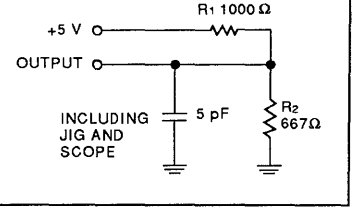
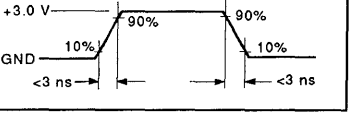
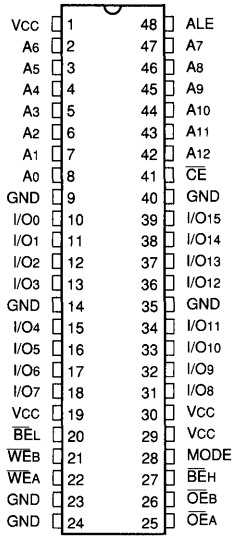


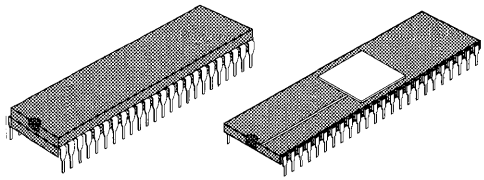
FIGURE 2.



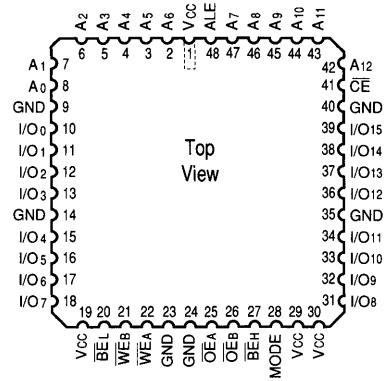
ORDERING INFORMATION

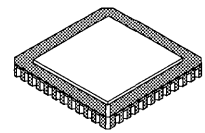
48-pin





48-pin
(550 x 550)

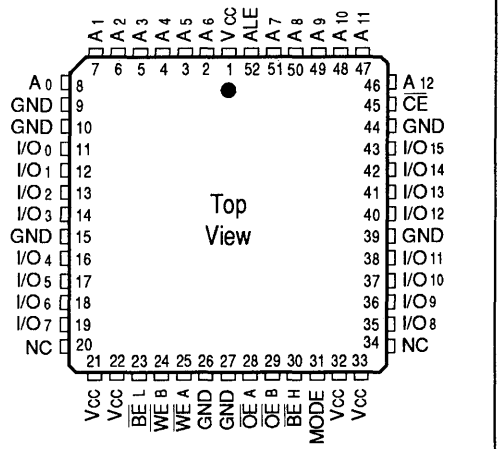


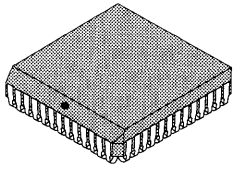


Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Ceramic Leadless Chip Carrier(K9)
	0°C to +70°C — Commercial Screening		
45 ns 35 ns 25 ns	L7C183PC or L7C184PC — 45 / 35 / 25	L7C183DC or L7C184DC — 45 / 35 / 25	L7C183KC or L7C184KC — 45 / 35 / 25
	–55°C to +125°C — Commercial Screening		
45 ns 35 ns		L7C183DM or L7C184DM — 45 / 35	L7C183KM or L7C184KM — 45 / 35
	–55°C to +125°C — Extended Screening		
45 ns 35 ns		L7C183DME or L7C184DME — 45 / 35	L7C183KME or L7C184KME — 45 / 35
	–55°C to +125°C — MIL-STD-883 Compliant		
45 ns 35 ns		L7C183DMB or L7C184DMB — 45 / 35	L7C183KMB or L7C184KMB — 45 / 35

ORDERING INFORMATION

52-pin





Speed	Plastic J-Lead Chip Carrier (J5)
	0°C to +70°C — COMMERCIAL SCREENING
45 ns 35 ns 25 ns 20 ns	L7C183JC or L7C184JC — 45, 35, 25, 20
	–55°C to +125°C — COMMERCIAL SCREENING
45 ns 35 ns 25 ns	
	–55°C to +125°C — EXTENDED SCREENING
45 ns 35 ns 25 ns	
	–55°C to +125°C — MIL-STD-883 COMPLIANT
45 ns 35 ns 25 ns	

64K x 1 Radiation-Hard Static RAM — L7CX187

FEATURES

- 64K × 1 Radiation-Hard Static RAM with Separate I/O, Chip Select Powerdown
- Address Access Time: ≤ 50 ns at 80°C
- Total Dose: $\geq 10^6$ Rads (SiO_2)
- Dose Rate Upset: $\geq 10^9$ Rads (Si)/s
- Dose Rate Survivability: $>10^{12}$ Rads (Si)/s
- Neutron Hardness: $>10^{14}$ N/cm^2
- SEU Immunity: $<10^{-7}$ errors/bit-day at 90°C, 4.5 V
- SEU Immunity: $<10^{-10}$ errors/bit-day at 25°C, 5.0V
- Latchup-Free Operation within Maximum Ratings
- Package Styles Available:
  - 24-pin Sidebraze, Hermetic DIP

DESCRIPTION

The **L7CX187** Radiation-Hard CMOS static RAM is a high-performance, low power device fabricated in a 1.25 µm bulk-CMOS radiation-hard process. The storage circuitry is organized as 65,536 words by 1 bit per word.

The L7CX187 performs at specification after exposure to 1×10^6 Rads (SiO_2) and retains data during exposure to transient radiation of up to 1×10^9 Rads (Si)/s. The single-event susceptibility is less than 10^{-10}errors/bit-day.

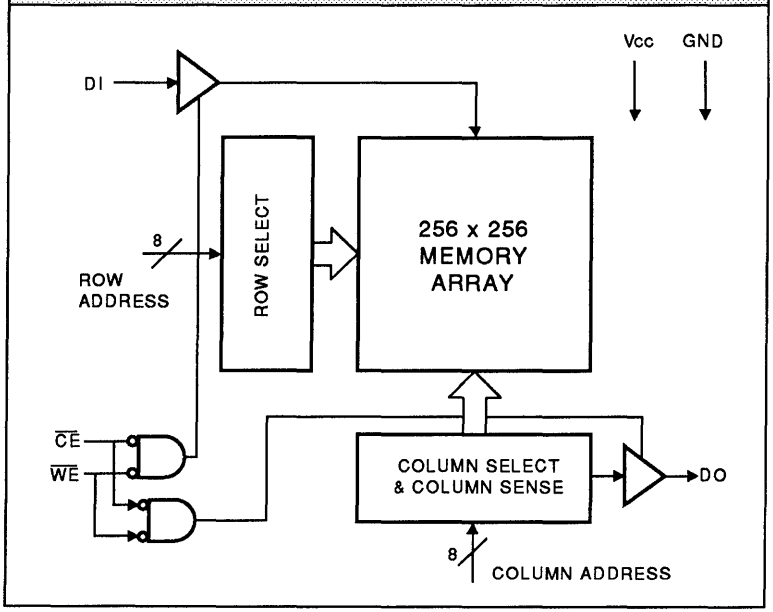
Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 225 mW (typical) at 50 ns. Dissipation drops to 3 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

The L7CX187 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A0 through A15. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

L7CX187 Block Diagram



OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.5	5.0	5.5	V
Ambient Temp.	T_A	0	25	80	°C

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground .... –0.3 V to +6.5 V
Voltage on any pin ..... –3.0 V to V_{CC} +0.3 V
Output current into low outputs ..... 25 mA

RADIATION-HARDNESS RATINGS

Parameter	Limits	Test Conditions
Total Dose	$\geq 10^6$ Rads (SiO_2)	T_A = 25°C, V_{CC} = 5.5V; Co60 gamma cell
Dose Rate Upset	$\geq 10^9$ Rads (Si)/s	Pulse Width < 1 µs; T_A = 25°C, V_{CC} = 4.5 V
Dose Rate Survivability	$>10^{12}$ Rads (Si)/s	Pulse Width < 50 ns; T_A = 25°C, V_{CC} = 5.0 V
Soft Error Rate (1)	$<10^{-7}$ errors/bit-day $<10^{-10}$ errors/bit-day	T_A = 90°C, V_{CC} = 4.5 V T_A = 25°C, V_{CC} = 5.0 V
Neutron	$>10^{14}$ N/cm^2	T_A = 25°C, Unbiased

(1) Refer to Figs. 3 and 4.

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

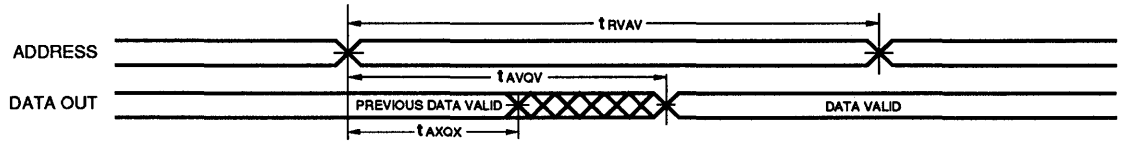
			0°C to +80°C		–55°C to +125°C		
Symbol	Parameter	Test Condition	Min	Max	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 16.0 mA		0.4		0.4	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.3	2.4	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–3.0	0.8	– 0.3	0.8	V
I_{IX}	Input Leakage Current			±10		±20	µA
I_{OZ}	Output Leakage Current			±10		±20	µA
I_{OS}	Output Short Current	(Note 3)		25		25	mA
I_{CC1}	V_{CC} Current, Active	Write Operation @ 20 MHz		60		70	mA
I_{CC2}	V_{CC} Current, TTL Inactive	$\overline{CE}$ > 2.4 V (Note 4)		5.0		8.0	mA
I_{CC3}	V_{CC} Current, CMOS Standby	$\overline{CE}$ > V_{CC} – 0.3 V (Note 5)		1.0		1.0	mA
C_{IN}	Input Capacitance	GND ≤ V_{IN} ≤ V_{CC} (Note 6)		6		6	pF
C_{OUT}	Output Capacitance	GND ≤ V_{OUT} ≤ V_{CC} (Note 6)		8		8	pF

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

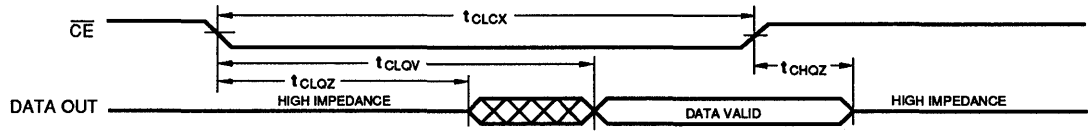
Read Cycle (Notes 7, 8, 17, 18, 19)

Symbol	Parameter	L7CX187-50			
		0°C to +80°C		−55°C to +125°C	
		Min	Max	Min	Max
tRVAV	Read Cycle Time (Address)	50		60	
tAVQV	Address Valid to Output Valid (Notes 9, 10)		50		60
tAXQX	Address Change to Data Hold (Notes 9, 10)	10		12	
tCLCX	Read Cycle Time (Chip Enable)	60		70	
tCLQV	Chip Enable Low to Output Valid (Notes 9, 11)		60		70
tCHQZ	Chip Enable High to Output High Z		10		12
tCLQZ	Chip Enable Low to Output Low Z		10		12

Read Cycle — Address Controlled (Notes 9, 10)



Read Cycle — $\overline{CE}$ Controlled (Notes 9, 11)



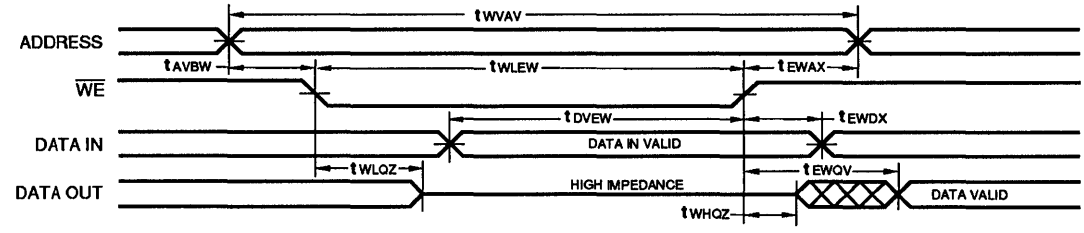
SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

Write Cycle (Notes 7, 8, 17, 18, 19)

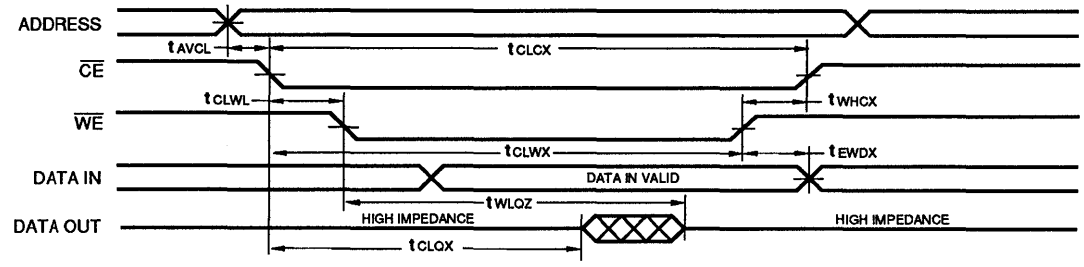
Symbol	Parameter	L7CX187-50			
		0°C to +80°C		–55°C to +125°C	
		Min	Max	Min	Max
tWVAV	Write Cycle Time (Address)	50		(1)	
tAVBW	Address Valid to Beginning of Write Cycle	0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		(1)	
tEWAX	End of Write Cycle to Address Change	5		6	
tDVEW	Data Valid to End of Write Cycle	40		(1)	
tEWDX	End of Write Cycle to Data Change	5		6	
tEWQV	End of Write Cycle to Data Valid	15		17	
tWLQZ	Write Enable Low to Output High Z (Notes 15, 16)		15		17
tWHQZ	Write Enable High to Output Low Z (Notes 15, 16)		15		17
tAVCL	Address Valid to Chip Enable Low	0		0	
tCLCX	Write Time Cycle (Chip Enable)	60		(1)	
tCLWL	Chip Enable Low to Write Enable Low	0		0	
tWHCH	Write Enable High to Chip Enable Low	5		6	
tCLWX	Chip Enable Low to Write Enable High	45		(1)	

(1) Refer to Figs. 3 and 4.

Write Cycle — WE Controlled (Notes 12, 13, 14)



Write Cycle — CE Controlled (Notes 12, 13, 14)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. Duration of the output short circuit should not exceed 30 seconds.

4. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \geq V_{IH}$.

5. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of VCC or ground.

6. These parameters are guaranteed but not 100% tested.

7. Test conditions assume input transition times of less than 5 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 50 pF (Fig. 1a), and input pulse levels of 0.8 to 2.40 V (Fig. 2).

8. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

9. $\overline{WE}$ is high for the read cycle.

10. The chip is continuously selected ($\overline{CE}$ low).

11. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

12. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

13. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

14. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

15. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

16. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

17. All address timings are referenced from the last valid address line to the first transitioning address line.

18. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

19. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

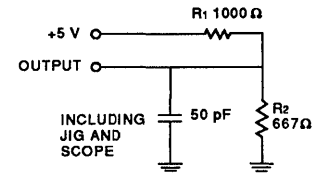


FIGURE 1b.

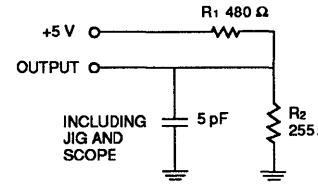
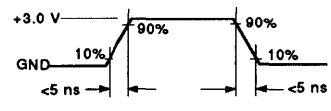


FIGURE 2.



TYPICAL PRE-RADIATION DC AND AC ELECTRICAL CHARACTERISTICS

Figure 3. Soft Error Rate vs Normalized Resistor

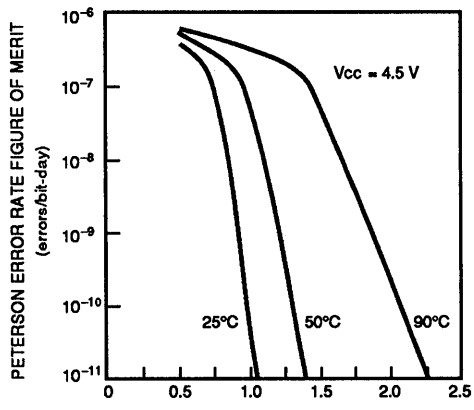
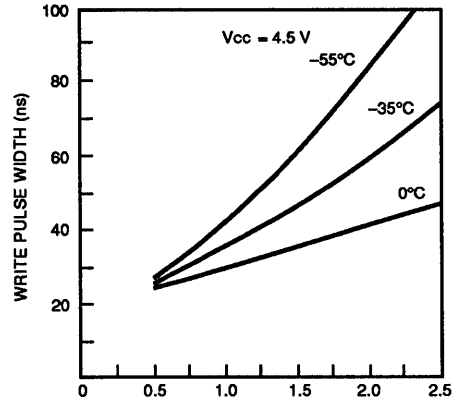


Figure 4. Norm. Write Pulse Width vs Norm. Resistor



TYPICAL POST-RADIATION DC AND AC ELECTRICAL CHARACTERISTICS

Figure 5. Access Time Delta vs Total Dose

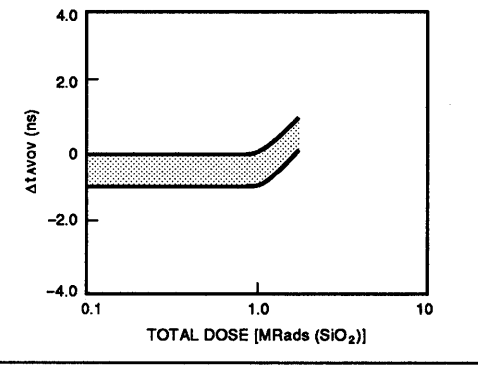


Figure 6. Norm. Stand-By Current vs Total Dose

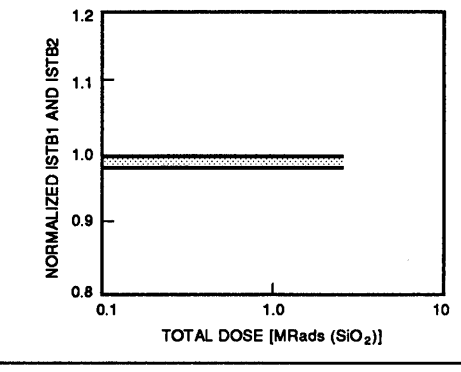


Figure 7. V_{IH} Delta vs Total Dose

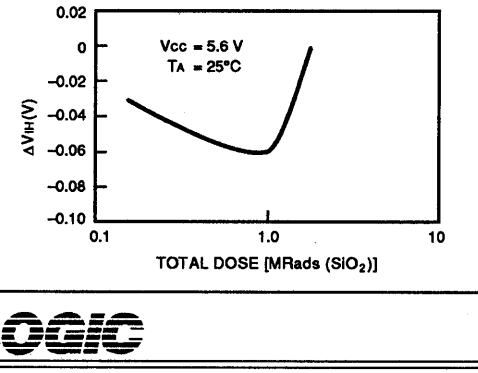
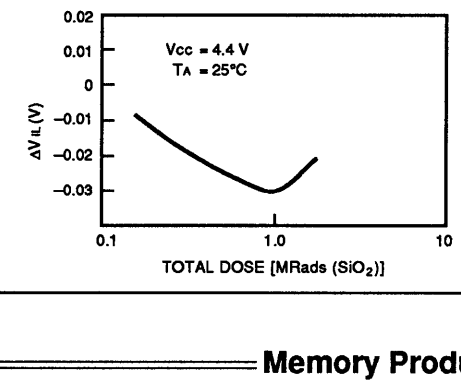
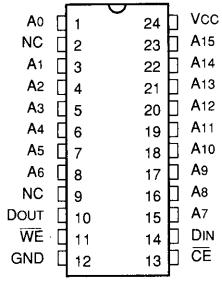


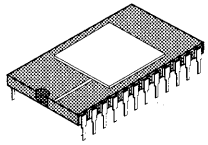
Figure 8. V_{IL} Delta vs Total Dose



ORDERING INFORMATION

24-pin
(0.6" wide)





Speed	Sidebraze Hermetic DIP (D1)
	0°C to +80°C — Commercial Screening
50 ns	L7CX187HC50
	–55°C to +125°C — Commercial Screening
50 ns	L7CX187HM50
	–55°C to +125°C — Extended Screening
50 ns	L7CX187HME50
	–55°C to +125°C — MIL-STD-883 Compliant
50 ns	L7CX187HMB50

256K x 1 Radiation-Hard Static RAM — L7CX197

FEATURES

- 256K × 1 Radiation-Hard Static RAM with Separate I/O, Chip Select Powerdown
- Address Access Time: ≤ 50 ns at 80°C
- Total Dose: $\geq 10^6$ Rads (SiO_2)
- Dose Rate Upset: $\geq 10^9$ Rads (Si)/s
- Dose Rate Survivability: $>10^{12}$ Rads (Si)/s
- Neutron Hardness: $>10^{14}$ N/cm^2
- SEU Immunity: $<10^{-7}$ errors/bit-day at 90°C, 4.5 V
- SEU Immunity: $<10^{-10}$ errors/bit-day at 25°C, 5.0V
- Latchup-Free Operation within Maximum Ratings
- Package Styles Available:
  - 24-pin Sidebraze, Hermetic DIP

DESCRIPTION

The **L7CX197** Radiation-Hard CMOS static RAM is a high-performance, low power device fabricated in a 1.25 µm bulk-CMOS radiation-hard process. The storage circuitry is organized as 262,144 words by 1 bit per word.

The L7CX197 performs at specification after exposure to 1×10^6 Rads (SiO_2) and retains data during exposure to transient radiation of up to 1×10^9 Rads (Si)/s. The single-event susceptibility is less than 10^{-10}errors/bit-day.

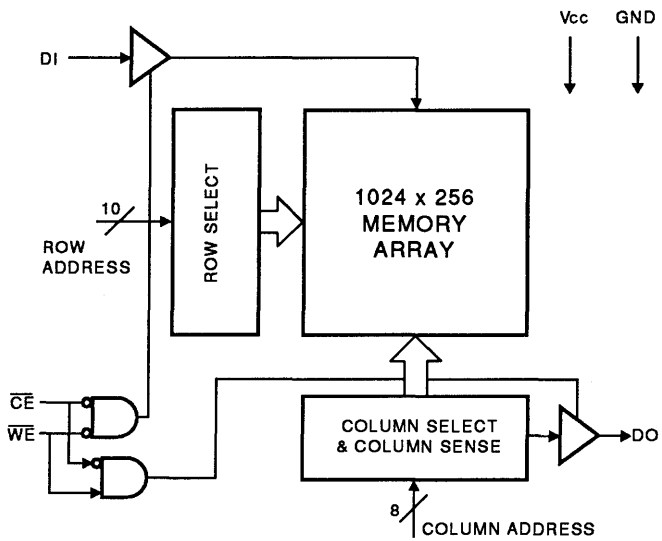
Operation is from a single +5 V power supply and all interface signals are TTL compatible. Power consumption is 260 mW (typical) at 50 ns. Dissipation drops to 3 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

The L7CX197 provides asynchronous (unclocked) operation with matching access and cycle times. An active-low Chip Enable and a three-state output simplify the connection of several chips for increased capacity.

Memory locations are specified on address pins A_0 through A_{15}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data Out pin within one access time. The output pin stays in a high-impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

Writing to an addressed location is accomplished when the active-low $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

L7CX197 Block Diagram



OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.5	5.0	5.5	V
Ambient Temp.	T_A	0	25	80	°C

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground .... –0.3 V to +6.5 V
Voltage on any pin ..... –3.0 V to V_{CC} +0.3 V
Output current into low outputs ..... 25 mA

RADIATION-HARDNESS RATINGS

Parameter	Limits	Test Conditions
Total Dose	$\geq 10^6$ Rads (SiO_2)	T_A = 25°C, V_{CC} = 5.5V; Co60 gamma cell
Dose Rate Upset	$\geq 10^9$ Rads (Si)/s	Pulse Width < 1 µs; T_A = 25°C, V_{CC} = 4.5 V
Dose Rate Survivability	$>10^{12}$ Rads (Si)/s	Pulse Width < 50 ns; T_A = 25°C, V_{CC} = 5.0 V
Soft Error Rate (1)	$<10^{-7}$ errors/bit-day $<10^{-10}$ errors/bit-day	T_A = 90°C, V_{CC} = 4.5 V T_A = 25°C, V_{CC} = 5.0 V
Neutron	$>10^{14}$ N/cm^2	T_A = 25°C, Unbiased

(1) Refer to Figs. 3 and 4.

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 5)*

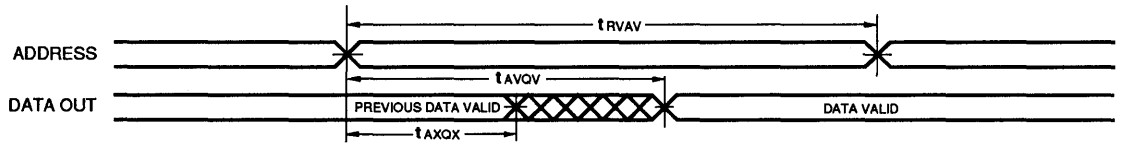
			0°C to +80°C		–55°C to +125°C		
Symbol	Parameter	Test Condition	Min	Max	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 16.0 mA		0.4		0.4	V
V_{IH}	Input High Voltage		2.4	V_{CC} + 0.3	2.4	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		–3.0	0.8	– 0.3	0.8	V
I_{IX}	Input Leakage Current			±10		±20	µA
I_{OZ}	Output Leakage Current			±10		±20	µA
I_{OS}	Output Short Current	(Note 3)		25		25	mA
I_{CC1}	V_{CC} Current, Active	Write Operation @ 20 MHz		60		70	mA
I_{CC2}	V_{CC} Current, TTL Inactive	$\overline{CE}$ > 2.4 V (Note 4)		5.0		8.0	mA
I_{CC3}	V_{CC} Current, CMOS Standby	$\overline{CE}$ > V_{CC} – 0.3 V (Note 5)		1.0		1.0	mA
C_{IN}	Input Capacitance	GND ≤ V_{IN} ≤ V_{CC} (Note 6)		6		6	pF
C_{OUT}	Output Capacitance	GND ≤ V_{OUT} ≤ V_{CC} (Note 6)		8		8	pF

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

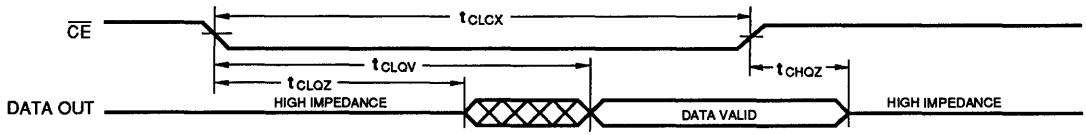
READ CYCLE (Notes 7, 8, 17, 18, 19)

Symbol	Parameter	L7CX197-50			
		0°C to +80°C		−55°C to +125°C	
		Min	Max	Min	Max
t_{RVAV}	Read Cycle Time (Address)	50		60	
t_{AVQV}	Address Valid to Output Valid (Notes 9, 10)		50		60
t_{AXQX}	Address Change to Data Hold (Notes 9, 10)	10		12	
t_{CLCX}	Read Cycle Time (Chip Enable)	60		70	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 9, 11)		60		70
t_{CHQZ}	Chip Enable High to Output High Z		10		12
t_{CLQZ}	Chip Enable Low to Output Low Z		10		12

READ CYCLE — ADDRESS CONTROLLED (Notes 9, 10)



READ CYCLE — $\overline{CE}$ CONTROLLED (Notes 9, 11)



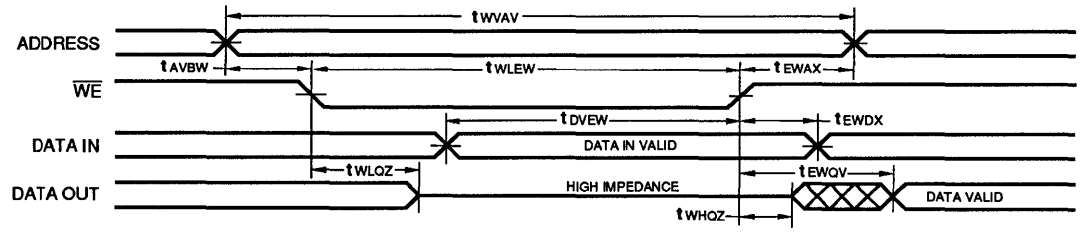
SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

WRITE CYCLE *(Notes 7, 8, 17, 18, 19)*

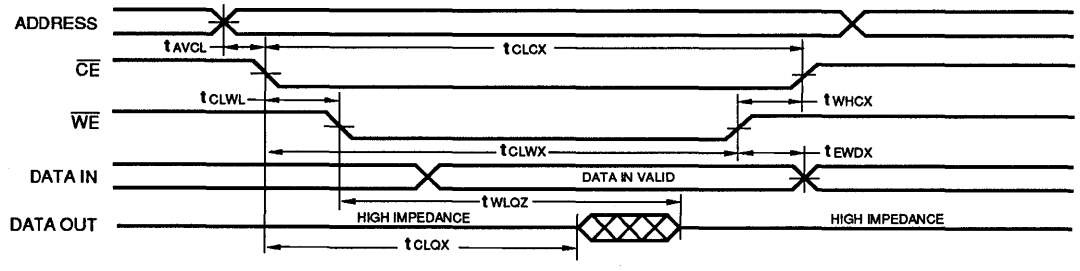
Symbol	Parameter	L7CX197-50			
		0°C to +80°C		–55°C to +125°C	
		Min	Max	Min	Max
tWVAV	Write Cycle Time (Address)	50		(1)	
tAVBW	Address Valid to Beginning of Write Cycle	0		0	
tWLEW	Write Enable Low to End of Write Cycle	45		(1)	
tEWAX	End of Write Cycle to Address Change	5		6	
tDVEW	Data Valid to End of Write Cycle	40		(1)	
tEWDX	End of Write Cycle to Data Change	5		6	
tEWQV	End of Write Cycle to Data Valid	15		17	
tWLQZ	Write Enable Low to Output High Z (Notes 15, 16)		15		17
tWHQZ	Write Enable High to Output Low Z (Notes 15, 16)		15		17
tAVCL	Address Valid to Chip Enable Low	0		0	
tCLCX	Write Time Cycle (Chip Enable)	60		(1)	
tCLWL	Chip Enable Low to Write Enable Low	0		0	
tWHCH	Write Enable High to Chip Enable Low	5		6	
tCLWX	Chip Enable Low to Write Enable High	45		(1)	

(1) Refer to Figs. 3 and 4.

WRITE CYCLE — $\overline{WE}$ CONTROLLED *(Notes 12, 13, 14)*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *(Notes 12, 13, 14)*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. Duration of the output short circuit should not exceed 30 seconds.

4. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \geq V_{IH}$.

5. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE} = V_{CC}$. Input levels are within 0.5 V of VCC or ground.

6. These parameters are guaranteed but not 100% tested.

7. Test conditions assume input transition times of less than 5 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 50 pF (Fig. 1a), and input pulse levels of 0.8 to 2.40 V (Fig. 2).

8. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

9. $\overline{WE}$ is high for the read cycle.

10. The chip is continuously selected ($\overline{CE}$ low).

11. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

12. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

13. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

14. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

15. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

16. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

17. All address timings are referenced from the last valid address line to the first transitioning address line.

18. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

19. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

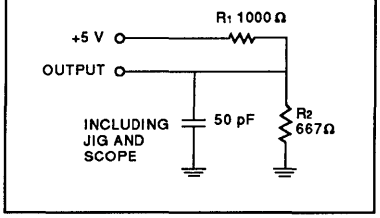


FIGURE 1b.

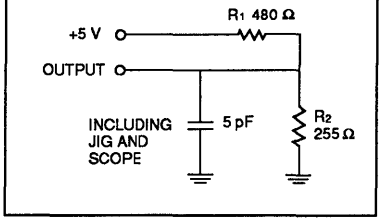
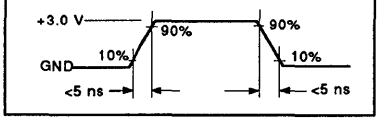


FIGURE 2.



TYPICAL PRE-RADIATION DC AND AC ELECTRICAL CHARACTERISTICS

FIGURE 3. SOFT ERROR RATE VS NORMALIZED RESISTOR

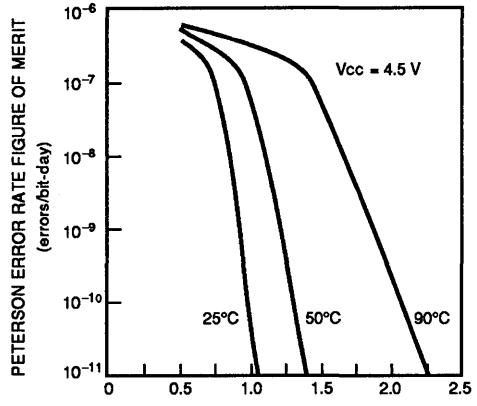
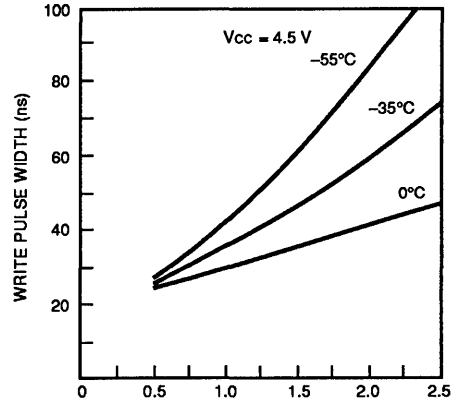


FIGURE 4. NORM. WRITE PULSE WIDTH VS NORM. RESISTOR



TYPICAL POST-RADIATION DC AND AC ELECTRICAL CHARACTERISTICS

FIGURE 5. ACCESS TIME DELTA VS TOTAL DOSE

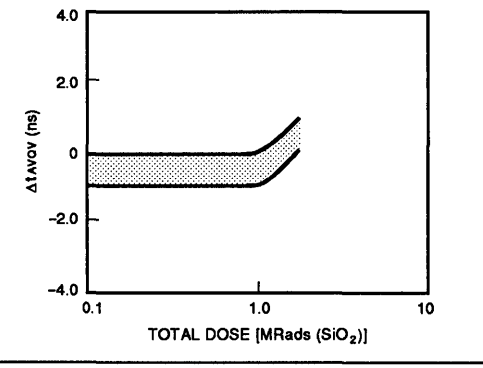


FIGURE 6. NORM. STAND-BY CURRENT VS TOTAL DOSE

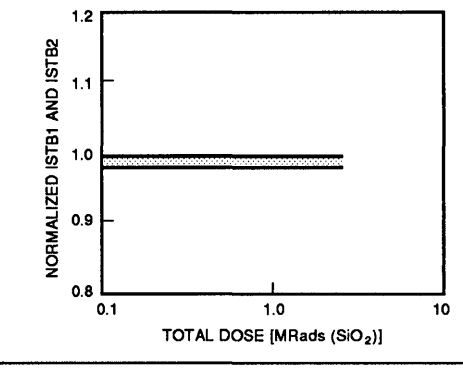


FIGURE 7. VIH DELTA VS TOTAL DOSE

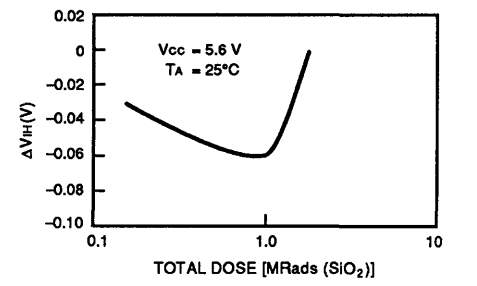
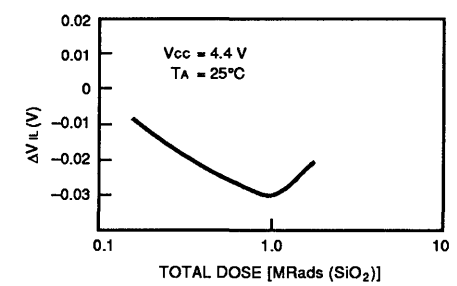
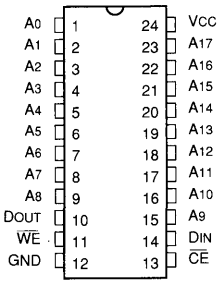


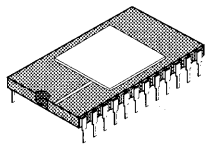
FIGURE 8. VIL DELTA VS TOTAL DOSE



ORDERING INFORMATION

24-pin
(0.6" wide)





Speed	Sidebraze Hermetic DIP (D1)
	0°C to +80°C — COMMERCIAL SCREENING
50 ns	L7CX197HC50
	–55°C to +125°C — COMMERCIAL SCREENING
50 ns	L7CX197HM50
	–55°C to +125°C — EXTENDED SCREENING
50 ns	L7CX197HME50
	–55°C to +125°C — MIL-STD-883 COMPLIANT
50 ns	L7CX197HMB50

Ordering Information

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FIFO Memory Products 3

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Logic Products

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LOGIC DEVICES INCORPORATED

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L8C202	1K × 9-bit	3-5
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L8C204	4K × 9-bit	3-5
L8C2011	512 × 9-bit with Flags + OE	3-17
L8C2021	1K × 9-bit with Flags + OE	3-17
L8C2031	2K × 9-bit with Flags + OE	3-17
L8C2041	4K × 9-bit with Flags + OE	3-17
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L8C402	64 × 5-bit without OE	3-29
L8C403	64 × 4-bit with OE	3-29
L8C404	64 × 5-bit with OE	3-29
L8C413	64 × 5-bit with Flags + OE	3-39
L8C408	64 × 8-bit with Flags + OE	3-49
L8C409	64 × 9-bit with Flags + OE	3-49

FIFO Memory Products Package Availability Guide

Part No.[1]	No. Pins	Package Availability Code[2]					
		Plastic DIP	CerDIP	SOIC (Gull-Wing)	SOJ (J-Lead)	Plastic LCC	Ceramic LCC
FIFO Memories							
L8C200	28/32	P9, P10	C6			J6	K7
L8C201	28/32	P9, P10	C6			J6	K7
L8C202	28/32	P9, P10	C6			J6	K7
L8C203	28/32	P9, P10	C6			J6	K7
L8C204	28/32	P9, P10	C6			J6	K7
L8C2011	32	P14				J6	K7
L8C2021	32	P14				J6	K7
L8C2031	32	P14				J6	K7
L8C2041	32	P14				J6	K7
L8C401	16/20	P12	C7	U3		J7	K8
L8C402	18/20	P12	C8	U3		J7	K8
L8C403	16/20	P12	C7	U3		J7	K8
L8C404	18/20	P12	C8	U3		J7	K8
L8C413	20	P13	C2	U3		J7	K8
L8C408	28/32	P9, P10	C6			J4	K7
L8C409	28/32	P9, P10	C6			J4	K7

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 10 – Packaging for package dimensions.

FIFO Memory Product Selection/Cross Reference

FIFO Memory — Product Selection

Part No.[1]	Description	Speed (ns) Com.	Speed (ns) Mil.	Power (mW) Opr.	Power (mW) Standby	Pins	Packages Available[2]
L8C200	256 x 9-bit	15	20	495	200	28/32	DIP, PLCC, LCC
L8C201	512 x 9-bit	15	20	495	200	28/32	DIP, PLCC, LCC
L8C202	1K x 9-bit	15	20	495	200	28/32	DIP, PLCC, LCC
L8C203	2K x 9-bit	15	20	495	200	28/32	DIP, PLCC, LCC
L8C204	4K x 9-bit	15	20	495	200	28/32	DIP, PLCC, LCC
L8C2011	512 x 9-bit with Flags + OE	15	20	495	200	32	DIP, PLCC, LCC
L8C2021	1K x 9-bit with Flags + OE	15	20	495	200	32	DIP, PLCC, LCC
L8C2031	2K x 9-bit with Flags + OE	15	20	495	200	32	DIP, PLCC, LCC
L8C2041	4K x 9-bit with Flags + OE	15	20	495	200	32	DIP, PLCC, LCC
L8C401	64 x 4-bit without OE	35 MHz	25 MHz	385	100	16/20	DIP, PLCC, LCC SOIC (Gull-Wing)
L8C402	64 x 5-bit without OE	35 MHz	25 MHz	385	100	18/20	DIP, PLCC, LCC SOIC (Gull-Wing)
L8C403	64 x 4-bit with OE	35 MHz	25 MHz	385	100	16/20	DIP, PLCC, LCC SOIC (Gull-Wing)
L8C404	64 x 5-bit with OE	35 MHz	25 MHz	385	100	18/20	DIP, PLCC, LCC SOIC (Gull-Wing)
L8C413	64 x 5-bit with Flags + OE	35 MHz	25 MHz	385	100	20	DIP, PLCC, LCC SOIC (Gull-Wing)
L8C408	64 x 8-bit with Flags + OE	35 MHz	25 MHz	695	125	28	DIP, PLCC, LCC
L8C409	64 x 9-bit with Flags + OE	35 MHz	25 MHz	695	125	28	DIP, PLCC, LCC

FIFO Memory — Product Cross Reference

	LOGIC DEVICES PART NUMBER							
Competitor	L8C200 (256 x 9)	L8C201 (512 x 9)	L8C202 (1K x 9)	L8C203 (2K x 9)	L8C204 (4K x 9)	L8C2011 (512 x 9)	L8C2021 (1Kx 9)	L8C2031 (2K x 9)
IDT	IDT7200S	IDT7201S	IDT7202S	IDT7203S	IDT7204S	IDT72011S	IDT72021S	IDT72031S
Cypress	NA	CY7C412	CY7C424	CY7C429	NA	NA	NA	NA
Samsung	NA	KM75C01A	KM75C02A	KM75C03A	NA	NA	NA	NA

	LOGIC DEVICES PART NUMBER							
Competitor	L8C2041 (4K x 9)	L8C401 (64 x 4)	L8C402 (64 x 5)	L8C403 (64 x 4)	L8C404 (64 x 5)	L8C413 (64 x 5)	L8C408 (64 x 8)	L8C409 (64 x 9)
IDT	IDT72041S	IDT72401	IDT72402	IDT72403	IDT72404	IDT72413	NA	NA
Cypress	NA	CY7C401A	CY7C402A	CY7C403A	CY7C404A	NA	CY7C408A	CY7C409A
Samsung	NA	NA	NA	NA	NA	NA	NA	NA

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 10 – Packaging for package dimensions.

256/512/1K/2K/4K x 9-bit First-In/First-Out (FIFO)

L8C200/201 L8C202/203/204

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- High Speed — to15 ns Access Time
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Empty and Full Warning Flags
- Auto Retransmit Capability
- Plug Compatible with IDT720x, Cypress CY7C4x, and Samsung KM75C0x
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin CerDIP
  - 32-pin Plastic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L8C200, L8C201, L8C202, L8C203,** and **L8C204** are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C200 – 256 × 9-bit
L8C201 – 512 × 9-bit
L8C202 – 1024 × 9-bit
L8C203 – 2048 × 9-bit
L8C204 – 4096 × 9-bit

Each memory utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty flags are provided to prevent data overflow and underflow. Three additional pins are also provided to allow for unlimited expansion in both word size and depth. Depth Expansion does not result in a flow-through penalty. The parts are hooked up with the data and control signals in parallel. The active device is determined by the Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$) signals which are daisy chained from device to device.

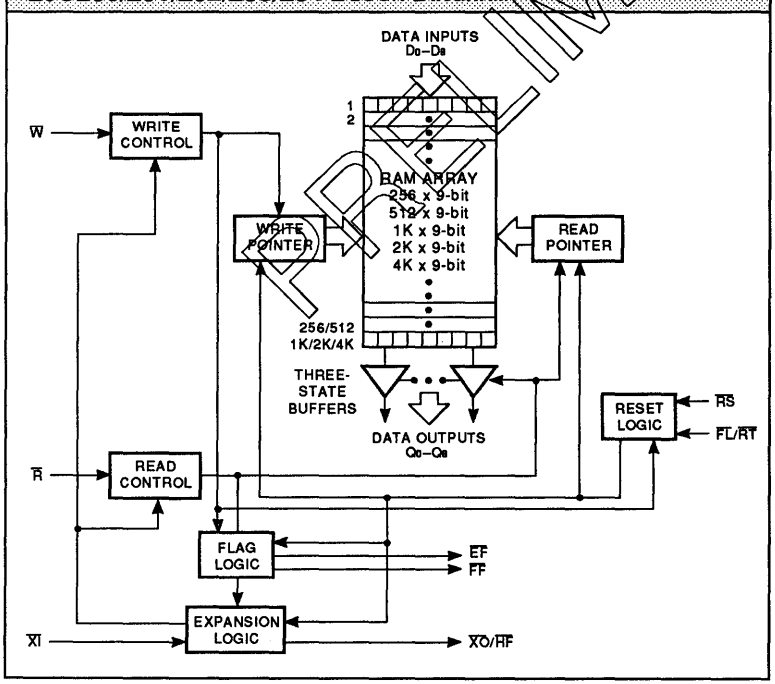
The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW. The nine data outputs go to the high impedance state when $\overline{R}$ is HIGH. A Retransmit ($\overline{RT}$) capability allows for reset of the read pointer when $\overline{RT}$ is pulsed LOW, allowing for retransmission of data from the beginning. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data. A Half Full ($\overline{HF}$) output flag is available in the single device and width expansion modes. In the depth expansion configuration, this pin provides the Expansion Out ($\overline{XO}$) information which is used to tell the next FIFO that it will be activated.

The FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

The FIFOs are designed for those applications requiring asychronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Latchup and static discharge protection is provided on-chip. The FIFOs can withstand an injection current of up to 200 mA on any pin without damage.

L8C200/201/202/203/204 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	–0.5 V to +7.0 V
DC input voltage	–3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	20 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	–55°C to +125°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA, V_{CC} = Min.			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–150	mA
I_{CC2}	V_{CC} Current, Standby	All Inputs = V_{IH} MIN (Note 7)			35	mA
I_{CC3}	V_{CC} Current, Powerdown	All Inputs = V_{CC} (Note 13)			20	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 8)			7	pF

			L8C200/201/202/203/204-					
Symbol	Parameter	Test Condition (MHz)➡	15	20	25	35	50	Unit
I_{CC1}	V_{CC} Current, Active	V_{CC} = Max., I_{OUT} = 0 mA (Notes 5, 6)	100	100	90	90	80	mA
Fs	Shift Frequency		40	33	25	20	15	MHz

SIGNAL DESCRIPTIONS

INPUTS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read enable ($\overline{R}$) and Write enable ($\overline{W}$) inputs must be in the high state during the window shown (i.e., t_{WHSH} before the rising edge of $\overline{RS}$) and should not change until t_{SHWL} after the rising edge of $\overline{RS}$. Hall-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold time must be adhered to with respect to the rising edge of the Write enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RHFH}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operation. After Read enable ($\overline{R}$) goes high, the Data Outputs (Q_0–Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operating has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WHEH} and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The FIFOs can be made to retransmit data when the Retransmit enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer.

Read enable ($\overline{R}$) and Write enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than the full memory has been written between resets. Retransmit will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

DATA INPUTS (D_0–D_8)

Data input signals for 9-bit wide data. Data has setup and hold time requirements with respect to the rising edge of $\overline{W}$.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 256 writes for the **L8C200**, 512 writes for the **L8C201**, 1024 wites for the **L8C202**, 2048 wites for the **L8C203**, and 4096 writes for the **L8C204**.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device Mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then deasserted by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q_0–Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read enable ($\overline{R}$) is in a high state or the device is empty.

OPERATING MODES

SINGLE DEVICE MODE

A single FIFO may be used when the application requirements are for the number of words in a single device. The FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded. In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is the active function of the combination pin $\overline{XO}/\overline{HF}$.

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be detected from any one device. Any word width can be attained by adding additional FIFOs. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. **Do not connect any output signals together.**

DEPTH EXPANSION (DAISY CHAIN) MODE

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. Any depth can be attained by adding additional FIFOs. The FIFOs operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device with the last device connecting back to the first.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing FIFOs. Care must be taken to assure that the appropriate flag is monitored by each system, i.e., $\overline{FF}$ is monitored on the device when $\overline{W}$ is used; $\overline{EF}$ is monitored on the device when $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode, the FIFO permits the reading of a single word after writing one word data into an empty FIFO. The data is enabled on the bus in (t_{WHEH} + t_{RLQV}) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{AHQZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will be de-assert the Empty Flag). However, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

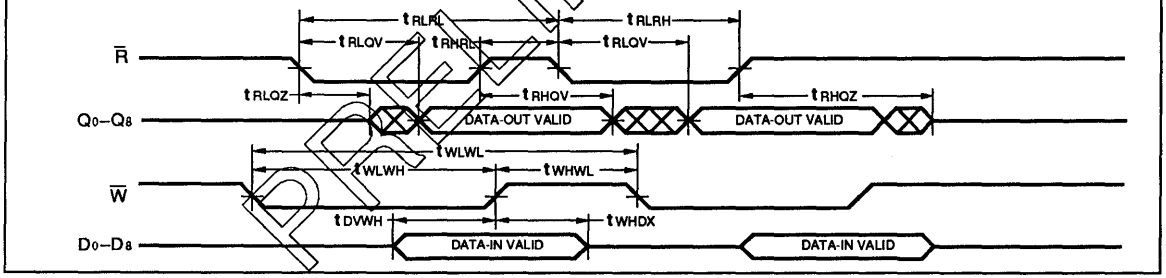
In the write flow-through mode, the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer. The user must be aware that there is no minimum value for t_{RLEL} and t_{WLFL}. These pulses may be slight during some operating conditions and lot variations.

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

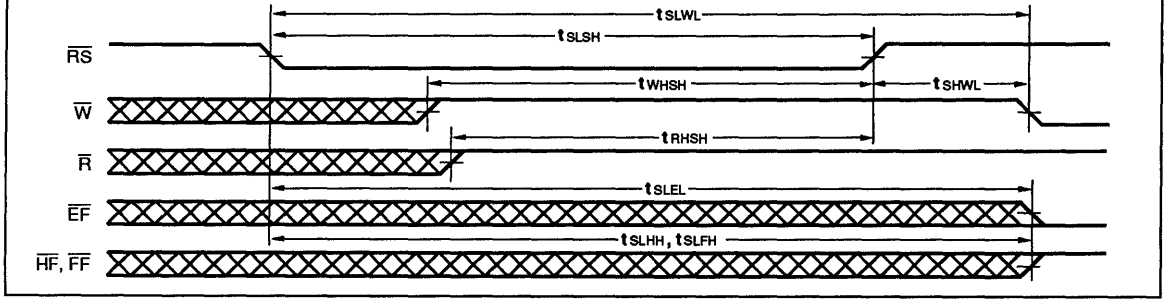
TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLRL	Read Cycle Time	65		45		35		30		25	
tRLQV	Read Low to Output Valid (Access Time)		50		35		25		20		15
tRHRL	Read High to Read Low (Notes 9, 10)	15		10		10		10		8	
tRLRH	Read Low to End of Read Cycle (Notes 9, 10)	50		35		25		20		15	
tRLQZ	Read Low to Output Low Z (Note 2)	10		5		5		5		3	
tRHQV	Read High to Output Valid	5		5		5		5		5	
tRHQZ	Read High to Output High Z (Note 15)		30		20		10		10		10
tWLWL	Write Cycle Time (Note 10)	65		45		35		30		25	
tWLWH	Write Low to Write High (Notes 9, 10)	50		35		25		20		15	
tWHWL	Write High to End of Write Cycle (Notes 9, 10)	15		10		10		10		8	
tDVWH	Data Valid to Write High (Notes 9, 10)	30		18		15		15		10	
tWHDX	Write High to Data Change (Notes 9, 10)	5		0		0		0		0	
tSLSH	Reset Cycle Time (Notes 10, 11)	50		35		25		20		15	
tSLWL	Reset Low to Write Low (Notes 10, 11)	65		45		35		30		25	
tWHSH	Write High to Reset High (Notes 10, 11)	50		35		25		20		15	
tRHSH	Read High to Reset High (Notes 10, 11)	50		35		25		20		15	
tSHWL	Reset High to Write Low (Notes 10, 11)	15		10		10		10		8	
tSLEL	Reset Low to Empty Flag Low		65		45		35		30		25
tSLHH	Reset Low to Half-Full Flag High		65		45		35		30		25
tSLFH	Reset Low to Full Flag High		65		45		35		30		25

ASYNCHRONOUS READ AND WRITE OPERATION



RESET TIMING

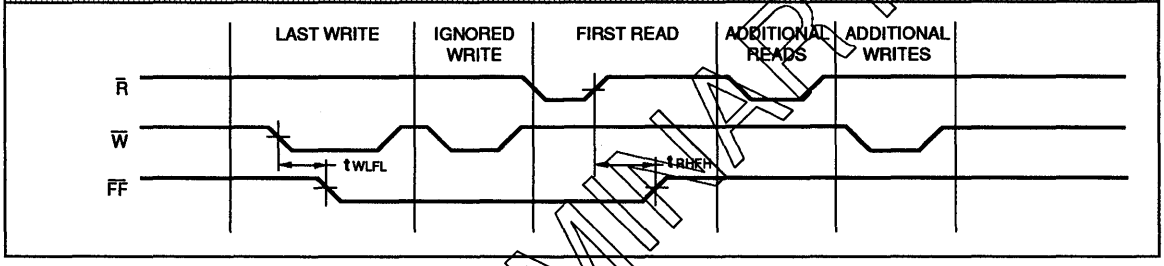


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

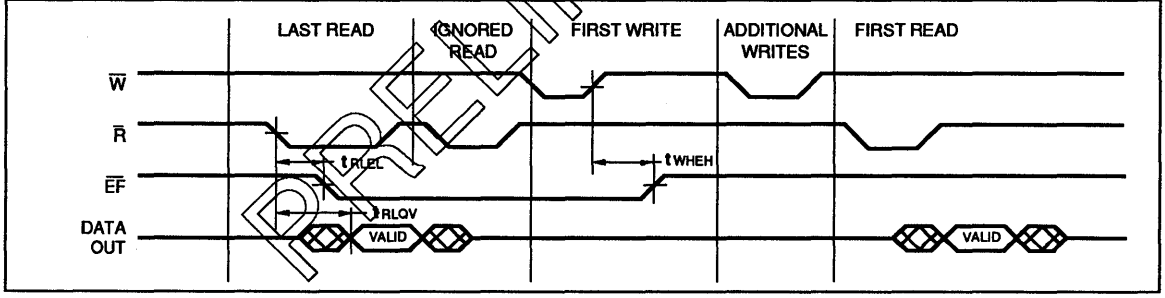
TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLQV	Read Low to Output Valid		50		35		25		20		15
tRLEL	Read Low to Empty Flag Low		45		30		25		20		15
tRHFH	Read High to Full Flag High		45		30		25		25		25
tWHEH	Write High to Empty Flag High		45		30		25		25		25
tWLFL	Write Low to Full Flag Low		45		30		25		20		15
tTLAL	Retransmit Cycle Time	65		45		35		30		25	
tTLTH	Retransmit Low to End of Retransmit Cycle (Notes 9, 10, 11)	50		35		25		20		15	
tAHTH	Read/Write High to Retransmit High (Notes 9, 10, 11)	50		35		25		20		15	
tTHAL	Retransmit High to Read/Write Low (Note 10)	15		10		10		10		8	

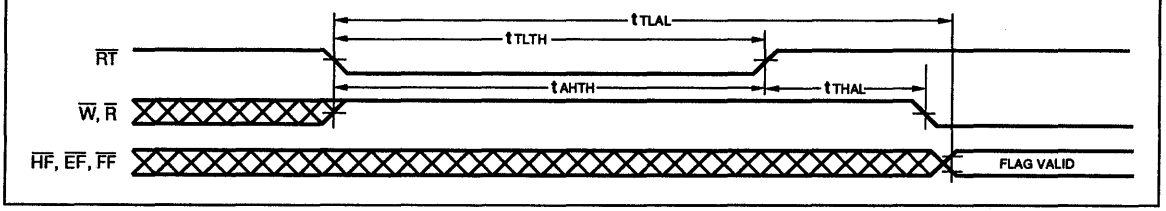
FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE



RETRANSMIT

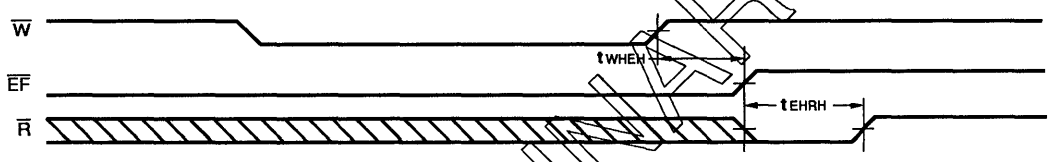


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

TIMING REFERENCES

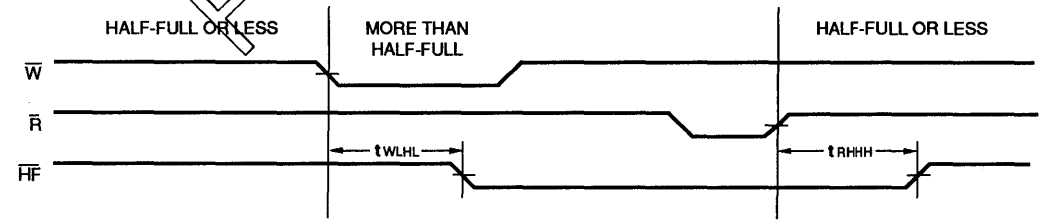
Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRHFH	Read High to Full Flag High		45		30		25		25		25
tEHRH	Read Pulse Width After Empty Flag High	50		35		25		20		15	
tRHHH	Read High to Half-Full Flag High		65		45		35		30		25
tWHEH	Write High to Empty Flag High		45		30		25		25		25
tWLHL	Write Low to Half-Full Flag Low		65		45		35		30		25
tFHWH	Write Pulse Width After Full Flag High (Note 10)	50		35		25		20		15	

EMPTY FLAG TIMING



FULL FLAG TIMING

HALF-FULL FLAG TIMING

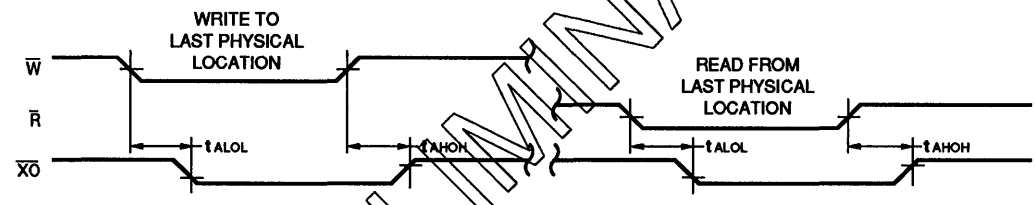


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

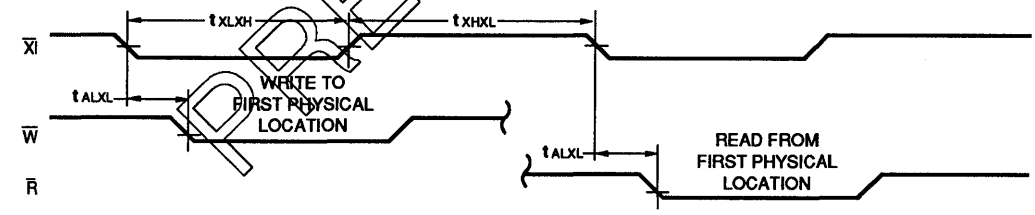
TIMING REFERENCES

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tALOL	Read/Write to Expansion Out Low (Note 12)		50		35		25		20		15
tAHOH	Read/Write to Expansion Out High (Note 12)		50		35		25		20		15
tXLXH	Expansion In Pulse Width (Notes 10, 12)	50		35		25		20		15	
tXHXL	Expansion In High to Expansion In Low (Notes 10, 12)		10		10		10		10		10
tALXL	Read/Write Low to Expansion In Low (Notes 10, 12)	15		10		10		10		10	

EXPANSION OUT



EXPANSION IN

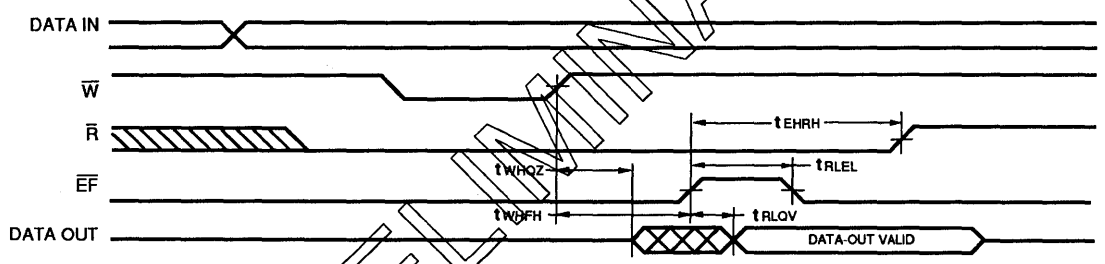


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

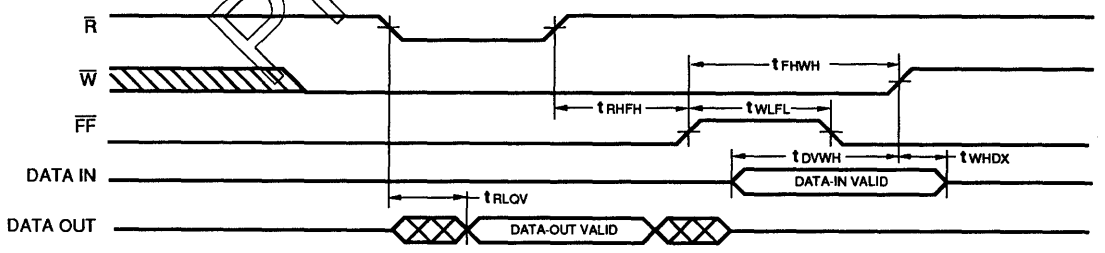
Timing References

Symbol	Parameter	L8C200/201/202/203/204- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLEL	Read Low to Empty Flag Low		45		30		25		20		15
tEHRH	Read Pulse Width After Empty Flag High	50		35		25		20		15	
tWHEH	Write High to Empty Flag High	45		30		25		25		25	
tRLQV	Read Low to Output Valid		50		35		25		20		15
tWHQZ	Write High to Output Low Z (Notes 14, 15)	15		10		5		5		3	
tRHFH	Read High to Full Flag High		45		30		25		25		25
tWLFL	Write Low to Full Flag Low		45		30		25		20		15
tFHWH	Write Pulse Width After Full Flag High	50		35		25		20		15	
tDVWH	Data Valid to Write High	30		18		15		15		10	
tWHDX	Write High to Data Change	5		0		0		0		0	

Read Data Flow-Through Mode



Write Data Flow-Through Mode



FIFO Memory (Depth Expansion) Block Diagram

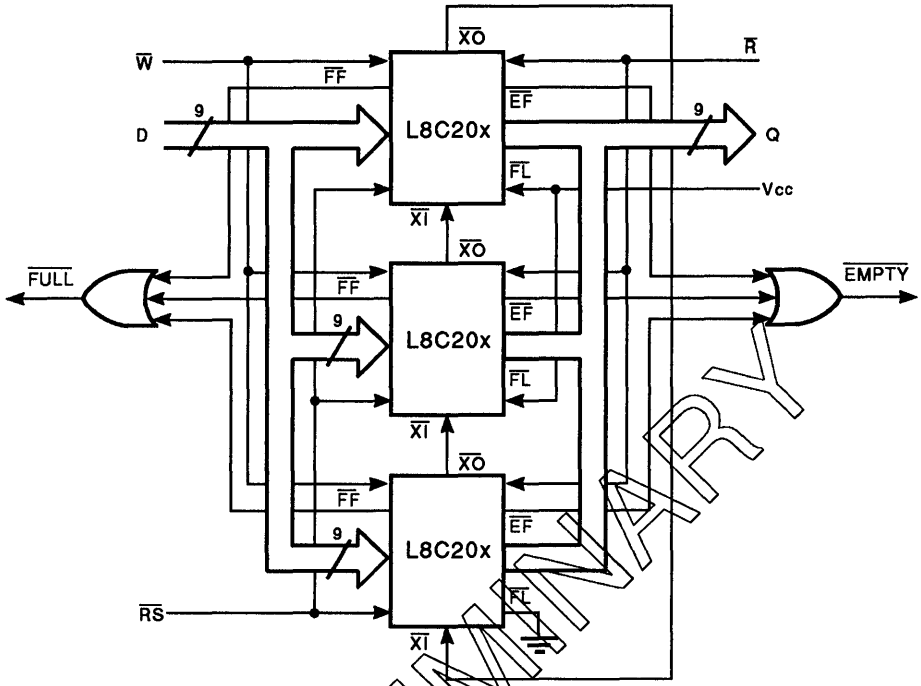


Table 1. Reset and Retransmit (Single Device Configuration/Width Expansion Mode)

MODE	INPUTS			INTERNAL STATUS		OUTUPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment	Increment	X	X	X

Table 2. Reset and First Load Truth Table (Depth Expansion/Compound Expansion Mode)

MODE	INPUTS			INTERNAL STATUS		OUTUPUTS	
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Others	0	1	(1)	Location Zero Disabled	Location Zero Disabled	0	1
Read/Write	1	(2)	(1)	X	X	X	X

(1) See Depth Expansion Block Diagram above.
(2) Unchanged.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. Tested with outputs open in the worst static input control signal combination (i.e., $\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{FL}$, and $\overline{RS}$).

8. These parameters are guaranteed but not 100% tested.

9. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RLRH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. When cascading devices, the reset pulse width must be increased to equal t_{SLSH} + t_{SLHH}.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

13. Tested with output open and $\overline{RS}$ = $\overline{FL}$ = $\overline{XI}$ = $\overline{R}$ = $\overline{W}$ = VCC.

14. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

15. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

16. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

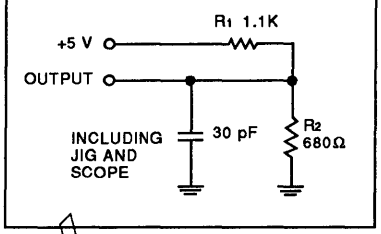


FIGURE 1b.

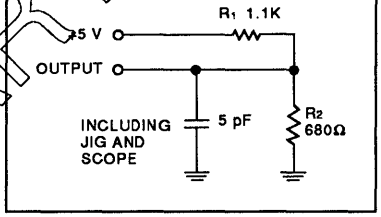
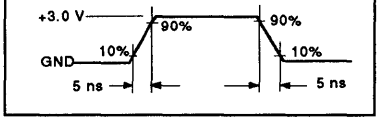


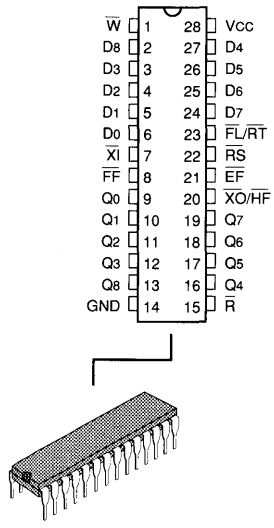
FIGURE 2.



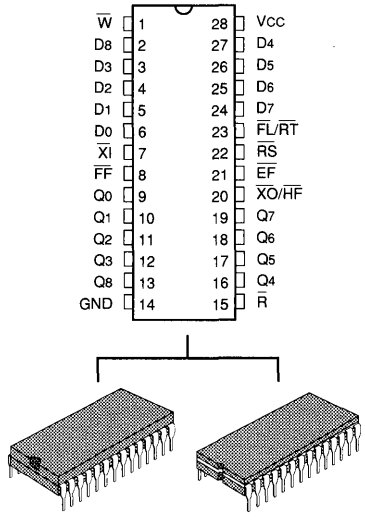
3

ORDERING INFORMATION

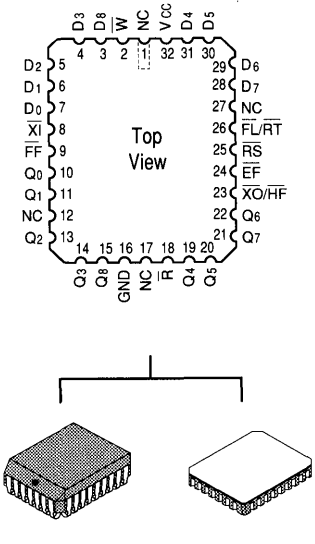
28-pin (0.3" wide)



28-pin (0.6" wide)



32-pin



Speed	Plastic DIP (P10)		Plastic DIP (P9)	CerDIP (C6)	Plastic Leaded Chip Carrier (J6)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening					
50 ns 35 ns 25 ns 20 ns 15 ns	L8C200PC – 50 L8C201PC – 35 L8C202PC – 25 L8C203PC – 20 or L8C204PC – 15		L8C200NC – 50 L8C201NC – 35 L8C202NC – 25 L8C203NC – 20 or L8C204NC – 15	L8C200CC – 50 L8C201CC – 35 L8C202CC – 25 L8C203CC – 20 or L8C204CC – 15	L8C200JC – 50 L8C201JC – 35 L8C202JC – 25 L8C203JC – 20 or L8C204JC – 15	L8C200KC – 50 L8C201KC – 35 L8C202KC – 25 L8C203KC – 20 or L8C204KC – 15
	–55°C to +125°C — Commercial Screening					
50 ns 35 ns 25 ns 20 ns 15 ns				L8C200CM – 50 L8C201CM – 35 L8C202CM – 25 L8C203CM – 20 or L8C204CM		L8C200KM – 50 L8C201KM – 35 L8C202KM – 25 L8C203KM – 20 or L8C204KM
	–55°C to +125°C — Extended Screening					
50 ns 35 ns 25 ns 20 ns 15 ns				L8C200CME – 50 L8C201CME – 35 L8C202CME – 25 L8C203CME – 20 or L8C204CME		L8C200KME – 50 L8C201KME – 35 L8C202KME – 25 L8C203KME – 20 or L8C204KME
	–55°C to +125°C — MIL-STD-883 Compliant					
50 ns 35 ns 25 ns 20 ns 15 ns				L8C200CMB – 50 L8C201CMB – 35 L8C202CMB – 25 L8C203CMB – 20 or L8C204CMB		L8C200KMB – 50 L8C201KMB – 35 L8C202KMB – 25 L8C203KMB – 20 or L8C204KMB

512/1K/2K/4K x 9-bit First-In/First-Out (FIFO) with Flags + OE

L8C2011/2021 L8C2031/2041

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- High Speed — to15 ns Access Time
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Empty and Full Warning Flags
- Independent Output Enable Control Pin $\overline{OE}$
- Almost Full or Empty Flag
- Auto Retransmit Capability
- Plug Compatible with IDT720xx
- Package Styles Available:
  - 32-pin Plastic DIP
  - 32-pin Plastic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L8C2011, L8C2021, L8C2031,** and **L8C2041** are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C2011 – 512 x 9-bit
L8C2021 – 1024 x 9-bit
L8C2031 – 2048 x 9-bit
L8C2041 – 4096 x 9-bit

Each memory utilizes a special algorithm that loads and empties data on a first-in/first-out basis. Full and Empty flags are provided to prevent data overflow and underflow. Three additional pins are also provided to allow for unlimited expansion in both word size and depth. Depth Expansion does not result in a flow-through penalty. The parts are hooked up with the data and control signals in parallel. The active device is determined by the Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$) signals which are daisy chained from device to device.

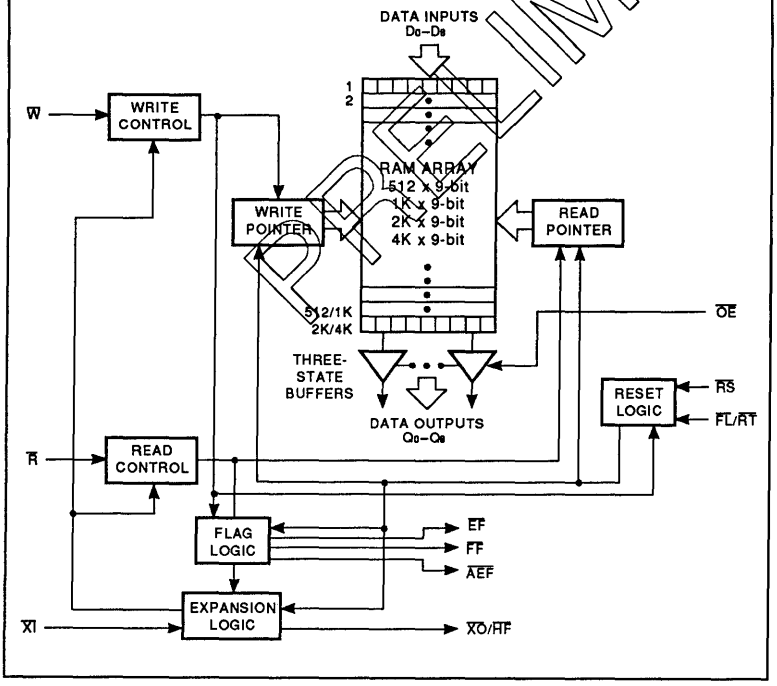
The read and write operations are internally sequential through the use of ring pointers. No address information is required to load and unload data. The write operation occurs when the Write ($\overline{W}$) signal is LOW. Read occurs when Read ($\overline{R}$) goes LOW and Output Enable ($\overline{OE}$) is LOW. The nine data outputs go to the high impedance state when $\overline{R}$ is HIGH or the $\overline{OE}$ is HIGH. A Retransmit ($\overline{RT}$) capability allows for reset of the read pointer when $\overline{RT}$ is pulsed LOW, allowing for retransmission of data from the beginning. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must both be HIGH during a retransmit cycle, and then $\overline{R}$ is used to access the data. A Half Full ($\overline{HF}$) output flag is available in the single device and width expansion modes. In the depth expansion configuration, this pin provides the Expansion Out ($\overline{XO}$) information which is used to tell the next FIFO that it will be activated.

The FIFOs are designed to have the fastest data access possible. Even in lower cycle time applications, faster access time can eliminate timing bottlenecks as well as leave enough margin to allow the use of the devices without external bus drivers.

The FIFOs are designed for those applications requiring asychronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Latchup and static discharge protection is provided on-chip. The FIFOs can withstand an injection current of up to 200 mA on any pin without damage.

L8C2011/2021/2031/2041 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	–0.5 V to +7.0 V
DC input voltage	–3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	20 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	–55°C to +125°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA, V_{CC} = Min.			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}	–10		+10	µA
I_{OZ}	Output Leakage Current	$\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max (Note 4)			–150	mA
I_{CC2}	V_{CC} Current, Standby	All Inputs = V_{IH} MIN (Notes 7, 17)			35	mA
I_{CC3}	V_{CC} Current, Powerdown	All Inputs = V_{CC} (Note 13)			20	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 8)			7	pF

			L8C2011/2021/2031/2041-					
Symbol	Parameter	Test Condition	50	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	V_{CC} = Max., I_{OUT} = 0 mA (Notes 5, 6, 17)	80	90	90	100	100	mA
Fs	Shift Frequency		15	20	25	33	40	MHz

SIGNAL DESCRIPTIONS

INPUTS

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read enable ($\overline{R}$) and Write enable ($\overline{W}$) inputs must be in the high state during the window shown (i.e., t_{WHSH} before the rising edge of $\overline{RS}$) and should not change until t_{SHWL} after the rising edge of $\overline{RS}$. Hall-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data setup and hold time must be adhered to with respect to the rising edge of the Write enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RHFH}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

OUTPUT ENABLE ($\overline{OE}$)

The data outputs Q_0–Q_8 are enabled when $\overline{OE}$ is low. Once enabled, the outputs behave according to the condition of $\overline{R}$ and $\overline{EF}$. When the $\overline{OE}$ is high, the outputs Q_0–Q_8 go to the high impedance state regardless of the value of $\overline{R}$ and $\overline{EF}$. The $\overline{OE}$ pin only inhibits the output buffers. It does not inhibit incrementing of the read pointer, therefore, it is possible to move the read pointer and have the Q_0–Q_8 bus remain tristated.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operation. After Read enable ($\overline{R}$) goes high, the Data Outputs (Q_0–Q_8) will return to a high impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operating has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WHEH} and a valid read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The FIFOs can be made to retransmit data when the Retransmit enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read enable ($\overline{R}$) and Write enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than the full memory has been written between resets. Retransmit will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

DATA INPUTS (D_0–D_8)

Data input signals for 9-bit wide data. Data has setup and hold time requirements with respect to the rising edge of $\overline{W}$.

OUTPUTS

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 512 writes for the **L8C2011**, 1024 wites for the **L8C2021**, 2048 wites for the **L8C2031**, and 4096 writes for the **L8C2041**.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device Mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then deasserted by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

ALMOST-EMPTY/ALMOST-FULL FLAG ($\overline{AEF}$)

The $\overline{AEF}$ signal indicates that the FIFO is between Empty and 1/8 Full or between 7/8 Full and Full. The distinstation between Almost-Empty and Almost-Full can be made by using $\overline{AEF}$ in conjunction with $\overline{HF}$. The $\overline{AEF}$ signal is primarily designed for use in standalone applications.

DATA OUTPUTS (Q_0–Q_8)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read enable ($\overline{R}$) is high, $\overline{OE}$ is high, or the device is empty.

STATUS FLAGS

NUMBER OF WORDS IN FIFO							
512	1K	2K	4K	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	0	H	L	H	L
1-63	1-127	1-255	1-511	H	L	H	H
64-128	128-512	256-1024	512-2048	H	H	H	H
129-448	513-896	1025-1792	2049-3584	H	H	L	H
449-511	897-1023	1793-2047	3585-4095	H	L	L	H
512	1024	2048	4096	L	L	L	H

OPERATING MODES

SINGLE DEVICE MODE

A single FIFO may be used when the application requirements are for the number of words in a single device. The FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded. In this mode the Half-Full Flag ($\overline{HF}$), which is an active low output, is the active function of the combination pin $\overline{XO}/\overline{HF}$.

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{AEF}$, $\overline{EF}$, $\overline{FF}$, and $\overline{HF}$) can be detected from any one device. Any word width can be attained by adding additional FIFOs. Flag detection is accomplished by monitoring the $\overline{AEF}$, $\overline{FF}$, $\overline{EF}$, and $\overline{HF}$ signals on either (any) device used in the width expansion configuration. **Do not connect any output signals together.**

DEPTH EXPANSION (DAISY CHAIN) MODE

The FIFOs can easily be adapted to applications where the requirements are for greater than the number of words in a single device. Any depth can be attained by adding additional FIFOs. The FIFOs operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device with the last device connecting back to the first.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing FIFOs. Care must be taken to assure that the appropriate flag is monitored by each system, i.e., $\overline{FF}$ is monitored on the device when $\overline{W}$ is used; $\overline{EF}$ is monitored on the device when $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode, the FIFO permits the reading of a single word after writing one word data into an empty FIFO. The data is enabled on the bus in ($t_{WHEH} + t_{RLQV}$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHQZ} ns. The $\overline{EF}$ line would have a pulse showing temporary de-assertion and then would be asserted. In the interval of time that $\overline{R}$ is low, more words can be written to the FIFO (the subsequent writes after the first write edge will be de-assert the Empty Flag). However, the same word (written on the first write edge) presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

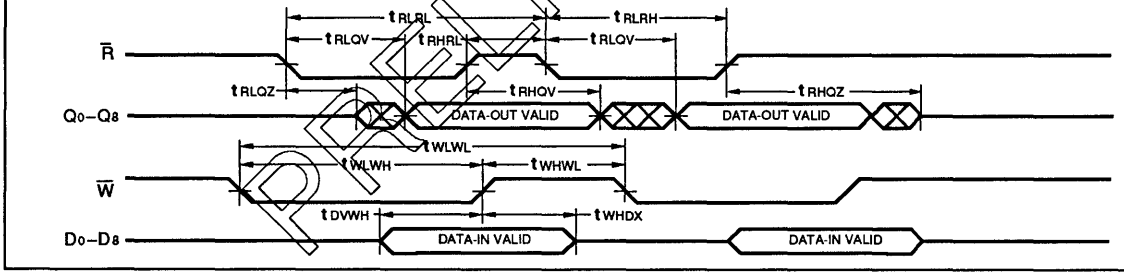
In the write flow-through mode, the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be de-asserted but the $\overline{W}$ line, being low, causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer. The user must be aware that there is no minimum value for t_{RLEL} and t_{WLFL}. These pulses may be slight during some operating conditions and lot variations.

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

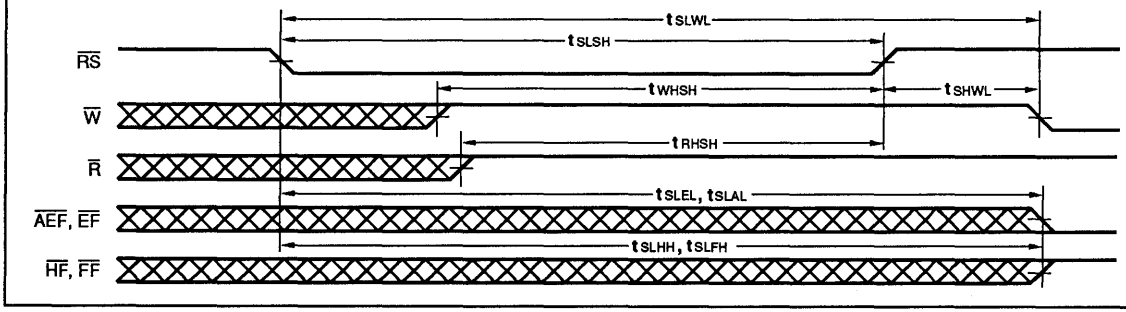
TIMING REFERENCES

		L8C2011/2021/2031/2041-									
		50		35		25		20		15	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
tRLRL	Read Cycle Time	65		45		35		30		25	
tRLQV	Read Low to Output Valid (Access Time)		50		35		25		20		15
tRHRL	Read High to Read Low (Notes 9, 10)	15		10		10		10		8	
tRLRH	Read Low to End of Read Cycle (Notes 9, 10)	50		35		25		20		15	
tRLQZ	Read Low to Output Low Z (Note 2)	10		5		5		5		3	
tRHQV	Read High to Output Valid	5		5		5		5		5	
tRHQZ	Read High to Output High Z (Note 15)		30		20		10		10		10
tWLWL	Write Cycle Time (Note 10)	65		45		35		30		25	
tWLWH	Write Low to Write High (Notes 9, 10)	50		35		25		20		15	
tWHWL	Write High to End of Write Cycle (Notes 9, 10)	15		10		10		10		8	
tDVWH	Data Valid to Write High (Notes 9, 10)	30		18		15		15		10	
tWHDX	Write High to Data Change (Notes 9, 10)	5		0		0		0		0	
tSLSH	Reset Cycle Time (Notes 10, 11)	50		35		25		20		15	
tSLWL	Reset Low to Write Low (Notes 10, 11)	65		45		35		30		25	
tWHSH	Write High to Reset High (Notes 10, 11)	50		35		25		20		15	
tRHSH	Read High to Reset High (Notes 10, 11)	50		35		25		20		15	
tSHWL	Reset High to Write Low (Notes 10, 11)	15		10		10		10		8	
tSLEL	Reset Low to Empty Flag Low		65		45		35		30		25
tSLHH	Reset Low to Half-Full Flag High		65		45		35		30		25
tSLFH	Reset Low to Full Flag High		65		45		35		30		25
tSLAL	Reset Low to Almost Empty/Full Flag Low		65		45		35		30		25

ASYNCHRONOUS READ AND WRITE OPERATION



RESET TIMING

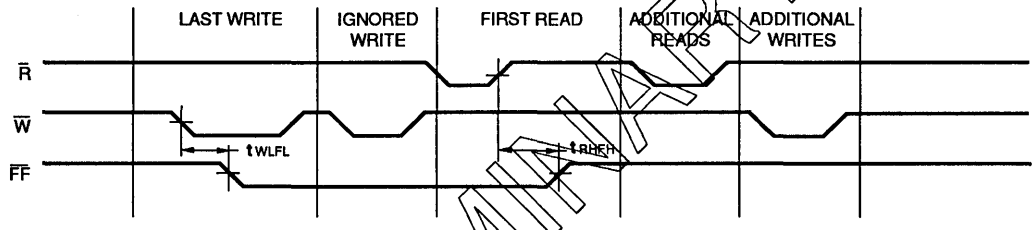


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

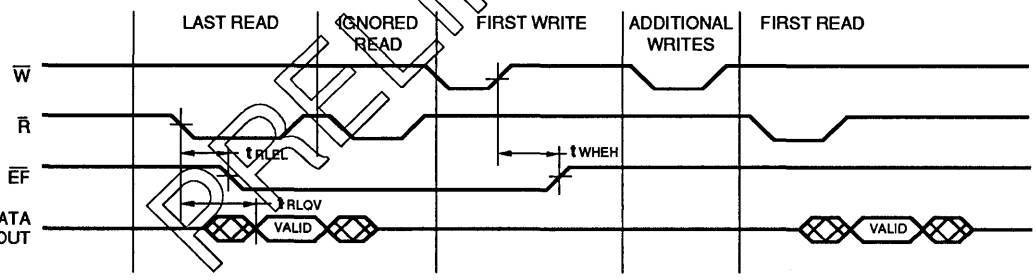
TIMING REFERENCES

Symbol	Parameter	L8C2011/2021/2031/2041- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLQV	Read Low to Output Valid		50		35		25		20		15
tRLEL	Read Low to Empty Flag Low		45		30		25		20		15
tRHFH	Read High to Full Flag High		45		30		25		25		25
tWHEH	Write High to Empty Flag High		45		30		25		25		25
tWLFL	Write Low to Full Flag Low		45		30		25		20		15
tTLAL	Retransmit Cycle Time	65		45		35		30		25	
tTLTH	Retransmit Low to End of Retransmit Cycle (Notes 10, 11)	50		35		25		20		15	
tAHTH	Read/Write High to Retransmit High (Notes 9, 10, 11)	50		35		25		20		15	
tTHAL	Retransmit High to Read/Write Low (Note 10)	15		10		10		10		8	

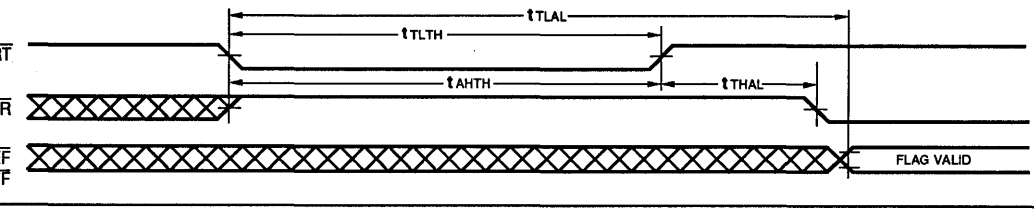
FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE



RETRANSMIT

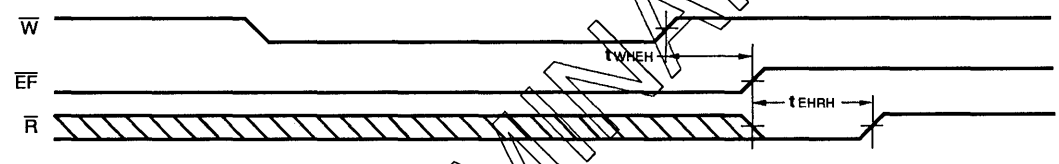


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

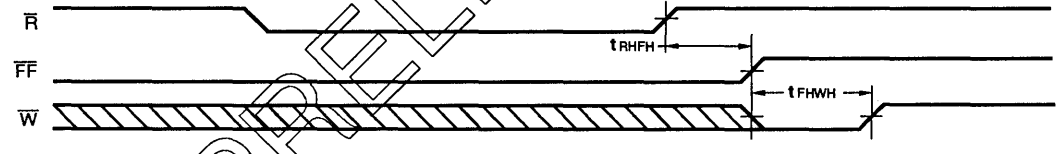
TIMING REFERENCES

Symbol	Parameter	L8C2011/2021/2031/2041- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRHFH	Read High to Full Flag High		45		30		25		25		25
tEHRH	Read Pulse Width After Empty Flag High	50		35		25		20		15	
tWHEH	Write High to Empty Flag High		45		30		25		25		25
tWLHL	Write Low to Half-Full Flag Low		65		45		35		30		25
tRHHH	Read High to Half-Full Flag High		65		45		35		30		25
tFHWH	Write Pulse Width After Full Flag High (Note 10)	50		35		25		20		15	
tRHTA	Read High to Transitioning $\overline{AEF}$		65		45		35		30		25
tWLTA	Write Low to Transitioning $\overline{AEF}$		65		45		35		30		25

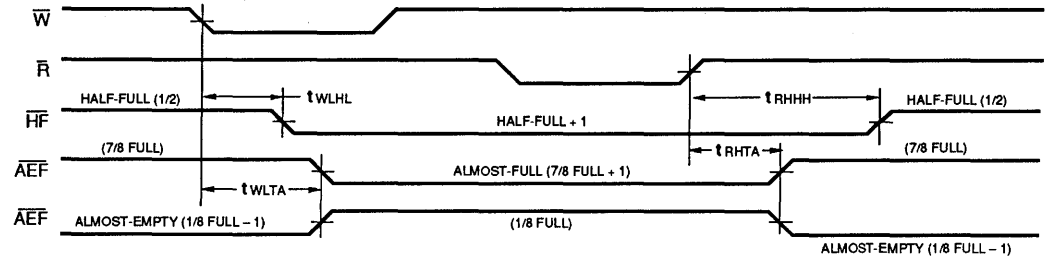
EMPTY FLAG TIMING



FULL FLAG TIMING



ALMOST-EMPTY/FULL FLAG AND HALF-FULL FLAG TIMING

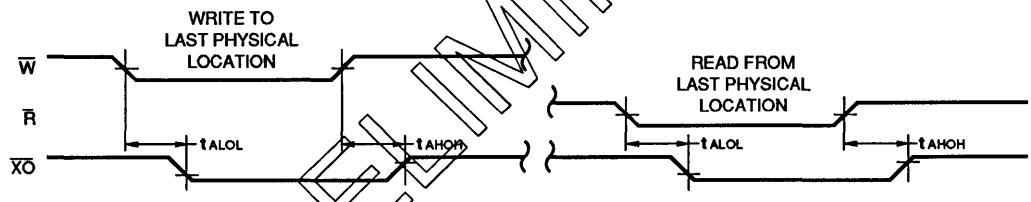


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

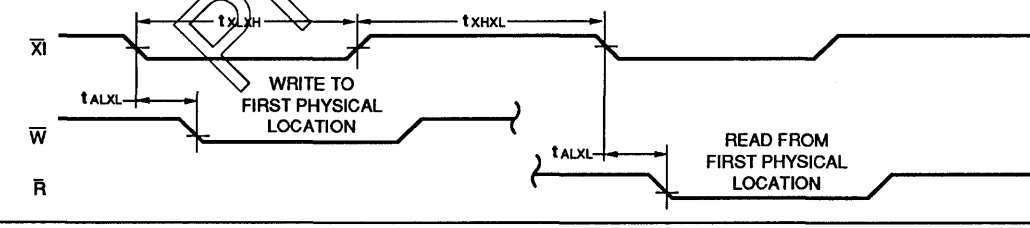
Timing References

Symbol	Parameter	L8C2011/2021/2031/2041- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
t_{ALOL}	Read/Write to Expansion Out Low (Note 12)		50		35		25		20		15
t_{AHOH}	Read/Write to Expansion Out High (Note 12)		50		35		25		20		15
t_{XLXH}	Expansion In Pulse Width (Notes 10, 12)	50		35		25		20		15	
t_{XHXL}	Expansion In High to Expansion In Low (Notes 10, 12)		10		10		10		10		10
t_{ALXL}	Read/Write Low to Expansion In Low (Notes 10, 12)	15		10		10		10		10	
t_{OHQZ}	Output Enable High to Output High Z (Disable)	0	25	0	17	0	12	0	10	0	10
t_{OLQZ}	Output Enable Low to Output Low Z (Enable)	0	25	0	17	0	12	0	10	0	10
t_{OLQV}	Output Enable Low to Output Valid (Q_0–Q_8)		30		20		15		10		10

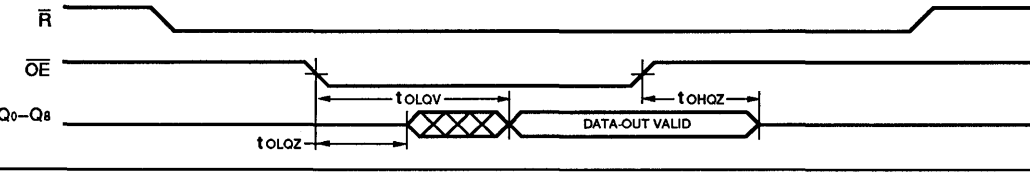
Expansion Out



Expansion In



Output Enable Timing

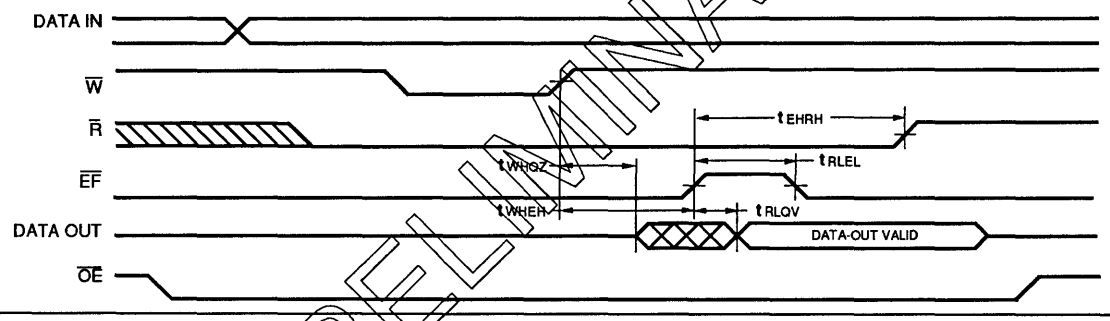


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

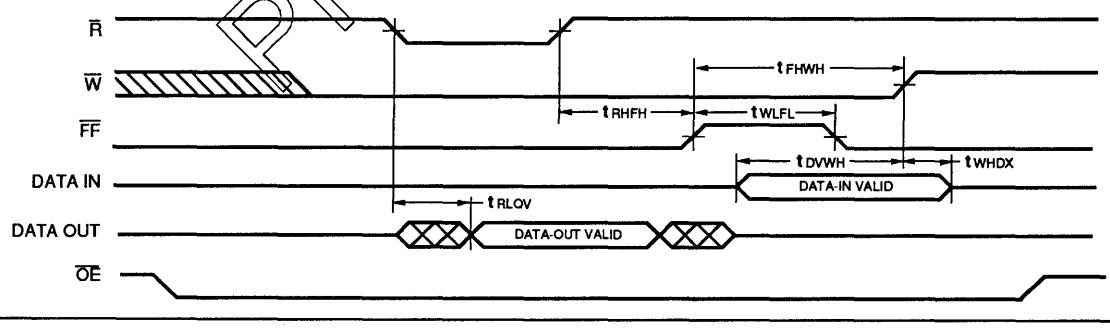
TIMING REFERENCES

Symbol	Parameter	L8C2011/2021/2031/2041- 50 Min	50 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRLEL	Read Low to Empty Flag Low		45		30		25		20		15
tEHRH	Read Pulse Width After Empty Flag High	50		35		25		20		15	
tWHEH	Write High to Empty Flag High	45		30		25		25		25	
tRLQV	Read Low to Output Valid		50		35		25		20		15
tWHQZ	Write High to Output Low Z (Notes 14, 15)	15		10		5		5		3	
tRHFH	Read High to Full Flag High		45		30		25		25		25
tWLFL	Write Low to Full Flag Low		45		30		25		20		15
tFHWH	Write Pulse Width After Full Flag High	50		35		25		20		15	
tDVWH	Data Valid to Write High	30		18		15		15		10	
tWHDX	Write High to Data Change	5		0		0		0		0	

READ DATA FLOW-THROUGH MODE



WRITE DATA FLOW-THROUGH MODE



3

FIFO Memory (Depth Expansion) Block Diagram

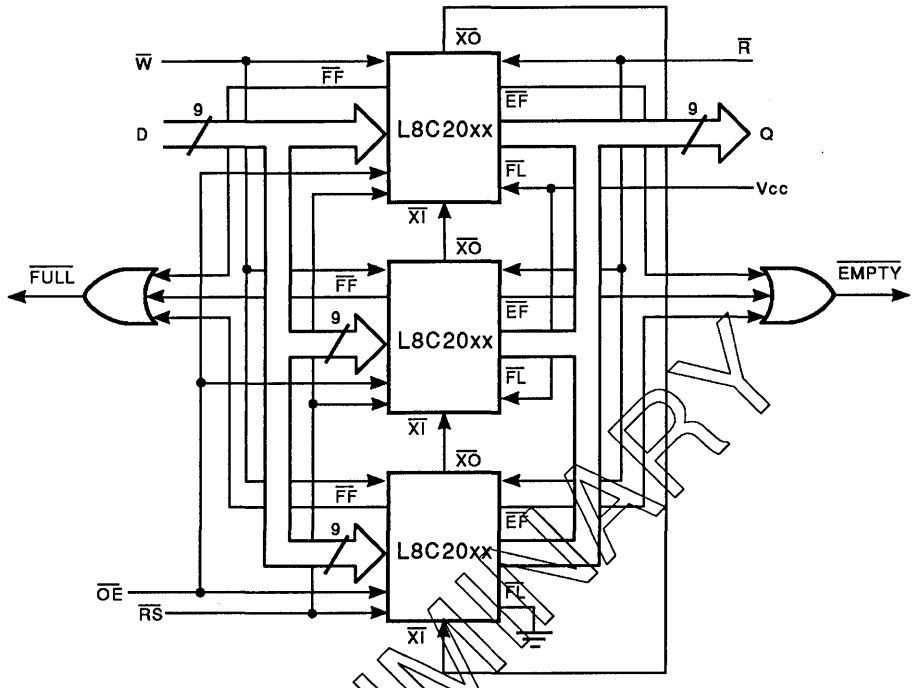


Table 1. Reset and Retransmit *(Single Device Configuration/Width Expansion Mode)*

MODE	INPUTS			INTERNAL STATUS		OUTUPUTS			
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$	$\overline{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment	Increment	X	X	X	X

Table 2. Reset and First Load Truth Table *(Depth Expansion/Compound Expansion Mode)*

MODE	INPUTS			INTERNAL STATUS		OUTUPUTS		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{AEF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1	0
Reset All Others	0	1	(1)	Location Zero Disabled	Location Zero Disabled	0	1	0
Read/Write	1	(2)	(1)	X	X	X	X	X

(1) See Depth Expansion Block Diagram above.
(2) Unchanged.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. Tested with outputs open in the worst static input control signal combination (i.e., $\overline{W}$, $\overline{R}$, $\overline{XI}$, $\overline{FL}$, $\overline{RS}$, and $\overline{OE}$).

8. These parameters are guaranteed but not 100% tested.

9. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RLRH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. When cascading devices, the reset pulse width must be increased to equal $t_{SLSH} + t_{SLHH}$.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

13. Tested with output open and $\overline{OE} = \overline{RS} = \overline{FL} = \overline{XI} = R = \overline{W} = V_{CC}$.

14. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

15. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

16. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

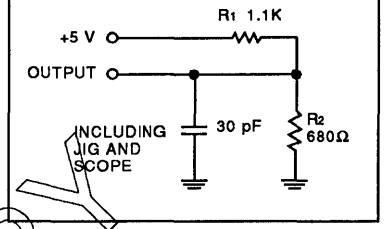


FIGURE 1b.

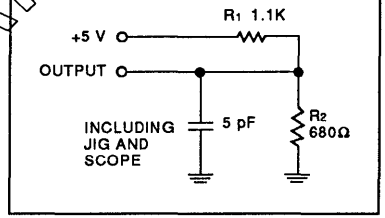
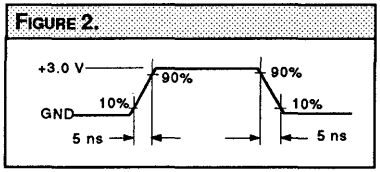


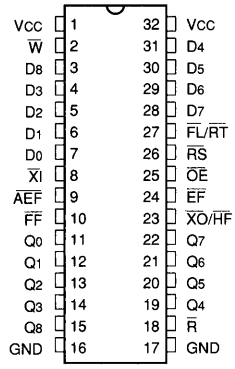
FIGURE 2.

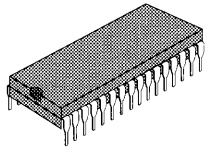


17. Both power and ground pins must be hooked up externally. The pads are not connected together on the die or package. If only one is connected, the device will not work! Pins 17 and 32 are the I/O GND and internal ground respectively.

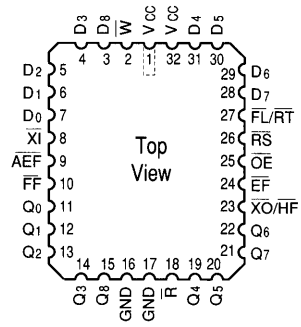
ORDERING INFORMATION

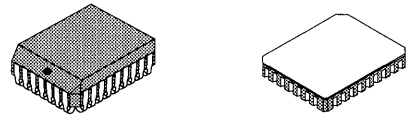
32-pin
(0.6" wide)





32-pin





Speed	Plastic DIP (P14)		Plastic Leaded Chip Carrier (J6)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening			
50 ns 35 ns 25 ns 20 ns 15 ns	L8C2011PC — 50 L8C2021PC — 35 L8C2031PC — 25 or — 20 L8C2041PC — 15		L8C2011JC — 50 L8C2021JC — 35 L8C2031JC — 25 or — 20 L8C2041JC — 15	L8C2011KC — 50 L8C2021KC — 35 L8C2031KC — 25 or — 20 L8C2041KC — 15
	–55°C to +125°C — Commercial Screening			
50 ns 35 ns 25 ns 20 ns 15 ns				L8C2011KM — 50 L8C2021KM — 35 L8C2031KM — 25 or — 20 L8C2041KM
	–55°C to +125°C — Extended Screening			
50 ns 35 ns 25 ns 20 ns 15 ns				L8C2011KME — 50 L8C2021KME — 35 L8C2031KME — 25 or — 20 L8C2041KME
	–55°C to +125°C — MIL-STD-883 Compliant			
50 ns 35 ns 25 ns 20 ns 15 ns				L8C2011KMB — 50 L8C2021KMB — 35 L8C2031KMB — 25 or — 20 L8C2041KMB

64 x 4-bit FIFO
64 x 5-bit FIFO

L8C401/403
L8C402/404

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- Maximum Shift Rate — 50 MHz
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Fast Bubble-Through Time – 16 ns
- Output Enable Available on L8C403 and L8C404
- Plug Compatible with IDT7240x, Cypress CY7C40x
- Package Styles Available:
  - 16/18-pin Plastic DIP
  - 16/18-pin CerDIP
  - 16/18-pin Plastic SOIC
  - 20-pin Plastic LCC
  - 20-pin Ceramic LCC

DESCRIPTION

The **L8C401, L8C402, L8C403,** and **L8C404** are dual-port First-In/First-Out (FIFO) memories. The FIFO memory products are organized as:

L8C401 – 64 × 4-bit
L8C402 – 64 × 5-bit
L8C403 – 64 × 4-bit with $\overline{OE}$
L8C404 – 64 × 5-bit with $\overline{OE}$

Data is shifted into the FIFO through 4-bit or 5-bit Data Input (D_0–D_3, D_4) pins on the rising edge of the Shift In (SI) signal. The stored data stack up at the Data Output (Q_0–Q_3, Q_4) pins in the same order as it entered. When the Shift Out (SO) signal is LOW, data at the next to last word shifts to the output while all other data shift down one location in the stack. The Input Ready (IR) signal acts as a flag to indicate whether the input is ready to accept new data (IR = HIGH), or to indicate when the FIFO is full (IR = LOW). The Output Ready (OR) signal acts as a flag to indicate whether the output contains valid data (OR = HIGH), or to indicate when the FIFO is empty (OR = LOW). The IR and OR signals are also used to provide a signal for cascading.

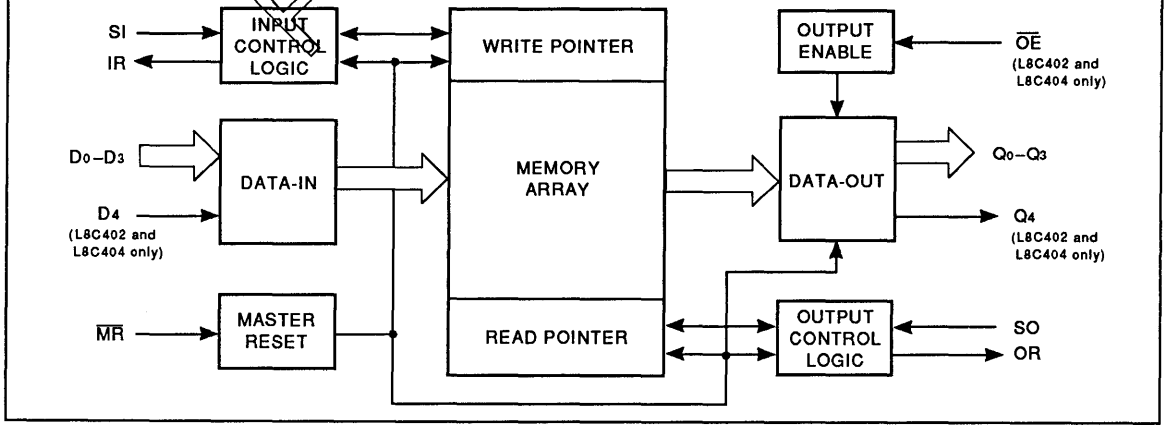
Width expansion is accomplished by logically ANDing the Input Ready (IR) and the Output Ready (OR) signals to form composite signals.

Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready (IR) pin of the receiving device is connected to the Shift Out (SO) pin of the sending device, and the Output Ready (OR) pin of the sending device to the Shift In (SI) pin of the receiving device.

The FIFOs are designed with completely asychronous read and write operations, allowing the FIFO to be used as data buffers between two digital systems of differing operating speeds. The 50 MHz data rate is ideal for high-speed communication and controller applications.

Latchup and static discharge protection is provided on-chip. The FIFOs can withstand an injection current of up to 200 mA on any pin without damage.

L8C401/402/403/404 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	–0.5 V to +7.0 V
DC input voltage	–3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	20 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	–55°C to +125°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA , V_{CC} = Min.			0.4	V
V_{IH}	Input High Voltage		2.0		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} (Note 3)	–10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max. (Note 4)	–20		–90	mA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V Output Disabled (L8C403 and L8C404)	–50		+50	µA
I_{CC}	V_{CC} Current	V_{CC} = Max., f = 10 MHz (Notes 5, 6, 13, 14)			35	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 8)			7	pF

OPERATING DESCRIPTION

CONCEPT

Unlike traditional FIFOs, these devices are designed using a dual-port memory, read and write pointer, and control logic. The read and write pointers are incremented by the Shift Out (SO) and Shift In (SI) respectively. The availability of an empty space to shift data into is indicated by the Input Ready (IR) signal, while the presence of data at the output is indicated by the Output Ready (OR) signal. The conventional concept of bubble through is absent. Instead the delay for input data to appear at the output is the time required to move a pointer and propagate an Output Ready (OR) signal. The Output Enable ($\overline{OE}$) signal provides the capacity to OR tie multiple FIFOs together on a common bus.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty condition signified by the Output Ready (OR) signal being LOW at the same time the Input Ready (IR) signal is HIGH. In this condition, the data outputs (Q_0–Q_3, Q_4) will be in a LOW state.

SHIFT IN (SI) DATA

Data is shifted in on the rising edge of the Shift In (SI) signal. This loads input data into the first word location of the FIFO. On the falling edge of the Shift In (SI) signal, the write pointer is moved to the next word position and the Input Ready (IR) signal goes HIGH indicating the readiness to accept new data. If the FIFO is full, the Input Ready (IR) will remain LOW until a word of data is shifted out.

SHIFT OUT (SO) DATA

Data is shifted out of the FIFO on the falling edge of the Shift Out (SO) signal. This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and the Output Ready (OR) signal will go HIGH. If data is not present, the Output Ready (OR) signal will stay LOW indicating the FIFO is empty. Upon the rising edge of Shift Out (SO), the Output Ready (OR) signal goes LOW. Previous data remains on the output until the falling edge of Shift Out (SO).

BUBBLE THROUGH

Two bubble through conditions exists. The first is when the device is empty. After a word is shifted into an empty device, the data propagates to the output. After a delay, the Output Ready (OR) flag goes HIGH indicating valid data at the output.

The second bubble through condition occurs when the device is full. Shifting data out creates an empty location which propagates to the input. After a delay, the Input Ready (IR) flag goes HIGH. If the Shift In (SI) signal is HIGH at this time, data on the input will be shifted in.

APPLICATION OF THE 25–50 MHz FIFOs

Application of the FIFO requires attention to characteristics not easily specified in a data sheet, but necessary for reliable operation under all conditions.

When an empty FIFO is filled with initial information, at maximum "shift in" (SI) frequency, followed by immediate shifting out of the data also at maximum "shift out" (SO) frequency, the designer must be aware of a window of time which follows the initial rising edge of the "output ready" (OR) signal during which the SO signal is not recognized. This condition exists only at high speed operation where more than one SO may be generated inside the prohibited window. This condition does not inhibit the operation of the FIFO at full frequency operation, but rather delays the full 25–50 MHz operation until after the window has passed.

There are several implementation techniques to manage the window so that all SO signals are recognized:

1. The first involves delaying the SO operation such that it does not occur in the critical window. This can be accomplished by causing a delay, initiated by the SI signal only when the FIFO is empty, to inhibit or gate the SO activity. This, however, requires that the SO operation at least temporarily be synchronized with the input SI operation. In synchronous applications, this may well be possible and a valid solution.
2. Another solution not uncommon in synchronous applications is to only begin shifting data out of the FIFO when it is greater than half full. This is a common method of FIFO application, as earlier FIFOs could not be operated at maximum frequency when near full or empty. Although Logic Devices FIFOs do not have this limitation, any system design in this manner will not encounter the window condition described above.
3. The window may also be managed by not allowing the first SO signal to occur until the window in question has passed. This can be accomplished by delaying the SO from the rising edge of the initial "output ready" (OR) signal. This, however, involves the requirement that this only occurs on the first occurrence of data being loaded into the FIFO from any empty condition and therefore requires the knowledge of "input ready" (IR) and (SI) conditions as well as (SO).
4. Handshaking with the OR signal can be a third method of avoiding the window in question. With this technique, the rising edge of SO, or the fact that the SO signal is HIGH, will cause the OR signal to go LOW. The SO signal is not taken LOW again, advancing the internal pointer to the next data, until the OR signal goes LOW. This assures that the SO pulse that is initiated in the window will be automatically extended sufficient time to be recognized.
5. There remains the decision as to what signal will be used to latch the data from the output of the FIFO into the receiving source. The leading edge of the OR signal is most appropriate because data is guaranteed to be stable prior to and after the OR leading edge for each FIFO. This is a solution for any number of FIFOs in parallel.

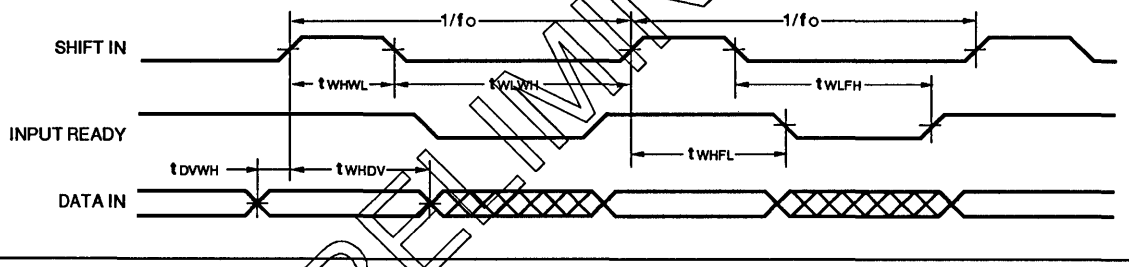
Any of the above solutions will provide a solution for correct operation of a Logic Devices' FIFO at 25–50 MHz. The specific implementation is left to the designer and dependent on the specific application needs.

SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 9)*

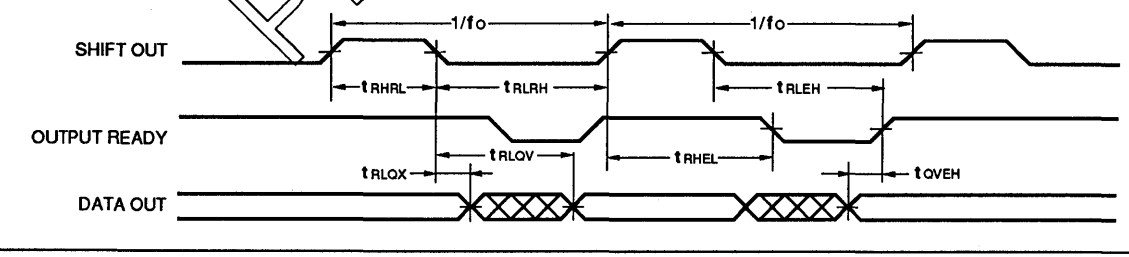
TIMING REFERENCES

Symbol	Parameter	L8C401/402/403/404- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	50 (MHz) Min	50 (MHz) Max
fo	Operating Frequency (in MHz) (Note 17)		15		20		25		35		50
tWHWL	Shift In High to Shift In Low (Note 10)	11		11		11		9		9	
tWLWH	Shift In Low to Shift In High (Note 10)	25		24		24		17		11	
tWLFH	Shift In Low to Input Ready High		40		35		28		20		18
tWHFL	Shift In High to Input Ready Low		35		28		21		18		18
tWHDV	Shift In High to Data Valid (Note 10)	30		25		20		15		13	
tDVWH	Data Valid to Shift In High (Note 10)	0		0		0		0		0	
tRHRL	Shift Out High to Shift Out Low (Note 10)	11		11		11		9		9	
tRLRH	Shift Out Low to Shift Out High	25		24		24		17		11	
tRLEH	Shift Out Low to Output Ready High		40		38		34		20		18
tRHEL	Shift Out High to Output Ready Low		35		28		19		18		18
tRLQV	Shift Out Low to Output Valid (Next Word)		55		45		35		25		17
tRLQX	Shift Out Low to Output Change (Previous Word) (Note 10)	5		5		5		5		5	
tQVEH	Output Valid to Output Ready High (Note 10)	0		0		0		0		0	

INPUT TIMING



OUTPUT TIMING

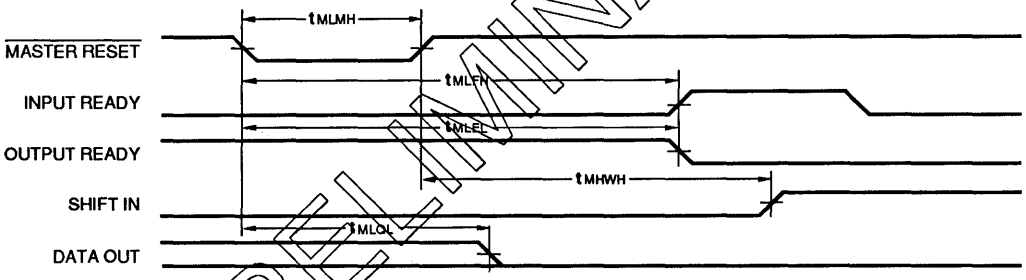


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 9)*

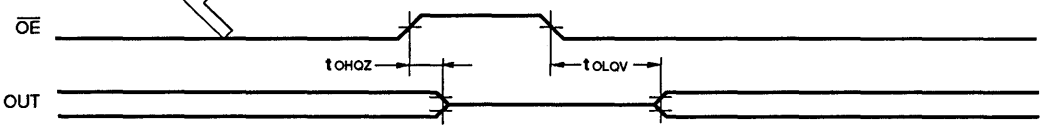
TIMING REFERENCES

Symbol	Parameter	L8C401/402/403/404- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	50 (MHz) Min	50 (MHz) Max
t_{MLMH}	Master Reset Low to Master Reset High (Notes 10, 11)	25		25		25		25		20	
t_{MLFH}	Master Reset Low to Input Ready High		35		35		35		28		25
t_{MLEL}	Master Reset Low to Output Ready Low		35		35		35		28		25
t_{MHWH}	Master Reset High to Shift In High (Note 10)	25		20		10		10		10	
t_{MLQL}	Master Reset Low to Output Low or Zero		35		30		25		20		20
t_{OHQZ}	Output Enable High to Output High Z (Notes 15, 16)		25		20		15		12		12
t_{OLQV}	Output Enable Low to Output Valid (Notes 15, 16)		30		25		20		15		12

MASTER RESET TIMING



OUTPUT ENABLE TIMING

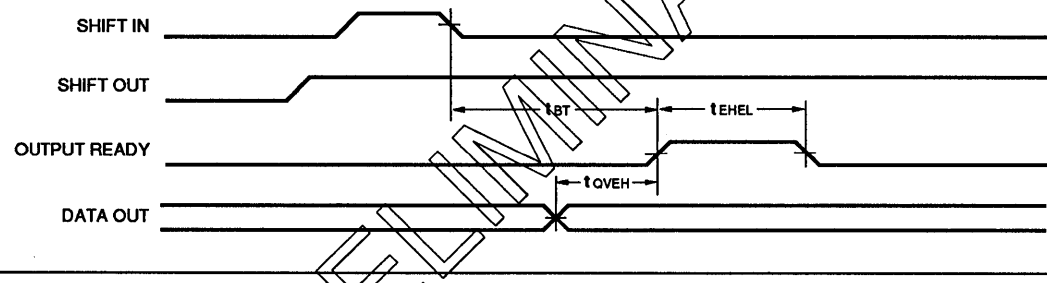


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 9)*

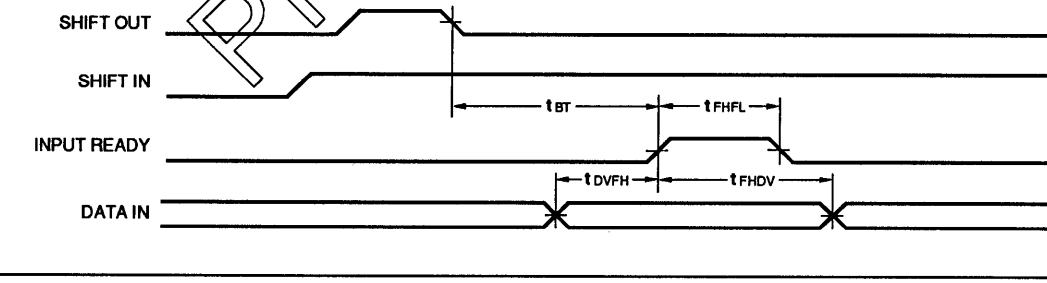
TIMING REFERENCES

Symbol	Parameter	L8C401/402/403/404- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	50 (MHz) Min	50 (MHz) Max
t_{BT}	Bubble Through Time		65		55		40		28		16
t_{EHEL}	Output Ready High to Output Ready Low (Note 18)	9		9		9		9		9	
t_{QVEH}	Output Valid to Output Ready High	0		0		0		0		0	
t_{FHFL}	Input Ready High to Input Ready Low (Note 18)	9		9		9		9		9	
t_{DVFH}	Data Valid to Input Ready High (Note 10)	5		5		5		3		3	
t_{FHDV}	Input Ready High to Data Valid (Note 10)	30		25		20		15		13	

BUBBLE THROUGH, DATA IN TO DATA OUT (CASCADEABLE)



BUBBLE THROUGH, DATA OUT TO DATA IN (CASCADEABLE)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. Tested with outputs open in the worst static input control signal combination.

8. These parameters are guaranteed but not 100% tested.

9. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{RHRL} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. When cascading devices, the reset pulse width must be increased to equal t_{MLMH} + t_{MLEL}.

12. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

13. Tested with output open and minimum capacitance. $\overline{OE}$ is high for L8C403 and L8C404.

14. Icc of devices running at high frequencies can be calculated using the following equation:

Commercial:

Icc = 35 mA + (1.5 mA × [f – 10 MHz]

Military:

Icc = 40 mA + (1.5 mA × [f – 10 MHz]

15. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

16. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

17. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

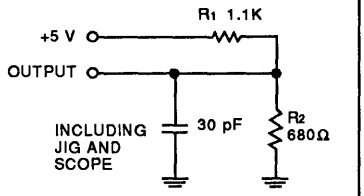


FIGURE 1b.

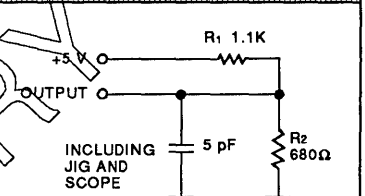
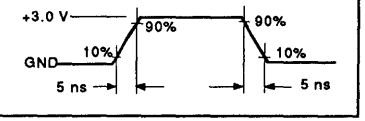


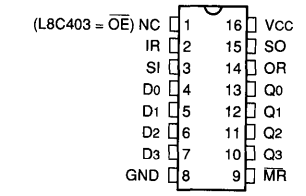
FIGURE 2.

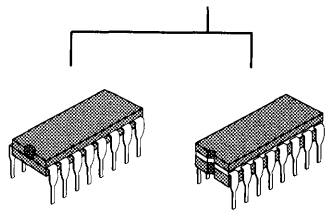


18. The user must be aware that there is no true minimum value for t_{RHEL} and t_{RHFL}. These pulses may be slight during high load under certain operating conditions and lot variations.

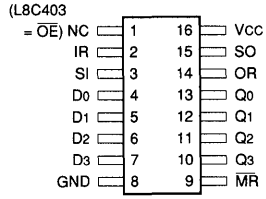
L8C401 and L8C403 ORDERING INFORMATION

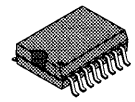
16-pin
(0.3" wide)



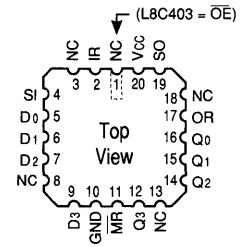


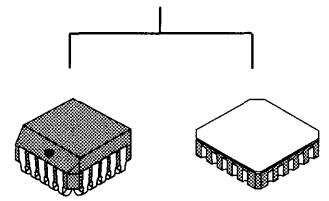
16-pin





20-pin

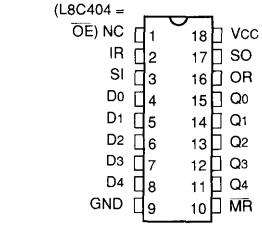


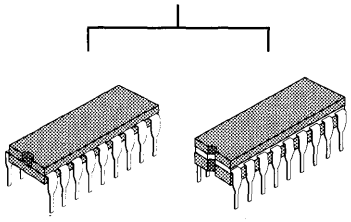


Speed (MHz)	Plastic DIP (P12)	CerDIP (C7)	Plastic SOIC (0.300" — U4)	Plastic Leaded Chip Carrier (J7)	Ceramic Leadless Chip Carrier (K8)
	0°C to +70°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz	L8C401PC or L8C403PC — 15, 20, 25, 35, 50	L8C401CC or L8C403CC — 15, 20, 25, 35, 50	L8C401UC or L8C403UC — 15, 20, 25, 35, 50	L8C401JC or L8C403JC — 15, 20, 25, 35, 50	L8C401KC or L8C403KC — 15, 20, 25, 35, 50
	–55°C to +125°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C401CM or L8C403CM — 15, 20, 25, 35			L8C401KM or L8C403KM — 15, 20, 25, 35
	–55°C to +125°C — Extended Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C401CME or L8C403CME — 15, 20, 25, 35			L8C401KME or L8C403KME — 15, 20, 25, 35
	–55°C to +125°C — MIL-STD-883 Compliant				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C401CMB or L8C403CMB — 15, 20, 25, 35			L8C401KMB or L8C403KMB — 15, 20, 25, 35

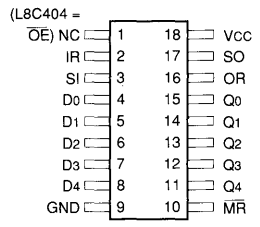
L8C402 and L8C404 ORDERING INFORMATION

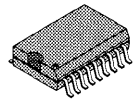
18-pin (0.3" wide)



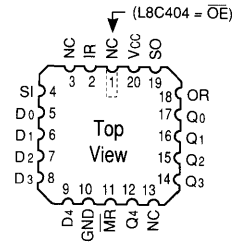


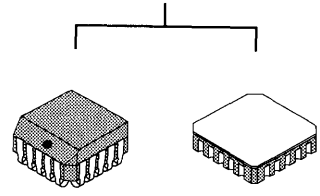
18-pin





20-pin





Speed (MHz)	Plastic DIP (P13)	CerDIP (C8)	Plastic SOIC (0.300" — U5)	Plastic Leaded Chip Carrier (J7)	Ceramic Leadless Chip Carrier (K8)
	0°C to +70°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz	L8C402PC or L8C404PC — 15, 20, 25, 35, 50	L8C402CC or L8C404CC — 15, 20, 25, 35, 50	L8C402UC or L8C404UC — 15, 20, 25, 35, 50	L8C402JC or L8C404JC — 15, 20, 25, 35, 50	L8C402KC or L8C404KC — 15, 20, 25, 35, 50
	–55°C to +125°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C402CM or L8C404CM — 15, 20, 25, 35			L8C402KM or L8C404KM — 15, 20, 25, 35
	–55°C to +125°C — Extended Screening				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C402CME or L8C404CME — 15, 20, 25, 35			L8C402KME or L8C404KME — 15, 20, 25, 35
	–55°C to +125°C — MIL-STD-883 Compliant				
15 MHz 20 MHz 25 MHz 35 MHz 50 MHz		L8C402CMB or L8C404CMB — 15, 20, 25, 35			L8C402KMB or L8C404KMB — 15, 20, 25, 35

64 x 5-bit FIFO with Flags — L8C413

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- Maximum Shift Rate — 45 MHz
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Fast Bubble-Through Time – 16 ns
- Cascadable by Word Depth at 25 MHz and 35 MHz
- Half Full and Almost Full/Empty Status Flags
- Plug Compatible with IDT72413
- Package Styles Available:
  - 20-pin Plastic DIP
  - 20-pin CerDIP
  - 20-pin Plastic SOIC
  - 20-pin Plastic LCC
  - 20-pin Ceramic LCC

DESCRIPTION

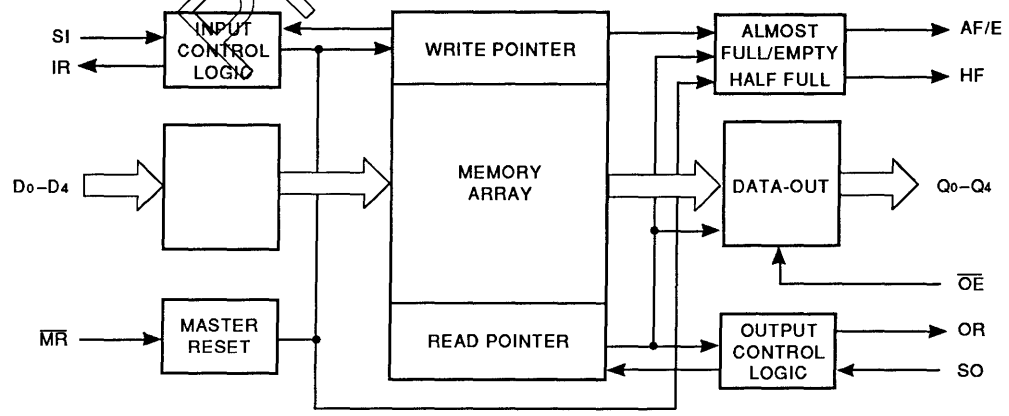
The **L8C413** is a dual-port 64 × 5-bit First-In/First-Out (FIFO) memory. In addition to the industry standard handshaking signals, Almost Full/Almost Empty (AF/E) and Half Full (HF) flags are provided. AF/E is HIGH when the FIFO is almost full or almost empty. Otherwise, AF/E is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW. The FIFO accepts data inputs (D_0–D_4) under the control of Shift In (SI) signal when the Input Ready (IR) control signal is HIGH. The data is output in the same order as it was stored on the data output pins (Q_0–Q_4) under the control of the Shift Out (SO) input when the Output Ready (OR) signal is HIGH. If the FIFO is full (IR = LOW), pulses at the SI input are ignored. When the FIFO is empty (OR = LOW), pulses at the SO input are ignored.

Cascading the FIFO horizontally (wider word size) or vertically or both can be accomplished by use of the IR and OR pins. Parallel expansion for wider words is done by logically ANDing the IR and OR outputs respectively of individual FIFOs together. This ensures that all FIFOs are either ready to accept more data (IR = HIGH) or ready to output data (OR = HIGH) and thus compensate for variations in propagation delay times between devices. Serial expansion for deeper FIFO words is possible except for the 45 MHz standalone devices.

The L8C413 is designed with completely asychronous read and write operations, allowing the FIFO to be used as data buffers between two digital systems of differing operating speeds. The 45 MHz data rate is ideal for high-speed communication and controller applications.

Latchup and static discharge protection is provided on-chip. The L8C413 can withstand an injection current of up to 200 mA on any pin without damage.

L8C413 Block Diagram



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	–0.5 V to +7.0 V
DC input voltage	–3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	50 mA
Latchup current	> 200 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	–55°C to +125°C	5.0 V ±10%

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –4.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA, V_{CC} = Min. (Q_0–Q_4)			0.5	V
		I_{OL} = 8.0 mA, V_{CC} = Min. (IR, OR, HF, AF/E)			0.4	V
V_{IH}	Input High Voltage		2.0		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} (Note 3)	–20		+20	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max. (Note 4)	–20		–90	mA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V Output Disabled	–50		+50	µA
I_{CC}	V_{CC} Current	V_{CC} = Max., f = 25 MHz (Notes 5, 6, 12, 13)			70	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 7)			7	pF

OPERATING DESCRIPTION

L8C413 ARCHITECTURE

The L8C413 FIFO consists of an array of 64 words of 5 bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer, and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AF/E) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard L8C401/402/403/404 FIFOs.

DUAL PORT RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asychronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional shift register architecture.

BUBBLE-THROUGH AND FALL-THROUGH

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fall-Through time (t_{BT}).

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubble-Through time (t_{BT}).

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-through time when it is empty (or nearly empty) and by the bubble-through time when it is full (or near full).

The conventional definitions of fall-through and bubble-through do not apply to the L8C413 FIFO because the data is not physically propagated through memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (Q_0–Q_4) will be LOW. The AF/E flag will be HIGH and the HF flag will be LOW.

SHIFTING DATA INTO THE FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH, a LOW-to-HIGH transition on the Shift In (SI) pin will load the data on the D_0–D_4 inputs into the FIFO.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH-to-LOW transition of the SI signal initiates the LOW-to-HIGH transition of the IR signal, as well as the AF/E flag and the HF flag if the FIFO conditions warrant.

SHIFTING DATA OUT OF THE FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset, all data outputs (Q_0–Q_4) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate the SO pulse.

AF/E AND HF FLAGS

Two flags, Almost Full/Almost Empty (AF/E) and Half Full (HF), describe how may words are stored in the FIFO, AF/E is HIGH when there are eight or less, or 56 or more, words stored in the FIFO. Otherwise the AF/E flag is LOW. HF is HIGH where there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO.

STATUS FLAGS DEFINITION TABLE

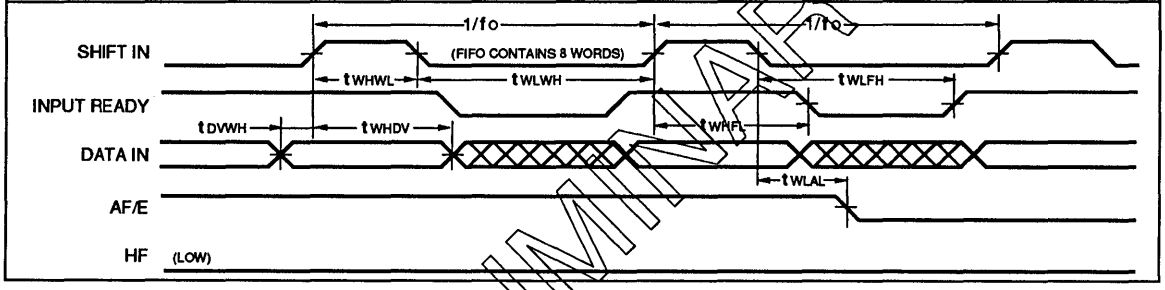
HF	AF/E	WORDS STORED
L	H	0–8
L	L	9–31
H	L	32–55
H	H	56–64

SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

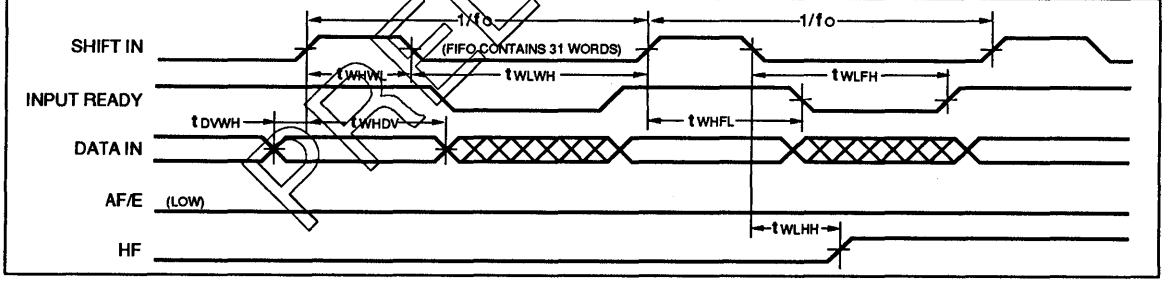
INPUT TIMING REFERENCES

Symbol	Parameter	L8C413- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
fo	Operating Frequency (in MHz) (Note 16)		15		20		25		35		45
tWHWL	Shift In High to Shift In Low (Note 9)	11		11		11		9		9	
tWLWH	Shift In Low to Shift In High (Note 9)	25		20		20		17		11	
tWLFH	Shift In Low to Input Ready High		35		28		25		20		18
tWHFL	Shift In High to Input Ready Low		35		28		21		18		18
tWHDV	Shift In High to Data Valid (Note 9)	30		25		20		15		13	
tDVWH	Data Valid to Shift In High (Note 9)	0		0		0		0		0	
tWLAH	Shift In Low to AF/E High		45		40		35		28		25
tWLAL	Shift In Low to AF/E Low		45		40		35		28		25
tWLHH	Shift In Low to Half Flag High		45		40		35		28		25

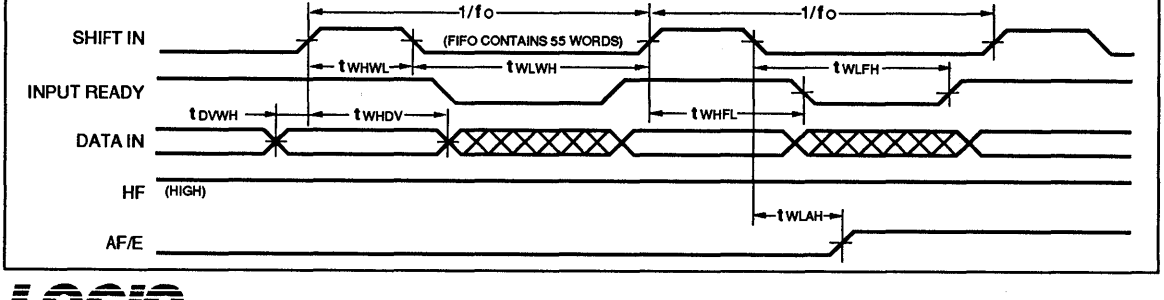
INPUT TIMING (FIFO CONTAINS 8 WORDS)



INPUT TIMING (FIFO CONTAINS 31 WORDS)



INPUT TIMING (FIFO CONTAINS 55 WORDS)

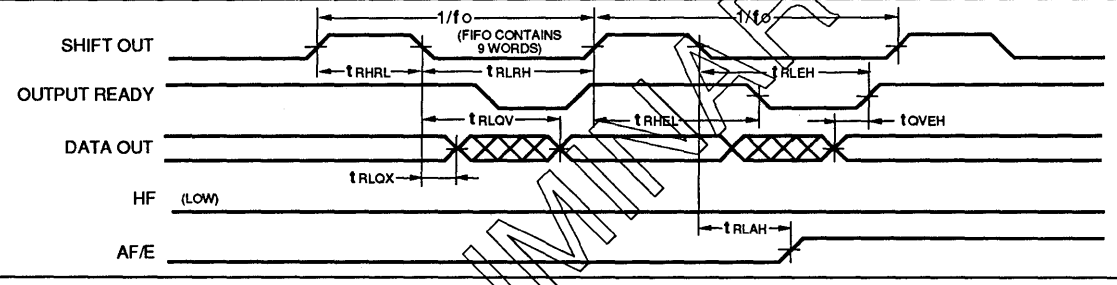


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

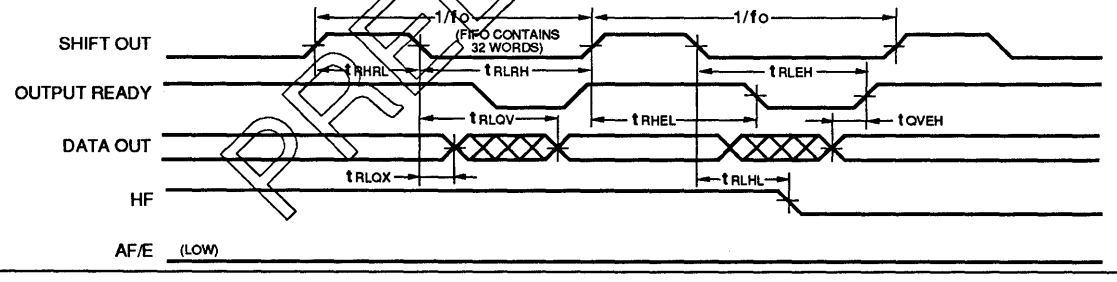
OUTPUT TIMING REFERENCES

Symbol	Parameter	L8C413- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
fo	Operating Frequency (in MHz) (Note 16)		15		20		25		35		45
tRHRL	Shift Out High to Shift Out Low (Note 9)	11		11		11		9		9	
tRLRH	Shift Out Low to Shift Out High	25		24		24		17		11	
tRLEH	Shift Out Low to Output Ready High		38		34		25		20		18
tRHEL	Shift Out High to Output Ready Low		35		28		19		18		18
tRLQV	Shift Out Low to Output Valid (Next Word)		25		25		20		20		17
tRLQX	Shift Out Low to Output Change (Previous Word) (Note 9)	5		5		5		5		5	
tQVEH	Output Valid to Output Ready High (Note 9)	0		0		0		0		0	
tRLAH	Shift Out Low to AF/E High		45		40		35		28		25
tRLAL	Shift Out Low to AF/E Low		45		40		35		28		25
tRLHL	Shift Out Low to Half Flag Low		45		40		35		28		25

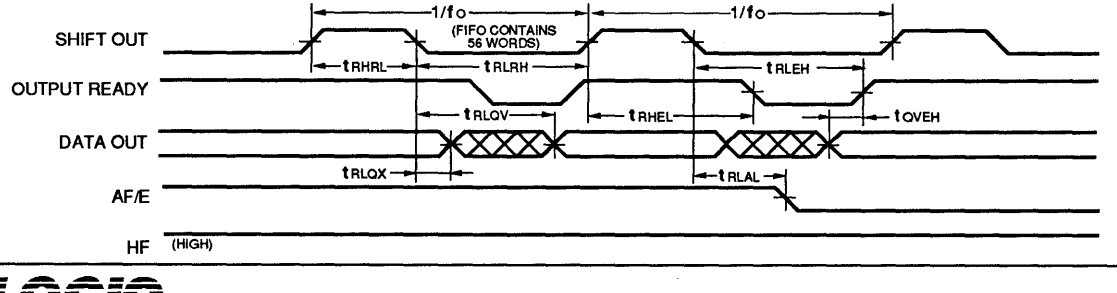
OUTPUT TIMING (FIFO CONTAINS 9 WORDS)



OUTPUT TIMING (FIFO CONTAINS 32 WORDS)



OUTPUT TIMING (FIFO CONTAINS 56 WORDS)

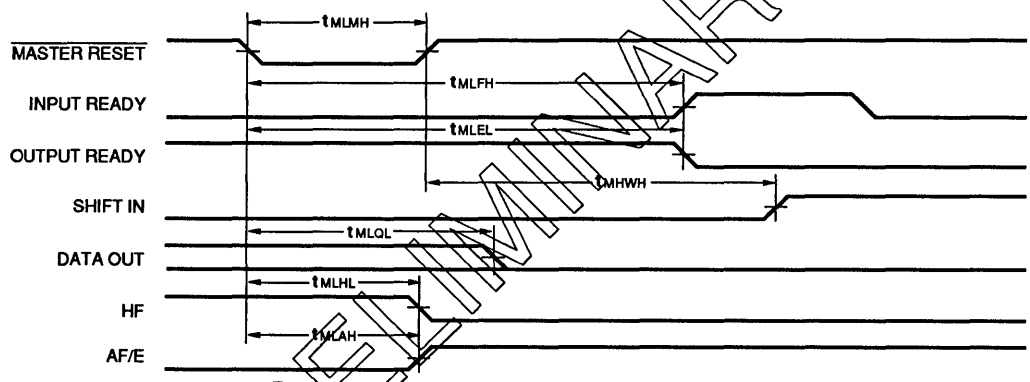


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

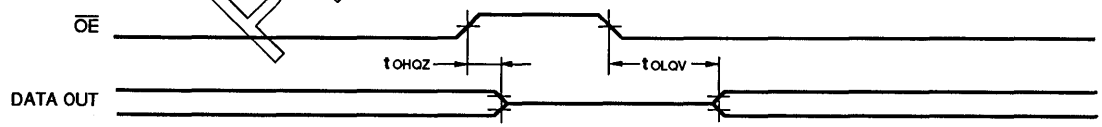
TIMING REFERENCES

Symbol	Parameter	L8C413- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
t_{MLMH}	Master Reset Low to Master Reset High (Notes 9, 10)	25		25		25		25		20	
t_{MLFH}	Master Reset Low to Input Ready High		35		35		35		28		25
t_{MLEL}	Master Reset Low to Output Ready Low		35		35		35		28		25
t_{MHWH}	Master Reset High to Shift In High (Note 9)	25		20		10		10		10	
t_{MLQ}	Master Reset Low to Output Low or Zero		35		30		25		20		20
t_{MLHL}	Master Reset Low to Half Flag Low		48		45		40		28		25
t_{MLAH}	Master Reset Low to AF/E High		48		45		40		28		25
t_{OHQZ}	Output Enable High to Output High Z (Notes 14, 15)		25		20		15		12		12
t_{OLQV}	Output Enable Low to Output Valid (Notes 14, 15)		30		25		20		15		12

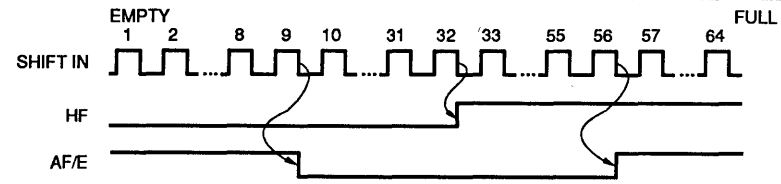
MASTER RESET TIMING



OUTPUT ENABLE TIMING



SHIFTING WORDS IN

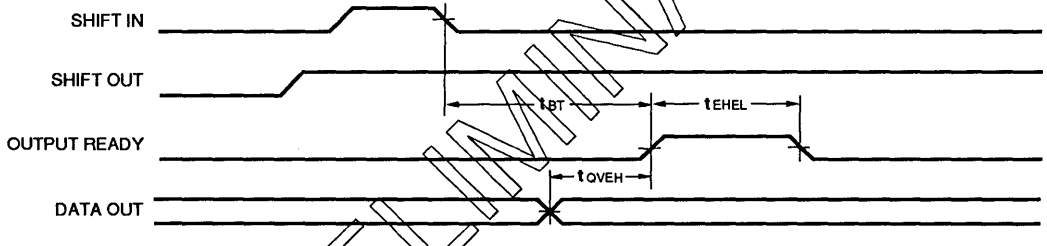


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

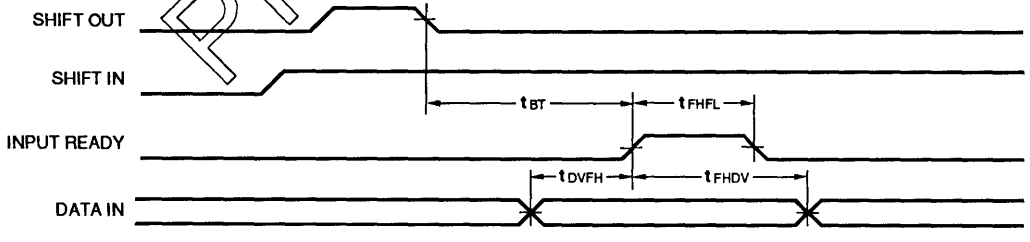
TIMING REFERENCES

Symbol	Parameter	L8C413- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
t_{BT}	Bubble Through Time		65		55		40		28		16
t_{EHEL}	Output Ready High to Output Ready Low (Note 17)	9		9		9		9		9	
t_{QVEH}	Output Valid to Output Ready High	0		0		0		0		0	
t_{FHFL}	Input Ready High to Input Ready Low (Note 17)	9		9		9		9		9	
t_{DVFH}	Data Valid to Input Ready High (Note 9)	5		5		5		3		3	
t_{FHDV}	Input Ready High to Data Valid (Note 9)	30		25		20		15		13	

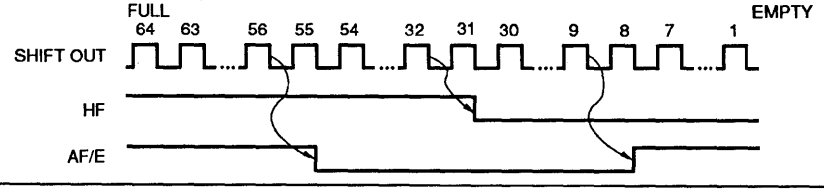
BUBBLE THROUGH, DATA IN TO DATA OUT (CASCADEABLE)



BUBBLE THROUGH, DATA OUT TO DATA IN (CASCADEABLE)



SHIFTING WORDS OUT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. These parameters are guaranteed but not 100% tested.

8. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

9. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{WLWH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. For example, t_{WLFH} is specified as a maximum since worst-case operation of any device always provides data within that time.

10. When cascading devices, the reset pulse width must be increased to equal t_{MLMH} + t_{MLEL}.

11. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

12. Tested with output open and minimum capacitance. $\overline{OE}$ is high.

13. Icc of devices running at high frequencies can be calculated using the following equation:

Commercial:

Icc = 70 mA + (1.5 mA × [f – 25 MHz])

Military:

Icc = 80 mA + (1.5 mA × [f – 25 MHz])

14. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

15. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

16. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

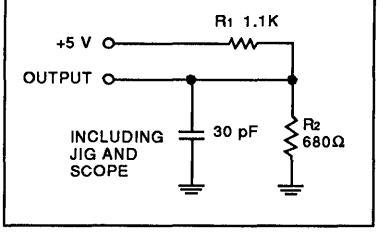


FIGURE 1b.

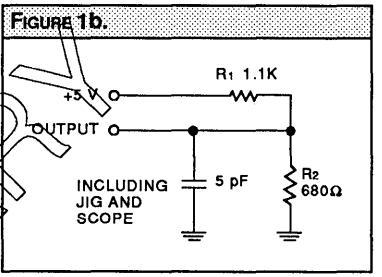
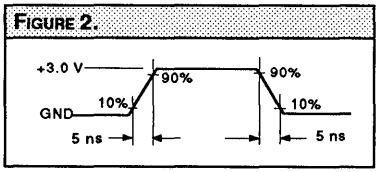


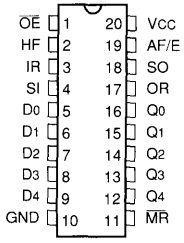
FIGURE 2.

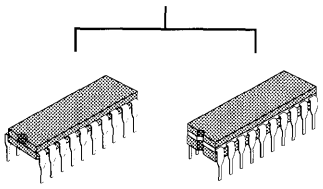


17. The user must be aware that there is no true minimum value for t_{EHEL} and t_{FHFL}. These pulses may be slight during high load under certain operating conditions and lot variations.

ORDERING INFORMATION

20-pin
(0.3" wide)





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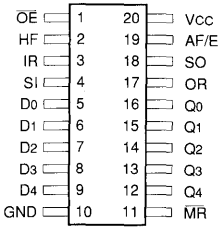
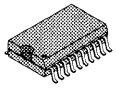
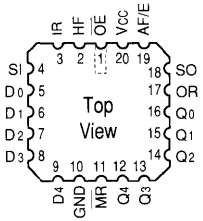
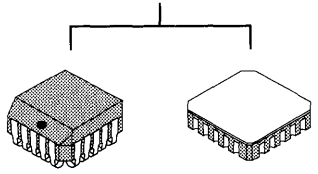




20-pin





Speed (MHz)	Plastic DIP (P6)	CerDIP (C2)	Plastic SOIC (0.300" — U3)	Plastic Leaded Chip Carrier (J7)	Ceramic Leadless Chip Carrier (K8)
	0°C to +70°C — Commercial Screening				
15 MHz	L8C413PC15	L8C413CC15	L8C413UC15	L8C413JC15	L8C413KC15
20 MHz	" " 20	" " 20	" " 20	" " 20	" " 20
25 MHz	" " 25	" " 25	" " 25	" " 25	" " 25
35 MHz	" " 35	" " 35	" " 35	" " 35	" " 35
45 MHz	" " 45	" " 45	" " 45	" " 45	" " 45
	–55°C to +125°C — Commercial Screening				
15 MHz		L8C413CM15			L8C413KM15
20 MHz		" " 20			" " 20
25 MHz		" " 25			" " 25
35 MHz		" " 35			" " 35
45 MHz					
	–55°C to +125°C — Extended Screening				
15 MHz		L8C413CME15			L8C413KME15
20 MHz		" " 20			" " 20
25 MHz		" " 25			" " 25
35 MHz		" " 35			" " 35
45 MHz					
	–55°C to +125°C — MIL-STD-883 Compliant				
15 MHz		L8C413CMB15			L8C413KMB15
20 MHz		" " 20			" " 20
25 MHz		" " 25			" " 25
35 MHz		" " 35			" " 35
45 MHz					

64 x 8- and 9-bit FIFO with Flags + OE — L8C408/409

FEATURES

- First-In/First Out (FIFO) using Dual-Port Memory
- Maximum Shift Rate — 45 MHz
- Asychronous and Simultaneous Read and Write
- Fully Expandable by both Word Depth and/or Bit Width
- Fast Bubble-Through Time – 16 ns
- Cascadable by Word Depth at 25 MHz and 35 MHz
- Half Full and Almost Full/Empty Status Flags
- Plug Compatible withCypress CY7C408/409
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin CerDIP
  - 28-pin Plastic SOIC
  - 28-pin Plastic LCC
  - 28-pin Ceramic LCC

DESCRIPTION

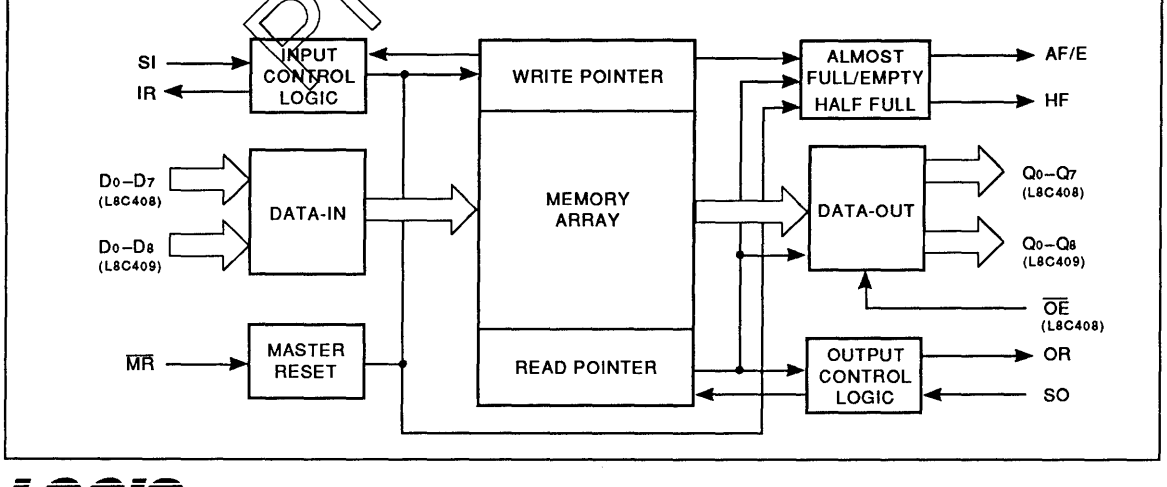
The **L8C408** and **L8C409** are dual-port First-In/First-Out (FIFO) memories organized as 64 x 8 (L8C408) and 64 x 9 (L8C409). In addition to the industry standard handshaking signals, Almost Full/Almost Empty (AF/E) and Half Full (HF) flags are provided. AF/E is HIGH when the FIFO is almost full or almost empty. Otherwise, AF/E is LOW. HF is HIGH when the FIFO is half full, otherwise HF is LOW. The FIFO accepts data inputs (D_0–D_7, D_8) under the control of Shift In (SI) signal when the Input Ready (IR) control signal is HIGH. The data is output in the same order as it was stored on the data output pins (Q_0–Q_7, Q_8) under the control of the Shift Out (SO) input when the Output Ready (OR) signal is HIGH. If the FIFO is full (IR = LOW), pulses at the SI input are ignored. When the FIFO is empty (OR = LOW), pulses at the SO input are ignored.

Cascading the FIFO horizontally (wider word size) or vertically or both can be accomplished by use of the IR and OR pins. Parallel expansion for wider words is done by logically ANDing the IR and OR outputs respectively of individual FIFOs together. This ensures that all FIFOs are either ready to accept more data (IR = HIGH) or ready to output data (OR = HIGH) and thus compensate for variations in propagation delay times between devices. Serial expansion for deeper is accomplished by connecting the data outputs of the FIFO closest to the data source (upstream device) to the data inputs of the following (downstream) FIFO.

The L8C408 and L8C409 are designed with completely asychronous read and write operations, allowing the FIFO to be used as data buffers between two digital systems of differing operating speeds. The 45 MHz data rate is ideal for high-speed communication and controller applications.

Latchup and static discharge protection is provided on-chip. The L8C408 and L8C409 can withstand an injection current of up to 200 mA on any pin without damage.

L8C408/409 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1 and 2)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
DC voltage applied to outputs in High Z state	−0.5 V to +7.0 V
DC input voltage	−3.0 V to +7.0 V
Power Dissipation	1.0 W
Output current into low outputs	20 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%
Active Operation, Military	−55°C to +125°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = Min.	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA, V_{CC} = Min.			0.4	V
V_{IH}	Input High Voltage		2.0		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	−3.0		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} (Note 3)	−10		+10	µA
I_{OS}	Output Short Current	V_{OUT} = GND, V_{CC} = Max. (Note 4)			−90	mA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, V_{CC} = 5.5 V Output Disabled	−50		+50	µA
I_{CC}	V_{CC} Current	V_{CC} = Max., f = 25 MHz (Notes 5, 6, 12, 13, 18)			90	mA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 4.5 V			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 7)			7	pF

OPERATING DESCRIPTION

L8C408 and L8C409 ARCHITECTURE

The L8C408 and L8C409 FIFOs consists of an array of 64 words of 8 and 9 bits each (which are implemented using a dual port RAM cell), a write pointer, a read pointer, and the control logic necessary to generate the handshaking (SI/IR, SO/OR) signals as well as the Almost Full/Almost Empty (AF/E) and the Half Full (HF) flags. The handshaking signals operate in a manner identical to those of the industry standard L8C401/402/403/404 FIFOs.

DUAL PORT RAM

The dual port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asychronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time that would be required for data to propagate through the memory, which would be the case if the memory were implemented using the conventional shift register architecture.

BUBBLE-THROUGH AND FALL-THROUGH

The time required for data to propagate from the input to the output of an initially empty FIFO is defined as the Fall-Through time (t_{BT}).

The time required for an empty location to propagate from the output to the input of an initially full FIFO is defined as the Bubble-Through time (t_{BT}).

The maximum rate at which data can be passed through the FIFO (called the throughput) is limited by the fall-through time when it is empty (or nearly empty) and by the bubble-through time when it is full (or near full).

The conventional definitions of fall-through and bubble-through do not apply to the L8C408 and L8C409 FIFOs because the data is not physically propagated through memory. The read and write pointers are incremented instead of moving the data. However, the parameter is specified because it does represent the worst case propagation delay for the control signals. That is, the time required to increment the write pointer and propagate a signal from the SI input to the OR output of an empty FIFO or the time required to increment the read pointer and propagate a signal from the SO input to the IR output of a full FIFO.

RESETTING THE FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) signal. This causes the device to enter the empty condition, which is signified by the OR signal being LOW at the same time that the IR signal is HIGH. In this condition, the data outputs (Q_0–Q_7, Q_8) will be LOW. The AF/E flag will be HIGH and the HF flag will be LOW.

SHIFTING DATA INTO THE FIFO

The availability of an empty location is indicated by the HIGH state of the Input Ready (IR) signal. When IR is HIGH, a LOW-to-HIGH transition on the Shift In (SI) pin will load the data on the D_0–D_7,D_8 inputs into the FIFO.

The IR output will then go LOW, indicating that the data has been sampled. The HIGH-to-LOW transition of the SI signal initiates the LOW-to-HIGH transition of the IR signal, as well as the AF/E flag and the HF flag if the FIFO condition warrants.

SHIFTING DATA OUT OF THE FIFO

The availability of data at the outputs of the FIFO is indicated by the HIGH state of the Output Ready (OR) signal. After the FIFO is reset, all data outputs (Q_0–Q_7, Q_8) will be in the LOW state. As long as the FIFO remains empty the OR signal will be LOW and all Shift Out (SO) pulses applied to it will be ignored. After data is shifted into the FIFO, the OR signal will go HIGH. The external control logic (designed by the user) should use the HIGH state of the OR signal to generate the SO pulse.

AF/E AND HF FLAGS

Two flags, Almost Full/Almost Empty (AF/E) and Half Full (HF), describe how may words are stored in the FIFO, AF/E is HIGH when there are eight or less, or 56 or more, words stored in the FIFO. Otherwise the AF/E flag is LOW. HF is HIGH where there are 32 or more words stored in the FIFO, otherwise the HF flag is LOW. Flag transitions occur relative to the falling edges of SI and SO.

STATUS FLAGS DEFINITION TABLE

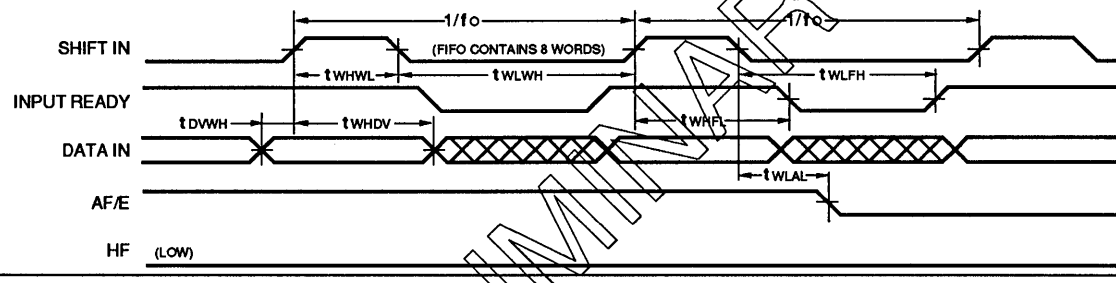
HF	AF/E	WORDS STORED
L	H	0–8
L	L	9–31
H	L	32–55
H	H	56–64

SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

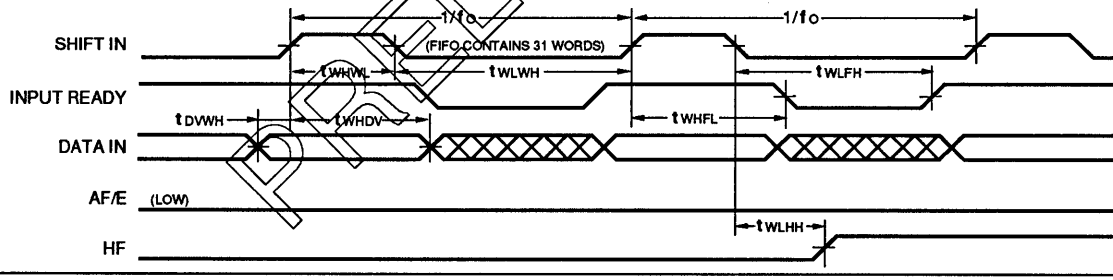
INPUT TIMING REFERENCES

Symbol	Parameter	L8C408/409- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
fo	Operating Frequency (in MHz) (Note 16)		15		20		25		35		45
tWHWL	Shift In High to Shift In Low (Note 9)	11		11		11		9		9	
tWLWH	Shift In Low to Shift In High (Note 9)	25		20		20		17		11	
tWLFH	Shift In Low to Input Ready High		35		28		25		20		18
tWHFL	Shift In High to Input Ready Low		35		28		21		18		18
tWHDV	Shift In High to Data Valid (Note 9)	30		25		20		15		13	
tDVWH	Data Valid to Shift In High (Note 9)	0		0		0		0		0	
tWLAH	Shift In Low to AF/E High		45		40		35		28		25
tWLAL	Shift In Low to AF/E Low		45		40		35		28		25
tWLHH	Shift In Low to Half Flag High		45		40		35		28		25

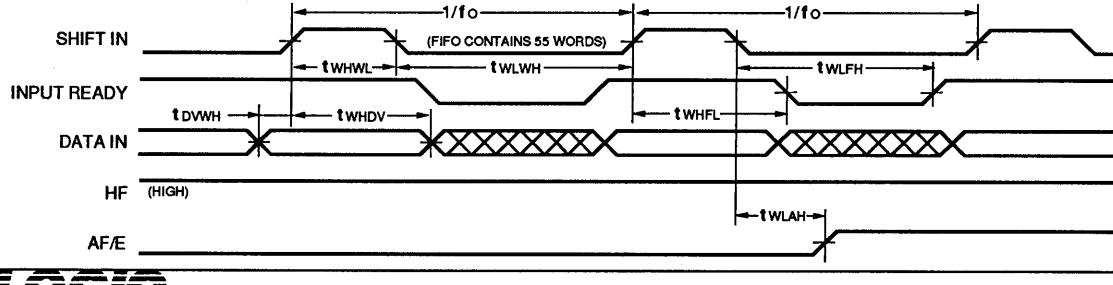
INPUT TIMING (FIFO CONTAINS 8 WORDS)



INPUT TIMING (FIFO CONTAINS 31 WORDS)



INPUT TIMING (FIFO CONTAINS 55 WORDS)

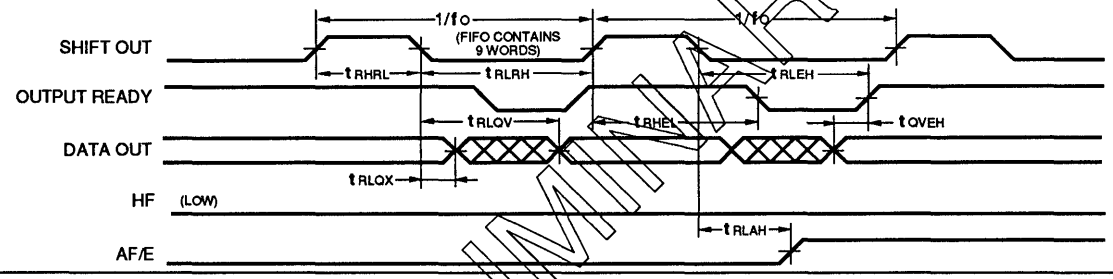


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

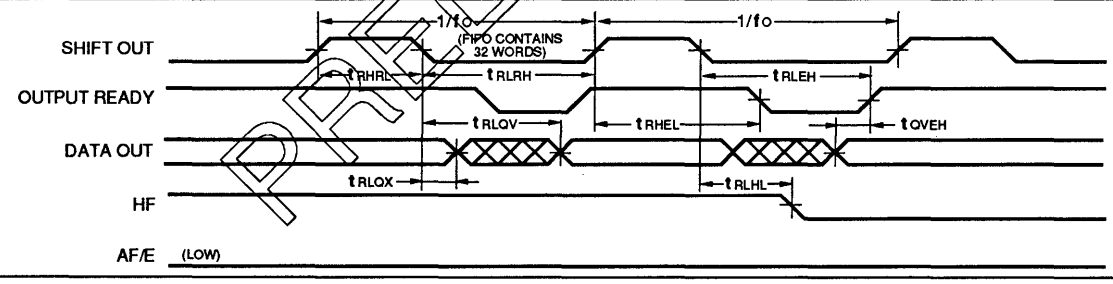
OUTPUT TIMING REFERENCES

Symbol	Parameter	L8C408/409- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
fo	Operating Frequency (in MHz) (Note 16)		15		20		25		35		45
tRHRL	Shift Out High to Shift Out Low (Note 9)	11		11		11		9		9	
tRLRH	Shift Out Low to Shift Out High	25		24		24		17		11	
tRLEH	Shift Out Low to Output Ready High		38		34		25		20		18
tRHEL	Shift Out High to Output Ready Low		35		28		19		18		18
tRLQV	Shift Out Low to Output Valid (Next Word)		25		25		20		20		17
tRLQX	Shift Out Low to Output Change (Previous Word) (Note 9)	5		5		5		5		5	
tQVEH	Output Valid to Output Ready High (Note 9)	0		0		0		0		0	
tRLAH	Shift Out Low to AF/E High		45		40		35		28		25
tRLAL	Shift Out Low to AF/E Low		45		40		35		28		25
tRLHL	Shift Out Low to Half Flag Low		45		40		35		28		25

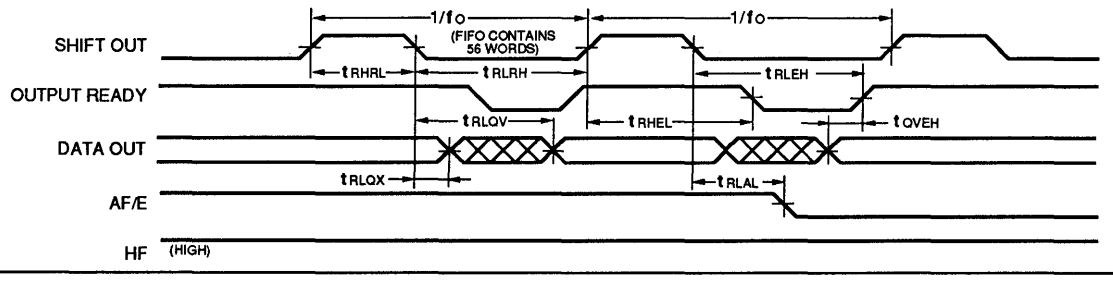
OUTPUT TIMING (FIFO CONTAINS 9 WORDS)



OUTPUT TIMING (FIFO CONTAINS 32 WORDS)



OUTPUT TIMING (FIFO CONTAINS 56 WORDS)

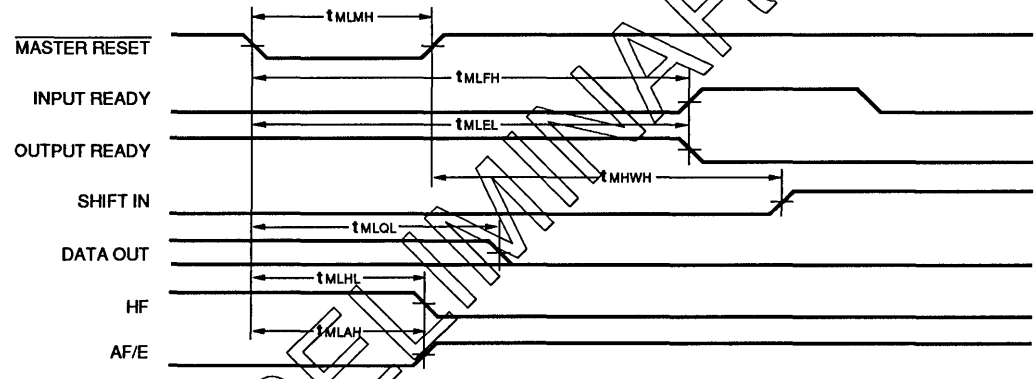


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

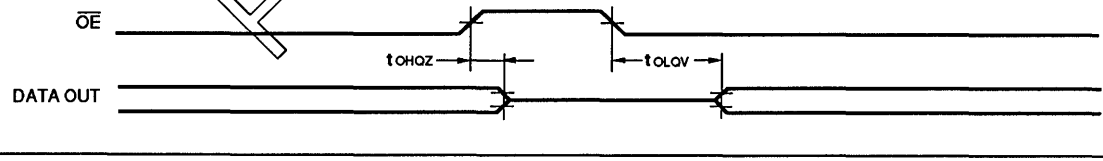
TIMING REFERENCES

Symbol	Parameter	L8C408/409- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
tMLMH	Master Reset Low to Master Reset High (Notes 9, 10)	25		25		25		25		20	
tMLFH	Master Reset Low to Input Ready High		35		35		35		28		25
tMLEL	Master Reset Low to Output Ready Low		35		35		35		28		25
tMHWH	Master Reset High to Shift In High (Note 9)	25		20		10		10		10	
tMLQL	Master Reset Low to Output Low or Zero		35		30		25		20		20
tMLHL	Master Reset Low to Half Flag Low		48		45		40		28		25
tMLAH	Master Reset Low to AF/E High		48		45		40		28		25
tOHQZ	Output Enable High to Output High Z (Notes 14, 15)		25		20		15		12		12
tOLQV	Output Enable Low to Output Valid (Notes 14, 15)		30		25		20		15		12

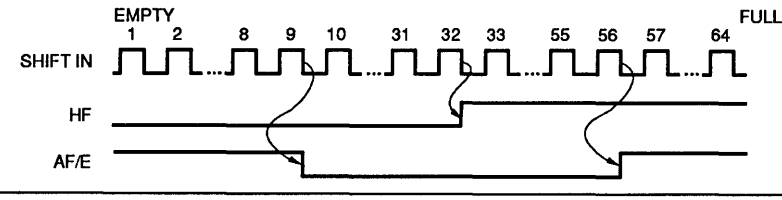
MASTER RESET TIMING



OUTPUT ENABLE TIMING



SHIFTING WORDS IN

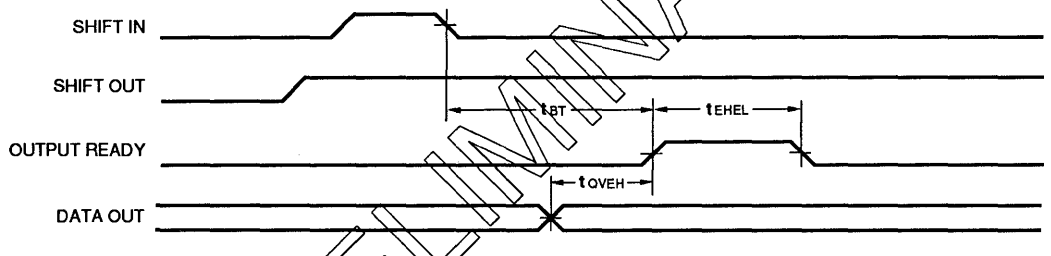


SWITCHING CHARACTERISTICS *Over Operating Range (ns except as noted) (Note 8)*

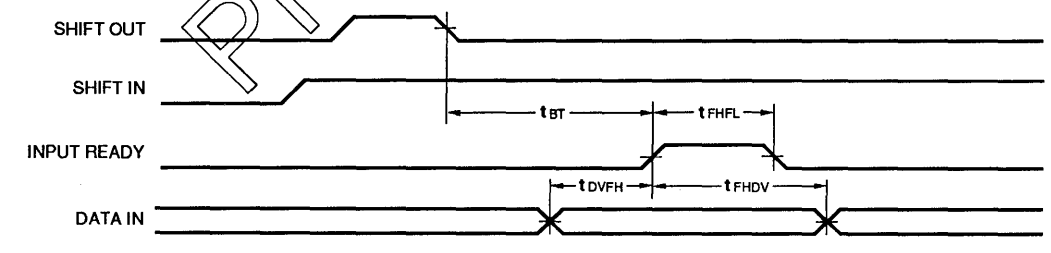
TIMING REFERENCES

Symbol	Parameter	L8C408/409- 15 (MHz) Min	15 (MHz) Max	20 (MHz) Min	20 (MHz) Max	25 (MHz) Min	25 (MHz) Max	35 (MHz) Min	35 (MHz) Max	45 (MHz) Min	45 (MHz) Max
t_{BT}	Bubble Through Time		65		55		40		28		16
t_{EHEL}	Output Ready High to Output Ready Low (Note 17)	9		9		9		9		9	
t_{QVEH}	Output Valid to Output Ready High	0		0		0		0		0	
t_{FHFL}	Input Ready High to Input Ready Low (Note 17)	9		9		9		9		9	
t_{DVFH}	Data Valid to Input Ready High (Note 9)	5		5		5		3		3	
t_{FHDV}	Input Ready High to Data Valid (Note 9)	30		25		20		15		13	

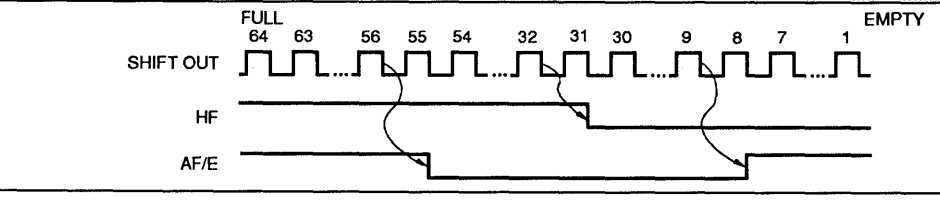
BUBBLE THROUGH, DATA IN TO DATA OUT (CASCADEABLE)



BUBBLE THROUGH, DATA OUT TO DATA IN (CASCADEABLE)



SHIFTING WORDS OUT



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and data inputs changing at the specified read and wrtie cycle rate. The device is neither full or empty for the test.

7. These parameters are guaranteed but not 100% tested.

8. Test conditions assume input transition times of 5 ns or less, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

9. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{WLWH} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. For example, t_{WLFH} is specified as a maximum since worst-case operation of any device always provides data within that time.

10. When cascading devices, the reset pulse width must be increased to equal t_{MLMH} + t_{MLEL}.

11. It is not recommended that Logic Devices and other vendor parts be cascaded together. The parts are designed to be pin-for-pin compatible but temperature and voltage compensation may vary from vendor to vendor. Logic Devices can only guarantee the cascading of Logic Devices parts to other Logic Devices parts.

12. Tested with output open and minimum capacitance. OE is high on the L8C408.

13. Icc of devices running at high frequencies can be calculated using the following equation:

Commercial:

Icc = 90 mA + (2.5 mA × [f – 25 MHz])

Military:

Icc = 100 mA + (2.5 mA × [f – 25 MHz])

14. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

15. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

16. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

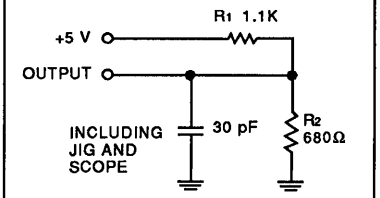


FIGURE 1b.

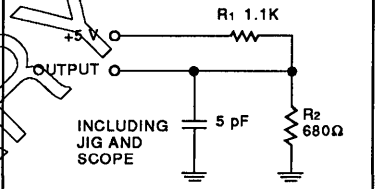
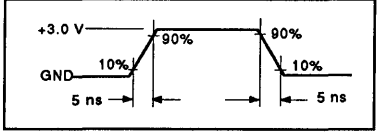


FIGURE 2.

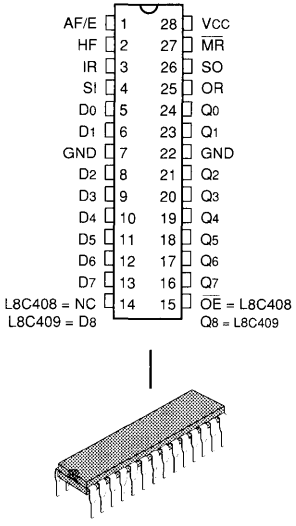


17. The user must be aware that there is no true minimum value for t_{EHEL} and t_{RHFL}. These pulses may be slight during high load under certain operating conditions and lot variations.

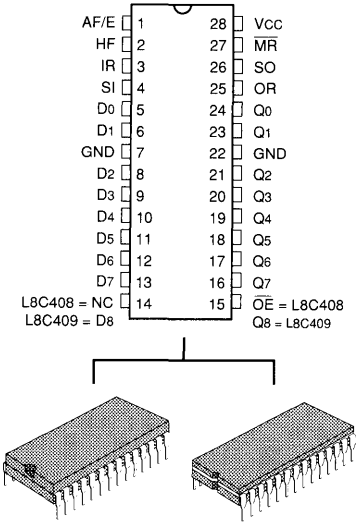
18. Both power and ground pins must be hooked up externally. The pads are not connected together on the die or package. If only one is connected, the device will not work! Pins 9 and 22 are the I/O GND and internal ground respectively.

ORDERING INFORMATION

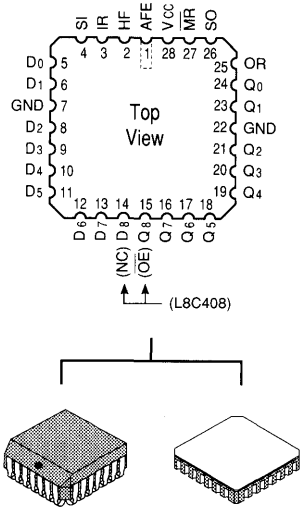
28-pin (0.3" wide)



28-pin (0.6" wide)



28-pin



Speed (MHz)	Plastic DIP (P10)	Plastic DIP (P9)	CerDIP (C6)	Plastic Leaded Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 45 MHz	L8C408PC or L8C409PC — 15, 20, 25, 35, 45	L8C408NC or L8C409NC — 15, 20, 25, 35, 45	L8C408CC or L8C409CC — 15, 20, 25, 35, 45	L8C408JC or L8C409JC — 15, 20, 25, 35, 45	L8C408KC or L8C409KC — 15, 20, 25, 35, 45
	–55°C to +125°C — Commercial Screening				
15 MHz 20 MHz 25 MHz 35 MHz 45 MHz			L8C408CM or L8C409CM — 15, 20, 25, 35		L8C408KM or L8C409KM — 15, 20, 25, 35
	–55°C to +125°C — Extended Screening				
15 MHz 20 MHz 25 MHz 35 MHz 45 MHz			L8C408CME or L8C409CME — 15, 20, 25, 35		L8C408KME or L8C409KME — 15, 20, 25, 35
	–55°C to +125°C — MIL-STD-883 Compliant				
15 MHz 20 MHz 25 MHz 35 MHz 45 MHz			L8C408CMB or L8C409CMB — 15, 20, 25, 35		L8C408KMB or L8C409KMB — 15, 20, 25, 35

Ordering Information

Memory Products

FIFO Memory Products

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LMM824 1 Megabit Static RAM Module, Monolithic Pinout + OE (128K × 8-bit) 4-17
LMM4016 4 Megabit Static RAM Module (256K × 64-bit) 4-23

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Product Selection Guide

Static RAM Memory Modules — Product Selection

Part No.[1]	Description	Maximum Speed (ns) Com.	Mil.	Typical Power (mW) Opr.	Standby	Pins	Packages Available[2]
LMM456	256K Module (64K x 4-bit)	15	—	5400	300	28	SIP
LMM624	1 Megabit Module (256K x 4-bit)	20	—	1440	1200	40	DIP
	(128K x 8-bit)			1680	1200		
	(64K x 16-bit)			2160	1200		
LMM824	1 Megabit Module (Monolithic Pinout) (128K x 8-bit) Output Enable	25	[ADVANCED INFORMATION]			32	DIP
LMM4016	4 Megabit Module (256K x 16-bit)		[ADVANCED INFORMATION]			40	DIP

Static RAM Memory Modules — Product Cross Reference

	LOGIC DEVICES PART NUMBER						
Competitor	LMM456 (256K)	LMM624 (1 Megabit)	LMM824 (1 Megabit)	LMM4016 (4 Megabit)			
IDT	IDT7MP456	IDT7M624S	IDT8M824S	IDT7M4016			
Cypress	NA	1621HD	1421HD	1641HD			

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 10 – Packaging for package dimension.

256K (64K x 4-bit) Static RAM Module — LMM456

FEATURES

- 256K (64K × 4-bit) Static RAM Module
- Advanced CMOS Technology
- High Speed — to 15 ns worst-case
- Low Power Operation
  Active: 900 mW
  Standby: 30 mW typical
- Single 5 V (±10%) Power Supply
- TTL-Compatible Inputs and Outputs
- Plug Compatible with IDT7MP456
- Package Styles Available:
  - 28-pin SIP Module

DESCRIPTION

The **LMM456** is a 256K high speed CMOS static RAM module organized as 64K × 4-bits. This module is constructed using four L7C187 64K × 1 static RAMs in plastic surface mount packages assembled on an epoxy laminate SIP substrate.

Memory locations are specified on Address pin A0 through A15. Writing to the memory module is accomplished when the active-low Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both low. Either signal may be used to terminate the Write operation.

Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data In/Data Out pins. The input/output pins stay in a high impedance state when $\overline{CE}$ is high or $\overline{WE}$ is low.

The LMM456 provides asynchronous (unclocked) operation with matching access and cycle times. All inputs and outputs are TTL compatible and operate from a single 5 V power supply.

Latchup and static discharge protection are provided on-chip. The LMM456 can withstand an injection current of up to 200 mA on any pin without damage.

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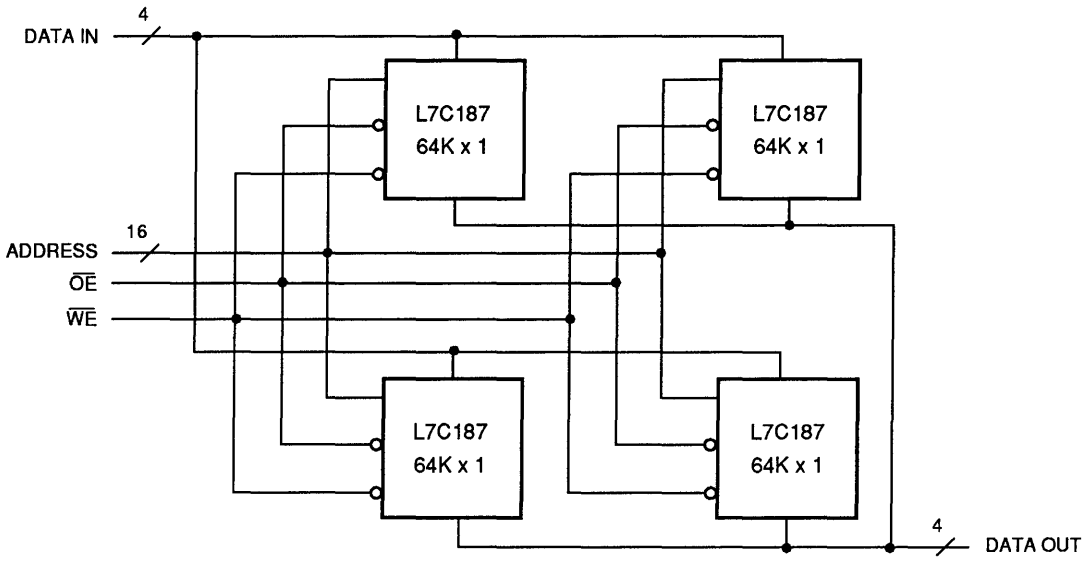
LMM456 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	−55°C to +125°C
Operating ambient temperature	0°C to +70°C
Temperature under bias	−10°C to +85°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
DC output current	50 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA, V_{CC} = 4.5 V			0.4	V
V_{IH}	Input High Voltage		2.2		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	−0.5		0.8	V
I_{IX}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = GND to V_{CC}			15	µA
I_{OZ}	Output Leakage Current	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}			15	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		60	170	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		0.4	2.0	mA
C_{IN}	Input Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, V_{IN} = 0.0 V			35	pF
C_{OUT}	Output Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, V_{OUT} = 0.0 V			40	pF

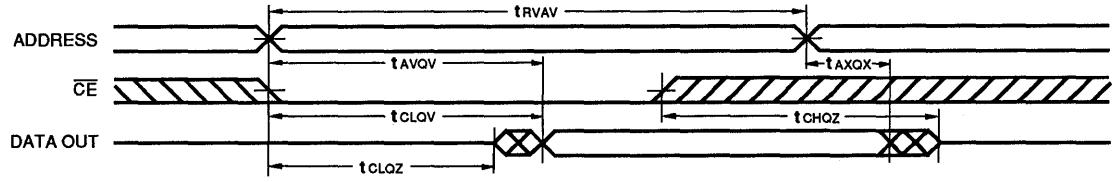
			LMM456-					
Symbol	Parameter	Test Condition	45	35	25	20	15	Unit
I_{CC1}	V_{CC} Current, Active	(Note 5, 6)	220	300	400	500	640	mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

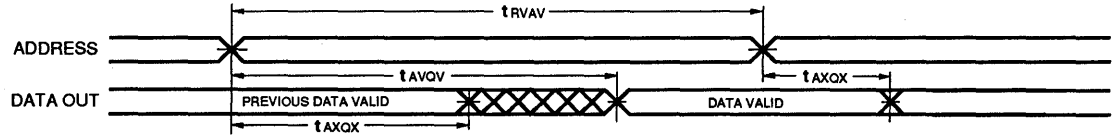
Read Cycle (Notes 11, 12, 22, 23, 24)

Symbol	Parameter	LMM456- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tRVAV	Read Cycle Time	45		35		25		20		15	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		20		15
tAXQX	Address Change to Output Hold	5		5		5		5		5	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		20		15
tCLQZ	Chip Enable Low to Output in Low Z (20, 21)	5		5		5		5		5	
tCHQZ	Chip Enable to Output in High Z (20, 21)		35		30		20		15		10
tPU	Chip Enable Low to Power Up (10, 19)	0		0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20		20

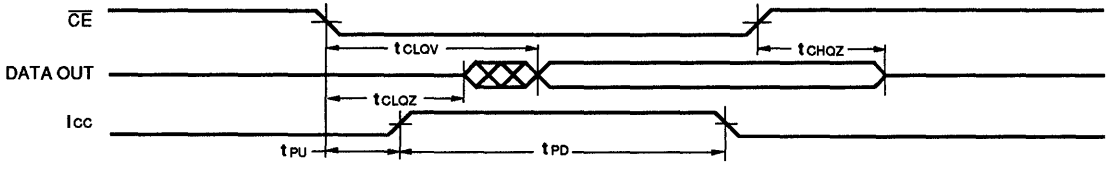
Read Cycle — Address Controlled No. 1 (Notes 13, 14)



Read Cycle — Address Controlled No. 2 (Notes 13, 15)



Read Cycle — CE Controlled (Notes 13, 15)



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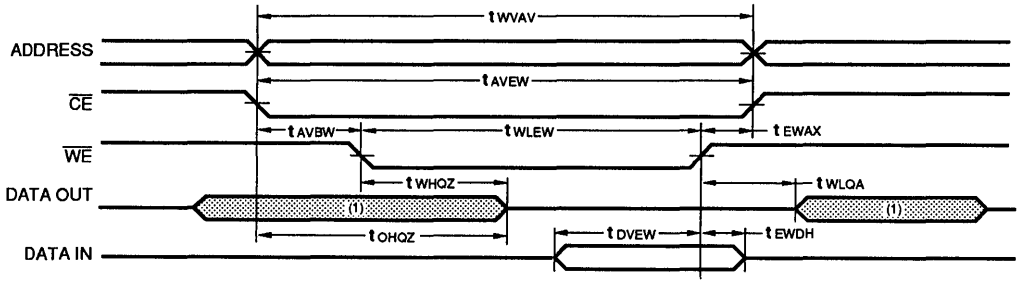
SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

Write Cycle (Notes 11, 12, 22, 23, 24)

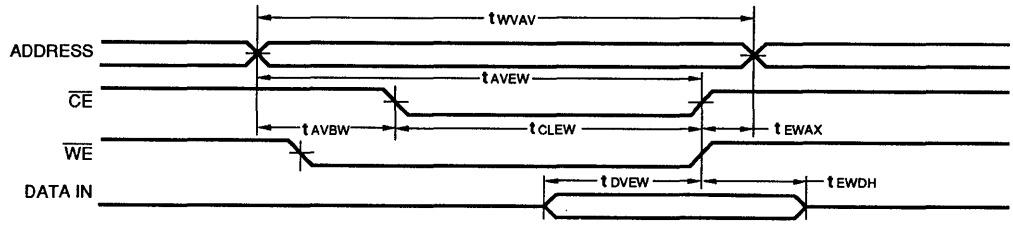
Symbol	Parameter	LMM456- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max	15 Min	15 Max
tWVAV	Write Cycle Time	45		35		25		20		15	
tCLEW	Chip Enable Low to End of Write Cycle	40		30		25		25		15	
tAVBW	Address Valid to Beginning of Write Cycle	5		5		5		5		5	
tAVEW	Address Valid to End of Write Cycle	40		30		25		25		15	
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	35		25		20		20		15	
tDVEW	Data to End of Write Cycle	25		20		15		15		10	
tEWDH	End of Write Cycle to Data Hold	5		5		5		5		5	
tWHQZ	Write Enable High to Output in High Z (20, 21)		30		25		20		20		15
tWLQA	Write Enable Low to Output Active (20, 21)	0		0		0		0		0	

Write Cycle — $\overline{WE}$ Controlled (Notes 16, 17, 18, 19)



(1) During this period, I/O pins are in the output state, and input signals must not be applied.

Write Cycle — $\overline{CE}$ Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.5 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.3 V. For all other inputs VIN ≥ VCC – 0.3 V or VIN ≤ 0.3 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be

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FIGURE 1a.

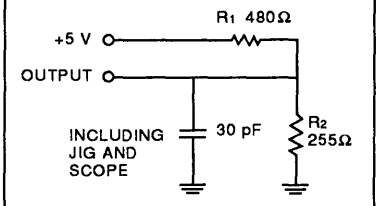


FIGURE 1b.

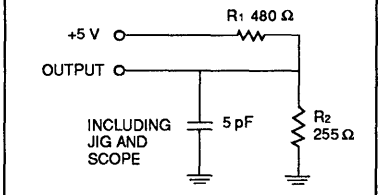
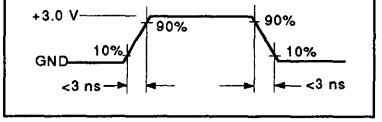
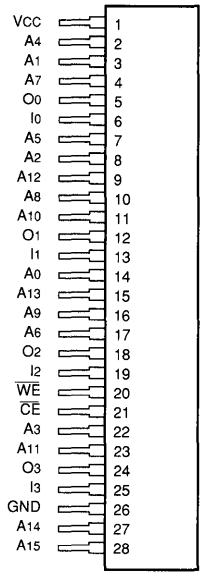


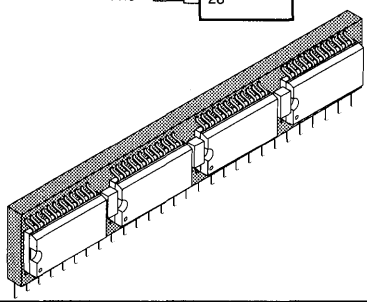
FIGURE 2.



ORDERING INFORMATION

28-pin





Speed	Plastic DIP Surface Mount (S1)
	0°C to +70°C — COMMERCIAL SCREENING
45 ns	LMM456SC45
35 ns	" " 35
25 ns	" " 25
20 ns	" " 20
15 ns	" " 15

1 Megabit (64K x 16-bit) Static RAM Module LMM624

FEATURES

- 1Megabit (64K × 16-bit) Static RAM Module
- Utilizes 16 L7C187 64K × 1 Static RAMs
- Advanced CMOS Technology
- High Speed, Low Power Consumption
- TTL Compatible Inputs and Outputs
- Plug Compatible with IDT7M624S
- Package Styles Available:
  - 40-pin DIP Module

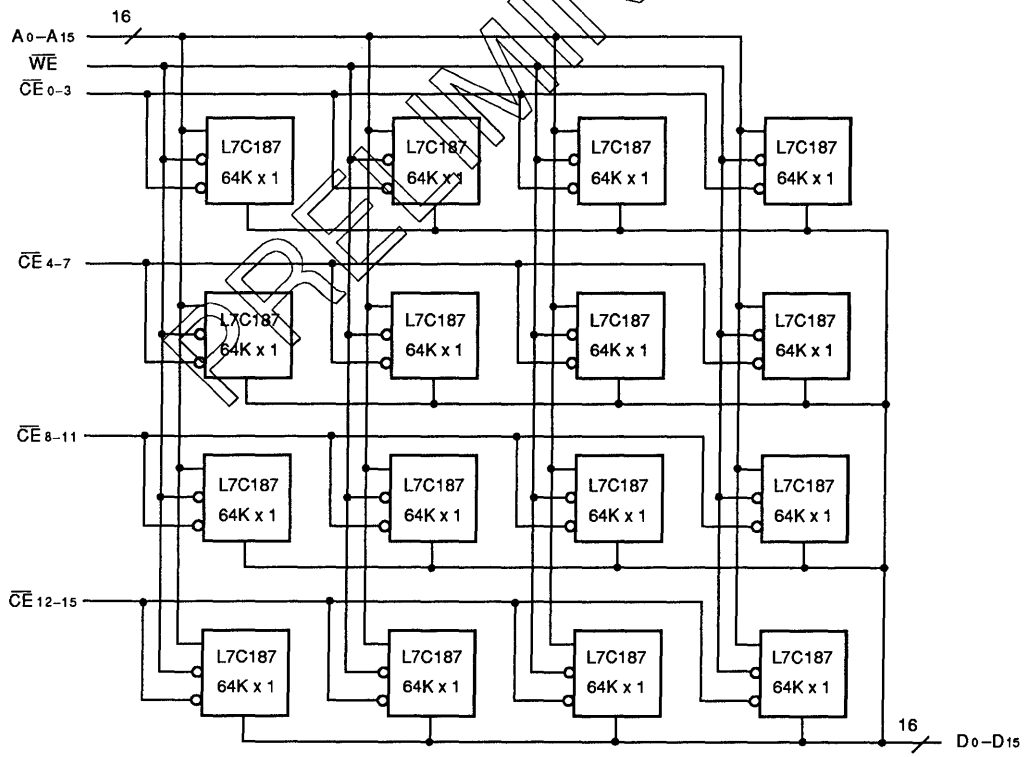
DESCRIPTION

The **LMM624** is a 1 megabit high performance static RAM module organized as 64K × 16 bits. The module is constructed using 16 L7C187, 64K × 1 static RAMs in plastic surface mount packages assembled on an epoxy laminate DIP substrate. Four separate Chip Enable ($\overline{CE}$) pins are available (one for each group of four RAMs). This allows the user to configure the memory as either 256K × 4, 128K × 8, or 64K × 16 organization.

Memory locations are specified on Address pins A_0 through A_{15}. Writing to the memory module is accomplished when the Chip Enable ($\overline{CE}$xx) and the Write Enable ($\overline{WE}$) inputs are both low. Reading from a designated location is accomplished by taking $\overline{CE}$xx low, while $\overline{WE}$ remains high. The data in the addressed memory location will appear on the Data pins. The Data Out is in the high impedance state when $\overline{CE}$xx is high, or $\overline{WE}$ is low.

Latchup and static discharge protection are provided on-chip. The LMM624 can withstand an injection current of up to 200 mA on any pin without damage.

LMM624 Block Diagram



Truth Table

MODE	$\overline{CE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High Z	Active

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... −55°C to +125°C
Operating ambient temperature ..... 0°C to +70°C
Temperature under bias ..... −10°C to +85°C
V_{CC} supply voltage with respect to ground ..... −0.5 V to +7.0 V
DC output current ..... 50 mA
Latchup current ..... > 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (V_{CC})
Active Operation, Commercial	0°C to +70°C	5.0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA, V_{CC} = 4.5 V (Note 11)	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA, V_{CC} = 4.5 V (Note 11)			0.4	V
		I_{OL} = 10.0 mA, V_{CC} = 4.5 V (Note 11)			0.5	V
V_{IH}	Input High Voltage		2.2		6.0	V
V_{IL}	Input Low Voltage	(Note 3)	−0.5		0.8	V
I_{IX}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = GND to V_{CC}			20	µA
I_{OZ}	Output Leakage Current	V_{CC} = 5.5 V, $\overline{CE}_{XX}$ = V_{IH}, V_{OUT} = GND to V_{CC}			20	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		240	480	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		2	16	mA
C_{IN}	Input Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, V_{IN} = 0.0 V			130	pF
C_{OUT}	Output Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, V_{OUT} = 0.0 V			35	pF

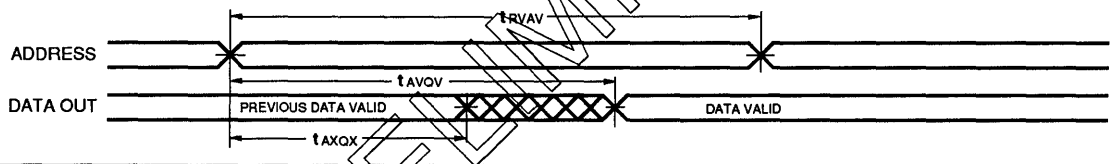
Symbol	Parameter	Test Condition	LMM624- 45	35	25	20		Unit
$I_{CC1(16)}$	V_{CC} Current, Active (x16)	(Notes 5, 6)	880	1200	1600	2000		mA
$I_{CC1(8)}$	V_{CC} Current, Active (x8)	(Notes 5, 6)	680	840	1040	1240		mA
$I_{CC1(4)}$	V_{CC} Current, Active (x4)	(Notes 5, 6)	580	660	760	860		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

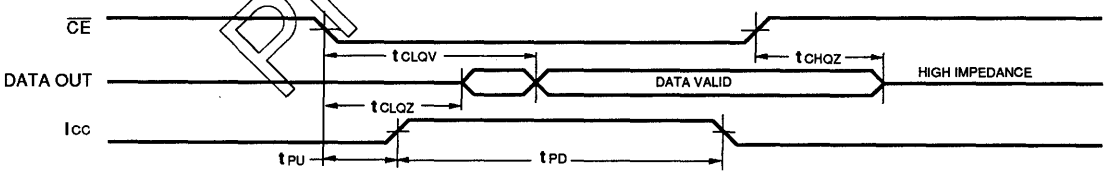
Read Cycle (Notes 11, 12, 22, 23, 24)

Symbol	Parameter	LMM624- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max
tRVAV	Read Cycle Time	45		35		25		20	
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		20
tAXQX	Address Change to Output Hold	5		5		5		5	
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		20
tCLQZ	Chip Enable Low to Output in Low Z (20, 21)	5		5		5		5	
tCHQZ	Chip Enable to Output in High Z (20, 21)		35		30		20		15
tPU	Chip Enable Low to Power Up (10, 19)	0		0		0		0	
tPD	Power Up to Power Down (10, 19)		45		35		25		20

Read Cycle — Address Controlled (Notes 13, 15)



Read Cycle — $\overline{CE}$ Controlled (Notes 13, 15)



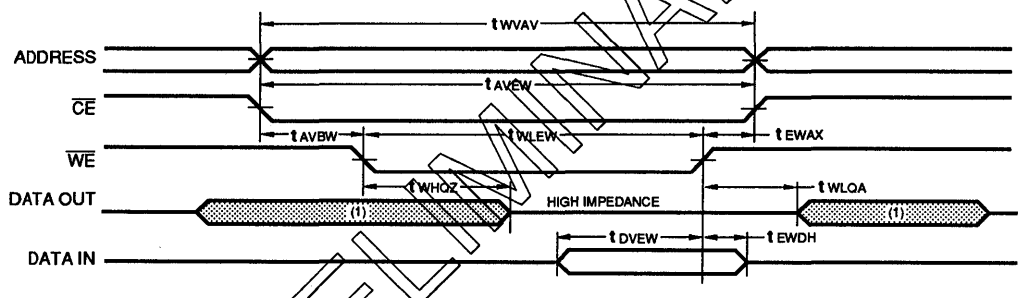
4

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

Write Cycle (Notes 11, 12, 22, 23, 24)

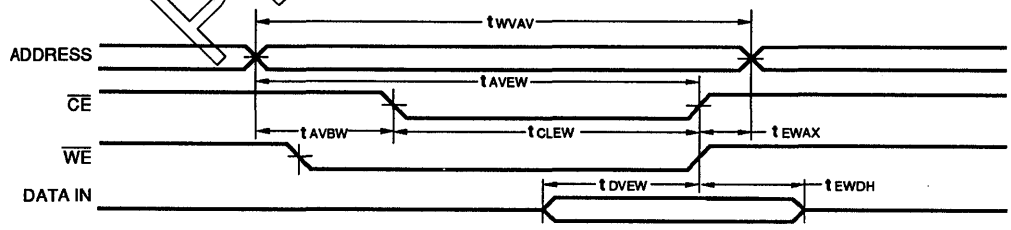
Symbol	Parameter	LMM624S- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	20 Min	20 Max
tWVAV	Write Cycle Time	45		35		25		20	
tCLEW	Chip Enable Low to End of Write Cycle	40		30		25		15	
tAVBW	Address Setup Time	5		5		5		0	
tAVEW	Address Valid to End of Write Cycle	40		30		25		15	
tEWAX	End of Write Cycle to Address Change	0		0		0		0	
tWLEW	Write Enable Low to End of Write Cycle	35		25		20		15	
tDVEW	Data to End of Write Cycle	25		20		15		10	
tEWDH	End of Write Cycle to Data Hold	5		5		5		5	
tWHQZ	Write Enable High to Output in High Z (20, 21)		30		25		20		15
tWLQA	Write Enable Low to Output Active (20, 21)	0		0		0		0	

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



(1) During this period, I/O pins are in the output state, and input signals must not be applied.

Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.5 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.3 V. For all other inputs VIN ≥ VCC – 0.3 V or VIN ≤ 0.3 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 5 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be

FIGURE 1a.

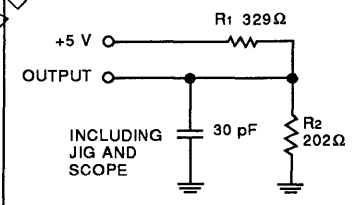


FIGURE 1b.

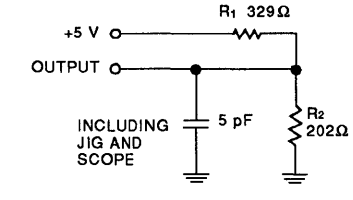
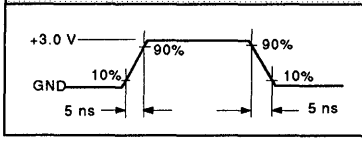
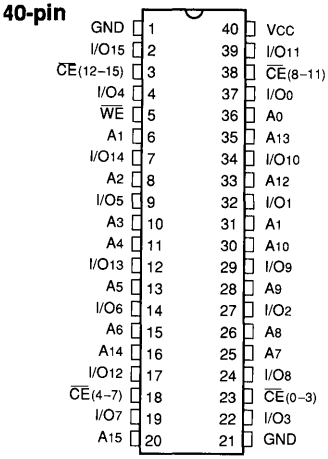


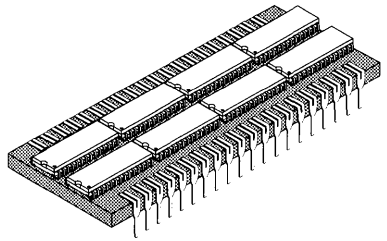
FIGURE 2.



ORDERING INFORMATION

40-pin





Speed	Plastic DIP Module (P16)
	0°C to +70°C — COMMERCIAL SCREENING
45 ns	LMM624P-C45
35 ns	" 35
25 ns	" 25
20 ns	" 20

PRELIMINARY

1 Megabit (128K x 8-bit) Static RAM Module — LMM824

FEATURES

- 1024K (128K × 8-bit) Static RAM Module
- Advanced CMOS Technology
- High Speed — to 25 ns worst-case
- Low Power Operation
  Active: 550 mW
  Standby: 20 mW typical
- Single 5 V (±10%) Power Supply
- Data Retention at 2 V for Battery Backup Operation
- TTL Compatible Inputs and Outputs
- Plug Compatible with IDT8M824S
- Package Styles Available:
  - 32-pin DIP Module

DESCRIPTION

The **LMM824** is a 1 Megabit high performance static RAM module organized as 128K × 8 bits. The module is constructed using four L7C199 32K × 8 static RAMs in plastic surface mount packages assembled on an epoxy laminate DIP substrate. A decoder intreprets the higher order addresses, A_{15} and A_{16}, and selects one of the four static RAMS.

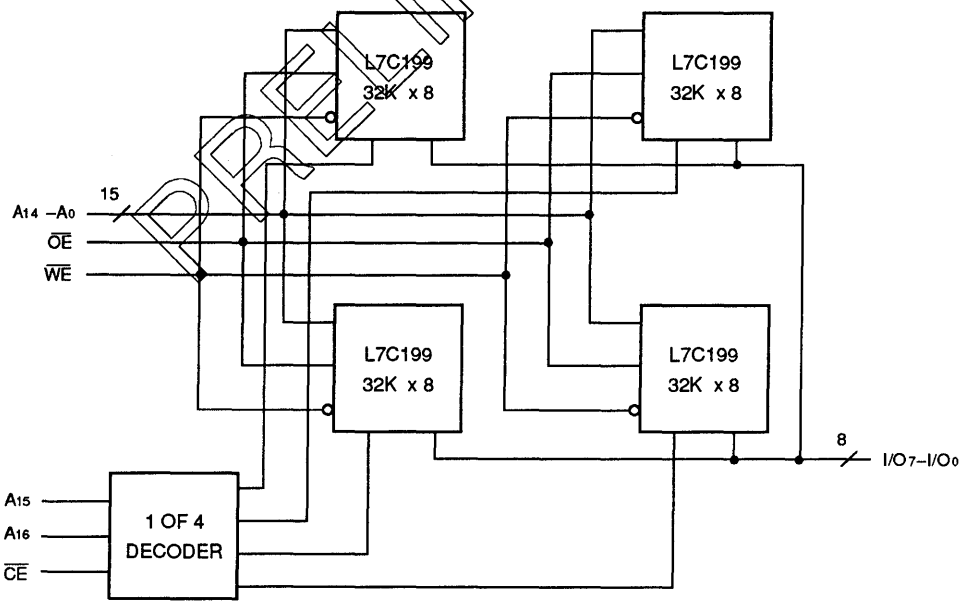
Memory locations are specified on Address pins A_0 through A_{16}. Writing to the memory module is accomplished when the active-low Chip Enable ($\overline{CE}$) and the Write Enable ($\overline{WE}$) inputs are both low. Either of these signals may be used to terminate the Write operation. Reading from a designated location is accomplished by presenting an address then taking $\overline{CE}$ and Output Enable ($\overline{OE}$) low, while $\overline{WE}$ remains high. The data in the addressed memory location will then appear on the Data In/Data Out pins. The input/output pins stay in a high impedance state unless the module is selected, the outputs are enabled, and $\overline{WE}$ is high.

The LMM824 provides asychronous (unclocked) operation with matching access and cycle times. All inputs and outputs are TTL compatible and operate from a single 5 V power supply.

Latchup and static discharge protection are provided on-chip. The LMM824 can withstand an injection current of up to 200 mA on any pin without damage.

4

LMM824 Block Diagram



Truth Table

MODE	CE	OE	WE	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	DATAOUT	Active
Read	L	H	H	High Z	Active
Write	L	X	L	DATAIN	Active

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... −55°C to +125°C
Operating ambient temperature ..... 0°C to +70°C
Temperature under bias ..... −10°C to +85°C
VCC supply voltage with respect to ground ..... −0.5 V to +7.0 V
DC output current ..... 50 mA
Latchup current ..... > 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage (VCC)
Active Operation, Commercial	0°C to +70°C	5 .0 V ±10%

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = −4.0 mA, VCC = 4.5 V	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA, VCC = 4.5 V			0.4	V
VIH	Input High Voltage		2.2		6.0	V
VIL	Input Low Voltage	(Note 3)	−0.5		0.8	V
IIX	Input Leakage Current	VCC = 5.5 V, VIN = GND to VCC			15	µA
IOZ	Output Leakage Current	VCC = 5.5 V, $\overline{CE}$ = VIH, VOUT = GND to VCC			15	µA
ICC2	VCC Current, TTL Inactive	(Note 7)		80	160	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		8	40	mA
CIN	Input Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, VIN = 0.0 V			35	pF
COUT	Output Capacitance	Amb. Temp. = 25°C, f = 1.0 MHz, VOUT = 0.0 V			40	pF

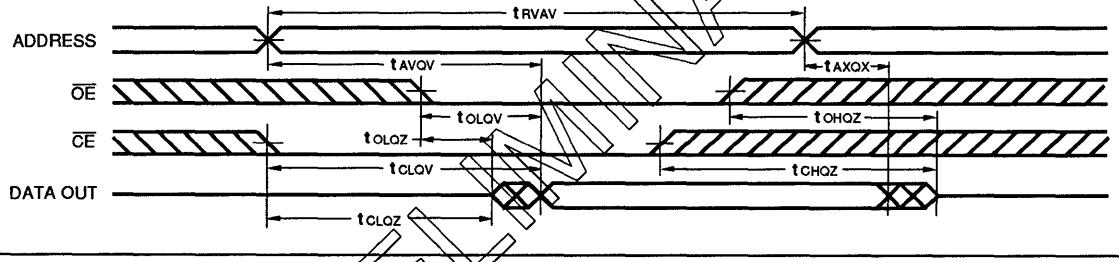
			LMM824-				
Symbol	Parameter	Test Condition	45	35	25		Unit
ICC1	VCC Current, Active	(Note 5, 6)	205	230	270		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

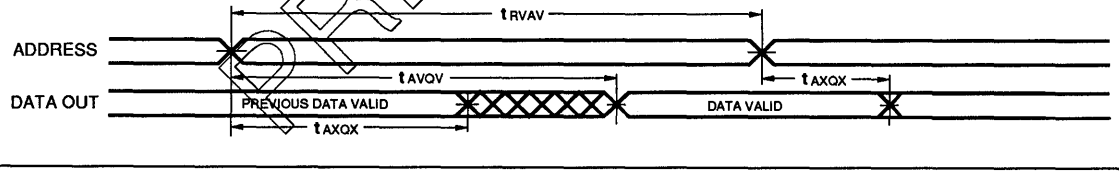
Read Cycle (Notes 11, 12, 22, 23, 24)

Symbol	Parameter	LMM824-45 Min	LMM824-45 Max	LMM824-35 Min	LMM824-35 Max	LMM824-25 Min	LMM824-25 Max		
tRVAV	Read Cycle Time	45		35		25			
tAVQV	Address Valid to Output Valid (13, 14)		45		35		25		
tAXQX	Address Change to Output Hold	5		3		3			
tCLQV	Chip Enable Low to Output Valid (13, 15)		45		35		25		
tCLQZ	Chip Enable Low to Output in Low Z (20, 21)	5		5		5			
tOHQZ	Output Disable to Output in High Z (20, 21)		20		20		20		
tCHQZ	Chip Enable to Output in High Z (20, 21)		20		20		20		
tOLQZ	Output Enable to Output in Low Z (20, 21)	5		5		5			
tOLQV	Output Enable to Output Valid		25		25		25		
tPU	Chip Enable Low to Power Up (10, 19)	0		0		0			
tPD	Power Up to Power Down (10, 19)		45		35		25		

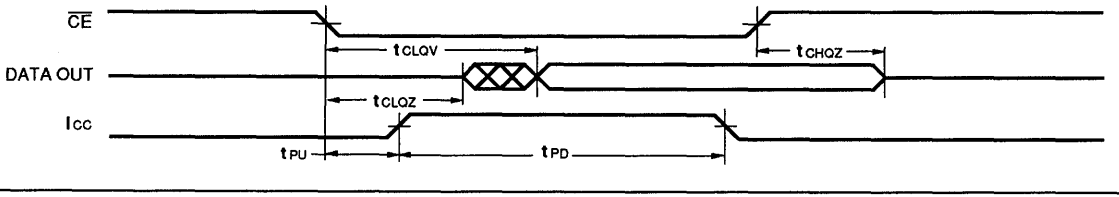
Read Cycle — Address Controlled No. 1 (Notes 13, 14)



Read Cycle — Address Controlled No. 2 (Notes 13, 15)



Read Cycle — CE Controlled (Notes 13, 15)



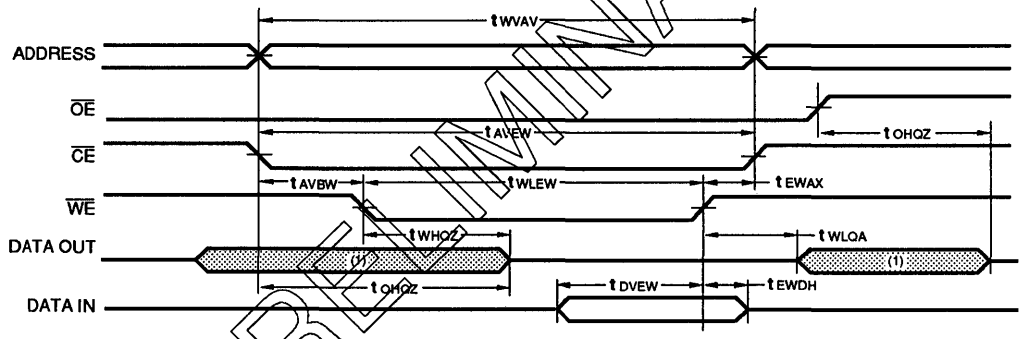
4

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

Write Cycle (Notes 11, 12, 22, 23, 24)

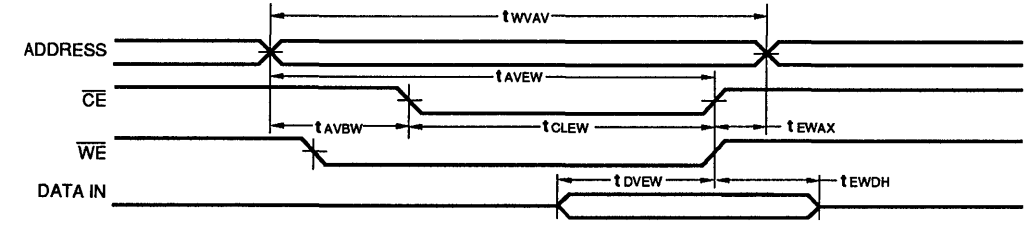
Symbol	Parameter	LMM824- 45 Min	45 Max	35 Min	35 Max	25 Min	25 Max	Min	Max
tWVAV	Write Cycle Time	45		35		25			
tCLEW	Chip Enable Low to End of Write Cycle	40		30		20			
tAVBW	Address Valid to Beginning of Write Cycle	5		5		5			
tAVEW	Address Valid to End of Write Cycle	40		30		20			
tEWAX	End of Write Cycle to Address Change	5		5		5			
tWLEW	Write Enable Low to End of Write Cycle	35		25		15			
tDVEW	Data to End of Write Cycle	20		15		15			
tEWDH	End of Write Cycle to Data Hold	5		3		3			
tWHQZ	Write Enable High to Output in High Z (20, 21)		15		15		15		
tWLQA	Write Enable Low to Output Active (20, 21)	5		5		5			
tOHQZ	Output Disable to Output in High Z		20		20		20		

Write Cycle — WE Controlled (Notes 16, 17, 18, 19)



(1) During this period, I/O pins are in the output state, and input signals must not be applied.

Write Cycle — CE Controlled (Notes 16, 17, 18, 19)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE} \le V_{IL}$, $\overline{WE} \le V_{IL}$.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE} \ge V_{IH}$.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = VCC. Input levels are within 0.5 V of VCC or ground.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{CE}$ must be ≥ VCC – 0.3 V. For all other inputs VIN ≥ VCC – 0.3 V or VIN ≤ 0.3 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE}$ low).

15. All address lines are valid prior-to or coincident-with the $\overline{CE}$ transition to low.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referenced to the signal that falls last or rises first.

17. If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high impedance state.

18. If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{CE}$.

b. Falling edge of $\overline{WE}$ ($\overline{CE}$ active).

c. Transition on any address line ($\overline{CE}$ active).

d. Transition on any data line ($\overline{CE}$ and $\overline{WE}$ active).

The device automatically powers down from ICC2 to ICC1 after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be

FIGURE 1a.

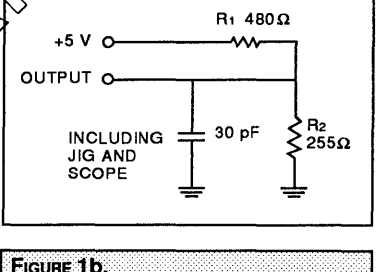


FIGURE 1b.

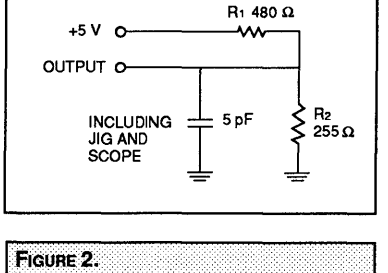
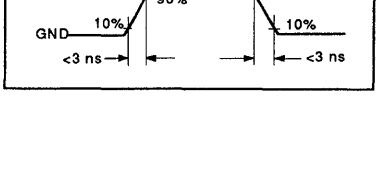
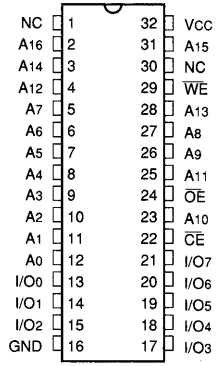


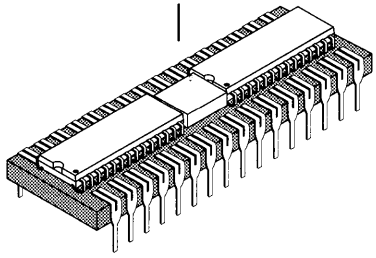
FIGURE 2.



ORDERING INFORMATION

32-pin





Speed	Plastic DIP Module (P15)
	0°C to +70°C — COMMERCIAL SCREENING
45 ns	LMM824P-45
35 ns	" 35
25 ns	" 25

PRELIMINARY

4 Megabit (256K x 16-bit) Static RAM Module LMM4016

FEATURES

- 4 Megabit (256K × 16-bit) Static RAM Module
- Utilizes 16 L7C197 256K × 1 Static RAMs
- Advanced CMOS Technology
- High Speed, Low Power Consumption
- TTL Compatible Inputs and Outputs
- Plug Compatible with IDT7M4016
- Package Styles Available:
  - 48-pin DIP Module

DESCRIPTION

The **LMM4016** is a 4 megabit high performance static RAM module organized as 256K × 16 bits. The module is constructed using 16 L7C197, 256K × 1 static RAMs in plastic surface mount packages assembled on an epoxy laminate DIP substrate. Four separate Chip Enable ($\overline{CE}$) pins are available (one for each group of 4 RAMs). This allows the user to configure the memory as either 1M × 4, 512K × 8, or 256K × 16 organization.

Memory locations are specified on Address pins A0 through A17. Writing to the memory module is accomplished when the Chip Enable ($\overline{CE}$xx) and the Write Enable ($\overline{WE}$U,L) inputs are both low. Reading from a designated location is accomplished by taking $\overline{CE}$xx low, while $\overline{WE}$U,L remains high. The data in the addressed memory location will appear on the Data pins. The Data Out is in the high impedance state when $\overline{CE}$xx is high, or $\overline{WE}$U,L is low.

Latchup and static discharge protection are provided on-chip. The LMM4016 can withstand an injection current of up to 200 mA on any pin without damage.

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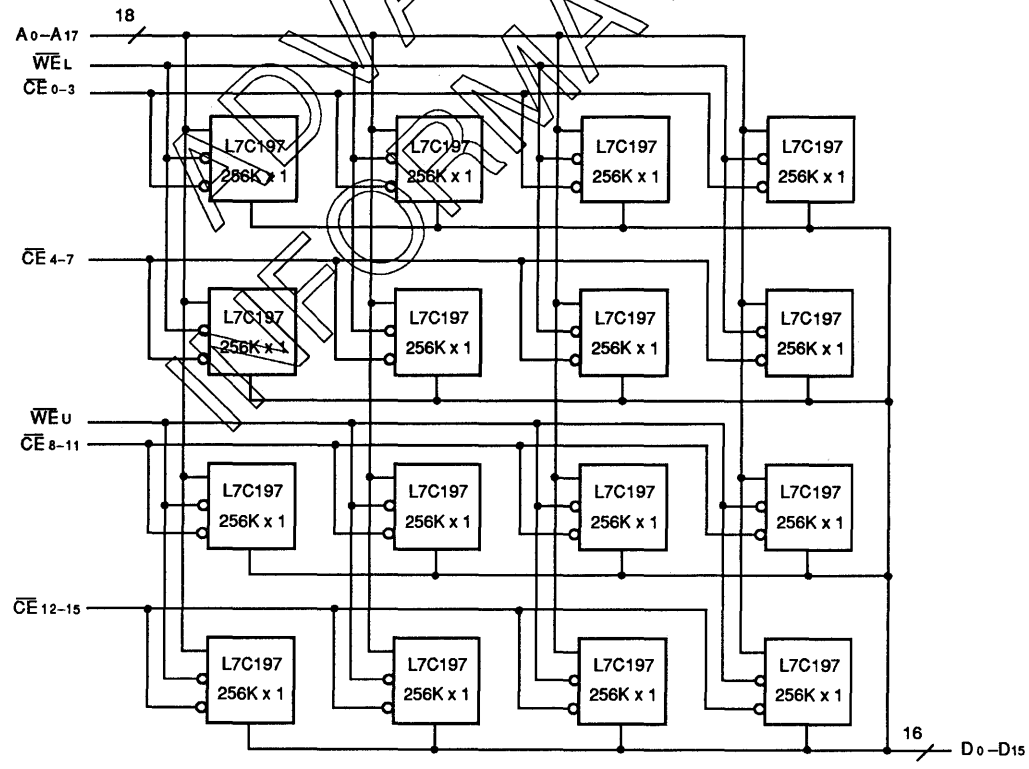
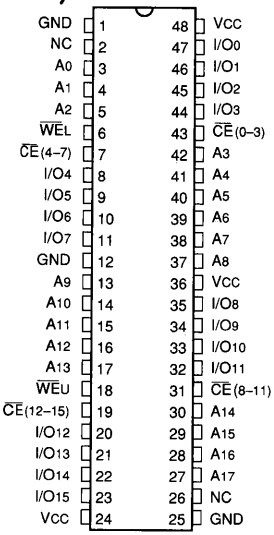
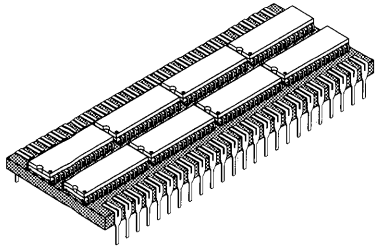
LMM4016 Block Diagram



ORDERING INFORMATION

48-pin Plastic DIP Module
(0.9" wide)





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Logic Products Package Availability Guide

Part No.[1]	No. Pins	Package Availability Code[2]						
		Plastic DIP	Sidebraze Hermetic DIP	CerDIP	Plastic LCC	Ceramic LCC	Pin Grid	Flat Pack
Multipliers								
LMU08	40/44	P3	D3		J1	K2		
LMU8U	40/44	P3	D3		J1	K2		
LMU557	40	P3	D3					
LMU558	40	P3	D3					
LMU12	64/68	P4	D6				G2	
LMU112	48/52	P5	D5		J5			
LMU16	64/68	P4	D6				G2	
LMU216	68				J2	K3		
LMU17	64/68	P4	D6				G2	
LMU217	68				J2	K3		
LMU18	84				J3		G3	
Multiplier-Accumulators								
LMA1009	64/68	P4	D6				G2	
LMA2009	68				J2	K3		
LMA1010	64/68	P4	D6				G2	
LMA2010	68				J2	K3		
Multiplier-Summer								
LMS12	84				J3		G3	
Pipeline Registers								
L29C520	24/28	P2	D2	C1	J4	K1		F1
L29C521	24/28	P2	D2	C1	J4	K1		F1
LPR520	40/44	P3	D3		J1	K2		
LPR521	40/44	P3	D3		J1	K2		
L29C524	28	P10	D10, D11		J4			
L29C525	28	P10	D10, D11		J4			
L10C11	24	P2	D2	C1				
L29C818	24/28	P2	D2	C1		K1		
Register Files								
LRF07	40/44	P3	D3			K2		
Arithmetic Logic Units								
L4C381	68				J2	K3	G1	
L29C101	64/68	P4	D6				G1	
Special Arithmetic Functions								
LSH32	68				J2	K3	G1	
LSH33	68				J2	K3	G1	
L10C23	24/28	P1, P2	D1, D2			K1		

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 10 – Packaging for package dimensions.

Product Selection Guide

Part No.[1]	Description	Maximum Speed (ns) Commercial	Maximum Speed (ns) Military	Power (mW)	Pins	Packages Available[2]
Multipliers						
LMU08 LMU8U	8 x 8 Signed 8 x 8 Unsigned	35	45	40	40/44	DIP, LCC, PLCC
LMU557 LMU558	8 x 8 Latched Output 8 x 8 Unregistered	60	70	85	40	DIP
LMU12	12 x 12	35	45	60	64/68	DIP, Pin Grid Array
LMU112	12 x 12 Reduced Pinout	50	60	50	48/52	DIP, LCC
LMU16	16 x 16	45	55	60	64/68	DIP, Pin Grid Array
LMU216	16 x 16 Surface Mount	45	55	60	68	LCC, PLCC
LMU17	16 x 16 Microprogrammable	45	55	60	64/68	DIP, Pin Grid Array
LMU217	16 x 16 Surface Mount	45	55	60	68	LCC, PLCC
LMU18	16 x 16/32 Outputs	35	45	150	84	Pin Grid Array, PLCC
Multiplier Accumulators						
LMA1009	12 x 12	45	55	60	64/68	DIP, Pin Grid Array
LMA2009	12 x 12 Surface Mount	45	55	60	68	LCC, PLCC
LMA1010	16 x 16	45	55	60	64/68	DIP, Pin Grid Array
LMA2010	16 x 16 Surface Mount	45	55	60	68	LCC, PLCC
Multiplier Summer						
LMS12	12 x 12 + 26 FIR	40	50	75	84	Pin Grid Array, PLCC
Pipeline Registers						
L29C520 L29C521	4 x 8-bit, Var. Delay, 1–4 Stages 4 x 8-bit, Var. Delay, 1–4 Stages	22	24	50	24/28	DIP, LCC, PLCC Flat Pack
LPR520 LPR521	4 x 16-bit, Var. Delay, 1–4 Stages 4 x 16-bit, Var. Delay, 1–4 Stages	22	24	50	40/44	DIP, LCC, PLCC
L29C524 L29C525	14 x 8-bit, Var. Delay, 0–14 Stages 16 x 8-bit, Var. Delay, 0–16 Stages	20	25	50	28 28	DIP, PLCC
L10C11	18 x 8-bit, Var. Delay, 3–18 Stages	25	30	50	24	DIP
L29C818	8-bit Serial Scan Shadow Register	25	30	50	24/28	DIP, LCC
Register Files						
LRF07	8 x 8, 3 Independent Port	35	35	40	40	DIP, LCC
Arithmetic Logic Units						
L4C381	16-bit, Add/Sub	26	30	60	68	Pin Grid Array, LCC, PLCC
L29C101	16-bit Slice, Quad 2901	35	45	75	64/68	DIP, Pin Grid Array
Special Functions						
LSH32	32-bit Barrel Shifter	32	40	60	68	Pin Grid Array, LCC, PLCC
LSH33	32-bit Barrel Shifter with Registers	30	40	60	68	Pin Grid Array, LCC, PLCC
L10C23	64 x 1 Digital Correlator	20	20	125	24/28	DIP, LCC

(1) See Section 1 – Ordering Information for assistance in constructing a valid part number.
(2) See Section 10 – Packaging for package dimensions.

Product Cross Reference Guide

LOGIC DEVICES		TRW	Analog Dev	IDT	Cypress	AMD	Weitek
LMU08	8 X 8 MULT	MPY008	ADSP1080				
LMU8U	8 X 8 MULT	MPY08U	ADSP1081				
LMU557	8 X 8 MULT					AM25S557 SN54557 SN74557	
LMU558	8 X 8 MULT					AM25S558 SN54558 SN74558	
LMU12	12 X 12 MULT	MPY012	ADSP1012	IDT7212			
LMU112	12 X 12 MULT	MPY112					
LMU16/ LMU216	16 X 16 MULT	MPY016 TMC216	ADSP1016	IDT7216	CY7C516	AM29516 AM29C516	WTL1016 WTL1516/2517
LMU17/ LMU217	16 X 16 MULT		ADSP1017	IDT7217	CY7C517	AM29517 AM29C517	
LMA1009/ LMA2009	12 X 12 MAC	TDC1009 TMC2009 TMC2109	ADSP1009	IDT7209		AM29C509	
LMA1010/ LMA2010	16 X 16 MAC	TDC1010 TMC2010 TMC2110 TMC2210	ADSP1010 ADSP1110	IDT7210 IDT7243	CY7C510	AM29510 AM29C510	WTL1010 WTL2010

LOGIC DEVICES		AMD	Performance	Wafer Scale	Intersil	IDT
L29C520	PIPELINE REGISTER	AM29520A 29C520CNS	P29PCT520	WS59520	ISP9520	IDT29FCT520A
L29C521	PIPELINE REGISTER	AM29521A	P29PCT521	WS59521	ISP9521	IDT29FCT521A

LOGIC DEVICES		TRW	IDT	Cypress	AMD
L29C101	16-BIT ALU		IDT49C401	CY7C9101	AM29C101
L10C23	CORRELATOR	TDC1023J			

8 x 8-bit Parallel Multiplier — LMU08/LMU8U

FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- LMU08 Replaces TRW MPY008H
- LMU8U Replaces TRW MPY08HU
- Two's Complement (LMU08), or Unsigned Operands (LMU8U)
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead (LMU08 only)
  - 44-pin Ceramic LCC (Type C)

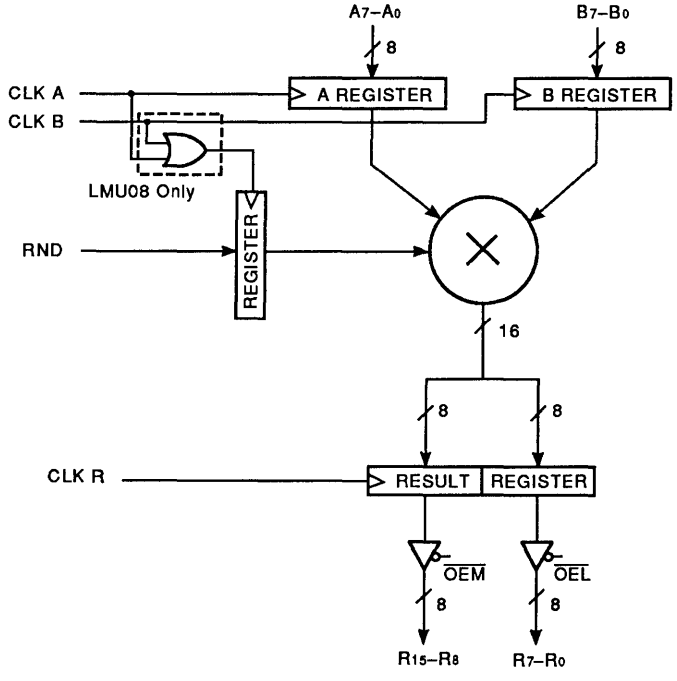
DESCRIPTION

The **LMU08** and **LMU8U** are 8-bit parallel multipliers which feature high speed with low power consumption. They are pin-for-pin equivalents with TRW MPY08H and MPY008HU type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU08 and the LMU8U produce the 16-bit product of two 8-bit numbers. The LMU08 accepts operands in two's complement format, and produces a two's complement result. The product is provided in two halves with the sign bit replicated as the most significant bit of both halves. This facilitates use of the LMU08 product as a double precision operand in 8-bit systems. The LMU8U operates on unsigned data, producing an unsigned magnitude result.

Both the LMU08 and the LMU8U feature independently controlled registers for both inputs and the product, which along with three-state outputs allows easy interfacing with microprocessor busses. Provision is made in the LMU08 and LMU8U for proper rounding of the product to 8-bit precision. The round input is loaded at the rising edge of the logical OR of CLK A and CLK B for the LMU08. The LMU8U latches RND on the rising edge of CLK A only. In either case, a '1' is added in the most significant position of the lower product byte when RND is asserted. Subsequent truncation of the least significant product byte results in a correctly rounded 8-bit result.

LMU08/LMU8U Block Diagram



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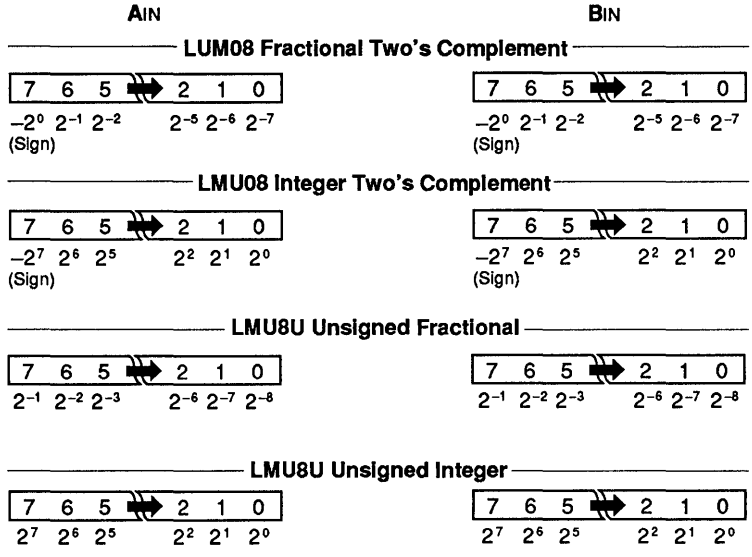
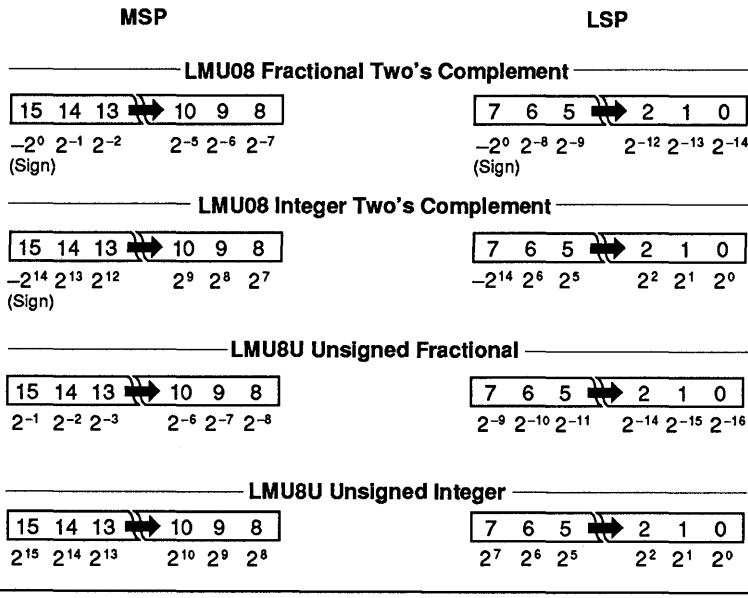
Input Formats



Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		8	24	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

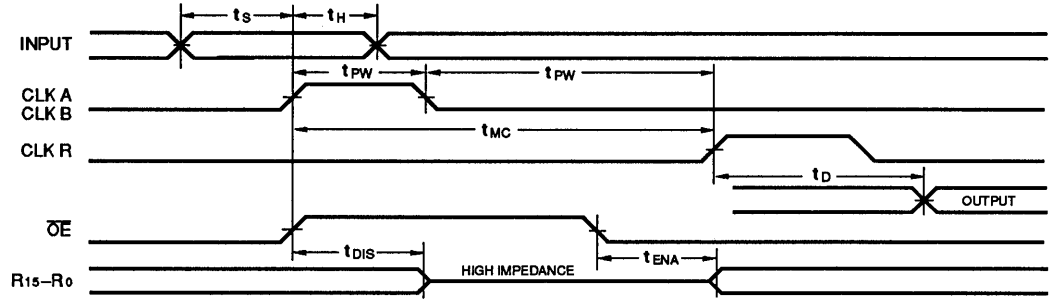
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU08/LMU8U-					
		70		50		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		70		50		35
t_D	Output Delay		25		20		18
t_{ENA}	Output Enable Time (Note 11)		20		18		18
t_{DIS}	Output Disable Time (Note 11)		18		17		17
t_{PW}	Clock Pulse Width	20		20		10	
t_H	Input Register Hold Time	4		0		0	
t_S	Input Register Setup Time	14		14		14	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU08/LMU8U-					
		90		60		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		90		60		45
t_D	Output Delay		35		20		20
t_{ENA}	Output Enable Time (Note 11)		35		20		20
t_{DIS}	Output Disable Time (Note 11)		35		18		18
t_{PW}	Clock Pulse Width	25		20		15	
t_H	Input Register Hold Time	5		0		0	
t_S	Input Register Setup Time	20		15		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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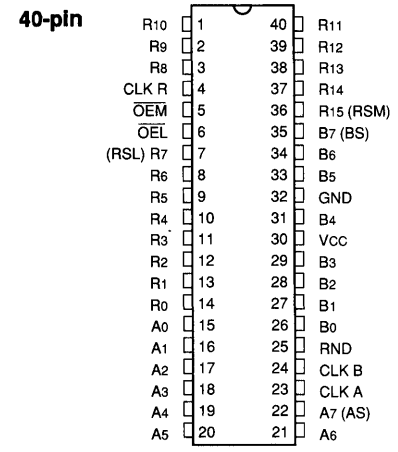
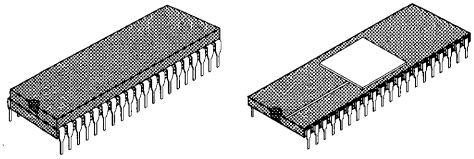
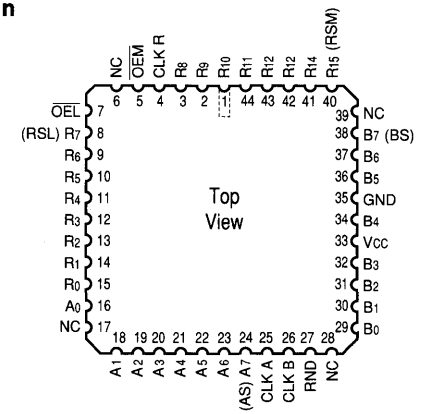
LMU08 — ORDERING INFORMATION

40-pin





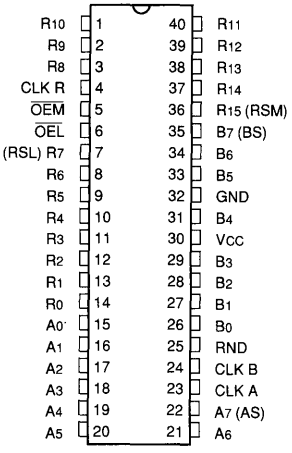
44-pin

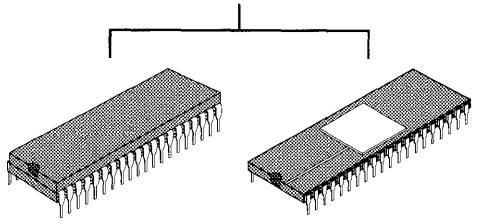


Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
70 ns	LMU08PC70	LMU08DC70	LMU08JC70	LMU08KC70
50 ns	" " 50	" " 50	" " 50	" " 50
35 ns	" " 35	" " 35	" " 35	" " 35
	–55°C to +125°C — Commercial Screening			
90 ns		LMU08DM90		LMU08KM90
60 ns		" " 60		" " 60
45 ns		" " 45		" " 45
	–55°C to +125°C — Extended Screening			
90 ns		LMU08DME90		LMU08KME90
60 ns		" " 60		" " 60
45 ns		" " 45		" " 45
	–55°C to +125°C — MIL-STD-883 Compliant			
90 ns		LMU08DMB90		LMU08KMB90
60 ns		" " 60		" " 60
45 ns		" " 45		" " 45

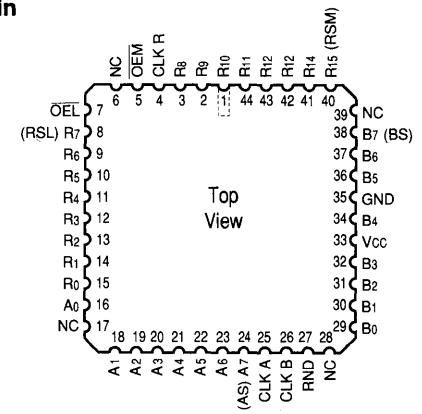
LMU8U — ORDERING INFORMATION

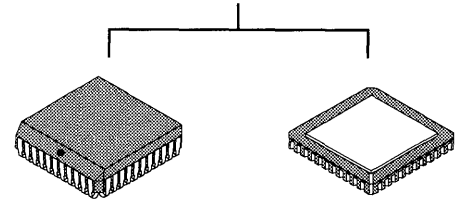
40-pin





44-pin





Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
70 ns	LMU8UPC70	LMU8UDC70	LMU8UJC70	LMU8UKC70
50 ns	" " 50	" " 50	" " 50	" " 50
35 ns	" " 35	" " 35	" " 35	" " 35
	–55°C to +125°C — Commercial Screening			
90 ns		LMU8UDM90		LMU8UKM90
60 ns		" " 60		" " 60
45 ns		" " 45		" " 45
	–55°C to +125°C — Extended Screening			
90 ns		LMU8UDME90		LMU8UKME90
60 ns		" " 60		" " 60
45 ns		" " 45		" " 45
	–55°C to +125°C — MIL-STD-883 Compliant			
90 ns		LMU8UDMB90		LMU8UKMB90
60 ns		" " 60		" " 60
45 ns		" " 45		" " 45

5

8 x 8-bit Parallel Multiplier — LMU557/558

FEATURES

- 60 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces Am25S557/558, 54S557/558
- Fully Combinatorial, No Clocks Required
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP

DESCRIPTION

The **LMU557** and **LMU558** are 8-bit parallel multipliers with high speed and low power operation. They are pin for pin equivalents with 54S557 and 54S558 type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

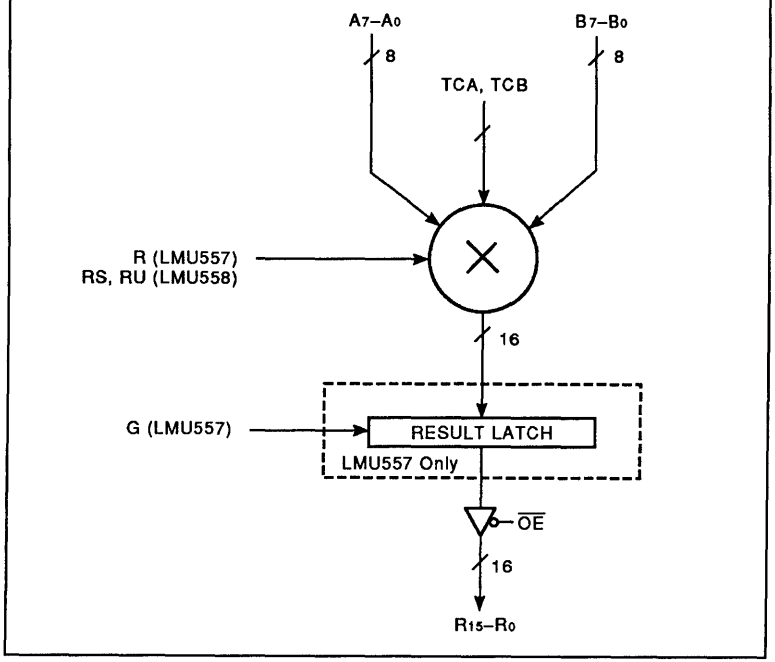
Both the LMU557 and LMU558 produce the 16-bit product of two 8-bit signed or unsigned numbers in a single unclocked operation. Assertion of control inputs TCA and TCB indicate that the corresponding input value is in two's complement notation.

Provision is made for proper rounding for any combination of signed or unsigned inputs. The RU input to the LMU557 causes the product to be rounded to 8 bits of precision for unsigned or mixed mode multiplication. For multiplication of two signed operands, the RS input is used for rounding, and the most significant bit of the product is discarded. [It will be identical to the sign bit for all except the $(-2^8)\bullet(-2^8)$ case, which will cause overflow if the result MSB is not considered.]

The LMU558 internally produces the RU and RS controls from a single round input, denoted R. With R asserted, RS rounding occurs if either TCA or TCB is asserted, while RU rounding is implemented for TCA and TCB not asserted. This implementation frees a pin for control of the transparent output latch in the LMU557 via the G input.

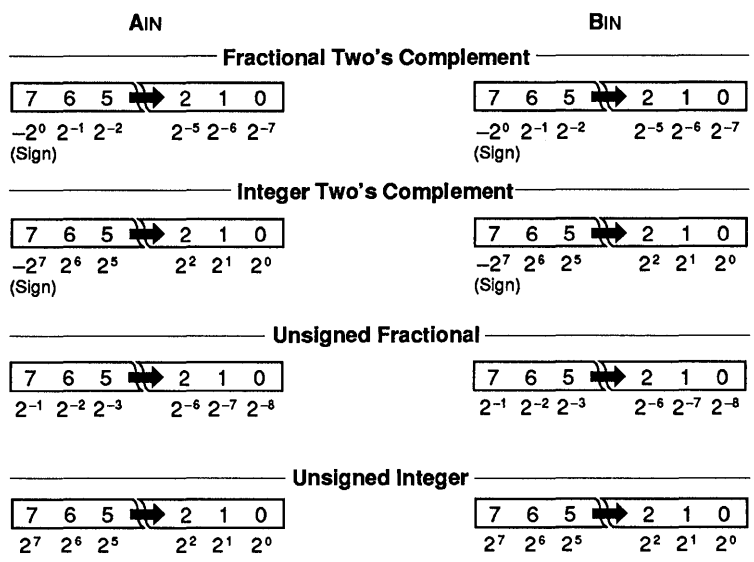
Both the LMU557 and LMU558 offer three-state output buffers controlled by the $\overline{OE}$ input. The LMU557 has a 16-bit transparent latch between the multiplier array and the output drivers for flexibility in implementing pipelined systems. This latch is transparent when G is high, and holds its state when G is low. In addition, both polarities of the result MSB (R15) are available as separate output pins to allow simple expansion to longer word lengths in signed multiplication.

LMU557/558 Block Diagram

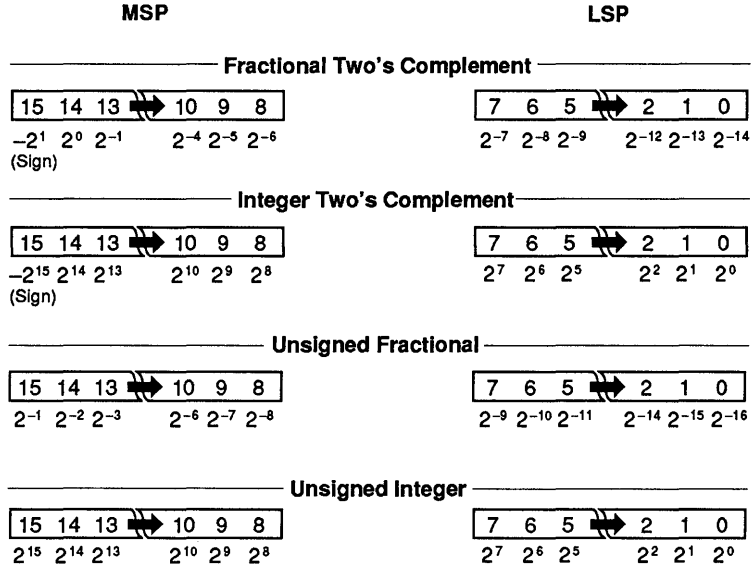


5

Input Formats



Output Formats



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		17	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

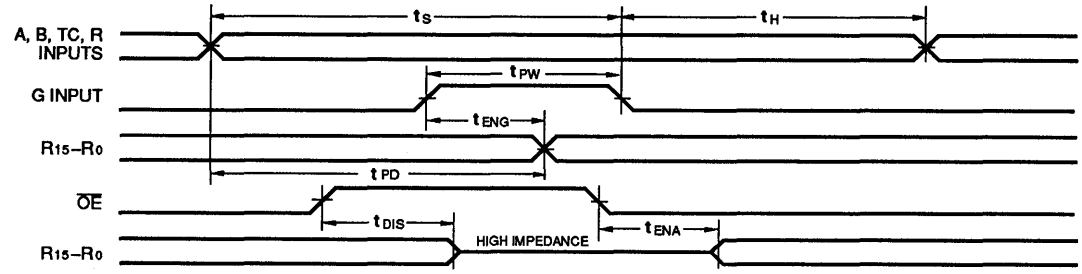
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU557/558-60 Min	LMU557/558-60 Max
t_{PD}	A, B, TC, R Inputs to R_{15}–R_8, $\overline{R_{15}}$		60
t_{PD}	A, B, TC, R Inputs to R_7–R_0		55
t_{ENG}	G Enable to Result		30
t_{ENA}	Output Enable Time (Note 11)		25
t_{DIS}	Output Disable Time (Note 11)		20
t_{PW}	G Pulse Width	15	
t_H	G to A, B, TC, R Hold Time	0	
t_S	A, B, TC, R Inputs to G Setup Time	45	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU557/558-70 Min	LMU557/558-70 Max
t_{PD}	A, B, TC, R Inputs to R_{15}–R_8, $\overline{R_{15}}$		70
t_{PD}	A, B, TC, R Inputs to R_7–R_0		60
t_{ENG}	G Enable to Result		35
t_{ENA}	Output Enable Time (Note 11)		30
t_{DIS}	Output Disable Time (Note 11)		25
t_{PW}	G Pulse Width	20	
t_H	G to A, B, TC, R Hold Time	0	
t_S	A, B, TC, R Inputs to G Setup Time	55	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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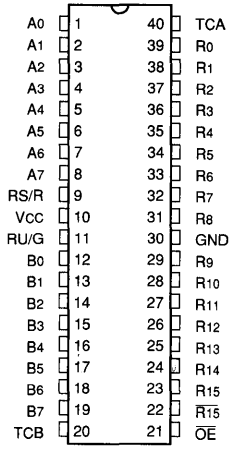
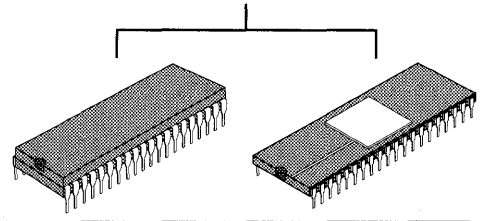
ORDERING INFORMATION

40-pin





Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	
	0°C to +70°C — Commercial Screening		
60 ns	LMU557PC60 or LMU558PC60	LMU557DC60 or LMU558DC60	
	–55°C to +125°C — Commercial Screening		
70 ns		LMU557DM70 or LMU558DM70	
	–55°C to +125°C — Extended Screening		
70 ns		LMU557DME70 or LMU558DME70	
	–55°C to +125°C — MIL-STD-883 Compliant		
70 ns		LMU557DMB70 or LMU558DMB70	

12 x 12-bit Parallel Multiplier — LMU12

FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY12HJ
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Pin Grid Array

DESCRIPTION

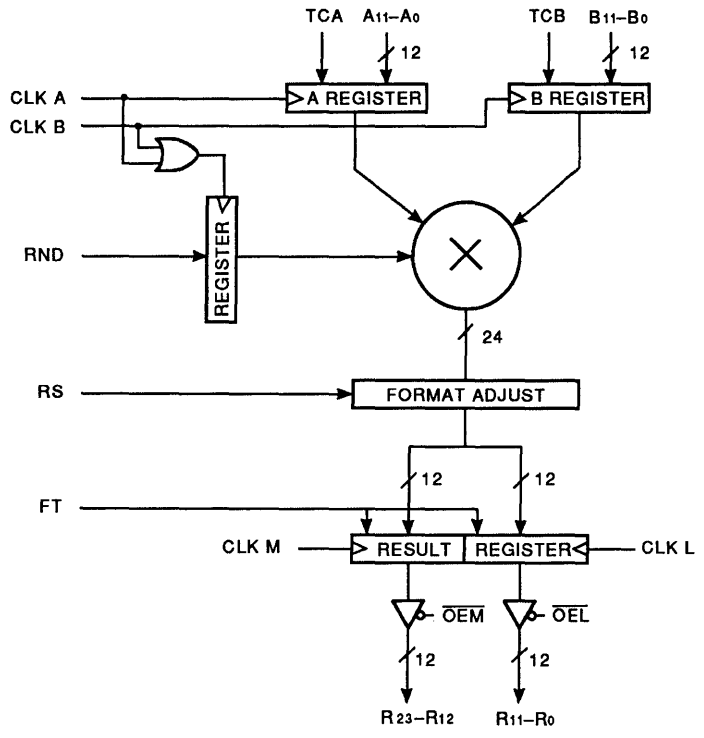
The LMU12 is a 12-bit parallel multiplier with high speed and low power consumption. It is pin and functionally compatible with TRW MPY12HJ devices. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU12 produces the 24-bit product of two 12-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded by CLK B. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. Rs high gives a full 32-bit product. Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

LMU12 Block Diagram



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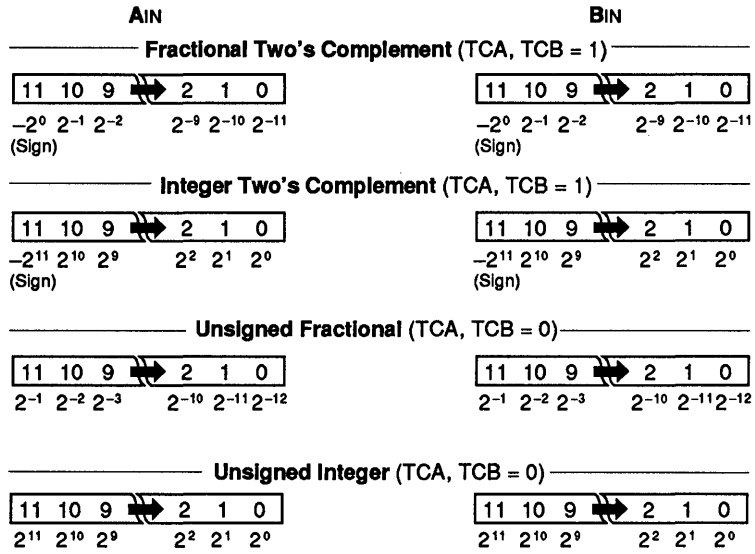
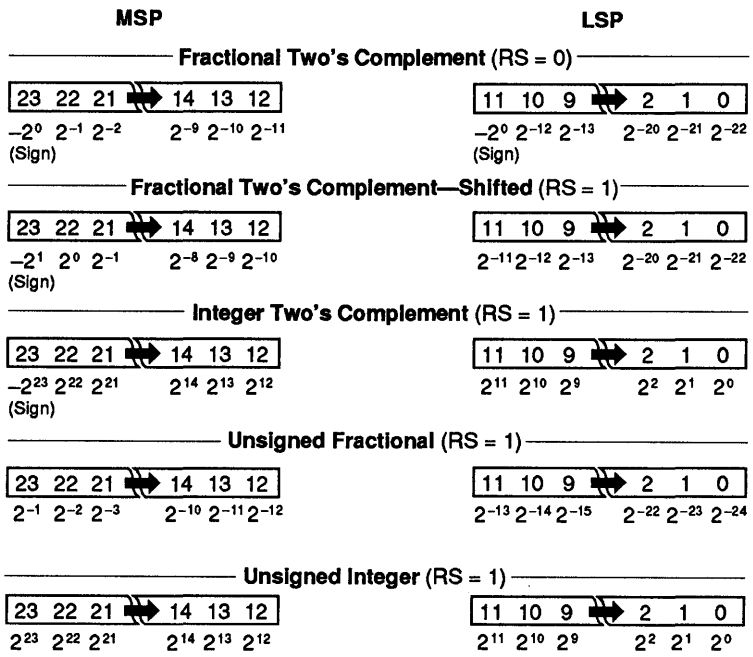
Input Formats



Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

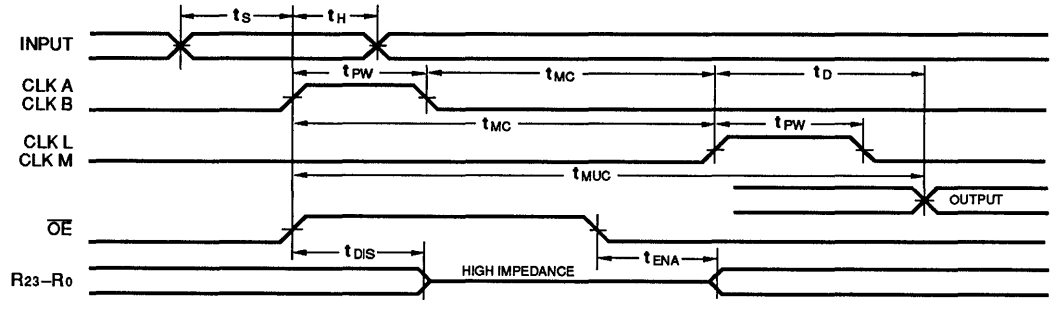
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU12-					
		65		45		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		45		35
t_{MUC}	Unclocked Multiply Time		95		65		55
t_D	Output Delay		26		25		25
t_{ENA}	Output Enable Time (Note 11)		22		22		20
t_{DIS}	Output Disable Time		20		20		18
t_{PW}	Clock Pulse Width	25		15		15	
t_H	Input Register Hold Time	2		2		2	
t_S	Input Register Setup Time	18		15		12	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU12-					
		75		55		45	
Symbol	Parameter					Min	Max
t_{MC}	Multiply Time (Clocked)		75		55		45
t_{MUC}	Unclocked Multiply Time		110		75		65
t_D	Output Delay		30		30		25
t_{ENA}	Output Enable Time (Note 11)		26		26		24
t_{DIS}	Output Disable Time		24		24		22
t_{PW}	Clock Pulse Width	25		20		15	
t_H	Input Register Hold Time	2		2		2	
t_S	Input Register Setup Time	18		15		12	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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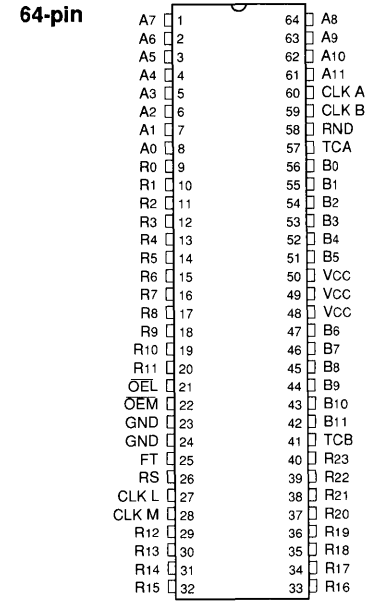
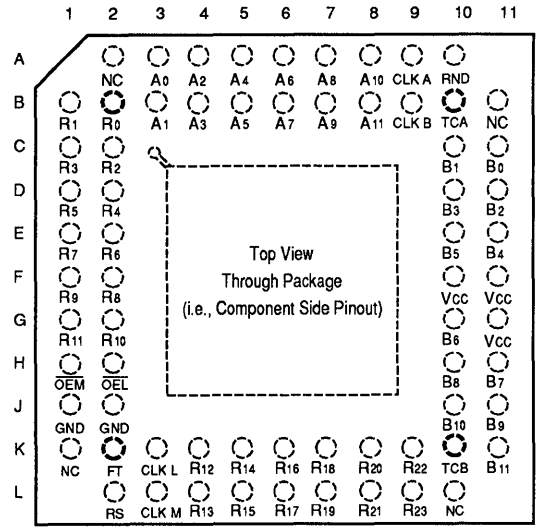
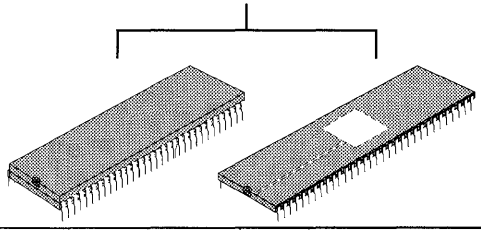
ORDERING INFORMATION

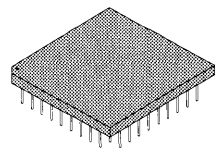
64-pin



68-pin







Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening		
65 ns	LMU12PC65	LMU12DC65	LMU12GC65
45 ns	" " 45	" " 45	" " 45
35 ns	" " 35	" " 35	" " 35
	–55°C to +125°C — Commercial Screening		
75 ns		LMU12DM75	LMU12GM75
55 ns		" " 55	" " 55
45 ns		" " 45	" " 45
	–55°C to +125°C — Extended Screening		
75 ns		LMU12DME75	LMU12GME75
55 ns		" " 55	" " 55
45 ns		" " 45	" " 45
	–55°C to +125°C — MIL-STD-883 Compliant		
75 ns		LMU12DMB75	LMU12GMB75
55 ns		" " 55	" " 55
45 ns		" " 45	" " 45

12 x 12-bit Parallel Multiplier — LMU112

FEATURES

- 50 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY112K
- Two's Complement or Unsigned Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 52-pin Plastic LCC, J-lead

DESCRIPTION

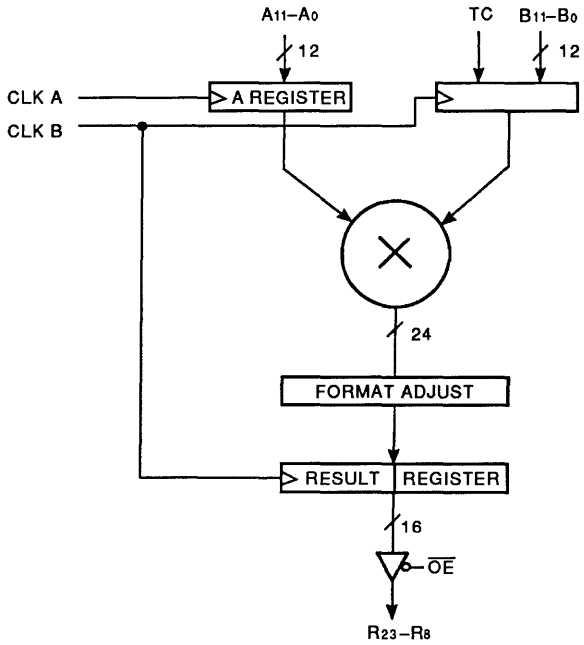
The **LMU112** is a high-speed, low power, 12-bit parallel multiplier built using advanced CMOS technology. The LMU112 is pin and functionally compatible with TRW's MPY112K.

The A and B input operands are loaded into their respective registers on the rising edge of the separate clock inputs (CLK A and CLK B). Two's complement or unsigned magnitude operands are accommodated via the operand control bit, TC, which is loaded along with the B operands. The operands are specified to be in two's complement format when TC is asserted and unsigned magnitude when TC is de-asserted. Mixed mode operation is not allowed.

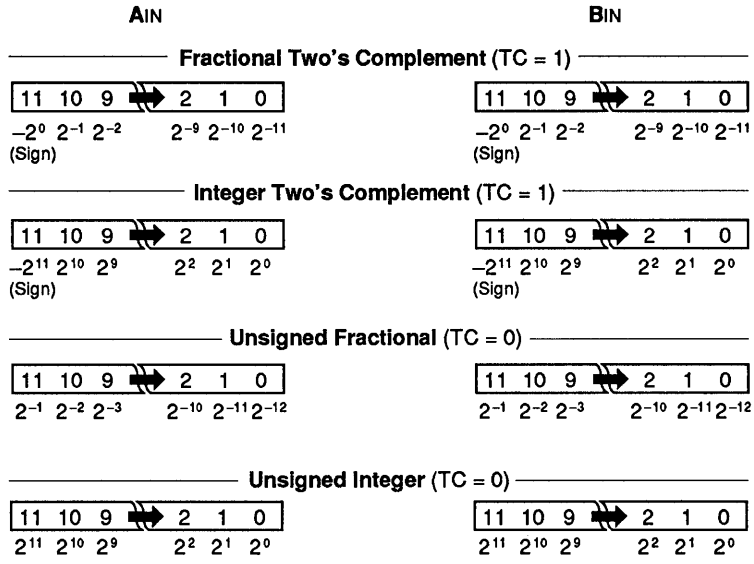
For two's complement operands, the 17 most significant bits at the output of the asynchronous multiplier array are shifted one bit position to the left. This is done to discard the redundant copy of the sign-bit, which is in the most significant bit position, and extend the bit precision by one bit. The result is then truncated to the 16 MSB's and loaded into the output register on the rising edge of CLK B.

The contents of the output register are made available via three-state buffers by asserting $\overline{OE}$. When $\overline{OE}$ is de-asserted, the outputs (R_{23}–R_8) are in the high impedance state.

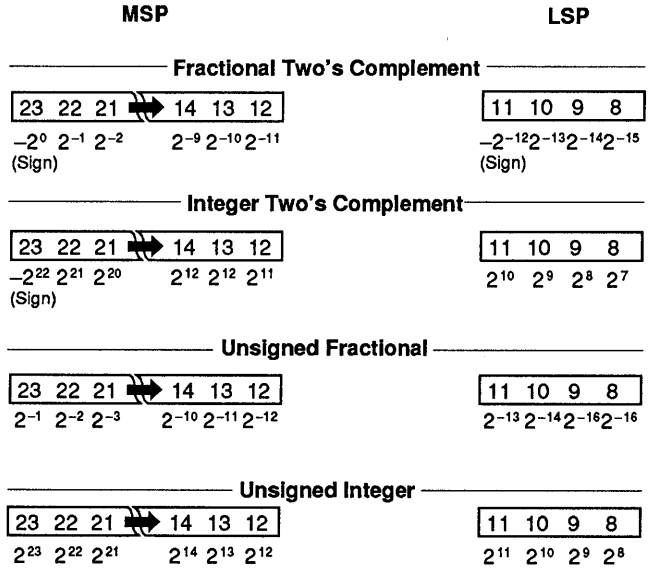
LMU112 Block Diagram



Input Formats



Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

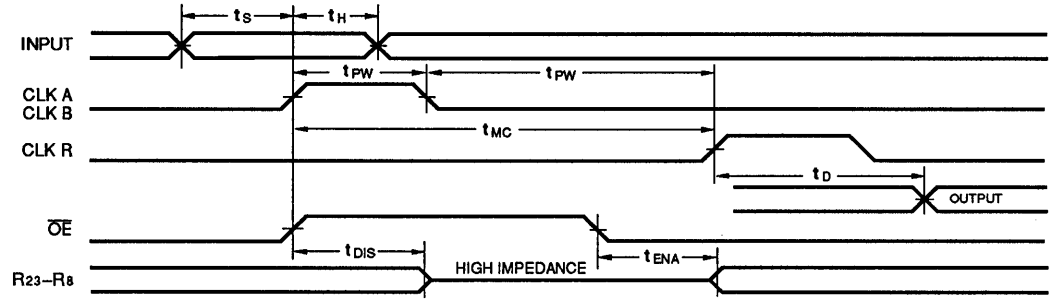
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU112- 60 Min	LMU112- 60 Max	LMU112- 50 Min	LMU112- 50 Max
t_{MC}	Multiply Time (Clocked)		60		50
t_D	Output Delay		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25
t_{PW}	Clock Pulse Width	15		15	
t_H	Input Register Hold Time	0		0	
t_S	Input Register Setup Time	15		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU112- 65 Min	LMU112- 65 Max	LMU112- 55 Min	LMU112- 55 Max
t_{MC}	Multiply Time (Clocked)		65		55
t_D	Output Delay		30		30
t_{ENA}	Output Enable Time (Note 11)		30		30
t_{DIS}	Output Disable Time (Note 11)		30		30
t_{PW}	Clock Pulse Width	20		20	
t_H	Input Register Hold Time	0		0	
t_S	Input Register Setup Time	15		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

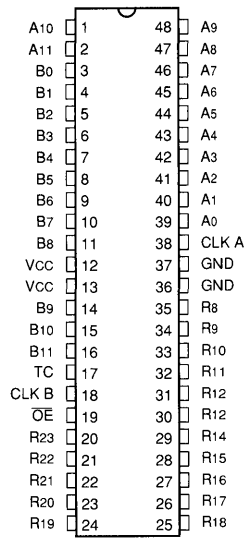
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

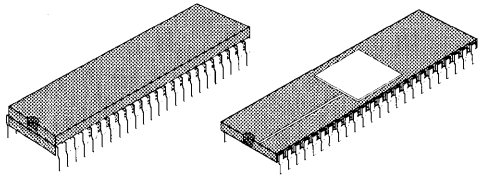
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

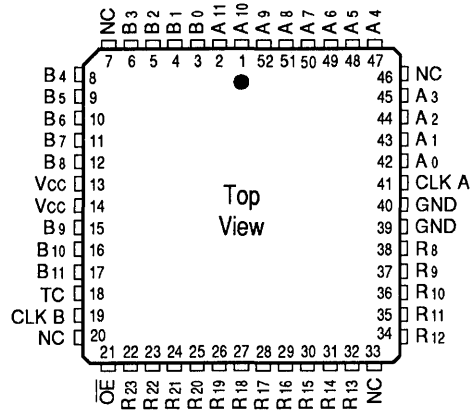
ORDERING INFORMATION

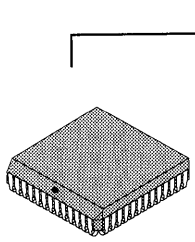
48-pin





52-pin





Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier(J5)	
	0°C to +70°C — COMMERCIAL SCREENING			
60 ns	LMU112PC60	LMU112DC60	LMU112JC60	
50 ns	" " 50	" " 50	" " 50	
	–55°C to +125°C — COMMERCIAL SCREENING			
65 ns		LMU112DM65		
55 ns		" " 55		
	–55°C to +125°C — EXTENDED SCREENING			
65 ns		LMU112DME65		
55 ns		" " 55		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
65 ns		LMU112DMB65		
55 ns		" " 55		

16 x 16-bit Parallel Multiplier — LMU16/216

FEATURES

- 45 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY016HJ and AMD Am29516
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The **LMU16** and **LMU216** are 16-bit parallel multipliers with high speed and low power consumption. They are pin and functionally compatible with TRW MPY016HJ and AMD Am29516 devices. The LMU16 and LMU216 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU16 and LMU216 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded by CLK B. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

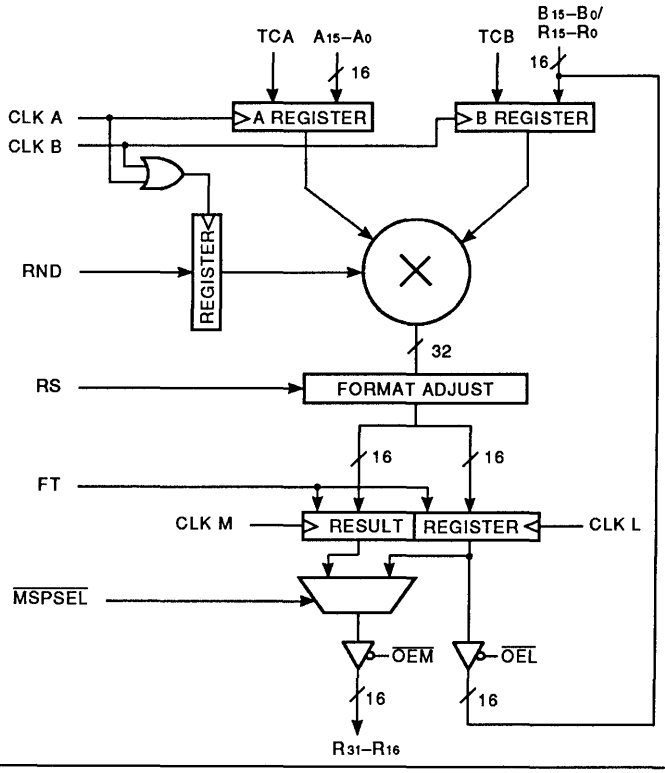
RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{\text{MSPSEL}}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{\text{MSPSEL}}$ high routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B input port through a separate three-state buffer.

The output multiplexer control $\overline{\text{MSPSEL}}$ uses a pin which is a supply ground in the TRW MPY16HJ. When this control is LOW (GND) the function is that of the MPY16HJ, thus allowing full compatibility.

LMU16/216 Block Diagram



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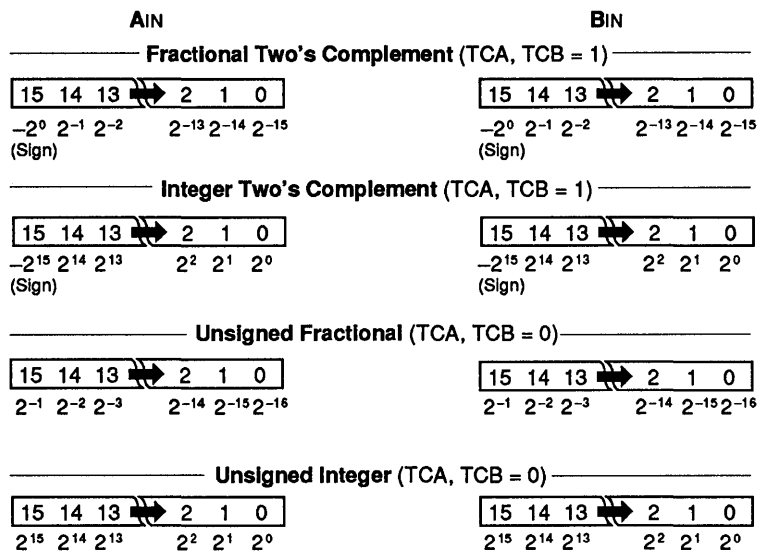
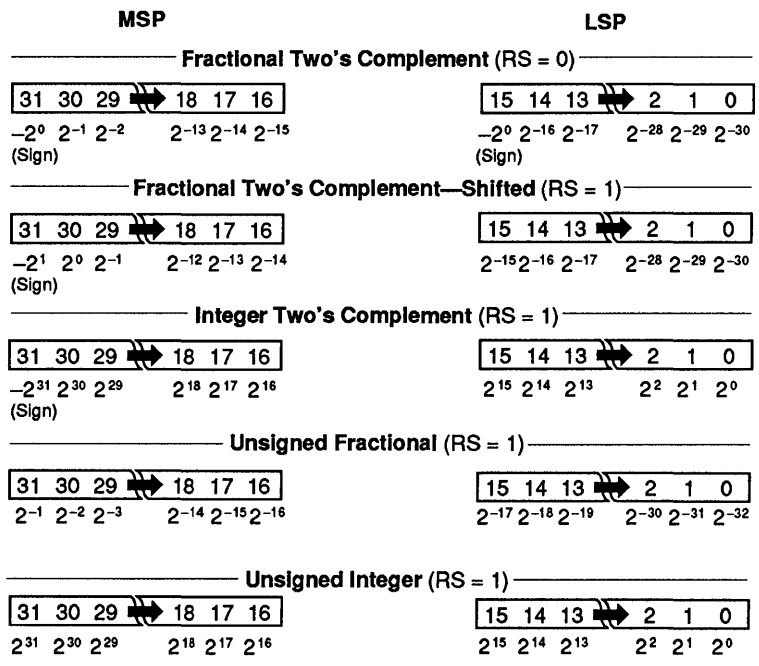
Input Formats



Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

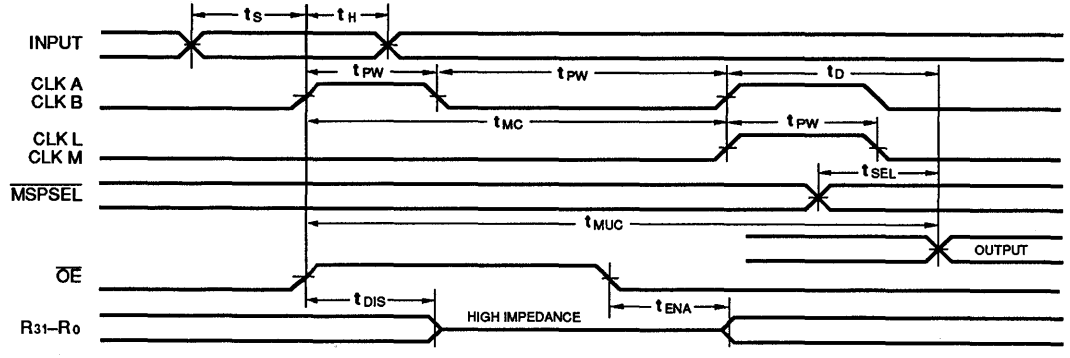
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU16/216-					
		65		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	1		1		1	
t_S	Input Register Setup Time	15		15		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU16/216-					
		75		65		55	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	2		2		2	
t_S	Input Register Setup Time	15		15		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

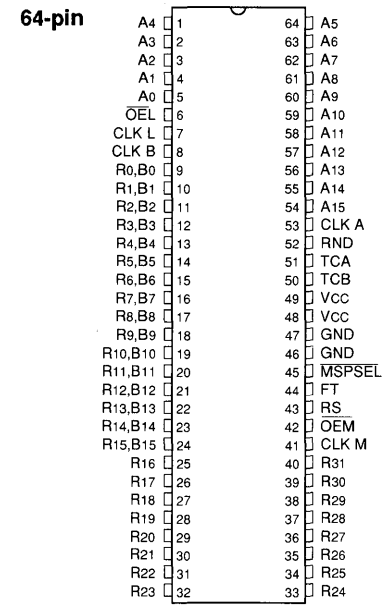
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

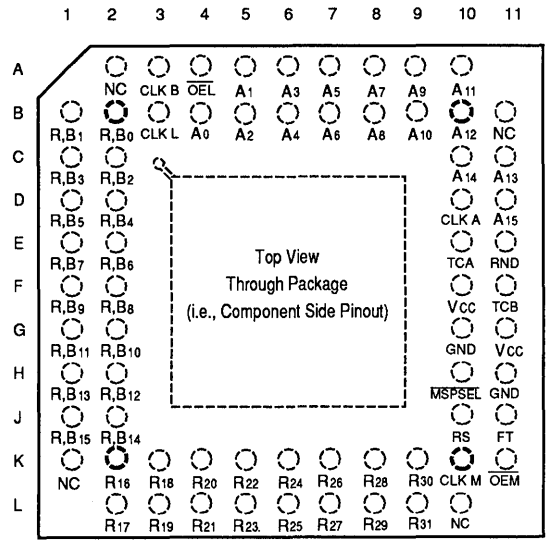
5

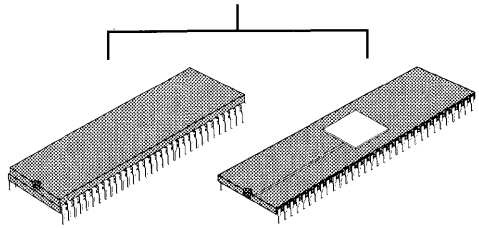
LMU16 — ORDERING INFORMATION

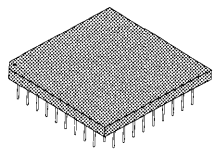
64-pin



68-pin



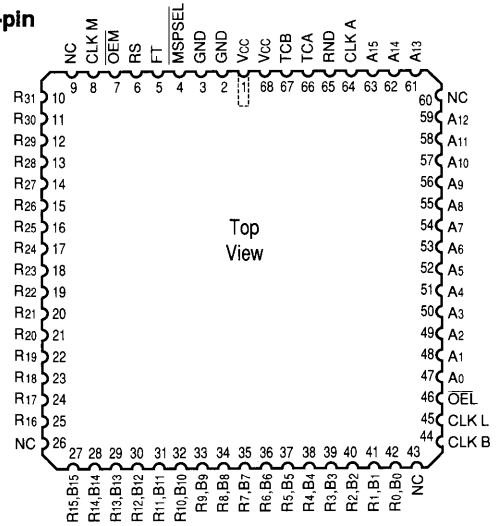


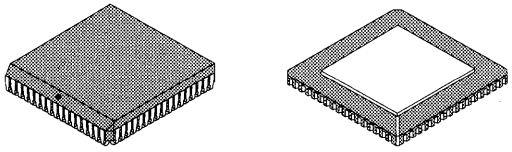


Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMU16PC65	LMU16DC65	LMU16GC65
55 ns	" " 55	" " 55	" " 55
45 ns	" " 45	" " 45	" " 45
	–55°C to +125°C — COMMERCIAL SCREENING		
75 ns		LMU16DM75	LMU16GM75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — EXTENDED SCREENING		
75 ns		LMU16DME75	LMU16GME75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns		LMU16DMB75	LMU16GMB75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55

LMU216 — ORDERING INFORMATION

68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — Commercial Screening			
65 ns 55 ns 45 ns	LMU216JC65 " " 55 " " 45	LMU216KC65 " " 55 " " 45		
	–55°C to +125°C — Commercial Screening			
75 ns 65 ns 55 ns		LMU216KM75 " " 65 " " 55		
	–55°C to +125°C — Extended Screening			
75 ns 65 ns 55 ns		LMU216KME75 " " 65 " " 55		
	–55°C to +125°C — MIL-STD-883 Compliant			
75 ns 65 ns 55 ns		LMU216KMB75 " " 65 " " 55		

5

16 x 16-bit Parallel Multiplier — LMU17/217

FEATURES

- 45 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces AMD Am29517
- Single Clock Architecture with Register Enables
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The **LMU17** and **LMU217** are 16-bit parallel multipliers with high speed and low power consumption. They are pin and functionally compatible with AMD Am29517 devices. The LMU17 and LMU217 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

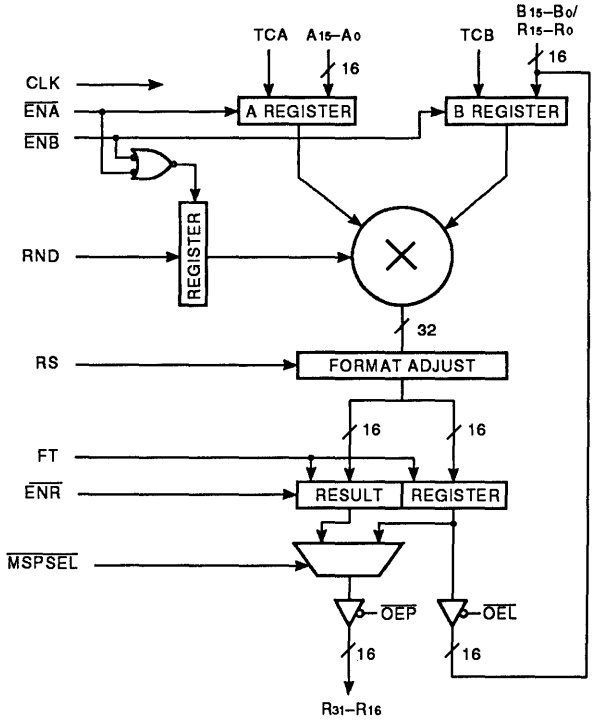
The LMU17 and LMU217 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When high, these prevent application of the clock to the respective register. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are low. RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is high, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

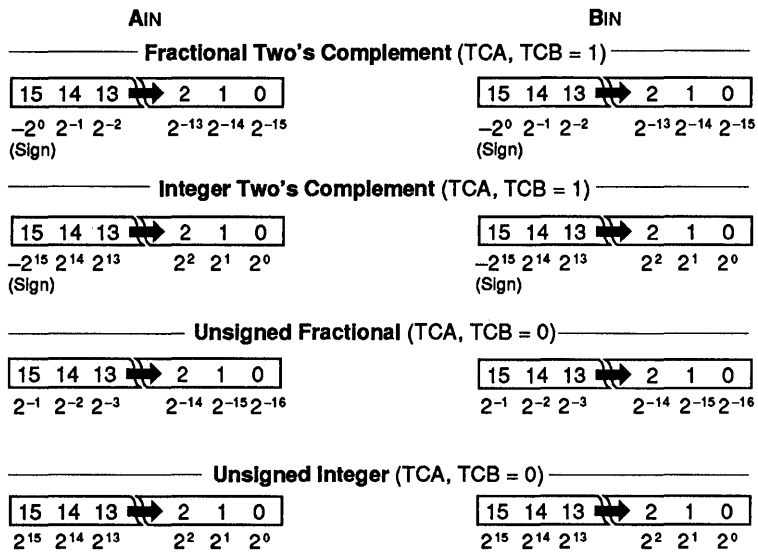
The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ high routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B input port through a separate three-state buffer.

LMU17/217 Block Diagram

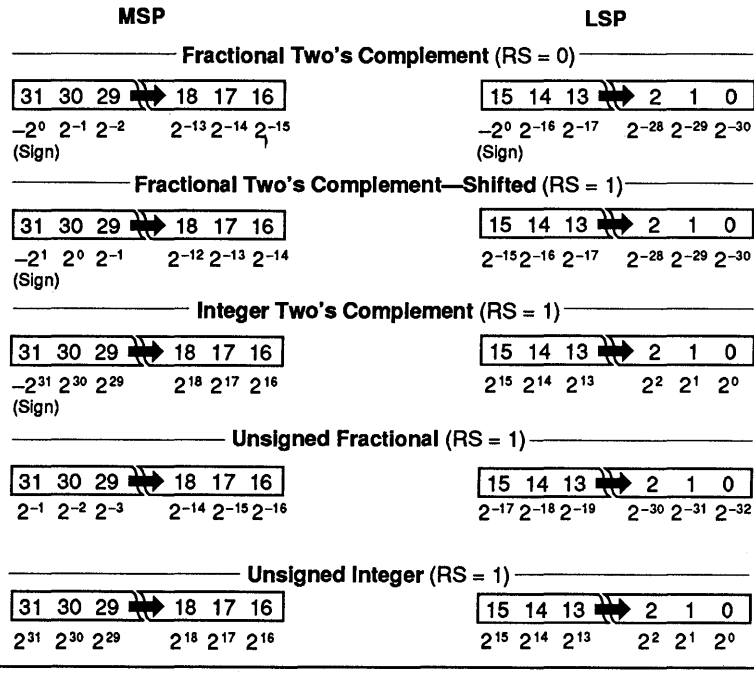


5

Input Formats



Output Formats



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

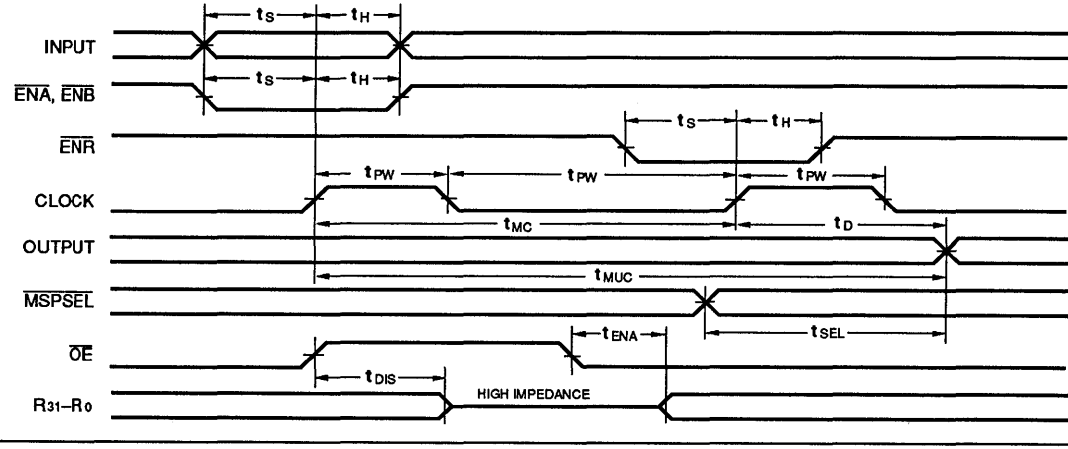
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU17/217-					
		65		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	3		3		3	
t_S	Input Register Setup Time	15		15		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU17/217-					
		75		65		55	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		25		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	3		3		3	
t_S	Input Register Setup Time	15		15		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

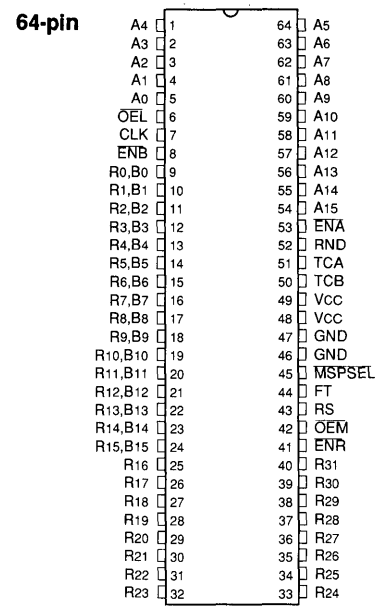
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

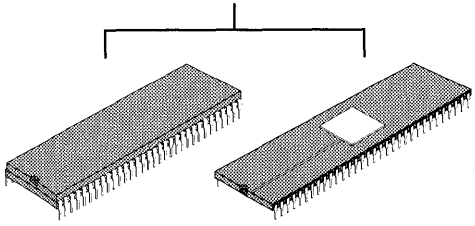
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

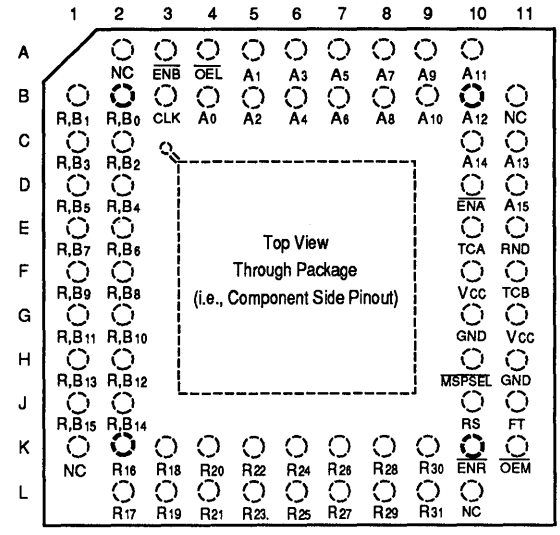
LMU17 — ORDERING INFORMATION

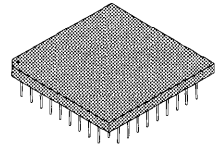
64-pin





68-pin

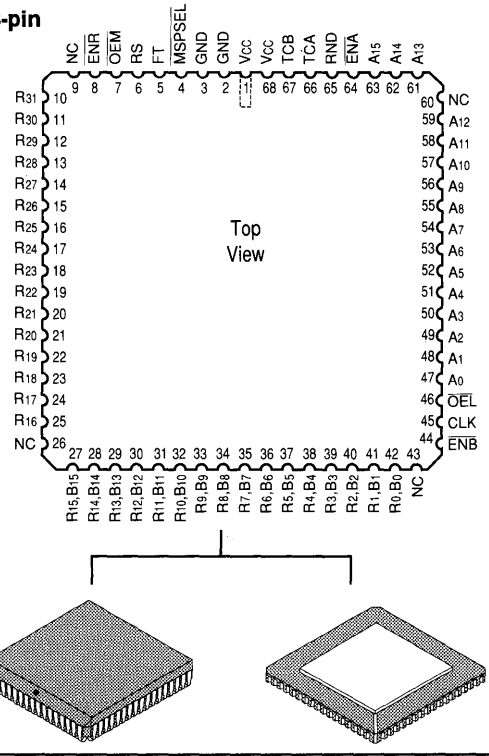




Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMU17PC65	LMU17DC65	LMU17GC65
55 ns	" " 55	" " 55	" " 55
45 ns	" " 45	" " 45	" " 45
	–55°C to +125°C — COMMERCIAL SCREENING		
75 ns		LMU17DM75	LMU17GM75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — EXTENDED SCREENING		
75 ns		LMU17DME75	LMU17GME75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns		LMU17DMB75	LMU17GMB75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55

LMU217 — ORDERING INFORMATION

68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — Commercial Screening			
65 ns	LMU217JC65	LMU217KC65		
55 ns	" " 55	" " 55		
45 ns	" " 45	" " 45		
	–55°C to +125°C — Commercial Screening			
75 ns		LMU217KM75		
65 ns		" " 65		
55 ns		" " 55		
	–55°C to +125°C — Extended Screening			
75 ns		LMU217KME75		
65 ns		" " 65		
55 ns		" " 55		
	–55°C to +125°C — MIL-STD-883 Compliant			
75 ns		LMU217KMB75		
65 ns		" " 65		
55 ns		" " 55		

5

16 x 16-bit Parallel Multiplier — LMU18

FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Full 32-bit Output Port — No Multiplexing Required
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Pin Grid Array

DESCRIPTION

The **LMU18** is a 16-bit parallel multiplier featuring high speed and low power consumption. The LMU18 is an 84-pin device which provides simultaneous access to all outputs. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

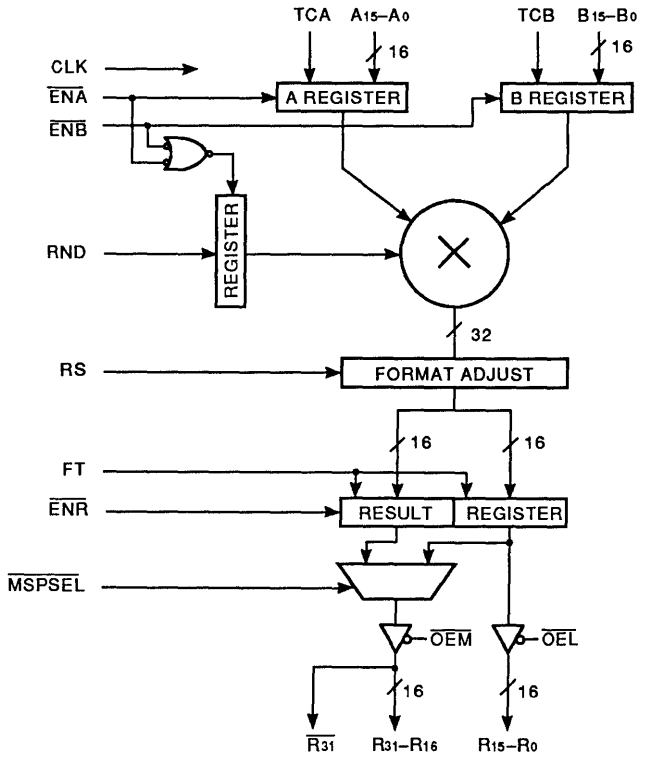
The LMU18 produces the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When high, these prevent application of the clock to the respective register. The mode controls TCA and TCB specify the operands as two's complement when high, or unsigned magnitude when low.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are low. RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the right shift control RS selects either of two output formats: RS low produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS high gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is high, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by taking the feed through control (FT) high.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ low causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ high routes the least significant half of the result to the MSP pins. The MSB of the result is available in both true and complemented form to aid implementation of higher precision multipliers.

LMU18 Block Diagram



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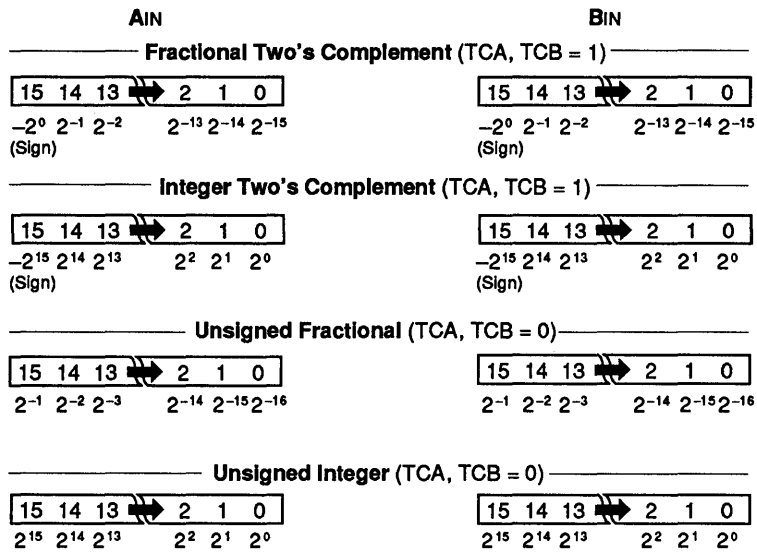
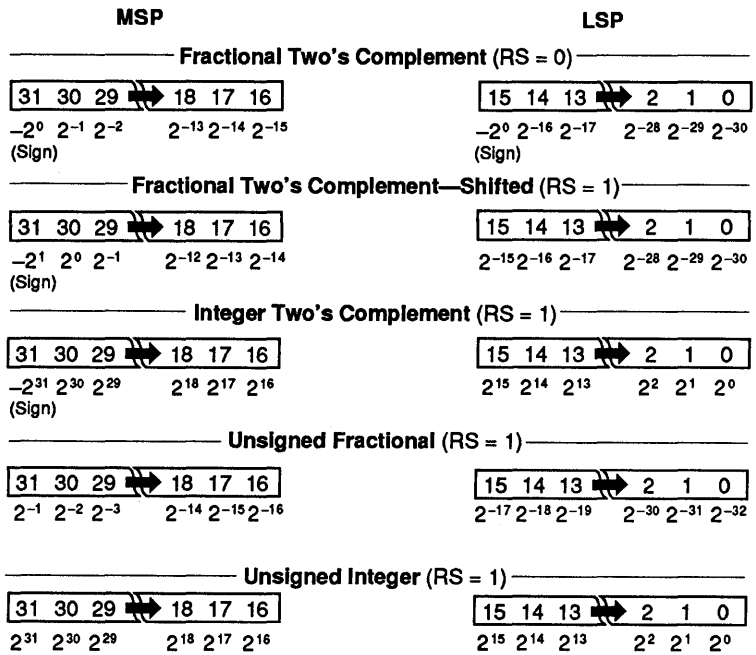
Input Formats



Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			−250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	45	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

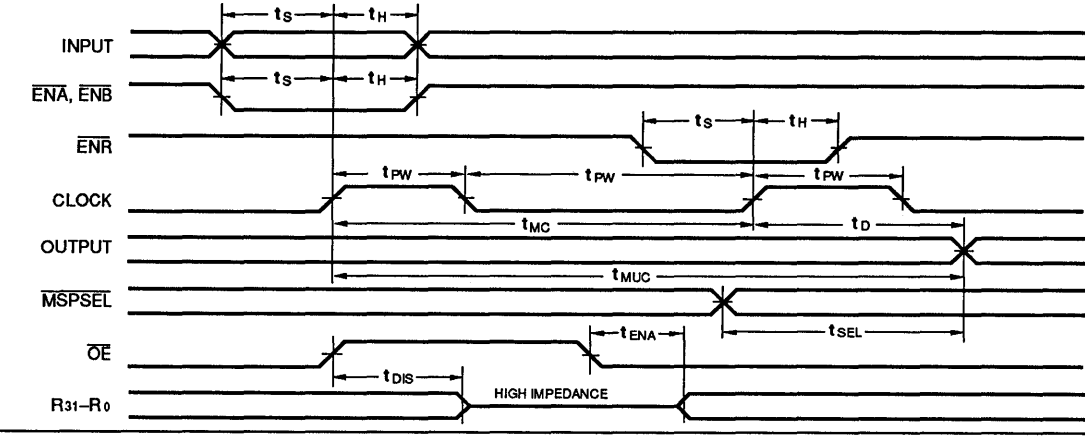
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU18-					
		65		45		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		45		35
t_{MUC}	Unclocked Multiply Time		85		65		55
t_D	Output Delay		30		30		25
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Output Enable Time (Note 11)		25		20		20
t_{DIS}	Output Disable Time (Note 11)		24		20		20
t_{PW}	Clock Pulse Width	15		15		15	
t_H	Input Register Hold Time	5		5		5	
t_S	Input Register Setup Time	15		15		12	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU18-					
		75		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		55		45
t_{MUC}	Unclocked Multiply Time		95		85		65
t_D	Output Delay		35		35		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Output Enable Time (Note 11)		25		20		20
t_{DIS}	Output Disable Time (Note 11)		24		20		20
t_{PW}	Clock Pulse Width	20		15		15	
t_H	Input Register Hold Time	5		5		5	
t_S	Input Register Setup Time	15		15		12	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

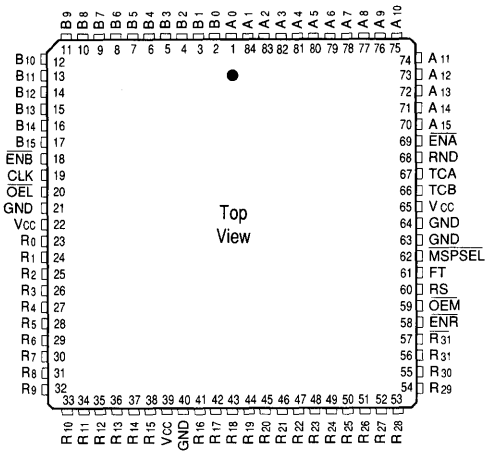
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

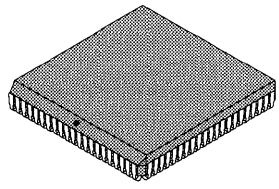
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

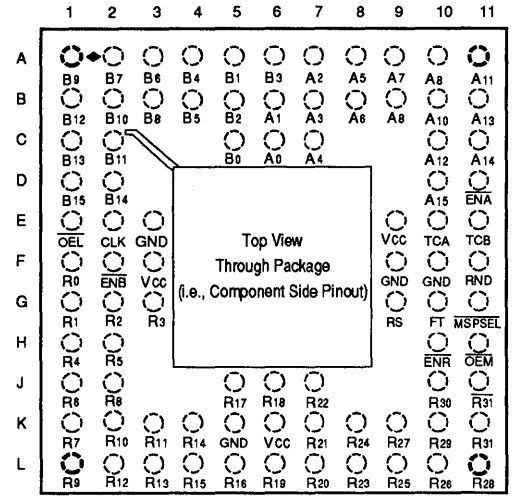
ORDERING INFORMATION

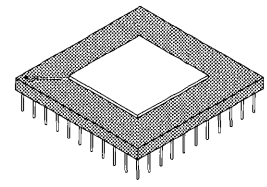
84-pin





84-pin





Speed	Plastic J-Lead Chip Carrier (J3)	Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening	
65 ns	LMU18JC65	LMU18GC65
45 ns	" " 45	" " 45
35 ns	" " 35	" " 35
	–55°C to +125°C — Commercial Screening	
75 ns		LMU18GM75
55 ns		" " 55
45 ns		" " 45
	–55°C to +125°C — Extended Screening	
75 ns		LMU18GME75
55 ns		" " 55
45 ns		" " 45
	–55°C to +125°C — MIL-STD-883 Compliant	
75 ns		LMU18GMB75
55 ns		" " 55
45 ns		" " 45

12 x 12-bit Multiplier-Accumulator LMA1009/2009

FEATURES

- 45 ns Worst-Case Multiply-Accumulate Time
- Low Power CMOS Technology
- Replaces TRW TDC1009
- Two's Complement, Unsigned, or Mixed Operands
- Accumulator Performs Load, Accumulate, Subtract
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The **LMA1009** and **LMA2009** are 12-bit CMOS multiplier-accumulators. They are pin-for-pin equivalent to the TRW TDC1009 bipolar multiplier-accumulator. Full ambient temperature range operation is achieved by the use of advanced CMOS technology.

The LMA1009 and LMA2009 produce the 24-bit product of two 12-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 27-bit precision with the multiplier product sign extended as appropriate.

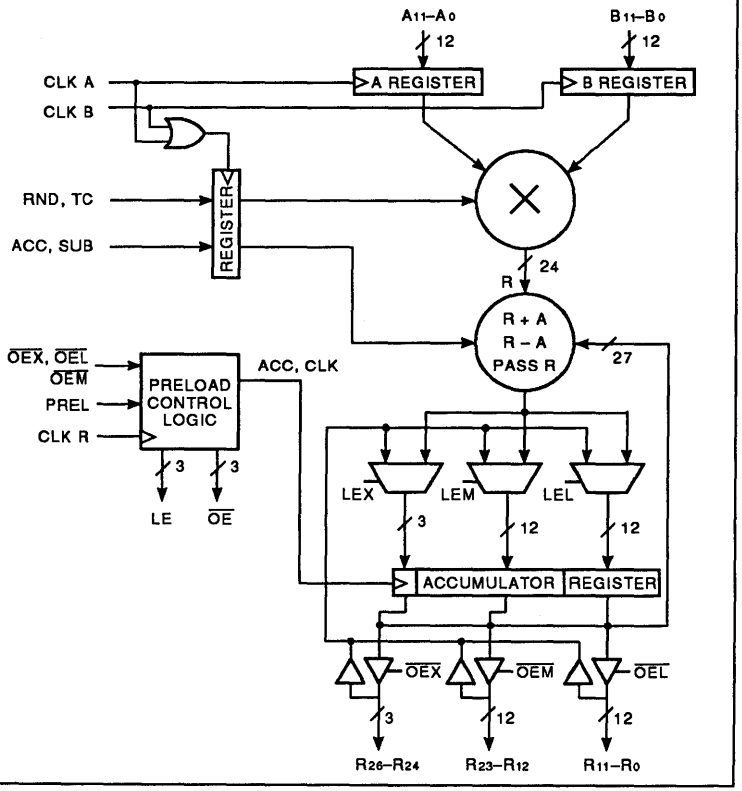
Data present at the A and B input registers (12 bits) is latched in on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. The TC control specifies the input as two's complement (TC high) or as unsigned magnitude (TC low). RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

The ACC and SUB inputs control accumulator operation. Assertion of ACC results in addition of the multiplier result and the accumulator contents, with the result stored in the accumulator register at the rising edge of CLK R. ACC and SUB high results in subtraction of the accumulator contents from the multiplier product, with the result again stored in the accumulator. With ACC low, no accumulation occurs and the next product is loaded directly into the output register.

The LMA1009 and LMA2009 output (accumulator) register is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 12 bits in length. The extended result register (XTR) is 3 bits long.

Each output register has an independent output enable control. In addition to providing control of the three-state output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are high and PREL is high, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is loaded in on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in the preload truth table.

LMA1009/2009 Block Diagram



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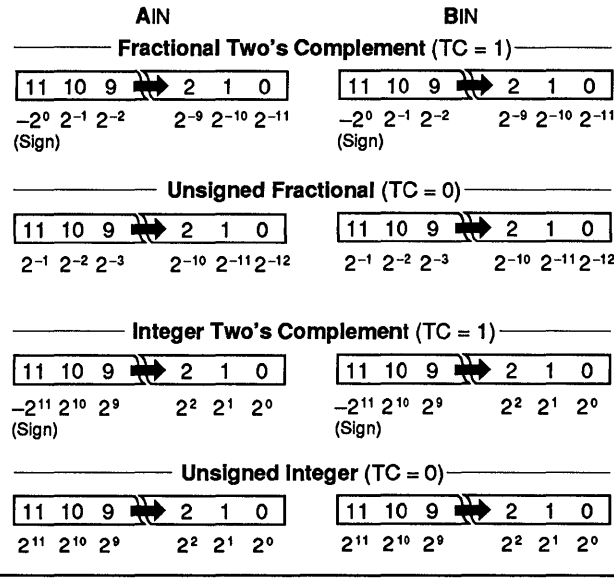
Preload Truth Table

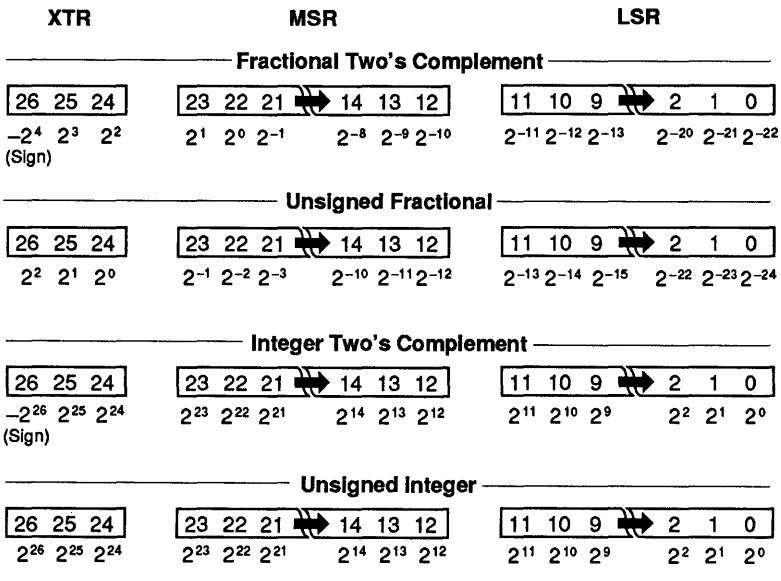
PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

OUT = Register available on output pins
Z = High impedance state
PREL = Data can be preloaded to appropriate register

Input Formats



Output Formats



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

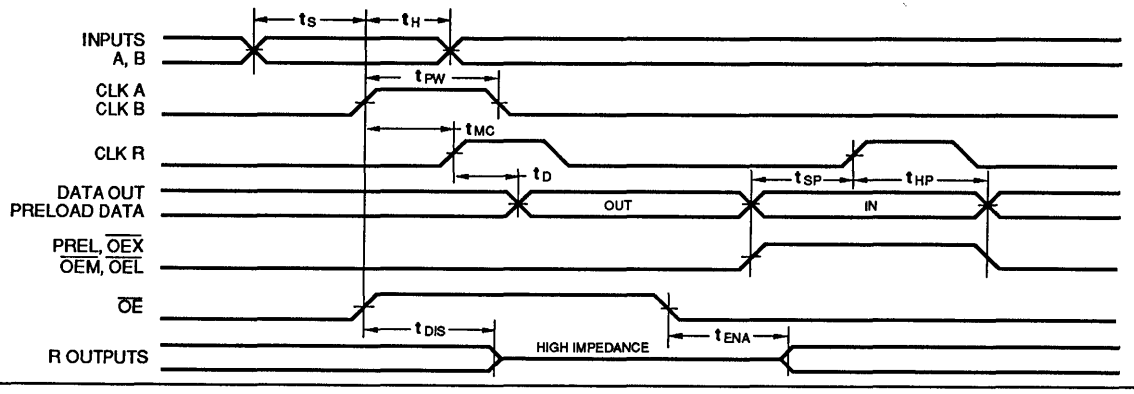
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1009/2009-					
		75		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		55		45
t_D	Output Delay		30		25		25
t_{ENA}	Output Enable Time (Note 11)		30		30		25
t_{DIS}	Output Disable Time (Note 11)		25		25		25
t_H	Input Register Hold Time	2		2		2	
t_{HP}	Preload Hold Time	2		2		2	
t_S	Input Register Setup Time	15		15		12	
t_{SP}	Preload Setup Time	15		15		12	
t_{PW}	Clock Pulse Width	15		15		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1009/2009-					
		95		65		55	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		95		65		55
t_D	Output Delay		35		30		25
t_{ENA}	Output Enable Time (Note 11)		35		35		30
t_{DIS}	Output Disable Time (Note 11)		30		30		30
t_H	Input Register Hold Time	2		2		2	
t_{HP}	Preload Hold Time	2		2		2	
t_S	Input Register Setup Time	20		20		15	
t_{SP}	Preload Setup Time	20		20		15	
t_{PW}	Clock Pulse Width	20		20		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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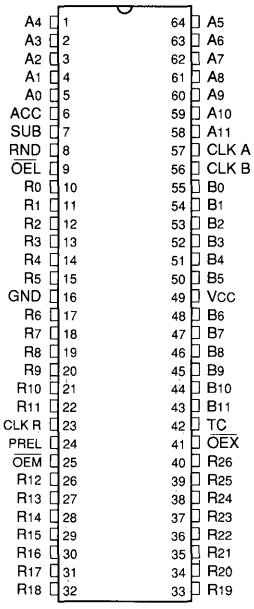
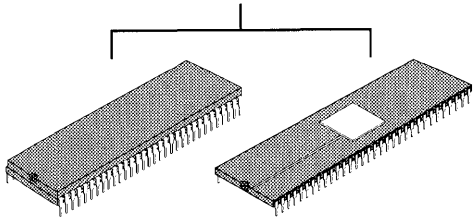
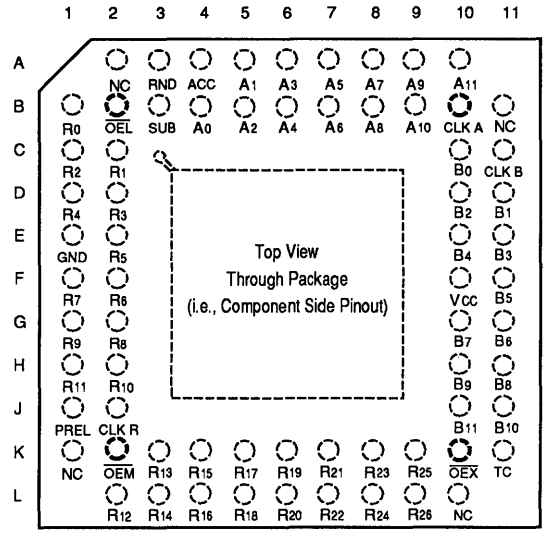
LMA1009 — ORDERING INFORMATION

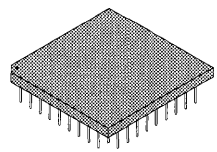
64-pin





68-pin

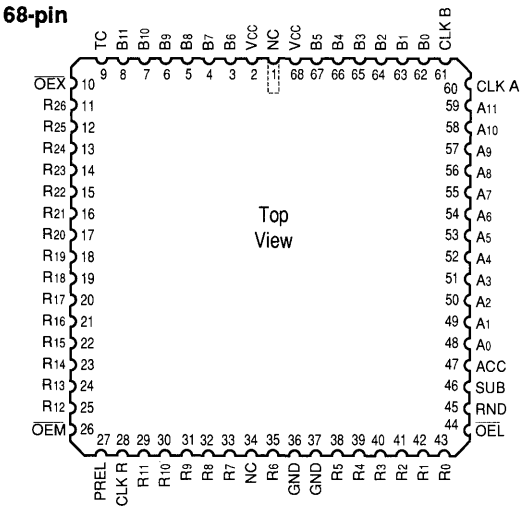


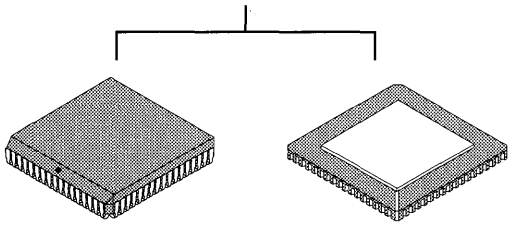


Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
75 ns	LMA1009PC75	LMA1009DC75	LMA1009GC75
55 ns	" " 55	" " 55	" " 55
45 ns	" " 45	" " 45	" " 45
	–55°C to +125°C — COMMERCIAL SCREENING		
95 ns		LMA1009DM95	LMA1009GM95
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — EXTENDED SCREENING		
95 ns		LMA1009DME95	LMA1009GME95
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
95 ns		LMA1009DMB95	LMA1009GMB95
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55

LMA2009 — ORDERING INFORMATION

68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
75 ns	LMA2009JC75	LMA2009KC75		
55 ns	" " 55	" " 55		
45 ns	" " 45	" " 45		
	–55°C to +125°C — COMMERCIAL SCREENING			
95 ns		LMA2009KM95		
65 ns		" " 65		
55 ns		" " 55		
	–55°C to +125°C — EXTENDED SCREENING			
95 ns		LMA2009KME95		
65 ns		" " 65		
55 ns		" " 55		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
95 ns		LMA2009KMB95		
65 ns		" " 65		
55 ns		" " 55		

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FEATURES

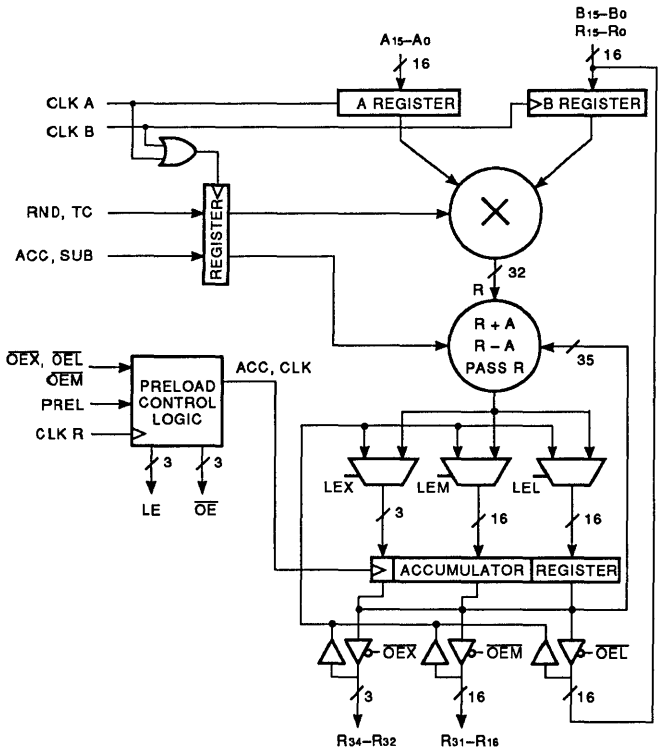
- 45 ns Worst-Case Multiply-Accumulate Time
- Low Power CMOS Technology
- Replaces TRW TDC1010 and AMD Am29510
- Two's Complement, Unsigned, or Mixed Operands
- Accumulator Performs Load, Accumulate, Subtract
- Three-State Outputs
- Available Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, HermeticDIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The **LMA1010** and **LMA2010** are high speed, low power multiplier-accumulators (MACs). They are pin-for-pin equivalent to the TRW TDC1010 and the AMD AM29510 bipolar multiplier accumulators. The LMA1010 and LMA2010 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is achieved with advanced CMOS technology.

The LMA1010 produces the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

LMA1010/2010 BLOCK DIAGRAM



Data present at the A and B inputs is loaded into the input registers on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are loaded on the rising edge of the logical OR of CLK A and CLK B. The TC control specifies the input as two's complement (TC high) or unsigned magnitude (TC low). RND, when high, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

The ACC and SUB inputs control accumulator operation. Assertion of ACC results in addition of the multiplier result and the accumulator contents, with the result stored in the accumulator register at the rising edge of CLK R. ACC and SUB high results in subtraction of the accumulator contents from the multiplier product, with the result again stored in the accumulator. With ACC low, no accumulation occurs and the next product is loaded directly into the output register.

The LMA1010 output (accumulator) register is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is 3 bits long. The LSR output pins are multiplexed with the B input pins.

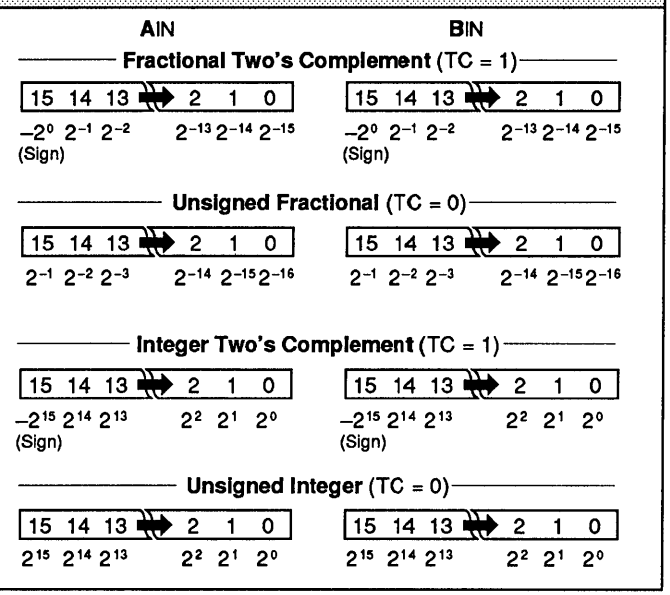
Each output register has an independent output enable control. In addition to providing three-state control of the output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are high and PREL is high, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is loaded in on the rising edge of CLK R. The interrelation of PREL and enable controls is summarized in the preload truth table.

Preload Truth Table

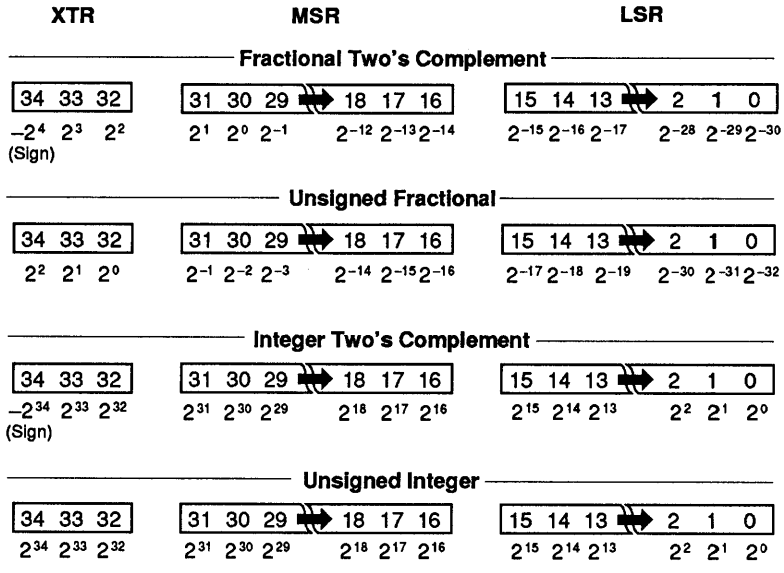
PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

OUT = Register available on output pins
Z = High impedance state
PREL = Data can be preloaded to appropriate register

Input Formats



Output Formats



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

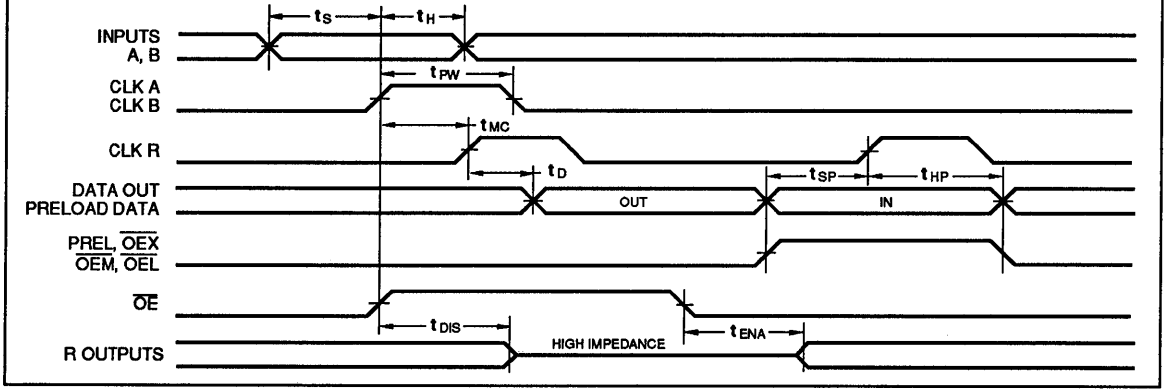
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1010/2010-					
		65		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		65		55		45
t_D	Output Delay		30		25		25
t_{ENA}	Output Enable Time (Note 11)		30		30		30
t_{DIS}	Output Disable Time (Note 11)		30		25		25
t_H	Input Register Hold Time	0		0		0	
t_{HP}	Preload Hold Time	0		0		0	
t_S	Input Register Setup Time	15		15		12	
t_{SP}	Preload Setup Time	15		15		12	
t_{PW}	Clock Pulse Width	15		15		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1010/2010-					
		75		65		55	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Multiply Time (Clocked)		75		65		55
t_D	Output Delay		35		30		30
t_{ENA}	Output Enable Time (Note 11)		35		30		30
t_{DIS}	Output Disable Time (Note 11)		35		25		25
t_H	Input Register Hold Time	0		0		0	
t_{HP}	Preload Hold Time	0		0		0	
t_S	Input Register Setup Time	20		15		12	
t_{SP}	Preload Setup Time	20		15		12	
t_{PW}	Clock Pulse Width	20		15		15	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

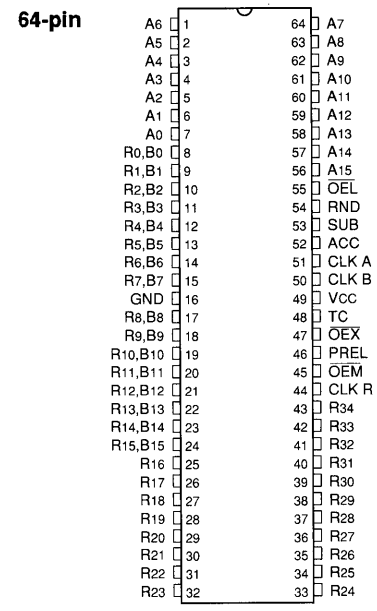
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

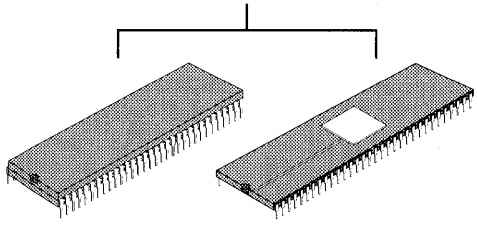
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

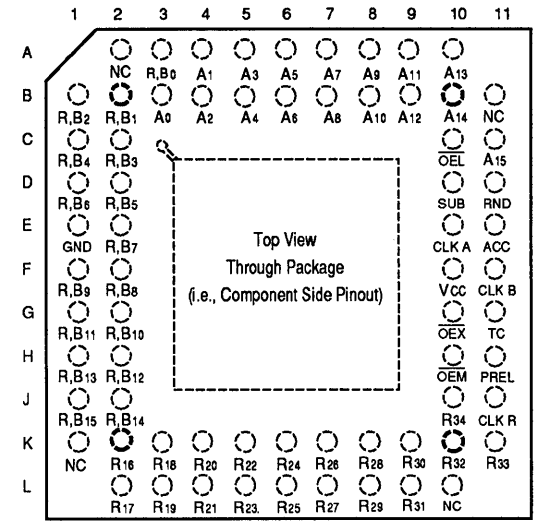
LMA1010 — ORDERING INFORMATION

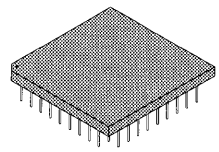
64-pin





68-pin

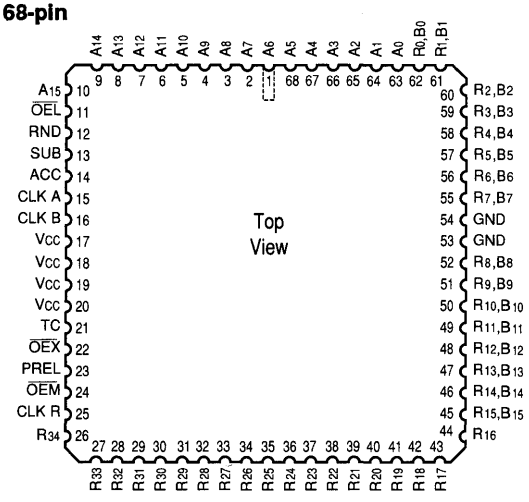


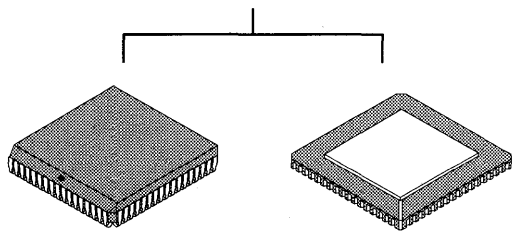


Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMA1010PC65	LMA1010DC65	LMA1010GC65
55 ns	" " 55	" " 55	" " 55
45 ns	" " 45	" " 45	" " 45
	–55°C to +125°C — COMMERCIAL SCREENING		
75 ns		LMA1010DM75	LMA1010GM75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — EXTENDED SCREENING		
75 ns		LMA1010DME75	LMA1010GME75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns		LMA1010DMB75	LMA1010GMB75
65 ns		" " 65	" " 65
55 ns		" " 55	" " 55

LMA2010 — ORDERING INFORMATION

68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMA2010JC65	LMA2010KC65		
55 ns	" " 55	" " 55		
45 ns	" " 45	" " 45		
	–55°C to +125°C — COMMERCIAL SCREENING			
75 ns		LMA2010KM75		
65 ns		" " 65		
55 ns		" " 55		
	–55°C to +125°C — EXTENDED SCREENING			
75 ns		LMA2010KME75		
65 ns		" " 65		
55 ns		" " 55		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMA2010KMB75		
65 ns		" " 65		
55 ns		" " 55		

5

12-bit Cascadable Multiplier-Accumulator LMS12

FEATURES

- 12 × 12-bit Multiplier with Pipelined 26-bit Output Summer
- Summer has 26-bit Input Port Fully Independent from Multiplier Inputs
- Cascadable to Form Video Rate FIR Filter with 3-bit Headroom
- A, B, and C Input Registers Separately Enabled for Maximum Flexibility
- 25 MHz Data Rate for FIR Filtering Applications
- High Speed, Low Power CMOS Technology
- Package Styles Available:
  - 84-pin Plastic LCC J-Lead
  - 84-pin Grid Array

DESCRIPTION

The **LMS12** is a high speed 12 × 12-bit combinatorial multiplier integrated with a 26-bit adder in a single 84-pin package. It is an ideal building block for the implementation of very high speed FIR filters for video, RADAR, and other similar applications. The LMS12 implements the general form (A•B) + C. As a result, it is also useful in implementing polynomial approximations to transcendental functions.

Architecture

A block diagram of the LMS12 is shown below. Its major features are discussed individually in the following paragraphs.

Multiplier

The A_{11}–A_0 and B_{11}–B_0 inputs to the LMS12 are captured at the rising edge of the clock in the 12-bit A and B input register, respectively. These registers are independently enabled by the $\overline{ENA}$ and $\overline{ENB}$ inputs. The registered input data are then applied to a 12 × 12-bit multiplier array, which produces a 24-bit result. Both the inputs and outputs of the multiplier are in 2's complement format. The multiplication result forms the input to the 24-bit product register.

Summer

The C_{25}–C_0 inputs to the LMS12 form a 26-bit 2's complement number which is captured in the C register at the rising edge of the clock. The C register is enabled by assertion of the $\overline{ENC}$ input. The summer is a 26-bit adder which operates on the C register data and the (sign extended) contents of the product register to produce a 26-bit sum. This sum is applied to the 26-bit S register.

Output Multiplexer

The FTS input controls a multiplexer which selects the data to be output on the S_{25}–S_0 lines. When FTS is asserted, the summer result is applied directly to the S output port. When FTS is deasserted, the multiplexer selects the S register for output on the S port, effecting a one-cycle delay of the summer result. The S output port can be forced to a high impedance state by driving the $\overline{OE}$ control line high. FTS would be asserted for conventional FIR filter applications, however the insertion of zero-coefficient filter taps may be accomplished by negating FTS. Negating FTS also allows application of the same filter transfer function to two interleaved datastreams with successive input and output sample points occurring on alternate clock cycles.

LMS12 Block Diagram

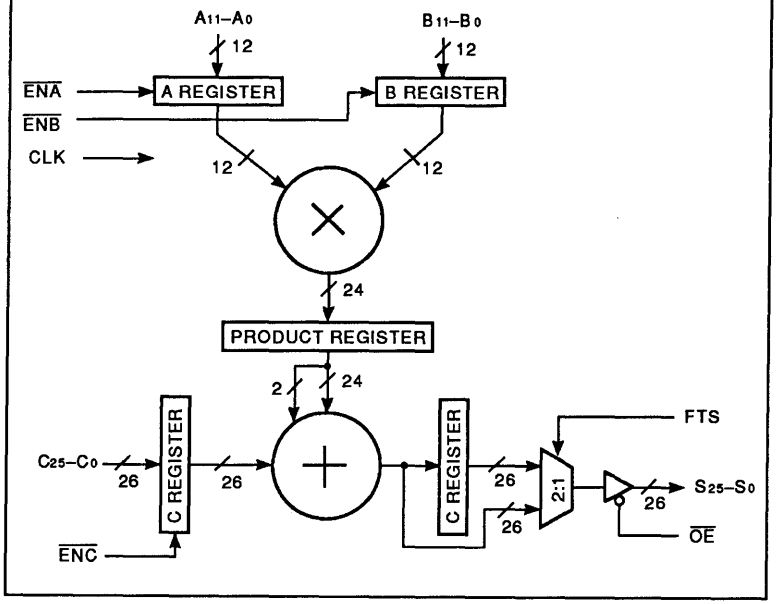
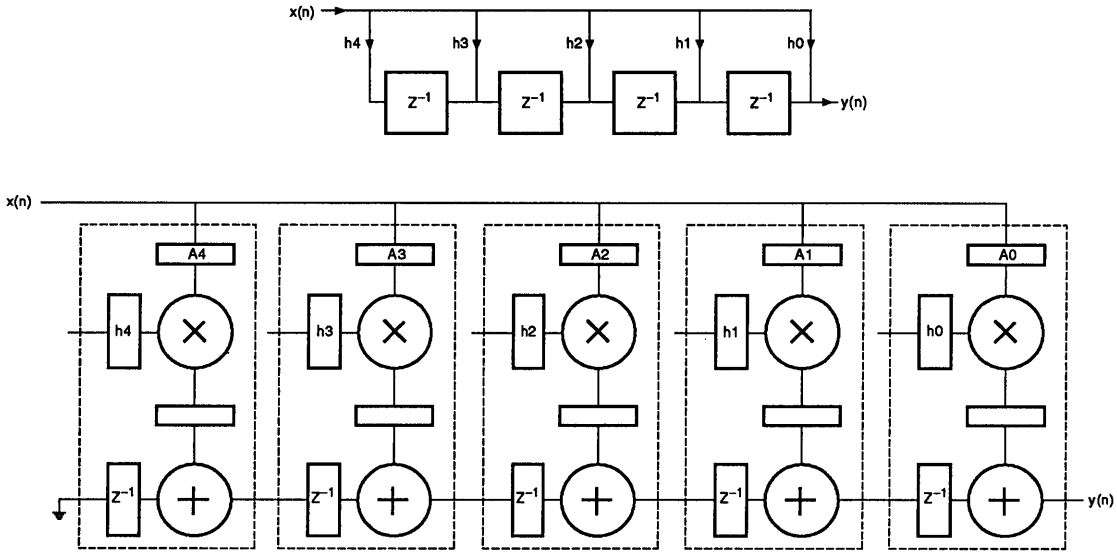


FIGURE 1. FLOW DIAGRAM FOR 5-TAP FIR FILTER.



Applications

The LMS12 is designed specifically for high speed FIR filtering applications requiring a throughput rate of one output sample per clock period. By cascading LMS12 units, the transpose form of the FIR transfer function is implemented directly, with each of the LMS12 units supplying one of the filter weights, and the cascaded summers accumulating the results. The signal flow graph for a 5-tap FIR filter and the equivalent implementation using LMS12's is shown in Fig. 1.

The operation of the 5-tap FIR filter implementation of Fig. 1 is depicted in Table 1. The filter weights h_4–h_0 are assumed to be latched in the B input registers of the LMS12 units. The x(n) data is applied in parallel to the A input registers of all devices. For descriptive purposes in the table, the A-register contents and Sum output data of each device is labelled according to the index of the weight applied by that device; i.e., S_0 is produced by the rightmost device, which has h_0 as its filter weight and A_0 as its input register contents. Each column represents one clock cycle, with the data passing a particular point in the system illustrated across each row.

TABLE 1. TIMING EXAMPLE FOR 5-TAP NONDECIMATING FIR FILTER.

CLK Cycle	1	2	3	4	5	6	7	8	9
$X_{(n)}$	X_n	X_{n+1}	X_{n+2}	X_{n+3}	X_{n+4}	X_{n+5}	X_{n+6}	X_{n+7}	X_{n+8}
A_4 Register Sum 4		X_n	X_{n+1} h_4X_n	X_{n+2} h_4X_{n+1}	X_{n+3} h_4X_{n+2}	X_{n+4} h_4X_{n+3}	X_{n+5} h_4X_{n+4}	X_{n+6} h_4X_{n+5}	X_{n+7} h_4X_{n+6}
A_3 Register Sum 3		X_n	X_{n+1} h_3X_n $+ h_4X_{n-1}$	X_{n+2} h_3X_{n+1} $+ h_4X_n$	X_{n+3} h_3X_{n+2} $+ h_4X_{n+1}$	X_{n+4} h_3X_{n+3} $+ h_4X_{n+2}$	X_{n+5} h_3X_{n+4} $+ h_4X_{n+3}$	X_{n+6} h_3X_{n+5} $+ h_4X_{n+4}$	X_{n+7} h_3X_{n+6} $+ h_4X_{n+5}$
A_2 Register Sum 2		X_n	X_{n+1} h_2X_n $+ h_3X_{n-1}$ $+ h_4X_{n-2}$	X_{n+2} h_2X_{n+1} $+ h_3X_n$ $+ h_4X_{n-1}$	X_{n+3} h_2X_{n+2} $+ h_3X_{n+1}$ $+ h_4X_n$	X_{n+4} h_2X_{n+3} $+ h_3X_{n+2}$ $+ h_4X_{n+1}$	X_{n+5} h_2X_{n+4} $+ h_3X_{n+3}$ $+ h_4X_{n+2}$	X_{n+6} h_2X_{n+5} $+ h_3X_{n+4}$ $+ h_4X_{n+3}$	X_{n+7} h_2X_{n+6} $+ h_3X_{n+5}$ $+ h_4X_{n+4}$
A_1 Register Sum 1		X_n	X_{n+1} h_1X_n $+ h_2X_{n-1}$ $+ h_3X_{n-2}$ $+ h_4X_{n-3}$	X_{n+2} h_1X_{n+1} $+ h_2X_n$ $+ h_3X_{n-1}$ $+ h_4X_{n-2}$	X_{n+3} h_1X_{n+2} $+ h_2X_{n+1}$ $+ h_3X_n$ $+ h_4X_{n-1}$	X_{n+4} h_1X_{n+3} $+ h_2X_{n+2}$ $+ h_3X_{n+1}$ $+ h_4X_n$	X_{n+5} h_1X_{n+4} $+ h_2X_{n+3}$ $+ h_3X_{n+2}$ $+ h_4X_{n+1}$	X_{n+6} h_1X_{n+5} $+ h_2X_{n+4}$ $+ h_3X_{n+3}$ $+ h_4X_{n+2}$	X_{n+7} h_1X_{n+6} $+ h_2X_{n+5}$ $+ h_3X_{n+4}$ $+ h_4X_{n+3}$
A_0 Register Sum 0		X_n	X_{n+1} h_0X_n $+ h_1X_{n-1}$ $+ h_2X_{n-2}$ $+ h_3X_{n-3}$ $+ h_4X_{n-4}$	X_{n+2} h_0X_{n+1} $+ h_1X_n$ $+ h_2X_{n-1}$ $+ h_3X_{n-2}$ $+ h_4X_{n-3}$	X_{n+3} h_0X_{n+2} $+ h_1X_{n+1}$ $+ h_2X_n$ $+ h_3X_{n-1}$ $+ h_4X_{n-2}$	X_{n+4} h_0X_{n+3} $+ h_1X_{n+2}$ $+ h_2X_{n+1}$ $+ h_3X_n$ $+ h_4X_{n-1}$	X_{n+5} h_0X_{n+4} $+ h_1X_{n+3}$ $+ h_2X_{n+2}$ $+ h_3X_{n+1}$ $+ h_4X_n$	X_{n+6} h_0X_{n+5} $+ h_1X_{n+4}$ $+ h_2X_{n+3}$ $+ h_3X_{n+2}$ $+ h_4X_{n+1}$	X_{n+7} h_0X_{n+6} $+ h_1X_{n+5}$ $+ h_2X_{n+4}$ $+ h_3X_{n+3}$ $+ h_4X_{n+2}$

5

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

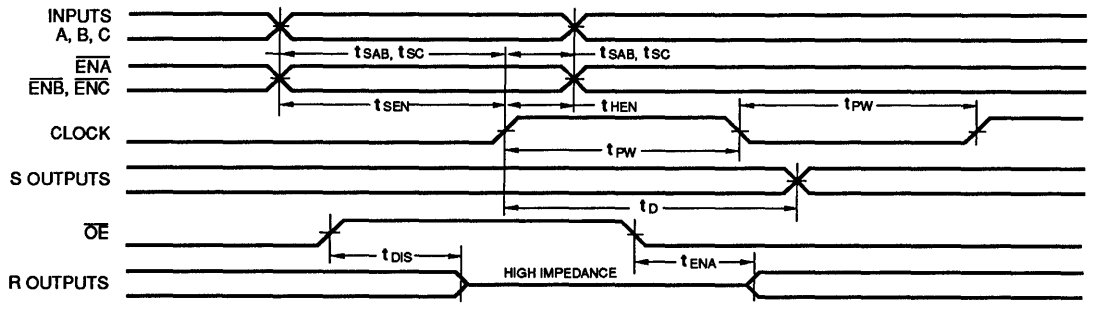
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMS12-					
		65		50		40	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCP	Clock Period	40		35		30	
tD	Clock to S–FT = 1		50		40		35
	Clock to S–FT = 0		25		25		25
tSC	C Data Setup Time	15		10		7	
tSAB	A, B Data Setup Time	15		12		12	
tSEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12		12	
tHC	C Data Hold Time	5		5		5	
tHAB	A, B Data Hold Time	5		5		5	
tHEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5	
tPW	Clock Pulse Width	15		15		12	
tENA	Output Enable Time (Note 11)		25		25		25
tDIS	Output Disable Time (Note 11)		22		22		22

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMS12-					
		65		50			
Symbol	Parameter	Min	Max	Min	Max	Min	Max
tCP	Clock Period	40		35			
tD	Clock to S–FT = 1		50		40		
	Clock to S–FT = 0		25		25		
tSC	C Data Setup Time	15		12			
tSAB	A, B Data Setup Time	15		12			
tSEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12			
tHC	C Data Hold Time	5		5			
tHAB	A, B Data Hold Time	5		5			
tHEN	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5			
tPW	Clock Pulse Width	15		15			
tENA	Output Enable Time (Note 11)		25		25		
tDIS	Output Disable Time (Note 11)		22		22		

SWITCHING WAVEFORMS



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

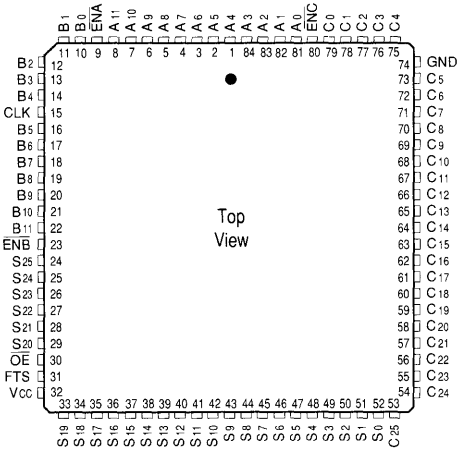
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

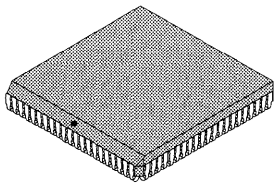
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

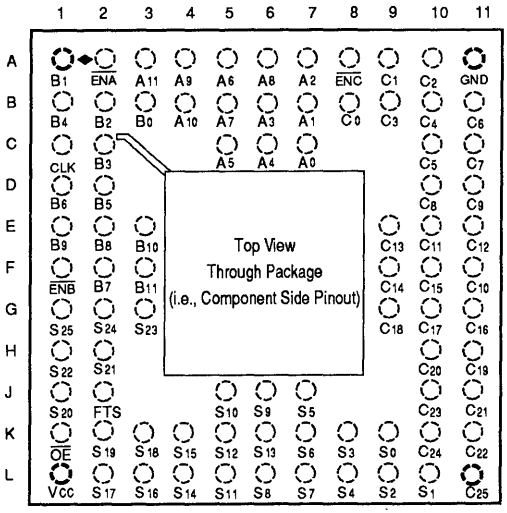
ORDERING INFORMATION

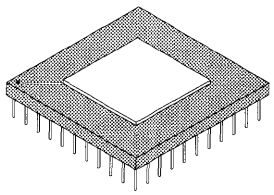
84-pin





84-pin





Speed	Plastic J-Lead Chip Carrier (J3)	Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening	
65 ns	LMS12JC65	LMS12GC65
50 ns	" " 50	" " 50
40 ns	" " 40	" " 40
	–55°C to +125°C — Commercial Screening	
65 ns		LMS12GM65
50 ns		" " 50
	–55°C to +125°C — Extended Screening	
65 ns		LMS12GME65
50 ns		" " 50
	–55°C to +125°C — MIL-STD-883 Compliant	
65 ns		LMS12GMB65
50 ns		" " 50

4 x 8-bit Multilevel Pipeline Register — L29C520/521

FEATURES

- Four 8-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with AMD AM29520 and AM29521
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Sidebraze, Hermetic DIP
  - 24-pin Ceramic Flatpack
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC (Type C)

DESCRIPTION

The Logic Devices **L29C520** and **L29C521** are pin-for-pin compatible with the Advanced Micro Devices AM29520 and AM29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_0 and I_1, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R_1 and shifted sequentially through R_2, R_3, and R_4. Also, for the L29C520, data may be loaded from the inputs into either R_1 or R_3 with only R_2 or R_4 shifting. The L29C521 devices differ from the L29C520 in that R_2 and R_4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_0 and I_1 may be set to prevent any register from changing.

The S_0 and S_1 select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1

I_1	I_0	L29C520 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

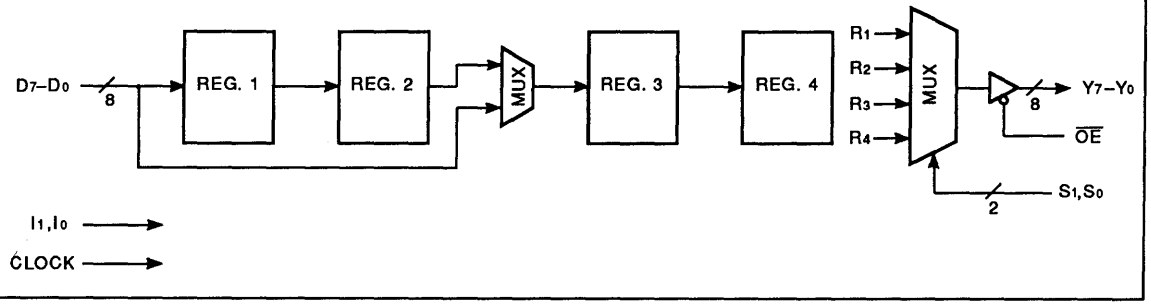
TABLE 2

I_1	I_0	L29C521 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 HOLD
H	L	D→R1 HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 3

S_1	S_0	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

L29C520/521 BLOCK DIAGRAM



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –3.0 V to +7.0 V
Signal applied to high impedance output ..... –3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –6.5 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

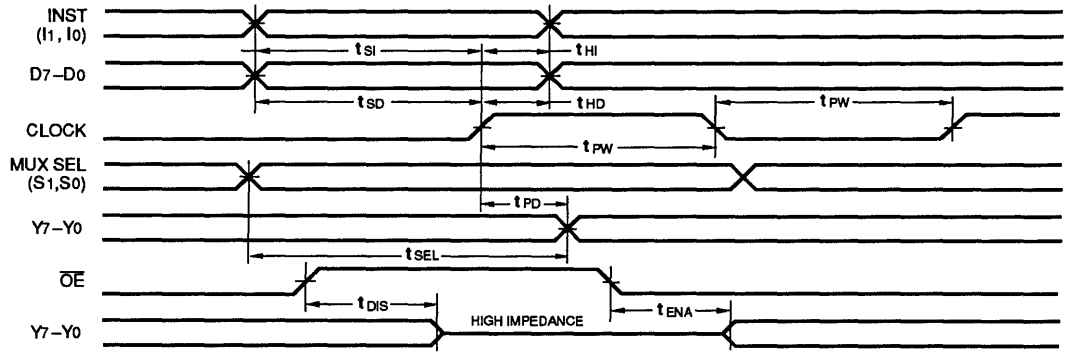
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C520/521- 25 Min	25 Max	22 Min	22 Max
t_{PD}	CLK to Y_7–Y_0		25		22
t_{SEL}	S_1,S_0 to Y_7–Y_0		25		20
t_{SD}	D_7–D_0 to CLK Setup	13		10	
t_{HD}	CLK to D_7–D_0 Hold	3		3	
t_{SI}	I_1,I_0 to CLK Setup	13		10	
t_{HI}	CLK to I_1,I_0 Hold	3		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21
t_{PW}	Clock Pulse Width	10		10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C520/521- 30 Min	30 Max	24 Min	24 Max
t_{PD}	CLK to Y_7–Y_0		30		24
t_{SEL}	S_1,S_0 to Y_7–Y_0		30		22
t_{SD}	D_7–D_0 to CLK Setup	15		10	
t_{HD}	CLK to D_7–D_0 Hold	5		3	
t_{SI}	I_1,I_0 to CLK Setup	15		10	
t_{HI}	CLK to I_1,I_0 Hold	5		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22
t_{PW}	Clock Pulse Width	15		10	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

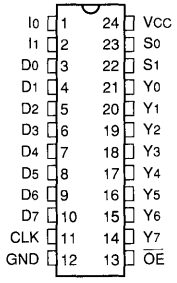
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

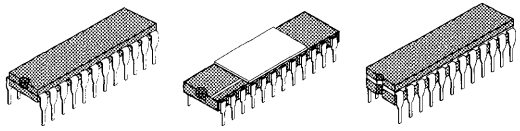
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

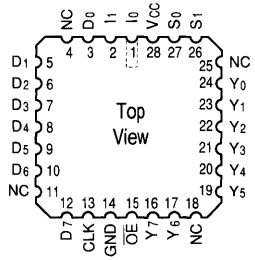
ORDERING INFORMATION

24-pin
(0.3" wide)





28-pin

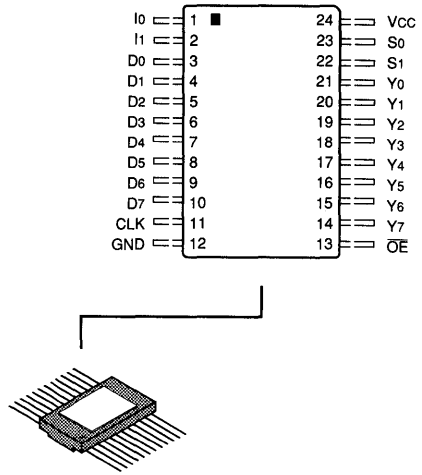


Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening				
25 ns 22 ns	L29C520PC or L29C521PC — 25 / 22	L29C520DC or L29C521DC — 25 / 22	L29C520CC or L29C521CC — 25 / 22	L29C520JC or L29C521JC — 25 / 22	L29C520KC or L29C521KC — 25 / 22
	–55°C to +125°C — Commercial Screening				
30 ns 24 ns		L29C520DM or L29C521DM — 30 / 24	L29C520CM or L29C521CM — 30 / 24		L29C520KM or L29C521KM — 30 / 24
	–55°C to +125°C — Extended Screening				
30 ns 24 ns		L29C520DME or L29C521DME — 30 / 24	L29C520CME or L29C521CME — 30 / 24		L29C520KME or L29C521KME — 30 / 24
	–55°C to +125°C — MIL-STD-883 Compliant				
30 ns 24 ns		L29C520DMB or L29C521DMB — 30 / 24	L29C520CMB or L29C521CMB — 30 / 24		L29C520KMB or L29C521KMB — 30 / 24

5

ORDERING INFORMATION

24-pin



Speed	Flatpack (F1)		
	0°C to +70°C — Commercial Screening		
25 ns 22 ns	L29C520FC or L29C521FC — 25 / 22		
	–55°C to +125°C — Commercial Screening		
30 ns 24 ns	L29C520FM or L29C521FM — 30 / 24		
	–55°C to +125°C — Extended Screening		
30 ns 24 ns	L29C520FME or L29C521FME — 30 / 24		
	–55°C to +125°C — MIL-STD-883 Compliant		
30 ns 24 ns	L29C520FMB or L29C521FMB — 30 / 24		

4 x 16-bit Multilevel Pipeline Register LPR520/521

FEATURES

- Four 16-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC (Type C)

DESCRIPTION

The Logic Devices **LPR520** and **LPR521** are functionally compatible with the Advanced Micro Devices AM29520 and AM29521 but are 16 bits wide. They are implemented in low power CMOS.

The LPR520 and LPR521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_0 and I_1, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R_1 and shifted sequentially through R_2, R_3, and R_4. Also, for the LPR520, data may be loaded from the inputs into either R_1 or R_3 with only R_2 or R_4 shifting. The LPR521 devices differ from the LPR520 in that R_2 and R_4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_0 and I_1 may be set to prevent any register from changing.

The S_0 and S_1 select lines control a 4 to 1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1

I_1	I_0	L29C520 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 R3→R4
H	L	D→R1 R1→R2 HOLD HOLD
H	H	ALL REGISTERS ON HOLD

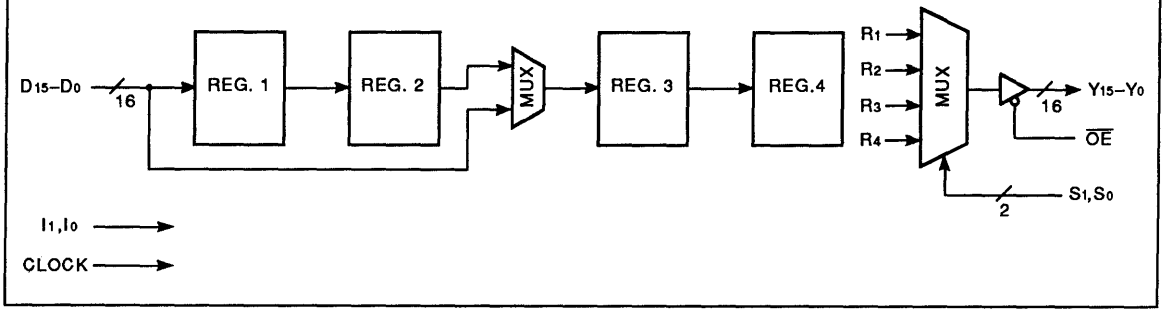
TABLE 2

I_1	I_0	L29C521 Instruction
L	L	D→R1 R1→R2 R2→R3 R3→R4
L	H	HOLD HOLD D→R3 HOLD
H	L	D→R1 HOLD HOLD HOLD
H	H	ALL REGISTERS ON HOLD

TABLE 3

S_1	S_0	Reg. Selected
L	L	Reg 4
L	H	Reg 3
H	L	Reg 2
H	H	Reg 1

LPR520/521 BLOCK DIAGRAM



5

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

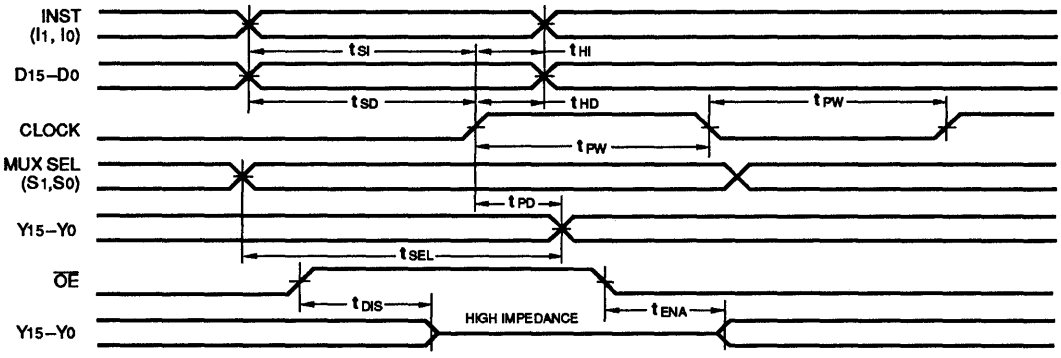
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LPR520/521- 25 Min	25 Max	22 Min	22 Max
t_{PD}	CLK to Y_{15}–Y_0		25		22
t_{SEL}	S_1,S_0 to Y_{15}–Y_0		25		20
t_{SD}	D_{15}–D_0 to CLK Setup	13		10	
t_{HD}	CLK to D_{15}–D_0 Hold	3		3	
t_{SI}	I_1,I_0 to CLK Setup	13		10	
t_{HI}	CLK to I_1,I_0 Hold	3		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25		15
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		21
t_{PW}	Clock Pulse Width	10		10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LPR520/521- 30 Min	30 Max	24 Min	24 Max
t_{PD}	CLK to Y_{15}–Y_0		30		24
t_{SEL}	S_1,S_0 to Y_{15}–Y_0		30		22
t_{SD}	D_{15}–D_0 to CLK Setup	15		10	
t_{HD}	CLK to D_{15}–D_0 Hold	5		3	
t_{SI}	I_1,I_0 to CLK Setup	15		10	
t_{HI}	CLK to I_1,I_0 Hold	5		3	
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		20		16
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		25		22
t_{PW}	Clock Pulse Width	15		10	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

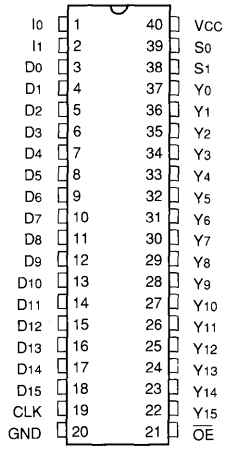
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

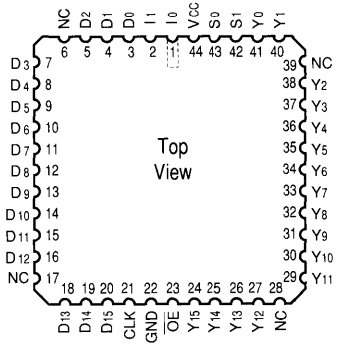
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

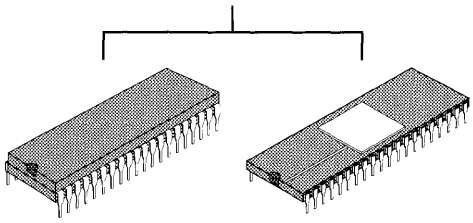
ORDERING INFORMATION

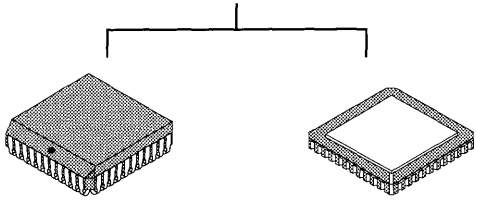
40-pin



44-pin







Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
25 ns 22 ns	LPR520PC or LPR521PC — 25 / 22	LPR520DC or LPR521DC — 25 / 22	LPR520JC or LPR521JC — 25 / 22	LPR520KC or LPR521KC — 25 / 22
	–55°C to +125°C — Commercial Screening			
30 ns 24 ns		LPR520DM or LPR521DM — 30 / 24		LPR520KM or LPR521KM — 30 / 24
	–55°C to +125°C — Extended Screening			
30 ns 24 ns		LPR520DME or LPR521DME — 30 / 24		LPR520KME or LPR521KME — 30 / 24
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns 24 ns		LPR520DMB or LPR521DMB — 30 / 24		LPR520KMB or LPR521KMB — 30 / 24

5

Dual Pipeline Register — L29C524/525

FEATURES

- Pipeline Registers — Dual 7-Deep (L29C524) or Dual 8-Deep (L29C525)
- Configurable to Single 14-Deep and Single 16-Deep
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with AMD AM29524 and AM29525
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin Plastic LCC

DESCRIPTION

The Logic Devices **L29C524** and **L29C525** are high performance, low power CMOS pipeline registers. They are pin-for-pin compatible with the Advanced Micro Devices Am29524 and Am29525. The products can be configured as two independent, 7-level (or 8-level) pipelines or as single 14-level (or 16-level) pipelines. The configuration implemented is determined by the instruction code (I_1,I_0) as shown in Table 2.

The I_1,I_0 instruction code controls the internal routing of data and loading of each register. For instruction I_1,I_0 = 00 (Push A & B), data applied at the D_7–D_0 inputs is loaded into register A_0 at the rising edge of the Clock. The contents of A_0 simultaneously moves to register A_1, A_1 moves to A_2, and so on. The contents of the last register on the "A" side (A_6 for the L29C524, A_7 for the L29C525) are wrapped back to register B_0. The registers on the B side are similarly shifted, with the contents of the last register on the B side (B_6 for the L29C524, B_7 for the L29C525) lost.

Instruction I_1,I_0 = 01 (Push B) acts similarly to the Push A & B instruction, except that only the B side registers are shifted. The input data is applied to register B_0, and the contents of the last register on the B side (B_6 for the L29C524, B_7 for the L29C525) are lost. The contents of the A side registers are unaffected. Instruction I_1,I_0 = 10 (Push A) is identical to the Push B instruction, except that A side registers are shifted and B side registers are unaffected.

Instruction I_1,I_0 = 11 (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

The contents of any of the registers is selectable at the output through the use of the S_3–S_0 control inputs. On the L29C524, the input pins D_7–D_0 may also be selected to drive the output, and all output pins may be forced to zero. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_3–S_0 controls is given in Table 3.

5

L29C524/525 Block Diagram

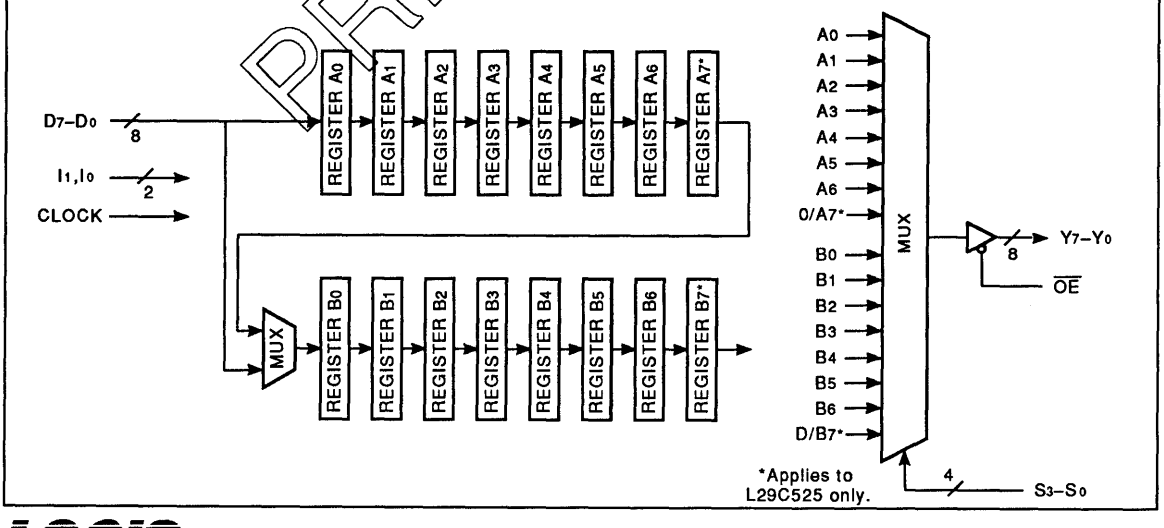
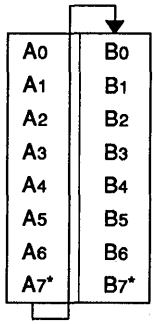
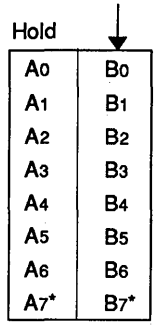
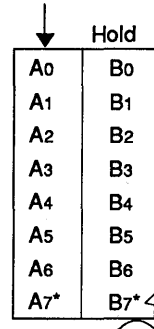
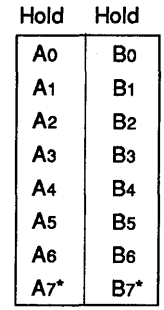


Table 1. Register Load Operations *(See Table 2 for Instruction Codes.)*

Single 14/16 Level	Dual 7/8 Level		
Push A & B	**Push B**	**Push A**	**No-Op**
			

* A7 and B7 registers apply only to L29C525

Table 2. Instruction Set Descriptions

Mnemonic	Inputs I1	Inputs I0	Description
Shift	0	0	Push A & B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	No-Op

Table 3. Select Operation Descriptions

S3	S2	S1	S0	Y7–Y0
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	0	A6
0	1	1	1	0 (L29C524) A7 (L29C525)
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	0	B6
1	1	1	1	D7–D0 (L29C524) B7 (L29C525)

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −12 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			−250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

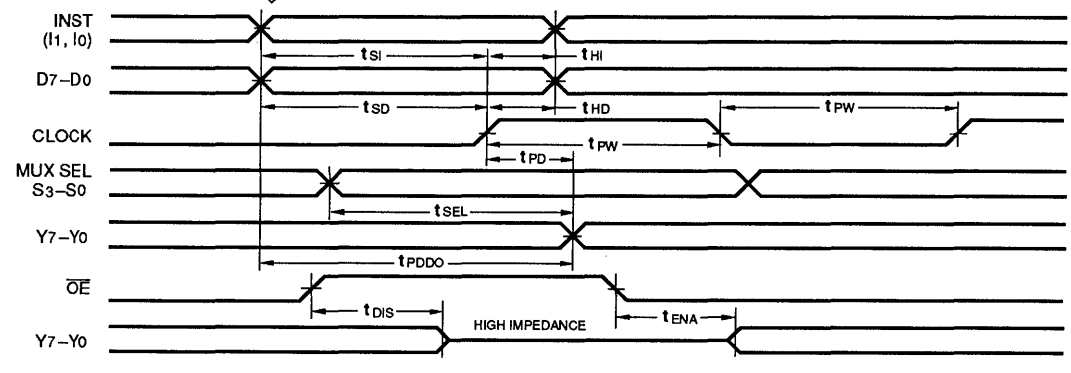
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C524/525-20 Min	L29C524/525-20 Max	L29C524/525- Min	L29C524/525- Max
t_{PD}	CLK to Y_7–Y_0		20		
t_{SEL}	S_3–S_0 to Y_7–Y_0		20		
t_{PDDO}	D_7–D_0 to Y_7–Y_0 (L29C524)		20		
t_{SD}	D_7–D_0 to CLK Setup	7			
t_{HD}	CLK to D_7–D_0 Hold	0			
t_{SI}	I_1,I_0 to CLK Setup	7			
t_{HI}	CLK to I_1,I_0 Hold	2			
t_{DIS}	$\overline{OE}$ to Output Disable Times (Note 11)		13		
t_{ENA}	$\overline{OE}$ to Output Enable Times (Note 11)		15		
t_{PW}	Clock Pulse Width	12			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C524/525-25 Min	L29C524/525-25 Max	L29C524/525- Min	L29C524/525- Max
t_{PD}	CLK to Y_7–Y_0		25		
t_{SEL}	S_3–S_0 to Y_7–Y_0		25		
t_{PDDO}	D_7–D_0 to Y_7–Y_0 (L29C524)		25		
t_{SD}	D_7–D_0 to CLK Setup	7			
t_{HD}	CLK to D_7–D_0 Hold	2			
t_{SI}	I_1,I_0 to CLK Setup	7			
t_{HI}	CLK to I_1,I_0 Hold	2			
t_{DIS}	$\overline{OE}$ to Output Disable Times (Note 11)		13		
t_{ENA}	$\overline{OE}$ to Output Enable Times (Note 11)		15		
t_{PW}	Clock Pulse Width	12			

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

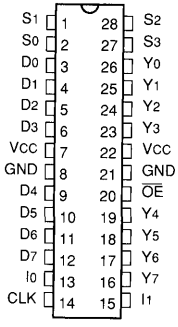
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

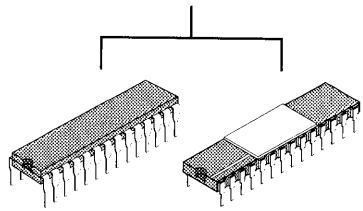
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

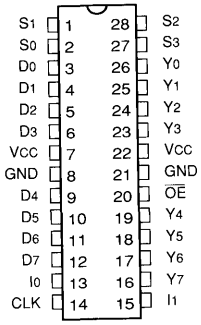
ORDERING INFORMATION

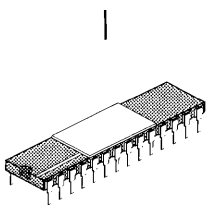
28-pin
(0.3" wide)



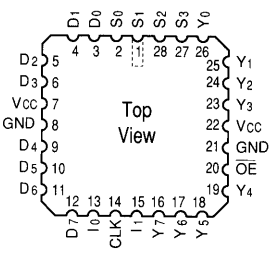


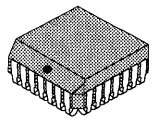
28-pin
(0.4" wide)





28-pin
(0.4" wide)





Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	Sidebraze Hermetic DIP (D11)	Plastic Leaded Chip Carrier (J4)
	0°C to +70°C — Commercial Screening			
20 ns	L29C524PC20 or L29C525PC20	L29C524DC20 or L29C525DC20	L29C524HC20 or L29C525HC20	L29C524JC20 or L29C525JC20
	–55°C to +125°C — Commercial Screening			
25 ns		L29C524DM25 or L29C525DM25	L29C524HM25 or L29C525HM25	
	–55°C to +125°C — Extended Screening			
25 ns		L29C524DME25 or L29C525DME25	L29C524HME25 or L29C525HME25	
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L29C524DMB25 or L29C525DMB25	L29C524HMB25 or L29C525HMB25	

Variable Length Shift Register — L10C11

FEATURES

- Variable Length 4 or 8-bit Wide Shift Register
- Selectable Length from 3 to 18 Stages
- Hold, Shift, Load Instructions
- Separate Data In and Data Out Pins
- High Speed, Low Power CMOS Technology
- Plug Compatible with TRW TDC1011
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin CerDIP
  - 24-pin Sidebraze, Hermetic DIP

DESCRIPTION

The **L10C11** consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock. Both shift registers can be programmed together to any length from 3 to 18 stages inclusive, or one register can be fixed at 18 stages of delay while the other is variable. The configuration implemented is determined by the Length code (L_3–L_0) and MODE line as shown in Table 1.

Each input is applied to a chain of registers which are clocked on the rising edge of the common CLK input. These registers are numbered R1 through R17 and R1' to R17', corresponding to the D_3–D_0 and D_7–D_4 data fields, respectively. A multiplexer serves to route the contents of any of registers R2 through R17 to the output register, denoted R18. A similar multiplexer operates on the contents of R2' through R17' to load R18'. Note that the minimum-length path from data inputs to outputs is R1 to R2 to R18, consisting of three stages of delay.

The MODE control input is registered, and determines whether one or both of the internal shift registers have variable length. When MODE = 0, both D_3–D_0 and D_7–D_4 are delayed by an amount which is controlled by the Length inputs. When MODE = 1, the D_7–D_4 field is delayed by 18 stages independent of the Length setting.

The Length code controls the number of stages of delay applied to the D inputs, as shown in Table 1 on the following page. When the Length register contains 0, the inputs are delayed by 3 clock periods. When the Length register contains 1, the delay is 4 clock periods, and so forth. The Length control field (L_3–L_0) and the MODE input are registered at the rising edge of the Clock. Both the length and MODE values may be changed at any time without affecting the contents of registers R17–R1.

L10C11 Block Diagram

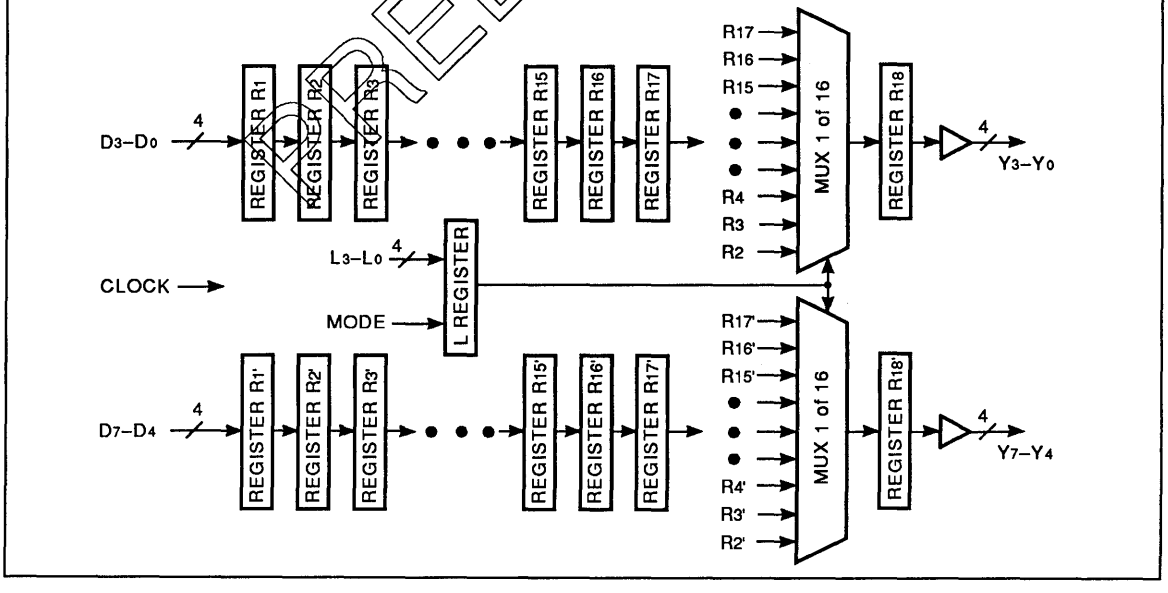


Table 1. Control Encoding

Input Code				Mode=0		Mode=1	
				Delay		Delay	
L_3	L_2	L_1	L_0	Y_{3-0}	Y_{7-4}	Y_{3-0}	Y_{7-4}
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Condition

To meet specified electrical and switching characteristics

Mode	Temperature Range	Supply Voltage
Active Operation, Com.	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Mil.	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –12.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

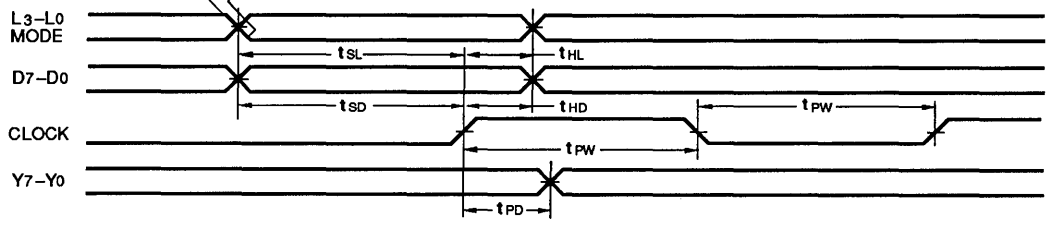
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L10C11-25 Min	L10C11-25 Max	L10C11- Min	L10C11- Max
t_{PD}	CLK to Y_7–Y_0		25		
t_{SD}	D_7–D_0 to CLK Setup	20			
t_{HD}	CLK to D_7–D_0 Hold	0			
t_{SL}	L_3–L_0, MODE to CLK Setup	20			
t_{HL}	CLK to L_3–L_0, MODE Hold	0			
t_{PW}	Clock Pulse Width	15			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L10C11-30 Min	L10C11-30 Max	L10C11- Min	L10C11- Max
t_{PD}	CLK to Y_7–Y_0		30		
t_{SD}	D_7–D_0 to CLK Setup	25			
t_{HD}	CLK to D_7–D_0 Hold	2			
t_{SL}	L_3–L_0, MODE to CLK Setup	25			
t_{HL}	CLK to L_3–L_0, MODE Hold	2			
t_{PW}	Clock Pulse Width	15			

SWITCHING WAVEFORMS



5

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

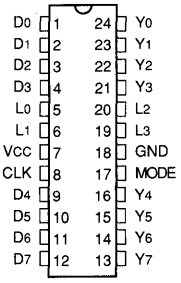
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

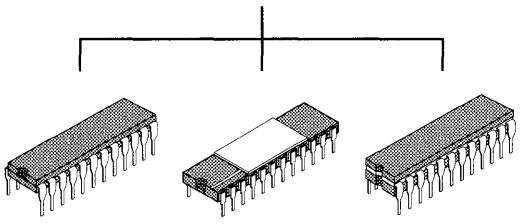
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

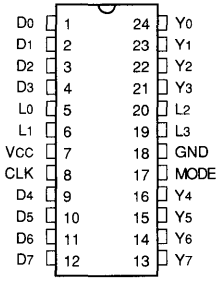
ORDERING INFORMATION

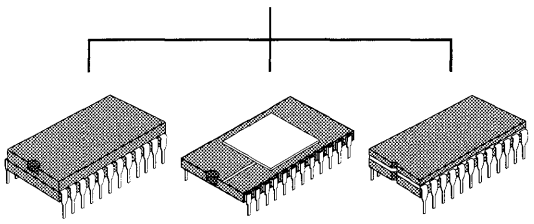
24-pin
(0.3" wide)





24-pin
(0.6" wide)





Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Plastic DIP (P1)	Sidebraze Hermetic DIP (D1)	CerDIP (C4)
	0°C to +70°C — Commercial Screening					
25 ns	L10C11PC25	L10C11DC25	L10C11CC25	L10C11NC25	L10C11HC25	L10C11IC25
	–55°C to +125°C — Commercial Screening					
30 ns		L10C11DM30	L10C11CM30		L10C11HM30	L10C11IM30
	–55°C to +125°C — Extended Screening					
30 ns		L10C11DME30	L10C11CME30		L10C11HME30	L10C11IME30
	–55°C to +125°C — MIL-STD-883 Compliant					
30 ns		L10C11DMB30	L10C11CMB30		L10C11HMB30	L10C11IMB30

5

Serial Scan Shadow Register — L29C818

FEATURES

- Octal Register with Additional 8-bit Shiftable Shadow Register
- Serial Load/Verify of Writable Control Store RAM
- Serial Stimulus/Observation of Sequential Logic
- High Speed, Low Power CMOS Technology
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with AMD Am29818
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C818** is a high-speed octal register designed especially for applications using serial-scan diagnostics or writable control store. It is pin and functionally compatible with the AMD Am29818 bipolar device.

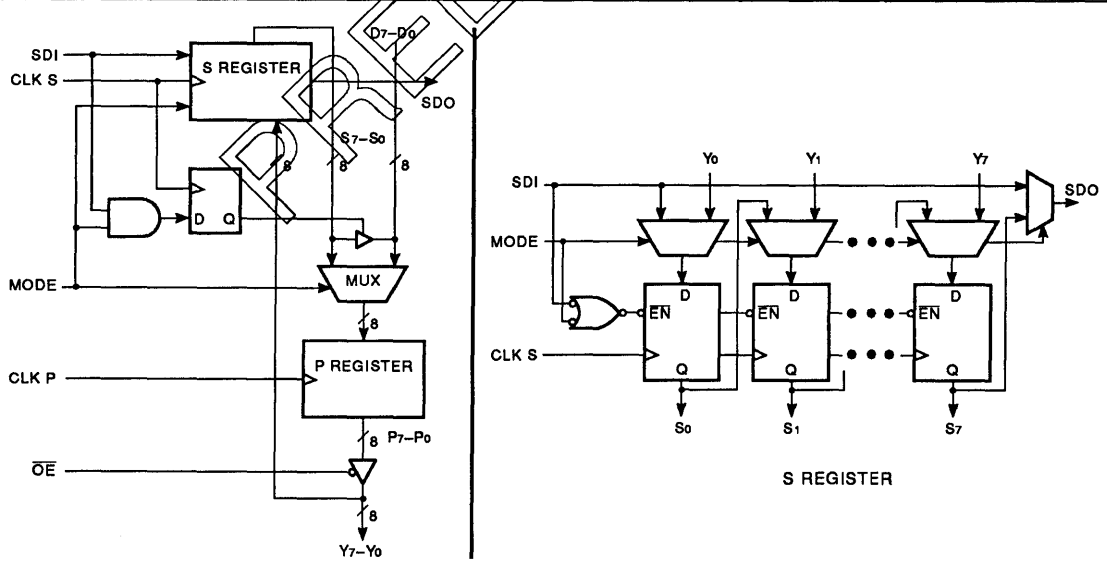
The L29C818 consists of an octal register (the "P" register), internally connected to an 8-bit shift register (the "S" register). Each has its own corresponding clock pin, and the P register has a three-state output control.

An input control signal MODE, in combination with the S register serial data input (SDI) pin controls data routing within the L29C818. When the MODE input is low, indicating normal operation, data present on the D_7–D_0 pins is loaded into the P register on the rising edge of CLK P. The contents of the P register are visible on the output pins Y_7–Y_0 when the $\overline{OE}$ control line is low.

Also, data present on the SDI pin is loaded into the least significant position of the S register on the rising edge of CLK S. In this mode, the S register performs a right shift operation, with the contents of each bit position replaced by the value in the next least significant location. The value in S_7 is shifted out on the serial data output (SDO) pin. The SDI and SDO pins allow serial connection of multiple L29C818 devices into a diagnostic loop. When MODE is low, the operation of the P and S registers are completely independent and no timing relationship is enforced between CLK P and CLK S.

When MODE is high, the internal multiplexers route data between the S and P registers, and the Y port. The contents of the S register are loaded into the P register on the rising edge of CLK P. In diagnostic applications,

L29C818 Block Diagram



this allows a data value input via serial scan to be loaded into the active data path of the machine.

When the MODE pin is high, CLK S causes a parallel rather than serial load of the S register. In this mode, the S register is loaded from the Y_7–Y_0 pins at the rising edge of CLK S. This is useful in writable control store applications for readback of the control store via the serial path.

When MODE is high, the SDI pin is used as a control input to enable or disable the loading of the S register, and it also affects routing of the S register contents onto the D_7–D_0 outputs. When SDI is low, the S register is enabled for loading as above. When SDI is high however, CLK S is prevented from reaching the S register, and no load occurs. In order to allow the SDI pin to serve as an enable signal for all L29C818 devices in a serial configuration, special handling of the SDI input is required. When MODE is high, the SDI input drives the SDO output directly, bypassing the S register. This means that the SDI value will apply simultaneously to all L29C818s in a serial loop. However, to ensure proper operation of a given device, the user must ensure that the SDI setup time to CLK S is extended by the sum of the SDI to SDO delays of all previous devices in the serial path.

The D_7–D_0 port is normally used as the input port to the D register. For writable control store applications however, this port is connected to the I/O pins of the RAM used as a control store. In order to load this RAM through the serial path, it is necessary to drive the S register contents onto the D_7–D_0 pins. This is accomplished when MODE and SDI are high, and a CLK S rising edge occurs. Note from above that with SDI high, no loading of the S register occurs. However, a flip-flop is set which synchronously enables the D port output buffer. The D output remains enabled until the first rising edge of CLK S during which either SDI or MODE is low. Thus to load a control store RAM, data would be shifted in with MODE low. When an entire control store word was present in the serial S registers, the SDI and MODE pins are brought high for one or more cycles, preventing further shifting of the S registers and enabling the contents onto the D port for writing into the RAM.

To verify the contents of a control store RAM, the RAM is read into the D register in the normal fashion. Then, the D contents are transferred in parallel to the S register by driving MODE high with SDI low. Then, the S register contents are scanned out serially by returning MODE to low and applying CLK S pulses.

Table 1. Function Table

Inputs				Outputs		Action		
MODE	SDI	CLK S	CLK P	P REG	S REG	Y_7–Y_0	D_7–D_0	SDO
0	X	↑	X	N/A	SHIFT	Normal	Hi-Z	S_7
0	X	X	↑	LOAD D	N/A	Normal	Input	S_7
1	0	↑	X	N/A	LOAD Y	Input*	Hi-Z	SDI
1	1	↑	X	N/A	HOLD	Normal	Output	SDI
1	X	X	↑	LOAD S	N/A	Normal	Hi-Z	SDI

* If $\overline{OE}$ is 0, the P register value will be loaded into the S register. If $\overline{OE}$ is 1, a value may be applied externally to the Y_7–Y_0 pins.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –12.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — NORMAL REGISTER OPERATION

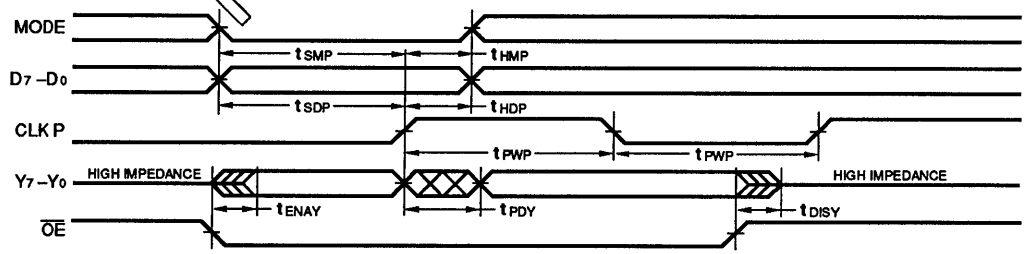
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-25 Min	L29C818-25 Max	L29C818- Min	L29C818- Max
t_{PDY}	CLK P to Y_7–Y_0		13		
t_{SDP}	D_7–D_0 to CLK P Setup	8			
t_{HDP}	CLK P to D_7–D_0 Hold	2			
t_{SMP}	MODE to CLK P Setup	15			
t_{HMP}	CLK P to MODE Hold	0			
t_{PWP}	CLK P Pulse Width	15			
t_{ENAY}	$\overline{OE}$ to Y_7–Y_0 Enable (Note 11)		25		
t_{DISY}	$\overline{OE}$ to Y_7–Y_0 Disable (Note 11)		15		

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-30 Min	L29C818-30 Max	L29C818- Min	L29C818- Max
t_{PDY}	CLK P to Y_7–Y_0		18		
t_{SDP}	D_7–D_0 to CLK P Setup	10			
t_{HDP}	CLK P to D_7–D_0 Hold	2			
t_{SMP}	MODE to CLK P Setup	15			
t_{HMP}	CLK P to MODE Hold	0			
t_{PWP}	CLK P Pulse Width	15			
t_{ENAY}	$\overline{OE}$ to Y_7–Y_0 Enable (Note 11)		30		
t_{DISY}	$\overline{OE}$ to Y_7–Y_0 Disable (Note 11)		20		

SWITCHING WAVEFORMS — NORMAL REGISTER OPERATION



SWITCHING CHARACTERISTICS — SERIAL SHIFT OPERATION

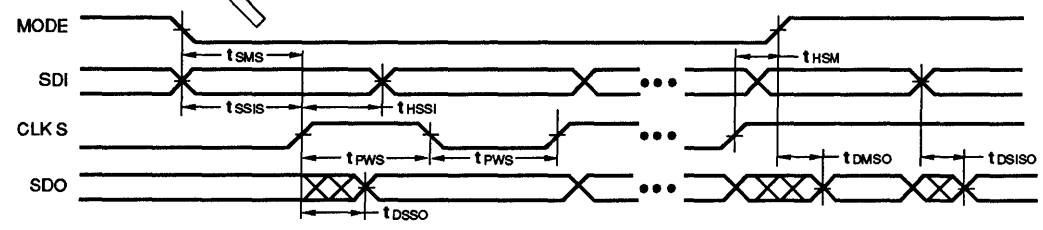
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818-			
		25			
Symbol	Parameter	Min	Max	Min	Max
t_{DSSO}	CLK S to SDO		25		
t_{SSIS}	SDI to CLK S Setup	10			
t_{HSSI}	CLK S to SDI Hold	0			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	2			
t_{PWS}	CLK S Pulse Width	25			
t_{DMSO}	MODE to SDO	16			
t_{DSISO}	SDI to SDO	16			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818-			
		30			
Symbol	Parameter	Min	Max	Min	Max
t_{DSSO}	CLK S to SDO		30		
t_{SSIS}	SDI to CLK S Setup	12			
t_{HSSI}	CLK S to SDI Hold	0			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	5			
t_{PWS}	CLK S Pulse Width	25			
t_{DMSO}	MODE to SDO	18			
t_{DSISO}	SDI to SDO	18			

SWITCHING WAVEFORMS — SERIAL SHIFT OPERATION



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SWITCHING CHARACTERISTICS — PIPELINE LOAD FROM SHADOW

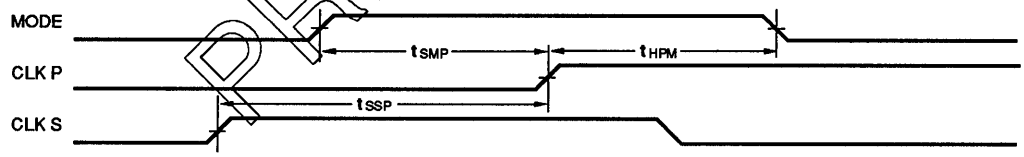
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 25 Min	Max	Min	Max
t_{SMP}	MODE to CLK P	15			
t_{HPM}	CLK P to MODE Hold	0			
t_{SSP}	CLK S to CLK P	10			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 30 Min	Max	Min	Max
t_{SMP}	MODE to CLK P	15			
t_{HPM}	CLK P to MODE Hold	0			
t_{SSP}	CLK S to CLK P	15			

SWITCHING WAVEFORMS — PIPELINE LOAD FROM SHADOW



SWITCHING CHARACTERISTICS — SHADOW LOAD FROM 'Y' PORT

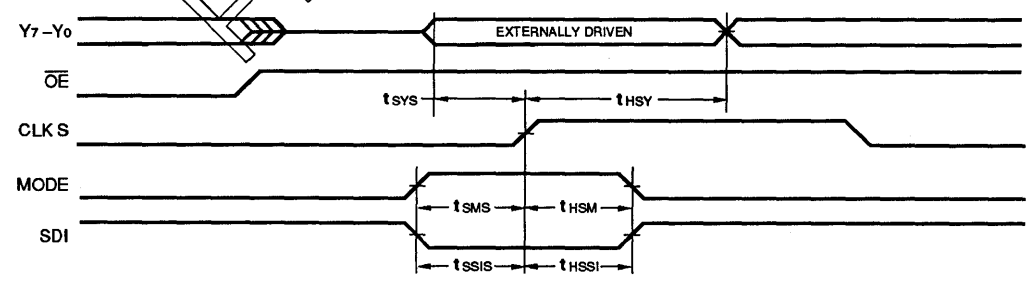
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-25 Min	L29C818-25 Max	L29C818- Min	L29C818- Max
t_{SYS}	Y_7–Y_0 to CLK S Setup	5			
t_{HSY}	CLK S to Y_7–Y_0 Hold	5			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	2			
t_{SSIS}	SDI to CLK S Setup	10			
t_{HSSI}	CLK S to SDI Hold	0			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-30 Min	L29C818-30 Max	L29C818- Min	L29C818- Max
t_{SYS}	Y_7–Y_0 to CLK S Setup	5			
t_{HSY}	CLK S to Y_7–Y_0 Hold	5			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	5			
t_{SSIS}	SDI to CLK S Setup	12			
t_{HSSI}	CLK S to SDI Hold	0			

SWITCHING WAVEFORMS — SHADOW LOAD FROM 'Y' PORT



SWITCHING CHARACTERISTICS — SHADOW READ VIA 'D' PORT

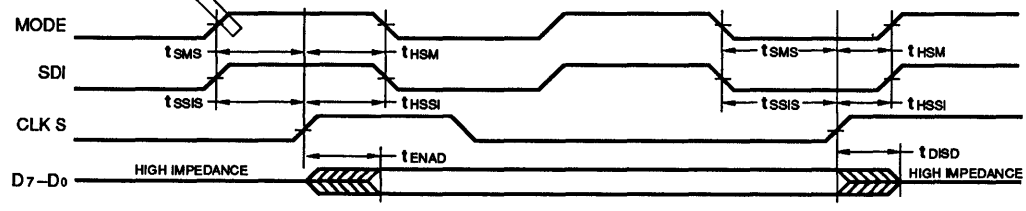
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-25 Min	L29C818-25 Max	L29C818- Min	L29C818- Max
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	2			
t_{SSIS}	SDI to CLK S Setup	10			
t_{HSSI}	CLK S to SDI Hold	0			
t_{ENAD}	CLK S TO D7–D0 Enable (Note 11)	85			
t_{DISD}	CLK S TO D7–D0 Disable (Note 11)	30			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-30 Min	L29C818-30 Max	L29C818- Min	L29C818- Max
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	5			
t_{SSIS}	SDI to CLK S Setup	12			
t_{HSSI}	CLK S to SDI Hold	0			
t_{ENAD}	CLK S TO D7–D0 Enable (Note 11)	90			
t_{DISD}	CLK S TO D7–D0 Disable (Note 11)	35			

SWITCHING WAVEFORMS — SHADOW READ VIA 'D' PORT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

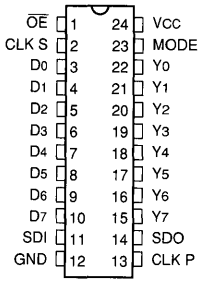
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

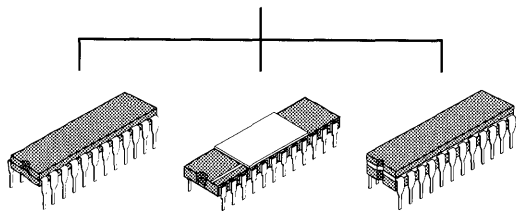
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

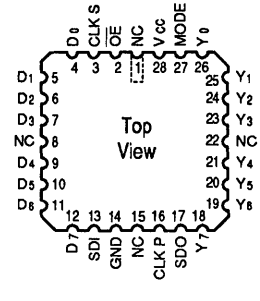
ORDERING INFORMATION

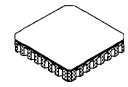
24-pin
(0.3" wide)





28-pin





Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Ceramic Leadless Chip Carrier (K1)	
	0°C to +70°C — COMMERCIAL SCREENING				
25 ns	L29C818PC25	L29C818DC25	L29C818CC25	L29C818KC25	
	–55°C to +125°C — COMMERCIAL SCREENING				
30 ns		L29C818DM30	L29C818CM30	L29C818KM30	
	–55°C to +125°C — EXTENDED SCREENING				
30 ns		L29C818DME30	L29C818CME30	L29C818KME30	
	–55°C to +125°C — MIL-STD-883 COMPLIANT				
30 ns		L29C818DMB30	L29C818CMB30	L29C818KMB30	

8 x 8-bit Three Port Register File — LRF07

FEATURES

- 8-word x 8-bit Three Port Memory
- Independently Addressable Ports: 1 Input, 1 Output, 1 Bidirectional
- High Speed, Low Power CMOS Technology
- Internally Latched Control Bits
- High Speed Scratchpad Memory with Overlapped Data Fetch/Store
- Fully TTL Compatible
- 60 mW Typical Power Dissipation
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Sidebraze, Hermetic DIP
  - 44-pin Ceramic LCC (Type C)

DESCRIPTION

The **LRF07** is an 8-word x 8-bit expandable register file with three independently addressable ports, designated A, B, and C. Each port has eight data lines, three address lines, and a port enable control. All address and control lines are registered to facilitate instruction pipelining in microprogrammed systems. All ports may be used simultaneously in any clock cycle.

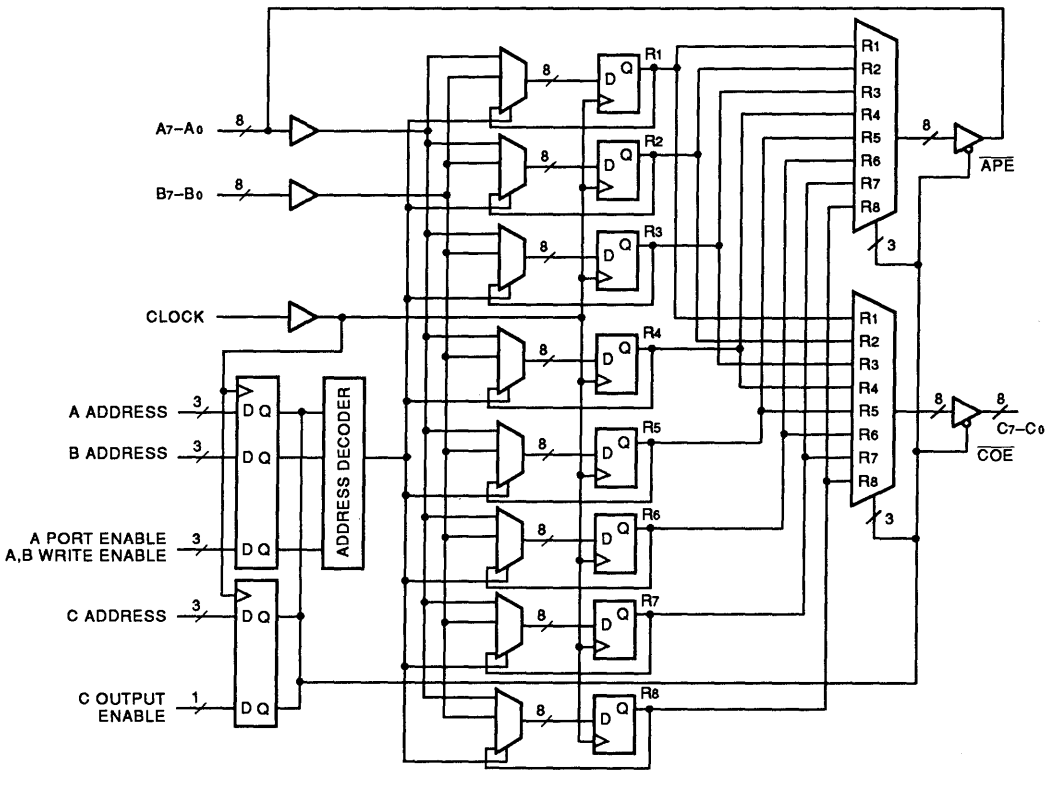
The C port is a read only port. C port address lines (CA_2–CA_0) are latched at the rising edge of the clock. The data indicated by the respective port address will be presented on the output lines one t_{ACC} following the clock edge on which the address is latched. If the same register is simultaneously addressed for writing from a different port, the data presented to the outputs is the contents of the register prior to the write operation.

The B port is a write port. B port address lines (BA_2–BA_0) are latched at the rising edge of the clock. The contents of the B address register are decoded to control data routing multiplexers. These supply data from the input pins to the desired register. Data meeting the setup time is latched into the addressed register on the clock edge following the one which latched the address.

The A port is a bidirectional port. The A Read/Write (AR/$\overline{W}$) control is latched along with the address lines

5

LRF07 Block Diagram



(AA_2–AA_0) and determines whether the A port acts as an input or an output during any clock period. When AR/$\overline{W}$ is a '1' at the clock edge, the A port presents the addressed data on the A_7–A_0 data lines. A port read operations are thus performed identically to C port reads. When AR/$\overline{W}$ is a '0' at the clock edge, A port writes are executed in the same manner as B port writes, with the data latched on the clock edge following application of the corresponding address.

All ports have associated port enable inputs. These inputs are internally registered and are applied simultaneously with the corresponding port address. In the case of the C port, the $\overline{COE}$ input is a three state output control. A '1' at these inputs places the corresponding data lines in a high impedance state beginning one t_{DIS} following the clock edge. The B port enable $\overline{BWE}$ serves as a registered write enable input. A '1' latched on these inputs disables write operations from the port on the following clock edge. The A port enable $\overline{APE}$, serves the dual function of write enable or three state enable depending on the direction of the A port.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2.0	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

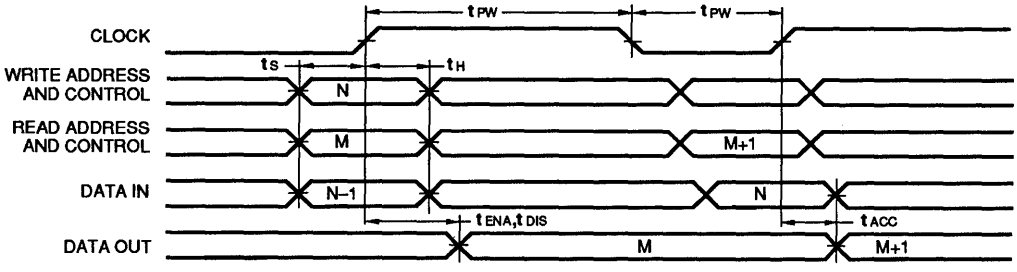
Symbol	Parameter	LRF07-35 Min	LRF07-35 Max
t_{ACC}	CLK to Output		35
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		25
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		35
t_{PW}	Clock Pulse Width	25	
t_S	Input Setup Time	15	
t_H	Input Hold Time	5	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LRF07-40 Min	LRF07-40 Max
t_{ACC}	CLK to Output		40
t_{DIS}	$\overline{OE}$ to Output Disable (Note 11)		30
t_{ENA}	$\overline{OE}$ to Output Enable (Note 11)		35
t_{PW}	Clock Pulse Width	25	
t_S	Input Setup Time	15	
t_H	Input Hold Time	5	

5

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

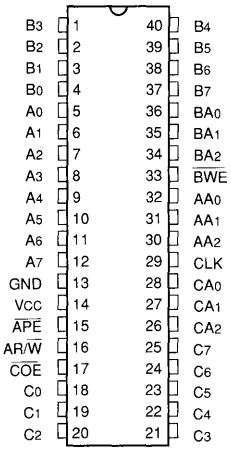
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

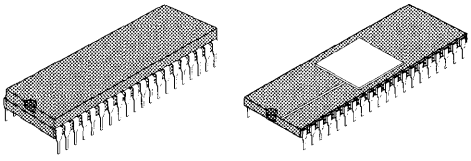
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

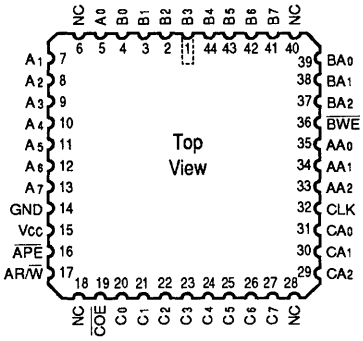
ORDERING INFORMATION

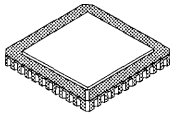
40-pin





44-pin





Speed	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Ceramic Leadless Chip Carrier (K2)	
	0°C to +70°C — COMMERCIAL SCREENING			
35 ns	LRF07PC35	LRF07DC35	LRF07KC35	
	–55°C to +125°C — COMMERCIAL SCREENING			
40 ns		LRF07DM40	LRF07KM40	
	–55°C to +125°C — EXTENDED SCREENING			
40 ns		LRF07DME40	LRF07KME40	
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
40 ns		LRF07DMB40	LRF07KMB40	

5

16-bit Cascadable ALU — L4C381

FEATURES

- High Speed (26 ns), Low Power 16-bit Cascadable ALU
- Implements Add, Subtract, Accumulate, Two's Complement, Pass, and Logic Operations
- All Registers Have a Bypass Path for Complete Flexibility
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Pin Grid Array
  - 68-pin Ceramic LCC (Type C)

DESCRIPTION

The **L4C381** is a flexible, high speed, cascadable 16-bit Arithmetic and Logic Unit implemented in CMOS technology. It combines four 381-type 4-bit ALUs, a look-ahead carry generator, and miscellaneous interface logic — all in a single 68-pin package. While containing new features to support high speed pipelined architectures and single 16-bit bus configurations, the L4C381 retains full performance and functional compatibility with the bipolar '381 designs.

Architecture

The L4C381 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided to support cascading to longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs, accommodating chain operations and accumulation. Furthermore, the A or B input can be forced to Zero allowing unary functions on either operand.

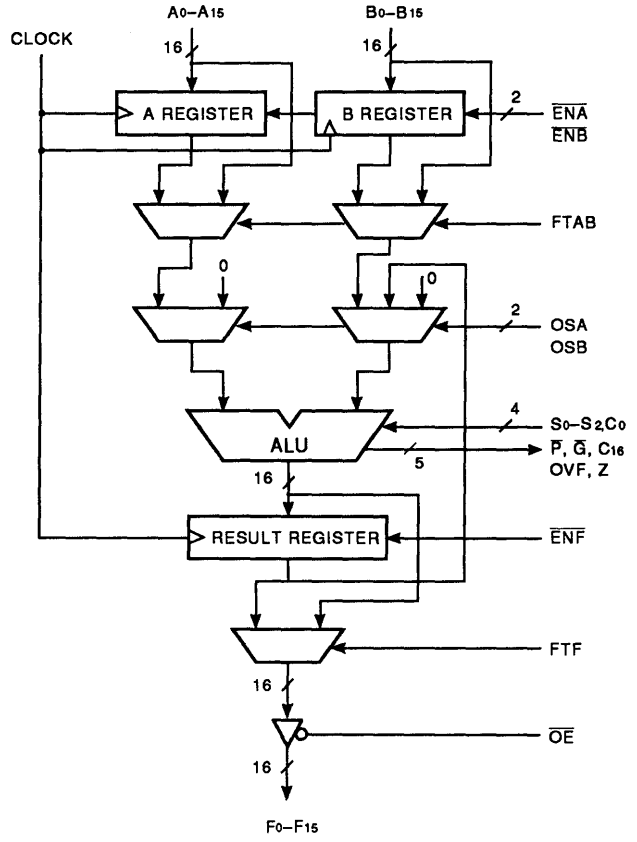
ALU Operations

The S_0–S_2 lines specify the operation to be performed. The ALU functions and their select codes are shown below.

S_2	S_1	S_0	Function
0	0	0	CLEAR (F=00 ... 0)
0	0	1	NOT (A) + B
0	1	0	A + NOT (B)
0	1	1	A + B
1	0	0	A XOR B
1	0	1	A OR B
1	1	0	A AND B
1	1	1	PRESET (F=11 ... 1)

The functions B minus A and A minus B can be achieved by setting the carry input of the least significant slice and selecting codes 001 and 010 respectively.

L4C381 Block Diagram



ALU Status

The ALU provides Overflow and Zero status bits. Carry, Propagate, and Generate outputs are also provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all 16 output bits are zero. The Generate, Propagate, C_{16}, and OVF flags for the A + B operation are defined in Table 1. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing A_i and B_i respectively in Table 1.

TABLE 1. ALU STATUS FLAGS

Bit Carry Generate = $g_i = A_iB_i$, for i = 0 ... 15
Bit Carry Propagate = $p_i = A_i + B_i$, for i = 0 ... 15

$P_0 = p_0$
$P_i = p_i (P_{i-1})$ for i = 1 ... 15

and

$G_0 = g_0$
$G_i = g_i + p_i (G_{i-1})$ for i = 1 ... 15
$C_i = G_{i-1} + P_{i-1} (C_0)$ for i = 1 ... 15

then

$\overline{G} = \text{NOT}(G_{15})$
$\overline{P} = \text{NOT}(P_{15})$
$C_{16} = G_{15} + P_{15}C_0$
$\text{OVF} = C_{15} \text{ XOR } C_{16}$

Operand Registers

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. Each register is independently enabled by control signals $\overline{\text{ENA}}$ and $\overline{\text{ENB}}$.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line. When the FTAB control is asserted, data is routed around the A and B input registers; however, they continue to function normally via the $\overline{\text{ENA}}$ and $\overline{\text{ENB}}$ controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

Output Register

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. The output register is enabled by the $\overline{\text{ENF}}$ control signal. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{\text{OE}}$ input allow the L4C381 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal. When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{\text{ENF}}$ control. The contents of the output register will again be available on the output pins if FTF is released. With both FTAB and FTF true (high) the L4C381 is functionally identical to four cascaded 54S381-type devices.

Operand Selection

The two operand select lines OSA and OSB control multiplexers that precede the ALU inputs. These multiplexers provide an operand force-to-zero function as well as F register feedback to the B input. Table 2 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

When both operand select lines are low, the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OSA true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FTF control. That is, the F outputs of the L4C381 may be driven directly by the ALU (FTF = true). The output register continues to function, however, and provides the ALU B operand source.

TABLE 2. OPERAND SELECTION CONTROL

OSB	OSA	Operand B	Operand A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C) *(ns) Notes 9, 10*

GUARANTEED MAXIMUM COMBINATIONAL DELAYS

From Input \ To Output	L4C381-55				L4C381-40				L4C381-26			
	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_0–S_2, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_0–S_2, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A_0–A_{15}, B_0–B_{15}	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_0–S_2, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A_0–A_{15}, B_0–B_{15}	55	36	46	37	40	30	40	32	26	22	22	22
Clock (OSA,B=0)	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_0–S_2, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE

Input	L4C381-55				L4C381-40				L4C381-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_0–A_{15}, B_0–B_{15}	8	2	35	2	8	2	28	2	8	2	16	2
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_0–S_2, OSA, OSB	44	0	44	0	32	0	32	0	18	0	18	0
ENA, ENB, ENF	10	2	10	2	10	2	10	2	8	2	8	2

THREE STATE ENABLE/DISABLE TIMES *(Note 11)*

	L4C381-55	L4C381-40	L4C381-26
t_{EN}	20	18	16
t_{DIS}	20	18	16

CLOCK CYCLE TIME AND PULSE WIDTH

	L4C381-55	L4C381-40	L4C381-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C) *(ns) Notes 9, 10*

GUARANTEED MAXIMUM COMBINATIONAL DELAYS

To Output / From Input	L4C381-65				L4C381-45				L4C381-30			
	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}	F_0–F_{15}	P,G	OVF,Z	C_{16}
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_0–S_2, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_0–S_2, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A_0–A_{15}, B_0–B_{15}	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_0–S_2, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A_0–A_{15}, B_0–B_{15}	65	44	56	44	45	32	46	36	30	28	28	28
Clock (OSA,B=0)	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_0–S_2, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE

Input	L4C381-65				L4C381-45				L4C381-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_0–A_{15}, B_0–B_{15}	10	3	43	3	8	3	33	3	8	3	20	3
C_0	25	0	25	0	20	0	20	0	12	0	12	0
S_0–S_2, OSA, OSB	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	12	2	12	2	10	2	10	2	10	2	10	2

THREE STATE ENABLE/DISABLE TIMES *(Note 11)*

	L4C381-65	L4C381-45	L4C381-30
t_{EN}	22	20	18
t_{DIS}	22	20	18

CLOCK CYCLE TIME AND PULSE WIDTH

	L4C381-65	L4C381-45	L4C381-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

CASCADING THE L4C381

Cascading the L4C381 to 32 bits is accomplished simply by connecting the C_{16} output of the least significant slice to the C_0 input of the most significant slice. The S_0–S_2, OSA, OSB, $\overline{ENA}$, $\overline{ENB}$, and $\overline{ENF}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C_{16} outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C_{16} output of the lower slice. Add this number to the delay from the C_0 input of the upper slice to the output of interest (of the C_0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C_{16} output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figures 1a through 1d.

Cascading to greater than 32 bits can be accomplished in two ways: The simplest (but slowest) method is to simply connect the C_{16} output of each slice to the C_0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C_0 to C_{16} delays for all intermediate slices must be added to the overall delay for each path. A faster method is to use an external carry-lookahead generator. The $\overline{P}$ and $\overline{G}$ outputs of each slice are connected as inputs to the CLA generator, which in turn produces the C_0 inputs for each slice except the least significant. The C_{16} outputs are not used in this case, except for the most significant one, which is the carry out of the overall system. The carry in to the system is connected to the C_0 input of the least significant slice, and also to the carry lookahead generator. Propagation delays for this configuration are the sum of the time to $\overline{P}$, $\overline{G}$, for the least significant slice, the propagation delay of the carry lookahead generator, and the C_0 to output time of the most significant slice.

5

FIGURE 1A. FTAB = 0; FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_0–S_2, OSA, OSB	→ Other	=	(S_0–S_2, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_0–S_2, OSA, OSB	Setup time	=	(S_0–S_2, OSA, OSB → C_{16}) + C_0 Setup
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

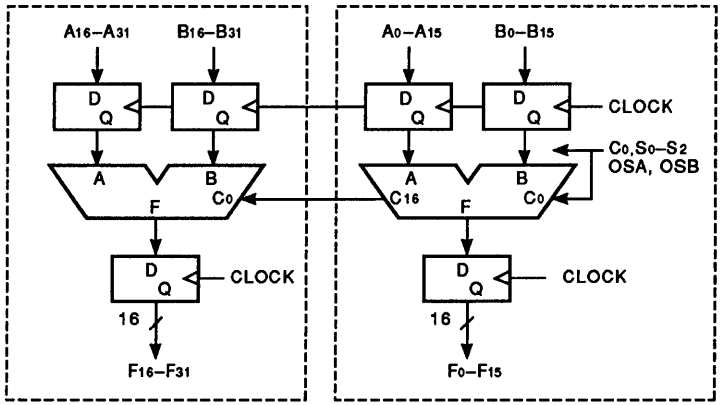


FIGURE 1B. FTAB = 0; FTF = 1

From	To		Calculated Specification Limit
Clock	→ F	=	(Clock → C_{16}) + (C_0 → F)
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ F	=	(C_0 → C_{16}) + (C_0 → F)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_0–S_2, OSA, OSB	→ F	=	(S_0–S_2, OSA, OSB → C_{16}) + (C_0 → F)
S_0–S_2, OSA, OSB	→ Other	=	(S_0–S_2, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_0–S_2, OSA, OSB	Setup time	=	(S_0–S_2, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

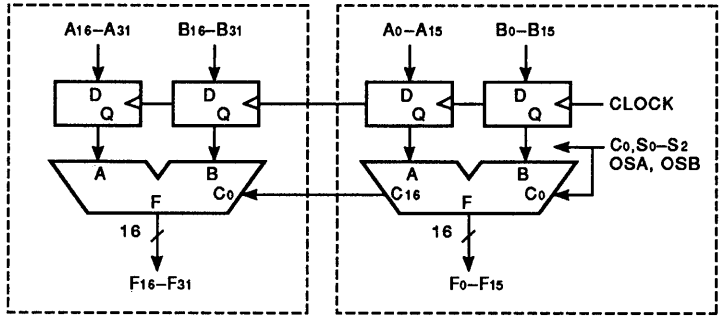


FIGURE 1C. FTAB = 1; FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time)
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)

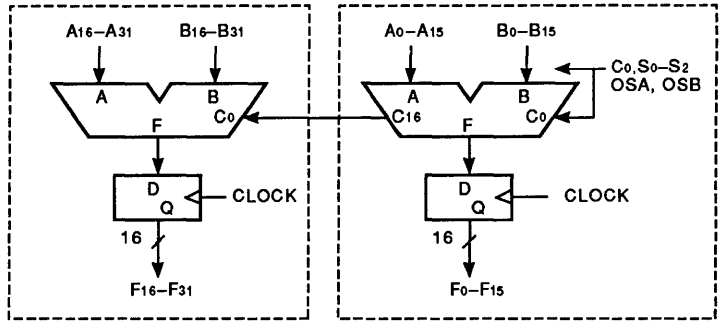
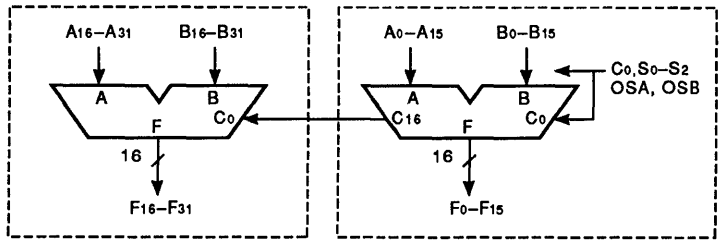


FIGURE 1D. FTAB = 1; FTF = 1

From	To		Calculated Specification Limit
A, B	→ F	=	(A, B → C16) + (C0 → F)
A, B	→ Other	=	(A, B → C16) + (C0 → Out)
C0	→ F	=	(C0 → C16) + (C0 → F)
C0	→ Other	=	(C0 → C16) + (C0 → Out)
S0–S2, OSA, OSB	→ F	=	(S0–S2, OSA, OSB → C16) + (C0 → F)
S0–S2, OSA, OSB	→ Other	=	(S0–S2, OSA, OSB → C16) + (C0 → Out)
A, B	Setup time	=	(A, B → C16) + (C0 Setup time)
C0	Setup time	=	(C0 → C16) + (C0 Setup time
S0–S2, OSA, OSB	Setup time	=	(S0–S2, OSA, OSB → C16) + (C0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C16) + (C0 Setup time)



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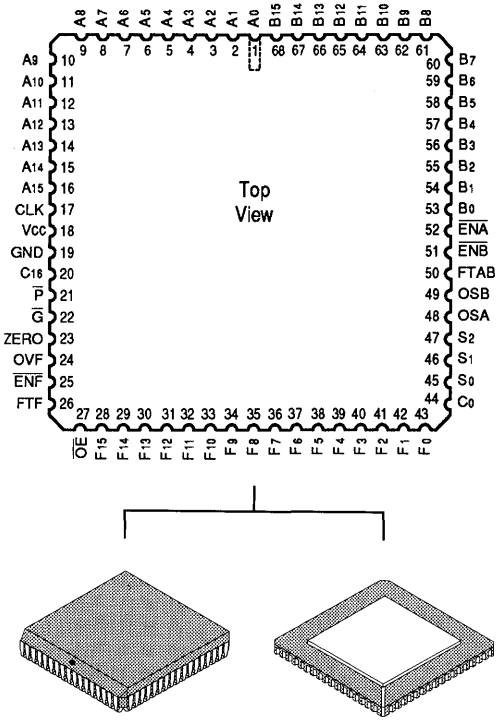
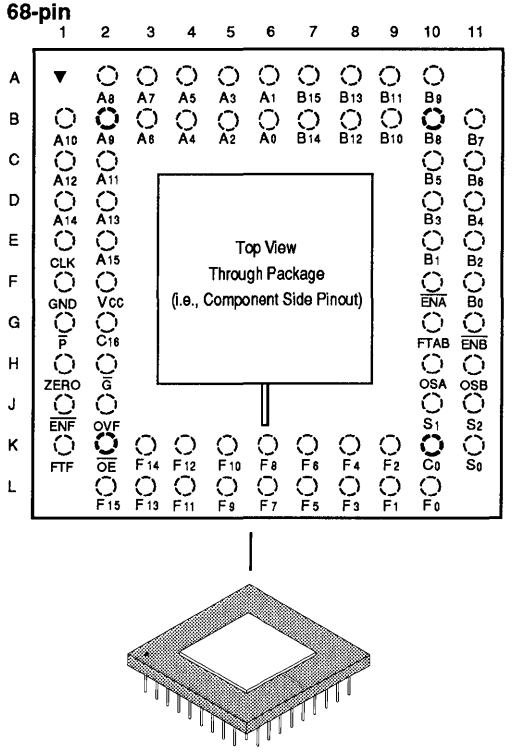
ORDERING INFORMATION

68-pin



68-pin



Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
55 ns	L4C381JC55	L4C381KC55	L4C381GC55
40 ns	" " 40	" " 40	" " 40
26 ns	" " 26	" " 26	" " 26
	–55°C to +125°C — Commercial Screening		
65 ns		L4C381KM65	L4C381GM65
45 ns		" " 45	" " 45
30 ns		" " 30	" " 30
	–55°C to +125°C — Extended Screening		
65 ns		L4C381KME65	L4C381GME65
45 ns		" " 45	" " 45
30 ns		" " 30	" " 30
	–55°C to +125°C — MIL-STD-883 Compliant		
65 ns		L4C381KMB65	L4C381GMB65
45 ns		" " 45	" " 45
30 ns		" " 30	" " 30

16-bit ALU Slice — L29C101

FEATURES

- Four-Wide 2910 ALU Plus Carry Look-ahead Logic and Full 16-bit Data Paths
- High Speed, Low Power CMOS Technology
- Fast Clock Period:
  35 ns Commercial, 45 ns Military
- Available 100% Screened to MIL-STD-883, Class B
- Functionally Equivalent to AMD AM29C101 and Cypress CY7C9101
- Package Styles Available:
  - 64-pin Plastic DIP
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Pin Grid Array

DESCRIPTION

The **L29C101** is a high- performance, expandable, 16-bit Arithmetic Logic Unit slice manufactured using CMOS technology. Completely code compatible with its 4-bit predecessors, the part can be used to implement the arithmetic section of central processors or many types of programmable controllers.

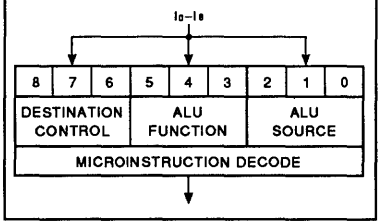
The microinstruction set of the L29C101 is straightforward, yet versatile enough so that the part can be used to emulate the ALU operations of most digital computers.

The L29C101 is comprised of functions equivalent to four 2901 bit-slice ALU's plus the 2902 carry look-ahead logic, all in a single 64-pin device.

Included are a 16-word by 16-bit dual-port register file, a 16-bit 8-function ALU, 16-bit shifters, and all the necessary decoding and control logic.

All status, shift linkage, and carry functions are cascadable to allow construction of architectures wider than

L29C101 Instruction Decoding



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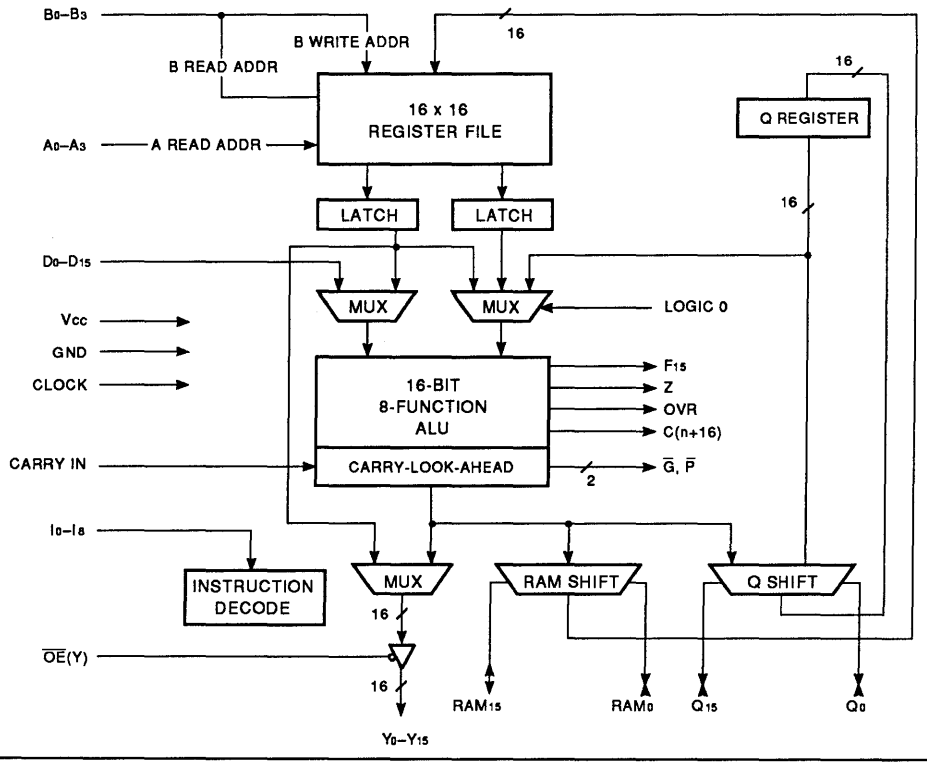
L29C101 Block Diagram



16-bits if desired. Expanded designs can take advantage of full carry-look-ahead for improved performance.

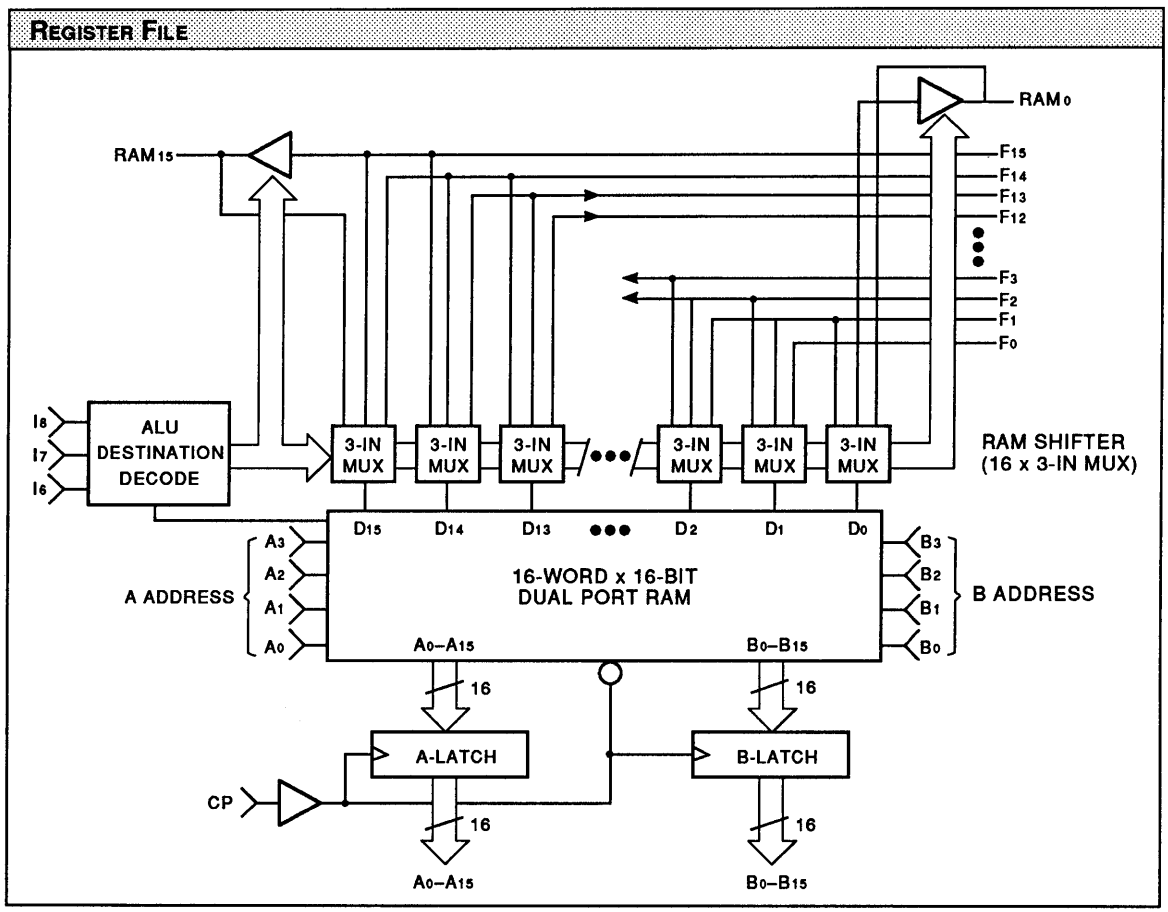
The L29C101 is fully pin and function compatible with the Am29C101. The L29C101 is available in High-Rel versions that are fully compliant with MIL-STD-883C, class B.

L29C101 Architecture

A typical execution cycle for the L29C101 consists of reading two operands simultaneously from the two-port register file, performing an ALU operation on these operands, and returning the result to the file. This entire operation can be completed in a single clock cycle, providing high performance and simple microcode. Optionally, the ALU operands may be sourced by the external data port, an auxiliary register denoted the Quotient or "Q" register, or forced to zero under instruction control. Also, the data returned to the register file and the Q register may be shifted one bit in either direction to aid multiplication and division operations.

Register File

The two-port register file has a capacity of 16 words of 16 bits each. The A-port address (A0–A3) specifies the register to be read from the A-port, and the B-port address (B0–B3) specifies the register to the read from the B-port. Both A and B addresses may be the same, in which case identical data will appear at both A and B ports. In addition, the B-port address can specify a register location for writing. Data from the locations indicated by the A and B addresses are read from the register file during the low period of the clock. The data is applied to two latches which are transparent during the clock low period, and hold their state during the clock high period. The purpose of these latches is to hold the A and B ALU operands constant while a computation result is written back to the register file at the B address. This allows for a read-modify-write cycle, which is useful in applications such as accumulation. Under control of the



Result Destination Field (I_6, I_8), data to be written to the register file is stored into the register addressed by the B field on the rising edge of the clock.

ALU Control

The ALU is capable of performing eight operations. These functions are described in Table 2. The control inputs I_3–I_5 select one of three arithmetic or five logical operations to be performed on the input operands. The integral carry-lookahead circuitry across all 16 ALU bits is functionally equivalent to the 2902 carry-look-ahead unit and provides significant speed advantages.

In the arithmetic mode, the ALU result is also a function of the Carry In input. When executing ALU Add or Subtract instructions, setting the C(n) input to '1' causes the addition of '1' to the result. Thus for 2's complement operations, C(n) of the least significant slice would be set to zero for addition, and to '1' for subtraction. This is because the L29C101 ALU naturally implements 1's complement subtraction, that is, a bitwise complement of one of the operands. In order to achieve a 2's complement result, a '1' must be added in the least significant position. This is accomplished using C(n). PASS and Negate operations are also available by combining arithmetic instructions (Add, Subtract) with any of the operand source options which set one operand to zero. Tables 5 and 6 show the detailed ALU logic and arithmetic functions and the operands selected. Table 5 includes ALU function selection.

Operand Source Control

As shown in the figure below, each of the ALU operands is supplied by a multiplexer, which allows significant flexibility in the selection of the operand source. The two 16-bit ALU inputs are denoted R and S. The R operand may be sourced by the A read port of the register file, from the D input pins, or may be forced to zero. The S operand may be sourced by the B read port of the register file, the A read port, (when the R operand is D or zero), the Q register, or forced to zero. Control of the operand selection multiplexers is encoded into control field I_2–I_0, as described in Table 1.

Result Destination Control

The instruction field I_6–I_8 is encoded to control the routing of the ALU

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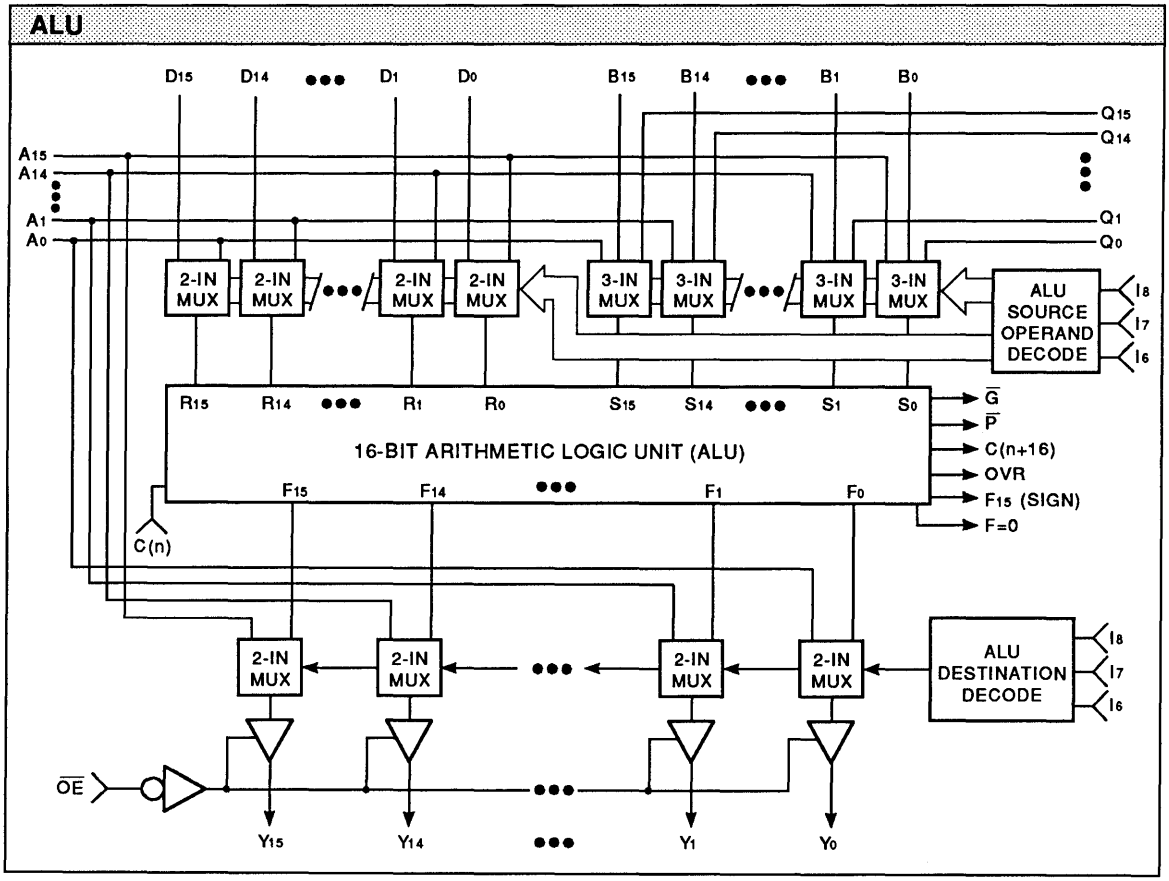

result field, denoted F, and the Q register contents. The encoding is defined in Table 3. Under instruction control, the ALU result can be stored in the register file, the Q register, or both. A No Operation capability is also provided during which the result is not stored in either location. This field also controls the value presented at the Y_0–Y_{15} outputs. These outputs generally reflect the ALU result F, but for one of the instruction decodes are driven by the A port value read from the register file. This provides the capability to read data from the register file while simultaneously performing an ALU operation. This is useful in applications such as postincrement address generation, for example.

In addition to destination control, up or down shifting of both the register file and Q register load values are controlled by the I_6–I_8 field. Each can be up or down shifted one position prior to storing in the destination register. The RAM_0 or Q_0 pins output the least significant bit of the value being stored for downshifts, and accept the bit to be stored in the least signficant position for upshifts. Similarly, the RAM_{15} or Q_{15} pins output the most significant bit for upshifts, and accept the bit to be stored in the most significant position for downshifts. Table 3 gives the various shift actions and data destinations controlled by the I_6–I_8 inputs.

Q-Register

The Q-register is intended primarily for use as a separate working register for multiplication and division routines but it also serves as an accumulator or for temporary storage. The Q register is loaded via a multiplexer, which allows either up or downshift of the Q register contents, or an unshifted load of the Q register with the ALU result.

Status Outputs

The $\overline{G}$ and $\overline{P}$ outputs are low-true Carry Generate and Carry Propagate signals. They are used in conjunction with an external carry-lookahead generator when cascading L29C101 slices beyond 32 bits. The C(n+16) is the Carry Out signal, which can be directly connected to the C(n) input of another L29C101 to implement a 32-bit system. The OVR output indicates 2's complement overflow for addition and subtraction. The logical definitions of the $\overline{G}$, $\overline{P}$, C(n+16), and OVR signals are given in Table 7.

The MSB of the ALU result (F_{15}) is provided so that the sign bit may be examined easily. The $\overline{Z}$ output is used for zero detection and is high when all of the F output bits are low. It is an open drain output which may be wire OR'ed across multiple slices.

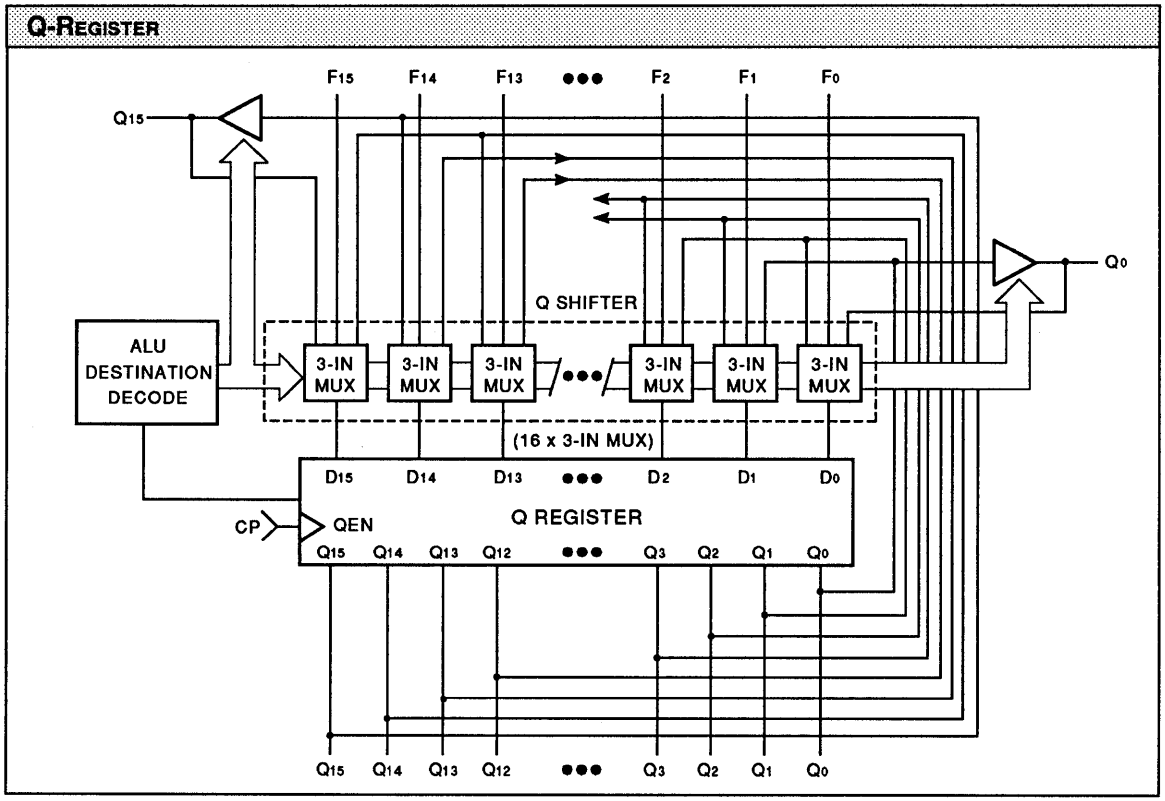

TABLE 1. ALU SOURCE OPERAND CONTROL

Mnemonic	Micro Code				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

TABLE 2. ALU FUNCTION CONTROL

Mnemonic	Micro Code				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	$\overline{R}$ OR S	
AND	H	L	L	4	R AND S	
NOTRS	H	L	H	5	R AND S	
EXOR	H	H	L	6	R EX-OR S	
EXNOR	H	H	H	7	R EX-NOR S	

TABLE 3. ALU DESTINATION CONTROL

Mnemonic	Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
	I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN_0	F_{15}	X	Q_{15}

TABLE 4. SOURCE OPERAND AND ALU FUNCTION MATRIX

Octal I_{543}	I_{210} →	0	1	2	3	4	5	6	7
	ALU Function	ALU Source							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C(n) = L R plus S C(n) = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C(n) = L S minus R C(n) = H	Q – A – 1 Q – A	B – A – 1 B – A	Q – 1 Q	B – 1 B	A – 1 A	A – D – 1 A – D	Q – D –1 Q – D	– D – 1 – D
2	C(n) = L R minus S C(n) = H	A – Q – 1 A – Q	A – B – 1 A – B	– Q –1 – Q	– B – 1 – B	– A – 1 – A	D – A – 1 D – A	D – Q – 1 D – Q	D – 1 D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	$\overline{A}$∧Q	0	0	0	$\overline{D}$∧A	$\overline{D}$∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	A∧B	Q	B	A	D∧A	D∧Q	0
6	R EX-OR S	A∀Q	A∀B	Q	B	A	D∀A	D∀Q	D
7	R EX-NOR S	$\overline{A∀Q}$	$\overline{A∀B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D∀A}$	$\overline{D∀Q}$	$\overline{D}$

TABLE 5. ALU LOGIC MODE FUNCTIONS

Octal I543, I210	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee A$
60	EX – OR	$A \forall Q$
61		$A \forall B$
65		$D \forall A$
66		$D \forall Q$
70	EX – NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{R}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	ZERO	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

TABLE 6. ALU ARITHMETIC MODE FUNCTIONS

Octal I543, I210	C(n) = 0 (Low)		C(n) = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD Plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q – 1	PASS	Q
13		B – 1		B
14		A – 1		A
27		D – 1		D
22	1's Comp.	– Q – 1	2's Comp. (Negate)	– Q
23		– B – 1		– B
24		– A – 1		– A
17		– D – 1		– D
10	Subtract (1's Comp.)	Q – A – 1	Subtract (2's Comp.)	Q – A
11		B – A – 1		B – A
15		A – D – 1		A – D
16		Q – D – 1		Q – D
20		A – Q – 1		A – Q
21		A – B – 1		A – B
25		D – A – 1		D – A
26		D – Q – 1		D – Q

TABLE 7. LOGIC FUNCTIONS FOR CARRY AND OVERFLOW CONDITIONS

I543	Function	P	G	C (n+16)	OVR
0	R + S	$\overline{P_0 \cdot P_1 \cdots P_{15}}$	$\overline{G_{15} + P_{15} G_{14} + P_{15} P_{14} G_{13} + \ldots}$	C_{16}	$C_{16} \forall C_{15}$
1	S – R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R – S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$R \wedge S$				
5	$R \wedge S$				
6	$\overline{R} \forall S$				
7	$\overline{R \forall S}$				

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5.0	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C) *(ns) Note 9*

OUTPUT ENABLE/DISABLE TIMES (Note 11)

Device	Input	Output	tEN	tDIS
L29C101-35	$\overline{OE}$	Y	20	17

CYCLE TIME AND CLOCK CHARACTERISTICS

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	35 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	30 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	20 ns

COMBINATIONAL PROPAGATION DELAYS (Note 12)

From Input \ To Output	Y	F15	C (n16)	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15
A,B Address	46	43	35	37	49	41	40	—
D	34	34	27	27	40	29	33	—
C(n)	27	24	20	—	28	23	28	—
I0, I1, I2	40	40	33	30	42	32	35	—
I3, I4, I5	41	38	32	28	40	36	38	—
I6, I7, I8	20	—	—	—	—	—	26	26
A bypass ALU (I = 2XX)	26	—	—	—	—	—	—	—
Clock	38	34	30	30	36	32	34	25

SETUP AND HOLD TIMES RELATIVE TO CLOCK INPUT (Note 12)

Input	Setup Time Before H → L	Hold Time After H → L	Setup Time Before L → H	Hold Time After L → H
A,B Source Address (Notes 14, 15)	24	3	35	—
B Destination Address (Note 13)	24	←Do Not Change→		0
D	—	—	26	0
C(n)	—	—	16	0
I0, I1, I2	—	—	30	0
I3, I4, I5	—	—	31	0
I6, I7, I8 (Note 13)	10	←Do Not Change→		0
RAM0, RAM15, Q0, Q15	—	—	12	0

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C) *(ns) Note 9*

OUTPUT ENABLE/DISABLE TIMES (Note 11)

Device	Input	Output	tEN	tDIS
L29C101-45	$\overline{OE}$	Y	23	20

CYCLE TIME AND CLOCK CHARACTERISTICS

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	45 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	25 MHz
Minimum Clock LOW Time	20 ns
Minimum Clock HIGH Time	20 ns

COMBINATIONAL PROPAGATION DELAYS (Note 12)

From Input \ To Output	Y	F15	C (n16)	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0 RAM15	Q0 Q15
A,B Address	52	50	40	38	48	46	43	—
D	37	36	30	32	40	32	35	—
C(n)	30	28	24	—	29	27	30	—
I0, I1, I2	44	43	36	34	46	38	41	—
I3, I4, I5	47	44	35	35	45	44	45	—
I6, I7, I8	22	—	—	—	—	—	30	30
A bypass ALU (I = 2XX)	27	—	—	—	—	—	—	—
Clock	44	39	32	32	40	36	34	28

SETUP AND HOLD TIMES RELATIVE TO CLOCK INPUT (Note 12)

Input	Setup Time Before H → L	Hold Time After H → L	Setup Time Before L → H	Hold Time After L → H
A,B Source Address (Notes 14, 15)	22	3	40	—
B Destination Address (Note 13)	22	←Do Not Change→		0
D	—	—	30	0
C(n)	—	—	20	0
I0, I1, I2	—	—	37	0
I3, I4, I5	—	—	36	0
I6, I7, I8 (Note 13)	10	←Do Not Change→		0
RAM0, RAM15, Q0, Q15	—	—	12	2

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or GND, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turnon/turnoff times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and GND leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed be-tween device V_{CC} and the tester common, and device ground and tester common.

b. GND and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition for t_{EN} is measured ±200 mV from steady-state voltage with specified loading.

12. A dash indicates a propagation delay or setup time constraint that does not exist.

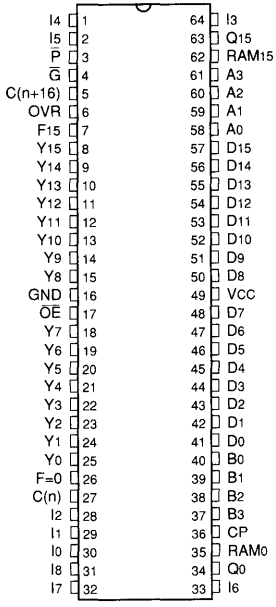
13. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."

14. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.

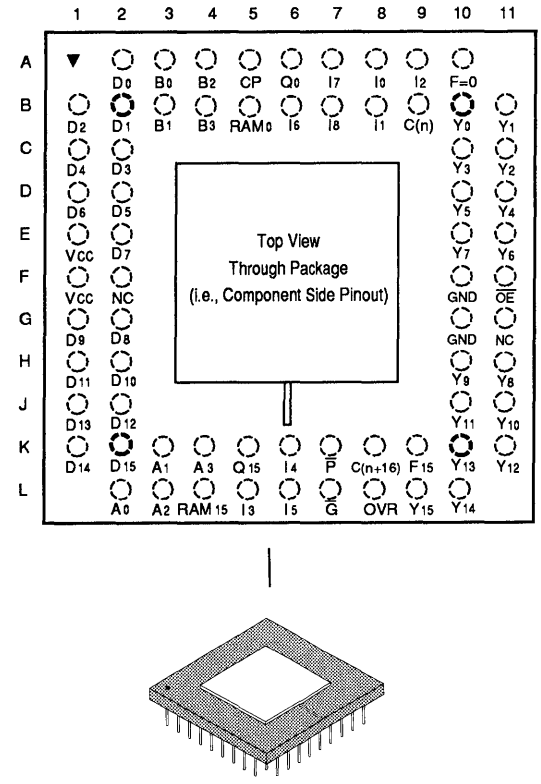
15. The setup time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

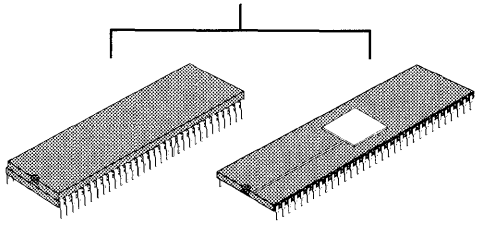
ORDERING INFORMATION

64-pin



68-pin





Speed	Plastic DIP (P4)	Sidebraze Hermetic DIP (D6)	Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
35 ns	L29C101PC35	L29C101DC35	L29C101GC35
	–55°C to +125°C — Commercial Screening		
45 ns		L29C101DM45	L29C101GM45
	–55°C to +125°C — Extended Screening		
45 ns		L29C101DME45	L29C101GME45
	–55°C to +125°C — MIL-STD-883 Compliant		
45 ns		L29C101DMB45	L29C101GMB45

32-bit Cascadable Barrel Shifter — LSH32

FEATURES

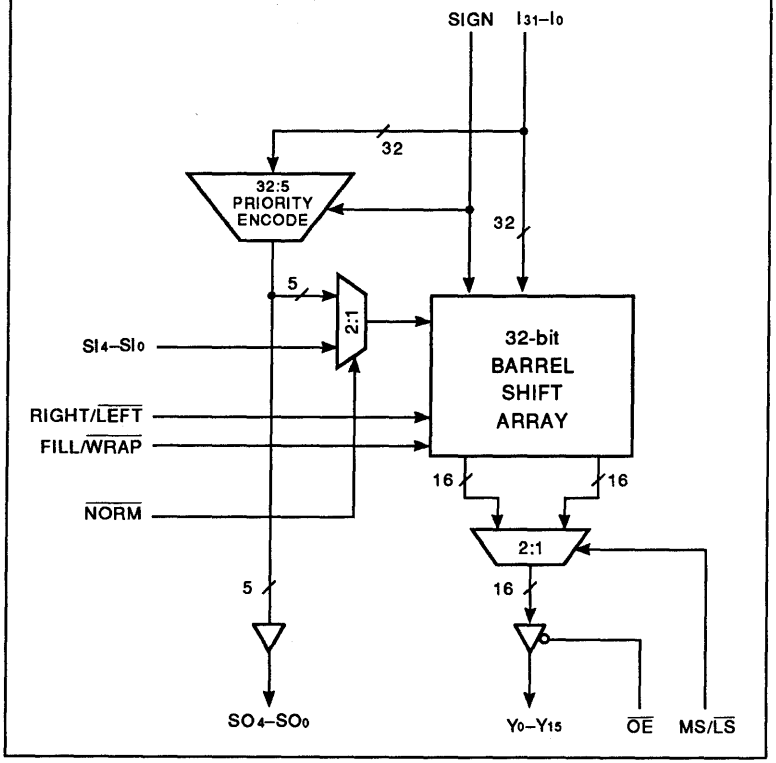
- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0–31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC (Type C)
  - 68-pin Pin Grid Array

DESCRIPTION

The **LSH32** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

The major features of the LSH32 architecture are discussed in the following paragraphs.

LSH32 Block Diagram



Shift Array

The 32 inputs to the LSH32 are applied to a 32-bit shift array. The 32 outputs of this array are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH32 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH32 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the Right/$\overline{\text{Left}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

5

Table 1. Wrap Mode Shift Code Definitions.

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	I_{31}
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	I_{29}	I_{30}
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•	I_0	I_{31}	•	•	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_{13}	I_{12}	I_1	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	I_2	I_1	I_0	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	I_1	I_0	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	I_0	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 2. Fill Mode Shift Code Definitions (Left Shift).

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	0
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	0	0
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	0	0
10000	I_{15}	I_{14}	I_{13}	•	I_0	0	•	•	0	0
10001	I_{14}	I_{13}	I_{12}	•	0	0	•	•	0	0
10010	I_{13}	I_{12}	I_{11}	•	0	0	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_3	I_2	I_1	•	0	0	•	•	0	0
11101	I_2	I_1	I_0	•	0	0	•	•	0	0
11110	I_1	I_0	0	•	0	0	•	•	0	0
11111	I_0	0	0	•	0	0	•	•	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH32 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

Output Multiplexer

The shift array outputs are applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

Priority Encoder

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs;

Table 3. Fill Mode Shift Code Definitions (Right Shift).

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	S	S	•	•	S	S	•	•	S	S
00001	S	S	•	•	S	S	•	•	S	I_{31}
00010	S	S	•	•	S	S	•	•	I_{31}	I_{30}
00011	S	S	•	•	S	S	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	S	S	S	•	S	S	•	•	I_{18}	I_{17}
10000	S	S	S	•	S	I_{31}	•	•	I_{17}	I_{16}
10001	S	S	S	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	S	S	S	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	S	S	S	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	S	S	S	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	S	S	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	S	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 4. Priority Encoder Function Table.

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}	•••	I_0	Shift Code
1	X	X	•••	X	X	X	•••	X	00000
0	1	X	•••	X	X	X	•••	X	00001
0	0	1	•••	X	X	X	•••	X	00010
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	1	X	X	•••	X	01111
0	0	0	•••	0	1	X	•••	X	10000
0	0	0	•••	0	0	1	•••	X	10001
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	0	0	0	•••	1	11111
0	0	0	•••	0	0	0	•••	0	11111

the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

Normalize Multiplexer

The $\overline{NORM}$ input, when asserted results in the priority encoder output driving the internal shift code inputs directly. It is exactly equivalent to routing the SO_4–SO_0 outputs back to the SI_4–SI_0 inputs. The $\overline{NORM}$ input provides faster normalization of 32-bit data by avoiding the delay associated with routing the shift code off chip. When using the $\overline{NORM}$ function, the LSH32 should be placed in fill mode, with the R/$\overline{L}$ input low.

Applications Examples

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH32. The $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH32 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

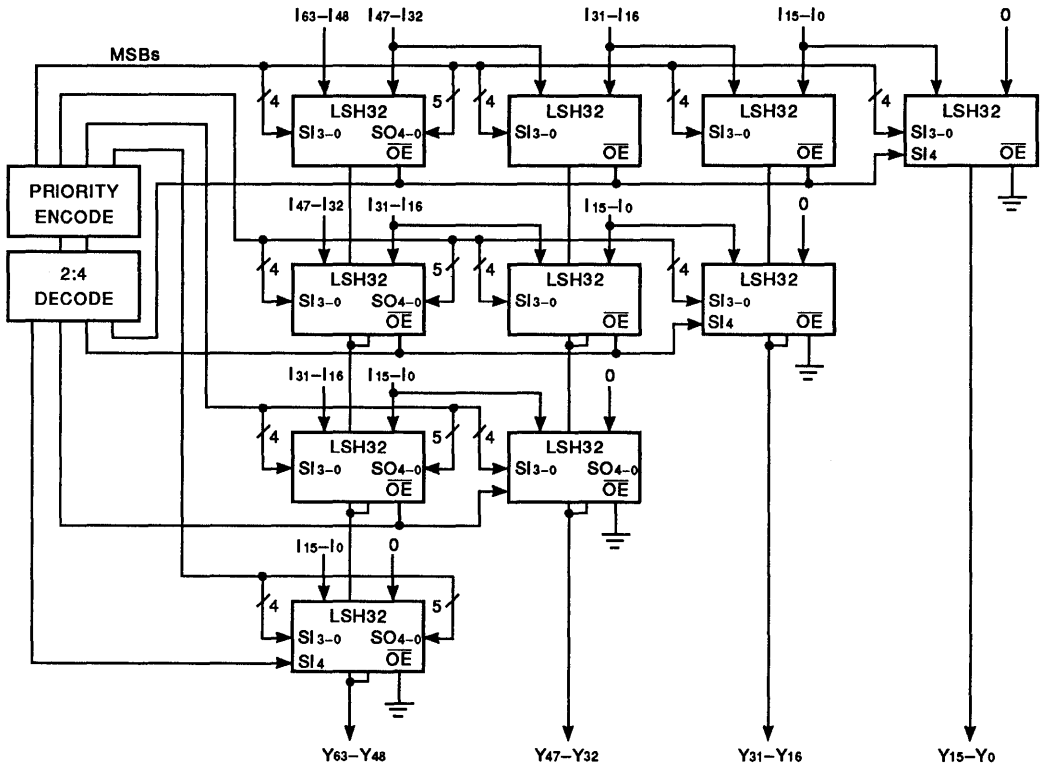
Long-Word Normalization (Multiple Cycles)

Normalization of floating point mantissas longer than 32 bits can be accomplished by cascading LSH32 units. When cascading for normalization, the device inputs are overlapped such that each device lower in priority than the first shares 16 inputs with its more significant neighbor. Fill mode and left shift are selected, however, internal normalization ($\overline{NORM}$) is not used. The most significant result half of each device is enabled to the output. The shift out (SO_4–SO_0) lines of the most significant slice are connected to the shift in lines of all slices, including the first. The exception is that all SI_4 lines are grounded, limiting the shift distance to 16 positions. The shift distance required for normalization is produced by the priority encoder in the most significant slice. The priority encoder will produce the shift code necessary to normalize the input word if the leading non-zero digit is found in the upper 16 bits. If this is the case, the number of shift positions necessary to accomplish normalization is placed on the SO_4–SO_0 outputs for use by all slices, and the appropriate 0–15 bit shift is accomplished. If the upper 16 bits are all zero, then the maximum shift of 15 places is executed. Single clock normalization requiring shifts longer than 16 bits can be accomplished by a bank-select technique described below.

Single Cycle Long-Word Normalization

An extension of the above concept is a single clock normalization of long words (potentially requiring shifts of more than 15 places). The arrangement of LSH32s required is shown in Figure 1. Cascading of LSH32 units is accomplished by connecting the SI_3–SI_0 input lines of each unit to the SO_3–SO_0 outputs of the most significant device in the row as before. Essentially the LSH32s are arranged in

Figure 1. Single Cycle Long-Word Normalization Using LSH32s.



multiple rows or banks such that the inputs to successive rows are left-shifted by 16 positions. The outputs of each row are multiplexed onto a three-state bus. The normalization problem then reduces to selecting from among the several banks that one which has the first non-zero bit of the input value among its 16 most significant positions. If the most significant one in the input file was within the upper 16 locations of a given bank, the SO_4 output of the most significant slice in that bank will be low. Single clock normalization can thus be accomplished simply by enabling onto the three-state output bus the highest priority bank in which this condition is met. In this way the input word will be normalized regardless of the number of shift positions required to accomplish this. The number of shift positions can be determined simply by concatenation of the SO_3–SO_0 outputs of the most significant slice in the selected row with the encoded Output Enable-bits determining the row number. Note that lower rows need not be fully populated. This is because they represent left shifts in multiples of 16 positions, and the lower bits of the output word will be zero filled. In order to accomplish this zero fill, the least significant device in each row is always enabled, and the row select is instead connected to the SI_4 input. This will force the shift length of the least significant device to a value greater than 15 whenever the row containing that device is not selected. This results in zero fill being accomplished by the equivalently positioned slice in a higher bank, as shown in the diagram.

Block Floating Point

With a small amount of external logic, block floating point operations are easily accomplished by the LSH32. Data resulting from a vector operation are applied to the LSH32 with the $\overline{NORM}$-input deasserted. The SO_4–SO_0 outputs fill then represent the normalization shift distance for each vector element in turn. By use of an external latch and comparator, the maximum shift distance encountered across all elements in the vector is saved for use in the next block operation (or block normalization). During this subsequent pass through the data, the shift code saved from the previous pass is applied uniformly across all elements of the vector. Since the LSH32 is not used in the internal normalize mode, this operation can be pipelined, thereby obtaining the desired shift distance for the next pass while simultaneously applying the normalization required from the previous pass.

5

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

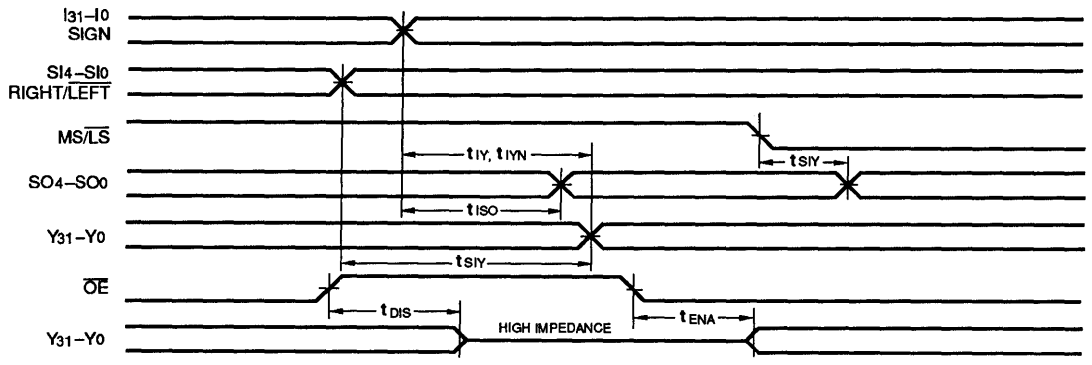
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LSH32-- 42 Min	42 Max	32 Min	32 Max
t_{IY}	I, SIGN Inputs to Y Outputs		42		32
t_{ISO}	I, SIGN Inputs to SO Outputs		55		42
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		75		60
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		52		40
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		28		24
t_{DIS}	$\overline{\text{OE}}$ to Output Disable (Note 11)		20		20
t_{ENA}	$\overline{\text{OE}}$ to Output Enable (Note 11)		20		20

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LSH32-- 50 Min	50 Max	40 Min	40 Max
t_{IY}	I, SIGN Inputs to Y Outputs		50		40
t_{ISO}	I, SIGN Inputs to SO Outputs		65		52
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		85		75
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		62		52
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		32		26
t_{DIS}	$\overline{\text{OE}}$ to Output Disable (Note 11)		22		20
t_{ENA}	$\overline{\text{OE}}$ to Output Enable (Note 11)		22		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

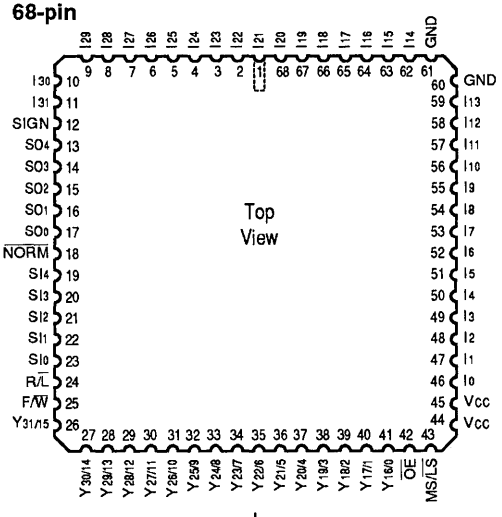
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

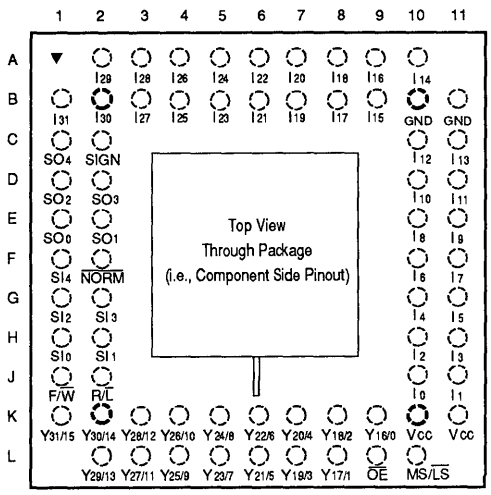
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

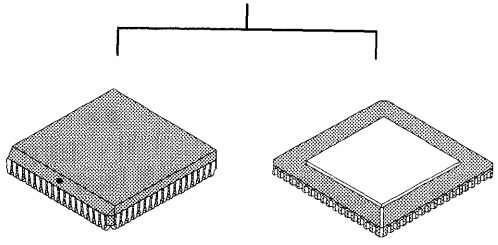
ORDERING INFORMATION

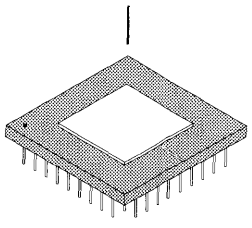
68-pin



68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
42 ns	LSH32JC42	LSH32KC42	LSH32GC42
32 ns	" " 32	" " 32	" " 32
	–55°C to +125°C — Commercial Screening		
50 ns		LSH32KM50	LSH32GM50
40 ns		" " 40	" " 40
	–55°C to +125°C — Extended Screening		
50 ns		LSH32KME50	LSH32GME50
40 ns		" " 40	" " 40
	–55°C to +125°C — MIL-STD-883 Compliant		
50 ns		LSH32KMB50	LSH32GMB50
40 ns		" " 40	" " 40

5

32-bit Barrel Shifter with Registers — LSH33

FEATURES

- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0–31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Fully Registered Input/Output with Independent Bypass Paths
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC (Type C)
  - 68-pin Pin Grid Array

DESCRIPTION

The **LSH33** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

Input/Output registers provide complete pipelined operation. Both have independent bypass paths for complete flexibility.

Shift Array

The 32 registered inputs to the LSH33 are applied to a 32-bit shift array. The 32 outputs of this array can be registered, then are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH33 is configured as a left shift device. That is, a shift code of 000002 results in no shift of the input field. A code of 000012 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 111112 (–110) results in a right shift of one position, etc.

When not in the wrap mode, the LSH33 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the Right/$\overline{\text{Left}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

LSH33 Block Diagram

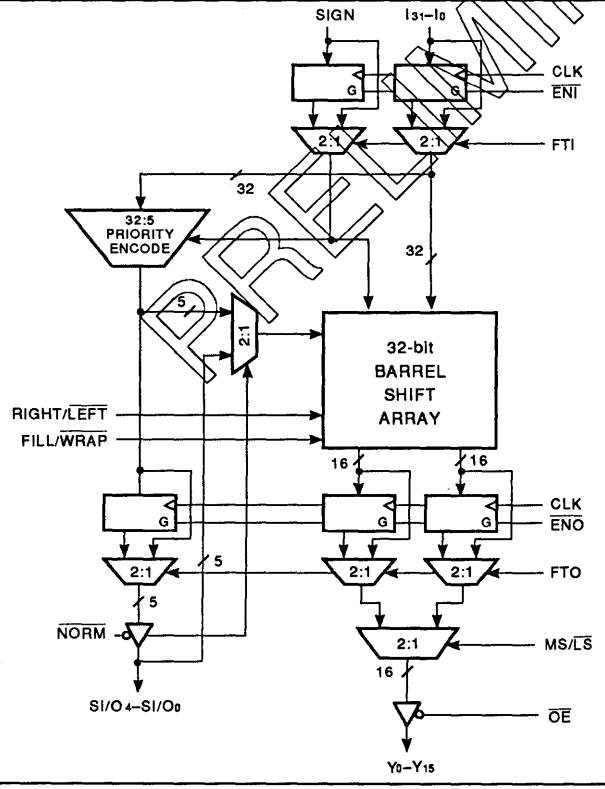


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Table 1. Wrap Mode Shift Code Definitions.

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	I_{31}
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	I_{29}	I_{30}
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•	I_0	I_{31}	•	•	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_{13}	I_{12}	I_1	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	I_2	I_1	I_0	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	I_1	I_0	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	I_0	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 2. Fill Mode Shift Code Definitions (Left Shift).

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	I_{31}	I_{30}	•	•	I_{16}	I_{15}	•	•	I_1	I_0
00001	I_{30}	I_{29}	•	•	I_{15}	I_{14}	•	•	I_0	0
00010	I_{29}	I_{28}	•	•	I_{14}	I_{13}	•	•	0	0
00011	I_{28}	I_{27}	•	•	I_{13}	I_{12}	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	I_{16}	I_{15}	I_{14}	•	I_1	I_0	•	•	0	0
10000	I_{15}	I_{14}	I_{13}	•	I_0	0	•	•	0	0
10001	I_{14}	I_{13}	I_{12}	•	0	0	•	•	0	0
10010	I_{13}	I_{12}	I_{11}	•	0	0	•	•	0	0
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	I_3	I_2	I_1	•	0	0	•	•	0	0
11101	I_2	I_1	I_0	•	0	0	•	•	0	0
11110	I_1	I_0	0	•	0	0	•	•	0	0
11111	I_0	0	0	•	0	0	•	•	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH33 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

Output Multiplexer

The shift array outputs can be registered and then applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

Priority Encoder

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs;

Table 3. Fill Mode Shift Code Definitions (Right Shift).

Shift Code	Y_{31}	Y_{30}	•	•	Y_{16}	Y_{15}	•	•	Y_1	Y_0
00000	S	S	•	•	S	S	•	•	S	S
00001	S	S	•	•	S	S	•	•	S	I_{31}
00010	S	S	•	•	S	S	•	•	I_{31}	I_{30}
00011	S	S	•	•	S	S	•	•	I_{30}	I_{29}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
01111	S	S	S	•	S	S	•	•	I_{18}	I_{17}
10000	S	S	S	•	S	I_{31}	•	•	I_{17}	I_{16}
10001	S	S	S	•	I_{31}	I_{30}	•	•	I_{16}	I_{15}
10010	S	S	S	•	I_{30}	I_{29}	•	•	I_{15}	I_{14}
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
11100	S	S	S	•	I_{20}	I_{19}	•	•	I_5	I_4
11101	S	S	S	•	I_{19}	I_{18}	•	•	I_4	I_3
11110	S	S	I_{31}	•	I_{18}	I_{17}	•	•	I_3	I_2
11111	S	I_{31}	I_{30}	•	I_{17}	I_{16}	•	•	I_2	I_1

Table 4. Priority Encoder Function Table.

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}	•••	I_0	Shift Code
1	X	X	•••	X	X	X	•••	X	00000
0	1	X	•••	X	X	X	•••	X	00001
0	0	1	•••	X	X	X	•••	X	00010
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	1	X	X	•••	X	01111
0	0	0	•••	0	1	X	•••	X	10000
0	0	0	•••	0	0	1	•••	X	10001
•	•	•	•••	•	•	•	•••	•	•
•	•	•	•••	•	•	•	•••	•	•
0	0	0	•••	0	0	0	•••	1	11111
0	0	0	•••	0	0	0	•••	0	11111

the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

Normalize Multiplexer

The $\overline{NORM}$ input, when asserted, results in the priority encoder output driving the internal shift code inputs directly. When using the $\overline{NORM}$ function, the LSH33 should be placed in fill mode, with the R/$\overline{L}$ input low.

When $\overline{NORM}$ is high (not asserted), the SI/O4–SI/O0 port acts as the shift code input to the shifter.

Applications Examples

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH33. The $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH33 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			–250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10*

GUARANTEED MAXIMUM COMBINATIONAL DELAYS (ns)

From Input \ To Output	LSH33-40		LSH33-30		
	Y_{15}–Y_0	SO_4–SO_0	Y_{15}–Y_0	SO_4–SO_0	
FTI = 0, FTO = 0					
CLK					
MS/$\overline{LS}$		—		—	
FTI = 0, FTO = 1					
CLK					
SI_4–SI_0		—		—	
R/$\overline{L}$, F/$\overline{W}$		—		—	
MS/$\overline{LS}$		—		—	
FTI = 1, FTO = 0					
CLK					
MS/LS		—		—	
FTI = 1, FTO = 1					
I_{31}–I_0, SIGN					
SI_4–SI_0		—		—	
R/$\overline{L}$, F/$\overline{W}$		—		—	
MS/$\overline{LS}$		—		—	

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE (ns)

Input	LSH33-40				LSH33-30					
	FTI = 0		FTI = 1		FTI = 0		FTI = 1			
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold		
I_{31}–I_0, SIGN										
SI_4–SI_0										
R/$\overline{L}$, F/$\overline{W}$										
$\overline{ENI}$, $\overline{ENO}$										

THREE STATE ENABLE/DISABLE TIMES (ns) Note 11

	LSH33-40	LSH33-30	
t_{EN}			
t_{DIS}			

CLOCK CYCLE TIME AND PULSE WIDTH (ns)

	LSH33-40	LSH33-30	
Minimum Cycle Time			
Highgoing Pulse			
Lowgoing Pulse			

5

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +120°C) *Notes 9, 10*

GUARANTEED MAXIMUM COMBINATIONAL DELAYS (ns)

To Output / From Input	LSH33-50 Y_{15}–Y_0	LSH33-50 SO_4–SO_0	LSH33-40 Y_{15}–Y_0	LSH33-40 SO_4–SO_0		
FTI = 0, FTO = 0						
CLK						
MS/$\overline{LS}$		—		—		
FTI = 0, FTO = 1						
CLK						
SI_4–SI_0		—		—		
R/$\overline{L}$, F/$\overline{W}$		—		—		
MS/$\overline{LS}$		—		—		
FTI = 1, FTO = 0						
CLK						
MS/LS		—		—		
FTI = 1, FTO = 1						
I_{31}–I_0, SIGN						
SI_4–SI_0		—		—		
R/$\overline{L}$, F/$\overline{W}$		—		—		
MS/$\overline{LS}$		—		—		

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE (ns)

Input	LSH33-50 FTI = 0 Setup	LSH33-50 FTI = 0 Hold	LSH33-50 FTI = 1 Setup	LSH33-50 FTI = 1 Hold	LSH33-40 FTI = 0 Setup	LSH33-40 FTI = 0 Hold	LSH33-40 FTI = 1 Setup	LSH33-40 FTI = 1 Hold		
I_{31}–I_0, SIGN										
SI_4–SI_0										
R/$\overline{L}$, F/$\overline{W}$										
$\overline{ENI}$, $\overline{ENO}$										

THREE STATE ENABLE/DISABLE TIMES (ns) Note 11

	LSH33-50	LSH33-40	
t_{EN}			
t_{DIS}			

CLOCK CYCLE TIME AND PULSE WIDTH (ns)

	LSH33-50	LSH33-40	
Minimum Cycle Time			
Highgoing Pulse			
Lowgoing Pulse			

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

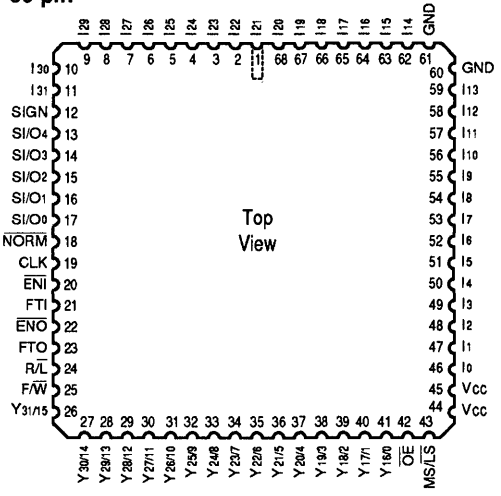
10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

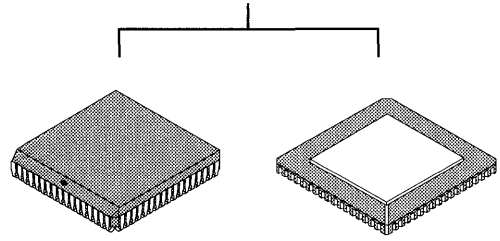
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

5

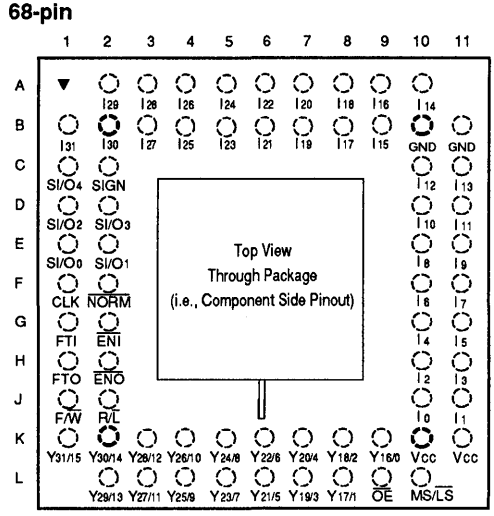
ORDERING INFORMATION

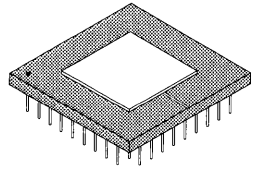
68-pin





68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening		
40 ns	LSH33JC40	LSH33KC40	LSH33GC40
30 ns	" " 30	" " 30	" " 30
	–55°C to +125°C — Commercial Screening		
50 ns		LSH33KM50	LSH33GM50
40 ns		" " 40	" " 40
	–55°C to +125°C — Extended Screening		
50 ns		LSH33KME50	LSH33GME50
40 ns		" " 40	" " 40
	–55°C to +125°C — MIL-STD-883 Compliant		
50 ns		LSH33KMB50	LSH33GMB50
40 ns		" " 40	" " 40

64-bit Digital Correlator — L10C23

FEATURES

- High Speed (50 MHz), Low Power (125 mW), CMOS 64-bit Digital Correlator
- Functionally and Pin Compatible with TRW TDC1023J
- Bits Can be Selectively Masked
- Three-State Outputs
- Available 100% Screended to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC (Type C)

DESCRIPTION

The **L10C23** is a high speed CMOS 64-bit digital correlator. It is pin-for-pin equivalent to the TDC1023 bipolar correlator. The L10C23 operates over the full military ambient temperature range using advanced CMOS technology.

The L10C23 produces the 7-bit correlation score of two input words of up to 64 bits, denoted A and B. The A and B inputs are serially shifted into two independently clocked 64-bit registers. The A register is clocked on the rising edge of CLK A, and the B register is clocked on the rising edge of CLK B.

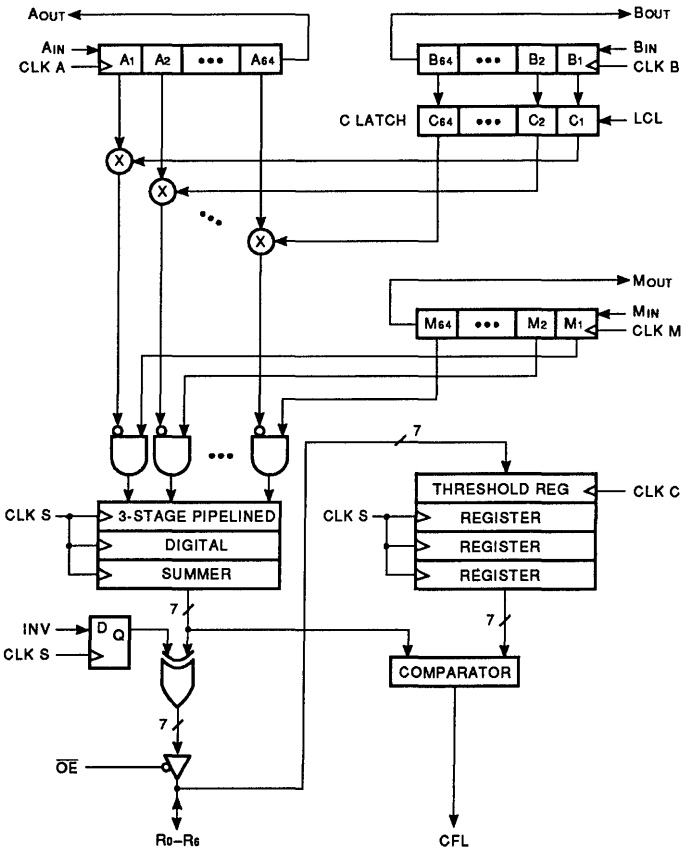
The outputs of the B register drive a 64-bit transparent latch, denoted the C latch. The C latch is controlled by the LCL (Load C Latch) input. A high level on the LCL input causes the C latch to be transparent, allowing the contents of the B register to be applied directly to the correlator array. When the LCL input is low, the data in the C latch is held, so that the B input may be loaded with a new correlation reference without affecting the current reference value stored in C.

Each bit in the A register is exclusive NOR'ed with the corresponding bit in the C latch, implementing a single bit multiplication at each bit position.

The mask register, denoted by M, is a third 64-bit register, which is serially loaded from the M input on the rising edge of CLK M. Bit positions in the M register which are set to zero mask the corresponding bits in the A and C registers from participating in the correlation score. This can be used to reduce the effective length of the correlation, or to correlate against only one channel of a bit-multiplexed datastream without deinterleaving the data.

The output of the masking process is a 64-bit vector which contains ones in the locations in which A and B data match, and which are unmasked (M register contains a '1'). This 64-bit vector is applied to a pipelined digital summer which calculates the total number of ones in the vector (the correlation score). The summer network contains three pipeline stages, which are clocked on the rising edge of CLK S. Calculation of a correlation

L10C23 Block Diagram



score therefore requires three clock cycles, but a new result can be obtained on each cycle once the pipeline is filled.

Because a portion of the summer logic is located between the input registers and the first pipeline register, some timing restrictions exist between CLK S and CLK A, CLK B, or CLK M. CLK S may be tied to an input clock (usually CLK A) to obtain a continuously updated correlation score, delayed by three cycles from the data. Under this condition, CLK S may be skewed later than CLK A by no more than t_{SK} to assure that the A register outputs have not changed before the S clock occurs.

Alternatively, CLK S may be asynchronous to the input clocks, as long as data is stable at the pipeline register inputs prior to the CLK S rising edge. This condition can be met by assuring that CLK S occurs at least t_{PS} after the input clock.

The summer output represents a count of the number of matching positions in the input data streams. This 7-bit result can be inverted (one's-complemented) by loading a '1' into the INV register.

Correlation values which exceed a predetermined threshold can be detected via the Threshold register and Comparator. The Threshold register is loaded with a 7-bit value via the R_6–R_0 pins at the rising edge of CLK C and while $\overline{OE}$ is logic high. To achieve synchronization with the digital summer, the Threshold register contents are fed into pipeline registers clocked by CLK S. The compare flag output ($\overline{CFL}$) goes high when the summer output is equal to or greater than the contents of the Threshold register.

Cascading the L10C23 devices for longer correlation lengths and more bits of reference or data precision is easily accomplished. The A, B, and M registers have serial outputs to directly drive the corresponding inputs of succeeding devices. The correlation scores of multiple devices in such a system should be added together to obtain the overall correlation score.

Correlation on data exceeding one bit of precision can be accomplished by first calculating single-bit correlation scores at each bit position, then adding the results after weighting them appropriately. Thus, one L10C23 would be used for each bit of precision in the data.

Logic Devices' L4C381 16-bit ALU can be used to assist in adding the outputs of several L10C23 correlators. When adding several 7-bit correlation scores, advantage can be taken of the fact that the sum of two 7-bit numbers will not exceed 8 bits. Thus the L4C381 can simultaneously perform *two* 7-bit additions. The first two operands are applied to A_6–A_0 and B_6–B_0, with the result appearing on F_7–F_0. The second pair of operands are applied to A_{14}–A_8 and B_{14}–B_8, with the result appearing in F_{15}–F_8. The unused inputs are tied to ground. If it can be guaranteed that at least one of the input scores will not reach its maximum value of 64, then this technique can also be applied in the second tier of adders. In this case, while the inputs have 8 bits of precision, the maximum value their sum can assume is 255, which is expressable in 8 bits.

Alternatively, when performing long correlations on relatively slow datastreams, one L4C381 can be configured using its feedback mode to accumulate the correlation scores of a number of L10C23s. To accomplish this, the outputs of all the correlators are tied together on a three-state bus. Each one is sequentially enabled and clocked into the L4C381, which accumulates the total resulting score.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	3.5			V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			−250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			0.5	mA

SWITCHING CHARACTERISTICS

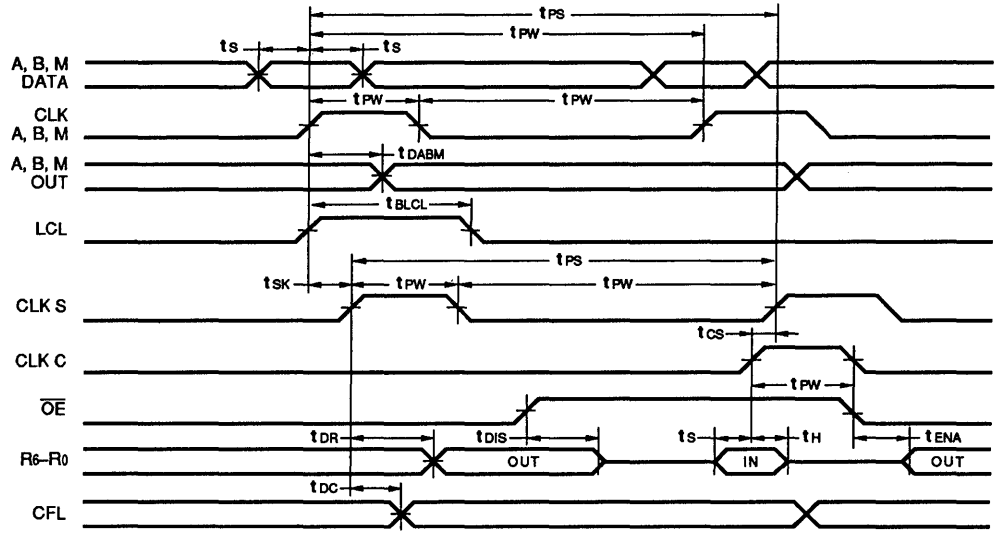
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L10C23-					
		50		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	50		28		20	
t_S	Input Data Setup Time	20		10		10	
t_H	Input Data Hold Time	0		0		0	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		12		8	
t_{DABM}	A, B, M Clock to A, B, M Out		25		20		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	50		28		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_6–R_0		35		30		22
t_{DC}	S Clock to CFL		25		20		18
t_{DIS}	Output Disable Time (Note 11)		35		16		14
t_{ENA}	Output Enable Time (Note 11)		30		18		16
t_{CS}	Clock C to Clock S	50		28		20	
t_{BLCL}	Clock B to LCL Hold	20		12		8	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L10C23-					
		60		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	58		33		20	
t_S	Input Data Setup Time	22		12		12	
t_H	Input Data Hold Time	0		0		0	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		14		8	
t_{DABM}	A, B, M Clock to A, B, M Out		30		23		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	58		33		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_6–R_0		40		35		25
t_{DC}	S Clock to CFL		30		23		18
t_{DIS}	Output Disable Time (Note 11)		40		18		16
t_{ENA}	Output Enable Time (Note 11)		35		20		18
t_{CS}	Clock C to Clock S	58		33		20	
t_{BLCL}	Clock B to LCL Hold	20		14		8	

Switching Waveforms



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

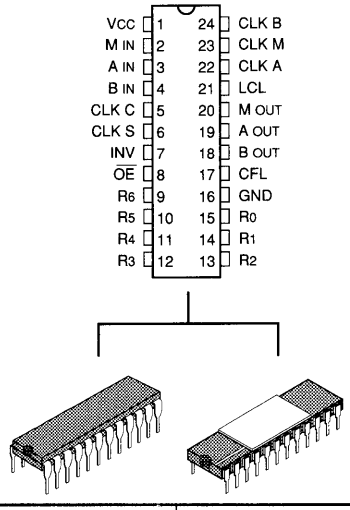
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

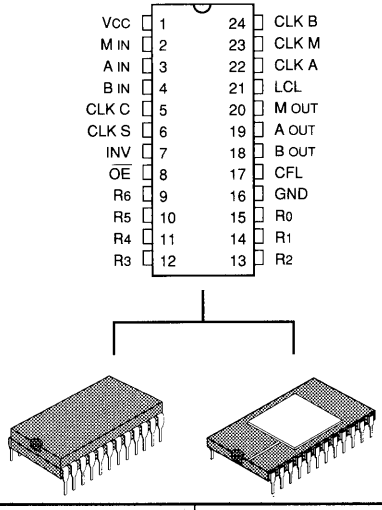
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

ORDERING INFORMATION

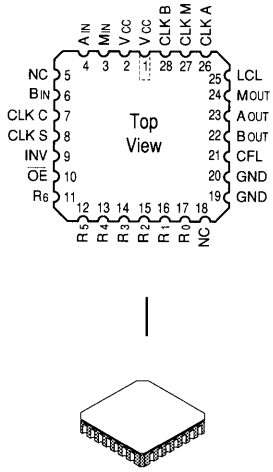
24-pin
(0.3" wide)



24-pin
(0.6" wide)



28-pin



Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	Plastic DIP (P1)	Sidebraze Hermetic DIP (D1)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening				
50 ns	L10C23NC50	L10C23HC50	L10C23PC50	L10C23DC50	L10C23KC50
30 ns	" " 30	" " 30	" " 30	" " 30	" " 30
20 ns	" " 20	" " 20	" " 20	" " 20	" " 20
	–55°C to +125°C — Commercial Screening				
60 ns		L10C23HM60		L10C23DM60	L10C23KM60
35 ns		" " 35		" " 35	" " 35
20 ns		" " 20		" " 20	" " 20
	–55°C to +125°C — Extended Screening				
60 ns		L10C23HME60		L10C23DME60	L10C23KME60
30 ns		" " 35		" " 35	" " 35
20 ns		" " 20		" " 20	" " 20
	–55°C to +125°C — MIL-STD-883 Compliant				
60 ns		L10C23HMB60		L10C23DMB60	L10C23KMB60
30 ns		" " 35		" " 35	" " 35
20 ns		" " 20		" " 20	" " 20

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Ordering Information

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L5380 SCSI Controller 6-3
L53C80 SCSI Controller 6-3

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Product Selection /Cross Reference Guide

Product Selection

Part No.	Description	Speed (ns) Com.	Speed (ns) Mil.	Power (mW)	Pins	Packages Available
L5380	SCSI Controller	4 Mbytes/s	2 Mbytes/s	50	40/44	DIP, PLCC
L53C80	SCSI Controller	4 Mbytes/s	2 Mbytes/s	50	48/44	DIP, PLCC

Product Cross Reference

LOGIC DEVICES		AMD	NCR	National
L5380	**SCSI**	AM5380	NCR5380 NCR5380-40	DP5380
L53C80	**SCSI**	AM53C80	NCR53C80	

CMOS SCSI Bus Controller — L5380/L53C80

FEATURES

- Asyncronous Transfer Rrate Up to 4 Mbytes/sec
- Pin and Functionally Compatible with NCR5380, but 2.5× Faster
- Low Power CMOS Technology
- On-Chip SCSI Bus Drivers
- Supports Arbitration, Selection/ Reselection, Initiator or Target Roles
- Programmed or DMA I/O, Handshake or Wait State DMA Interlock
- Package Styles Available:
  - 40/48-pin Plastic DIP
  - 40/48-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

DESCRIPTION

The **L5380/ L53C80** are very high performance CMOS controllers which support the physical layer of the SCSI (Small Computer System Interface) bus as defined by the ANSI X3T9.2 committee. It is pin and functionally compatible with the NMOS NCR5380, while offering up to a 2.5× performance improvement, 10× power reduction, and lower cost. Replacement of the NMOS 5380 by the LOGIC Devices L5380/L53C80 will result in an immediate transfer rate improvement due to $\overline{REQ}/\overline{ACK}$ and DRQ/$\overline{DACK}$ handshake response times up to 5 times faster than previous devices.

While remaining firmware compatible with the NCR5380, the L5380/L53C80 provides bug fixes and state machine enhancements allowing even larger throughput gains for new designs.

The L5380/L53C80 supports asyncronous data transfer between initiator and target at up to 4 Mbytes/sec. It operates in either initiator or target roles, and offers a choice of programmed I/O (direct microprocessor manipulation of handshake) or any of several DMA modes (autonomous handshake and data transfer operations). The L5380/L53C80 has

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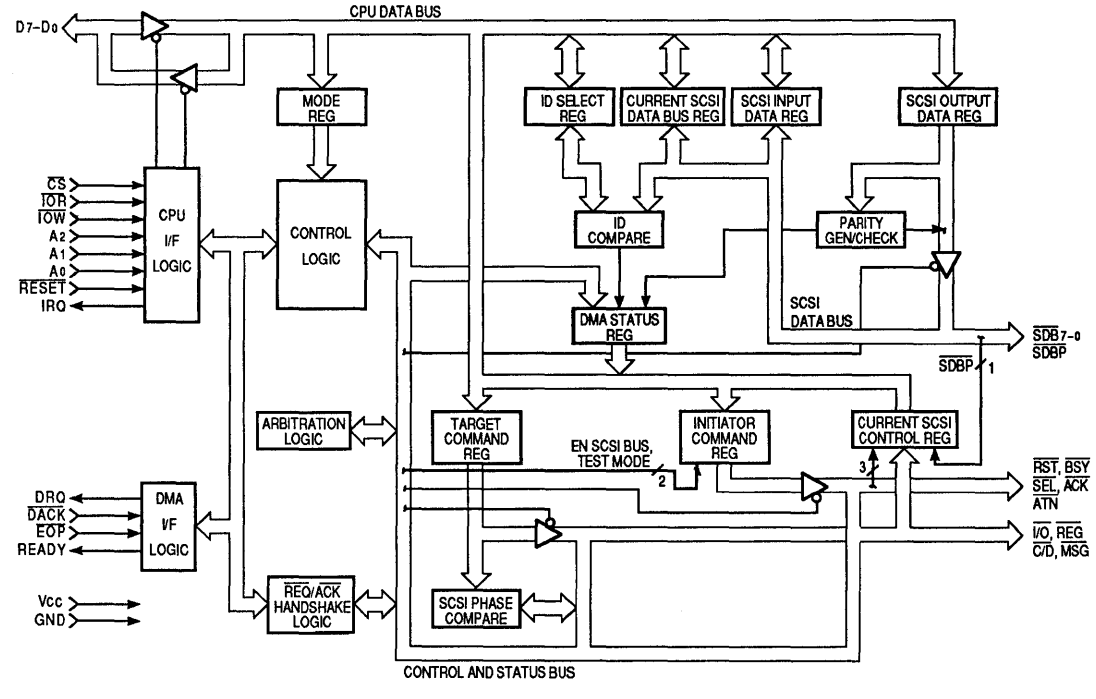
L5380/L53C80 Block Diagram



internal hardware to support arbitration, and can monitor and generate interrupts for a variety of error conditions. It provides extensive bus status monitoring features, and includes buffers capable of directly driving a terminated SCSI bus for a compact implementation.

PIN DEFINITION

A. SCSI Bus

$\overline{SDB}_{7-0}$ — SCSI DATA BUS 7–0: Bidirectional/Active low. The 8-bit SCSI data bus is defined by these pins. $\overline{SDB7}$ is the most significant bit. During arbitration phase, these lines contain the SCSI ID numbers of all initiators arbitrating for the SCSI bus; $\overline{SDB7}$ represents the initiator with the highest priority. During the selection/reselection phase, these lines contain the ID number of the device that won the arbitration along with the ID number of the device to be selected/reselected.

$\overline{SDBP}$ — SCSI DATA BUS PARITY: Bidirectional/Active low. $\overline{SDBP}$ is the parity bit of the SCSI data bus. Odd parity is used, meaning that the total number of ones on the bus, including the parity bit, is odd. Parity is always generated when sending information, however checking for parity errors when receiving information is a user option. Parity is not valid during arbitration phase.

$\overline{SEL}$ — SELECT: Bidirectional/Active low. $\overline{SEL}$ is asserted by the initiator to select a target. It is also asserted by the target when reselecting it as an initiator.

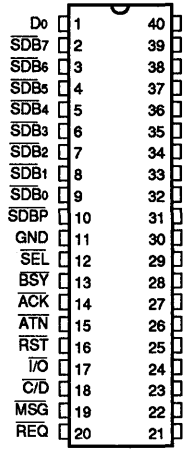
$\overline{BSY}$ — BUSY: Bidirectional/Active low. $\overline{BSY}$ is asserted to indicate that the SCSI bus is active.

$\overline{ACK}$ — ACKNOWLEDGE: Bidirectional/Active low. $\overline{ACK}$ is asserted by the initiator, during any information transfer phase, in response to assertion of $\overline{REQ}$ by the target. Similarly, $\overline{ACK}$ is deasserted after $\overline{REQ}$ becomes inactive. These two signals form the data transfer handshake between the initiator and target. Data is latched by the target on the lowgoing edge of $\overline{ACK}$ for target receive operations.

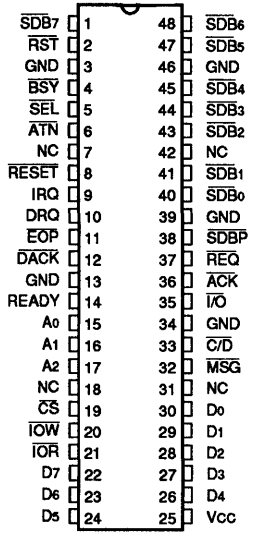
$\overline{ATN}$ — ATTENTION: Bidirectional/Active low. $\overline{ATN}$ is asserted by the initiator after successful selection of a target, to indicate an intention to send a message to the target. The target responds to $\overline{ATN}$ by entering the MESSAGE OUT phase.

PIN ASSIGNMENTS

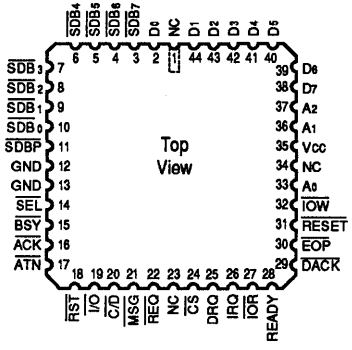
L5380 — 40-pin Plastic DIP (P)
40-pin Hermetic DIP (D)



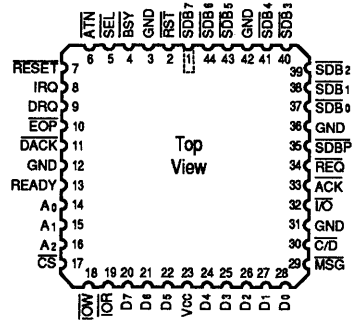
L53C80 — 48-pin Plastic DIP (P)
48-pin Hermetic DIP (D)



L5380 — 44-pin J-Lead (J)
44-pin Ceramic LCC (K)



L53C80 — 44-pin J-Lead (J)
44-pin Ceramic LCC (K)



$\overline{RST}$ — SCSI BUS RESET:
Bidirectional/Active low. $\overline{RST}$ when active indicates a SCSI bus reset condition.

$\overline{I/O}$ — INPUT/OUTPUT:
Bidirectional/Active low. $\overline{I/O}$ is controlled by the target and specifies the direction of information transfer. When $\overline{I/O}$ is asserted, the direction of transfer is to the initiator. $\overline{I/O}$ is also asserted by the target during RESELECTION phase to distinguish it from SELECTION phase.

$\overline{C/D}$ — CONTROL/DATA:
Bidirectional/Active low. $\overline{C/D}$ is controlled by the target and when asserted, indicates CONTROL (command or status) information is on the SCSI data bus. DATA is specified when $\overline{C/D}$ is deasserted.

$\overline{MSG}$ — MESSAGE:
Bidirectional/Active low. $\overline{MSG}$ is controlled by the target, and when asserted indicates MESSAGE phase.

$\overline{REQ}$ — REQUEST:
Bidirectional/Active low. $\overline{REQ}$ is asserted by the target to begin the handshake associated with transfer of a byte over the SCSI data bus. $\overline{REQ}$ is deasserted upon receipt of $\overline{ACK}$ from the initiator. Data is latched by the initiator on the lowgoing edge of $\overline{REQ}$ for initiator receive operations.

B. Microprocessor Bus

$\overline{CS}$ — CHIP SELECT:
Input/Active low. This signal enables reading or writing of the internal registers by the microprocessor, using memory mapped I/O. An alternate method for reading selected registers is available for DMA.

DRQ — DMA REQUEST:
Output/Active high. This signal is used to indicate that the L5380/L53C80 is ready to execute the next cycle of a DMA transfer on the microprocessor bus. For send operations, it indicates that the output data register is ready to receive the next byte from the DMA controller or CPU. For receive operations, it indicates that the input data register contains the next byte to be read by the DMA controller or CPU.

IRQ — INTERRUPT REQUEST:
Output/Active high. The L5380/L53C80 asserts this signal to indicate to the microprocessor that one of the several interrupt conditions have been met. These include SCSI bus fault conditions as well as other events requiring microprocessor intervention. Most interrupt types are individually maskable.

$\overline{IOR}$ — I/O READ:
Input/Active low. $\overline{IOR}$ is used in conjunction with $\overline{CS}$ and A_{2-0} to execute a memory mapped read of a L5380/L53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA read of the SCSI input data register.

READY — READY:
Output/Active high. Ready is used rather than DRQ as an alternate method for controlling DMA data transfer. This DMA type is termed blockmode DMA, and must be specifically enabled by the CPU. In blockmode DMA, data is throttled by treating the L5380/L53C80 as wait state memory. $\overline{I/O}$ (DMA) cycles are initiated at the maximum rate sustainable by the DMA controller/memory subsystem, but all cycles are extended (wait-states inserted) until READY is asserted by the L5380/L53C80. This is generally the fastest DMA method since memory subsystem addressing can be overlapped with SCSI operations (flyby mode).

$\overline{DACK}$ — DMA ACKNOWLEDGE:
Input/Active low. $\overline{DACK}$ is used in conjunction with $\overline{IOR}$ or $\overline{IOW}$ to enable reading or writing the SCSI Input and Output Data Registers when in DMA mode. $\overline{DACK}$ resets DRQ and must not occur simultaneously with $\overline{CS}$.

$\overline{EOP}$ — END OF PROCESS:
Input/Active low. This input is used to indicate to the L5380/L53C80 that a DMA transfer is to be concluded. The L5380/L53C80 can automatically generate an interrupt in response to receiving $\overline{EOP}$ from the DMA controller.

$\overline{RESET}$ — CPU BUS RESET:
Input/Active low. This input clears all internal registers and state machines. It does not result in assertion of the $\overline{RST}$ signal on the SCSI bus and therefore affects only the local L5380/L53C80 and not other devices on the bus.

$\overline{IOW}$ — I/O WRITE:
Input/Active low. $\overline{IOW}$ is used in conjunction with $\overline{CS}$ and A_{2-0} to execute a memory mapped write of a L5380/L53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA write of the SCSI output data register.

A_2, A_1, A_0 — ADDRESS 2,1,0:
Inputs/Active high. These signals, in conjunction with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$, address the L5380/L53C80 internal registers for CPU read/write operations.

D_{7-0} — DATA 7–0:
Bidirectional/Active high. These signals are the microprocessor data bus. D_7 is the most significant bit.

6

L5380/L53C80 INTERNAL REGISTERS

Overview

The L5380/L53C80 contains registers that are directly addressed by the microprocessor. These registers allow for monitoring of SCSI bus activity, controlling the operation of the L5380/L53C80, and determining the cause of interrupts. In many cases, a read-only and a write-only register are mapped to the same address. Some addresses are dummy registers which are used to implement a control operation but do not correspond to a physical register. The state of the CPU data bus when writing or reading these dummy registers is 'don't care.' Tables 1 and 3 show the address and name of each register as well as bit definitions.

Register Descriptions

A. WRITE OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/L53C80 internal registers for write operations as shown in Table 1.

WRITE ADDRESS 0 — Output Data Register

The Output Data Register is a write-only register used for sending information to the SCSI data bus. During arbitration, the arbitrating SCSI device asserts its ID via this register. The device which wins arbitration also asserts the "OR" of its ID and the ID of the target/initiator to be selected/reselected. In programmed I/O, this register is written using $\overline{CS}$ and $\overline{IOW}$ with $A_{2-0} = 000$. In DMA mode, it is written when $\overline{IOW}$ and $\overline{DACK}$ are simultaneously active, irrespective of the state of the address lines. Note that a "1" written to the Output Data Register becomes a low state when asserted on the active-low SCSI bus.

WRITE ADDRESS 1 — Initiator Command Register

The Initiator Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the initiator. Some bits in this register are not readable, and these positions are mapped to status bits useful in monitoring the progress of arbitration. These, along with the initiation of systemwide reset and test functions may also be of use to the target.

R1 Bit 7 - Assert $\overline{RST}$

When this bit is set, the L5380/L53C80 asserts the $\overline{RST}$ line on the SCSI bus, initializing all devices on the bus to the reset condition. All logic and internal registers of the L5380/L53C80 are reset, except for the Assert $\overline{RST}$ bit itself, the Testmode bit (R1 bit 6) and the IRQ (interrupt request) latch. The IRQ pin becomes active indicating a SCSI bus reset interrupt. This interrupt is not maskable.

R1 Bit 6 - Testmode

When this bit is set, the L5380/L53C80 places all outputs including both SCSI and CPU signals, in a high impedance state. This effectively removes the device from the system as an aid to system diagnostics. Note that internal registers may still be written while in testmode. The L5380/L53C80 returns to normal operation when Testmode is reset. The Testmode bit is reset by writing a 0 to R1 bit 6, or via the $\overline{RESET}$ (CPU reset) pin. Testmode is not affected by the $\overline{RST}$ (SCSI bus reset) signal, or by the Assert $\overline{RST}$ bit in the Initiator Command Register (R1 bit 7).

R1 Bit 5 - Not Used

R1 Bit 4 - Assert $\overline{ACK}$

When this bit is set, $\overline{ACK}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{ACK}$. Note that $\overline{ACK}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is reset, indicating that the L5380/L53C80 is acting as an initiator.

R1 Bit 3 - Assert $\overline{BSY}$

When this bit is set, $\overline{BSY}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{BSY}$. $\overline{BSY}$ is asserted to indicate that the device has been selected or reselected, and deasserting $\overline{BSY}$ causes a bus free condition.

R1 Bit 2 - Assert $\overline{SEL}$

When this bit is set, $\overline{SEL}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{SEL}$. $\overline{SEL}$ is normally asserted after a successful arbitration.

R1 Bit 1 - Assert $\overline{ATN}$

When this bit is set, $\overline{ATN}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{ATN}$. $\overline{ATN}$ is asserted by the initiator to request message out phase. Note that $\overline{ATN}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is reset, indicating that the L5380/L53C80 is acting as an initiator.

R1 Bit 0 - Assert Data Bus

When this bit is set, the open drain SCSI data bus and parity drivers are enabled and the contents of the Output Data Register are driven onto the SCSI data lines. In addition to the Assert Data Bus bit, enabling of the SCSI bus drivers requires one of the following two sets of conditions:

When the L5380/L53C80 is operating as an initiator, the Targetmode bit (R2 bit 6) must be reset, the I/O pin must be negated (initiator to target transfer) and no phase mismatch condition exist. A phase mismatch occurs when the $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ bits of the Target Command Register (R3) do not match the corresponding SCSI control lines.

When the L5380/L53C80 is operating as a target, the Targetmode bit will be set, and in this case Assert Data Bus will enable the outputs unconditionally.

The Assert Data Bus bit need not be set for arbitration to occur; when the Arbitrate bit (R2 bit 0) is set, and a bus free condition is detected, the data bus will be enabled for arbitration independent of the state of the Assert Data Bus bit.

Finally, note that the Testmode bit (R1 bit 6) overrides all other controls including Assert Data Bus and Arbitrate, and disables all outputs.

WRITE ADDRESS 2 — Mode Register

The Mode register is a read/write register which provides control over several aspects of L5380/L53C80 operation. Programmed I/O or two different types of DMA transfer may be selected, initiator or target device operation is accommodated, and parity checking and interrupts may be enabled via this register. The function of each individual bit is described as follows:

R2 Bit 7 - Blockmode

This bit must be used in conjunction with DMA Mode (R2 bit 1). It is used to select the type of handshake desired between the L5380/L53C80 and the external DMA controller. See "L5380/L53C80 Data Transfers" for a complete discussion of the transfer types supported.

R2 Bit 6 - Targetmode

When this bit is set, the L5380/L53C80 will operate as a SCSI target device. This enables the SCSI signals $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, and $\overline{REQ}$ to be asserted. When Targetmode is reset, the device will operate as an initiator. This enables the SCSI signals $\overline{ATN}$ and $\overline{ACK}$ to be asserted. Targetmode also affects state machine operation for DMA transfers, and the conditions necessary for enabling the SCSI Data bus drivers. (See Assert Databus, R1 bit 0).

TABLE 1. WRITE REGISTER CHART.

Address 0 — Output Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	TEST MODE		ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C/D}$	ASSERT $\overline{I/O}$

Address 4 — ID Select Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 5 — Start DMA Send

7	6	5	4	3	2	1	0

Address 6 — Start DMA Target Receive

7	6	5	4	3	2	1	0

Address 7 — Start DMA Initiator Receive

7	6	5	4	3	2	1	0

R2 Bit 5 - Enable Parity Check

When this bit is set, information received on the SCSI data bus is checked for odd parity. When Enable Parity Check is set, the Parity Error latch will be set whenever data is received under DMA control or the Current SCSI Data Register (Read Register 0) is read by the CPU. The state of the parity error latch can be determined by reading R5 bit 5, and it can be reset by a read to Address 7. Note that enable parity check must be set if parity error interrupts are to be generated. This interrupt can be separately masked by the Enable Parity Interrupt bit (R2 bit 4) while retaining the state of the parity error latch for later examination by the CPU.

R2 Bit 4 - Enable Parity Interrupt

When this bit is set, the L5380/L53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a parity error. Enable Parity Check (R2 bit 5) must also be set if parity error interrupts are desired.

R2 Bit 3 - Enable End Of DMA Interrupt

When this bit is set, the L5380/L53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a valid $\overline{EOP}$ (End of Process) signal. $\overline{EOP}$ is normally generated by a DMA controller to indicate the end of a DMA transfer. $\overline{EOP}$ is valid only when coincident with $\overline{IOR}$ or $\overline{IOW}$ and $\overline{DACK}$.

R2 Bit 2 - Monitor Busy

When this bit is set, the L5380/L53C80 continuously monitors the state of the $\overline{BSY}$ signal. Absence of $\overline{BSY}$ for a period longer than 400 ns (but less than 1200 ns) will cause the L5380/L53C80 to set the BSYERR and IRQ (interrupt request) latches. In addition, the 6 least significant bits of the Initiator Command Register are reset, and all SCSI data and control outputs are disabled until the BSYERR latch is reset. This effectively disconnects the L5380/L53C80 from the SCSI bus in response to an unexpected disconnect by another device. It also allows the CPU to be interrupted when the SCSI bus becomes free in systems where arbitration is not used and an $\overline{EOP}$ signal is not available.

R2 Bit 1 - DMA Mode

When this bit is set, the L5380/L53C80's internal state machines automatically control the SCSI signals $\overline{REQ}$ and $\overline{ACK}$ (as appropriate for initiator or target operation) and the CPU signals' DRQ and READY. DMA Mode must be set prior to starting a DMA transfer in either direction. The DMA Mode bit is reset whenever a bus free condition is detected ($\overline{BSY}$ is not active). This aborts DMA operations when a loss of $\overline{BSY}$ occurs, regardless of the state of the Monitor Busy bit (R2 bit 2.) The DMA Mode bit is not reset when $\overline{EOP}$ is received, but must be specifically reset by the CPU. $\overline{EOP}$ does however inhibit additional DMA cycles from occurring.

R2 Bit 0 - Arbitrate

This bit is set to indicate a desire to arbitrate for use of the SCSI bus. Before setting the Arbitrate bit, the SCSI Output Data Register (Write Register 0) must be written with the SCSI ID assigned to the arbitrating SCSI device. The bit position of register R0 which is set represents the priority number of the SCSI device, with bit 7 the highest priority. See the section on "Arbitration" for a full discussion of the L5380/L53C80 arbitration procedure.

WRITE ADDRESS 3 — Target Command Register

The Target Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the target. In addition, this register contains a read-only status flag useful in unambiguously determining when the last byte of a DMA transfer has actually been sent over the SCSI bus.

When operating as an initiator with DMA mode set, the ASSERT $\overline{MSG}$, ASSERT $\overline{C/D}$, and ASSERT $\overline{I/O}$ bits are used as a template to compare against the corresponding SCSI control signals provided by the target. A phase mismatch interrupt will be generated on the falling edge of the $\overline{REQ}$ input if the template does not match the state of the signals. Therefore the CPU should initialize these bits to the phase of the expected data transfer. An interrupt then will signal an intent by the target to change to a new phase. The SCSI information transfer phases and their associated direction of data transfer are given in Table 2.

TABLE 2. SCSI INFORMATION TRANSFER PHASES

MSG	C/D	I/O	Phase	Direction		
0	0	0	Data Out	Initiator	→	Target
0	0	1	Data In	Target	→	Initiator
0	1	0	Command	Initiator	→	Target
0	1	1	Status	Target	→	Initiator
1	0	0	Unused			
1	0	1	Unused			
1	1	0	Message Out	Initiator	→	Target
1	1	1	Message In	Target	→	Initiator

R3 Bits 7–4 - Not Used

R3 Bit 3 - Assert $\overline{REQ}$

When this bit is set, $\overline{REQ}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{REQ}$. Note that $\overline{REQ}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target.

R3 Bit 2 - Assert $\overline{MSG}$

When this bit is set, $\overline{MSG}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{MSG}$. Note that $\overline{MSG}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{MSG}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 1 - Assert $\overline{C/D}$

When this bit is set, $\overline{C/D}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{C/D}$. Note that $\overline{C/D}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{C/D}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 0 - Assert $\overline{I/O}$

When this bit is set, $\overline{I/O}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{I/O}$. Note that $\overline{I/O}$ will be asserted only if the TARGETMODE bit (R2 bit 6) is set, indicating that the L5380/L53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{I/O}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

WRITE ADDRESS 4 —
ID Select Register

The ID Select Register is a write-only register which is used to monitor for selection or reselection attempts to the L5380/L53C80. In arbitrating systems, an ID number is assigned to each SCSI device by setting a single bit position of the ID select register. Each SCSI data pin is inverted and compared with the corresponding bit in the ID Select Register. If any matches are found while a bus free condition exists and $\overline{SEL}$ is active, the L5380/L53C80 will generate an interrupt to indicate a selection or reselection. During selection or reselection, parity checking may be enabled by setting the Enable Parity Check bit (R2 bit 5). This interrupt may be masked by resetting all bits in this register.

WRITE ADDRESS 5 —
Start DMA Send

This is a dummy register. Writes to this location are detected and cause the L5380/L53C80 internal state machine to execute a DMA send operation. This location is used for either initiator or target DMA send. The DMAMODE bit (R2 bit 1) must be set prior to writing this location.

WRITE ADDRESS 6 —
Start DMA Target Receive

This is a dummy register. Writes to this location are detected and cause the L538/L53C80 internal state machine to execute a target DMA receive operation. The DMAMODE bit (R2 bit 1) and the TARGETMODE bit (R2 bit 6) must be set prior to writing this location.

WRITE ADDRESS 7 —
Start DMA Initiator Receive

This is a dummy register. Writes to this location are detected and cause the L5380/L53C80 internal state machine to execute an initiator DMA receive operation. The DMAMODE bit (R2 bit 1) must be set and the TARGETMODE bit (R2 bit 6) must be reset prior to writing this location.

B. READ OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/L53C80 internal registers for read operations as shown in Table 3.

READ ADDRESS 0 — Current SCSI Data Bus

The Current SCSI Data Bus Register allows the microprocessor to monitor the SCSI data bus at any time, by asserting CS and IOR with address lines A2–0 = 000. The SCSI data lines are not actually registered, but gated directly onto the CPU bus whenever address 000 is read by the CPU. Therefore, reads of this location should only be done when the SCSI data lines are guaranteed to be stable by the SCSI protocol. For systems which implement SCSI bus arbitration, this location is read to determine whether devices having higher priorities are also arbitrating. Programmed I/O data transfer uses this location for reading data transferred on the SCSI data bus. With parity checking enabled, SCSI data bus parity checking is done at the beginning of the read cycle for fast error detection. Note that the SCSI data bus is inverted to become active high when presented to the CPU.

READ ADDRESS 1 — Initiator Command Register

Reading bit 7 or bits 4–0 of the Initiator Command Register simply reflects the status of the corresponding bit in the register. Bits 6 and 5 are mapped to other signals as discussed below:

R1 Bit 6 - Arbitration In Progress

For this bit to be active, the ARBITRATE bit (R2 bit 0) must be set. When ARBITRATION IN PROGRESS is set, it indicates that the L5380/L53C80 has detected a bus free condition and is currently arbitrating for control of the bus. See the section on "Arbitration" for a complete discussion of the L5380/L53C80 arbitration mechanism. Resetting the ARBITRATE bit will reset ARBITRATION IN PROGRESS.

R1 Bit 5 - Lost Arbitration

For this bit to be active, the ARBITRATE bit (R2 bit 0) must be set. When LOST ARBITRATION is set, it indicates that the L5380/L53C80 has arbitrated for the SCSI bus (see R1 bit 6 above) and has detected the assertion of SEL by another (higher priority) device. The L5380/L53C80 responds to loss of arbitration by immediately discontinuing the arbitration attempt. Resetting the ARBITRATE bit will reset LOST ARBITRATION.

READ ADDRESS 2 — Mode Register

Reading the Mode Register simply reflects the status of the bits in that register.

READ ADDRESS 3 — Target Command Register

Reading the Target Command Register simply reflects the status of the bits in that register, except for bit 7, LAST BYTE SENT.

R3 bit 7 - Last Byte Sent

This read only bit indicates that the last byte of data loaded into the L5380/L53C80 during a DMA send operation has actually been transferred over the SCSI bus. Note that the end of process flag and the corresponding interrupt occur when this byte is loaded into the L5380/L53C80, but do not reflect whether it has actually been sent. This bit is not present in the NCR5380, but is present in the NCR53C80. Last Byte Sent is reset when the DMAMODE bit (R2 bit 1) is reset.

READ ADDRESS 4 — Current SCSI Control Register

The Current SCSI Control Register provides a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 100 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 5 — DMA Status Register

The DMA Status Register provides a means for the CPU to determine the status of a DMA transfer and to determine the cause of an interrupt. It also makes available the final two SCSI bus signals which are not included in the Current SCSI Control Register. The function of each individual bit is defined as follows:

R5 Bit 7 - End of DMA

When this bit is set, it indicates that a valid $\overline{EOP}$ has been received during a DMA transfer. A valid $\overline{EOP}$ occurs when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active for the minimum specified time. End of DMA is reset when the DMAMODE bit (R2 bit 1) is reset.

Note that for DMA send operations, an END OF DMA status indicates only that the last byte of the transfer is loaded into the Output Data Register of the sending device, not that it has actually been transferred over the SCSI bus. For this reason, the L5380/L53C80 provides an additional status bit; LAST BYTE SENT (R3 bit 7) which indicates that this final byte has been transferred to the receiving end. This bit is not present in the NCR5380.

Also, note that the DMAMODE bit is reset automatically whenever a loss of busy condition is detected, which in turn resets END OF DMA. Therefore

the DMA Status Register should be read prior to resetting the ASSERT $\overline{BSY}$ bit (R1 bit 3) at the conclusion of a DMA transfer.

R5 Bit 6 - DMA Request

This bit reflects the state of the DRQ (DMA Request) signal. In programmed I/O, this bit can be polled by the CPU to determine whether there is a pending request for byte transfer. For DMA send operations, DMA REQUEST is reset when $\overline{DACK}$ and $\overline{IOW}$ are simultaneously asserted. For DMA receive operations, simultaneous $\overline{DACK}$ and $\overline{IOR}$ will reset DMA REQUEST. DMA REQUEST is reset unconditionally when the DMAMODE bit (R2 bit 1) is reset.

R5 Bit 5 - Parity Error

This bit can only be set if ENABLE PARITY CHECK (R2 bit 5) is set. When enabled, the PARITY ERROR bit is set if incoming SCSI data in either initiator or target mode, or during selection phase, does not correctly reflect odd parity. PARITY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 4 - Interrupt Request

This bit reflects the state of the IRQ signal. The L5380/L53C80 asserts IRQ to generate an interrupt to the CPU. See the section on "Interrupts" for further information on the possible sources of interrupts in the L5380/L53C80. INTERRUPT REQUEST can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 3 - Phase Match

When this bit is set, it indicates that the $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ lines match the state of the ASSERT $\overline{MSG}$, ASSERT $\overline{C/D}$, and ASSERT $\overline{I/O}$ bits in the Target Command Register. PHASEMATCH is not actually registered, but represents a continuous comparison of these three phase bits to the corresponding internal register

TABLE 3. READ REGISTER CHART.

Address 0 — Current SCSI Data Bus

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	ARB. IN PRO-GRESS	LOST ARB.	ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C/D}$	ASSERT $\overline{I/O}$

Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{PARITY}$

Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ.	PARITY ERROR	INTER-RUPT REQ.	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Address 6 — Input Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 7 — Reset Error/Interrupt Register

7	6	5	4	3	2	1	0

6

locations. This bit is intended for use by the initiator to detect that the target device has changed to a different information transfer phase. When the L5380/L53C80 detects a phase mismatch, PHASEMATCH is reset, and information transfer to or from the SCSI bus is inhibited.

R5 Bit 2 - Busy Error

This bit can only be set if the MONITOR BUSY bit (R2 bit 2) is set. When set, BUSY ERROR indicates that the BSY pin has been false for a period at least equal to a bus settle delay (400 ns) When the BUSY ERROR condition is detected, all SCSI signal pins are disabled, and the DMAMODE bit (R2 bit 1) and bits 0–5 of the Initiator Command Register are reset. BUSY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bits 1, 0 - $\overline{ATN}$, $\overline{ACK}$

Like the Current SCSI Control Register, these bits provide a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 5 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 6 —
Input Data Register

This register acts as a temporary holding register for information received from the SCSI data bus during DMA transfers (DMAMODE bit, R2 bit 1 is set). In the initiator mode, the L5380/L53C80 latches the SCSI data when $\overline{REQ}$ goes active, while in the target mode data is latched when $\overline{ACK}$ goes active. The contents of this register represent the negation of the low-true SCSI data. The contents of the SCSI Input Data Register are gated onto the CPU data bus when $\overline{DACK}$ and $\overline{IOR}$ are simultaneously true, or by a CPU read of location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously, to prevent conflicting read operations. Parity may optionally be checked on the data as it is loaded into this register.

READ ADDRESS 7 —
Reset Error/Interrupt Register

This is a dummy register. Reads to this location are detected and used to reset the Interrupt Request Latch (IRQ signal) and the PARITY ERROR, INTERRUPT REQUEST, and BUSY ERROR latches (visible as bits 5, 4, and 2 of Register 5).

INTERRUPTS

The L5380/L53C80 generates interrupts to the CPU by setting the Interrupt Request Latch, which directly drives the IRQ (Interrupt Request) line. The IRQ output will reflect the state of the Interrupt Request Latch under all conditions except when TESTMODE (R1 bit 6) is active, when it is in a high impedance state. The Interrupt Request Latch may be reset by reading Address 7, the Reset Error/Interrupt Register. A read of this location also resets several error condition latches as discussed in the section on "Internal Registers."

Interrupts may be caused by any of six conditions, most of which may be masked by resetting enable bits in the appropriate registers. The following sections describe each interrupt type, its cause, and how it may be reset. Upon receiving an interrupt, the CPU may read the Current SCSI Control Register (R4) and the DMA Status Register (R5) to determine the cause of the interrupt. While the following discussions indicate the expected values of these registers following an interrupt, it is recommended that bits in these registers which are not germane to determining the cause of an interrupt be masked off in firmware prior to implementing a comparison. A typical operational sequence for an interrupt service routine is given at the end of this section.

SCSI Bus Reset Interrupt

A SCSI Bus Reset Interrupt occurs when the SCSI $\overline{RST}$ signal becomes active. This may be due to another SCSI device driving the $\overline{RST}$ line, or because the ASSERT $\overline{RST}$ bit (R1 bit 7) has been set, causing the L5380/L53C80 to drive the SCSI $\overline{RST}$ line. The value of the SCSI $\overline{RST}$ line is visible as R4 bit 7; however, this line is not latched and therefore may have changed state by the time the CPU responds to the interrupt and polls this location. For this reason a SCSI Bus Reset Interrupt should be assumed if no other interrupt condition is active when reading Registers 4 and 5.

The SCSI Bus Reset Interrupt is nonmaskable. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Selection/Reselection Interrupt

A Selection/Reselection Interrupt occurs when the SCSI $\overline{SEL}$ signal becomes active, the SCSI bus matches the bit set in the ID Select Register, and $\overline{BSY}$ has been false for at least a bus settle delay. When the $\overline{I/O}$ pin is as-serted, the interrupt should be interpreted as a reselection. The Selection/Reselection Interrupt may be masked by resetting all bits in the ID Select Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Loss of Busy Interrupt

A Loss of Busy Interrupt occurs when the SCSI $\overline{BSY}$ signal has been inactive for at least a bus settle delay (400 ns). The Loss of Busy Interrupt may be masked by resetting the MONITOR BUSY bit (R2 bit 2). Resetting MONITOR BUSY also prevents the BUSY ERROR latch (Read R5 bit 2) from being set. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Phase Mismatch Interrupt

A Phase Mismatch Interrupt occurs when the DMAMODE bit (R2 bit 1) is set, $\overline{REQ}$ is active on the SCSI bus, and the SCSI phase signals $\overline{MSG}$, $\overline{C/D}$, and $\overline{I/O}$ do not match the corresponding bits in the Target Command Register. This interrupt is intended for use by the initiator to detect a change of phase by the target during a DMA transfer. When operating as a target, the SCSI phase lines will normally be asserted via the Target Command Register, so no phase mismatch will be generated unless another SCSI device is erroneously driving the phase lines to an unintended state.

The result of the continuous comparison of the SCSI phase lines to the Target Command Register contents is visible as the PHASE MATCH bit (Read R5 bit 3). This flag operates irrespective of the state of DMAMODE and $\overline{REQ}$. As long as a phase mismatch condition persists, the L5380/L53C80 is prevented from recognizing active $\overline{REQ}$ inputs, and SCSI output data drivers are disabled.

The Phase Mismatch interrupt is nonmaskable, however it will only occur when operating in DMAMODE. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Parity Error Interrupt

A Parity Error Interrupt occurs when incorrect parity is detected during a read of the SCSI bus. Parity checking occurs under the following conditions: Parity is checked during a programmed I/O read of the Current SCSI Data Register (Read R0), when $\overline{CS}$ and $\overline{IOR}$ are active and the A2-0

TABLE 4. INTERRUPT READ VALUES

Read Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C/D}$	$\overline{I/O}$	$\overline{SEL}$	$\overline{PARITY}$
SCSI Bus Interrupt							
X	0	0	0	0	0	0	0
Selection/Reselection Interrupt							
0	0	0	X	X	1=RESEL	1	X
Loss of Busy Interrupt							
0	0	0	0	0	0	0	0
Phase Mismatch Interrupt							
0	1	1	X	X	X	0	X
Parity Error Interrupt							
0	X	X	X	X	X	X	X
End of DMA Interrupt							
0	1	X	X	X	X	0	X

Read Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ.	PARITY ERROR	INTERRUPT REQ.	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$
SCSI Bus Interrupt							
0	0	0	1	1	0	0	0
Selection/Reselection Interrupt							
0	0	0	1	X	0	X	0
Loss of Busy Interrupt							
0	0	0	1	X	1	0	0
Phase Mismatch Interrupt							
0	0	0	1	0	X	X	0
Parity Error Interrupt							
X	X	1	1	X	X	X	X
End of DMA Interrupt							
1	0	0	1	X	0	0	X

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lines are 000. Parity is also checked during DMA read operations (DMAMODE bit, R2 bit 1 is set) when $\overline{ACK}$ is active for target receive, or $\overline{REQ}$ is active for initiator receive.

The PARITY ERROR latch is set when parity error checking is enabled and one of the above parity error conditions is encountered. This latch is visible as bit 5 of the DMA Status Register (Read R5). The Parity Error Interrupt may be masked and setting of the PARITY ERROR latch prevented by resetting the ENABLE PARITY CHECK bit (Write R2 bit 5). The PARITY ERROR latch can be reset by reading the Reset Error/Interrupt Register (Read R7). The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

End of DMA Interrupt

An End of DMA Interrupt occurs when a valid $\overline{EOP}$ (End of Process) signal is detected during a DMA transfer. $\overline{EOP}$ is valid when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously asserted for the minimum specified time. $\overline{EOP}$ inputs not occurring during I/O read or write operations are ignored.

The End of DMA latch is set whenever the DMAMODE bit (R2 bit 1) is set and a valid $\overline{EOP}$ is received. This latch is visible as bit 7 of the DMA Status Register (Read R5). The End of DMA Interrupt may be masked by resetting the ENABLE EODMA INTERRUPT bit (Write R2 bit 3). This bit does not affect the END OF DMA latch, however. The End of DMA latch can be reset by resetting the DMAMODE bit in the Mode Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

DATA TRANSFERS

The L5380/L53C80 supports programmed I/O under CPU control or DMA transfer via a DMA controller when transferring information to and from the SCSI data bus. Programmed I/O can be implemented entirely in firmware or using minimum external logic for accessing the appropriate registers. Under DMA control, the L5380/L53C80's DMA interface logic and internal state machines provide the necessary control of the $\overline{REQ}$-$\overline{ACK}$ handshake. Each type of transfer is fully described in the following sections.

Programmed I/O

Two forms of programmed I/O are supported by the L5380/L53C80. For normal programmed I/O, the SCSI handshake is accomplished by setting bits in the Initiator or Target Command registers to assert SCSI control lines, and polling the Current SCSI Control and DMA Control registers for the appropriate responses. Since for this method the control is contained in firmware, the cycle times are relatively slow. It is most appropriate for transferring small blocks of data such as SCSI command blocks or messages, where the overhead of

TABLE 5. TYPICAL INTERRUPT SERVICE ROUTINE POLLING SERVICE

Read Address 5 > TEMP	: Read DMA Status Reg to variable TEMP
IF TEMP "AND" HEX (10) = 0 THEN GO TO NEXT DEVICE	: IRQ not active, so L5380/L53C80 was not the source of this interrupt
TEMP "AND" HEX (AC) → TEMP	: Mask off irrevelant bits
IF TEMP > HEX (7F) THEN GO TO EODMA	: End of DMA Interrupt
IF TEMP > HEX (1F) THEN GO TO PARERR	: Parity Error Interrupt
IF TEMP > HEX (03) THEN GO TO BYSERR	: Loss of Busy Interrupt
IF TEMP ≠ HEX (00) THEN GO TO PHASERR	: Phase Mismatch Interrupt
Read Address 4 → TEMP	: Read Current SCSI Control Reg to variable TEMP
TEMP "AND" HEX (06) → TEMP	: Mask off irrevelant bits
IF TEMP = HEX (06) THEN GO TO RESEL	: Reselection Interrupt
IF TEMP = HEX (02) THEN GO TO SEL	: Selection Interrupt
IF TEMP = HEX (00) THEN GO TO RESET	: SCSI Bus Reset Interrupt

setting up a DMA controller could be significant.

Pseudo DMA

An alternate method of programmed I/O allows the state machines of the L5380/L53C80 to handle the SCSI handshake, thereby improving performance in systems which do not employ a hardware DMA controller. To implement Pseudo DMA, the DMAMODE bit is set. The CPU polls the DRQ bit in the DMA Control Register to determine when a byte should be written to or read from the L5380/L53C80. When reading or writing, external logic must be used to decode the L5380/L53C80 location and produce $\overline{DACK}$, since it is used by the internal state machines. Also, $\overline{CS}$ must be suppressed since it may not be asserted simultaneously with $\overline{DACK}$.

Normal DMA Mode

Normal DMA mode is obtained when the DMAMODE bit is set but the BLOCKMODE bit is reset. The DMA process is started by writing to the Start DMA Send, Start DMA Initiator Receive, or Start DMA Target Receive locations as appropriate. Once started, the internal state machines of the L5380/L53C80 manage the $\overline{REQ}$ - $\overline{ACK}$ handshake protocol, as well as the DRQ-$\overline{DACK}$ handshake with the DMA controller.

The L5380/L53C80 will assert DRQ whenever it is ready to transfer a byte to or from the DMA controller. In response to DRQ, the controller asserts $\overline{DACK}$ and $\overline{IOR}$ to read the byte, or $\overline{DACK}$ and $\overline{IOW}$ to write a byte to the L5380/L53C80. For write operations, the byte is latched at the rising edge of the logical AND of $\overline{DACK}$ and $\overline{IOW}$. The transfer can be terminated by asserting $\overline{EOP}$ during a read or write operation, or by resetting the DMAMODE bit.

Block DMA Mode

When the BLOCKMODE bit is set, the DMA handshake is no longer dependent on interlocked DRQ-$\overline{DACK}$ cycles. Instead, the DMA controller may be allowed to free-run, with data flow throttled by inserting "wait-states" in the DMA transfer to or from the L5380/L53C80. Wait-states, which are idle clock cycles inserted during the I/O read or write operation, are inserted by the DMA controller until the READY output of the L5380/L53C80 goes true, allowing the bus cycle to conclude.

The READY output will be deasserted under the following conditions: For send operations, READY will be false whenever the Output Data Register contains a byte which has not been transferred over the SCSI bus. This allows the DMA controller to access RAM to fetch the next byte, but postpones the end of the CPU bus cycle until the previous byte has been transferred, freeing the Output Data Register to receive it.

For receive operations, READY will be false whenever the Input Data Register is empty. This allows the DMA controller to address the RAM for a write operation, but postpones the end of the CPU bus cycle until the incoming byte is stored in the Input Data Register and is available on the CPU bus.

Note that when blockmode is employed, $\overline{DACK}$ may optionally remain asserted throughout the DMA transfer, since it is not used in an interlocked DMA handshake. (Its interlock function is replaced by $\overline{IOR}$ or $\overline{IOW}$.) Also, DRQ will be asserted in the normal way when operating in blockmode. To gain the abovementioned performance benefits, it should be used only to initiate the first byte transfer, with READY used to throttle succeeding transfers. This methodology is compatible with DMA controllers such as the Intel 8237 and AMD Am9516/9517.

In summary, blockmode operation offers the potential for improved transfer rates by overlapping the DMA memory access with the SCSI transfer. This is of particular value when used with DMA controllers capable of "flyby" operation, where the data is transferred directly from memory to the peripheral, and does not pass through the DMA controller itself. This transfer rate gain is achieved at the expense of locking up the CPU bus for a time equal to the SCSI transit time of the entire block. This may be strongly preferable in some systems where net disk access time is a crucial performance factor. Also, the time required to arbitrate for the CPU bus on a byte-by-byte basis may well be longer than the cycles wasted waiting for SCSI transfers to take place, especially with fast peripherals which operate from a high speed sector buffer.

Terminating DMA Transfers

DMA transfers, either normal or blockmode, may be terminated in a number of ways. The following sections describe these methods, along with providing information about correct sequencing of various signals to effect a clean exit from a DMA process.

$\overline{EOP}$ Signal

The $\overline{EOP}$ signal is usually generated by a DMA controller to indicate that its transfer counter has decremented to zero. In order to be recognized by the L5380/L53C80, it should be asserted simultaneously with the $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals corresponding to the last byte in the transfer. Note that in the case of send operations, asserting $\overline{EOP}$ indicates to the L5380/L53C80 that SCSI transfers should cease after transmission of the

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byte loaded while $\overline{EOP}$ is asserted. In order to determine when this last byte has actually been sent, the LAST BYTE SENT flag in the Target Command Register may be examined. This flag is not present in the NCR implementation of the 5380, but is available in the 53C80, a non-pin-compatible variant. The $\overline{EOP}$ input does not reset the DMAMODE bit, but after transmission of the last byte causes the internal state machine to return to an idle condition, so that no further SCSI handshaking will occur until another transmission is explicitly initiated. Note that the NCR version of the 5380, upon receiving an $\overline{EOP}$, will stop asserting DRQ, but will continue to issue $\overline{ACK}$ in response to additional $\overline{REQ}$ inputs, potentially causing data loss if the target initiates another data transmission without an intervening phase change. The L5380/L53C80 prevents this spurious DMA handshake from occurring.

DMAMode Bit

Resetting the DMAMODE bit in the Mode Register causes a hard reset of the internal DMA state machines, and thus an effective termination of a DMA transfer. Since unlike the $\overline{EOP}$ case the state machine is not allowed to exit gracefully, care must be taken in the timing of DMAMODE reset.

For receive operations, the DMAMODE bit should be reset after the last DRQ is received, but prior to asserting $\overline{DACK}$ to prevent an additional $\overline{REQ}$ or $\overline{ACK}$ from occurring. For normal DMA mode, resetting this bit will cause DRQ to go inactive. However the last byte received remains in the SCSI Input Data Register and may be read either by the normal $\overline{DACK}$ and $\overline{IOR}$ DMA read or using a CPU read of Address 6. For blockmode DMA, READY will remain asserted when DMAMODE is reset, allowing the DMA controller to retrieve the last byte in the normal fashion. The NCR version of the 5380 fails to keep ready asserted when DMAMODE is reset, potentially causing deadlock on the CPU bus.

Bus Phase Mismatch

When operating in DMAMODE as an initiator, a bus phase mismatch can be used to terminate a data transfer. If the $\overline{C/D}$, $\overline{I/O}$, and $\overline{MSG}$ lines fail to match the corresponding bits in the Target Command Register, it will prevent recognition of $\overline{REQ}$, and will disable the SCSI data and parity output drivers. Also, when $\overline{REQ}$ becomes active, an interrupt will be generated. Because $\overline{REQ}$ is not recognized, the effect is to stop the DMA transfer, although the state machine does not return to idle until either DMAMODE is reset or a valid $\overline{EOP}$ is received.

One caution should be observed when using phase changes to end DMA transfers: While this method obviates the need for the initiator to keep a transfer counter, it depends on the target causing a phase change between any two consecutive information transfer phases. Since this is not required by the protocol, it must be guaranteed by the target software. Otherwise the target may begin a new information transfer without the initiator recognizing the boundary between the two.

ARBITRATION

The L5380/L53C80 contains on-chip hardware to assist in arbitrating for the SCSI bus. This arbitration logic cooperates with the host firmware to effect SCSI arbitration, as described in the following paragraphs:

The SCSI arbitration timeline begins with detection of a bus free condition at time t0. Bus free is defined as BSY and $\overline{SEL}$ inactive for at least a bus settle delay (400 ns). Following the bus settle delay, the SCSI device must wait an additional bus free delay of 800 ns, for a total of 1200 ns after t0, prior to driving any signal. Thus a minimum of 1200 ns must elapse from initial deassertion of $\overline{BSY}$ to the beginning of an arbitration attempt. A final constraint is that arbitration may not begin if more than a bus set delay (1800 ns) has elapsed since $\overline{BSY}$ became active (arbitration began), corresponding to 2200 ns after t0.

The CPU indicates a desire to arbitrate by setting the ARBITRATE bit (R2 bit 0.) When ARBITRATE is set, the L5380/L53C80 will monitor the state of $\overline{BSY}$ and $\overline{SEL}$ to detect a bus free condition. The actual implementation uses an internal delay line to provide a time reference for detection of a bus free condition. This delay is nominally 800 ns during which $\overline{BSY}$ and $\overline{SEL}$ must be inactive. This time represents the center of the window between the Bus Settle Delay (400 ns) and the Bus Free Delay (400 + 800 = 1200 ns). When Bus Free is detected, the L5380/L53C80 waits for an additional time of nominally 900 ns (1700 ns nominal since t0) and asserts $\overline{BSY}$ and the contents of the Output Data Register. This time represents the center of the 1200 ns–2200 ns window between the earliest and latest legal arbitration attempt. Since the actual delays are process and temperature dependent, they will vary in practice, but will always remain well within the specified limits.

Once arbitration has begun ($\overline{BSY}$ and the Output Data Register asserted,) the ARBITRATION IN PROGRESS bit (R1 bit 6) will be set, allowing the CPU to detect the fact that arbitration has begun. The CPU should then wait one arbitration delay (2.2 µs) before reading the bus to determine whether

arbitration has been won or lost. The LOST ARBITRATION bit (R2 bit 7) will be active if the L5380/L53C80 has detected $\overline{SEL}$ active on the SCSI bus, indicating that another SCSI device has declared itself the winner of the arbitration. $\overline{SEL}$ active also disables the SCSI output drivers, allowing the winning arbitrator to proceed with its transfer.

BUG FIXES/ENHANCMENTS

The NCR5380 and the Am5380 have some architectural bugs, both published and unpublished. The **Logic Devices L5380/L53C80** was designed to eliminate these bugs while maintaining pin and architectural compatibility. A list of these errors along with solutions implemented in the L5380/L53C80 is itemized below.

1. When executing blockmode DMA send operations, the READY signal is intended to insert memory wait states as a mechanism to throttle data transfer, with the DMA controller in a free-running loop. The NCR/Am5380 erroneously allows the contents of the Output Data Register to be overwritten by subsequent bytes prior to acknowledgment of the current byte by the SCSI receiver. This causes loss of data when operating in blockmode if the sender's DMA cycle is faster than the receiver's.

2. Assertion of $\overline{EOP}$ during blockmode DMA transfers fails to cause assertion of READY in the NCR/Am5380. This may prevent the CPU from becoming bus master and can result in lockup of the CPU bus in a not-ready state. In block DMA send mode when $\overline{EOP}$ is received, the L5380/L53C80 reasserts READY immediately after transmitting the final byte. For receive mode, READY is asserted immediately.

3. When a valid $\overline{EOP}$ is detected, the NCR/Am5380 prevents assertion of additional DRQ's, but continues to respond to SCSI handshakes. This means that additional data transmitted without phase change may be lost. The L5380/L53C80, like the NCR/Am5380 remains in DMAMODE after an $\overline{EOP}$. However, the internal state machine returns to an idle condition and does not respond to additional SCSI handshake attenpts until another data transfer is explicitly initiated.

4. When operating as an initiator in DMAMODE, the NCR/Am5380 leaves $\overline{ACK}$ asserted after receipt of a valid $\overline{EOP}$, requiring the CPU to deassert it. When a valid $\overline{EOP}$ is detected, the L5380/L53C80 deasserts $\overline{ACK}$ properly.

5. If the NCR/Am5380 is not terminated on the SCSI side, the floating $\overline{RST}$ pin will cause spurious interrupts. The L5380/L53C80 contains internal high value pullups to set unterminated SCSI pins to the inactive state.

6. During DMA send operations, when a valid $\overline{EOP}$ signal is received by the NCR/Am5380, no convenient indication exists to indicate that the last byte of data (loaded simultaneously with EOP) has in fact been successfully transmitted. The L5380/L53C80 provides LAST BYTE status bit mapped to bit 7 of the Target Command Register. This bit will be set after a valid $\overline{EOP}$ has occurred, and the final byte has been transmitted successfully.

7. During the reselection phase, the NCR/AM5380 may reset the reselection interrupt if the contents of the Target Command Register do not match the current SCSI bus phase. The L5380/L53C80 does not spuriously reset this interrupt.

8. In the NCR/Am5380, the phase mismatch interrupt is captured in an edge triggered fashion on the active edge of $\overline{REQ}$. During reselection, this interrupt might not be generated even though a phase change has occurred. The reason for this is as follows:

- The initiator DMAMODE bit must be set in order to receive a phase-match interrupt.
- However, the DMAMODE bit cannot be set unless $\overline{BSY}$ is active.
- $\overline{BSY}$ will be driven active by the target only after the relesection has occurred.
- Once $\overline{BSY}$ has been asserted by the target, it may then assert $\overline{REQ}$ before the initiator has set the DMAMODE bit, and the initiator will then fail to generate an interrupt.

The L5380/L53C80 interrupt latch will be set if a phase mismatch condition exists when the later of $\overline{REQ}$ or DMAMODE become active. In this way, the mismatch will always be detected, even if the target asserts request before the initiator sets DMAMODE.

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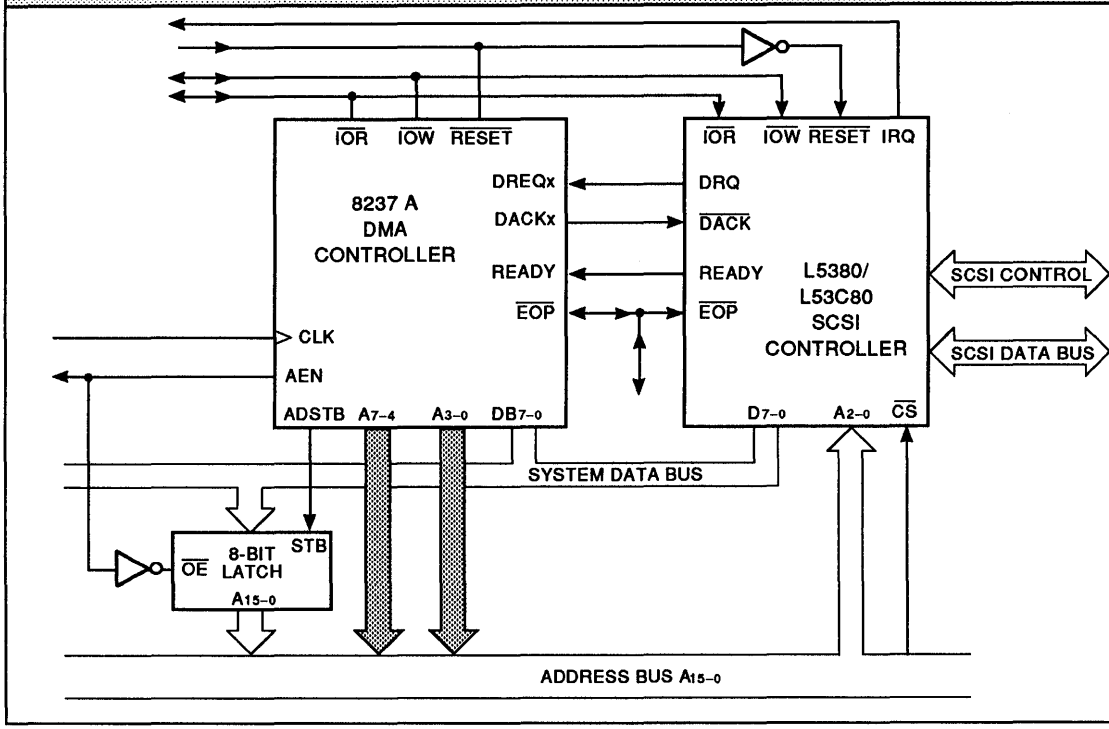
DMA Interface with 8237 A.

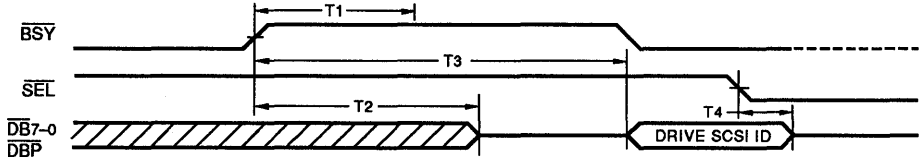


SWITCHING CHARACTERISTICS

Arbitration Timing *(Units measured in ns — except where noted)*

Symbol	Parameter	Commercial Min	Commercial Max	Military Min	Military Max
T1	$\overline{BSY}$ False Duration to Detect Bus Free Condition	0.4 µs	1.1 µs	0.4 µs	1.1 µs
T2	SCSI Bus Clear (High Z) from $\overline{BSY}$ False		1.1 µs		1.1 µs
T3	Arbitrate ($\overline{BSY}$ and SCSI ID Asserted) from $\overline{BSY}$ False (Bus Free Detected)	1.2 µs	2.2 µs	0.8 µs	2.4 µs
T4	SCSI Bus Clear (High Z) from $\overline{SEL}$ True (Lost Arbitration)		60		60

Arbitration Waveforms

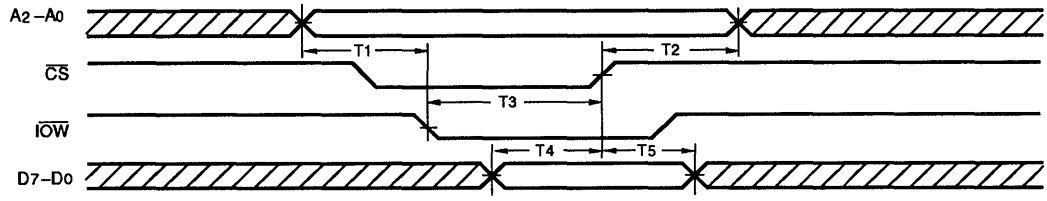


SWITCHING CHARACTERISTICS

A. CPU Write Cycle Timing *(Units measured in ns)*

		Commercial				Military	
		2 Mbytes/sec		4 /Mbytes/sec		2 Mbytes/sec	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
T1	Address Setup to Write Enable	10		5		10	
T2	Address Hold from End of Write Enable	0		0		0	
T3	Width of Write Enable	40		20		40	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	10		5		10	

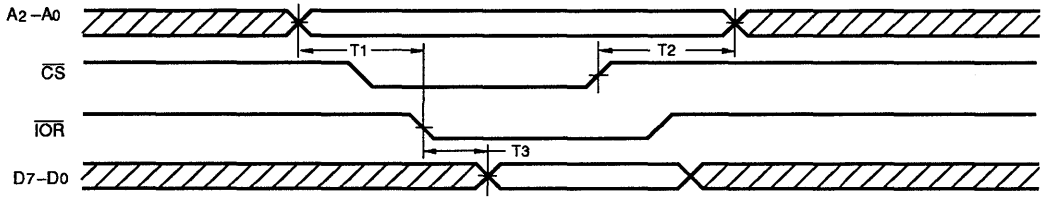
A. CPU Write Cycle Waveforms



B. CPU Read Cycle Timing *(Units measured in ns)*

		Commercial				Military	
		2 Mbytes/sec		4 /Mbytes/sec		2 Mbytes/sec	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
T1	Address Setup to Read Enable	10		5		10	
T2	Address Hold from End of Read Enable	0		0		0	
T3	Data Access Time from Read Enable		50		20		50

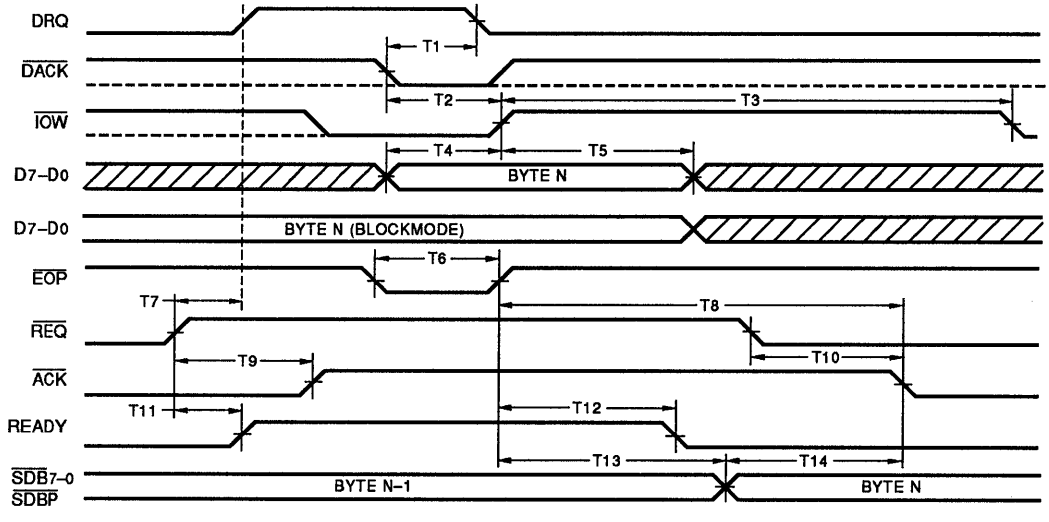
B. CPU Read Cycle Waveforms



C. DMA Write Initiator Send Timing *(Units measured in ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 /Mbytes/sec Min	Commercial 4 /Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
The following apply for all DMA Modes							
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30		60
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20		60	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	15		5		15	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20		50	
T9	$\overline{REQ}$ False to $\overline{ACK}$ False		90		45		90
T13	End of Write Enable to Valid SCSI Data		65		45		65
T14	SCSI Data Setup Time to $\overline{ACK}$ True	60		65		60	
The following apply for Normal DMA Mode only							
T7	$\overline{REQ}$ False to DRQ True		60		30		60
T8	$\overline{DACK}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		140		140		140
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{DACK}$ False)		70		35		70
The following apply for BLOCKMODE DMA only							
T3	$\overline{IOW}$ Recovery Time	40		20		40	
T8	$\overline{IOW}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		140		140		140
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{IOW}$ False)		70		35		70
T11	$\overline{REQ}$ False to READY True		60		30		60
T12	$\overline{IOW}$ False to Ready False		70		35		70

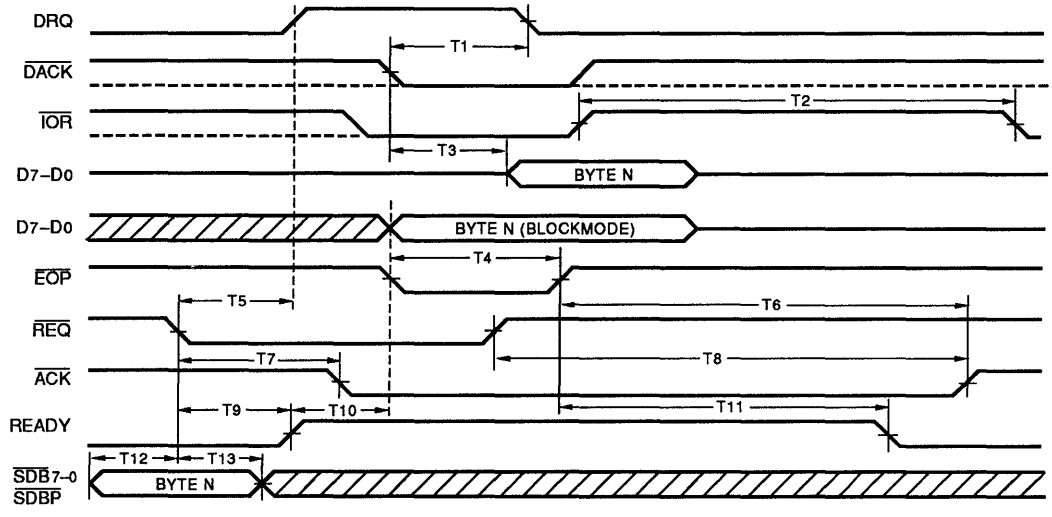
C. DMA Write Initiator Send Waveforms



D. DMA Read Initiator Receive Timing *(Units measured in ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 /Mbytes/sec Min	Commercial 4 /Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
	The following apply for all DMA Modes						
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30		60
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20		60
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20		50	
T7	$\overline{REQ}$ True to $\overline{ACK}$ True		70		35		70
T12	SCSI Data Setup Time to $\overline{REQ}$ True	20		5		20	
T13	SCSI Data Hold Time from $\overline{REQ}$ True	15		5		15	
	The following apply for Normal DMA Mode only						
T5	$\overline{REQ}$ True to DRQ True		60		30		60
T6	$\overline{DACK}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45		90
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)		80		45		80
	The following apply for BLOCKMODE DMA only						
T2	$\overline{IOR}$ Recovery Time	40		20		40	
T6	$\overline{IOR}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45		90
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{IOR}$ False)		80		45		80
T9	$\overline{REQ}$ True to READY True		60		30		60
T10	READY True to CPU Data Valid		15		15		15
T11	$\overline{IOR}$ False to Ready False		70		35		70

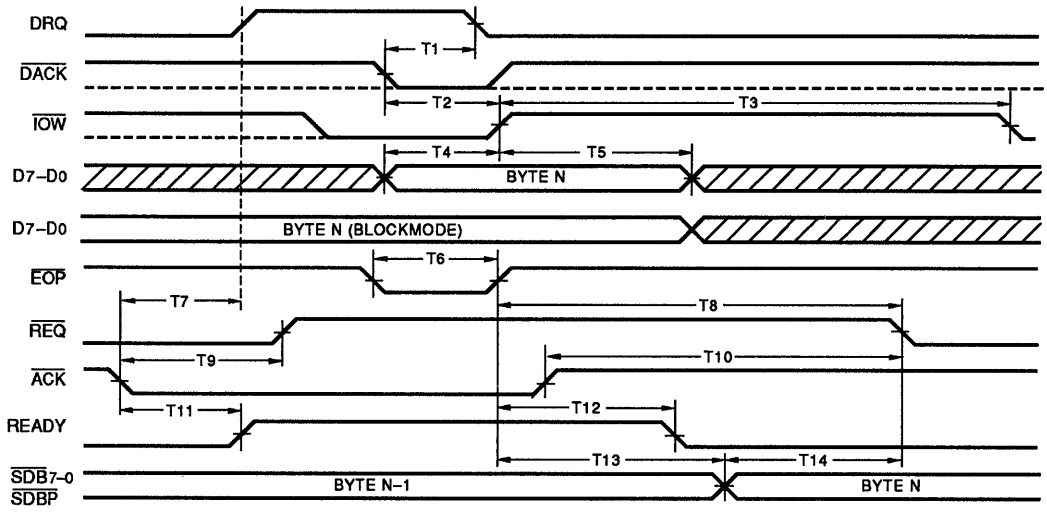
D. DMA Read Initiator Receive Waveforms



E. DMA Write Target Send Timing *(Units measured in ns)*

Symbol	Parameter	Commercial				Military	
		2 Mbytes/sec		4 /Mbytes/sec		2 Mbytes/sec	
		Min	Max	Min	Max	Min	Max
The following apply for all DMA Modes							
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30		60
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20		60	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	15		5		15	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20		50	
T9	$\overline{ACK}$ True to $\overline{REQ}$ False		90		45		90
T13	End of Write Enable to Valid SCSI Data		60		45		60
T14	SCSI Data Setup Time to $\overline{REQ}$ True	60		65		60	
The following apply for Normal DMA Mode only							
T7	$\overline{ACK}$ True to DRQ True		60		30		60
T8	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		130		130		140
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		70		35		70
The following apply for BLOCKMODE DMA only							
T3	$\overline{IOW}$ Recovery Time	40		20		40	
T8	$\overline{IOW}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		130		130		140
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOW}$ False)		70		35		70
T11	$\overline{ACK}$ True to READY True		60		30		60
T12	$\overline{IOW}$ False to Ready False		70		35		70

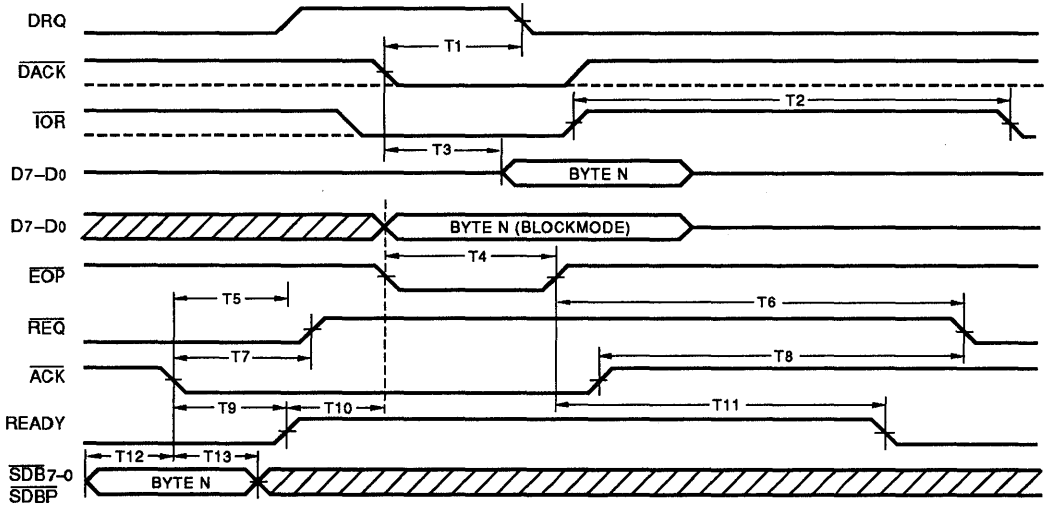
E. DMA Write Target Send Waveforms



F. DMA Read Target Receive Timing *(Units measured in ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 /Mbytes/sec Min	Commercial 4 /Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
The following apply for all DMA Modes							
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30		60
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20		60
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20		50	
T7	$\overline{ACK}$ True to $\overline{REQ}$ False		70		35		70
T12	SCSI Data Setup Time to $\overline{ACK}$ True	20		5		20	
T13	SCSI Data Hold Time from $\overline{ACK}$ True	15		5		15	
The following apply for Normal DMA Mode only							
T5	$\overline{ACK}$ True to DRQ True		60		30		60
T6	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45		90
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		80		45		80
The following apply for BLOCKMODE DMA only							
T2	$\overline{IOR}$ Recovery Time	40		20		40	
T6	$\overline{IOR}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45		90
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOR}$ False)		80		45		80
T9	$\overline{ACK}$ True to READY True		60		30		60
T10	READY True to CPU Data Valid		15		15		15
T11	$\overline{IOR}$ False to Ready False		70		35		70

F. DMA Read Target Receive Waveforms



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... −65°C to +150°C
V_{CC} supply voltage with respect to ground ..... −0.5 V to +7.0 V
Output voltage ..... 0.0 to V_{CC}
Input voltage ..... 0.0 to 5.5 V
I_{OL} Low Level Output Current (SCSI Bus) ..... 48 mA
I_{OL} Low Level Output Current (other pins) ..... 8 mA
I_{OH} High Level Output Current (other pins) ..... −4 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

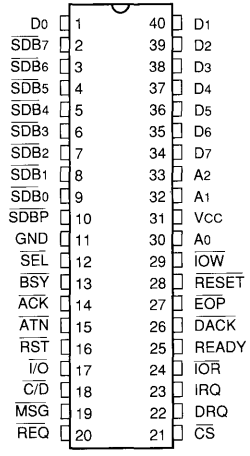
Electrical Characteristics *Over Operating Conditions*

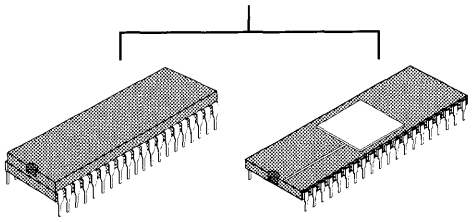
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Low Level Input Voltage		0.0		0.8	V
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{OL}	Low Level Output Voltage (SCSI bus)	V_{CC} = Min, I_{OL} = 48 mA			0.5	V
V_{OL}	Low Level Output Voltage (other pins)	V_{CC} = Min, I_{OL} = 8 mA			0.5	V
VOH	High Level Output Voltage (other pins)	V_{CC} = Min, I_{OH} = −4 mA	3.5			V
I_{IN}	Input Current*	V_{CC} = Max, V_{IN} = 0 – V_{CC} (SCSI bus)			65	µA
I_{IN}	Input Current*	V_{CC} = Max, V_{IN} = 0 – V_{CC} (other pins)			20	µA
I_{CC}	Supply Current	V_{CC} = Max, V_{IH} = 2.4, V_{IL} = 0.4, 4 MHz cycle, No Load, No Termination		10	20	mA
I_{CC}	Supply Current Quiescent	As above, inputs stable			1.0	mA

* Not tested at low temperature extreme.

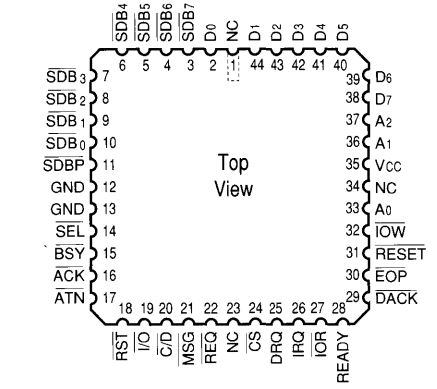
L5380 — ORDERING INFORMATION

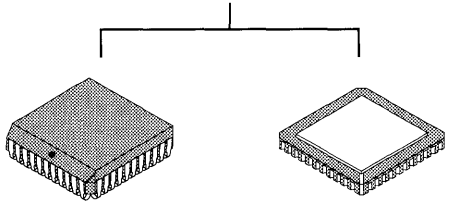
40-pin





44-pin



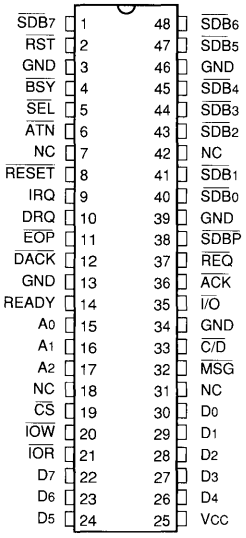


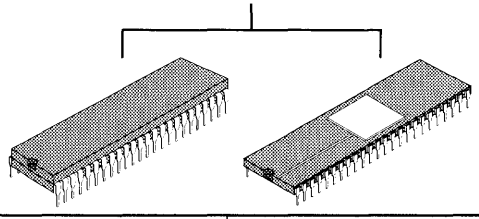
Mbytes/ sec	Plastic DIP (P3)	Sidebraze Hermetic DIP (D3)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
4	L5380PC4	L5380DC4	L5380JC4	L5380KC4
2	" " PC2	" " DC2	" " JC2	" " KC2
	–55°C to +125°C — COMMERCIAL SCREENING			
2		L5380DM2		L5380KM2
	–55°C to +125°C — EXTENDED SCREENING			
2		L5380DME2		L5380KME2
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
2		L5380DMB2		L5380KMB2

6

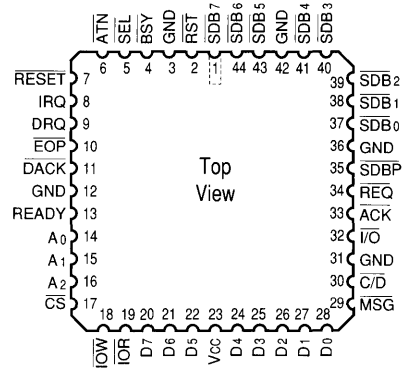
L53C80 — ORDERING INFORMATION

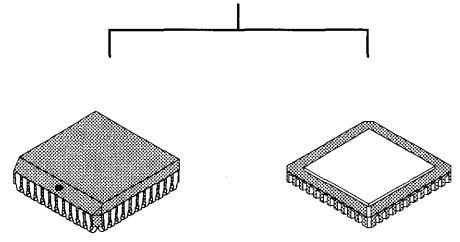
48-pin





44-pin





Mbytes/ sec	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
4	L53C80PC4	L53C80DC4	L53C80JC4	L53C80KC4
2	" " PC2	" " DC2	" " JC2	" " KC2
	–55°C to +125°C — Commercial Screening			
2		L53C80DM2		L53C80KM2
	–55°C to +125°C — Extended Screening			
2		L53C80DME2		L53C80KME2
	–55°C to +125°C — MIL-STD-883 Compliant			
2		L53C80DMB2		L53C80KMB2

Ordering Information

Memory Products

FIFO Memory Products

Memory Modules

Logic Products

Peripheral Products

Quality and Reliability 7

Technology and Design Features

Packaging

Application Notes

Technical Articles

Sales Offices

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7

Overview — Commitment to Quality

Management Commitment Statement

A successful quality program requires that every employee act as a member of the quality organization. This applies particularly to the management team who establish acceptable behavior by their actions. Bill Volz, President/CEO of Logic Devices Incorporated encourages active participation of all departments in a quality oriented operation.

At Logic Devices, the quality department strives to maintain a proactive relationship with Manufacturing, Design, Marketing, and Sales emphasizing training and procedural controls. Training and good communication allow employees to understand which practices lead to good quality and reliability and make them willing participants in the quality program. This attitude has allowed Logic Devices to continually improve the quality of its product line.

Organization

The Quality/Reliability Department reports directly to the President/CEO. The quality operation is divided into two functions:

1. Quality Administration
2. Reliability Engineering

Quality Administration performs all inspections/Q.A. monitors in assembly/test operations including incoming inspection of all direct materials. Q.A. Administration also includes the document control function.

The Reliability Engineering function is responsible for assuring that all products manufactured by Logic Devices meet our rigid standards for reliability. Activities that support this function include qualifications of new products, reliability monitor testing, failure analysis, and corrective action.

Documentation

All manufacturing and Q.A. procedures are controlled in the document control area and are available in controlled binders located in the appropriate manufacturing areas. In addition, the program plans for the quality and reliability functions are described in individual manuals:

Quality Manual. The quality function is described in the quality program plan as outlined in the Quality Manual. The program plan has been designed to the requirements of Appendix A of Mil-M-38510.

Reliability Manual. The reliability of Logic Devices' products is among the best in the industry and will continue to be. The Reliability Manual has been created to insure that we maintain high visibility of reliability data. This manual also describes the reliability function and goals at Logic Devices.

Mil-Std-883C. All products to be sold as 883C compliant are manufactured to this specification. As new revisions are released, they are evaluated and changes implemented as required.

Mil-M-38510. This document is referenced continuously by Mil-Std-883C and specifically defines program requirements for compliance to 883C programs.

Available Processing Flows

Logic Devices offers many processing flows to provide the best combination of reliability assurance and cost. Available flows are:

1. Commercial Plastic Flow.
2. Commercial Plastic Flow with 48 hr burn-in.
3. Commercial Hermetic Flow — 0° to +70°C.
4. Commercial Hermetic Flow — -55°C to +125°C.
5. Hi Rel Hermetic Flow — 0°C to +70°C with 48 hr burn-in.
6. Hi Rel Extended Flow — Per Logic Devices Flow.
7. Hi Rel 883C Flow — Per Mil-Std-883C, Methods 5004 and 5005.

Samples

Logic Devices on occasion provides samples of its products to customers for the purpose of assessing their suitability for the end application. Samples fall into two categories, depending on the maturity of the device in question. For devices already in production, the devices provided as samples will be pulled from inventory, and will have undergone the assembly flows and qualifications detailed elsewhere in this section.

In the case of new products however, it is often desirable to provide samples to a customer before a complete assessment of the performance and reliability of the new product has been made. Logic Devices' procedure is to label such devices with the words "ENGINEERING SAMPLE" or a contraction thereof. It is important for the customer who accepts engineering samples for evaluation to understand the limitations of the screening which these devices undergo.

In general, devices marked with "Engineering Sample" will not have undergone a reliability assessment. In addition, the characterization of the device, and therefore the electrical specifications to which it will ultimately be guaranteed, may still be evolving. The testing of engineering samples is at the sole discretion of Logic Devices product engineering, but generally will include elevated temperature AC testing with a limited class of patterns. A data sheet prominently marked "PRELIMINARY" will be provided with the samples as a means for the customer to understand the electrical limits to which the samples have been tested. However, the data sheet and test

LOGIC

DEVICES INCORPORATED

Reliability Manual

Introduction

Logic Devices Incorporated is committed to a reliability program plan that insures the highest reliability possible on it's CMOS technology. At Logic we realize that reliability is the product of designs carefully matched to well characterized and controlled processes with all manufacturing materials tightly controlled. Logic is committed to long term relationships with our customers and believe that reliability is one of their highest priorities.

This manual contains the reliability program plan for Logic Devices and data that is gathered through new product qualifications and ongoing reliability monitors. Device qualifications reference MIL-STD-883C, Method 5005, and JEDEC-STD-22B. These standards establish the criteria for qualifying product in military and commercial applications. This publication is updated quarterly.

Reliability Methods

Definition of Reliability

Reliability of an integrated circuit is the probability that it will perform it's defined functions in the operating environment for a reasonable period of time. This definition becomes more useful when broken into its component parts:

Defined Functions

Typically established by the manufacturer's data sheet or customer specification.

Operating Environment

Consisting of temperature, humidity, voltage, pressure, etc.

Reasonable Period of Time

Devices are expected to provide long term operation without failure. Evaluation of time to failure is an indication of reliability.

Probability

Statistical evaluation of time to failure data allow prediction of a device's long term reliability to a certain confidence level.

Reliability Indicators

Semiconductor reliability is typically expressed in terms of failure rate. Common methods of expressing failure rates in this industry are:

1. Mean Time to Failure (MTTF).
2. Mean Time Between Failures (MTBF).
3. Percent failures/1000 hours.
4. FIT rate – Failures in 10^9 hours.

Failure rate is the ratio of device failures to the total number of device hours. The reciprocal of failure rate is MTBF. The probability that a device will operate beyond the MTBF is expressed as:

$$R = e^{-t/M} \text{ or } 1/e^{t/M} \; ; \qquad (1)$$

where

R = reliability,
t = operating time,
M = MTBF.

Acceleration Factors

Under normal operating conditions an integrated circuit may operate well beyond our lifetime without failure, making data collection impractical. Placing devices in environments of increased temperature along with other stress conditions is known to accelerate failure mechanisms allowing for collection of data that will approximate the longer term failure time. Extended temperature exposure accelerates the physiochemical reactions associated with device failure. A mathematical expression known as the Arrhenius Equation makes it possible to calculate a reaction rate and therefore an acceleration factor.

$$R(\text{reaction rate}) = R_0 \exp(Ea/KT) \; , \qquad (2)$$

where

R_0 = a constant,
Ea = the activation energy,
K = Boltzmans Constant,
T = temperature in degrees Kelvin (°C + 273°C).

Assuming a linear reaction in time, the product of reaction rate and fail time at one temperature will equal the product of reaction rate and fail time at a second temperature:

$$R_1t_1 \text{ for } T_1 = R_2t_2 \text{ for } T_2 \qquad (3)$$

This allows the calculation of an acceleration factor:

$$AF = t_2/t_1 = e^{(Ea/K)(1/t2 - 1/t1)} \qquad (4)$$

By knowing the time to failure for the accelerated temperature it is now possible to calculate the time to failure under normal operating conditions.

FIT Calculation

Once the Acceleration Factor is known it is relatively simple to calculate the FIT rate (failures in ten-to-the-ninth hours).

The total device hours at normal conditions equal total accelerated hours times the acceleration factor. The failure rate is then calculated from the Chi Squared distribution where the degrees of freedom is 2(c+1) and *c* equals total failures. Dividing the Chi Squared value by the total device hours at normal conditions gives the FIT rate at a given confidence level.

Failure Mechanisms

Semiconductor Failure Patterns:

Characterization of semiconductors show that failure rates change during a device's lifetime. During early life, failure rates are higher and failures are classified as infant mortalities. After approximately 100 hours of

operation the failure rate remains fairly constant until the device enters the wearout phase of its operating life. Wearout is rarely observed. Infant mortality is attributed to manufacturing defects. Random defects account for failures during normal life.

Common Failure Mechanisms:

Table 1-1 shows typical fail modes for CMOS semiconductors and associated activation energies. Also listed are typical methods of detection and prevention.

Table 1-1. Common failure modes and association energies along with detection tests and preventative actions.

Fail Mode	Activation Energy	Detection	Prevention
Oxide defects	0.3 eV	High voltage operation	Ultra clean process
Contamination	1.0 eV	High temperature bias	Ultra clean process
Silicon defects	0.5 eV	High voltage stress	Quality Control/ Clean process
Metal electromigration	0.5 eV	High temperature operating life	Optimum design rules and process control
Mask/Assembly defects	0.5 eV	High temperature life	Quality Control/ Inspection
Microcracks	NA	Temperature cycling	Process control
Soft error	NA	Low voltage operation and accelerated alpha source	Process control, Optimum design, and Material quality

Logic Devices Reliability Program

Objective

The objective of Logic Device's Reliability program is to insure the highest possible reliability of all our products. This is accomplished through strict control of all direct materials used in manufacturing and comprehensive characterization and qualification of all Logic Devices products. All changes to designs, processes or materials are evaluated and approved prior to release to the manufacturing area and hence to the customer. Establishing requirements and performing qualification testing are the responsibility of the reliability department. Existing products are monitored by the reliability department to insure detection of any reliability problem at the earliest point possible.

Reliability Program Components

Qualification Policy:

All new products, packages, and processes receive an initial qualification according to internal specification QAP-1035. All changes in design, mask layers, process, and package are evaluated for qualification requirements and requalified according to the requirements found in MIL-M-38510 paragraph 3.4.2. Changes classified as major are requalified according this document and notification is sent to existing customers prior to final production approval.

Reliability Monitor Program:

Production products are monitored on a regular basis as specified in Section 3.

Failure Analysis/Corrective Action:

Any failure in qualification or monitor testing receives a failure analysis by the reliability department. Evaluation of the fail mode will determine the appropriate corrective action. Records of all failure analyses and corrective actions will be kept on record for a minimum of 5 years.

Data Preparation/Reporting:

Preliminary qualification data, customer qualification data (883C), and monitor data is prepared by the reliability department. This data is continuously being generated and is added to the reliability manual on a quarterly basis.

Qualification Program

Criteria for performing a qualification is divided into three major areas:

1. Process Qualifications,
2. Product Qualifications,
3. Package/Assembly Qualifications.

Qualification Procedure:

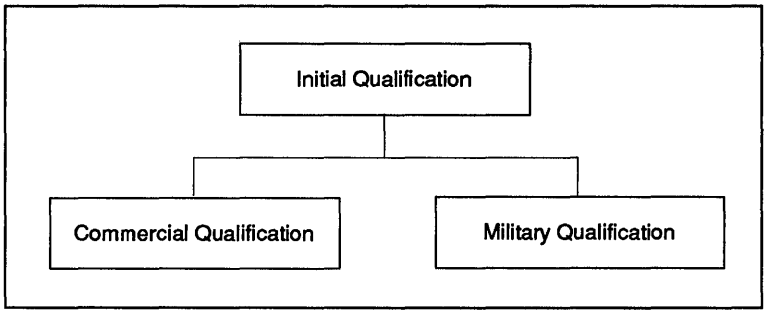
New products requiring qualification will typically follow the flow shown in Fig. 2-1. The Quality Assurance department is responsible for performing all qualifications.

Preliminary Qualification – An internal procedure designed to give timely reliability information on new products or processes. Preliminary qualification consists of Operating Life, Temperature Humidity Bias, Temperature Cycling, ESD, and Latchup testing. This testing is intended to provide early data on reliability for new products.

Military Qualification – All products intended to be marked as 883C compliant will be qualified according to the Military Qualification Flow. This flow is derived from Mil-Std-883C, method 5005.

Commercial Qualification – Commercial qualifications are done on products offered in non-hermetic packages. The qualification is based on JEDEC STD-22B. Differences between this qualification and the military qualification are primarily associated with

Figure 2-1. New product qualification flow.



environmental package tests designed for plastic packages.

Qualification Data – Qualification data is prepared by the Quality/Reliability Department and is added to this report on a quarterly basis.

Qualification Requirements:

Table 2-1 indicates minimum qualification requirements of all Logic products. The extent of the qualification is based on the category of change ranging from a new product or process, to minor changes to existing products, processes, or packages.

Package/Assembly Qualification:

The following criteria will invoke a package/assembly qualification.

1. New package
2. Package material of process change
3. New assembly plant

Qualification Test Flows

Military Qualification Flow:

Products offered as compliant to MIL-STD-883C are qualified per Method 5005 as a minimum requirement. At the discretion of the reliability department, more stringent testing may be completed for evaluation purposes.

Commercial/Industrial Qualification Flow:

Qualifications for commercial/Industrial products are done on devices in non-hermetic packages. This data is supplemented by the data generated from military qualifications. Test methods used for testing non-hermetic packages are found in JEDEC-STD-22B. Differences in military and commercial/industrial qualifications are related to package related tests although some conditions on other tests may vary slightly. Refer to JEDEC-STD-22B and test methods in MIL-STD-883C.

Military Test Groups, MIL-STD-883C

Group A:

The purpose of Group A testing is verification that all electrical parameters meet the specification limits over the specified temperature range. Typically the sample size is 116, accepting on no failures. This test is performed on each military lot.

Group B:

As shown in the Military Test Flows, tests done in this subgroup are designed to insure the integrity of the assembly process. This group is also required for each military lot.

Group C:

Better known as life test, devices are subjected to a minimum 125°C temperature for 1000 hours. Accelerated life testing may be performed at the manufacturers discretion as long as the chip temperature does not exceed it's absolute maximum rating. The minimum requirement for performing this test on a device family is within 4 quarters of the device date code.

Group D:

As shown in the Military Test Flows, these tests are designed to accelerate stresses on the device package. Devices are subjected to variations of temperature, humidity, mechanical pressure and corrosive environments.

Table 2-1. Minimum qualification requirements for all Logic Device' products.

Process	Qualification Requirement
1. New Fab Process	Full Military/Commercial Qual
2. New Fab Location	Full Military/Commercial Qual
3. Process Modification	Per 38510 para. 3.4.2
4. New Fab Equipment	Per Logic Q.A. determination
Product	
1. New product in qualified Fab.	Full Military/Commercial Qual
2. Mask (Layer) Change	Group A, C, Temp. Cycling
3. Design Change	Full Military/Commercial Qual
Package/Assembly	
1. New Package — Non-hermetic	Temp. Cycle, Thermal Shock, THB, Autoclave, Phys. Dim., Lead Integ., X-ray
2. New Package — Hermetic	Temp. Cycle, Thermal Shock, Phys. Dim., Lead Integ., Lid Torque, X-ray

The minimum requirement for Group D qualification is within 52 weeks of the device date code.

Environmental Test Descriptions

Temperature Cycling. Devices are subjected to alternating ambient temperatures of –65°C to +150°C. Cycle time is 30 minutes.

Thermal Shock. Devices are subjected to rapid temperatures controlled by liquid environments for a specified number of cycles.

Biased Humidity Life. This test is performed on non-hermetic packages only. Devices are subjected to 85% humidity and 85°C temperatures for 1000 hours minimum while under bias.

Autoclave (Pressure Cooker). As the name indicates, devices are subjected to pressure and elevated temperature in 100% humidity with no bias. This test is designed for non-hermetic packages only.

Salt Atmosphere. Devices are placed in a corrosive environment for a minimum of 24 hours and evaluated for corrosion.

Resistance to Solvents. Device marking are exposed to solvents and must remain legible.

Mechanical Shock. Devices are subjected to 5 shock pulses of 1500 G's for 0.5 μS each pulse and then evaluated for visual and electrical damage.

Moisture Resistance. Devices are subjected to temperature cycling in 90-100% humidity to simulate a corrosive environment.

Reliability Monitor Program

Objective

Logic Devices reliability monitor program is designed to minimize any potential impact of a reliability problem on our customers by continuous evaluation of key products within each generic process family and package technology. This program is also intended to gather ongoing data for evaluation of reliability improvements. Additional tests may be added for evaluation purposes at the discretion of the reliability department. Rejected devices receive failure analysis leading to appropriate corrective action. Each process/package family is tested a minimum frequency of 6 months and each process family quarterly.

Monitor tests

See Table 3-2 for monitor test conditions.

7

Table 3-1. Monitor Test conditions.

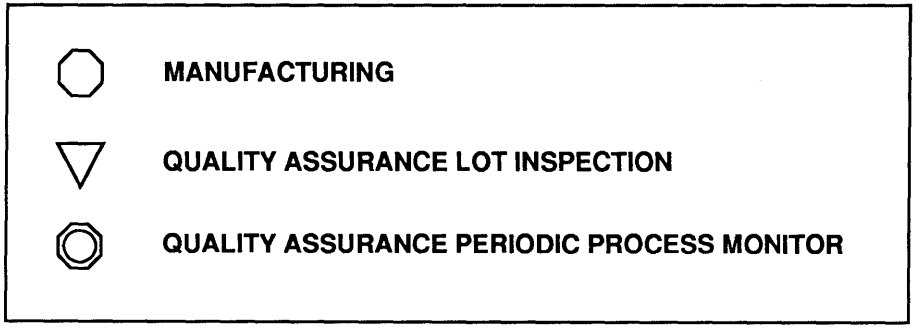
Test Name	Conditions	Sample Size
Early Failure Rate	80 hours, 125°C	77
Latent Failure Rate	2000 hours, 125°C	77
Pressure Cooker	96 hours, A102*	100
Biased Humidity Life	1000 hours, A101*	77
Temperature Cycle	15 Cycles, Note 1	77

*JEDEC STD-22B Test Methods. Done on plastic packages only.

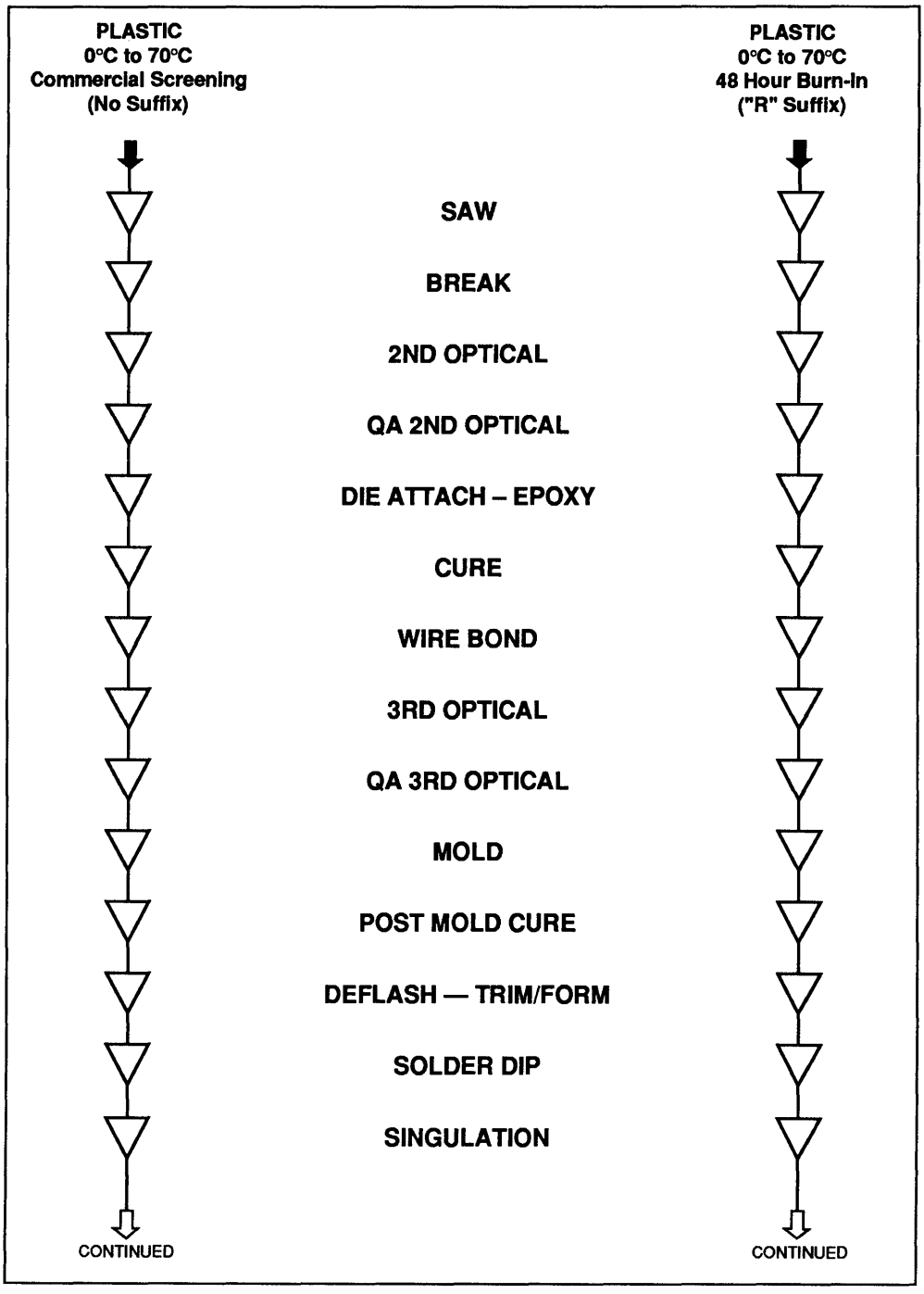
Note 1: Plastic packages tested to A104, condition B. Hermetic packages tested to Method 1010, condition C of MIL-STD-883C.

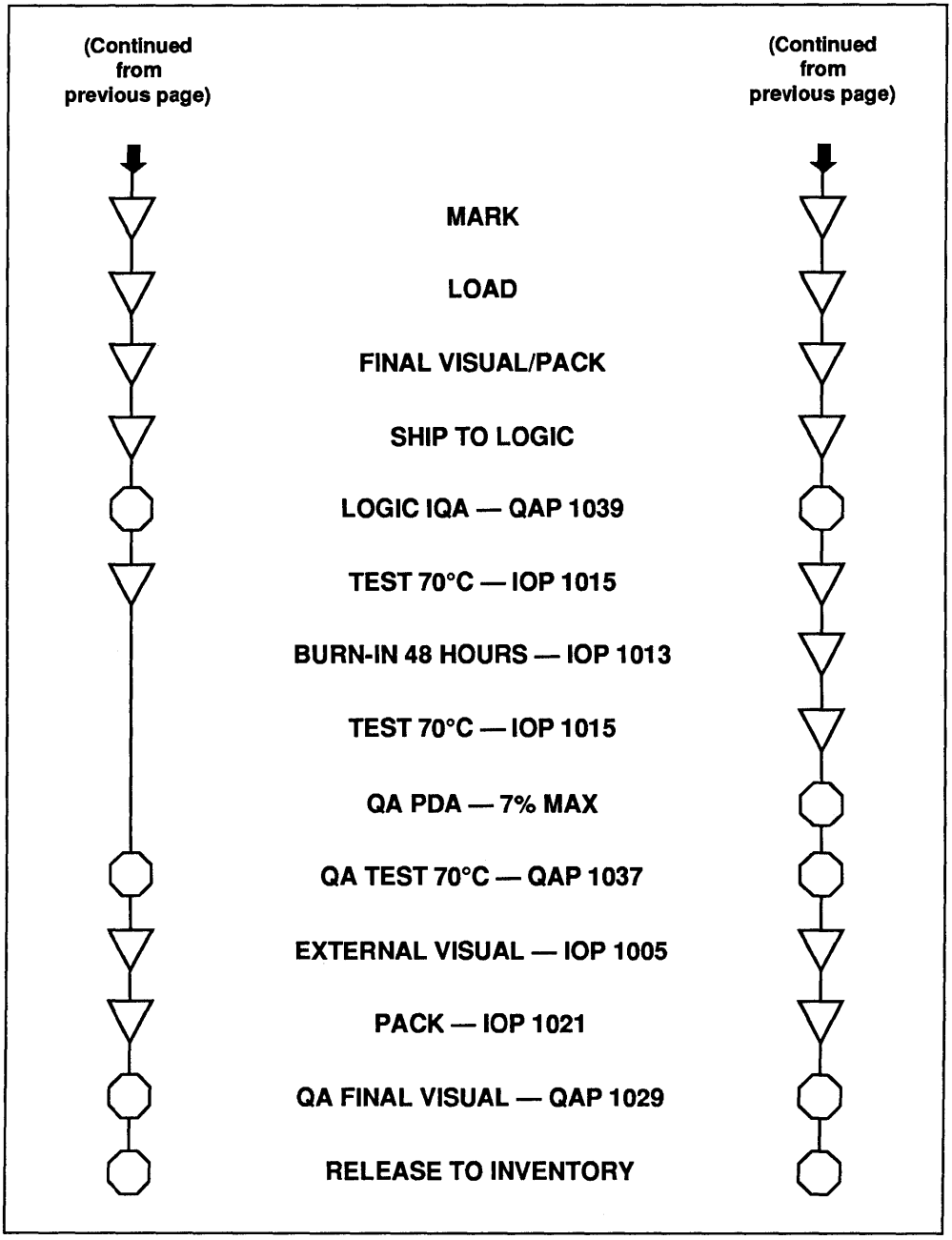
Assembly Flows

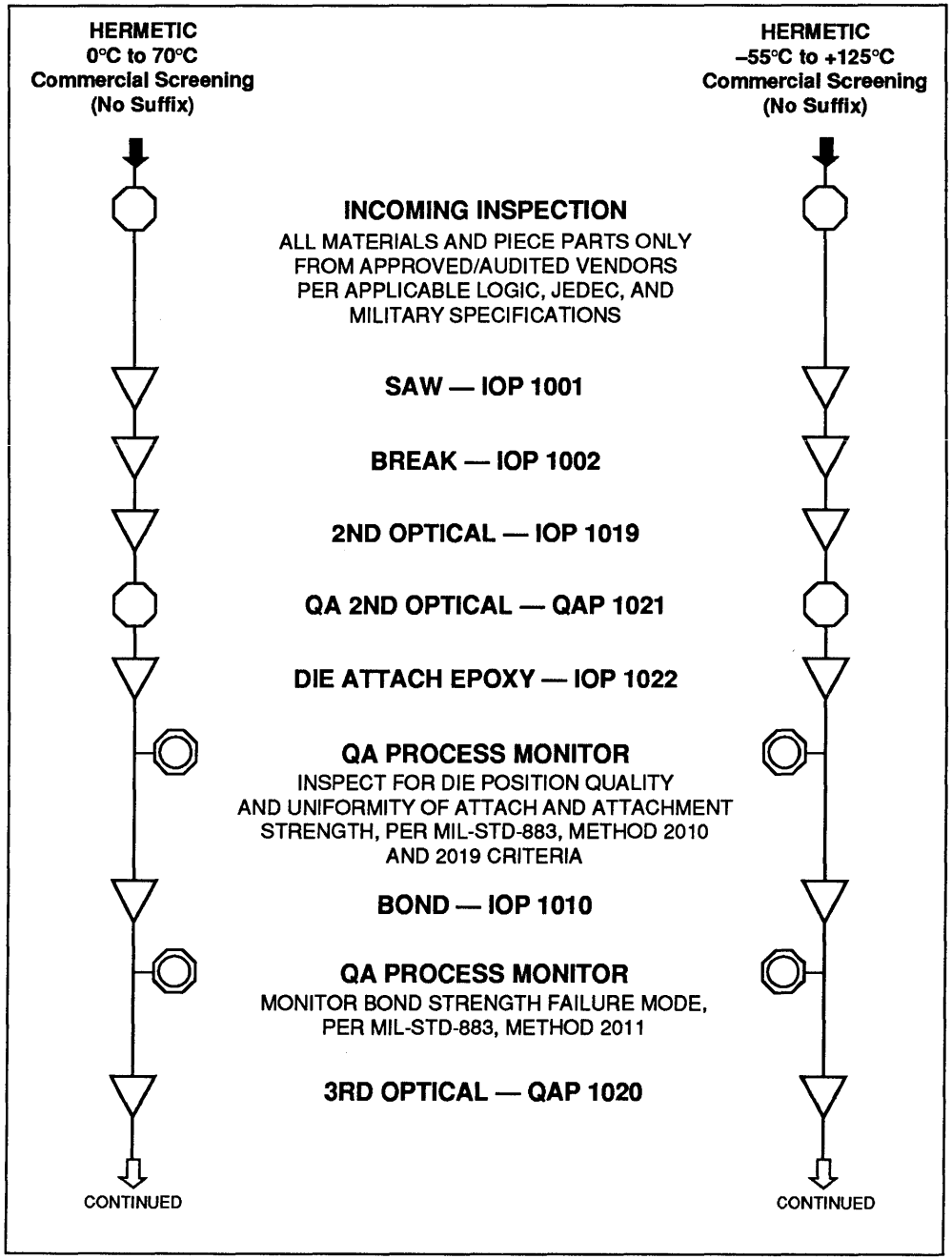
KEY:

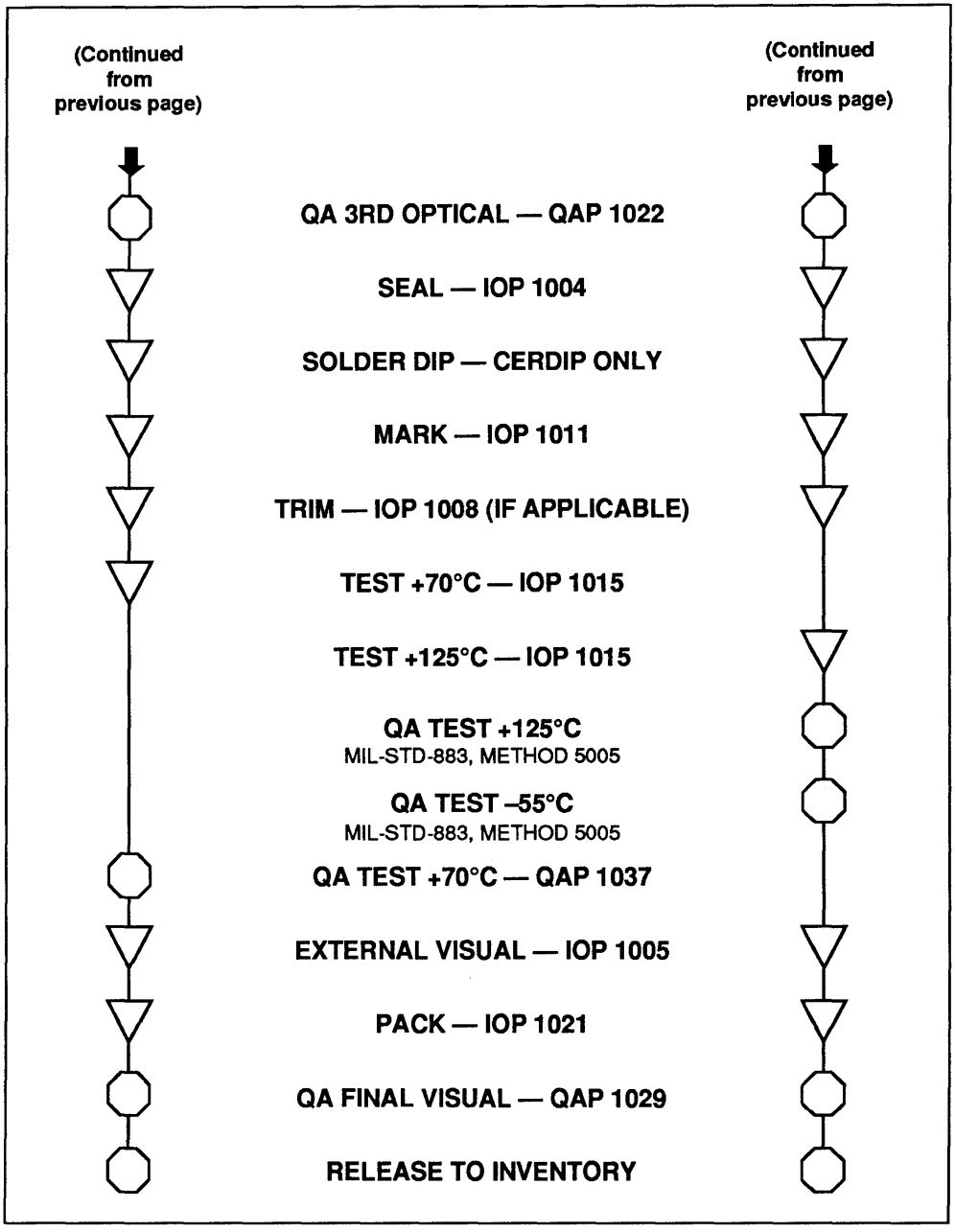


The following diagrams represent nominal process flows as of the date of issue. Specific details are available in Logic Devices Manufacturing Instructions.


PLASTIC
0°C to 70°C
Commercial Screening
(No Suffix)
PLASTIC
0°C to 70°C
48 Hour Burn-In
("R" Suffix)
SAW
BREAK
2ND OPTICAL
QA 2ND OPTICAL
DIE ATTACH – EPOXY
CURE
WIRE BOND
3RD OPTICAL
QA 3RD OPTICAL
MOLD
POST MOLD CURE
DEFLASH — TRIM/FORM
SOLDER DIP
SINGULATION
CONTINUED
CONTINUED

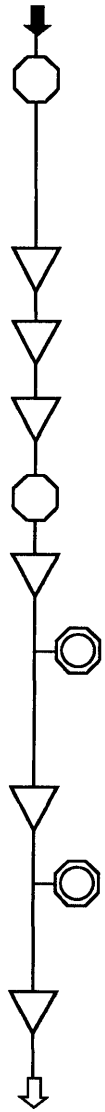

(Continued from previous page)
(Continued from previous page)
MARK
LOAD
FINAL VISUAL/PACK
SHIP TO LOGIC
LOGIC IQA — QAP 1039
TEST 70°C — IOP 1015
BURN-IN 48 HOURS — IOP 1013
TEST 70°C — IOP 1015
QA PDA — 7% MAX
QA TEST 70°C — QAP 1037
EXTERNAL VISUAL — IOP 1005
PACK — IOP 1021
QA FINAL VISUAL — QAP 1029
RELEASE TO INVENTORY


HERMETIC
0°C to 70°C
Commercial Screening
(No Suffix)
HERMETIC
–55°C to +125°C
Commercial Screening
(No Suffix)
INCOMING INSPECTION
ALL MATERIALS AND PIECE PARTS ONLY
FROM APPROVED/AUDITED VENDORS
PER APPLICABLE LOGIC, JEDEC, AND
MILITARY SPECIFICATIONS
SAW — IOP 1001
BREAK — IOP 1002
2ND OPTICAL — IOP 1019
QA 2ND OPTICAL — QAP 1021
DIE ATTACH EPOXY — IOP 1022
QA PROCESS MONITOR
INSPECT FOR DIE POSITION QUALITY
AND UNIFORMITY OF ATTACH AND ATTACHMENT
STRENGTH, PER MIL-STD-883, METHOD 2010
AND 2019 CRITERIA
BOND — IOP 1010
QA PROCESS MONITOR
MONITOR BOND STRENGTH FAILURE MODE,
PER MIL-STD-883, METHOD 2011
3RD OPTICAL — QAP 1020
CONTINUED
CONTINUED


(Continued from previous page)
(Continued from previous page)
QA 3RD OPTICAL — QAP 1022
SEAL — IOP 1004
SOLDER DIP — CERDIP ONLY
MARK — IOP 1011
TRIM — IOP 1008 (IF APPLICABLE)
TEST +70°C — IOP 1015
TEST +125°C — IOP 1015
QA TEST +125°C
MIL-STD-883, METHOD 5005
QA TEST –55°C
MIL-STD-883, METHOD 5005
QA TEST +70°C — QAP 1037
EXTERNAL VISUAL — IOP 1005
PACK — IOP 1021
QA FINAL VISUAL — QAP 1029
RELEASE TO INVENTORY

7

HERMETIC
0°C to 70°C
48Hour Burn-In
("R" Suffix)



INCOMING INSPECTION
ALL MATERIALS AND PIECE PARTS ONLY
FROM APPROVED/AUDITED VENDORS
PER APPLICABLE LOGIC, JEDEC, AND
MILITARY SPECIFICATIONS

SAW — IOP 1001

BREAK — IOP 1002

2ND OPTICAL — IOP 1019

QA 2ND OPTICAL — QAP 1021

DIE ATTACH EPOXY — IOP 1022

QA PROCESS MONITOR
INSPECT FOR DIE POSITION QUALITY
AND UNIFORMITY OF ATTACH AND ATTACHMENT
STRENGTH, PER MIL-STD-883, METHOD 2010
AND 2019 CRITERIA

BOND — IOP 1010

QA PROCESS MONITOR
MONITOR BOARD STRENGTH FAILURE MODE,
PER MIL-STD-883, METHOD 2011

3RD OPTICAL — QAP 1020

CONTINUED

(Continued from previous page)

QA 3RD OPTICAL — QAP 1022

SEAL — IOP 1004

MARK — IOP 1011

TRIM — IOP 1008 (IF APPLICABLE)

TEST +70°C — IOP 1015

BURN-IN 48 HOURS — IOP 1013

TEST +70°C — IOP 1015

QA PDA — 7% MAX

QA TEST +70°C — QAP 1037

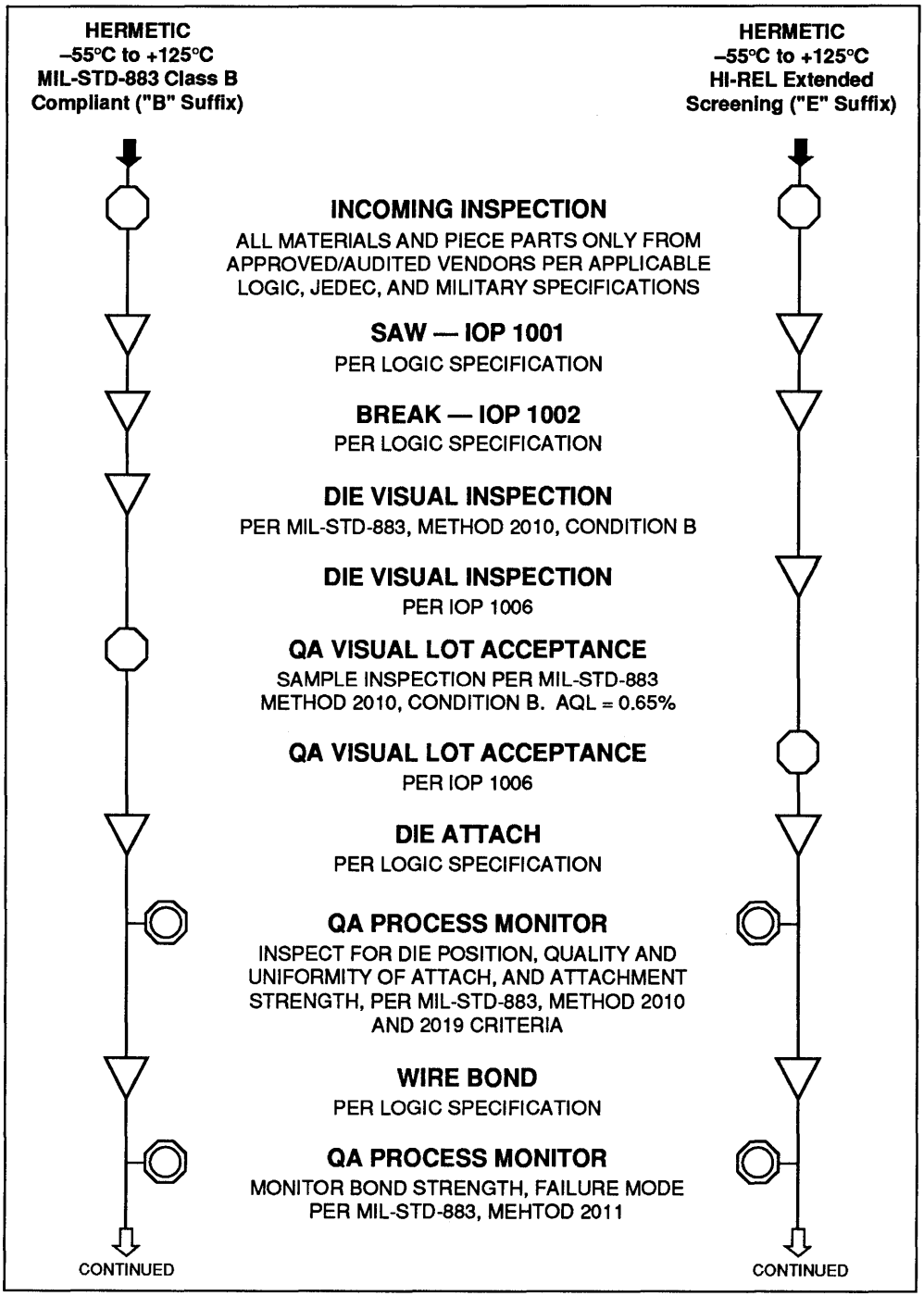
EXTERNAL VISUAL — IOP 1005

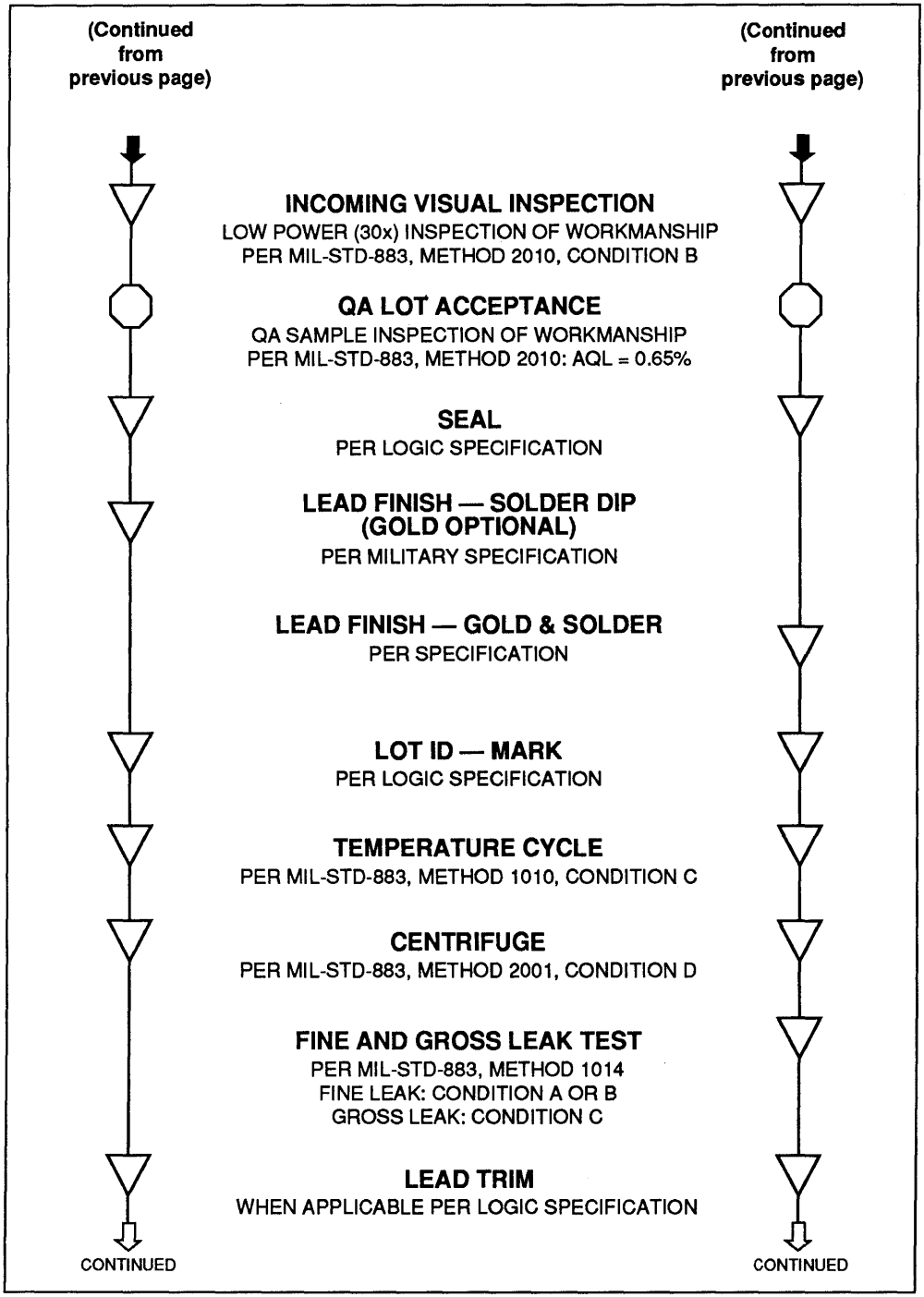
PACK — IOP 1021

QA FINAL VISUAL — QAP 1029

RELEASE TO INVENTORY

7


HERMETIC
–55°C to +125°C
MIL-STD-883 Class B
Compliant ("B" Suffix)
HERMETIC
–55°C to +125°C
HI-REL Extended
Screening ("E" Suffix)
INCOMING INSPECTION
ALL MATERIALS AND PIECE PARTS ONLY FROM APPROVED/AUDITED VENDORS PER APPLICABLE LOGIC, JEDEC, AND MILITARY SPECIFICATIONS
SAW — IOP 1001
PER LOGIC SPECIFICATION
BREAK — IOP 1002
PER LOGIC SPECIFICATION
DIE VISUAL INSPECTION
PER MIL-STD-883, METHOD 2010, CONDITION B
DIE VISUAL INSPECTION
PER IOP 1006
QA VISUAL LOT ACCEPTANCE
SAMPLE INSPECTION PER MIL-STD-883 METHOD 2010, CONDITION B. AQL = 0.65%
QA VISUAL LOT ACCEPTANCE
PER IOP 1006
DIE ATTACH
PER LOGIC SPECIFICATION
QA PROCESS MONITOR
INSPECT FOR DIE POSITION, QUALITY AND UNIFORMITY OF ATTACH, AND ATTACHMENT STRENGTH, PER MIL-STD-883, METHOD 2010 AND 2019 CRITERIA
WIRE BOND
PER LOGIC SPECIFICATION
QA PROCESS MONITOR
MONITOR BOND STRENGTH, FAILURE MODE PER MIL-STD-883, MEHTOD 2011
CONTINUED
CONTINUED


(Continued from previous page)
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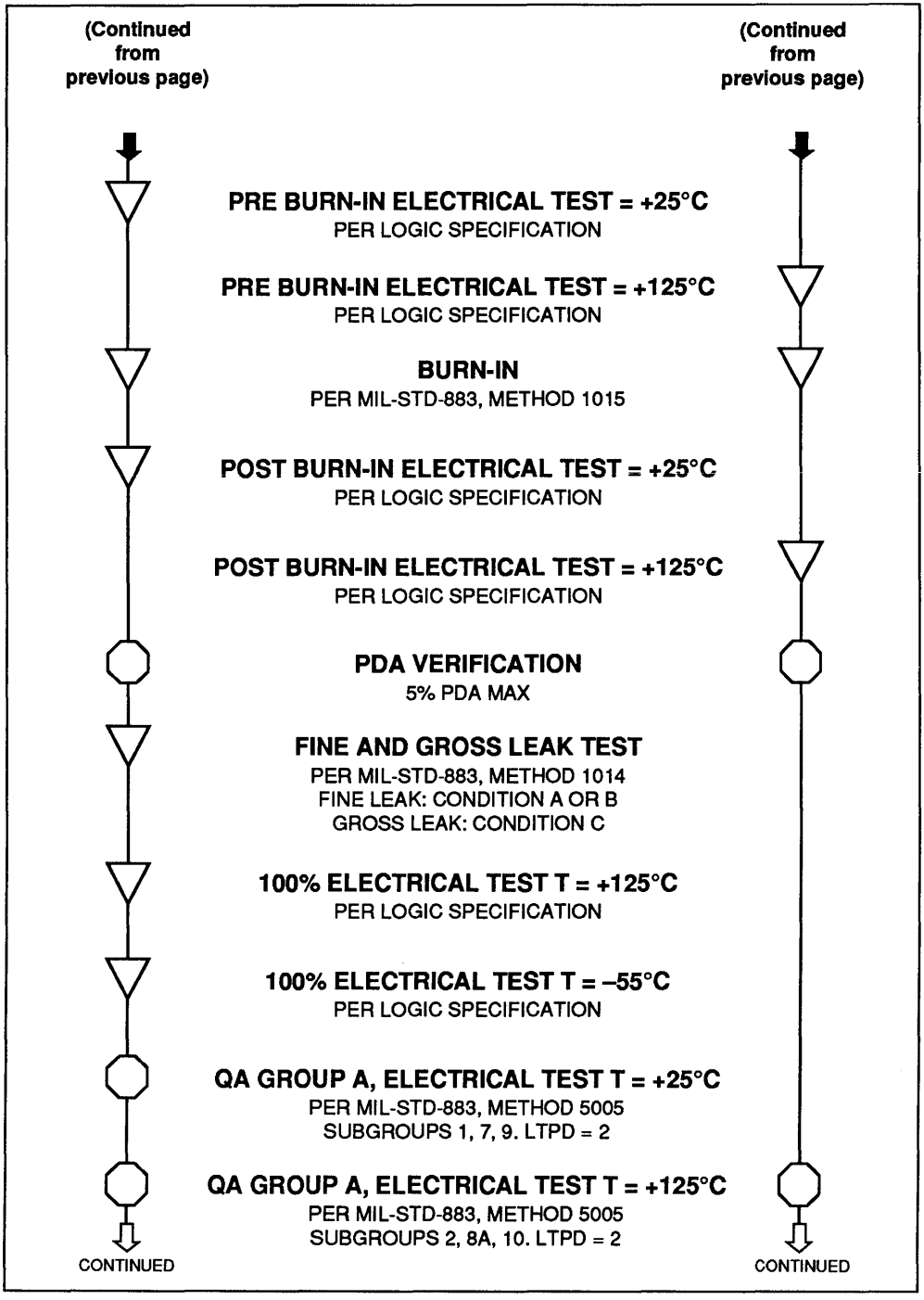
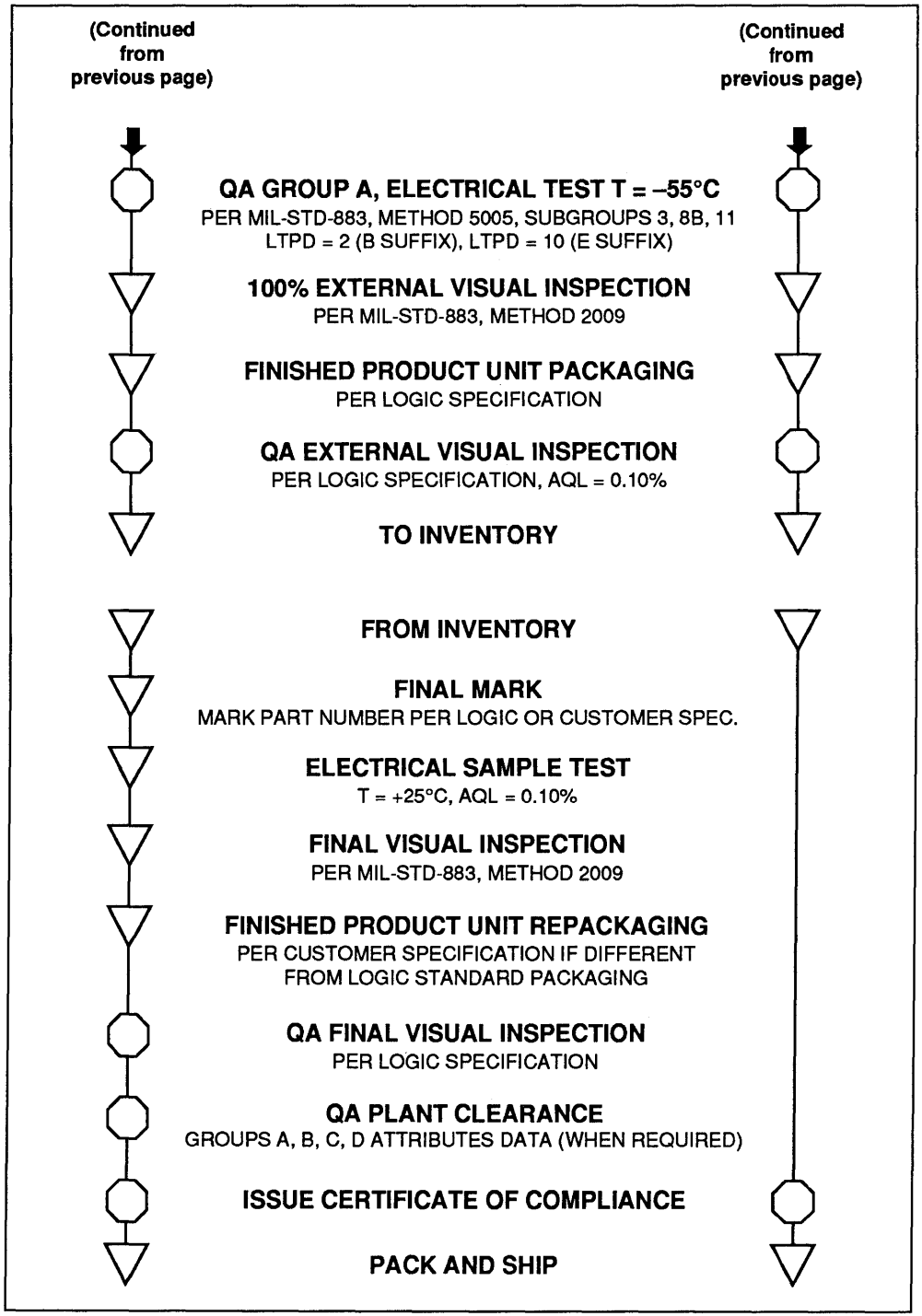
INCOMING VISUAL INSPECTION
LOW POWER (30x) INSPECTION OF WORKMANSHIP
PER MIL-STD-883, METHOD 2010, CONDITION B
QA LOT ACCEPTANCE
QA SAMPLE INSPECTION OF WORKMANSHIP
PER MIL-STD-883, METHOD 2010: AQL = 0.65%
SEAL
PER LOGIC SPECIFICATION
LEAD FINISH — SOLDER DIP (GOLD OPTIONAL)
PER MILITARY SPECIFICATION
LEAD FINISH — GOLD & SOLDER
PER SPECIFICATION
LOT ID — MARK
PER LOGIC SPECIFICATION
TEMPERATURE CYCLE
PER MIL-STD-883, METHOD 1010, CONDITION C
CENTRIFUGE
PER MIL-STD-883, METHOD 2001, CONDITION D
FINE AND GROSS LEAK TEST
PER MIL-STD-883, METHOD 1014
FINE LEAK: CONDITION A OR B
GROSS LEAK: CONDITION C
LEAD TRIM
WHEN APPLICABLE PER LOGIC SPECIFICATION
CONTINUED
CONTINUED

7


(Continued from previous page)
(Continued from previous page)
PRE BURN-IN ELECTRICAL TEST = +25°C
PER LOGIC SPECIFICATION
PRE BURN-IN ELECTRICAL TEST = +125°C
PER LOGIC SPECIFICATION
BURN-IN
PER MIL-STD-883, METHOD 1015
POST BURN-IN ELECTRICAL TEST = +25°C
PER LOGIC SPECIFICATION
POST BURN-IN ELECTRICAL TEST = +125°C
PER LOGIC SPECIFICATION
PDA VERIFICATION
5% PDA MAX
FINE AND GROSS LEAK TEST
PER MIL-STD-883, METHOD 1014
FINE LEAK: CONDITION A OR B
GROSS LEAK: CONDITION C
100% ELECTRICAL TEST T = +125°C
PER LOGIC SPECIFICATION
100% ELECTRICAL TEST T = –55°C
PER LOGIC SPECIFICATION
QA GROUP A, ELECTRICAL TEST T = +25°C
PER MIL-STD-883, METHOD 5005
SUBGROUPS 1, 7, 9. LTPD = 2
QA GROUP A, ELECTRICAL TEST T = +125°C
PER MIL-STD-883, METHOD 5005
SUBGROUPS 2, 8A, 10. LTPD = 2
CONTINUED
CONTINUED


(Continued from previous page)
(Continued from previous page)
QA GROUP A, ELECTRICAL TEST T = –55°C
PER MIL-STD-883, METHOD 5005, SUBGROUPS 3, 8B, 11
LTPD = 2 (B SUFFIX), LTPD = 10 (E SUFFIX)
100% EXTERNAL VISUAL INSPECTION
PER MIL-STD-883, METHOD 2009
FINISHED PRODUCT UNIT PACKAGING
PER LOGIC SPECIFICATION
QA EXTERNAL VISUAL INSPECTION
PER LOGIC SPECIFICATION, AQL = 0.10%
TO INVENTORY
FROM INVENTORY
FINAL MARK
MARK PART NUMBER PER LOGIC OR CUSTOMER SPEC.
ELECTRICAL SAMPLE TEST
T = +25°C, AQL = 0.10%
FINAL VISUAL INSPECTION
PER MIL-STD-883, METHOD 2009
FINISHED PRODUCT UNIT REPACKAGING
PER CUSTOMER SPECIFICATION IF DIFFERENT
FROM LOGIC STANDARD PACKAGING
QA FINAL VISUAL INSPECTION
PER LOGIC SPECIFICATION
QA PLANT CLEARANCE
GROUPS A, B, C, D ATTRIBUTES DATA (WHEN REQUIRED)
ISSUE CERTIFICATE OF COMPLIANCE
PACK AND SHIP

883C Test Flows

The following tables define the testing performed on Logic Devices 883C compliant products. Table 1 defines test subgroups 1 through 11 (per MIL-STD-883 method 5005, Table 1) in terms of the specific electrical parametric tests which make up the subgroup. The specific electrical limits for the tests within each subgroup are given in the device data sheet. Data sheet specifications bearing a note stating that the parameter is guaranteed but not 100% tested are excluded from subgroup testing. Table 2 defines which of these subgroups of tests are performed at various stages in the production and qualification processes.

TABLE 1.

SUBGROUP	DEFINITION	COMMENTS
1. 2. 3.	Static tests @ 25°C Static tests @ max temp Static tests @ min temp	Static tests are defined as those given under the heading "Electrical Characteristics" in the device data sheet, with the exception of CIN (Input Capacitance) and COUT (Output Capacitance).
4. 5. 6.	Dynamic tests @ 25°C Dynamic tests @ max temp Dynamic tests @ min temp	The only dynamic test defined for Logic Devices products are CIN (Input Capacitance) and COUT (Output Capacitance).
7. 8A. 8B.	Functional tests @ 25°C Functional tests @ max temp Functional tests @ min temp	Functional tests are not explicitly given in the data sheets, but consist of stimulation of the device inputs and monitoring of the device outputs with a pattern judged to give a good probability of detecting any internal functional defect. The specific patterns used for any Logic Devices' product are available on request.
9. 10. 11.	Switching Tests @ 25°C Switching tests @ max temp Switching tests @ min temp	Switching tests are essentially the same patterns used in subgroups 7, 8A, and 8B, with the exception that the device is required to successfully execute these patterns within the timing constraints given under the heading "Switching Characteristics" in the device data sheet.

TABLE 2.

TEST REQUIREMENTS	MIL-STD-883 METHOD	SUBGROUPS TESTED	COMMENTS
Final Electrical Test	5004	1, 2, 3, 7, 8, 9, 10, 11	PDA applies to 1, 7 only
GROUP A	5005	1, 2, 3, 4, 7, 8, 9, 10, 11	Subgroup 4 tested only at initial qualification and after major process or design changes
GROUP C & D Endpoint Electrical	5005	1, 2, 3, 7, 8	

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8

Latchup and ESD Protection

Latchup is a destructive phenomenon which was once common in CMOS circuits but has now been largely eliminated by improved circuit design techniques. Latchup takes place because of the existence in CMOS of an inherent p/n/p/n or n/p/n/p structure between V_{CC} and ground. Either of these two can form a pair of transistors connected so as to form a positive feedback loop, with the collector of one transistor driving the base of the other. The result is a low-impedance path from V_{CC} to ground, which cannot be interrupted except by the removal of power. This condition can be destructive if the area involved is sufficiently large to dissipate excessive power. One example of the formation of such a structure is shown in Fig. 1. The equivalent circuit is shown in Fig. 2.

As shown in Fig. 1, the n+ regions which form the source and drain of an n-channel MOS transistor, also act as the emitters of a parasitic npn transistor. The p-well forms the base region, and the n-substrate is the collector. The current gain of this transistor is relatively high because it is formed vertically and therefore the base width is quite small. This is especially true of fine-geometry CMOS processes which tend to have very shallow wells to reduce sidewall capacitance. The p+ region in the well is called a well tap, and is present to form a low-resistance connection between the well and ground. The source region cannot serve this function because it forms a diode between the n+ source and the p-well.

Also shown in Fig. 1 is an additional parasitic pnp transistor. The source and drain regions of the p-channel MOS device form the emitters, the n-substrate is the base, and the p-well is the collector. This transistor is a pnp, and generally has a beta much less than 1 since it is formed laterally and the gate region is relatively large. Like the vertical npn, it can have multiple emitters. The n+ region tied to V_{CC} in the substrate functions similarly to the well tap discussed above.

Note that the base of the npn and the collector of the pnp are a common region (the p-well), and similarly the base of the pnp and the collector of the npn are common (the n-substrate). Thus, the pnpn structure necessary for latchup is formed. Also, due to the the physical distance between the well and substrate taps and the base regions which they attempt to contact, a small resistance exists between the base regions and their respective well taps, denoted R_S (substrate) and R_W (well).

Latchup begins when a perturbation causes one of the bipolar transistors to turn on. An example would be excursion of the output pad below ground or above V_{CC} due to transmission-line ringing. If the pad goes more than 0.7 V below ground, the npn will turn on since its base is at approximately ground potential. The npn's collector current will cause a voltage drop across R_S, the bulk substrate resistance. This voltage drop turns on the pnp.

The pnp transistors' collector current forces a similar voltage drop across R_W, the well resistance. This raises the base voltage of the npn above ground, and can cause the npn to continue to conduct even after the output pad returns to a normal voltage range. In this case, the current path shifts to the grounded emitter.

Note that any effect which can cause a transient turn-on of either transistor can cause the latchup process. Common causes include:

1. Ringing of unprotected I/O pins outside the ground to V_{CC} region.
2. Radiation-induced carriers generated in the base of the bipolar transistors.
3. Hot-powerup of the device, with inputs driven high before V_{CC} is applied.
4. Electrostatic discharge.

Protecting Against Latchup

Latchup, while once a severe problem for CMOS, is now a relatively well-understood phenomenon. In order for latchup to occur, the product of the current gains of the two parasitic transistors must exceed 1. Thus, the primary means for avoiding latchup is the insertion of structures known as "guard rings" around all MOS

Figure 1. Parasitic transistor structures in parallel CMOS.

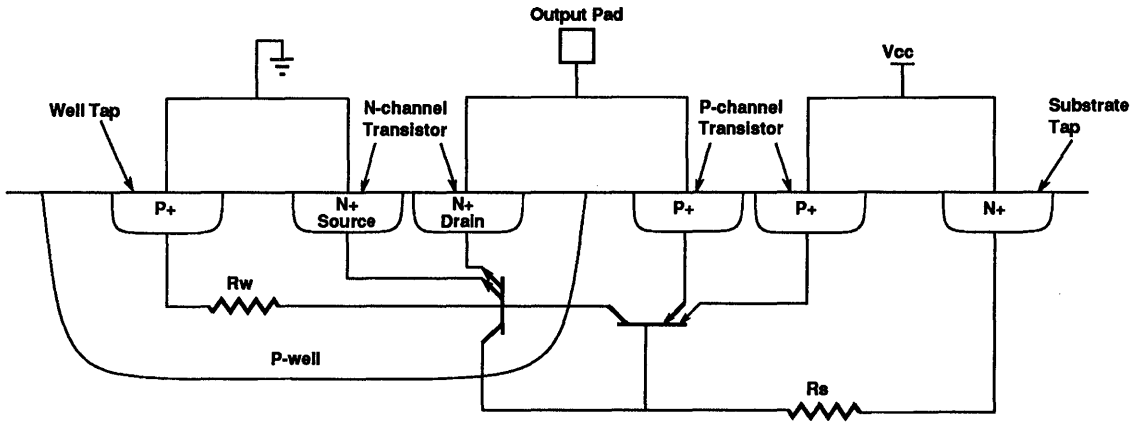
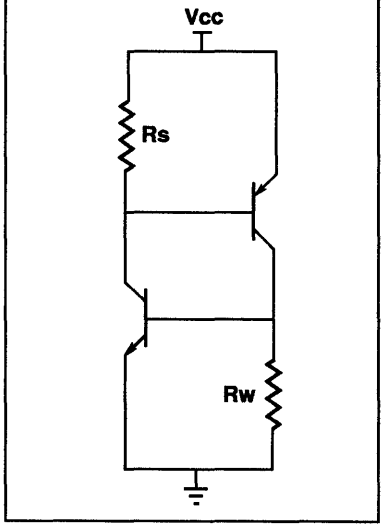


Figure 2. Equivalent circuit for Latchup path.



transistors (and other structures) likely to be subjected to latchup-causing transients. This includes output buffer transistors and any devices which form a part of the ESD protection network. These guard rings absorb current which would otherwise drive the base of the lateral device, and thus dramatically reduce its gain.

Since external electrical perturbations are the dominant cause of latchup in non-radiation environments, protecting the "periphery" of the chip is most important. Therefore, since guard rings require a lot of area, they are generally used only in critical areas such as those mentioned above.

As an additional protective measure, strict rules are enforced in the layout regarding the positioning of the substrate and well taps. They are spaced closely together throughout the die, reducing the values of Rs and Rw. This makes it more difficult to develop the base drive necessary to regenerate the latchup condition.

Measurement of susceptibility to latchup is done by connecting a current source to an input or output of the device under test. By increasing the current forced to flow into the pin and noting the point at which latchup occurs, a measure of the device's ability to resist latchup-inducing carrier injection is obtained. Note that depending on the device, the current source may require a rather large voltage compliance in order to provide an adequate test.

While early CMOS devices had a latchup trigger current of a few tens of milliamps, most current Logic Devices products typically can withstand more than 1 amp without latching. As a result, latchup is no longer a practical concern, except for extreme conditions such as driving multiple inputs high with a low-impedance source during powerup of the device.

Electrostatic Discharge

Input protection structures on CMOS devices are used to protect against damage to the gate oxides of input transistors when accumulated static charge is discharged through a device. This charge can often reach potentials of several thousand volts. The input protection network is designed to shunt this charge safely to ground or Vcc, bypassing the delicate MOS transistors.

Several features are required of a good input protection network. Since static discharge pulses exhibit very fast risetimes, it must have a very fast turnon time. It must be capable of carrying large instantaneous currents without damage. It must prevent the voltage at the circuit input from rising above about 10 V during the time when the several-thousand-volt discharge is shunted to ground. It must not create appreciable delay for fast edges which are within the 0–5 V input range. And finally, it must be well protected against latchup caused by inputs which are driven beyond the supply rails, injecting current into the substrate. Much research and experimentation has been devoted to optimizing the tradeoffs between these conflicting goals.

All Logic Devices products employ one of three input protection structures shown in Fig. 3. Most devices currently use the Type 1 input protection. This structure is designed to absorb very high static discharge energies and will draw substantial current from the input pin if driven beyond either supply rail. Hence, it provides a "hard" clamp. Besides its advantages for static protection, this clamp can effectively reduce undershoot energy, preventing oscillation of an unterminated input back above the 0.8 V Vil MAX level. This makes the circuit ideal for noisy environments and ill-behaved signals. This input structure may not be driven to a high level without power applied to the device, however. To do so would result in current flowing through the diode connected to the devices' V_{CC} rail, and supplying power to the entire board or system backward through the device V_{CC} pin. This may overstress the bond wire or device metallization, resulting in failure.

The Type 2 structure employs a series resistor prior to the two clamp diodes. This results in a "soft" clamping effect. This structure will withstand the transient application of voltages outside the supply rails for brief periods without drawing excessive current. In contrast to the Type 1 structure, this circuit will provide only a modest reduction of the energy in an undershoot pulse. It is somewhat more tolerant of power-up sequences which cause the inputs to be driven before V_{CC} is applied, however. In the course of routine product upgrades, devices employing this structure are being redesigned to use a Type 1 input protection.

The Type 3 structure uses a large area N-channel transistor (part of an open-drain output buffer) to protect the input. The drain-well junction of this device serves the function of a diode connected between the input and ground, protecting against negative excursions of the input. The avalanche breakdown of the output device serves to protect against positive pulses, giving the effect of a zener diode between the input and ground. This circuit is used only for inputs which are designed to have their inputs driven without power applied. The lack of a diode to V_{CC} prevents sourcing of power from the inputs to the Vcc supply.

Table 1 gives Latchup figures for the three input protection structures used in Logic Devices products. Table 2 indicates the input structure used for each part type.

8

FIGURE 3. INPUT PROTECTION DEVICES.

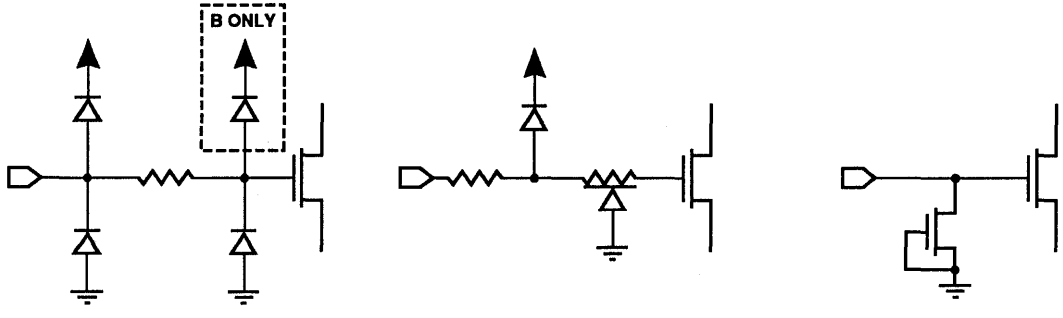


TABLE 1. LATCHUP IMMUNITY.

Structure	Latchup Current Immunity	
	Min	Typ
Type 1A/B	400 mA	1000 mA
Type 2	150 mA	250 mA
Type 3	400 mA	1000 mA

TABLE 2. INPUT STRUCTURE LIST BY PART NUMBER.

Device	Input Structure	Device	Input Structure
Multipliers/Multiplier Accumulators		**Register Files**	
LMU08/8U	Type 1A	LRF07	Type 2
LMU557/558	Type 1A	**Peripheral Products**	
LMU12/112	Type 1A	L5380	Type 1A,3
LMU16/216	Type 1A	L53C80	Type 1A,3
LMU17/217	Type 1A	**16K Static RAMs**	
LMU18	Type 1A	ALL	Type 1B
LMA1009/2009	Type 1A	**64K Static RAMs**	
LMA1010/2010	Type 1A	ALL	Type 1B
LMS12	Type 1A	**256K Static RAMs**	
Arithmetic/Logic Units		ALL	Type 1B
L4C381	Type 1A	**Special Architecture RAMs**	
L29C101	Type 1A	ALL	Type 1B
Special Functions		**FIFOs**	
LSH32	Type 2	ALL	Type 1B
LSH33	Type 1A		
L10C23	Type 1A		
Pipeline Registers			
L29C520/521	Type 1A		
LPR520/521	Type 1A		
L29C524/525	Type 1A		
L10C11	Type 1A		
L29C818	Type 1A		

Power Dissipation in Logic Devices Products

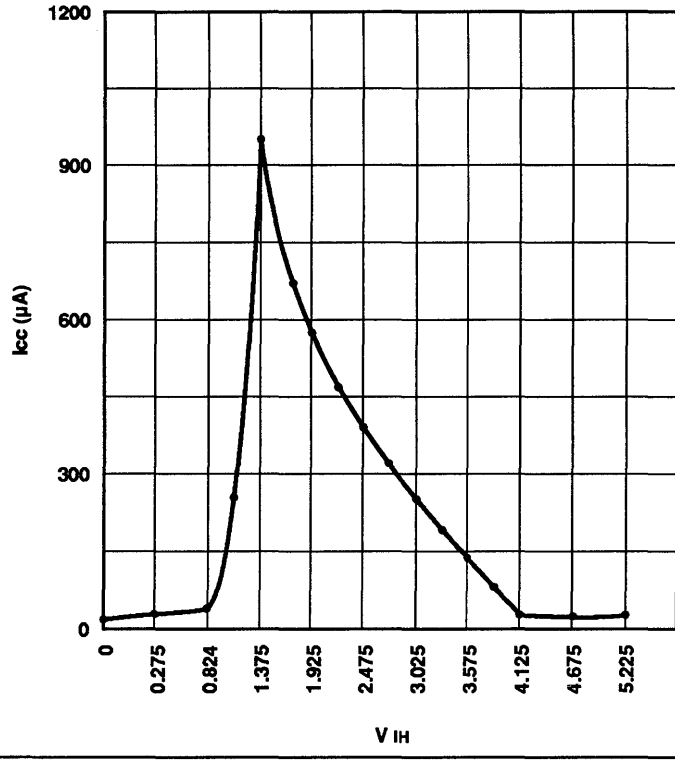
In calculating the power dissipation of Logic Devices products, attention must be given to a number of formerly second-order effects which were generally ignored when dealing with bipolar and NMOS technologies. By far the dominant contributor to power dissipation in most CMOS devices is the effective current path from the supply to ground, created by the repetitive charging and discharging of the load capacitance. This is distinct from DC loading effects, which may also consume power. The power dissipated in the load capacitance is proportional to CV^2F, where C is the load capacitance, V is the voltage swing, and F is the switching frequency. This mechanism can frequently contribute 80% or more of the total device dissipation of a truly complementary device operating at a high clock rate.

The second contributor to the power dissipation of a CMOS device is the DC current path between V_{CC} and ground present in the input level translators. These circuits are voltage amplifiers which are designed to convert worst case 0.8–2.0 V TTL-compatible input levels to 0 and 5 V internal levels. With 2.0 V applied to the input of most level translator circuits, about 1 mA will flow from the power supply to ground. A floating input will at best have similar results, and may result in oscillations which can dissipate orders of magnitude more power and cause malfunctioning of the device.

The power dissipation of input level translators exhibits a strong peak at about 1.4 V, but is reduced substantially when the input voltage exceeds 3.0 V (see Fig. 1). Fortunately, this voltage is easy to achieve in practice, even for bipolar devices with TTL I/O structures. These generally will produce a V_{OH} of at least 3.5 V if not fully loaded. As a result, dissipation in the input structures is usually negligible compared to other sources.

Two further sources of power dissipation in CMOS come from the core logic. The sources of internal power dissipation are the same as those

FIGURE 1.



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discussed for external nodes, namely repetitive charging of the parasitic load capacitances on each gate output, and the power drawn due to a direct current path to ground when gate input voltage levels transition through the linear region. In practice, the internal voltage waveforms are characterized by high edge rates and rail-to-rail swings. For this reason, the latter source of dissipation is usually negligible, unless NMOS or other non-complementary logic design techniques have been used.

The capacitance of typical internal nodes in CMOS logic circuits are a few femtofarads. However, there can be thousands, or tens of thousands of such nodes. As a result, the core power dissipation is strongly dependent on the average rate at which these nodes switch (the "F" in CV^2F). Fortunately, for most complex logic circuits, with non-pathological external stimulus only a small fraction of the logic nodes switch on any given cycle. For this reason, internal power is generally quite small for these device types. Exceptions include devices containing long shift registers or other structures which can exhibit high duty cycles on most internal nodes. These devices can dissipate significant power in the core logic if stimulated with alternating data patterns and clocked at a high rate.

To summarize, of the several contributors to power dissipation, the CV^2F power of the outputs is usually dominant. Because output loading is system-dependent, it is not possible for the manufacturer to accurately predict total power dissipation in actual use. As a result, Logic Devices extrapolates measured power dissipation values to a zero-load environment, and publishes the resulting value. This value includes the effects of worst-case input and power-supply voltages, temperature, and stimulus pattern, but not CV^2F. This value is weakly frequency dependent, and the frequency at which it is measured is published in the device data sheet. The maximum value is for worst-case pattern, and the typical is for a more random pattern and is therefore more representative of what would be experienced in actual practice.

A good estimate of total power dissipation in a particular system under worst-case conditions can be obtained by adding the calculated output power to the *typical* published figure. The output power is given by:

$$\frac{N}{2}\left(CV^2\frac{F}{2}\right)$$

where:

- N = the number of device outputs (divided by 2 to account for the assumption that on average half of the outputs switch on any given cycle)
- C = the output load capacitance, per pin, given in Farads
- V = the power supply voltage
- F = the clock frequency (divided by 2 to account for the fact that a registered output can at most switch at only half the clock rate).

A less pessimistic estimate, appropriate for complex devices when reasonable input voltage levels and non-pathological patterns can be expected, would neglect the published value and use only the calculated value as given above.

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C4 — 24-pin, 0.6" wide 9-10
C5 — 28-pin, 0.3" wide 9-10
C6 — 28-pin, 0.6" wide 9-10
C7 — 16-pin, 0.3" wide 9-11
C8 — 18-pin, 0.3" wide 9-11
C9 — 32-pin, 0.6" wide 9-11

Hermetic DIP, Sidebraze — (Type D, H)

D1 — 24-pin, 0.6" wide 9-12
D2 — 24-pin, 0.3" wide 9-12
D3 — 40-pin, 0.6" wide 9-12
D4 — 64-pin, 0.9" wide 9-13
D5 — 48-pin, 0.6" wide 9-13
D6 — 64-pin, 0.9" wide, cavity down 9-13
D7 — 20-pin, 0.3" wide 9-14
D8 — 22-pin, 0.3" wide 9-14
D9 — 28-pin, 0.6" wide 9-14
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F1 — 24-pin 9-16
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Ceramic Pin Grid Array — (Type G)

G1 — 68-pin 9-17
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Plastic Leaded Chip Carrier (J-Lead — PLCC) — (Type J)

J1 — 44-pin, 0.690" × 0.690" 9-18
J2 — 68-pin, 0.990" × 0.990" 9-18
J3 — 84-pin, 1.190" × 1.190" 9-18
J4 — 28-pin, 0.490" × 0.490" 9-19
J5 — 52-pin, 0.790" × 0.790" 9-19
J6 — 32-pin, 0.490" × 0.590" 9-19
J7 — 20-pin, 0.390" × 0.390" 9-19

Ceramic Leadless Chip Carrier (LCC) — (Type K)

K1 — 28-pin, 0.450" × 0.450" 9-20
K2 — 44-pin, 0.650" × 0.650" 9-20
K3 — 68-pin, 0.950" × 0.950" 9-20
K4 — 22-pin, 0.290" × 0.490" 9-21
K5 — 28-pin, 0.350" × 0.550" 9-21

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Contents

Ceramic Leadless Chip Carrier (LCC) — (Type K) (continued)
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K7 — 32-pin, 0.450" × 0.550" ... 9-22
K8 — 20-pin, 0.350" × 0.350" ... 9-22
K9 — 48-pin, 0.550" × 0.550" ... 9-22
Ceramic Leaded Chip Carrier — (Type L)
L1 — 68-pin ... 9-23
Plastic DIP — (Type P, N)
P1 — 24-pin, 0.6" wide ... 9-23
P2 — 24-pin, 0.3" wide ... 9-23
P3 — 40-pin, 0.6" wide ... 9-24
P4 — 64-pin, 0.9" wide ... 9-24
P5 — 48-pin, 0.6" wide ... 9-24
P6 — 20-pin, 0.3" wide ... 9-25
P7 — 32-pin, 0.3" wide ... 9-25
P8 — 22-pin, 0.3" wide ... 9-25
P9 — 28-pin, 0.6" wide ... 9-26
P10 — 28-pin, 0.3" wide ... 9-26
P11 — 28-pin, 0.4" wide ... 9-26
P12 — 16-pin, 0.3" wide ... 9-27
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W1 — 24-pin, 0.300" wide ... 9-32
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W4 — 16-pin, 0.300" wide ... 9-33
W5 — 18-pin, 0.300" wide ... 9-33

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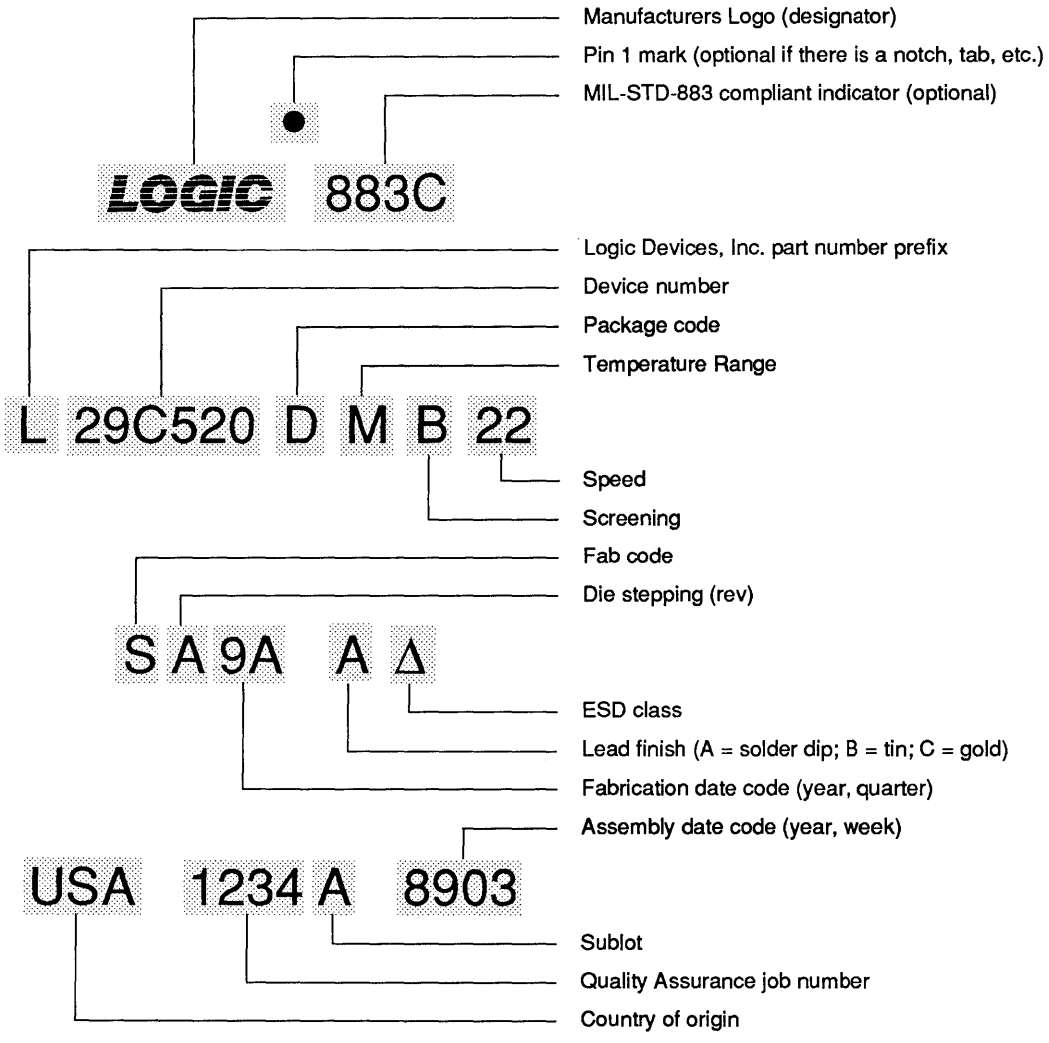
Products Listing 38510 Package Codes

Logic Devices Pkg. Code	38510 Pkg. Code
CerDIP — (Type C, I)	
C1 — 24-pin, 0.3" wide	D9-1
C2 — 20-pin, 0.3" wide	D8-1
C3 — 22-pin, 0.3" wide	NA
C4 — 24-pin, 0.6" wide	D3-1
C5 — 28-pin, 0.3" wide	NA
C6 — 28-pin, 0.6" wide	D10-1
C7 — 16-pin, 0.3" wide	D2-1
C8 — 18-pin, 0.3" wide	D6-1
C9 — 32-pin, 0.6" wide	NA
Hermetic DIP, Sidebraze — (Type D, H)	
D1 — 24-pin, 0.6" wide	D3-3
D2 — 24-pin, 0.3" wide	D9-3
D3 — 40-pin, 0.6" wide	D5-3
D4 — 64-pin, 0.9" wide	D13-3
D5 — 48-pin, 0.6" wide	D14-3
D6 — 64-pin, 0.9" wide, cavity down	D13-3
D7 — 20-pin, 0.3" wide	D8-3
D8 — 22-pin, 0.3" wide	NA
D9 — 28-pin, 0.6" wide	D10-3
D10 — 28-pin, 0.3" wide	NA
D11 — 28-pin, 0.4" wide	NA
Ceramic Flat Pack — (Type F)	
F1 — 24-pin	F6-2
F2 — 28-pin	F12-2
Ceramic Pin Grid Array — (Type G)	
G1 — 68-pin	NA
G2 — 68-pin, cavity down	NA
G3 — 84-pin	NA
Ceramic Leadless Chip Carrier (LCC) — (Type K)	
K1 — 28-pin, 0.450" × 0.450"	C-4
K2 — 44-pin, 0.650" × 0.650"	C-5
K3 — 68-pin, 0.950" × 0.950"	C-7
K4 — 22-pin, 0.290" × 0.490"	NA
K5 — 28-pin, 0.350" × 0.550"	C-11
K6 — 20-pin, 0.290" × 0.425"	C-13
K7 — 32-pin, 0.450" × 0.550"	C-12
K8 — 20-pin, 0.350" × 0.350"	C-2
K9 — 48-pin, 0.550" × 0.550"	NA

Product Marking Guide



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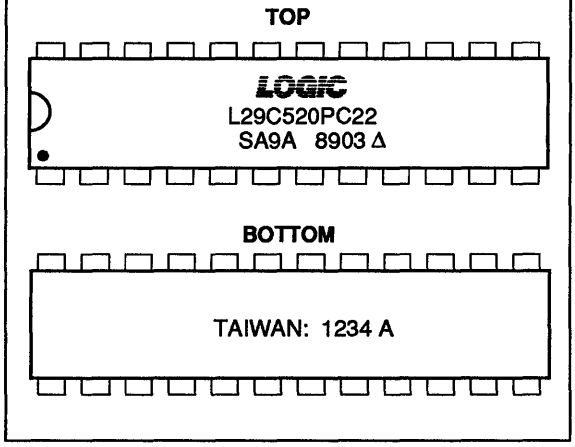
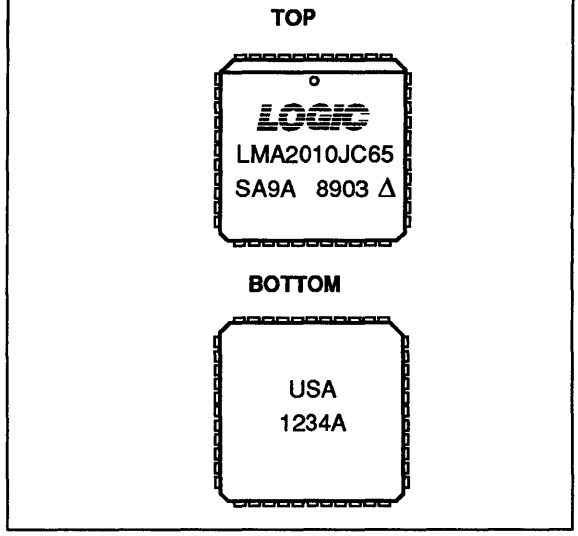
Product Marking Guide

Plastic Package Marking (Plastic DIP, SOIC, SOJ)



Plastic Leaded Chip Carrier

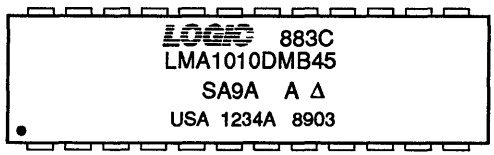


Sidebraze Hermetic Package Marking

TOP ONLY — CAVITY UP: 300 MIL

TOP ONLY — CAVITY UP: 600 MIL

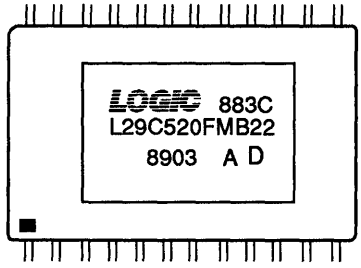
TOP ONLY — CAVITY DOWN



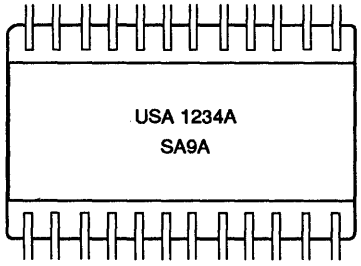
NOTE: Package marking may vary due to space limitations.

Flatpack Package Marking

TOP

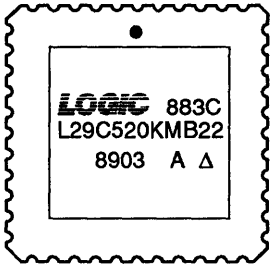


BOTTOM

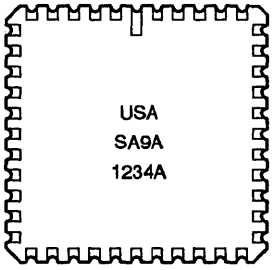


Leadless Chip Carrier Package Marking

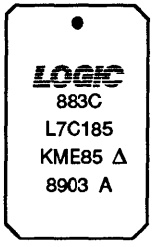
TOP



BOTTOM

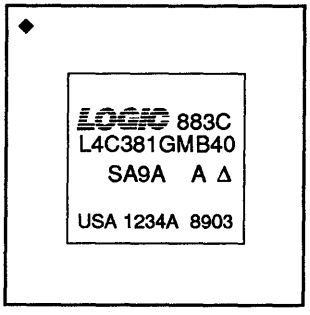


SRAM — TOP



Pin Grid Array Package Marking

TOP ONLY

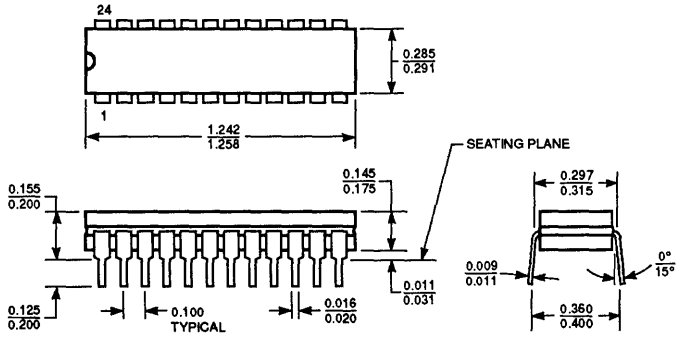


NOTE: Package marking may vary due to space limitations.

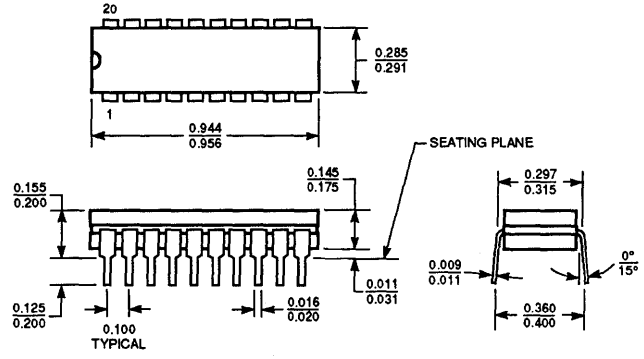
Mechanical Drawings

CerDIP — Type C

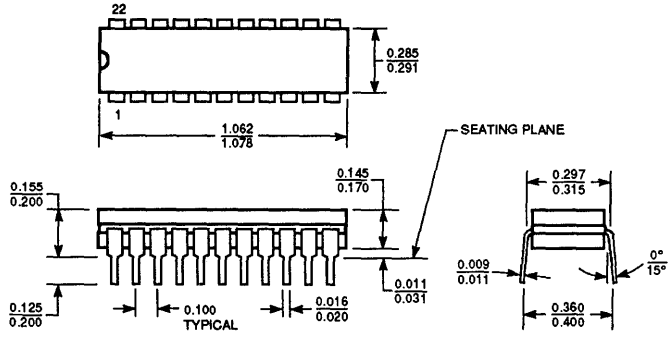
C1 — 24-pin CerDIP (0.3" Wide)



C2 — 20-pin CerDIP (0.3" Wide)



C3 — 22-pin CerDIP (0.3" Wide)



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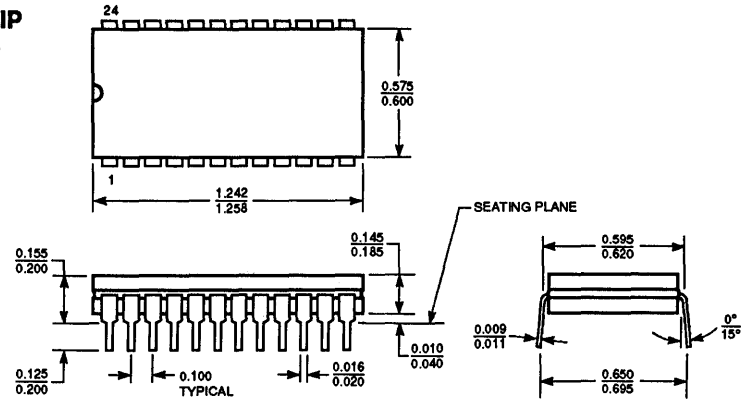
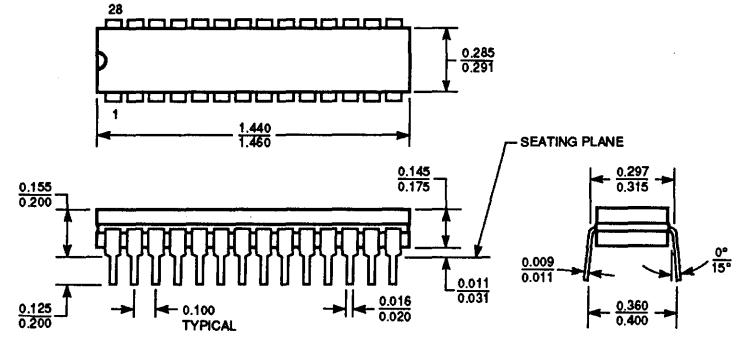
CerDIP — Type C

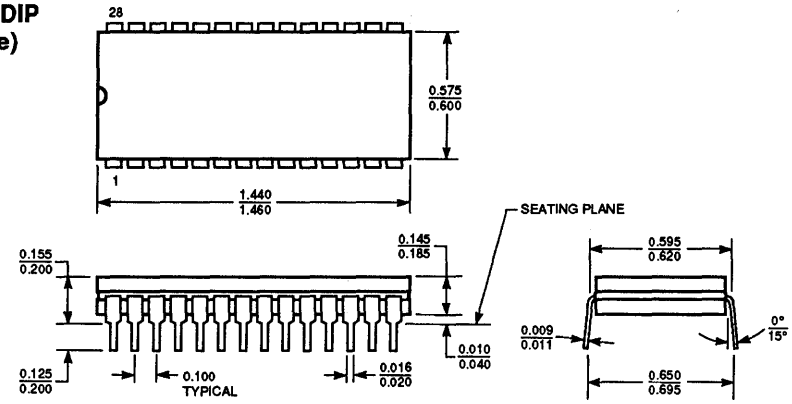
C4 — 24-pin CerDIP (0.6" Wide)



C5 — 28-pin CerDIP (0.3" Wide)

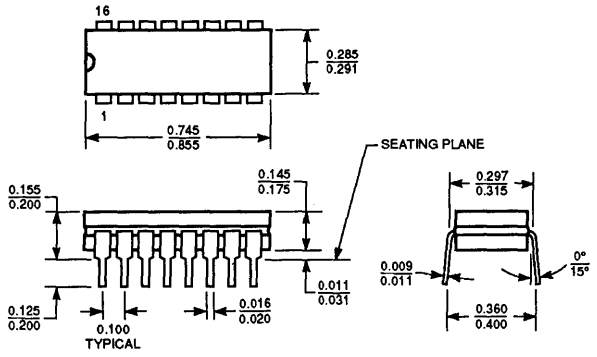


C6 — 28-pin CerDIP (0.6" Wide)

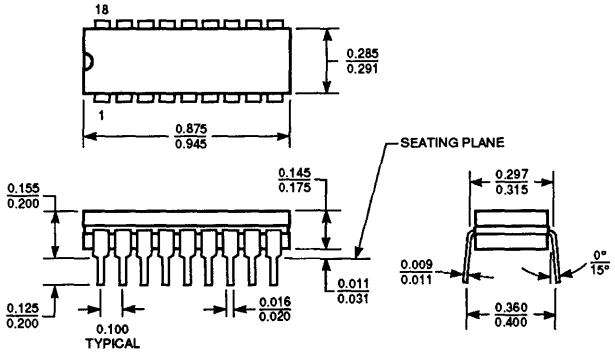


CerDIP — Type C

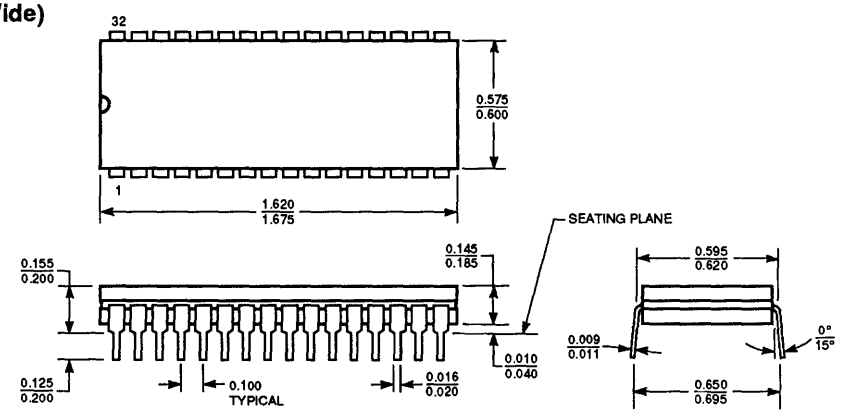
C7 — 16-pin CerDIP (0.3" Wide)



C8 — 18-pin CerDIP (0.3" Wide)



C9 — 32-pin CerDIP (0.6" Wide)



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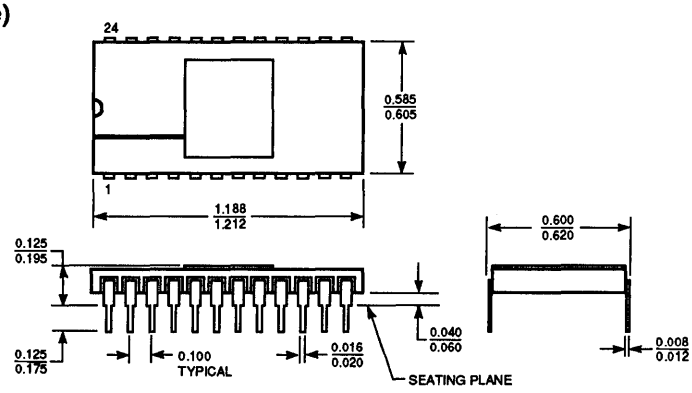
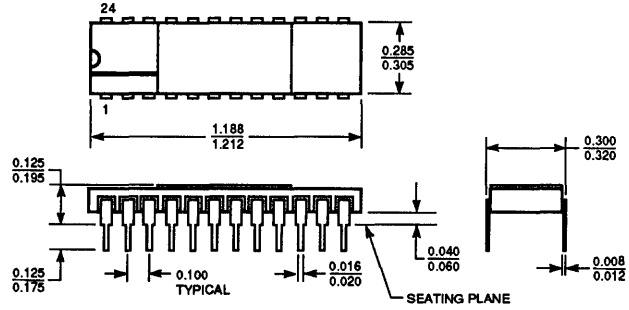
SIDEBRAZE, HERMETIC DIP — TYPE D

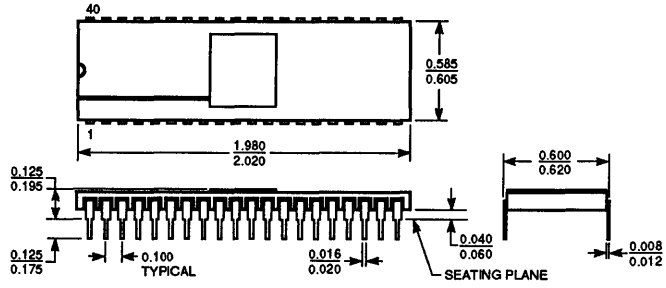
D1 — 24-pin Hermetic DIP (0.6" Wide)



D2 — 24-pin Hermetic DIP (0.3" Wide)

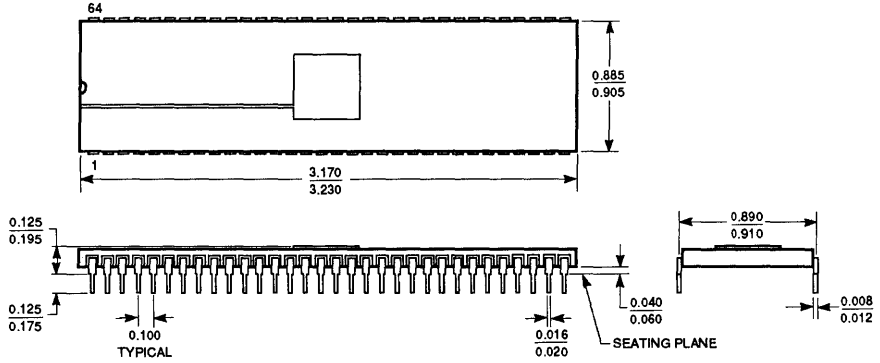


D3 — 40-pin Hermetic DIP (0.6" Wide)

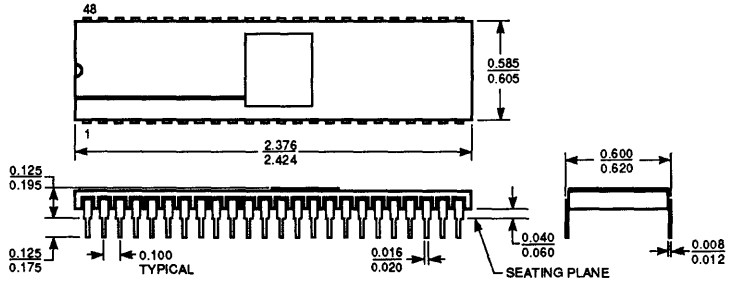


SIDEBRAZE, HERMETIC DIP — TYPE D

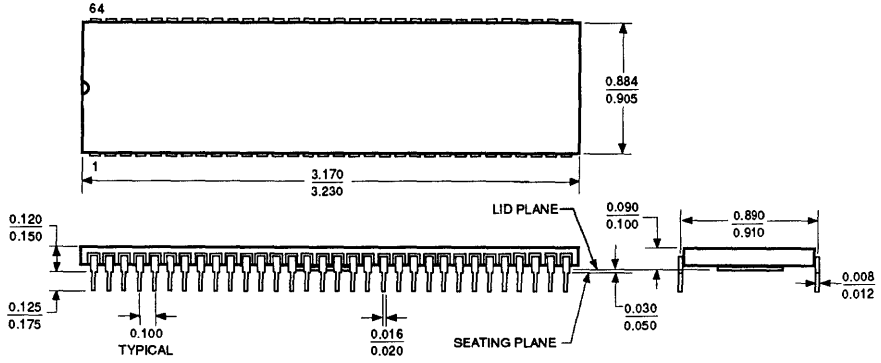
D4 — 64-pin Hermetic DIP (0.9" Wide)



D5 — 48-pin Hermetic DIP (0.6" Wide)



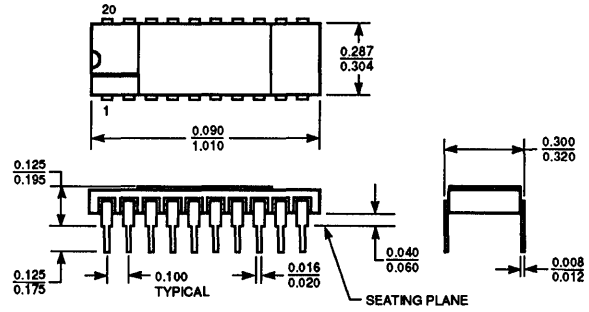
D6 — 64-pin Hermetic DIP (Cavity Down) (0.9" Wide)



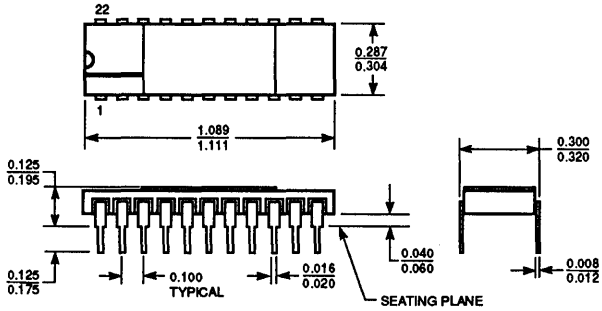
9

SIDEBRAZE, HERMETIC DIP — TYPE D

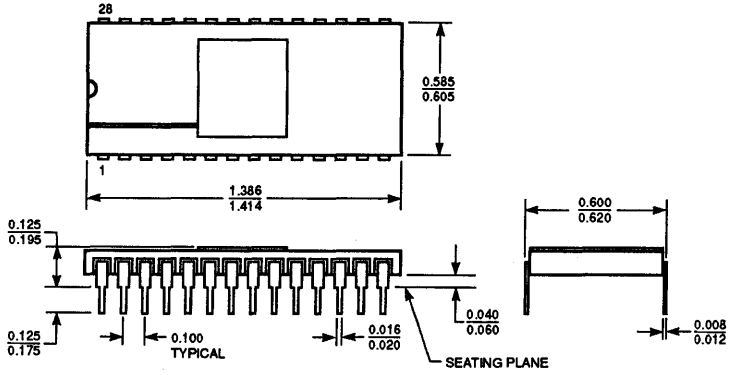
D7 — 20-pin Hermetic DIP (0.3" Wide)



D8 — 22-pin Hermetic DIP (0.3" Wide)

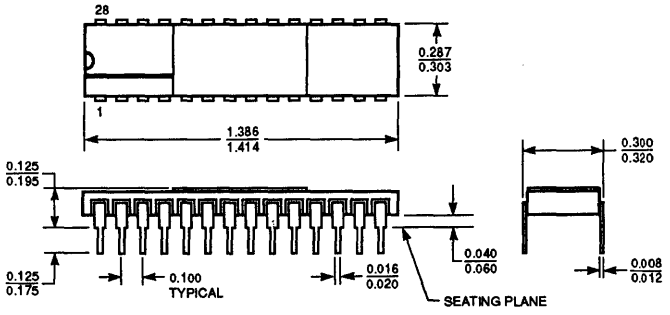


D9 — 28-pin Hermetic DIP (0.6" Wide)

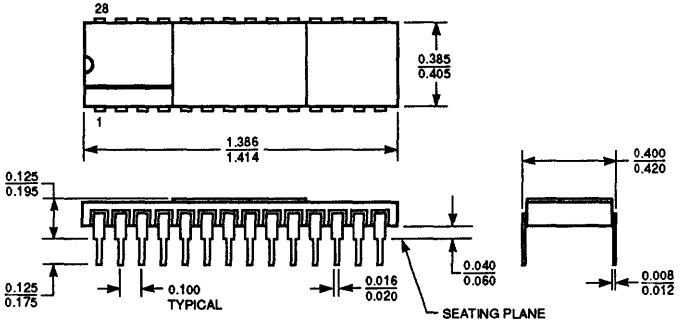


SIDEBRAZE, HERMETIC DIP — TYPE D

D10 — 28-pin Hermetic DIP (0.3" Wide)



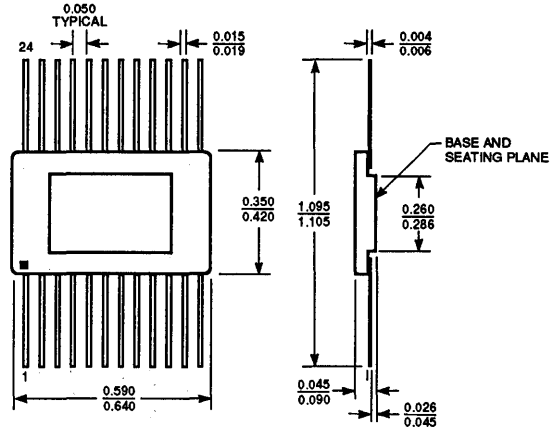
D11— 28-pin Hermetic DIP (0.4" Wide)



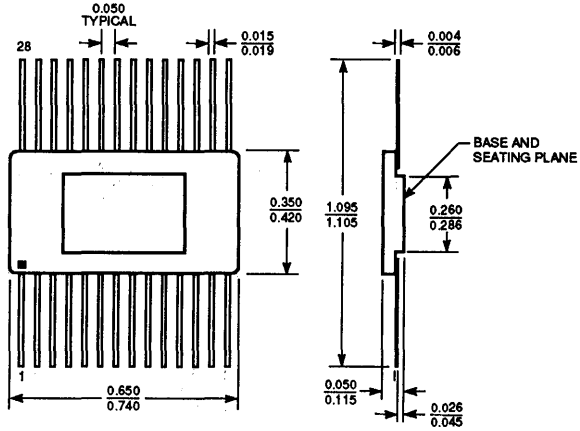
9

Ceramic Flat Pack — Type F

F1 — 24-pin Ceramic Flat Pack

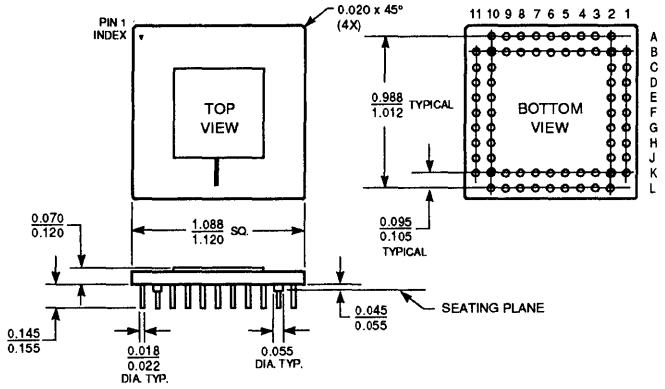


F2 — 28-pin Ceramic Flat Pack

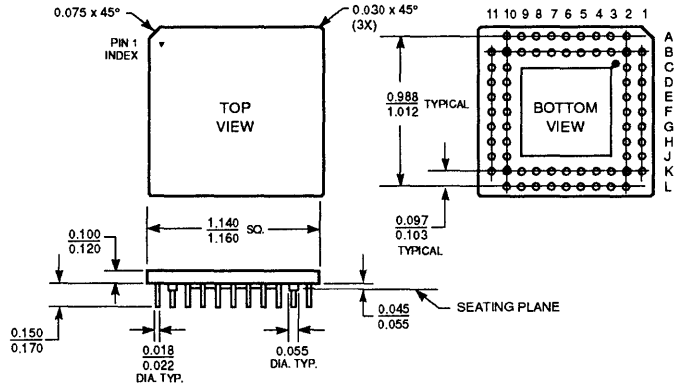


Ceramic Pin Grid Array — Type G

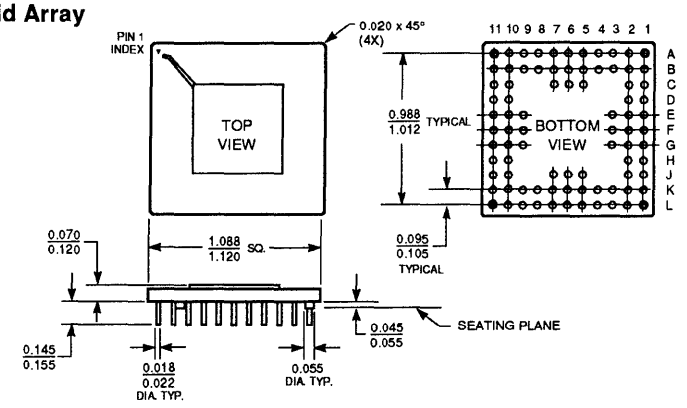
G1 — 68-pin Grid Array



G2 — 68-pin Grid Array (Cavity Down)



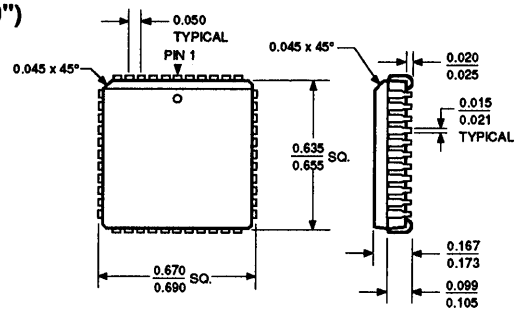
G3 — 84-pin Grid Array



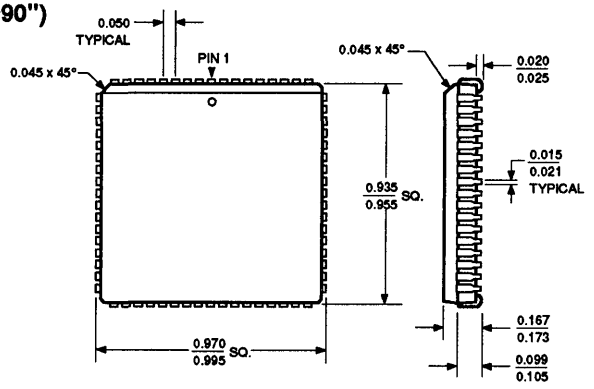
9

Plastic J-Lead Chip Carrier — Type J

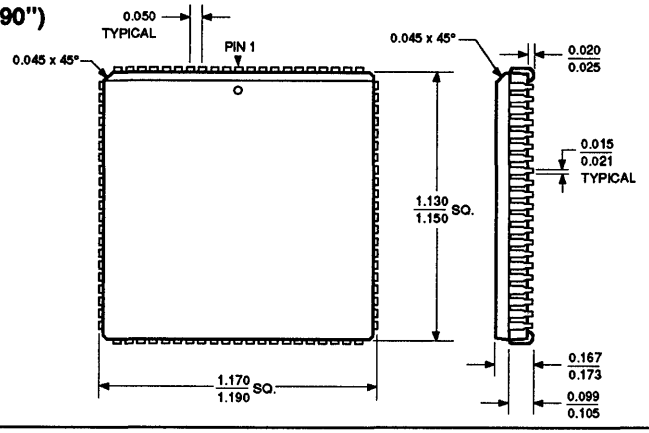
J1 — 44-pin Plastic J-Lead (0.690" x 0.690")



J2 — 68-pin Plastic J-Lead (0.990" x 0.990")

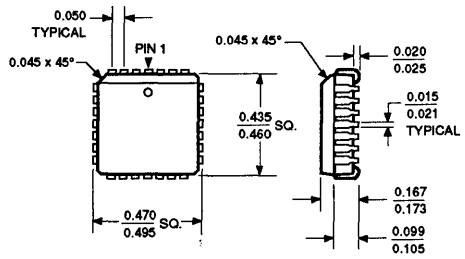


J3 — 84-pin Plastic J-Lead (1.190" x 1.190")

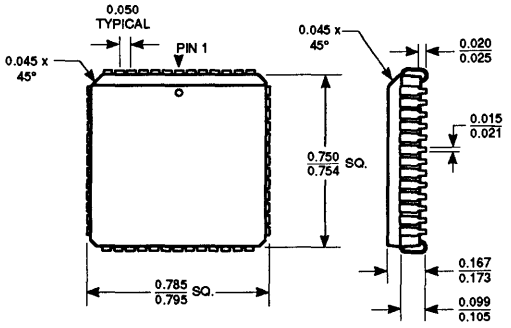


Plastic J-Lead Chip Carrier — Type J

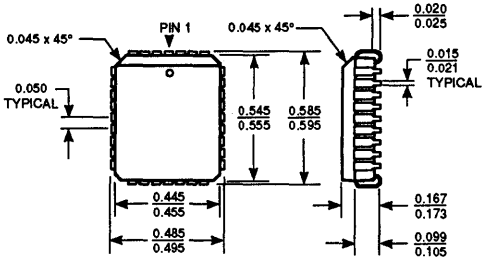
J4 — 28-pin Plastic J-Lead (0.490" x 0.490")



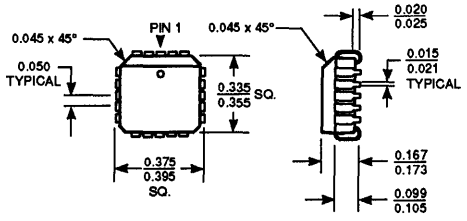
J5 — 52-pin Plastic J-Lead (0.790" x 0.790")



J6 — 32-pin Plastic J-Lead (0.490" x 0.590")



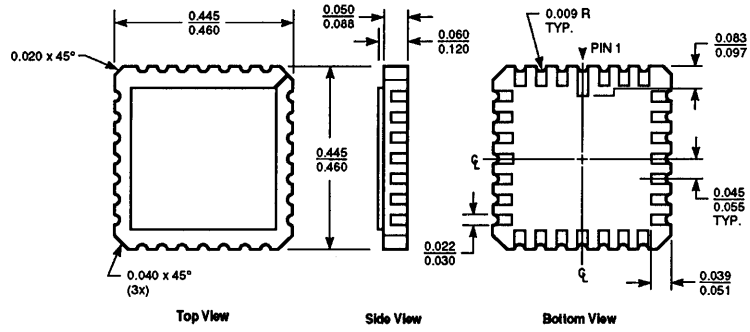
J7 — 20-pin Plastic J-Lead (0.390" x 0.390")



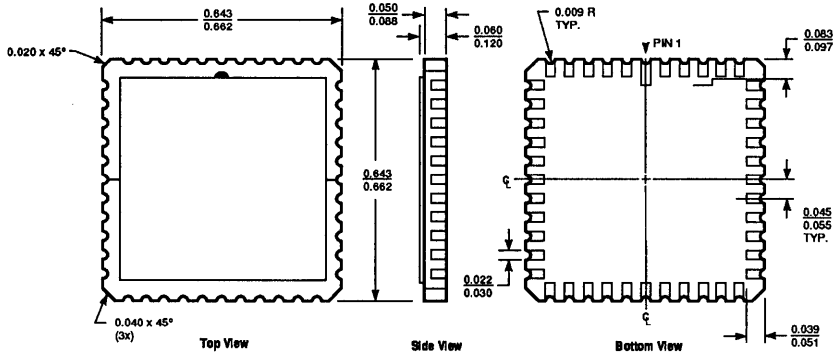
9

Ceramic Leadless Chip Carrier — Type K

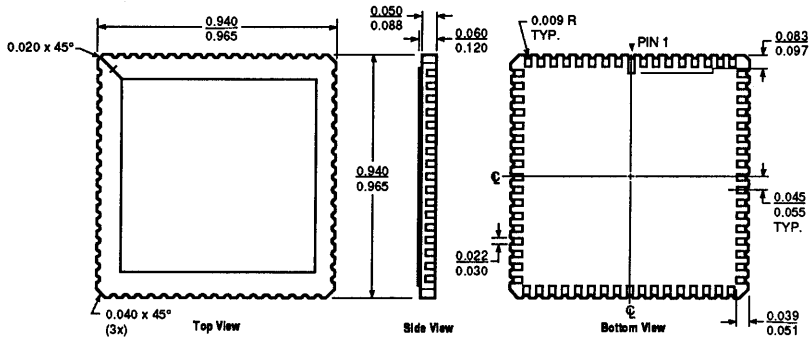
K1 — 28-pin Ceramic LCC (0.450" x 0.450")



K2 — 44-pin Ceramic LCC (0.650" x 0.650")

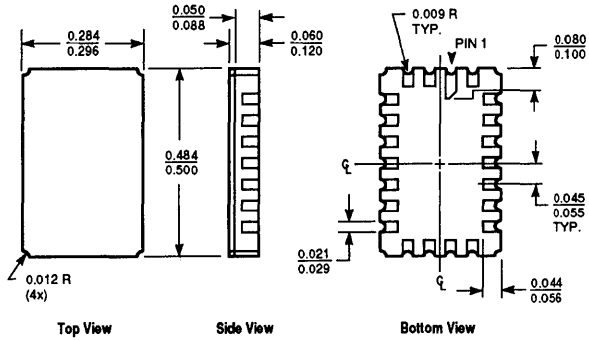


K3 — 68-pin Ceramic LCC (0.950" x 0.950")

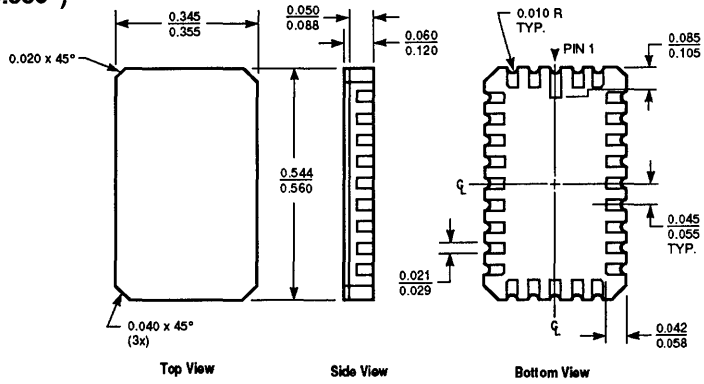


Ceramic Leadless Chip Carrier — Type K

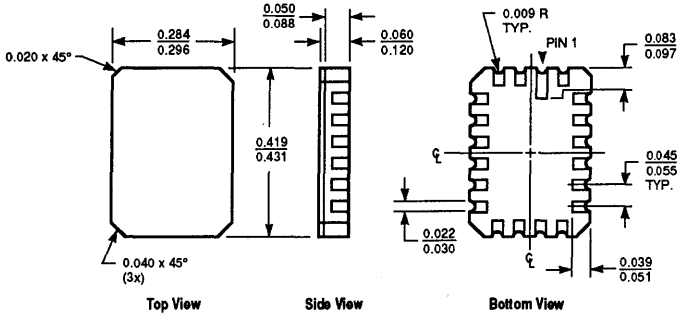
K4 — 22-pin Ceramic LCC (0.290 "x 0.490")



K5 — 28-pin Ceramic LCC (0.350" x 0.550")



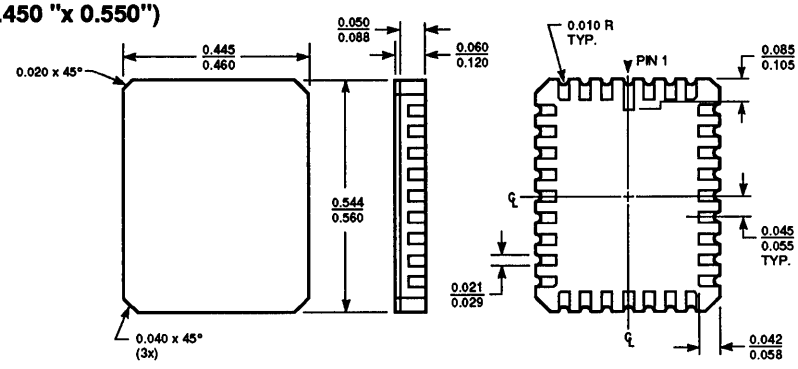
K6 — 20-pin Ceramic LCC (0.290" x 0.425")



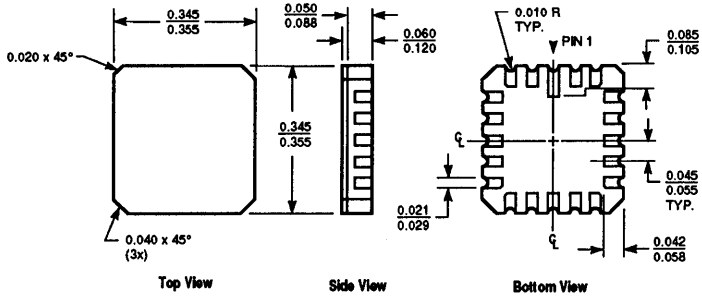
9

Ceramic Leadless Chip Carrier — Type K

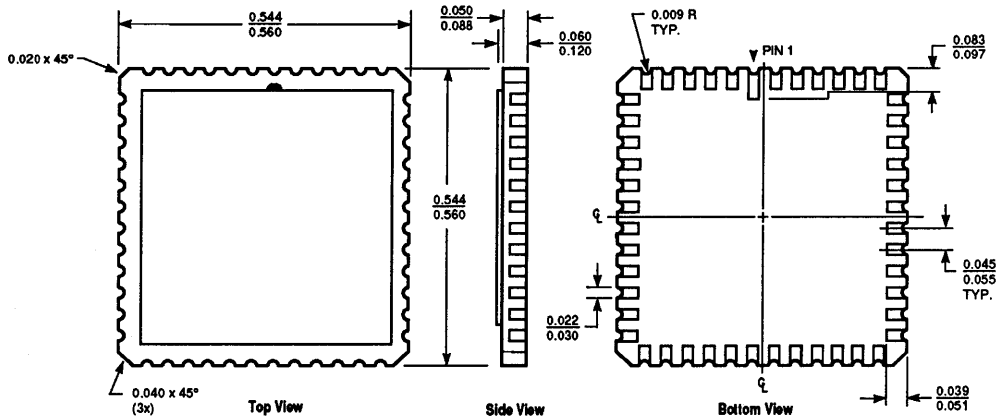
K7— 32-pin Ceramic LCC (0.450 "x 0.550")



K8 — 20-pin Ceramic LCC (0.350" x 0.350")

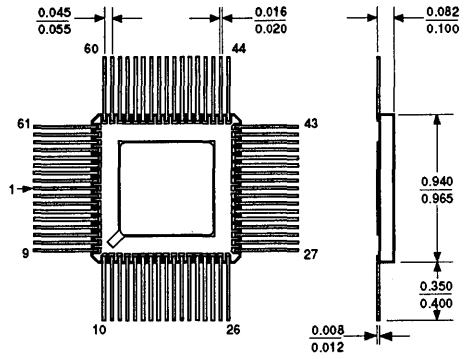


K9 — 48-pin Ceramic LCC (0.550" x 0.550")



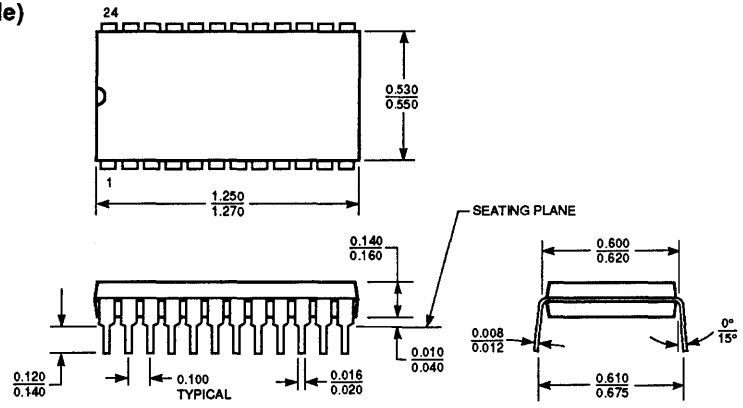
Ceramic Leaded Chip Carrier — Type L

L1 — 68-pin Ceramic Leaded Chip Carrier

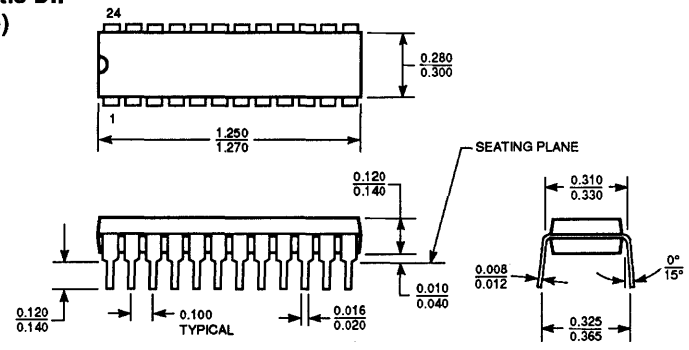


Plastic DIP — Type P

P1 — 24-pin Plastic DIP (0.6" Wide)



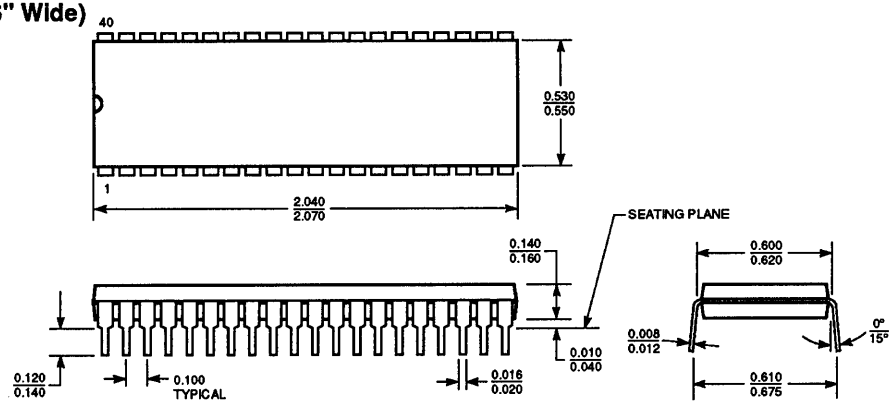
P2 — 24-pin Plastic DIP (0.3" Wide)



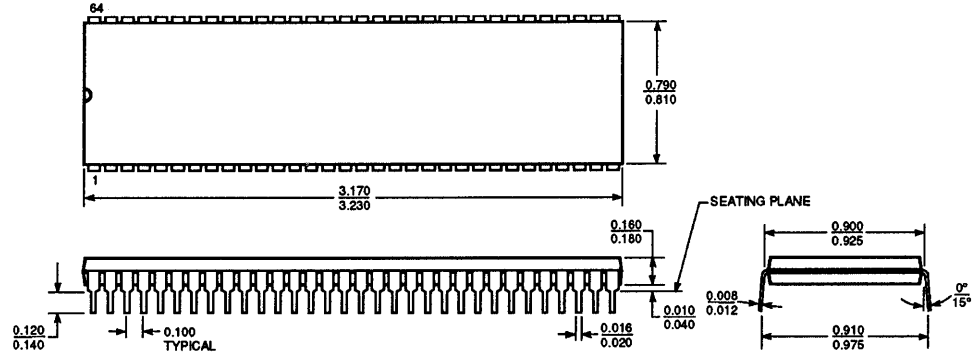
9

PLASTIC DIP — TYPE P

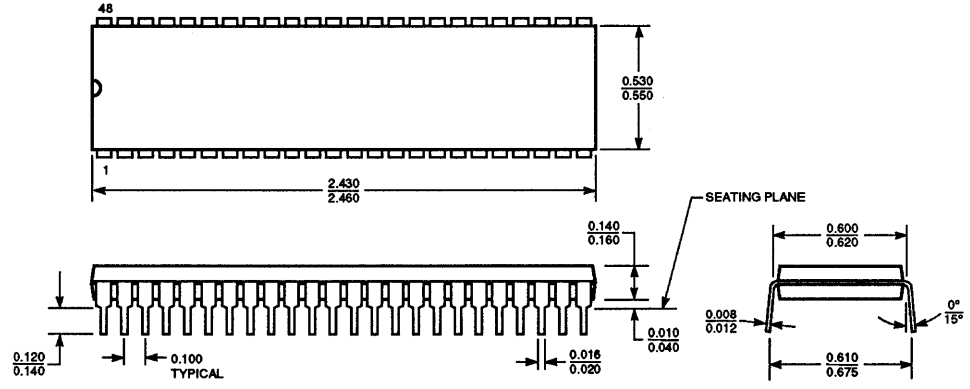
P3 — 40-pin Plastic DIP (0.6" Wide)



P4 — 64-pin Plastic DIP (0.9" Wide)

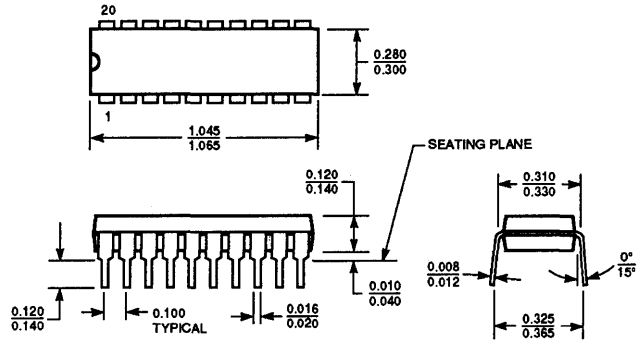


P5 — 48-pin Plastic DIP (0.6" Wide)

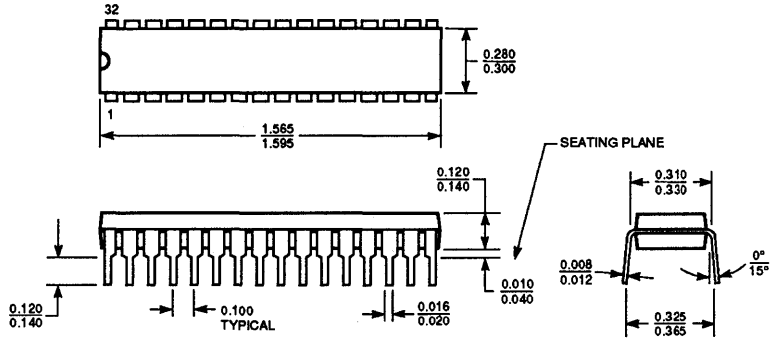


PLASTIC DIP — TYPE P

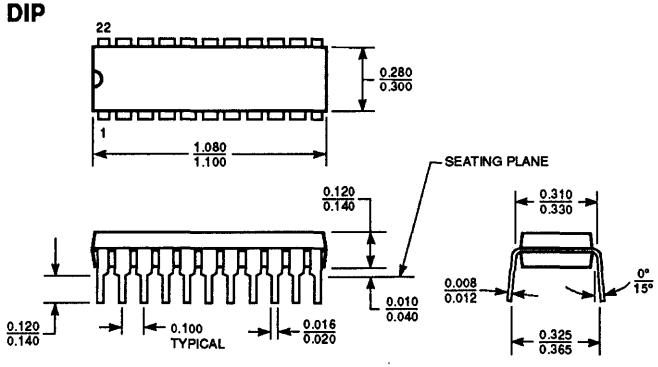
P6 — 20-pin Plastic DIP (0.3" Wide)



P7 — 32-pin Plastic DIP (0.3" Wide)



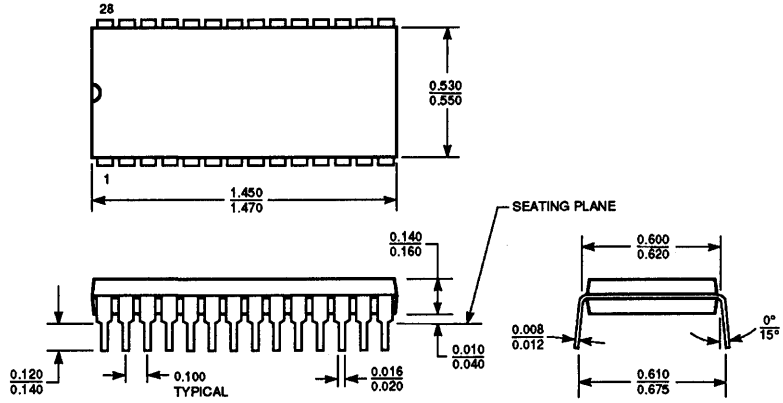
P8 — 22-pin Plastic DIP (0.3" Wide)



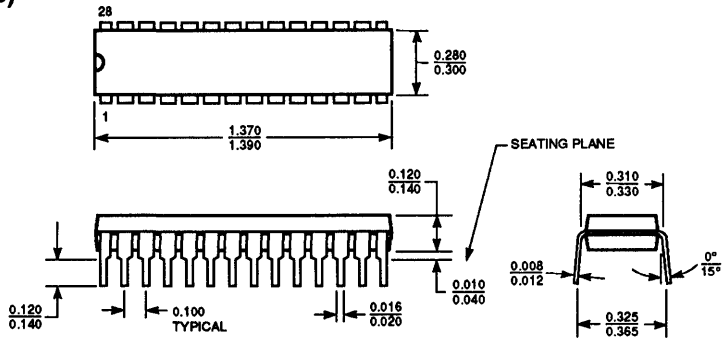
9

PLASTIC DIP — TYPE P

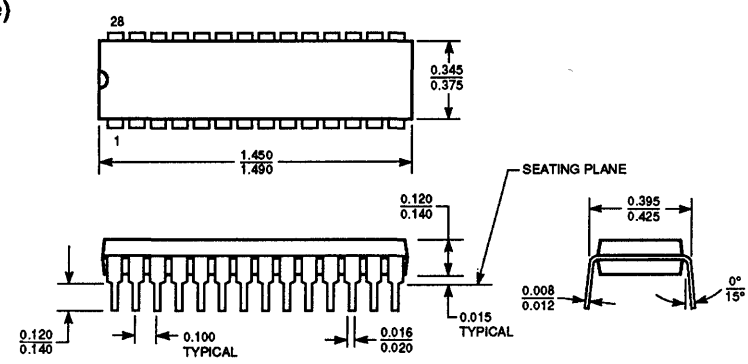
P9 — 28-pin Plastic DIP (0.6" Wide)



P10 — 28-pin Plastic DIP (0.3" Wide)

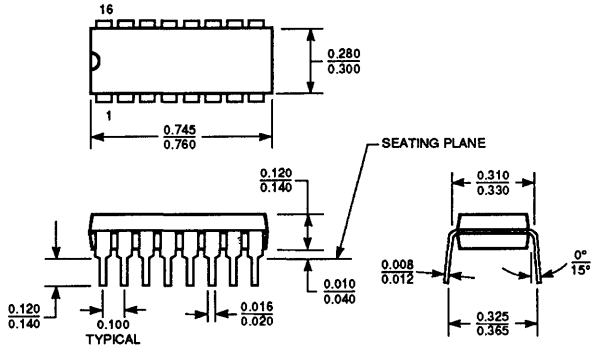


P11 — 28-pin Plastic DIP (0.4" Wide)

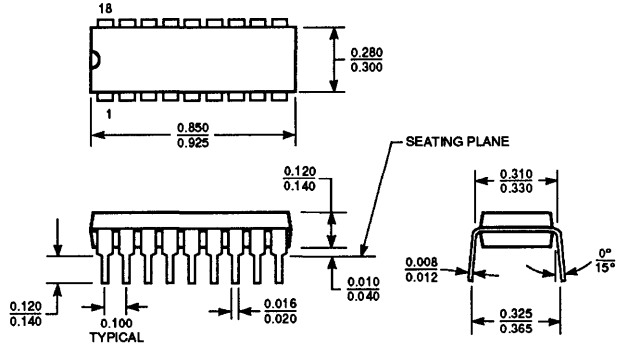


PLASTIC DIP — TYPE P

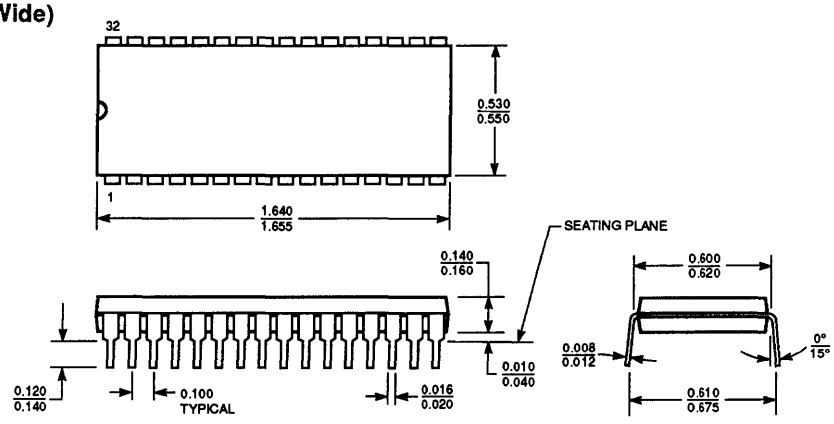
P12 — 16-pin Plastic DIP (0.3" Wide)



P13 — 18-pin Plastic DIP (0.3" Wide)



P14 — 32-pin Plastic DIP (0.6" Wide)



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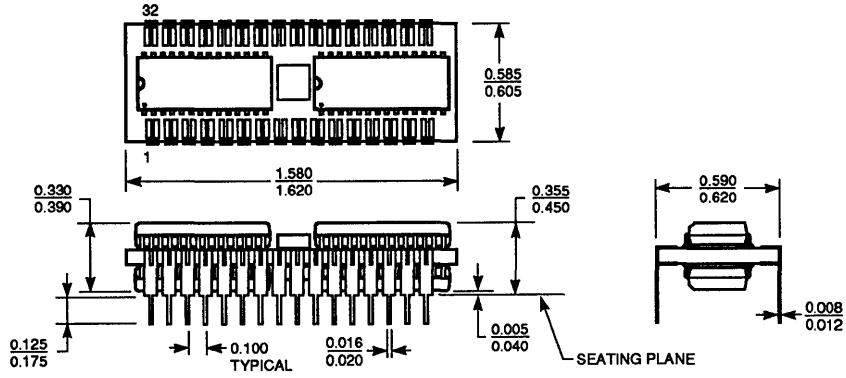
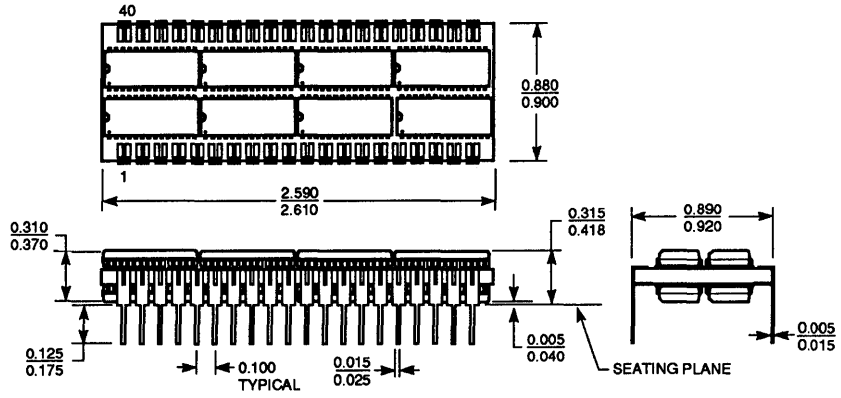
PLASTIC DIP — TYPE P

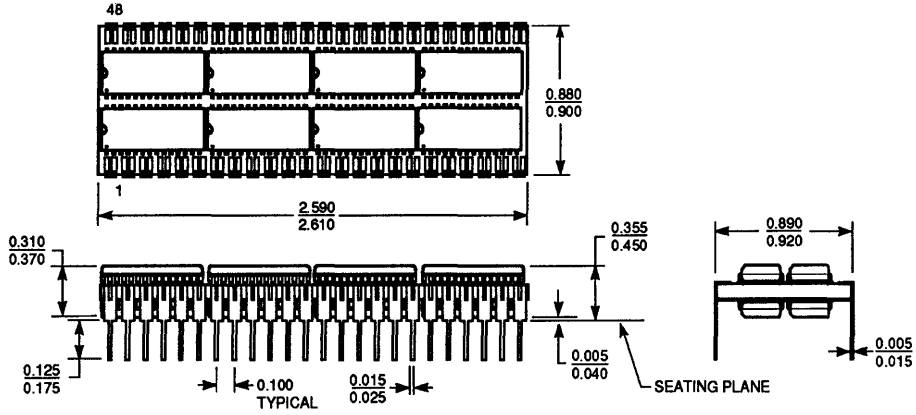
P15 — 32-pin DIP Module



P16 — 40-pin DIP Module

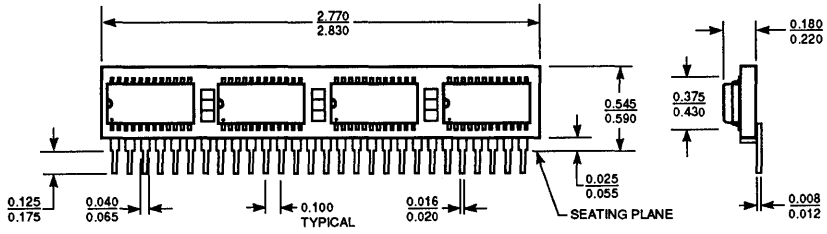


P17 — 48-pin DIP Module



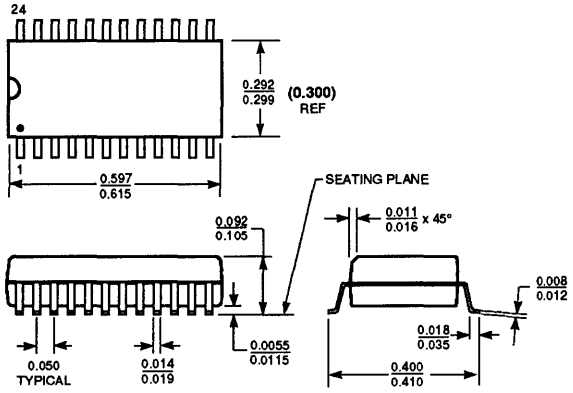
SIP Substrate — Type S

S1 — 28-pin SIP Module

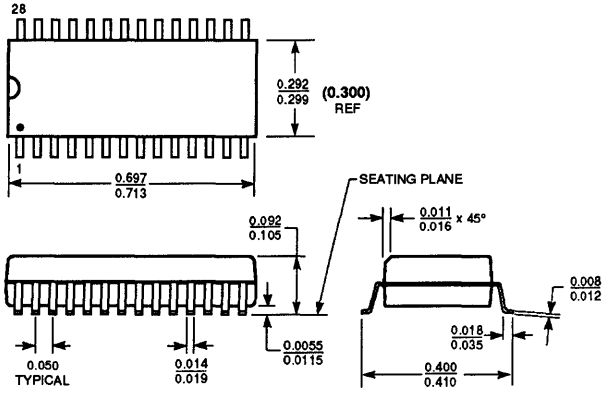


Plastic SOIC (Gull-wing) (0.300" wide) — Type U

U1 — 24-pin Plastic SOIC (0.300" Wide)



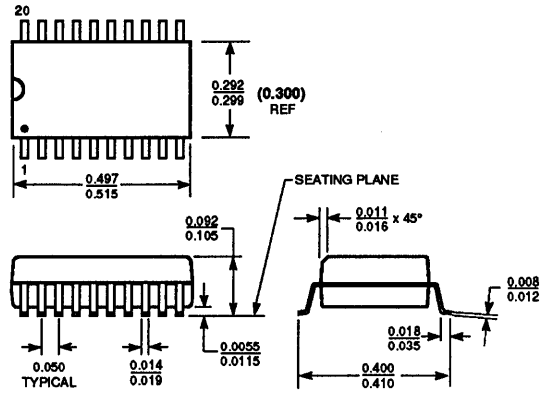
U2 — 28-pin Plastic SOIC (0.300" Wide)



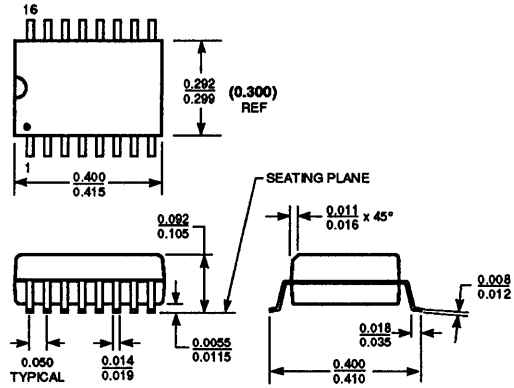
9

PLASTIC SOIC (GULL-WING) (0.300" WIDE) — TYPE U

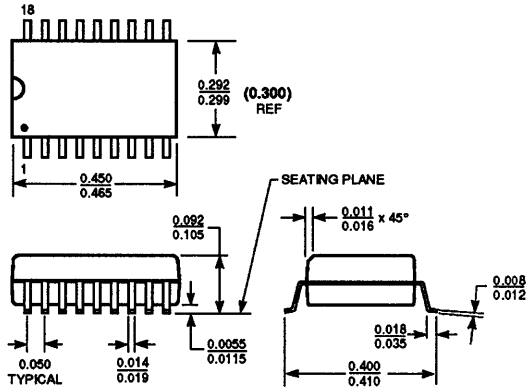
U3 — 20-pin Plastic SOIC (0.300" Wide)



U4 — 16-pin Plastic SOIC (0.300" Wide)

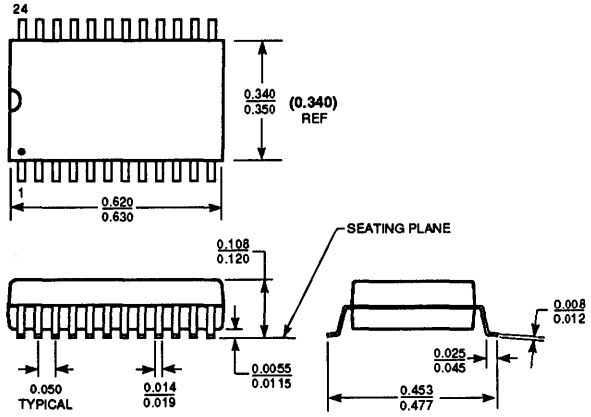


U5 — 18-pin Plastic SOIC (0.300" Wide)

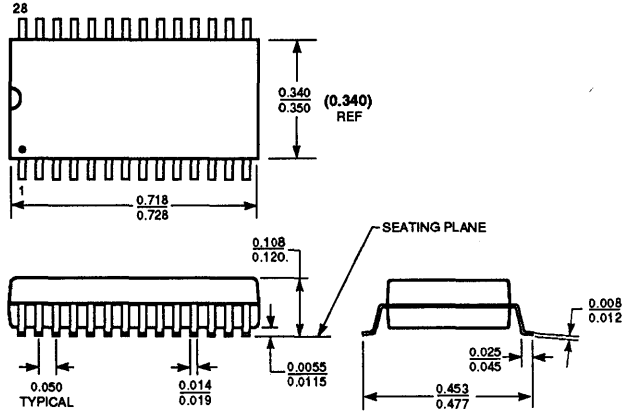


Plastic SOIC (Gull-wing) (0.340" wide) — Type V

V1 — 24-pin Plastic SOIC (0.340" Wide)



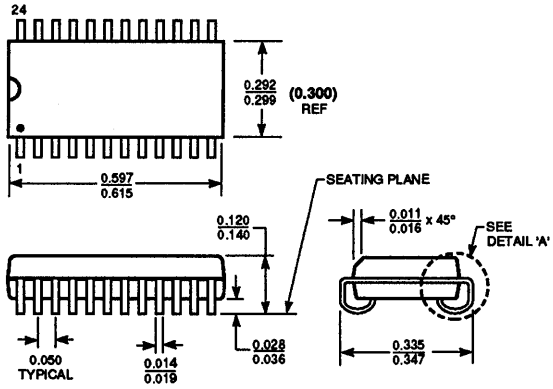
V2 — 28-pin Plastic SOIC (0.340" Wide)

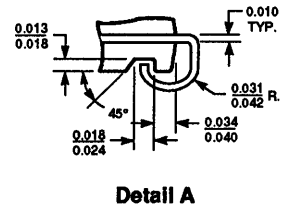


9

PLASTIC SOJ (J-LEAD) — TYPE W

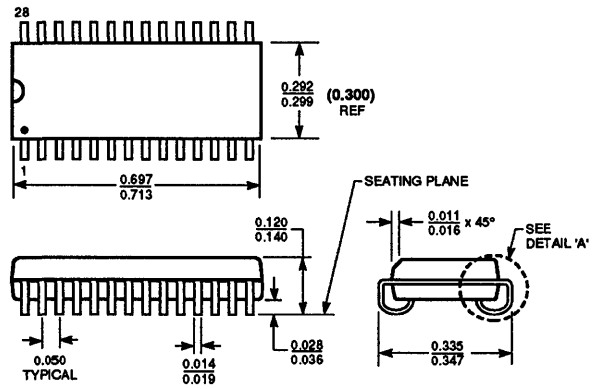
W1 — 24-pin Plastic SOJ (0.300" Wide)



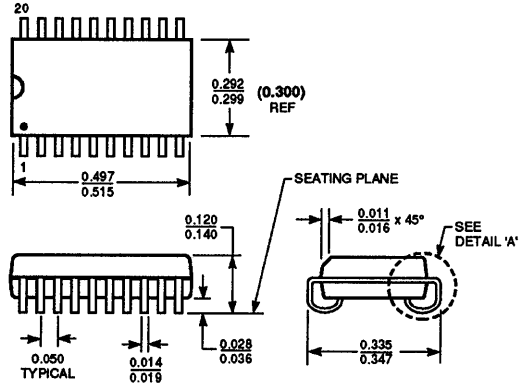


Detail A

W2 — 28-pin Plastic SOJ (0.300" Wide)

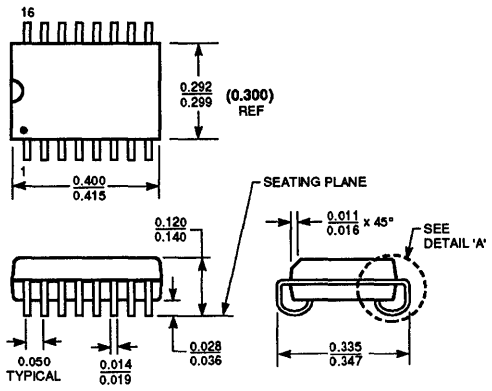


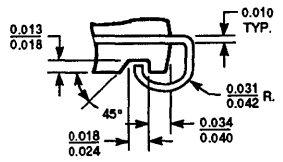
W3 — 20-pin Plastic SOJ (0.300" Wide)



Plastic SOJ (J-lead) — Type W

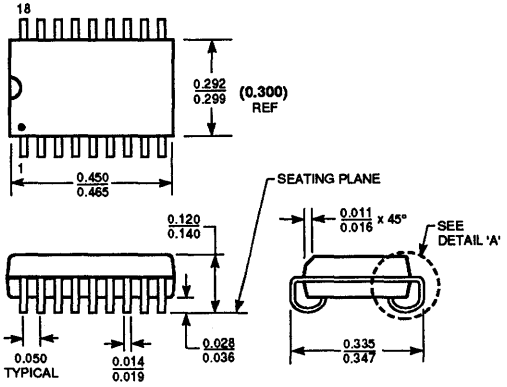
W4 — 16-pin Plastic SOJ (0.300" Wide)





Detail A

W5 — 18-pin Plastic SOJ (0.300" Wide)



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Thermal Considerations

The temperature at which a semiconductor device operates is one of the primary determinants of its reliability. This temperature is often referred to as the "junction temperature", although this term is more appropriate for bipolar than MOS technologies. Heat dissipated in the device during operation escapes through a path consisting of one or more series thermal impedances terminating in the surrounding air (see Fig. 1).

The presence of this nonzero thermal impedance causes the temperature of the device to rise above that of the air. Each of the components of the overall thermal impedance causes a rise in temperature which is linearly dependent on the power dissipated in the device. The coefficient is called θ, and has the units °C/W. The θ value for each thermal impedance represents the amount of temperature rise across the impedance as a function of the power dissipation. Usually, θ is given a subscript indicating the two points between which the impedance is measured. Thus the junction temperature of an operating device is given by:

$$T_j = T_{AMB} + (Pd \bullet \theta_{JA})$$

where:

T_j = junction temperature of the device, °C,

T_{AMB} = ambient air temperature, in°C

Pd = power dissipation of the device, in W,

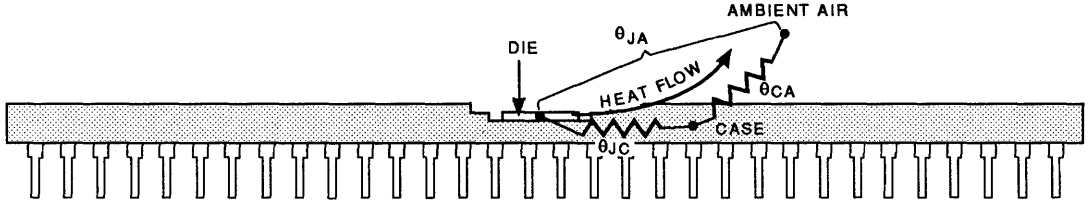
θ_{JA} = sum of all thermal impedances between the die and the ambient air, in °C/W.

The thermal impedance of a given device is dependent on several factors. The package type is the predominant effect; ceramic packages have much lower thermal impedances than plastic, and packages with large surface areas tend to dissipate heat faster. Another factor which is beyond the control of the device manufacturer but which is nonetheless important is the temperature and flow rate of the cooling air. Secondary effects include the size of the die, the method of attaching the die to the package, and the organization of high power dissipation elements on the die.

Because all Logic Devices products are built with low-power CMOS technology, thermal impedance is less of a concern than it would be for higher power technologies. As an example, consider a typical NMOS multiplier similar to the LMU16, packaged in a 64-pin plastic DIP. Assuming 1 W power dissipation and θ_{JA} of 50°C/W, the actual die temperature would be 50°C above the surrounding air. By contrast, the Logic Devices LMU16 has a typical power dissipation of only 60 mW. This device in the same package would operate at only 3° above the ambient air temperature. Since operating temperature has an exponential relationship to device failure rate (see Quality & Reliability, Section 5), the reduction of die temperature available with Logic Devices low-power CMOS translates to a marked increase in expected reliability.

9

FIGURE 1.



To assist the user in calculating cooling requirements and in making reliability predictions based on MIL-HDBK-217, the following table of estimated θ_{JA} values for Logic Devices products is provided below:

No. Leads	Width (in)	Package Code	Approx. θ_{JA} (Still air)
Plastic Dual-Inline			
20		P6	65–80
22		P8	65–80
24	0.3	P2	60–75
24	0.6	P1	50–70
28	0.3	P10	60–80
28	0.6	P9	50–80
40		P3	50–60
48		P5	40–60
64		P4	40–60
Sidebraze, Dual-Inline			
20		D7	35–45
22		D8	35–45
24	0.3	D2	30–40
24	0.6	D1	25–40
28	0.3	D10	30–40
28	0.6	D9	25–40
40		D3	25–35
48		D5	20–40
64		D4	20–30
64	Cav. dn	D6	20–30

No. Leads	Width (in)	Package Code	Approx. θ_{JA} (Still air)
CerDIP, Dual-Inline			
20		C2	60–75
22		C3	60–75
24	0.3	C1	55–70
24	0.6	C4	40–55
28	0.3	C5	55–70
28	0.6	C6	40–55
Pin Grid Array			
68		G1	40–60
68	Cav Dn	G2	30–50
84		G3	20–40
Plastic J-Lead Chip Carrier			
28		J4	50–70
44		J1	40–60
68		J2	35–55
84		J3	35–55
Ceramic Leadless Chip Carrier			
28		K1	40–60
44		K2	35–60
68		K3	25–50
84		K4	20–40

No. Leads	Width (in)	Package Code	Approx. θ_{JA} (Still air)
Plastic SOIC (Gull-Wing)			
24		U1	65–80
28		U2	60–75
Plastic SOJ (J-Lead)			
24		W1	65–80
28		W2	60–75

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Real-Time Digital Image Transformation

by

Joel H. Dedrick

This application brief describes the design of a special effects generator for commercial broadcast television application. It demonstrates efficient realization of real-time pixel filtering, two dimensional interpolation, first order coordinate transformation, and display memory address generation. These operations are used in a variety of applications including mechanical and electrical CAD/CAM, image recognition, machine vision, RADAR/SONAR display processing, and other similar problems in which two or three dimensional data must be reformatted or manipulated for display.

Introduction

The television special effects generator is commonly used to provide a range of effects for broadcast use. These include the inclusion of reduced size, live or frozen inset pictures (e.g., "scene of the accident" shots in news programs) contained anywhere in the main video shot. Also, causing images or text (the network logo, a photograph and statistics of an athlete, etc.) to overlay the main video, and to be moved around the screen, rotated, and sized as appropriate.

The design described here can accomplish any first order translation (displacement in 2D space), rotation, and scaling (enlargement or reduction) on the input image in real time. By first order we mean that the translation, rotation, and scaling of the image is constant throughout the image for a given direction (X or Y), and thus no curvature of the image may be produced. Introducing second or higher order warping is a straightforward extension of the concepts presented. By real time, we mean that the system is capable of altering the effect generated throughout its range on a frame-by-frame basis, effectively providing for smooth progressions in the translation, rotation, and scaling operations giving the appearance of motion of the processed image around the screen.

Image Transformation — A System Overview

The image transformation system works essentially in two steps: First, the incoming image is lowpass filtered in both the vertical and horizontal directions. This is done because the effect required may include shrinking the picture. This essentially amounts to subsampling, or extracting every "n^{th}" pixel sample from the input image to form the output image. Subsampling the input image without filtering would result in aliasing, since the new spatial sample rate may be insufficient to meet the Nyquist criterion. (The Nyquist criterion for calculating the required sample rate in a sampled data system states that the sampling frequency must be at least twice that of the highest frequency component in the signal. Aliasing is the term for the type of distortion which occurs if this condition is not met.)

It is important to note that the cutoff frequency for the lowpass filters should be selected so that the above criterion is met, but a lower cutoff frequency than necessary results in loss of information (a "smearing" of the output image). For this reason, the cutoff frequency, and therefore the coefficients, of this filter must be adjusted according to the amount of scaling desired. This is done independently in the horizontal (X) and vertical (Y) directions.

The second step in the transformation process is to extract the individual pixels in the input image in the specific sequence required to form the output image.

Simple Transformation Examples

Some examples of the transformation process will illustrate the steps required:

For a simple shrink of an image by a factor of two in each direction, (Figs. 1 and 2) every other pixel (PIcture ELement) of the image would be extracted to form a scan line in the output image. Since this results in only half the number of pixels required on the scanline for television, the remaining pixels are blanked. Similarly, in the

vertical direction every other scanline is skipped, effecting a similar shrink along the Y axis.

The capability of moving the input image around the output image plane, called translation, is accomplished during the creation of the output image. By controlling on a line-by-line basis, when the sampling of the input image begins, and by blanking all pixels which map to coordinates outside the input image, translation can be accomplished. In addition to scaling, Fig. 2 shows translation of the (reduced size) input image to the center of the output image.

A more complex example arises when the image must be reduced in size as above, and also rotated 45° (Fig. 3). In this case, the scan direction (order in which pixels are displayed to produce an image) has changed between the input and output image, as shown by the arrows in Fig. 3. Because the in-put image is now being scanned at an angle rather than in the normal horizontal direction, the desired sample points will generally fall in between the actual locations of available pixels (Fig. 4). Note that this will also occur with simple scaling when the scale factor is not an integer. Because of this phenomenon, some type of interpolation will be required

Figure 1. Normal TV image.

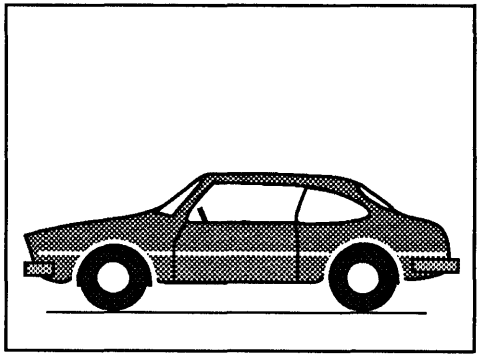


Figure 2. Same image after 2:1 shrink in both axes, and translation to center of output frame.

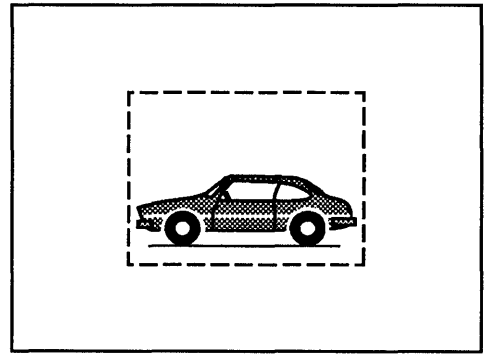


Figure 3. Addition of 45° rotation to the scaled image. The arrows show the scan directions in the input (small arrow) and output coordinate frames.

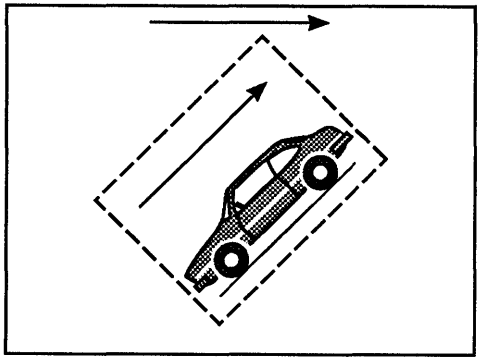
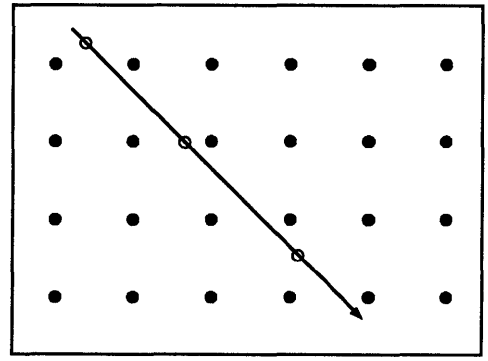


Figure 4. Sample points on one scanline through the input to form the result in Fig. 3. The black dots are the input (normal) image samples, the white dots are the desired sample points for the scaled and rotated output. The sample rate is reduced (spacing increased) to shrink the image, and the scan angle causes rotation.



to calculate the value of a point which does not fall exactly on a pixel location. For the system under discussion, bilinear interpolation is used for this calculation.

Image Transformation System Implementation

The video effects generator block diagram is shown in Fig. 5. Television signals are expressed digitally as three channels of data. One channel, containing luminance or brightness information, is sampled at 14.3 MHz. The other two channels together express the chrominance or color of the image, and the aggregate of these also represents a 14.3 MHz data stream. It is common practice to split the datapath into two halves, one operating on the luminance channel, and the other operating in an interleaved fashion on the chrominance channel, with control information common between the two. The diagram represents a single such channel easily capable of sustaining a 14.3 MHz datarate.

Display Memory, Display Address Counter

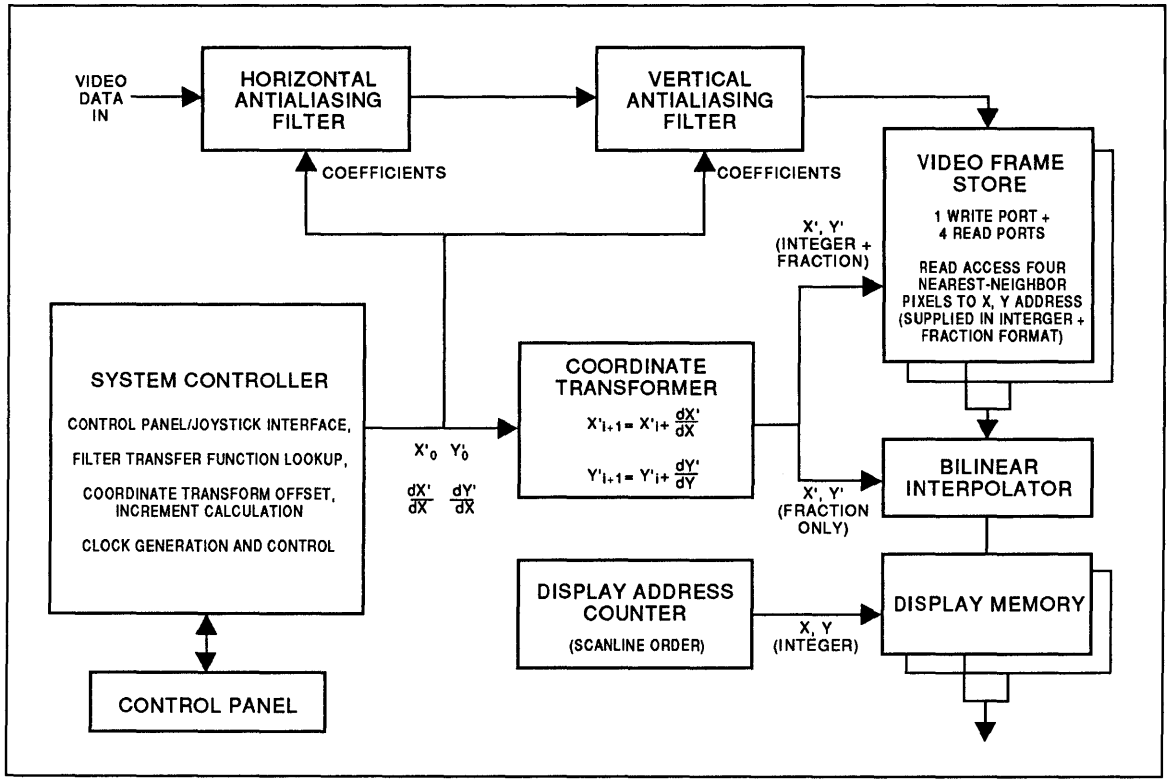
The system is composed of several major blocks as shown in Fig. 5. The Display Memory contains the output video image. The address sequence for this memory is provided by a Display Address Counter, which counts in a fixed sequence, scanning the pixels within a line from left to right, and sequential lines from the top to the bottom of the image. The address provided to this memory uniquely selects an individual pixel in the output image, and is denoted by (X,Y), respectively the horizontal and vertical displacement from the upper left corner.

Coordinate Transformer

The Coordinate Transformer calculates the address of the pixel location in the input image, denoted by (X',Y'), corresponding to the location currently addressed by the Display Address Counter. A general first order transformation from one 2D coordinate space to another can be implemented as:

$$X' = aX + bY + c$$
$$Y' = dX + eY + f \qquad (1)$$

Figure 5. Video special effects generator block diagram.



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By appropriate choice of the six coefficients a–f, this set of equations can map any point in the X,Y (output) image plane to the corresponding point in the X',Y' plane if the two images are related by any combination of translation, rotation, and scaling.

However, since the Display Memory (X,Y) is always scanned in a fixed order, a generalized transformation as given above is not required. Significant hardware savings can be realized by taking advantage of the fact that once the input image point corresponding to the first pixel on an output image scan line is known, the locations of successive input points are related to the first by fixed offsets in X' and Y'. This is true because while the input image may be scanned at any angle, the path through the input image corresponding to an output scan line is always a straight line (for first order transformations). Thus, generating addresses in the X',Y' space is reduced to a simple recursion formula requiring only two additions and no multiplications. This formula takes the form:

$$X'_{i+1} = X'_i + dX'/dX$$

$$Y'_{i+1} = Y'_i + dY'/dX \qquad (2)$$

Note here that dX'/dX and dY'/dX are constants, so a simple programmable accumulator suffices to calculate input image addresses once the starting point for a given scanline is known.

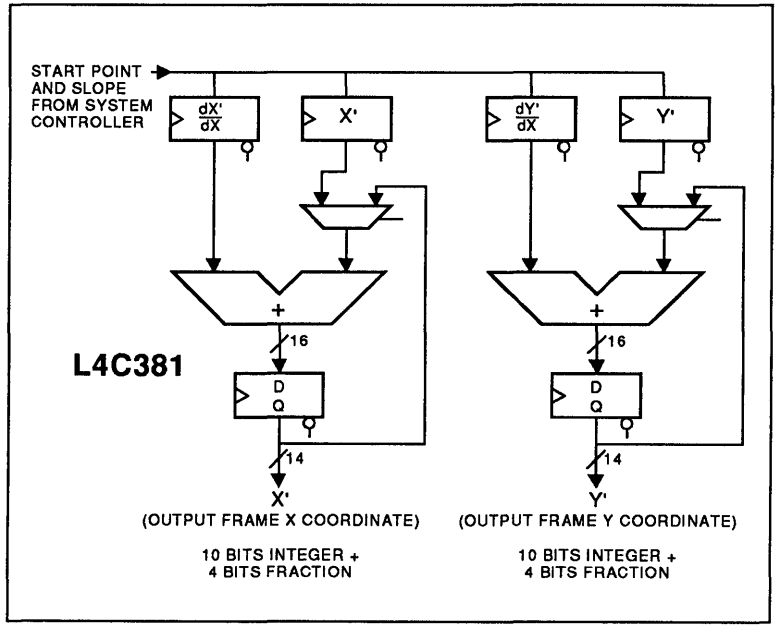
Figure 6 shows the coordinate transformer implemented with two Logic Devices L4C381 ALU's. The operand select function of the L4C381 is used to feed back the contents of the output register to the B input, implementing a programmable-rate increment function. By allocating one ALU for X' and one for Y', the recursions in Eq. (2) are implemented in only two devices. The B operand register of the ALUs holds the starting value for the next scanline, which is passed to the F register to initialize it. The A operand register holds the increment value dX'/dX or dY'/dX which is added to the accumulator (F register) contents on each cycle.

As discussed above, the desired pixel location in general does not correspond to the actual location of a pixel in the Frame Store. As a result, the X',Y' address must provide much finer resolution than the actual pixel grid used in the image. This is accomplished by providing both an integer and a fraction part of the X' and Y' displacements. For example, if 10 bits of integer and 4 bits of fraction (14 bits each for X' and Y') then a 1024×1024 image could be addressed to a spatial resolution of one sixteenth of a pixel. This fine resolution is required to produce adequate interpolation of the pixel value which is stored in the Display Memory. The L4C381 implementation of the coordinate transformer easily meets this requirement: In implementing a 16-bit accumulator for both X' and Y, the L4C381 provides two additional bits of resolution so that the address increments in X' and Y' directions can be specified to a full 16 bits of precision, even though only 14 bits are actually used. This is important because in a recursion formula, small errors in the desired increment accumulate with each cycle. The net effect is quantization error in the desired angle of rotation. The additional bits provide finer control over the desired angle.

Video Frame Store

The Video Frame Store is a RAM bank which stores the filtered input image. It is designed to execute four simultaneous read operations per clock cycle. For each address (X',Y') of the desired location provided by the Coordinate Transformer, the

Figure 6. Coordinate Transformer. The L4C381 ALU is used as an address counter with programmable step size.



Frame Store outputs the values of the *four stored pixel values closest to the addressed point.* In order to accomplish this, only the integer part of the X',Y' address need be considered. If I(X') is taken to mean the integer part of X', and similarly with Y', then for an input address X',Y' the desired four pixel locations are:

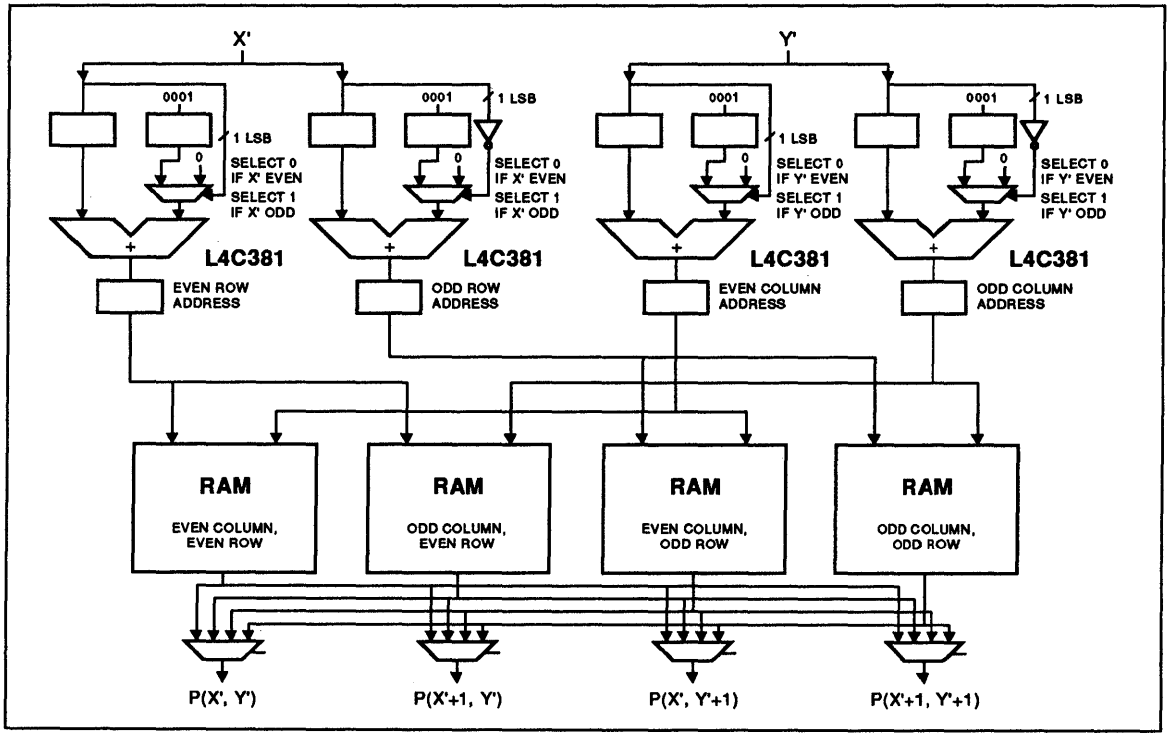
I(X'), I(Y')	I(X')+1, I(Y')
I(X'), I(Y')+1	I(X')+1, I(Y')+1

The organization of a memory capable of executing these simultaneous read operations is shown in Fig. 7. Pixel data is assigned to four internal RAM banks in such a way that adjacent pixels are never stored in the same bank, i.e., one bank is assigned to even row numbers and even column numbers only, etc.

The X' and Y' addresses are processed by a set of L4C381 ALU devices in order to generate internal addresses used to access the four RAM banks. The input X' and Y' addresses are each applied to a pair of ALU's configured so as to selectively increment the address depending on whether it is even or odd. For example, if the Y' address (row number) is even, then the RAM banks containing data for even row numbers should be supplied with this address directly, and those containing odd row numbers should be supplied with Y'+1. Conversely, if Y' is odd, it will be incremented for presentation to the even row RAM, and passed directly to the odd RAM. As an aside, note that since the data for any row is distributed between two RAM banks, the least significant bit of the address generated above will be discarded. This is so that data elements are stored in contiguous locations in the RAM banks, fully utilizing the available storage. As a result, the actual address supplied to the even and odd row data may be the same, or may differ by one.

The X' address is similarly modified to produce internal addresses for even and odd column numbers, and the resulting four addresses are combined to access the four RAM banks. The assumption here is that a row and column address can be concatenated

Figure 7. Video Frame Store. This special purpose memory accepts a desired sample location (X and Y Address) and reads the four pixel values closest to the desired point.



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to address a RAM bank, i.e., the internal plane sizes are integral powers of 2. Once these addresses are formed, four memory accesses are executed in parallel. Finally, multiplexers route the appropriate data to the four output ports, with selection of these muxes again determined by whether X' and Y' are even or odd.

Bilinear Interpolation

The four pixel values read from the Frame Store on each clock cycle are processed by the Bilinear Interpolator to produce the actual value written to the Display Memory. Bilinear interpolation is a means for interpolating a value between sample points in a two dimensional grid. It operates as shown in Fig. 8.

The four shaded points P1–P4 in the figure represent actual pixel values in the Frame Store. These are the four closest pixels to the desired point, denoted by P. P represents location of the point addressed by (X',Y'). As discussed above, X' and Y' have both an integer and fractional part, with the fractional part of each representing offsets in the horizontal and vertical direction *between pixels in the Frame Store.* The interpolator is presented with the four pixel values P1–P4, and the fractional parts of X' and Y', denoted dX' and dY'. The interpolation process can then be derived as follows:

First, the value of an imaginary pixel located between P1 and P2 is determined. This point, labeled P' in Fig. 8, is offset from P1 by dX', the same horizontal offset as the output point P. Unlike P, however, P' has the same vertical value as P1 and P2, so it represents interpolation in the X direction only. P' can be seen in Eq. 3 to be a weighted sum of P1 and P2, with the weights inversely proportional to the distance of P' from P1 and P2.

$$P' = P1(1 - dX') + P2(dX') \qquad (3)$$

Note that the weights applied to P1 and P2, namely (1 – dX') and (dX') sum to one, resulting in no net amplitude gain through this process.

In a similar way, a point P" can be determined which is a horizontal axis interpolation between P3 and P4 (Eq. 4).

$$P'' = P3(1 - dX') + P4(dX') \qquad (4)$$

Having determined P' and P", the final step is to interpolate between these two to determine the desired point P, with the fractional part of the Y axis address dY' used as the weighting factor (Eq. 5).

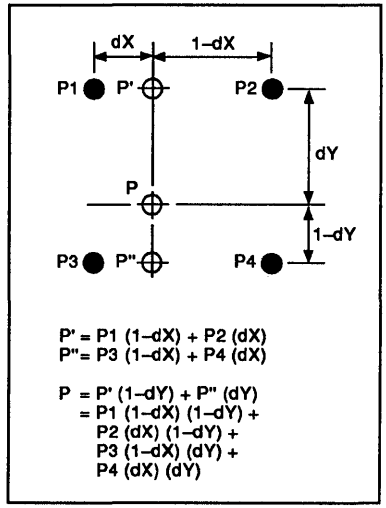
$$P = P'(1 - dY') + P''(dY') \qquad (5)$$

By substituting Eqs. (1) and (2) into (3), the following is obtained:

$$\begin{aligned} P = {} & P1(1 - dX')(1 - dY') + \\ & P2(dX')(1 - dY) + \\ & P3(1 - dX')(dY') + \\ & P4(dX')(dY') \end{aligned} \qquad (6)$$

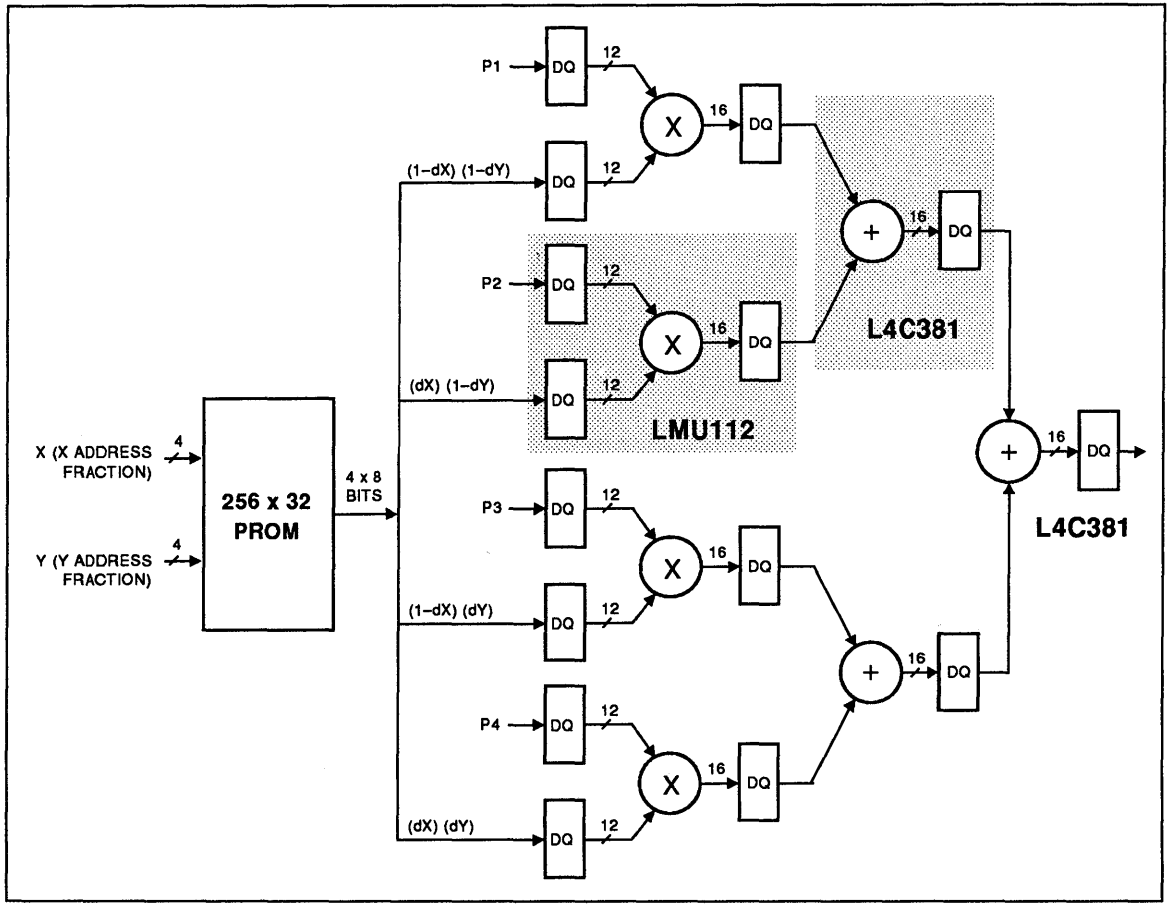
Figure 9 shows the implementation of the bilinear interpolator. The inputs are dX' and dY'; the fractional parts of the coordinate transform address. Each of these fractions is 4 bits, for a total of 8 bits. A 256 word lookup table PROM is used to derive the four weights required for the interpolation in parallel. Four LMU112 multipliers apply these weights to the four pixel values P1–P4 in parallel. The LMU112 is a 12 × 12 multiplier which is available in a 48-pin package, due to the fact that only the 16 most significant outputs are brought out. Since 16 bits of information is more than sufficient for video, it is an appropriate choice to save space over the more typical 64-pin implementations of 12 × 12 multipliers. The four weighted pixel values are then summed using a network of three L4C381 ALU devices. These provide the 16-bit add function required, as well as integrating the pipeline registers necessary to maintain the desired clock rate.

Figure 8. Bilinear Interpolation. Bilinear interpolation involves first executing linear interpolations between two pairs of adjacent points on successive scanlines, resulting in P' and P". Then, a final linear interpolation is performed between these two intermediate results to form an approximation of the image value at the desired location P.



One final function is performed by the interpolator: The transformations available on the input image may result in portions of the output display which contain no video data. A simple instance occurs when the input image is reduced in size, in which case the remaining portions of the display must be blanked. Also, since the amount of size reduction can be changed in real time, the pixels to be blanked must also be set on a scanline-by-scanline basis. This requirement is conveniently met by the L4C381, since its instruction set contains a force-to-zero function. By

Figure 9. Bilinear Interpolator. LMU112 12 x 12 multipliers and L4C381 ALUs form a compact implementation of the equations in Fig. 8. The coefficients are precomputed and stored in PROM.



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setting the function control lines of the last ALU stage to 000 (force-to-zero instruction) when writing the nonimage areas of the display memory, the pixel data stored in these locations is blanked. This instruction control is provided by the system controller.

Horizontal/Vertical Anti-aliasing Filters

Prior to any operation on the data which involves resampling, a lowpass filtering pass must be applied to the data to avoid aliasing distortion. The filter chosen here is a Finite Impulse Response (FIR) type.

Figure 10 shows the conventional flow diagram for an FIR filter. The data is applied to a delay network, the length of which corresponds to the desired filter length. Each delay element output is weighted (multiplied) by the appropriate coefficient, and the results are summed to form the filter output.

Figure 11 shows an alternate, but equivalent implementation of the same flow diagram. In this implementation (known as the transpose form,) the delay elements are distributed through the summation or output path, with the input data distributed simultaneously to all of the weighting operators. This form of the flow graph is more convenient for implementation in LSI form, since it results in a series of identical functional blocks, each of which performs

a multiply, add, and delay function. The dotted line in Fig. 11 illustrates the repeated function, and Fig. 12 shows an implementation of the flow diagram for the horizontal filter using the LOGIC Devices LMS12.

The LMS12 is a filter building block especially suited to the transpose form FIR structure. It provides a 12×12 bit multiplication, and addition of a third input of 26 bits to the result. Thus the FIR structure under consideration can be implemented with no external logic using this device, saving considerable real estate over more conventional implementations using multipliers and discrete external adders and delay elements.

The vertical (Y dimension) filter is formed in a similar way (Fig. 13) except that a delay equal to the length of each horizontal scanline is inserted between each LMS12 and its neighbor. In this way, the input pixels contributing to a given output sample are vertically adjacent, i.e., separated in the input datastream by a number of samples equal to one less than the length of one scanline. Since this filter implementation makes available all of the coefficient registers independently, they can be loaded at any time by the system controller with coefficients appropriate for the cutoff frequency desired.

Figure 10. F.I.R. Filter (Canonical Form).

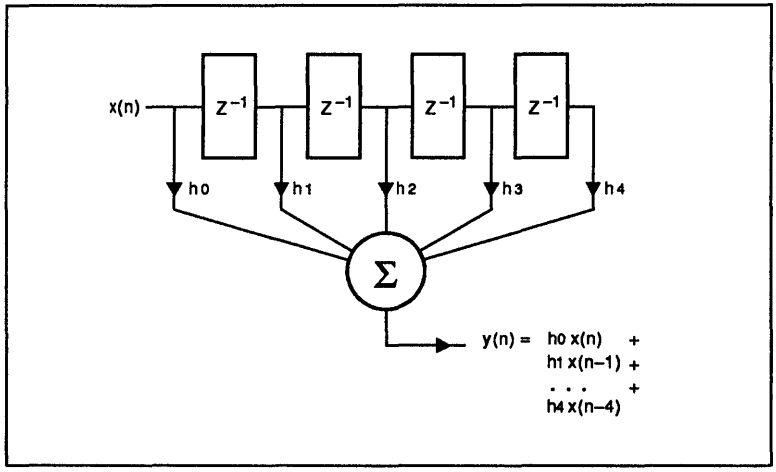


Figure 11. F.I.R. Filter (Transpose Form).
An alternate formulation of the equation in Fig. 10 allowing implementation by cascading identical functional blocks. The summation is now distributed across the filter delay and is therefore inherently pipelined.

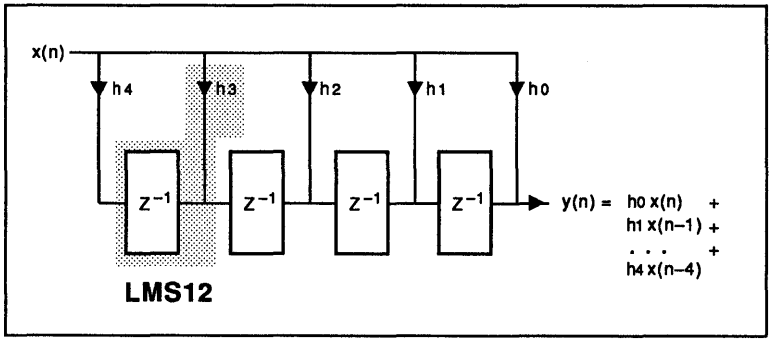


Figure 12. Horizontal Anti-aliasing Filter.
This realization of the transfer function in Fig. 11 uses the LMS12 filter building block. It is capable of exceeding 25 MHz data rates for any filter length, while allowing instantaneous coefficient changes.

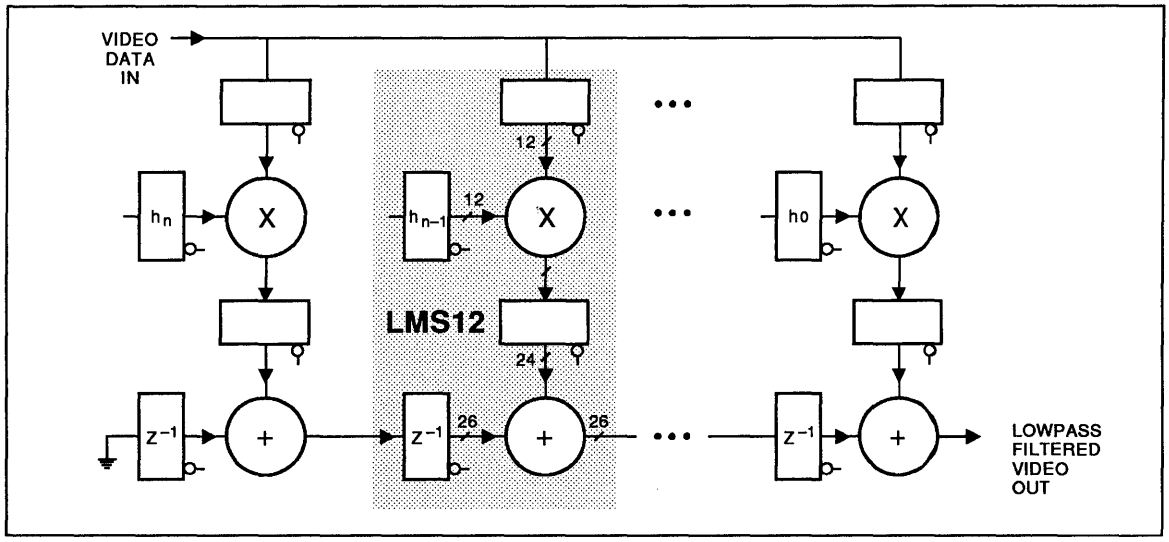
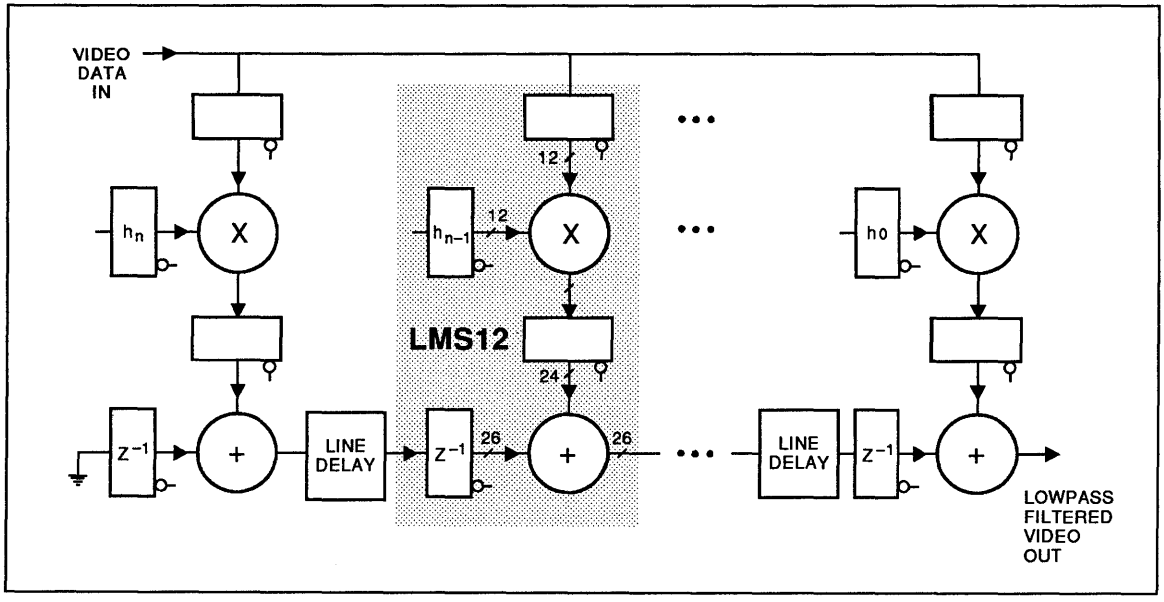


Figure 13. Vertical Anti-aliasing Filter.
A modification of Fig. 12 allows filtering in the vertical direction by inserting a delay equal to the length of a scanline between each pair of filter taps.



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Ultra-High Performance FFT Using DSP 'Designer Chips'

by
Edgar R. Macachor and
Joel H. Dedrick

New high-speed CMOS building blocks provide a clean implementation of the FFT for applications where single-chip DSP microprocessors cannot provide the necessary throughput.

Introduction

As single-chip microprocessors for DSP mature, digital spectrum analysis for low to medium bandwidth application has become widely available at reasonably low cost. For many real-time applications however, the single-chip units do not have the throughput to do the job. This article shows how to determine when you've outgrown a single-chip solution, and gives implementation details for an FFT engine which is 10 to 100 times faster than the single-chip units studied.

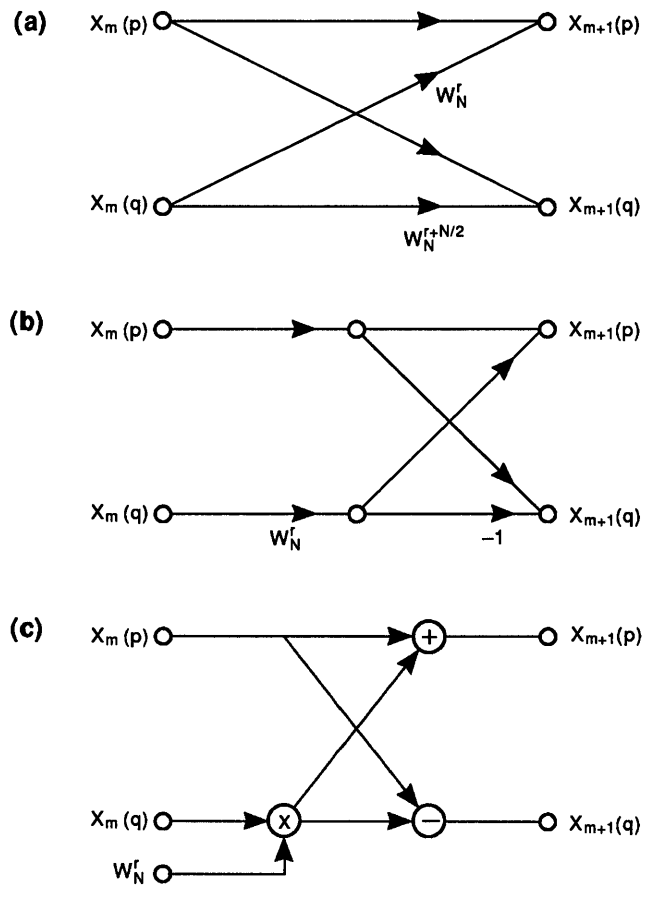
The FFT and Current Single-Chip DSP Microprocessors

In digital signal processing (DSP), the Fast Fourier Transform (FFT) is used to evaluate the Discrete Fourier Transform (DFT) of a signal. Typically, the signal is continuous and periodic in the time domain. To obtain the DFT of a continuous signal, the FFT is necessary to reduce the computation time. For example, if the original signal is represented as having real and imaginary components and sampled N times during its full period it takes $4N^2$ multiplications and N(4N–2) additions to compute the DSP directly. In contrast, the FFT, in particular the decimation-in-time algorithm, only requires $(N/2)\log_2 N$ stages of multiplications and additions. Each stage is defined by the basic cell of the FFT, the butterfly flow graph, and shown in Fig. 1(a) using the notation of Ref. 1. By taking advantage of the symmetric property of the W_N^r term, Fig. 1(b) allows for better computational efficiency. Figure 1(c) is further obtained to serve as the working model and shows that four multiplications, three additions and three subtractions are required per butterfly. The additions and subtractions are combined with the multiplications via a multiplier/accumulator (subtractor) unit.

The FFT butterfly computation can be accomplished using presently available single-chip DSP units. These current third-generation products can be categorized into two groups. The first group contains some on-chip memory to hold the executable instructions and the data to be processed. The TI TMS32010/20 and the NEC μPD77230 belong to this group. The architecture of these devices allows the process to be "optimized" if both program and data are in the on-chip memory at all times throughout the whole process. However, the computational throughput is still slow since only two data elements can be operated on at any given cycle. Another drawback is that, if the number of sample data points to be processed exceeds the on-chip memory capacity, then data need to be stored externally. As a result, additional cycles to fetch data from external memory further degrade the computational throughput. Still another factor is the increase in software overhead. Since data is now fetched from external memory, instructions that would have enabled parallel processing cannot be taken advantage of anymore. Therefore, one has to resort to straight-line coding to get maximum performance at the expense of increasing the code size.

The second group of "single-chip" DSP units require external memory for program and data storage. The National LM32900 and the Analog Devices ADSP2100 belong in this category. Their architecture allows for efficient access to both program and data memory via independent busses. However, these DSP units still can only process one set of operands at

Figure 1. Butterfly Cell working models



$$X_{m+1}(p) = X_m(p) + X_m(q)\,W_N^r$$
$$= \{Re[X_m(p)] + (A-D)\} + \{Im[X_m(p)] + (B+C)\}$$

$$X_{m+1}(q) = X_m(p) - X_m(q)\,W_N^r$$
$$= \{Re[X_m(p)] - (A-D)\} + \{Im[X_m(p)] - (B+C)\}$$

$A = Re[X_m(q)] \cdot Re[W_N^r]$ $\quad C = Re[X_m(q)] \cdot Im[W_N^r]$

$B = Re[W_N^r] \cdot Im[X_m(q)]$ $\quad D = Im[X_m(q)] \cdot Im[W_N^r]$

any given cycle. For FFTs involving 32-bit complex data, external memory fetch cycles degrade the computational throughput. One method of improving the performance is by operating two devices in parallel to handle two sets of operands at a time. In this case, however, the user is faced with issues regarding synchronization and control of the two devices.

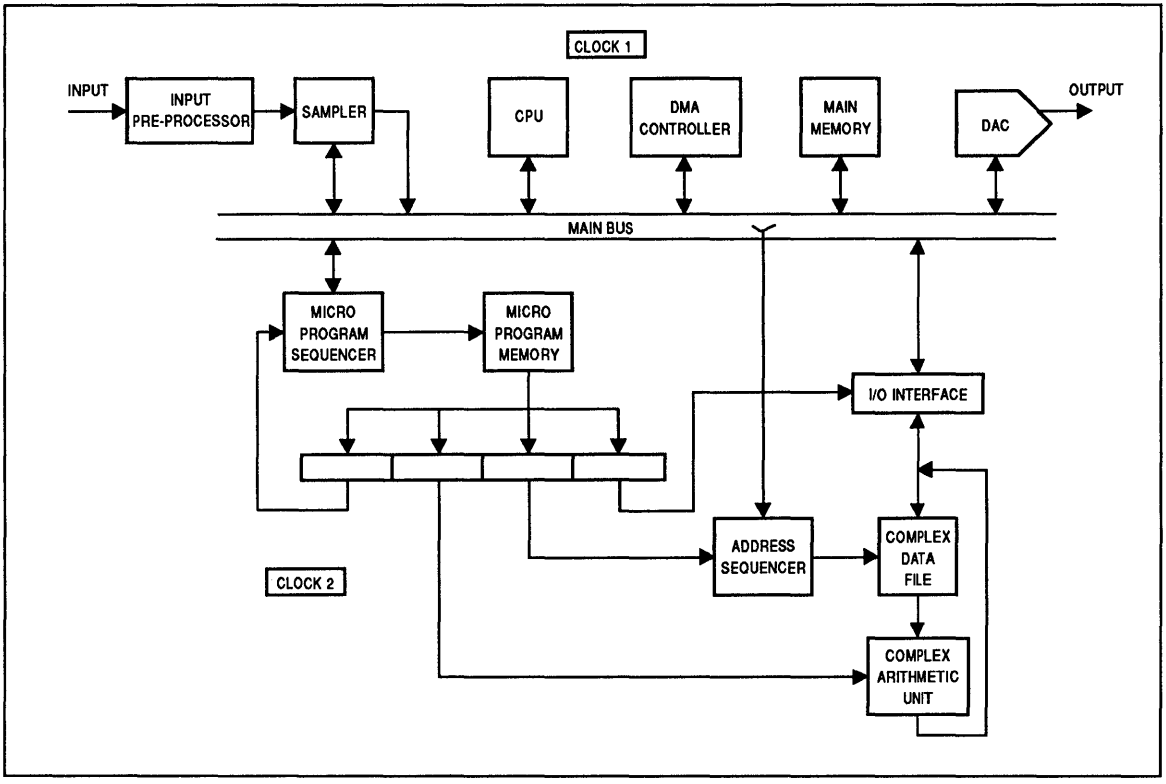
Building Block Approach

The "functional building block" architecture overcomes the limitations of the "single-chip" DSP units. This method allows the user flexibility in achieving the high-throughput requirement by minimizing the number of machine cycles per butterfly computation. The only penalty is the typical increase in the number of components used. However, this penalty is more than offset by the increased performance. An efficient functional building block architecture for high-speed DSP is shown in the block diagram of Fig. 2. The architecture achieves 2 machine cycles per butterfly, pipelined for 32-bit complex data FFT. The detailed implementation of the butterfly cell is shown in Fig. 3. The architecture is described as follows.

In the block diagram of Fig. 2, the butterfly cell is embedded in the system, under microprogram control, to handle the FFT computation. The overall architecture utilizes both a general purpose CPU, i.e., a Motorola 68000 or equivalent and functional building blocks to serve as the FFT coprocessor. The architecture allows for the execution of four phases to obtain the DFP. The four phases are: sampling, data formatting, computation, and outputting the DFP via the DAC.

The analog input signal is first fed into a pre-processor where it is band-limited via an anti-aliasing filter. The input signal can also be split into its

Figure 2. A representative system block diagram DSP



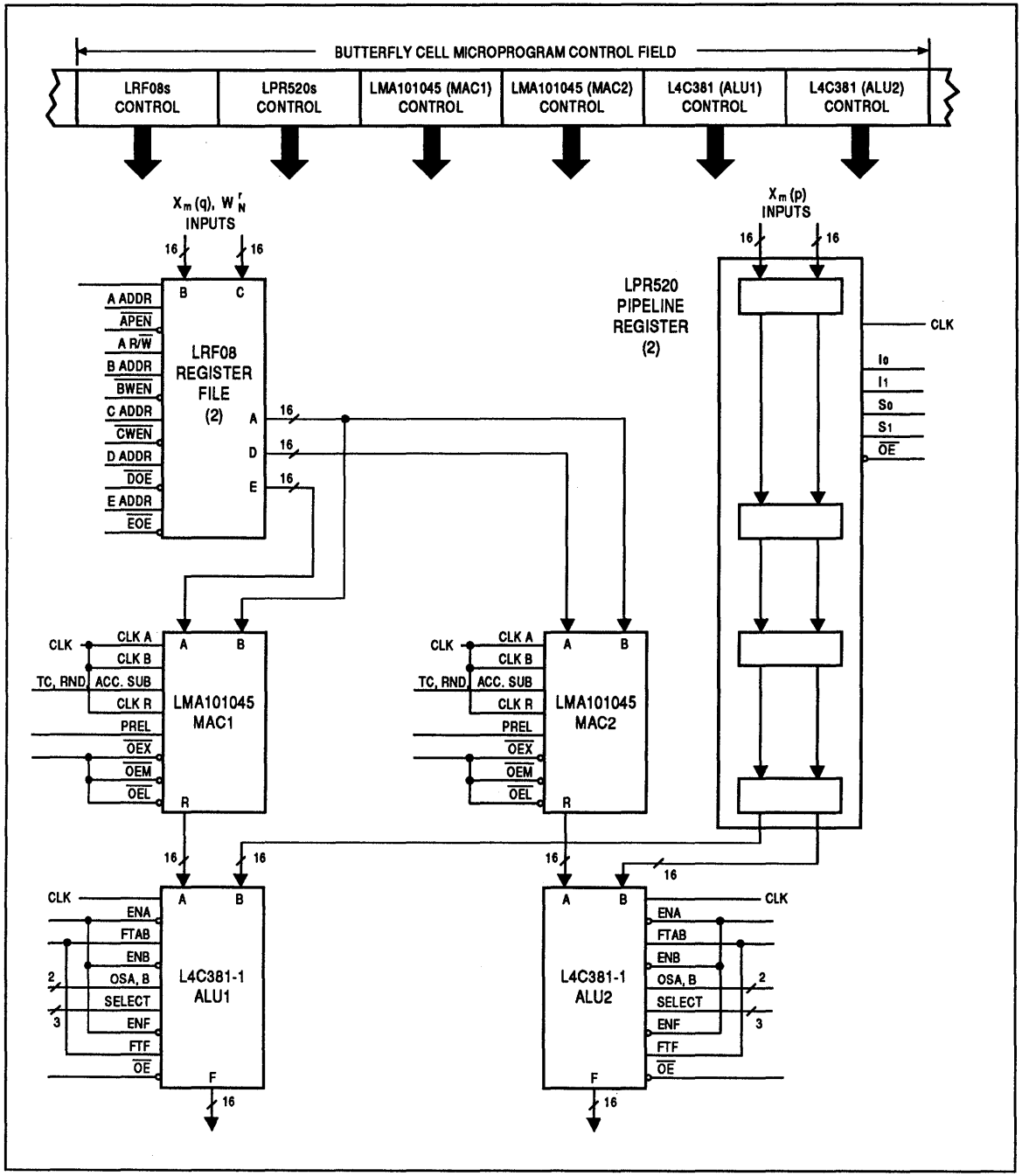
quadrature components at this stage or this may occur as a result of other operations such as heterodyning implemented digitally. The SAMPLER converts the analog signal into its equivalent digital data representation. The sampling process can be controlled either by the CPU or the DMA controller. Reference 2 shows that the controlling element also determines the maximum throughput rate of the sampling process; hence, the maximum input signal bandwidth. After sampling, or at the conclusion of other DSP processes, each of the real and imaginary data samples is assumed to be stored in contiguous memory locations in main memory. Therefore, real data can be stored in even address and imaginary data in odd addresses.

Data Formatting

Assume that in the 16-bit system of Fig. 1 the analog input signal is sampled 1024 times to represent one sample period. Furthermore, if all the samples are real numbers and storage is to begin at address 0000H, then the normal data storage sequence is such that the consecutive samples are stored in contiguous memory locations in main memory. This is particularly true in the case where the sampling process is treated as a data block transfer under CPU or DMA control. However, to be able to execute an in-place computation of the decimation-in-time FFT algorithm, the original data sequence obtained during the sampling phase must be restructured. This process involves address-bit reversal and is illustrated in Fig. 4.

An algorithm for generating the addresses in the bit-reverse order is discussed in Ref. 3. As pointed out, a highly flexible FFT Address Sequencer is sometimes required if the data buffer is not located at address 0000H, or if the FFT size is variable, due to the different sizes and fields of the address bits that need to undergo bit-reversal. Further complications are encountered when X(N) data is complex. As shown in Fig. 2, the 16-bit real and 16-bit imaginary data in main memory is to be mapped into a 32-bit field in the COMPLEX DATA RAM. A general purpose FFT Address Sequencer can be efficiently implemented with the combination of Logic

Figure 3. Detailed Butterfly Cell Implementation with the control field.



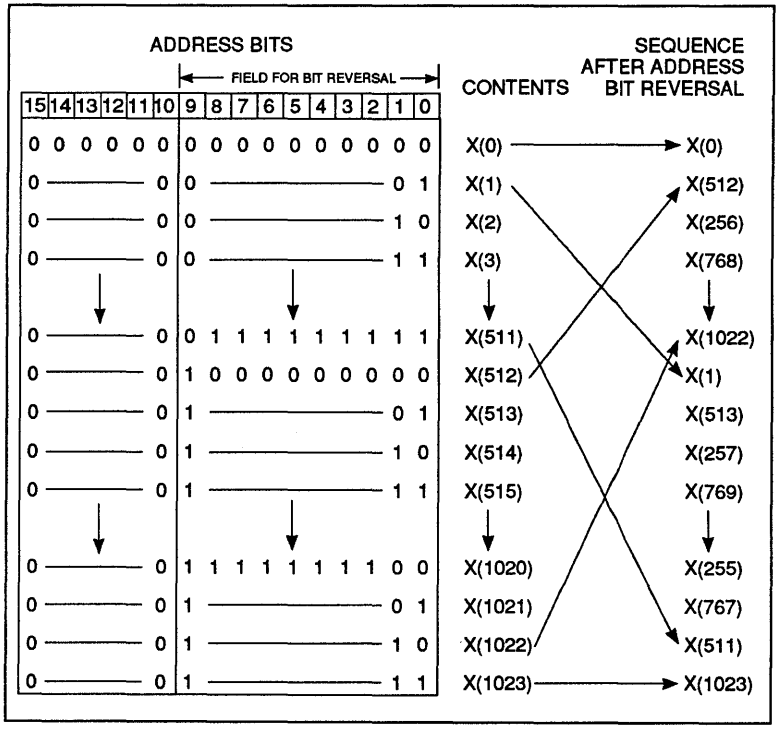
Devices' LRF08 multiport register file and L4C381 16-bit ALU. Because of their ability to be controlled by microcode, these two high-speed CMOS LSI devices provide the flexibility required of the FFT Address Sequencer. Also, the overhead time required to pre-sort the complex data sequence prior to the computation phase is reduced.

Handling the Computation

In Figure 1, the butterfly operands $X_m(p)$, $X_m(q)$, and W_N^r are all complex variables. The results of the computations $X_{m+1}(p)$ and $X_{m+1}(q)$ are also complex variables. W_N^r are known coefficients and stored in a read-only memory device as part of the COMPLEX DATA FILE in Fig. 2. The other part of the COMPLEX DATA FILE consist of the input data samples stored in COMPLEX DATA RAM in sorted order as defined by the bit-reversal process. The elements of the COMPLEX DATA FILE are 32 bits wide to accommodate the 16-bit real and 16-bit imaginary components.

The computation phase starts with the CPU generating a code for the MICROSEQUENCER. The MICROSEQUENCER interprets this code to access the first microinstruction in the MICROPROGRAM MEMORY and stores it in the MICROINSTRUCTION REGISTER. The microinstruction is horizontally organized so that different processing blocks can be controlled simultaneously; thus executing one microinstruction in one cycle of CLOCK2. The microinstruction field for controlling the butterfly cell is shown in Fig. 3 along with the detailed hardware implementation of the butterfly which consist of Logic Devices' LRF08 multiport register file (2), LPR520 pipeline register (2), LMA1010 16-bit multiplier/accumulator (2) and L4C381 16-bit ALU (2). The operands $X_m(q)$ and W_N^r are to be held in the register file temporarily while the $X_m(p)$ is passed down the pipeline register. The computations are done in a pipelined fashion and facilitated by the internal pipeline registers of the LMA1010s and L4C381s. The results of the computations can then be stored back into the COMPLEX DATA RAM to be used in the next iteration. This is really the essence of the in-place computation of the decimation-in-time FFT algorithm. The status of the components comprising the butterfly cell is outlined in the state matrix of Fig. 5.

Figure 4. Normal data sequence during sampling phase and result of re-structuring via address bit reversal. The new data sequence is stored in the complex data RAM.



Digging into the Microcode

During state SO, the Address for storing one of the first set of operands, $X_m(q)$ is loaded into the B and C Address Port register of the LRF08s. Since $X_m(q)$ is composed of 16-bit real, $Re[X_m(q)]$, and 16-bit imaginary data, $Im[X_m(q)]$, the LRF08s' registers are set up such that $Re[X_m(q)]$ will be stored in register R0 and $Im[X_m(q)]$ in R1. This is easily done by setting up the microcode to take advantage of the simultaneous register access capability of the LRF08. In this case, the address bits are $B_2B_1B_0 = 000$ and $C_2C_1C_0 = 001$ respectively. During S1, $X_m(q)$ is written into the LRF08s via the B and C input ports and at the same time the address for storing the real and imaginary part of W_N^r, $Re[W_N^r]$ and $Im[W_N^r]$ respectively, are also written into the B and C Address Port registers. This time the address bits are $B_2B_1B_0 = 010$ and $C_2C_1C_0 = 011$. This will allow storage of $Re[W_N^r]$

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Figure 5. Butterfly computation state matrix.

DEVICE	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
LRF08 REGISTER FILE	LOAD $X_m(q_0)$. WRITE ADR.	WRITE $X_m(q_0)$. LOAD $[W_N^r]_0$ WRITE ADR.	WRITE $[W_N^r]_0$. READ $Im[X_m(q_0)]$ & $[W_N^r]_0$. LOAD $X_m(q_1)$ WRITE ADR.	WRITE $X_m(q_1)$ LOAD $[W_N^r]_1$ WRITE ADR. READ $[W_N^r]_0$	WRITE $[W_N^r]_1$. READ $Im[X_m(q_1)]$ & $[W_N^r]_1$ LOAD $X_m(q_2)$ WRITE ADR.	S3	S4	S3	S4	S3	S4
LRP520 PIPELINE REGISTER			$X_m(p_0) \rightarrow R1$	$X_m(p_0) \rightarrow R2$ $X_m(p_1) \rightarrow R1$	$X_m(p_0) \rightarrow R3$ $X_m(p_1) \rightarrow R2$ $X_m(p_2) \rightarrow R1$	$X_m(p_0) \rightarrow R4$ $X_m(p_1) \rightarrow R3$ $X_m(p_2) \rightarrow R2$	HOLD	$X_m(p_1) \rightarrow R4$ $X_m(p_2) \rightarrow R3$	HOLD	$X_m(p_2) \rightarrow R4$	HOLD
LMA1010 MAC1			$Im[W_N^r]_0$ &	LOAD $Im[W_N^r] = D$ $Im[X_m(q_0)]$	$Im[X_m(q_0)] \times Re[W_N^r]_0 -$ LOAD $Re[W_N^r]_0$ & $Re[X_m(q_0)]$	$\{Re[X_m(q_0)] \times Re[X']$. $D = Re[X']$. S3 LOAD.	OUTPUT EVALUATE "NEW" D.	S5	S6	S5	S6
LMA1010 MAC2			$Re[W_N^r]_0$ &	LOAD $Re[W_N^r] = B$ $Im[X_m(q_0)]$	$Im[X_m(q_0)] \times Im[W_N^r]_0 +$ LOAD $Im[W_N^r]_0$ & $Re[X_m(q_0)]$	$\{Re[X_m(q_0)] \times Im[X']$. $B = Im[X']$. S3 LOAD.	OUTPUT EVALUATE "NEW" B.	S5	S6	S5	S6
L4C381 ALU 1							$Re[X_m(p_0)] - Re[X'] = Re[X_{m+1}(q_0)]$	$Re[X_m(p_0)] - Re[X'] = Re[X_{m+1}(p_0)]$	S6	S7	S6
L4C381 ALU 2							$Im[X_m(p_0)] - Im[X'] = Im[X_{m+1}(q_0)]$	$Im[X_m(p_0)] - Im[X'] = Im[X_{m+1}(p_0)]$	S6	S7	S6
								$X_{m+1}(q_0)$	$X_{m+1}(p_0)$	$X_{m+1}(q_1)$	$X_{m+1}(q_1)$

into register R2 and $Im[W_N^r]$ into R3 of the LRF08s. During S2, W_N is written via the B and C input ports and simultaneously read out via the D and E output ports. The imaginary part of $X_m(q)$ is also read out of the bi-directional A-port. In addition, the address for storing a "new" $X_m(q)$ is written into the B and C Address Port registers. $X_m(p)$ is also loaded into the LPR520 pipeline register. Note that during this state two sets of complex operands, W_N^r and $X_m(p)$, are simultaneously accessed from the COMPLEX DATA FILE. During this state all the complex data operands for the first FFT butterfly computation are available in the working registers. For a 1024-point FFT, the first set of operands correspond to

$X_m(p) = X(0)$, the first sample

$X_m(q) = X(512)$, the 513th sample

$W_N^r = W_N^o = 1$

The operands $Im[W_N^r]$, $Re[W_N^r]$ and $Im[W_N^r]$ are latched into the LMA1010s input registers during S3. From Fig. 1(c), note that the $Im[X_m(q)]$ term is common to the expressions for B and D. Therefore, B and D can be simultaneously evaluated during S4 and the result stored in the corresponding LMA1010's accumulator. During S6, ALU1 and ALU2 control bits are set so that both L4C381s will act as subtractors. The contents of the MAC1 and MAC2 output registers are shifted into the input registers of the L4C381s. The other operands are the real and imaginary components of $X_m(p)$, $Re[X_m(p)]$ and $Im[X_m(p)]$ respectively, which has been shifted down the LPR520 pipeline registers during states S2, S3, S4 and S5. Referring to Figs. 1(c), 4, and 5, the real component of $X_{m+1}(q)$ is evaluated by ALU1 while the imaginary component is evaluated in ALU2. A new set of D and B values are also evaluated. The new D and B values correspond to the new set of $X_m(q)$ and W_N^r operands loaded into the MAC1 and MAC2 input registers

during S5. The real and imaginary components of $X_{m+1}(p)$ are evaluated in ALU1 and ALU2 respectively during S7. By holding the contents of the LPR520s, all the operands needed to obtain $X_{m+1}(q)$ during S6 are also available to obtain $X_{m+1}(p)$ during S7. The in-place computation is realized by storing $X_{m+1}(q)$, during S7, into the location in COMPLEX DATA FILE occupied by $X_m(q)$. In the same manner, $X_{m+1}(p)$ is loaded into $X_m(p)$ during S8.

From the state matrix of Fig. 5, note that a steady state condition occurs after, the state S6 such that a butterfly computation is completed every two cycles after an initial overhead of only 6 cycles. The efficient handling of the computation is largely aided by the flexibility of the LRF08 multiport register file. A good example is illustrated during state S3 when the real and imaginary components of a new $X_m(q)$ are written into register R4 and R5 via the B and C data input ports and at the same time "previous" $Re[X_m(q)]$, $RE[W_N^r]$ and $Im[W_N^r]$ are read out of register R0, R1 and R3 via the output ports A, D and E respectively.

Dealing with Overflow, Underflow and Precision

Overflow can occur at the front end when the input signal exceeds the full-scale range of the ADC. Depending upon the application, this can be prevented by using an automatic gain control (AGC) stage within the INPUT SIGNAL PROCESSOR or a hard limiting circuit to limit the maximum excursion of ADC. Another overflow condition involves exceeding the dynamic range of the fractional number representation. If the operands $X_m(p)$, $X_m(q)$ and W_N^r are fractions in fractional 2's-complement form, then the product of any of two operands is always a fraction. However, the FFT also involves accumulation of the product terms and the addition of two large positive fractions could result in an integer and a fraction. In this case the highest fractional number represented is exceeded and an overflow condition occurs.

From Fig. 3, the output of the LMA1010s are rounded to a 16-bit, single precision value and applied to the ALUs. However, the internal accumulation/subtraction process uses the full 35-bit double precision value. Overflow occurs when the MAC1/MAC2 operands are both –1.0, i.e., 8000H, and the product is added to an accumulator containing +1.0. One way of handling this is to provide a fixed divide-by-two scale factor by using the R31–R16 output bits of the MACs. Since the bits have the significance of 2^1 to 2^{-14}, the dynamic range is reduced by 1 bit, which might be unacceptable in certain applications. Another method is to limit the most negative number representation of the coefficient, W_N^r, to be –1.0 + 1 LSB (8001H). This guarantees the result of the multiplication/accumulation to be less than 2.0. In this case, the MACs R30–R15 output bits having the significance 2^0 to 2^{-15} are used and the dy-namic range is improved by 1 bit. Another potential source of overflow is at the ALU1 and ALU2 when the MACs outputs are added with the operands at the output of the LPR520s.

The modified butterfly cell, shown in Fig. 6, implements block-floating-point arithmetic to handle the potential overflows by means of the LSH32 32-bit Barrel Shifter/Normalizer. In this configuration, for a given stage of the FFT the ALU's outputs are fed into the SHIFT ENCODER LOGIC block. If either one or both the ALU's output is greater than 0.5, a shift code corresponding to the maximum output of either ALU is generated and latched. This is done because if either ALU's outputs is equal to or greater than 0.5 for the current FFT stage, then an overflow could occur during the next stage. To avoid this possibility, the shift code that is latched during the current stage is fed into the S14–S0 inputs of the LSH32s. Then during the next stage all the input operands are uniformly scaled down by shifting right.

Underflow can occur when two large negative fractions produce a result less than the most negative fractional number that can be represented by the system. The hardware that handles the overflow condition at the $X_{m+1}(p)$ output can be replicated and used to handle the underflow condition at the $X_{m+1}(q)$ output.

The addition of the LSH32 for input scaling certainly adds flexibility to the system at the expense of additional hardware. However, it may not be needed in applications where it is known that overflow or underflow cannot possibly occur. In this situation, only the sign bit (R31) and the 15 most significant fractional parts (R30–R16) at the LMA1010s outputs are applied to the input of the L4C381s. Regardless of the presence or absence of the LSH32s, the conversion to single precision result is obtained by rounding up the accumulator contents of the LMA1010s. Rounding up is done automatically by asserting the RND control bit of the LMA1010s. The performance rating of the Logic Devices' "functional building block" architecture is shown in Fig. 7 along with the single-chip DSP units. Note that although the instruction cycle time is approximately the same, the Logic Devices' architecture is close to an order of magnitude faster. It is also important to note that the 100 ns cycle time of the Logic Devices' architecture using high-speed CMOS components is comparable to architectures implemented with bipolar components with an added advantage of much lower power dissipation.

Figure 6. Modified Butterfly Cell Implements block-floating-point arithmetic to handle potential

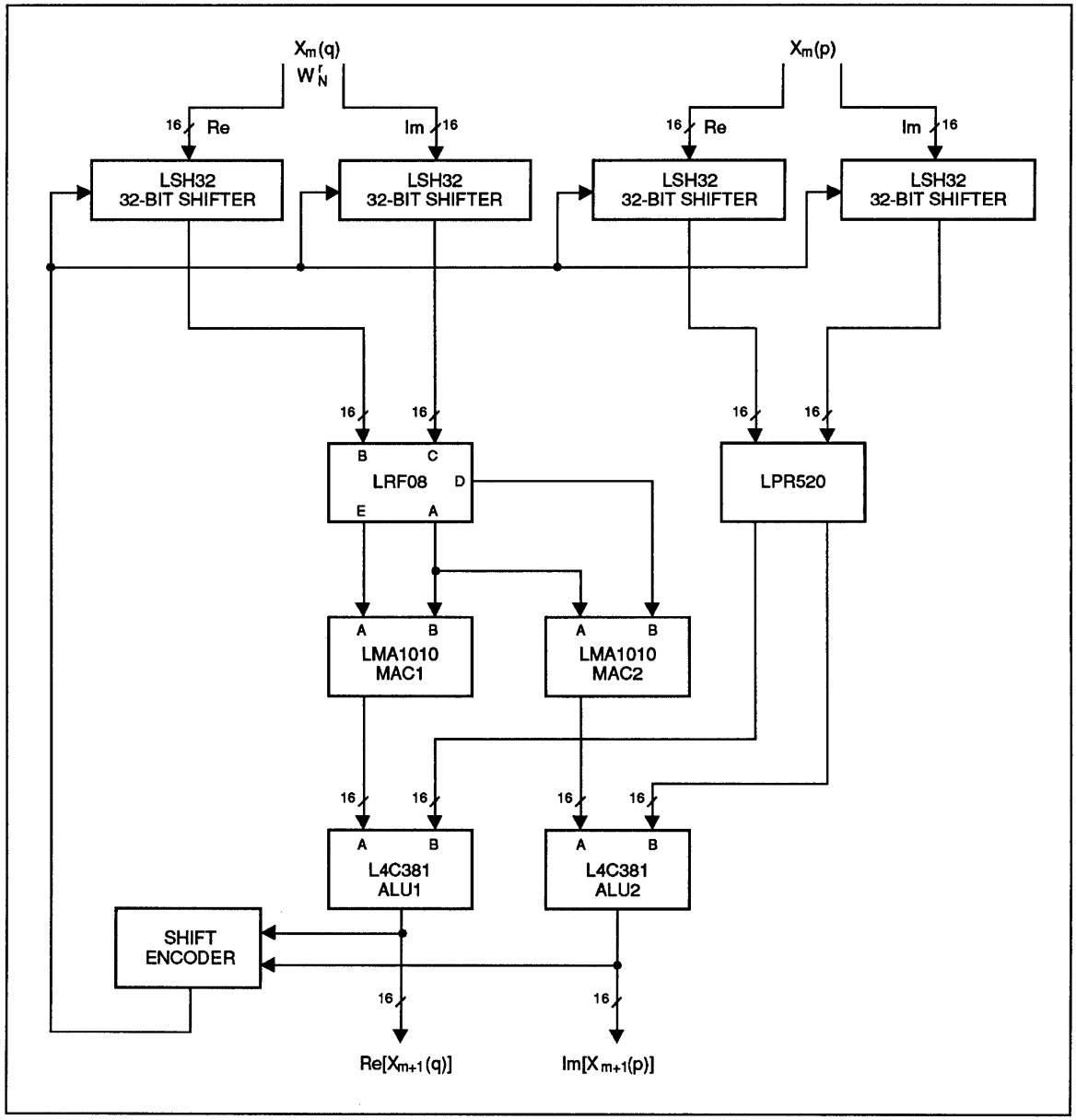

Figure 7. Performance ratings for different DSP units based on execution time of 1024-point, complex FFT.

DSP UNIT	MEMORY (1)	INSTRUCTION CYCLE TIME	1024-POINT COMPLEX FFT	SAMPLING RATE (MAX)
TMS32010 (TI)	144 x 16 -D -RAM 1536 x 16 -P -ROM	200 ns	75.9 ms (2)	13.1 kHz
µPD77230 (NEC)	2-512 x 32 -D -RAM 1K x 32 -D -ROM 1K x 32 -P -ROM	150 ns	10.75 ms (3)	100 kHz
LM32900 (NNational)	EXTERNAL	100 ns	13.42 ms (3)	78 kHz
ADSP2100 (Analog Dev.)	EXTERNAL	125 ns	7.2 ms (3)	142 kHz
LOGIC DEVICES (Fig. 3) BUILDING BLOCKS	EXTERNAL	50 ns	0.5 ms	2 MHz

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Contents

"Minimize Parasitic Problems in High-Speed Dgital Systems" 11-3

Design Feature

Reprinted from EDN, March 29, 1990

Minimize parasitic problems in high-speed digital systems

Parasitics are usually small enough to have little effect on performance. However, the organizational, access-time, and coordinated-switching requirements of today's high-speed digital systems make ideal breeding grounds for these undesirable signals. Therefore, you must now account for those parasitics you could previously ignore.

James K Murashige, *Logic Devices Inc*

Parasitic problems, which are rarely overtly obvious, musn't be neglected in your system's design process. If they are, your system may be plagued with bugs, glitches, gremlins, and intermittent failures.

When digital designers encounter system problems, they frequently place the blame on the circuit ICs. However, IC manufacturers go to great lengths to characterize and test their devices. In most cases, it is not the ICs that are the main cause of parasitic problems. Rather, it is the pc-board interconnects between circuit components that prove problematic. Compounding the problem further is the fact that today's faster ICs are very susceptible to noise.

Parasitic problems due to pc-board-interconnect wiring are difficult to diagnose and cure because the parasitics are speed, layout, and material sensitive. It's possible to have thousands of interactions on a typical circuit board, and under certain conditions these interactions can combine to exceed digital noise margins and cause false triggering. Unchecked parasitics can also increase your circuit's power consumption, cause data loss, and cause devices to fail. By modeling the mechanics of parasitic operation early in the system-design phase, you can effectively anticipate and suppress problems.

In essence, electronic design involves the use of components to control, convert, and manipulate voltage and current to develop a useful function. Designers must therefore characterize electronic components in terms of how they interact with and relate to voltage and current. The defining relationships are resistance, capacitance, and inductance.

In the real world, no component is a pure resistance, capacitance, or inductance—all devices exhibit a mixture of R, C, and L. One of these components usually predominates; the others are considered parasitics. Wiring, whether discrete or printed, also contains R, C, and L components.

Resistance is the least troublesome parasitic because it has no dependence on speed. Even if the C and L quantities are quite small, parasitic capacitance and inductance cause a great many problems because they define a differential relationship between voltage and current.

The parasitic values of R, L, and C in circuit-board

In the real world, no component is a pure resistance, capacitance, or inductance—all devices exhibit a mixture of R, C, and L.

wiring are interrelated. A study of the makeup of resistive, capacitive, and inductive parasitics (**Fig 1**) makes it much easier to minimize their effects.

Copper-clad, glass-epoxy boards are typically used to achieve the desired high conductivity/low resistance qualities so important to wiring. Copper-foil thickness is customarily specified as the number of ounces of pure copper per square foot of board area. Each ounce contributes 0.00135 in. of thickness to the cladding. Parasitic resistance has a low value—a 10-mil-wide trace on a 2-oz copper-clad board has a resistivity of only 2.27 mΩ/linear in. Also, because resistivity is inversely proportional to the cross-sectional trace area, increasing cladding thickness or widening the trace proportionally lowers resistivity.

Parasitic capacitance arises because a circuit trace is one plate of a pc-board capacitor. Adjacent circuit traces, or inner layers of a multilayer board, are the other plates. The dielectric material for this parasitic capacitor is air and/or the board material itself. Dielectric constants vary for different board materials (it's about 5 for commonly used G10 epoxy boards). You can calculate board capacitance using the expression

$$C = KA/d,$$

where K equals dielectric constant, A equals the plate's surface area, and d equals the distance between the plates. Obviously, capacitance will be greatest over a large plate area with minimal plate separation. For example, a 10-mil-wide trace has a parasitic capacitance of 1.2 pF/linear in. of trace; the capacitance will double for a 20-mil-wide trace.

The self-induced magnetic field generated around a circuit trace carrying a current produces the parasitic inductance. Parasitic inductance is dependent on the length, width, and thickness of the trace as given by the expression

$$l = \text{length}/(\text{width} + \text{thickness}).$$

A 10-mil-wide trace will have an inductance of approximately 17.5 nH/in. Note that the above expression indicates that inductance will decrease as you increase either trace width or cladding thickness.

The simplified case of using a 10-mil-wide trace gives you some working values for R, C, and L, and also determines the qualitative effects of varying trace geometry. Though these parasitics have low values, they can become significant when you're working with high-speed signals. Digital-system designers should pay particular attention to the areas of power distribution and signal transmission.

Proper power distribution is critical

To operate at high speeds, ICs must, when switching, supply high levels of drive current on their outputs. Internal IC circuitry will draw more power when activated for full-speed operation. It is relatively simple to design a board's power-distribution system so that it satisfies steady-state conditions. However, parasitics in the system can cause momentary current limitations and supply-voltage drops. These transient conditions can show up in the signal outputs or couple through the power-distribution system to adjacent devices in the circuit.

To illustrate parasitic problems, consider the task of supplying power to an L7C185 8k × 8-bit static RAM (**Fig 2a**). Here, the L7C185 sits 6 in. away from an ideal 5V supply. V_{CC} is routed to the RAM along a

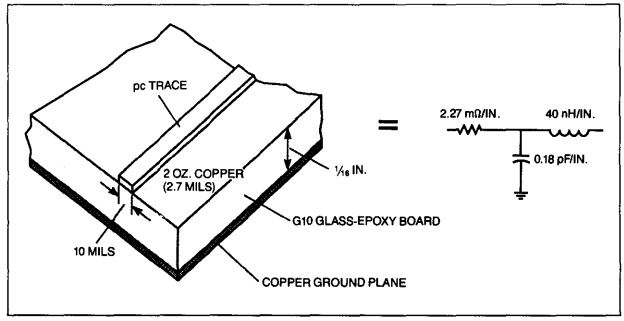

***Fig 1—You can minimize parasitic problems** by thinking of the pc board as a component. As the electrical-equivalent circuit illustrates, traces are really comprised of a combination of resistance, capacitance, and inductance.*

6-in.-long, 10-mil-wide trace, while a second 10-mil-wide, 6-in.-long trace provides the ground return. Each trace will have a parasitic resistance of $6 \times 27\ m\Omega = 162\ m\Omega$ and an inductance of $6 \times 17.5\ nH = 105\ nH$. The L7C185 draws a quiescent current of 20 mA; for full-speed operation, it requires 160 mA.

Because a 160-mA current will introduce only a 26-mV drop in both the V_{CC} line and the ground return, the RAM's parasitic resistance will be negligible. The RAM's V_{CC} value will be 4.948V. However, parasitic trace inductance can cause problems because, as its defining equation $V = Ldi/dt$ illustrates, rapidly changing current through an inductor produces significant voltage drops. For example, a 20-nsec read operation from the L7C185 will generate an inductive voltage drop of $105\ nH \times 140\ mA/20\ nsec = 0.735V$ across both traces, leaving only $5 - 1.47 = 3.53V$ at the RAM's supply pin. Such a low value can lead to signal transients or cause data loss until V_{CC} can stabilize.

A more serious condition exists when the RAM powers back down and tries to stop the current flow. The sudden decrease in current generates a large negative voltage spike across the trace-inductive reactances relative to the power supply. For a 20-nsec off time, the chip's instantaneous voltage will be $5 + 1.47 = 6.47V$. The result is the creation of signal transients that may overstress and damage the IC.

Good layout can make a difference

There are several solutions to the problem of parasitic inductance in power distribution, the most obvious being to widen the power traces. Widening power traces from 10 to 100 mils decreases inductance to 13.1 nH/in. In fact, the most effective board layouts employ multilayer boards, which have separate power and ground planes. In addition to providing the lowest possible inductance, this separate plane approach also simplifies the design of the power-distribution system.

The best solution to trace-inductance problems uses bypass capacitors to provide localized power sources for each IC. By physically locating decoupling capacitors next to each IC, you shorten the I_{CC} current loop to the physical length of the traces between capacitor and IC (**Fig 2b**). You can reduce trace length even more by using modern under-the-chip capacitors, which attach directly to the IC power pins—virtually reducing the trace length to zero (**Fig 2c**).

Before you can calculate minimum capacitor values, you must first establish an acceptable variation in the chip's supply voltage and then apply the defining equations for capacitance. Most modern ICs are specified to operate with a $5V \pm 10\%\ V_{CC}$. While a 0.5V variation may be acceptable if you're considering only one IC, it may be too high when you consider the contributive effects of neighboring ICs switching at the same time. In memory systems, for example, simultaneous access to banks of eight or 16 devices is quite common. In this case, it is wise to hold the supply variation to 0.05V. Using the previous full-speed-operation figures of 140 mA and 20 nsec for current and switching time, respectively, the calculations yield a capacitance value of 0.056 μF.

By shortening the inductive trace length, decoupling

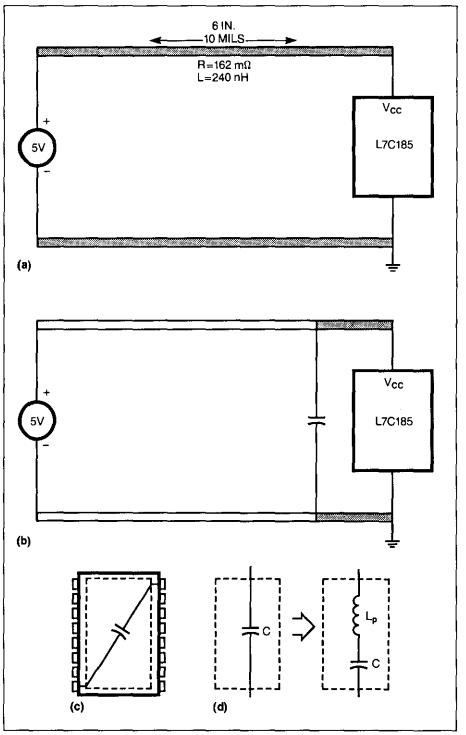

***Fig 2—Proper decoupling techniques** can significantly reduce parasitic problems. The design goal here is to minimize the effects of parasitic inductance by keeping the I_{CC} current loop as short as possible.*

Digital-system designers should pay particular attention to power distribution and signal transmission.

capacitors also minimize overstress voltage by absorbing any inductive voltage spikes. In essence, you can think of decoupling capacitors as temporary current storage devices that help to smooth peak IC current demands.

Designers typically employ standard-value 0.1-μF capacitors for decoupling service. So why not use larger capacitors to reduce supply-voltage variations even further? There are a number of reasons, all of which are related to capacitor characteristics. The first has to do with size considerations—it's simply more difficult to physically place large capacitors close to ICs. Second, construction limitations increase the parasitic inductance in large capacitors. Large-value capacitors can have the equivalent inductance of several inches of circuit-board trace and negate the advantage gained by using larger capacitance values.

Finally, there's the problem of EMI. For maximum EMI suppression the decoupling capacitor must reach resonance in the frequency range of interest—typically 30 to 50 MHz. Again, larger-valued capacitors have intrinsically larger inductance values. Viewed from the standpoint of resonance, this larger inductance value lowers both the capacitor's resonant frequency and its EMI suppression effectiveness. Thus, smaller-valued capacitors with higher resonant frequencies suppress EMI much better. (Ceramic-type capacitors generally exhibit the best high-frequency characteristics for EMI suppression.)

The same interconnect parasitics that cause problems in power distribution also plague signal transmission, which is not surprising because power distribution and signal transmission are functional complements of each other. In power distribution, the signal source (power supply) remains constant while the load changes; in signal transmission, the signal source changes while the load stays the same.

The previous analysis of power-distribution parasitics used an empirical approach (a lumped parasitic circuit model) to solve the problem. The approach yielded good results and also simplified the explanation of the underlying principles involved. In signal transmission, however, the principal parasitic effects stem from the even distribution of parasitics along a line. Therefore, you must use a different approach to analyze the problem. Though this new approach involves a more involved circuit model, the analysis is applicable to power-distribution problems.

Because parasitic resistance is constant over frequency, it is generally not problematic. Parasitic capacitance and inductance, on the other hand, greatly affect signal transmission because of the time-derivative relationships they define between voltage and current.

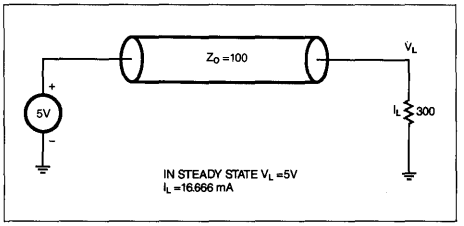

***Fig 3—You must match a line's characteristic impedance** at all interfaces if you want to minimize ringing, undershooting, or overshooting problems.*

One bad effect is delay. As a signal propagates down a trace it has to charge the distributed capacitors and inductors along the way, thereby introducing delay. System designers often neglect circuit-trace propagation delay when calculating worst-case delay paths. Instead, they focus on the source and driver specifications of the circuit's ICs. Unfortunately, trace-propagation delay can become a significant factor in high-speed systems that require large loads or critical timing requirements.

Assuming you have an ideal signal source, the propagation delay T_{PD} through a line will be equal to $\sqrt{LC}$. Returning to the 10-mil-wide trace example in **Fig 2A**, the delay per unit length calculates out to $T_{PD} = \sqrt{17.5\ nH \times 1.2\ pF} = 0.145$ nsec/in. The trace delay itself is small, but when it's combined with even moderate loading values it can create large signal delays.

When you're working with MOS circuitry, for example, loading is principally capacitive. You can evaluate the effect of this loading by applying the formula for T_{PD} to a calculated bulk value of C and L. Doing so, you obtain $T_{PD} = \sqrt{L(C_T + C_l)} = \sqrt{(LC_T) + (LC_l)}$, where C_T equals total trace capacitance and C_l is the total capacitive load value. C_T is usually much smaller than C_l, so T_{PD} will be predominantly caused by the parasitic trace inductance combined with load capacitance—the LC_l factor.

To illustrate delay problems, consider the design of a memory array utilizing a single source to drive eight L7C185 SRAMs (static RAMs) and in which similar signals (such as addresses) are daisy chained from one chip to the next. Each L7C185 presents a 5-pF load

on each input. With eight SRAMs in parallel, the total load capacitance equals 40 pF. If the circuit board is laid out well, the SRAMs will be located close to each other to keep trace lengths to a minimum.

Assuming that you can use a 6-in. length of 10-mil trace to connect all the RAMs, the trace contributes a capacitance value of 7.2 pF and an inductance of 105 nH to the delay calculation. Total T_{PD} then becomes $\sqrt{105 \times 7.2 + 40} = 2.23$ nsec. The example illustrates that trace inductance and IC load capacitance are indeed the major contributors to signal delay, with trace capacitance making only a minor contribution. It's obvious that, as with power distribution, propagation delay occurs because trace inductance retards the instantaneous flow of current. Therefore, the best way to minimize propagation delay is to minimize trace inductance by maximizing trace crosssectional area—by widening trace widths or paralleling trace runs.

Bring characteristic impedance into play

Because of the time-derivative properties of the distributed capacitance and inductance along the trace, voltage and current propagating down the trace maintain a fixed-phase relationship to each other. Given this fixed-phase relationship, you can use characteristic impedance, expressed by the relation $\sqrt{L/C}$, to model traces for signal-transmission analysis.

A second, more serious consequence of parasitic capacitance and inductance is the introduction of signal transients. These transients arise because of the reluctance of the distributed capacitance and inductance to allow instantaneous changes in voltage and current along the trace.

Signal transients—in the form of undershoot, overshoot, and ringing—can occur unless you match the characteristic impedance of a trace at its interfaces. Reflected voltage and current wavefronts generated to satisfy boundary conditions generate these transients, which can cause false switching, increase power dissipation, and generate EMI.

To illustrate the problem, consider the case of a 5V signal propagating down a 100Ω line terminated with a 300Ω load (**Fig 3**). Initially, a 50-mA current front (5V/100Ω) follows the voltage front as it propagates down the line. When the fronts reach the 300Ω load, a discontinuity develops—a 50-mA current is flowing through the line, but 5V into 300Ω equals only 16.7 mA. To satisfy this boundary condition, fronts of 2.5V and −25 mA reflect back down the line toward the signal source. The load voltage is now 5+2.5=7.5V

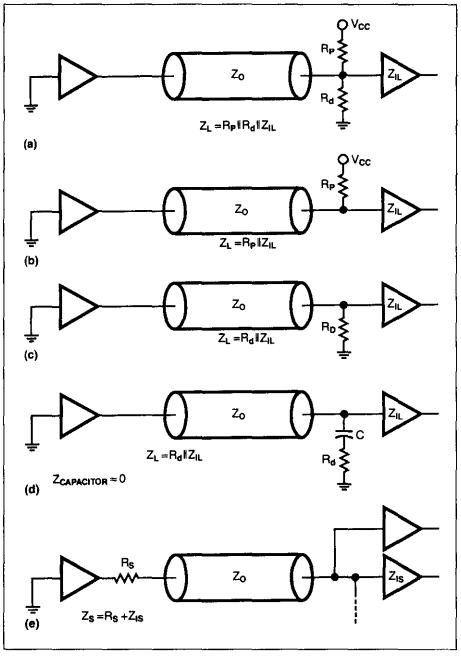

***Fig 4—There are many impedance-matching techniques** available to solve transient problems. Though load-matching schemes **(a), (b), (c), (d)** are usually the preferred choice, you must turn to a source-matching scheme **(e)** when you're dealing with multiple loads.*

and current is 50−25 mA—values which satisfy the boundary conditions.

Back at the source, the reflected voltage and current fronts must again satisfy boundary conditions. Doing so may lead to more reflected waves. In time, the oscillations decay, and the line will achieve a steady-state condition of 5V throughout its entire length with a current flow of 16.6666 mA. A matching load of 100Ω would have satisfied boundary conditions and created no reflected waves.

Line reflections occur anytime signals are transmitted along unmatched lines. However, they only cause problems when they fail to coincide with the edge of the driven signal, a condition which arises when the signal rise time is faster than the period over which the reflections dampen out. To simplify reflection-mag-

The most effective solution to trace-inductance problems uses bypass capacitors to provide localized power sources for each IC.

nitude calculations, it's useful to define a reflection coefficient p where $V_{r(reflected)} = pV_{i(incident)}$. In general, you can derive p by satisfying boundary conditions as follows.

The voltage and current initially flowing through the line are V_i and V_i/R_o. At the boundary, the termination impedance, R_t, equals V_t/I_t. After reflection occurs, $V_t/I_t = R_t$. Given this relationship, you can calculate the reflection coefficient as

$$(R_t - R_o)/(R_o + R_t).$$

An examination of p yields several bits of information. If R_t is greater than R_o, positive voltage reflections will occur. Negative voltage relections occur when the opposite is true. For an open-circuited line, R_t dominates and $p = +1$. In this case, $V_r = V_i$ and the termination interface will generate a reflection of $2V_i$. High-impedance terminations such as this can possibly create overvoltage conditions and increase power consumption because of the higher voltage levels they generate. Sufficient overvoltage levels can damage the input of ICs or induce latchup in a CMOS device. With a short-circuited line, R_o dominates and $p = -1$. Therefore, $V_r = -V_i$, which negates V_i. Negative voltage reflections can cause false switching action when you're dealing with multiple signal edges.

When line and load impedances are matched, there are no transmission problems. Voltage reflections ping-pong along the line, attenuating themselves by p each time they reach the source or load. The reflections eventually decay to zero and the line achieves steady-state conditions. The decay time of the voltage reflections depends entirely on the reflection coefficients p at either end of the line and the amount of propagation delay down the line.

Choosing a suppression technique

You can suppress transmission-line transients by matching impedances at either the source or the load. Load matching is the best option because it allows you to minimize source impedance, which enhances drive capability and improves signal rise time and dc drive capability. Typically, the load will be the high-impedance input of a MOS IC, which means you'll have to lower load impedance to match the line impedance.

There are several ways to lower load impedance. One utilizes an active termination employing a pull-up/pull-down resistor network (**Fig 4a**). The effective load impedance equals the parallel combination of R_P, R_D, and the output impedance of the IC. In addition to matching impedances, this technique also establishes an active termination voltage, which can be used to help a weak source driver with rise-time and fall-time performance. The matching technique does have one drawback, however: there's a dc current constantly being dissipated through the termination resistors.

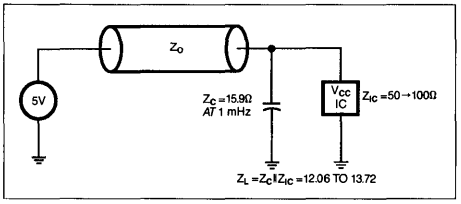

***Fig 5—Transient problems in power-distribution systems** are significantly reduced when you use decoupling capacitors to minimize load-impedance variations.*

A second load-matching approach uses just a pull-up (**Fig 4b**), or pull-down resistor (**Fig 4c**). Either of these schemes solves the dissipation problem, but weaker source drivers will have problems with the additional load imposition, especially if multiple load paths are involved.

You can avoid all dc loading problems by using an ac-coupled load-termination scheme (**Fig 4d**). During the switching phase, the capacitor is virtually transparent, and the pull-down-resistor impedance combines in parallel with the load impedance to match the line impedance. Under steady-state conditions, the capacitor blocks any current flow and removes the resistive load from the circuit. You choose the capacitor value to achieve a minimum impedance at the voltage-reflection frequency $V_{VR} = 1/2T_{PD}$.

To this point we've considered only a single impedance discontinuity at the load. In a typical system, however, discontinuities may occur anywhere there is a physical change in the transmission path. Such changes occur when you split a trace to drive multiple IC inputs, widen or narrow a trace, or pass through a connector.

With several discontinuities in each line or with multiple load locations, it may become impractical to match all load impedances. If so, you must opt for source-impedance matching. Typically, the signal source employs a low-impedance driver, so you must raise the network's source impedance to match that of the line. To raise the source-output impedance you simply add

a series resistor at the driver output (**Fig 4e**).

Again, power distribution and signal transmission are complements of each other. You can see the relationship by applying the impedance-analysis techniques to power distribution (**Fig 5**). As the figure shows, the power-supply voltage remains constant while the impedance of the load varies. Voltage reflections and fluctuations occur during the transition between steady-state conditions. In order to minimize transients, therefore, you must minimize the factors that cause fluctuations from a steady-state condition.

Load impedance is the variable factor in power distribution, so your goal is to minimize load variations. Adding decoupling capacitors minimizes impedance variations because the capacitors become the dominant factor in the load-impedance equation. For example, assume that an IC being powered by the 5V power supply varies its current consumption from 50 to 100 mA. Correspondingly, the IC's output impedance varies from 100 to 50Ω—a 100% variation. At 1 MHz, a 0.01-μF decoupling capacitor has an impedance of 15.9Ω. When you consider the parallel combination of capacitive and IC impedances, the load will now vary from 12.06 to 13.72Ω—a 13.8% variation—which will lead to significant reductions in voltage transients.

EDN

Author's biography

James K Murashige is responsible for new product planning and application at Logic Devices Inc (Sunnyvale, CA). As such, he is involved in the development of high-speed DSP logic circuits, static RAMs, and SCSI controllers. James holds a BSEE degree from Johns Hopkins University (Baltimore, MD). In his off hours, he enjoys bicycling, hiking, gardening, and woodworking.

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		FAX: (303) 469-8585
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Deltatronics	Blue Bell, PA	(215) 641-9930
		FAX: (215) 641-9934
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Dyne-A-Mark	Clearwater, FL	(813) 441-4702
		FAX: (813) 447-4120
	Ft. Lauderdale, FL	(305) 771-6501
		FAX: (305) 772-0114
	Casselberry, FL	(407) 831-2822
		FAX: (407) 834-4524
	Palm Bay, FL	(407) 725-7470
		FAX: (407) 984-2719
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Electramark	Norcross, GA	(404) 446-7915
		FAX: (404) 263-6389
IDAHO		
Western Technical Sales		
	Spokane, WA	(509) 922-7600
		FAX: (509) 922-7603
ILLINOIS		
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		FAX: (312) 310-8844
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Applied Data Management		
	Batesville, IN	(513) 579-8108
		FAX: (513) 579-8510
IOWA		
Cahill, Schmitz & Howe		
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		FAX: (319) 377-0958
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Applied Data Management		
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		FAX: (513) 579-8510
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Comptech	Irving, TX	(214) 751-1181
		FAX: (214) 550-8113
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		FAX: (617) 272-2467
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Aldridge Assoc. Inc.	Eden Prairie, MN	(612) 944-8433
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NEW JERSEY (South)		
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		FAX: (505) 883-9044

North American Sales Representatives

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NEW YORK (Upstate)		
Labtronics	Syracuse, NY	(315) 455-7314
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NORTH DAKOTA		
Aldridge Assoc. Inc.	Eden Prairie, MN	(612) 944-8433
		FAX: (612) 944-8378
OHIO		
Applied Data Management		
	Cincinnati, OH	(513) 579-8108
		FAX: (513) 579-8510
OKLAHOMA		
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Western Technical Sales		
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		FAX: (503) 644-8200
PENNSYLVANIA (Eastern)		
Deltatronics	Blue Bell, PA	(215) 641-9930
		FAX: (215) 641-9934
PENNSYLVANIA (Western)		
Applied Data Management		
	Cincinnati, OH	(513) 579-8108
		FAX: (513) 579-8510
PUERTO RICO		
A/D Nova Sales	Burlington, MA	(617) 270-9600
		FAX: (617) 272-2467
RHODE ISLAND		
A/D Nova Sales	Burlington, MA	(617) 270-9600
		FAX: (617) 272-2467

Company	City/State	Telephone
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Blue Ridge Sales	Raleigh, NC	(919) 790-8094
		FAX: (919) 872-8851
SOUTH DAKOTA		
Aldridge Assoc. Inc.	Eden Prairie, MN	(612) 944-8433
		FAX: (612) 944-8378
TENNESSEE		
Electramark	Norcross, GA	(404) 446-7915
		FAX: (404) 263-6389
TEXAS		
Comptech	Irving, TX	(214) 751-1181
		FAX: (214) 550-8113
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	Houston, TX	(713) 492-0005
		FAX: (713) 492-6116
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Western Region Marketing		
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VERMONT		
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Advanced Technology Sales		
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